POLITECNICO DI TORINO

Corso di Laurea in Electronic Engineering

Master Thesis

Hyper-scanning EEG Platform

POLITECNICO
DI TORINO

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I wish to acknowledge the support of my family, Rocco, Davide, Emanuele, Cora, my friends and of all those that have been so crazy to believe in me. As my unique girlfriend, Virginia, daily does.

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You'll always walk with me.

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1. Abstract

Hyperscanning is a method thanks to which two or more subjects can mutually interact while their brains are simultaneously scanned by means of multiple, simultaneous EEG, allowing the study of the brain responses that determine important social interactions. The types of interactions that can be studied are diverse, ranging from competitive games, to cooperative tasks or musical performances. (Astolfi, et al., 2011)

The objective of this thesis was to design and build a low-cost, open-source, wireless platform for multi-nodal time-synchronized EEG recording (hyperscanning): the time-synchronization has been achieved via the network clock from a Wi-Fi network.

The system is composed by different devices interconnected, both hardware and software. A Raspberry Pi 3 was used as "central computer" for data collection and transmission, data coming from a custom designed Raspberry Pi 3 shield board: this printed circuit board gives the possibility to connect and monitor up to 8 simultaneous EEG channels. Another peculiarity of the system is the usage of custom-made in ear-EEG electrodes from the Lab, which allowed more portability in exchange of a reduced signal amplitude and less monitored brain regions.

Some of the tasks achieved were based on and inspired by open-source work available on the Web.

The experience stretched from many fields such as hardware and software design for an embedded and biomedical system, allowing a personal growth in independently managing a whole digital system design project and related problems solving. Unfortunately, a malfunction in the ADC conversion made us obtain weak results preventing to achieve the goal to perform a hyper-scanning auditory evoked potential experiment with real EEG data streams. Anyway, simulated data could be perfectly sent via wireless for a real-time visualization on MATLAB, meaning that after refining the ADC behaviour, reasonable performances could likely be reached.

The whole project has been evaluated as feasible and worth the work on it, being a possible, valid starting point for future progressions on EEG hyper-scanning from a very solid level.

2. Introduction

2.1. Neuro Tech Lab

This master thesis experience occurred in Aarhus, the second largest city in Denmark, at the NeuroTechnology Lab of Aarhus University who hosted me as a guest student.
The NeuroTechnology Lab (Neuro Technology Laboratory, s.d.) is a research laboratory running several cross projects and activities related to the human nervous system. This includes measuring on and modelling of the nervous system, innovating and engineering novel interfacing technologies, applying advanced signal processing and machine learning methods for electrophysiological signals primarily from the central and peripheral nervous system, and facilitate experimental research within this field. The Laboratory is headed by Senior Associate Professor Preben Kidmose, my host professor and point of reference.

The purpose of the lab is to facilitate applied and experimental research within technologies for interfacing to the human nervous system. In particular there is a focus on wearable systems that are feasible for recording over long periods of time and with integration with other sensor modalities.

Technologies researched covers medical, neuroscience, professional and consumer applications. Within the medical area the technologies can be applied for diagnosing and monitoring of diseases, for assistive devices used in rehabilitation, and for management and monitoring of chronical diseases. Technologies for monitoring of mental, physiological or psychological states in natural environments and over long periods of time is a long standing imperative within neuroscience. Fatigue monitoring and estimation of attention or working memory capacity are of high relevance in many professional applications. And finally, sleep monitoring, estimation of affective states or cognitive training through neuro-feedback are examples of possible future consumer applications.

2.2. Hyperscanning method background

Hyperscanning (or hyper-scanning) (Montague, Berns, Cohen, & Others, 2001) is a method by which multiple subjects can interact with one another while their brains are simultaneously scanned. (Babiloni & Astolfi, 2012): it is called (RB & I, 1968).

One of the most relevant traits of the sociality is given by the cooperative behaviour, in fact through cooperation we can reach goals that we could not achieve as individuals.

The simultaneous measuring of different brains' activity through electroencephalography (EEG) recording from people interacting in cooperative or competitive games, allows us to study the physiology of the group. (Koike, Tanabe, & Sadato, 2014)

In recent years powerful brain-scanning techniques such as fMRI (functional Magnetic Resonance Imaging) and HR-EEG(high resolution EEG) allowed us to begin studies in the field, recording brain activity in different subjects during the performing of an identical sensory, cognitive or motor task. But those studies were limited by the impossibility to monitor neural activity for more than one attendee in real-time, so neural activity in the brains of a group could only be conjectured. This is due to the fact that direct brain interactions couldn't be really analyzed with models and assumptions, nor generalizations, being that performing the same task doesn't necessarily mean the same neuronal response for different subjects, and thus the use of the same neuronal patterns.

With the hyperscanning is introduced the possibility to have a multi-nodal functional monitoring of neuronal activity allowing us to have a real-time "social interaction analysis" (Zhang). It can be performed with fMRI, EEG or MEG (magnetoencephalography).

Neuro Tech Lab is specialized in EEG studies, therefore this thesis will focus on a project whose aim is to create precisely a low-cost, portable EEG platform. In the end, it is important to underline that these studies are just at their dawn, hiding a huge potential in many fields.

Figure 1 – EEG hyperscanning setup during a card game

3. State of the art

Let's go a little bit further in the hyperscanning background.
The field of neuroscience has only started to investigate brain activity during social interactions in the last decades.

In recent years, neuroscientists have started to investigate the cerebral structures supporting the processes involved in the social cognition abilities of humans, starting with experimental evidence drawn from brain lesion studies and autism.
From many studies social cognition (Overwalle & Baetens, 2009) appears that specific cerebral regions are involved in tasks that require the processing of information relevant for social cognition. In particular, the temporo-parietal junction (TPJ) was described as being consistently activated during tasks involving the short-time estimate of intentions, desires and goals related to other people.

Neuroscientist Read Montague of Virginia Polytechnic Institute and State University (the father of the "hyperscanning" term), spent many years forming a team with the aim of studying this method possibilities, by scanning two (or more) subjects using fMRI or EEG devices during social interactions such as basic games.

With the aid of web-based computational power more complex tests could be conducted, with a crescendo of relevance and depth approaching the essence of how human social interactions work and collecting data could be a first step to better understand ourselves as a social being. The possibilities and advantages of such knowledges, shared through the web with neuroscience researchers, are beyond words and thought.

4. Project overview

4.1. System specifications

The project was born with the intent of developing a low-cost, multi-nodal, open-source EEG system able to transmit data of 8 input channels in real-time over a Wi-Fi hotspot, with the final aim to perform hyper-scanning EEG experiments obtaining a valid research platform for the simultaneous analysis of the evoked potential in multiple subjects, with sociological and behavioural studies purposes.

Evoked potentials (also called evoked response) are the electrical signals to the brain generated by the nervous system exposed to a stimulus, usually coming from senses such as hearing, touch, or sight. These signals are very weak, staying in the range from 1nV to 10nV, often in a noisy environment (10mV and more).

Being that there are not low-cost hyperscanning platforms available on the market, this project gains more relevance. EEG data recorded is transferred to a MATLAB script where a graphical representation is allowed for the incoming real-time stream of data.

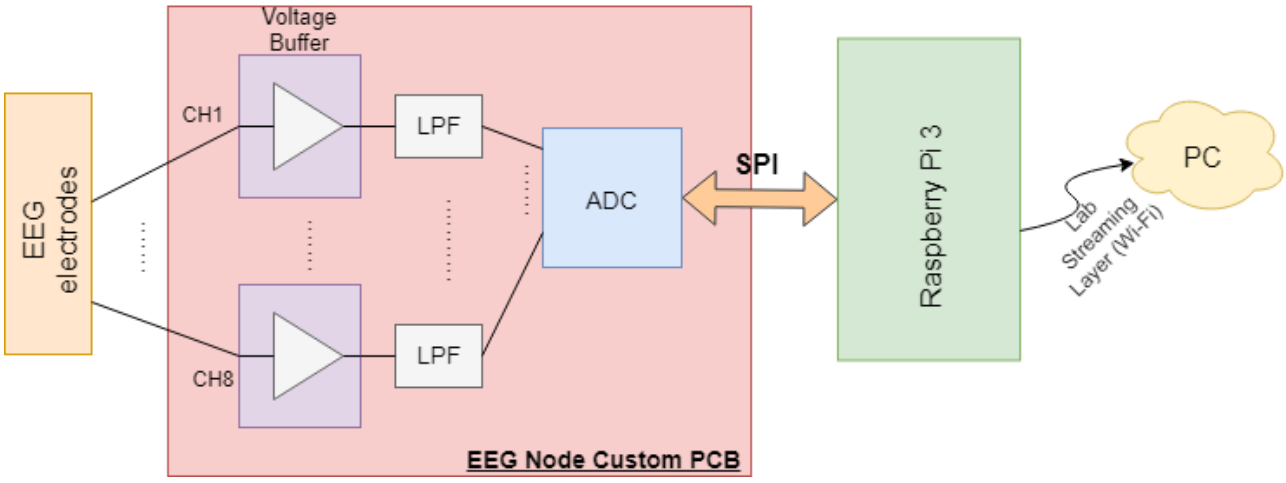

Figure 2 - EEG Node custom PCB and its connections block diagram

The hardware system was intended to consist in different parts as the above block diagram shows.

The 8 EEG channels are connected through peculiar coaxial cables to the EEG node PCB, where every single signal is channelled in voltage buffers in order to avoid source to be affected by load currents.
The signals are filtered across a precaution low pass filter before entering the ADC, where they're converted and then sent through a Serial Peripheral Interface to the Raspberry Pi 3 microcontroller.
As a final step the EEG waveforms are transmitted through Wi-Fi to a terminal, where they can be analyzed in real-time and easily processed with MATLAB and other tools.

In order to obtain good results in terms of general performances, noise immunity and other useful parameters, the supervisor suggested to respect the maximum number of the following specifications, choosing hardware components accordingly.

- *Critical specifications:*
  - Highest CMRR possible: $\mathrm{CMRR} \leq -120\ \mathrm{dB}$.
  - High input impedance: $\mathrm{Zin} \geq 10\ G\Omega$.
  - ADC resolution: $M \geq 16\ bit$.
  - Noise reduction: for shielding and guarding purposes.
  - $\Delta Zload\ /\ \Delta Zin$ shall be the smaller possible and similar for the sensors.
  - Channels: 8 EEG channels desired (4 left + 4 right).
  - ADC Bandwidth: the ADC needs to be able to cope with 0.1Hz-100Hz bandwidth.

4.2. System architecture

4.2.1. Features

The chosen electronic design automation (EDA) application for schematic capture, printed circuit board (PCB) layout, place and route and computer-aided manufacturing (CAM) was EAGLE© for many reasons: it is simple, open-source, with a big dedicated community, flexible and has a free student license which covers without doubt most needs, including multilayer design.

The PCB designed was meant to be the EEG Node for analog signals conversions to digital and their transmission to a terminal computer, where data would have been processed.

It was decided to design it on four layers, having a similar manufacturing cost of a 2-layer PCB and allowing an easier place and route. As for the schematic, also for the PCB design it was decided to immediately sketch some main traits in order to cope with our necessities. The board was designed to respect the Raspberry Pi 3 dimensions, 57mm x 86 mm, in order to make it a plug-in shield, making the system more compact, portable and single supplied, with a couple of 3.7V batteries, guaranteeing around 10 hours of use. After several checks the board was printed in Belgium by Eurocircuits and obtained for soldering in around a week.

The board has a protection circuit from potential power supply excess voltages.

Moreover, a Driven Right Leg (DRL) (MettingVanRijn, Peper, & Grimbergen) circuit has been added to avoid common-mode interference, but this will be discussed further in the next chapters.

4.2.2. Complete system block diagram

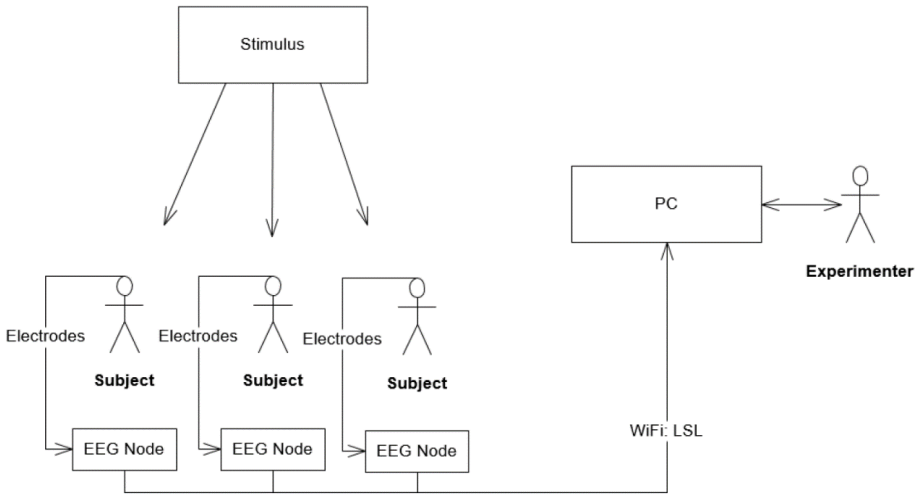

Figure 3 - The complete system block diagram

The final goal of this thesis was to create an easy-to-use, low cost EEG platform for neuroscience studies in multiple brains monitoring during social cooperation (hyper-scanning). To achieve this a multiple channel analog-to-digital converter was either necessary and crucial: every subject under analysis (up to four people in our case, 8 channels divided by two) is connected to the electroencephalographic node, based on the

Raspberry Pi 3 attached to the custom shield board, from which the collected digital data is sent via WiFi to a main computer, where data is processed by MATLAB.

For a better understanding, main devices and tools used are described in next chapter.

4.3. Project management

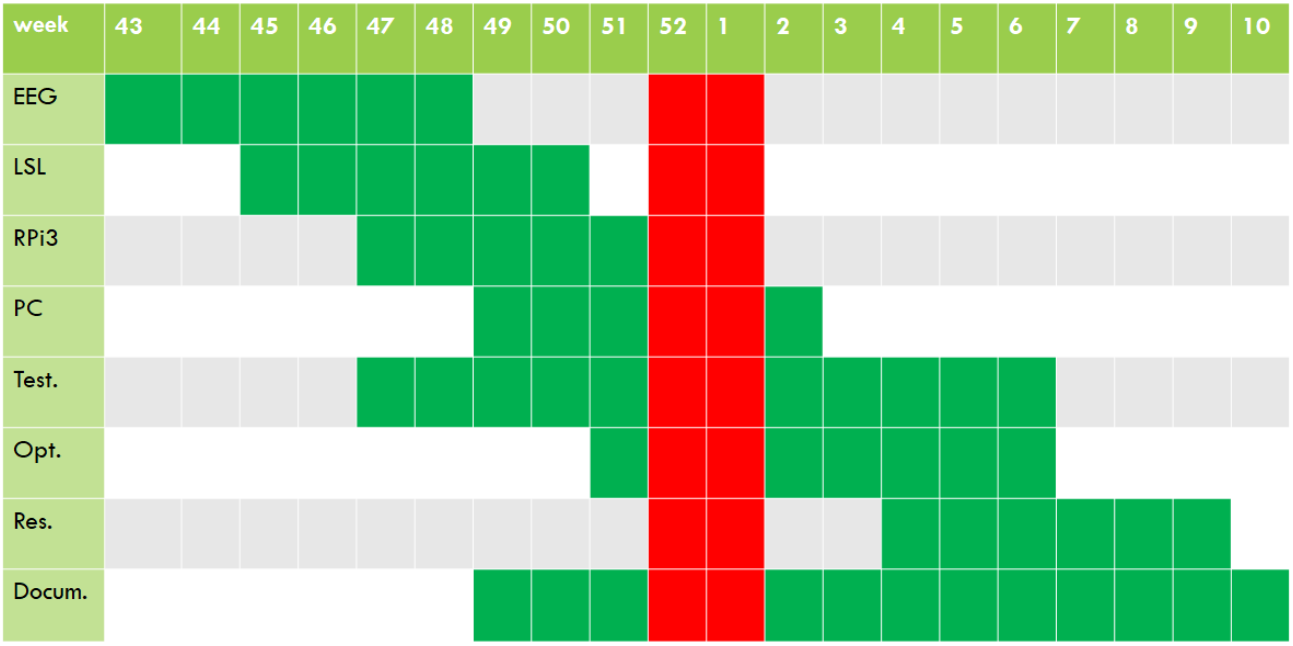

Figure 4 - Gantt diagram of the workload

Being guest in a foreign university also meant a good organization in terms of load of work and corresponding scheduling. With the help of professor Kidmose a temporary initial time schedule was established as follows in Figure 3.

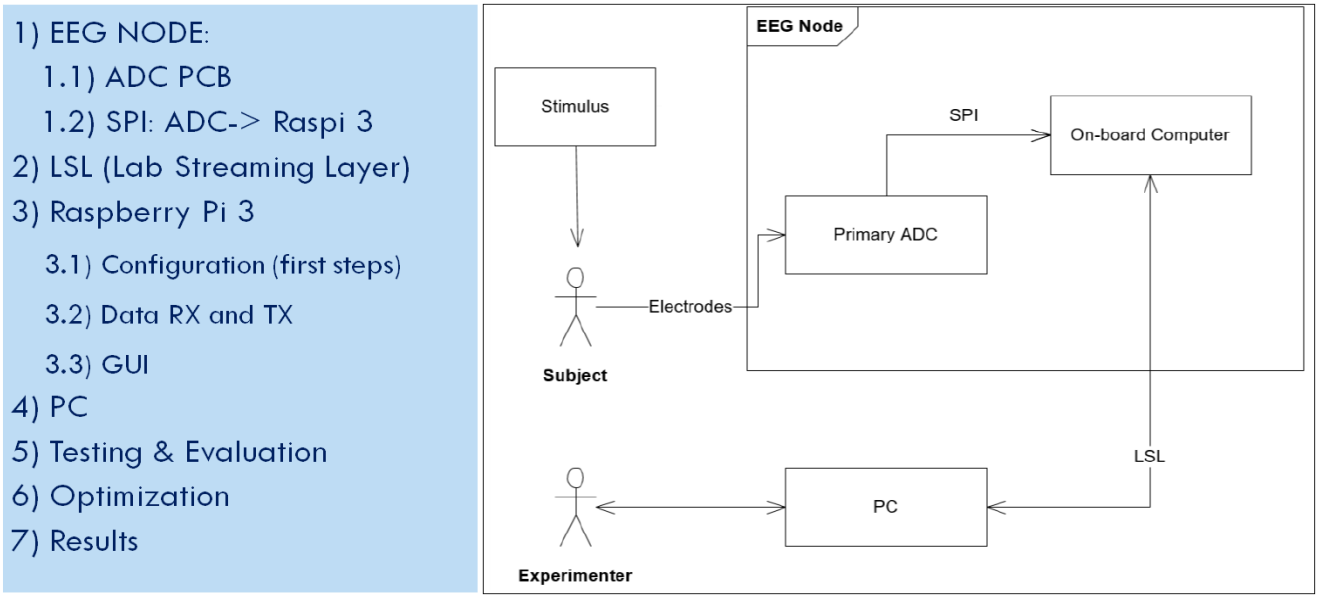

Figure 5 – Scheme of the system as it was conceived with a step by step schedule (on the left)

The thesis experience was controlled and directed by having weekly meetings in the form of a PowerPoint presentation to show the supervisor the progresses.

The schedule in the diagram form wasn't adjourned in the following months, but every step and objective had a flexible but still indicative expiration date to avoid time wasting in order to switch to another topic in a block situation.

The first proposed working outline has turned out to be a valid schedule, so the graph that follows represents the list of steps faced along the thesis period.

Let's analyze the outline in Figure 2. First of all, the so called "EEG Node" was designed, creating the desired Raspberry Pi 3-shaped shield board.

It was then thought a method for the correct management of the Serial Peripheral Interface communication, analogously to the second step, the "Lab Streaming Layer".

The following stages were to study and analyze both the Lab Streaming Layer toolkit and the Raspberry Pi 3 capabilities, trying to establish a Wi-Fi communication between the PC and the on-board computer (the Raspberry itself), starting from existing scripts and apps.

Validated the correct transmission and receiving of data from the Raspberry through a simulation, the board components were mounted and many electrical circuit tests were made to validate the correctness of the board.

Therefore, the whole system was tested by applying known, low frequency and low amplitude signals, to check the correct work of the analog-to-digital converter.
In the meanwhile it was also considered the creation of an ad-hoc Graphical User Interface (GUI) to make the whole system more user-friendly and to easily choose how to make the acquisition work for an easier testing.

4.4. Raspberry Pi

The Raspberry Pi is a credit card sized single-board computer that costs around 25£, designed for basic computer science teaching purposes by the British Raspberry Pi Foundation, becoming very popular also outside its target market for uses such as robotics or IoT.

The model we employed, the Raspberry Pi 3 (Foundation, s.d.) Model B, was released in February 2016 with a 1.2Ghz, 64-bit quad core processor, and has on-board Wi-Fi, Bluetooth, Ethernet, HDMI, SD card ports and multiple USB ports with boot capabilities.

The operating system decided to be employed on it was Raspbian. Raspbian is a distribution of Debian specifically optimized for the Raspberry Pi line of single-board computers. It is provided by the Raspberry Pi Foundation.

4.5. ADS1299 analog-to-digital converter

The shield board cornerstone was the analog-to-digital converter ADS1299 from Texas Instruments. The ADS1299 is a eight-channel, low-noise, 24-bit, simultaneous-sampling delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) with a built-in programmable gain amplifier (PGA), internal reference, and an onboard oscillator. It includes all commonly required features for extracranial electroencephalogram (EEG) and electrocardiography (ECG) applications for devices reduced in size, power and overall cost.

The ADS1299-x family operates at data rates from 250 SPS to 16 kSPS (samples per second). It has a input multiplexer per channel that can be independently connected to inner-generated signals for test, temperature and lead-off detection.

Dually, any input channel configuration can be selected for derivation of the patient bias output signal. Optional Stimulus-Reference-Bias (SRB) pins are available to route a common signal to multiple inputs for a referential montage configuration.

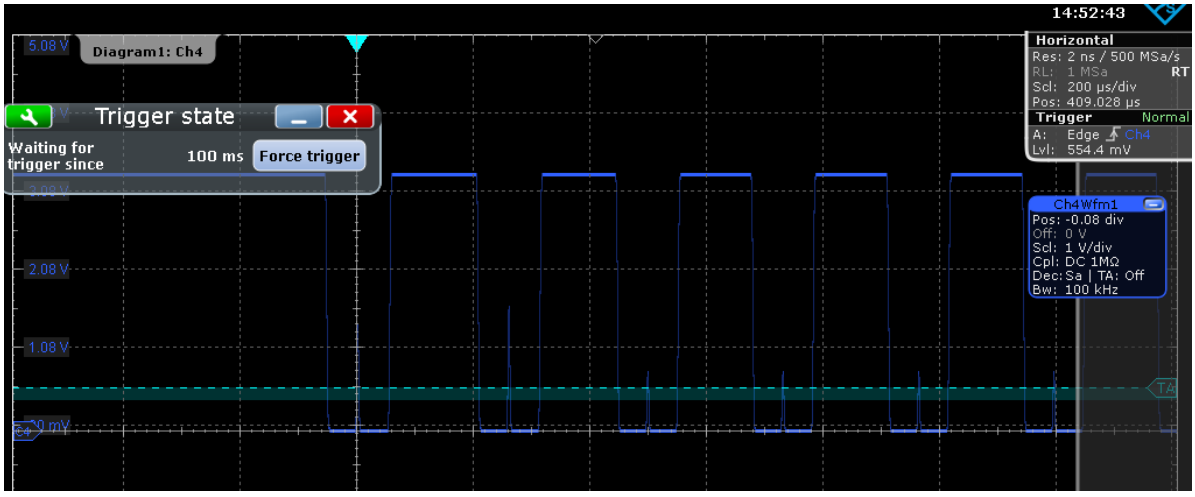

Figure 6 – CS signal going low each time a read is done

4.6. Lab Streaming Layer

The lab streaming layer (LSL) is a system designed at the Swartz Center for Computational Neuroscience, UCSD, a work funded by the Army Research Laboratory, for the unified collection of measurement time series in research experiments able to handle the networking, time-synchronization, real-time access as well as the centralized collection, viewing and recording of the data. (Kothe, s.d.)

The Lab Streaming Layer distribution is built of a core general-purpose library (named "liblsl") and its language interfaces (C, C++, Python, Java, C#, MATLAB). It is a cross-platform, supporting Windows/Linux/MacOS, 32/64 bit.

In conjunction with it there is a suite of tools built, including recording programs, online viewers, importers and data-acquisition apps for different hardware available on the lab network (for example audio, EEG, or motion capture).

4.7. Serial Peripheral Interface

Serial Peripheral Interface (SPI) is a highly common communication protocol used for two-way communication between two devices at a time. A standard SPI bus consists of four signals, Master Out Slave In (MOSI), Master In Slave Out (MISO), the Slave Select (SS) and the the serial clock (SCK). SPI is not symmetric as a bus has one master, able to talk to any slave and one or more slaves, which can only talk to the master. Each slave on the bus must have its own unique slave select signal, used by the master to select which slave it will be talking to. The SS signal is low active and where it is, the master is free to start sending data. SPI transfer is full-duplex, meaning that data is sent from the master to the slave and from the slave to the master at the same time. In case the master makes a transfer, device(s) will send dummy bytes (usually all 1's or all 0's) when communication should be one way. Dually, if the master it is reading data in for a slave, the slave knows to ignore the data received by the master.

5. System design

5.1. HW design

5.1.1. Schematic

5.1.1.1. Schematic overview

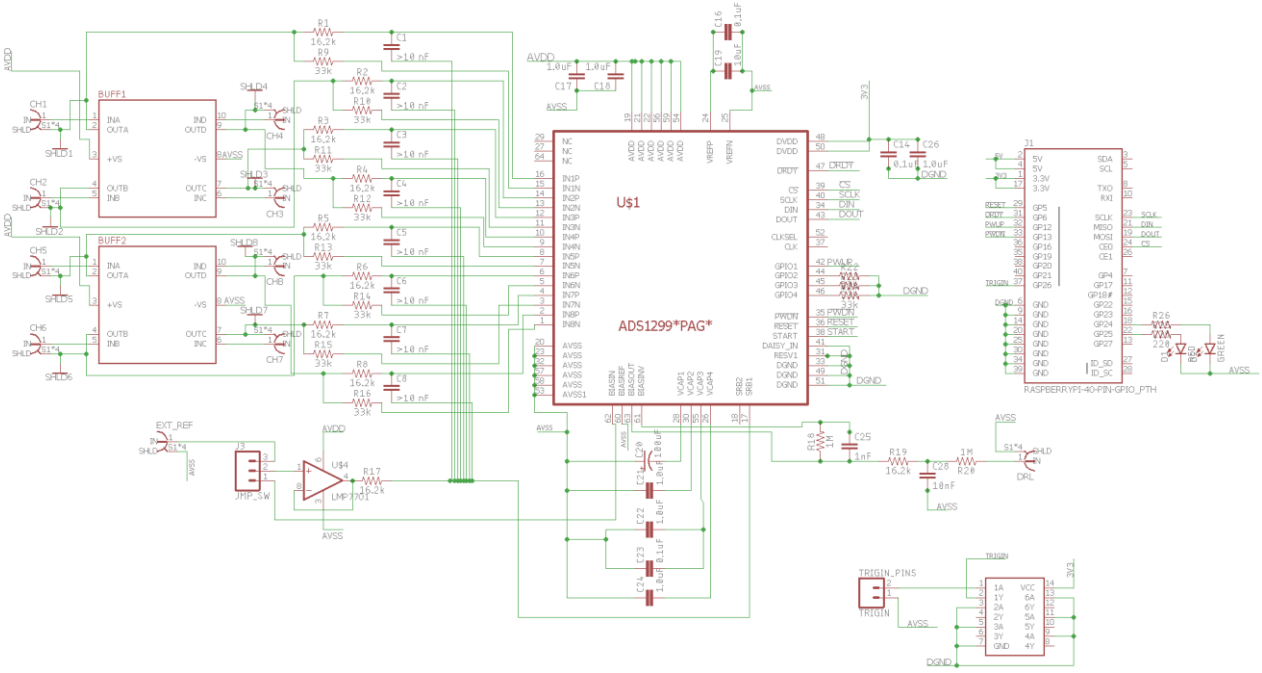

Figure 7 - Complete schematic of the EEG Node PCB except the Power Supply Unit

The EEG Node PCB purposes have been roughly described in chapter 4.2, whereas in this one we go further in detail behind every choice.

As it should be clear from the above schematic screenshot from EAGLE schematic entry EDA, the circuit has been designed in a methodical way dividing the analog circuitry, on the left, and the digital one, on the right.

For an easier understanding the circuit is split and illustrated in its principal parts: the power supply unit, the input circuitry, the analog-to-digital converter and the Raspberry Pi interface; they are described in the following sub-chapters.

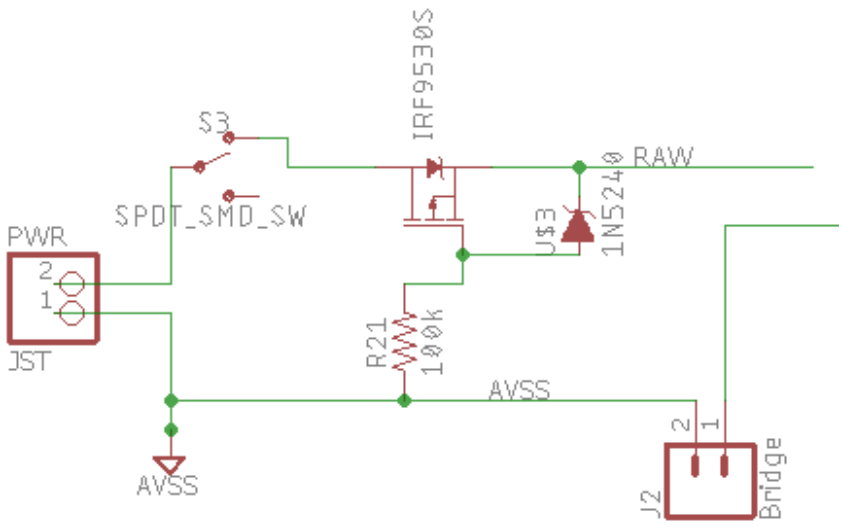

Figure 8 - First part of the PSU

5.1.1.2. Power supply unit

The power supply unit is a critical subject: the aim is to both optimize it and protect the circuit.

The whole system is intended to work supplied by 7.4 V obtained by putting in series two 3.7 V Li-ion batteries in series and regulating thus the resulting 7.4 V down to 5 V. The raw voltage needed then to be regulated to two different 5V sources, a more accurate one for the analog supply and a less precise one for the digital supply.

However, let's first analyze the figure above (Fig. 2), which represents the initial part of the power supply unit.

The ground and power cables are connected to a JST connector: the power source passes through a single-pole double-pole (SPDT) switch and a small reverse polarity protection circuit based on the p-channel MOSFET IRF9530S, the 100kΩ resistor and the 1N5240 Zener diode.

This protects the circuit from accidental reversed current, shutting off the MOS in this unwanted case.

Focusing now on the second part of the circuit. In Fig. 3 it can be noticed that the raw 7.4 V power source (called RAW) is split for the two different needed supply lines, both at 5 V but with different noise immunity.

The analog supply requirements are indeed stability and noiselessness and in order to assure these, the regulator chosen is a Low Drop-Out (or LDO) one, a peculiar low-noise, low-dropout voltage, linear voltage regulator, the LT1763 by Linear Technology. The main key feature of the LT1763 regulator family is in general the low output noise, a critical aspect, working with so low voltages such as the EEG signals.

The capacitors chosen are used for decoupling, suggested by the datasheet (for both voltage regulators).

As regards the digital supply, no need of precision and noise reduction bring to the choice of a traditional and well-known linear voltage regulator, the L7805 by STMicroelectronics, with a tolerance of 2% on the output voltage.

As it can be seen from the picture below (Fig. 3), the ground is double: analog and digital grounds, but reason and details will be treated in chapter “5.1.2.1. Power supply unit”.

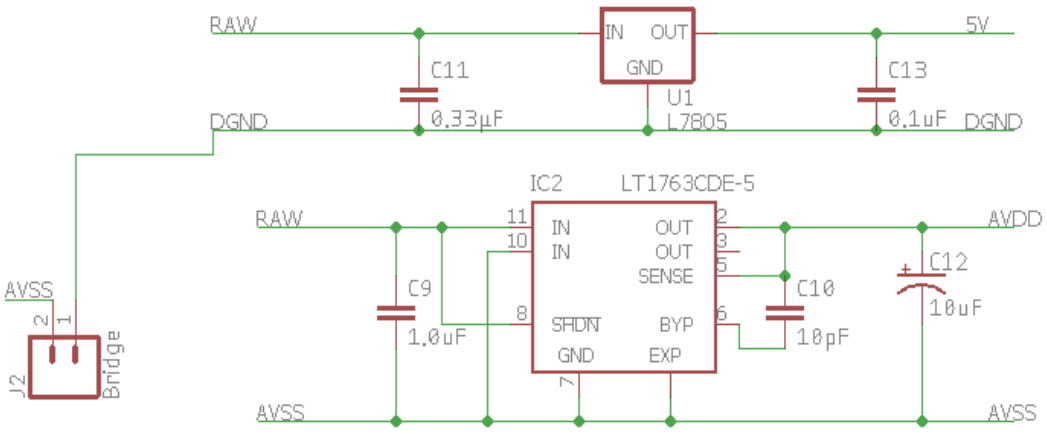

Figure 9 - Second part of the PSU

5.1.1.3. Electrodes input circuitry

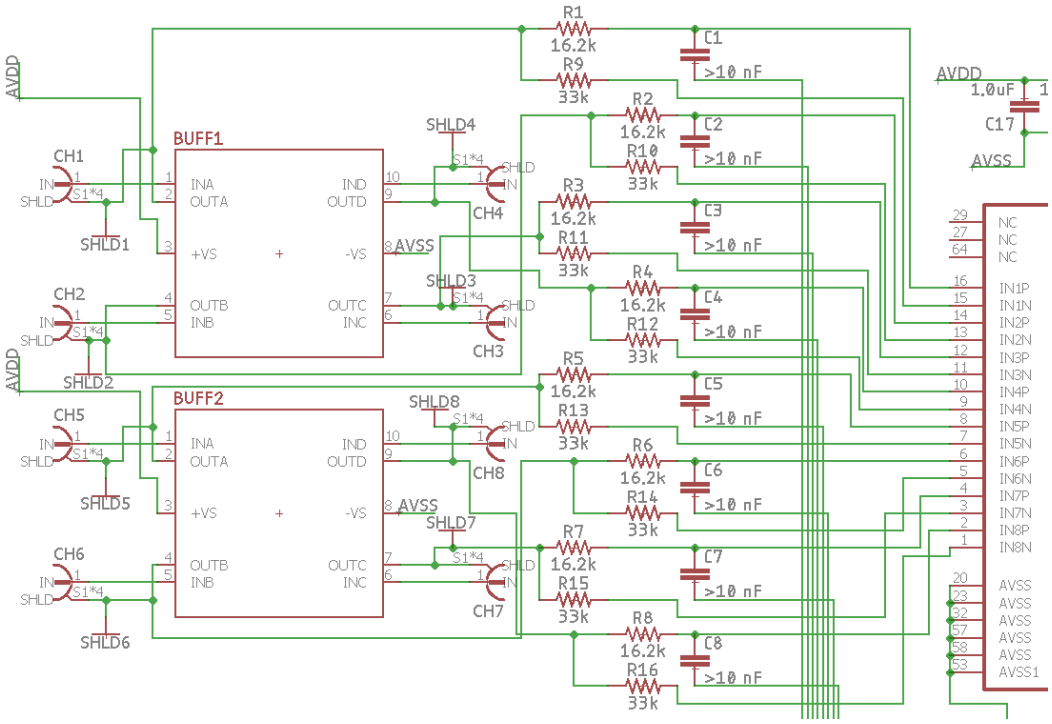

Figure 10 - Electrodes input circuitry

As already told in previous chapters, the system is designed to work with EEG signals, feeble, low frequency (3-15Hz, changing depending on the type of EEG wave: delta, beta, alpha, teta)

The inputs are driven through particular coaxial cables, EPL.00.250.NTN from LEMO granting a high noise immunity.

The eight incoming signals are routed in two buffers, four signals each.

The precision, low power, quad unity-gain buffer chosen is the AD8244, excellent to isolate the input analog impedances, allowing almost zero current noise (2 pA maximum), being thus suitable for biopotential electrodes and medical applications.

The very high input 10 TΩ impedance assures that the electrodes signals are not affected from the voltage divider:

$$V_{sig} = V_{in} \,.\, Z_{in}/(Z_{in} + Z_s)$$

Where Z_s is the small impedance between the electrodes and the buffer. Moreover, other critical specifications are a high analog-to-digital converter input impedance (10 TΩ in our case) and a consequent high CMRR, -120dB in our case.

Every buffer has four outputs that are splitted in two: a first branch passes through a differential low-pass filter, feeding then the ADC positive input pin. The second branch, instead, is routed out of the ADS1299 from BIAS_IN pin into an averaging amplifier: the average of the ADC negative inputs is thus fed back into the ADS1299 through SRB1 to the common differential reference voltage inside the converter itself.

5.1.1.4. ADS1299 analog-to-digital converter

The whole EEG Node PCB has its core in the analog-to-digital converter, a device with the purpose of canalising the EEG evoked potentials sensed, thus converting them into digital in order to easily monitor and re-elaborate data to have an analytical evaluation. To respect the critical specifications, which are all related to the converter, an accurate search of the correct device brought to choose the ADS1299, a 24-bit, 8-channel delta-sigma (ΔΣ) ADC. It operates at data rates from 250 SPS (samples per second) to 16 kSPS, it has an integrated programmable gain amplifier (PGA) and a CMRR equal to -110 dB, which fits almost perfectly our necessities.

ADS1299 1GΩ input impedance does not fulfill the requirement of 10GΩ, but the buffers abundantly compensates for it.

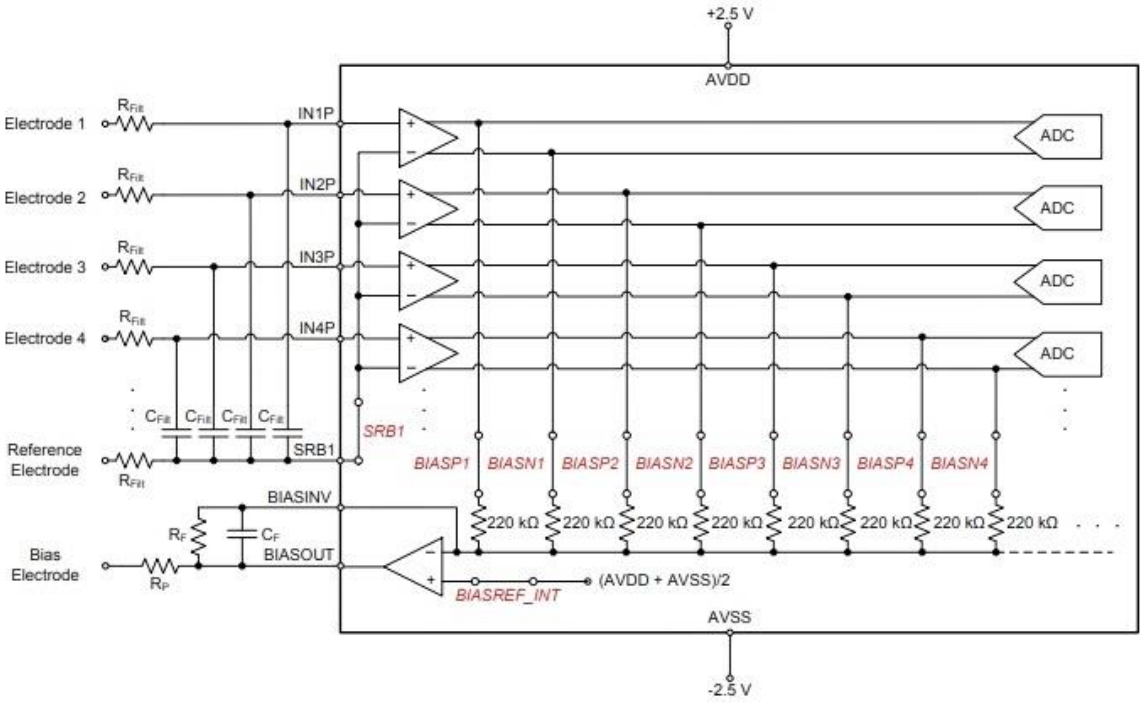

Figure 11 - Schematic of the ADC in an EEG data acquisition application, referential montage

This device is mainly suited for many medical applications, such as extracranial EEG and ECG studies in addition to sleep study monitor and Evoked Audio Potential (EAP), keeping a low cost and low power solution.

Many input configurations are possible, having a flexible input multiplexer per channel. The one chosen for this project is the Referential Montage (Figure 5): as already mentioned in chapter 5.1.1.3, while the ADS1299 positive inputs are directly connected to the internal delta-sigma converters, the negative ones are combined together into an averaging amplifier after exiting the ADS1299 through BIAS_IN pin. Such amplifier feeds the delta-sigma converters with an average value between the negative inputs (see chapter 5.1.2.3 for more details).

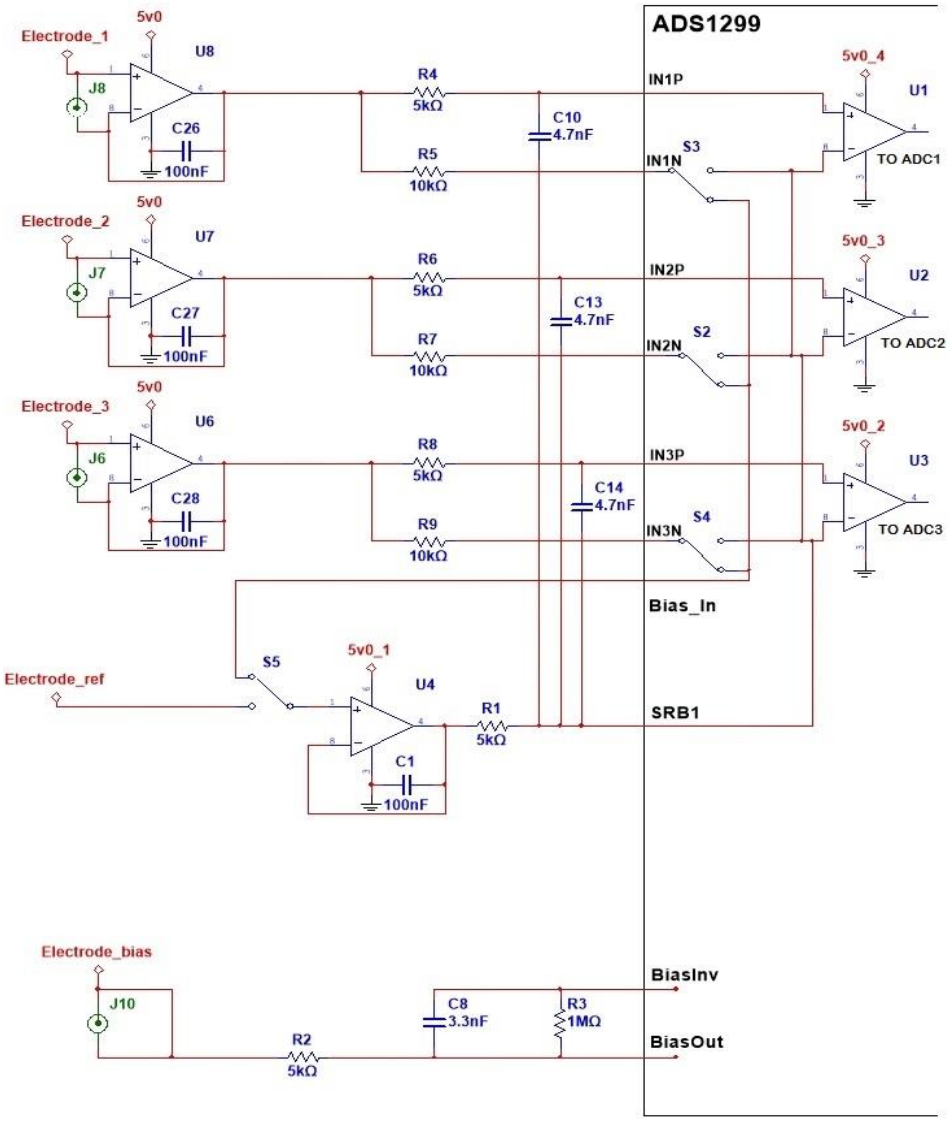

Figure 12 – This project ADC referential montage configuration

The main difference between the exemplified referential montage and this project's one lays in the fact that our reference voltage can be chosen, by means of an adjustable SPDT (single pole double throw) switch, between an external source or the average of all negative inputs, while just the first option is possible in the example in Figure 5.
Another detail of the input circuitry is the electrode bias (see Figure 6), used to reduce common-mode interference. This signal is brought to the patient to compensate the fact that the human body can act as an antenna, thus catalysing electromagnetic noise, which can possibly eclipse the brain activity we want to monitor.
This expedient can be associated to the Driven Right Leg (DRL) circuit, a noise removal method to improve common-mode rejection by feeding the common-mode signal back to the patient's body in a closed loop.
Obviously, in order to obtain this whole configuration, the ADS1299 has to be specifically programmed.

5.1.1.5. Raspberry Pi 3 interface

As already mentioned, the custom EEG Node PCB is designed to perfectly fit the Raspberry Pi 3 as a shield through a 40-pin header.

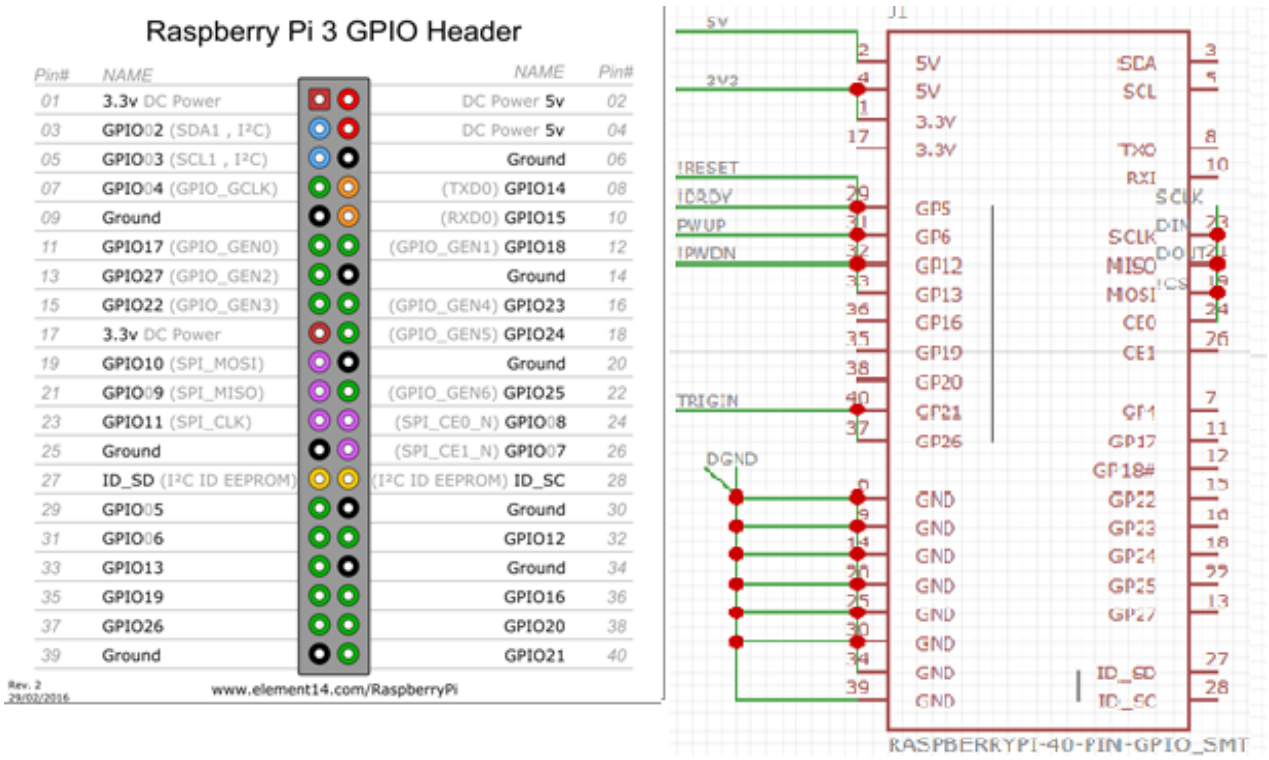

Figure 13 – Raspberry Pi 3 header pinout (left) and 40-pin GPIO header on PCB (right)

Since we want to wedge the Raspberry in our PCB, this last is designed as a 86.5mm x 57.5mm rectangle, against the 85mm x 56mm of the Raspberry.

By the way, a mistake in the design brought to have MISO and MOSI pins (SPI input and output) inverted, but the connection between the devices resulted possible by means of a modified 40-pin ribbon cable.

As regards the unused pins, they are just unconnected on the PCB.

5.1.2. PCB layout: considerations and design

5.1.2.1. PCB layout overview

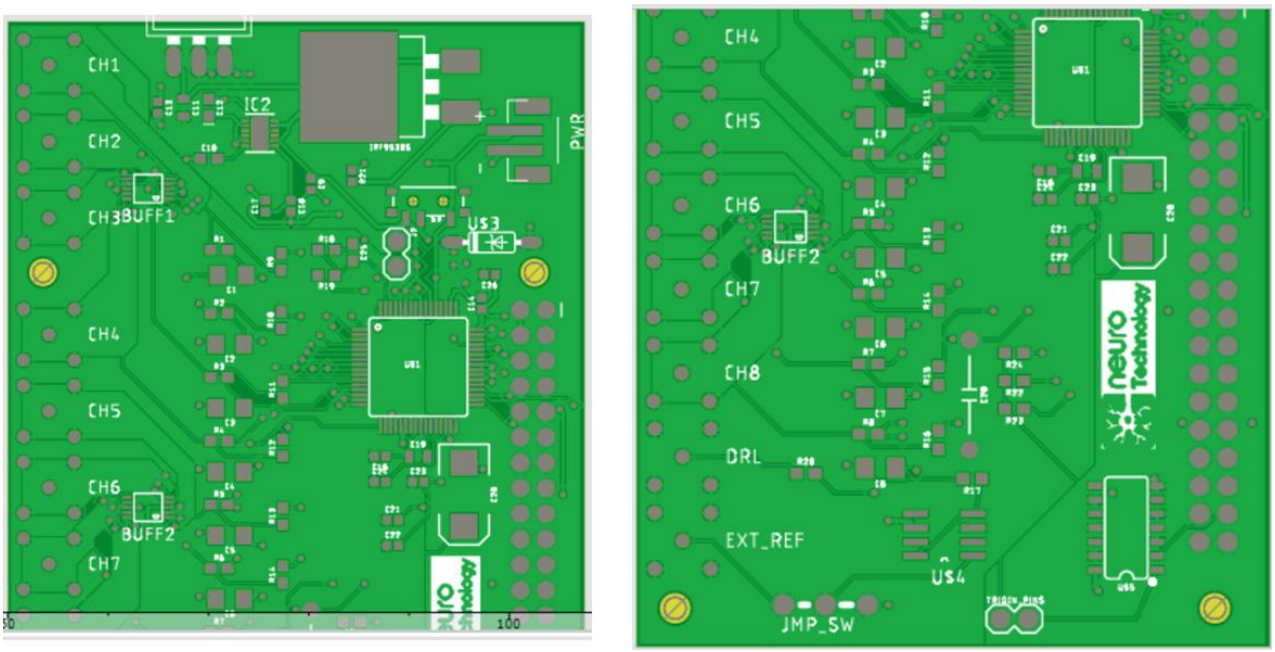

Figure 14 –Realistic top view of the PCB (divided into two, upper part is on the left)

While in the previous subchapter it has been depicted the circuital schematic, in this one is treated the printed circuit board (PCB) layout design.

EAGLE is always the chosen Electronic Design Automation (EDA) tool to accomplish the Place and Route stage.

The design of the PCB was cautiously planned in many details. First of all, its dimensions are almost identical to the Raspberry Pi 3, as already exposed, but a most important decision has been to design it on four layers, instead of the initial idea of using just two, also because of the negligible cost increment.

This is an optimal choice: in fact, having four layers available allows to avoid crowding traces and to isolate parts of the circuit on different layers. This lead to advantages in terms of performance and tidiness, especially during Place and Route.

The four layers have the same thickness (check Fig. 11) and are the following:

1) Top layer: on this layer are placed most beginning of main traces that then dive into lower layers. As it can be seen in Figure 9 (on the left) there are some mixed signals, but mostly short analog traces.
2) Route 2 layer: its traces are mostly ADS1299 input connections.
3) Route 15 layer: contains mixed analog and digital remaining traces.
4) Bottom layer: ground plane and Raspberry header footprint lay in it.

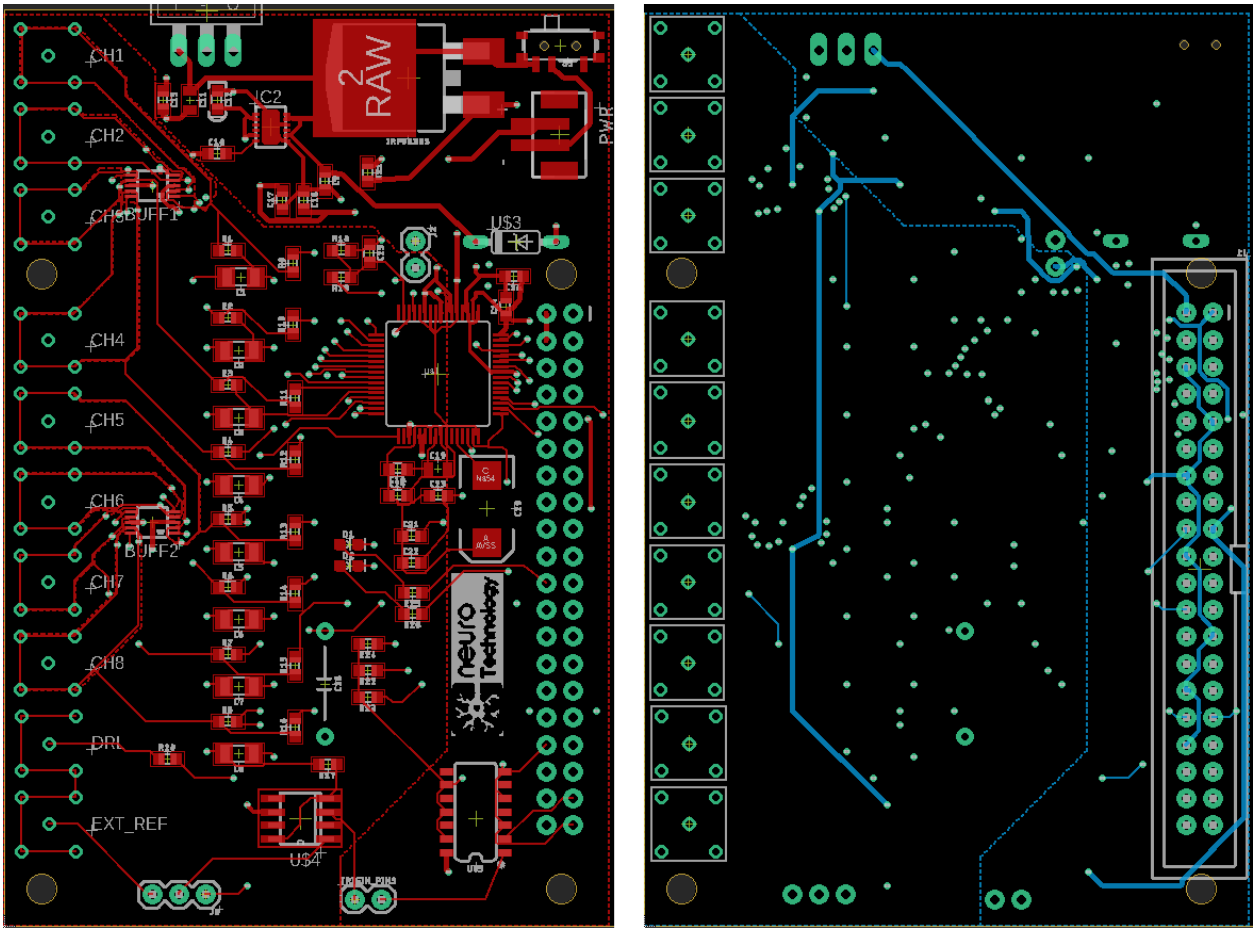

Figure 15 – Bottom (right) and Top (left) layers view

The necessity of isolating certain signals or circuitry on a single layer or part of it is fully satisfied with this place and route, also thanks to the abundance of vias on the board (the small green circles in the figure 9 and 10).

It can be seen the silkscreen logo of the Neuro Technology Lab added below the ADS1299, put in the central-right part of the PCB.

The dashed line divides the analog and the digital part of the circuit, respectively on the left and right side of it.

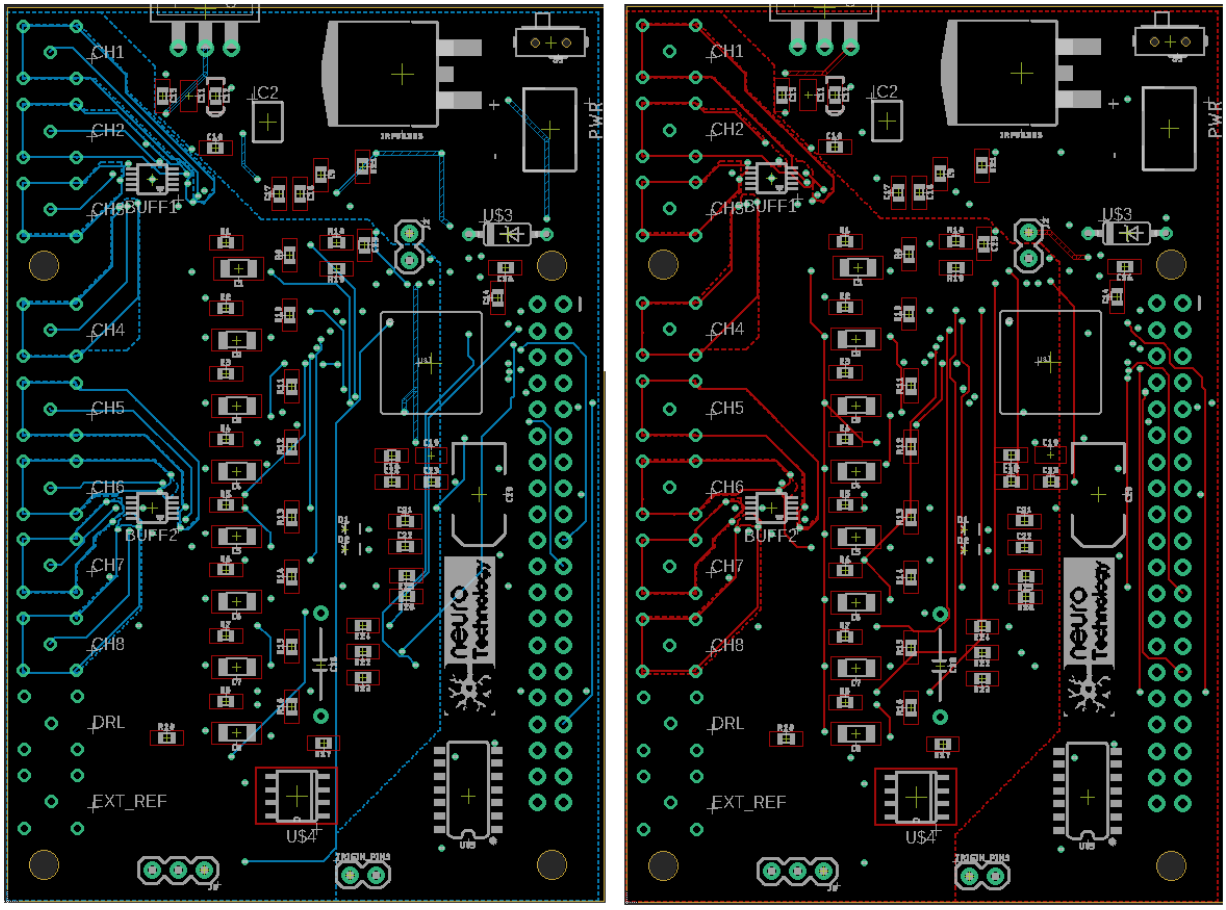

Figure 16 – Inner layers Route 2 (left) and Route 15 (right) view

This division can be also be noticed in Figure 10, which illustrates the inner, not visible layers called Route 2 and Route 15.

The first one mostly has analog signals, connecting the buffers outputs to ADC input channels. Route 15 contains the missing analog and digital signals , thus avoiding to crowd bottom or top layer.

Figure 11 shows the selected Design Rules (also known as DRU) from a Eurocircuits rules set, while in Figure 12 a tridimensional top view of the PCB can be observed.

Figure 17 – Layers detail from Eurocircuits Design Rules (DRU)

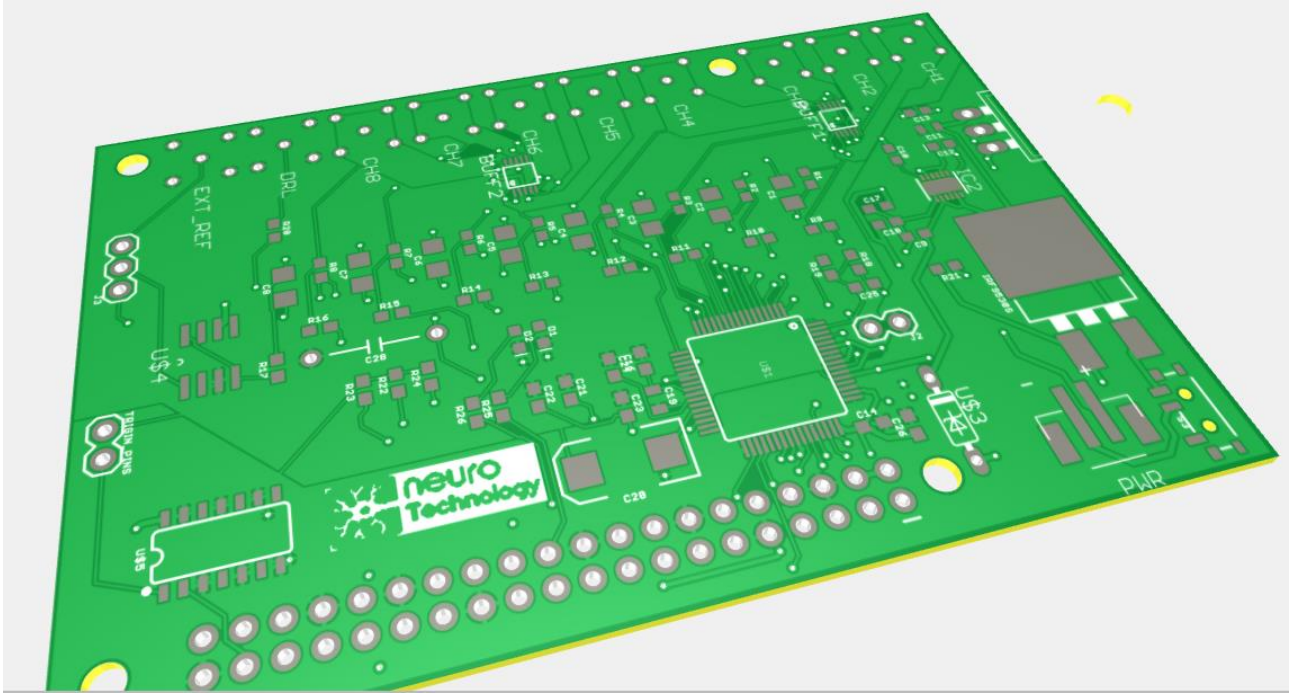

Figure 18 – 3D view of the final PCB

5.1.2.2. Power supply unit

After some considerations it was decided to design the PCB splitting analog and digital parts, in order to prevent digital noise from obscuring the weak and sensitive analog input signals; for this reason, the Power Supply Unit is isolated in the upper-right part of the board.

The grounds, analog and digital, are completely separated for all the four layers, but are joined in a single point, usually called “star point”, to have a common referential potential. To avoid the introduction of currents in analog ground the star point is chosen close to the supply unit: in our PCB is a 2-pin header connector working as a

"bridge" between the two grounds. Another major reason for the grounds division is that analog-to-digital converters usually require two different reference grounds (AGND and DGND). Another peculiar feature is the placement of a Single Pole Double Throw (SPDT) switch at the very entry of the power supply unit, to switch eventually off the whole board in case of emergency or better, to avoid power wastes.

5.1.2.3. Electrodes input circuitry

The electrodes input circuitry is a very critical one, due to the high noise intolerance, as testifies the amount of tricks to avoid it treated in this subchapter.

The ADS1299 (Feuer, s.d.) is fed by eight electrodes for eight channels, plus an electrode for the reference (optional) and one for the bias.

The reference has two modes from which the user can choose from, single and average reference.

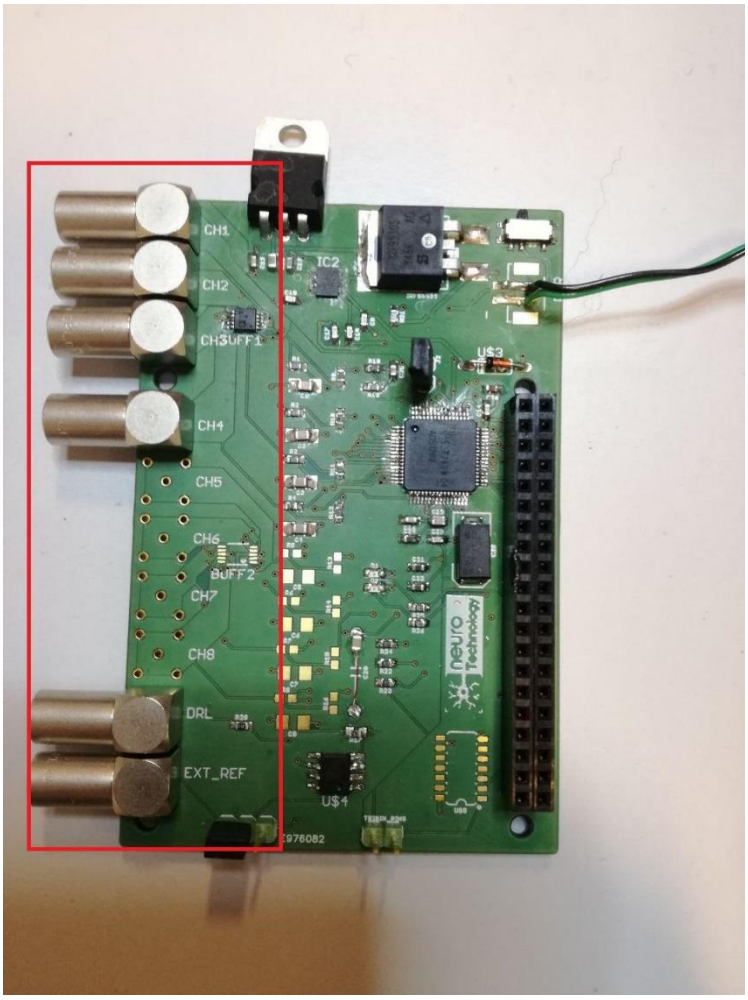

Figure 19 - Final PCB. Input circuitry is highlighted in the red rectangle

For the first one, a reference electrode is connected to drive the common reference voltage, while in the second mode an average of the inputs is used for this purpose.
In Figure 13 a photo of the final PCB contains the input circuitry just depicted: for testing celerity purposes, just four channels of coaxial connectors have been soldered, plus the reference and the DRL ones.

EEG signals are in the range of µV, but noise usually is in the order of mV, thus seriously threatening the quality of input signals.
Some expedients have been thought to increase noise attenuation, a crucial requirement. Common-mode noise is caused by common-mode signals coming from several points along the circuit, as well as the human body, which acts as an antenna for 50-60 Hz radiation. Luckily, it can be canceled by using a Bias Drive, which consists in driving back to the subject the inverse of the common-mode signals in a closed loop, in order to maximize the CMRR. It is also known as Driven Right Leg (DRL) circuit as the feedback loop is closed with an extra electrode on the patient's right leg.
The ADS1299 has an in-built Bias Drive that supports this, through BIAS_OUT pin.

Another expedient to overcome the noise is, as already sketched, to use differential low pass filters between the reference and the positive inputs. Capacitors between the lines are seen as large impedances for low frequency components of the signal, but high frequency signal components are identically present on both lines. The low-pass filters used have a cut-off of 0.98 KHz and allow the attenuation of high-frequency noise.

An extra precaution to assure the high, essential CMRR is the presence of the AD8244 buffers. This thanks to its huge input impedance of 10 TΩ, which permits to respect the CMRR requirement, according to the formula in section 5.1.1.3.

But maybe the most peculiar and relevant noise reduction factor is given by the Active Shielding. Evoked potentials come to the board protected by the outer shell of the

coaxial cable. The concept of Active Shielding is to keep this kind of protection valid all the way to the buffers.

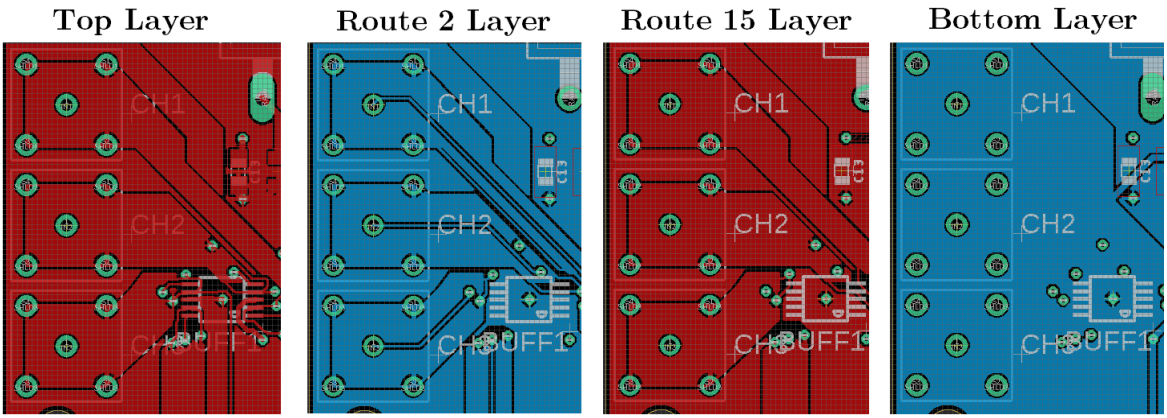

Figure 20 – Detail of the three entry signals circuitry for the four layers. The difference with Figure 16 is that the copper pouring is missing to have a better view while here the planes are filled with it.

The coaxial cable shield is connected to the first three planes, linked through the vias (for each channel, the four green dots that shape a square).

Analysing Figure 14, Top and Route 15 layers work as external case encapsulating and protecting the weak, feeble EEG signal laying in Route 2 plane.

As regards the Bottom layer instead, it is just a general ground plane, for further covering from electromagnetic interference (EMI).

In Route 2 Layer can be noticed the thin traces bringing the EEG signals, again encompassed by the coaxial shield by means of copper poured and wrapped around it. Using such a shield gives some benefits, such the reduction of environmental interferences and parasitic capacitances effects.

5.1.2.4. ADS1299 analog-to-digital converter

The ADS1299 is positioned in the central-right part of the circuit, but still in the analog subdivision. This to maintain a certain distance between the very sensitive input signals and the noisy digital section. Simultaneously, the pins on its right side are all digital, and this makes the connections with the close Raspberry Pi 3 much easier.

The 64-pin ADC is the most expensive component of the PCB due to its complexity and high performances.

Data streams managed by ADS1299 are 216 bit long: the first 24 bits are employed for the registers values configuration, while the rest are 24 bits for each of the 8 channels. Every channel's data is converted to 2's complement by inverting the bits and adding 1, neglecting overflow case. The ADS1299 is configured in the desired mode by giving the wanted values to some registers, as it can be seen in Table 1:

Register	Hex Value	Bit Value
CONFIG1	0x96	0b1001 0110
CONFIG3	0xEC	0b1110 1100
CHnSET	0x07	0b0000 0111
BIAS_SENSP	0x00	0b0000 0000
MISC1	0x20	0b0010 0000

Table 1 – Registers values for the desired configuration

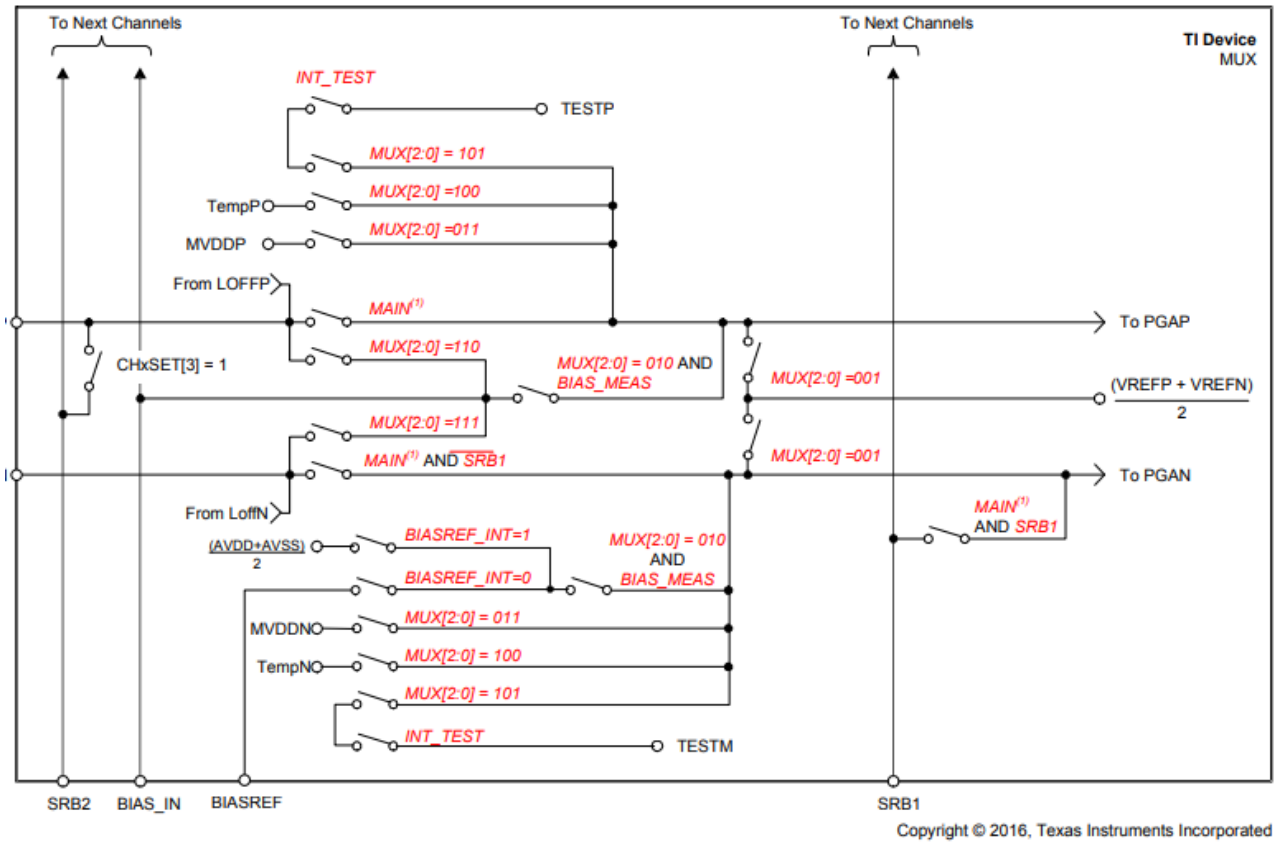

Figure 21 – ADS1299 inner view: the programmable multiplexers are highlighted in red

This permits to program the inner multiplexers in order to make the converter function in the desired way (see Figure 15 for an intuitive outline of the possible multiplexers combinations).

The board also has a Schmitt Trigger on it, introduced to sense a possible external trigger (connected through two a two-pin header connector in the lowest part of the PCB) for emergency or other particular events. It has not been used at all, but it could be employed just by reading the appropriate pin (TRIGIN) on the Raspberry Pi 3.

5.1.2.5. Raspberry Pi 3 interface

As already mentioned in section 5.1.1.5, a pin inversion in the design brought to have MISO and MOSI pins switched. In Figure 16 is depicted the arranged solution, by using a custom 40-pin ribbon cable.

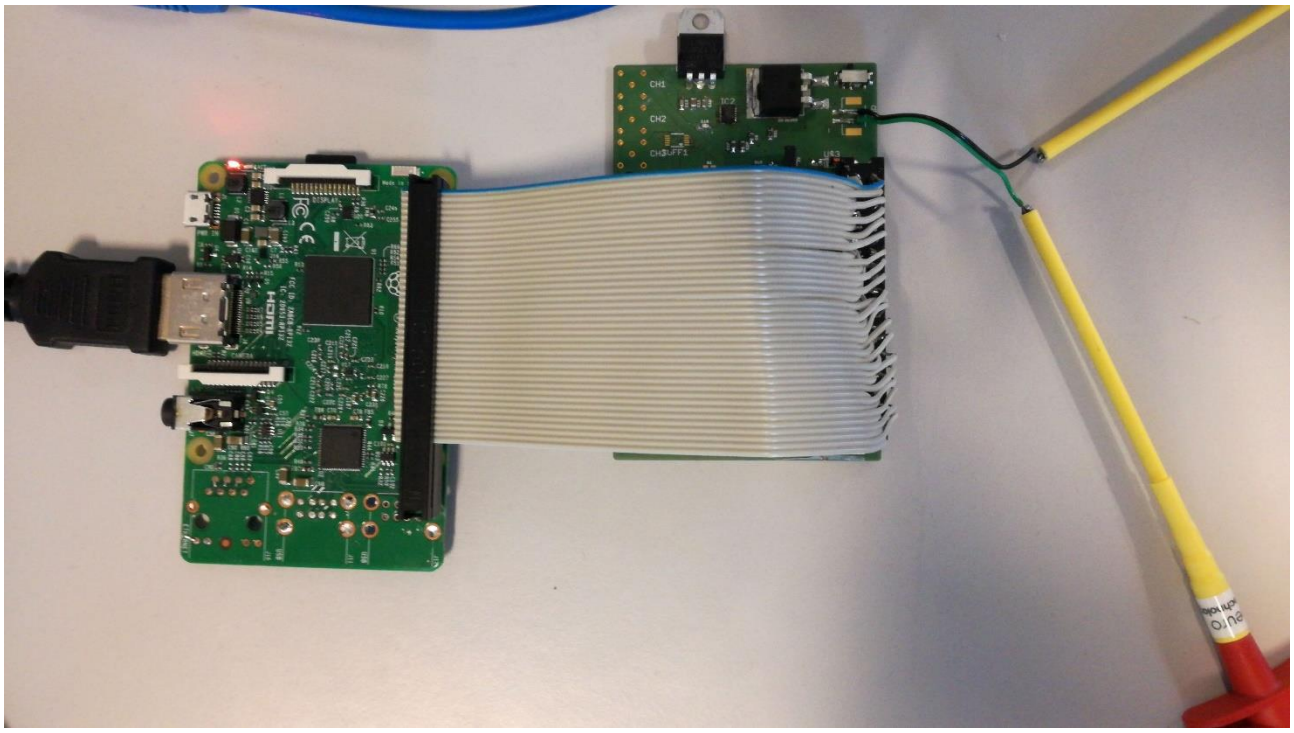

Figure 22 – The EEG node PCB connected through a 40-pin ribbon cable to the Raspberry Pi 3 computer

Even if not the most aesthetically elegant solution, it has resulted suitable in terms of effectiveness.

5.1.3. Physical verification

A small parenthesis on the PCB design checks shall be done.
Physical verification, in fact, is a check process for integrated circuits layout design, by means of EDA software tools to assure that certain criteria are met.
The two checks done by the EAGLE EDA tool are Electric Rule Checking (ERC) and Design Rule Checking (DRC).

The first one, the Electric Rule Checking, controls the whole electrical connections that are considered dangerous in the circuit and ensures correct power and ground connections.

The Design Rule Checking is the determination of whether the physical layout of a chip respects some required technology parameters, from the semiconductor manufacturers, called design rules. Usually the DRC checks width, spacing and enclosure between traces and components on a board, with the main objective of enhancing the overall yield and reliability of the design. The design rules are not strictly mandatory, but, in case of violation, the design may not be functional.
For this project a set of peculiar EAGLE Design Rules from Eurocircuits has been used (see Figure 11), to make the printing of the PCB by the same manufacturing house easier, faster and safer. The printing and shipping of the PCB by the specialized manufacturer Eurocircuits took around two weeks.

5.1.4. Final PCB: size and features

The design of the EEG Node PCB covered almost a couple months of work and, with the exception of the error already quoted in section 5.1.1.5., the result is a small, solid, functional Raspberry Pi 3 shield with the ADS1299 as its central core.
The many design precautions, obtained and adjusted by the precious lead of Prof. Kidmose, brought to a highly satisfying achievement.
In figures 17, 18, 19, some pictures of the design steps can be observed.

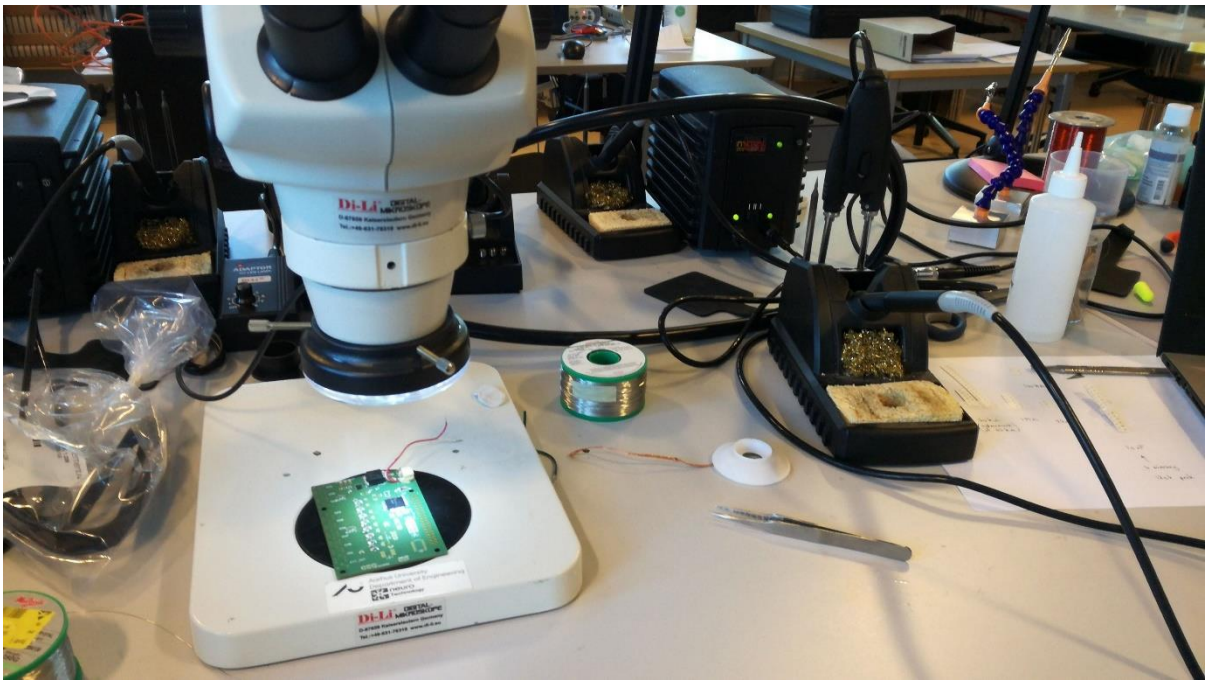

Figure 13 – PCB components soldering in the Neuro Technology Laboratory

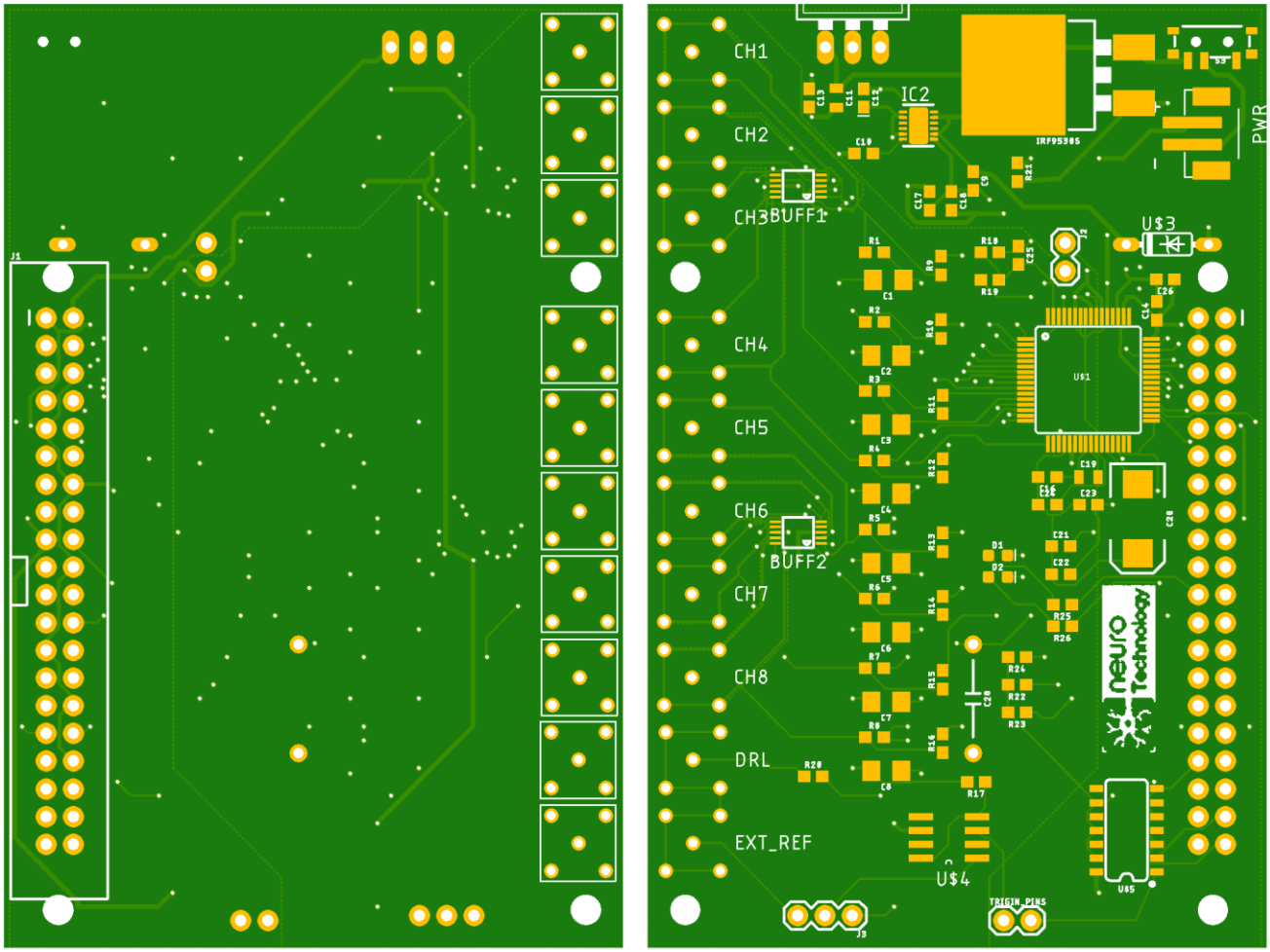

Figure 24 – Top (right) and bottom (left) views of the final EEG Node PCB

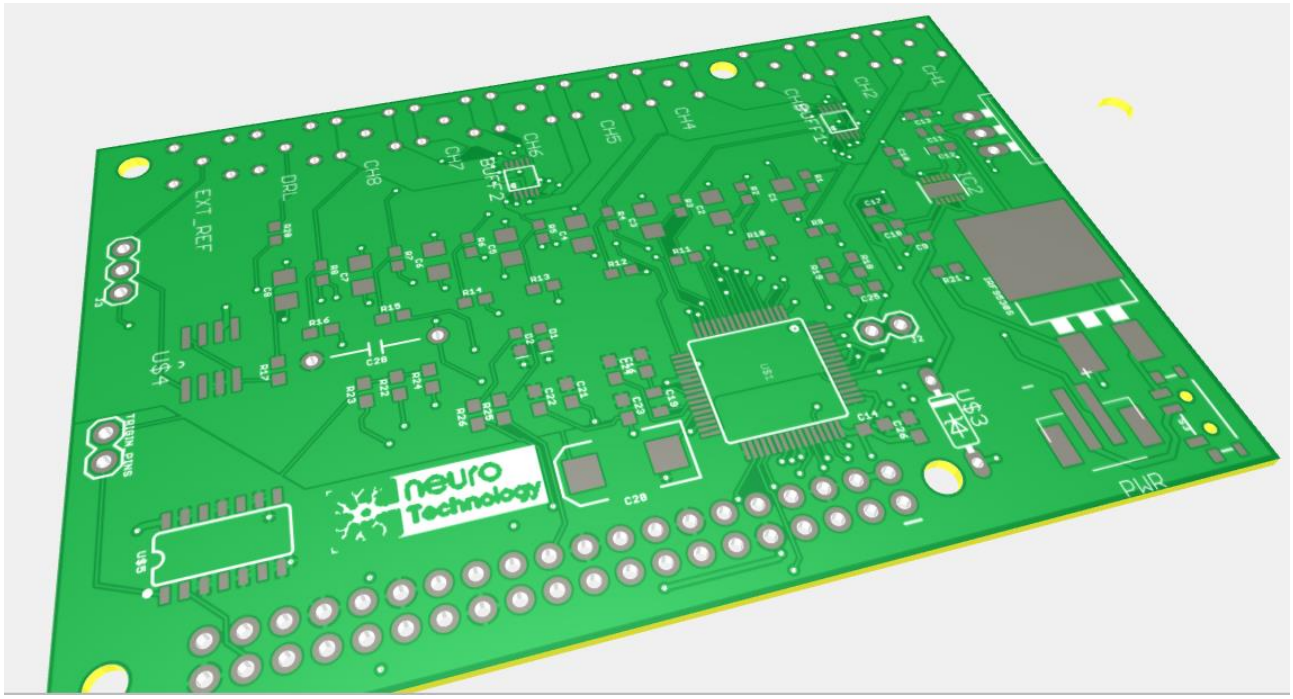

Figure 25 - Tridimensional top view of the PCB

Chosing to use four layers means having an orderly board, allowing a good spacing between traces and components of each layer, simplifying Place and Route.

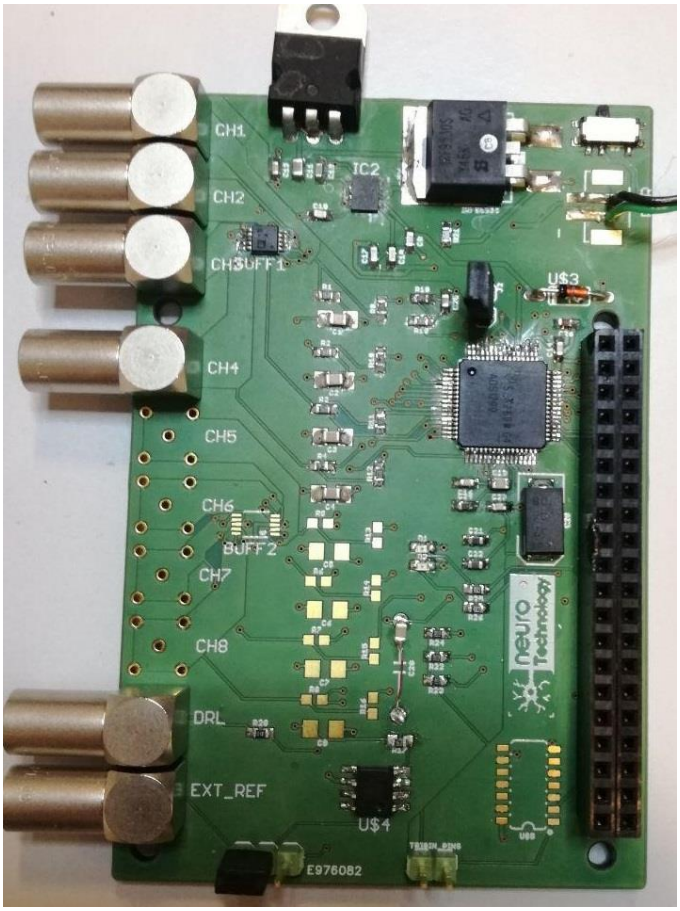

Figure 26 – Final PCB in its entirety

The components are partially soldered (see Figure 20) for celerity testing purposes, as already revealed in section 5.1.2.3.

In the end, final PCB size is 86.5mm per 57.5mm, reproducing almost perfectly Raspberry Pi 3 dimensions, fitting on it as a shield.

5.2. Lab Streaming Layer and Software

The Lab Streaming Layer (or LSL), previously faced in chapter 4.6, is a software device created by the University of California San Diego for research purposes to synchronize a stream of data across devices, while monitoring it.

This powerful tool was used for the testing phase of this project, specifically to have a graphical representation of the real-time stream of data coming from the EEG channels.

First of all, it is essential to understand the correct flow of the EEG streams from the beginning to the end.

The electrodes sense the evoked potentials and transmit it as an electric signal through the coaxial cables and the input connector to the created board.

After the input filtering and the precautions already discussed, data signals are converted into digital by the ADS1299 analog-to-digital converter.

The output stream of data is transmitted via the SPI communication protocol (supported by both the Raspberry Pi 3 and the ADS1299), indeed, serially, in a sequence of bits thus dissected and managed by a specific custom program written in C language and run on the Raspberry Pi 3.

This program is crucial for many reasons: it defines a start and an end points for the data streams acquisition, offers a graphical user interface (or GUI) for an easier testing and allows a deeper, custom interaction with the many programmability chances of the ADS1299.

The program's code contains a library available in C to access the BCM2837 chip from Broadcom, which has the quad-core ARM Cortex A53 (which runs at 1.2GHz) as central nucleus.

This means having the ability to access the GPIO pins on the Raspberry Pi 3 header and use some for SPI function (or I2C, but it's not the case of this project).

Moreover, the data transfer through the lab streaming layer, from the Raspberry to the computer, is synchronized is mainly based on the use of these four elements:

- Stream Outlets: data streams given available as outputs on the lab network. Data can be sent either sample by sample or in chunks (not in this case). Follows a syntactic example:
  Syntax: info = lsl_create_streaminfo (group name , signal type , channels, frequency , data type, stream name);
  * outlet = lsl_create_outlet (info , chunk size , buffer size);
- Resolve Functions: used to resolve streams on network, also based on the meta-data of the outlet or its group name.
  Syntax: result = lsl_resolve_byprop (lib , property type , property);
- Stream Inlets: allows the reception of stream outlets. Data is collected in the same order as it was pushed into the outlet. The one that follows is a syntax use example in MATLAB.
  Syntax: inlet = lsl_inlet (result);
  [vec ,ts] = inlet.pull_sample (chunk size);
- Built-in Clock: the complete synchronization is guaranteed by a network clock. Each inlet and outlet are paced by the network clock, which means every important event is "timestamped". Time synchronization can be customized.

The software is based on a C language program and is thought to be run on the Raspberry Pi 3 to make the whole system work as desired, in order to obtain a real-time representation of the 8 EEG incoming channels.
The source code descends from the pre-existing one written by the Danish students this thesis heavily relies on.

It is divided in three files, "mainProg_fz.c", "ads1299_fz.c" and "ads1299_fz.h".
The first one contains the main functions and the overall flow of work of the program, as well as the rudimentary UI (user interface), which is more precisely a menu, allowing to choose between different options and work modes (see Figure 21).
In file "ads1299_fz.c" functions are specifically described, in order to read, transmit and convert incoming data from the converter, as well as reset or modify its registers.

Eventually, in the third header (.h) file, “ads1299_fz.h”, many basic used libraries are defined as well as other definitions (#define) and function prototypes.
The use of a variety of commands, macros and functions is possible due to the inclusion of the core external libraries employed, BCM2835 (AirSpayce, s.d.) and LSL ones, backed by several C libraries.

Working on Raspbian (Debian distribution for Raspberry Pi ARM architecture) meant acquiring the ability to navigate through the Unix environment and being capable of exploiting it. The compilation of the program was feasible with the following command which included all the libraries from the correct directories:

- gcc -Lusr/local/lib/lsl -o prog_fz mainProg_fz.c ads1299_fz.c -l:liblsl32.so -lbcm2835

Furthermore, the program was run with:

- sudo ./prog_fz

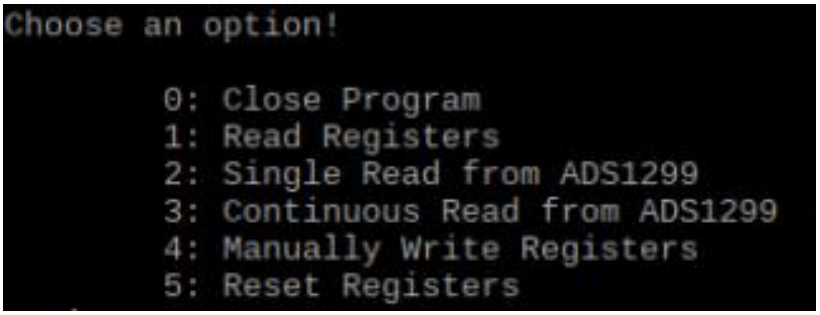

Figure 27 – The menu used as UI (user interface)

The menu offers the user six options:

0) Close Program: exits the program.
1) Read Registers: scans the register values and prints them.
2) Single Read from ADS1299: prints a single read from the converter for the 8 channels, even not connected ones (see Figure 22). Useful for short testing purposes.
3) Continuous Read from ADS1299: the values from the 8 EEG channels are converted and printed continuously in a real-time representation. This one is meant to be the established, default mode for the nominal work of the system.
4) Manually Write Registers: changes internal ADS1299 registers values to modify the multiplexers positioning and, for instance, to vary the Programmable Gain Amplifier.

5) Reset Registers: resets many register to a prearranged set of values.

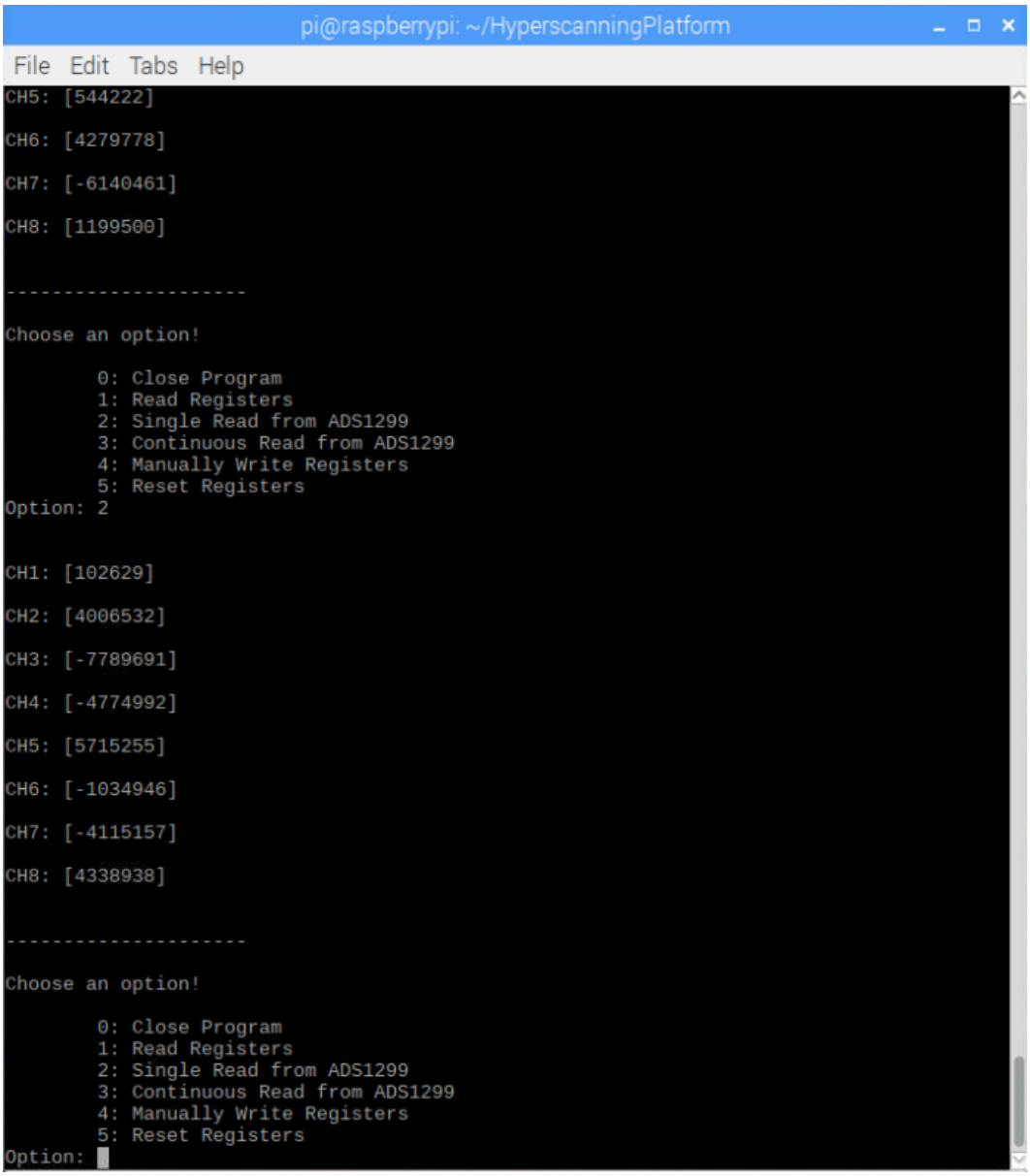

Figure 28 – An example of Single Read from the EEG channels

In Figure 22, a Single Read execution: the weird, high values (some negative, too) are due to the fact that the corresponding channels are connected to nothing, and thus at the mercy of the noisy environment.

10.1. Overall system analysis

A summary of this project printed circuit board's main features follows.

The custom designed PCB was created to be a Raspberry Pi 3 shield, even if it has not been possible because of the pin inversion mistake, problem solved by using a ribbon cable.

Several precautions were taken to attenuate noise (CMRR, low pass filtering, active shielding).

The price was maintained low thanks to the attention in the design built almost from scratch. For further cost details, refer to section 9.2.

Thanks to the very well developed earlier code the software adjusting did not take too long and, even if the user interface was not extremely elegant, it showed to be truly practical.

The analog and digital separated grounds was an almost mandatory choice to reduce digital interferences to the feeble inputs. Analogously and for the same reasons, the analog and digital power sources necessary to supply the ADS1299, come from two different units.

A final thus relevant information about the system regards the fact that it is designed to work autonomously thanks to a battery as power supply: the desired autonomy consists in 10 hours of life, and a couple of 3.7V batteries in series, for a total of 7.4V, can be considered enough to meet the above requirement.

6. Testing and Debugging

6.1. Performance simulations

In order to test the system the first idea was to exploit a Python example program to demonstrate how to manage a multi-channel EEG transmission through the lab streaming layer. The line of code that follows describes the type of data in the time series vector, that is a EEG content on 8 channels at the frequency of 100Hz, float-valued data and id label 'myuid'.

- info = StreamInfo('BioSemi', 'EEG', 8, 100, 'float32', 'myuid')

After several tries, the Raspberry Pi 3 and the PC (connected to the same WLAN of course) were able to communicate and the "fake" stream of data was acknowledged by both a receiving Python sample program and a MATLAB script, both part of the suite of tools and apps provided by the Lab Streaming Layer distribution.

In Figure 23 can be viewed the MATLAB plot of the already mentioned 8-channel transmission of fake data for the simulation.

This first step was a complete success, having a very accurate and plot, with the possibility of recording data within a log file for subsequent analysis.

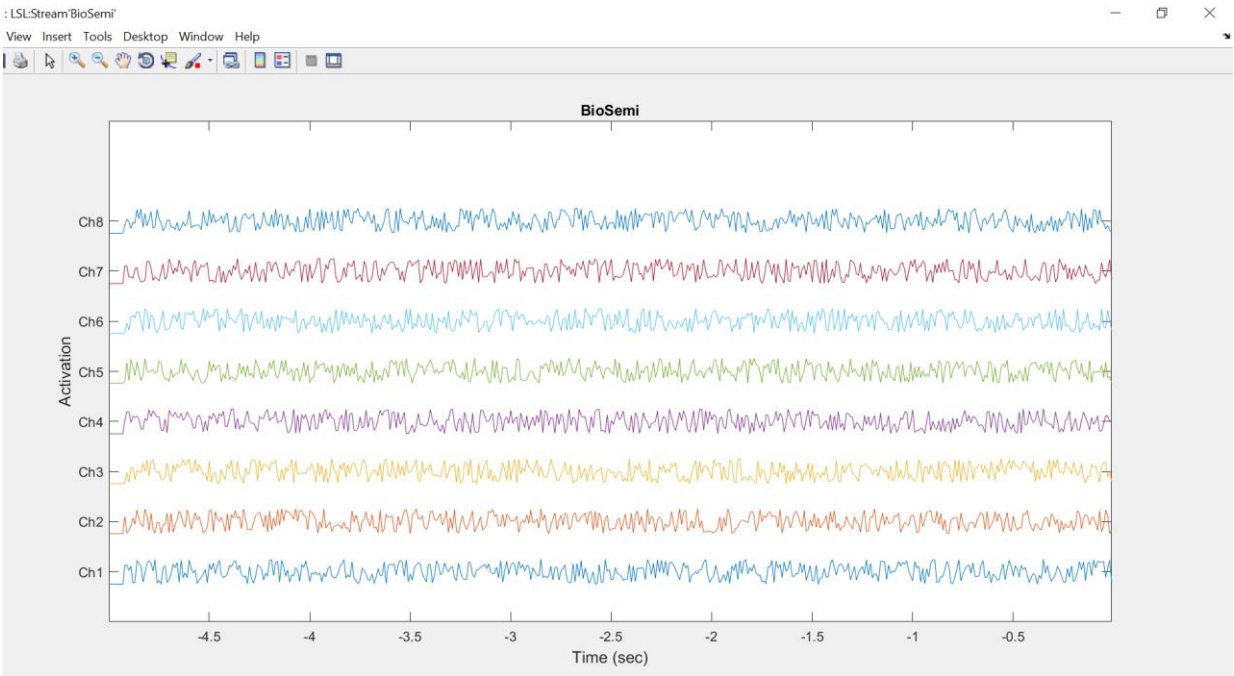

Figure 29 – The 8 channels of simulated EEG data streams

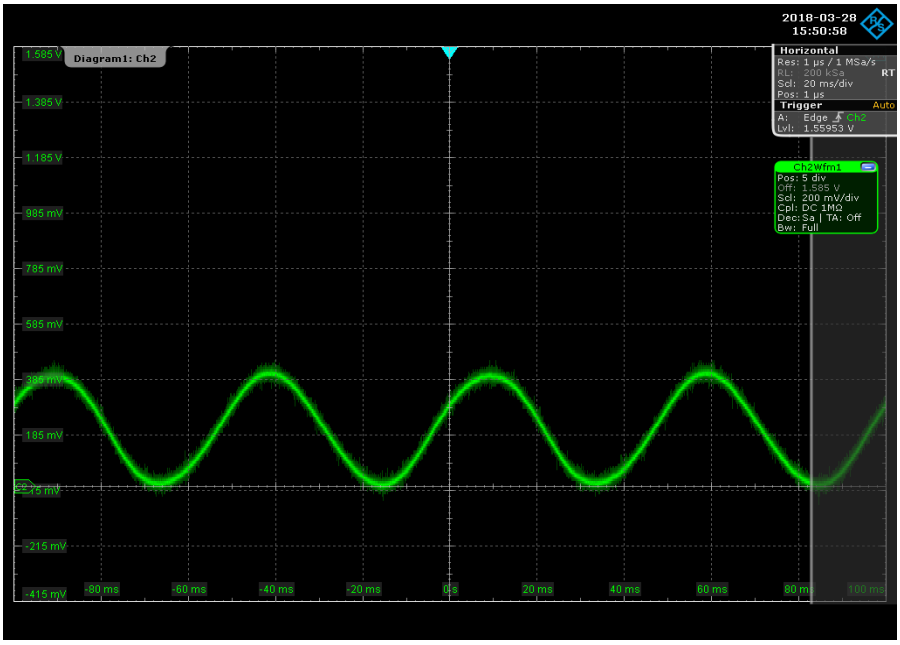

Figure 30 – Input signal at 20Hz, 300mVpp with 175mV as offset

Another interesting peculiarity of the Lab Streaming Layer is the possibility of accessing the data streams in real-time on this virtual multi-channel from as many terminals as desired, so the same real-time results could be seen from different posts (but still connected to the same WLAN).

Then the testing move forward to a second phase: the acquiring of an analog input by the ADS1299, its conversion into digital to the inside of a certain range and it's transmission to the LSL as the previous simulated data.

This became to be the most demanding difficulty because of the complexity of understanding, using and adapting data management commands and functions of the SPI protocol, the LSL C library and, mainly, the ADS1299 rules for analog data acquisition and its correct conversion into digital.

Despite many different attempts with analog input variations and entire days of code manipulation to obtain a proper output from the analog-to-digital converter, this final step failed. The possible causes are treated in the next sub-section, '6.2 Results and predictions'.

In Figure 24 and example of analog input chosen. The waveform was a sinusoid at the frequency of 20Hz, 300mV peak-to-peak amplitude and an offset of 175mV.

The modifications to the inputs were mostly on the offset, while the frequency oscillated from 5 to 50Hz, being the EEG scalp evoked potentials in a range from few Hz up to around 32Hz.

The peak-to-peak amplitude values were expressly way larger than the EEG typical ones (from 10µV to 100µV) to make test easier and clearer.

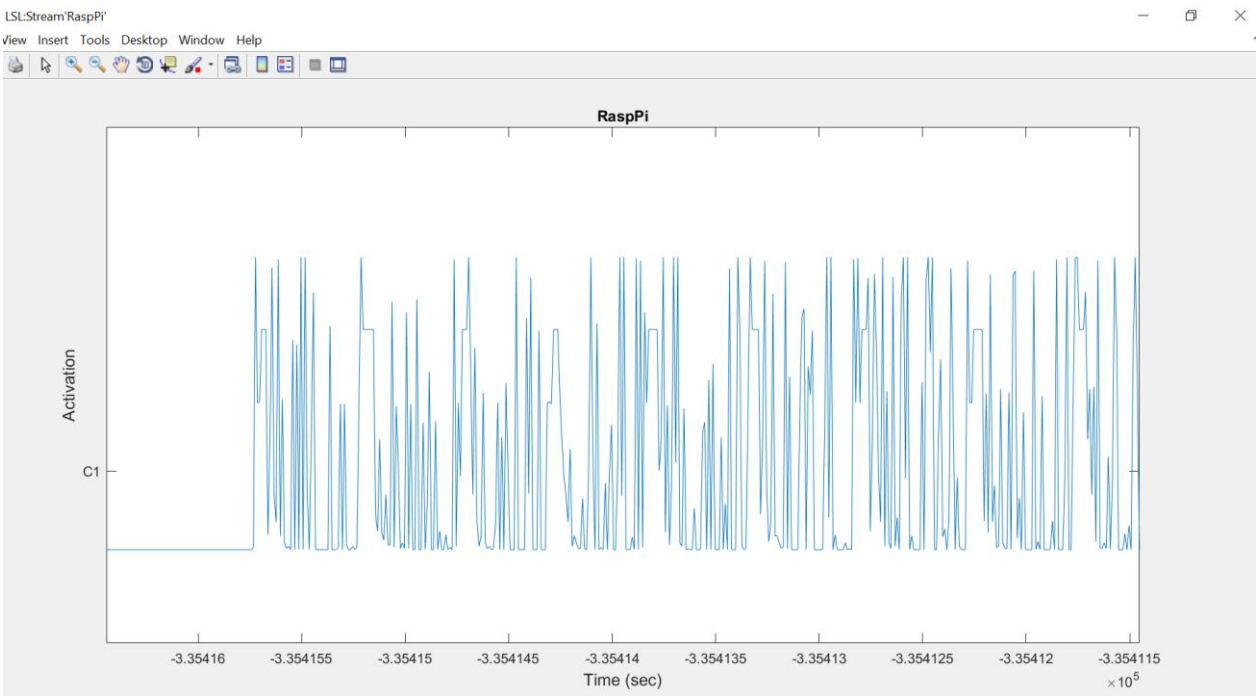

Figure 31 – CH1 ADS1299 output: signal saturates to very high peaks of voltage, maybe because of DC noise

6.2. Results and possible improvements

The designed system complexity did not prevent to succeed in the majority of the tasks set. In fact, this project encompasses electrical circuits and electronic systems backgrounds, HW PCB design and ECAD tools skills, as well as C programming knowledges applied to complex ICs such as the ADS1299 analog-to-digital converter.

After many tests no errors were eventually found in data transmission over the Lab Streaming Layer. All the major requirements set were met or at least attempted to be overtaken. Unfortunately, a last obstacle was not overcome because of the harshness of the problem: debugging and fixing a possible code error in data conversion absolutely needed at least another month of work.

However, many other aspects of the project could be improved. Here are some ideas.
A worth and obvious enhancement could be, as already mentioned, the correct conversion of data input and the calibration of the ADC output to have a working system even with waveforms way over the EEG signals ranges.

A review of the HW design could also be useful to prevent and remove the residual, likely DC noise coming from the power supply unit.
Indeed, as it can be analyzed in Figure 25, a possible cause for the corruption of converted data could be due to the higher magnitude of noise with respect to the analog inputs.

Another further step could be the exploitation of every single feature implemented and not used in this project (such as the external reference).

A next goal could be customization: it would be nice to have a more elegant User Interface (made in MATLAB or Qt, perhaps) and a careful change in the Lab Streaming Layer apps used (being open-source), also in terms of facilitation for the user or next student working on this project to clearly understand how the system works, how it can be run and potentially customized.

With respect to this intention, the modularity of the many features of the project could be more accurate and fluid.

To have a valid feedback regarding the autonomy of the system supplied by the 7.4V battery, some experiments could be performed as well.
The system was developed to work with dry electrodes, which brings more options while choosing electrodes but some disadvantages in terms of noise and performances, to this day.

Eventually, after a final simulation with multi-channel pseudo-EEG analog input signals, single and then multiple, hyperscanning experiments could be performed to realize the sociological and biomedical studies hinted at in the abstract, the final goal of this entire work.

And after collecting plausible data, a comparison with similar studies could be done, also facing the innovative use of the dry electrodes, whose performances are so far uncertain but exciting.

7. Conclusion

The amount of work of this project was huge, very difficult to be managed entirely by a single master thesis student in just six months.
However, thanks to the amazing previous thesis work by the Danish students Paul Rajani Lassen and Mikkel Hartmann Rasmussen, the careful and lovely supervision of professor Preben Kidmose and a lot of open-source material (the Lab Streaming Layer distribution by the UCSD, for instance), the aim of building a low-cost, open-source, wirelessly connected system for EEG hyperscanning studies purposes was surely reached at least in an embryonic stage.

The final cost of the designed component stays around 290€ (120€ to print three PCBs and 170€ for the components to be soldered on two of them, which were mostly already present in the laboratory, lowering the expense to about 130€), but being the commercial price of around 15.000$ for this peculiar device (the lab was equipped with a couple of them for a variety of experiments), the savings with this open-source platform are surely remarkable (go to sub-section 9.2 Bill of Materials for more details).

The ADS1299 by Texas Instrument turned out to be the perfect candidate to manage EEG (and ECG too) signals, assuring high performances and a full set of options for the evoked potential acquisition.
Also the low-noise buffers and the almost entirely SMD (surface mounted device) components for the compactness of the board are wisely chosen

This project can be in any case included as a perfectly formative experience, which challenged me in many ways and sharpened my skills. Moreover, the satisfactory result and the proud of having the outcome of hard work is immense.

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9. Appendices

Appendix A - Datasheets

Appendix B – Software: C Code

Appendix C – System Design: schematic and board layout

10. Bill of Materials and Cost Estimate

The BOM (Bill of Materials) brought, as already mentioned, to a final expense of 10,72€, being many components already present in the lab, while the PCBs prints costed about 120€.

In the following tables a summary of the proper bill of materials.

Bill Of Materials

Part	Value	Price (€)
C22	10pF	0,094
C23	100uF	0,9713
C25	1nF	0,323
C19	10uF	0,18
SMD LEDs:		
D1	RED0603	0,612
D2	GREEN0603	0,612
LDO regulator:		
IC2	LT1763CDE-5	4,45
P-Mos:		
IRF9530S	IRF9530S	0,8433
Connectors:		
PWR	JST_2PIN-SMT	0,6388
SPDT Switch:		
S3	SPDT_SMD_SW	0,66
Zener Diode:		
U$3	1N5240	0,12
Schmitt-Trigger:		
U$5	74HC7014	1,22
TOTAL COST IN €:		10,7244

R21	100kΩ	0,221
R22	33kΩ	0,221
R23	33kΩ	0,221
R24	33kΩ	0,221
R25	220Ω	0,255
R26	220Ω	0,255
C1	10nF	0,4682
C2	10nF	0,4682
C3	10nF	0,4682
C4	10nF	0,4682
C5	10nF	0,4682
C6	10nF	0,4682
C7	10nF	0,4682
C8	10nF	0,4682
C21	10nF	0,4682
C14	0.1uF	0,323
C16	0.1uF	0,323

Already in the lab or in the shopping cart:		
CH1	EPL.00.250.NTN (coax)	
CH2	EPL.00.250.NTN (coax)	
CH3	EPL.00.250.NTN (coax)	
CH4	EPL.00.250.NTN (coax)	
CH5	EPL.00.250.NTN (coax)	
CH6	EPL.00.250.NTN (coax)	
CH7	EPL.00.250.NTN (coax)	
CH8	EPL.00.250.NTN (coax)	
DRL	EPL.00.250.NTN (coax)	
EXT_REF	EPL.00.250.NTN (coax)	
U1	L7805 (volt.reg.)	
U$4	LMP7701 (prec. opamp)	
U$1	ADS1299 (ADC)	
J2	CONN_02	0,0426
TRIGIN_PINS_TRIGIN	CONN_02	0,0426
JMP_SW	CONN_03	0,2981
R1	16.2kΩ	0,221
R2	16.2kΩ	0,221
R3	16.2kΩ	0,221
R4	16.2kΩ	0,221
R5	16.2kΩ	0,221
R6	16.2kΩ	0,221
R7	16.2kΩ	0,221
R8	16.2kΩ	0,221
R9	33kΩ	0,221
R10	33kΩ	0,221
R11	33kΩ	0,221
R12	33kΩ	0,221
R13	33kΩ	0,221
R14	33kΩ	0,221
R15	33kΩ	0,221
R16	33kΩ	0,221
R17	16.2kΩ	0,221
R18	1MΩ	0,085
R19	16.2kΩ	0,221
C23	0.1uF	0,323
C9	1.0uF	0,111
C17	1.0uF	0,111
C18	1.0uF	0,111
C21	1.0uF	0,111
C22	1.0uF	0,111
C24	1.0uF	0,111
C26	1.0uF	0,111
C11	0.33uF	0,493
C10	10pF	0,578
C12	10uF	0,578
C13	0.1uF	0,111
BUFF1	AD8244MSOP	4,22
BUFF2	AD8244MSOP	4,22
J1	RPI-40-PIN-GPIO_PTH	1,661

Table 2 – Bill of Materials