POLITECNICO DI TORINO

Department of Electronics and Telecommunications

Master's Degree in Electronic Engineering

Master's Thesis

Design of a Switched-Capacitor Step-Down Converter

Supervisor

Prof. Franco Fiori

Candidate

Francesco Ferilli

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"When you base your expectations only on what you see,
you blind yourself to the possibility of a new reality."
(cit.)

Acknowledgments

A year has passed since I started working on my master thesis, when my advisor entrusted me with this challenging topic. But this work is the only thing most people can see of a 5-years path, the tip of an iceberg, underneath you can find many special people supporting it. Those people deserve a special thank for giving me a reason not to give up the pace of this intense period.

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It's time to thank the TrickingTO team. Our friendship may not be so longstanding, but I sincerely feel it is going to be that way. It didn't took long to realize this group, even though so heterogeneous, is something deeper than just a sporting team. You and the tricking came to my life when I needed the most. I will be back soon for training to be your personal GIF-man.

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Elena, Federico, Adrian, Andrea...each of you deserve his own section, but I feel like it wouldn't be the same if you were not all together, because you really are like a family to me. We know each other, we laugh at each other, we challenge each other. I hope future is not going to separate us. Maria, you may be the last member of the group, and you may live far away but you are part of this pack, too.

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You really are one of a kind !

Abstract

Nowadays, cars are moving toward the 42 V battery architecture, but part of the electronics still rely on the 14 V power line. The alternator, for this type of system, is designed to deliver 42 V. Hence, a converter is needed to deliver power also to the 14 V power line. The typical 14 V-load power consumption is about 1 kW, which is a relatively high power. When working at high power, the most critical parameter to take care of is the efficiency: in the first place, to avoid internal energy dissipation to be critical for the reliability of the converter, but also to make battery-based systems last as long as possible.

Instead of resorting to conventional converters (studied for so long, hence reliable and mature in control), this work aims at studying a switched-capacitor converter solution. The most remarkable feature of this type of converter is that high efficiency can be achieved without making use of any inductor. Indeed, this type of converter does not resort to magnetic energy conservation, and uses only capacitors and switches for voltage conversion. Except for low-power applications, in which the output voltage can be regulated maintaining high-efficiency, the voltage gain is fixed (*e.g.*, doubling, halving, inverting the input voltage); that is why they are mainly employed as charge pumps, for instance in electrically re-programmable memories to boost up the voltage and erase the memory, or to drive high-side MOSFETs, as an alternative solution to the bootstrap technique.

Starting from an overview of the different available converter solutions, the subset of the switched-capacitors converter is introduced, presenting also some examples where they have been implemented even for high power conversion. Next, this type of converter is studied more in detail. First, the analysis of a simple 1-to-1 switched-capacitors converter is performed, to define the criteria that make any

switched-capacitors converter work in its most efficient operating conditions. Hence, some generic rules are derived for what concern efficiency when energy is exchanged between capacitors, and also the reason why a switched-capacitors converter is not so much sensitive to duty ratio variations.

The previous analysis is not enough to extract design equations to size the components, and neither the state-space average method (the most generic method, applicable to any converter) helps out, because it is not possible to derive easy-to-handle equations. Hence, an alternative analysis method has been studied: exploiting from an already available one, a further study has been developed to determine the value of the capacitances, number of parallel capacitors, ESRs, on-resistance of the switches. The proposed algorithm is then applied to the selected topology that performs 42-to-14 (hence, 3-to-1) conversion, to be implemented in the aforementioned automotive application.

The sizing of the components and the validation of the design method through simulation was just the first problem faced. With the aim of realizing the converter, many others problems related to how to drive the converter arose. Starting from including the model of real MOS-transistors, other problems came in succession such as driving a multilevel switch structure, defining start-up procedure safe in all conditions, isolating the switching timing signals (etc.). Each component model that had to be included, was simulated first to ensure the behavior of the system was not altered.

To compare the results, a buck-based converter has been designed, too. Since a single buck looked to be too much stressed, a multi-phase converter has been designed. Conventional solutions have a limit on the conversion ratio, because it is directly dependent on the duty ratio (typically larger than 25%, *i.e.*, 4-to-1), which heavily affects the system efficiency. That is why, even if isolation is not needed, a transformer sometimes is employed to increase the conversion ratio. On the other hand, switched-capacitor converters' efficiency does not depend on the voltage gain but rather it depends on switching frequency, capacitance values, ESRs and on-resistances of the switches. That is because, if correctly designed, the capacitors work at an almost fixed voltage, ad the main loss contributions are related to charge-balance losses when capacitors exchange energy, and to parasitic resistive power dissipation.

Hence this type of converters can be implemented either for low voltage gain applications (*e.g.*, 2-to-1), either for high conversion ratios (*e.g.*, 10-to-1) with high performances. This fixed response is what make them hard to regulate, because the converter is very low-sensitive with respect to the duty ratio.

Since, as explained, the overall behavior is much that of a transformer than that of a regulator, a better situation can be studied comparing a transformer-based traditional converter with a switched-capacitors-based converter (where no isolation is strictly needed). This particular application do not need any kind of regulation, because the input (*i.e.*, the output of the alternator) is already regulated at 42 V by a different system, and transients typically do not last more than 100-200 ms. That's why the switched-capacitor technique can be meaningfully compared to conventional solutions, in this environment.

Simulations have been run for both projects, initially to validate the switched-capacitors converter sizing algorithm, and then to compare the characteristics of both converters. The aspects that have been taken into account are efficiency performances, and number of components needed (intrinsically related to costs and area/volume). The result is that switched-capacitor converters seem to show a quite remarkable alternative to the traditional solutions. The conditions they have been design for are as close as possible to each other: same switching frequency, similar number of switches. For what concern magnetic and electric potential energy comparison, the number of inductors needed is much less than that of the capacitors actually required. What does matter eventually is the size of each single component.

A further step of this work would be the realization of the PCB and the measurement of the actual performances (to be compared with simulation results), as well as emission-related issues.

Contents

CHAPTER 1

State of the art of power supply

Power may come from different sources such as mechanical, electrical, heat, light. In order to provide power to electrical systems, a power converter working as voltage regulator is usually needed.

A power converter generates output voltage and current for a load from a given input electrical power source. The most suited solution, for each application, have to be designed taking care of efficiency, area/volume, accurate output regulation, cost, transient response, etc.

In this chapter, different available methods for power converters are presented (refer to [2] and [21]). First the oldest solution, the linear regulator. Then, switching power supplies are presented from theoretical point of view, then switched-capacitor converters are introduced.

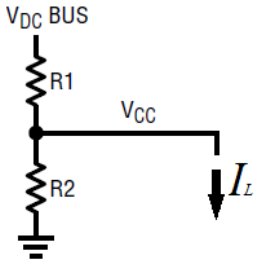
1.1 Linear Regulator (LR)

It was the basis for the power supply industry until switching mode power supplies became prevalent after the 1960s. Even today, linear regulators are still widely used in a wide range of applications.

The key idea of the linear regulator comes from voltage division, as shown in Figure 1.1.1. It can be easily seen that the voltage V_{CC} heavily varies depending on the loading conditions.

The solution to this problem can be to implement R_1 as a variable resistor, in order to keep the output voltage constant. A variable resistor can be implemented by

means of a transistor working in linear region (*e.g.*, for a MOSFET, $R_{channel} \propto V_{GS}$). In Figure 1.1.1 a simplified circuit is presented.



$$\begin{cases} V_{CC} = V_{DD} \cdot \dfrac{R_1}{R_1 + R_2}, & \text{at no load} \\ V_{CC} = V_{DD} \cdot \dfrac{R_1}{R_1 + R_2} - I_L(R_1 // R_2), & \text{with load} \end{cases}$$

Figure 1.1.1: Resistor divider

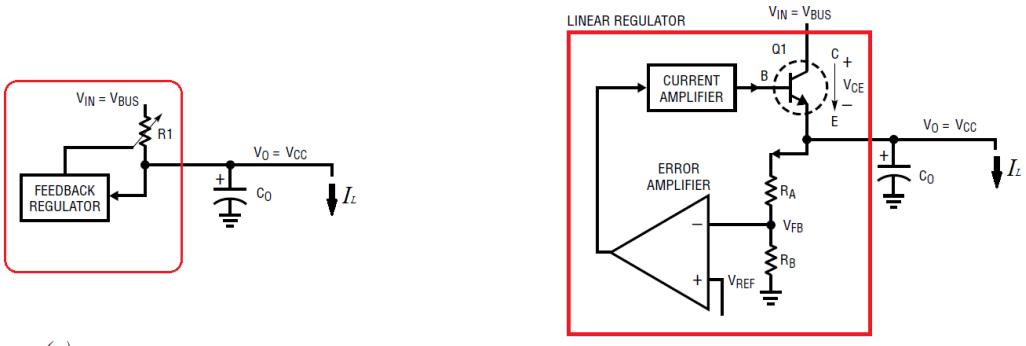


Figure 1.1.2: Variable resistance implementation: conceptual circuit (a); implementation example (b)

Some advantages and disadvantages are here presented:

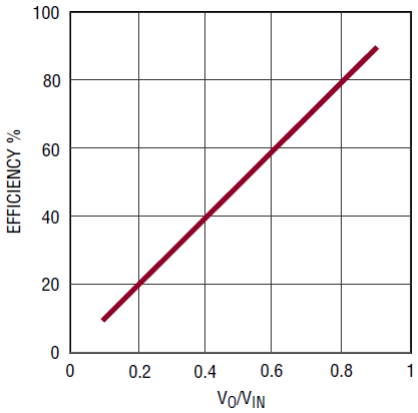
- it can only be used for step-down regulation.
- no galvanic isolation available between input and output of the LR.
- input and output voltages can only have the same polarity.
- this regulator is simple and easy to implement (hence, low-cost), especially for low-power applications, where thermal stress is not critical.
- it produces almost no EMI noise.

- the output voltage ripple is very small.
- it can be implemented in fast-transient applications, since the feedback-loop control bandwidth is larger compared to switching regulators.
- current-sharing concept can be implemented to increase power handling.

The most critical issue is related to efficiency. The main power loss comes from the resistive behavior of the transistor: $P_{LOSS} \approx (V_{in} - V_O) \cdot I_O$ (assuming negligible power losses of the control circuitry).

Hence the efficiency is

$$\eta_{LR} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{LOSS}} \approx \frac{V_O \cdot I_O}{V_O \cdot I_O + (V_{in} - V_O) \cdot I_O} = \frac{V_O}{V_{in}}$$



It means that the transistor have to be thermally designed for the worst case, which means the largest dropout ($V_{do} = V_{in} - V_O$) possible, and maximum load.

In applications where the input voltage is close to the output, the standard LR is no the best solution: in order to further increase the efficiency a low-dropout solution is needed (LDO).

1.2 Switching Mode Power Supply (SMPS)

Instead of using transistors as variable resistors, in this type of converters, they are used as switches: when conducting, the gate voltage is fixed and high enough to keep the on-resistance of the active device very low. This way, the voltage drop across

it remains small, even if the current it has to sustain is very high. This allows for improved efficiency, because the active devices dissipate much less power.

In Figure 1.2.1 is presented the elementary topology of a buck converter, together with the typical set of waveform (assuming square wave control):

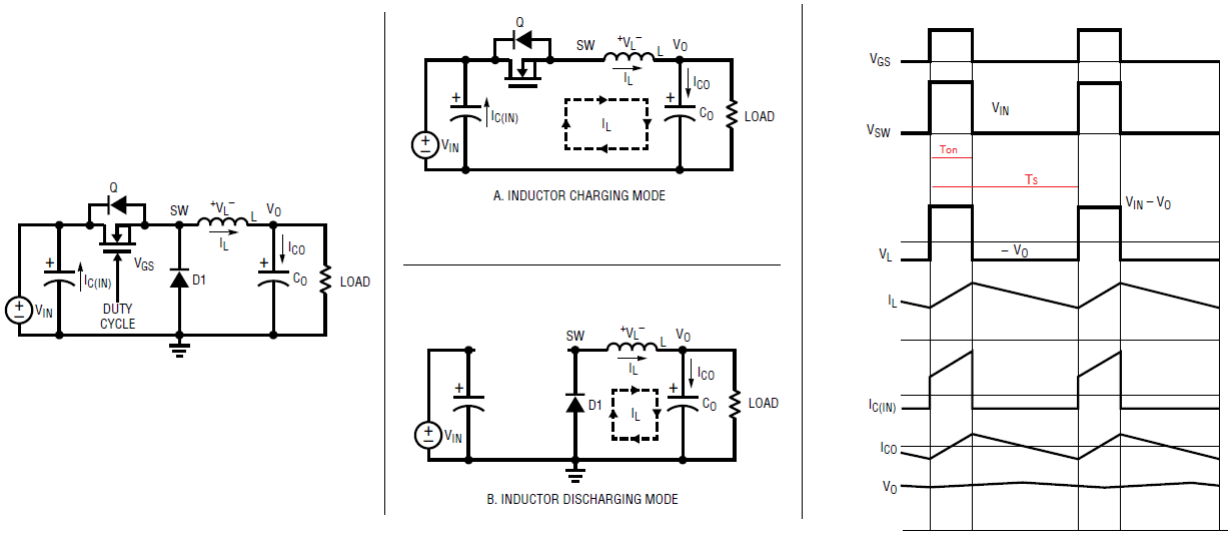


Figure 1.2.1: SMPS buck basic topology

Some features of this type of converter are presented:

- high efficiency, due to having transistors driven as switches

$$\eta_{SMPS} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{LOSS}}$$

  In this type of converter the losses that have to be taken into account are:

  - *conduction losses* of the switch, of the free-wheeling diode and of the parasitic resistance of the wire.

    Note that if the conduction losses of the diode are much larger that the switch conduction losses, a synchronous solution can be applied (Figure 1.2.2). Losses due to the body-diode conducting in the dead-times are still present, in synchronous converters.

  - *switching losses* of the transistor(s), including also gate-driving losses.

  - losses of the control circuit

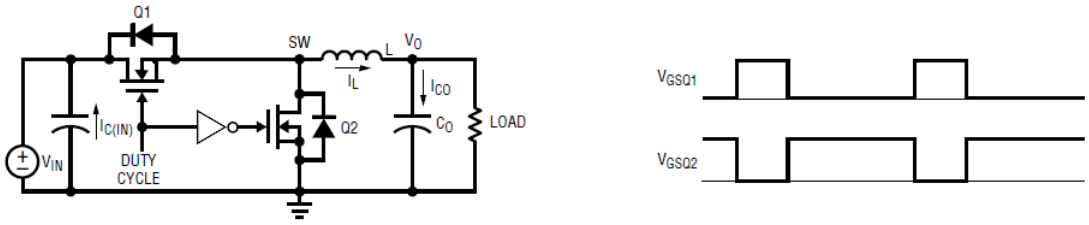


Figure 1.2.2: synchronous buck topology and its gate driving control signals

- galvanic isolation between input and output is available for more advanced topologies (input and output voltage may have different polarity.
- noisy waveform due to the high frequency switching action (EMI issues).
- slower transient response compared to LR.
- always need magnetic components for high frequency. Nevertheless, it is usually a less expensive solution compared to LR.
- not as easy to design as LR regulator.

1.3 Switched-Capacitor Converter (SCC)

Switched-capacitor converters (hereafter *SCC* either for singular or plural), are converters made only of switches and capacitors. According to how the switches are driven, different topologies sequentially come in succession in a cyclic way, in order to provide a specific voltage conversion ratio. In order to sharply increase the conversion ratio, different stages can be cascaded (with reduced efficiency).

Switched-capacitor converters have always been used in commercial applications mainly as charge pumps, providing fixed voltage transformation (halving, doubling, inverting...). They are still implemented for re-programmable memories (*e.g.*, for FLASH memories), and for level shifting (*e.g.*, for the RS232 standard, high-side MOSFET gate driving, etc.).

Many topologies of switched-capacitor voltage transformers are available, to step-up, step-down the voltage; unfortunately, most of them can only be implemented for low power applications, since efficiency easily drops as the load current significantly

increases (especially for regulated converters, because, as it will be explained in following chapters, the conversion ratio is no use to trim it, since the converter is very lightly sensitive to duty ratio variations). Typically they are just used for voltage transformation, but some converters have been also developed in order to provide tight voltage regulation, for small loads. Some ready-to-buy devices are available such as MAX5008. As it can be seen in the following instances, the efficient operating region is limited to low load operation.

MAX5008

This device [24] is a regulated charge pump, which provides 5 V at the output.

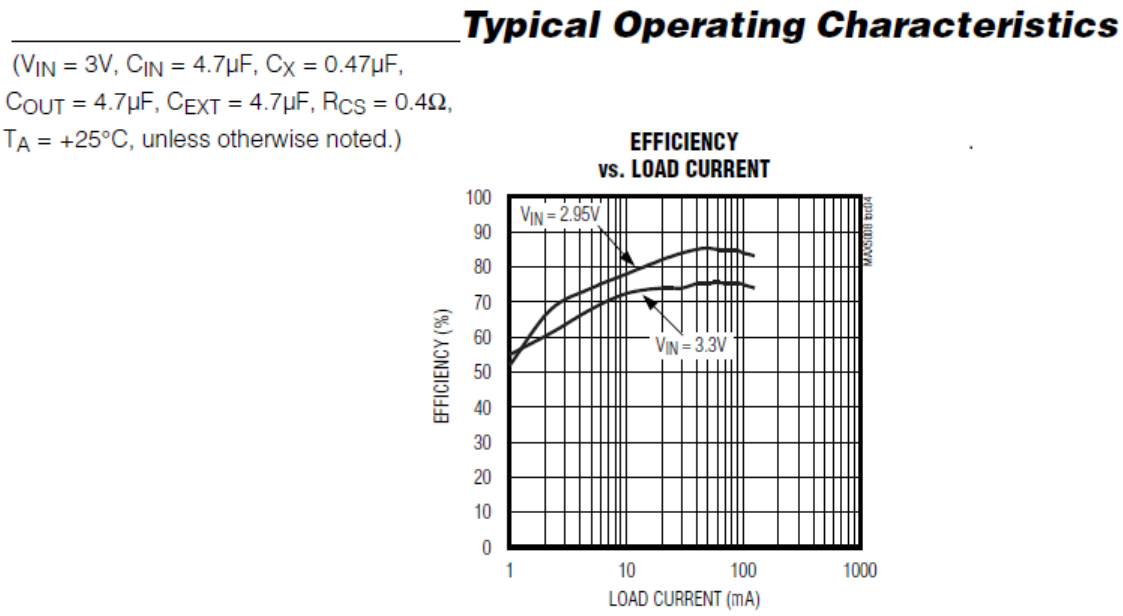


Figure 1.3.1: Efficiency compared to load variations

1.4 High Power Applications

In literature are available some SCC topologies implemented with discrete components, to improve power handling. In such applications, the SCC cannot be directly regulated, because otherwise the low efficiency regime may lead to severe reliability and failure problem, due to high power internal dissipation of the converter.

1.4.1 Discrete Converter - Exponential SCC

The work presented in [8], [9] and [10] is based on a two-stage converter. This type of converter is composed of a first stage SCC, followed by a second-stage buck converter (Figure 1.4.1).

The first stage behaves as a voltage transformer (step-down transformation), while the cascaded buck converter is assumed to work mainly as a voltage regulator. Keeping separated voltage transformation and voltage regulation, the overall system can be seen as a whole buck converter with improved characteristics.

High-voltage-gain can be achieved depending on how many sub-structures are implemented (each of them performs a 2-to-1 voltage transformation).

This solution is well suited in applications where voltage isolation is not needed, and an inductive transformer is a more expensive solution compared to capacitive transformer.

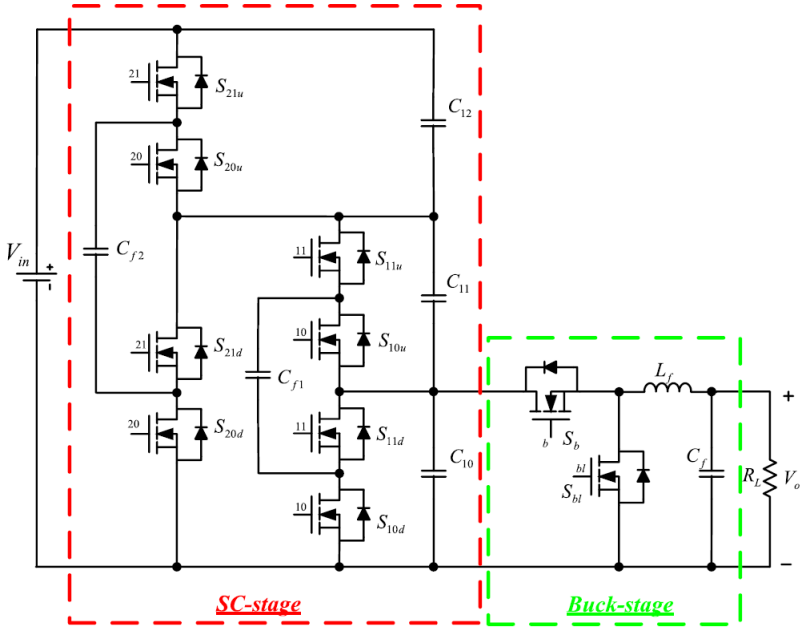


Figure 1.4.1: Topology of the two-stage second-order ESC converter

The SCC stage is composed by cascaded elementary cells. The operating states of each cell are shown in Figure 1.4.2.

Each single cell provides a 2-to-1 voltage ratio. In order to correctly control the switches, the control signals must be shifted in time depending on the number of

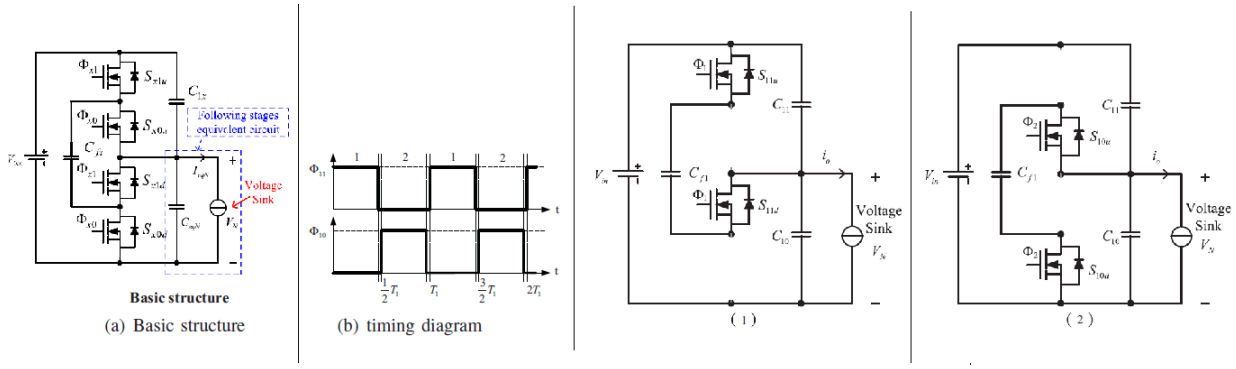


Figure 1.4.2: ESC basic cell switching states

cascaded cells, as shown in the timing diagram in Figure 1.4.3. However, the duty ratio of each elementary cell still remains the same (50% in this case).

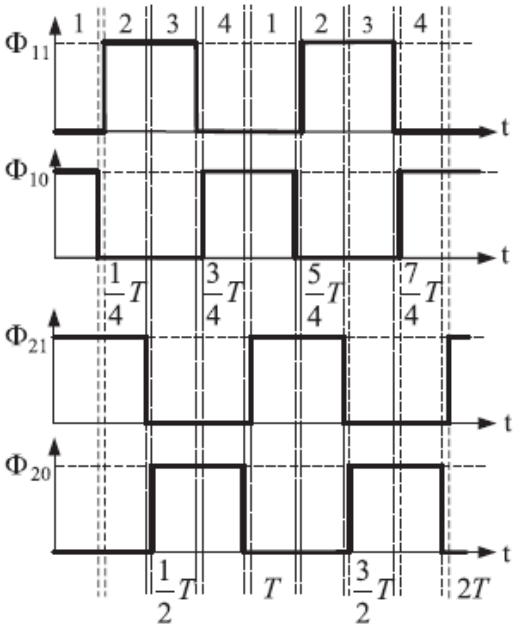


Figure 1.4.3: Timing diagram of the SC stage

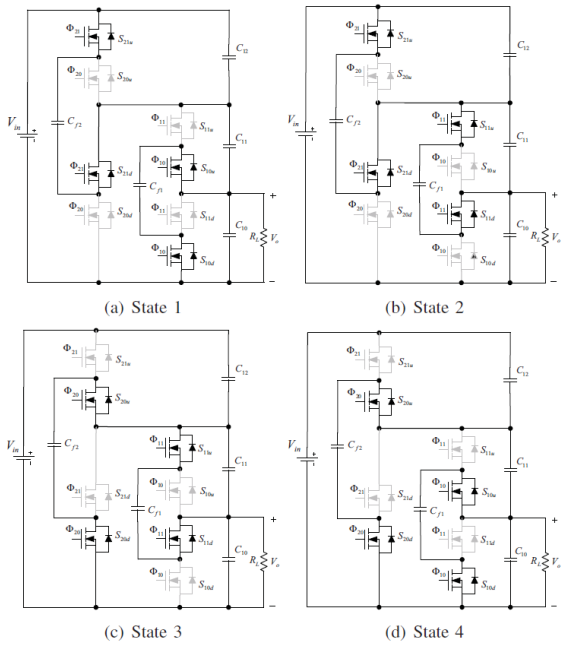


Figure 1.4.4: Clocked Topologies

Here are two different buck converters characteristics, along with their datasheet efficiency graphs:

\ \ \	IR3820	MAX8655
V_{in}	2.5 V - 21 V	4.5 V - 25 V
V_o	1.8 V	1.2 V
f_s	300 kHz	400 kHz
L_f	1.7 µH	0.82 µH
C_f	47 µF (2X)	47 µF (4X)

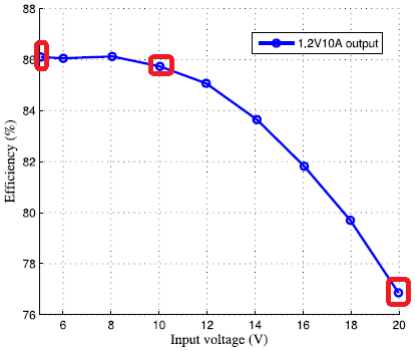


Figure 1.4.5: MAX8655 efficiency versus Vin, at Pout 12 W

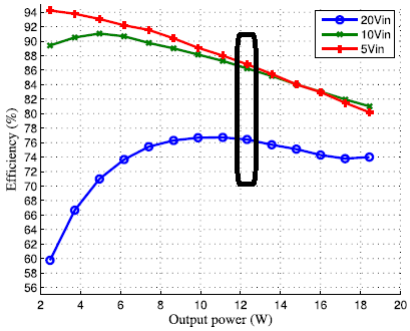


Figure 1.4.6: MAX8655 efficiency versus Pout

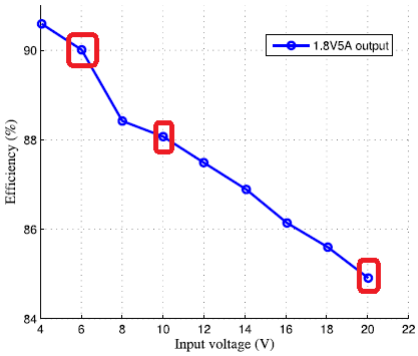


Figure 1.4.7: IR3820 efficiency versus Vin, at Pout 9 W

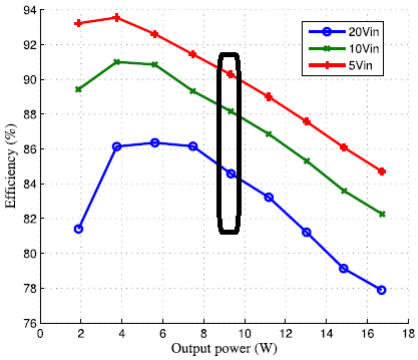


Figure 1.4.8: IR3820 efficiency versus Pout

Table 1.1: design parameters

\ \ \	first order	second order
switches	NTMFS4897NF	NTMFS4897NF
C_{10}	47 µF (x1)	47 µF (x1)
C_{11}	47 µF (x1)	47 µF (x1)
C_{12}	NA	47 µF (x1)
C_{f1}	47 µF (x6)	47 µF (x6)
C_{f2}	NA	47 µF (x6)

Two different SCC have been used as first stage. The parameters of the ESC converters implemented are listed in Table 1.1, and the results of the experiments are reported in Figure 1.4.9 to 1.4.12.

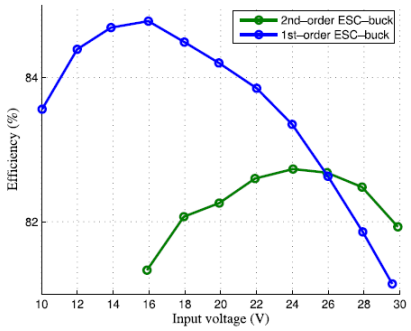


Figure 1.4.9: ESC and MAX8655 efficiency versus Vin

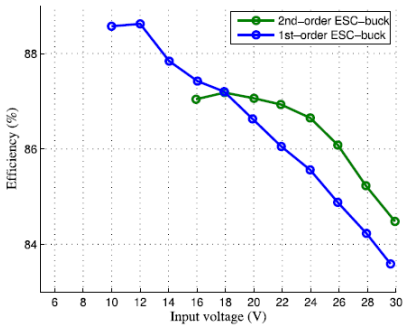


Figure 1.4.10: ESC and IR3820 efficiency versus Vin

Diagrams shows that a high voltage gain efficient conversion can be achieved over a wide power range. The higher efficiency obtained compared to the single-stage buck converter, validates the use of SCC as a high-voltage-gain first-stage. Moreover, the equivalent input range of the two-stage converter is enlarged.

Since the unregulated SCC is used just as voltage transformer, its output voltage is self-adjusted, following the input voltage variations, and to different loading conditions.

It can be noticed that, as power increases, the efficiency trend mostly depends on the one of the buck converter. This is due to the power level the SCC and the buck

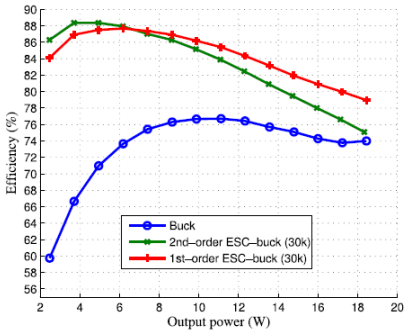


Figure 1.4.11: MAX8655 efficiency versus Pout, at Vin 20 V

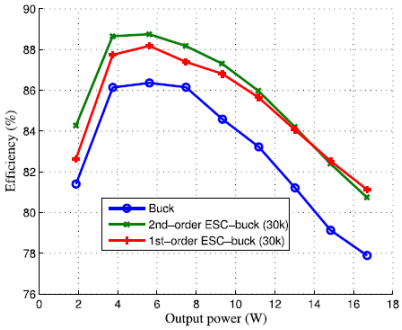


Figure 1.4.12: IR3820 efficiency versus Pout, at Vin 20 V

converter are designed for.

This was the first work to be analyzed. Even if the power level is high, compared to ready-to-buy devices, the search for higher power implementations led to the projects presented in the following sections.

1.4.2 Multilevel SCC

The following topology is an improvement of the one in [14]-[15], and it refers to the work presented in [12]-[13].

In this instance, the SCC is designed to be the interface between the 42 V electric power bus and the 14 V bus in an automotive environment. The power level the converter is designed for is 1 kW. The main purpose is to provide energy coming from the alternator, to recharge the battery in addition to supply high-voltage loads.

The design parameters and the experimental results are reported.

By means of very big capacitors, they were able to achieve very high efficiency even at very high power with a relatively high-voltage-gain and with a quite low switching frequency (compared to typical SMPS solutions).

The components implemented are aluminum electrolytic through-hole capacitors; hence, they are bulky.

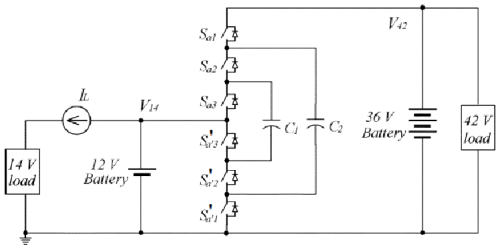


Figure 1.4.13: 4-level topology

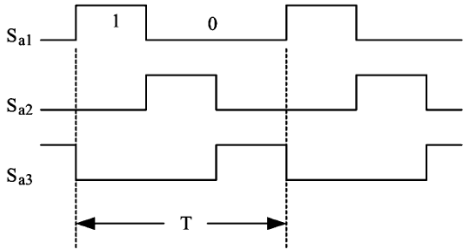


Figure 1.4.14: timing of the 4-level converter

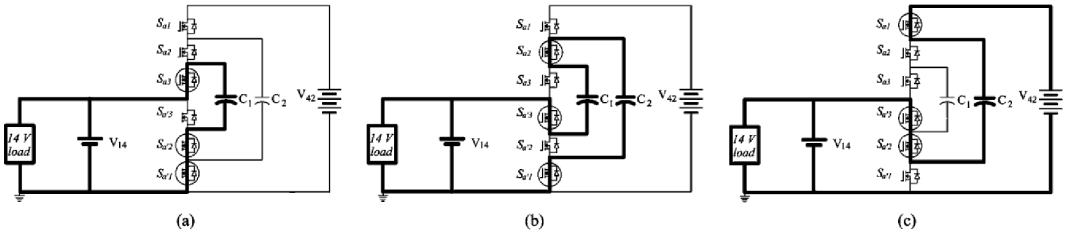


Figure 1.4.15: clocked topologies

Table 1.2: design parameters

Power level	1 kW
V_{in}	43.2 V
transformation ratio	1:3
f_s	5 kHz
switches	30 V, 2.8 mΩ/5 = 0.56 mΩ (5 X)
C_1	3300 µF electrolytic, $ESR = 7\,\text{m}\Omega$ (10 X)
C_2	2200 µF electrolytic, $ESR = 12\,\text{m}\Omega$ (10 X)

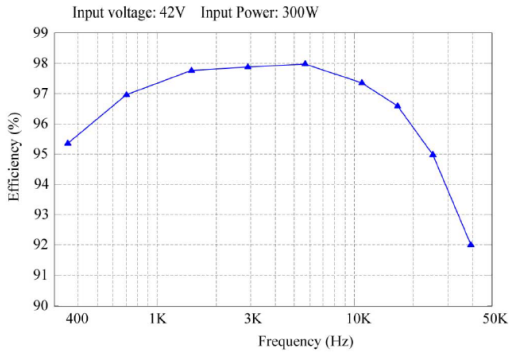


Figure 1.4.16: efficiency versus switching frequency

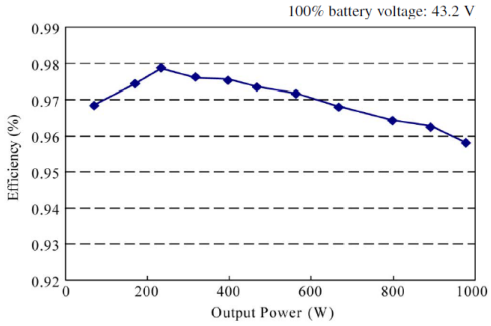


Figure 1.4.17: efficiency versus output power

CHAPTER 2

Practical rules in designing SCCs

In the previous chapter it is just given for granted that SCCs usually work with fixed conversion ratio, and that they are rarely regulated, especially for high power applications. In this chapter, an introduction about the basic design rules and working conditions that allow to design a highly efficient SCC. What is described in this chapter is a detailed description of what is presented in [3] (refer also to Appendix A for what concerns mathematical developments).

In the following analysis, simple charging/discharging situations are analyzed, that may appear in any switched-capacitor circuit, in order to have some basic principles to refer to.

It is worth recall that in this type of power converters, the topology contains only power switches and flying capacitors (*i.e.*, capacitors with at least one node floating, connected to switches). Moreover, the converter switches cyclically topology; hence, in order to evaluate the efficiency, the average power per cycle is taken into account:

$$\eta = \frac{\overline{P_{out}}}{\overline{P_{in}}} = \frac{\frac{1}{T} \cdot \int_{t_0}^{t_0+T} v_{out} \cdot i_{out}\, dt}{\frac{1}{T} \cdot \int_{t_0}^{t_0+T} v_{in} \cdot i_{in}\, dt} = \frac{\Delta E_{out}}{\Delta E_{in}}$$

being T the time interval in which the energy transfer occurs.

2.1 Charging a Capacitor from a Voltage Source

Focusing on charging a capacitor from a voltage source, an equivalent RC circuit can be identified, as shown in Figure 2.1.1).

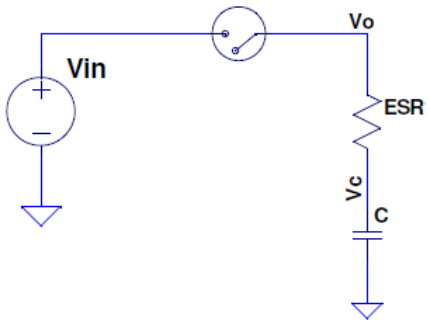


Figure 2.1.1: Charging a capacitor from a voltage source

Assuming R_{ch} to be the total resistance along the charging path, hence the sum of all the different contributions: $R_{ch} = R_{ESR} + R_{ds,on} + R_{loss}$, which are respectively the equivalent series resistance of the capacitor, the resistance model of the device which implements the switch, and parasitic resistance of interconnects.

Assuming the capacitor to be already charged with a voltage V_{Ci}, and the input voltage to be $V_{in} > V_{Ci}$, the efficiency of the capacitor charging process is (refer to Appendix A.1)

$$\eta_{ch} = \frac{1}{2}\left(\frac{V_{Ci} + V_{Cf}}{V_{in}}\right) = \frac{\overline{V_C}}{V_{in}} = 1 - \frac{1}{2V_{in}} \cdot [(V_{in} - V_{Cf}) + (V_{in} - V_{Ci})]$$

where V_{Cf} is the final voltage across the capacitance.

If $V_{Ci} = 0$, $V_{in} > 0$: the maximum efficiency achievable is 50%, only if the charging process is completed ($V_{Cf} = V_{in}$).

To achieve the highest possible efficiency, the capacitor have to work with V_{Ci} as close to V_{in} as possible.

To assess this theoretical result, a simulation has been run. In Figure 2.1.2, two different conditions are simulated.

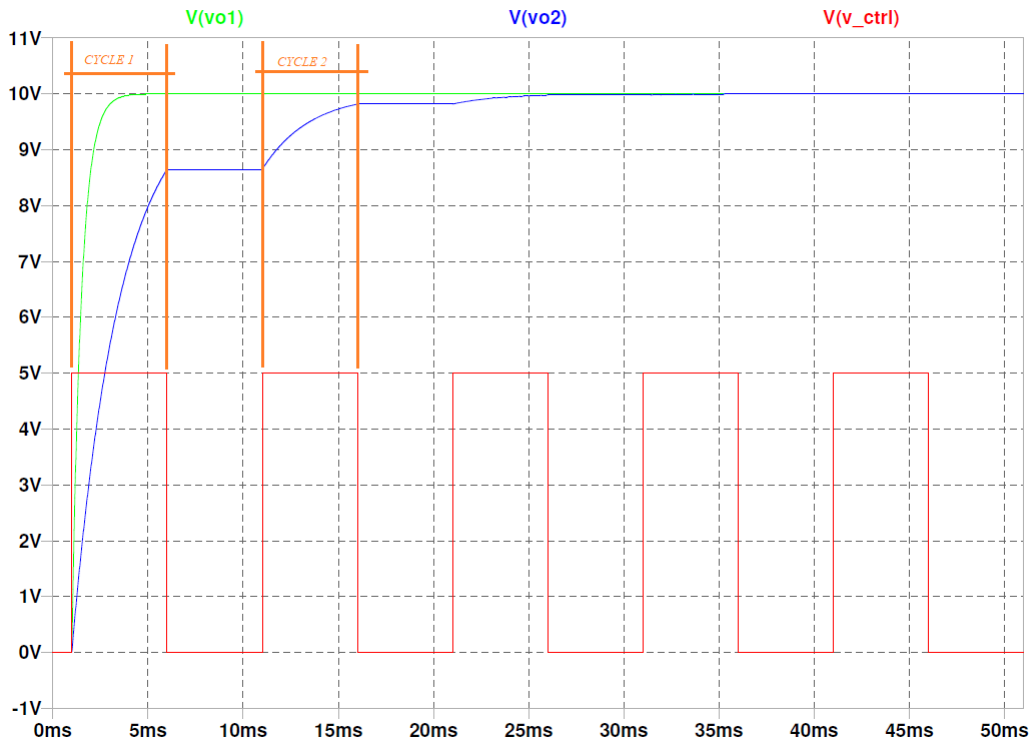


Figure 2.1.2: Green: $R_{on} = 5\,\text{m}\Omega$. Blue: $R_{on} = 25\,\text{m}\Omega$

Simulated data have been compared with the expectations. The analysis results are reported in Figure 2.1.3.

The parameter *'efficiency tot'* represents the efficiency of the charging process extracted from simulation, while *'expected efficiency tot'* is the efficiency from the model mentioned above. As it can be seen, the model suits well the simulation results:

- first let's evaluate the whole simulation period. Both conditions start with the capacitors completely discharged. Since both are charged from the same voltage source, and they are completely charged (being the simulation time large enough, compared to the time constants), the efficiency is 50%.
- focusing only on the first charging cycle, the different time constants of the two circuits make the final voltage to be different. The circuit with the lowest time constant charges faster, hence its final voltage will higher, hence, its efficiency.
- in the second charging cycle, the two capacitors start from a different voltage;

```
Vin =  10.00 V

  C =  0.100 mF
ESR =  10.00 mOhm

Ron1 =  5.00 Ohm
Ron2 =  25.00 Ohm
```

	@	Ron x1	Ron x5
Whole simulation period:			
	efficiency tot --	50.09%	50.02%
	(Vc0+Vcf)/2 --	5.000V	5.000V
	expected efficiency tot --	50.00%	50.00%
1st cycle			
	efficiency tot --	50.09%	43.25%
	(Vc0+Vcf)/2 --	5.000V	4.322V
	expected efficiency tot --	50.00%	43.22%
2nd cycle			
	efficiency tot --	100.00%	92.31%
	(Vc0+Vcf)/2 --	10.000V	9.230V
	expected efficiency tot --	100.00%	92.30%

Figure 2.1.3: simulation and expected results

indeed, the efficiency of the charging process of the two circuits is higher compared to the previous cases.

2.2 Charge Balance - Charging a Capacitor with Capacitors

Another common situation is when two parallel capacitors exchange energy, in order to balance the voltage drop across them.

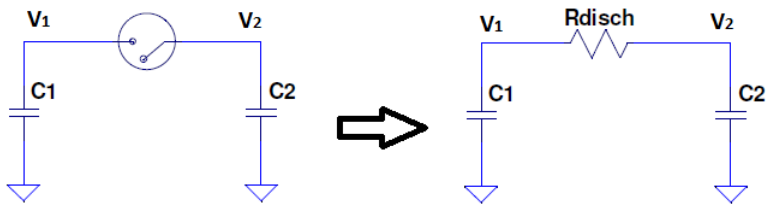


Figure 2.2.1: Charge balance between capacitors

Assuming $V_{C1,0}$ and $V_{C2,0}$ to be the initial voltage of the capacitors (before closing the switch), and

$$\begin{cases} C_1 = C \\ C_2 = x \cdot C \end{cases} \qquad \begin{cases} V_{1,i} = V \\ V_{2,i} = y \cdot V \end{cases}$$

the final voltage V_{QB}, assuming to wait for the complete transient to expire, can be derived from the charge conservation, before and after closing the switch

$$C_1V_1 + C_2V_2 \quad = \quad Q_i = Q_f \quad = \quad V_{QB}(C_1 + C_2)$$

$$V_{QB} = V \cdot \frac{1 + xy}{1 + x}$$

The efficiency must take into account how much energy is delivered to the low-voltage capacitor compared to how much energy the high-voltage capacitor must supply. Assuming $V_{f1} = V_{f2} = V_{QB}$:

$$\eta_{QB} = \frac{\Delta E_2}{\Delta E_1} = \frac{E_{2,f} - E_{2,i}}{E_{1,f} - E_{1,i}} = \frac{\frac{C_2}{2}(V_{f2}^2 - V_2^2)}{\frac{C_1}{2}(V_{f1}^2 - V_1^2)} = \frac{1 + y + 2xy}{2 + x + xy}$$

(in Appendix A.2.1 the computations are developed)

A simulation is presented in Figure 2.2.2. Refer to the table in Figure 2.2.3 for the simulation parameters. the expected efficiency actually is $\eta_{QB} \approx 0.81$.

A comparison of the expect efficiency and the one computed from simulation is presented in Figure 2.2.4.

From the results, presented in this section and in the previous one, it is possible to claim that high efficiency can be achieved if capacitor voltage ripples, in a SCC working at steady-state, are kept as small as possible; hence capacitors have to work around a certain fixed voltage.

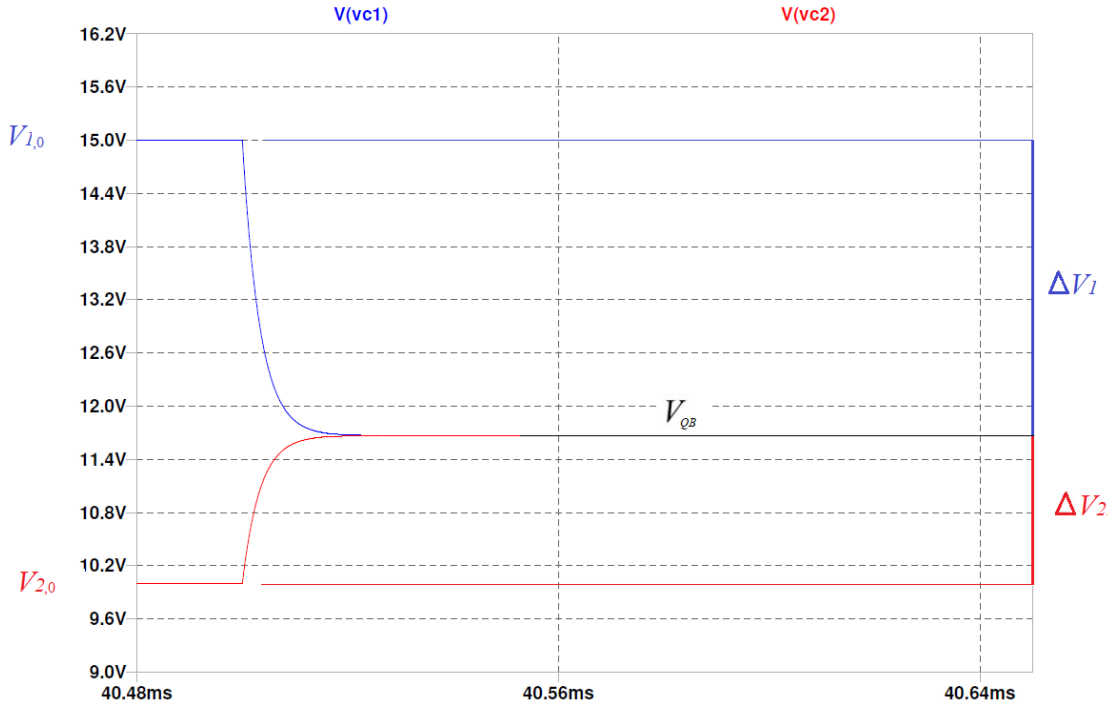


Figure 2.2.2: Charge balance process

$V_{C1,0}$	15 V
$V_{C2,0}$	10 V
y	$\frac{2}{3}$
C_1	500 µF
C_2	1000 µF
x	2
R_{on}	10 mΩ

Figure 2.2.3

```
          Cin =  0.500 mF
         Cout =  1.000 mF
 starting Vin =  15.00 V
starting Vout =  10.00 V

    simulated efficiency --  81.15%

     expected efficiency --  81.25%
```

Figure 2.2.4

2.3 How the Load Affects the Efficiency of an SCC

How the components and the characteristics of the SCC affect the efficiency at different power levels, will be better discussed in next Chapter. For now, resorting to a 1-to-1 SCC, the following analysis is focused on evaluating the working condition when a current sinking load (modeled as a resistor) needs to receive power.

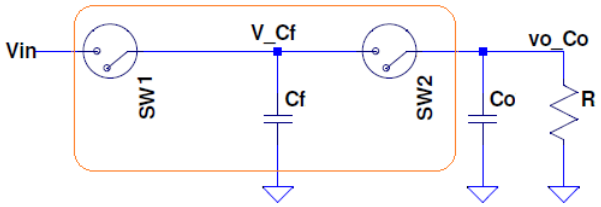


Figure 2.3.1: 1-to-1 SCC

It is worth notice that the topology in Figure 2.3.1, is used in integrated circuits to emulate the behavior of a variable resistor, controlled by the switching frequency: $R_f = \frac{1}{f_{sw} C_f}$. In next chapters a similar way to model the converter will be presented, in order to carry out the design.

Being SW_1 and SW_2 driven by two complementary signals, the flying capacitor C_f is connected to the input in one switching phase, to recharge itself, and, in the other switching phase, it refreshes lost charges by C_O to supply the load (modeled with a resistor R).

The steady-state behavior of the system is shown in Figure 2.3.2.

The circuit simulation parameters are listed in Table 2.1.

In the charging phase (T_{ch}), the lost charges of C_f are restored, while capacitor C_o supplies the current to the load.

In the discharging phase, two phenomena occur:

- a first time interval (T_{QB}), in which the dominant process is the charge balance between the two capacitors: C_f provides both the charge to C_o and the current to supply the load.

- when the previous process stops, a new process starts (in T_{disch}): capacitor C_o current changes (instant identified by $I_{Co} = 0$, when V_o is flat), so that both C_f

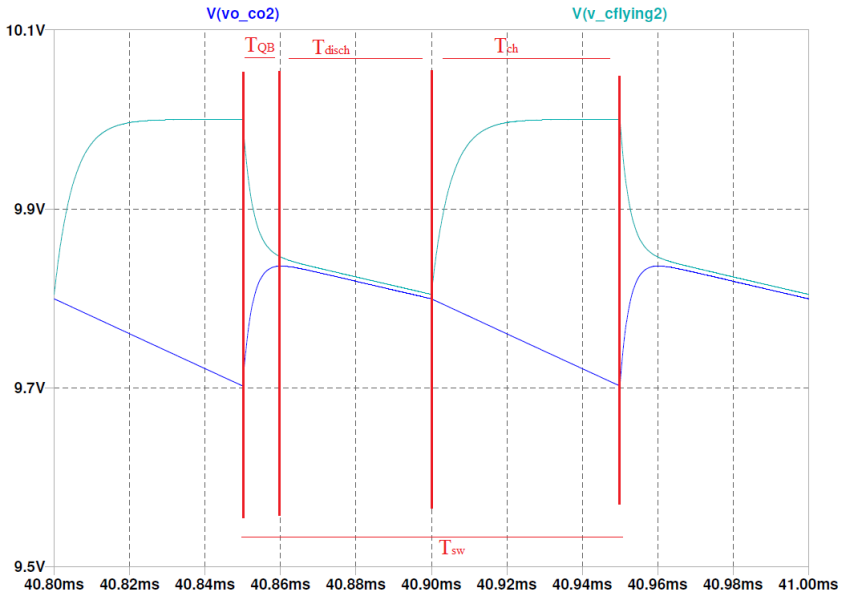


Figure 2.3.2: 1-to-1 SCC, time behavior

Table 2.1: Simulation parameters

V_{in}	10 V
transformation ratio	1:1
f_s	10 kHz
C_f	500 µF
C_o	500 µF
R_{on}	10 mΩ

and C_o supply current to the load.

2.4 SCC Duty Ratio Sensitivity

The fact that SCC are not much affected by duty ratio variations is conceptually due to the fact that the charge/discharge of the capacitors is much faster than the switching occurences, which means that the transient expires very fast, reaching the balance voltage. A mathematical proof of the small sensitivity is given in [7].

The general method to resort to for the analysis of any switching regulator is the one in [1] (also known as the Middlebrook *State-Space Average Method*), which is the most complete analysis to determine what are the parameters that affect the input-output relationship, from which the sensitivity with respect to a particular parameter can be further computed.

Some different control methods have been developed (refer to [19]-[20]), but they may imply a significant loss in efficiency; hence, for practical purposes related to maximum power dissipation, they may only be applied to low-power applications:

- variable frequency:

  this technique modify the equivalent output resistance of the SCC by trimming the switching frequency instead of the duty ratio. The reason why it works will be clear from next chapter. For now, it is just worth notice that if the switching frequency decreases, the voltage decay of each capacitor in a cycle increases, because the switching period increases; so, resorting to what has been described in this chapter, the efficiency decreases. As a result, the power level this technique can be applied to is very low.

  This method may reveal itself quite useful when the power consumption varies, to implement an adaptive switching frequency related to the load absorption.

- adjustable conversion ratio:

  this technique is a sort of *forward control* in conventional switching topologies. Input voltage regulation may be available if self-adjustable conversion ratio can be implemented.

The most significant issue is the fact that the possible conversion ratios can just be a finite set. Hence, this technique is accurate only if the input voltage is not so high: for instance, if a 42 V to 14 V conversion is needed (*i.e.*, 6-to-2); but, assuming the voltage may increase up to 49 V, in order to keep 14 V at the output a 7-to-2 conversion ratio is needed. Instead, assuming a 5 V to 3.3 V conversion is needed, and the voltage may rise up to 6 V, even if the conversion is not precise, the error at the output may be negligible.

The discretization may not be trimmed at will with a specific resolution, unless a large device with any components is implemented. This is typically why a regulator is needed together with the SCC.

It is worth also notice that the control may not be trivial: there is the need for a topology with many switches, that allows to change driving sequence at will, to change the conversion ratio at runtime. Many switches, leads to decreased performances. The most convenient way to drive it is by creating more than one point of load, each a different voltage, and connect the load to the desired voltage.

For integrated devices (hence low-medium power applications), also some combinations of the two can be implemented without resorting to an extra regulator at the output; this because the efficiency drop, does not imply high power dissipation. For instance, assuming 10 W are required at the output, and assuming the efficiency is kept above 80%, then the input power will be approximately 12.5 W, which means approximately 3 W of power dissipation losses, and that may be acceptable or not depending on heat-sinks, etc.

CHAPTER 3

Efficiency Analysis and Design of SCCs

The previous analysis is not meant for practical use, but just to introduce the problem to be faced and to understand the working conditions. In this chapter, some available methods are presented in order to:

- define maximum performance of SCCs (conversion ratio and efficiency)
- determine the overall losses contribution of an SCC
- select the components that suit best for the SCC performances

Starting from an equivalent model of the SCC, a method to determine the parameters of the model is computed with respect to the switching frequency. Therefore, from the parameters, the equations to size the components are derived.

3.1 Ideal Behavior of SCCs

Refering to [5], we can model the SC converter as a transformer with an output resistance.

Assuming to work without a load, the ideal transformation ratio can be defined by inspection of the different clocked topologies the converter goes through; this because the steady-state capacitor voltages are dc only under no-load condition.

$$\begin{cases} M = Vo/V_{in} \\ R_L \to \infty, \text{ which practically means } I_o \to 0 \end{cases}$$

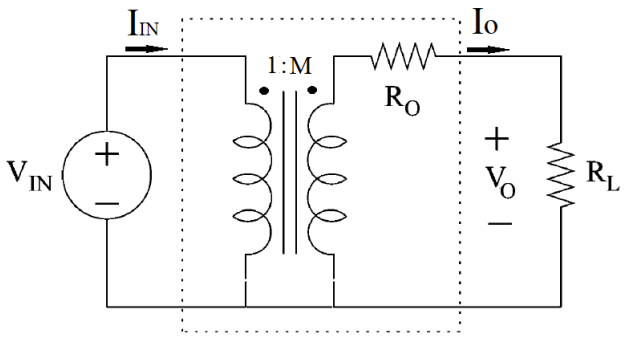


Figure 3.1.1: switched-capacitor converter equivalent model

Now, the maximum achievable efficiency can be defined as

$$\eta = \frac{V_o}{V_{in}}\frac{I_o}{I_{in}} = \frac{V_o}{V_{in}}\frac{1}{M} = \frac{MV_{in}\cdot\frac{R_L}{R_L+R_o}}{V_{in}}\cdot\frac{1}{M} = \frac{1}{1+\frac{R_o}{R_L}}$$

(*note that the parameters refer to time-averaged values*)

It is worth notice that R_o is never null, even if assuming ideal components with no parasitic elements (capacitor ESR, parasitic inductance and resistance of the leads, and switch on-resistance null). This because capacitors are periodically charged/discharged, in order to supply the output current to the load; which means that capacitor voltages have an ac-ripple component. As already stated in chapter 2, one way to reduce charge balance is to increase the switching frequency: the time interval in which capacitors discharge on the load is reduced. In next section, some further observations are pointed out.

3.2 Efficiency and Switching Frequency Limits

If the load is modeled as a current sinker, and the SCC with a Thevenin equivalent circuit, the efficiency can be derived as

$$\eta = \frac{V_o}{M\cdot V_{in}}\frac{I_o}{I_o} = \frac{M\cdot V_{in}-V_{Ro}}{M\cdot V_{in}} = 1-\frac{V_{Ro}}{M\cdot V_{in}} = 1-\frac{R_o}{M\cdot V_{in}}I_o$$

It can be noticed that, as load power increases (*i.e.*, I_o increases), efficiency decreases. Hence it is important to be able to determine R_o, depending on circuit parameters.

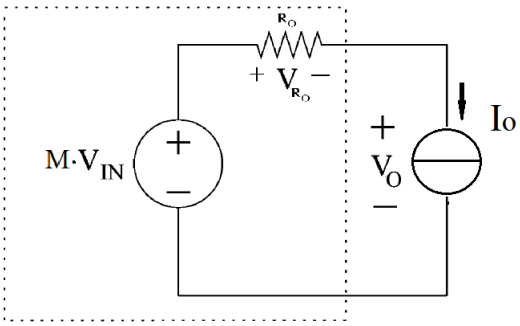


Figure 3.2.1: Thevenin model of the SCC

For this purpose, it is possible to refer to what was previously stated in section 2, when talking about charge balance between capacitors: the smaller the ripple across capacitors, the smaller the losses. In order to do so, one possible way is to increase the switching frequency: all the capacitors in the converter are affected at the same time, because the time interval in which the capacitors discharge to the load is reduced, hence the voltage decay across capacitors is reduced.

Simulation and eperimental results lead to the behavior showed below ([19]):

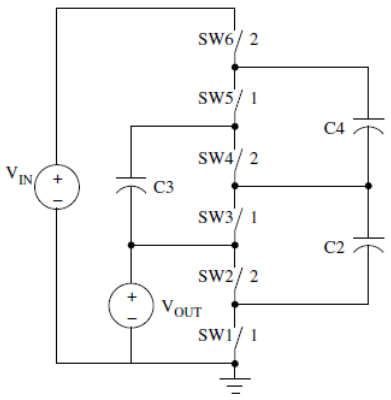


Figure 3.2.2: four-stage ladder converter

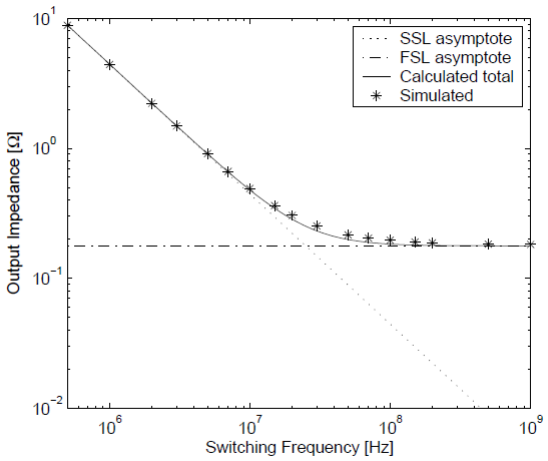


Figure 3.2.3: converter impedance versus switching frequency

It can be seen that in the first frequency range we have a behavior of $-20\,\mathrm{dB}$ per decade, which means that R_{eq} is inversely proportional to f_{sw}. Then, from a certain frequency on, the value saturates and stops decreasing.

Namely, the two different behavior are called *slow switching limit* (SSL), and *fast switching limit* (FSL).

$\underline{R_{eq,SSL}}$ This behavior can be analytically determined assuming all components to be ideal, *i.e.*, neglecting the finite resistances of the switches, capacitors, and interconnect. Power losses are practically determined as charge balance losses between capacitors, which is the main loss contribution (slow switching implies large ripple).

$\underline{R_{eq,FSL}}$ This behavior defines the operating region in which losses of parasitic resistances are dominant: from a certain frequency on, the capacitor voltages are assumed to be constant (very small ripple, hence very small charge balance losses), and the parasitic elements of the circuit are what determines the main power loss.

The expected optimal operating point is at the boundary of the two asymptotic limits, which leads to minimum R_{eq} (maximum efficiency), and minimum f_{sw} (minimum switching losses).

Unfortunately, no model is still available to fairly predict the behavior in between those asymptotic boundaries. That is why, in Figure 3.2.3, the experimental data differs from expectations: the resonance (together with its harmonics), introduced by parasitic inductances, is typically not included in the model, and not taken into account (at least in early steps of the design). Note that for high-power implementations, very high current is flowing in the converter, and the effect of parasitic inductances may be not negligible even at lower frequencies.

In order to achieve an optimal design of SC converters, there is the need of mathematical tools, which allows to perform a meaningful steady-state analysis. There are some available methods that allow for the optimization of a switched-capacitor converter.

- **state-space averaging**: historically the state-space averaging (SSA) method is among the earliest approaches (refer to [1]). It requires the switching frequency to be much higher than input and output variations, and higher than the natural frequencies of the converter. This method is not very useful for designing SC converters, since it does not give too much insight of the different contributions

of the components. But, it still remains an easy method to identify how the voltage gain weakly depends on the duty ratio (as showned in [7]).

- **energy-flow-path**: this method, presented in [10], is supposed to be the most general method to be applied to any SCC. This type of analysis provide deep knowledge of all the paths the energy from the supply flows through, before discharging to the load. This allows to point out which are the most efficient paths, so that the design of the components is performed in such a way that most of the energy flows in the most efficient paths. This method is assumed to provide:
  - clear insight of how the value of each capacitor affects the efficiency at a particular operating condition and switching frequency
  - a way to analyze also bidirectional energy flow within the same switching state of the converter
  - a simpler way to analyze high-order (also called multi-phase, or multilevel) SCCs, having more than two nominal phases
  - insight of how the circuit parameters have to be modified in order to increase the efficiency and performances of the converter

  This method may require a quantitative analysis, which means that deep simulations must be done in order to have meaningful parameters to deal with.

- **output resistance evaluation**: this method (refer to [5]) allows to determine the asymptotic limits of the equivalent output resistance both in the SSL and FSL operating regions as a function of circuit parameters.

  It is a relatively easy method, especially when applied to two-phase converters, and, depending on how deep the analysis is, it can take into account all power loss contributions (charge transitions between capacitors, ESR of capacitors, on-resistance of the switches, gate drive, switching losses, ...). The contribution of each component in the circuit is well defined. The formulas allow for different design optimizations.

In the following sections the last method is illustrated, as well as the design procedure implemented that refers to the parameters identified in the method.

3.3 Equivalent Output Resistance Model

As already seen in the previous chapter, the equivalent output model of the SCC is an ideal transformer with a series resistance at the output.

The equivalent series resistance model exploits all the different losses in the converter: the equivalent series resistance of the capacitors, the on-resistance of the components used as switch, the switching losses, the charge balance losses, the driving losses, the losses coming from the parasitic inductances, and so on. A resistive model for each contribution can be carried out. Hence, each resistance contribution is summed up:

$$R_{out} = R_{ESR} + R_{Ron} + R_{QBalance} + R_{switching} + R_{driver} + R...$$

Referring to the two switching regimes identified in Figure 3.2.3 (namely the SSL and FSL), and recalling that there is a dominant loss in each one, only three contributions have been included in the model, in the design presented in the following chapter: charge balance, because the losses associated to it increase as the switching frequency decreases (the opposite of switch drivers); and parasitic resistances of capacitors and switches, because they are actually in series to the load, ad do not allow the R_{out} to decrease below a certain level.

To apply the analysis and better explain the meaning of the equations and coefficients, the analysis will be performed on a 3-to-1 ladder converter (refer to Figure 3.3.1).

Note that here the analysis of [4] is reported and extended, to better understand what was previously mentioned. In the next chapter this method is applied straightforward to the topology to be designed.

The following equations derived in this chapter are generalized for a converter with $p = \{1, 2, ..., N\}$ phases, $h = \{1, 2, ..., H\}$ capacitors (not including the output one), and $k = \{1, 2, ..., K\}$ switches.

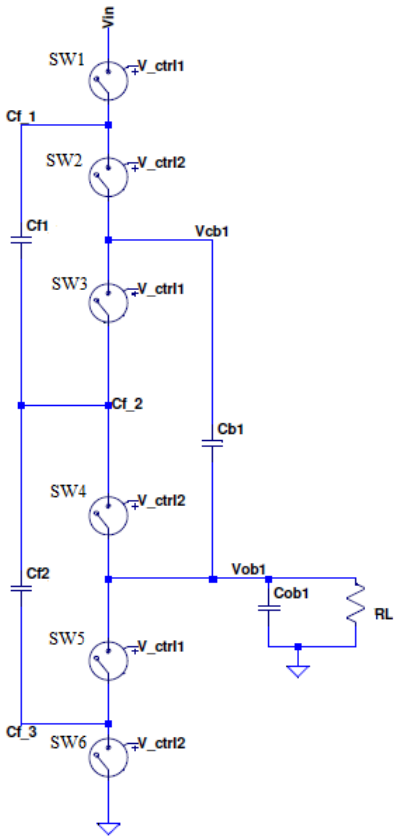


Figure 3.3.1: 3-to-1 ladder converter

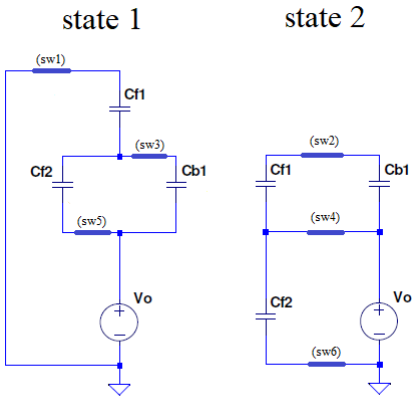


Figure 3.3.2: switching states

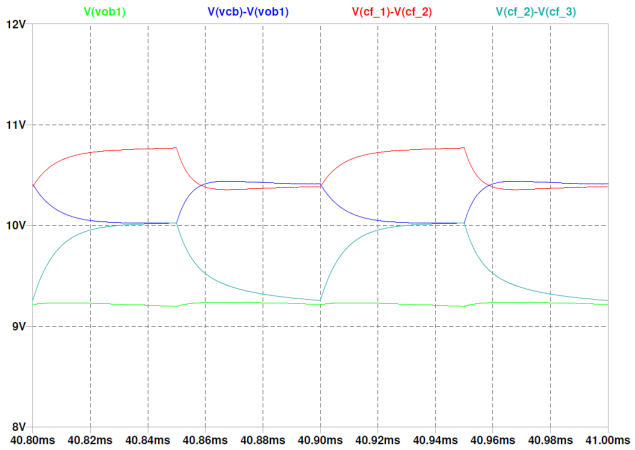


Figure 3.3.3: waveforms

3.3.1 Charge Balance Loss (SSL)

The basic idea to determine the *SSL* resistance is resorting to the theoretical way:

1. turn-off all independent sources
2. substitute the load with an ideal voltage source
3. evaluate the current flowing in the voltage source
4. at this point: $R_{out} = -\dfrac{V_O}{I_O}$

As already claimed in the previous chapter, the *SSL* limit can be computed assuming losses to be dominantly due to charge balance process, neglecting all parasitic resistive losses.

The current flow between input source, output load, and capacitors are assumed to be impulsive, hence, modeled as charge transfers. From this model, depending on how many switching states are needed, the same number of charge multiplier vectors are defined. Those correspond to charge flows occurring right after the switches close at the beginning of each switching cycle. Each element of the vectors is associated to a capacitor, or an independent voltage source, being associated to the charge flow in that component. The vector element are derived by applying the KCL to each sub topology defined by the switches.

$$\mathbf{q}^{(p)} = \begin{bmatrix} q_{out}^{(p)} & q_1^{(p)} & q_2^{(p)} & \dots & q_H^{(p)} \end{bmatrix}^T$$

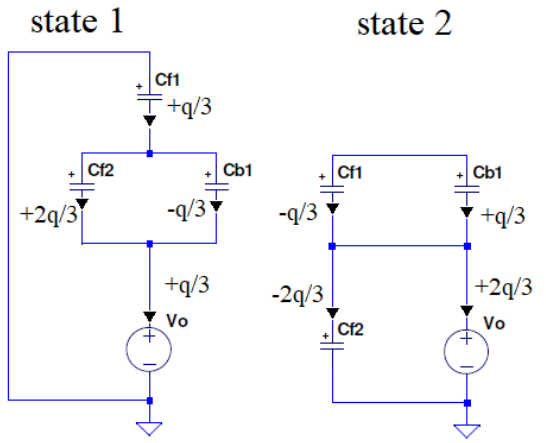
being $p = \{1, 2, ..., N\}$ the number of phases, and H the number of capacitors.

Normalized with respect to $q_{out} = q_{out}^1 + q_{out}^2 + ... + q_{out}^N$

$$\mathbf{a}^{(p)} = \mathbf{q}^{(p)} / q_{out} = \begin{bmatrix} a_{out}^{(p)} & \mathbf{a}_{capacitors}^{(p)} \end{bmatrix}^T$$

The single element is positive or negative depending on the direction of the current flow: in this case, it is positive when flowing into the component.

In the instance above, two states can be defined, as well as two charge vectors. Refer to Figure 3.3.4.



Choosing

$$\mathbf{a}_{capacitors} = [a_{cf2} \quad a_{cf1} \quad a_{cb1}]$$

$$\begin{cases} \mathbf{a}^1 = \left[\frac{1}{3}, \quad \frac{2}{3}, \quad -\frac{1}{3}, \quad \frac{1}{3}\right] \\ \mathbf{a}^2 = \left[\frac{2}{3}, \quad -\frac{2}{3}, \quad \frac{1}{3}, \quad -\frac{1}{3}\right] \end{cases}$$

Figure 3.3.4: 3-to-1 ladder converter charge multiplier elements

Applying KCL to *state 1*:

$$\begin{cases} q_o^{(1)} = q_{f1}^{(1)} \\ q_{f1}^{(1)} = q_{f2}^{(1)} + q_{b1}^{(1)} \end{cases}$$

Applying KCL to *state 2*:

$$\begin{cases} q_o^{(2)} + q_{f2}^{(2)} = 0 \\ q_{f1}^{(2)} + q_{b1}^{(2)} = 0 \end{cases}$$

Some constraints must hold:

1. the sum of all coefficient related to the output must give: $\sum_p^N a_{out}^{(p)} = 1$
2. in each state $a_{out}^{(p)} > 0$
3. since we assume to work at steady-state, the energy exchange is balanced between the switching phases; hence, the sum of all coefficients related to each capacitor must give: $\sum_p^N a_{cap,h}^{(p)} = 0$

Applying the last constraint to the KCLs in both states:

$$\begin{cases} q_{f1}^{(1)} + q_{f1}^{(2)} = 0 \\ q_{f2}^{(1)} + q_{f2}^{(2)} = 0 \\ q_{b1}^{(1)} + q_{b1}^{(2)} = 0 \end{cases}$$

Expressing all equations as functions of $q_{b1}^{(2)} = q$

$$\begin{cases} q_{out} = q_o^{(1)} + q_o^{(2)} = q + 2q = 3q \\ q_{f1}^{(1)} = -q_{f1}^{(2)} = q \\ q_{f2}^{(1)} = -q_{f2}^{(2)} = -2q \\ q_{b1}^{(1)} = -q_{b1}^{(2)} = -q \end{cases}$$

This demonstrates the coefficients in Figure 3.3.4.

At this point, the vectors of the steady-state voltages in each phase have to be introduced:

$$\mathbf{v}^{(p)} = \begin{bmatrix} v_{out}^{(p)} & v_{cf1}^{(p)} & v_{cf2}^{(p)} & v_{cb1}^{(p)} \end{bmatrix}^T$$

Resorting to Tellegen's theorem, the dot product $\mathbf{a}^{(p)} \cdot \mathbf{v}^{(p)}$ can be applied. The power conservation principle introduced by Tellegen's theorem can be extended here to be an energy conservation principle, since we work in a cyclic regime, and we just consider the exchanged energy per switching phase:

$$\Delta E_{c,h}^{(p)} = E_{c,h}^{(p)} = q_{c,h}^{(p)} \cdot v_{c,h}^{(p)}$$

The power conservation principle leads to:

$$\sum_{h}^{H} \left(E_{cap,h}^{(p)} \right) + E_{out}^{(p)} = E_{in}^{(p)}$$

Being $E_{in}^{(p)} = 0$ since all independent input source have been switched off, and extending the previous equation to all switching phases:

$$\sum_{p}^{N} \left[\sum_{h}^{H} \left(E_{cap,h}^{(p)} \right) + E_{out}^{(p)} \right] = 0$$

Exploiting the coefficients:

$$V_{out} \left(q_{out}^{(1)} + q_{out}^{(2)} + ... + q_{out}^{(N)} \right) + \sum_{h}^{H} \left(q_{c,h}^{(1)} V_{c,h}^{(1)} + q_{c,h}^{(2)} V_{c,h}^{(2)} + ... + q_{c,h}^{(N)} V_{c,h}^{(N)} \right) = 0$$

Normalizing everything with respect to q_{out}^2 (being $a_x = \frac{q_x}{q_{out}}$):

$$\frac{V_{out}}{q_{out}} + \frac{1}{q_{out}} \sum_h^H \left(a_{c,h}^{(1)} V_{c,h}^{(1)} + a_{c,h}^{(2)} V_{c,h}^{(2)} + ... + a_{c,h}^{(N)} V_{c,h}^{(N)} \right) = 0$$

From the steady-state constraint, $a_{c,h}^{(N)} = -\sum_p^{N-1} \left(a_{c,h}^{(p)} \right)$

$$\frac{V_{out}}{q_{out}} + \frac{1}{q_{out}} \sum_h^H \left[a_{c,h}^{(1)} \left(V_{c,h}^{(1)} - V_{c,h}^{(N)} \right) + a_{c,h}^{(2)} \left(V_{c,h}^{(2)} - V_{c,h}^{(N)} \right) + ... + a_{c,h}^{(N-1)} \left(V_{c,h}^{(N-1)} - V_{c,h}^{(N)} \right) \right] = 0$$

$$\frac{V_{out}}{q_{out}} + \frac{1}{q_{out}} \sum_h^H \left[-a_{c,h}^{(1)} \Delta V_{c,h}^{(N),(1)} - a_{c,h}^{(2)} \Delta V_{c,h}^{(N),(2)} + ... - a_{c,h}^{(N-1)} \Delta V_{c,h}^{(N),(N-1)} \right] = 0$$

being $\Delta V_{c,h}^{(p2),(p1)}$ the voltage variation between two phase.

It can be better expressed as the voltage variation of consecutive phases: for instance

$$\Delta V_{c,h}^{(3),(1)} = V_{c,h}^{(3)} - V_{c,h}^{(1)} =$$
$$= V_{c,h}^{(3)} - V_{c,h}^{(2)} + V_{c,h}^{(2)} - V_{c,h}^{(1)} =$$
$$= \Delta V_{c,h}^{(3),(2)} + \Delta V_{c,h}^{(2),(1)}$$

The voltage variation of a capacitor in each phase can be expressed resorting to the charge delivered to, or removed from, the capacitor:

$$\Delta V_{c,h}^{(p+1),(p)} = \frac{q_{c,h}^{(p+1)}}{C_h}$$

Hence, rewriting the last equation of the capacitor as

$$\frac{\Delta V_{c,h}^{(p+1),(p)}}{q_{out}} = \frac{a_{c,h}^{(p+1)}}{C_h}$$

it is possible to derive an equation with only simple and known coefficients.

$$\frac{V_{out}}{q_{out}} + \sum_h^H \frac{1}{C_h} \left[-a_{c,h}^{(1)} \left(a_{c,h}^{(2)} + ... + a_{c,h}^{(N)} \right) - a_{c,h}^{(2)} \left(a_{c,h}^{(3)} + ... + a_{c,h}^{(N)} \right) + ... - a_{c,h}^{(N-1)} \left(a_{c,h}^{(N)} \right) \right] = 0$$

Recalling, and applying again, the third constraint $a_{c,h}^{(N)} = -\sum_p^{N-1} \left(a_{c,h}^{(p)} \right)$

$$\frac{V_{out}}{q_{out}} + \sum_h^H \frac{1}{C_h} \left[\sum_{p=1}^{(N-1)} \left(a_{c,h}^{(p)} \sum_{m=p}^{N-1} a_{c,h}^{(m)} \right) \right] = 0$$

Simplifying the equation, a new coefficient can be computed:

$$\frac{V_{out}}{q_{out}} + \sum_{h}^{H} \frac{1}{C_h} \left[A_{c,h}^2\right] = 0$$

At this point the model for R_{SSL} can be derived over a switching cycle:

$$R_{SSL} = \frac{-Vo}{q_{out}/T_{sw}} = \sum_{h}^{H} \frac{1}{f_{sw} C_h} \left[A_{c,h}^2\right]$$

3.3.2 Resistive Losses (FSL)

Either considering the ESR of a capacitor, or the R_{on} of a MOSFET, the equivalent model can be derived the same way.

In this situation, the following assumptions have to be recalled:

1. parasitic resistance losses are assumed to be dominant compared to charge balance losses
2. charge balance losses will be neglected by considering constant the voltage across the capacitors (very small ripple)
3. hence, current flow between capacitors will be constant, too

By defining the current trough a resistive component in a switching phase as:

$$i_{R,k}^{(p)} = \frac{q_{R,k}^{(p)}}{d^{(p)} \cdot Tsw}$$

being $d^{(p)}$ the portion of switching period for the single phase time interval.

Introducing in the formula the q_{out} dependence:

$$i_{R,k}^{(p)} = \frac{q_{R,k}^{(p)}}{d^{(p)} \cdot Tsw} \cdot \frac{q_{out}}{q_{out}} =$$

$$= \frac{1}{d^{(p)}} \cdot \frac{q_{R,k}^{(p)}}{q_{out}} \cdot q_{out} f_{sw} =$$

$$= \frac{a_{R,k}^{(p)}}{d^{(p)}} \cdot i_{out}$$

In the *FSL*, the charge flows must be the same as in the *SSL*. Therefore, the $\mathbf{a}_{R,k}^{(p)}$ coefficient must extracted from the $\mathbf{a}^{(p)}$ coefficients.

The power dissipated in a cycle can be expressed as:

$$P_R = R \cdot d^{(p)} \left(i_{R,k}^{(p)}\right)^2 = R \cdot d^{(p)} \left(\frac{a_{R,k}^{(p)}}{d^{(p)}} \cdot i_{out}\right)^2 = \frac{R}{d^{(p)}} \cdot \left(a_{R,k}^{(p)}\right)^2 i_{out}^2$$

At this point it is necessary to put in evidence the fact that:

$$R_{FSL} = R_{FSL,ESR} + R_{FSL,R_{on}}$$

each sub-contribution will be analyzed.

ESR losses

Focusing on the ESR contributions, with respect to the circuit under test:

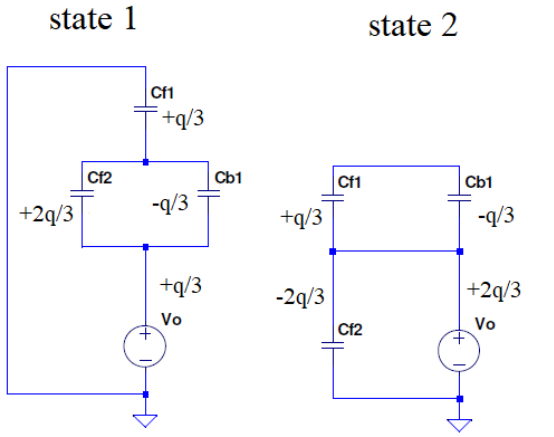


Figure 3.3.5: 3-to-1 ladder converter charge multiplier ESR

Choosing

$$\mathbf{a}_{ESR} = \begin{bmatrix} a_{cf2} & a_{cf1} & a_{cb1} \end{bmatrix}$$

Being $d^{(1)} = d^{(2)} = \frac{1}{2}$

$$\begin{cases} \mathbf{a}_{ESR}^1 = \begin{bmatrix} \frac{2}{3}, & \frac{1}{3}, & \frac{1}{3} \end{bmatrix} \\ \mathbf{a}_{ESR}^2 = \begin{bmatrix} \frac{2}{3}, & \frac{1}{3}, & \frac{1}{3} \end{bmatrix} \end{cases}$$

Summing up all the contributions:

$$P_{ESR} = \sum_h^H \left[ESR_h \sum_p^N \left(\frac{1}{d^{(p)}} \cdot \left(a_{ESR,h}^{(p)}\right)^2 i_{out}^2 \right) \right] = \sum_h^H \left[ESR_h \sum_p^N \left(\frac{1}{d^{(p)}} \cdot \left(a_{ESR,h}^{(p)}\right)^2 \right) \right] \cdot \left(i_{out}^2\right)$$

Being the power loss modeled as output voltage drop, and depending on the output current, the equivalent output resistance $R_{FSL,ESR}$ power loss can be expressed as:

$$P_{loss} = R_{FSL,ESR} \cdot i_{out}^2$$

Hence, by inspection, $R_{FSL,ESR}$ can be determined as:

$$R_{FSL,ESR} = \sum_h^H \left[ESR_h \sum_p^N \left(\frac{1}{d^{(p)}} \cdot \left(a_{ESR,h}^{(p)}\right)^2 \right) \right]$$

$$R_{FSL,ESR} = \sum_{h}^{H} \left[ESR_h \cdot A_{e,h}^2 \right]$$

Rds,on losses

Focusing on the $R_{ds,on}$ contributions, with respect to the circuit under test:

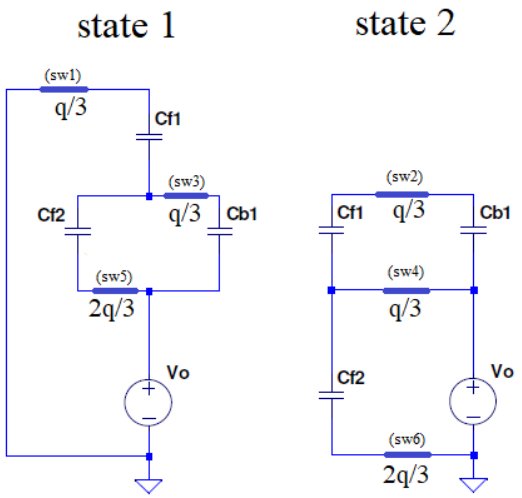


Figure 3.3.6: 3-to-1 ladder converter charge multiplier Ron

Choosing

$\mathbf{a}_{R_{on}} =$

$= \begin{bmatrix} a_{sw1} & a_{sw2} & a_{sw3} & a_{sw4} & a_{sw5} & a_{sw6} \end{bmatrix}$

Being $d^{(1)} = d^{(2)} = \frac{1}{2}$

$$\begin{cases} \mathbf{a}_{R_{on}}^1 = \begin{bmatrix} \frac{1}{3}, & 0, & \frac{1}{3}, & 0, & \frac{2}{3}, & 0 \end{bmatrix} \\ \mathbf{a}_{R_{on}}^2 = \begin{bmatrix} 0, & \frac{1}{3}, & 0, & \frac{1}{3}, & 0, & \frac{2}{3} \end{bmatrix} \end{cases}$$

Summing up all the contributions:

$$P_{R_{on}} = \sum_{k}^{K} \left[R_{on,k} \sum_{p}^{N} \left(\frac{1}{d^{(p)}} \cdot \left(a_{R_{on},h}^{(p)} \right)^2 i_{out}^2 \right) \right] = \sum_{k}^{K} \left[R_{on,k} \sum_{p}^{N} \left(\frac{1}{d^{(p)}} \cdot \left(a_{R_{on},h}^{(p)} \right)^2 \right) \right] \cdot \left(i_{out}^2 \right)$$

Being the power loss modeled as output voltage drop, and depending on the output current, the equivalent output resistance $R_{FSL,R_{on}}$ power loss can be expressed as:

$$P_{loss} = R_{FSL,R_{on}} \cdot i_{out}^2$$

Hence, by inspection, $R_{FSL,R_{on}}$ can be determined as:

$$R_{FSL,R_{on}} = \sum_{k}^{K} \left[R_{on,k} \sum_{p}^{N} \left(\frac{1}{d^{(p)}} \cdot \left(a_{R_{on},h}^{(p)} \right)^2 \right) \right]$$

$$R_{FSL,R_{on}} = \sum_{k}^{K} \left[R_{on,k} \cdot A_{s,k}^2 \right]$$

3.3.3 Wrap-up

The losses contributions can be identified as frequency-dependent, or independent. They are respectively associated to the slow-switching, and to the fast-switching regime. This is the meaning of the frequency behavior presented in Figure 3.2.3 of the the output resistance model.

Unfortunately, neither of the two limits is optimal for the converter to work. In the *SSL*, the output resistance model is too high, while, in the *FSL*, the frequency is too high, and other problems may arise. Indeed, the best working point is at the frequency where the two limits meet: the frequency is not too high, as in the *FSL*, and the output impedance is kept low, approaching the high-frequency limit. No accurate model is available in that operating region; so, the typical procedure to determine the output resistance in between the two limits is to combine the results by means of a squared average:

$$R_o = \sqrt{(R_{SSL})^2 + (R_{FSL})^2}$$

Recalling that $R_{FSL} = R_{FSL,ESR} + R_{FSL,R_{on}}$

3.4 Optimization, and Components Selection

In previous section the model of the contribution of each component to the efficiency have been exploited: all losses have been reflected in the computation of a real resistance. Now the process must be reversed: starting from some specifications on the performances, it necessary to derive the circuit requirements in order to minimize that output resistance as wished.

The optimization procedure requires knowledge of the working voltage of both capacitors and switches, Respectively, two vectors can be defined, $\mathbf{v}_{c,Rated}$ and $\mathbf{v}_{s,Rated}$, to represent this kind of information. To simplify the notation, they will be written as $\mathbf{v}_{c,X}$ and $\mathbf{v}_{s,X}$.

In order to optimize the design, an optimization metric must be first defined. For what concerns capacitors, the optimization metric is the energy storage capability C-V^2. For what concerns switches, the optimization metric is the V-A capability, that can be translated in a G-V^2 product (being G the switch conductance: $G = \frac{1}{R_{on}}$).

Since the *FSL* does not depend on capacitance values, because only the *SSL* does depend on it, then the optimization procedure can be decoupled: optimizing over the FSL

The optimization algorithm that will be used both for the *SSL* and the *FSL* makes use of the Lagrangian optimization.

3.4.1 SSL Optimization

The constraint for the capacitor optimization is the total energy storage capability, summed over all capacitors:

$$E_{tot} = \sum_{h}^{H} \frac{1}{2} C_h V_{cX,h}^2$$

Since it does not involve the switching frequency, the optimization of R_{SSL} will be developed without taking into account the switching frequency, for now.

Resorting to the Lagrangian optimization, a function L is defined as:

$$L = \sum_{h}^{H} \frac{A_{c,h}^2}{C_h} - \lambda \left(\sum_{h}^{H} \frac{1}{2} C_h V_{cX,h}^2 - E_{tot} \right)$$

To minimize the R_{SSL}:

$$\begin{cases} \dfrac{\partial L}{\partial \lambda} = 0 \\ \\ \dfrac{\partial L}{\partial C_h} = 0 \end{cases}$$

Expressing the partial derivatives:

$$\begin{cases} \dfrac{\partial L}{\partial \lambda} = \displaystyle\sum_{h}^{H} \frac{1}{2} C_h V_{cX,h}^2 - E_{tot} = 0 \\ \\ \dfrac{\partial L}{\partial C_h} = -\dfrac{A_{c,h}^2}{C_h^2} + \dfrac{\lambda}{2} V_{cX,h}^2 = 0 \end{cases}$$

The first equation holds to be the same as the starting constraint.

Taking into account, for instance $h = 1$, for the second equation can be re-written as:

$$\frac{\lambda}{2} = \frac{A_{c,1}^2}{C_1^2} \cdot \frac{1}{V_{cX,1}^2} \quad \rightarrow \quad \sqrt{\frac{\lambda}{2}} = \left| \frac{A_{c,1}}{C_1 \cdot V_{cX,1}} \right|$$

Hence, any capacitance could be expressed as:

$$C_h = \left|\frac{A_{c,h}}{V_{cX,h}}\right| \sqrt{\frac{2}{\lambda}} = C_1 \left|\frac{V_{cX,1}}{A_{c,1}}\right| \cdot \left|\frac{A_{c,h}}{V_{cx,h}}\right|$$

Re-writing the constraint equation:

$$E_{tot} = \sum_h^H \frac{1}{2} C_h V_{cX,h}^2 = \frac{C_1}{2} \left|\frac{V_{cX,1}}{A_{c,1}}\right| \sum_h^H |A_{c,h} \cdot V_{cX,h}|$$

From last equation, C_1 can be extracted:

$$C_1 = \frac{2 \cdot E_{tot}}{\sum_h^H |A_{c,h} \cdot V_{cX,h}|} \cdot \left|\frac{A_{c,1}}{V_{cX,1}}\right|$$

Extending the solution to any capacitor C_α, the optimal capacitance value can be determined as follows:

$$C_\alpha = \frac{2 \cdot E_{tot}}{\sum_h^H |A_{c,h} \cdot V_{cX,h}|} \cdot \left|\frac{A_{c,\alpha}}{V_{cX,\alpha}}\right| = K_C \cdot \left|\frac{A_{c,\alpha}}{V_{cX,\alpha}}\right|$$

Being K_C constant for any capacitor.

Re-writing the R_{SSL} impedance just as a function of design parameters:

$$R_{SSL} = \frac{1}{f_{sw}} \sum_h^H \frac{A_{c,h}^2}{C_h} = \frac{1}{f_{sw} K_C} \sum_h^H A_{c,h} \cdot V_{cX,h} = \frac{\left(\sum_h^H A_{c,h} \cdot V_{cX,h}\right)^2}{2 \cdot E_{tot} \cdot f_{sw}}$$

3.4.2 FSL Optimization

The constraint for the switches optimization is the total G-V^2 metric, summed over all switches:

$$S_{tot} = \sum_k^K \frac{1}{2} G_k V_{sX,k}^2$$

Resorting to the Lagrangian optimization, a function L is defined as:

$$L = \sum_k^K \frac{A_{s,k}^2}{G_k} - \lambda \left(\sum_k^K G_k V_{sX,k}^2 - S_{tot} \right)$$

To minimize the R_{FSL}:

$$\begin{cases} \dfrac{\partial L}{\partial \lambda} = 0 \\ \\ \dfrac{\partial L}{\partial G_k} = 0 \end{cases}$$

Expressing the partial derivatives:

$$\begin{cases} \dfrac{\partial L}{\partial \lambda} = \displaystyle\sum_{k}^{K} G_k V_{sX,k}^2 - S_{tot} = 0 \\ \\ \dfrac{\partial L}{\partial G_k} = -\dfrac{A_{s,k}^2}{G_k^2} + \lambda V_{sX,k}^2 = 0 \end{cases}$$

The first equation holds to be the same as the starting constraint.

Taking into account, for instance $h = 1$, for the second equation can be re-written as:

$$\lambda = \frac{A_{s,1}^2}{G_1^2} \cdot \frac{1}{V_{sX,1}^2} \quad \rightarrow \quad \sqrt{\lambda} = \left| \frac{A_{s,1}}{G_1 \cdot V_{sX,1}} \right|$$

Hence, any switch conductance could be expressed as:

$$G_k = \left| \frac{A_{s,k}}{V_{sX,k}} \right| \sqrt{\frac{1}{\lambda}} = G_1 \left| \frac{V_{sX,1}}{A_{s,1}} \right| \cdot \left| \frac{A_{s,k}}{V_{sx,k}} \right|$$

Re-writing the constraint equation:

$$S_{tot} = \sum_{k}^{K} G_k V_{sX,k}^2 = G_1 \left| \frac{V_{sX,1}}{A_{s,1}} \right| \sum_{k}^{K} |A_{s,k} \cdot V_{sX,k}|$$

From last equation, G_1 can be extracted:

$$G_1 = \frac{S_{tot}}{\sum_k^K |A_{s,k} \cdot V_{sX,k}|} \cdot \left| \frac{A_{s,1}}{V_{sX,1}} \right|$$

Extending the solution to any switch conductance G_α, the optimal value can be determined as follows:

$$G_\alpha = \frac{S_{tot}}{\sum_k^K |A_{s,k} \cdot V_{sX,k}|} \cdot \left| \frac{A_{s,\alpha}}{V_{sX,\alpha}} \right| = K_S \cdot \left| \frac{A_{s,\alpha}}{V_{sX,\alpha}} \right|$$

Being K_S constant for any component.

Re-writing the $R_{FSL,R_{on}}$ impedance just as a function of design parameters:

$$R_{FSL,R_{on}} = \sum_{k}^{K} \frac{A_{s,k}^2}{G_k} = \frac{1}{K_S} \sum_{k}^{K} A_{s,k} \cdot V_{sX,k} = \frac{\left(\sum_k^K A_{s,k} \cdot V_{sX,k} \right)^2}{S_{tot}}$$

3.5 Wrap-up

In the next chapter the design procedure adopted will be described in detail. For now, the use for the results obtained will be showed.

As first design approach, the steps to be followed are the following:

1. SPECIFICATIONS: set of specifications needed in order to complete the sizing of components
   - convertion ratio ($M = \frac{V_O}{V_{in}}$) at no load
   - input voltage (V_{in})
   - maximum power (P_{max}), or maximum output current ($I_{L,max}$)
   - minimum efficiency when working at maximum power (η_{min})
2. TOPOLOGY CHOICE: depending on the requirements, a topology may perform better than another one with respect to the following parameters
   - number of capacitors
   - number of switches
   - number of switching phases
   - multilevel switch gate driving
3. TOPOLOGY CONSTRAINTS: from specifications, some parameters can be derived
   - model for the output sinking load, when working at maximum power

     $$P_{max} = \frac{(\eta_{min} V_O)^2}{R_{L,min}} = \left(\frac{\eta_{min} V_{in}}{M}\right)^2 \frac{1}{R_{L,min}} \quad \rightarrow \quad R_{L,min} = \left(\frac{\eta_{min} V_{in}}{M}\right)^2 \frac{1}{P_{max}}$$

     (Note that since the output voltage is not regulated, and it depends on the input voltage and on the efficiency, *i.e.*, on the equivalent output resistance, resorting to what is described in Section 3.1, in order to actually have P_{max} supplied to the output, the efficiency have to be included in the model of the equivalent load resistance)

- output resistance boundary, when working at maximum power

$$\eta_{min} = \frac{R_{L,min}}{R_{L,min} + R_{o,max}} \quad \rightarrow \quad R_{o,max} = R_{L,min}\left(\frac{1-\eta_{min}}{\eta_{min}}\right)$$

- the charge multiplier coefficients, from KCL constraints applied to the switching phases

$$\mathbf{a}_{cX} \quad , \quad \mathbf{a}_{sX}$$

- the working voltages can be derived depending on the switching phases; so, the rated voltages for the components can be selected

$$\mathbf{v}_{cX} \quad , \quad \mathbf{v}_{sX}$$

4. COMPONENT SIZING: after having derived all practical specifications, the sizing algorithm can be performed in order to satisfy the specifications

- switching frequency selection f_{sw}
- recalling that $R_o^2 = R_{SSL}^2 + R_{FSL}^2$, the weight of each contribution can be chosen

$$\left(\frac{R_{SSL}}{R_o}\right)^2 + \left(\frac{R_{FSL}}{R_o}\right)^2 = w_{SSL}^2 + w_{FSL}^2 = 1$$

- capacitance values lower limit

$$R_{o,max} \quad , \quad w_{SSL} \quad \rightarrow \quad C_h \quad , \quad ESR_h$$

- switch on-resistance upper limit

$$R_{FSL,R_{on}} = (R_{FSL} - R_{FSL,ESR}) \quad \rightarrow \quad G_k = \frac{1}{R_{on,k}}$$

CHAPTER 4

Switched-Capacitor Converter Design

In this chapter, the design of a SCC is performed, resorting to the equations obtained in previous chapter. Starting from a description of the application in which the converter will be implemented, the specifications will be derived. Hence, the design of the converter and the components needed will be carried out. Therefore, the component selection is discussed, as well as some implementation issues.

4.1 Case of study: specifications

The electrical load of vehicles has been dramatically increased ([12]-[18]). This because most of the on-board functions are better controlled by electrical interfaces, instead of mechanical. Moreover, the advantage of replacing mechanical actuators with electrical actuators is the possibility of reducing weight and volume, increasing packaging flexibility.

The original electrical system in automotive environment was based on a single 14 V supply. As the aforementioned electrical loads increased, the power increased too, and the current as well. To face the issue, today's vehicle are moving toward the 42 V system; but it is not straightforward to move all the devices from the 14 V power line to the high-voltage power line, hence many vehicles implement a dual voltage supply system.

Two different electrical system alternatives are available to supply both power rails: a dual battery system, and a single battery system (as shown in Figure 4.1.1). Both solutions have some advantages with respect to the counterpart, but the most

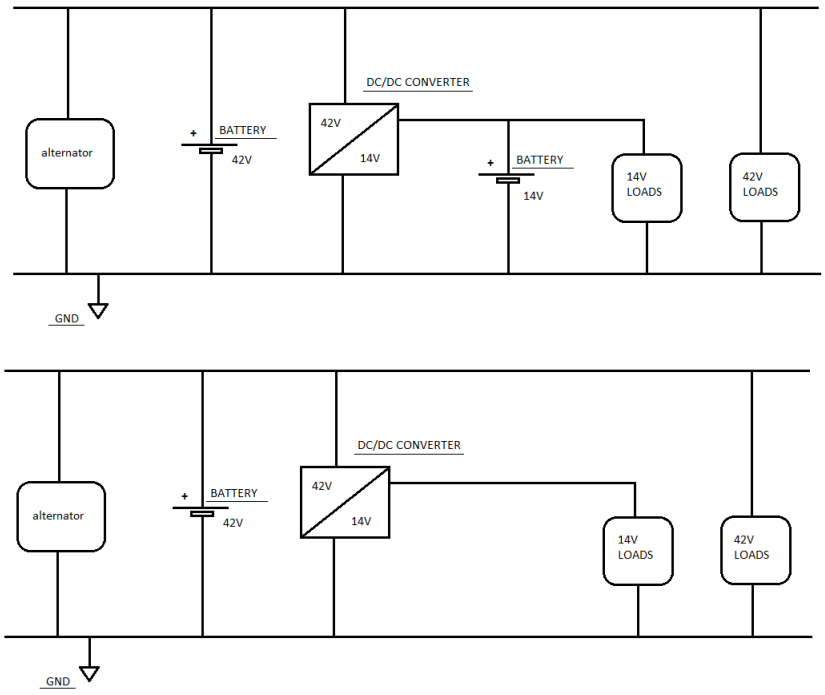


Figure 4.1.1: Simplified automotive electrical system: dual battery system; single battery system

important thing is that they both have in common a dc/dc converter as interface between the 42 V rail. For example, the dual battery solution allows manufactures to better deal with *key-off* loads, which means the environment is more adapt to distinguish between ignition-loads and *key-off*-loads. To better explain, the main idea is to separate the battery draining auxiliary features (such as the clock, the keyless entry, the theft alarm and some more) with those features that are too much important for the ignition of the engine, hence are strictly related to the start-up of the system.

Independently of the solution implemented, the power when the engine is running comes from the alternator, whose electrical model is shown in Figure 4.1.2. Part of that power is used to recharge the batteries, while supporting the power delivery to the different loads.

In this work a switched-capacitor converter between the 42 V and the 14 V rails will be designed, assuming to work in a dual-battery system.

The typical load to be supplied to the 14 V is about 1 kW average. From this, a

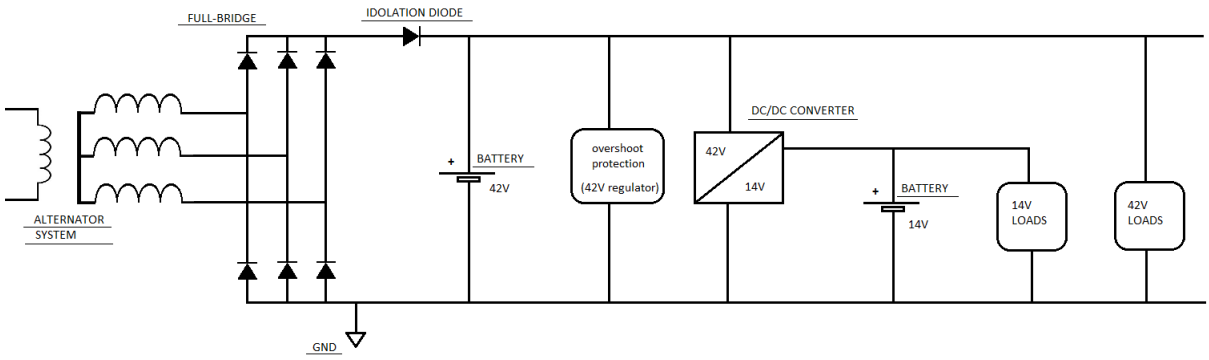


Figure 4.1.2: Working environment

first set of specifications can be derived:

- input voltage: $V_{in} = 42\,\mathrm{V}$ (in the $30\,\mathrm{V}$ - $50\,\mathrm{V}$)
- output voltage: $V_o = 14\,\mathrm{V}$
- maximum power: $P = 1\,\mathrm{kW}$

Next steps will be about the choice of the topology and sizing of the components, that are going to be described in next sections.

4.2 Topology Analysis

First the topology choice is discussed; then, topology stresses are analyzed; finally, the coefficients needed for the design are extracted.

4.2.1 Topology Choice

Between all the possible circuits, two in particular were selected: the ladder topology in Figure 3.3.1, and the multilevel topology in Figure 1.4.13.

For selecting the topology, the following criteria have been followed:

- minimum number of capacitors
- minimum number of switches

\ \ \	*ladder*	*multilevel*
M	1/3	1/3
switches	6	6
capacitors	$2+3$	$2+2$
switching phases	2	3

Table 4.1: topology comparison

The characteristics of the two circuits are compared in Table 4.1 (note that two capacitors are needed as input and output capacitors).

The most important characteristic is the minimum number of capacitor in the multilevel topology, paid off by increasing the number of switching phases with respect to the ladder topology. Since the multilevel topology has the least number of components, it has been chosen over all other possibilities.

The selected topology is reported in Figure 4.2.1.

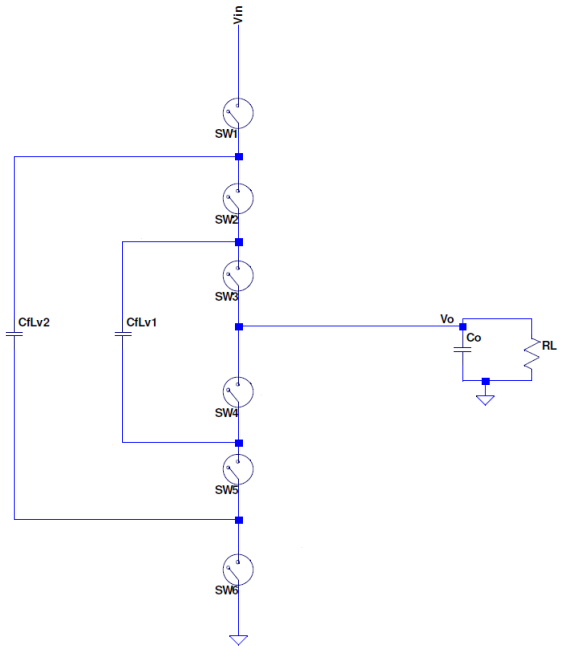


Figure 4.2.1: 4-level SCC circuit

4.2.2 Topology Analysis

First thing to look at is the timing of the circuit. The complementary behavior of the switches is shown in Figure 4.2.2.

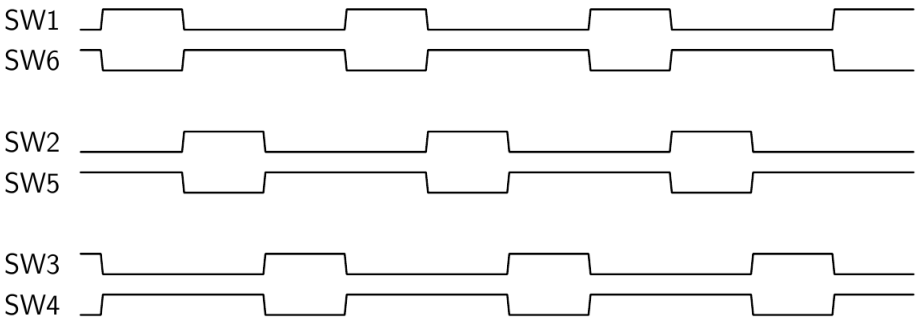


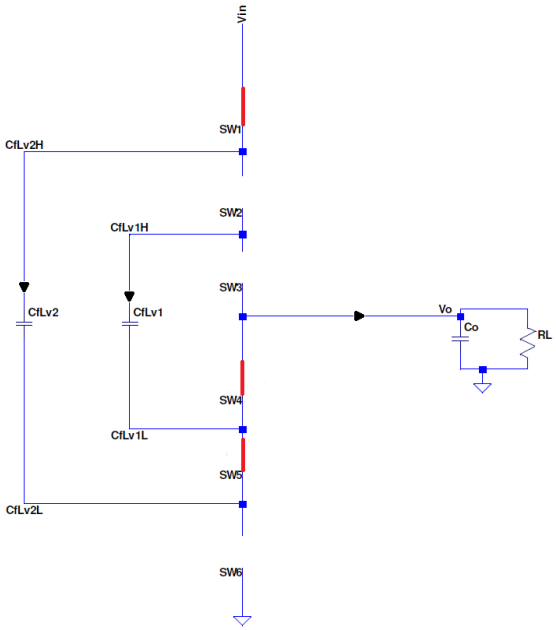
Figure 4.2.2: SCC switch control timing

Three different switching phases can be identified:

phase 1: $SW1$, $SW4$, $SW5$ are turned on (Figure 4.2.3)

phase 2: $SW2$, $SW4$, $SW6$ are turned on (Figure 4.2.4)

phase 3: $SW3$, $SW5$, $SW6$ are turned on (Figure 4.2.5)



KVL :

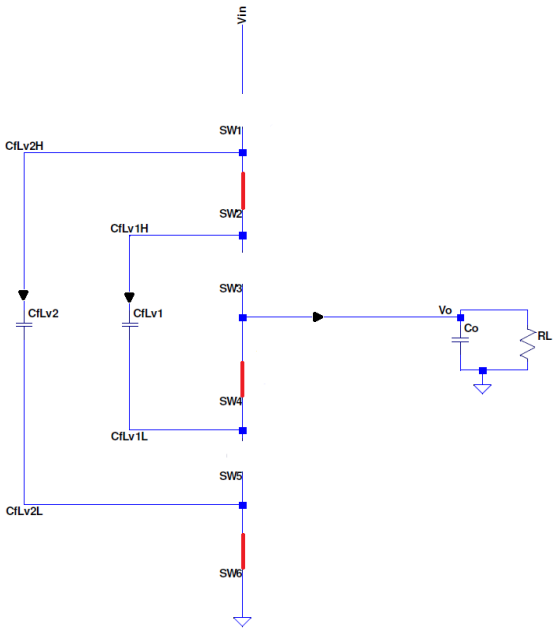
$$V_{in} = V_{c2} + V_o$$

KCL (modeled as impulsive charge transfer):

$$q_o^{(1)} = q_{c2}^{(2)}$$

$$q_{c1}^{(1)} = 0$$

Figure 4.2.3: phase 1



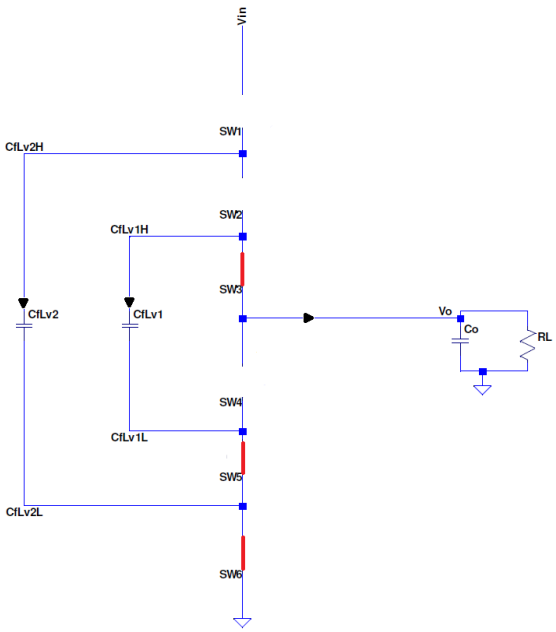
KVL :

$$V_{c2} = V_{c1} + V_o$$

KCL (modeled as impulsive charge transfer):

$$q_o^{(2)} = q_{c1}^{(2)} = -q_{c2}^{(2)}$$

Figure 4.2.4: phase 2



KVL :

$$V_{c1} = V_o$$

KCL (modeled as impulsive charge transfer):

$$q_o^{(3)} = -q_{c1}^{(3)}$$

$$q_{c2}^{(3)} = 0$$

Figure 4.2.5: phase 3

The ideal average equilibrium voltages when working in cyclic conditions can be extracted from the KVL in the three switching phases:

$$\begin{cases} V_o = V_{in}/3 = 14\,\mathrm{V} \\ V_{c1} = V_{in}/3 = 14\,\mathrm{V} \\ V_{c2} = 2 \cdot V_{in}/3 = 28\,\mathrm{V} \end{cases}$$

Hence, the conversion ratio is $M = v_o/V_{in} = 1/3$.

The voltage stresses of the switches are all equal to the minimum voltage of the system, $Vo = Vin/3$.

Some more specifications can be derived:

- minimum voltage rating of capacitors:

$$\mathbf{v}_{cX} = [v_{c1X}, v_{c2X}] = [63, 63]$$

- minimum voltage rating of switches:

$$\mathbf{v}_{cX} = [v_{sw1X}, v_{sw2X}, v_{sw3X}, v_{sw4X}, v_{sw5X}, v_{sw6X}] = [60, 60, 60, 60, 60, 60]$$

The components seem to be over-rated. The reason will be better explained in following sections (it is basically due to start-up working conditions).

From KCL impulsive charge transfer constraints, the charge multiplier coefficients for the equivalent output resistance design method can be derived. Recalling that the following condition must hold:

$$\begin{cases} q_{out} = q_o^{(1)} + q_o^{(2)} + q_o^{(3)} \\ q_{c1}^{(1)} + q_{c1}^{(2)} + q_{c1}^{(3)} = 0 \\ q_{c2}^{(1)} + q_{c2}^{(2)} + q_{c2}^{(3)} = 0 \end{cases}$$

it ends up with:

$\mathbf{a}_c = [a_{c1} \quad a_{c2}]$

$$\begin{cases} \mathbf{a}_c^{(1)} = \begin{bmatrix} 0 & \frac{1}{3} \end{bmatrix} \\ \mathbf{a}_c^{(2)} = \begin{bmatrix} \frac{1}{3} & -\frac{1}{3} \end{bmatrix} \\ \mathbf{a}_c^{(3)} = \begin{bmatrix} -\frac{1}{3} & 0 \end{bmatrix} \end{cases}$$

$$\mathbf{a}_{ESR} = \begin{bmatrix} a_{c1} & a_{c1} \end{bmatrix}$$

$$\begin{cases} \mathbf{a}_{ESR}^{(1)} = \begin{bmatrix} 0 & \frac{1}{3} \end{bmatrix} \\ \mathbf{a}_{ESR}^{(2)} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} \end{bmatrix} \\ \mathbf{a}_{ESR}^{(3)} = \begin{bmatrix} \frac{1}{3} & 0 \end{bmatrix} \end{cases}$$

$$\mathbf{a}_{R_{on}} = \begin{bmatrix} a_{sw1} & a_{sw2} & a_{sw3} & a_{sw4} & a_{sw5} & a_{sw6} \end{bmatrix}$$

$$\begin{cases} \mathbf{a}_{R_{on}}^{(1)} = \begin{bmatrix} \frac{1}{3} & 0 & 0 & \frac{1}{3} & \frac{1}{3} & 0 \end{bmatrix} \\ \mathbf{a}_{R_{on}}^{(2)} = \begin{bmatrix} 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} \end{bmatrix} \\ \mathbf{a}_{R_{on}}^{(3)} = \begin{bmatrix} 0 & 0 & \frac{1}{3} & 0 & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \end{cases}$$

4.3 Design Procedure and Components Selection

In order to size capacitors and conductance of switches some constraints must be derived first from the specifications and from circuit analysis (refer to Section 3.5 and 4.2.2); moreover some prior choices must be done:

- choosing as constraint the minimum efficiency, at maximum power (note that, as already said, this model will only take care of capacitors and switches conduction losses, even if it can be extended to other losses contributions, as gate driving losses):

  $$\eta > 95\%$$

  The choice is related to the fact that the output voltage have to be larger 12 V in order to be able to recharge also the battery. Resorting to the model in Section 3.1

  $$V_o = \eta \cdot M \cdot V_{in} = 0.95 \cdot \frac{12\,\mathrm{V}}{3} = 13.3\,\mathrm{V}$$

  That's not the only reason: since the system has to work at high power, the choice is also related to feasibility issues point of view, for what concern dissipated power.

- input voltage:

  $$40\,\mathrm{V} < V_{in} < 50\,\mathrm{V}$$

Nominal steady voltage: $V_{in} = 42\,\mathrm{V}$; hence, switches and capacitors must be rated for at least 60 V.

- ideal conversion ratio:

$$M = V_{in}/V_o = 1/3$$

- load current:

$$I_o \approx \frac{P_{max}}{V_o} = \frac{1\,\mathrm{kW}}{14\,\mathrm{V}} = 72\,\mathrm{A}$$

- model of the load resistance

$$R_L > \frac{(\eta_{min} V_{in} M)^2}{P_{max}} = \frac{1}{1\,\mathrm{kW}} \cdot \left(\frac{0.95 \cdot 42\,\mathrm{V}}{3}\right)^2 \approx 180\,\mathrm{m\Omega}$$

- model of the equivalent output resistance of the SCC:

$$R_{out} < R_{L,min}\left(\frac{1-\eta_{min}}{\eta_{min}}\right) = 180\,\mathrm{m\Omega} \cdot \left(\frac{1-0.95}{0.95}\right) \approx 9.5\,\mathrm{m\Omega}$$

- charge multiplier coefficients (derived in previous section):

$\mathbf{a}_c = [a_{c1} \quad a_{c2}]$

$$\begin{cases} \mathbf{a}_c^{(1)} = \left[0 \quad \frac{1}{3}\right] \\ \mathbf{a}_c^{(2)} = \left[\frac{1}{3} \quad -\frac{1}{3}\right] \\ \mathbf{a}_c^{(3)} = \left[-\frac{1}{3} \quad 0\right] \end{cases}$$

$\mathbf{a}_{ESR} = [a_{c1} \quad a_{c1}]$

$$\begin{cases} \mathbf{a}_{ESR}^{(1)} = \left[0 \quad \frac{1}{3}\right] \\ \mathbf{a}_{ESR}^{(2)} = \left[\frac{1}{3} \quad \frac{1}{3}\right] \\ \mathbf{a}_{ESR}^{(3)} = \left[\frac{1}{3} \quad 0\right] \end{cases}$$

$\mathbf{a}_{R_{on}} = [a_{sw1} \quad a_{sw2} \quad a_{sw3} \quad a_{sw4} \quad a_{sw5} \quad a_{sw6}]$

$$\begin{cases} \mathbf{a}_{R_{on}}^{(1)} = \left[\frac{1}{3} \quad 0 \quad 0 \quad \frac{1}{3} \quad \frac{1}{3} \quad 0\right] \\ \mathbf{a}_{R_{on}}^{(2)} = \left[0 \quad \frac{1}{3} \quad 0 \quad \frac{1}{3} \quad 0 \quad \frac{1}{3}\right] \\ \mathbf{a}_{R_{on}}^{(3)} = \left[0 \quad 0 \quad \frac{1}{3} \quad 0 \quad \frac{1}{3} \quad \frac{1}{3}\right] \end{cases}$$

- selecting the operating frequency:

$$f_{sw} = 100\,\mathrm{kHz}$$

- choosing the duty ratio for each phase:

$$\mathbf{d} = \begin{bmatrix} d^{(1)} & d^{(2)} & d^{(3)} \end{bmatrix} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix}$$

This is the set of data required to go on with the design algorithm.

A *MatLab* script has been written in order to speed up the computations (refer to Appendix C.1). Three different steps are identified:

(step-0) the first section of code, common to all steps, helps to keep trace of the system characteristics.

(step-1) in this part, it is possible to perform a first guess of the order of magnitude of the flying capacitors.

Assuming at first an equal weight between $w_{SSL} = w_{FSL}$:

$$R_{out}^2 = (R_{SSL})^2 + (R_{FSL})^2 \;\rightarrow\; \left(\frac{R_{SSL}}{R_{out}}\right)^2 + \left(\frac{R_{FSL}}{R_{out}}\right)^2 = 1$$

$$w_{SSL} + w_{FSL} = 1 \;\rightarrow\; w_{SSL} = w_{FSL} = 0.5$$

$$R_{SSL} = \frac{R_{out}}{\sqrt{2}} = \frac{9.5\,\mathrm{m\Omega}}{\sqrt{2}} \approx 6.7\,\mathrm{m\Omega}$$

This leads to

$$C_1 = C_2 \approx 340\,\mu\mathrm{F}$$

assuming to use only one capacitor for each flying capacitor.

The data are reported in a *.txt* file, formatted is such a way that the real components characteristics can be overwritten: capacitance value, capacitance tolerance, ESR, ESR tolerance, number of parallel capacitors.

The first thing to take care of is the fact that a single capacitor cannot sustain the full load current. Assuming to employ 12 parallel capacitors, with respect to what described in Appendix B.1:

- $C = 39\,\mu\mathrm{F}$
- tolerance 20%

- $ESR = 50\,\mathrm{m\Omega}$
- current $I_C = 6\,\mathrm{A}$

The equivalent capacitor will have the following characteristics:

- $C_{eq} = 470\,\mu\mathrm{F}$ ($370\,\mu\mathrm{F}$, worst case tolerance 20%)
- $ESR_{eq} \approx 6\,\mathrm{m\Omega}$ (assuming 50% tolerance)
- current $I_{C,eq} = 72\,\mathrm{A}$

(step-2) in this step, the number of parallel capacitors is evaluated depending on the relative weight of the ESR with respect to the on-resistance of the MOSFETs (this because of the fact that it is much harder to find a low-ESR, high rms current, capacitor than a low-r_{on} , high-current MOSFET):

$$R_{FSL} = R_{FSL,Ron} + R_{FSL,ESR}$$

$$\frac{R_{FSL,Ron}}{R_{FSL}} + \frac{R_{FSL,ESR}}{R_{FSL}} = w_{R,on} + w_{ESR} = 1$$

The thresholds of the weights can be selected at will, depending on the requirements about the conductance of the switches.

Assuming to keep the threshold on the *SSL* limit $R_{SSL} < \frac{R_{out}}{\sqrt{2}}$, the threshold on the ESR is set at $w_{ESR} = 0.75$.

The algorithm gives back the actual number of capacitors needed to reduce the equivalent ESR to the selected threshold. The final result is $N = 19$.

(step-3) in this last step, the upper limit for the switch conductance is defined. Always assuming worst case scenario for what concerns tolerances, the equivalent resistance of the switches end up to be: $R_{on,j} \approx 1\,\mathrm{m\Omega}$, being j=1,2,...,6.

To sum up, the components must satisfy a quite demanding set of requirements. This because the power involved is quite high, which means the current can be a bottleneck in the design procedure.

This procedure is just a first approach design: real component are not taken into account yet, but it has been just implemented as guideline, to define some

extra boundaries. This because one thing in particular have to be noticed: 19 parallel capacitor are too many, for practical reasons related to PCB requirements (for instance, current crowding effect which as a result aggravates electromigration effect).

The bottleneck in step-2 is mainly related to the ESR: it has to be reduced in order to reduce as well the number of capacitors. Depending on the current capability and on the ESR, a reasonable maximum number of components is about 5-8 (also because of costs, especially for high power devices).

Picking up a film capacitor, instead of electrolytic, with the following characteristics (look for component part numbers in Chapter 6):

- $C = 50\,\mu\text{F}$
- tolerance 10%
- $ESR = 6\,\text{m}\Omega$
- $I_{rms} = 15\,\text{A}$
- $V_{max} = 550\,\text{V}$

now the ESR is small enough to avoid employing many parallel capacitors. Therefore, the weight on R_{SSL} can be enlarged. Starting again the procedure:

(step-0) enlarging the constraint on the *SSL* limit: $w_{SSL} = 0.75$:

(step-1) a first guess of the order of magnitude of the flying capacitors with respect to the previous constraint:

$$R_{SSL} = R_{out} \cdot \sqrt{0.75} = 9.5\,\text{m}\Omega \cdot \sqrt{0.75} \approx 8\,\text{m}\Omega$$

Which leads to

$$C_1 = C_2 \approx 290\,\mu\text{F}$$

assuming to use only one capacitor for each flying capacitor.

Assuming to use 8 parallel capacitors with the parameters described above, the equivalent capacitor will have the following characteristics:

- $C_{eq} = 400\,\mu\text{F}$ ($360\,\mu\text{F}$, worst case tolerance 10%)
- $ESR_{eq} \approx 1.2\,\text{m}\Omega$ (assuming 50% tolerance)
- current $I_C = \dfrac{72\,\text{A}}{8} = 9\,\text{A}$

Being the equivalent resistance quite small, it is possible to reduce the constraint on the ESR weight, and enlarging the one related to the switch conductance.

(step-2) setting the threshold on the ESR is set at $w_{ESR} = 0.25$.

The algorithm gives back the actual number of capacitors needed to reduce the equivalent ESR to the selected threshold. The final result is $N = 8$. Nothing changes compared to step-1; the requirements are already met.

(step-3) always assuming worst case scenario for what concerns tolerances, the equivalent resistance of the switches ends up to be: $R_{on,j} \approx 2\,\text{m}\Omega$, being j=1,2,...,6.

In order to assess the results, the ideal structure in Figure 4.2.1 has been simulated.

The output capacitor has been sized with the same characteristics of the flying capacitor (including ESR parameter), in order to limit the output voltage ripple.

The steady-state behavior is presented in Figure 4.3.1 (for the efficiency analysis, refer to Chapter 6.).

To analyze the performance, only the samples of the last cycle (recalling that $T_{sw} = 10\,\mu\text{s}$) are considered. Theoretically, assuming V_{in} and R_L as constants

$$\eta = \frac{\overline{P_{out}}}{\overline{P_{in}}} = \frac{\frac{1}{T_{sw}} \cdot \int_{t_0}^{t_0+T_{sw}} v_{out}(t) \cdot i_{out}(t)\,dt}{\frac{1}{T_{sw}} \cdot \int_{t_0}^{t_0+T_{sw}} v_{in}(t) \cdot i_{in}(t)\,dt} \approx \frac{\frac{1}{R_L} \cdot \int_{t_0}^{t_0+T_{sw}} v_{out}^2(t)\,dt}{V_{in} \cdot \int_{t_0}^{t_0+T_{sw}} i_{in}(t)\,dt}$$

The simulation leads to $\eta = 0.96$ as expected.

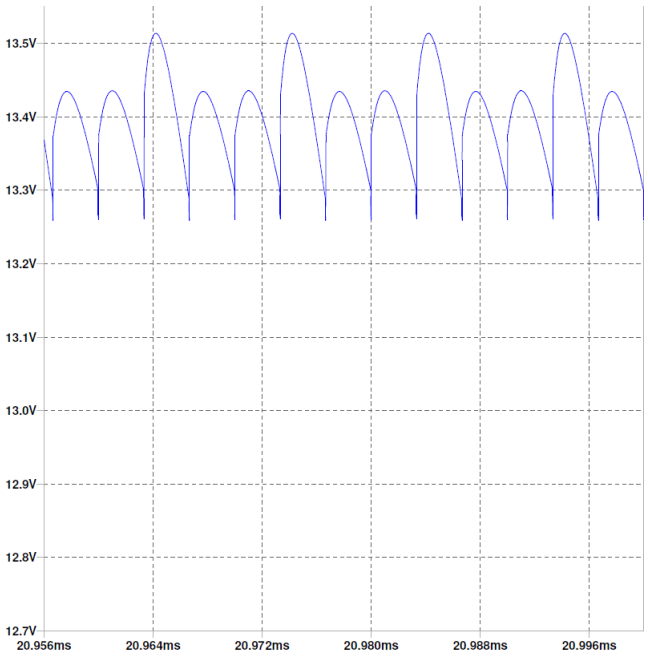


Figure 4.3.1: output voltage ripple

4.4 MOSFETs Driving

At this point it is important to substitute the ideal switches with real MOSFETs, and the related problems.

Always referring to Figure 4.2.1, the topology presents a multilevel switch structure, with 6 MOSFETs (look for part number in Chapter 6) in series. The goal in this section is to face, and solve, the problems related to driving a multilevel structure: type of driving, control signal isolation, pre-charging sequence at start-up.

4.4.1 Driving a Multilevel Switch Structure

Typically, two different types of driving are generally applied: low-side and high-side (assuming to work only with n-MOSFETs). For what concerns low-side driving, the MOSFET source terminal is supposed to be connected to the reference voltage; as for the high-side, the drain terminal is supposed to be connected to the supply voltage.

Here are presented the issues related to driving the multilevel switch structure:

1. the source terminal of the MOSFETs is not fixed, but pulsed with a 14 V excursion (generally speaking, $\Delta V_s = \frac{V_{in}}{M} = \frac{42\,\text{V}}{3} = 14\,\text{V}$)

2. typically, the maximum voltage applicable between gate-source is about 20 V, and must not be reversed

3. the gate-source voltage cannot be negative, for typical power n-MOSFETs

4. identify whether a MOSFET has to be driven as a low-side or a high-side

5. 3 couples of switches must be driven in a complementary way, hence a synchronous drivers (high-side and low-side) are preferred to isolated ones

6. for the high-side driving, two techniques are available to supply a gate voltage higher than the supply voltage: charge pumps and bootstrap; it must defined if both them can be implemented

In order to solve all these problems a solution similar to what described in [14]: after having identified what a basic cell is composed of, it is possible to define a self-supplied cell Figure 4.4.1.

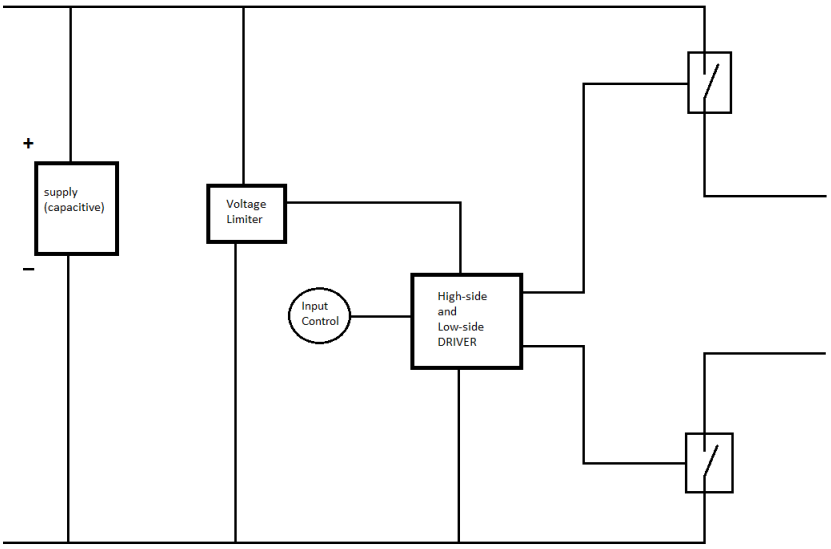


Figure 4.4.1: Elementary cell system diagram

A basic cell can be defined starting from a couple of switches that have to be driven in a complementary way. Since the (equivalent) flying capacitors involved in the converter have a quite large capacitance value, and a very small ESR, it is possible

to use them as power supplies. Hence, the converter components can be clustered as in Figure 4.4.2.

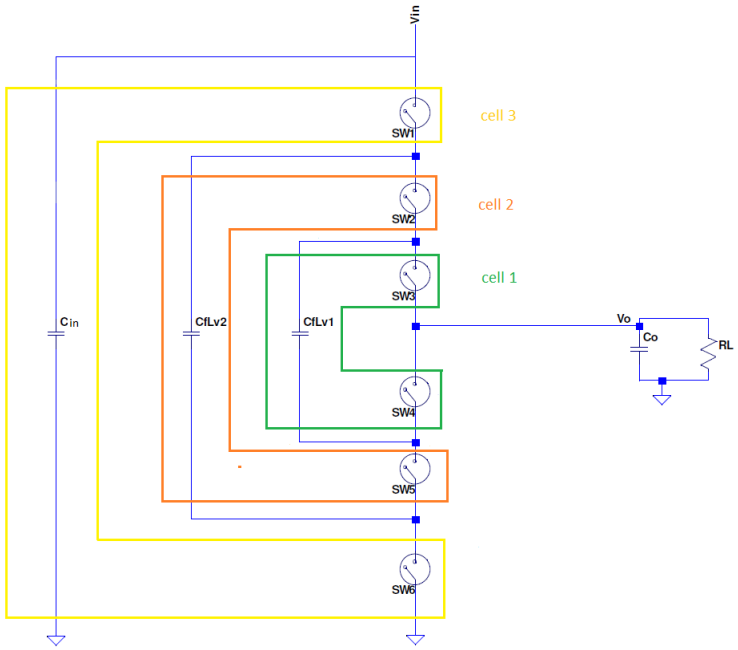


Figure 4.4.2: Elementary cells identification

This solution allows to solve all the previous problems:

1. since each transistor is driven with respect to its source voltage, it is not possible to have a negative gate-source voltage

2. even if the voltage applied to the capacitors may be higher than 20 V, some voltage limiting technique can be applied in order to avoid over-voltage

3. since each transistor is driven with respect to its source voltage, it is not possible to have a negative gate-source voltage (same of what described at point-*1*)

4. since in the structure one MOSFET is referred to its input capacitor reference voltage, and the other to the capacitor high voltage, and being the voltage across almost constant, it is possible to consider them respectively a low-side transistor, and a high-side transistor

5. now that the structure has been identified with a high-side and a low-side that must be driven in a complementary way at steady-state, this driving method

helps in solving the problem

6. expanding what discussed in point-*1*,*2*,*3*, the bootstrap solution is the best one, because the gate-source voltage can be fixed at will, since the driver is referred to the high-side source potential of the transistor

One aspect must be studied more in depth, *i.e.*, how to limit the gate-source voltage applied to the MOSFETs (see point-*2*). Since the voltage applied to a single cell may be far larger than 10 V (for instance the 42 V applied at the input), the solution adopted resorts to a zener-supply technique (refer to Figure 4.4.3).

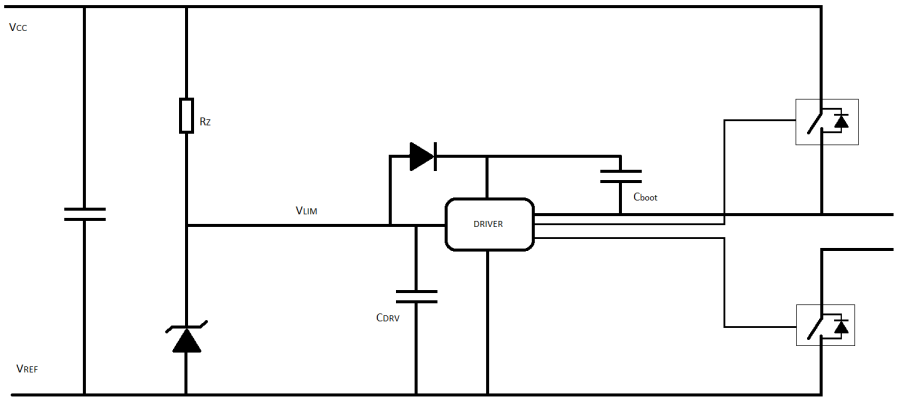


Figure 4.4.3: Elementary cell driver supply

This way, both the driver and the bootstrap capacitor voltages are limited to the zener voltage.

The zener resistor has to be sized in order not to dissipate too much, but at the same time it has to show a resistance value low enough to recharge the bootstrap capacitor of the driver. Both requirements cannot be fulfilled at the same time (unless resorting to a buck dc/dc solution, in place of the resistor-zener diode solution); hence, in Figure 4.4.4 an alternative schematic is reported.

This way the two requirements are independent to one another, but an extra zener diode is needed to set a threshold on the bootstrap capacitor.

Picking up a 10 V-zener diode both for the supply and for the bootstrap circuit, its power consumption must be limited. Setting the maximum power at $P_{Z,max} = 0.5\,\mathrm{W}$

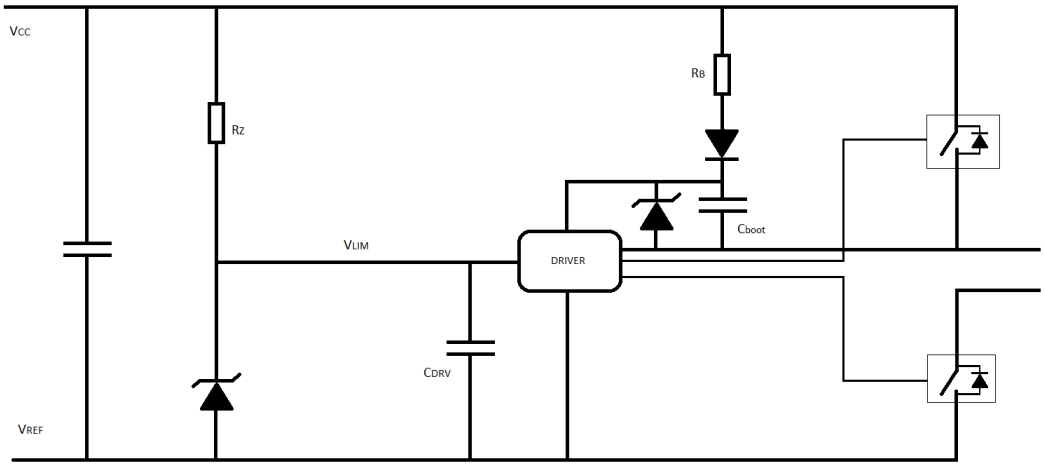


Figure 4.4.4: Elementary cell driver supply - modified

$$I_Z < \frac{P_{Z,max}}{V_Z} = \frac{0.5\,\mathrm{W}}{10\,\mathrm{V}} = 50\,\mathrm{mA}$$

Hence, the resistance value shall be

$$R_Z > \frac{V_{CC} - V_{LIM}}{I_Z} = \frac{42\,\mathrm{V} - 10\,\mathrm{V}}{50\,\mathrm{mA}} \approx 700\,\Omega$$

For each cell, a different value is picked, because of different values of V_{CC} (the nominal steady-state voltage):

$$R_{Z,1} = 100\,\Omega\ ,\ R_{Z,2} = 1\,\mathrm{k}\Omega\ ,\ R_{Z,3} = 1.5\,\mathrm{k}\Omega$$

For what concerns resistor R_B, a value of $150\,\Omega$ is selected for all cells bootstrap circuit. Two are the reasons:

- the sizing refers to the same concept of (voltage across resistor is not so high, approximately 5 V, recalling the 10 V voltage drop across the bootstrap zener diode)
- there is a direct electrical connection between the input and the output voltage even when the system is not active, but this is not much of a problem. Better insight of the problem is given in Section 4.4.3.

To wrap-up, it is worth notice that this solution may lead to a new set of problems, in particular for what concerns electromagnetic issue; this because there are components (such as the drivers) that are not refereed to ground potential. Some other problems may arise for what concern MOSFET gate driving, such as overcurrents when driving MOSFETs due to the capacitive input, and input gate-source voltage ringing which may cause multiple on/off switching of the transistor. This type of study is related to PCB requirements and it goes beyond the scope of this work.

4.4.2 Control Signal Decoupling

The SCC topology chosen deals with components whose reference voltage is not connected to ground. This means that the control signal cannot come directly from the timing circuit (it can be a microcontroller with PWM available), because its output signal is referred to ground potential (note that this is good also for decoupling the power signals from the control signals).

In order to solve this problem, an optocoupler can be employed. In order to complete this task, it is necessary to point out some implementation issues.

Resorting to the schematic in Figure 4.4.5, many possible solutions are available. For this project, the solution selected is (d).

Before discussing the topology choice, a brief description of the system behavior is discussed. By looking at the driver point of view, the transistor makes the driver input voltage to switch from its reference voltage and its supply voltage. The resistor connected either to the BJT collector node, or to the emitter node, must be sized to ensure the BJT to work in saturation region ($V_{CE,sat} \approx 0.4\,\mathrm{V}$). The sizing has to be done with respect to the current it is supposed to flow:

$$V_{CE} = V_{CC} - R_{BJT} \cdot I_{CE} < V_{CE,sat}$$

$$R_{BJT} > \frac{V_{CC} - V_{CE,sat}}{I_{CE}}$$

Typical values of collector current on the BJT side are of the order of 1 mA to 10 mA. Choosing a worst case value of 2 mA

$$R_{BJT} > \frac{10\,\mathrm{V} - 0.4\,\mathrm{V}}{2\,\mathrm{mA}} = 4.8\,\mathrm{k\Omega}$$

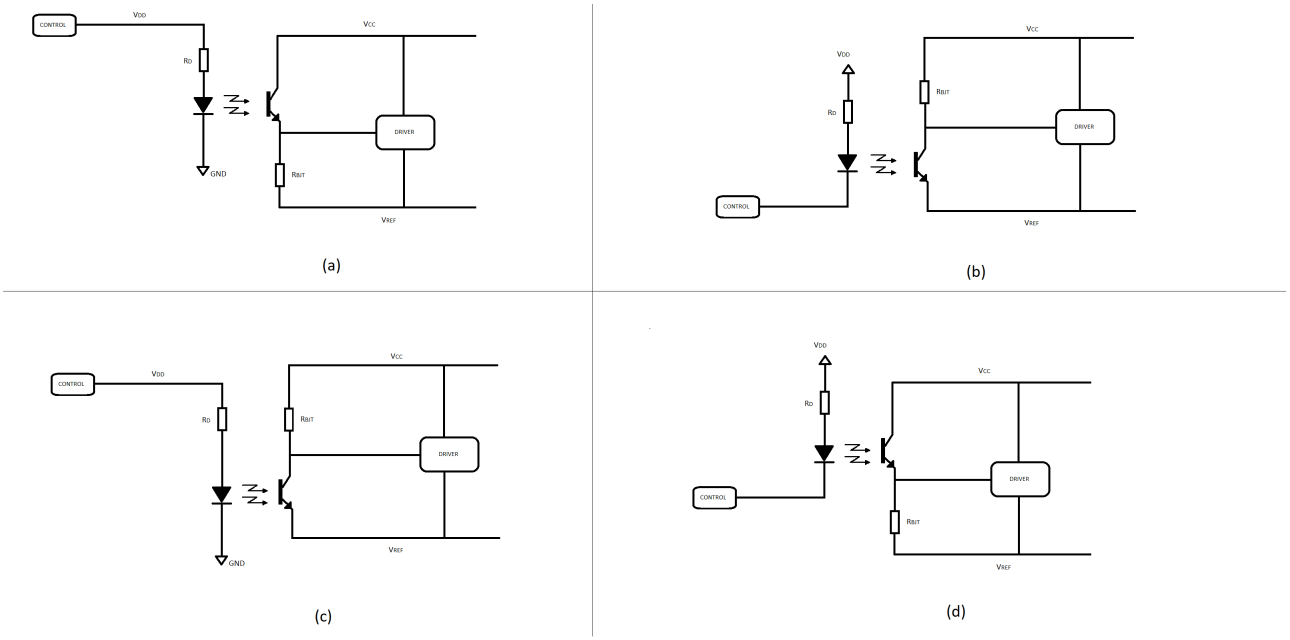


Figure 4.4.5: Optocoupler circuit schematic

This is not the only boundary condition that has to be met: recalling there is a zener diode, that diode must be kept in breakdown conditions, hence when the transistor conducts, a resistor divider shows up, and $V_{LIM} > 10\,\mathrm{V}$ must be guaranteed.

$$\frac{V_{LIM}}{V_{CC}} < \frac{1}{1+\frac{R_Z}{R_{BJT}}} \quad \rightarrow \quad R_{BJT} > \frac{R_Z}{\frac{V_{CC}}{V_{LIM}}-1} = \frac{1.5\,\mathrm{k\Omega}}{\frac{42\,\mathrm{V}}{10\,\mathrm{V}}-1} \approx 500\,\Omega$$

This result is not in contrast to the limit obtained before.

Now, by looking at the controller point of view, the photo-diode has to be driven with a suitable current in order to correctly drive the BJT (current transfer ratio, CTR, parameter).

Typically, the current needed for the photo-diode to correctly work is about some tens of mA. Unfortunately, any microcontroller current capability is very limited; hence, an extra driving stage is needed for the diode (see Figure 4.4.6).

Assuming:

- the controller supply voltage to be $V_{DD} = 3.3\,\mathrm{V}$
- the diode current set at $I_D = 15\,\mathrm{mA}$

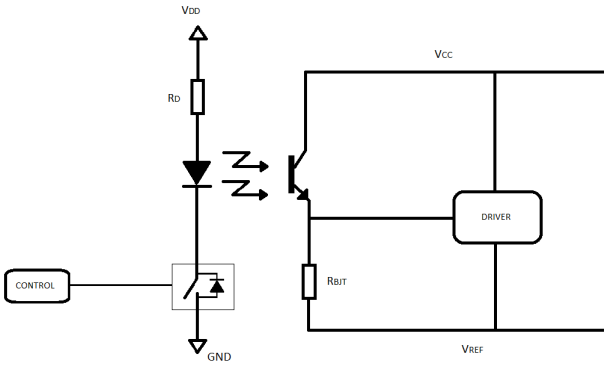


Figure 4.4.6: Optocoupler circuit schematic, with photo-diode driver

– the diode forward voltage to be $V_{fw} = 1.2\,\mathrm{V}$

the required resistance is

$$R_D \approx \frac{V_{DD} - V_{fw}}{I_D} = \frac{3.3\,\mathrm{V} - 1.2\,\mathrm{V}}{15\,\mathrm{mA}} = 140\,\Omega$$

Many are there reasons related to the choice of solution (d):

- at first glance, the most suited solution may appear to be driving the BJT as a low-side transistor. Unfortunately, from simulations it ended up to be a very risky solution: if R_{BJT} is incorrectly sized, the BJT may not enter saturation and the voltage may be above 2 V. This is not a problem only for what concerns power dissipation, but also because of the driver input sensibility to recognize a high/low voltage; typically the threshold is set around 1.5 V, which means that a MOSFET does not switch off as expected, leading to dangerous cross-conduction phenomena. This is not a problem when the BJT is connected as high-side transistor because, even if the voltage drop would be of 2 V, the voltage threshold is satisfied anyway (8 V).

- since an extra switch is needed to drive the photo-diode, it is better to use an n-type MOSFET, in a low-side fashion. This fixes the diode-side type of connection.

- using as a reference the connection of the diode, it must be defined the type of connection of the BJT; this is also related to the control signal, if it has to

be an inverted, or a non-inverted, one. To correctly choose, it is important to notice that if the system has to be stalled for any reason, it must not dissipate. Hence, the topology in Figure 4.4.6 allows keep the system off from switching, and without having extra conduction paths.

To better explain, assuming the input control voltage to be grounded, the MOSFET does not conduct, therefore the diode, too. Being the photo-diode switched off, the BJT cannot conduct; hence, the pull-down resistor (R_{BJT}) keeps the driver input voltage at logical '*0*'. It means that both sides are not conducting, and this cannot be achieved otherwise.

4.4.3 Start-up Issues

For what concerns the pre-charging phase, some points have to be discussed. One thing is for sure, the converter cannot be driven directly in steady-state cyclic condition, either because the flying capacitors are not already charged and we would have a too-high current through capacitors and MOSFETs, either because the not all of the drivers are supplied, so it would be difficult to run the system.

To correctly start up the system, it is necessary to look first at the environment the SCC has to work in, both at the input, and at the output side. Referring to the simplified schematic of Figure 4.1.2 some observations can be pointed out.

First thing to take care of is the analysis of the initial conditions. Since the output voltage is already charged at approximately 14 V, the start-up procedure must be studied in deep, because some parasitic diodes of the switched-capacitors converter may be forward biased unexpectedly (see Figure 4.4.7). The selected solution to start-up the system is, among the others, the safest, easiest and most flexible; it can be even used in case the initial output voltage is null.

Starting from the assumption that both capacitors are completely discharged, and that diodes are ideal and not in conduction (no voltage drop across them), the quiescent point can be identified as the initial condition

$$V_{C1} = V_{C1,H} - V_{C1,L} = 0 \quad \rightarrow \quad V_{C1,H} = V_{C1,L} = V_o$$

$$V_{C2} = V_{C2,H} - V_{C2,L} = 0 \quad \rightarrow \quad V_{C2,H} = V_{C2,L} = V_o$$

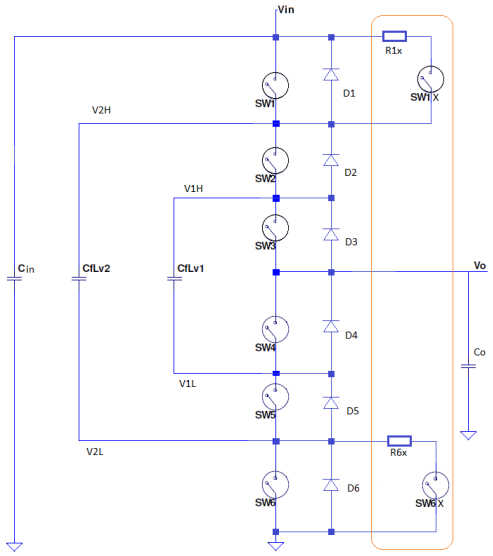


Figure 4.4.7: Parasitic diodes included in the model

At this point, the only MOSFETs that can be activated (without potential damage) are $SW1$ and $SW6$, because their drivers are the only one already supplied by the input voltage. But this is not enough, because the only way to have a control on the pre-charging process is to introduce parallel branches that allow to limit the current flow (by means of a resistor); hence, the switches that are going to be activated are $SW1$x and $SW6$x.

Here, it is important to care about timing: the two switches will not be turned on simultaneously, but the first one to be activated has to be $SW6$x. Imposing $V_{2,L} = V_{2,H} = 0$,

$$V_{D3} = V_o - V_{1,H}$$

$$V_{D2} = V_{1,H} - V_{2,H}$$

The voltage drop across the two diodes turns out to be

$$V_{D3} + V_{D2} = V_o - V_{2,H} = V_o$$

which means that if $V_o > 0$, capacitor C_2 is charged at $V_{C2} = V_o$ with a current peak limited by $R6$x.

By keeping $SW6$x conducting, $SW5$ can be activated too in order to charge C_1 (by implicitly activating $D3$) at $V_{C1} = V_o$

Recalling that now $V_{C2} = V_{C1} = V_o$, by switching off both $SW6x$ and $SW5$, the new quiescent point (always defined by the fact that no current flows through the diodes) becomes

$$V_{C1,L} = V_o \quad , \quad V_{C1,H} = V_{C1,L} + V_{C1} = 2 \cdot V_o$$

$$V_{C2,L} = V_o \quad , \quad V_{C2,H} = V_{C2,L} + V_{C2} = 2 \cdot V_o$$

If the switch $SW1x$ is now turned on, then

$$V_{2,H} = V_{in} \quad \rightarrow \quad V_{2,L} = V_{2,H} - V_{C2} = V_{in} - V_o$$

$$V_{D5} = V_{2,L} - V_{1,L}$$

$$V_{D4} = V_{1,L} - V_o$$

The voltage drop across the two diodes turns out to be

$$V_{D5} + V_{D4} = V_{2,L} - V_o = V_{in} - 2V_o$$

which means that if $V_{in} - 2V_o > 0$, capacitor C_2 is charged at $V_{C2} = V_{in} - V_o$ with a current peak limited by $R1x$ (it is worth notice that if $V_{in} - 2V_o < 0$, the isolation diode in Figure 4.1.2 does not allow current to flow backward).

The timing diagram is shown in Figure 4.4.8

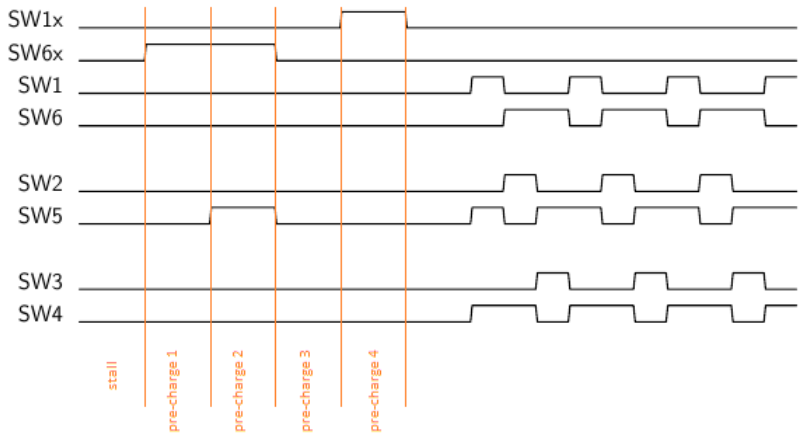


Figure 4.4.8: Start up timing diagram, and steady state control

Note that this specific type of start-up procedure is worth if the output voltage is already at a voltage close to the steady state one.

For this project, the switches of the start-up branches are taken of the same technology of those used for steady-state operation. An extra resistor is used to reduce current peaks.

It is worth notice some more implementation aspects. The transistors for the pre-charge phase are connected in such a way that they share the source terminal with the transistors that play a role at steady state; for what concerns the low side MOSFET, this is mainly because otherwise it can not be considered a low-side transistor, hence its source terminal must be connected to ground potential; while, for the high-side transistor, the aforementioned connection is to save space and components: since the two transistors are never meant to work simultaneously, that allows to share the bootstrap capacitor. But more importantly both synchronous drivers for the steady-state, and the pre-charge, share the same supply, thanks to the fact that they never have to be active at the same time (Figure 4.4.9).

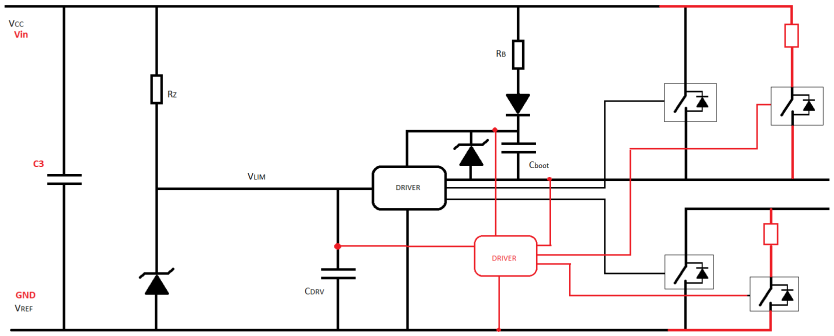


Figure 4.4.9: Elementary cell driver supply - input cell, with pre-charge branches

4.4.4 Input and Output Capacitors

The input and the output capacitors are both stressed components in this topology, most importantly because they have to bear the same current peaks of the SCC internal capacitors. As a result, they are chosen to be of the same size and technology of the flying capacitors. Just to recall, the single component characteristics are listed again:

– $C = 50\,\mu\text{F}$

- tolerance 10%
- $ESR = 6\,\text{m}\Omega$
- $I_{rms} = 15\,\text{A}$
- $V_{max} = 550\,\text{V}$

The total number of parallel capacitors is 8, for both C_{in} and C_{out}, as well as for the flying capacitors, so that the currents are (theoretically) balanced for each single capacitor.

4.4.5 Protections

Since the converter is not regulated, and the output voltage range is not so wide, it is important to introduce a control on the input voltage.

Two are the main phenomena that occur:

- load damp: it is referred to the temporary disconnection of the load, causing overvoltages peaks that may last $\approx 100\,\text{ms}$
- engine switching off: the alternator does not give power to the load anymore

In both conditions the converter must not be active, to avoid any damage.

Two different problem arise, what kind of protection circuit, and the supply of the control system.

Thresholds and Operating Conditions

Three different thresholds have been introduced, at 30 V, 40 V and 50 V, by means of three comparators (see Figure 4.4.10).

Employing a microcontroller for the timing control, it is possible to use it to distinguish between different operating conditions.

1. START:

   Default state at start up, when the controller supply start working. The input voltage is again below 30 V threshold The system is still completely shut down. Wait for the voltage to be above 30 V, to exit this state.

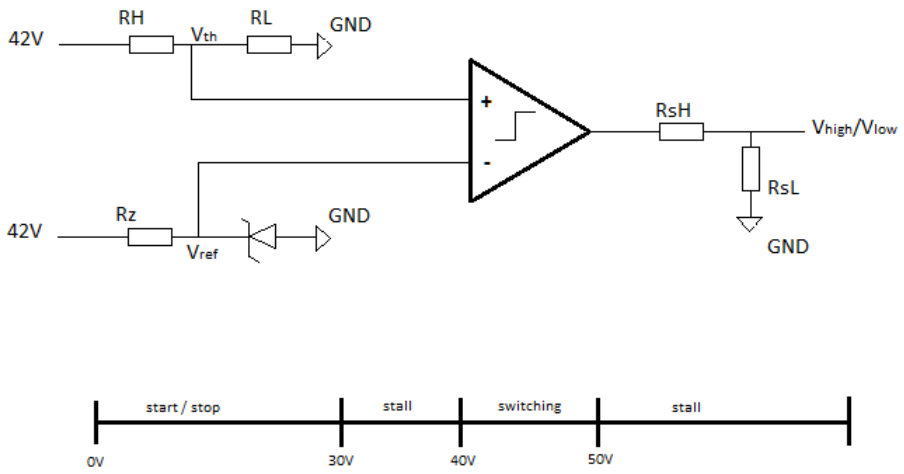


Figure 4.4.10: Thresholds comparator circuit

2. STALL40V:

   The 30 V threshold has been overcome, or the input voltage is again below 40 V threshold. The start-up procedure (Figure 4.4.8) can be cyclically repeated:

   $stall - preCharge1 - preCh2 - preCh3 - preCh4 - stall - stall - preCh1 - ...$

   This, in order to keep the capacitors voltage close to the steady-state, ready to start switching at full load. The system cannot exit from this state, unless the running pre-charging procedure is ending.

3. SWITCHING:

   The 40 V threshold has been overcome, or the input voltage is again below 50 V threshold. The converter can work at full load.

4. STALL50V:

   The 50 V threshold has been overcome. The system is momentarily not switching: the start-up procedure is stopped at phase 2.

   $$stall - preCharge1 - preCharge2 - preCharge2 - preCharge2 - ...$$

   The system cannot exit from this state, unless a $preCharge2$ state is reached, and the start-up procedure is completely executed, before starting to switch again.

The firmware behavior is described as a state flow chart in Figure 4.4.11

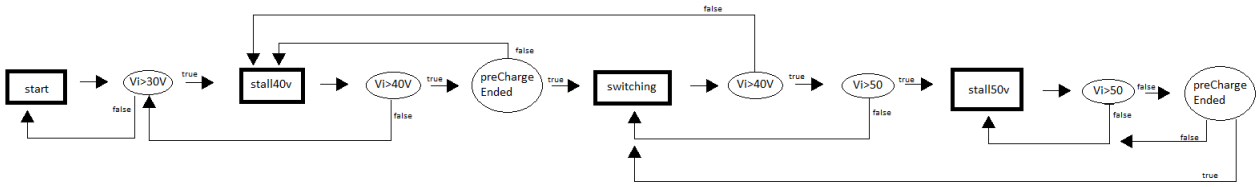


Figure 4.4.11: Firmware state flow diagram

Control System Supply Strategies

The system deals with two batteries. The main strategy behind it is related to isolate *key-off* loads, which means those electrical loads which draw power even when the ignition is off (e.g., clock, theft alarm, keyless entry), causing battery (total) discharge of a car if not used for too long.

Other reasons why not all of the electronics and electro-mechanic actuators in a vehicle have been referred to the high-voltage side is due to the fact that not all components can be easily adapted, or the fact that they do not improve the system characteristics, leading to no benefit at all.

One last problem still need to be solved: to determine to which supply rail the protection circuit shall be connected to. Of course those systems, as well as the microcontroller, do not have to be supplied by the *ignition* rail, but rather from the *key-off* rail. Independently of the rail the ignition system is connected to, the voltage to be sensed to start the system is the non-isolated rectified alternator voltage (Figure 4.4.12).

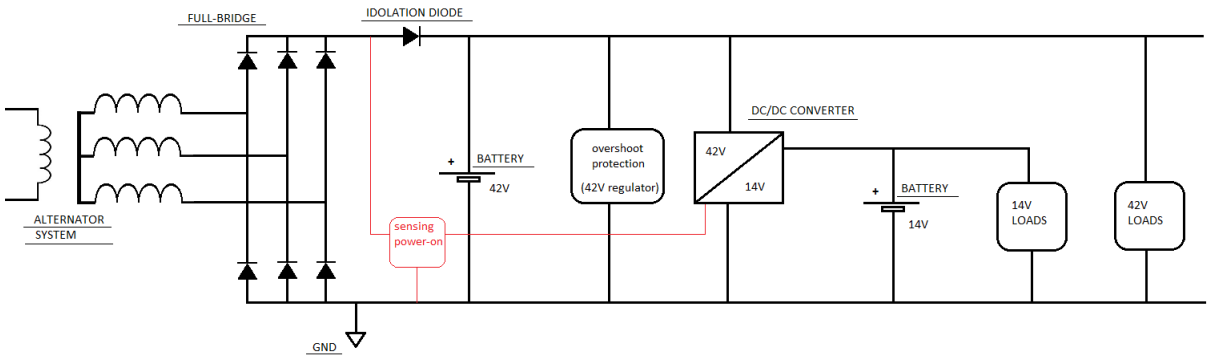


Figure 4.4.12: power sensing schematic

The system can be made (almost) consumption-free when the engine is off if the technique presented in Figure 4.4.13 is adopted. At least, the supply rail to which the systems are supplied from can be decided independently of the distinction, and can be connected to the most convenient battery rail.

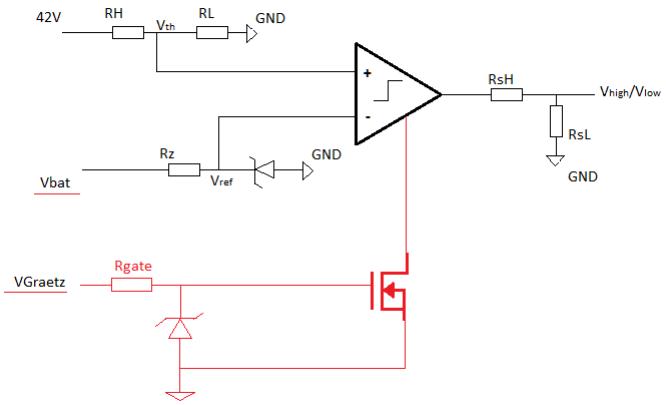


Figure 4.4.13: power sensing implementation - source independent

CHAPTER 5

Buck Topology Design

The target application is the same presented in Section 4.1.

At first, a 1-phase solution is developed, but it will be demonstrated that it may not be the best solution (too much stressed). Hence, a multi-phase technique is adopted.

5.1 One-phase buck design constraints

At first, the application specifications are needed. The specifications presented in [18], are reported in Table 5.1.

First step is recalling that a buck converter performs better in continuous conduction mode (CCM), so it will be designed to work in that condition.

Choosing some key-parameters:

- output voltage fixed at $V_o = 14\,\mathrm{V}$

Vin	$30\,\mathrm{V} - 50\,\mathrm{V}$
Vo	$11\,\mathrm{V} - 16\,\mathrm{V}$
$Power$	$1\,\mathrm{kW}$
ΔV_o	$300\,\mathrm{mV}$
ΔI_o	$1\,\mathrm{A}$

Table 5.1: converter specifications

- switching frequency $f_{sw} = 100\,\text{kHz}$, due to the medium-high power level
- resorting to the ΔI_o specification, the minimum power level for *CCM* (continuous conduction mode) boundary is

$$P_{min} = V_o \cdot I_{o,min} = V_o \cdot \Delta I_o/2 = 14\,\text{V} \cdot 500\,\text{mA} = 7\,\text{W}$$

It is worth notice that

$$\frac{7\,\text{W}}{1\,\text{kW}} < 1\%$$

In oreder to have an inductor not too much expensive, the minimum power is set at

$$P_{min} = 10\% \cdot P_{max} = 100\,\text{W}$$

Hence, some other specifications can be derived from the complete set of specifications and key-parameters:

- $d_{max} = \dfrac{V_o}{V_{in,min}} = \dfrac{14\,\text{V}}{30\,\text{V}} = 0.47$
- $d_{min} = \dfrac{V_o}{V_{in,max}} = \dfrac{14\,\text{V}}{50\,\text{V}} = 0.28$
- $I_{o,max} = \dfrac{P_{max}}{V_o} = \dfrac{1\,\text{kW}}{14\,\text{V}} = 71.4\,\text{A}$
- $I_{o,min} = \dfrac{P_{min}}{V_o} = \dfrac{100\,\text{W}}{14\,\text{V}} = 7.1\,\text{A}$
- $R_{L,min} = \dfrac{V_o^2}{P_{max}} = \dfrac{(14\,\text{V})^2}{1\,\text{kW}} \approx 0.2\,\Omega$
- $R_{L,max} = \dfrac{V_o^2}{P_{min}} = \dfrac{(14\,\text{V})^2}{100\,\text{W}} \approx 2\,\Omega$

At this point the discrete components can be designed.

inductor L the inductor design equation is

$$L > \frac{V_o \cdot (1 - d_{min})}{\Delta I_o \cdot f_{sw}} = \frac{14\,\text{V} \cdot (1 - 0.28)}{1\,\text{A} \cdot 100\,\text{kHz}} = 100\,\mu\text{H}$$

The inductance value selected is $L = 150\,\mu\text{H}$.

The peak current the inductor has to sustain is

$$I_{L,max} = I_{o,max} + \frac{V_o \cdot (1 - d_{min})}{2 \cdot L \cdot f_{sw}} = 71.4\,\text{A} + \frac{14\,\text{V} \cdot (1 - 0.28)}{2 \cdot 150\,\mu\text{H} \cdot 100\,\text{kHz}} = 71.8\,\text{A}$$

The RMS-current of the inductor is approximately

$$I_{L,rms} \approx I_{o,max} = 71.4\,\text{A}$$

high-side MOS Choosing the maximum drain-source voltage, when turned on, to be

$$V_{ds,on} < 2\% \cdot V_{in,min} = 0.02 \cdot 30\,\text{V} = 0.6\,\text{V}$$

Hence, the maximum equivalent resistance of the MOSFET device must satisfy:

$$r_{ds,on-COLD} < \frac{r_{ds,on-HOT}}{1.8} = \frac{V_{ds,on-max}}{I_{L,max}} \cdot \frac{1}{1.8} = \frac{0.6\,\text{V}}{1.8 \cdot 71.8\,\text{A}} \approx 4\,\text{m}\Omega$$

The rated voltage must be $V_{mos,rated} > 50\,\text{V}$.

The RMS-current that flows into the device is

$$I_{mos,rms} \approx I_{o,max} \cdot \sqrt{d_{max}} = 71.4\,\text{A} \cdot \sqrt{0.47} = 48.8\,\text{A}$$

Hence, the static power loss of the device can be defined as

$$P_{loss,STATIC} < r_{ds,on-HOT} \cdot I_{mos,rms}^2 = \frac{0.6\,\text{V}}{71.8\,\text{A}} \cdot (48.8\,\text{A})^2 = 20\,\text{W}$$

Assuming a model for the dynamic power loss as the one in Appendix B.2, the dynamic power losses can be computed as

$$P_{loss,DYNAMIC} \approx \frac{f_{sw}}{2} \cdot (t_{on} \cdot V_{ds,B} \cdot I_{ds,A} + t_{off} \cdot V_{ds,A} \cdot I_{ds,B})$$

Further assuming:

- the MOSFET turn-on and turn-off time to be equal

$$t_{on} = t_{off} = t_s$$

- the turn-on, turn-off time to be smaller than 1% of the switching time

$$t_{on}, t_{off} < \frac{T_{sw}}{100} = 100\,\text{ns}$$

– the MOSFET dynamic losses to be of the same order of magnitude of the MOSFET static losses

$$P_{loss,DYNAMIC} \approx P_{loss,STATIC} \approx 20\,\mathrm{W}$$

– the voltage and current to be respectively

$$V_{ds,A-B} = V_{in,max} = 50\,\mathrm{V}$$

$$I_{ds,A-B} = I_{o,max} = 71.4\,\mathrm{A}$$

The estimated dynamic power loss is

$$P_{loss,DYNAMIC} < \frac{100\,\mathrm{kHz}}{2} \cdot 2 \cdot (100\,\mathrm{ns} \cdot 50\,\mathrm{V} \cdot 71.4\,\mathrm{A}) = 35.7\,\mathrm{W}$$

diode The average diode current is

$$I_{D,avg} = I_{o,max} \cdot (1 - d_{min}) = 71.4\,\mathrm{A} \cdot (1 - 0.28) = 51.4\,\mathrm{A}$$

If the diode forward voltage is taken at $V_{D,fw} = 1\,\mathrm{V}$, the power the diode needs to dissipate per unit voltage is

$$\frac{P_{D,loss}}{1\,\mathrm{V}} = \frac{(V_{D,fw} \cdot I_{D,avg})}{V_{D,fw}} = \frac{1\,\mathrm{V} \cdot 51.4\,\mathrm{A}}{1\,\mathrm{V}} = 51.4\,\mathrm{W/V}$$

If a MOSFET is used in place of the diode, hence implementing a synchronous converter

$$I_{synch,rms} = I_{o,max} \cdot \sqrt{1 - d_{max}} = 71.4\,\mathrm{A} \cdot \sqrt{1 - 0.28} = 60.6\,\mathrm{A}$$

Picking up the same upper bound for the equivalent drain-source resistance as for the high-side MOSFET, it follows that the static and dynamic power loss can be computed as

$$r_{ds,on-HOT} = 1.8 \cdot r_{ds,on-COLD} = 1.8 \cdot 4\,\mathrm{m\Omega}$$

$$P_{loss,STATIC} < r_{ds,on-HOT} \cdot I^2_{mos,rms} = 1.8 \cdot 4\,\mathrm{m\Omega} \cdot (60.6\,\mathrm{A})^2 = 15\,\mathrm{W}$$

$$P_{loss,DYNAMIC} < \frac{100\,\mathrm{kHz}}{2} \cdot 2 \cdot (100\,\mathrm{ns} \cdot 50\,\mathrm{V} \cdot 71.4\,\mathrm{A}) = 35.7\,\mathrm{W}$$

capacitor C_{out} assuming to take an output capacitor of ceramic type, the inductor ripple current is needed

$$\Delta I_L = \frac{V_o \cdot (1 - d_{min})}{f_{sw} \cdot L} = 0.7\,\text{A}$$

The output capacitor will be:

$$C_{out} = \frac{1}{8 \cdot f_{sw}} \cdot \frac{\Delta I_{L,max}}{\Delta V_o} = \frac{1}{8 \cdot 100\,\text{kHz}} \cdot \frac{0.7\,\text{A}}{0.3\,\text{V}} = 2.8\,\mu\text{F}$$

A normalized value $C_{out} = 3.3\,\mu\text{F}$ is selected.

The capacitor must be rated for $V_{Co,rated} > 14\,\text{V}$; hence a 25 V component is chosen.

For what concerns the RMS-current:

$$I_{Co,rms} = \frac{\Delta I_{L,max}}{\sqrt{12}} = \frac{0.7\,\text{A}}{\sqrt{12}} \approx 0.2\,\text{A}$$

capacitor C_{in} The voltage the capacitor has to sustain must be $V_{Ci,rated} > 50\,\text{V}$ (a 63 V component can be safely chosen).

The RMS-current the input capacitor is asked to tolerate is

$$I_{Ci,rms} = I_{o,max} \cdot \sqrt{d_{max} \cdot (1 - d_{max})} = 71.4\,\text{A} \cdot \sqrt{0.47 \cdot 0.53} \approx \frac{71.4\,\text{A}}{2} = 35.7\,\text{A}$$

For what concerns the capacitance value, since no specification is given about the input filter characteristic, the cheapest component can be selected.

As a result, all the components are really much stressed. Hence, the it may be worth resorting to a multiphase buck topology. The design procedure will be developed in detail in next section.

5.2 Multiphase design constraints

Paralleling different buck power stages means to have more than one copy of the same power stage. Each replica has its own set of inductor, transistors, drivers, but they all share the output and input capacitors (Figure 5.2.1).

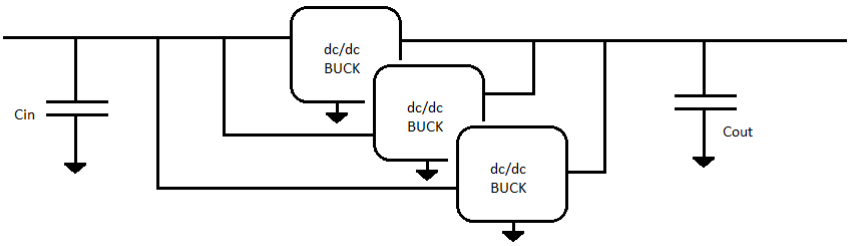


Figure 5.2.1: simplified schematic of a multi-phase buck dc/dc converter

\ \ \	$N_{phi} = 1$	$N_{phi} > 1$
Vin	$30\,\mathrm{V} - 50\,\mathrm{V}$	$30\,\mathrm{V} - 50\,\mathrm{V}$
Vo	$11\,\mathrm{V} - 16\,\mathrm{V}$	$11\,\mathrm{V} - 16\,\mathrm{V}$
$Power$	$1\,\mathrm{kW}$	$(\frac{1\,\mathrm{kW}}{N_{phi}}) \times N_{phi}$
ΔV_o	$300\,\mathrm{mV}$	$300\,\mathrm{mV}$
ΔI_o	$1\,\mathrm{A}$	$\frac{(N_{phi} \times 1\,\mathrm{A})}{N_{phi}}$

Table 5.2: converter specifications

When working at steady-state, each phase is sequentially activated after a spacing interval of (T_{sw}/N_{ϕ}), being N_{ϕ} the total number of phases, and being T_{sw} the time it takes for each phase to be activated again; this means that the output ripple frequency turns out to be $f_{sw,out} = N_{\phi} \cdot f_{sw,\phi}$.

Paralleling different de-phased buck converters has many advantages related to components stresses, whether for the shared capacitors, whether for the components in each individual phase, at the expense of larger area, volume and system complexity.

How can each component be less stressed, it will be discussed within the design procedure.

First step in designing a multiphase dc/dc converter is to select the number of phases. In Table 5.2, the new specifications for each phase are derived as a function of the number of phases (highlighted in round brackets).

For the target application, the key-parameters are selected as before:

- output voltage fixed at $V_o = 14\,\mathrm{V}$

- switching frequency $f_{sw} = 100\,\text{kHz}$, due to the medium-high power level
- The number of phase has to be selected, too. For this design $N_{phi} = 3$ (refer to the last comment in Appendix B.4, to know what the choice is due to).
- Resorting to the ΔI_o specification, the minimum power level for *CCM* (continuous conduction mode) boundary is

  $$P_{min,\phi} = V_o \cdot I_{\phi,min} = V_o \cdot \Delta I_\phi/2 = 14\,\text{V} \cdot 1.5\,\text{A} = 21\,\text{W}$$

  It is worth notice that

  $$\frac{P_{min,\phi}}{P_{max,\phi}} = \frac{21\,\text{W}}{333\,\text{W}} \approx 6\%$$

  In oreder to have an inductor not too much expensive (even if in this instance, it not so much different), also in this case the minimum power is set at

  $$P_{min} = 10\% \cdot P_{max} = 33\,\text{W}$$

The missing parameters needed to complete the sizing of the components is listed:

- $d_{\phi,max} = \dfrac{V_o}{V_{in,min}} = \dfrac{14\,\text{V}}{30\,\text{V}} = 0.47 \rightarrow d_{max} = N_\phi \cdot d_{\phi,max} = 1.41$
  The value seems to be quite high if compared with the last comment of Appendix B.4. In this project it will be accepted because it is expected that the low voltage only show up when the engine start working (and so the alternator), or that this working condition is only transient.
- $d_{min} = \dfrac{V_o}{V_{in,max}} = \dfrac{14\,\text{V}}{50\,\text{V}} = 0.28 \rightarrow d_{max} = N_\phi \cdot d_{\phi,max} = 0.84$
- $I_{\phi,max} = \dfrac{P_{\phi,max}}{V_o} = \dfrac{333\,\text{W}}{14\,\text{V}} = 23.8\,\text{A}$
- $I_{\phi,min} = \dfrac{P_{min}}{V_o} = \dfrac{33\,\text{W}}{14\,\text{V}} = 2.4\,\text{A}$
- $R_{L,min-\phi} = \dfrac{V_o^2}{P_{\phi,max}} = \dfrac{(14\,\text{V})^2}{333\,\text{W}} \approx 0.6\,\Omega$
- $R_{L,max-\phi} = \dfrac{V_o^2}{P_{min}} = \dfrac{(14\,\text{V})^2}{33\,\text{W}} \approx 6\,\Omega$

To start, the components that are not shared between each phase are taken into account, since the procedure is not much different from the 1-phase.

inductor L the inductor design equation is

$$L > \frac{V_o \cdot (1 - d_{\phi,min})}{\Delta I_\phi \cdot f_{sw}} = \frac{14\,\mathrm{V} \cdot (1 - 0.28)}{3\,\mathrm{A} \cdot 100\,\mathrm{kHz}} = 33\,\mu\mathrm{H}$$

The inductance value selected is $L = 47\,\mu\mathrm{H}$.

The peak current the inductor has to sustain is

$$I_{L,max} = I_{\phi,max} + \frac{V_o \cdot (1 - d_{\phi,min})}{2 \cdot L \cdot f_{sw}} = 23.8\,\mathrm{A} + \frac{14\,\mathrm{V} \cdot (1 - 0.28)}{2 \cdot 47\,\mu\mathrm{H} \cdot 100\,\mathrm{kHz}} = 24.2\,\mathrm{A}$$

The RMS-current of the inductor is approximately

$$I_{L,rms} \approx I_{\phi,max} = 23.8\,\mathrm{A}$$

high-side MOS Choosing the maximum drain-source voltage, when turned on, to be

$$V_{ds,on} < 2\% \cdot V_{in,min} = 0.02 \cdot 30\,\mathrm{V} = 0.6\,\mathrm{V}$$

Hence, the maximum equivalent resistance of the MOSFET device must satisfy:

$$r_{ds,on-COLD} < \frac{r_{ds,on-HOT}}{1.8} = \frac{V_{ds,on-max}}{I_{L,max}} \cdot \frac{1}{1.8} = \frac{0.6\,\mathrm{V}}{1.8 \cdot 24.2\,\mathrm{A}} \approx 13\,\mathrm{m\Omega}$$

The rated voltage must be $V_{mos,rated} > 50\,\mathrm{V}$.

The RMS-current that flows into the device is

$$I_{mos,rms} \approx I_{\phi,max} \cdot \sqrt{d_{\phi,max}} = 23.8\,\mathrm{A} \cdot \sqrt{0.47} = 16.5\,\mathrm{A}$$

Hence, the static power loss of the device can be defined as

$$P_{loss,STATIC} < r_{ds,on-HOT} \cdot I^2_{mos,rms} = \frac{0.6\,\mathrm{V}}{23.8\,\mathrm{A}} \cdot (16.5\,\mathrm{A})^2 = 6.8\,\mathrm{W}$$

Assuming a model for the dynamic power loss as the one in Appendix B.2, the dynamic power losses can be computed as

$$P_{loss,DYNAMIC} \approx \frac{f_{sw}}{2} \cdot (t_{on} \cdot V_{ds,B} \cdot I_{ds,A} + t_{off} \cdot V_{ds,A} \cdot I_{ds,B})$$

Further assuming:

– the MOSFET turn-on and turn-off time to be equal

$$t_{on} = t_{off} = t_s$$

– the turn-on, turn-off time to be smaller than 1% of the switching time

$$t_{on}, t_{off} < \frac{T_{sw}}{100} = 100\,\text{ns}$$

– the MOSFET dynamic losses to be of the same order of magnitude of the MOSFET static losses

$$P_{loss,DYNAMIC} \approx P_{loss,STATIC} \approx 5\,\text{W}$$

– the voltage and current to be respectively

$$V_{ds,A-B} = V_{in,max} = 50\,\text{V}$$

$$I_{ds,A-B} = I_{\phi,max} = 23.8\,\text{A}$$

The estimated dynamic power loss is

$$P_{loss,DYNAMIC} < \frac{100\,\text{kHz}}{2} \cdot 2 \cdot (100\,\text{ns} \cdot 50\,\text{V} \cdot 23.8\,\text{A}) = 12\,\text{W}$$

diode The average diode current is

$$I_{D,avg} = I_{o,max} \cdot (1 - d_{min}) = 23.8\,\text{A} \cdot (1 - 0.28) = 17.2\,\text{A}$$

If the diode forward voltage is $V_{D,fw} = 1\,\text{V}$, the power the diode needs to dissipate per unit voltage can be estimated as

$$\frac{P_{D,loss}}{1\,\text{V}} = \frac{(V_{D,fw} \cdot I_{D,avg})}{V_{D,fw}} = \frac{1\,\text{V} \cdot 17.2\,\text{A}}{1\,\text{V}} = 17.2\,\text{W/V}$$

If a MOSFET is used in place of the diode, hence implementing a synchronous converter

$$I_{synch,rms} = I_{\phi,max} \cdot \sqrt{1 - d_{\phi,max}} = 23.8\,\text{A} \cdot \sqrt{1 - 0.28} = 20.2\,\text{A}$$

Picking up the same upper bound for the equivalent drain-source resistance as for the high-side MOSFET, it follows that the static and dynamic power loss can be computed as

$$r_{ds,on-HOT} = 1.8 \cdot r_{ds,on-COLD} = 1.8 \cdot 13\,\text{m}\Omega$$

$$P_{loss,STATIC} < r_{ds,on-HOT} \cdot I^2_{mos,rms} = 1.8 \cdot 13\,\mathrm{m\Omega} \cdot (20.2\,\mathrm{A})^2 = 9.6\,\mathrm{W}$$

$$P_{loss,DYNAMIC} < \frac{100\,\mathrm{kHz}}{2} \cdot 2 \cdot (100\,\mathrm{ns} \cdot 50\,\mathrm{V} \cdot 23.8\,\mathrm{A}) = 12\,\mathrm{W}$$

capacitor C_{out} assuming to take an output capacitor of ceramic type, the inductor ripple current is needed

$$\Delta I_L = \frac{V_o \cdot (1 - d_{min})}{f_{sw} \cdot L} = 0.7\,\mathrm{A}$$

The output capacitor will be:

$$C_{out} > \frac{1}{8 \cdot f_{sw}} \cdot \frac{\Delta I_{L,max}}{\Delta V_o} = \frac{1}{8 \cdot 100\,\mathrm{kHz}} \cdot \frac{0.7\,\mathrm{A}}{0.3\,\mathrm{V}} = 2.8\,\mu\mathrm{F}$$

The capacitor must be rated for $V_{Co,rated} > 14\,\mathrm{V}$; hence a 25 V component is chosen.

For what concerns the RMS-current:

$$I_{Co,rms} = \frac{\Delta I_{L,max}}{\sqrt{12}} = \frac{0.7\,\mathrm{A}}{\sqrt{12}} \approx 0.2\,\mathrm{A}$$

Even if oversized, the component selected for this project is the same one used for the SCC converter:

$$C_o = 50\,\mu\mathrm{F} \quad , \quad ESR = 6\,\mathrm{m\Omega} \quad , \quad V_{rated} = 550\,\mathrm{V} \quad , \quad I_{rms} = 15\,\mathrm{A}$$

capacitor C_{in} The voltage the capacitor has to sustain must be $V_{Ci,rated} > 50\,\mathrm{V}$ (a 63 V component can be safely chosen).

The RMS-current the input capacitor is asked to tolerate is (refer to Appendix B.4)

$$I_{Ci,rms} = I_\phi \cdot \sqrt{N\left[(dN-1)^2\left(\frac{2}{N} - d\right) + (2 - dN)^2\left(d - \frac{1}{N}\right)\right]} \leq \frac{I_\phi}{2} =$$

$$= \frac{23.8\,\mathrm{A}}{2} = 12\,\mathrm{A}$$

For what concerns the capacitance value, since no specification is given about the input filter characteristic, the cheapest component can be selected.

The chosen component is the same one used for the flying capacitors design. Since the rms-current capability is 15 A, two of them are put in parallel.

$$C_{in} = 150\,\mu\text{F} \quad , \quad ESR = 3\,\text{m}\Omega \quad , \quad V_{rated} = 550\,\text{V} \quad , \quad I_{rms} = 30\,\text{A}$$

At this point it is possible to estimate an upper limit for the efficiency of the converter, working in the worst case scenario.

$$\eta_{max} = \frac{P_{load}}{P_{load} + P_{loss}}$$

Where

$$P_{loss} > 3 \cdot (P_{MOS,H-static} + P_{MOS,H-dynamic} + P_{MOS,L-static} + P_{MOS,L-dynamic}) =$$

$$= 3 \cdot (6.8\,\text{W} + 12\,\text{W} + 9.6\,\text{W} + 12\,\text{W}) = 116\,\text{W}$$

Hence

$$\eta < \frac{1\,\text{kW}}{1\,\text{kW} + 116\,\text{W}} \approx 0.90$$

In order to increase the efficiency, a MOSFET with lower drain-source resistance can be employed.

It has to be noticed that the system is supposed to implemented a current mode feedback compensation (see next section), hence the sensing resistors power losses are still missing.

5.3 Feedback Control

Working at high power implies dealing with high currents. The feedback control method adopted is the peak current mode control.

Since the system implements more than one phase, the current feedback must replicated for each phase. This is not true for the voltage feedback, which is unique.

Using Figure 5.3.1 as reference, it can be noticed that all signals to be sensed are approximately at 14 V. But the controller integrated circuit selected deals with very low input voltages (5 V), hence the signals to be sensed have to be conditioned.

The internal reference voltage of the controller is 700 mV. This voltage is used for the current sensing thresholds, as well as for the output voltage gain.

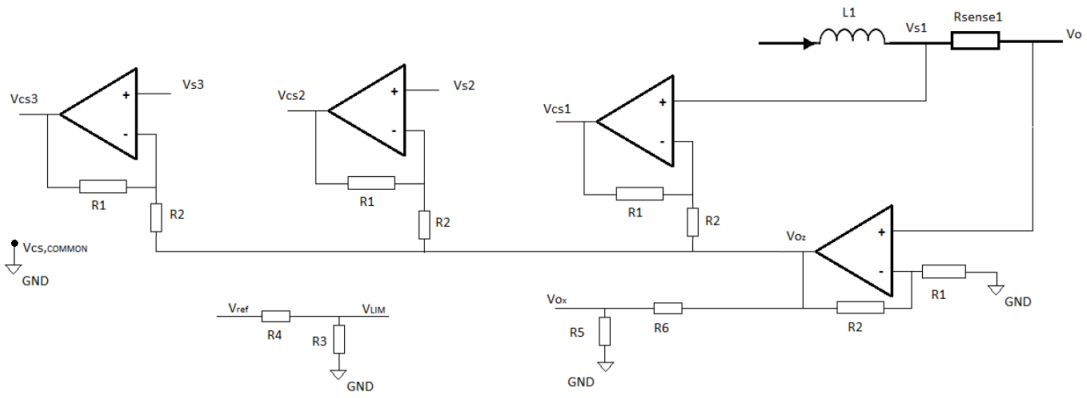


Figure 5.3.1: Conventional current sensing technique

5.3.1 Current Loop

Starting from the current loop, the manufacturer suggests the *emulated current sensing* technique (refer to Appendix B.3), but a conventional current sensing technique is implemented for this project (Figure 5.3.1).

Even if the input of the controller is already differential, the absolute voltage the pin can withstand is only 5 V. Hence the common reference pin is connected to ground, while the other current-sense pins will be connected to the output of the signal conditioning stages. The output of the each stage will be

$$V_{cs,x} = (V_{s,x} - V_o) \cdot \left(1 + \frac{R_1}{R_2}\right) = \Delta V_{s,x} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

Assuming to use a 2 mΩ sensing resistor, the maximum voltage drop across it can be estimated as

$$\Delta V_{s,x} = R_{s,x} \cdot I_{\phi,max} = 2\,\text{m}\Omega \cdot 24.2\,\text{A} \approx 50\,\text{mV}$$

Power dissipation ends up to be almost negligible compared to the losses related to the transistors

$$P_{sense} = R_{s,x} \cdot I_{L,rms}^2 = 2\,\text{m}\Omega \cdot (23.8\,\text{A})^2 \approx 1.2\,\text{W}$$

The thresholds of the current have to be set the same for all of the phases, since all of them have been designed for the same power level. At first, the gain of the

amplifying stage must be determined; setting the limit at 200 mV

$$\frac{R_1}{R_2} = \frac{V_{cs,x}}{\Delta V_{s,x}} - 1 = \frac{200\,\text{mV}}{50\,\text{mV}} - 1 = 3$$

Picking up $R_1 = 27\,\text{k}\Omega$, $R_2 = 10\,\text{k}\Omega$ (1% tolerance, refer to 5.3.2), the actual gain will be

$$1 + 2.7 = 3.7$$

The differential input signal (which has been transformed in a single ended signal by connecting the common node pin to ground potential) is internally increased by a 2.7 factor, and compared with a threshold derived from the reference voltage. Hence, the voltage threshold is

$$V_{LIM} = 2.7 \cdot \left(1 + \frac{R_1}{R_2}\right) \cdot \Delta V_{s,x} = 2.7 \cdot 3.7 \cdot 50\,\text{mV} = 500\,\text{mV}$$

The value of resistors R_3 and R_4 must be properly chosen to set the threshold

$$\frac{V_{LIM}}{V_{ref}} = \frac{1}{1 + \dfrac{R_4}{R_3}}$$

$$\frac{R_4}{R_3} = \frac{V_{ref}}{V_{LIM}} - 1 = \frac{700\,\text{mV}}{500\,\text{mV}} - 1 = 0.4$$

$$\frac{R_3}{R_4} = 2.5$$

Picking up $R_3 = 25.5\,\text{k}\Omega$ and $R_4 = 10.2\,\text{k}\Omega$, their tolerances have to be 1% for the system to behave as expected.

5.3.2 Voltage Loop

First thing to take care of is the fact that the system does not have to drain power from the battery when the engine is not running. Hence, the output voltage must be sensed elsewhere, to compare it with the internal reference voltage of the controller (a 2.5 V reference).

The adopted solution takes the signal at the output of the first operational amplifier stage (still refer to Figure 5.3.1). The voltage at the output of the amplifying stage is

$$V_{o,z} = V_o \cdot \left(1 + \frac{R_2}{R_1}\right) = 14\,\text{V} \cdot \left(1 + \frac{1}{2.7}\right) = 19.2\,\text{V}$$

It is worth notice that at the previous point the resistor values were taken with a 1% tolerance, and here is the reason why: since the output voltage is the one to be controlled, it must be precise.

Being the controller input voltage limited, the new output voltage to be compared is set at 4 V (compliant with the 5 V limit). Hence, a resistive partition must be introduced (always 1% components)

$$\frac{V_{o,x}}{V_{o,z}} = \frac{1}{1 + \dfrac{R_6}{R_5}}$$

$$\frac{R_6}{R_5} = \frac{V_{o,z}}{V_{o,x}} - 1 = \frac{19.2\,\mathrm{V}}{4\,\mathrm{V}} - 1 = 3.8$$

The selected values are $R_5 = 13.7\,\mathrm{k\Omega}$ and $R_6 = 52.3\,\mathrm{k\Omega}$

At this point, the frequency compensation is needed. Dealing with a current mode control, the power stage has a zero and a pole ([21]). In Figure 5.3.2), the frequency behavior expected (not scaled).

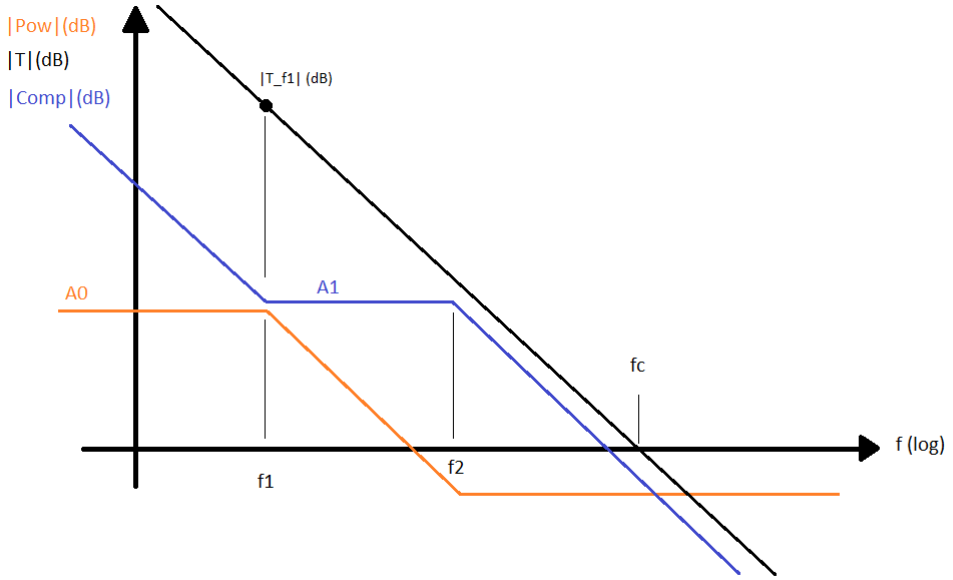


Figure 5.3.2: Current sensing compensation - frequency behavior

The available parameter at the beginning are

– $f_1 = \dfrac{1}{2\pi \cdot R_{L,min} \cdot C_o} = \dfrac{1}{2\pi \cdot 0.2\,\Omega \cdot 50\,\mu\mathrm{F}} = 16\,\mathrm{kHz}$

– $f_2 = \dfrac{1}{2\pi \cdot C_o \cdot ESR_o} = \dfrac{1}{2\pi \cdot 50\,\mu\text{F} \cdot 6\,\text{m}\Omega} = 530\,\text{kHz}$

– $A_0 = \dfrac{R_{L,min}}{R_{sense}} = \dfrac{0.2\,\Omega}{2\,\text{m}\Omega} = 100$

The parameter to choose is

$$f_c = \frac{f_{sw}}{5} = \frac{100\,\text{kHz}}{5} = 20\,\text{kHz}$$

which leads to

– $|T(f_1)|_{dB} = \dfrac{f_c}{f_1} = \dfrac{20\,\text{kHz}}{16\,\text{kHz}} = 1.25$

– $A_0 = \dfrac{|T(f_1)|_{dB}}{A_0} = \dfrac{1.25}{100} = 12.5 \times 10^2$

In Figure 5.3.3 the type-II compensator to be designed.

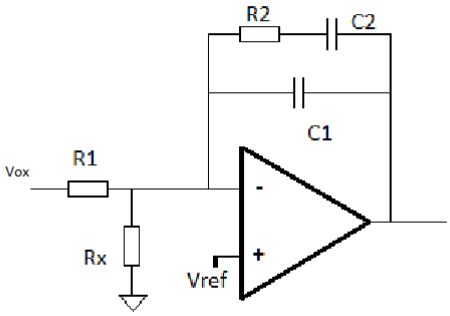


Figure 5.3.3: Current sensing compensation - frequency behavior

Always referring to [21], the design of the filter is the following

1. starting assumption

$$C_1 = 100\,\text{pF}$$

2. associating the frequency f_2 to the pole introduced by R_2, C_1

$$f_2 = \frac{1}{2\pi \cdot R_2 \cdot C_1} \quad \rightarrow \quad R_2 = \frac{1}{2\pi \cdot f_2 \cdot C_1}$$

$$R_2 = \frac{1}{2\pi \cdot 530\,\text{kHz} \cdot 100\,\text{pF}} = 3\,\text{k}\Omega \quad \rightarrow \quad 2.7\,\text{k}\Omega$$

3. associating the frequency f_1 to the zero introduced by R_2, C_2

$$f_1 = \frac{1}{2\pi \cdot R_2 \cdot C_2} \quad \rightarrow \quad C_2 = \frac{1}{2\pi \cdot f_1 \cdot C_2}$$

$$C_2 = \frac{1}{2\pi \cdot 16\,\text{kHz} \cdot 2.7\,\text{k}\Omega} = 3.7\,\text{nF} \quad \rightarrow \quad 3.9\,\text{nF}$$

4. the in-band gain is related to R_1, R_2

$$A_1 = \frac{R_2}{R_1} \quad \rightarrow \quad R_1 = \frac{R_2}{A_1}$$

$$R_1 = \frac{2.7\,\text{k}\Omega}{0.0125} = 216\,\text{k}\Omega \quad \rightarrow \quad 220\,\text{k}\Omega \quad (1\%tolerance)$$

5. finally the bias resistance, to match the reference voltage with the equivalent output voltage

$$\frac{V_{ox}}{V_{ref}} = 1 + \frac{R_1}{R_x} \quad \rightarrow \quad R_x = R_1 \cdot \frac{1}{\frac{V_{ox}}{V_{ref}} - 1}$$

$$R_x = \frac{220\,\text{k}\Omega}{\frac{4\,\text{V}}{2.5\,\text{V}} - 1} = 367\,\text{k}\Omega \quad \rightarrow \quad 365\,\text{k}\Omega \quad (1\%tolerance)$$

CHAPTER 6

Simulation Results

In this chapter simulation results will be presented. Starting from the analysis of the circuit simulated, the difference and the both the start-up and the steady state are analyzed. Next the efficiency profile is presented, either with respect to power, either with respect to the switching frequency. Moreover it will be compared to the one of the buck converter.

6.1 Simulation models

The procedure used to carry on the simulations for the SCC is the following one:

0. before adding any component to the model (such as the MOSFETs, the optoisolators, etc.) a characterization of the devices has been carried out, to verify the electrical characteristics specified in the datasheet.

1. at first the simulated circuit was only made up of input source, the output load, the flying capacitors, and ideal switches, with an equivalent $R_{on} = 2\,\mathrm{m}\Omega$ and $R_{off} = 1\,\mathrm{M}\Omega$. At this point nothing else has been considered but the correct behavior of the system.

2. first problem to be faced has been adding the model of the real components to the circuit. For each new component added, the staedy-state behavior of the SCC was the only concern. At first, the ideal switches were substituted by the MOSFETs; therefore, drivers and optocouplers were introduced.

See Figure 6.1.1 for the transistor characterization. Since the behavior is modeled to be linear even above $V_{ds} = 1\,\mathrm{V}$, the equivalent on-resistance can be defined as:

$$R_{on} = \frac{V_{ds}}{I_d} = \frac{1\,\mathrm{V}}{489\,\mathrm{A}} \approx 2\,\mathrm{m\Omega}$$

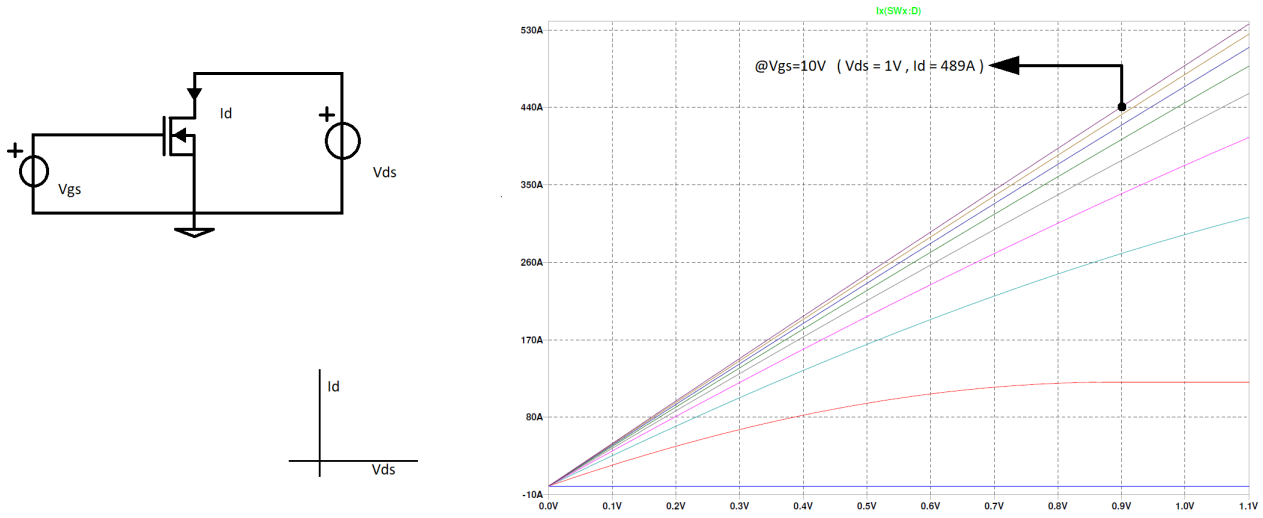


Figure 6.1.1: MOSFET characterization

For what concerns the optocoupler characterization, refer to Figure 6.1.2. The current through the photodiode is in the 5 mA to 30 mA range, which is the parameter the different BJT collector currents depend on.

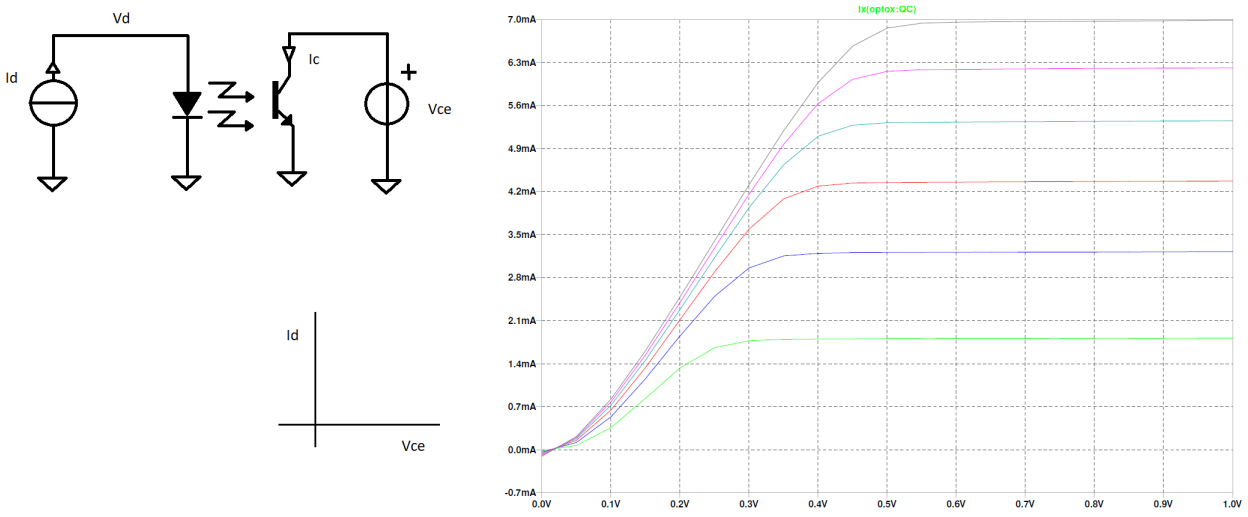


Figure 6.1.2: Optoisolator characterization

\ \ \	$H \times 1, L \times 1$	$H \times 2, L \times 2$	$H \times 2, L \times 3$
$P_{sw,1}$	4.8 W	1.5 W	1.5 W
$P_{sw,2}$	5.8 W	2 W	2 W
$P_{sw,3}$	5.2 W	1.5 W	1.5 W
$P_{sw,4}$	10.5 W	3.5 W	1.5 W
$P_{sw,5}$	10 W	3 W	1.5 W
$P_{sw,6}$	11 W	3.5 W	1.5 W

Table 6.1: comparison of the reference work and the revised version

3. at this point the number of parallel MOSFETs needed to satisfy power dissipation capability has been determined. In Table 6.1 the results obtained (H, L stand respectively for the set $\{SW1, SW2, SW3\}$ and $\{SW4, SW5, SW6\}$).

4. with the introduction of an output battery and the input isolation diode, the start-up procedure has been face leading to many different solutions, that ended ith the ine described in 4.4.3. Resorting to Figure 6.1.3, the input isolation has been introduced as it is needed from specifications. Instead, dealing with the output battery, its voltage has been set to 12.2 V to simulate a discharged battery; moreover, in order to decouple the output node from the battery voltage, a series parasitic resistance has been introduced to allow the output voltage to be above the one of the battery, hence charging it.

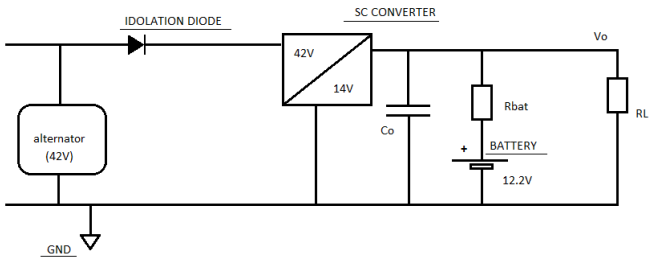


Figure 6.1.3: input alternator and output battery models

5. the shared bootstrap technique has been tested (see Section 4.4.3). The result in Figure 4.4.8 have to be compared with the one described in Figure 6.1.4. In

the simulation it is possible to notice the forward voltage drop of the parasitic diodes of the MOSFETs.

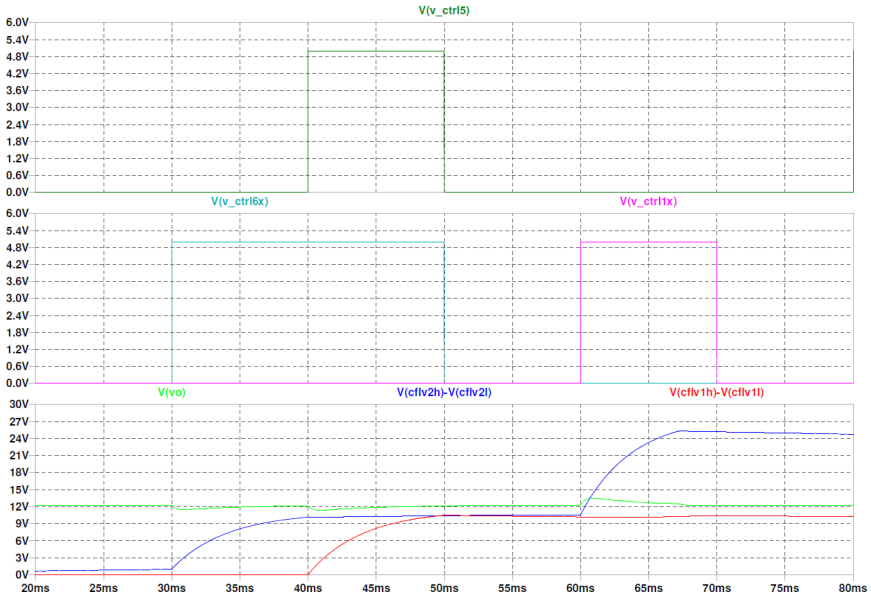


Figure 6.1.4: Start up timing diagram - simulation

6. a parasitic inductance in the model has been introduced to see how they affect the performances. From a schematic point of view, the parasitic inductances has been introduced in series with each flying capacitor, so that, in each in each sub-switching state, they affect the circuit behavior. The value has been set at $L_p = 10\,\text{nH}$ (refer to Figure 6.1.5).

The introduction of a parasitic inductance allows to have a more real behavior of the impulsive currents which occur when a capacitor is placed in parallel either to a voltage source, either to an other capacitor, in a mash characterized by a small resistance. Refer to Figure 6.1.6 and Figure 6.1.7 to compare the two behaviors. If, at design time, it was picked up the rms-current estimated from the simulations without the model of the parasitic inductance included, it would have been much more critical.

Another important thing should be noticed, that is to say that the switch must allow bidirectional current to flow. This is the reason that led to choosing a MOSFET transistor among the possible alternatives.

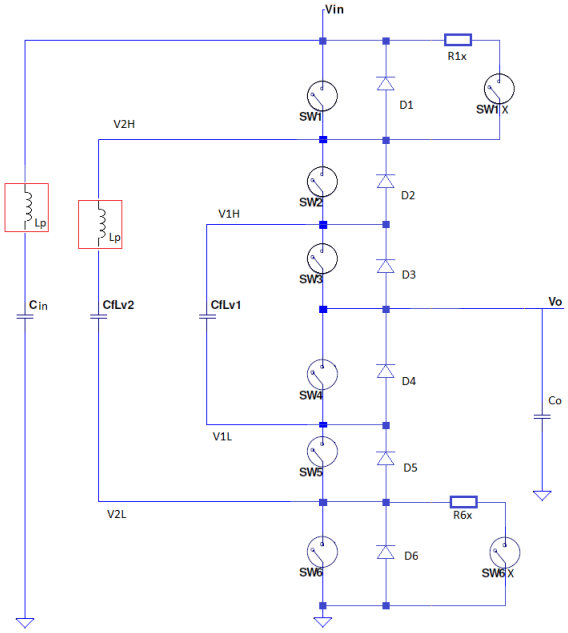


Figure 6.1.5: parasitic inductances - estimation

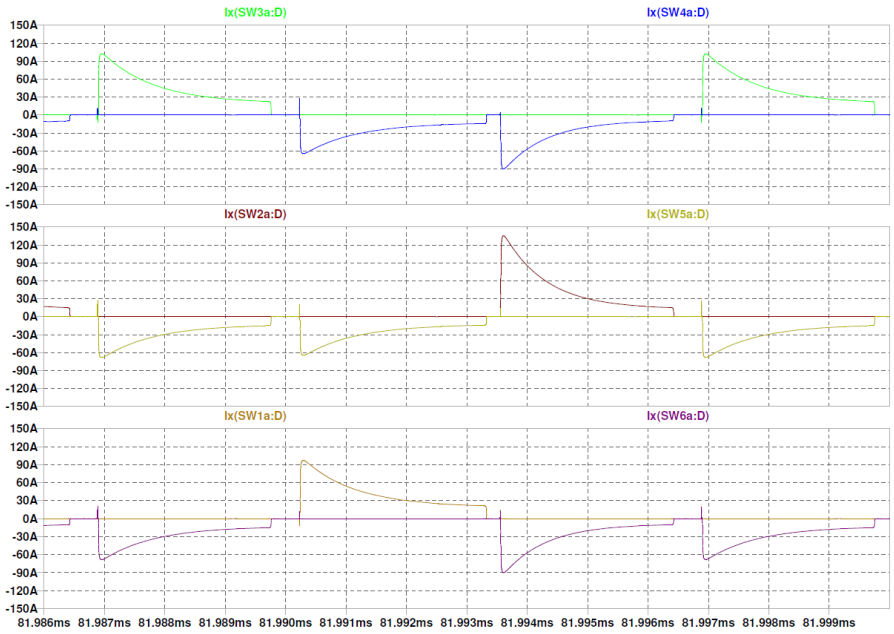


Figure 6.1.6: switch currents - no parasitic inductance

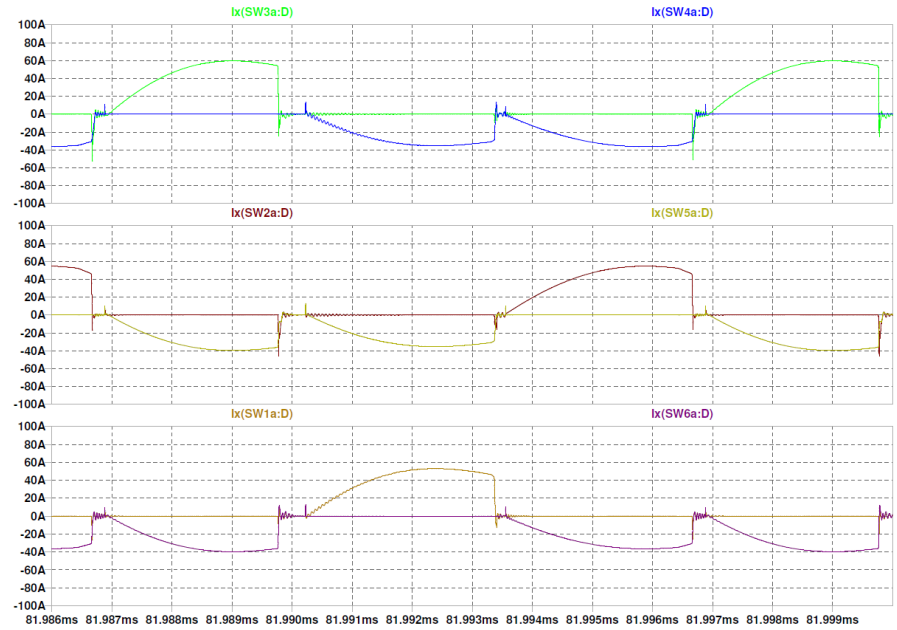


Figure 6.1.7: switch currents - with parasitic inductance

6.2 Steady-state profiles

The SCC has been made work in different loading conditions, from 10%, up to 150% of the power level the converter has been designed for. Being the input voltage fix at 42 V, two different type of simulations have been carried out: one without the parasitic inductance, and one with the parasitic inductance. In figure Figure 6.2.1 the results are reported.

As it can be seen, the efficiency at high power hold above 92%, while at lower power levels the efficiency drops because of the constant power dissipated to supply the drivers, and all the other devices that allow the topology to correctly work.

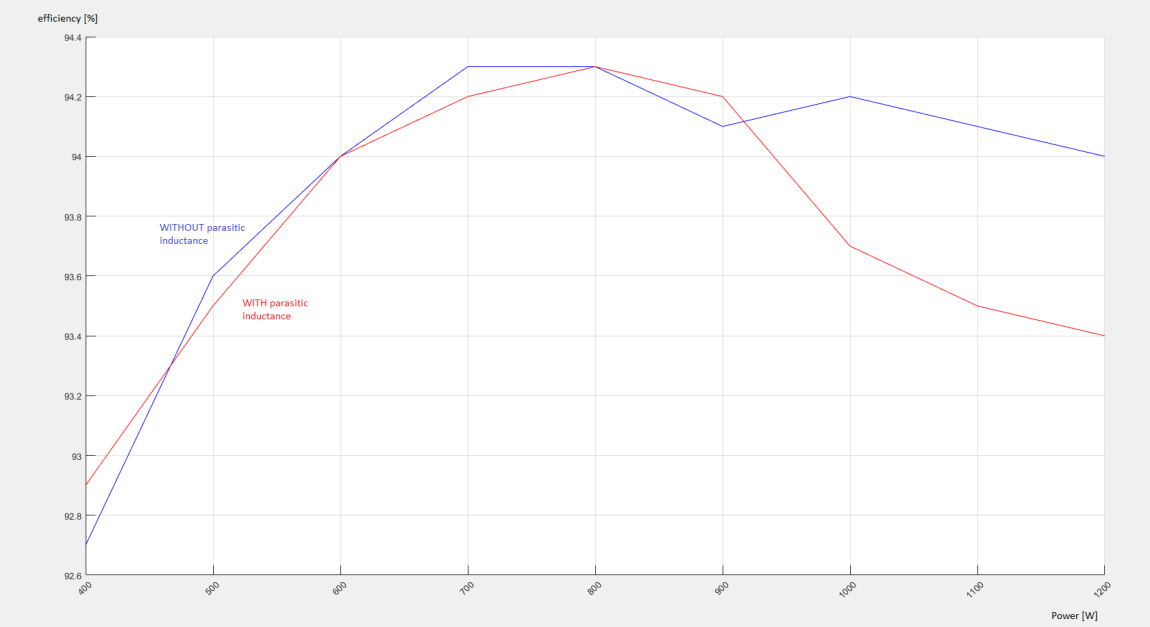


Figure 6.2.1: efficiency performance - SCC

An efficiency profile has been derived also for the buck topology. This has to be considered just a reference, because the simulations have been performed in open-loop configuration, manually trimming the duty ratio so that $V_o = 14\,\text{V}$. In figure Figure 6.2.2, both the 1- and the 3-phase buck are reported.

To compare the the four situation available, refer to Figure 6.2.3

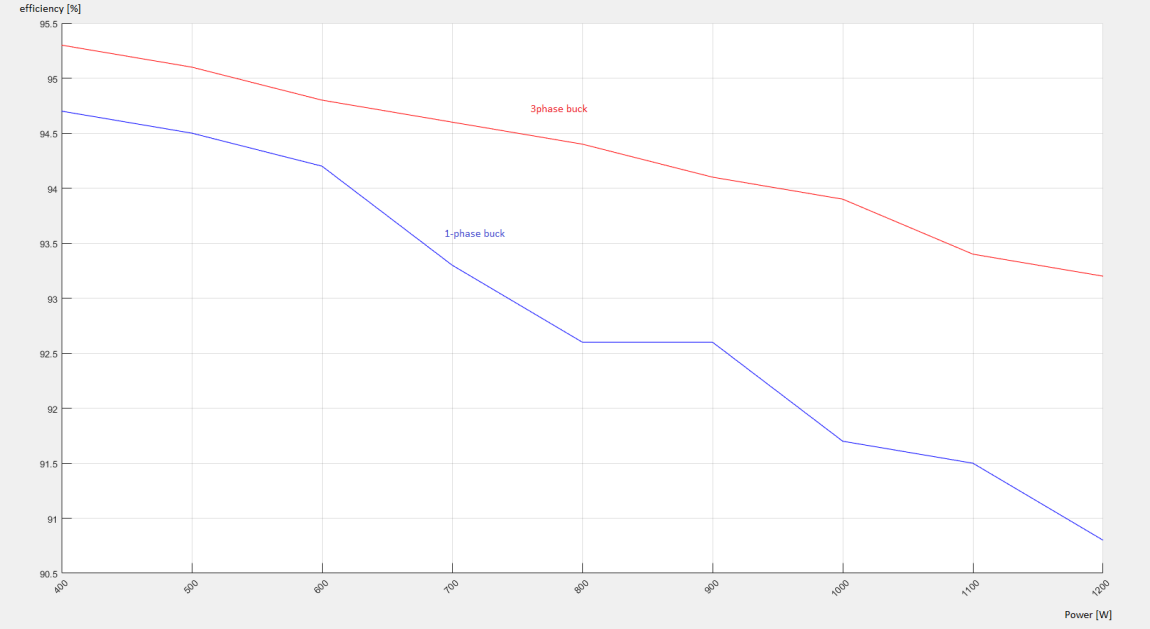


Figure 6.2.2: efficiency performance - Buck

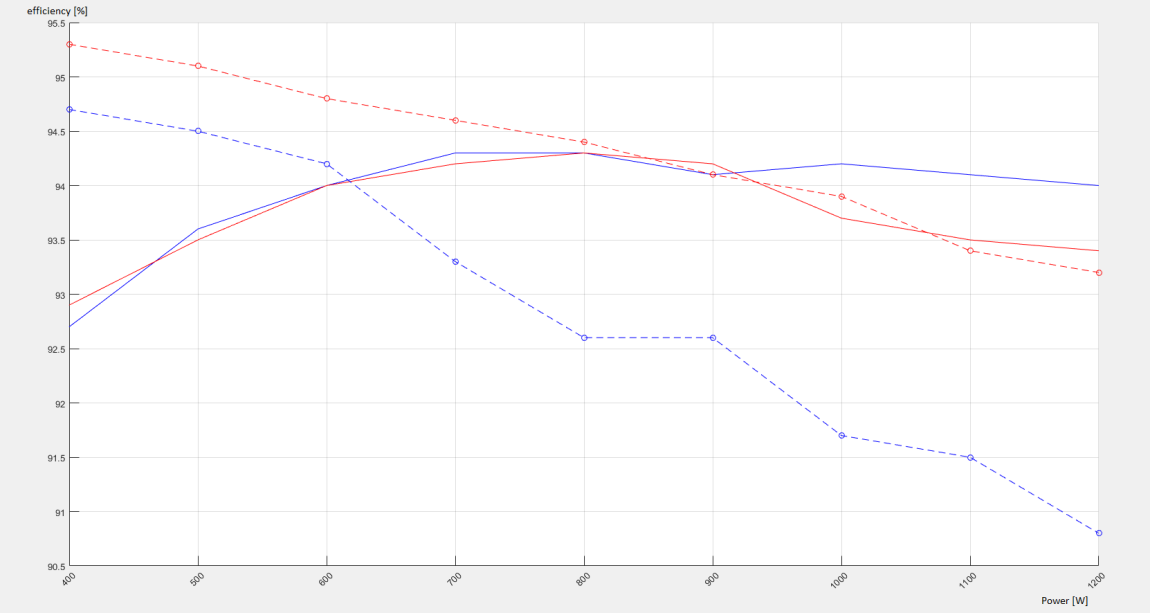


Figure 6.2.3: efficiency performance - Buck and SCC comparison

CHAPTER 7

Conclusions and Further Developments

Standard solutions for high power step-down conversion resort to buck-based topologies; this includes isolated buck converters, when the transformation ratio required is high, or multi-phase solutions, when isolation is not needed and the conversion ratio is not too high. This work is supposed to be a preliminary study related to the feasibility of a high-power SCC. Three are the aims:

1. look for an algorithm that allows to determine an upper bound for the conversion efficiency, and to adapt it to more-than-two switching states SCC.

2. using as reference design the device presented in 1.4.2, the next aim is to demonstrate (through the method previously proposed) that it is possible to build a switched-capacitor converter, to be employed for the same application, with increased characteristics, such as lower capacitance value working at higher frequency; hence, to demonstrate that the original design was oversized, also with respect to volumes (since bulky electrolytic capacitors were implemented).

3. therefore, to compare this new solution with a conventional buck topology, for what concern performances and component costs. This, in order to evaluate if the new solution can be a competitive solution to be employed for the specific application.

One last thing has to be noticed before proceeding. All the electronic system connected to the 14 V power rail has their own regulator to decrease the working voltage for low power requirements. At the same time, the battery is able to withstand

up to 16 V (refer to [18]), which is approximately the 50 V threshold set in the protection control for the input voltage. This to say that even if the voltage is not regulated, power converters are present anyway, and they act as loads for the SCC. Hence, a regulated solution, in this instance, is not necessarily needed, and just a voltage transformer may be enough (refer to Figure 7.0.1). In this case the SCC in not a point of load converter, but a system supply.

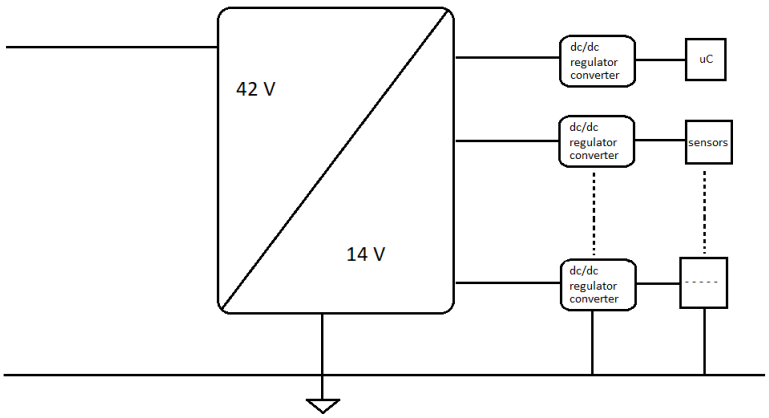


Figure 7.0.1

Conclusions

Starting from what concern the design algorithm, the one used seems to be quite precise to predict the behavior of the system. This because, if the system is well designed, the main loss contributions are those related to charge balance effect and parasitic resistances. In this case, the required efficiency was $\eta \approx 95\%$, and that is close to what has been obtained in Section 6.2.

For what concern the comparison with the reference work presented in Section 1.4.2, no concrete result may be pointed out, since no prototype has been built. The only thing that can be discussed is the fact that the capacitors actually seem to be oversized; referring to Table 7.1. The different switching frequency is due to the fact the this parameter has been used as a starting degree of freedom for the design. Since the goal was to reduce the capacitance needed to perform the conversion (which also means reduced volume/area), a frequency one order of magnitude higher (actually 20 times) has been chosen. If now the equivalent capacitances are compared (recalling

that there is one order of magnitude as offset due to the different switching frequency), first thing to point out is the fact that there is no practical reason (neither upheld by the authors, neither found out by myself, neither found out by chance) for the two flying capacitors to be different, since the adopted design procedure ends up with both of them being equal. As it can be noticed, the $ESRs$ and the on-resistance of the switches have approximately the same order of magnitude; hence, a metric to compare the two solutions will be represented by the following parameter "p"

$$p = C_{tot} \cdot f_{sw}$$

$$p_{old} = 10 \cdot 3300\,\mu\text{F} \cdot 5\,\text{kHz} = 165 \qquad p_{new} = 8 \cdot 50\,\mu\text{F} \cdot 100\,\text{kHz} = 40$$

The two parameters differ by a factor close to 4. Since the target efficiency and power are the same, the reference converter can be claimed to be oversized, even if the operating conditions are different.

The last point that deserves a comment is the comparison of the SCC solution with respect to the well-known switching buck topology. There are two aspects to take care of: performances and costs. Performances are referred to the efficiency profile (refer to 6.2), while the costs to the bill of materials (*a.k.a., BOM*). Speaking about performances, the

Speaking about BOM, only the main components will be discussed. For the switched-capacitor converter: input/output/flying capacitors, switches, swich-drivers; for the buck (3-phase): input/output capacitor, inductors, switches, switch-drivers.

By looking at Table 7.2 it can pointed out that:

- both the input and the output capacitors of the SCC are much more stressed than the one of the buck converter
- the number of switches is higher in the SCC, hence more drivers are needed
- the inductors are the most voluminous component, and 3 of them are required On the other hand, many capacitors are needed (16), and even if they may be smaller, they turn out to be quite a lot to be placed on a PCB

As a result, for this particular application where the voltage conversion ratio is small enough to avoid a transformer for the buck converter, the SCC seems to

\ \ \	$reference$	$revised$
f_{sw}	5 kHz	100 kHz
η_{target}	95%	95%
$Power$	1 kW	1 kW
- - - - - - - -	- - - - - - - -	- - - - - - - -
C_1	3300 µF	50 µF
$tolerance_1$	N/A	10%
ESR_1	7 mΩ	6 mΩ
$I_{rms,1}$	N/A	15 A
$\#parallelCap_1$	10	8
$V_{rated,C1}$	N/A	550 V
$type$	$electrolytic$	$film$
- - - - - - - -	- - - - - - - -	- - - - - - - -
C_2	2200 µF	50 µF
$tolerance_2$	N/A	10%
ESR_2	12 mΩ	6 mΩ
$I_{rms,2}$	N/A	15 A
$\#parallelCap_2$	10	8
$V_{rated,C2}$	N/A	550 V
$type$	$electrolytic$	$film$
- - - - - - - -	- - - - - - - -	- - - - - - - -
$R_{sw,on}$	2.8 mΩ	2.4 mΩ
$total\#swtches$	$6 \cdot 5$	$2 \times 3 + 3 \times 3$
$V_{rated,SW}$	30 V	60 V

Table 7.1: comparison of the reference work and the revised version

\ \ \	$BUCK_{3\phi}$	SCC
f_{sw}	100 kHz	100 kHz
$Power$	1 kW	1 kW
- - - - - - - -	- - - - - - - -	- - - - - - - -
$R_{sw,on}$	12 mΩ	2.4 mΩ
$total\#swtches$	6 (including diodes for a non-synchronous buck)	$6 + 2(startup)$
$V_{rated,SW}$	60 V	60 V
- - - - - - - -	- - - - - - - -	- - - - - - - -
C_{fly}	N/A	50 µF
ESR	N/A	6 mΩ
I_{rms}	N/A	72 A/8
$total\#capacitors$	N/A	8×2
- - - - - - - -	- - - - - - - -	- - - - - - - -
L	2200 µH	N/A
I_{rms}	25 A	N/A
$total\#inductors$	3	N/A
- - - - - - - -	- - - - - - - -	- - - - - - - -
C_{in}	50 µF	50 µF
I_{rms}	36 A/2	72 A/8
$total\#capacitors$	2	8
- - - - - - - -	- - - - - - - -	- - - - - - - -
C_{out}	2.8 µF	50 µF
I_{rms}	< 1 A	72 A/8
$total\#capacitors$	1	8

Table 7.2: comparison of the buck and the SCC critical components

perform quite well compared to conventional converters. The components are in general much more stressed with respect to those of the buck converter, and a larger number is needed (even if total area/volume is what really matters).

To conclude, with an easy-to-use method for the analysis and the design, switched-capacitor converters turn out to be a reasonable solution to conventional converters, but they have to be studied more in deep to make them really competitive. In such applications where a high voltage gain is required, and also no isolation is needed, a better comparison may be between SCC and a buck-derived (*i.e.*, dc/dc buck and transformer) topology.

Further Developments

Whatever the application, the leading aims of any kind of project are reduced costs, reduced volumes, high performances. This is always quite challenging, and many trade-off shall be made. In this case, some more alternatives should be analyzed before prototyping (or to compare the different performances).

Independently of the converter topology used (SCC or standard-SMPS), two different concepts may be applied as showed in [18]: distributed or centralized power distribution. In Figure 7.0.2, a particular distributed solution is shown.

Assuming the *key-off* battery is the 14 V one, and that the only *key-off* loads are those connected to the low-voltage battery, it is possible to define more-than-one 14 V domains. This is possible because the dc/dc converter does not need a battery at the output to work. This way each converter can be sized for a lower power rating, but the most interesting thing is that it is completely independent of the other low-voltage domains. This solution may reduce, together with the power requirements, the costs, because components are much less stressed. For sure, the trade-off may be the area/volume needed, that in an automotive system is always a critical point.

A further study is related to the analysis of the EMI emissions, both conducted and emitted. This is important especially for applications connected to the electric power line, in which a SCC will play the role of a non isolated transformer. Just to recall, the SCC perform far better than conventional converters when a high voltage

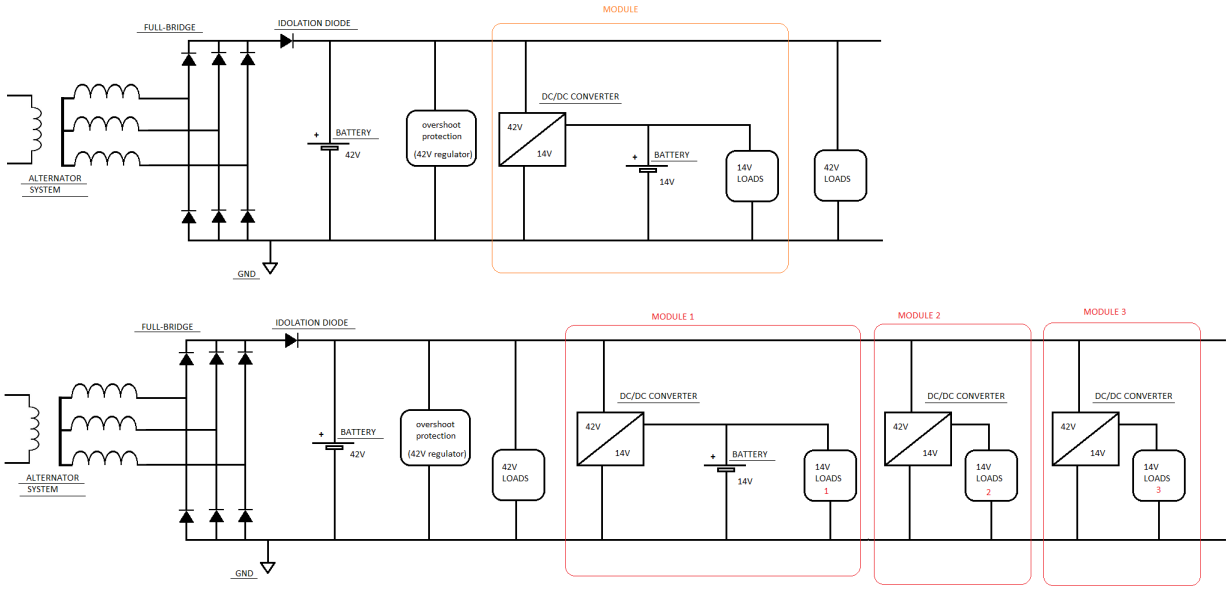


Figure 7.0.2: distributed (down) and centralized (up)

gain is needed, because capacitors work at almost fixed voltage, but the main limiting feature is the current capability (which bounds the power level of a SCC). That is why SCC can be a temping solution in hybrid electric vehicles (*HEVs*), where very high voltage gain is needed to transform 300 V-400 V to 14 V or 48 V.

Appendices

APPENDIX A

Mathematical steps and results

A.1 SCC: capacitor charging

The situation in Figure 2.1.1 is reported again in Figure A.1.1, for notation issues.

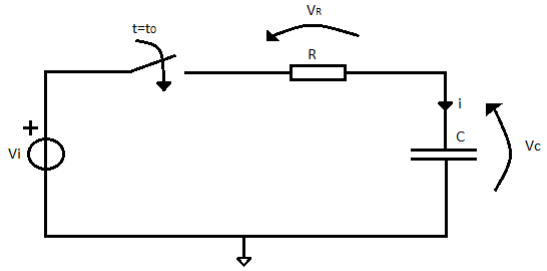


Figure A.1.1: reference notation

Starting conditions:

- $V_C(t_0) = V_{Ci}$, capacitor voltage before switching
- $V_{Ci} < V_i$
- capacitor voltage after switching

$$V_C(t) = V_{Ci} \cdot e^{\frac{t-t_0}{-\tau}} + V_i \left(1 - e^{\frac{t-t_0}{-\tau}}\right) = V_{Ci} + (V_i - V_{Ci}) \cdot \left(1 - e^{\frac{t-t_0}{-\tau}}\right)$$

- current behavior after switching

$$i(t) = C \cdot \frac{dV_C(t)}{dt} = \frac{-C}{-\tau} \cdot (V_i - V_{Ci}) \cdot e^{\frac{t-t_0}{-\tau}} = \frac{(V_i - V_{Ci})}{R} \cdot e^{\frac{t-t_0}{-\tau}}$$

- $t_0 = 0$, to simplify the analysis
- T, the predefined time for which the voltage source is connected to the capacitor
- capacitor voltage after a time T, from t_0

$$V_C(t_0 + T) = V_{Cf} = V_{Ci} \cdot e^{\frac{t}{-\tau}} + V_i \left(1 - e^{\frac{T}{-\tau}}\right)$$

- $\tau = RC$

First step is to determine the variation of the energy stored in the capacitor ΔE_C

$$\Delta E_C = \int_0^T V_C(t) \cdot i(t)\, dt = \frac{(V_i - V_{Ci})^2}{R} \left[\int_0^T e^{\frac{t}{-\tau}}\, dt - \int_0^T e^{\frac{2t}{-\tau}}\, dt\right] + \frac{V_{Ci}\,(V_i - V_{Ci})}{R} \left[\int_0^T e^{\frac{t}{-\tau}}\, dt\right] =$$

$$= \frac{(V_i - V_{Ci})^2}{R} \left[\frac{\tau}{2} - \tau e^{\frac{T}{-\tau}} + \frac{\tau}{2} e^{\frac{2T}{-\tau}}\right] + \tau \frac{V_{Ci}\,(V_i - V_{Ci})}{R} \left(1 - e^{\frac{T}{-\tau}}\right) =$$

$$= \frac{\tau}{2} \frac{(V_i - V_{Ci})}{R} \left[(V_i - V_{Ci}) \left(1 - 2e^{\frac{T}{-\tau}} + e^{\frac{2T}{-\tau}}\right) + 2V_{Ci} \left(1 - e^{\frac{T}{-\tau}}\right)\right] =$$

$$= \frac{C}{2} (V_i - V_{Ci}) \left[V_i \left(1 - 2e^{\frac{T}{-\tau}} - e^{\frac{2T}{-\tau}}\right) - V_{Ci} \left(2 - 2e^{\frac{T}{-\tau}} - 1 + 2e^{\frac{T}{-\tau}} - e^{\frac{2T}{-\tau}}\right)\right] =$$

$$= \frac{C}{2} (V_i - V_{Ci}) \left[V_i \left(1 - e^{\frac{T}{-\tau}}\right)^2 - V_{Ci} \left(1 - e^{\frac{2T}{-\tau}}\right)\right] =$$

$$= \frac{C}{2} (V_i - V_{Ci}) \left[V_i \left(1 - e^{\frac{T}{-\tau}}\right) \left(1 - e^{\frac{T}{-\tau}}\right) - V_{Ci} \left(1 - e^{\frac{T}{-\tau}}\right) \left(1 + e^{\frac{T}{-\tau}}\right)\right] =$$

$$= \frac{C}{2} \left(\frac{V_{Cf} - V_{Ci} \cdot e^{\frac{T}{-\tau}}}{1 - e^{\frac{T}{-\tau}}} - V_{Ci}\right) \left[\left(V_{Cf} - V_{Ci} \cdot e^{\frac{T}{-\tau}}\right) \left(1 - e^{\frac{T}{-\tau}}\right) - V_{Ci} \left(1 - e^{\frac{T}{-\tau}}\right) \left(1 + e^{\frac{T}{-\tau}}\right)\right] =$$

$$= \frac{C}{2} \left(V_{Cf} - V_{Ci} \cdot e^{\frac{T}{-\tau}} - V_{Ci} + V_{Ci} \cdot e^{\frac{T}{-\tau}}\right) \left[\left(V_{Cf} - V_{Ci} \cdot e^{\frac{T}{-\tau}}\right) - V_{Ci} \left(1 + e^{\frac{T}{-\tau}}\right)\right] =$$

$$= \frac{C}{2} (V_{Cf} - V_{Ci}) [V_{Cf} + V_{Ci}]$$

Hence

$$\Delta E_C = \frac{C}{2} \left(V_{Cf}^2 - V_{Ci}^2\right)$$

Next step is to determine the energy delivered by the sourceΔE_i

$$\Delta E_i = \int_0^T V_i \cdot i(t)\, dt = \frac{V_i\,(V_i - V_{Ci})}{R} \left[\int_0^T e^{\frac{t}{-\tau}}\, dt\right] =$$

$$= \tau \frac{V_i\,(V_i - V_{Ci})}{R} \left[1 - e^{\frac{T}{-\tau}}\right] = CV_i \left(1 - e^{\frac{T}{-\tau}}\right) (V_i - V_{Ci}) =$$

$$= C\left(V_{Cf} - V_{Ci}\cdot e^{\frac{T}{-\tau}}\right)\left(\frac{V_{Cf} - V_{Ci}\cdot e^{\frac{T}{-\tau}}}{1-e^{\frac{T}{-\tau}}} - V_{Ci}\right) =$$

$$= C\left(V_{Cf} - V_{Ci}\cdot e^{\frac{T}{-\tau}}\right)\frac{\left(V_{Cf} - V_{Ci}\cdot e^{\frac{T}{-\tau}} - V_{Ci} + V_{Ci}\cdot e^{\frac{T}{-\tau}}\right)}{1-e^{\frac{T}{-\tau}}} =$$

$$= C\frac{\left(V_{Cf} - V_{Ci}\cdot e^{\frac{T}{-\tau}}\right)}{1-e^{\frac{T}{-\tau}}}\left(V_{Cf} - V_{Ci}\right)$$

Hence

$$\Delta E_i = CV_i\left(V_{Cf} - V_{Ci}\right)$$

Now it is possible to determine the efficiency

$$\eta = \frac{\Delta E_c/T}{\Delta E_i/T} =$$

$$= \frac{C}{2}\left(V_{Cf}^2 - V_{Ci}^2\right)\cdot\frac{1}{CV_i\left(V_{Cf} - V_{Ci}\right)} =$$

$$= \frac{1}{2}\cdot\frac{\left(V_{Cf} - V_{Ci}\right)\left(V_{Cf} + V_{Ci}\right)}{V_i\left(V_{Cf} - V_{Ci}\right)} =$$

Therefore

$$\eta = \frac{1}{2}\cdot\frac{V_{Cf} + V_{Ci}}{V_i}$$

A different can be derived

$$\eta = \frac{1}{2}\cdot\frac{\left[\left(V_{Cf} - V_i\right) + V_i\right] + \left[\left(V_{Ci} - V_i\right) + V_i\right]}{V_i} =$$

$$= \frac{2V_i}{2V_i} - \frac{V_i - V_{Cf}}{2V_i} - \frac{V_i - V_{Ci}}{2V_i} =$$

$$= 1 - \frac{1}{2V_i}\left[\left(V_i - V_{Cf}\right) + \left(V_i - V_{Ci}\right)\right] =$$

If $T \to \infty$ (actually $T > 5\tau$ is enough, with a negligible error), the final voltage will be

$$V_{Cf} = V_i$$

Hence

$$\eta = \frac{1}{2}\left(1 + \frac{V_{Ci}}{V_i}\right)$$

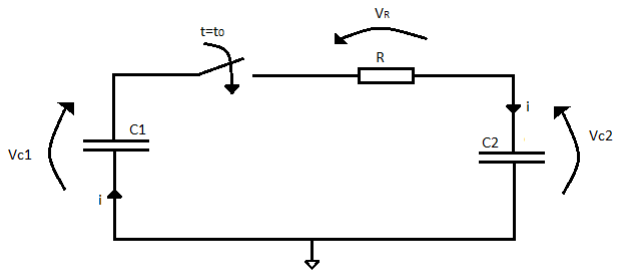


Figure A.2.1: reference notation

A.2 SCC: C-load

The situation in Figure 2.2.1 is reported again in Figure A.2.1, for notation issues.

Starting conditions:

- $V_{C1}(t_0) = V_1$, capacitor voltage before switching
- $V_{C2}(t_0) = V_2$, capacitor voltage before switching
- $V_2 < V_1$
- V_{QB}, the charge balance voltage
- $t_0 = 0$, to simplify the analysis
- T, the predefined time for which the voltage source is connected to the capacitor
- $\tau = R\left(\dfrac{C_1 C_2}{C_1 + C_2}\right)$

Being the initial charge

$$Q_i = C_1 V_1 + C_2 V_2$$

and the final charge

$$Q_f = V_{QB}\,(C_1 + C_2)$$

the balance voltage will be such that

$$Q_i = Q_f \quad \rightarrow \quad C_1 V_1 + C_2 V_2 = V_{QB}\,(C_1 + C_2)$$

$$V_{QB} = \frac{C_1 V_1 + C_2 V_2}{C_1 + C_2}$$

Assuming

$$C_1 = C \quad , \quad C_2 = xC \quad , \quad x > 0$$

$$V_1 = V \quad , \quad V_2 = yV \quad , \quad 0 \leq y \leq 1$$

$$\rightarrow \quad V_{QB} = V \cdot \frac{1+xy}{1+x}$$

In Appendix A.1, it has been demonstrated that the energy variation across the capacitor only depends on te final voltage and the starting voltage across the capacitor (being $V_{Cf} < V_{QB}$ the voltage after time T)

$$\Delta E_C = \frac{C}{2}\left(V_{Cf}^2 - V_{Ci}^2\right)$$

For C_1, assuming $T > 5\tau$, $V_{Cf,1} = V_{Cf,2} = V_{QB}$

Since the model for C_1 uses the electric generator convention, a negative sign is introduced

$$\Delta E_1 = -\frac{C_1}{2}\left(V_{Cf,1}^2 - V_1^2\right) = -\frac{C}{2}\left[V_{QB}^2 - V^2\right] =$$

$$= -\frac{C}{2}\left[\left(V^2\frac{1+xy}{1+x}\right)^2 - V^2\right] = -\frac{C\cdot V^2}{2\left(1+x\right)^2}\left[(1+xy)^2 - (1+x)^2\right] =$$

$$= -\frac{C\cdot V^2}{2\left(1+x\right)^2}\left[1 + x^2y^2 + 2xy - 1 - x^2 - 2x\right] =$$

$$= -\frac{C\cdot V^2}{2\left(1+x\right)^2}\left[x^2(y^2-1) + 2x(y-1)\right] =$$

$$= -\frac{xC\cdot V^2}{2\left(1+x\right)^2}\left[x(y-1)(y+1) + 2\right] =$$

$$= -\frac{xC\cdot V^2}{2\left(1+x\right)^2}(y-1)\left[x(y+1) + 2\right]$$

$$= -\frac{xC\cdot V^2}{2\left(1+x\right)^2}(y-1)\left[xy + x + 2\right]$$

For C_2, assuming $T > 5\tau$, $V_{Cf,1} = V_{Cf,2} = V_{QB}$

$$\Delta E_2 = \frac{C_2}{2}\left(V_{Cf,1}^2 - V_1^2\right) = \frac{xC}{2}\left[V_{QB}^2 - (yV)^2\right] =$$

$$= \frac{xC}{2}\left[\left(V^2\frac{1+xy}{1+x}\right)^2 - (yV)^2\right] = \frac{xC\cdot V^2}{2\left(1+x\right)^2}\left[(1+xy)^2 - y^2(1+x)^2\right] =$$

$$= \frac{xC \cdot V^2}{2\,(1+x)^2}\left[1 + 2xy + x^2y^2 - y^2(1 + 2x + x^2)\right] =$$

$$= \frac{xC \cdot V^2}{2\,(1+x)^2}\left[1 + 2xy + x^2y^2 - y^2 - 2xy^2 - y^2x^2\right] =$$

$$= \frac{xC \cdot V^2}{2\,(1+x)^2}\left[1 + 2xy - y^2 - 2xy^2\right] =$$

$$= \frac{xC \cdot V^2}{2\,(1+x)^2}\left[2xy(1-y) + (1-y^2)\right] =$$

$$= \frac{xC \cdot V^2}{2\,(1+x)^2}\left[2xy(1-y) + (1-y)(1+y)\right] =$$

$$= \frac{xC \cdot V^2}{2\,(1+x)^2}(1-y)\left[2xy + 1 + y\right]$$

Hence the efficiency turns out to be

$$\eta = \frac{\dfrac{xC \cdot V^2}{2\,(1+x)^2}(1-y)\left[2xy + 1 + y\right]}{-\dfrac{xC \cdot V^2}{2\,(1+x)^2}(y-1)\left[xy + x + 2\right]} =$$

$$= \frac{2xy + 1 + y}{xy + x + 2} =$$

APPENDIX B

Practical observations

B.1 Capacitors in Parallel

When designing electronic circuits, one issue is sizing the components, in particular when two components are bounded one another by a certain relationship: limited set of values available may be an issue.

For what concerns capacitors, especially when dealing with discrete components, the typical issue is to look for components with high capacitance, and, at the same time, low ESR and ESL. Unfortunately, capacitors with such characteristics may be hard to find, unless expensive ones. Hence, the typical technique implemented is paralleling capacitors of the same technology: resorting to the equivalent model of a capacitor ([22], [23]):

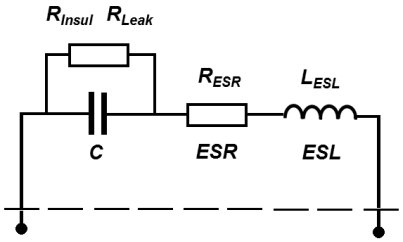


Figure B.1.1: Real capacitor - equivalent circuit

its equivalent impedance, assuming the parallel leakage to be negligible, is

$$Z_C = R + sL + \frac{1}{sC}$$

If some capacitors having the same nominal capacitance value (and almost the same parasitic resistance and inductance) are put in parallel:

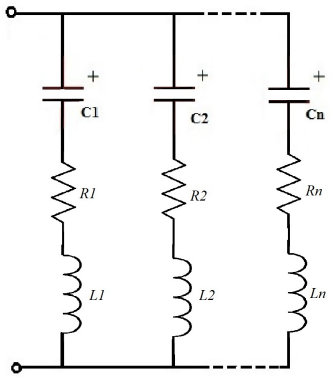


Figure B.1.2: Paralleled real capacitors - equivalent circuit

At $n = 3$, the equivalent impedance is

$$Y_{eq} = \frac{1}{R_1 + sL_1 + \frac{1}{sC_1}} + \frac{1}{R_2 + sL_2 + \frac{1}{sC_2}} + \frac{1}{R_3 + sL_3 + \frac{1}{sC_3}} = \frac{s(3C)}{1 + sRC + s^2CL}$$

$$Z_{eq} = \left(\frac{R}{3}\right) + s\left(\frac{L}{3}\right) + \frac{1}{s(3C)}$$

The equivalent component will have a capacitance 3 times bigger, and both ESR, ESL parasitic effects reduced by 3 times.

Note that this is not so easy when dealing with high power, because parasitic effects of the traces may unbalance the effect of reducing the parasitic resistance and inductance of the conductive path, leading to a higher current to flow in those capacitors which have shorter conductive path (refer to current crowding and electromigration effect).

B.2 MOSFET Dynamic Power Loss

Switching losses of MOSFETs must not be underestimated, because they may be of the same order of magnitude of the conduction losses, especially when dealing with inductive loads.

For the following analysis, the inductance will be approximated with a constant current source, assuming to work with a switching dc/dc converter at steady-state.

Moreover, to simplify the analysis, the structure in Figure B.2.1 will be used as reference, but the mathematical model that will be derived is valid for any high-side, low-side MOSFET in similar way.

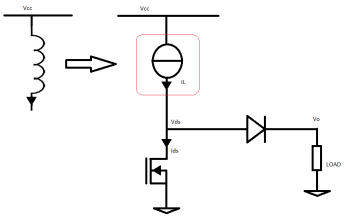


Figure B.2.1: Dynamic power estimation - circuit under test

The MOSFET turn-off current and voltage waveforms are showed in Figure B.2.2. When the transistor opens abruptly, the inductance tries to keep the current constant by increasing the drain node voltage up to the point where $V_{ds} = V_o$, when the diode starts conducting and the MOSFET drain current can start decreasing. The behavior of the two waveforms are approximated with a linear function with respect to time.

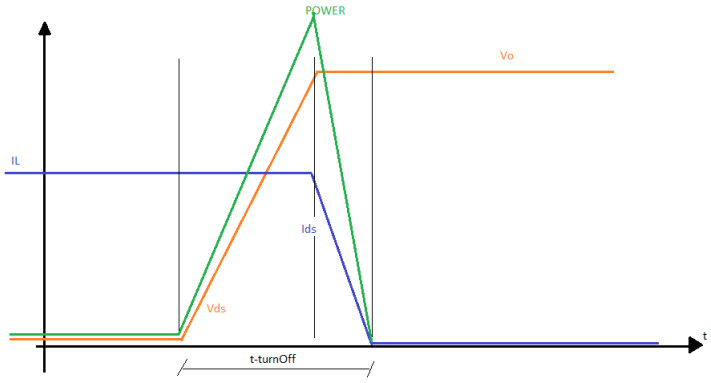


Figure B.2.2: Dynamic power estimation - circuit under test

The mathematical model to estimate the power dissipated refers to the area of the triangle, weighted by the switching frequency (since we assumed to work at steady-state)

$$P_{turnOff} = f_{sw}cdot\left(\frac{1}{2}\cdot t_{turnOff}\cdot V_{ds,A}I_{ds,B}\right)$$

Note that the symbols A and B respectively mean *after* opening, and *before* opening.

The turn-on procedure can just be seen as the inverse with respect to time of the turn-off: as the MOSFET start conducting, the diode current decreases; only when

the diode no longer conducts, the drain-source voltage can start to reduce itself. Hence, the model for the tunr-on is similar, but this time the voltage is the one before closing the switch, and the current is the one after closing the switch

$$P_{turnOn} = f_{sw} \cdot \left(\frac{1}{2} \cdot t_{turnOff} \cdot V_{ds,B} I_{ds,A} \right)$$

The total dynamic power loss model turns out to be

$$P_{loss,DYNAMIC} \approx \frac{f_{sw}}{2} \cdot (t_{on} \cdot V_{ds,B} \cdot I_{ds,A} + t_{off} \cdot V_{ds,A} \cdot I_{ds,B})$$

B.3 Emaulated Current Sensing

The standard technique for sensing the current in a buck converter is placing a resistor between the output node and the inductor. This is due to the fact that the differential amplifier needed to sense the voltage across the sensing resistor need a much lower common mode voltage with respect to placing the sensing resistor between the inductor and the node connected to the MOSFET and the diode.

The conventional solution may introduce a loss which is not negligible. Hence, to solve the problem an alternative solution may be adopted where the parasitic DCR (direct current resistance) of the inductor plays the role of the sensing resistor. The intrinsic time constant $\frac{L}{DCR}$ can be made emulated by an R-C circuit with the same intrinsic time constant

$$\frac{L}{DCR} = R \cdot C$$

In figure Figure B.3.1 the schematic is presented.

If the components are sized in such a way that the two time constants are equal, then the voltage drop across the DCR is the same across the capacitance if working in a switching steady-state regime.

It is worth notice that some conditions have to be satisfied to make this technique efficient:

- the resistance must be at least of the order of 10 kΩ, in order to have a very small current flowing in the R-C branch, to keep losses absolutely negligible
- the differential sensing can be done the same way it was done for the extra sensing resistor

– a voltage gain can be obtained by reducing the time constant of the R-C circuit (the faster the transient, the higher the voltage drop across the capacitor). This gain is limited, with respect to the switching frequency: as long as the linear approximation is valid for the transient, the gain can be trimmed at will

$$\frac{L}{DCR} = \tau_L = \frac{\tau_C}{k} = \frac{RC}{k}$$

$$V_C = k \cdot V_{DCR}$$

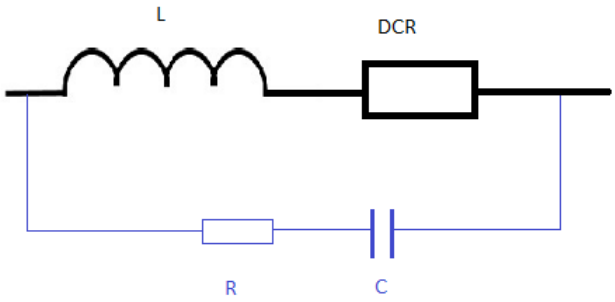


Figure B.3.1: emulated current sensing

As a matter of fact, the disadvantage of this technique is the knowledge of the precise DCR value parameter.

B.4 Multiphase Buck Converter: Duty Ratio Boundaries

A component which is stressed very much in a buck converter is the input capacitor, whose rms-current is typically the highest, compared to other components. One of the advantages of implementing a multiphase buck converter is the reduction of the stresses the input capacitor is subject to. This is because of the current sharing: referring to Figure B.4.1, to derive the equations, the number of phases is set to 3. In the schematic some assumptions have been made:

– to simplify computations, a flat-top approximation is applied

– the switching period is defined as $T_{sw} = T$

– a pulsed current flows through the switches. The frequency decomposition allows to distinguish the average DC value from the other frequency components (wrapped as an AC signal). In steady-state working conditions, the duty ratio of each phase is assumed to be equal ($d_\phi = d$).

$$I_{sw,avg} = I_{DC} = 3(d \cdot I_\phi) \quad \rightarrow \quad I_{DC} = d \cdot N \cdot I_\phi = d \cdot I_o$$

– the input capacitor is supposed to filter out all the AC component (note that the average current through a capacitor when working in a switching steady-state regime is null).

$$I^2_{C,in-rms} = I_{AC,rms} = \frac{1}{T}\int_0^T I^2_{C,in}(t)\,dt = \frac{1}{T}\int_0^T \left(I_{sw}(t) - I_{DC}\right)^2\,dt$$

– the input battery is modeled as a constant current source, providing the average DC current flowing through the switches.

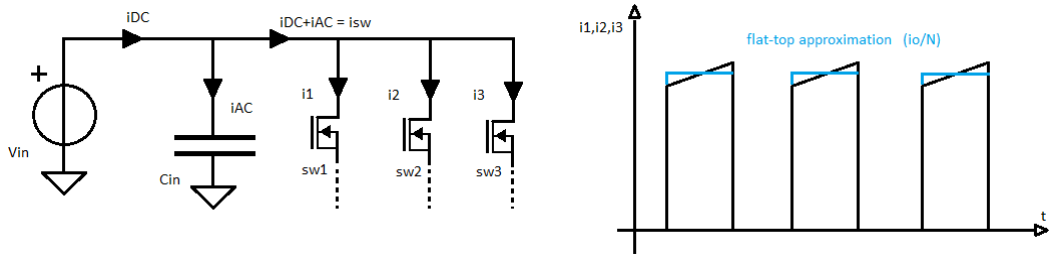


Figure B.4.1: 3-phases buck input node

Depending on the number of phases (N), the same number of situation occur. For instance, assuming $N = 3$, the possibilities are

1. non-overlapping phases ($0 < d < \frac{1}{3}$, in Figure B.4.2).

   The current I_{sw} switches between 0 and I_ϕ 3-times within a cycle, each lasting a time $\left(\frac{1}{3} - d\right) \cdot T$ and $d \cdot T$ respectively.

$$I^2_{AC,rms} = 3 \cdot \frac{1}{T}\int_0^T I^2_{C,in}(t)\,dt = \frac{3}{T}\int_0^T \left(I_{sw}(t) - I_{DC}\right)^2\,dt =$$

$$= \frac{3}{T}\left[\int_0^{\left(\frac{1}{3}-d\right)\cdot T} (0 - 3dI_\phi)^2\,dt + \int_0^{d\cdot T} (I_\phi - 3dI_\phi)^2\,dt\right] =$$

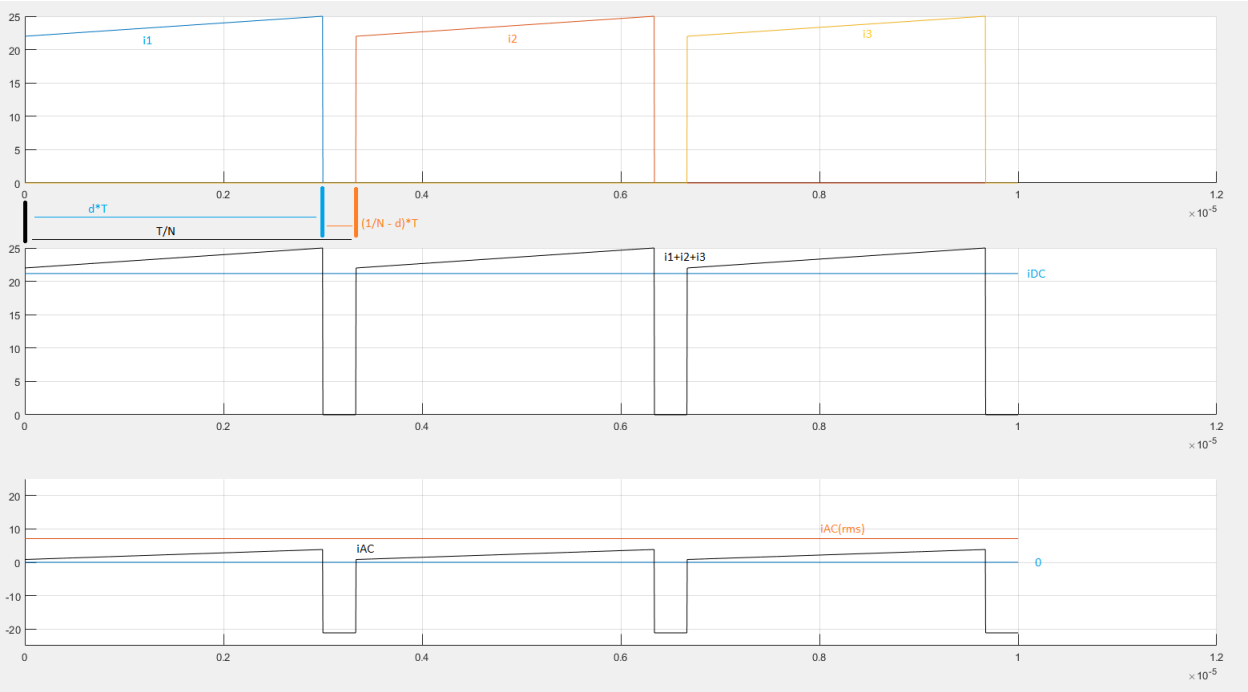


Figure B.4.2: 3-phases buck - no phase overlapped (d = 0.3)

$$\rightarrow \quad = \frac{N}{T}\left[\int_0^{\left(\frac{1}{N}-d\right)\cdot T} (0 - dNI_\phi)^2\, dt + \int_0^{d\cdot T} (I_\phi - dNI_\phi)^2\, dt\right] =$$

$$= \frac{N}{T}\left[I_\phi^2 (dN)^2 \left(\frac{1}{N} - d\right) T + I_\phi^2 (1 - dN)^2\, dT\right] =$$

$$= N \cdot I_\phi^2 \left[(dN)^2 \left(\frac{1}{N} - d\right) + (1 - dN)^2\, d\right]$$

2. phases overlap two-by-two ($\frac{1}{3} < d < \frac{2}{3}$, in Figure B.4.3).

   The current I_{sw} switches between I_ϕ and $2I_\phi$ 3-times within a cycle, each lasting a time $\left(\frac{2}{3} - d\right) \cdot T$ and $\left(d - \frac{1}{3}\right) \cdot T$ respectively.

$$I_{AC,rms}^2 = 3 \cdot \frac{1}{T}\int_0^T I_{C,in}^2(t)\, dt = \frac{3}{T}\int_0^T (I_{sw}(t) - I_{DC})^2\, dt =$$

$$= \frac{3}{T}\left[\int_0^{\left(\frac{2}{3}-d\right)\cdot T} (I_\phi - 3dI_\phi)^2\, dt + \int_0^{\left(d-\frac{1}{3}\right)\cdot T} (2I_\phi - 3dI_\phi)^2\, dt\right] =$$

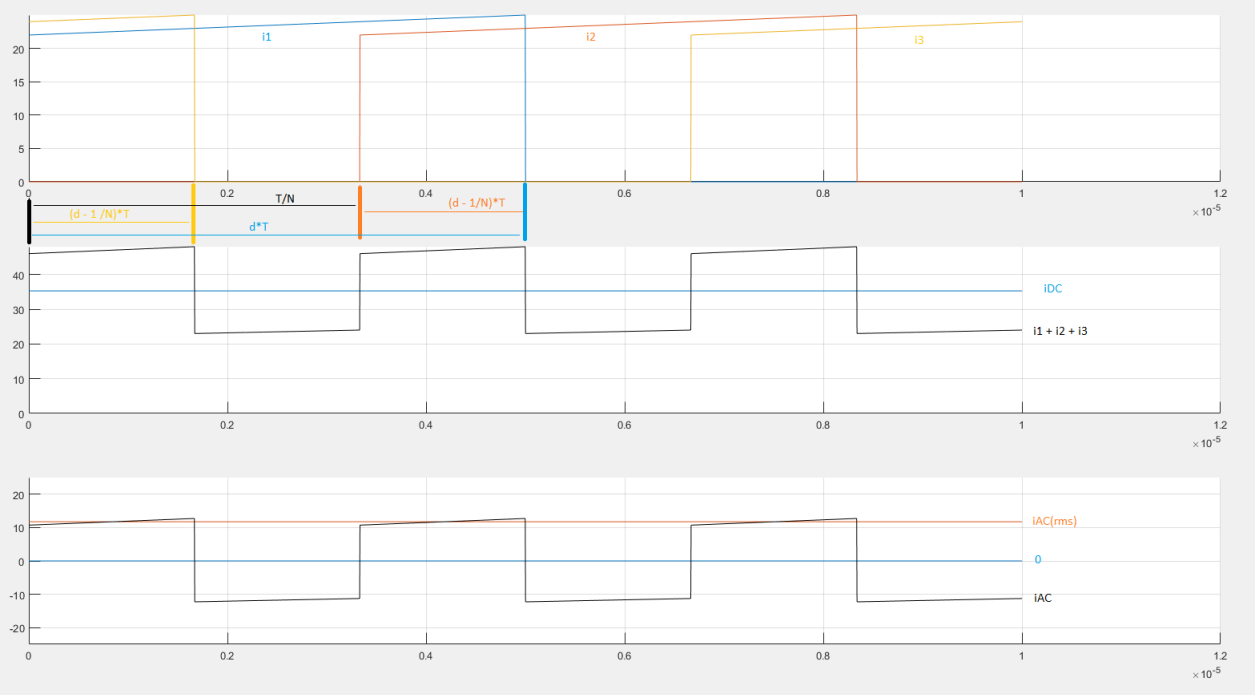


Figure B.4.3: 3-phases buck - 2 phases overlapped (d = 0.5)

$$\rightarrow \quad = \frac{N}{T}\left[\int_0^{\left(\frac{2}{N}-d\right)\cdot T} \left(I_\phi - NdI_\phi\right)^2\, dt + \int_0^{\left(d-\frac{1}{N}\right)\cdot T} \left(2I_\phi - NdI_\phi\right)^2\, dt\right] =$$

$$= \frac{N}{T}\left[I_\phi^2(dN-1)^2\left(\frac{2}{N}-d\right)T + I_\phi^2(2-dN)^2\left(d-\frac{1}{N}\right)\cdot T\right] =$$

$$= N\cdot I_\phi^2\left[(dN-1)^2\left(\frac{2}{N}-d\right) + (2-dN)^2\left(d-\frac{1}{N}\right)\right]$$

3. all phases overlapped ($\frac{2}{3} < d < 1$, in Figure B.4.4).

   (this case has not been developed)

Comparing the equations in cases 1 and 2, a generic formula for the rms input current can be defined. Being $M = floor(N \cdot d)$,

$$I_{AC,rms} = \sqrt{N\left[(1+M-Nd)^2\left(d-\frac{M}{N}\right) + (M-Nd)^2\left(\frac{1+M}{N}-d\right)\right]}$$

The validity of the model has been compared with the value computed from the waveforms. Refer to Figure B.4.5: the two plotted functions are equal (the red one just lack in resolution)

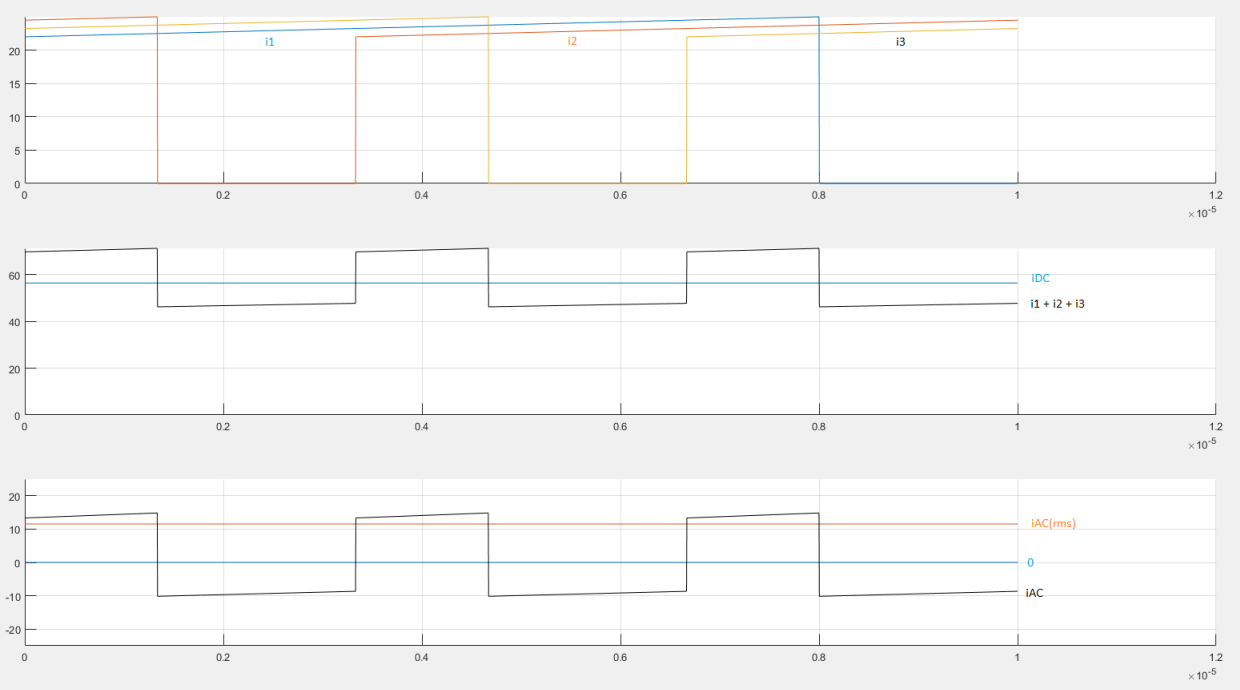


Figure B.4.4: 3-phases buck - all phases overlapped (d = 0.8)

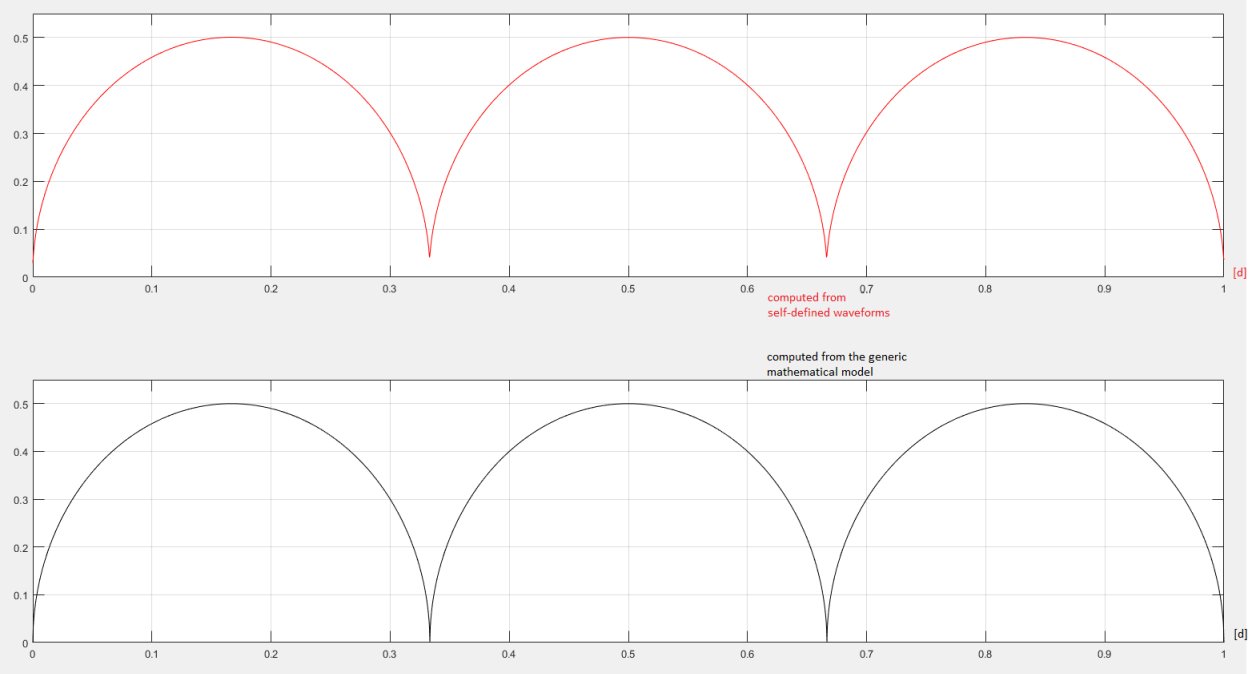


Figure B.4.5: model validation

(All the procedure refer to the *MatLab* script in Appendix C.2, which has been written by myself)

It is worth notice that particular care must be taken on the duty ratio of each phase. Recalling that

$$I_{DC} = I_{DC} = d \cdot N \cdot I_{\phi} = d \cdot I_o$$

in order to design an efficient converter, the equivalent duty ratio must be kept close to 1

$$d_{eq} = D = N \cdot d \approx 1$$

otherwise, the current delivered by the source (I_{DC}) increase too much (see Figure B.4.3 and Figure B.4.4); and, being the voltage fixed, the power dissipation increases as well, leading to very high power dissipation (and very awful efficiency).

APPENDIX C

MatLab codes

C.1 SCC design algorithm

```
close all;
clear all;
%-------------------------------------------------------------------------
step = 3
%-------------------------------------------------------------------------
maxPower = 1e3;
VinMax = 42;
M = 3;
d = [1/3 , 1/3 , 1/3];
eff = 95/100;
fsw = 100e3;
%-------------------------------------------------------------------------
VcRATED = 550;
VswRATED = 60;

ac = [
    0 1/3
    1/3 -1/3
    -1/3 0
    ];
vc = ones(1,length(ac(1,:))) * VcRATED;
aesr = abs(ac);
asw = [
    1/3 0 0 1/3 1/3 0
    0 1/3 0 1/3 0 1/3
    0 0 1/3 0 1/3 1/3
    ];
vsw = ones(1,length(asw(1,:))) * VswRATED;
%-------------------------------------------------------------------------
RL = (eff*VinMax/M)^2/maxPower;

Ro = RL * (1-eff)/eff;
%-------------------------------------------------------------------------

    A = zeros(1,length(ac(1,:)));
    for h=1:length(ac(1,:))
        for p=1:(length(d)-1)
            x=0;
            for m=p:(length(d)-1)
            x = x + ac(m,h);
            end
            A(h) = A(h) + ac(p,h)*x;
        end
    end
    A = sqrt(A);

    T = zeros(1,length(aesr(1,:)));
    for h=1:length(aesr(1,:))
        for p=1:length(d)
            T(h) = T(h) + aesr(p,h)^2/d(p);
        end
    end
    T = sqrt(T);


    S = zeros(1,length(asw(1,:)));
    for i=1:length(asw(1,:))
        for p=1:length(d)
            S(i) = S(i) + asw(p,i)^2/d(p);
        end
```

```
    end
    S = sqrt(S);


%boundaries CHOICE
thresholdWeightRSSL = 0.75;
thresholdESRweight = 0.25;

%CAPACITORS OPTIMIZATION-----------------------------------------------------

if step == 1

    weightRSSL = thresholdWeightRSSL;
    weightRFSL = 1 - weightRSSL;

    RSSL = Ro * sqrt(weightRSSL);
    RFSL = Ro * sqrt(weightRFSL);
    K2c=0;
    for h=1:length(ac(1,:))
        K2c = K2c + A(h)*vc(h);
    end
    Etot = K2c^2/2/fsw/RSSL;
    K1c = 2*Etot/K2c;
    C = K1c * A./vc;

    fid=fopen('designProcedure_step1_results.txt','wt');
    fprintf(fid, '%s\t%s\t%s\t%s\t%s\t%s\t%s\t\r\n', 'C1', 'C2', 'tolerance1', 'tolerance2', 'ESR1', 'ESR2', 'ParallelCap');
    fprintf(fid, '%f\t%f\t%d\t%d\t%d\t%d\t%d\t\r\n', C(1), C(2), 0, 0, 0, 0, 1);
    fclose(fid);




%ESR vs RFSL-----------------------------------------------------------------

elseif step == 2
    filename = 'designProcedure_step1_results.txt';
    delimiterIn = '\t';
    headerlinesIn = 1;
    F = importdata(filename,delimiterIn,headerlinesIn);

    ParallelCap = F.data(7);
    tolerance = [F.data(3) , F.data(4)];
    C = [F.data(1), F.data(2)]; %take the min value due to tolerance -> nominal value * (1-tolerance) > Ccomputed
    ESR = [F.data(5) , F.data(6)]*(150/100);%NOTE: the 150/100 factor is related to the ESR tolerance (50%)

    weightRSSL = 1;
    weightResr = 1;
    %
    while weightResr > thresholdESRweight
    while weightRSSL > thresholdWeightRSSL
        RSSL = 0;
        for h=1:length(C(1,:))
            RSSL = RSSL + A(h)^2/(C(h)*(1-tolerance(h)));
            %take the min value (worst case) due to tolerance -> nominal value
```

```
(1-tolerance) > Ccomputed
118         end
119         RSSL = RSSL / fsw / ParallelCap;
120         weightRSSL = (RSSL / Ro)^2;
121 
122         if weightRSSL > thresholdWeightRSSL
123            ParallelCap = ParallelCap + 1;
124         end
125     end
126 
127         weightRFSL = 1 - weightRSSL;
128         RFSL = Ro * sqrt(weightRFSL);
129 
130         RESR = 0;
131         for h=1:length(aesr(1,:))
132             RESR = RESR + ESR(h)*T(h).^2;
133         end
134         RESR = RESR / ParallelCap;
135 
136         weightResr = RESR / RFSL;
137 
138         if weightResr > thresholdESRweight
139                ParallelCap = ParallelCap + 1;
140            end
141         RSW = RFSL - RESR;
142 
143     end
144 
145     fid=fopen('designProcedure_step2_results.txt','wt');
146     fprintf(fid, '%s\t%s\t%s\t%s\t%s\t%s\t%s\t%s\t\r\n', 'C1', 'C2', 'tolerance1',↙
'tolerance2', 'ESR1', 'ESR2', 'ParallelCap');
147 %     fprintf(fid, '%f\t%f\t%s\t%s\t%s\t%s\t%d\t\r\n', C(1), C(2), tolerance(1),↙
tolerance(2), ESR(1), ESR(2), ParallelCap0*ParallelCap);
148     fprintf(fid, '%f\t%f\t%s\t%s\t%s\t%s\t%d\t\r\n', C(1), C(2), tolerance(1),↙
tolerance(2), ESR(1)*(100/150), ESR(2)*(100/150), ParallelCap);
149     fclose(fid);
150 
151 
152 
153 
154 
155 %SWITCHES OPTIMIZATION-----------------------------------------------------
156 elseif step == 3
157 
158     filename = 'designProcedure_step2_results.txt';
159     delimiterIn = '\t';
160     headerlinesIn = 1;
161     F = importdata(filename,delimiterIn,headerlinesIn);
162 
163     tolerance = [F.data(3) , F.data(4)];
164     ParallelCap = F.data(7);
165     C = [F.data(1), F.data(2)];
166     RSSL = 0;
167     for h=1:length(C(1,:))
168             RSSL = RSSL + A(h)^2/C(h)/(1-tolerance(h));
169             %take the min value (worst case) due to tolerance -> nominal value ↙
(1-tolerance) > Ccomputed
170     end
171     RSSL = RSSL / fsw / ParallelCap;
172     weightRSSL = (RSSL / Ro)^2;
```

```
173     weightRFSL = 1 - weightRSSL;
174
175     ESR = [F.data(5) , F.data(6)]*(150/100);%NOTE: the 150/100 factor is related
to the ESR tolerance (50%)
176
177     RESR = 0;
178     for h=1:length(aesr(1,:))
179         RESR = RESR + ESR(h)*T(h)^2;
180     end
181     RESR = RESR / ParallelCap;
182     RFSL = Ro * sqrt(weightRFSL);
183
184     weightResr = RESR / RFSL;
185
186     RSW = Ro * sqrt(weightRFSL) * (1- weightResr);
187     K2s=0;
188     for i=1:length(asw(1,:))
189         K2s = K2s + S(i)*vsw(i);
190     end
191     Atot = K2s^2/RSW;
192     K1s = Atot/K2s;
193     G = K1s * abs(S./vsw);
194     R = 1./G;
195
196
197     ESR = [F.data(5) , F.data(6)];
198     fid=fopen('designProcedure_step3_results.txt','wt');
199     fprintf(fid, '%25s = %.2f uF\r\n', 'C1', C(1)*1e6);
200     fprintf(fid, '%25s = %d V\r\n', 'rated voltage', vc(1));
201     fprintf(fid, '%25s = %.1f mOhm\r\n', 'ESR1', ESR(1)*1e3);
202     fprintf(fid, '%25s = %d%%\r\n', 'tolerance', tolerance(1)*100);
203     fprintf(fid, '%25s = %d\r\n', 'Parallel Capacitors', ParallelCap);
204     fprintf(fid, '%25s = %.2f uF (%d%% tolerance)\r\n', '-----> C1 Total', C(1)
*1e6*ParallelCap, tolerance(1)*100);
205     fprintf(fid, '%25s = %.1f mOhm\r\n', '---> ESR1 Total', ESR(1)
*1e3/ParallelCap);
206
207     fprintf(fid, '\n\n');
208     fprintf(fid, '%25s = %.2f uF\r\n', 'C2', C(2)*1e6);
209     fprintf(fid, '%25s = %d V\r\n', 'rated voltage', vc(2));
210     fprintf(fid, '%25s = %.1f mOhm\r\n', 'ESR2', ESR(2)*1e3);
211     fprintf(fid, '%25s = %d%%\r\n', 'tolerance2', tolerance(2)*100);
212     fprintf(fid, '%25s = %d\r\n', 'Parallel Capacitors', ParallelCap);
213     fprintf(fid, '%25s = %.2f uF (%d%% tolerance)\r\n', '-----> C2 Total', C(2)
*1e6*ParallelCap, tolerance(2)*100);
214     fprintf(fid, '%25s = %.1f mOhm\r\n', '---> ESR2 Total', ESR(2)
*1e3/ParallelCap);
215     fprintf(fid, '\n\n');
216     fprintf(fid, '%25s = %.1f V\r\n', 'Vds,off', VswRATED);
217     fprintf(fid, '%25s = %.1f mOhm\r\n', 'Ron1', R(1)*1e3);
218     fprintf(fid, '%25s = %.1f mOhm\r\n', 'Ron2', R(2)*1e3);
219     fprintf(fid, '%25s = %.1f mOhm\r\n', 'Ron3', R(3)*1e3);
220     fprintf(fid, '%25s = %.1f mOhm\r\n', 'Ron4', R(4)*1e3);
221     fprintf(fid, '%25s = %.1f mOhm\r\n', 'Ron5', R(5)*1e3);
222     fprintf(fid, '%25s = %.1f mOhm\r\n', 'Ron6', R(6)*1e3);
223
224 %     fprintf(fid, '\n\n');
225 %     fprintf(fid, '%15s = %.2f mOhm\r\n', 'Expected Ro', Ro;
226     fclose(fid);
227
```

```
228
229 %     fid=fopen('designProcedure_step4_results.txt','wt');
230 %
231 %     R = floor(R*1e3)/1e3; %using integer multiples of [mOhm]
232 %
233 %     RSSL =
234 %
235 %     fclose(fid);
236
237 else %
238 end%STEP
239
240 clear i h p m x;
```

C.2 Multi-phase Buck Converter rms-Input Capacitor Current

```
clc
clear all
close all


%_____________________________________________________________________
%RMS current computation and waveform plot of Cin
%_____________________________________________________________________

%Starting working conditions
T = 10e-6;
Dmax=1;
Nphi=3;
Imax=25;
Imin=22;

dI = Imax-Imin;
Io = (Imax+Imin)/2;

D=linspace(0,Dmax,Dmax*Nphi*1e3+1);
t = linspace(0, T, Nphi*1e3);
dt = T/length(t);

Ton = T*D;
m = (Imax-Imin)./Ton;

i_RMS = zeros(1,length(D));
i_AVG = zeros(1,length(D));
c = zeros(1,length(D));
f = zeros(1,length(D));

%waveforms
for d=1:length(D)
%-------------------------
jx = 1;
x = zeros(1,length(t));
x(jx) = Imin;
for j=jx+1:(length(t)*D(d))
    i = j-1;
    x(j) = x(i) + m(d)*dt;
end

    if D(d)==0.3 | D(d) ==0.5 | D(d)==0.8
    figure
    subplot(3,1,1)
    hold on
    plot(t,x);
    ylim([0 inf])
    end

for n=2:Nphi
    jx=(n-1)*length(t)/Nphi+1;
    xx = zeros(1,length(t));
    xx(jx) = Imin;
    for j=jx+1:(jx+length(t)*D(d))
        if j>length(t)
            j = j-length(t);
        end
        i = j-1;
        if i==0
```

```
            i=length(t);
        end
        xx(j) = xx(i) + m(d)*dt;
    end

    x = x + xx;

    if D(d)==0.3 | D(d) ==0.5 | D(d)==0.8
    subplot(3,1,1)
    hold on
    plot(t,xx);
    ylim([0 inf])
    end
end
    grid on
%-------------------------

%waveform characteristics
i_AVG(d)=mean(x);
i_RMS(d)=rms(x-i_AVG(d));
irmsX = i_RMS(d)*ones(1,length(t));
iavgX = i_AVG(d)*ones(1,length(t));

if D(d)==0.3 | D(d) ==0.5 | D(d)==0.8

subplot(3,1,2)
hold on
plot(t,iavgX);
plot(t,x,'k');
ylim([0 inf])
grid on
%
subplot(3,1,3)
hold on
plot(t,zeros(1,length(t)));
plot(t,irmsX);
plot(t,x-i_AVG(d),'k');
ylim([-25 25])
grid on
end


%------ equivalent model to be tested
    M = floor(Nphi*D(d));
    AA = D(d) - 1/Nphi*M;
    BB = 1/Nphi - AA;
    CC = M + 1 - Nphi*D(d);
    DD = M - Nphi*D(d);

    c(d) =        AA*CC^2;
    c(d) = c(d) + BB*DD^2;
    c(d) = c(d) * Nphi;

    c(d) = c(d)^0.5;
%------
end

figure
hold on
subplot(2,1,1)
```

```
121 plot(D,i_RMS/Io,'r')
122 ylim([0 0.55])
123 grid on
124 subplot(2,1,2)
125 plot(D,c,'k')
126 ylim([0 0.55])
127 grid on
128
129
130
```

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