POLITECNICO DI TORINO

Master degree in Electronic Engineering

Master degree Thesis

Fabrication of highly scalable Non Volatile Memory

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A mio padre

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Summary

This thesis investigates the design and fabrication of advanced non-volatile memory (NVM) technologies capable of meeting the demands of next-generation computing systems. As traditional memory architectures face limitations in terms of scalability, power efficiency, and integration with advanced CMOS nodes, this work explores alternative memory solutions that offer improved performance, endurance, and miniaturization potential.

The study begins with an in-depth exploration of ferroelectric field-effect transistors (Fe-FETs) utilizing hafnium oxide as the ferroelectric material. Emphasis is placed on material selection, interfacial layer engineering, and process integration to enable scalable, low-power memory solutions. The investigation then shifts to resistive switching memory (ReRAM), focusing on hafnium oxide-based switching layers, electrode materials, and fabrication strategies to optimize switching reliability and device endurance.

Further, the thesis explores carbon nanotube-based memory (CNT-NRAM), examining the synthesis, purification, and alignment of CNTs for high-speed, low-power memory applications. Comparative analyses of single-walled and multi-walled CNTs, as well as their deposition and integration methods, are presented to evaluate their suitability for future memory systems.

Finally, the work addresses gate-all-around (GAA) based memory architectures, including SONOS and Fe-FET implementations. These structures are evaluated for their superior electrostatic control, scalability, and compatibility with nanosheet and nanowire configurations. Physical design considerations such as geometry, material selection, and device structure are analyzed to enhance memory performance and integration with modern CMOS technologies.

Overall, the thesis offers a fabrication-driven perspective on emerging NVM technologies, laying the groundwork for their adoption in advanced semiconductor applications including artificial intelligence, edge computing, and high-density storage.

Acknowledgements

I would like to express my gratitude towards Prof. GIANLUCA PICCININI for providing me this thesis topic and his valuable guidance throughout my work. I am also immensely grateful to Dr. MO FABRIZIO, Dr. ARDESI YURI, Mr LISTO ROBERTO , for their continuous support, feedback and valuable discussions which have greatly enhanced the content of the thesis.

I express my sincere gratitude to my parents whose love and unconditional support have been my guiding source of strength. Finally, I am grateful to all my friends and colleagues who have supported me in various ways to complete this work.

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If you cannot understand my
argument, and declare
it's Greek to me
you are quoting Shakespeare.

[B. Levin, Quoting Shakespeare]

Chapter 1

Introduction

1.1 Background

The future of electronics is on the verge of transformation with the increasing demand for faster, low-power, and efficient devices.Central to this transformation is the growing demand for non-volatile memories (NVMs), which retain data in the absence of power. This technology is crucial for the smooth operation of energy-efficient systems,enabling devices to store data and run programs without a constant power supply.As the field of electronics advances, NVM has become an integral component of energy-efficient systems.

The limitations of DRAM and Flash memory are becoming more prominent as technology scales down.As device dimensions shrink, the shortcomings of traditional memory technologies become more evident in terms of scalability, endurance, power efficiency, and write latency [55].To overcome these limitations, the industry is exploring alternative memory architectures and materials that offer high scalability without compromising performance.

The scaling down of Flash memory beyond the 2D planar architecture has led to innovations such as 3D NAND [126], yet it still suffers from endurance issues and increased fabrication complexity.Similarly, DRAM, although not an NVM, is volatile and constrained by refresh cycles and high energy consumption [133].These technologies face critical bottlenecks in terms of endurance, scalability, latency, and power consumption [167, 118, 21].

With the increasing adoption of AI/ML workloads and edge computing, these limitations are no longer acceptable, prompting the semiconductor industry to pursue alternative NVM solutions.

1.2 The Need for Scalable NVMs

As computing becomes seamlessly integrated into everyday life, there is an urgent need for NVM technologies that are scalable, reliable, energy-efficient, and CMOS-compatible. Scaling memory technologies ensures increased data density and improved performance. However, shrinking memory devices below the 10 nm regime introduces complexities such as short-channel effects, increased leakage, and reduced retention [153]. Traditional memory technologies like DRAM and Flash memory encounter severe limitations at smaller technology nodes. These issues demand novel device architectures and materials to maintain non-volatility without sacrificing device performance.

Emerging non-volatile memory (NVM) technologies—such as Ferroelectric Field-Effect Transistors (Fe-FETs), Resistive Random-Access Memory (ReRAM), Carbon Nanotube-based NRAM (CNT-NRAM), and Gate-All-Around (GAA) NVM architectures—have shown significant potential in overcoming the limitations of conventional NVMs. For example, ReRAM operates by altering the resistance state of a material to store information, in contrast to traditional SONOS memory, which relies on charge trapping mechanisms for data retention [155]. Furthermore, the discovery of ferroelectric properties in hafnium oxide (HfO_2), a material compatible with standard

CMOS fabrication processes, has paved the way for scalable and CMOS-integrable ferroelectric memory technologies [104]. Moreover, advances in Gate-All-Around (GAA) transistor structures further enhance electrostatic control and enable continued device scaling [163].

In conclusion, continued scaling of non-volatile memory (NVM) technologies is crucial to ensuring that device performance remains uncompromised as technology nodes continue to shrink. Advanced NVM solutions—such as Resistive RAM (ReRAM), Ferroelectric FETs (Fe-FETs), Gate-All-Around FET (GAAFET)-based NVMs, and Carbon Nanotube-based NVMs (CNT-NVMs)—have emerged as strong candidates to address the challenges posed by aggressive miniaturization. These next-generation memory technologies offer the potential to meet the growing demands for faster, more efficient, and compact devices. Furthermore, they are well-positioned to support future advancements in key domains such as machine learning, artificial intelligence, and the Internet of Things (IoT), thereby sustaining innovation across the electronics industry.

1.3 Motivation

The continuous scaling of semiconductor devices, as predicted by Moore's Law, has led to significant advancements in computing performance and integration density. However, traditional memory technologies such as DRAM and Flash are facing fundamental limitations in terms of scalability, power efficiency, speed, and endurance. These constraints are becoming increasingly critical in the context of emerging applications like artificial intelligence, edge computing, the Internet of Things (IoT), and high-performance mobile systems, which demand faster, smaller, and more energy-efficient memory solutions.

To meet these demands, there is a pressing need to explore and develop alternative non-volatile memory (NVM) technologies that can offer superior performance while remaining compatible with advanced CMOS nodes. Innovations in materials, device structures, and fabrication techniques have opened up promising avenues, including ferroelectric FETs (Fe-FETs), resistive RAM (ReRAM), carbon nanotube-based memories (CNT-NRAM), and Gate-All-Around (GAA) architectures.

This thesis is motivated by the potential of these emerging NVM technologies to overcome the existing bottlenecks of conventional memory and to pave the way for a new generation of memory systems that are faster, more reliable, and highly scalable. By focusing on the fabrication and integration challenges, this work aims to contribute to the practical realization of these novel memory technologies.

1.4 Scope of the Thesis

The scope of this thesis is to explore, analyze, and compare the fabrication methodologies and material characteristics of emerging non-volatile memory (NVM) technologies that are suitable for integration into advanced CMOS technology nodes. As the limitations of conventional memories like DRAM and Flash become increasingly pronounced in terms of scalability, endurance, and power efficiency, this work investigates novel memory architectures that promise higher density, faster switching, and lower power consumption.

Specifically, the thesis encompasses the following areas:

- **Chapter 2: Ferro-electric based Non Volatile Memories :** This chapter is dedicated to the exploration of Ferroelectric Field-Effect Transistors (Fe-FETs) as a next-generation non-volatile memory technology. The chapter begins with a conceptual overview of ferroelectricity and its relevance to memory applications, followed by a focused discussion on hafnium oxide — a scalable, CMOS-compatible ferroelectric material. The scope includes an in-depth examination of the fabrication steps of Fe-FETs, from substrate and interfacial layer selection to gate material deposition, source/drain implantation, and contact formation.

- **Chapter 3: Resistive Switching Memories :** The chapter explores the fundamental principles of resistive switching, classifying the different switching mechanisms and their relevance to memory applications. It outlines the complete fabrication process—from substrate selection to electrode deposition—and emphasizes the importance of material choice for both the switching layer and electrodes. Special attention is given to hafnium dioxide (HfO) as a switching material, including its deposition techniques and optimal thickness. The chapter also includes a comparative analysis of electrode materials based on performance metrics and identifies suitable configurations for various applications. Overall, this chapter establishes a fabrication-centric understanding of ReRAM technology, highlighting key parameters that influence its scalability and integration into modern semiconductor processes.
- **Chapter 4: Carbon Nanotube-based Non-Volatile Memory :** This chapter explores the potential of Carbon Nanotube (CNT)-based Non-Volatile Memory (NRAM) as a highly scalable, high-speed, and low-power memory technology. It provides a comprehensive overview of the fabrication process, encompassing substrate selection, bottom electrode deposition, CNT synthesis and purification, CNT alignment on the wafer, and top electrode formation. The chapter discusses the underlying working mechanisms of CNT-based memories, including charge trapping, resistive switching, and electromechanical switching. It also addresses critical design parameters such as electrode material selection, CNT layer thickness, and deposition techniques that influence device performance. Furthermore, it offers a comparative analysis of Single-Walled CNTs (SWCNTs) and Multi-Walled CNTs (MWCNTs) in terms of reliability, efficiency, and integration potential, and evaluates different purification methods and their effects on memory behavior.
- **Chapter 5: Advanced GAA-Based NVM Architectures and Their Fabrication :** This delves into the development and fabrication of Gate-All-Around (GAA)-based Non-Volatile Memory (NVM) architectures, highlighting their potential for scaling beyond the limits of traditional planar and FinFET structures. The chapter details the complete fabrication processes for two prominent GAA-based NVM types: GAA-SONOS and GAA-FeFET, emphasizing their respective structural flows, material stacks, and integration strategies. It provides an in-depth discussion of the working mechanisms for both devices—charge trapping in SONOS and polarization switching in FeFETs—explaining how GAA configurations enhance electrostatic control and improve device reliability. Additionally, the chapter compares nanosheet and nanowire-based GAA structures, analyzing their impact on performance parameters such as threshold control, retention, and scalability. Considerations around material selection, geometrical dimensions (e.g., nanowire diameter, nanosheet thickness/width), and physical design are also explored to optimize GAA-based NVM integration for future CMOS technologies.

Overall, the research aims to provide a comprehensive understanding of the fabrication techniques, material selection, and design trade-offs involved in realizing future-proof, high-density NVMs.

1.5 Use of AI Tools in Thesis Preparation

During the development of the thesis Fabrication of highly scalable Non Volatile Memory open Ai's ChatGPT was used for language refinement, paraphrasing, analyze complex technical papers and latex code generation.ChatGPT was not used to generate any simulations, research data, or figures.

Applications of ChatGPT in This Work

1. **Rephrasing** – Detailed technical inputs were provided based on my analysis of academic papers, and ChatGPT was used to rephrase the content into grammatically accurate and academically presentable format. All outputs were manually verified.

2. **Summarization** – ChatGPT assisted in simplifying and summarizing highly technical papers that were challenging to interpret, aiding in conceptual clarity.

3. **Comparative Tables** – Based on data and insights I supplied, ChatGPT was used to organize content into tabular comparisons (e.g., fabrication process evaluations). The tables were reviewed and validated manually.

4. **LaTeX Code Generation** – ChatGPT was extensively used to generate and format LaTeX code for tables, equations, and overall document structure. The outputs were tested and edited to ensure academic accuracy and formatting compliance.

Chapter 2

Ferro-electric based Non Volatile Memories

2.1 Introduction

Ferroelectric-based Non-Volatile Memories (FeFETs) represent a transformative advancement in memory technology by harnessing the unique properties of ferroelectric materials. Unlike traditional dielectrics, ferroelectrics retain polarization after the removal of an electric field, enabling non-volatile data storage. Among various dielectric types, ferroelectric materials such as hafnium oxide (HfO) stand out due to their scalability, CMOS compatibility, and robust retention and endurance. This chapter delves into the fundamental principles of ferroelectricity, the evolution of HfO as a viable material for FeFETs, and the comprehensive fabrication processes that enable their integration into advanced semiconductor devices. The chapter also explores material selection for interfacial layers and gate electrodes, deposition techniques for ferroelectric films, and doping methods crucial for enhancing FeFET performance in next-generation memory applications.

2.2 Ferroelectricity – A generalized view

Ferroelectric materials are a type of dielectric insulator. Dielectrics can be classified into four main types [124]:

- Paraelectricity (Para-electrics)
- Piezoelectricity (Piezo-electrics)
- Pyroelectricity (Pyroelectrics)
- Ferroelectricity (Ferroelectrics)

These four categories are not entirely distinct, but they are related to each other as illustrated in 2.1.

When a voltage is applied to a dielectric material, no electric current flows. Instead, the material becomes polarized, with one side accumulating positive charges and the other negative charges. This process is known as *polarization*. In paraelectric materials, polarization disappears once the external voltage is removed. However, in ferroelectric materials, the polarization remains even when the voltage is reduced to zero.

Piezoelectric materials are unique in that they become polarized when subjected to mechanical stress or deformation. Conversely, they can also deform when a voltage is applied to them. *Pyroelectric* materials, on the other hand, generate electrical potentials in response to changes in temperature. When heated, an imbalance of charge occurs due to the disruption of the balance with surface valence electrons, resulting in polarization. Like ferroelectrics, pyroelectrics can

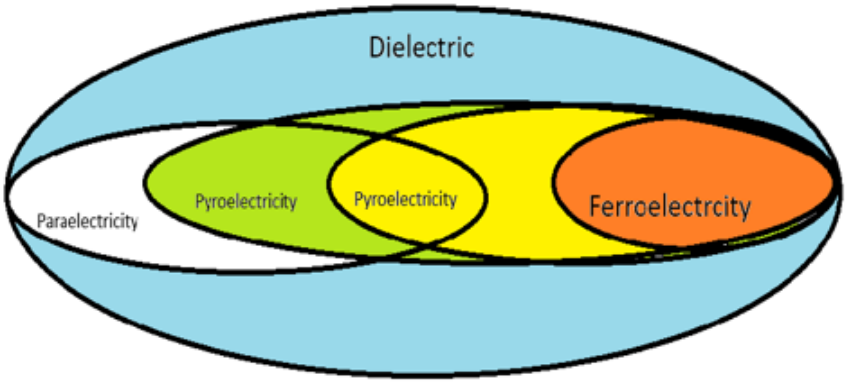

Figure 2.1: Venn diagram denoting the categories of dielectric materials.

exhibit spontaneous polarization even without an applied voltage, although their polarization direction cannot be reversed.

Ferroelectrics exhibit both piezoelectric and pyroelectric properties, meaning they respond electrically to both applied voltage and mechanical stress.Additionally, some ferroelectrics have atomic structures that respond to magnetic fields as well. *Ferromagnetism* shares similar traits with ferroelectricity, as ferromagnetic materials also form domains that remain magnetized even when no external magnetic field is present. The term *ferroelectricity* is derived from *ferromagnetic* materials, reflecting this similarity.

Historically, potassium sodium tartrate (also known as Rochelle salt) was a commonly used ferroelectric material. More recently, potassium dihydrogen phosphate (KDP) and barium titanate ($BaTiO_3$) have become typical examples of ferroelectrics.

2.3 Ferroelectricity in Hafnium Oxide

Ferroelectric materials have long been essential for memory and sensing applications, with perovskite-based compounds playing a dominant role. However, their integration into modern semiconductor technology is severely limited by scalability, reliability, and environmental concerns. Perovskite ferroelectrics require high crystallization temperatures (>600°C) and a minimum thickness of ∼50 nm, making them unsuitable for sub-10 nm nodes [98]. Additionally, issues such as fatigue, retention loss, and regulatory restrictions on lead-based materials further hinder their widespread adoption.

The discovery of ferroelectricity in hafnium oxide (HfO_2) has revolutionized the field by offering a CMOS-compatible alternative to traditional perovskites. Unlike perovskites, HfO_2 can exhibit ferroelectricity in ultra-thin films (<10 nm), making it highly scalable [98]. It also requires a lower crystallization temperature (∼400°C), aligning more effectively with semiconductor processing requirements [98]. Furthermore, HfO_2 demonstrates a high coercive field (0.8–2 MV/cm), significantly enhancing retention and endurance while maintaining scalability [97].

HfO_2-based Ferroelectric Field-Effect Transistors (FeFETs) offer significant advantages over perovskite-based alternatives. The ability of HfO_2 to sustain ferroelectricity in ultra-thin films allows FeFETs to be integrated into advanced semiconductor nodes, overcoming the scalability limitations of perovskites [98]. Its lower crystallization temperature ensures compatibility with standard CMOS fabrication processes, eliminating the need for high-temperature processing that could damage other semiconductor components [98]. The high coercive field of HfO_2 improves data retention, making FeFETs more reliable for long-term memory applications [97].

Additionally, the polarization of HfO_2 (30–60 $\mu C/cm^2$) is comparable to PZT, ensuring strong

and stable charge storage, while its significantly lower permittivity (∼30 vs. ∼1000 for PZT) minimizes leakage and enhances endurance [97]. This balance of properties is crucial for FeFETs, which rely on stable ferroelectric switching for efficient memory operation. The structural versatility of HfO_2, particularly its ability to transition into the desired ferroelectric orthorhombic phase through SiO_2 doping and mechanical encapsulation, further strengthens its suitability for FeFETs [97]. Without this phase stabilization, FeFETs would suffer from performance degradation due to unwanted transitions into non-ferroelectric phases.

The role of the cap layer in maintaining the orthorhombic phase is another key advantage for FeFETs. A cap layer is an additional material layer, typically made of metals or dielectrics, deposited on top of the hafnium oxide film during or after crystallization. By controlling stress and thermal conditions during crystallization, the cap layer ensures that HfO_2 remains in its ferroelectric state, thereby maintaining the device's reliability and endurance [97]. This makes FeFETs based on HfO_2 highly robust against fatigue and retention loss, issues that commonly affect perovskite-based memories.

HfO_2's ferroelectric properties make it an ideal candidate for FeFETs, where data storage is achieved through the polarization states of the gate insulator. These devices leverage the orthorhombic phase of HfO_2 for non-volatile memory applications, offering lower power consumption and faster switching speeds compared to conventional Flash memory [97]. The combination of CMOS compatibility, ultra-thin scalability, high endurance, and reliable retention establishes hafnium oxide as the leading ferroelectric material for next-generation FeFET technology.

2.4 Fe-FET Fabrication

FeFETs have gained significant interest for non-volatile memory (NVM) applications due to their low power consumption, fast switching speeds, and CMOS compatibility [3]. However, fabricating FeFETs involves several complex steps, each influencing device performance, endurance, and scalability.

Key fabrication steps include:

1. Substrate Selection
2. Interfacial Layer (IL) Formation
3. Deposition of Ferroelectric HfO_2 Layer
4. Gate Electrode Formation
5. Source/Drain Implantation and Activation
6. Contact

Substrate Selection

A **p-type bulk silicon (Si)** substrate is selected as the base material for FeFET fabrication 2.2.

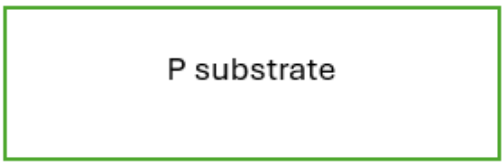

Figure 2.2: Substrate Selection

Interfacial Layer

An **interfacial layer of silicon oxynitride** was developed by rapid thermal annealing [129] as illutrated in figure 2.3.

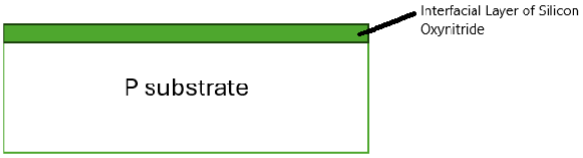

Figure 2.3: Interfacial layer formation

Deposition of Ferroelectric HfO_2 Layer

The hafnium layer is deposited using atomic layer deposition (ALD), followed by rapid thermal annealing (RTA) to activate the ferroelectric property of hafnium dioxide [102, 129, 146] as illutrated in figure 2.4.

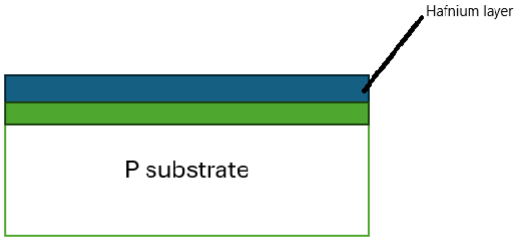

Figure 2.4: Deposition of Ferroelectric HfO_2 Layer

Gate Electrode Formation

Titanium Nitride gate electrode is deposited by PVD (Physical Vapor Deposition) as illutrated in figure 2.5.

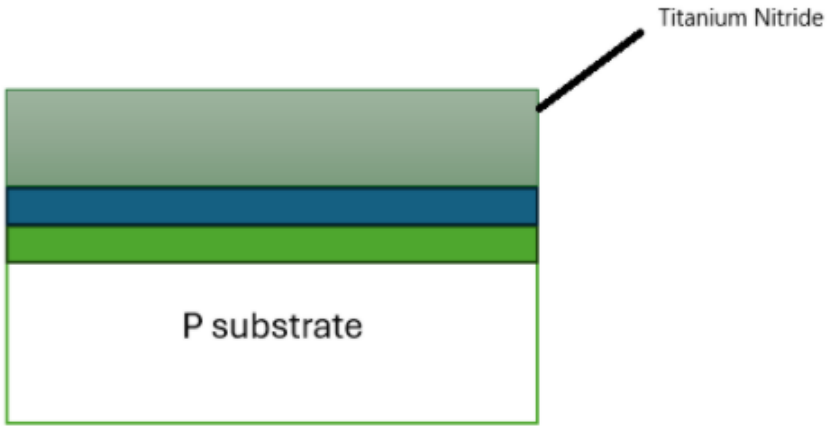

Figure 2.5: Gate Electrode Formation

Gate Lithography

A polysilicon layer is deposited over the TiN gate 2.6, followed by a standard masking and etching process to define the gate area 2.7.

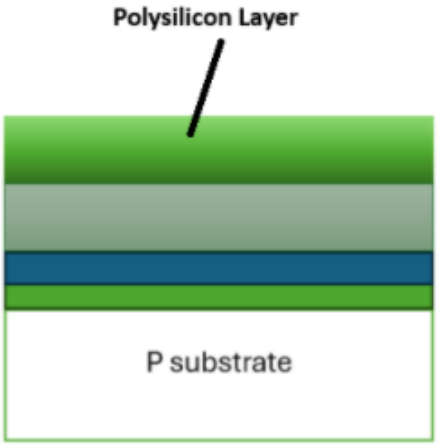

Figure 2.6: Polysilicon Formation

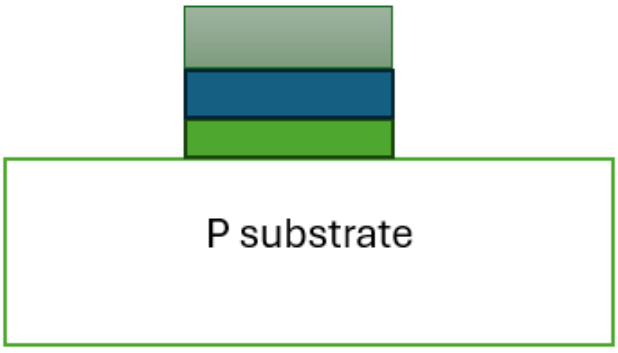

Figure 2.7: Device after standard photolithography and etching

Spacers Formation

Sidewall spacers are formed using dielectric materials (e.g., SiN or SiO_2). The deposited spacer material is etched back to leave only the sidewall spacers as illustrated in the figure 2.8. These spacers help isolate the gate from the source/drain regions.

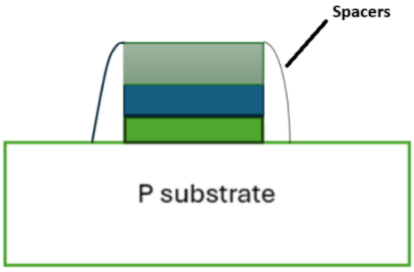

Figure 2.8: Spacer formation

Source/Drain Implantation and Activation

Dopants (Arsenic) are implanted into the source and drain (S/D) regions using ion implantation. Rapid thermal annealing (RTA) at approximately 1000 °C activates the implanted dopants. Annealing also repairs implantation damage and improves junction quality.

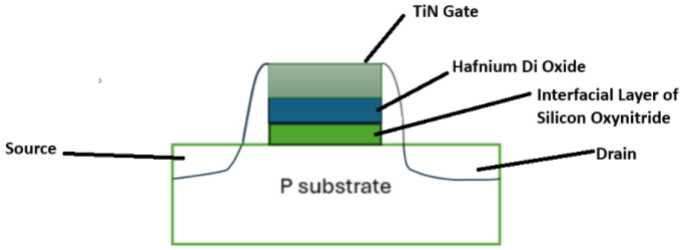

Figure 2.9: Final Device after Ion implantation and dopant activation

2.5 Substrate Selection

The choice between Bulk FeFET and SOI FeFET architectures is crucial for optimizing memory window (MW), interlayer field (E_{IL}), and overall device reliability in non-volatile memory (NVM) applications. A detailed numerical comparison demonstrates the clear advantages of SOI FeFETs over Bulk FeFETs, particularly in MW stability, E_{IL} reduction, and endurance.

Bulk FeFETs are constructed on a conventional silicon substrate, offering benefits such as low manufacturing costs and straightforward fabrication. However, as device dimensions continue to scale down, challenges such as short-channel effects and parasitic capacitances become more pronounced. To mitigate these issues, Silicon-on-Insulator (SOI) technology was introduced, which incorporates a thin silicon layer separated from the bulk substrate by an insulating layer. This structural modification provides enhanced electrostatic control, reduced leakage currents, and improved scalability, though it comes at the cost of increased fabrication complexity and potential thermal management challenges.

While Bulk FeFETs offer simpler fabrication, they also introduce performance trade-offs, including hot electron effects, where electrons from the substrate become trapped in the dielectric layer. This phenomenon adversely affects memory window, data retention, and device endurance. One strategy to address these limitations is by modifying the gate metal work function, which can improve the memory window and reduce charge trapping [92]. However, this approach also increases the electric field stress on the dielectric layer, potentially leading to reduced device longevity [92].

In contrast, SOI FeFETs provide an additional advantage through back-gate control, which improves electrostatic management and results in a larger memory window [92]. Unlike Bulk FeFETs, where gate work function modification is necessary, SOI FeFETs eliminate this requirement, thus minimizing electric field stress on the dielectric layer and enhancing overall device reliability [92].

In conclusion, both architectures offer distinct features. The bulk structure provides ease of fabrication and low cost, but introduces trade-offs such as short-channel effects, hot electrons, and increased electric field stress. These challenges are addressed in the SOI architecture, which exhibits better electrostatic control, a larger memory window, and reduced E_{IL}, making it a more robust solution for high-performance, scalable non-volatile memory applications.

2.6 Interfacial Layer (IL)

The interfacial layer (IL) in ferroelectric field-effect transistors (Fe-FETs) is a thin dielectric layer that sits between the ferroelectric HfO_2 layer and the semiconductor channel (typically silicon). This layer plays a critical role in determining Fe-FET performance by influencing charge trapping, polarization switching, retention, and endurance [130].

2.6.1 Materials Used for Interfacial Layer in FeFETs

The most commonly used interfacial layer (IL) materials in FeFET fabrication are reported in the table below [130, 144, 129]:

Table 2.1: Comparison of Common Interfacial Layer Materials Used in FeFET Fabrication

Material Used	**Composition**	**Advantages**	**Challenges**
Silicon Dioxide (SiO_2)	Thin oxide layer between the Fe-layer and the semiconductor	- Reduces charge injection - Provides a stable dielectric interface	- Higher charge trapping - Memory Window (MW) shrinkage over cycles
Silicon Oxynitride (SiON)	SiO_2 with incorporated nitrogen (N) atoms	- Lowers defect density - Reduces charge trapping and improves endurance - Better retention compared to SiO_2	- Higher flicker noise - Requires precise RTA processing
High-k IL (HfSiON, Al_2O_3, Ta_2O_5)	Alternative high-k IL materials used in advanced FeFETs	- Suppresses depolarization effects - Enables better polarization stability	- Higher process complexity - Needs optimization for CMOS compatibility

2.6.2 Techniques for Depositing the Interfacial Layer (IL)

Various deposition techniques are deployed based on the material type and the required interface quality. Some of the commonly used methods include thermal oxidation, rapid thermal annealing (RTA), and atomic layer deposition (ALD). Each of these has its unique advantages and limitations, which are summarized in the table below [130, 144, 129]:

Table 2.2: Comparison of Deposition Techniques for Interfacial Layers (ILs) in FeFETs

Technique	**Process Description**	**Materials Used**	**Thickness Control**	**Key Benefits**	**Challenges**
Thermal Oxidation (SiO_2)	Self-terminating chemical oxidation in an oxygen-rich environment to grow a uniform SiO_2 layer on the Si substrate.	SiO_2	∼1 nm	- Simple and widely used - Compatible with CMOS processing	- High charge trapping - Memory window (MW) shrinkage over cycles
RTA in N_2 (SiON)	SiO_2 layer is annealed in a nitrogen-rich environment at 900–1050 °C, incorporating nitrogen atoms into the layer.	SiON (N-doped SiO_2)	∼1 nm	- Improves endurance and MW stability - Reduces charge trapping	- Higher flicker noise - Requires precise annealing conditions
Atomic Layer Deposition (ALD) for High-k ILs	Ultra-thin, layer-by-layer deposition using precursors ($HfCl_4$, $SiCl_4$, Al-based) in a cyclic process.	HfSiON, Al_2O_3, Ta_2O_5	∼1 nm (high precision)	- Better control over IL thickness - Suppresses depolarization effects - Enhances FeFET endurance	- Complex and costly process - Integration challenges with standard CMOS FeFET fabrication

Thus, the interfacial layer (IL) material selection and fabrication process play a crucial role in FeFET performance, impacting memory window (MW) stability, endurance, and retention. Silicon dioxide (SiO_2), typically formed through thermal oxidation, experiences significant charge trapping, which contributes to MW shrinkage over multiple cycles. In contrast, silicon oxynitride (SiON), produced via rapid thermal annealing (RTA) in a nitrogen (N_2) environment, exhibits enhanced endurance, better retention, and improved noise immunity, making it a more reliable choice for FeFET applications.

Further advancements involve high-k interfacial layers (e.g., HfSiON, Al_2O_3), deposited using atomic layer deposition (ALD), which provide superior charge screening and suppress depolarization effects, ensuring long-term stability. However, these materials introduce higher fabrication complexity, requiring precise process control to integrate effectively into FeFET structures.

In terms of performance, SiON is superior to SiO_2 as an interfacial layer in FeFETs due to its enhanced switching efficiency, larger and more stable memory window, improved endurance, better retention, reduced charge trapping, and greater scalability for advanced memory applications [4].

To optimize FeFET reliability and scalability, future research should focus on hybrid IL structures, process refinements in RTA and ALD techniques, and minimizing IL thickness to reduce charge trapping. By implementing optimized IL engineering strategies, FeFETs can be positioned as a leading candidate for next-generation non-volatile memory (NVM) and neuromorphic computing applications.

2.7 Deposition of Ferroelectric HfO_2 Layer

The deposition technique of the hafnium dioxide (HfO_2) layer in FeFETs plays a critical role in determining the device's performance, particularly in terms of scalability, retention, endurance, and switching characteristics.

As previously discussed, the ferroelectric properties of HfO_2 arise from its metastable orthorhombic phase, which is strongly influenced by both the deposition method and subsequent thermal treatment. The stabilization of this phase is governed by several factors, including doping, oxygen vacancies, surface/interface or grain boundary energy, electric fields, and mechanical stress [138, 146]. Therefore, a thorough understanding of different deposition techniques and their impact on ferroelectric behavior is essential.

Commonly used HfO deposition techniques include Atomic Layer Deposition (ALD), Physical Vapor Deposition (PVD) and Pulsed Laser Deposition (PLD). The ferroelectric phase is typically induced through a post-deposition thermal process, such as Rapid Thermal Annealing (RTA) or other heating treatments, which facilitate the phase transformation necessary for ferroelectricity.

2.7.1 Atomic Layer Deposition

Atomic Layer Deposition (ALD) is a precise thin-film growth technique that falls under the category of chemical vapor deposition (CVD). It relies on the sequential and self-limiting reactions of chemical precursors, which interact with the substrate surface one at a time [183]. By alternating exposure to these reactants, a thin film is gradually formed, allowing for exceptional control over thickness and uniformity.

The deposition of hafnium oxide (HfO_2) thin films using ALD requires careful selection of hafnium precursors and oxygen sources to achieve high-quality films with desirable electrical and structural properties. The choice of precursor influences thermal stability, impurity levels, growth rate, and film density, all of which impact the performance of HfO_2-based semiconductor devices.

Different hafnium precursors are used in ALD depending on thermal stability, contamination risk, and growth rate. Three of the most studied precursors, along with their advantages and disadvantages, are reported below [146]:

A. Hafnium Chloride ($HfCl_4$)

- **Pros:**
  - High thermal stability, making it suitable for high-temperature ALD.
  - Well-established in thermal ALD processes.
- **Cons:**
  - Produces corrosive by-products like HCl, which can lead to contamination issues.
  - Chlorine residues in the film can degrade device performance.

B. Cyclopentadienyl Hafnium Precursors (Cp_2HfMe_2, $(MeCp)_2HfMe_2$, $(MeCp)_2Hf(OMe)Me$)

- **Pros:**
  - Good thermal stability.
  - Lower impurity contamination compared to chloride-based precursors.
- **Cons:**
  - Slower growth rate, making deposition less efficient compared to other hafnium precursors.

C. Alkylamide (or Alkoxide) Precursors ($Hf(NetMe)_4$, $Hf(NMe_2)_4$)

- **Pros:**
  - Low impurity contamination, leading to high-purity HfO_2 films.
  - Produces dense, high-quality films.
  - Compatible with both thermal ALD and plasma-enhanced ALD (PEALD).
- **Cons:**
  - Limited thermal stability (250–300 °C), which restricts process flexibility.

Additionally, thermal budget, dopant concentrations, and film thickness are crucial features in determining the performance of the fabricated device. The following table summarizes the effects of these factors on the phase stability of HfO_2, highlighting the conditions needed to achieve the desired ferroelectric properties [146].

Table 2.3: Factors Affecting HfO_2 Phase Stability

Factor	**Role in HfO_2 Phase Stability**
Thermal Budget	Determines phase stability; transitions from monoclinic (low temperature) → tetragonal (moderate temperature) → orthorhombic (high temperature, ferroelectric).
Dopant Size < 155 pm	Promotes tetragonal phase; with annealing, it transforms into the orthorhombic phase (ferroelectric).
Dopant Size > 155 pm	Promotes cubic phase, which acts as an intermediate before transitioning to the orthorhombic phase.
Film Thickness < 10 nm	Forms monoclinic phase, which is non-ferroelectric.
Film Thickness > 10 nm	Promotes orthorhombic phase, exhibiting ferroelectricity.

2.7.2 Sputtering

Sputtering deposition is a physical vapor deposition (PVD) method utilized for thin-film fabrication, where atoms are dislodged from a target material and deposited onto a substrate, such as a silicon wafer [170]. This process occurs when high-energy particles bombard the target, causing atoms to be ejected and subsequently settle onto the substrate surface.

The process is initiated by the impact of positively charged ions, most commonly Ar^+ gas, chosen for its affordability, chemical stability, and high sputtering efficiency in material deposition [46].

Advantages of Sputtering for HfO_2 Deposition

The key advantages of using sputtering for depositing ferroelectric HfO_2 are summarized below [146]:

1. **Rapid Deposition Rate:**
   - Sputtering takes place under low-pressure conditions, allowing for a faster deposition process in comparison to other thin-film deposition techniques such as atomic layer deposition (ALD).
2. **Reduced Impurity Incorporation:**
   - Unlike other deposition methods, sputtering exhibits minimal interaction with contaminants such as carbon (C), nitrogen (N), or hydrogen (H).
   - This is particularly important for ferroelectric HfO_2, as impurities can disrupt phase stability and impair ferroelectric performance.
3. **Room Temperature Deposition and Flexibility:**
   - The sputtering process enables thin-film growth at room temperature, making it well-suited for flexible substrates with low thermal resistance.
   - This capability is valuable for wearable electronics, flexible memory devices, and advanced low-temperature processing applications.

Challenges of Sputtering for HfO_2 Deposition

Despite its benefits, sputtering also presents several challenges for depositing high-quality HfO_2 films [146]:

1. **Potential Film Damage from High-Energy Ions:**
   - The high-energy ion bombardment in sputtering can cause structural damage to the deposited film or the underlying layers, negatively affecting device performance.
2. **Limitations in 3D Deposition:**
   - Unlike ALD, which provides excellent conformal coverage on high-aspect-ratio structures, sputtering struggles to achieve uniform film deposition on complex 3D geometries.
   - As a result, it is less suitable for advanced memory architectures, including 3D FeFETs and high-density vertical structures.
3. **Process Complexity and Optimization Challenges:**
   - Several parameters impact sputtering efficiency, such as gas composition, chamber pressure, power settings, and substrate alignment.
   - The difficulty in precisely controlling these variables makes it challenging to optimize sputtering for different applications.

2.7.3 Pulsed Laser Deposition

Pulsed Laser Deposition (PLD) is a physical vapor deposition (PVD) technique that employs a high-energy laser to irradiate a target material within a vacuum chamber, generating a plasma plume that transfers the material onto a substrate [161].

The laser wavelengths used in PLD range from the mid-infrared, such as the CO_2 laser (10.6 µm), to the near-infrared and visible spectrum, including the Nd:YAG laser (1064 nm, 532 nm), and extend into the ultraviolet region, where excimer lasers are commonly utilized with wavelengths of 308 nm (XeCl), 248 nm (KrF), 193 nm (ArF), and 157 nm (F_2) [161].

PLD is capable of producing epitaxial thin films, which are recognized for their well-ordered atomic arrangement and are ideal for investigating the ferroelectric properties of HfO_2. Their growth is achieved by using substrates with compatible lattice constants, such as yttria-stabilized zirconia (YSZ) and lanthanum strontium manganese oxide (LSMO), while ensuring precise temperature control between 600–1000 °C and maintaining optimal oxygen pressure to achieve high-quality thin-film deposition [146].

Epitaxial HfO_2 films demonstrate excellent endurance, capable of withstanding electric fields up to 5 MV/cm, while their coercive field (E_c) falls within the range of 3–4 MV/cm, signifying their polarization switching capability. These characteristics make PLD-grown HfO_2 films highly robust and well-suited for ferroelectric memory applications, including FeFETs [146].

2.7.4 Comparison of HfO Deposition Techniques for FeFET Applications

Table 2.4: Comparison of Deposition Techniques for HfO_2 Thin Films

Deposition Technique	**Process Type**	**Key Features**	**Advantages**	**Challenges**	**Best Use Cases**
Atomic Layer Deposition (ALD)	Chemical Vapor Deposition (CVD) variant	Layer-by-layer growth, high precision, uniform deposition	Excellent thickness and uniformity control; Ideal for high-aspect-ratio 3D structures; Minimal impurities, high film density	Slow deposition rate; Requires high-temperature processing	High-performance FeFETs; CMOS-compatible ferroelectric devices; 3D memory architectures
Sputtering (PVD)	Physical Ejection of Target Atoms	Ion bombardment causes material deposition on the substrate	Fast deposition rate; Scalable for industrial applications; Low contamination risk	Non-uniform deposition on high-aspect-ratio surfaces; High-energy ions may cause film damage; Challenging optimization due to multiple variables	Large-area thin film applications; Low-cost manufacturing; Simple FeFET structures
Pulsed Laser Deposition (PLD)	Physical Vapor Deposition (Laser Ablation)	High-energy laser ablates target material, forming plasma plume for film growth	Can produce high-quality epitaxial films; Suitable for material research; Good control over film stoichiometry	Poor scalability for large-scale manufacturing; Requires precise temperature and pressure control; Film consistency issues	Fundamental material studies; Epitaxial FeFET films; High-endurance memory applications

2.8 Gate Electrode for FeFET Applications

2.8.1 Material Selection for Gate Layer

The choice of gate material in Ferroelectric Field-Effect Transistors (FeFETs) is critical as it directly influences device stability, endurance, switching behavior, and memory window retention. The gate material must provide good electrical conductivity, compatibility with high-k ferroelectric layers like HfO_2, and stability under high-temperature processing conditions.

Two of the most commonly studied gate materials for FeFETs are **Polysilicon (Poly-Si)** and **Titanium Nitride (TiN)**. Each has distinct advantages and challenges, influencing its suitability for specific FeFET applications.

2.8.2 Polysilicon as a Gate Material for FeFETs

Polysilicon (Poly-Si) has historically been used as a gate material due to its compatibility with CMOS processes, work function tunability, and ability to support self-aligned gate technology. Its extensive integration in traditional semiconductor manufacturing has made it a familiar choice for many device architectures, including FeFETs.

Table 2.5: Advantages and Challenges of Polysilicon in FeFETs [154]

Aspect	**Advantages**	**Challenges**
Thermal Stability	High melting point (1414°C) allows it to withstand high-temperature FeFET fabrication processes.	Poly Depletion Effect increases effective oxide thickness, reducing capacitance and degrading switching behavior.
Gate Process Alignment	Supports Self-Aligned Gate Process, ensuring proper alignment with source/drain regions, reducing variability, and improving switching speed.	Charge Trapping and Threshold Voltage Variability leads to memory window shrinkage over multiple read/write cycles.
Work Function Modulation	Doping-based work function tunability allows tuning of threshold voltage (V_t) by adjusting n-type or p-type doping levels.	Poor compatibility with High-k Dielectrics—Polysilicon reacts with HfO_2 and other high-k materials, forming unwanted silicides that degrade device performance.
CMOS Compatibility	Fully compatible with standard CMOS fabrication processes, making it scalable and reliable.	Higher V_t in advanced nodes—In smaller technology nodes (<45nm), polysilicon leads to high threshold voltage, making it unsuitable for ultra-low-power applications.

Deposition Techniques of Polysilicon for FeFET Gate

The deposition technique used for poly-Si affects its grain size, resistivity, stress levels, and compatibility with FeFET processing. The most common techniques along with their advantages and challenges with respect to Fe-FET are reported in the below table :

Various deposition techniques for Fe-FET are reported below [164, 41] :

Deposition Technique	**Description**	**Relevance to FeFETs**
Low-Pressure Chemical Vapor Deposition (LPCVD)	Uses SiH (Silane) at 500–650°C to grow polysilicon.	Preferred for FeFETs due to high-quality films, uniform thickness, and good dopant activation.
Plasma-Enhanced CVD (PECVD)	Uses RF plasma to deposit Si at lower temperatures (300–400°C).	Enables low-temperature FeFET fabrication, but produces amorphous Si requiring post-deposition crystallization.
Epitaxial Polysilicon Growth (Epi-Poly)	Deposited in an epitaxial reactor, allowing high growth rates (1 µm/min).	Useful for thick gate stacks, but less common in FeFETs.
Solid-Phase Crystallization (SPC)	Deposits amorphous silicon (a-Si) first, then anneals it at 600–1100°C to form poly-Si.	Used to control grain structure in FeFETs while minimizing stress effects.
Sputtering	A non-chemical method where high-energy Ar ions eject Si atoms from a target, forming a thin film on the substrate.	Enables room-temperature polysilicon deposition, preventing ferroelectric degradation in FeFETs. Allows in-situ doping, reducing fabrication complexity. Requires post-deposition annealing (laser or thermal) for grain structure optimization.

Table 2.6: Deposition techniques for FeFET fabrication

The deposition method chosen for polysilicon gate formation in FeFETs plays a crucial role in determining the overall device performance, scalability, and compatibility with CMOS technology. Low-Pressure Chemical Vapor Deposition (LPCVD) remains the preferred technique due to its capability to produce high-purity, uniform polysilicon films with precise doping control and excellent step coverage, making it highly suitable for FeFET applications.

For low-temperature FeFET manufacturing, sputtering presents itself as a strong alternative, particularly in applications where minimizing thermal impact on the ferroelectric layer is essential. However, sputtered polysilicon requires post-deposition annealing, such as thermal or excimer laser annealing, to improve crystallinity and electrical characteristics. Similarly, Plasma-Enhanced Chemical Vapor Deposition (PECVD) allows for polysilicon deposition at reduced temperatures but necessitates an additional crystallization step since the as-deposited silicon remains amorphous.

Epitaxial polysilicon (Epi-Poly) growth offers superior crystalline quality and electrical performance, but its high-temperature process (>900°C) can degrade ferroelectric layers, making it less ideal for FeFET integration. Alternatively, Solid-Phase Crystallization (SPC) provides effective stress control during polysilicon formation, though it introduces additional annealing steps, increasing process complexity.

LPCVD continues to be the most widely adopted approach for FeFET polysilicon gate deposition due to its well-established process maturity and superior film quality. However, sputtering combined with optimized annealing techniques holds great potential, especially for low-temperature FeFET fabrication in emerging memory technologies. Moving forward, refining deposition techniques to balance film quality, processing temperature, and scalability will be essential for improving FeFET performance and advancing its commercial feasibility.

2.8.3 Titanium Nitride (TiN) as a Gate Material for Fe-FETs

Titanium Nitride (TiN) is a widely used metal gate material in FeFETs due to its low resistivity, high thermal stability, and excellent compatibility with high-k ferroelectric materials [37] . Compared to polysilicon, TiN eliminates the poly depletion effect, reduces charge trapping, and enhances device reliability.

Deposition Techniques for Titanium nitride Gate in FeFETs

Three of the mostly studied deposition techniques for Titanium nitride are ALD, CVD,PVD [7]. The table below presents a comparison of ALD, CVD, and PVD deposition techniques for TiN gate materials in FeFETs [37, 185].

Deposition Method	**Key Characteristics**
ALD (TiN)	- Better nitrogen retention - Higher oxygen suppression - Stable work function - Enhances FeFET endurance - Reduces charge trapping - Better interface quality - Reduces Vt variation - Prevents boron diffusion - Maintains FeFET performance over extended cycles
PVD TiN (Ti-rich)	- More prone to oxygen diffusion - Higher Ti penetration into HfO - Leads to higher dielectric degradation - Causes FeFET reliability issues
CVD TiN	- Faster deposition speed - High impurity content - Increased charge trapping - Poor boron blocking capability

Table 2.7: Comparison of ALD, CVD, and PVD TiN as Gate Materials for FeFETs

ALD TiN is the most suitable choice for FeFET applications due to its superior material properties, enhanced device performance, and long-term reliability. It offers better nitrogen retention, higher oxygen suppression, and a stable work function, ensuring the integrity of the gate stack. Compared to PVD TiN, ALD TiN effectively prevents oxygen diffusion and Ti penetration into HfO, thereby reducing dielectric degradation and improving FeFET reliability. Additionally, it minimizes charge trapping, reduces Vt variation, and enhances endurance, which is crucial for maintaining FeFET performance over extended cycles. Unlike CVD TiN, which has high impurity content and poor boron blocking capability, ALD TiN prevents boron diffusion, ensuring stable threshold voltage characteristics. With its better interface quality, lower trap density, and scalability, ALD TiN is the ideal choice for FeFET memory and logic applications.

2.8.4 Performance Comparison of Poly-Silicon Gate and Titanium Nitride Gate for Fe-FET

Titanium Nitride (TiN) outperforms Polysilicon as a gate material in FeFETs due to its superior endurance, higher memory window stability, and better retention characteristics. While Polysilicon offers lower switching voltage and compatibility with traditional CMOS fabrication, it suffers from poly depletion effects, higher charge trapping, and reduced endurance over multiple switching cycles.

Key Comparison Metrics: [113, 72, 103]

- **Memory Window (MW):** TiN supports a wider MW (1–3V), ensuring more reliable multi-level storage, whereas Polysilicon has a smaller MW (1.5–2.5V), limiting storage scalability.
- **Switching Voltage:** TiN requires a higher switching voltage, which improves charge stability and reduces variability. Polysilicon, while offering lower switching voltages, suffers from degradation over time.
- **Endurance:** TiN-based FeFETs demonstrate better endurance (10^5–10^7 cycles) compared to Polysilicon, which degrades faster due to charge trapping and poly depletion effects.
- **Retention:** TiN retains stored data longer, making it ideal for long-term non-volatile memory applications. Polysilicon experiences faster memory window shrinkage due to interface defects.
- **On/Off Ratio:** Both materials provide an On/Off ratio $> 10^3$–10^4, ensuring distinct readout states.

Application-Specific Suitability:

- **Polysilicon FeFETs:** Suitable for low-power embedded applications and logic circuits, where lower switching voltages and CMOS compatibility are prioritized.
- **Titanium Nitride FeFETs:** Preferred for high-endurance, high-retention non-volatile memory (NVM) applications, such as FeRAM, 3D NAND, and neuromorphic computing, where robust switching and longer data retention are essential.

Conclusion: *Titanium Nitride is the superior gate material for FeFETs, offering enhanced memory performance, endurance, and long-term reliability, making it the preferred choice for next-generation high-density FeFET storage solutions.*

2.9 S/D implantation

S/D implantation is a doping technique used to introduce carriers (electrons or holes) into the source and drain regions. It typically involves:

- **Ion Species:** Phosphorus (P), Arsenic (As) for n-type FeFETs, and Boron (B) for p-type FeFETs.
- **Energy Levels:** Low-energy implantation to prevent deep diffusion into the ferroelectric layer.
- **Doping Concentration:** Adjusted to balance conductivity and leakage.

Ferroelectric Field-Effect Transistors (FeFETs) are promising for non-volatile memory (NVM), neuromorphic computing, and low-power logic applications. However, as FeFETs scale down, Source/Drain (S/D) implantation plays a crucial role in their performance, affecting threshold voltage stability, leakage currents, and device performance [74, 33].

Table 2.8: Common Dopants and Characteristics

FeFET Type	**Dopant Type**	**Dopant Materials**	**Reason for Choice** [8]
n-type Fe-FET	Donor (n^+)	Phosphorus (P), Arsenic (As)	Phosphorus and arsenic are favoured for their electrical properties, silicon compatibility, and high solubility limits, which prevent crystal defects.
p-type Fe-FET	Acceptor (p^+)	Boron	For Silicon substrate Boron is an ideal choice due to its solubility which enhances conductivity.

2.9.1 S/D Implantation Techniques for FeFET

Below, we report various Source/Drain (S/D) implantation techniques used in the fabrication of Ferroelectric Field-Effect Transistors (FeFETs). These techniques play a critical role in determining the electrical characteristics, scalability, and reliability of the devices. Each method offers specific advantages and limitations depending on process compatibility, dopant activation efficiency, junction abruptness, and thermal budget. The comparative analysis of these techniques is summarized in the table that follows.

Table 2.9: Advantages and Challenges of Implantation Techniques for FeFETs

Technique	**Advantages**	**Challenges**
Ion Implantation [127, 29]	• Improved threshold voltage control, switching speed, and device yield • High-volume manufacturing compatible • Allows selective doping • Replaces diffusion-based doping	• Low throughput at ultra-low energies • Limits scalability due to poor control over ultra-shallow junction formation • Alters device structure and affects ultra-shallow junction stability • Makes doping of 3D structures (e.g., FinFET, trenches) difficult, causing performance variations.
Plasma Doping (PLAD) [127]	• Low cost and simplicity • High dose rate • No line-of-sight limitations • Minimal charging issues • Compact footprint	• Complex process dynamics • Incompatibility with standard diagnostics • Lack of TCAD simulation models
Spin-on Dopant (SOD) Diffusion [12]	• Low-cost and simple process • Uniform doping profiles • Selective doping capability • Scalable for integration	• Oxygen contamination and oxide formation • Requires optimization for carrier activation • Limited penetration depth

Ferroelectric Field-Effect Transistors (Fe-FETs) require highly controlled doping to ensure threshold voltage stability, switching performance, and leakage reduction, while also preserving the integrity of the ferroelectric layer. Among the three doping techniques—Ion Implantation, Plasma Doping (PLAD), and Spin-on Dopant (SOD) Diffusion—ion implantation is less suitable for Fe-FETs due to potential damage to the ferroelectric material and challenges in achieving ultra-shallow junctions.

PLAD is the most effective choice for Fe-FETs, particularly in advanced 3D architectures, due to its ability to provide uniform, low-energy doping without structural damage. Meanwhile, SOD diffusion is well-suited for planar Fe-FETs, offering a cost-effective and selective doping solution, though it may not be ideal for 3D designs.

Although PLAD and SOD diffusion are better suited for Fe-FET applications, ion implantation remains the leading doping method in the semiconductor industry, valued for its precision, scalability, and seamless integration into fabrication processes. It allows for controlled substrate doping concentration adjustments, as evidenced in Fe-FET fabrication, where it enables threshold voltage (V_{th}) tuning while ensuring low gate leakage current and stable data retention [84]. Its role in CMOS scaling has been instrumental in junction depth control, subthreshold swing optimization, and non-volatile memory applications.

Although challenges such as ultra-shallow junction formation limitations and potential ferroelectric material damage exist, ion implantation remains a cornerstone of semiconductor technology due to its process reliability, selective doping capability, and high-volume manufacturing efficiency. However, with the evolution of Fe-FET technology, alternative methods like PLAD and SOD are emerging as more compatible solutions for Fe-FET-specific fabrication needs.

2.10 Contact Formation in Fe-FETs

2.10.1 Common Contact Materials

Table 2.10: Comparison of Contact Materials for FeFET Integration

Material	**Type**	**Advantages**	**Challenges**
Titanium Nitride (TiN) [36]	Metal	• High thermal stability • Low resistivity • CMOS compatible • Corrosion resistant • Good mechanical strength • Minimal diffusion	• Variability in Film Thickness & Phase Uniformity • Texture/crystal variability • Adhesion issues (PVD)
Titanium Silicide (TiSi) [38]	Silicide	• Good electrical performance • Low silicon consumption	• High resistance in p-type contacts
Cobalt Silicide (CoSi, $CoSi_2$) [38]	Silicide	• 40% lower p-contact resistance • Suitable for high-performance applications	• High leakage with Co+Ti cap • Needs precise RTA
Nickel Silicide (NiSi) [38]	Silicide	• Lowest leakage current due to low silicon consumption • Good for memory nodes	• Higher p-type resistance • Poor thermal stability
Tungsten (W) [100]	Metal	• Thermal stability • Electromigration resistance • Excellent gap fill	• Higher resistivity ($5.6 \times 10^{-8}\,\Omega\cdot$m)

TiN is the best overall choice for FeFET contacts due to its low resistivity, compatibility with CMOS fabrication, and excellent stability. Despite PVD-related challenges, these can be mitigated using advanced deposition techniques like Atomic Layer Deposition (ALD) or optimized CVD TiN.

Nickel Silicide (NiSi) is a good alternative if leakage current minimization is the top priority, but its higher resistance can limit overall FeFET performance. However, NiSi is currently preferred due to its low contact resistivity [17].

Cobalt Silicide (CoSi) is useful for reducing contact resistance, but higher leakage makes it less suitable for FeFETs.

Titanium Silicide (TiSi) is not ideal for FeFETs due to its higher p-type resistance, which can affect threshold voltage control.

Tungsten is ideal for deep-trench FeFET contacts, but its high resistivity makes it less desirable for standard planar FeFETs.

2.10.2 Contact Formation Techniques

Table 2.11: Comparison of Deposition Techniques for FeFET Contacts

Technique	**Advantages**	**Materials Deposited**	**Challenges**
Sputtering (PVD) [36, 77]	• Cost effective • High corrosion resistance • Enhances conductivity	TiN	• Variability in film thickness and phase uniformity • Crystal structure and texture variability • Adhesion problems
Chemical Vapor Deposition (CVD) [80]	• Superior step coverage and gap fill • Electromigration resistance • Good thermal expansion compatibility	Tungsten	• Selectivity control (preventing unwanted deposition on dielectric surfaces). • High contact resistance • Encroachment issues, where tungsten spreads beyond the intended area. • Slow growth rate • Device leakage, caused by uncontrolled tungsten deposition
Silicidation [87]	• Low resistivity • High-temperature stability • Forms ohmic contact with silicon	NiSi, $CoSi_2$	• Vertical penetration of silicide into junctions • Lateral penetration of silicide across the junction • Silicide phase transformation leading to unwanted resistivity changes • Silicide removal, causing discontinuities in electrical pathways

PVD TiN is a viable contact material for FeFETs; however, process optimization, including enhanced adhesion layers and precise thickness control, is necessary to minimize variability issues. CVD tungsten is well-suited for 3D FeFETs, but the integration of a TiN barrier layer is essential to reduce contact resistance, along with careful process management to prevent leakage. NiSi and CoSi are effective for planar FeFETs, though stringent process control is required to prevent silicide diffusion into the ferroelectric layer.

2.11 Conclusion

Ferroelectric Field-Effect Transistors (FeFETs) represent a pivotal advancement in non-volatile memory technology, leveraging the unique properties of hafnium oxide (HfO) to achieve scalable, low-power, and high-endurance memory solutions. The discovery of ferroelectricity in ultra-thin HfO films has enabled CMOS-compatible integration, overcoming limitations posed by traditional perovskite-based materials. The success of FeFET technology hinges on meticulous fabrication, including optimal substrate choice, interfacial layer engineering, precise doping techniques, and gate/contact material selection. Among various materials, silicon oxynitride (SiON) offers superior interfacial performance, while atomic layer deposition (ALD) and sputtering have emerged as key deposition methods for ensuring high-quality ferroelectric films. Titanium nitride (TiN) outperforms polysilicon as a gate and contact material due to its superior endurance, retention, and memory window stability. Furthermore, SOI architectures enhance electrostatic control and reliability compared to bulk counterparts. With continuous improvements in material science and processing techniques, FeFETs are poised to become a cornerstone technology for next-generation memory, neuromorphic systems, and energy-efficient computing applications.

Chapter 3

Resistive Switching Memories

3.1 Introduction

Non-Volatile Memories (NVMs) are the backbone of the electronics industry as they retain data even when power is turned off. This field has been extensively explored to develop highly scalable and efficient NVM solutions. Traditional Dynamic Random-Access Memory (DRAM) and silicon-based Flash memory technologies face limitations such as low speed, poor endurance, the need for additional circuitry, and, most importantly, limited scalability [117].

Several next-generation NVM technologies have been investigated to overcome these limitations, among which two major advancements include:

- **Magnetoresistive RAM (MRAM)** [181]: Utilizes magnetic tunnel junctions to store data.
- **Ferroelectric RAM (FRAM)** [179]: Utilizes reversible polarization to store information.

Despite their advantages, both technologies encounter significant challenges related to scaling. In this literature review, we focus on another promising candidate for NVM applications: **Resistive Switching RAM (RRAM)**.

Resistive RAM (ReRAM) is a type of NVM that stores data by switching between different resistance states within the memory element. ReRAM operates on the principle that the resistance of certain materials changes under the application of an electric field [117]. Various material systems, including binary oxides, solid electrolytes, perovskites, and organic compounds, exhibit this behavior.

RRAM devices possess a simple architecture, typically realized with a Metal–Insulator–Metal (MIM) structure [88]. The memory cell of RRAM can be scaled down to as small as $4F^2$, where F is the feature size of the technology node used in fabrication [117].

In conclusion, due to its simple structure and ultra-small size, RRAM stands out as a strong contender in the NVM landscape. In the following sections, we will delve deeper into its fabrication techniques, switching mechanism, and performance metrics.

3.2 Classification of Resistive Switching Memories

RERAM can be classified into two ways based on the switching behaviour and switching mechanism.

1. Classification Based on Switching Behavior

Resistive switching exhibits two states: Low Resistance State (LRS) and High Resistance State (HRS) under the application of electrical stimuli [117, 24, 150, 169]. When the resistance changes

from HRS to LRS, it is called the **SET** process. Conversely, a change from LRS to HRS is known as the **RESET** process. These states persist even after the electrical stimuli is removed, demonstrating the non-volatility of ReRAM.

Based on the relationship between the SET and RESET processes, resistive switching behavior can be classified into two categories:

- **Unipolar Switching:** The change from HRS to LRS does not depend on the polarity of the applied voltage. Devices exhibiting unipolar behavior typically have a *symmetrical structure*, meaning the top and bottom electrodes are made of the same material.
- **Bipolar Switching:** The SET and RESET processes depend on the polarity of the applied voltage. Devices with bipolar behavior generally have an *asymmetrical structure*, where the top and bottom electrodes are made of different materials.

2. Classification Based on Switching Mechanism

Based on the switching mechanism, ReRAM can be categorized into:

- **Filament-Type Switching:** In these devices, conduction in the LRS is confined to a filament formed in the insulating matrix of the MIM structure. During HRS, the current flows uniformly throughout the device.
  - The resistance in LRS is independent of device size, as it depends on filament formation.
  - In HRS, resistance increases as device size decreases, since the current distribution is more uniform.
  - The effective device size is determined by the filament size, and studies indicate that the device must be approximately twice the filament size for proper operation [117, 24, 150, 169].
  - Recent research has shown that filament size can be scaled to the nanoscale, making filament-type switching ideal for highly-scaled NVM applications.
- **Interface-Type Switching:** This mechanism is based on variations in the barrier height between the electrode and the dielectric material.
  - When the barrier height is reduced, LRS is achieved.
  - When the barrier height is increased, HRS is achieved.
  - Interface-type devices typically operate at lower currents, making them more efficient for NVM applications.

3.3 Structure of RERAM

ReRAM has the simplest structure. It consists of a top electrode made of metal and a bottom electrode made of metal separated by an insulator [88]. This type of structure is referred to as the MIM structure. Due to its simplest structure ReRAM has gain attention for crossbar memory structures.

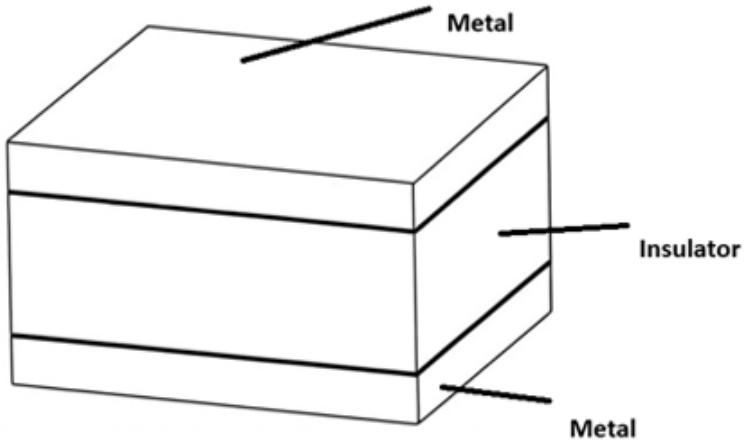

Figure 3.1: Structure of ReRAM

3.4 Fabrication Steps

Resistive Random Access Memory (ReRAM) devices are typically built using a straightforward Metal-Insulator-Metal (MIM) structure, in which the core component is the resistive switching layer. This layer is responsible for the memory effect by changing its resistance states under an applied voltage. The fabrication process of ReRAM is relatively simple compared to other emerging memory technologies and is largely compatible with existing semiconductor manufacturing methods. As a result, ReRAM can be conveniently integrated with standard CMOS processes, making it a strong candidate for high-density, low-power, and scalable non-volatile memory applications. The following section outlines the key fabrication steps involved in the development of a ReRAM cell.

3.4.1 Substrate Selection

A P type silicon wafer is taken as the initial substrate and a layer of SiO2 is grown using thermal oxidation [165]. SiO acts as an insulating layer, preventing leakage current between memory cells.

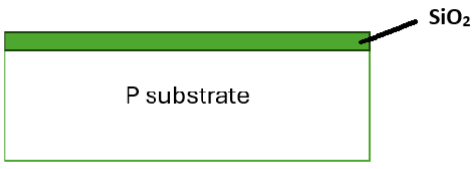

Figure 3.2: Substrate Selection

3.4.2 Bottom Electrode formation

An adhesive layer of Ti 20nm (Titanium (Ti) acts as a scavenging layer in HfO-based RRAM devices, positioned between the HfO switching layer and the top electrode (typically TiN). During or after deposition, Ti undergoes oxidation by reacting with oxygen from the HfO layer, forming a TiO interfacial layer. This process promotes the formation of oxygen vacancies in the HfO, which are essential for filament-based resistive switching [19] is deposited to form the base of the bottom electrode by electron beam evaporation technique followed by the deposition of the bottom electrode of Pt(50nm) by electron beam evaporation technique [78].

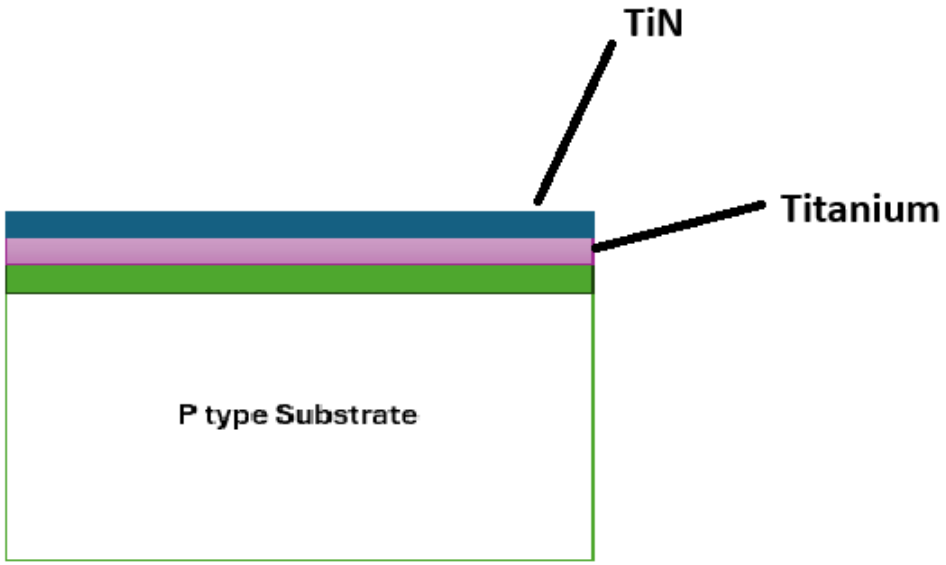

Figure 3.3: Bottom Electrode deposition

3.4.3 Deposition of the switching layer

A 50 nm Hafnium Dioxide (HfO_2) film was deposited using RF magnetic sputtering at 600 °C, followed by a post-annealing process at 650 °C to activate the resistive property of the switching layer [116].

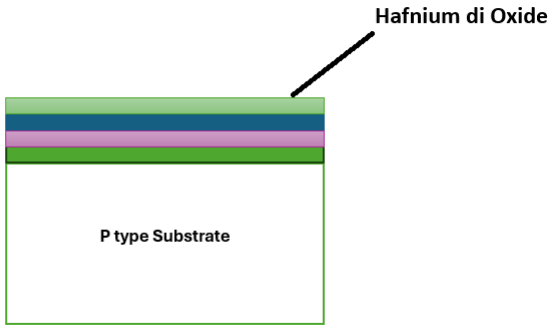

Figure 3.4: Deposition of the hafnium layer

3.4.4 Deposition of the Top Electrode

An adhesive layer of Ti (20nm) is deposited by electron beam evaporation technique followed by the deposition of the top electrode of Cu (150 nm) by DC magnetron sputtering Technique [78].

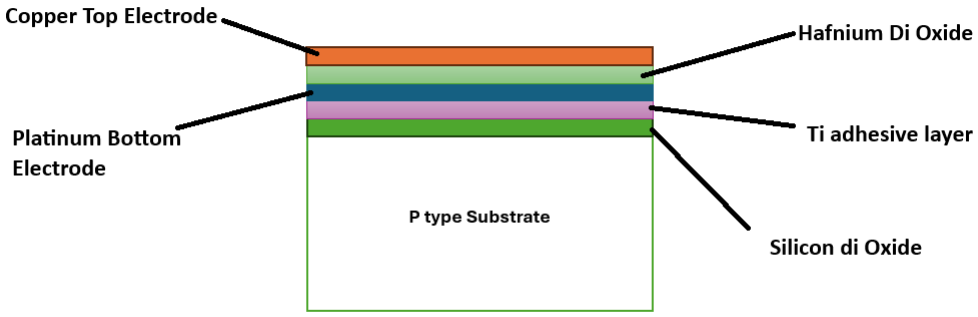

Figure 3.5: Deposition of the hafnium layer

3.5 Electrode Material Evaluation for ReRAM Devices

Electrode materials in Resistive Random Access Memory (ReRAM) significantly influence the device's switching characteristics, including SET/RESET voltages, resistive state stability, endurance, and retention [30, 110]. These parameters are critical for tailoring ReRAM devices for specific applications such as non-volatile memory storage or hardware-based security primitives. This section presents an evaluation of commonly used top and bottom electrode combinations in ReRAM devices employing Hafnium Dioxide (HfO_2) as the switching layer.

3.5.1 Common Electrode Materials

In a typical ReRAM (Resistive Random Access Memory) structure, the top electrode (TE) and bottom electrode (BE) serve as essential electrical terminals that facilitate key switching mechanisms such as charge injection, ion migration, and redox reactions within the active layer [22, 35]. The physical and chemical properties of these electrodes—particularly their work function, reactivity, diffusivity, and thermal stability—are critical in determining the formation, stability, and rupture of conductive filaments in the resistive switching material.

Experimental studies have shown that device performance and switching reliability are significantly enhanced when the work function difference between the TE and BE is greater than or equal to 0.70 eV, which ensures improved control over the electrochemical processes and stability under various operating conditions [30]. For instance, using Ag (Silver) as the top electrode results in a high ON/OFF resistance ratio of approximately 2000, while replacing Ag with Au (Gold) reduces the ON/OFF ratio to about 900, indicating a decline in switching contrast and device efficiency [137]. These observations highlight the critical role of electrode selection in optimizing ReRAM performance for memory and neuromorphic applications.

- **Titanium Nitride (TiN)**: A chemically stable, CMOS-compatible electrode material that can function as either TE or BE. It offers excellent thermal stability and is commonly used in high-endurance devices [182].

- **Titanium (Ti)**: Ti is a reactive transition metal known to enhance filament formation, contributing to better switching contrast but typically requiring higher operating voltages [20].

- **Gold (Au)**: Au is a noble metal with high conductivity and chemical inertness, suitable for low-power operation and frequently used in devices where variability and entropy are desired [196].

- **Platinum (Pt)**: Pt is a robust and inert electrode widely used as a bottom electrode due to its high endurance and compatibility with various oxides [196].

- **Indium Tin Oxide (ITO)**: ITO is a transparent conducting oxide occasionally used in ReRAM devices, particularly in applications requiring transparency or flexibility. ITO-based ReRAM devices can exhibit reliable and reproducible bipolar resistive switching behaviour [63].

- **p^+ Silicon**: p^+ Si is compatible with standard CMOS processing techniques, making it a viable option for integration into semiconductor devices. Research indicates that devices utilizing p^+-Si as an electrode material can demonstrate reliable resistive switching characteristics, although specific endurance metrics can vary based on device architecture and fabrication processes [73].

- **Copper (Cu) and Aluminium (Al)**: Both Cu and Al are known for their high electrical conductivity and cost-effectiveness, making them attractive choices for electrode materials in various electronic applications [178, 177].

Each material presents trade-offs between performance, scalability, and integration potential. The following table and analysis highlight how specific TE/BE combinations influence key switching metrics.

3.5.2 Performance Data of ReRAM Devices with Various Electrodes

Based on various experimental studies reported in recent literature, the performance of ReRAM devices is shown to be highly dependent on the choice of top and bottom electrodes. Electrode materials influence key device parameters such as High Resistance State (HRS)/Low Resistance State (LRS) resistance ratio, data retention, endurance (switching cycles), and operating voltages (forming, set, and reset). Research findings highlight that materials like Ti, TiN, Cu, Al, and Au, when paired with different bottom electrodes (e.g., Pt, ITO, p^+Si), demonstrate a wide range of electrical characteristics suitable for different memory applications. The table below summarizes the performance metrics of selected ReRAM configurations, providing insights into their optimal use-cases.

Table 3.1: Performance Metrics of ReRAM Devices with Various Electrode Combinations

Top Electrode	Bottom Electrode	HRS/LRS	Retention (s)	Endurance	Vf	V_{set}	V_{reset}	I_{cc}	Ref.
Cu	p+ Si	10^4	10^4	NS	3V	-0.5—1V	NS	NS	[1]
Al	FTO	$>10^3$	NS	NS	FF	0.5V	-0.5V	NS	[116]
TiN	Pt	10^6	10^4	NS	FF	-4.3V	6V	NS	[197]
Ti	TiN	10^5	10^4	$>10^7$	NS	3V	-3.5V	1mA	[147]
Au	Pt	15	500	200	FF	0.2V	-0.5V	NS	[99]
Au	ITO	10^2	100	10^4	3V	3V	-2.1V	NS	[189]
Ti	Au	5127	NS	NS	FF	2.0V	-2.0V	NS	[143]
Ti	Pt	906	NS	NS	FF	5.4V	-2.6V	NS	[143]
Au	p+ Si	900	NS	NS	NS	2.04V	-4—5V	NS	[137]
Al	Al	10^4	NS	NS	1V	1.8V	0.8V	1µA–1mA	[26]

3.5.3 Best Applications of ReRAM Devices Based on Electrode Configuration

Resistive Random-Access Memory (ReRAM) has emerged as a promising non-volatile memory technology due to its simple structure, low power consumption, and high scalability. Electrode material selection significantly influences ReRAM performance metrics such as the HRS/LRS ratio, retention, endurance, and operating voltages. Based on the data presented, we can classify optimal applications for various electrode configurations:

1. High-Endurance and Retention Applications: Ti/TiN Configuration

- Ti/TiN-based ReRAM [147] exhibits outstanding retention and endurance, making it highly suitable for mission-critical storage, space electronics, and defence applications.
- Operates at moderate voltages ($V_f = 3$V, $V_{reset} = -3.5$V) and controlled current levels (1 mA), enhancing energy efficiency.

2. Ultra-High HRS/LRS Ratio: TiN/Pt Configuration

- The TiN/Pt pair [197] delivers an exceptional HRS/LRS ratio of 10^6, ensuring better read margin and data reliability in high-noise environments.
- Ideal for enterprise-level memory systems and secure memory storage.
- Requires a relatively high V_{set} (6V), suitable for non-power-constrained applications.

3. Transparent and Flexible Electronics: Al/FTO and Au/ITO Configurations

- Al/FTO [116] and Au/ITO [189] structures are compatible with transparent and flexible substrates, ideal for wearable electronics, displays, and biosensors.
- Al/FTO: $V_{set} = 0.5$V, $V_{reset} = -0.5$V – suitable for low-power applications.
- Au/ITO: Endurance = 10^4 cycles, Retention = 10^2 seconds – supports moderate reusability.

4. Cost-Effective and CMOS-Compatible Designs: Cu/p$^+$Si and Au/p$^+$Si

- Cu/p$^+$Si [1] and Au/p$^+$Si [137] are CMOS-compatible and cost-effective, enabling integration with semiconductor processes.
- Cu/p$^+$Si: HRS/LRS = 10^4, $V_{reset} = -0.5$V to -1V – ideal for consumer and IoT applications.
- Au/p$^+$Si offers similar characteristics with further optimization needed.

5. Low Voltage and Low Power Memory: Au/Pt and Al/Al

- Au/Pt [99]: $V_f = 0.2$V, $V_{reset} = -0.5$V – excellent for battery-operated and medical devices.
- Al/Al [26]: HRS/LRS = 10^4, operating current = 1μA–1mA – suitable for ultra-low-power applications.

6. High-Speed and Neuromorphic Computing: Ti/Au and Ti/Pt

- Ti/Au and Ti/Pt [143]: HRS/LRS ratios of 5127 and 906 respectively, with symmetric voltages ($\pm$2V to $\pm$5V).
- Suitable for analog switching and synaptic devices in neuromorphic systems.

3.6 Switching Material Selection for ReRAM Devices

The choice of the switching material determines the overall performance of the device. The basic principle of resistive switching is based on the formation and rupture of the filament created by oxygen vacancies. Several materials, particularly oxides, exhibit switching behavior; among these, transition metal oxides are the most commonly used. In addition to oxides, nitrides and chalcogenides also show resistive switching behavior, although they are less commonly employed.

Among these materials, the most commonly used is hafnium dioxide (HfO_2) [78], due to its existing compatibility with modern fabrication processes. Its high dielectric constant (high-k value), along with its ability to form stable oxygen vacancies, makes HfO_2 a superior contender for the switching layer. Moreover, deposition techniques such as Atomic Layer Deposition (ALD) and Chemical Vapor Deposition (CVD) allow precise control over the thickness and quality of HfO_2, enabling various optimization strategies to enhance device performance.

3.6.1 Deposition of Hafnium Dioxide for ReRAM application

Resistive Random-Access Memory (ReRAM) is an emerging non-volatile memory technology that leverages resistive switching (RS) phenomena in metal-insulator-metal (MIM) structures. Hafnium oxide (HfO_2) has gained significant attention as a switching layer due to its high dielectric constant, excellent thermal stability, and compatibility with CMOS technology. The performance of ReRAM devices heavily depends on the deposition technique used for HfO_2, as it directly influences the film's structure, defect density, and electrical properties.

Various deposition techniques, such as Atomic Layer Deposition (ALD), Sputtering, Chemical Vapor Deposition (CVD), and Pulsed Laser Deposition (PLD), have been employed to fabricate HfO_2-based ReRAM devices. These methods impact key device parameters, including SET/RESET voltage, switching endurance, retention, and resistance ratio (HRS/LRS ratio) [192]. The choice of deposition technique also determines the concentration of oxygen vacancies, which play a critical role in filamentary or interfacial resistive switching mechanisms.

In this article, we compare different HfO_2 deposition techniques for ReRAM applications, discussing their film properties, advantages, limitations, and overall impact on device performance. This information provides insights into optimizing HfO_2 thin-film fabrication to achieve high-performance, reliable, and scalable ReRAM devices.

Table 3.2: Comparison of Deposition Techniques for HfO_2-Based ReRAM Devices

Technique	**Resistive Switching Performance**	**Advantages**	**Disadvantages**
ALD [52]	Low SET/RESET, stable switching, high endurance	Precise control of thickness, minimal defects	The random formation and dissolution of conductive filaments cause inconsistent resistance states, leading to device variability and switching instability in RRAM.
RF Sputtering [134, 111]	Stable switching, high ON/OFF ratio, good retention	High film quality, avoids charge build-up	It is required to control the O/Ar ratio for better performance. Optimal O/Ar ratio is 0.8
Sol-Gel [131]	Reliable switching	Simple, low-cost, scalable, eco-friendly	Requires forming process, possible instability due to oxygen vacancies.
Chemical Beam Vapor Depostion [89, 166]	Lower SET and RESET voltages, a wider resistance window, improved retention, and reduced endurance.	Enables homogeneous film deposition on large-area substrates with high reproducibility, Effective for thin film deposition as in case of ReRAM	High-vacuum conditions must be maintained, adding to system requirements, Still not widely industrialized

Among the various thin-film deposition techniques, **Atomic Layer Deposition (ALD)** is the most preferred due to its precise control, low defect density, and high endurance in ReRAM applications. However, its performance can be affected by the random formation and dissolution of conductive filaments, leading to device variability. **Sputtering (RF sputtering)** offers stable resistive switching and high ON/OFF resistance ratios, but requires careful optimization of the O_2/Ar ratio. **Sol-Gel Deposition** is a cost-effective and environmentally friendly option, though it may introduce oxygen vacancy-related instability. **Chemical Beam Vapor Deposition (CBVD)** provides a wider resistance window and improved retention, but its high-vacuum requirements limit industrial adoption. While each method has its advantages and challenges, ALD remains the most widely used technique for achieving stable and high-performance ReRAM devices.

3.6.2 Thickness of the Hafnium Oxide for ReRAM Devices

The thickness of the hafnium dioxide (HfO_2) switching layer plays a critical role in the resistive switching (RS) behaviour of hafnium oxide-based resistive random-access memory (ReRAM). It directly influences the overall performance of the device. Thinner films may suffer from leakage currents and unstable filament formation due to poor crystallinity or porous structures, leading to unreliable switching behaviour [119]. Conversely, very thick films may prevent forming because the electric field across the film becomes too weak to initiate conductive paths, requiring higher voltages and increasing power consumption [188].

Table 3.3: Optimal Thickness Range for HfO_2-Based ReRAM

HfO_2 Thickness	**Characteristics**	**Best Use Case**
<5 nm	• Low forming voltage • Gradual and weak reset behaviour • Low endurance • Lower set voltage variance (typically around 1V) [75, 192]	• Low-power devices • Neuromorphic computing (where gradual/analog switching is acceptable and low energy matters more than lifespan)
5–10 nm	• Medium forming voltage • Mixed reset behaviour • Moderate endurance • Lower set voltage variance (typically around 1V) [75, 192]	• General-purpose memory • Reliable RRAM prototypes • Best mix of low power and reliability
10–20 nm	• High forming voltage • Abrupt switching behaviour • Higher endurance • Higher set voltage variance (typically around 4V) [75, 192]	• Endurance-critical memory • Data storage with strong ON/OFF contrast • Industrial/automotive-grade memory

3.7 Conclusion

Resistive Random-Access Memory (ReRAM) has emerged as a compelling alternative in the field of non-volatile memories (NVM), offering a promising solution to the limitations faced by conventional technologies like DRAM and Flash. Unlike other emerging NVMs such as MRAM and FRAM, ReRAM distinguishes itself through its simple Metal-Insulator-Metal (MIM) structure and its reliance on changes in material resistance to store data. This makes it highly scalable and energy-efficient, characteristics that are crucial in today's data-driven world.

ReRAM can be categorized based on switching behavior (unipolar or bipolar) and mechanism (filamentary or interfacial), which allows for tailored performance based on specific application requirements. Filament-type devices are particularly promising for aggressive scaling, while interfacial types excel in low-power applications.

From a structural and fabrication standpoint, ReRAM's straightforward architecture makes it easier to integrate with existing CMOS technologies. The fabrication process, including substrate preparation, electrode deposition, and the formation of the resistive switching layer (often HfO_2), is relatively simple yet critically important for performance optimization.

The choice of electrode materials plays a pivotal role in defining ReRAM performance metrics such as switching speed, retention, endurance, and power consumption. Combinations like Ti/TiN, Au/ITO, and Cu/p^+Si serve different application needs—from high-endurance memory for aerospace to transparent electronics for wearable devices.

Equally vital is the selection and deposition method of the switching layer material, particularly hafnium oxide. Techniques such as Atomic Layer Deposition (ALD) and sputtering offer trade-offs in terms of defect control, film uniformity, and process scalability. Among these, ALD is generally preferred for its precision. Additionally, the thickness of the HfO_2 layer directly influences device behavior—thinner layers support low-power, neuromorphic systems, while thicker layers are suited for robust, high-endurance storage.

In summary, ReRAM stands at the crossroads of simplicity and sophistication. Its flexibility in design, adaptability to various application domains, and compatibility with existing manufacturing processes make it not only a strong candidate for next-generation NVM but also a foundational technology for the future of computing.

Chapter 4

Carbon Nanotube-based Non-Volatile Memory

4.1 Introduction

Carbon Nanotube-based Non-Volatile Random Access Memory (CNT-NRAM) is an emerging memory technology that leverages the unique electrical and mechanical properties of carbon nanotubes to achieve high-speed, energy-efficient, and scalable data storage. Unlike conventional memory devices, CNT-NRAM operates through the reversible mechanical movement of nanotubes, enabling bistable resistance states that correspond to binary logic. The fabrication of CNT-NRAM involves a series of precisely controlled steps—including substrate preparation, electrode deposition, CNT synthesis, and layer assembly—each of which significantly influences device performance and reliability. This document outlines the fabrication process, working principles, material choices, and comparative evaluations essential to the development of CNT-NRAM systems.

4.2 Fabrication Steps

4.2.1 Substrate Selection

The fabrication of CNT-based non-volatile memory (NRAM) starts with choosing and preparing a p-type silicon substrate that is fully compatible with standard CMOS processing technologies.

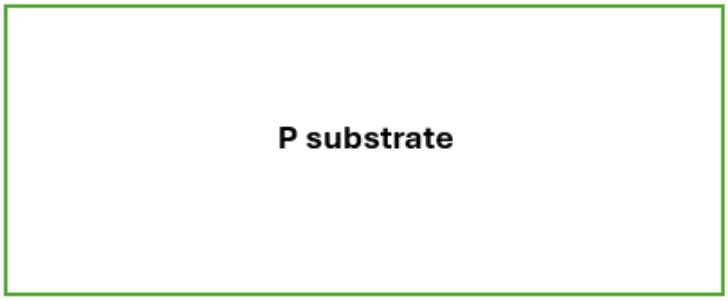

Figure 4.1: Substrate Selection

4.2.2 Deposition of Bottom Electrode

A layer of 30nm Titanium Nitride (TiN) is deposited on a silicon (Si) wafer to serve as the bottom electrode for the NRAM device [149]. Titanium Nitride is chosen because of its excellent electrical conductivity, chemical inertness, thermal stability, and strong adhesion to silicon-based substrates [182].

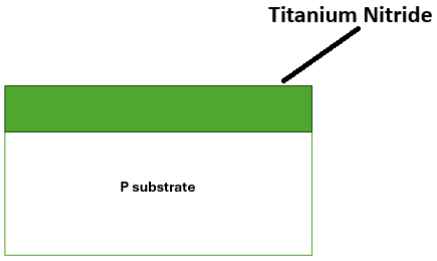

Figure 4.2: Deposition of Titanium Nitride as bottom electrode

4.2.3 Synthesis of the CNT

Carbon nanotubes (CNTs) were synthesized using the arc discharge method [5], a process in which a high-current arc is struck between two graphite electrodes in an inert gas atmosphere such as helium or argon. The intense heat generated by the arc vaporizes the carbon from the anode, allowing it to condense and form nanotubes on a cooler surface. This method is well known for producing CNTs with high crystallinity and excellent structural quality.

4.2.4 Purification of CNTs

CNTs were purified using a liquid phase method involving filtration, acid-solvent treatment to remove impurities, and centrifugation to isolate the cleaned nanotubes [61].

4.2.5 Placement of CNTs on the Wafer [120, 132]

A purified carbon nanotube solution is applied onto a wafer pre-patterned with round electrodes. The wafer is then spin-coated, utilizing centrifugal force to achieve a uniform distribution of nanotubes across the wafer surface and electrodes. During this process, the nanotubes orient randomly. The resulting CNT layer typically has a thickness of approximately 30 nm [47]. Subsequent fabrication steps remove excess nanotubes and form electrical interconnections, with each electrode area covered by nanotubes, thereby creating individual memory cells.

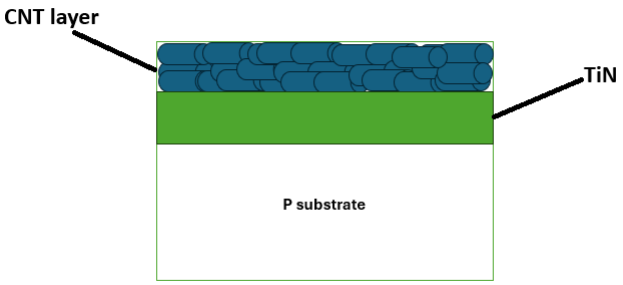

Figure 4.3: Deposition of CNT layer

4.2.6 Deposition of Top Electrode

A layer of Titanium Nitride (TiN) of 10nm is deposited on a silicon (Si) wafer to serve as the top electrode for the NRAM device [149].

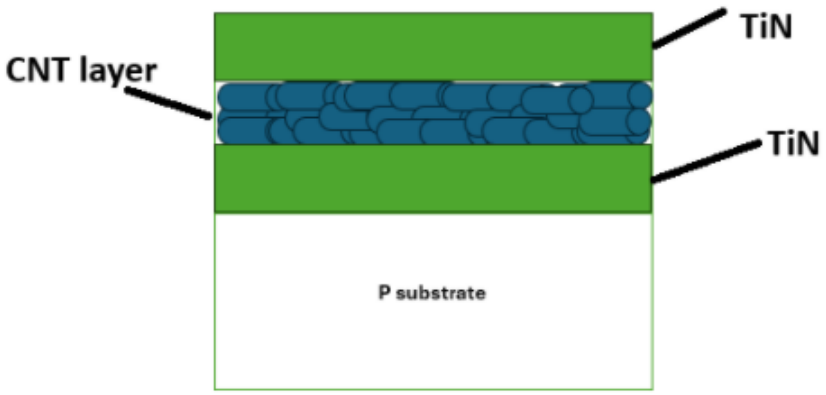

Figure 4.4: Deposition of Titanium Nitride as top electrode

4.3 Working Mechanism of CNT based memories

Non-Volatile Random Access Memory (NRAM) utilizing carbon nanotubes (CNTs) operates based on the relative mechanical displacement of CNTs with respect to an electrode [135]. This memory technology exploits the pronounced resistance difference between the nanotube's contact and suspended configurations, enabled by their intrinsic electromechanical characteristics [132].

1. Bit Representation (0 and 1) [45]

NRAM stores binary data by exploiting the bistable mechanical states of carbon nanotubes (CNTs):

- **'0' State (High Resistance State / Set State / OFF):**
  CNTs are suspended above the bottom electrode and are not in contact as illustrated in figure 4.5. The gap creates a high resistance path, interpreted as logic "0".
- **'1' State (Low Resistance State / Reset State / ON):**
  CNTs are deflected downward, making physical contact with the bottom electrode due to van der Waals and electrostatic forces as illustrated in figure 4.6. This results in a low resistance state, interpreted as logic "1".

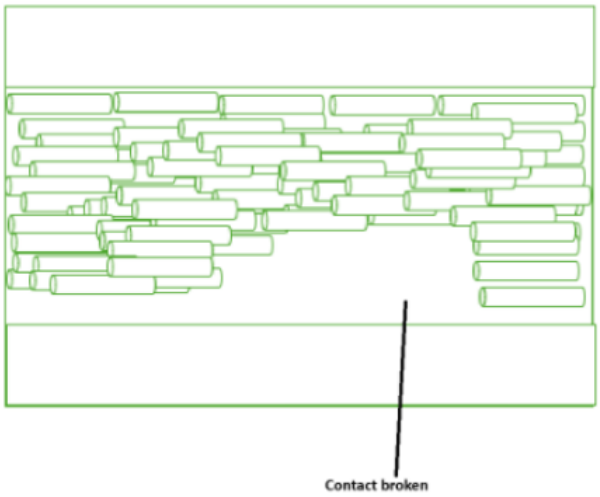

Figure 4.5: High Resistance State

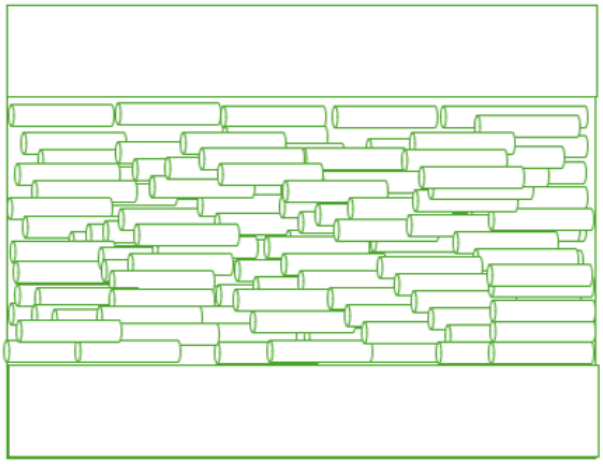

Figure 4.6: Low Resistance State

2. Write Operation

- A voltage pulse is applied between the top and bottom electrodes.
- The electrostatic force generated pulls the CNTs downward (if writing a '1') or releases them (if writing a '0').
- Once the voltage is removed, van der Waals forces or elastic strain hold the CNT in place — maintaining its state non-volatilely (without needing power).

3. Read Operation

- A small read voltage is applied across the memory cell.
- The resulting current is measured:
  - High resistance → CNT not in contact → logic '0'
  - Low resistance → CNT in contact → logic '1'
- The read voltage is kept low enough not to disturb the CNT position.

4.4 Synthesis of Carbon Nanotubes for CNT-Based NRAM

The production of high-quality carbon nanotubes (CNTs) is a critical prerequisite in the fabrication of CNT-based non-volatile random-access memory (NRAM). For such applications, it is essential that CNTs possess high structural quality, a high degree of purity, uniformity in length and diameter, and stable electrical characteristics, as these factors significantly influence the device's performance, dependability, and scalability [135].

Three primary synthesis techniques that are widely used [123]:

1. **Arc Discharge Method**
2. **Laser Ablation Method**
3. **Chemical Vapor Deposition (CVD)**

Table 4.1: Comparative Analysis of CNT Synthesis Techniques for NRAM Applications

Parameters	**Arc Discharge** [5] [123] [58] [61]	**Laser Ablation**[123] [156] [61]	**Chemical Vapor Deposition** [123] [61] [85] [162] [139]
CNT Type	Mostly MWCNTs, some SWCNTs	Mostly SWCNTs	SWCNTs or MWCNTs (controllable)
Purity	Moderate (70–80%)	High (>90%)	High (90%, tunable)
Crystallinity	Very High	Very High	High (process-dependent)
Diameter Control	Poor	Good	Excellent (1–3 nm)
Length Control	Limited	Moderate	Good (time-controlled)
Alignment of CNTs	Poor	Poor	Excellent (aligned growth possible)
Scalability	Low	Very Low	High
CMOS Compatibility	No (due to high temperature)	No (due to high temperature)	Yes
Growth Temperature	3000°C	1200°C	600–900°C
Yield / Throughput	Low	Very Low	High
Fabrication Cost	Moderate	High	Low
Suitability for NRAM	Limited to research	High purity but poor scalability	Highly suitable for commercial devices
Advantages	High-quality CNTs can be produced	High purity, uniform diameter	Scalable, CMOS-compatible, tunable growth
Limitations	Poor alignment, low yield, metal impurities	Expensive, not scalable, limited placement control	Catalyst contamination (manageable)

Each carbon nanotube (CNT) synthesis technique offers distinct advantages and limitations. The arc discharge method is particularly noted for producing high-quality CNTs, especially with excellent crystallinity. However, it is inherently limited by its low scalability and batch processing nature, making it less suitable for large-scale production.

The laser ablation method is also capable of generating high-purity single-walled CNTs (SWCNTs) with uniform diameters. Nonetheless, its high operational costs—stemming from the use of high-energy lasers—and the difficulty in scaling the process present significant drawbacks for industrial adoption.

In contrast, the chemical vapor deposition (CVD) method is regarded as the most scalable and cost-effective technique, making it highly favourable for mass production. Despite this advantage, CNTs synthesized via CVD generally exhibit lower crystallinity and purity compared to those produced by arc discharge or laser ablation.

In summary, the selection of a CNT synthesis method should be guided by the specific application requirements. For small-scale applications demanding high structural quality, arc discharge and laser ablation are more appropriate. Conversely, for large-scale manufacturing where cost and throughput outweigh purity, CVD emerges as the practical choice.

4.5 Electrode Selection for NRAM

The efficiency and reliability of CNT-based non-volatile random-access memory (NRAM) are significantly affected by the selection of electrode materials. These electrodes must support effective charge transport, provide robust adhesion, exhibit chemical and thermal stability, and remain compatible with both CNT integration and CMOS fabrication processes. In a typical NRAM architecture, the bottom electrode acts as the static contact layer, whereas the top electrode interfaces with the suspended CNTs to facilitate bistable switching between high and low resistance states.
Materials such as Titanium Nitride (TiN), Platinum (Pt) and Gold (Au) are commonly employed due to their varied electrical and physical properties. Among these, TiN is frequently chosen because of its high electrical conductivity, excellent thermal stability, and strong adherence to silicon substrates [182]. While Pt and Au are chemically inert and provide low contact resistance, their use is limited by high cost and integration complexity [176] [175].
An ideal electrode material for NRAM applications should offer minimal contact resistance with CNTs, resist material diffusion, and maintain high electromigration resistance under high-speed switching conditions [49].

Table 4.2: Comparison of Common Electrode Materials for CNT-Based NRAM

Material	**Electrical Conductivity**	**Thermal Stability**	**CNT Contact Resistance**	**CMOS Compatibility**	**Cost**	**Suitability**
TiN [112, 19, 51]	High	Excellent	Low	Yes	Low	Highly suitable for commercial use
Pt [176, 32]	Very High	Excellent	Very Low	Limited	High	Suitable but expensive
Au [175, 79, 9]	Very High	Good	Very Low	Limited	High	Suitable for research purpose

Based on the comparative analysis of electrode materials, **Titanium Nitride (TiN)** emerges as the most suitable choice for CNT-based NRAM applications. It offers a balanced combination of high electrical conductivity, excellent thermal stability, strong adhesion to silicon substrates, and full CMOS process compatibility, all of which are essential for reliable and scalable memory fabrication. Furthermore, TiN provides low contact resistance with CNTs and is cost-effective, making it ideal for both research and industrial-scale production.

While **Platinum (Pt)** and **Gold (Au)** deliver superior chemical inertness and extremely low contact resistance, their high cost and limited CMOS integration restrict their practicality to niche or research-based implementations.

In conclusion, TiN offers the best trade-off between performance, compatibility, and manufacturability, making it the electrode of choice for CNT-based NRAM devices.

4.6 Thickness of the CNT Layer in NRAM Devices

The thickness of the carbon nanotube (CNT) layer is a critical parameter in the fabrication of CNT-based non-volatile random-access memory (NRAM), as it directly influences the device's electrical performance, mechanical reliability, and scalability. Although exact thickness values are seldom disclosed in public literature due to the proprietary nature of commercial NRAM

technologies, studies and industrial presentations suggest that controlling the CNT layer thickness is essential for ensuring proper device operation.

In general, the CNT layer must be thin enough to support rapid electro-mechanical switching, yet dense and continuous enough to ensure reliable electrical conduction and contact with electrodes. According to Nantero's Hot Chips 2018 presentation, multi-layer CNT configurations have been explored to enhance memory density, implying that layer uniformity and tunable thickness are actively engineered within the fabrication process [44].

The thickness of the CNT layer can be precisely controlled during the deposition process, as it depends on parameters such as material concentration, deposition duration, and process conditions, all of which influence the final film uniformity and thickness. Some technical reports on CNT thin films for electronic applications indicate that film thicknesses in the range of **30–50 nm** [47, 187, 186] are desirable for achieving consistent switching behaviour and adequate surface coverage. While these values are more commonly referenced in the context of general CNT-based electronics rather than NRAM specifically, a thickness of approximately 30 nm is often considered optimal for balancing mechanical responsiveness and electrical conductivity in nanoscale devices [47].

Therefore, while precise thickness specifications for CNT-based NRAM remain undisclosed, it is generally accepted that the CNT layer must be carefully optimized to balance mechanical flexibility, electrical connectivity, and process compatibility.

4.7 Deposition of Carbon Nanotube (CNT) Layers on Substrates for NRAM

Carbon nanotubes (CNTs) are widely used in NRAM due to their high electrical conductivity, mechanical strength, and nanoscale dimensions. The quality of CNT deposition on substrates directly impacts device performance, making the deposition process critical[42]. Several techniques have been explored to deposit aligned or randomly oriented CNTs, each with specific benefits and limitations.

Table 4.3: Comparison of CNT Deposition Techniques

Technique	Alignment	Temperature	Scalability	Advantages	Limitations
CVD [40]	Random	High (>600°C)	High	Direct growth, high purity	High temperatures (>600°C) may be unsuitable for some substrates, Complex control of growth parameters
Spin Coating [42]	Random	Low	Medium	Simple, uniform, good control over film thickness	Random orientation, Difficult to coat large areas uniformly due to spin speed limitations, Non-uniform material distribution which gets worse on larger substrates.
Drop Casting [60, 67]	Random	Low	Challenging for industrial scaling	Simple and cost-effective, No specialized equipment required, Fast deposition method, Compatible with a wide variety of nanoparticles and substrates	Inhomogeneous surface modification due to the coffee ring effect, Reproducibility issues, Particle aggregation or detachment
Inkjet Printing [68, 14]	Partial alignment achieved using surface treatment (OTS), but overall films are composed of random and semi-aligned CNT networks.	Printing is done at room temperature but post-print annealing at 140°C to remove residual NMP	High scalability and suitable for large-area and industrial-scale fabrication	Direct patterning of materials, No need for masks or etching, Compatible with flexible substrates, Printable on various surfaces (glass, Si, plastic), Surfactant-free stable ink formulation.	Clogging issues in nozzles due to CNT bundling, Limited control over CNT alignment and density.
Dielectrophoresis [191]	Highly aligned	Low	High	Simple, precise control, low cost, CMOS compatible	Limited by electric field gradient, MWNTs align less effectively, Not ideal for very large areas
Langmuir-Blodgett [16, 81, 180]	Highly controlled alignment	Low	It is not necessarily scalable in size or throughput but this technique is more suited to precision over volume	Excellent control over film structure, Fabricate ultrathin to multilayer films with varied compositions.	Requires precise control of multiple variables—temperature, surface pressure, deposition speed, substrate type, and sub-phase composition—with high environmental sensitivity, making it complex and less suitable for large-scale production.

Each deposition method has unique strengths suited to specific applications:

- **Best for industrial scalability:** Inkjet printing offers good scalability, room-temperature processing, and patterning flexibility, though alignment control is limited.
- **Best for precision and alignment:** Langmuir-Blodgett and Di-electrophoresis provide high alignment and structural control but are less scalable.
- **Best for direct synthesis and purity:** CVD is ideal when high purity and in-situ growth are needed, albeit with high temperature and complexity constraints.
- **Best for simplicity and cost-effectiveness:** Drop casting and Spin coating are economical but suffer from poor alignment and reproducibility issues.

For scalable applications requiring moderate alignment and pattern ability (e.g., flexible electronics), **inkjet printing with surface treatment** offers the most balanced approach. For high-precision lab-scale work, **Langmuir-Blodgett or Di-electrophoresis** are preferred.

4.8 Comparative Analysis of SWCNT and MWCNT in Non-Volatile Random Access Memory (NRAM) Applications

As the demand for faster, energy-efficient, and non-volatile memory technologies continues to grow, carbon nanotube-based NRAM has emerged as a promising candidate to replace or complement conventional memory architectures such as DRAM and flash. Carbon nanotubes (CNTs), owing to their exceptional electrical, thermal, and mechanical properties, have been widely studied for such applications. Two primary forms of CNTs—Single-Walled Carbon Nanotubes (SWCNTs) and Multi-Walled Carbon Nanotubes (MWCNTs)—offer unique advantages and challenges when integrated into NRAM devices.

This comparative analysis explores the structural, electrical, thermal, and integration-related characteristics of SWCNTs and MWCNTs in the context of NRAM technology. The goal is to highlight the trade-offs between performance and practicality that influence the choice of CNT type in commercial and research memory applications.

Table 4.4: Comparison of SWCNT and MWCNT for NRAM Applications

Parameters	**SWCNT (Single-Walled CNT)**	**MWCNT (Multi-Walled CNT)**
Structure [122]	Single graphene sheet rolled into a cylinder	Multiple concentric graphene cylinders
Thermal Conductivity [15]	Extremely high	Lower than SWCNT
Electrical Conductivity [114]	10^6 S/m	10^5 S/m
NRAM Switching Mechanism	Electromechanical deflection of nanotubes to toggle resistance	Similar mechanism
Fabrication Complexity [62, 106]	More complex due to structural sensitivity, selective growth needs, and demanding purification	Easier and cheaper to fabricate, more robust, better for bulk use
Purity [62]	Impure	Pure

SWCNT (Single-Walled Carbon Nanotubes) – Best Choice for NRAM

After a detailed comparative analysis, it is evident that Single-Walled Carbon Nanotubes (SWCNTs) are more suitable for Non-Volatile Random Access Memory (NRAM) applications than Multi-Walled Carbon Nanotubes (MWCNTs). Despite challenges such as higher fabrication complexity and lower inherent purity, SWCNTs offer a suite of critical advantages that make them highly effective in next-generation memory technologies.

Superior Electrical and Thermal Properties

SWCNTs exhibit ballistic electron transport and can behave as either metallic or semiconducting depending on their chirality, enabling precision switching—a core requirement in NRAM. Additionally, their exceptionally high thermal conductivity allows efficient heat dissipation, which is crucial for the stability and longevity of high-performance memory devices.

Smaller Diameter & High Aspect Ratio

With a diameter of approximately 1 nm [62], SWCNTs enable the development of ultra-high-density memory cells, making them ideal for nanoscale device integration and aggressive scaling.

Better Electrostatic Control

The one-dimensional structure of SWCNTs provides enhanced electrostatic gate control, improving device stability, reducing leakage, and ensuring low-power operation—all key aspects for energy-efficient NRAM.

Proven Use in NRAM Prototypes

Many academic and commercial implementations, such as those by Nantero Inc. [107], have successfully employed SWCNT networks due to their tuneable conductivity and van der Waals-based switching mechanisms, further validating their effectiveness in practical NRAM systems.

Comparison with MWCNTs

On the other hand, MWCNTs, while easier to synthesize and possessing higher purity, suffer from drawbacks such as larger diameters, unpredictable inter-shell interactions, and less controllable electrical behaviour. These factors make them less suited for the precision and miniaturization required in modern non-volatile memory design.

SWCNTs clearly outperform MWCNTs in the context of NRAM applications, providing the essential attributes for scalable, fast, stable, and energy-efficient memory. Their use aligns perfectly with the stringent demands of future memory technologies.

4.9 Comparison of Purification Methods for Carbon Nanotubes (CNTs)

Carbon nanotubes (CNTs) often come with impurities like metal catalysts, amorphous carbon, and other residues after production. To unlock their full potential, they must be purified—but different methods have trade-offs in effectiveness, yield, and nanotube integrity. Below is a comparative overview of commonly used purification techniques.

Table 4.5: Comparative Overview of Common CNT Purification Techniques

Purification Technique	**Advantages**	**Disadvantages**
Gas Phase Oxidation [56]	• Simplicity and low cost. • Effective for MWCNTs. • Opens CNT ends for functionalization. • Scalable for small quantities.	• Limited yield for SWCNTs. • Difficulty in discriminating CNTs from amorphous carbon. • Requires multiple treatment cycles. • High-temperature oxidation may introduce defects.
Liquid Phase Oxidation [56]	• Removes amorphous carbon and metal residues in one step. • Uniform and efficient purification via solution penetration.	• Strong oxidants can damage CNTs, especially SWCNTs. • Sample loss due to aggressive oxidation. • Scaling issues and post-treatment complexity.
Electrochemical Oxidation [56]	• Selective removal of defective carbon. • Real-time process control (e.g., via CV). • Suitable for vertically aligned CNTs. • Rapid and efficient.	• Ineffective against well-protected or defect-free impurities. • Limited scalability. • Performance depends on CNT sample quality.

Purification Technique	**Advantages**	**Disadvantages**
Centrifugation [56, 195, 13]	• Simple and scalable. • Enables density-based separation of CNTs and impurities. • Selective via speed: low-speed for amorphous carbon, high-speed for SWCNTs.	• Requires acid treatment—can damage CNTs. • Not highly selective for similar carbon structures. • Ineffective for catalyst residue removal.
Filtration [56, 11]	• Non-destructive. • Effective with surfactants and sonication. • Can be repeated for improved results.	• CNT breakage. • Time-consuming. • Filter clogging and retention of adhered carbon particles.
Thermal Annealing [56, 57]	• Effective for removing encapsulated metals. • Enhances CNT quality.	• High energy requirement. • May affect CNT structural properties like chirality and diameter.

4.10 Conclusion

Carbon Nanotube-based Non-Volatile Random Access Memory (CNT-NRAM) represents a compelling frontier in memory technology, combining the exceptional electrical, mechanical, and thermal properties of carbon nanotubes (CNTs) with a scalable, low-power, and high-speed non-volatile data storage mechanism. This technology harnesses the bistable mechanical states of CNTs—achieved through precise electrostatic manipulation—to enable reliable binary switching without the need for continuous power, thereby offering significant advantages over conventional memory types such as DRAM and flash.

The fabrication of CNT-NRAM involves carefully coordinated steps including substrate preparation, electrode deposition, CNT synthesis, purification, and controlled deposition, all of which collectively determine the device's efficiency and manufacturability. Titanium Nitride (TiN) emerges as the optimal electrode material due to its favourable electrical, thermal, and CMOS-compatible characteristics, while SWCNTs (Single-Walled Carbon Nanotubes) are identified as the superior choice for active memory elements because of their exceptional conductivity, small diameter, and well-controlled switching behaviour.

Among CNT synthesis techniques, Chemical Vapor Deposition (CVD) stands out as the most viable method for commercial-scale production, offering tunable growth, CMOS compatibility, and high throughput. Similarly, inkjet printing and spin coating present practical approaches for scalable CNT deposition, whereas techniques like di-electrophoresis and Langmuir-Blodgett offer high alignment for research-grade devices.

In summary, the integration of SWCNTs, optimized electrode materials like TiN, and scalable fabrication techniques positions CNT-NRAM as a highly promising candidate for next-generation memory systems. Its unique combination of speed, scalability, low power consumption, and non-volatility addresses the critical limitations of current memory technologies, paving the way for widespread adoption in both high-performance computing and portable electronics.Additionally, our comparative analysis of CNT purification techniques—including oxidation (gas, liquid, electrochemical), centrifugation, filtration, and high-temperature annealing—highlights the pivotal role of purification in achieving the structural and chemical integrity necessary for reliable NRAM performance. Selecting the appropriate purification pathway based on application-specific requirements ensures that CNTs can be effectively integrated into robust and high-performing memory architectures.

Chapter 5

Advanced GAA-Based NVM Architectures and Their Fabrication

5.1 Introduction

Gate-All-Around (GAA) transistor architecture has emerged as a key technology in advanced semiconductor nodes, offering enhanced electrostatic control, excellent scalability, and reduced short-channel effects compared to FinFET and planar structures. These benefits make GAA an attractive platform not only for logic circuits but also for the integration of non-volatile memory (NVM) devices.

Among the various NVM technologies explored for compatibility with GAA structures, SONOS (Silicon–Oxide–Nitride–Oxide–Silicon) and FeFET (Ferroelectric Field-Effect Transistor) are the two most well-researched and experimentally validated candidates. In both cases, the memory functionality is embedded directly within the GAA transistor itself. SONOS achieves non-volatility through charge trapping in a nitride layer, while FeFET relies on remanent polarization within a ferroelectric gate dielectric. This integration allows the transistor to serve simultaneously as the storage and switching element.

In contrast, other NVM technologies such as ReRAM, MRAM, PCRAM, and CBRAM primarily utilize GAA transistors as access or selector devices in 1T1R configurations, where the actual memory function is performed by a separate element external to the transistor. While these architectures benefit from the leakage suppression and density advantages of GAA, the memory mechanism is not intrinsic to the FET.

This chapter focuses on the fabrication and integration of SONOS and FeFET as true GAA-based non-volatile memory technologies, where the GAA structure plays a central role in both switching and data storage.

5.2 Fabrication Steps

Gate-All-Around (GAA) transistors, with their superior electrostatic control and scalability, offer a robust platform for the integration of non-volatile memory (NVM) technologies. Among these, SONOS (Silicon–Oxide–Nitride–Oxide–Silicon) [174] and FeFET (Ferroelectric Field-Effect Transistor) [173] have emerged as two of the most well-researched and experimentally validated architectures in which the memory function is embedded directly within the GAA transistor structure.

In GAA SONOS memory, data storage is achieved by trapping charges within a silicon nitride layer embedded in the gate dielectric stack, while GAA FeFET utilizes a ferroelectric material

to modulate the transistor's threshold voltage through reversible polarization. Both approaches modify the gate stack of a GAA FET, enabling it to act as both the switching and memory element in a single device. The fabrication of these devices involves a shared sequence of fundamental CMOS-compatible steps—such as channel formation, gate wrapping, and source/drain engineering—followed by specialized steps for memory-specific gate stack formation.

The following sections present a detailed, generalized flow of the fabrication process for GAA-based SONOS and FeFET devices, highlighting both their commonalities and the distinct requirements that arise from their differing memory mechanisms.

5.2.1 Fabrication of GAA based SONOS [23]

Substrate Selection and Preparation

The process begins with the selection of a suitable substrate. Typically, a silicon wafer or a Silicon-On-Insulator (SOI) [2] wafer is used to enhance isolation and reduce parasitic capacitance. In this case, an 8-inch p-type silicon substrate is used to form the foundation of the device. The wafer is thoroughly cleaned using standard RCA[172] cleaning methods to remove organic and ionic contaminants, ensuring a defect-free surface for subsequent processing.

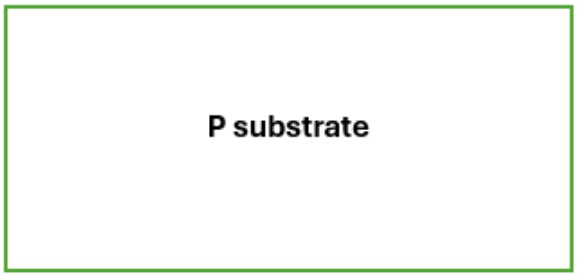

Figure 5.1: Substrate Selection

Vertical Nanowire Fabrication

The vertical silicon nanowires [194] were fabricated using a top-down, CMOS-compatible approach. Initially, circular resist dots (160 to 600 nm in diameter) were patterned on an 8-inch silicon wafer, followed by deep silicon etching ($\sim$1 μm) under a SiN hard mask using SF_6 chemistry.

The resulting pillars were oxidized at 1150°C to reduce their diameter and form a stable base, leveraging the slower oxidation rate at high-curvature points. This oxidation step created smooth, cylindrical silicon cores, which were then exposed by removing the oxide layer in dilute hydrofluoric acid (DHF).

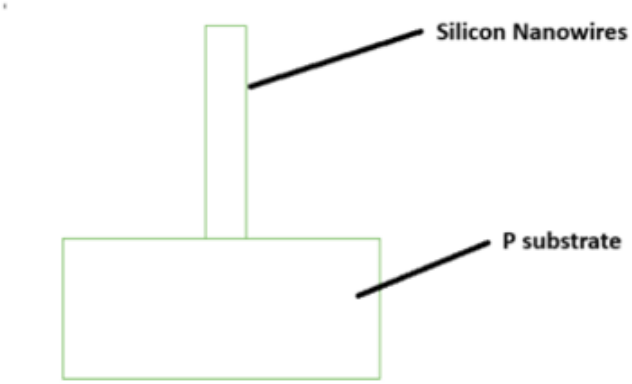

Figure 5.2: Vertical Nanowires formation

Source implantation

The source region in the vertical silicon nanowire devices was created using ion implantation, a process where ions of a specific element—arsenic (As)—are accelerated to high energies and directed at the silicon substrate. A rapid thermal annealing (RTA) step at approximately 1000°C for 10 seconds was applied to activate the dopants[94].

A silicon nitride hard mask was used to protect the tip of the nanowire from implantation, ensuring precise doping only in the desired source region [66].

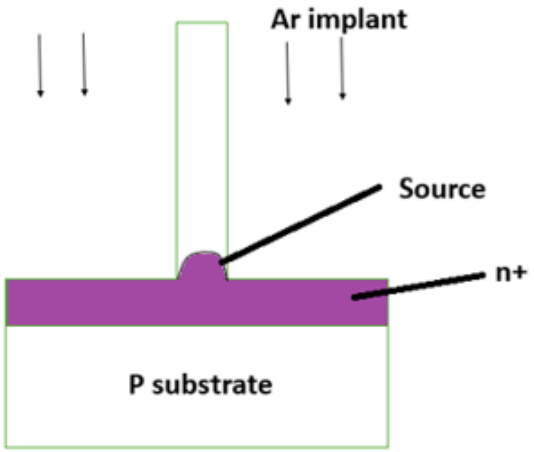

Figure 5.3: Source Implantation

Formation of the Charge Trapping Layer and Gate Formation

A 120 nm oxide layer is formed to protect the base of the nanowires by first depositing high-density plasma (HDP) oxide [109], followed by a dilute hydrofluoric acid (DHF) etch-back.

Next, a 5 nm tunneling oxide is thermally grown on the exposed nanowire surfaces, after which a 5 nm silicon nitride charge-trapping layer and a 6 nm blocking oxide layer are deposited using low-pressure chemical vapor deposition (LPCVD) [69].

This sequence is followed by polysilicon deposition to create the gate stack, which is then patterned and etched to form the gate pad, providing a poly-extension for the gate contact.

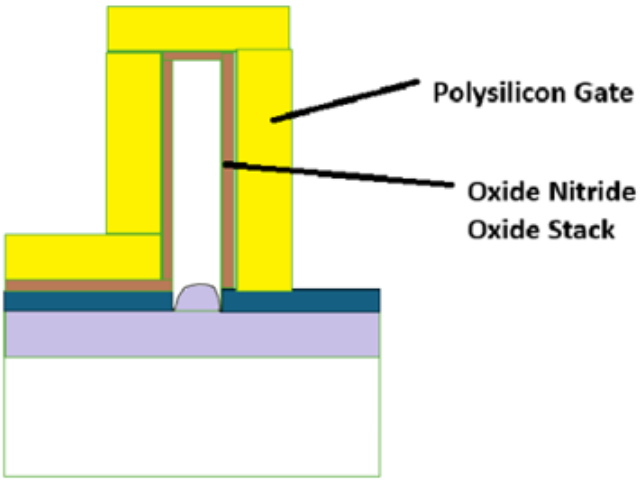

Figure 5.4: Charge trapping layer

Drain Formation

An additional layer of high-density plasma (HDP) oxide is deposited and then etched back to selectively expose the top portion of the polysilicon, while maintaining protection over the underlying gate pad. The uncovered polysilicon and any remaining silicon hard mask are subsequently etched away using reactive ion etching (RIE) [34], exposing the upper part of the nanowires.

Arsenic (As^+) ions are then implanted to form the drain region. A rapid thermal annealing (RTA) step at approximately 1000°C for 10 seconds is applied to activate the dopants [94].

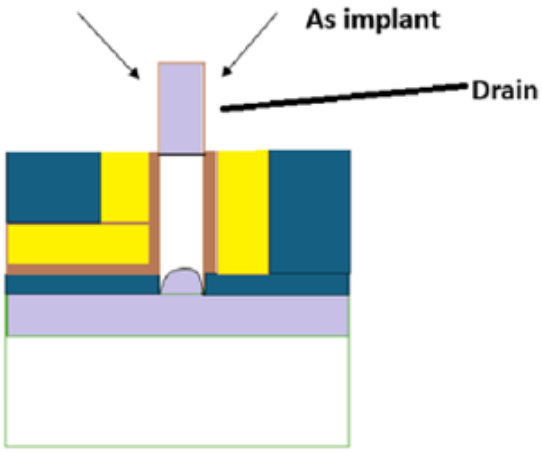

Figure 5.5: Drain formation

Contact formation

The process concludes with a final deposition of high-density plasma (HDP) oxide, which is then etched back to expose the silicon tip. This selective etch-back enables the formation of the metal contact through standard metallization techniques, completing the device structure.

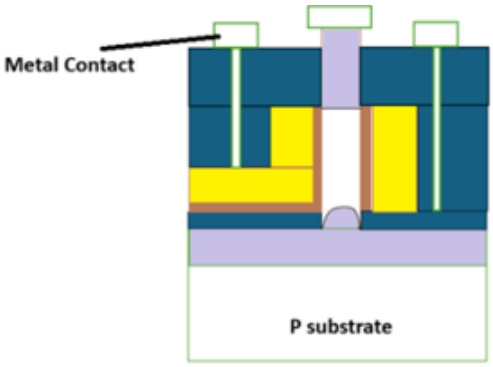

Figure 5.6: Final Device

Working Mechanism

Program Operation (Write)

- A positive voltage is applied to the control gate (poly-Si).
- Electrons tunnel from the Si nanowire channel through the tunneling oxide into the silicon nitride layer.
- These electrons become trapped in the nitride layer, shifting the threshold voltage.
- **Result:** The cell is programmed and will conduct less current during read.

Erase Operation

- A negative voltage is applied to the control gate, and a positive voltage to the drain.
- This creates a field that causes electrons to tunnel back from the nitride layer to the channel or recombine.
- **Result:** The threshold voltage decreases, restoring high current flow during read.

Read Operation

- A small gate voltage is applied that is not sufficient to cause tunneling.
- A small drain-to-source voltage is applied to allow current flow.
- The amount of current depends on whether electrons are trapped:
  - Trapped electrons – Low or no current → Logical “1”
  - No trapped electrons – Current flows → Logical “0”

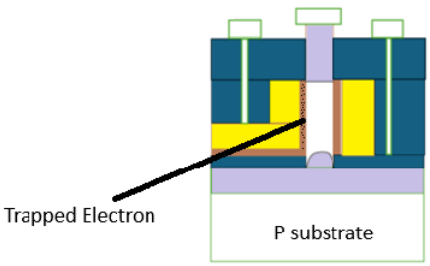

Figure 5.7: Charge Trapping at the ONO laye

5.2.2 Fabrication of GAA based Fe-FET

Substrate Selection

The process begins with the selection of a suitable substrate. Typically, a silicon wafer or a Silicon-On-Insulator (SOI) [2] wafer is used to enhance isolation and reduce parasitic capacitance. In this case, a p-type SOI substrate is used to form the foundation of the device.

The wafer is thoroughly cleaned using standard RCA [172] cleaning methods to remove organic and ionic contaminants, ensuring a defect-free surface for subsequent processing.

The SOI wafer consists of a thin layer of single-crystal silicon, typically around 20 nm thick, situated atop a thicker buried silicon dioxide (SiO_2) layer, approximately 100 nm thick. This structure is supported by a silicon handle wafer. The layered architecture provides both electrical isolation and mechanical stability, which are crucial for reliable device fabrication.

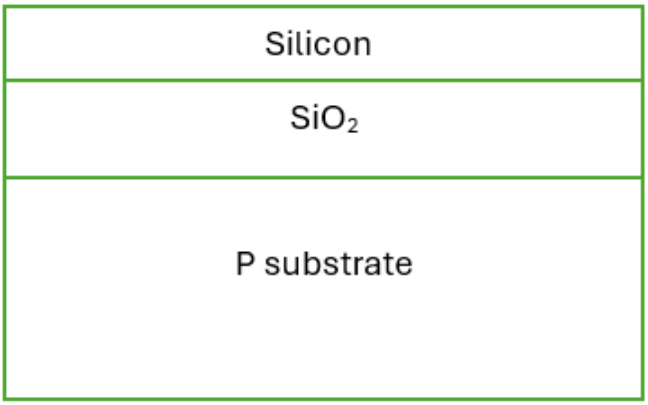

Figure 5.8: Substrate selection

Nanowire Fabrication

- **Resist Coating and Patterning:**
  Hydrogen silsesquioxane (HSQ) [171], a high-resolution, negative-tone electron beam (e-beam) resist, is spin-coated onto the SOI substrate. HSQ is chosen for its exceptional ability to resolve features down to the nanometre scale, making it ideal for fabricating narrow nanowire structures. The HSQ resist is then exposed to a focused e-beam, which selectively cross-links the exposed regions, forming the nanowire pattern. The unexposed areas remain soluble in the developer solution [64].

- **Development of the Nanowire Pattern:**
  After exposure, the substrate is developed in a tetramethylammonium hydroxide (TMAH) solution, which dissolves the unexposed HSQ, leaving behind the hardened, cross-linked nanowire structure [43].

- **Reactive Ion Etching (RIE)[34]:**
  The developed HSQ structures serve as a durable etch mask during the subsequent RIE step. RIE uses chemically reactive plasma to etch away the exposed silicon, transferring the nanowire pattern into the underlying silicon layer. This step is highly anisotropic, resulting in well-defined, vertical nanowires with precise control over diameter and height. The buried oxide layer in the SOI substrate acts as an effective etch stop, ensuring consistent nanowire lengths [43].

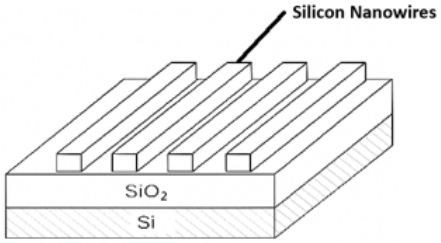

Figure 5.9: Top view of the nanowires [95]

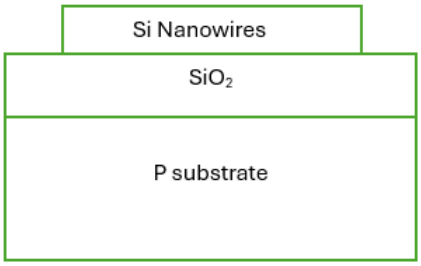

Figure 5.10: Side view of the nanowires

Thermal Oxidation

A thin thermal SiO_2 shell, approximately 5 nm thick, is grown around the silicon nanowires during this step [165]. This thermally grown oxide layer provides essential electrical isolation between the silicon core and the surrounding materials.

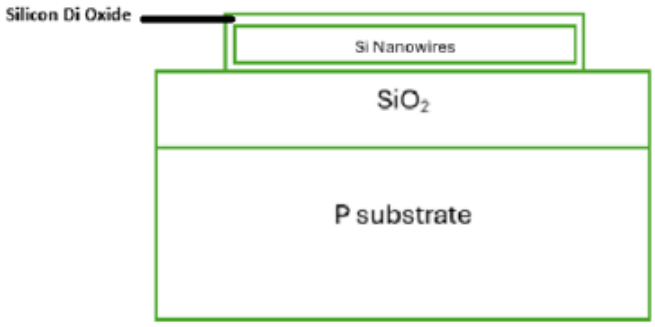

Figure 5.11: Thermal Oxidation

HfO_2 Layer Deposition

The hafnium dioxide (HfO_2) layer is deposited using atomic layer deposition (ALD), which provides excellent thickness control and conformality—especially important for three-dimensional nanostructures.

Following deposition, a rapid thermal annealing (RTA) step is applied to activate the ferroelectric properties of the HfO_2 layer [102, 129, 146] as illustrated in figure 5.12 . This step is critical for enabling memory functionality in ferroelectric field-effect transistors (FeFETs).

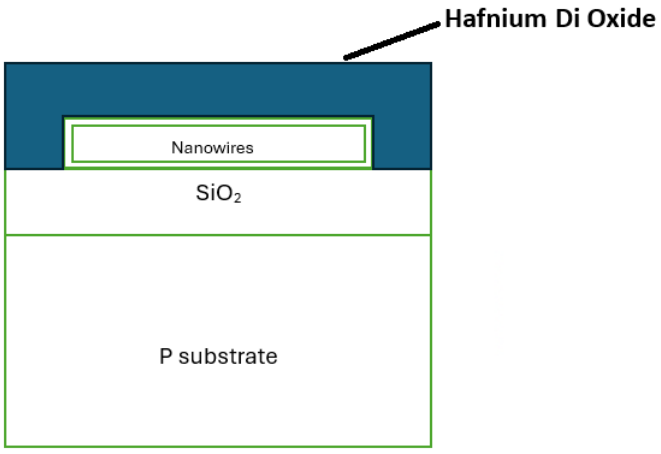

Figure 5.12: HfO_2 Layer Deposition

Gate Electrode Formation

Titanium Nitride gate electrode is deposited by PVD [159].

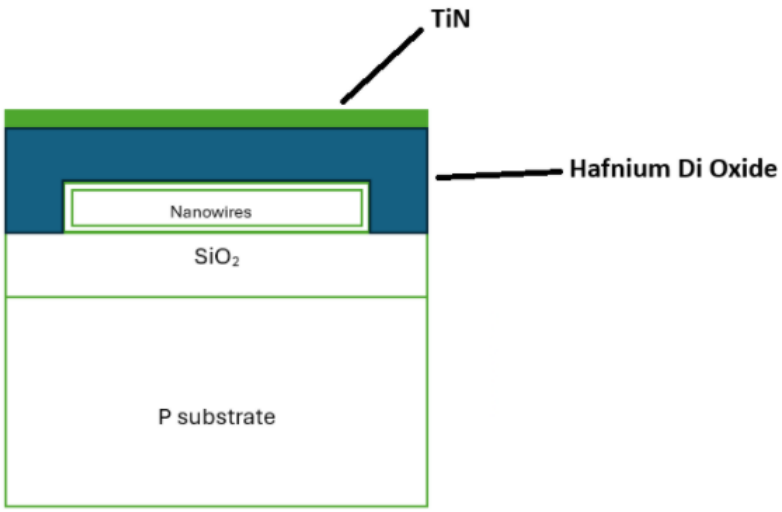

Figure 5.13: Gate Layer Deposition

Gate Lithography

A polysilicon layer is deposited over the TiN gate followed standard masking and etching process is carried out to form define the gate area (refer to chapter 1)

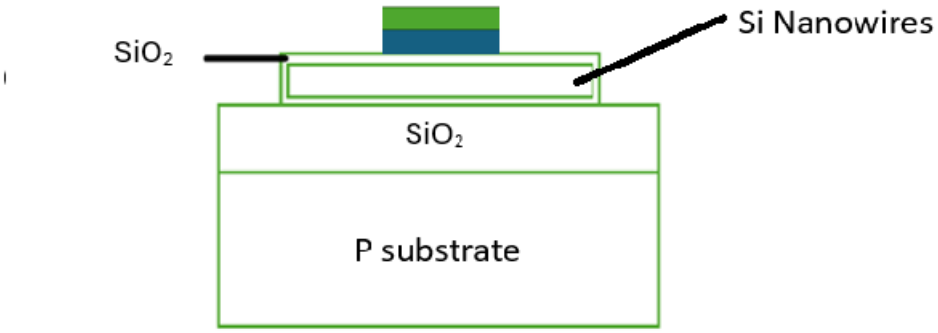

Figure 5.14: Standard Lithography

Contact formation

Deposit a thin nickel (Ni) film (typically 10-20 nm) as contact onto the exposed silicon nanowire structures using physical vapor deposition (PVD) methods such as sputtering [160].

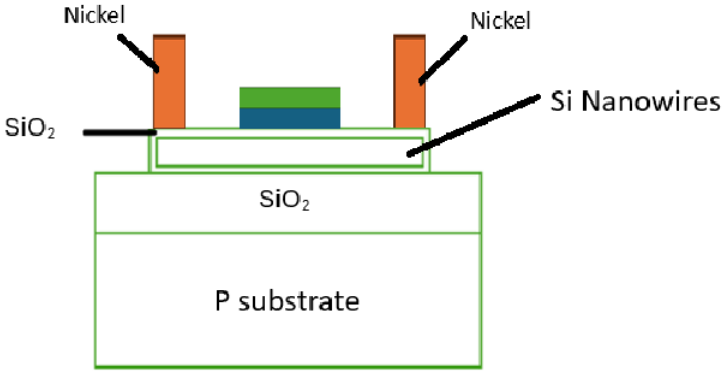

Figure 5.15: Contact formation

Source and Drain Formation

Perform Rapid Thermal Annealing (RTA) in a forming gas atmosphere (e.g., 10% H_2 and 90% N_2) to initiate the silicidation reaction. The annealing temperature typically ranges from 400 °C to 500 °C. For $NiSi_2$ formation, a temperature around 450 °C is preferred, while higher temperatures (approximately 700 °C) may promote the formation of NiSi [70].

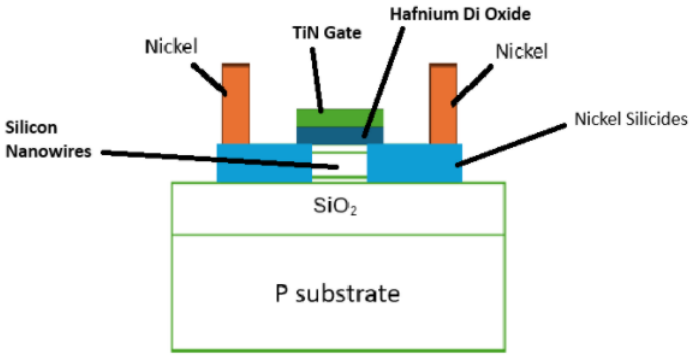

Figure 5.16: Final Device

Working Mechanism

Program Operation

- Apply a positive voltage pulse at the gate.
- **Effect:** Aligns the ferroelectric dipoles to reinforce the depletion of holes in the p-type conduction (intrinsic Si → more "off") as illustrated in the figure 5.17.
- The transistor turns less conductive → interpreted as logic **'0'**.

ERASE Operation

- Apply a negative voltage pulse at the gate.
- **Effect:** Aligns dipoles to reduce channel depletion, enhancing conduction as illustrated in the figure 5.18.

- The transistor turns more conductive → interpreted as logic **'1'**.

READ Operation

- Apply a non-intrusive gate voltage.
- **Effect:** Doesn't disturb the polarization state.
- Measure drain current:
  - High Drain Current ⇒ State = **'1'** (erased)
  - Low Drain Current ⇒ State = **'0'** (programmed)

Figure 5.17: Programmed State

Figure 5.18: Erased State

5.3 Gate-All-Around (GAA) Structures

Gate-All-Around (GAA) transistor structures represent a significant advancement in semiconductor technology, aimed at extending Moore's Law and enhancing device performance in the sub-5 nm technology nodes. Unlike traditional FinFETs, GAA devices provide superior electrostatic control over the channel by completely surrounding it with the gate, resulting in reduced short-channel effects, improved scalability, and enhanced power efficiency.

Currently, two primary types of GAA structures are widely used in practice: nanowires and nanosheets [10]. These structures differ significantly in their geometries, fabrication methods, and electrical performance characteristics, each offering unique advantages depending on the specific application.

Both nanowire and nanosheet GAA structures are critical to the development of next-generation CMOS technologies, with applications ranging from high-speed logic circuits to low-power IoT devices. As semiconductor scaling continues, these GAA architectures are expected to play a crucial role in enabling further performance improvements while reducing power consumption.

5.3.1 Evaluating GAA Nanowire and Nanosheet Structures for NVM Devices

The table below provides a comparative evaluation of GAA nanowire and nanosheet structures with respect to their suitability for non-volatile memory (NVM) applications. Key parameters such as channel geometry , electrostatic control , drive current , short-channel effects (SCEs) , fabrication complexity , and scalability are analyzed to highlight the trade-offs and advantages of each architecture.

Table 5.1: Comparison of GAA Nanowire vs. Nanosheet for NVM Applications

Parameter	**GAA Nanowire (NW)**	**GAA Nanosheet (NS)**
Channel Geometry [141]	Cylindrical or square cross-section; fully surrounded by gate	Rectangular cross-section; gate wraps around top and sides
Electrostatic Control [10]	Excellent due to full gate enclosure	Very good; slightly less than NW due to partial gate enclosure
Drive Current [10, 6]	Moderate; limited by smaller effective channel width	Higher; larger effective channel width allows greater current drive
Short-Channel Effects (SCEs) [10]	Superior suppression due to full gate control	Good suppression; slightly more susceptible than NW
Fabrication Complexity [6, 184, 125]	Simpler	Complex
Scalability [184]	Excellent; suitable for sub-5nm nodes	Good; challenges arise below 5nm due to increased variability
Suitability for NVM [190, 23, 121]	Promising; excellent control beneficial for charge retention in NVM cells	Highly suitable; higher drive current and integration density advantageous for NVM

Both GAA Nanowire and Nanosheet architectures offer compelling benefits for NVM applications, but they cater to different priorities:

- **GAA Nanowires (NW):** Ideal for ultra-scaled, high-density NVM cells due to superior

electrostatic control and simpler fabrication. This makes them a promising choice for deeply scaled technologies below 5 nm, where control over leakage currents is critical.

- **GAA Nanosheets (NS):** Better suited for current and near-future NVM technologies due to their higher drive current, robust variability tolerance, and efficient charge retention, which are essential for high-speed and high-capacity memory cells.

Given the current trend towards higher performance and integration density in NVM, GAA Nanosheets generally offer a more balanced trade-off between manufacturability and performance, making them the more favourable option for mainstream NVM applications.

5.4 Material Selection for GAA in Non-Volatile Memory (NVM) Applications

Material selection plays a pivotal role in defining the electrical, thermal, and mechanical performance of Gate-All-Around Field-Effect Transistors (GAA FETs). These advanced transistors demand materials that not only support high carrier mobility but also offer compatibility with nanoscale fabrication processes and stability under high operating stresses.

Traditional materials such as silicon and silicon-germanium remain widely used due to their proven reliability and integration with existing CMOS platforms [53]. However, to overcome scaling limitations and enhance device functionality, researchers have turned toward emerging materials like graphene, transition metal dichalcogenides (TMDs), and semiconductor nanowires, which provide superior electrostatic control and reduced short-channel effects.

The selection of suitable materials is therefore fundamental to achieving the desired electrical characteristics and ensuring the long-term viability of GAA FET technology.

Table 5.2: Material Selection for GAA in NVM Applications

Category	**Material**	**Key Characteristics**
Established Materials	Silicon (Si) [18, 93, 190]	Bandgap: ∼1.12 eV – suitable for low leakage and good off-state behavior. Carrier Mobility: 1900 $cm^2/V{\cdot}s$ (n-type) – adequate for general-purpose electronics. Scalability: High – highly compatible with advanced CMOS scaling. Thermal Conductivity: 150 W/m·K – excellent for heat dissipation. NVM Suitability: High – widely used in existing NVM technologies.
	Germanium [128, 27, 193]	Bandgap: ∼0.66 eV. Carrier Mobility: ∼3900 $cm^2/V{\cdot}s$ (n-type) – excellent charge transport. Scalability: Moderate – some integration limitations. Thermal Conductivity: ∼60 W/m·K – decent heat dissipation. NVM Suitability: Moderate – fair compatibility.
	Silicon-Germanium (SiGe) [59, 157, 28]	Bandgap: 0.66–1.12 eV – tunable for performance and leakage trade-offs. Carrier Mobility: 1000–2000 $cm^2/V{\cdot}s$ – faster than silicon. Scalability: High – CMOS compatible. Thermal Conductivity: 20–60 W/m·K – moderate, varies with Ge content. NVM Suitability: High – versatile for memory structures.
Emerging Materials	III-V Semiconductors [148]	High electron mobility ideal for high-speed, low-power use.
	Graphene [148]	High conductivity, excellent mechanical strength – promising for future devices.
	TMDs [148]	Atomically thin, direct bandgap, and good electrostatic control.

From the comparative analysis of established and emerging materials, Silicon (Si) remains the foundational choice for GAA FETs due to its high scalability, robust thermal conductivity, and mature integration with CMOS technologies, making it ideal for mainstream applications and non-volatile memory (NVM).

Germanium (Ge) and Silicon-Germanium (SiGe) offer higher carrier mobility than silicon, making them suitable for performance-critical applications. SiGe presents a balanced trade-off between performance and manufacturability, with high scalability and tunable bandgap, positioning it as a strong complementary material for next-generation transistors.

III-V semiconductors offer superior electron mobility, making them ideal for high-speed and low-power applications, although their integration challenges persist.

Among emerging materials, Graphene and TMDs (e.g., MoS_2) stand out for their excellent electrical properties and atomic-scale thickness, providing enhanced electrostatic control. However, their use in commercial-scale GAA FETs remains experimental, requiring further research for reliable and reproducible integration.

In conclusion, Si and SiGe currently offer the best combination of performance, scalability, and

process maturity for GAA FET integration, while Ge, III-Vs, and 2D materials hold significant promise for specialized or future-oriented applications.

5.5 Comparison of Nanowire and Nanosheet Fabrication for GAA NVM

The selection of an appropriate fabrication method for these nanoscale structures is crucial, as it significantly influences their electrical characteristics, manufacturability, and overall device performance. In this chapter, we present a systematic comparison of various fabrication techniques for nanowires and nanosheets, outlining their respective advantages and disadvantages, to determine the most effective approaches for GAA-based NVM applications.

Table 5.3: Comparative Analysis of Fabrication Techniques for GAA-Based Nanowire and Nanosheet Structures (Part 1)

Fabrication Method	**Material**	**Advantages**	**Disadvantages**
Vapor-Liquid-Solid (VLS) Growth [101]	Nanowires	Widely used for high-volume production, applicable to various materials (e.g., Si, III-V semiconductors), predictable growth, high aspect ratios.	Contamination risk (e.g., Au), instability at high temperatures, diameter control issues, requires precise control over temperature, pressure, and feedstock composition.
Electrospinning [54, 152]	Nanowires	Simple, scalable, cost-effective, and high throughput.	Limited material compatibility, lower structural uniformity.
Chemical Vapor Deposition (CVD) [86]	Both	High quality, scalable, good morphology control.	High cost, complex setup, lower deposition rate.
Top-Down Lithography (e.g., Photolithography, Electron Beam Lithography) [25, 158, 105]	Both	High precision, CMOS compatible.	Expensive, time-consuming, limited scalability.
Reactive Ion Etching (RIE) [76, 115, 140]	Both	High aspect ratio, good dimensional control.	High equipment cost, sidewall roughness.
Metal-Assisted Chemical Etching (MACE) [83]	Both	Large-scale production, relatively low cost, room temperature operation, high aspect ratio and density, CMOS compatible, flexible geometries.	Metal contamination, surface roughness, diameter control difficulty, dendrite and pore formation.

Table 5.4: Comparative Analysis of Fabrication Techniques for GAA-Based Nanowire and Nanosheet Structures (Part 2)

Fabrication Method	Material	Advantages	Disadvantages
Molecular Beam Epitaxy (MBE) [50]	Both	High purity, atomic precision, excellent growth control.	Very complex, extremely slow, expensive.
Laser Ablation [86]	Nanowires	High material purity, simple operation, excellent control over growth parameters and composition.	Requires costly equipment, slow growth rate.
Sol-Gel Method[71, 31]	Both	High product purity, simple, cost-effective.	Complex drying, long processing time, limited scalability, contamination sensitive.

For GAA-based NVM, **VLS Growth** is ideal for nanowire structures due to its scalability and control over high aspect ratios, while **CVD** is preferred for nanosheet structures because of its superior film quality and scalability. However, the choice ultimately depends on the specific application, cost considerations, and the required device dimensions.

5.6 Physical Design Considerations for GAA-Based Non-Volatile Memory (NVM)

Gate-All-Around (GAA) architectures have emerged as a promising solution for extending Moore's Law, particularly in advanced memory applications. For non-volatile memory (NVM), where data retention, write/read efficiency, and device reliability are critical, GAA FETs provide superior electrostatic control and scalability. However, the performance and reliability of GAA-based NVMs are significantly influenced by physical dimensions such as nanowire diameter, nanosheet thickness, and nanosheet width. The following sections discuss how each of these factors affects NVM performance and recommend optimal ranges for design.

5.6.1 Nanowire Diameter and Its Impact on NVM Performance

The diameter of nanowires in GAA-based NVM structures plays a key role in dictating charge confinement, programming speed, and overall reliability. A careful trade-off exists between quantum effects and electron transport efficiency.

Table 5.5: Impact of Nanowire Diameter on NVM Performance

Diameter	Impact on NVM Performance
<10 nm [39, 151]	Improved programming speed and retention time due to stronger quantum confinement effects. Increased surface scattering causing reduced electron mobility.
>10 nm [168]	Parasitic capacitance decreases. Lower drive current. Lower retention and endurance. Reduced quantum confinement results in leakage current.

Sub-10nm technology nodes offer superior retention and programming speed due to enhanced quantum confinement effects, making them highly suitable for reliable non-volatile memory (NVM) performance. However, these benefits come at the cost of reduced electron mobility from increased surface scattering and greater fabrication complexity. On the other hand, nodes larger than 10nm help alleviate some physical limitations such as parasitic capacitance but suffer from lower data retention, endurance, and increased leakage current due to diminished quantum effects. Therefore, the optimal technology node for NVM lies around the 10nm range, where a balance is achieved between quantum confinement benefits, manufacturability, and manageable parasitic and mobility-related trade-offs.

5.6.2 Nanosheet Thickness and Its Impact on NVM Performance

Nanosheet thickness in GAA FETs significantly influences electrostatic control, switching efficiency, and long-term data integrity. Thickness optimization is necessary to meet the performance and scaling demands of modern NVM devices.

Table 5.6: Impact of Channel Thickness on NVM Suitability

Thickness	Characteristics	Suitability for NVM
2–5 nm [91]	Quantum confinement leads to severe performance loss, reliability degradation, degraded subthreshold swing (SS), and increased charge trapping sensitivity.	Low – Reliability concerns
5–10 nm [91]	Balances switching efficiency, write/read speed, and reliability.	High – Recommended range
10–15 nm [91]	Weaker electrostatic control, poor SS, suboptimal scaling.	Moderate – Trade-offs involved

For non-volatile memory (NVM) applications, device reliability, data retention, and scalability are paramount. Among the various physical parameters influencing device behaviour, nanosheet thickness plays a critical role in determining electrostatic control, charge confinement, switching efficiency, and long-term reliability.

Empirical studies and simulation data consistently demonstrate that a thickness range between 5 nm and 10 nm is optimal for NVM applications. This range provides a balanced trade-off across multiple key performance metrics:

- **Reliable Operation:** Devices in the 5–10 nm range show reduced susceptibility to charge trapping and variability compared to thinner (2–5 nm) structures, which suffer from quantum confinement effects that can degrade device stability and performance.
- **Good Data Retention:** Adequate physical separation and barrier height are maintained in this thickness range, enhancing charge storage capabilities and retention times—both of which are critical for memory devices.
- **Enhanced Electrostatic Control:** Compared to thicker structures (>10 nm), the 5–10 nm range offers superior gate control over the channel, resulting in better subthreshold swing (SS) and reduced short-channel effects (SCEs), which are essential for scaling down NVM cell dimensions.
- **Scalability:** This thickness range aligns well with sub-7 nm technology nodes, allowing for the continued miniaturization of memory arrays without compromising performance or increasing power consumption drastically.
- **Optimal Switching Characteristics:** Devices within this range achieve fast and efficient write/read cycles, which are essential for high-performance and low-latency memory applications, while still mitigating the reliability concerns that plague thinner implementations.

In contrast, nanosheets with thicknesses below 5 nm encounter significant drawbacks such as quantum confinement-induced degradation, elevated gate leakage, and increased variability. On the other end, thicknesses above 10 nm compromise the electrostatic integrity and lead to increased off-state leakage and weaker gate control, which are detrimental in densely packed NVM architectures.

Conclusion: Targeting a **5–10 nm** nanosheet thickness provides the most effective compromise between performance, reliability, and manufacturability, making it the most suitable design window for advanced NVM applications in emerging technology nodes.

5.6.3 Nanosheet Width and Its Impact on NVM Performance

Table 5.7: Impact of Nanosheet Width on NVM Performance

Nanosheet Width Range	**Structural Characteristics**	**Impact on NVM Performance**	**Suitability for NVM**
<10 nm [91, 82]	Ultra-thin. High surface-to-volume ratio. Increased surface states.	Enhanced quantum confinement. Potential for higher charge storage density. Increased susceptibility to surface defects and oxidation.	Moderate to High
10–50 nm [91, 108, 53]	Balanced thickness. Improved structural stability.	Lower leakage, better threshold stability, and superior subthreshold performance—essential for reliable data retention and switching.	High
>50 nm [91, 108, 53]	Thicker sheets. Reduced surface-to-volume ratio.	Excessive leakage, degraded threshold control, and poor subthreshold performance, which compromise data retention and reliability.	Low

Based on the nanosheet width-dependent structural and electrical characteristics, the 10–50nm range emerges as the optimal choice for NVM applications, striking a balance between structural stability and electronic performance. Ultra-thin nanosheets (<10nm) offer potential benefits like higher charge storage but suffer from reliability concerns due to surface effects. Conversely, widths >50nm lead to excessive leakage and poor threshold control, making them unsuitable for reliable memory retention. Therefore, nanosheet widths in the **10–50nm** range are best suited for high-performance and reliable NVM design.

5.7 Conclusion

The evolution of Gate-All-Around (GAA) transistors represents a pivotal advancement in enabling high-performance, scalable, and energy-efficient non-volatile memory (NVM) technologies. This chapter has explored the integration of SONOS and FeFET architectures within GAA frameworks, highlighting their fabrication processes and performance-critical design considerations.

From the detailed fabrication flows of GAA-based SONOS and FeFET devices to material and structural optimization—such as nanowire diameter, nanosheet thickness, and width—it is clear that careful physical and material engineering is crucial for achieving reliable data storage, fast switching, and long retention. Among GAA architectures, nanosheet structures offer higher drive current and are generally preferred for mainstream NVM applications, while nanowires provide superior electrostatic control, making them suitable for ultra-scaled nodes.

Material selection also plays a defining role, with silicon and silicon-germanium remaining the most practical choices due to their CMOS compatibility, while emerging materials like graphene and TMDs offer future potential.

In conclusion, the synergy between advanced GAA structures and embedded memory technologies like SONOS and FeFET presents a viable pathway toward next-generation NVM solutions. By optimizing fabrication techniques, material choices, and physical dimensions, GAA-based

NVM can meet the increasing demands for speed, density, and energy efficiency in future computing systems.

Chapter 6

Conclusion and Comparative Analysis

This thesis explores technologies like ferro-electric based NVM, GAAFET based NVM, resistive switching based NVM and CNT based NVM analyzing their mechanism and potential to replace traditional memory technology. These technologies are highly scalable, energy efficient and compatible with the existing fabrication process. The exploration of emerging non-volatile memory (NVM) technologies reveals a dynamic and rapidly advancing field driven by the need for faster, denser, and more energy-efficient data storage solutions.
The exploration of emerging non-volatile memory (NVM) technologies reveals a dynamic and rapidly advancing field driven by the need for faster, denser, and more energy-efficient data storage solutions. Each of the technologies discussed—FeFET, ReRAM, CNT-NRAM, and GAA-based NVM architectures—brings unique advantages and faces specific challenges.

Ferroelectric Field-Effect Transistors (FeFETs) stand out for their CMOS compatibility and excellent scalability, leveraging hafnium oxide's ferroelectric properties. ReRAM distinguishes itself with a simple structure and broad tunability in performance via switching mechanisms and material choices. CNT-NRAM offers unmatched speed and mechanical stability, harnessing the superior properties of carbon nanotubes for ultra-fast and low-power operation. GAA-based NVM architectures, meanwhile, represent a future-forward approach to physical transistor scaling, optimizing electrostatics and enabling robust integration with next-generation memory like SONOS and FeFETs.

As research continues to refine materials, interfaces, and fabrication techniques, these technologies are poised to significantly reshape the memory landscape. Each serves different niches in computing—from AI and neuromorphic systems to high-density storage and mobile applications.Below is a comparative summary of these NVM technologies:

Technology	Endurance (Cycles)	Retention	CMOS Compatibility	Fabrication Complexity	Power Consumption
FeFET	10^5–10^7 (refer to Chapter 2)	≥10 years [57, 90]	Excellent	Moderate: requires ferroelectric HfO_2 deposition and careful IL control	Ultra Low [145]
ReRAM	10^{10} [24]	10 years (refer to Chapter 3)	Good	Relatively simple due to MIM structure	Low [65, 48]
NRAM	$\sim 10^{12}$–10^{15} [136, 96, 45]	>300 years (even at +300°C) [45]	Potentially CMOS compatible (still emerging) [96]	Complex: carbon nanotube uniformity needed	Low
GAA-based NVM [23, 142]	10^4–10^5	>10 years	Good (all-silicon process)	Moderate	Low to Moderate

Table 6.1: Comparative Summary of Emerging NVM Technologies

Conclusion: ReRAM is the Most Promising NVM Technology

After a thorough analysis of key emerging NVM candidates—FeFET, ReRAM, NRAM, and GAA-based NVMs—based on metrics such as endurance, retention, CMOS compatibility, fabrication complexity, and power consumption, ReRAM emerges as the most balanced and promising solution for future memory integration.

Exceptional Endurance and Retention
ReRAM stands out with endurance of 10^{10} cycles, significantly higher than FeFET (10^5–10^7) and GAA-based NVMs (10^4–10^5), and competitively close to NRAM ($\sim 10^{12}$–10^{15}). Its data retention of over 10 years ensures reliable long-term storage, meeting and exceeding industrial standards for persistent memory.

Simple and Scalable Fabrication
ReRAM benefits from a relatively simple Metal-Insulator-Metal (MIM) structure, requiring fewer lithography and alignment steps compared to the more complex CNT-NRAM (requiring carbon nanotube synthesis and alignment) and GAA NVMs (which demand advanced nanosheet/nanowire fabrication). This makes ReRAM cost-effective and scalable for mass production.

Low Power and Good CMOS Compatibility
ReRAM consumes low power during both read and write operations—making it ideal for energy-sensitive applications like IoT and mobile. It also demonstrates good CMOS compatibility, facilitating integration into existing semiconductor manufacturing flows without extensive changes.

Maturity and Commercial Momentum
Unlike NRAM (still emerging) or GAA-based NVMs (more academic at present), ReRAM has already seen prototypes and early commercialization, indicating greater technical maturity and a clearer path to adoption.

While FeFET offers ultra-low power and CMOS compatibility, its limited endurance and complex IL management limit scalability. NRAM is highly promising but suffers from fabrication challenges due to nanotube alignment. GAA-based NVMs offer innovation in structure but are not yet as proven.

ReRAM strikes the optimal balance across all critical parameters—performance, manufacturability, integration readiness, and longevity—making it the most promising and practical NVM technology among current contenders.

6.1 Future Work

This thesis offers a thorough exploration of cutting-edge non-volatile memory (NVM) technologies—including FeFET, ReRAM, CNT-NRAM, and GAA-based NVMs—examining how they're made, the materials involved, and their potential impact on memory architecture. By comparing these emerging technologies, we lay the groundwork for the next logical step: shifting from theoretical research to hands-on experimentation and real-world implementation of hybrid memory systems.

One particularly exciting avenue for future work is the development of *heterogeneous memory architectures*—integrating multiple NVM technologies into a single memory hierarchy or even a single chip. Instead of depending on just one type of NVM to deliver all the desired performance, endurance, and efficiency, this approach would combine the unique strengths of different memory technologies. For example, some might excel in speed, others in density or energy efficiency, and blending them could unlock new possibilities for computing systems.

This direction not only builds on the insights from this review but also opens doors to more adaptable, high-performance memory solutions for tomorrow's applications.

Each of the emerging non-volatile memory (NVM) technologies we've studied brings something special to the table:

- **FeFETs** shine with their CMOS compatibility and ultra-low power consumption, making them a natural fit for embedded systems and energy-efficient designs.
- **ReRAM** stands out with its high endurance (surviving millions of write cycles) and simple metal-insulator-metal (MIM) structure, which keeps fabrication straightforward.
- **CNT-NRAM** boasts blazing-fast speeds and exceptional long-term data retention, ideal for applications where performance and reliability are critical.
- **GAA-SONOS** offers superior scalability and high integration density, paving the way for next-gen ultra-compact memory solutions.

Rather than forcing one technology to do it all, the real magic happens when we combine them intelligently. Imagine:

- Layered stacks where different NVMs complement each other in a single structure.
- Hierarchical tiers that assign the right memory type to the right task—like fast CNT-NRAM for cache and high-density GAA-SONOS for storage.
- Application-specific zones where ReRAM handles frequent writes, while FeFETs manage low-power standby modes.

This hybrid approach lets us balance speed, power, endurance, and density in ways no single NVM could achieve alone. It's not just about picking the best memory—it's about orchestrating them to unlock new possibilities in computing.

While this study is rooted in theoretical analysis, its real value lies in paving the way for hands-on innovation. By synthesizing insights on fabrication methods, material behaviors, and architectural trade-offs, we've created a practical roadmap for the next era of memory technology.

The future of NVMs is about smart integration. Whether through hybrid memory arrays, tiered architectures, or application-specific designs, the goal is clear: real-world solutions that balance speed, power, density, and reliability.

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