Politecnico di Torino

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Design of a Signal Acquisition System for Local Field Potentials (LFPs)

Master's Thesis

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To my grandparents, Romano and Luciana,
born in the Piedmont countryside during the war years
and later becoming entrepreneurs in the 1970s,
whose commitment, trust,
hard work, love, and sacrifice
granted me such an important achievement
and have loved me immensely every day of my life.

Abstract in Italiano

Questa tesi tratta lo sviluppo e la valutazione delle prestazioni di un sistema di acquisizione di segnali a basso consumo progettato esclusivamente per la registrazione neurale periferica in vivo, sfruttando il SoC nRF5340 di Nordic Semiconductor. L'obiettivo principale è valutare se il convertitore analogico-digitale a registrazione successiva (SAADC) integrato potesse essere adattato per la registrazione dei Potenziali di Campo Locale (LFP). Nello specifico, l'ADC dovrebbe essere in grado di campionare accuratamente segnali nell'ordine delle centinaia di microvolt, con una larghezza di banda compresa tra 250 e 500 Hz, garantendo l'integrità del segnale per applicazioni neuroscientifiche. Per validare il sistema di acquisizione per questa applicazione, l'ADC periferico è stato programmato con una frequenza di campionamento massima di 1 kHz, mentre i dati differenziali acquisiti dalla scheda di sviluppo sono stati memorizzati in tempo reale su una microSD esterna, formattata con il file system FAT, e comunicavano con il SoC tramite un protocollo SPI a 8 MHz. I test hanno rivelato diverse sfide relative alla capacità del sistema di catturare segnali a bassa ampiezza e registrare accuratamente specifiche gamme di frequenza, evidenziando la necessità di un ADC esterno dedicato per gestire efficacemente questi segnali. I futuri miglioramenti si concentreranno anche sull'aumento dell'affidabilità del sistema attraverso ottimizzazioni nella programmazione dello scheduler.

Abstract in English

This dissertation explores the feasibility of a low-power signal acquisition system designed exclusively for in-vivo peripheral neural recordings, leveraging the nRF5340 SoC from Nordic Semiconductor. The primary objective was to assess whether the on-chip Successive Approximation Register Analog-to-Digital Converter (SAADC) could be adapted for Local Field Potential (LFP) recordings. Specifically, the ADC should be capable of accurately sampling signals in the hundred-microvolt range, with a frequency bandwidth between 250 and 500 Hz, ensuring signal integrity for neuroscientific applications. To validate the acquisition system for this application, the peripheral ADC was programmed with a maximum sampling frequency of 1 kHz, while the differential data acquired from the development board was stored in real time on an external microSD card, formatted with the FAT file system, and communicated with the SoC via an 8 MHz SPI protocol. Tests revealed several challenges related to the system's ability to capture low-amplitude signals and accurately record specific frequency ranges, highlighting the necessity of an external dedicated ADC to effectively handle these signals. Future improvements will also focus on enhancing the system's reliability through optimized scheduler programming.

Chapter 1

Introduction

1.1 The Nervous System: Structure and Function

The nervous system is a complex network of organs and specialized cells responsible for receiving, processing, and transmitting stimuli to regulate physiological functions and behavioral responses. It is divided into the central nervous system (CNS) and the peripheral nervous system (PNS) (Figure 1.1).

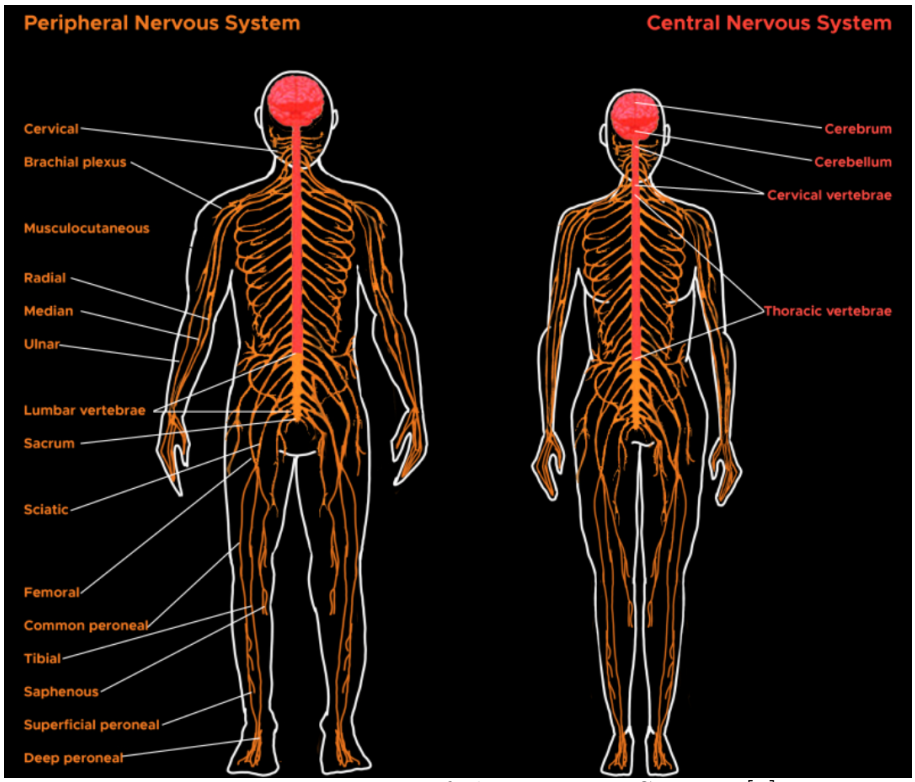

Figure 1.1: Diagram of the Nervous System [1]

The CNS, consisting of the brain and spinal cord, is responsible for processing sensory input, coordinating motor responses and regulating cognitive functions. The brain, enclosed within the skull, is composed of the cerebrum, cerebellum, and medulla oblongata, and it governs sensory perception, motor control, emotions,

communication and memory (Figure 1.2). The brain can be easily damaged and it is protected by the skull, meninges, and cerebrospinal fluid. In addition, the blood-brain barrier acts as a selective permeability system, preventing harmful substances and pathogens from entering the brain while allowing essential nutrients to pass through [1]. The cerebrum, the largest part of the brain, is divided into the right and left hemispheres, which are connected by the corpus callosum and are responsible for higher cognitive functions such as reasoning, memory, and learning. The cerebellum plays a very important role in maintaining balance and coordinating movements, while the medulla oblongata regulates vital autonomic functions, including respiration and heart rate. While the CNS is primarily involved in processing and integrating neural information, it cannot function all by itself. The PNS ensures communication between the CNS and the rest of the body, enabling coordinated responses to internal and external stimuli. It acts as a conduit between the CNS and peripheral tissues and it is divided into the somatic nervous system (SNS) and the autonomic nervous system (ANS). The SNS governs voluntary movements, while the ANS regulates involuntary physiological processes and it is further divided into the sympathetic nervous system (SNS) and the parasympathetic nervous system (PSNS). The first one prepares the body for stress-related responses, which is known as fight-or-flight response, and the last one promotes relaxation and homeostasis, supporting the rest-and-digest mechanism. Both the sympathetic and parasympathetic nervous systems contain afferent fibers, which deliver sensory information to the central nervous system, and efferent fibers, responsible for transmitting motor commands to target organs. These motor pathways typically consist of two neurons in series: a preganglionic neuron, with its cell body in the CNS, and a postganglionic neuron in the periphery that innervates the target tissues [2]. Neurons, the fundamental units of the nervous system, are specialized cells that transmit electrical and chemical signals through synaptic connections. Each neuron consists of a cell body called soma, dendrites, which receive incoming signals, and a single axon, which propagates impulses to other neurons, muscles, or glands. The human brain contains approximately 86 billion neurons that communicate through a combination of electrical and electrochemical signals. Neurons establish synaptic connections that can vary from just a few to hundreds of thousands. These connections can be estabilished with nearby or distant neurons, and in some cases, even with the neuron itself. Each synapse is composed of a presynaptic and a postsynaptic terminal, where neurotransmitters are released and received, facilitating neural communication [3]. This complex network plays a fundamental role in regulating essential physiological functions and adapting to environmental changes. A complete understanding of the nervous system structure and function is essential for the study of neural signals, including Local Field Potentials (LFPs).

1.1.1 The Central Nervous System

The CNS is responsible for processing sensory input such as coordinating motor responses and regulating cognitive functions. It is composed of the brain and spinal cord, which are protected by the skull, vertebral column, cerebrospinal fluid, and meninges. The brain, the most complex organ of the CNS, is divided into several

key regions. The cerebrum, responsible for voluntary movement, sensory processing, learning, and reasoning, is divided into the left and right hemispheres by a deep longitudinal fissure. The two hemispheres remain in contact and communication with one another through the corpus callosum. Each hemisphere is further subdivided into the frontal, parietal, occipital, and temporal lobes, and is characterized by different functions (Figure 1.3)[4].

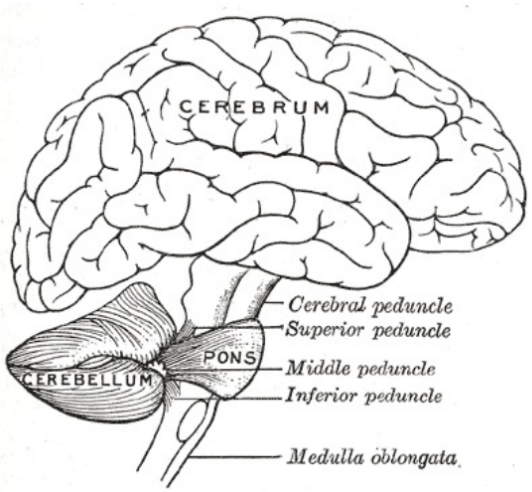

Figure 1.2: The brain showing the cerebellum, pons, and medulla oblongata [10]

The frontal lobe plays an important role in reasoning, decision-making, and motor control in fact a damage to this region can affect social behavior and speech production. For this reason people with frontal lobe damage may struggle to regulate their emotions, interact appropriately with other people or make complex decisions. The parietal lobe processes sensory information. In fact, damage to this part of the brain may make it difficult for an individual to identify a sensation and its location on their body. The temporal lobe plays a crucial role in auditory processing and memory formation; in fact, damage to the right temporal lobe may lead to persistent talking and deficits in nonverbal memory. The occipital lobe is dedicated to visual perception, and damage to this lobe may lead to visual defects and the inability to recognize written words [5]. Beneath the cerebrum lies the diencephalon, which includes the thalamus and hypothalamus. The thalamus relays sensory information to the cortex, while the hypothalamus regulates autonomic functions like temperature, hunger, thirst, and endocrine activity. The cerebellum, positioned in the posterior part of the brain, maintains posture, balance, and fine motor coordination by integrating sensory and motor signals. Acting as a bridge between the brain and spinal cord, the brainstem, consisting of the midbrain, pons, and medulla oblongata governs vital functions like respiration, heart rate, and reflexes. The medulla oblongata, in particular, is responsible for regulating involuntary processes such as breathing, blood pressure, and digestion.

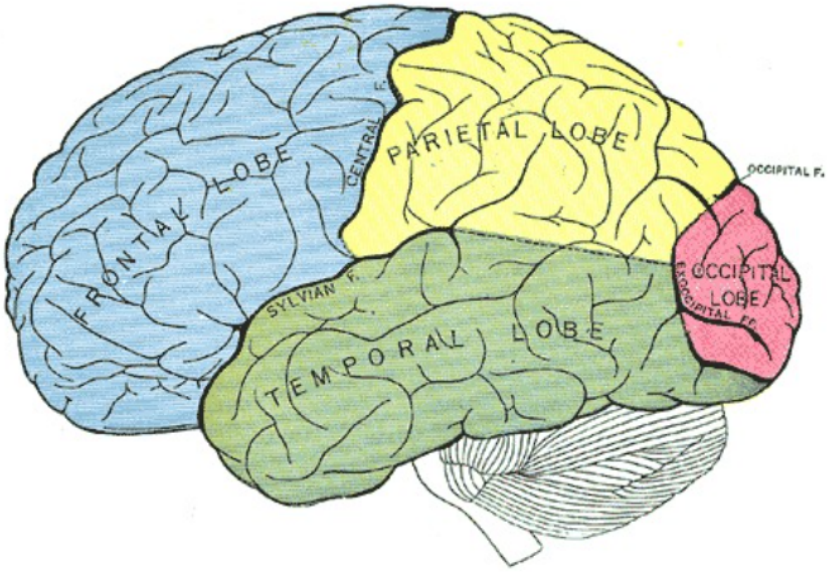

Figure 1.3: The cerebrum and its lobes [6]

A good understanding of the structural and functional components of the CNS provides the necessary foundation for analyzing neural signals, such as LFPs, which constitute the primary focus of this study. The brain and spinal cord are protected by three layers of membrane collectively known as the meninges (Figure 1.4), with the cranial meninges specifically referring to the section that covers the brain. From the external to the internal layer, the three layers are the dura mater, arachnoid mater, and pia mater. The dura mater is composed of dense connective tissue and is attached to the inner surface of the skull and vertebrae. The arachnoid mater is a thin, delicate membrane located beneath the dura mater and above the pia mater. The pia mater is an even thinner, transparent layer that closely follows the surface of the brain and spinal cord. These layers create three key spaces: the epidural, subdural, and subarachnoid spaces, from the outermost to the innermost. The main function of the meninges is to protect the contents of the brain and spinal cord [7].

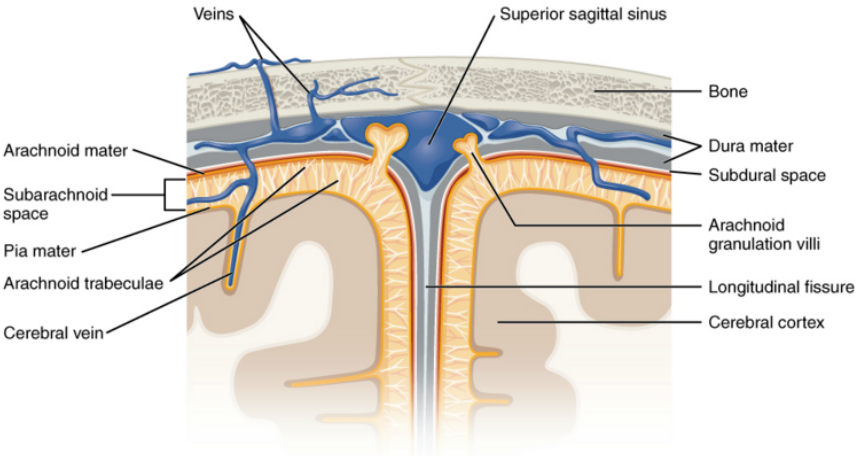

Figure 1.4: The meninges and their protective layers [7]

1.1.2 The Spinal Cord and Reflexes

The spinal cord serves as the primary communication channel between the brain and the peripheral nervous system, facilitating the transmission of sensory information to the brain and motor commands to the muscles. It is structurally segmented, with each section corresponding to specific motor and sensory functions. The spinal cord is a long, cylindrical structure that continues from the lower part of the brainstem, specifically the medulla oblongata. In adults, it extends from the first cervical vertebra to the first lumbar vertebra, while in young children, it reaches up to the upper part of the third lumbar vertebra because their vertebral column is shorter. Like the brain, the spinal cord is delicate and protected by the vertebrae, which form the spinal column. It contains millions of neurons, whose fibers create pathways that carry signals up and down. The spinal cord is surrounded by three meninges and cushioned by cerebrospinal fluid (CSF) in the subarachnoid space [8]. A fundamental function of the spinal cord is the mediation of reflex arcs, which enable rapid and automatic responses to external stimuli. Reflex arcs involve three types of neurons that operate in a highly coordinated manner: sensory neurons, which detect stimuli and transmit signals to the spinal cord; interneurons, which process and relay the information; and motor neurons, which generate the appropriate response by activating the relevant muscles. This coordination ensures that reactions to stimuli are immediate and precise, minimizing potential harm to the body. A classic example is the withdrawal reflex: when an individual touches a hot object, the sensory neuron transmits a signal directly to the spinal cord, bypassing the brain. The spinal cord, in turn, activates the motor neuron, triggering an immediate withdrawal of the hand (Figure 1.5). The analysis of neural signals within the spinal cord, particularly Local Field Potentials (LFPs), provides valuable insights into the coordination and regulation of reflex arcs, which is directly relevant to this study. In addition to enabling quick reflexes, the spinal cord is essential for processing and transmitting neural signals, ensuring smooth communication within the nervous system.

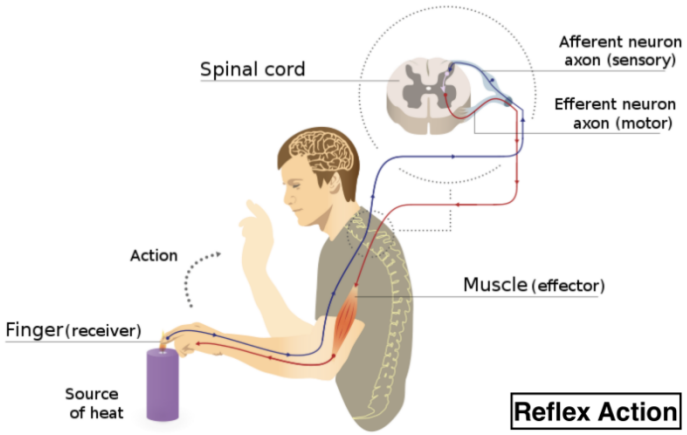

Figure 1.5: Diagram of the spinal cord and the reflex arc [9]

1.1.3 The Neuron and the Synapse

Neurons, the fundamental units of the nervous system, are specialized in transmitting nerve impulses. Each neuron comprises three main components: the cell

body, which contains the nucleus and integrates incoming signals; dendrites, which receive signals from other neurons and transmit them toward the cell body; and the axon, a long projection that propagates impulses to other neurons, muscles, or glands (Figure 1.6). Neuronal communication occurs at synapses, where chemical or electrical signals are transmitted. When an action potential reaches the axon terminal, neurotransmitters are released into the microscopic gap between neurons called the synaptic cleft. These neurotransmitters bind to specific receptors on the dendrites of the postsynaptic neuron, facilitating signal transmission and if the signal reaches the threshold, a new action potential is generated in the postsynaptic neuron, propagating the neural impulse further. Neurotransmitters are endogenous chemicals that allow neurons to communicate with each other throughout the body and they enable the brain to perform a variety of functions through the process of chemical synaptic transmission. Chemical synaptic transmission mainly involves the release of neurotransmitters from presynaptic neurons to receptors on the postsynaptic cell. Imbalances in specific neurotransmitters have been linked to various neurological disorders, such as Parkinson's disease, schizophrenia, depression, and Alzheimer's disease [10]. The intricate communication between neurons through synaptic transmission generates measurable electrical signals, such as LFPs, which provide valuable insights into the coordinated activity of neural networks and their functional dynamics. Neurons are classified based on their function: sensory neurons transmit signals from sensory receptors to the CNS; motor neurons convey signals from the CNS to muscles and glands; and interneurons establish connections between sensory and motor neurons, facilitating complex reflexes and information processing. Thus, neurons and their synaptic interactions constitute the foundation of neural communication, enabling the intricate processes underlying both voluntary and involuntary functions of the nervous system.

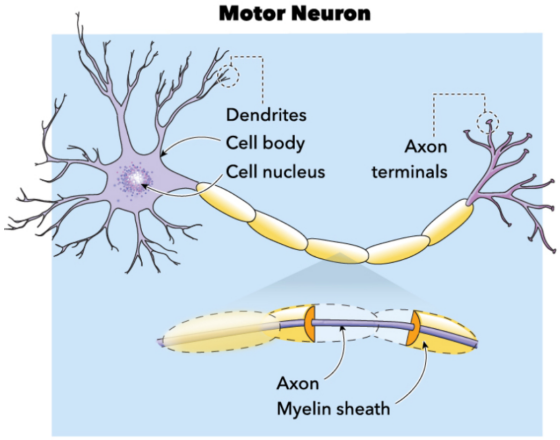

Figure 1.6: Diagram of a motor neuron, illustrating the cell body, dendrites, axon, myelin sheath, and axon terminals [11]

1.1.4 The Peripheral Nervous System

The PNS includes all neural structures outside the CNS and serves as the primary communication link between the CNS and the rest of the body and consists of cranial nerves, spinal nerves, and their associated ganglia. Cranial nerves emerge directly

from the brain and control sensory and motor functions, such as vision, hearing, smell, and facial movement. On the other hand, spinal nerves originate from the spinal cord and facilitate the transmission of motor commands and sensory information between the CNS and peripheral structures. The primary function of the PNS is to transmit sensory and motor signals, enabling both voluntary and involuntary bodily processes. Ganglia, located along spinal and cranial nerves, serve as critical processing centers for sensory and motor information, ensuring efficient communication between the CNS and peripheral structures. The PNS is divided into the SNS and ANS. The SNS controls voluntary movements and sensory perception. It includes motor neurons that activate skeletal muscles and sensory neurons that send information from the skin, muscles, and joints to the CNS. The SNS also plays a role in reflex arcs, allowing quick and automatic reactions to stimuli. This system enables precise movements, such as reaching for an object or walking, by directly controlling skeletal muscles. In contrast, the ANS regulates involuntary physiological functions, including heart rate, digestion, and respiration. It is further subdivided into the sympathetic nervous system, which prepares the body for stress-related activities, and the parasympathetic nervous system, which promotes relaxation and energy conservation. The ANS controls unconscious and involuntary functions essential for maintaining body homeostasis. These functions are crucial for survival and help us adapt to different environments. While the endocrine system regulates long-lasting processes, the ANS acts quickly with short-term effects. It controls various functions, including blood circulation by regulating heart rate and blood pressure, temperature regulation through sweating and shivering, digestion by coordinating the gut and glands, urinary movement, and eye functions such as pupil adjustment and tear production [12].
The role of the PNS in transmitting neural signals from sensory receptors to the CNS is fundamental for understanding the electrical activity underlying LFPs. The PNS plays an important role in relaying sensory input that contributes to the generation of LFPs, which reflect the collective electrical activity of neural populations. These signals are essential for investigating neural communication and function within the peripheral nervous system. Collectively, the components of the PNS enable adaptive responses to external stimuli and internal physiological demands, maintaining homeostasis and supporting the precise coordination of bodily functions.

1.2 Local Field Potential (LFPs)

1.2.1 Introduction to Local Field Potentials (LFPs)

Local Field Potentials (LFPs) are electrical signals that come from the activity of groups of neurons in a specific area of the nervous system. Unlike action potentials, which are fast spikes from single neurons, LFPs represent the slower and more synchronized activity of the brain. They are influenced by neural network dynamics and can be recorded for long periods to study different brain regions. These signals are useful for understanding how neurons interact and how brain activity is organized. LFPs show characteristic oscillations at different frequency bands, such as delta, theta, alpha, beta, and gamma. Each of these bands is linked to specific cognitive

and motor functions. LFPs can be broken down into separate oscillatory components, called oscillons, which reflect structured patterns of neural synchronization. In the hippocampus, for example, LFPs usually show one main theta-band oscillon and several gamma-band oscillons, suggesting that each frequency range has a distinct role [13]. To measure LFPs, neural electrodes are placed near brain tissue to capture extracellular signals. These recordings help researchers analyze neural activity at a level between single neurons and whole-brain imaging techniques like functional MRI (fMRI). LFPs are valuable because they provide high spatial resolution and can detect rapid changes in neural activity, making them important for studying neurological disorders. That's why LFP recordings are widely used in both neuroscience research and clinical studies. They reflect the combined effects of excitatory and inhibitory synaptic inputs on neurons in a specific brain region. In the cortex, LFPs are linked to sensory processing, decision-making, and motor planning. In the hippocampus, they play a crucial role in memory formation and spatial navigation, often showing theta and gamma oscillations. In the basal ganglia, LFPs are studied in movement disorders like Parkinson's disease, where excessive beta oscillations are often seen. Similarly, thalamic LFPs show both slow-wave activity and gamma oscillations, which are related to sleep regulation and sensory processing. The different oscillation patterns across brain regions highlight their specific roles in neural function (Figure 1.7).

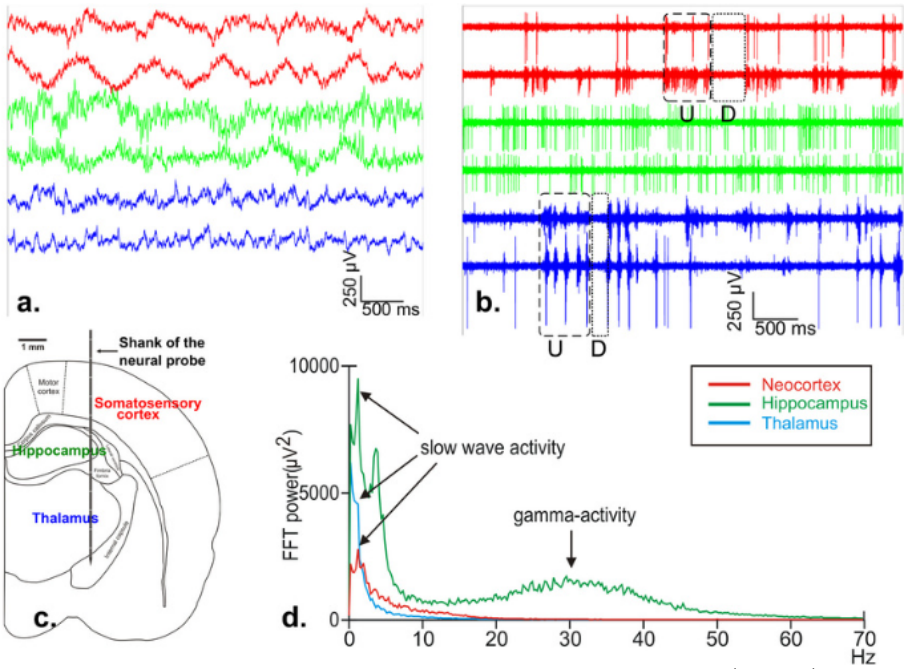

Figure 1.7: Simultaneous recordings of Local Field Potentials (LFPs) from the neocortex, hippocampus, and thalamus, illustrating differences in oscillatory activity across brain regions [14]

LFPs display rhythmic activity at different frequency bands, each linked to a specific brain function. Delta waves are mainly involved in deep sleep and slow-wave activity, while theta rhythms play a role in learning, memory, and navigation. Alpha waves are connected to states of attention and relaxation, whereas beta oscillations

are related to motor control and cognitive processes. Gamma frequencies are important for sensory processing, attention, and more complex cognitive tasks (Table 1.1). Besides these common frequency bands, there are also high-frequency oscillations (100–500 Hz) and unitary spikes (>500 Hz), which are particularly useful for studying fast neural activity and conditions like epilepsy.

Frequency Band	**Range (Hz)**	**Functional Associations**
Delta	0.5–4	Deep sleep, slow-wave activity.
Theta	4–8	Learning, memory, navigation.
Alpha	8–12	Attention, relaxation.
Beta	13–30	Motor control, cognitive functions.
Gamma	30–100	Sensory processing, attention, higher-order cognitive functions.
HFOs	100–500	Fast oscillations, epilepsy, neural encoding.
Unitary Spikes	500–3000	Action potentials, neural communication.

Table 1.1: Frequency Bands of Local Field Potentials (LFPs) and Their Functional Associations, including High-Frequency Oscillations (HFOs) and Unitary Spikes.

Studying LFPs helps us understand how neural circuits process information and regulate behavior. These signals are widely used to explore neurological disorders like epilepsy, Parkinson's disease, and Alzheimer's. They also play a key role in brain-computer interfaces, helping decode motor intentions and enabling communication for people with paralysis. Furthermore, the analysis of oscillatory dynamics through LFPs recordings contributes to the development of computational models of brain function. Cerebral LFPs serve as a critical tool for advancing both fundamental neuroscience research and clinical applications, linking microscopic and macroscopic levels of neural activity [15].

1.2.2 Local Field Potentials in the Peripheral Nervous System

Local Field Potentials in the PNS are generated by the combined electrical activity of nerve fibers and synaptic interactions within the peripheral nerves and ganglia. Unlike cerebral LFPs, which mainly reflect cortical oscillations and large scale synaptic inputs, peripheral LFPs mainly capture the synchronized activity of sensory and motor axons. These signals are very important for understanding synaptic transmission, how the nervous system processes information, and how the central and peripheral nervous systems work together. Peripheral LFPs can be recorded using implanted microelectrodes or non-invasive surface electrodes, enabling the measurement of neural activity in both afferent sensory pathways and efferent motor pathways. Sensory LFPs arise from mechanoreceptors, nociceptors, and proprioceptors, transmitting information related to touch, pain, temperature, and muscle proprioception. In contrast, motor LFPs originate from efferent pathways, reflecting neural signals responsible for muscle contractions and autonomic functions. The study of peripheral LFPs is fundamental for understanding neural communication in both physiological and pathological conditions. These recordings are extensively employed in the investigation of neuropathies, chronic pain syndromes, and motor

dysfunctions. Furthermore, they play an important role in intraoperative neurophysiological monitoring, where real-time assessment of nerve integrity enhances surgical outcomes and minimizes the risk of iatrogenic damage. Peripheral LFPs also hold significant importance in neuroprosthetics and neuromodulation. In neuroprosthetic applications, they facilitate the decoding of movement-related neural signals, enabling precise control of prosthetic devices [16]. As shown in Figure 1.8, an analysis of LFPs in response to a stimulation train illustrates sensory and motor pathway activity. In closed-loop neuromodulation systems, peripheral LFPs allow real-time monitoring of neural activity, supporting dynamic adjustments of stimulation parameters to optimize therapeutic efficacy in neurological disorders. By analyzing LFPs in the PNS, researchers can refine diagnostic methodologies, enhance therapeutic interventions, and advance neural interface technologies aimed at improving motor and sensory restoration. These advancements contribute to bridging the gap between the peripheral and central nervous systems, offering a more comprehensive understanding of neural communication pathways.

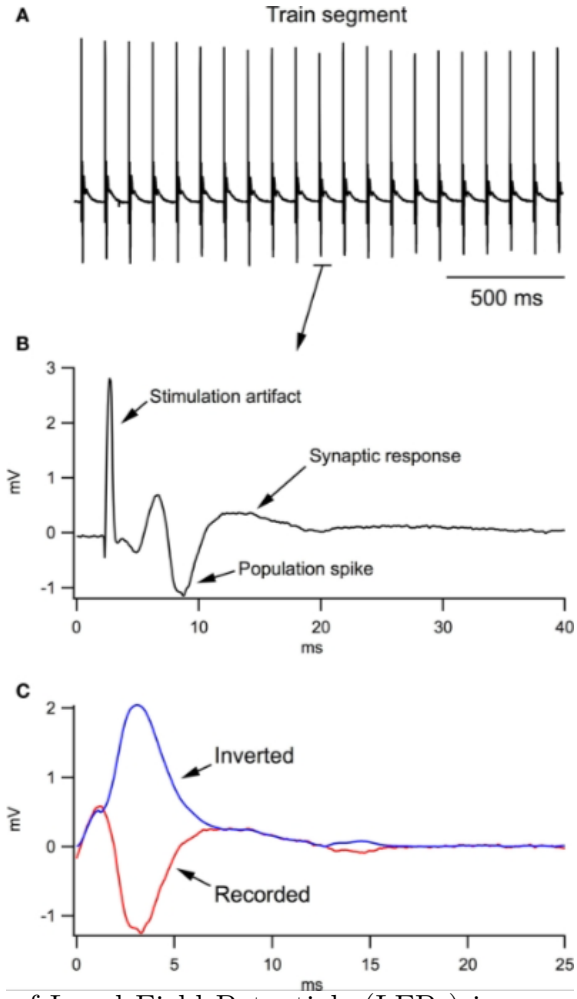

Figure 1.8: Analysis of Local Field Potentials (LFPs) in response to a stimulation train, illustrating sensory and motor pathway activity [17]

1.2.3 Comparison Between Cerebral and Peripheral LFPs

Local Field Potentials recorded in the brain and the peripheral nervous system share fundamental characteristics, as both reflect the electrical activity of neuronal populations. However, they also exhibit significant differences due to the distinct anatomical and physiological properties of these regions. While LFPs provide insights into neural processing at a mesoscopic scale, their origins, properties, and functional roles vary considerably. Cerebral LFPs predominantly arise from the summation of synaptic inputs onto neuronal dendrites and somas within cortical and subcortical structures. These signals are characterized by oscillatory patterns associated with cognitive functions, sensory processing, and motor coordination. Lower-frequency oscillations, such as delta (0.5–4 Hz) and theta (4–8 Hz) waves, are linked to rest, sleep, and memory functions, whereas higher-frequency oscillations, including beta (13–30 Hz) and gamma (30–100 Hz) bands, are implicated in attention, perception, and voluntary movement. Cortical LFPs are modulated by large-scale network activity, facilitating information processing and behavioral control through the integration of signals across different brain regions. In contrast, peripheral LFPs originate from the extracellular electrical activity of afferent and efferent nerve fibers, as well as synaptic connections within peripheral nerves and ganglia. These signals encode sensory inputs from the periphery and motor commands from the central nervous system. Unlike cerebral LFPs, which are shaped by large-scale neural circuit dynamics, peripheral LFPs are more directly influenced by nerve conduction velocity, synaptic transmission at neuromuscular junctions, and the autonomic regulation of organ function. While cerebral LFPs exhibit well-defined oscillatory patterns, peripheral LFPs do not follow the same frequency band structure and instead reflect the modulation of neural activity in response to sensory and motor processing demands. The clinical and research applications of cerebral and peripheral LFPs further underscore their distinctions. Peripheral LFPs are integral to medical diagnostics and therapeutic interventions, including intraoperative nerve monitoring, neuropathy detection, and the design of neuroprosthetic devices for restoring motor and sensory functions. Additionally, peripheral LFPs are essential in closed-loop neuromodulation systems, where real-time monitoring of neural activity informs dynamic adjustments to therapeutic stimulation parameters. Ascending sensory pathways transmit peripheral LFP signals to the brain, influencing cortical activity, while descending motor pathways relay cerebral LFP outputs to peripheral nerves, modulating muscle and organ function. Understanding these bidirectional interactions is essential for the development of advanced neural interfaces and closed-loop systems that integrate central and peripheral signals, paving the way for more effective treatments of neurological and neuromuscular disorders.

1.2.4 LFP and their potentiality in diagnostic

Local Field Potentials (LFPs) have become a crucial tool for studying the electrical activity of groups of neurons in both the central and peripheral nervous systems. By connecting microscopic neuronal activity with larger neural patterns, LFPs offer a valuable way to understand sensory processing, motor control, and cognitive functions. In the brain, cerebral LFPs help researchers investigate brain oscilla-

tions and their involvement in perception, memory, and neurological conditions [18]. On the other hand, peripheral LFPs give us insights into neuromuscular function, sensory-motor integration, and how the central and peripheral systems interact. Future developments in LFPs research are set to improve our understanding of how neural circuits work and expand their use in medical treatments. Innovations in high-resolution signal processing and machine learning algorithms are expected to refine the analysis of LFP recordings, improving the detection of pathological signatures and enabling more accurate, personalized diagnostics for conditions such as epilepsy, Alzheimer's disease, and movement disorders. These advances could help with early diagnosis and create more targeted treatments, leading to better and personalized therapies [19]. The combination of LFP analysis with brain-computer interfaces (BCIs) and neuroprosthetic technologies offers exciting possibilities. By using the detailed information in LFPs, BCIs could become more accurate and flexible, helping users perform complex tasks or communicate through brain signals. In neuroprosthetics, decoding LFPs in real time could improve the control and function of prosthetic devices, making the interaction between the nervous system and artificial parts easier. Another important use of LFP research is in creating closed-loop neuromodulation systems. These systems use real-time LFP feedback to adjust stimulation settings, providing personalized treatments for neurological conditions. For example, they could improve deep brain stimulation for Parkinson's disease by focusing on specific brain patterns or adjust spinal cord stimulation for better chronic pain relief. Looking ahead, collaboration between neuroscience, engineering, and computer science will probably lead to new discoveries in LFP research. As we learn more about how neural circuits create and control LFPs, new treatment methods will be developed, like advanced brain-machine interfaces, better neuromodulation techniques, and tools to improve brain flexibility. These advances will not only improve treatments but also help create new neurotechnologies, giving us a better understanding of how the brain works and communicates.

1.3 Neuroprosthetics: Commercial and Research Applications

1.3.1 Introduction to Neuroprosthetics

Neuroprosthetics is a field focused on developing devices that interface with the nervous system to restore lost motor, sensory, or cognitive functions. By integrating artificial components with neural circuits, these technologies aim to enhance functional recovery in individuals affected by neurological disorders or severe injuries. Neuroprosthetic systems are divided into invasive and non-invasive types based on where the electrodes are placed and how the neural signals are collected. Their main purpose is to create two-way communication between the nervous system and external devices, allowing for real-time control and sensory feedback. In recent years, advancements in neuroprosthetic research have been driven by innovations in neural interfaces, signal processing, and artificial intelligence (AI). A key breakthrough is the integration of AI algorithms to decode neural signals with greater accuracy, al-

lowing for more intuitive and adaptive control of prosthetic devices. These AI-driven systems interpret motor intentions from neural signals in real time, significantly improving the functionality, responsiveness, and user experience of neuroprostheses. Recent studies show that AI can help amputees control a prosthetic hand with finger and wrist movements, reaching an accuracy of 97–98%. This shows how AI can improve the connection between the human nervous system and prosthetic devices, leading to better and more natural neuroprosthetic solutions.

1.3.2 Commercially Available Neuroprosthetic Devices

Several neuroprosthetic devices have been developed and are currently used in clinical practice. One of the most well-established applications is cochlear implants, which restore hearing in individuals with hearing loss by directly stimulating the auditory nerve. Similarly, retinal implants, such as the Argus II system, provide partial vision restoration for patients with retinal degenerative diseases by converting visual information into electrical impulses that stimulate the optic nerve.
Motor neuroprosthetics are now widely used. Myoelectric prostheses help improve the appearance and provide some arm and hand function for people who have lost their upper limbs [20]. An example is the Ottobock bebionic hand and the DEKA Arm that uses electromyographic (EMG) signals from residual muscles to control prosthetic limb movements. Additionally, brain-controlled prostheses based on Brain-Computer Interfaces (BCIs) have shown promising results, allowing individuals with paralysis to control robotic arms or exoskeletons using neural signals. BCI combined with regular rehabilitation can help improve arm movement and attention in stroke patients. This method might be a good option for people who have had a stroke [21].
Another category of neuroprosthetic solutions focuses on neuromodulation. Spinal cord stimulators and deep brain stimulation (DBS) devices modulate neural activity for therapeutic purposes. Figure 1.9 illustrates a DBS system used for neuromodulation which is used in the treatment of Parkinson's disease delivering controlled electrical pulses to specific brain regions. Recent research has explored AI-driven DBS systems that dynamically adjust stimulation parameters based on real-time analysis of patient-specific neural activity patterns, potentially enhancing treatment outcomes for movement disorders. The effectiveness of these devices relies on precise neural signal acquisition and processing. High sampling frequencies, typically ranging from 1 kHz to 12.5 kHz, are commonly used depending on the type of neural signals being recorded. In this study, a sampling rate of 12.5 kHz ensures accurate and responsive neuroprosthetic control, facilitating a smooth integration between the device and the patient's nervous system.

1.3.3 Neuroprosthetics in Research and Experimental Applications

In addition to the devices available today, research is working on new neuroprosthetic systems that can better connect with the nervous system and adapt to the user. Cortical implants, like those from Neuralink and BrainGate, are designed to

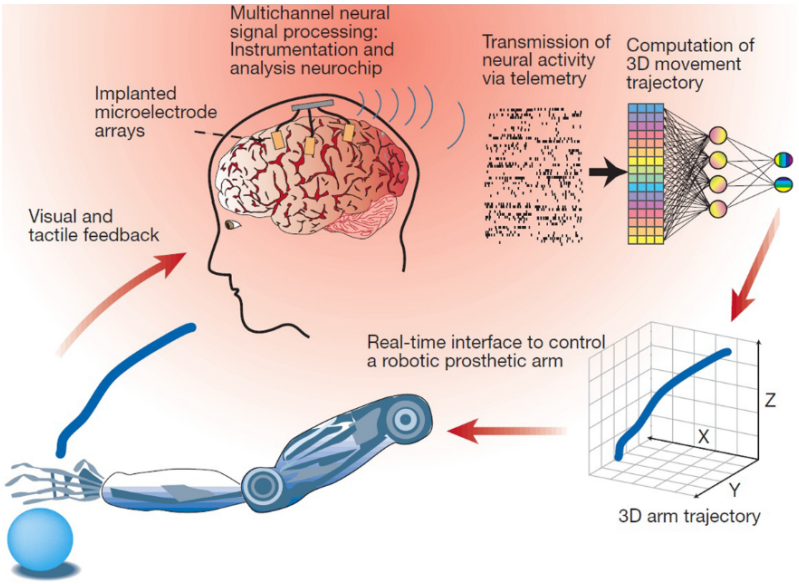

Figure 1.9: Illustration of a Deep Brain Stimulation (DBS) system used for neuromodulation [22]

improve brain controlled interfaces by using advanced electrodes that can read neural activity more accurately. Figure 1.10 illustrates the application of nanofabricated ultraflexible electrode arrays for high-density intracortical recordings, highlighting significant advancements in both signal resolution and adaptability [23]. These advanced Brain-Computer Interfaces have shown great promise in helping people with complete paralysis regain motor function, allowing them to control devices just with their brain signals. Sensory neuroprosthetics represent another critical area of research. Scientists are developing retinal implants with improved pixel resolution and tactile feedback systems that restore the sense of touch in prosthetic limbs. Additionally, closed-loop neuroprosthetic systems are gaining increasing attention. These systems process neural signals in real time, dynamically adjusting stimulation parameters to optimize motor rehabilitation and sensory feedback. By integrating machine learning algorithms, these interfaces adapt to the user's unique neural patterns, improving performance and usability over time. Neuroprosthetics are also being used to improve brain function, with research exploring how neural interfaces can help improve memory and learning. Some experimental projects are looking at the possibility of using cortical implants to restore cognitive functions lost due to diseases like Alzheimer's, opening up new opportunities for future treatments.

1.3.4 Challenges and Future Perspectives

Despite significant advancements, neuroprosthetic technologies still face several critical challenges. One of the primary limitations is long-term signal stability, particularly in invasive implants, where tissue reactions can degrade electrode performance over time. To mitigate this issue, researchers are developing biocompatible materials, such as flexible electrode arrays and conductive polymers, which aim to improve long-term stability while minimizing immune responses to implanted devices. Additionally, miniaturization and wireless energy transfer remain essential for enhancing

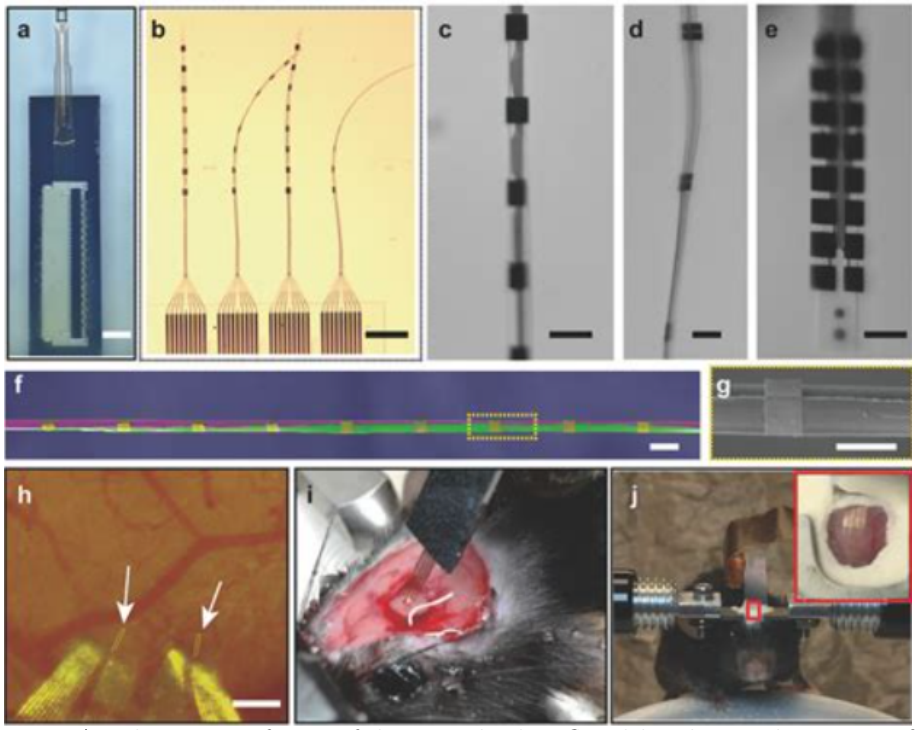

Figure 1.10: Application of nanofabricated ultraflexible electrode arrays for high-density intracortical recordings [23]

the practicality and usability of these devices in everyday life. Ethical and regulatory considerations also play a pivotal role in the widespread adoption of neuroprosthetic systems. As these technologies are used more in healthcare and business, important issues like user privacy, long-term safety, and who owns neural data need to be carefully considered. Also, the ability of Brain-Computer Interfaces (BCIs) to read and even affect brain activity raises concerns about protecting people's mental privacy and their freedom to think. Future advancements in neuroprosthetic technologies will likely prioritize biocompatibility, durability, and adaptive neural interfaces, while enhancing real-time bidirectional communication between neuroprostheses and the nervous system. A major research focus is the development of closed-loop neuromodulation systems [24], where neural activity is continuously monitored to dynamically adjust stimulation parameters, optimizing therapeutic outcomes. The convergence of neural engineering, computational neuroscience, and biotechnology is expected to drive the next generation of neuroprosthetic devices, enabling more smoother integration with the human body and significantly improving the quality of life for users.

1.3.5 Recording Local Field Potentials in Peripheral Nerves for Neuroprosthetics application

LFPs are low-frequency electrical signals that reflect the collective activity of neural populations. While LFPs are traditionally studied within the central nervous system (CNS), their presence in peripheral nerves offers valuable insights into sensory and motor signal transmission. However, recording LFPs from peripheral nerves in-

volves unique challenges, such as small signal amplitudes, susceptibility to external noise, and the need for high-resolution electrode arrays capable of accurately capturing neural activity. To acquire peripheral nerve LFPs, specialized electrodes are required, such as cuff electrodes [25] or intraneural electrodes, which are implanted around or within nerve fibers. These electrodes detect extracellular voltage fluctuations generated by neural activity, which are subsequently amplified and processed for analysis.
Multi-electrode array recordings have been used to investigate the spatial and temporal dynamics of neural activity in the dorsal horn following primary afferent stimulation, demonstrating the feasibility of LFP acquisition from peripheral nerve structures. Advanced signal processing techniques, including filtering and feature extraction, are essential to isolate relevant LFP components from background noise, thereby enhancing the quality and reliability of neural recordings. This research aims to develop a real-time LFP acquisition system designed to sample neural signals from peripheral nerves for diagnostic purposes, neural classification, and targeted stimulation in neuroprosthetic applications. Real-time LFP analysis enables the decoding of neural patterns associated with motor commands and sensory feedback, which is critical for achieving closed-loop control of peripheral neuroprostheses. Moreover, the integration of machine learning algorithms for LFP classification can significantly improve the precision of neural decoding, allowing neuroprosthetic devices to adapt to the unique neural activity patterns of individual users. Advancements in real-time LFP recording and processing will play a pivotal role in shaping the next generation of neural interfaces. By refining signal acquisition methods and enhancing electrode biocompatibility, this research will contribute to the development of minimally invasive, high-resolution neuroprosthetic systems that seamlessly integrate with the peripheral nervous system. These innovations have the potential to revolutionize the field of neuroprosthetics, offering improved functionality and adaptability for a wide range of applications.

1.3.6 Thesis Outline

This thesis is structured into the following chapters:

- Chapter 1 - Introduction: This chapter lays the scientific foundation of the study by introducing the central and peripheral nervous systems and highlighting the importance of Local Field Potentials in understanding neural activity. It also reviews the latest advancements in neuroprosthetics, covering both research developments and existing commercial solutions. Finally, the chapter defines the main goal of this thesis: designing a sampling system capable of accurately capturing and analyzing neural signals with very small amplitudes (around 1 mVpp), typical of Local Field Potentials.

- Chapter 2 - Materials and Methods: This chapter explains the hardware and software used in the study, such as the microcontroller, the sampling algorithm, and the signal processing techniques we applied.

- Chapter 3 - Experimental Setup and Results: This chapter describes the ex-

perimental procedures and presents the obtained results, evaluating the performance of the developed system.

- Chapter 4 - Discussion and Conclusion: In this part are discussed the effects of frequency on the acquired signal and the limitations in low amplitude signal acquisition.

Materials and methods provides a detailed description of the hardware and software components employed in this study. It outlines the architecture of the Nordic nRF5340 microcontroller, including its application core, operating system, and key peripherals such as hardware timer, analog-to-digital converter, and the Distributed Programmable Peripheral Interconnect, DPPI. The experimental setup is explained in detail, with a particular focus on the methodology used to determine the sampling frequency limits of the microcontroller and evaluate their compatibility with the typical Local Field Potential's frequency range that goes from 250 Hz to 500 Hz. The firmware implementation is discussed in detail, highlighting SD card management, the advantages of the EasyDMA mechanism in the ADC for efficient data transfer, and the role of hardware timers in ensuring precise sampling.
This chapter also includes experimental tests conducted using sinusoidal signals generated by a function generator, with amplitudes ranging from 1 mVpp to 600 mVpp and a sampling frequency that varies from 1 kHz to 12.5 kHz. The results chapter presents the outcomes of the experimental validation and data analysis. Sampled waveforms are compared with the original signals generated by the function generator, highlighting both the strengths and limitations of the system. The discussion identifies situations where the sampling process worked well and where it had limitations. It looks at possible reasons for poor performance at certain frequencies and suggests ways to make the system more efficient and reliable for real-time use. Finally, the conclusion summarizes the key findings of this work, reflecting on the effectiveness of the proposed methodology and its implications for future research.

Chapter 2

Materials and Methods

2.1 Microcontroller: nRF5340

The nRF5340 microcontroller (Figure 2.1), developed by Nordic Semiconductor, is a high-performance dual-core system-on-chip (SoC) designed for advanced embedded applications. It integrates two Arm Cortex-M33 processors: the Application Core, optimized for computationally intensive tasks, and the Network Core, dedicated to low-power wireless communication. The Application Core operates at either 128 MHz or 64 MHz, depending on power and performance requirements, while the Network Core is designed for efficient low-power operation. The microcontroller operates within a supply voltage range of 1.7 V to 5.5 V, making it adaptable to various power sources. It supports single 32 MHz crystal operation and provides 48 general-purpose I/O (GPIO) pins, allowing flexible interfacing with external peripherals. The nRF5340 includes 1 MB of flash memory and 512 kB of RAM, with a configurable memory partitioning mechanism that allows dynamic allocation between the two cores. The RAM is divided into 448 kB available to the Application Core and 64 kB dedicated to the Network Core. For peripheral connectivity, it features SPI master/slave interfaces, I2C-compatible two-wire interfaces, and UART interfaces, enabling efficient communication with external devices. Regarding signal acquisition and timing, the microcontroller integrates three 32-bit timers with counter mode, two 24-bit real-time counters (RTC), and a 12-bit, 200 ksps successive approximation ADC (SAADC) with up to eight configurable channels and programmable gain settings. These features are essential for applications requiring precise timing and analog signal processing. The microcontroller is fully compatible with Zephyr OS, a real-time operating system widely used in embedded applications, which provides efficient task scheduling and peripheral management. Thanks to its high processing capability, low power consumption, extensive peripheral set, and robust security features, the nRF5340 represents an optimal solution for various applications, including IoT devices, biomedical instrumentation, wearable technology, industrial automation, wireless audio devices, gaming controllers, and professional lighting systems.

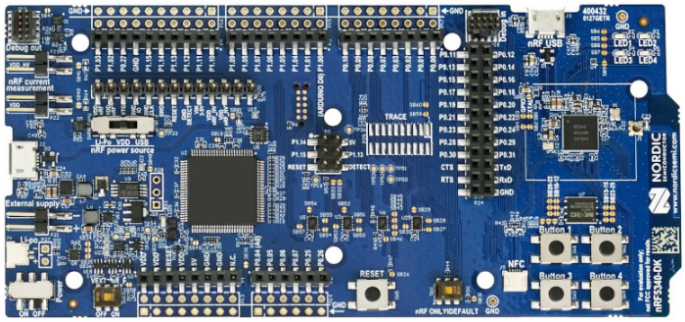

Figure 2.1: The nRF5340 microcontroller development board: [27]

2.1.1 Application Core

The Application Core of the nRF5340 microcontroller is based on an Arm Cortex-M33 processor with Arm TrustZone technology, designed to manage intensive tasks in embedded applications. Both cores support Arm TrustZone technology, enhancing security by enabling secure and non-secure execution environments. In this project, the Application Core operates at 128 MHz,even though it can be configured to run at 64 MHz to optimize power consumption when lower processing power is required. A key feature of the Application Core is the Distributed Programmable Peripheral Interconnect (DPPI), which enables direct communication between peripherals without CPU intervention. The nRF5340 supports up to 32 DPPI channels, providing efficient peripheral interactions. In this project, a dedicated 32 bit hardware timer is used to precisely synchronize ADC sampling, using the DPPI to autonomously trigger conversions every millisecond, while counting with microsecond precision, ensuring high timing accuracy. The firmware developed for this project is based on Zephyr OS, a real-time operating system (RTOS) that provides efficient task such as scheduling, peripheral management, and low-level hardware control and this makes Zephyr OS a robust choice for real-time data acquisition applications. These features make the Application Core of the nRF5340 particularly well-suited for the real-time signal acquisition system implemented in this project. The hardware timer ensures precise synchronization of ADC sampling, while the DPPI efficiently manages peripheral communication, allowing the timer to trigger ADC conversions autonomously, without software latency. Additionally, the GPIO interface, with up to 48 available pins, is used to manage push-buttons for user interaction, while the SPI controller enables data storage on an external SD card, ensuring reliable and efficient data acquisition.

2.1.2 Real-Time Operating System: Zephyr OS

The nRF5340 microcontroller is designed to work with real-time operating systems (RTOS), with Zephyr OS being the officially recommended choice by Nordic Semiconductor. Zephyr is an open-source RTOS optimized for embedded systems, making hardware management more efficient. It features a multithreading kernel that supports both preemptive and cooperative scheduling, ensuring smooth task execution. Threads are managed based on priority, allowing critical operations like ADC sampling and data logging to run with minimal delay. Zephyr also provides

tools like semaphores and mutexes to handle communication between threads and prevent resource conflicts. One of Zephyr's key advantages is its Device Tree based driver model, which simplifies hardware configuration and peripheral management. Instead of manually configuring the nRF5340 registers, developers can use high-level APIs to set up and control hardware components more easily. In this project, Zephyr manages key peripherals, including a 32 bit hardware timer, ADC, GPIO buttons, and the SPI interface for SD card storage. It ensures precise ADC sampling by allowing the timer to autonomously trigger conversions via DPPI, eliminating software delays.
The GPIO interface handles user interaction through button presses and manages hardware interrupts efficiently. Meanwhile, the SPI controller enables smooth data storage on an external SD card. The use of Zephyr OS significantly simplifies the implementation of the firmware, providing a structured software environment for managing peripherals and ensuring reliable real-time execution. Without Zephyr, it would be necessary to manually program and control every hardware component at the register level making the development process significantly more complex.

2.1.3 Memory Usage and Resource Allocation

The firmware developed for this project efficiently manages memory resources to ensure high performance with minimal overhead. The nRF5340 microcontroller has 1 MB of flash memory and 512 kB of RAM, with 448 kB available to the Application Core. During the flashing process, memory usage remains relatively low, with about 8% of flash memory and 63% of available RAM in use. This efficiency comes from the firmware's specific focus on real-time ADC sampling and data storage, rather than heavy computations. Unlike applications involving floating-point operations, machine learning, or real-time digital signal processing, this system mainly handles buffered data transfers between the ADC and external storage. As a result, the codebase remains efficient, with minimal memory usage. By using DPPI, peripherals can communicate with each other directly based on events, which reduces the need for CPU involvement. Moreover, EasyDMA (Direct Memory Access) transfers ADC samples straight to RAM, lightening the processing load and making better use of memory. These hardware features help manage data efficiently without overloading the system with extra buffer allocation.
Another factor contributing to memory efficiency is the modular architecture of Zephyr OS, which ensures that only the necessary kernel components and peripheral drivers are included in the final build. The device tree configuration further optimizes resource allocation by enabling only the required peripherals, preventing unnecessary memory consumption. The firmware also implements a structured data buffering strategy, temporarily storing ADC samples before writing them to the SD card using the FAT32 file system. This approach reduces the frequency of direct write operations, minimizing SD card usage while ensuring an efficient data transfer process. Since the firmware doesn't use multiple threads at once, it doesn't need things like stack allocations or inter-thread communication methods such as mutexes and semaphores. Real-time tasks are managed with hardware timers and interrupts, which helps avoid wasting CPU cycles and keeps RAM usage low. The firmware is

designed to use only the necessary resources while keeping the system stable and responsive during data collection. By using hardware-based data transfers, direct communication between peripherals, and Zephyr's efficient resource management, the system keeps memory usage low without affecting performance. These optimizations allow the microcontroller to run smoothly with the available RAM and flash memory, making it ideal for embedded biomedical applications that need efficient signal processing.

2.1.4 Peripherals Used

Analog-to-Digital Converter (ADC)

The nRF5340 includes a 12-bit Successive Approximation Register (SAR) ADC, capable of sampling at up to 200 ksps. The SAADC (Successive Approximation Analog-to-Digital Converter) supports both single-ended and differential input configurations, allowing flexibility in signal acquisition across up to eight configurable channels. The ADC (Figure 2.2) includes configurable gain settings and multiple reference voltage options, including an internal reference voltage (VDD/4, 0.6V, or 0.6V differential) or an external reference voltage. The selection is handled through the SAADC registers, enabling precise analog measurements.
It supports input channels with programmable acquisition time, ensuring optimal signal integrity and noise reduction for precise measurements. The total sampling rate is affected by both the acquisition time (t_{ACQ}) and the conversion time (t_{conv}), and is determined by the following relationship:

$$f_{\text{SAMPLE}} < \frac{1}{t_{\text{ACQ}} + t_{\text{conv}}}$$

To improve efficiency, the SAADC integrates EasyDMA (Direct Memory Access), which enables efficient data transfers to memory without CPU intervention, reducing processing overhead and allowing the processor to focus on other real-time tasks. This feature is particularly useful in applications requiring continuous signal acquisition, such as the system implemented in this project. The SAADC allows a resolution of 8, 10, or 12 bits, with the possibility of achieving an effective resolution of 14 bits through oversampling. The resolution setting affects both conversion time and power consumption, with higher resolutions requiring longer acquisition times. This technique enhances the signal-to-noise ratio by averaging multiple samples, thereby reducing quantization noise and improving measurement accuracy.
In this implementation, ADC sampling is triggered via the Distributed Programmable Peripheral Interconnect (DPPI), which links the 32-bit hardware timer to the SAADC. This configuration ensures that sampling occurs at precise intervals without requiring CPU intervention, minimizing jitter and improving synchronization for real-time signal acquisition. The nRF Connect SDK provides different approaches for interacting with the SAADC. One possibility is the use of the Zephyr ADC API, which facilitates software development by abstracting hardware details and integrating power management functionalities.
Alternatively, the nrfx SAADC API allows for lower-level control, providing direct

access to hardware registers and enabling more precise and optimized configurations for high-speed sampling. In this project, the nrfx SAADC API was selected to guarantee precise synchronization and full configurability of the ADC, ensuring the accuracy and reliability of the acquired data.

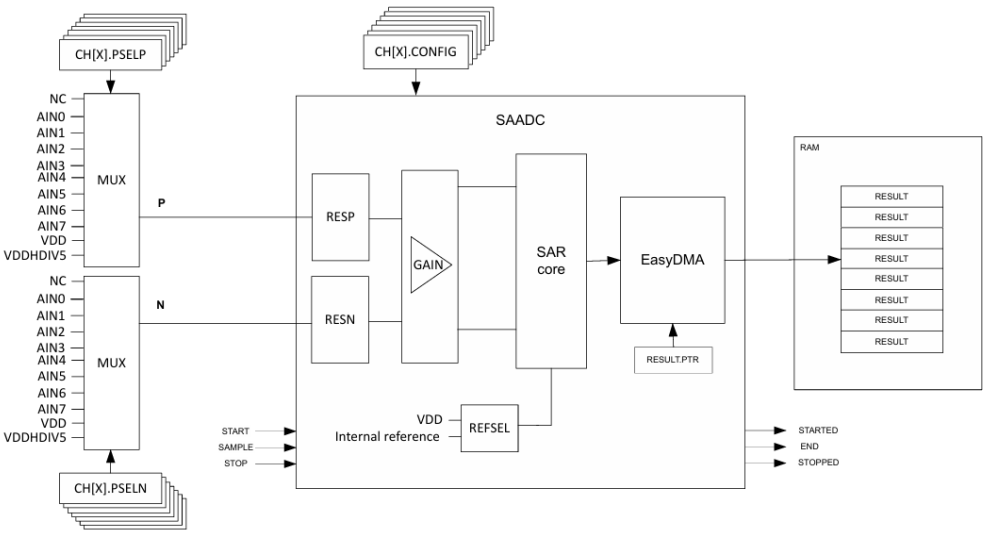

Figure 2.2: Block diagram of the nRF5340 SAADC: [27]

Hardware Timers

The nRF5340 (Figure 2.3) includes up to five general-purpose 32 bit timers and two 24 bit real-time counters that support various operating modes, such as capture and compare and counter, enabling accurate event timing and signal generation.
Each timer includes a configurable prescaler, which allows adjusting the timer frequency by selecting a base clock of either 16 MHz or 1 MHz. This flexibility enables precise timing adjustments depending on the application requirements.
The timer operates in BITMODE, which defines the counter width, allowing configurations of 8-bit, 16-bit, 24-bit, or 32-bit. In this project, the timer is set to 32-bit mode to ensure precise microsecond timing. Each timer features multiple compare/capture channels, which can be used to generate periodic events or measure external signals with high precision. The timers also support interrupt generation, allowing easy integration into real-time applications. In this project, a 32-bit general-purpose timer is used to generate periodic interrupts for ADC sampling and is configured to operate at microsecond resolution, ensuring high accuracy in signal processing.
Additionally, it is linked to the DPPI (Distributed Programmable Peripheral Interconnect), allowing the timer to autonomously trigger ADC conversions at precise intervals without requiring CPU intervention. This reduces jitter and ensures synchronization in real-time data acquisition. Additionally, the real-time counters can be used for long-duration timing operations, supporting low-power applications where energy efficiency is critical.

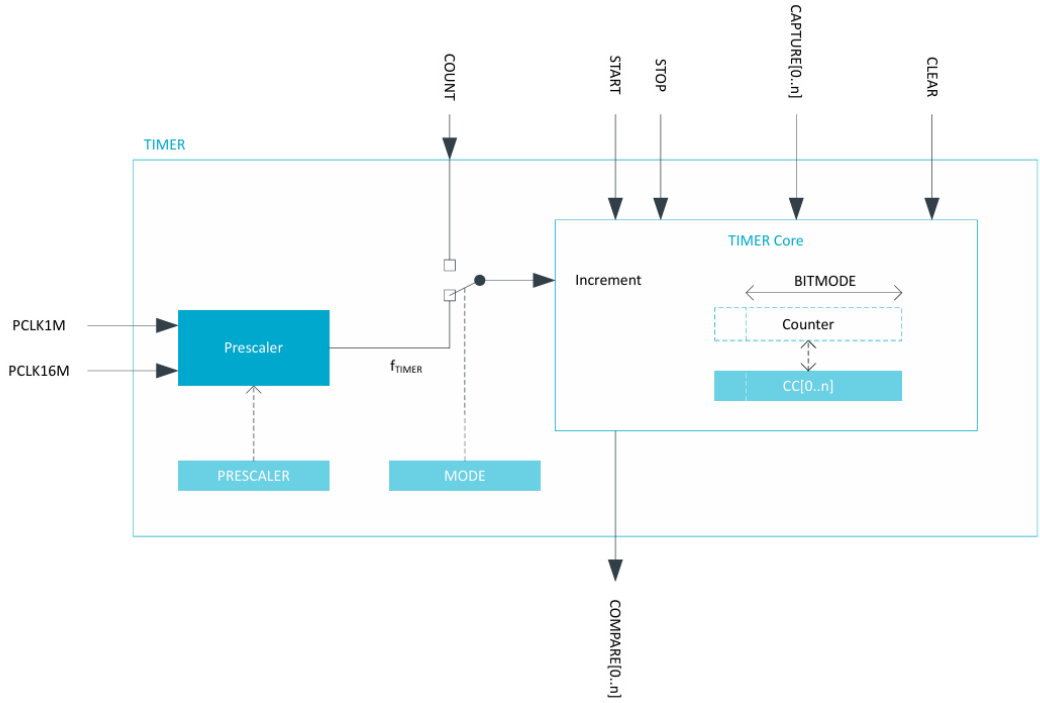

Figure 2.3: Block diagram of the nRF5340 hardware timer: [27]

Distributed Programmable Peripheral Interconnect (DPPI)

The nRF5340 has a system called Distributed Programmable Peripheral Interconnect (DPPI), which allows peripherals to communicate directly with each other without using the CPU. DPPI is a more flexible version of the old Processor Peripheral Interface (PPI) and supports faster, event based actions. It can handle up to 32 independent channels, allowing peripherals like timers, ADC, SPI, and GPIOs to send and receive events in a simple way. In this setup, one peripheral can trigger an event on a channel, and other peripherals can react to that event by listening to the same channel. This approach eliminates the need for software intervention, improving the efficiency of the system. Additionally, DPPI significantly reduces CPU load by allowing direct peripheral communication without software intervention, which is particularly beneficial in a Zephyr-based system where efficient task scheduling is required. This minimizes processing overhead and enhances real-time responsiveness, making it ideal for high-performance embedded applications. Compared to the old PPI system, DPPI offers more flexibility and scalability, reducing the need for extra hardware connections and allowing events to be routed more easily. In this project, DPPI is used to connect the 32-bit hardware timer to the ADC, making sure the ADC triggers automatically and precisely at set time intervals. The DPPI system is set up through register-based configuration, where the timer can trigger an event and the ADC will respond to it. This setup eliminates the need for software-based polling or manual triggers, reducing timing issues and making data acquisition more stable and accurate.

General-Purpose Input/Output (GPIO)

The nRF5340 has 48 general-purpose I/O (GPIO) pins, which can function as inputs, outputs, or bidirectional signals. Each GPIO can be configured with internal pull-up or pull-down resistors to improve signal integrity when connected to external components. The drive strength can be adjusted to control power usage and signal quality, depending on the needs of the circuit. Also, the GPIO system has low-power modes to save energy when not in use. GPIOs support interrupt-based event handling, allowing the system to respond efficiently to external inputs without constant CPU processing. They can also generate hardware events via DPPI, enabling direct communication between peripherals without software intervention. This improves response times and reduces processing load in real-time applications. In this project, GPIOs are used to handle user input via push-buttons, which control the start, stop, and data-saving functions of the firmware. Button presses trigger interrupt-driven events, ensuring fast response times and smooth interaction with the data acquisition system.

Serial Peripheral Interface (SPI)

The nRF5340 integrates five independent SPI master/slave instances, allowing multiple SPI peripherals to operate simultaneously without conflicts. The SPI module supports full-duplex and simplex communication, allowing simultaneous or independent data transmission and reception. It also supports configurable clock speeds, ranging up to 8 Mbps, along with adjustable data modes (CPOL and CPHA) and frame sizes, enabling flexible communication with a wide range of external devices. The SPI peripheral integrates EasyDMA, which allows direct memory transfers in the background, significantly reducing CPU load and enabling seamless data logging to the SD card. This allows continuous data streaming, minimizing processing overhead and ensuring optimal real-time performance. In this project, the SPI interface facilitates communication with an external SD card, enabling real-time storage of ADC samples. By leveraging EasyDMA-based SPI transfers, data is efficiently written to storage without blocking CPU resources, ensuring seamless real-time acquisition and processing.

File System and Data Storage

The nRF5340 microcontroller supports external storage using a microSD card formatted with FAT32, ensuring compatibility with Windows, Linux, and macOS. FAT32 was chosen for its wide support and ability to handle large data sets efficiently. In this project, the FAT32 file system is mounted via Zephyr's file system API. The microSD card is initialized and mounted at `/SD` using the `fs_mount()` function, with `FS_FATFS` as the selected file system type. Once mounted, the microcontroller can create, read, and write files as needed. ADC samples are stored in text files for easy post-processing and analysis. During data acquisition, a new file is opened using `f_open()` with the flags `FA_WRITE | FA_CREATE_ALWAYS`. Data is written via `f_write()`, while a temporary buffer (`sdbuffer`) reduces the number of direct writes to the SD card, minimizing wear. After recording, the file is closed

with `f_close()` to ensure data integrity. By combining FAT32 with Zephyr's file system API, this approach provides a reliable and efficient way to store data, making retrieval from the SD card straightforward for further analysis.

2.2 Firmware Development and Implementation

2.2.1 Development and Optimization

The firmware for the nRF5340 based sampler was developed through multiple iterations to improve precision and efficiency. At the beginning, ADC values and timestamps were acquired separately, requiring manual collection and analysis. The first implementation used PuTTY, a serial terminal, that printed ADC values via UART. While this approach allowed basic data acquisition, it lacked synchronization between samples, leading to inconsistent results. To address this issue, an interrupt-based approach with a sampling frequency of 1 kHz using the OS timer was introduced, triggering the ADC at regular intervals. However, this software timer had limitations in precision, causing the system to collect 994 samples per second instead of the expected 1000 Hz. The inaccuracy was due to the software overhead and the limited resolution of the OS timer, which was unable to guarantee precise millisecond intervals. To improve timing accuracy, the OS timer was replaced with a 32-bit hardware timer running at 1 MHz, ensuring microsecond precision. This timer generated an interrupt every millisecond, allowing exactly 1000 samples per second to be acquired. However, ADC sampling was still managed via CPU interrupts, increasing processor workload and introducing potential timing jitter. Initially, the ADC operated in single-ended (SE) mode, measuring the input voltage relative to ground. This setup had limitations, particularly with signals containing negative components, which the ADC could not represent properly. Switching to differential (DIFF) mode solved this issue by allowing the ADC to measure the voltage difference between two input channels.
This ensured correct acquisition of negative signals, enabling an accurate representation of symmetrical waveforms like sine waves. For further optimization, DPPI was used to simplify ADC sampling. The timer's COMPARE event triggered the SAADC START task, enabling sampling controlled by hardware and reducing software delays. EasyDMA was then introduced to transfer ADC results directly to RAM, further reducing CPU load. With this system based on events, the firmware achieved stable and accurate 1000 Hz sampling with minimal jitter. The DPPI mechanism reduced the CPU workload, letting the microcontroller focus on data acquisition without extra processing. Also, since the CPU was not active during ADC sampling, energy efficiency improved, and the processor was activated only for data storage or user input. After achieving reliable 1 kHz sampling, further tests were conducted to push the system's capabilities. The sampling frequency was first increased to 5 kHz, confirming that the timer maintained accurate timing.
Encouraged by these results, the sampling rate was pushed to 12.5 kHz while maintaining precise timing. To handle higher sampling rates efficiently, buffer management was optimized. The initial implementation used a double-buffering approach, which was sufficient at lower frequencies but introduced limitations at higher speeds.

The final firmware expanded this to 16 buffers, each holding 8000 samples.
The decision to use 8000 samples per buffer, instead of 8196, simplified memory allocation and file storage while ensuring efficient RAM utilization. This multi-buffering approach reduced CPU load and prevented data loss, allowing seamless data acquisition and improved system stability at 12.5 kHz. Another important development in the firmware has been made with the buffer management.
At first with the sampling frequency at 1 kHz everytime a buffer was ready it was subsequently used for saving data but in total were used only two buffers and the management was easier. In the final firmware with the frequency of 12.5 kHz the buffer management was different because as the frequency was higher, more samples were acquired and only two buffers were not enough so the approach has been modified. In particular, 16 buffer were used and when one buffer was full, it was indexed and that meant that it was ready to be saved on the SD card. To simplify the explanation, the block diagram in Figure 2.4 provides a visual representation of the system, highlighting the key components involved in signal acquisition and storage.

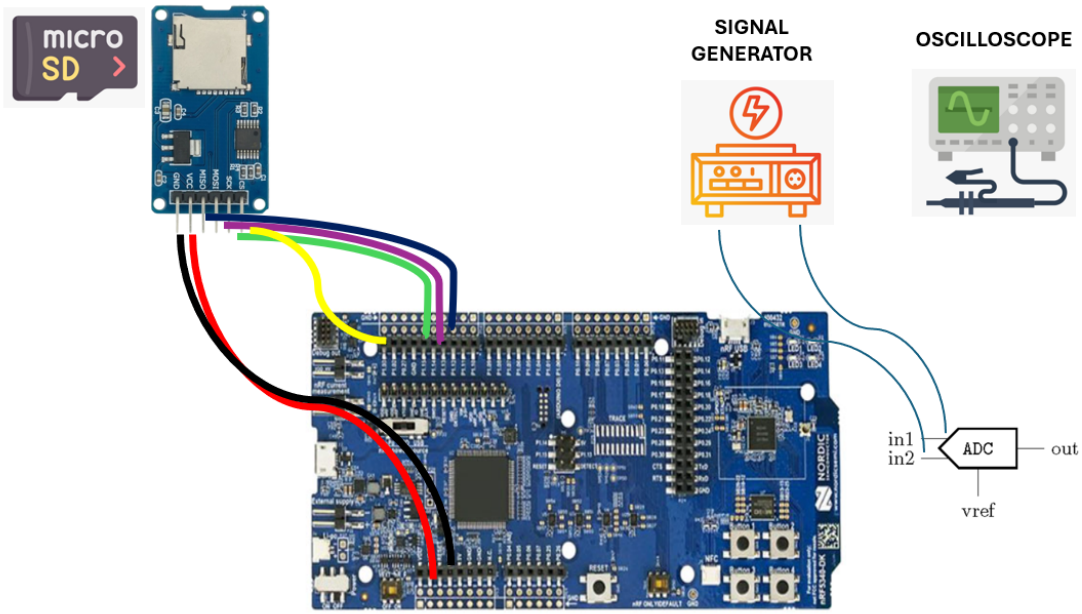

Figure 2.4: Hardware setup for signal acquisition using the nRF5340 microcontroller. The signal generator provides an input to the ADC, which samples the waveform. The acquired data is stored on a microSD card via SPI communication. The oscilloscope is used for signal monitoring. (Designed by the author.)

Additionally, to provide a clearer overview of the firmware structure and its key components, a flowchart is presented in Figure 2.5.

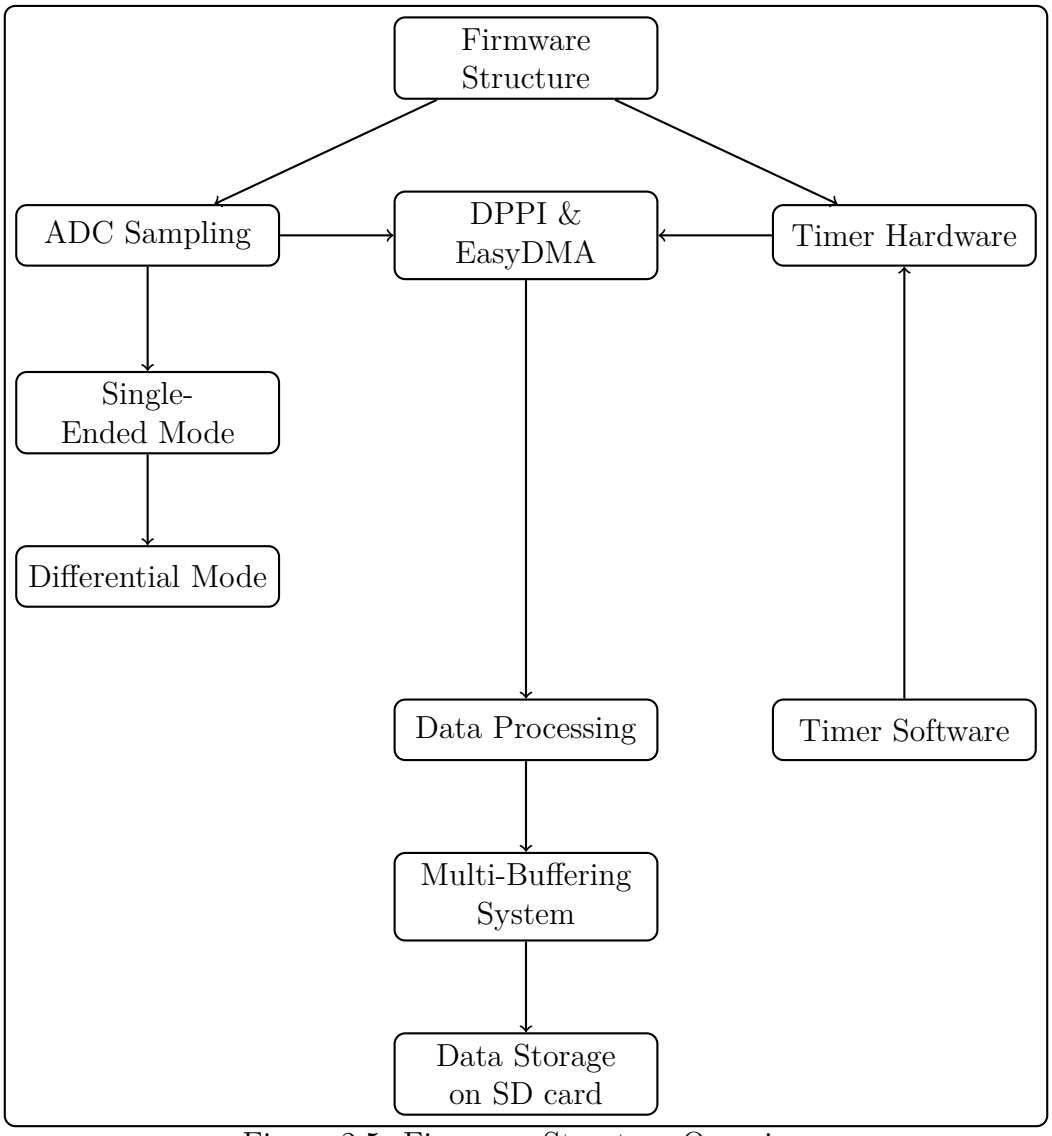

Figure 2.5: Firmware Structure Overview

2.2.2 System Validation and Performance Analysis

To evaluate the performance of the sampling system, a series of tests were conducted using a signal generator to produce sinusoidal waveforms at different frequencies and amplitudes. The goal was to determine the frequency range in which the microcontroller could reliably sample signals and evaluate its ability to capture low-frequency oscillations typical of LFPs, which usually extend up to 500 Hz. The nRF5340 microcontroller was initially set to a fixed sampling rate of 1 kHz, meaning that, according to the Nyquist theorem, it could theoretically detect frequencies up to 500 Hz. To verify this in practice, sinusoidal signals were generated between 20 Hz and 500 Hz, increasing in steps of 50 to 100 Hz.

The signal amplitude was also varied at different levels: 600 mVpp, 400 mVpp, 300 mVpp, 200 mVpp, 100 mVpp, 50 mVpp, 25 mVpp and 10 mVpp. The acquired data was then processed in MATLAB, where the reconstructed waveforms were compared to the original signals to assess fidelity and distortion. For frequencies up to 250

Hz, the sampled signals maintained good fidelity, with minimal phase and amplitude distortion. However, as the signal amplitude decreased, noise became more noticeable, making it harder to distinguish the sinusoidal waveform. Between 250 Hz and 500 Hz, noise became dominant, significantly affecting signal quality and revealing the system's limitations near the Nyquist threshold as it was expected. To explore performance at higher frequencies, the sampling rate was first increased to 5 kHz and later to 12.5 kHz, while maintaining the 16-buffer structure to handle data efficiently. At 5 kHz, the system accurately reconstructed signals up to 2 kHz, but distortions began to appear at 3 kHz, showing that real world performance are quite different from what we expect in theory. At 12.5 kHz, additional tests were done with the aim of acquiring low-amplitude signals because LFPs are typically in a microvolt range. The first test used a 100 mVpp sinusoidal signal, which was accurately reconstructed and then different approaches were used to reduce the signal amplitude. The first method reduced the signal amplitude artificially in MATLAB. This provided an estimate, but it was not completely accurate because it did not include hardware noise. The second method used an LTSpice simulation with a resistor network to model signal attenuation under ideal conditions. While the results looked promising, they did not reflect real-world noise and limitations. The third method involved applying a 60 dB attenuation using three attenuators in series (20 dB, 30 dB, and 12 dB). A voltage divider without an amplifier was also tested, but it introduced excessive noise and waveform distortion, making it impractical. These tests helped define the system's limits when operating without an amplifier. The results confirmed that, without active amplification, very low-amplitude signals could not be reliably acquired due to hardware noise and signal attenuation. This shows the need for a better analog front-end with low-noise amplifiers (LNA) and filters to improve signal quality and accurately capture neural signals.

2.2.3 Firmware Architecture and Implementation

The firmware developed for the nRF5340 microcontroller is designed to enable real-time acquisition of analog signals using the Successive Approximation Analog-to-Digital Converter (SAADC), synchronized via a hardware timer, and stored on an SD card through the SPI interface. The implementation follows a structured approach where different firmware components interact to ensure precise and efficient data acquisition. At the beginning, the firmware initializes the essential peripherals required for the acquisition process. The first one is the hardware timer that is configured to generate periodic events with a configurable sampling interval. In the current configuration, the timer is set to trigger every 80 microseconds, allowing for a sampling rate of 12.5 kHz, but this can be adjusted for different applications. The SAADC is set up in differential mode to acquire input signals with a reference voltage of $\pm 0.6V$, making it suitable for the targeted analog signals. To ensure autonomous ADC triggering, the DPPI is employed, allowing direct hardware connections between the timer and the ADC. One DPPI channel links the COMPARE0 event of the timer to the SAADC SAMPLE task, ensuring periodic ADC conversions without CPU intervention. Another DPPI channel connects the ADC END event to the START task, enabling continuous sampling. Additionally, GPIOs are con-

figured to interface with push-buttons, which allow the user to control the system, and LEDs are used as status indicators.

Data Buffering and SD Storage

To efficiently manage the high volume of acquired data, a circular buffering system with 16 alternating buffers, each capable of storing 8000 samples, is implemented. When a buffer is filled, it is flagged for storage while data acquisition continues in the next buffer, ensuring uninterrupted operation. The recorded data is formatted as text and written to the SD card asynchronously. To facilitate file handling and cross-platform compatibility, the SD card is formatted using the FAT32 file system, allowing easy access to stored data on Windows, Linux, and macOS without additional software. FAT32 also ensures efficient memory allocation and sequential data writing, making it well-suited for high-frequency sampling applications. The firmware limits the creation of files to a maximum of 20 per acquisition session, with filenames structured as file1.txt, file2.txt, etc., to ensure structured data management over multiple recording sessions.

Testing the firmware architecture

The system follows a state-driven process to manage data acquisition. It has five main states that control how the system works. In the IDLE state, the system waits for user input. No data is acquired, and even though the SD card is mounted, no writing happens. Pressing Button 1 moves the system to the OPEN_FILE state, where a new file is created for storing data. If the maximum number of files (twenty) is reached, the system blocks new file creation to prevent overwriting. When Button 2 is pressed, the system enters the SAMPLING state. The ADC samples data at 12.5 kHz, storing it in buffers in real time. The DPPI mechanism triggers each sample automatically, so the CPU does not need to intervene. When a buffer is full, it is marked for writing to the SD card. Pressing Button 3 stops data acquisition, closes the current file, and returns the system to IDLE. Pressing Button 4 moves the system to the STOP_DEVICE state. In this state, sampling stops, open files are safely closed, and the system resets. State changes happen when the user presses a button. LED indicators and Zephyr's logging module provide real-time feedback. This state-driven approach helps manage data efficiently while reducing CPU workload.

Real-Time Execution and Optimizations

To meet real-time constraints and ensure consistent performance, several optimizations have been implemented:

- EasyDMA is used to reduce CPU load during SPI transactions.
- Hardware-triggered ADC sampling eliminates software-based delays.
- The circular buffering mechanism minimizes the number of write operations on the SD card, improving efficiency.

The entire firmware execution is managed by a real-time thread (coreThread), which runs with high priority (-16) and ensures that the FSM continuously processes user inputs and buffer management tasks without preemption. The thread is created as a non-preemptive task, meaning it remains active and ensures deterministic execution of the acquisition process. This structured firmware implementation ensures efficient, real-time data acquisition while leveraging the advanced features of the nRF5340 microcontroller. The combination of event-driven processing, hardware-level peripheral control, and optimized data management makes the system highly reliable for applications requiring precise and continuous signal sampling.

2.3 Experimental Setup

To develop and validate the real-time signal acquisition system, a dedicated hardware and software setup was implemented. The firmware for the nRF5340 microcontroller was developed using Visual Studio Code with the nRF Connect SDK and the Nordic toolchain. The nRF Connect for VS Code extension was used to facilitate project creation, compilation, debugging, and flashing of the firmware onto the development board. The firmware was designed to configure the ADC in differential mode, manage data acquisition through hardware timers, and store the sampled signals on an external microSD card via the SPI interface. For signal generation and validation, an Hantek HDG2032B arbitrary waveform generator (Figure 2.6) was used to provide a sinusoidal input signal to the ADC. The generator was configured to output signals with frequencies of 20 Hz, 50 Hz, 100 Hz, 150 Hz, 200 Hz, 250 Hz, 300 Hz, 400 Hz, 500 Hz, 1 kHz, 2 kHz and 3kHz. Additionally, the amplitude of the generated signal was varied from 600 mVpp to 1 mVpp to evaluate the ADC's ability to correctly capture and digitize signals of different magnitudes. The differential output of the generator was connected to the ADC input channels on the nRF5340 development board, ensuring high-fidelity acquisition. Since the firmware was configured to perform sampling at 1 kHz, these tests were conducted to analyze how different input signal frequencies were digitized. By comparing the sampled signals with the original waveforms, the system's aliasing behavior, frequency response, and amplitude accuracy were assessed. To verify the correctness of the acquired signals, a Rigol DS1054Z digital oscilloscope (Figure 2.7) was employed to monitor both the generated input signal and the digitized output stored by the microcontroller.

Figure 2.6: Hantek HDG2032B arbitrary waveform generator used for signal generation. Photo by the author.

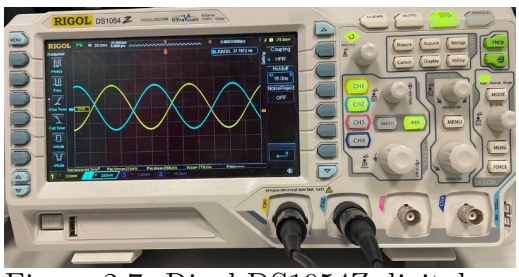

Figure 2.7: Rigol DS1054Z digital oscilloscope used for signal monitoring. Photo by the author.

The oscilloscope was used to visualize the waveform in real time and compare the original and digitized signals. It also helped detect distortions, phase shifts, or signal integrity issues, especially at low amplitudes. The nRF5340 development board ran the firmware responsible for ADC sampling, data storage, and user interaction via push-buttons. The sampled data was saved on a 32 GB microSD card for later analysis. The acquired signals were then processed in MATLAB, where the stored samples were plotted to evaluate the digitized waveforms. This analysis showed the ADC's resolution and noise levels, confirming the system's ability to accurately capture and process signals across different frequencies and amplitudes. This setup provided a structured approach to validating the sampling system's performance, ensuring that the nRF5340 microcontroller could reliably acquire analog signals in a real-time embedded application.

Chapter 3

Results

3.1 Preliminary Tests

To verify the correct functioning of the designed sampler, preliminary tests were conducted using a Hantek HDG2032B signal generator, with data acquisition and analysis performed in MATLAB. The tests aimed to evaluate the system's ability to reconstruct sinusoidal waveforms across a range of amplitudes and frequencies. A fixed sampling frequency of 1 kHz was used, while the input signal amplitude was varied across 10, 25, 50, 100, 200, 300, 400, 500, and 600 mVpp. The results indicate that signals up to 125 Hz were accurately reconstructed, while higher-frequency signals exhibit increasing levels of distortion. The distortion is primarily due to the limited sampling rate, which affects the system's ability to resolve rapid signal variations. Additionally, signals with lower amplitudes suffer from increased noise, making waveform reconstruction more challenging. Specifically, the 10 mVpp signal required filtering to improve its clarity. The signal degradation at high frequencies and low amplitudes suggests a trade-off between resolution and frequency fidelity, which should be considered in further applications.

3.1.1 ADC Data Processing

The acquired ADC values were processed in MATLAB using the following conversion formula, derived from the ADC datasheet:

$$V_{\text{adc}} = V_{\text{digital}} \times \frac{V_{\text{ref}} \times (1/G)}{2^{11}} \tag{3.1}$$

where:

- V_{adc} is the reconstructed voltage value,
- V_{digital} is the raw ADC output value,
- G is the gain setting,
- $V_{\text{ref}} = \pm 0.6V$ is the ADC reference voltage,

- The division by 2^{11} accounts for the 12-bit differential ADC, where the output range spans from -2048 to $+2047$ instead of the standard -4096 to $+4095$ used in single-ended mode.

This formula ensures that the digital output values are properly scaled according to the ADC reference voltage and gain configuration.

3.1.2 Visualization of Acquired Signals

To further analyze the system's performance, the acquired waveforms were plotted and examined. The following figures show the reconstructed sinusoidal signals for increasing amplitude levels, from 10 mVpp to 600 mVpp at 1 kHz. For lower amplitudes the signals appear noisier and as the amplitude increases, the waveforms become progressively clearer. However, for frequencies beyond 200 Hz, noticeable distortions occur in fact at 500 Hz signal exhibits visible aliasing effects due to the sampling rate limitation. In order to investigate the system's capability to capture higher-frequency signals and to improve the signal quality at lower amplitudes, the firmware was updated to support increased sampling rates. The following section describes the modifications applied to the firmware and the results obtained at 5 kHz and 12.5 kHz.

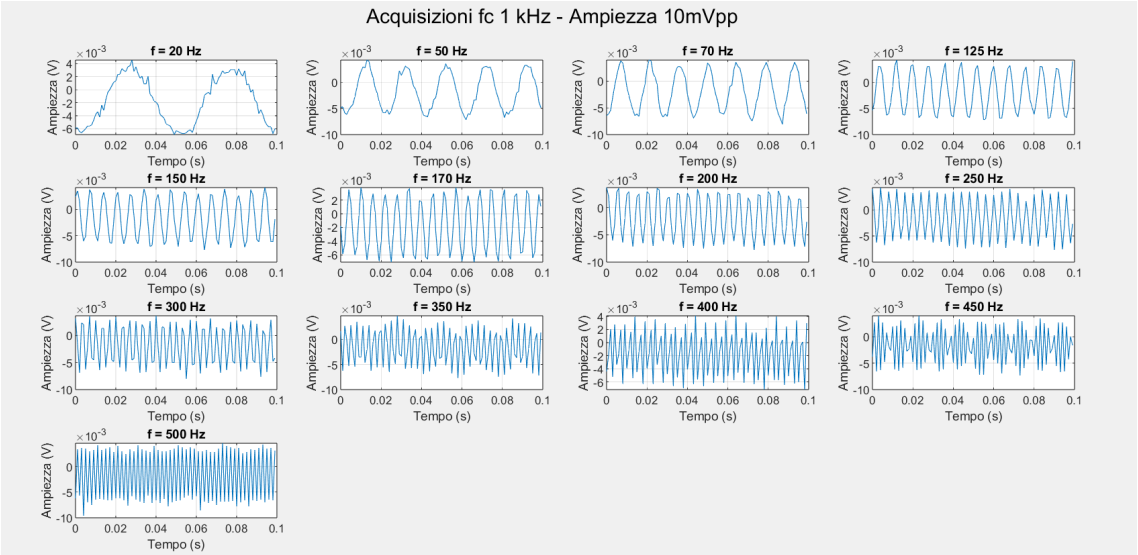

Figure 3.1: Acquired signals at 10 mVpp

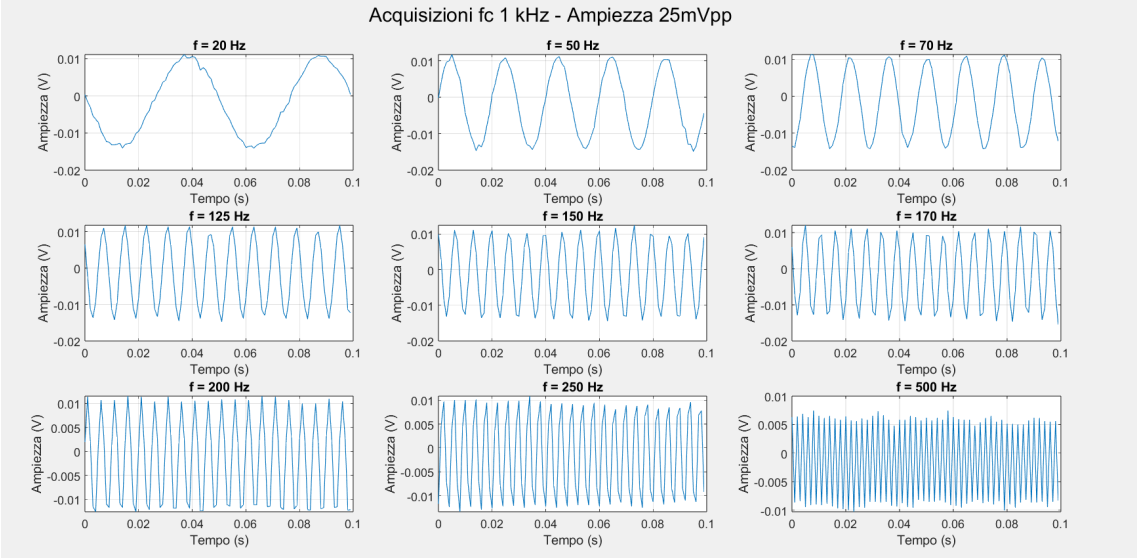

Figure 3.2: Acquired signals at 25 mVpp

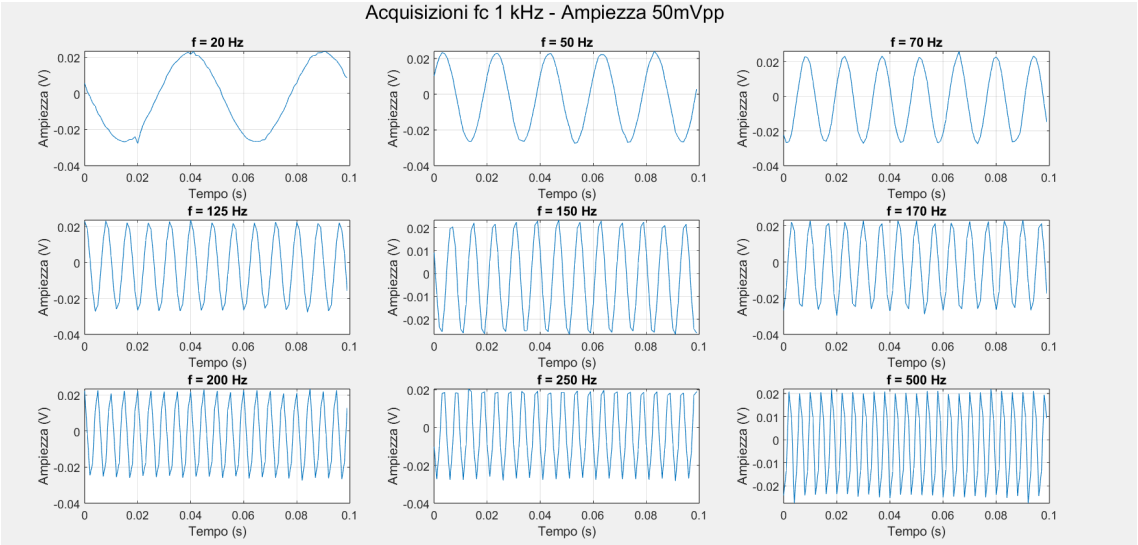

Figure 3.3: Acquired signals at 50 mVpp

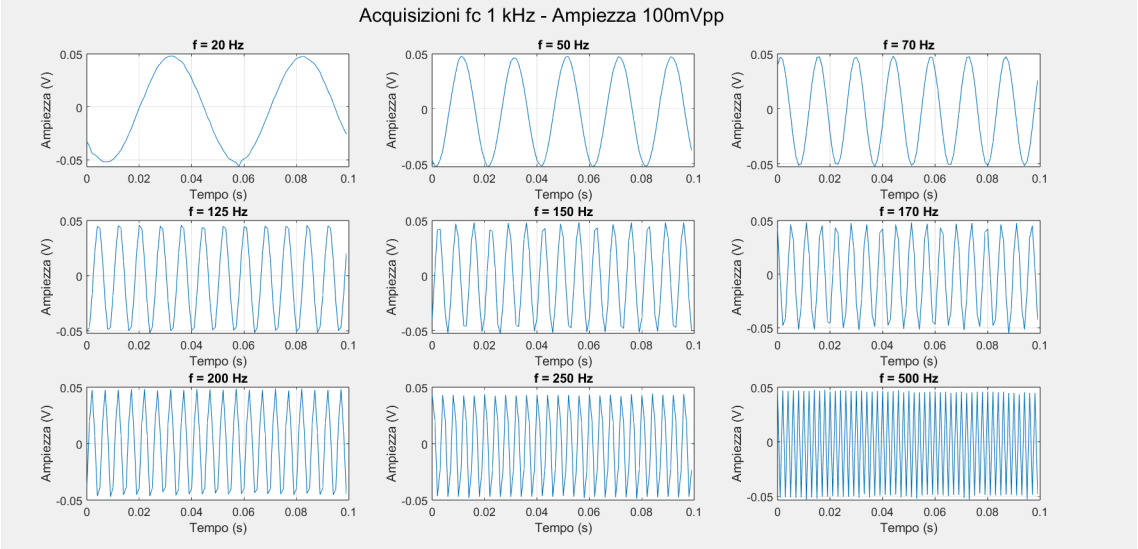

Figure 3.4: Acquired signals at 100 mVpp

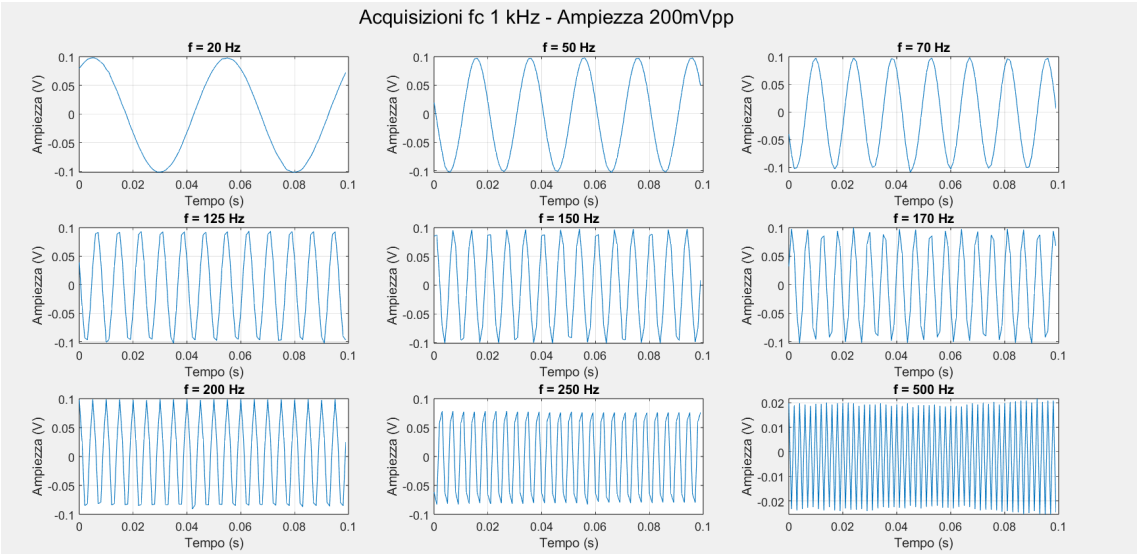

Figure 3.5: Acquired signals at 200 mVpp

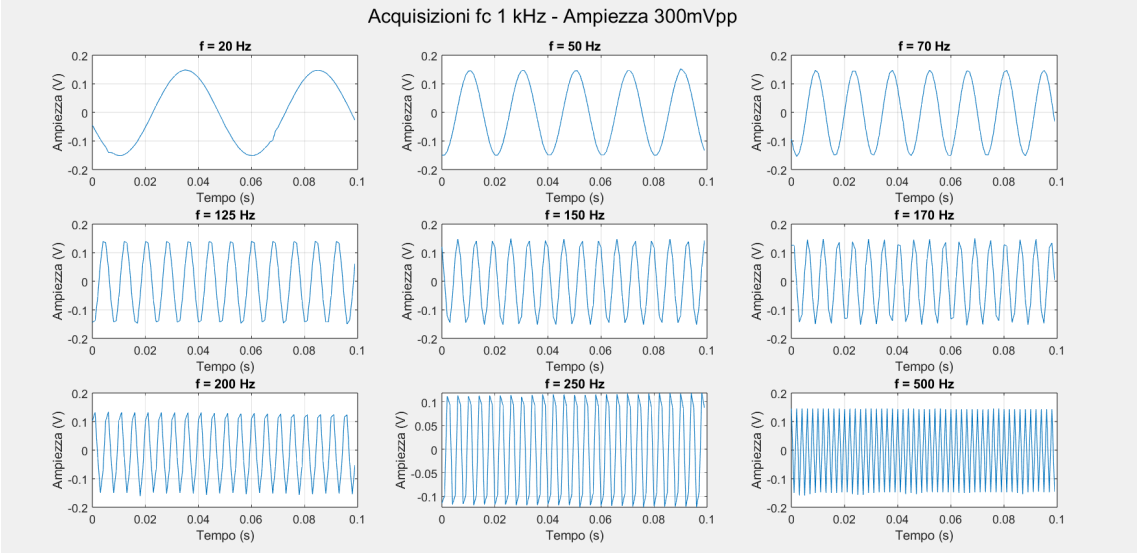

Figure 3.6: Acquired signals at 300 mVpp

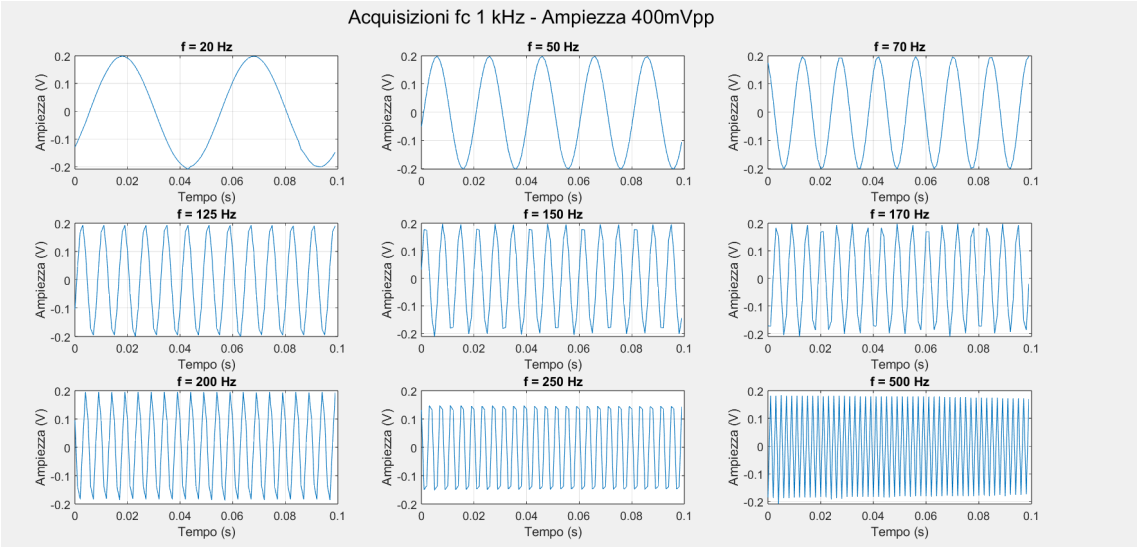

Figure 3.7: Acquired signals at 400 mVpp

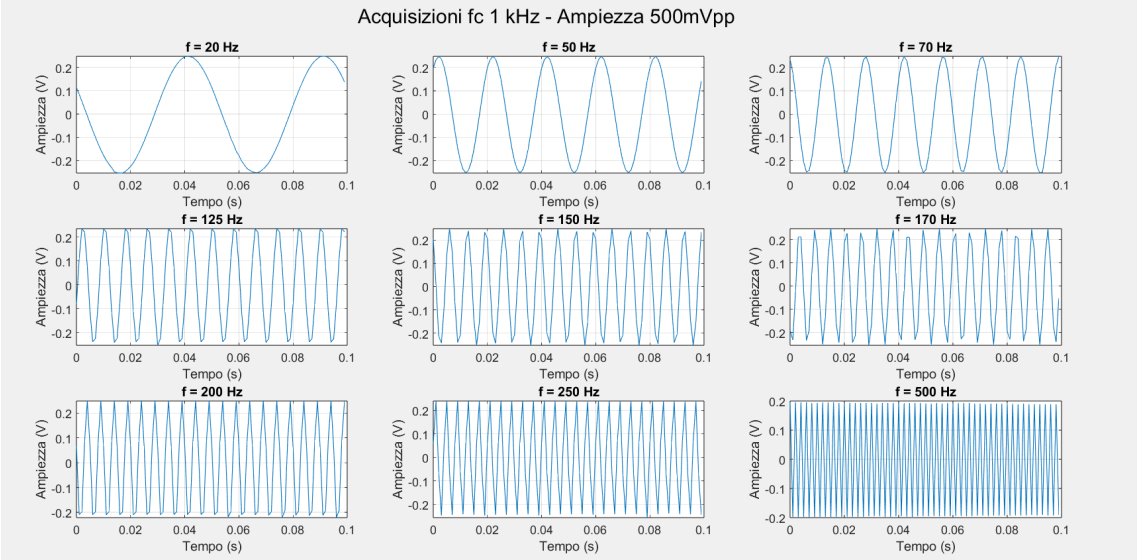

Figure 3.8: Acquired signals at 500 mVpp

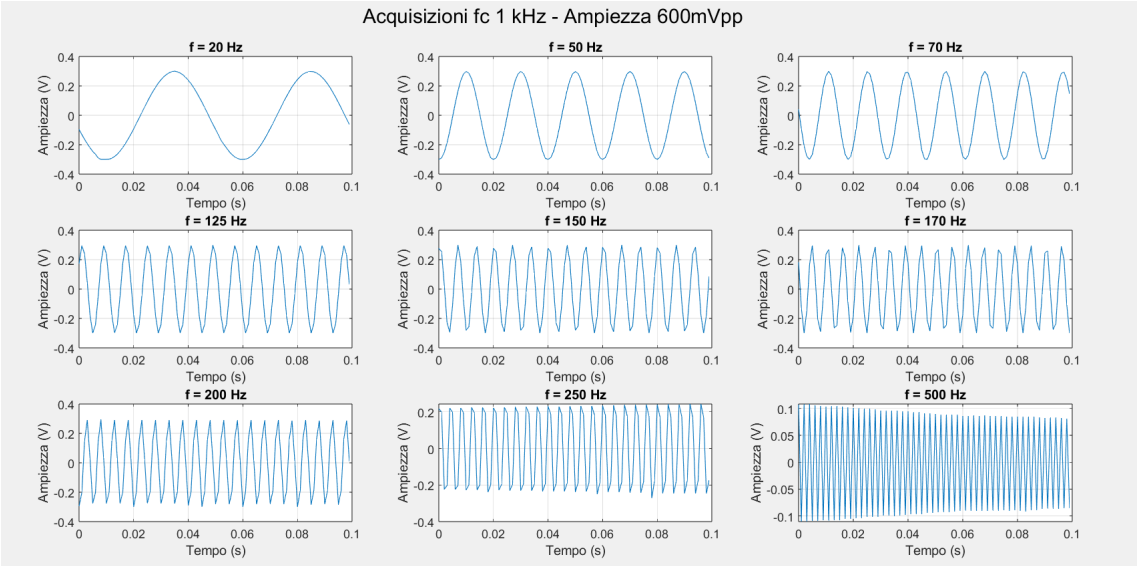

Figure 3.9: Acquired signals at 600 mVpp

3.1.3 Increased Sampling Frequency Tests

To better test the sampler, the firmware was updated to support higher sampling rates. The first tests were done at 1 kHz, but later, additional tests were run at 5 kHz and 12.5 kHz. This was to check if the system could handle faster sampling. The main goal was to improve the reconstruction of high-frequency signals and reduce noise in weaker signals. Increasing the sampling frequency required modifying the timer configuration and adjusting buffer sizes to handle the larger data flow. This change was necessary to prevent data loss and ensure continuous acquisition. The updated firmware allowed real-time processing and data storage while avoiding buffer overflows that could have affected data integrity. The first test at 5 kHz was performed using a 100 mVpp sine wave. The results, analyzed in MATLAB, confirmed that the sampling period remained stable and consistent. Since the system

maintained expected performance at this rate, further tests were carried out at 12.5 kHz. These included signals with amplitudes of 10, 7, 5, and 1 mVpp to examine how noise influenced lower signal levels. At 12.5 kHz, the system successfully reconstructed the signals, preserving the expected sampling rate and waveform shape. However, as the amplitude decreased, particularly at 1 mVpp, noise became more visible, making the waveform less clear. This result highlights a common balance: increasing the sampling frequency improves resolution but can also amplify noise, which is an important factor when working with very low-amplitude signals.

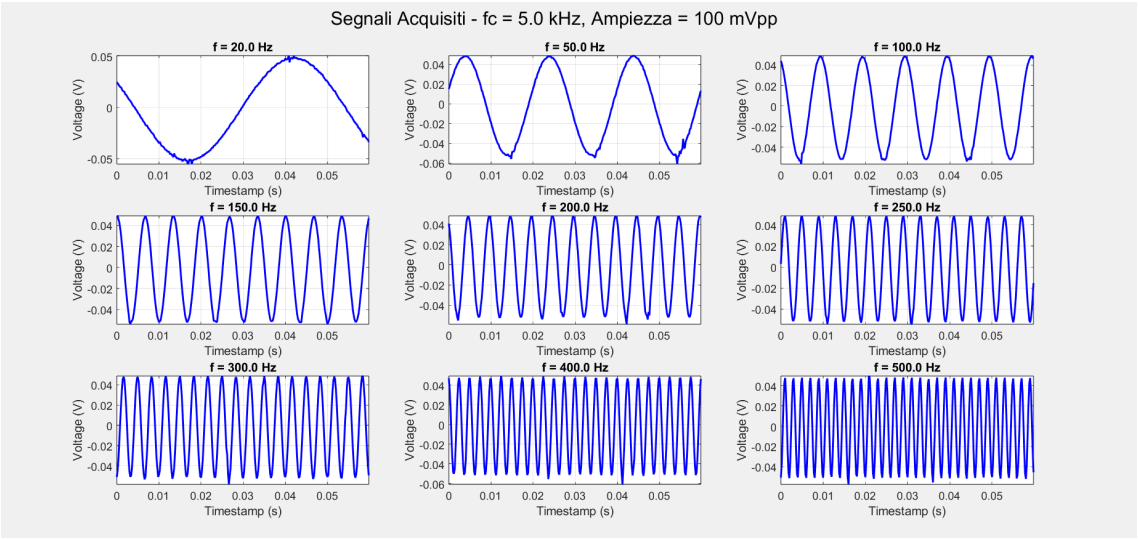

Figure 3.10: Acquired signal at 5 kHz, 100 mVpp

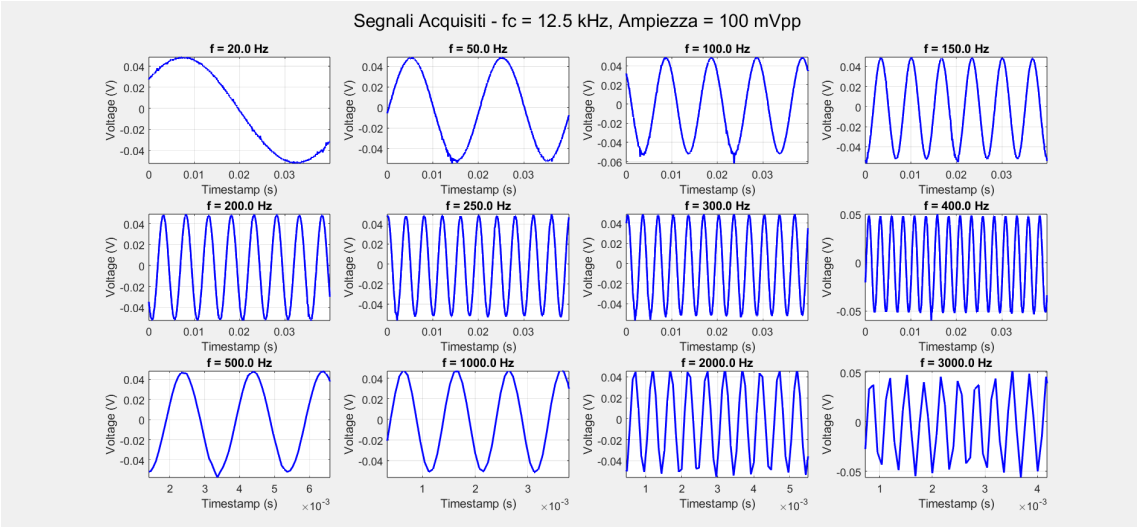

Figure 3.11: Acquired signal at 12.5 kHz, 100 mVpp

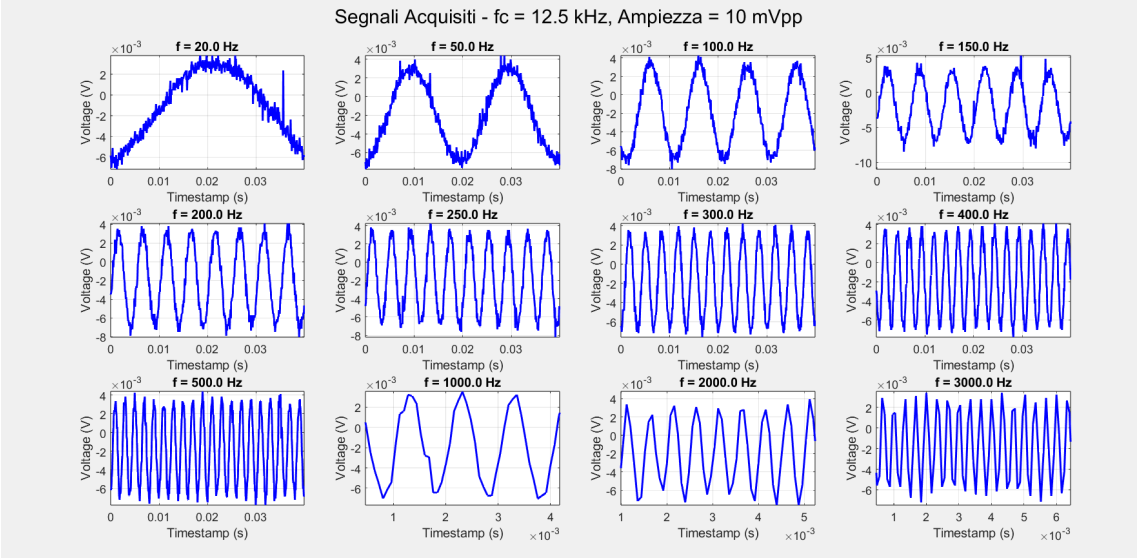

Figure 3.12: Acquired signal at 12.5 kHz, 10 mVpp

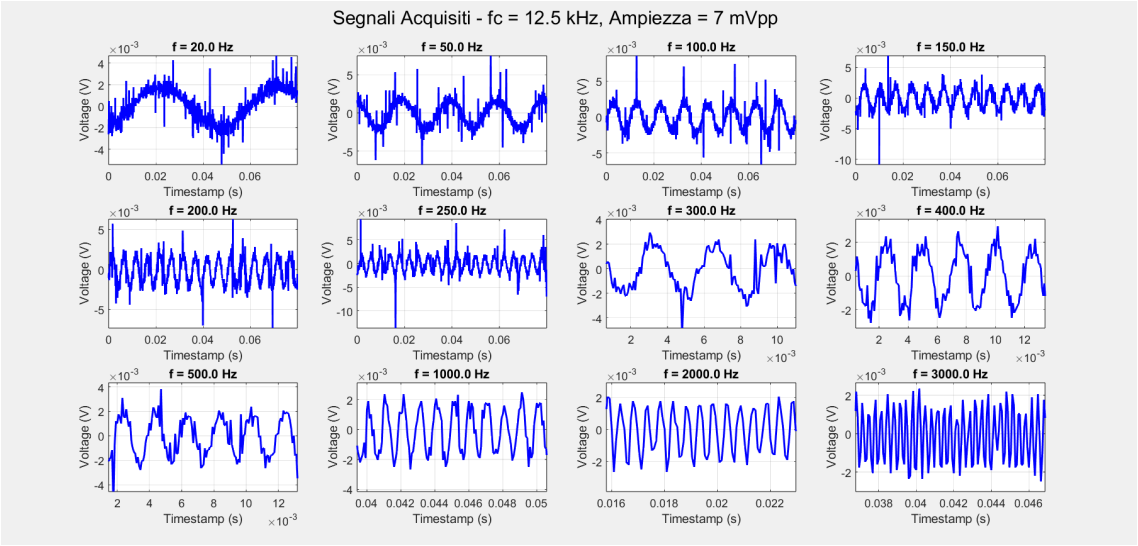

Figure 3.13: Acquired signal at 12.5 kHz, 7 mVpp

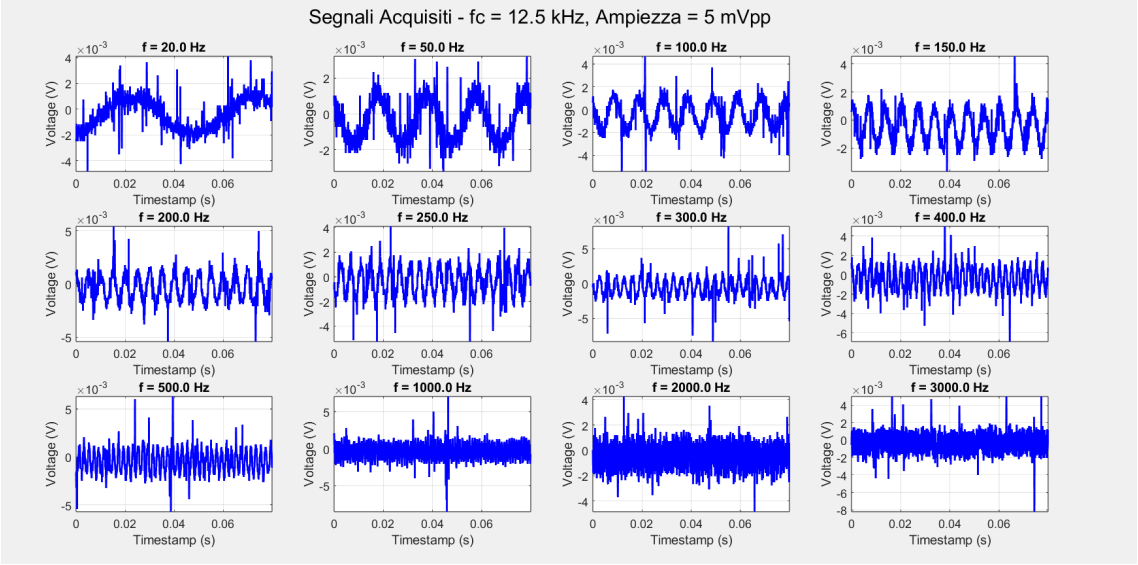

Figure 3.14: Acquired signal at 12.5 kHz, 5 mVpp

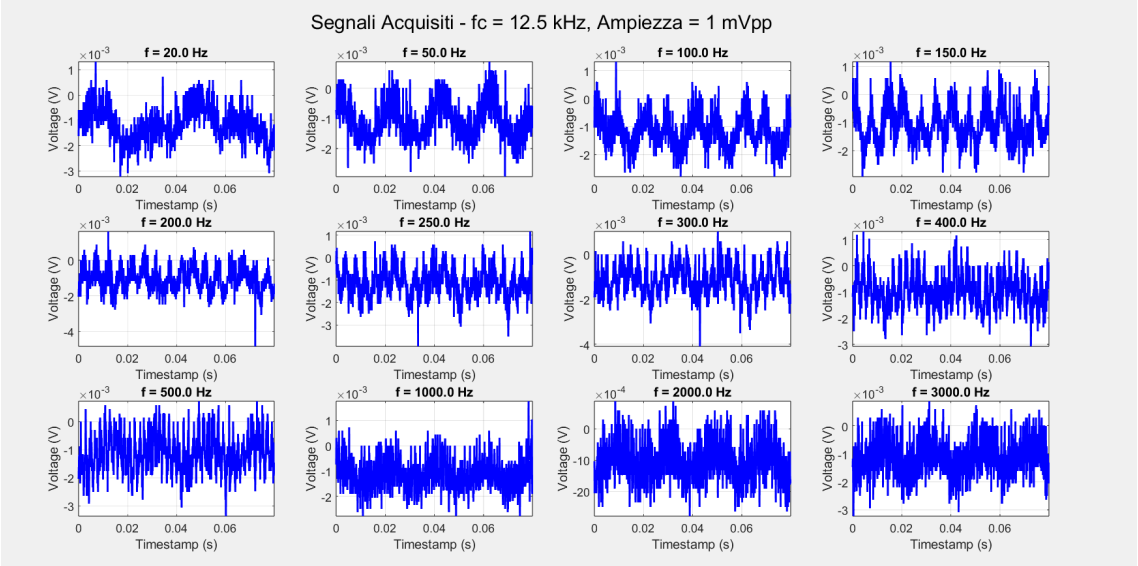

Figure 3.15: Acquired signal at 12.5 kHz, 1 mVpp

3.1.4 Evaluation of Sampling Accuracy

To evaluate the accuracy of the acquisitions, we compared them with ideal sine waves and calculated the Root Mean Square (RMS) error. This metric helps quantify how much the acquired signal deviates from the theoretical one, allowing us to assess the quality of the sampling process. The RMS error is particularly important because it provides a direct measure of how much the acquired signal differs from the original one. This parameter is widely used in various applications, including signal sampling, digital filtering, and ADC performance evaluation.
If the RMS error is low, it means that the acquired signal closely follows the original, confirming good sampling accuracy. On the other hand, a high RMS error indicates a significant difference between the sampled and original signal, which could be

caused by aliasing, noise, or quantization errors. To compute the RMS error in MATLAB, we compared the acquired signal with an ideal sine wave. Specifically, we took the first 250 samples from both the sampled signal and the ideal sine wave, ensuring they had the same frequency and amplitude. The difference between these two signals represents the instantaneous error at each point. To avoid cancellation effects and give more importance to larger deviations, each error value was squared. Then, we calculated the average of these squared values, obtaining a single number that represents the mean squared error.
Since this value is still in squared units ($Volt^2$), we took the square root to express it in the same scale as the original signal amplitude. The final RMS error quantifies the average deviation of the sampled signal from the ideal one in Volts. In addition to amplitude differences, another key factor affecting the accuracy of the sampled signal is the phase shift. In an ideal scenario, a sine wave starts at zero, but the sampled signal often has a different initial phase due to the sampling process and hardware delays. To account for this, a phase estimation step was included in MATLAB. The initial phase of the sampled signal was estimated based on the first two acquired samples and applied to the ideal sine wave before calculating the RMS error. This correction ensures a more accurate comparison by aligning the two signals in both amplitude and phase. The RMS error values were calculated in MATLAB by comparing the sampled signals with their ideal sine waves. These values show how much the acquired signal differs from the expected one.
Table 3.1 lists the RMS errors for different signal frequencies, helping us understand how accurate the sampling process is at different frequencies.

Table 3.1: RMS error values computed in MATLAB for different signal frequencies.

Frequency (Hz)	**RMS Error**
20	0.0053061
50	0.067098
100	0.052311
150	0.023981
200	0.0048858
250	0.021431
300	0.0060018
400	0.062849
500	0.022757
1000	0.010209
2000	0.065767
3000	0.036573

The plots in Figure 3.16 compare the sampled signal with the ideal sine wave at different frequencies. Up to 500 Hz, the sampled signal closely follows the theoretical waveform, showing minimal deviation. However, as the frequency increases beyond 500 Hz, noticeable discrepancies start to appear. These deviations are likely caused by quantization errors, phase shifts, and the limited number of sampling points available at higher frequencies.
At 1000 Hz and above, distortions become more evident, and at 2000 Hz and 3000 Hz, the sampled signal significantly deviates from the ideal wave, confirming the

challenges of accurate sampling at high frequencies.

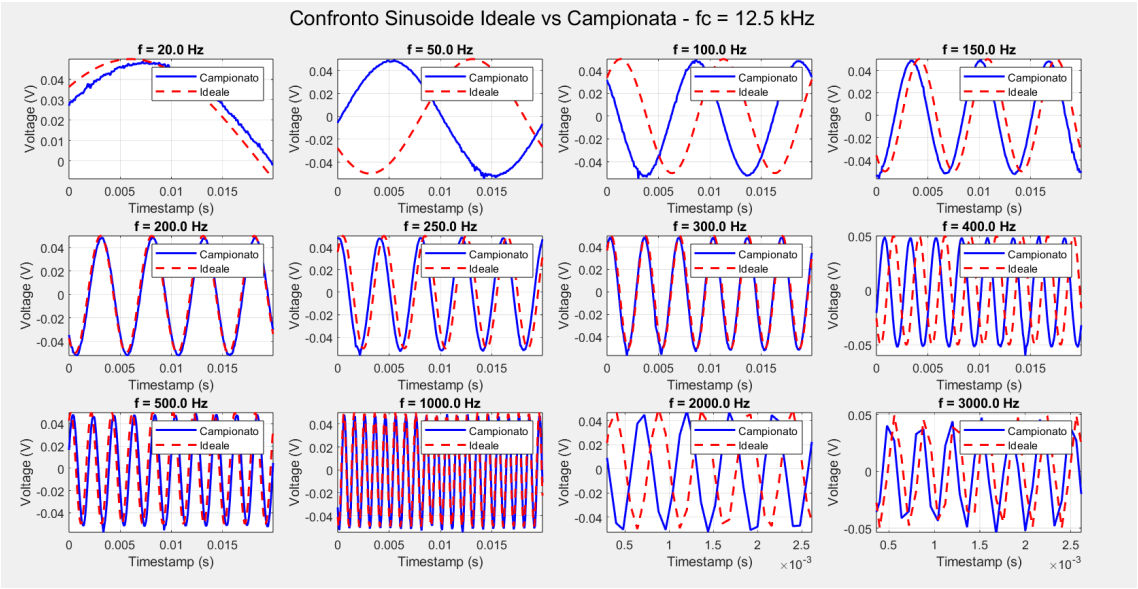

Figure 3.16: Comparison between the sampled and ideal sine wave at different frequencies (Author's own work)

Chapter 4

Discussion

4.0.1 Effects of Frequency on the Acquired Signal

The acquired signals show a clear relationship between input frequency and acquisition quality. At a sampling rate of 1 kHz, the system captures signals up to 125 Hz with good accuracy, maintaining a clean and well-defined sinusoidal shape. However, beyond 150 Hz, distortions begin to appear. Between 170 Hz and 250 Hz, the signal quality degrades further, and at 500 Hz, the waveform is no longer recognizable. This suggests that at 1 kHz sampling, the upper limit for accurate acquisition is around 125 Hz. Above this threshold, aliasing and other sampling artifacts become significant. This behavior aligns with the Nyquist theorem, which defines the theoretical maximum frequency that can be reconstructed as:

$$f_{\text{Nyquist}} = \frac{f_s}{2} = 500 \text{ Hz} \tag{4.1}$$

In theory, signals below this limit should be reconstructed accurately. However, distortions appear at 150 Hz, indicating that other factors contribute to signal degradation. The ADC conversion time, signal-to-noise ratio, and filtering strategy all play a role. The low-pass filter, dynamically set to $1.2 \times f_{\text{signal}}$, helps reduce high-frequency noise but does not fully prevent distortion above 125 Hz. Raising the sampling rate to 5 kHz noticeably enhances signal quality. The sinusoidal waveforms remain well-defined up to 500 Hz, demonstrating that a higher sampling rate improves the reconstruction of higher-frequency components. Within this range, no significant distortions are observed, confirming its suitability for the frequency band of interest in LFP analysis. At 12.5 kHz, the system successfully reconstructs sinusoidal signals up to 2 kHz. Tests conducted with a 100 mVpp input confirm that the system preserves the expected waveform. However, at lower amplitudes, noise becomes more dominant. When the input is reduced to 10 mVpp or 7 mVpp, the sinusoidal shape is still recognizable, but noise is increasingly present. At 5 mVpp, the signal is strongly affected, and at 1 mVpp, it is nearly indistinguishable from background noise. One reason for this difficulty at very low amplitudes is the limited resolution of the ADC. When a signal represents only a small fraction of the ADC's full-scale range, it is mapped onto a limited number of quantization steps. For example, a signal at 1/100 of the full-scale range is spread over just 40 ADC steps, increasing quantization distortion and making the waveform less accurate. Choosing

an appropriate sampling rate is essential to ensure accurate signal reconstruction. For low-amplitude signals, additional noise reduction techniques may be necessary to preserve signal integrity and minimize distortion.

4.0.2 Filtering Strategy for Improved Signal Clarity

To reduce high-frequency noise and enhance signal clarity, a dynamic low-pass filtering approach was implemented. Instead of a fixed cutoff frequency, the filter was set to $1.4 \times f_{\text{signal}}$, with a maximum limit of 300 Hz. This ensured effective suppression of unwanted components while preserving the integrity of the acquired waveform. A third-order Butterworth low-pass filter was chosen because of its smooth response, which reduces high-frequency noise without distorting the signal too much. This was especially useful for frequencies between 150 Hz and 500 Hz, where distortions were more noticeable. By adjusting the cutoff frequency dynamically, the filtered signals appeared cleaner, and aliasing effects were reduced. Despite the improvements, some limitations remained. For signals above 125 Hz, filtering helped reduce noise but could not fully correct distortions caused by the sampling process and ADC limitations. At 500 Hz, the signal weakened significantly due to the limited sampling rate and Nyquist constraint, making it almost completely hidden by noise. In the visual representation, the filtered signal is shown as a dashed blue line to make it easily distinguishable from the original waveform. The Butterworth filter was selected because of its smooth frequency response, which minimizes distortion while effectively reducing high-frequency noise. These results confirm that adaptive filtering improves signal clarity but is ultimately limited by the system's sampling rate and inherent noise. Future enhancements could involve advanced noise reduction techniques or higher-order filters to further improve signal quality.

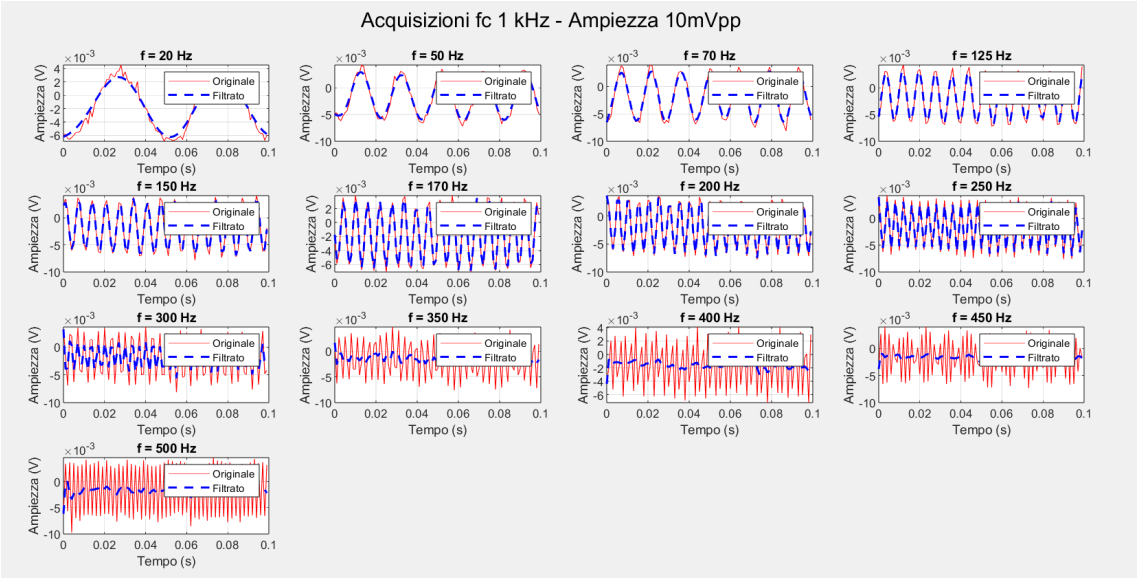

Figure 4.1: Acquired signals at 10 mVpp

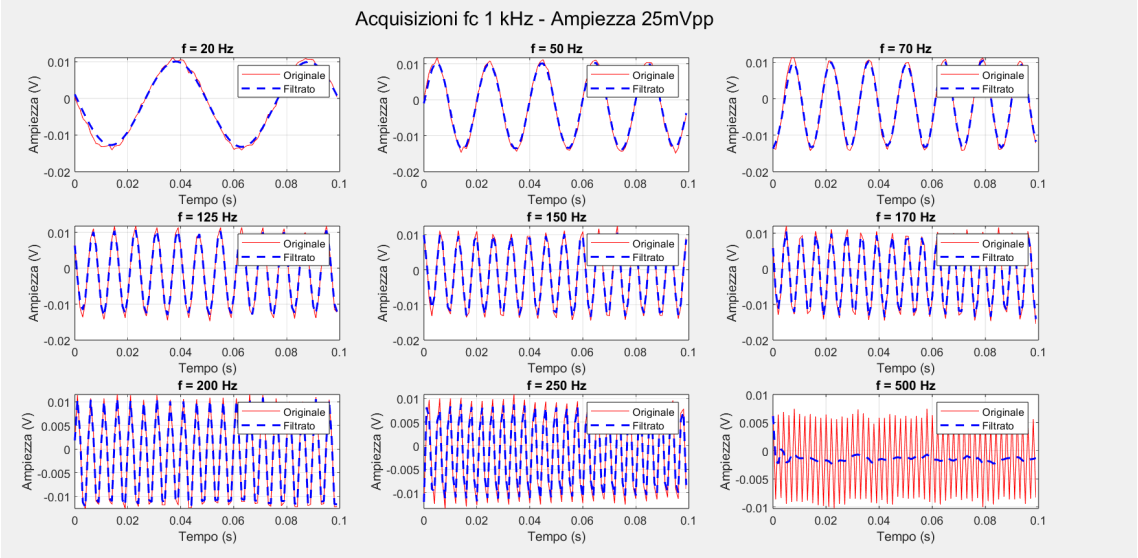

Figure 4.2: Acquired signals at 25 mVpp

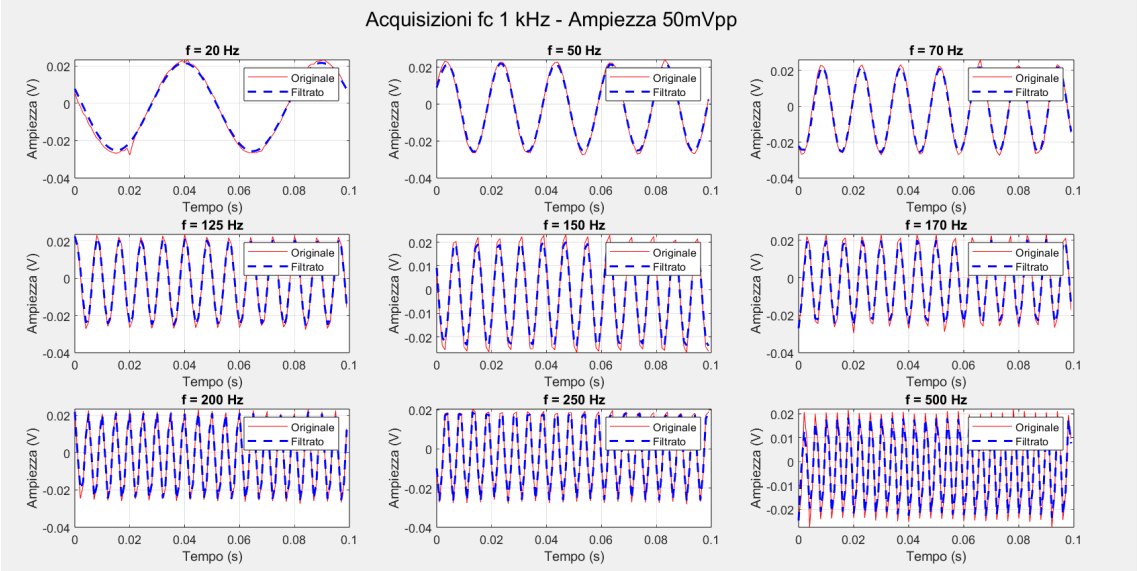

Figure 4.3: Acquired signals at 50 mVpp

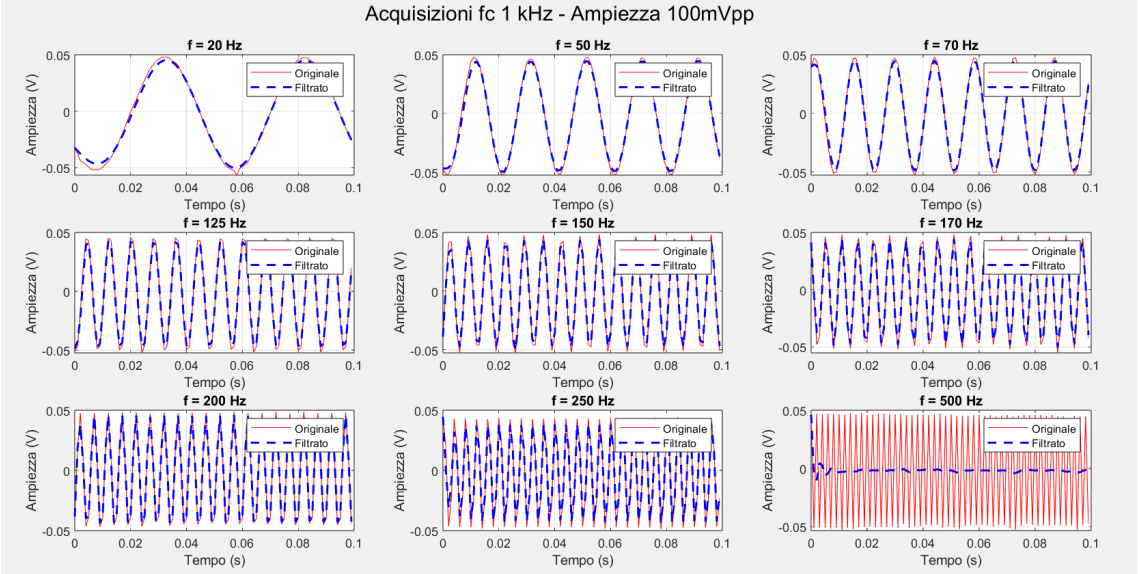

Figure 4.4: Acquired signals at 100 mVpp

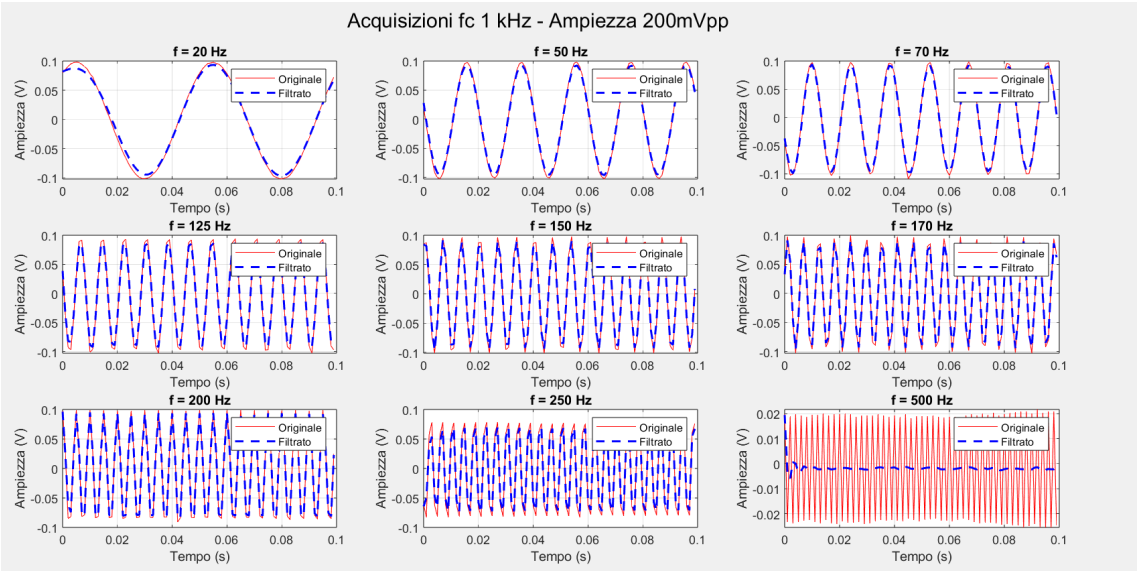

Figure 4.5: Acquired signals at 200 mVpp

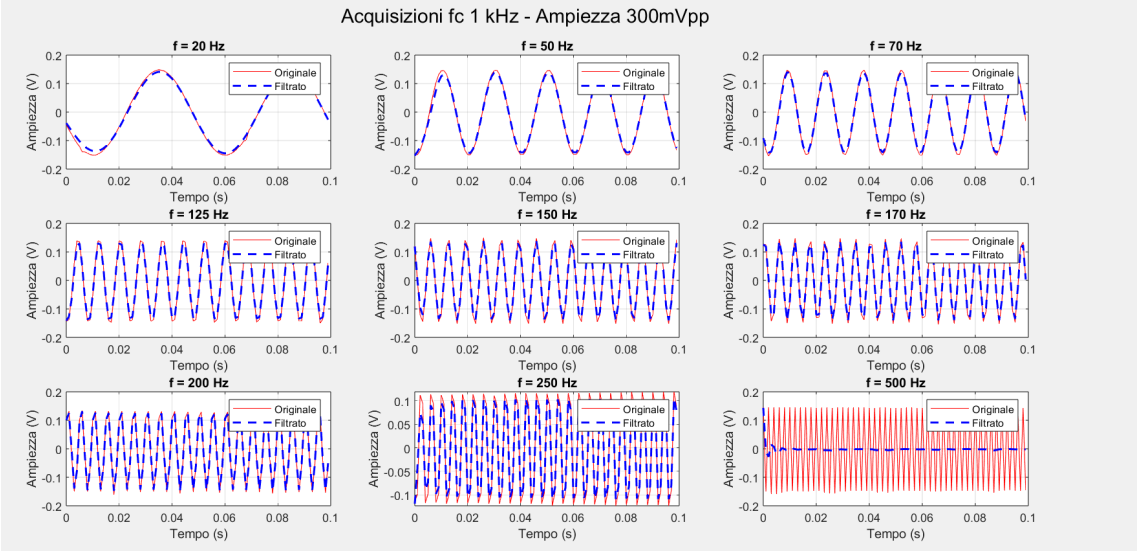

Figure 4.6: Acquired signals at 300 mVpp

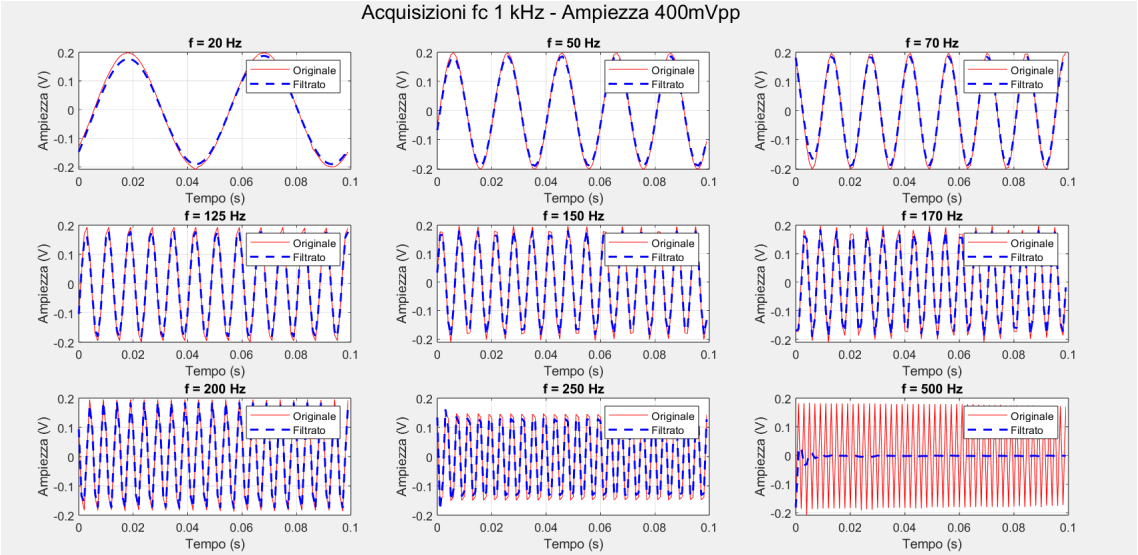

Figure 4.7: Acquired signals at 400 mVpp

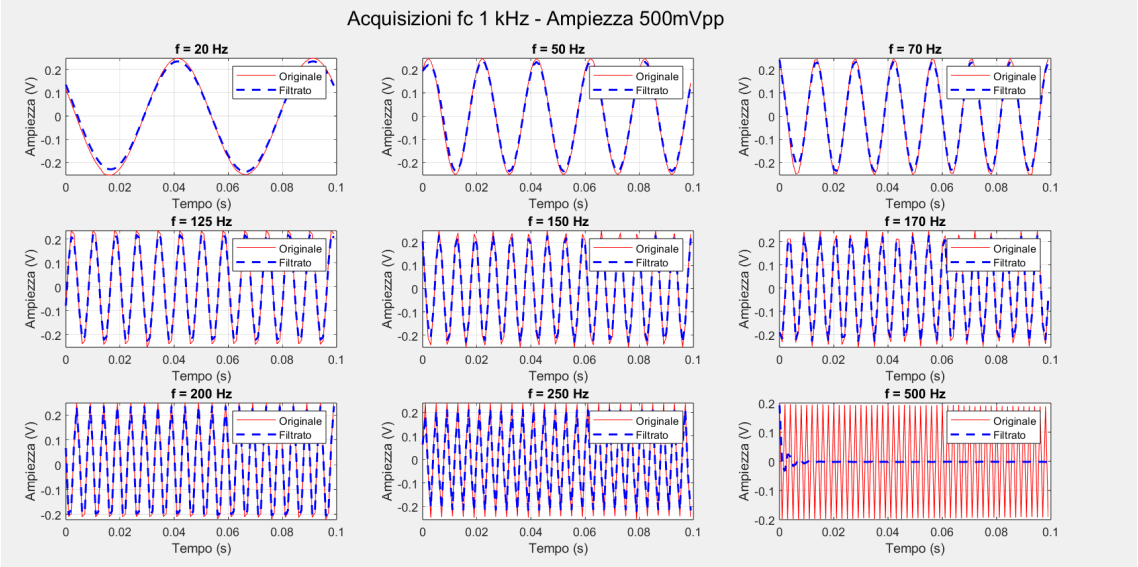

Figure 4.8: Acquired signals at 500 mVpp

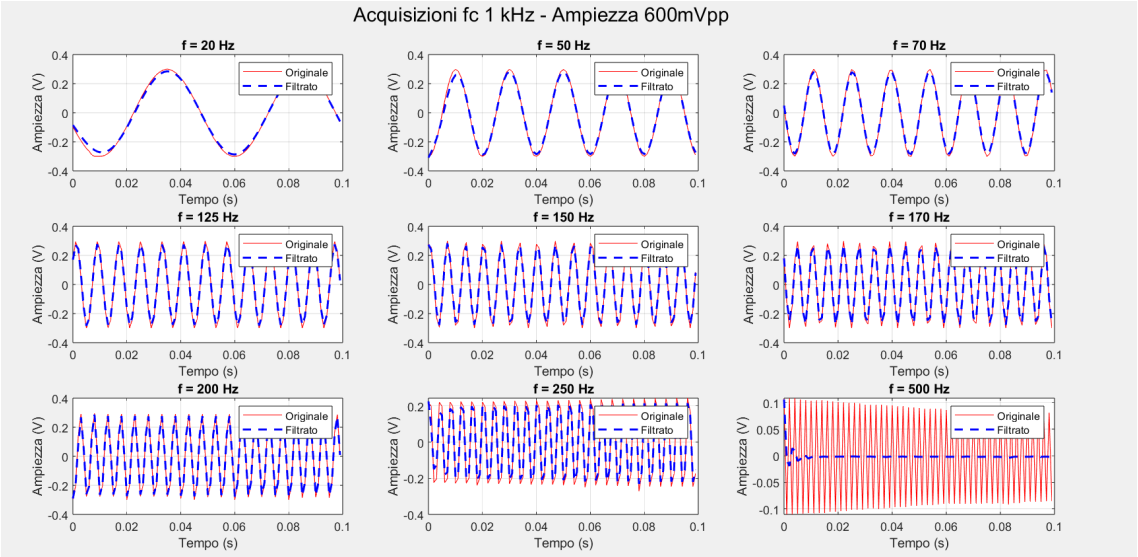

Figure 4.9: Acquired signals at 600 mVpp

4.0.3 Limitations in Low-Amplitude Signal Acquisition

Acquiring low-amplitude signals at 12.5 kHz presents several challenges. In the performed tests, signals with amplitudes of 10 mVpp, 7 mVpp, 5 mVpp, and 1 mVpp showed significant degradation, making it difficult to distinguish the waveform from background noise. This happens because the ADC has limited resolution, low-amplitude signals are more affected by quantization noise, and they are more easily disturbed by external interference. To find the cause of the problem, a Hantek signal generator was used, which can produce signals as low as 2 mVpp. The goal was to check if the issue came from the signal source. However, even with this generator, the waveforms still had noise, confirming that the problem was not due to the previous signal source. A passive voltage divider was also tested to systematically reduce

the signal amplitude. Since a 100 mVpp sine wave was clearly visible, a resistive divider was built using two 100 $k\Omega$ resistors and two 1 $k\Omega$ resistors to proportionally scale down the signal. However, even with this setup, the acquired waveforms were still heavily distorted, with noise overpowering the expected sinusoidal shape. Despite this setup, the acquired waveforms remained highly degraded, with noise overwhelming the expected sinusoidal pattern. There are several ways to improve signal quality and system performance. One option is to use software techniques like adaptive filtering or baseline correction to reduce noise. Another approach is to add an amplifier and hardware filters to improve the signal before digitization. Reducing interference from wired connections, such as by testing Bluetooth transmission, could also help minimize external noise. Other techniques, such as data compression, could optimize storage and transmission while preserving essential signal characteristics. Exploring multichannel acquisition might offer redundancy, allowing signal averaging to reduce noise artifacts. Finally, adjusting ADC parameters or using oversampling techniques could enhance precision in low-amplitude signal acquisition. These improvements could help overcome current limitations, ensuring better signal fidelity and more reliable recordings for further analysis.

Chapter 5

Conclusion

This work focused on developing and testing a system for acquiring low-frequency electrophysiological signals, addressing the challenges of detecting low-amplitude signals and optimizing data acquisition parameters. The system was evaluated under different sampling rates and signal amplitudes to assess its performance in real conditions. The results showed that increasing the sampling rate from 1 kHz to 12.5 kHz improved waveform reconstruction, especially for higher-frequency components. However, at very low amplitudes such as 1 mVpp, noise became a major issue, making it difficult to extract useful information. Several strategies were tested, including different filtering techniques and hardware adjustments, but noise remained a key limitation. These findings emphasize the need for better signal preprocessing and hardware optimization to improve acquisition quality. Despite these limitations, the study provided useful insights into the challenges of low-amplitude signal acquisition and potential improvements. Future work could explore advanced noise reduction methods, such as adaptive filtering and signal averaging, as well as integrating hardware amplifiers to enhance the signal-to-noise ratio. Alternative ADC configurations and wireless data transmission methods could also be investigated to optimize system performance. In summary, this study highlights the balance between different factors in electrophysiological signal acquisition and provides a foundation for future developments to enhance the accuracy and reliability of low-amplitude signal measurements.

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