POLITECNICO DI TORINO

Department of Electronics and Telecommunications
Master Degree in Electronic Engineering

Thesis in Integrated System Technologies

The use of FinFET and UTBB technologies for the realisation of analog and RF structures

Supervisors:
Prof. Gianluca PICCININI
Doct. Fabrizio MO
Doct. Roberto LISTO

Candidate:
S302412 - Ten. Marco FALCO

2023 -2024

To my family
To my friends
To myself

Abstract

This thesis explores the potential of replacing traditional MOSFET technology with FinFET devices, focusing on performance improvements in digital and analog applications. The study analyses FinFET's advantages over MOSFETs, particularly regarding power efficiency, speed, and scalability in advanced semiconductor nodes. Emphasis is placed on FinFET's enhanced control over SCE due to its three-dimensional gate structure, which reduces leakage currents and improves overall device performance.

In addition to comparing the fundamental characteristics of MOSFET and FinFET technologies, the thesis also examines the impact of FinFET geometry, including parameters such as H_{FIN}, W_{FIN} and AR, on device performance. Special attention is given to the implications of these geometric factors on analog circuit design, such as VCOs and LNAs.

The research extends to real-world implementations and simulations, demonstrating how FinFET technology can be leveraged in RF applications. The work also investigates future trends, such as using nanosheet and nanowire devices, which promise to improve analog and RF circuits' capabilities. Additionally, this study highlights the importance of precise electrical measurements and model extraction techniques necessary for accurate FinFET-based analog designs.

Ultimately, the thesis concludes that while FinFET technology presents significant advantages, carefully considering design parameters, material choices, and fabrication processes is essential for fully realising its potential to replace MOSFETs in modern electronics. The experimental results and simulations offer insights into the future trajectory of FinFET integration into both digital and analog circuits.

Summary

This thesis analysed the chance to substitute the solid, but old MOSFET technology with a more recent FinFET one. The elaboration is divided into two main parts. The first one tries to expose a general view of the argument with the support of several papers. The first chapter offers a general introduction to understanding the following sections. Main parameters are introduced in subsections from one to eleven of the first section. The second section exposes the comparison made in the paper [SD06]. In the first subsection, the focus is the digital performance, and in the second the analog. In the third the impact of the series resistance. Then VCO and LNA realised. Both the devices were tested in the fourth. All the third section is based on [PWBVKSJBMDDLVDHD07]. The subsections briefly overview different analogue components and their FinFET implementation. In the last section, the importance of spacing [;12]. In the second chapter, the actual situation is exposed. The first section focuses on the role of geometry at the same wavelength as the first chapter's latter section. It is based on [SS15]. In the first subsection a general overview, then in the second the effects of H_{FIN}, in the third of W_{FIN} and in the fourth of AR. The second section takes a look at step FinFET technologies. The analysis is based on [RT17]. The first subsection is related to analog, second to RF and third to digital parameters. The third section investigates the realisation of the RF FinFET of [LS18]. The study results are in the first subsection and the second focus on a deep n-well analog device. The last section exposes FinFETs with different drain extension designs based on [HC18]. Chapter three is the last of the chronological-like examination. This chapter indicates the possible next technological steps in the analog field. In the first section, nanosheet devices are considered [YB20]. The second explains the importance of extensive electrical measures [RF21], motivating why and how to extract the parameters to make a RF analysis in the various subsections. The third section introduces nanowires [RR22] and then analyses the impact of L_G, subsection one, geometrical parameters, subsection two, surface orientation, subsection three and multichannel stacks, subsection four. Chapter four tries to answer some additional questions. The first section deeply investigates the differences between MOSFETs and FinFETs. The first subsection considers the materials, the second one the fabrication processes, the third, dimensions and geometries, the fourth makes some design consideration and then in the Fifth some examples from [YB20], [RF21], [RR22] and [Try]. In the second section, the question was how to realise an analog circuit with a Finfet so, as in the previous, some considerations were made. In the first subsection, performance is taken into account, in the second, design considerations, in the third, layout techniques, in the fourth some extra points and

in the Fifth examples from [Che16] and [Try]. The third section lists several examples to show which model to use to simulate the circuits. The examples are taken from [KA07], [SS15], [RT17], [Sar18], [YB20], [RR22] and [Try]. The second part of the elaboration is meant to expose the experimental part. The first chapter lists all the instruments used. In every section, the analysed tool is deeply described. In the second chapter, the various simulations are discussed. The first section shows how to import a VerilogA model. Then in the second how to test an n-FinFET. In the third, the beginning circuit realised, a common source amplifier taken from [Try].

Acknowledgements

Contents

List of Tables

List of Figures

List of Symbols

A_V Voltage Gain. 8, 12–14, 17, 18, 33–35, 41, 44, 45, 49, 65, 66, 69, 87, 88, 91, 98, 99, 109–116

C_{EPI} EPI-to-gate Capacitance. 57, 58

C_{GD} Gate-Drain Capacitance. 16, 18, 58, 89, 93–96, 109

C_{GG} Total Gate Capacitance. 14–16, 61, 66, 71, 72, 74, 78, 92–96, 106

C_{GS} Gate-Source Capacitance. 44, 58, 89, 90

C_G Gate Capacitance. 16, 18, 71, 78, 90, 109, 111, 113–116, 122

C_{IF} Inner Fringe Capacitance. 57, 58

C_{INNER} INNER Capacitance. 105

C_{OF} Outer Fringe Capacitance. 57, 58, 92, 93

C_{OUTER} OUTER Capacitance. 105

C_{OUT} OUTput Capacitance. 79

C_{OV} Overlap Capacitance. 57, 92, 93

C_{OX} OXide Capacitance. 8, 38, 39

C_{PARA} Parasitic Capacitance. 57, 58, 93, 94

C_{SUB} Substrate Capacitance. 100

D_{NW} Nano Wires Diameter. 112

F_0 Oscillation Frequence. 47

F_{MAX} MAXimum oscillation Frequency. 13, 15–18, 51, 58, 82–85, 87–96, 105, 106, 109–111, 115, 116

F_M Offset Frequence. 47

F_T Cutoff Frequency. 12–18, 41, 44, 46, 51, 58, 59, 61, 66, 67, 71, 72, 74, 78, 82–85, 87, 89–96, 105, 106, 109–116

$V_{TH,sat}$ THreshold Voltage at SATuration. 8, 12, 33, 37, 41, 42

V_{TH} THreshold Voltage. 13, 14, 20, 34, 36–38, 42, 44, 45, 63, 64, 68, 75, 88, 93, 97, 155, 156, 161

V_T Thermal Voltage. 12, 39, 43, 44, 85

W_{FIN} EFFective Width. 57, 58, 84, 91–94

W_{FIN} Width of FINs. 4, 5, 9, 13, 14, 41, 43, 50, 56, 57, 61, 63–72, 74, 92, 93, 96, 97, 112, 116, 118

W_{NS} Nano Sheets Width. 16, 92, 94–96, 112

$\frac{1}{f}$ Flicker noise. 16, 84, 86, 140

μ_{EFF} effective electron mobility. 18, 114, 115

Acronyms

AC Alternate Current. 46, 94, 100, 153, 159

ADE Analog Design Environment. 139, 150

AR Aspect Ratio. 4, 5, 9, 15, 59, 61, 72, 73

BEOL Back End Of Line. 55, 56, 101

BJT Bipolar Junction Transistor. 8, 35, 39, 70

BOX Buried OXide. 40–42, 74, 99–101, 121

CET Capacitance Equivalent Thickness. 41

CIW Command Interpreter Window. 19, 145

CLM Channel Lenght Modulation. 8, 33, 34, 39, 43, 64, 66, 68, 77, 78, 99

CMOS Complementary Metal-Oxide-Semiconductor. 49, 51, 53, 64

CPP Contacted Poly Pitch. 91

DC Direct Current. 55, 91, 94–96, 104, 126, 156, 157, 159, 161

DG Double Gate. 64

DGC Double-side Gate Contact. 15, 83

DIBL Drain Induced Barrier Lowering. 18, 64, 66, 84, 99, 108, 109, 111–113, 140

DRC Design Rule Checking. 138

EDA Electronic Device Automation. 122, 138

EOT Equivalent Oxide Thickness. 62, 74

ERC Electrical Rule Checking. 138

ESD ElectroStatic Discharge. 49

FD Full Depleted. 100

FD-SOI Fully Depleted Silicon On Insulator. 17, 64, 99, 101–103, 106, 119

FEOL Front End Of Line. 91

FET Field-Effect Transistor. 8, 34–37, 39, 59, 61, 81, 85

FoM Figure of Merit. 41, 42, 47–49, 103, 106, 110

GBW Gain BandWidth. 52–54

GFP Gain Frequency Product. 78

ggnMOS Gate-Grounded Metal-Oxide-Semiconductor. 49

GIDL Gate Induced Drain Leakage. 140

GIFBE Gate Induced Floating Body Effect. 104

HCI Hot Carrier Injection. 140

HDD Highly Doped Drain. 40

HiK HIgh K. 40–42, 51, 62

I/O Input/Output. 16, 81, 84, 85

IP3 $3^{RD} Intercept Point$. 49, 88

ITP Intrinsic Transistor Performance. 41

ITRS International Technology Roadmap for Semiconductor. 54

LD Drain Lenght. 62

LDD Low Doped Drain. 87

LNA Low Noise Amplifier. 4, 9, 46, 48, 49, 55, 125, 126

LO Local Oscillator. 51

LS Source Lenght. 62

LVS Layout VS Schematic. 138

MG Metal Gate. 40, 42, 64, 92–96

MiM Metal Insulator Metal. 50

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor. 4, 5, 8, 17, 33–46, 48, 49, 55, 56, 62, 64, 70, 72, 99, 102, 109, 110, 112, 119, 159

NF Noise Figure. 49, 55

NS Nano Sheet. 18, 92, 94–96, 107–116, 118, 120

NTV Near Threshold Voltage. 126

NW Nano Wire. 18, 96–99, 101, 107–116, 120

OTA Operational Transconductance Amplifier. 9, 52, 53

P Power consumption. 47, 54

PN Phase Noise. 47, 56

PTS Punch Throught Stopper. 118

PVT Process Voltage Temperature. 139

Q Quality factor. 48, 50, 55, 56

RF Radio Frequency. 4, 5, 11, 18, 44, 50, 55, 58, 79, 81, 85–87, 91, 96, 103, 105, 106, 109–116, 118, 119, 122, 125, 126, 138

RMG Replacement Metal Gate. 15, 83

S/D Source/Drain. 40, 43, 49, 56–58, 74, 82, 92–95, 105, 118, 140

SCE Short Channel Effect. 4, 36, 39, 50, 61, 63, 64, 66–70, 72, 75, 84, 92, 94, 96, 97, 99

SEG Selective Epitaxial Growth. 56, 58

SGC Single-side Gate Contact. 15, 83

SH Self Heating. 99–103, 140

SLVT Super Low Threshold Voltage. 85

SoC System on Chip. 138

SOI Silicon On Insulator. 42, 50, 56, 101, 119

SS Subthreshold Slope. 8, 12, 18, 33, 39, 41, 42, 64, 97, 111, 112

STI Shallow Trench Isolation. 16, 85

SUB SUBstrate. 100, 101

TDDB Time Dependent Dielectric Breakdown. 140

TEM Transmission Electron Microscopy. 118, 119

TGF Transconductance Generation Factor. 13–15, 65, 70, 77

TLP Transmission Line Pulse. 49

ULVT Ultra Low Threshold Voltage. 85

UTBB Ultra Thin Body and Buried oxide. 99, 101

UWB Ultra Wide Band. 51

VCO Voltage Controlled Oscillator. 4, 9, 12, 46–48, 55, 56, 125, 126

VEA EArly Voltage. 8, 14, 20, 33, 39, 40, 44, 65, 66, 70, 99, 157

Consider ye the seed from which ye sprang;
Ye were not made to live like unto brutes,
But for pursuit of virtue and of knowledge.

[Henry Wadsworth Longfellow,
Quoting Dante Alighieri]

Part I

Theory

Chapter 1

General introduction

1.1 Planar Bulk MOSFETs vs FinFETs

Before starting with the practical part of my thesis, I have researched the fundamentals of using a FinFET in an analogic circuit. I structured it in such a way as to start from the past and evaluate technological evolution up to the current state of the art. Let's start with the first steps, planar bulk MOSFETs versus FinFETs. Based mainly on two papers from 2006 [SD06] and 2007 [GJM05] a rough comparison was carried out between the two technologies evaluating parameters such as:

- Transconductance (G_M);
- Output conductance (G_{DS});
- Voltage Gain (A_V);
- ON current (I_{ON});
- OFF current (I_{OFF});
- THreshold Voltage at SATuration ($V_{TH,sat}$);
- Single gate material work function;
- Parasitic capacitance/oxide capacitance (Cb/Cox);
- Subthreshold Slope (SS);
- Channel Lenght Modulation (CLM);
- EArly Voltage (VEA);
- Speed.

1.1.1 Transconductance (G_M)

G_M is a key parameter in the context of amplifiers and transistors. It represents the relationship between a device's output current and input voltage. It indicates how effectively a device can control current flow based on an input voltage. It is expressed as:

$$G_m = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \tag{1.1}$$

It is typically expressed in Siemens (S) or Amperes per Volt (A/V). A higher G_M generally indicates that the device can amplify better. The G_M can vary with the operating point of the device. Also, temperature can affect its value due to the effect on the carriers' mobility. In a MOSFET, G_M is defined as:

$$G_m = \frac{2I_D}{V_{GS} - V_{TH}} \tag{1.2}$$

where I_D is the Drain current, V_{GS} is the Gate-Source Voltage, and V_{TH} is the THreshold Voltage.

1.1.2 Output conductance (G_{DS})

G_{DS} is a parameter of FETs and similar semiconductor devices. It is the change in I_D concerning a change in the V_{DS}. V_{GS} has to be kept constant. It can be expressed as:

$$G_{DS} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}\text{ const.}} \tag{1.3}$$

In the saturation region of a MOSFET, the G_{DS} can be thought of as a measure of CLM, where an increase in V_{DS} leads to a slight increase in I_D. A lower G_{DS} is desirable in amplifier applications, leading to better A_V. A higher G_{DS} reduces linearity and increases distortion in analog applications. In many applications, G_{DS} can be related to the G_M and the R_{OUT} through the relation:

$$R_{OUT} = \frac{1}{G_{DS}} \tag{1.4}$$

1.1.3 Voltage Gain (A_V)

A_V measures the amplification or attenuation of a V_{IN} signal by an electronic circuit, such as an amplifier. It is defined as the ratio of the V_{OUT} to the V_{IN} of the amplifier. The formula for Voltage Gain is given as:

$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{1.5}$$

A_V is a dimensionless quantity often expressed in decibels (dB) for better understanding. The conversion to decibels can be done using the formula:

$$A_v(dB) = 20\log_{10}(A_v) \tag{1.6}$$

If:

- $A_V > 1$ or $A_V(\text{dB}) > 0$, the circuit amplifies the input signal.
- $A_V < 1$ or $A_V(\text{dB}) < 0$, the circuit attenuates the input signal.
- $A_V = 1$ or $A_V(\text{dB}) = 0$, the input signal is neither amplified nor attenuated.

A_V can vary depending on the type of amplifier (inverting, non-inverting, common emitter, etc.) and the specific component configurations. It changes with frequency, leading to a response curve important in the design and analysis of electronic circuits.

1.1.4 ON current (I_{ON})

In a transistor, particularly in the context of BJTs and FETs, the term on current, often denoted as I_{ON}, refers to the current flowing through the device when it is in the "on" state, meaning it is actively allowing current to pass from the collector to the emitter (in BJTs) or from the drain to the source (in FETs).

BJTs

In a BJT, when the base-emitter junction is forward-biased (the base receives a sufficiently positive voltage relative to the emitter for an NPN transistor), the transistor is considered "on." The key characteristics of I_{ON} in this context include:

- **Input Current (I_B)** A small input current flows into the base terminal;
- **Output Current (I_C)** A larger current flows from the collector to the emitter due to the transistor action.
- **Saturation Region** When the BJT is forced into saturation, I_{ON} is greatest, and the transistor allows for a large current to flow through it with minimal voltage drop across it.

The relationship can be illustrated as:

$$I_C = \beta \cdot I_B \tag{1.7}$$

Where I_C represents the collector current (equivalent to I_{ON} when the transistor is saturated) and β the current gain.

FETs

For Field-Effect Transistor (including MOSFETs):

- V_G The transistor is "on" when a sufficient voltage is applied to the gate terminal (relative to the source for enhancement mode MOSFETs).
- **Channel Formation** This voltage creates an inversion channel allowing current to flow between the drain and source terminals.
- I_D In the linear or saturation region, the I_D (which represents I_{ON}) will depend not only on the V_G but also on the characteristics of the MOSFET (such as its V_{TH}, G_M, etc.).

In the case of a MOSFET, the relationship can be simplified for the saturation region as:

$$I_D = k \times (V_{GS} - V_{th})^2 \tag{1.8}$$

Where:

- I_D is the Drain current;
- **k** is a constant that depends on the device characteristics;
- V_{GS} is the Gate-Source Voltage;
- V_{TH} is the THreshold Voltage.

1.1.5 OFF current (I_{OFF})

It is a small current flowing through a transistor while is in the off state. In this state, the transistor is not active. The V_{GS} Has to be below the V_{TH}. I_{OFF} is generally very small compared to the I_{ON}. Generally expressed in nA or μA. However, its magnitude can vary based on temperature, supply voltage, and the specific transistor technology. It is often considered a form of leakage current. In practical applications, especially in low-power devices, this leakage can significantly influence overall power consumption, as it represents the current that flows even when the transistor is not actively switching. The off current tends to increase with temperature due to the increased carrier generation and reduced mobility of charge carriers in the semiconductor material. Therefore, thermal management is crucial in high-frequency or high-density integrated circuits where transistors may operate near their limits. In FETs, even below the V_{TH}, the device allows some current to flow due to subthreshold conduction. This conduction is exponential vs V_{GS}, leading to sensitivity in leakage in low-voltage applications. As transistors are scaled down in size for modern applications (like in CMOS technology), I_{OFF} becomes a critical parameter. Smaller transistors may exhibit increased leakage due to SCEs, which are particularly significant at nanometer scales. This can limit the benefits of scaling, such as reduced capacitance and enhanced performance. In digital integrated circuits, reducing I_{OFF} is important to reduce static power consumption, especially in idle states of transistors in active devices.

1.1.6 THreshold Voltage at SATuration ($V_{TH,sat}$)

The $V_{TH,sat}$ refers to a specific voltage in certain electronic devices, particularly for semiconductor devices. It is a critical parameter that indicates the transition point between different operational states of the device. When the V_{GS} exceeds a certain V_{TH}, the MOSFET turns on. Beyond a further increase in V_{GS}, the MOSFET enters the saturation region where it can maintain a steady current regardless of the V_{DS}, as long as V_{DS} is above a certain value known as $V_{DS,sat}$. The voltage required to create a conductive channel between the source and drain terminals is called V_{TH}. Here $V_{TH,sat}$ might sometimes be referred to in conjunction with this threshold when considering saturation effects. For amplifier circuits, $V_{TH,sat}$ may also refer to the minimum voltage at which the output avoids saturation distortion. The $V_{TH,sat}$ is crucial for designing circuits, as it helps define not only the operational limits of the device but also the stability and performance of the circuits designed around such components. $V_{TH,sat}$ can be determined from the device's transfer characteristics, which plot the I_D against the V_{GS} at a fixed V_{DS}.

1.1.7 Single gate material work function

The work function of a material is a critical parameter in semiconductor physics and materials science. It represents the minimum energy required to remove an electron from the surface of a material into the vacuum. In FETs, the work function can significantly influence the device's electrical characteristics, including the V_{TH} and the overall performance. For commonly used gate materials, the typical work functions are:

- **Silicon (n-type)** Approximately 4.05 eV;
- **Silicon (p-type)** Approximately 4.20 eV;
- **Aluminum** Approximately 4.1 eV;
- **Poly-Silicon (doped)** Typically between 4.0 to 4.5 eV;
- **Titanium** Approximately 4.33 eV;
- **Tungsten** Approximately 4.5 eV;
- **Gold** Approximately 5.1 eV;
- **Platinum** Approximately 5.3 eV.

The precise value of the work function can vary based on factors such as the material's surface conditions, crystallographic orientation, and any chemical treatments or coatings applied to the surface. The work function plays a role in devices' design for applications like quantum computing, photovoltaics, and sensors, where electron emission and transfer are critical. In practical applications, understanding and controlling the work function is essential to enhance device performance, reducing leakage currents, and improving overall efficiency.

1.1.8 Parasitic capacitance/oxide capacitance (Cb/Cox)

Parasitic capacitance (C_b)

Parasitic bulk capacitance (C_b) refers to the unintended capacitance within electronic components and circuits. This capacitance is not intentionally designed into the circuit but can arise due to physical layout, packaging, and the electrical characteristics of materials used. It often occurs in semiconductor devices, integrated circuits, and PCB traces where conductive pathways, insulating materials, and nearby components electrically interact. In microelectronics, Cb can be attributed to junction capacitances in transistors, oxide layers in MOSFETs, and the capacitance between silicon layers. It can affect the performance of high-speed circuits by introducing delays, signal distortion, and unintended coupling between signals. It can also lead to increased power consumption and noise in analog circuits.

Oxide capacitance (C_{OX})

It is the capacitance per unit area of the gate oxide in MOSFET devices. The gate oxide is a thin layer of insulating material (like silicon dioxide, SiO_2) between the gate terminal and the transistor's channel. It is represented by:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{1.9}$$

Where:

- C_{ox} is the oxide capacitance per unit area ($\mathrm{F/m^2}$).
- ϵ_{ox} is the permittivity of the oxide material. It is equal to $\epsilon_{ox} = \epsilon_0 \cdot \kappa_{ox}$, where ϵ_0 is the vacuum permittivity (approximately $8.85 \times 10^{-12}\,\mathrm{F/m}$) and κ_{ox} is the dielectric constant of the oxide. For SiO_2, κ_{ox} is typically around 3.9.
- t_{ox} is the thickness of the oxide layer (m).

As technology scales down, the thickness of the gate oxide layer decreases, which increases C_{ox} and allows for better control of the channel conductivity in MOSFET devices. However, very thin oxides can lead to reliability issues, such as gate leakage current.

Ratio

The ratio $\frac{C_b}{C_{ox}}$ can influence the performance of the MOSFET including V_{TH}, G_M, and overall device behaviour. A high ratio may indicate that the device is more susceptible to changes in the body potential, which can affect transistor operation, especially in analog applications. Values for $\frac{C_b}{C_{ox}}$ vary depending on the technology, fabrication processes, and specific device structure. In modern MOSFET technologies, this ratio could range widely and is often fitted for particular applications.

1.1.9 Subthreshold Slope (SS)

$$SS = \ln 10 \cdot V_T(1 + \frac{C_D}{C_{OX}}) \tag{1.10}$$

Where V_T is the Thermal Voltage, C_D is the depletion layer capacitance and C_{OX} is the OXide Capacitance. It is an important metric for the efficiency and performance of transistors The SS is the rate at which the current increases as the V_G is increased in the subthreshold region. It is measured in mV/decade. It describes how quickly a transistor can switch on when the V_G is below its threshold. For an ideal transistor, the SS is theoretically limited to 60 mV/decade at room temperature. This means that for every 60 mV increase in gate voltage, the I_D increases by a factor of ten (one decade). This limit arises from the thermionic emission theory. A lower subthreshold slope indicates better device performance, as it allows for faster switching and lower power consumption. This is particularly critical in modern applications like mobile computing and deep-submicron technology. Real-world transistors may exhibit a SS greater than 60 mV/decade due to physical effects such as SCEs, surface roughness scattering, and other non-idealities. These effects can degrade the electrical characteristics of the transistor. To achieve steeper SS, we need different materials and device architectures like Fin, Tunnel and negative capacitance FETs.

1.1.10 Channel Lenght Modulation (CLM)

A phenomenon observed in FETs where the V_{DS} increases in the saturation region. Despite what we can expect the effective channel length of the MOSFET decreases with higher V_{DS}. This reduction in effective channel length affects the current flowing through the device. Under normal saturation conditions, an increase in V_{DS} leads to an increase in the I_D due to CLM. With higher V_{DS}, the pinch-off point moves closer to the source. This results in a shorter effective channel length. The effective increase in I_D due to CLM is:

$$I_D \approx I_{D(0)}\,(1 + \lambda V_{DS}) \tag{1.11}$$

Here, $I_{D(0)}$ is the drain current at zero V_{DS}, and λ is the CLM parameter, which is related to the R_{OUT} of the device. In the output characteristics of a MOSFET, CLM can be observed as a slope in the saturation region rather than a flat characteristic. The curve will deviate slightly from horizontal as V_{DS} increases, indicating that I_D is sensitive to changes in V_{DS} due to CLM. CLM affects parameters such as gain, R_{OUT}, and linearity in analog applications.

1.1.11 EArly Voltage (VEA)

The concept of early voltage refers to a specific parameter in BJTs called the Early effect, named after its discoverer James M. Early. Often denoted as VEA, is a measure of the effect of V_{CB} on the width of the base region in a BJT. As the V_{CB} increases, it causes the base region to narrow slightly, which leads to an increase in the I_C. This effect is more pronounced in some transistors than others. Higher VEA indicates less sensitivity to V_{CB} changes. It's an important parameter in analog circuit design, especially for

current sources and amplifiers. Typical values range from about 15V to 150V for silicon transistors. VEA is often represented as the x-intercept of the extrapolated I_C- curves on a transistor's output characteristics graph. It is particularly important in High-gain amplifiers, current mirrors and cascode configurations.

1.2 Comparison

Wafers with a 145-nm BOX thickness have been used to build the [Bie04] FinFETs. Fin patterning produces fins with widths as small as 25 nm and heights of 60 nm. Then come spacer formation, HDD implant, HiK dielectric and TiN MG deposition, S/D extension implant, and Ni silicidation. For the FinFETs, neither channel doping nor pocket (halo) implants have been carried out. This is the procedure flow that [GJM05] describes:

1. Si film thinning;
2. Active litho and MESA etch;
3. H_2-anneal;
4. V_T adjust implants;
5. Well anneal;
6. Gate stack deposition;
7. Gate litho and etch;
8. Extension and halo implants;
9. Spacer deposition and etch;
10. HDD implants;
11. Spike anneal (1050°C);
12. Nickel Silicide.

Planar bulk MOSFETs have been fabricated on bulk p-type wafers with TaN as the MG and HfO_2 or SiON as the gate dielectric. Halo and S/D extension implants, spacer formation, HDD implantation, and Ni silicidation and backend flow have been performed after that. [Bie04] indicates the process flow description as follows:

1. STI isolation;
2. Gate stack deposition:
   (a) SiO_2 (1.4nm, 2.0nm, 2.5nm, 3.0nm, 3.5nm);
   (b) Plasma nitridation;
   (c) 20nm PVD TaN;

(d) MGI (optional);
(e) 100nm α-Si + PECVD oxide hard mask;
(f) 193nm litho + gate etch;

3. Pocket implant (Low, Med, Hi dose);
4. Extension implant (Low, Hi dose);
5. Low-temperature spacer (400°C);
6. HDD + 1030°C spike;
7. NiSi;
8. Back-end: level 1 metal.

With a CET of 1.8 nm, the FinFETs and the bulk MOSFETs were produced using the same backend procedures. The overlap capacitances are 0.5 and 0.3 fF/μm, respectively, and the gate-to-channel capacitance is 19 fF/μm^2. Both digital and analog FoM have been characterised to evaluate device performance. The ITP, $V_{TH,sat}$, and SS are among the digital-performance parameters. The primary analog-performance parameters consist of F_T, , G_M, and G_{DS}. Characterisations of physical lengths between 60 nm and 1 μm have been made, focusing on the 60-nm device. Where appropriate, the supplied data are width-normalized, and the V_{DS} is 1.2 V. The formula N_{FIN} (W_{FIN} + 2H_{FIN}) is used to determine the width of the FinFET. The Number of FINs, W_{FIN}, and H_{FIN} represent the Number of FINs, Width of FINs, and Height of FINs, respectively.

1.2.1 Digital performance

Because of a smaller gate leakage component, bulk MOSFETs with HiK dielectric are seen to have a substantially lower I_{OFF} than bulk MOSFETs with SiON dielectric. Moreover, it is seen that the I_{OFF} is much lower in the case of FinFETs, which is explained by a significantly lower component of junction leakage caused by the presence of the BOX layer.

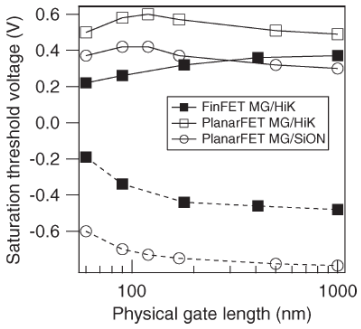


Figure 1.1. $V_{TH,sat}$ (V_{DS} = 1.2 V) versus physical gate length. [SD06]

FinFETs with MG and HiK exhibit lower values of $V_{TH,sat}$ (0.2–0.4 V), which is more acceptable for a 45-nm technology, compared to bulk MOSFETs with MG and HiK, which are seen to have $V_{TH,sat}$ between 0.5 and 0.6 V. This is because of the BOX layer and the fins' undoped nature, which both lower the voltage drop across the semiconductor. The consequence is a smaller V_{TH}, the total voltage drops between the semiconductor and oxide as the work function. With their intrinsically high V_{TH}s, HiK/MG stacks may benefit from this effect in the V_{TH} optimisation process. Additionally, it is observed that for fully depleted SOI technologies, acceptable work functions can be achieved with a single midgap gate material (such as TiN); however, when using a single gate material (in this case, TaN) for bulk MOSFETs, it can lead to unacceptably large V_{TH} for p-MOSFETs.

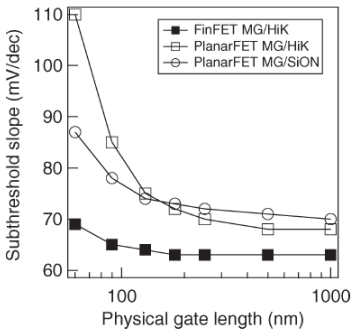


Figure 1.2. SS in saturation (V_{DS} = 1.2 V) versus physical gate length. [SD06]

FinFETs have superior SS values (less than 70 mV/dec) in comparison to bulk MOSFETs. This is explained because FinFETs with low body doping and the BOX layer present have a lower depletion charge. For the FinFET, the ratio Cb/Cox is 0.011, while for the bulk MOSFET, it is 0.1. FinFETs have a lower SS than bulk MOSFETs because of their smaller Cb/Cox.

1.2.2 Analog performance

The analog FoM shown below was assessed with gate overdrive VGS - Vt = 0.2 V and V_{DS} = 1.2 V. This is because a fair trade-off between speed and power consumption may be achieved at this biasing point since, at 0.2 - V_{OV}, the transistor is in strong inversion with G_M/I_D about $10V^{-1}$.

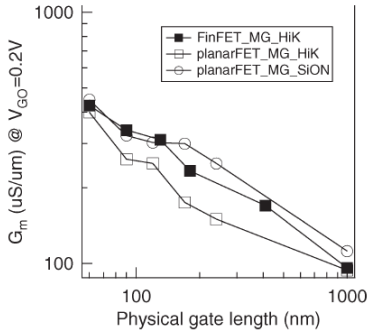


Figure 1.3. G_M at V_{DS} = 1.2 V and (V_{GS} - V_T) = 0.2 V. [SD06]

It is observed that G_M scales with L for bulk MOSFETs and FinFETs down to 60 nm. This suggests that the full velocity saturation has not yet occurred, as G_M would not scale with L in that scenario.

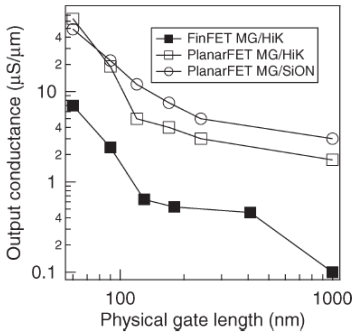


Figure 1.4. G_{DS} at V_{DS} = 1.2 V and (V_{GS} - V_T) = 0.2 V. [SD06]

FinFETs demonstrate more than an order of magnitude lower G_{DS} than bulk MOSFETs. The thin W_{FIN} and the gate wrapping around the fin on three sides cause the transistor body to be completely depleted. The body is already completely exhausted, therefore raising the V_D above pinch-off does not cause any more depletion. Consequently, the channel shortening caused by the growth of the depletion zone near the drain is represented by a low CLM. The change in I_D is likewise reduced due to the decrease in the electrical channel length; hence, the change in G_{DS}, which indicates the change in I_D with V_D, is also minimal. Compared to the FinFET, there is now less gate control over the channel when considering the bulk MOSFET. Furthermore, the bulk MOSFET is not completely depleted, opposite to the FinFET, which makes it more vulnerable to the effects of CLM and depletion region expansion. Furthermore, a halo (pocket) implant that creates a barrier at the S/D is present in the bulk MOSFET. This barrier increases G_{DS} by introducing an extra modulation by the drain, which is sensitive to the V_D.

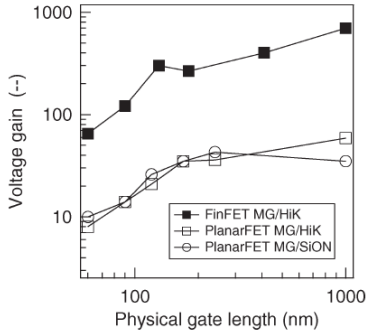


Figure 1.5. A_V at V_{DS} = 1.2 V and (V_{GS} - V_T) = 0.2 V. [SD06]

In quantitative terms, a greater VEA can be used to explain the FinFET's lower G_{DS} in comparison to the bulk MOSFET. It has been demonstrated that the halo (pocket) implant's barrier height modification can also lessen the VEA. Moreover, the halo lack of FinFETs results in a greater VEA. The FinFET has a lower G_{DS} and a greater VEA than a bulk MOSFET for all the reasons mentioned above. For an overdrive of 0.2 V, the intrinsic F_T ($= \frac{G_M}{2\pi C_{GS}}$) provides a high-frequency performance measure.

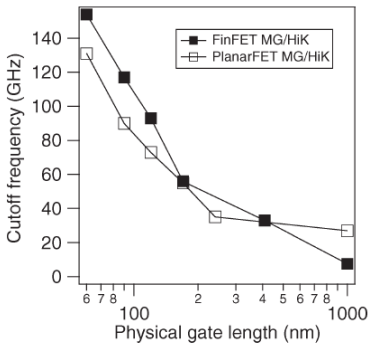


Figure 1.6. F_T at V_{DS} = 1.2 V and (V_{GS} - V_T) = 0.2 V. [SD06]

Because of their comparable G_M and C_{GS} values, FinFETs and bulk MOSFET are seen to display similar F_Ts in this region. FinFETs have not shown any discernible deterioration in noise or linearity when compared to planar bulk MOSFETs. From the above, it can be inferred that FinFETs have similar F_T and greater compared to planar bulk MOSFETs for analogue levels of noise and linearity, around a V_{GS} - V_{TH} of 0.2 V, which is ideal for low-power analog/RF design.

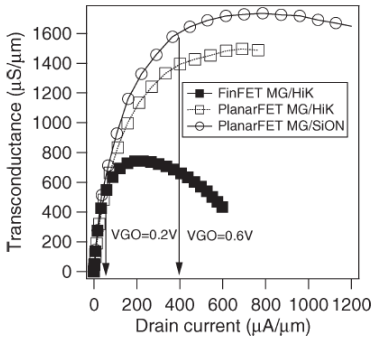


Figure 1.7. G_M vs I_D for V_{DS} = 1.2 V and increasing V_{OV}. [SD06]

It can be observed that up to V_{GS} - V_{TH} = 0.3 V, the G_M of the FinFET and bulk MOSFET are the same. Beyond this, there are differences between the FinFET G_M and the bulk MOSFET. The decline in G_M leads to a decline in and the G_M-to-I_D ratio. Analog performance in the high current regime may also be seen as a plot of at $G_{M,max}$ (A_V@$G_{M,max}$) against $G_{M,max}$.

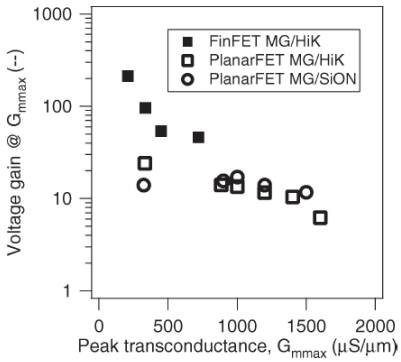


Figure 1.8. A_V vs peak G_M at V_{DS} = 1.2 V. [SD06]

The trade-offs between speed and gain that may be made with the MOSFET and FinFET designs, together with their advantages and disadvantages, are displayed in this plot: Although the FinFET has a large A_V, the greatest G_M that can be achieved is limited by its high series resistance. Conversely, bulk MOSFETs can yield large G_M values; nevertheless, their inadequate gate control over the channel leads to a decrease in
.

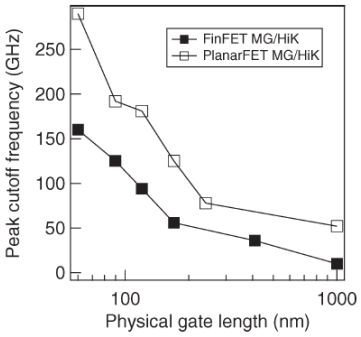


Figure 1.9. peak F_T at V_{DS} = 1.2 V. [SD06]

Bulk MOSFETs is observed to have a greater F_T, which makes it appealing for high-frequency applications.

1.2.3 Impact of Series Resistance

Reduced gate-source and effective V_{DS} across the transistor channel significantly affect the parasitic series resistance. The real V_{GS} across the channel for an applied V_{GS} of 1.2 V is only 0.9 V, with the remaining 0.3 V appearing across the parasitic resistance. This degrades analog and digital performances (driving current and G_M). At overdrives of 0.2 and 0.6 V, the R_{OUT} of the 60-nm FinFET is found to be 30 and 10 kΩ, respectively. This is significant compared to the parasitic resistance of the FinFET, which is $\frac{1000\ \Omega \cdot \mu m}{4 \mu m} = 250\Omega$. Therefore, how parasite resistance affects G_{DS} is negligible. However, bulk MOSFETs has a lower extracted series resistance (around 50 $\Omega \cdot \mu$m), and there is very little difference between the applied and the V_{GS} across the channel, indicating that series resistance has little effect in this situation.

1.2.4 Circuit Performance at 5GHz

These measurements have been utilised to extract AC small-signal parameters for planar bulk MOSFETs and FinFETs, which are then used to simulate the performance of two key components at 5 GHz: the VCO and the LNA.

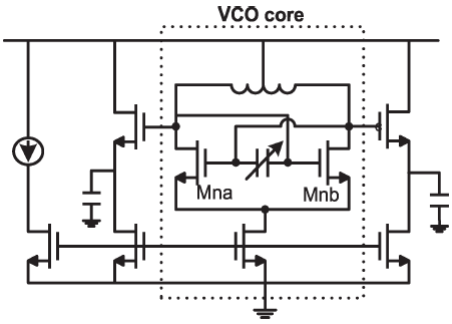


Figure 1.10. Schematic of 5-GHz LC tank VCO. [SD06]

An LC tank intended to resonate at 5 GHz and a cross-coupled transistor pair serving as a negative Transconductance to offset losses in the tank circuit constitute the fundamental components of the VCO circuit. The cross-coupled pair's negative Transconductance can be found using:

$$G_{M,NEG} = -\frac{G_M}{2} + \frac{G_{DS}}{2} \tag{1.12}$$

where the Transconductance and Output conductance of each individual transistor are represented by G_M and G_{DS}. The latter represents a potential loss in addition to the LC tank's loss. The bias point at startup is represented by the absolute value of G_M,neg, which should be a little more than the comparable loss conductance. Assuming a small-signal operation, this number can be calculated at startup.

The oscillation begins when G_M,neg is negative, and it eventually reaches an amplitude that makes small-signal operation unassumable. This amplitude can be roughly calculated by multiplying the DC by the tank resistance. The phase noise is also computed using this value. Phase noise and power consumption are the VCO's primary parameters. For a VCO, these two parameters are concatenated in the commonly used FoM.

$$FOM_{VCO} = (\frac{F_0}{F_M})^2 \frac{1}{PN \cdot P} \tag{1.13}$$

PN is the Phase Noise measured relative to the output power, P is the Power consumption, and F_0 is the Oscillation Frequence, F_M is the Offset Frequence (the difference in Hertz between the oscillation frequency and the frequency at which phase noise is measured).

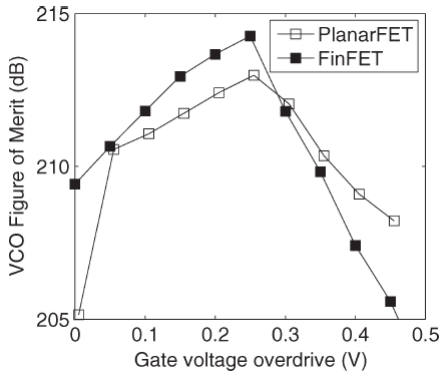


Figure 1.11. FOM of the VCO. [SD06]

It is observed that the FoM depends on the V_{OV} of the cross-coupled pair's transistors. The oscillation amplitude at low-to-moderate current levels is directly proportional to the DC bias. Since the "signal" is small, a low bias current that corresponds to a low V_{OV} results in a high phase noise and a low signal-to-noise ratio, which in turn produces a low FoM. Phase noise decreases with increasing current; the FoM rises.

However, the FoM drops at high overdrive levels because the noise contributions continue to rise as the current increases although the amplitude is maximum (constrained by the power supply). As can be observed, the gate V_{OV} yields a peak FoM in the 0.2–0.3 V range; this value is higher for the FinFET than for the bulk MOSFET. Better performance is achieved by the FinFET VCO because of the reduced transistor loss G_{DS} compared to the MOSFETs.

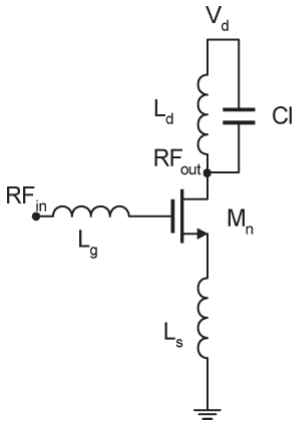


Figure 1.12. Schematic of 5-GHz common source LNA. [SD06]

A fixed input matching Q of 2.5 has been used to size the LNA. The following formula

provides the FoM of the LNA:

$$FOM_{LNA} = \frac{A_V \cdot IIP_3}{V_{DD} \cdot I_D \cdot (NF - 1)} \tag{1.14}$$

where IP3 is the $3^{RD} Intercept Point$, NF is the Noise Figure, and A_V is the Voltage Gain. The FinFET's FoM is seen to be greater than the bulk MOSFETs.

1.3 Analog components

Based on a 2007 paper [GJM05], I developed a brief overview of the various components that could interest the analog field.

1.3.1 ESD protection structures

Diodes and ggnMOS, for instance, can serve as the foundation for bulk CMOS and ESD protection structures. A poly-spaced diode is a diode in FinFET technology. This structure uses fins with oppositely doped S/D regions. The diode's p+ and n+ regions are defined by the gate material. The undoped fin is therefore composed of an N-type zone on one side and a P-type region on the other. A TLP tester has been used to measure the ESD robustness of a standalone diode and ggnMOS device.

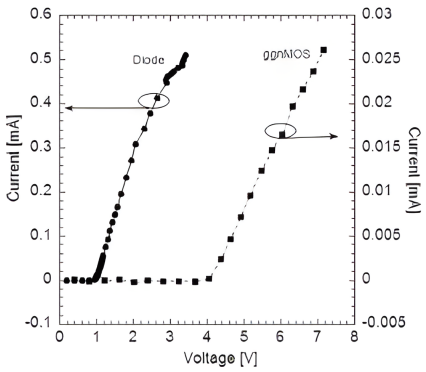


Figure 1.13. High current IV characteristics of a 20 μm wide single fin diode and a 125 fin ggnMOS device. [GJM05]

The robustness of the ggnMOS is 4–6 mA/μm, whereas that of the diode is approximately 10 mA/μm. The ggnMOS device can only be used as a self-protecting output; it cannot be utilised to offer any ESD protection for input pins, despite demonstrating ESD robustness (about 5 mA per μm of actual silicon fin footprint width).

1.3.2 Resistors

For analog/RF designs, resistor solutions like unsilicided, medium-ohmic, and high-ohmic poly resistors have always been easily accessible. Thin film resistors with minimal parasitic capacitance to the substrate have been manufactured in the back end for high-end applications. There are solutions where the MiM capacitors' bottom electrode is repurposed as a thin-film resistor. The stoichiometry of the film can be adjusted for low-temperature coefficients when materials like TaN are utilised. It is necessary to assess the availability of these traditional polysilicon resistors with metal gate technology. It is challenging to remove the metal from underneath the polysilicon top layer in the gate stack since it is placed there due to contamination. These resistors still offer fascinating sheet resistances as long as the metal coating is thin (5 to 10 nm). FinFET technology presents an alternative where the fin can be a resistor solution instead of the poly gate.

1.3.3 Varactors

FinFETs can be used to create varactors by shorting their source and drain. The variable capacitance is between the gate and the shorted source and drain. FinFET varactors have tuning ranges that are higher than seven.

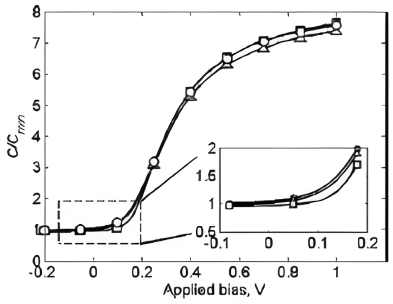


Figure 1.14. Measured tuning range of n-FinFET varactors for different fin widths (squares: 70 nm; circles: 670 nm; triangles: 4870 nm) and a gate length of 385nm. [GJM05]

The fins' series resistance limits the Q, however using excessively wide fins is allowed. W_{FIN} has a significant role in controlling the SCE in transistors. Wide totally depleted SOI-type structures, on the other hand, can be applied to varactors, and it has been shown that this produces greater Q without appreciably affecting the tuning range.

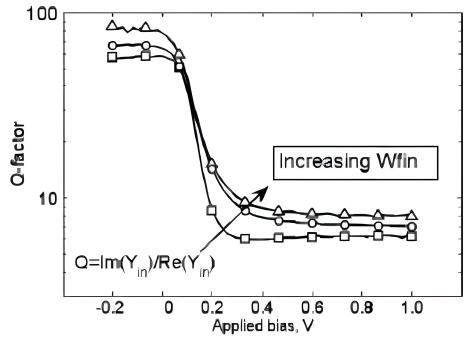


Figure 1.15. Quality factor of n-FinFET varactors measured at 5 GHz, as a function of the applied bias for different fin widths (squares: 70 nm; circles: 670 nm; triangles: 4870 nm). [GJM05]

1.3.4 Tunable oscillator

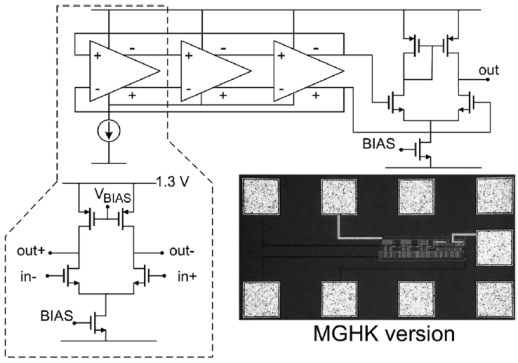


Figure 1.16. Tunable oscillator of a UWB impulse radio and its micrograph. [GJM05]

Using a poly-SiON gate stack and a TiN-HfO2 metal-gate HiK stack, the LO of a UWB impulse radio has been processed in a 90-nm planar bulk CMOS node (Lphys = 65nm) and FinFET technology with 45-nm physical gate length transistors. This low starting time oscillator needs to be tunable in the frequency range of 3 to 10 GHz. Up to 6 GHz, the power consumption of the various models is comparable for a given frequency. The high series resistance in the transistors is the primary reason the FinFET version cannot operate above 8 GHz. Conversely, the 90-nm variant has a tuning range of up to 15 GHz. Furthermore, table-based FinFET model circuit simulations closely resemble observations. Lastly, there is no discernible difference in performance between the various FinFET gate stacks. This demonstrates the low gigahertz range in which 45-nm L_{CH} FinFETs can function. However, at this time, their frequency limitations (F_T, $F_{MAX} \leq$ 100GHz) are greater than those of 90-nm node planar bulk transistors, which have peak F_T and F_{MAX}

of 170 and 240 GHz, respectively.

1.3.5 Operational Transconductance Amplifier (OTA)

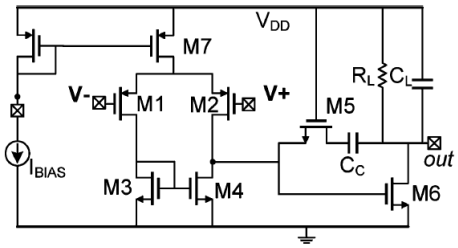


Figure 1.17. Miller-compensated OTA designed in a FinFET technology. [GJM05]

The table-based FinFET model that was used to develop this OTA is shown in the following table:

	M1-M2	M3-M4	M5	M6	M7
L(nm)	225	265	115	45	115
W(μ)	112	288	2.7	67	18
nFins	702	1806	18	670	112

Table 1.1. Dimensions of the transistors in the OTA. [GJM05]

150 MHz is the standard on the GBW. A 200 Ω resistance in parallel with a 20 pF capacitance as the load. The output transistor M6's 45 nm channel length is sufficient to drive this high load. At 1V, the circuit uses 2.8 mW of power. The open-loop gain has been determined by placing the OTA in a feedback loop that is only active at low frequencies.

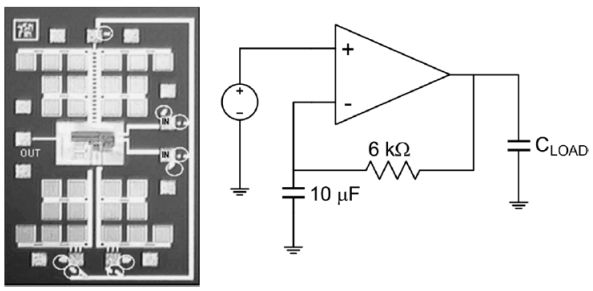


Figure 1.18. Micrograph of the OTA and measurement setup for the low-frequency small-signal gain. [GJM05]

This allows for the measurement of an open-loop gain of 50 dB, which is 8 dB higher than the OTA in a 65-nm planar bulk CMOS process $V_{DD} = 1.2$ V with a classical poly-SiON gate stack, and 5 dB higher than the OTA $V_{DD} = 1.5$ V that employs FinFETs with a poly-SiON gate stack and gate lengths not less than 250 nm.

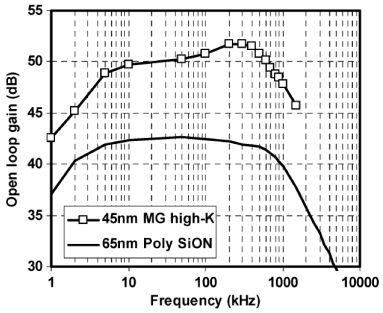


Figure 1.19. Frequency response of two OTAs: the metal-gate high-k FinFET OTA and a reference design in a 65-nm CMOS process (classical gate stack). [GJM05]

1.3.6 Fully differential OTA

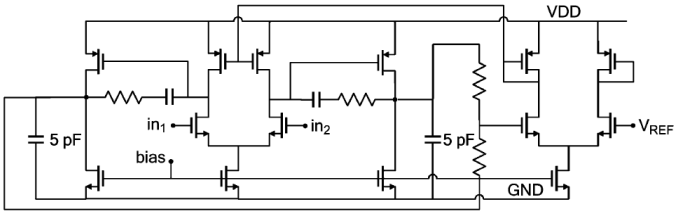


Figure 1.20. Fully differential OTA ($V_{DD} = 1$ V). [GJM05]

In the paper they have simulated and compared the fully differential OTA with a 90-nm bulk CMOS variant.

	90 nm node bulk	45 nm bulk	45 nm FinFET
A_0	60 dB	46 dB	73 dB
DC	1.12 mA	746 μA	863 μA

Table 1.2. Performance of the fully differential OTA. [GJM05]

This OTA contains a specification for the voltage gain A_0 of 60 dB and a specification for the GBW of 100 MHz. For both the differential and common-mode feedback, the phase margin standard is 60. The 45-nm planar bulk transistors' intrinsic gain satisfies

the ITRS standard. The latter is, for L = 5 $\times L_{MIN}$, at least thirty. The barrier at the drain side from the halo implant causes the 45-nm bulk version to have a low voltage gain even with longer transistors in the input stage. The transistors in the input stage have a 1 μm channel length to match the gain criterion, whereas the output stage transistors in the 90-nm version are the shortest. For the same gain and phase margin specification, this restricts the GBW to less than 200 MHz. With FinFETs, a voltage gain of 38 dB is already achieved in the first stage, and the transistors have a maximum length of 0.35 μm. This method obtains a GBW above 400 MHz for the specified phase margin and gain. In conclusion, two stages are sufficient to create high-speed, high-gain FinFET opamps; but, in planar bulk 45 nm, more stages are required, necessitating the usage of cascodes or more current. However, the latter option is challenging due to the low V_{DD}.

1.3.7 High speed comparator

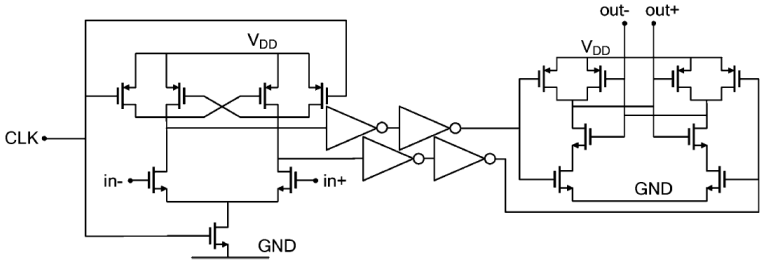


Figure 1.21. High-speed clocked comparator (V_{DD} = 1 V). [GJM05]

A clocked comparator has been built using FinFETs and planar bulk transistors. The average P for the FinFET variant is 169 μW at a clock frequency of 1.25 GHz, while the bulk version's is 112 μW. The consumption in the planar bulk process at 90 nm is 250 μW. The speed during the slewing and regeneration phases determines the comparator speed. When the clock input is first high, slewing happens because a steady current discharges the drain nodes of the regenerating pMOS transistors. Following this slewing, there is an initial exponential reliance on the differential input during the regeneration phase. The exponential time constant τ is determined by the regenerating transistors' G_M and differential capacitance between their drains. Compared to the bulk version (25 V/ns), the FinFET variant's slew rate (11 V/ns) is more than twice as low. The bulk version can run up to 5 GHz, whereas the FinFET version's maximum clock frequency is limited to 2 GHz due to its slower slewing behaviour, slightly lower at 23 ps compared to 28 ps for the bulk version. The gate-drain capacitances seen at the regeneration transistor drains impact the FinFET comparator's speed. In a FinFET version simulation experiment, the slew rate is increased to 62 V/ns and τ is reduced to 5 ps by using an extrinsic gate-drain capacitance CgdExt that is five times lower. Because of the drain-bulk junction capacitors, the impact of CgdExt is comparatively less in the bulk version.

1.3.8 5-GHz LNA-Mixer Combination

Using inductors in a 5-metal layer BEOL, the two 45-nm transistor types have been used to design the 5-GHz LNA-mixer combination. Every inductor has a Q of less than 10. The planar bulk version has a conversion gain of 15.8 dB (from a 5-GHz input to an output at 10 MHz), whereas the FinFET version has a 6 dB lower gain. Both versions have a bias current of 2 mA and a single-sideband NF of 6.6 dB with these characteristics. This indicates that the RF performance is not significantly impacted by the low $\frac{G_M}{G_{DS}}$ of the bulk transistors. In comparison, the same above-IC technique for the inductors has been used to rebuild the 90-nm planar bulk single-stage cascode 5-GHz LNA in 45 nm.

5 GHz	planar bulk 45nm	FinFET 45 nm	90nm
Gain (S21 - dB)	13.2	13.5	19
NF (dB)	1.3	1.5	1.4
DC (mA)	2.3	2.9	4
S11 (dB)	-20	-25	<-10

Table 1.3. Performance of a 1-stage LNA in different technologies. [GJM05]

The 45-nm bulk version performs somewhat better than the FinFET version, similar to the LNA-mixer combination. Additionally, the 45-nm designs have a lower DC than the 90-nm designs, but they also have a lower gain.

1.3.9 60-GHz VCO

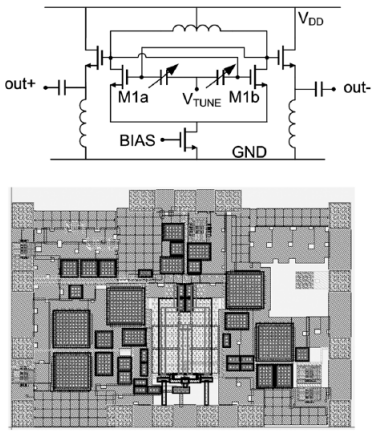


Figure 1.22. 60-GHz VCO (V_{DD} = 1 V) and its layout. [GJM05]

The two types of transistors have been used to replicate the 60-GHz VCO. The MOSFET varactors are used in the planar bulk version. The varactors have a length of 85 nm and

a fin width of 1 μm for the FinFET variant. For the planar bulk MOSFET varactors, the Q at 60 GHz over the tuning range is between 8 and 12.5, and for the FinFET varactor, it is between 5 and 14.5. With a difference of 14.5, the inductor, modelled using a 3-D electromagnetic simulator, is a coplanar transmission line in the upper layer of the 5-metal level BEOL. The simulations have modelled the layout's most significant interconnects. The cross-coupled pair's negative transconductance is enlarged by a factor of two to guarantee VCO startup. This transconductance should have a bigger absolute value than the total loss conductance at 60 GHz. The bulk version's core draws 10 mA and, at a 1-MHz offset, has a worst-case PN over the tuning range of - 89.5 dBc/Hz. The output power is 1.7 dBm, and the tuning range is 6.8 GHz.In contrast, the 60-GHz VCO in 90-nm SOI has an output power of -6.8 dBm, a power consumption of 14 mA V_{DD} = 1.5 V, and a worst-case PN of -85 dBc/Hz at a 1-MHz offset for a tuning range of 8.3 GHz. Because the devices in the FinFET variant are larger, the parasitic capacitances that increase the tank capacitance are greater for a given gm of M1a–M1b. The gate-drain capacitance of M1a–M1b controls the parasitic capacitance. This restricts the FinFET version's tuning range to 3 GHz. It uses 14 mW of power. In simulations, the tuning range is increased to 10.8 GHz with a five-fold lower CgdExt. This demonstrates once more how much extrinsic gate-drain capacitance matters.

1.4 The importance of spacing

Based on design criteria, a 2012 paper [;12] focused mostly on spacing effects. Parasitic components will be important even though nanoscale FinFETs may reduce electrostatic restrictions in further scaling. For instance, the proximity of the S/D SEG region to the gate causes an increase in fringe capacitances, and the narrow W_{FIN} causes a rise in series resistances. These parasites impaired performance.

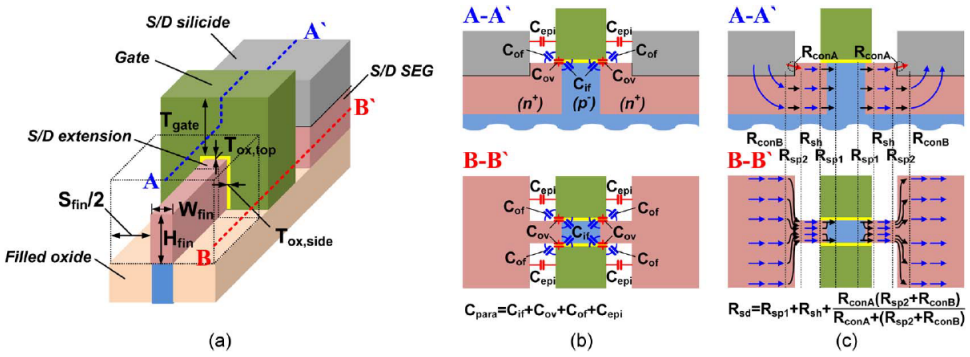


Figure 1.23. (a) Three-dimensional illustration of a FinFET device. The S/D SEG region on the front side is intentionally stripped to show the fin geometry, whereas, on the back, it remains to show the SEG geometry. (b) Cross sections along the line A - A' and the line B - B' to denote parasitic capacitance components. (c) Cross sections along A - A' and B - B' lines denote series resistance components, defined according to the current flows designated as arrows. [;12]

There are four main parts to the Parasitic Capacitance that separates the gate from the S/D regions of C_{PARA}:

1. Inner Fringe Capacitance (C_{IF});
2. Overlap Capacitance (C_{OV});
3. Outer Fringe Capacitance (C_{OF});
4. EPI-to-gate Capacitance (C_{EPI}).

A typical 2-D model is used to model each component. Based on current flows, the S/D R_{SD} is composed of five primary components:

1. Spread resistance between the channel layer and the S/D extension (R_{SP1});
2. sheet resistance of the S/D extension beneath the sidewall spacer (R_{SH});
3. spread resistance between the S/D extension and the S/D SEG region (R_{SP2});
4. contact resistances between the S/D SEG region and the S/D silicide through the side surface (R_{CON_A});
5. through the bottom surface (R_{CON_B}).

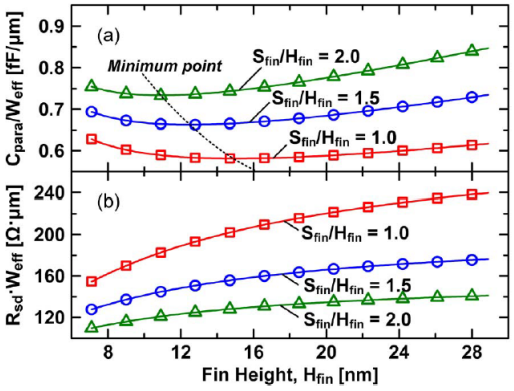


Figure 1.24. Width-normalized (a) parasitic capacitances (Cpara/Weff) and (b) S/D resistances (Rsd · Weff) as functions of Hfin and Sfin with several S_{FIN}-to-H_{FIN} ratios. [;12]

Because of charge sharing between the two side gates and conduction via the top gate, the W_{FIN} is defined as $2H_{FIN}$ rather than as $2H_{FIN} + W_{FIN}$ as long as the W_{FIN} is narrow enough to allow full depletion. The rationale behind treating both H_{FIN} and S_{FIN} as independent variables with a set S_{FIN}-to-H_{FIN} ratio is that process integration factors, including tilted ion implantation and over-etch to eliminate stringers, limit the ability to

achieve both a high H_{FIN} and a small S_{FIN}. Denser fins reduce areas of the gate and S/D SEG regions per fin, hence a small S_{FIN}-to-H_{FIN} ratio lowers the C_{PARA}/W_{FIN}, respectively. The effects of H_{FIN} and S_{FIN} are balanced, so at a given S_{FIN}-to-H_{FIN} ratio, there is an optimal $H_{FIN}(S_{FIN})$ to reduce C_{PARA}/W_{FIN}. Increasing S_{FIN} at a fixed H_{FIN} increases C_{PARA}/W_{FIN} because enlarging areas of the gate and S/D SEG regions increases the C_{OF} and C_{EPI} components, and increasing H_{FIN} at a fixed S_{FIN} decreases C_{PARA}/W_{FIN} because the C_{PARA} fraction induced by the top gate is reduced when normalised by W_{FIN}. In addition, a high S_{FIN}-to-H_{FIN} ratio helps lower the $R_{SD} \cdot W_{FIN}$. The contact resistances, RconA and RconB, are the main constituents of R_{SD}, and RconB depends on the volume of the S/D SEG region. Increasing the S_{FIN}-to-H_{FIN} reduces $R_{SD} \cdot W_{FIN}$ because it increases the effective volume for RconB. Increasing $H_{FIN}(S_{FIN})$ at a given Sfin-to-H_{FIN} increases $R_{SD} \cdot W_{FIN}$, suggesting that decreasing R_{SD} by volume increase is less effective than increasing W_{FIN} increment by increasing H_{FIN}. $0.5 \cdot C_{PARA}$ is the base for the C_{GS} (C_{GD}), and $0.5 \cdot R_{SD}$ is the value for the Rs(Rd). Thus, by C_{GS}, C_{GD}, R_S, and R_D, capacitive and resistive parasitics greatly reduce the F_T and F_{MAX}. Since the inversion layer effectively screens the under operating conditions, the C_{IF} for C_{PARA} should be eliminated. Since $R_{SP1}+R_{SH}$ already affects the G_M and G_{DS} in the 3-D simulation, the resistive components for R_{SD} from the Source/Drain (S/D) diffusion edge to the sidewall spacer edge ($R_{SP1}+R_{SH}$) should be excluded.

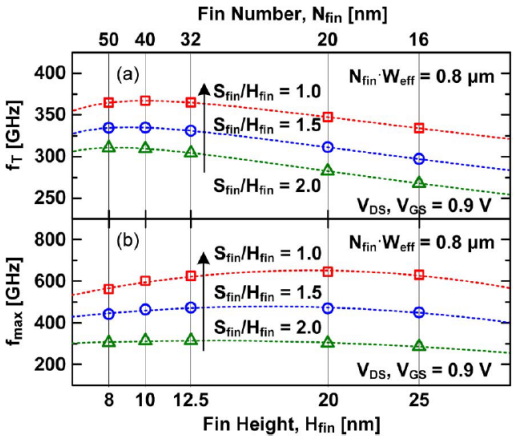


Figure 1.25. Calculated (a) current-gain F_T and (b) F_{MAX} as functions of Hfin and Sfin with several S_{FIN}-to-H_{FIN} ratios. N_{FIN} of each different H_{FIN} is adjusted to have the same device width (Nfin · Weff) for a fair comparison of fmax. [;12]

R_G, which depends on N_{FIN}, determines the F_{MAX}. For a fair comparison, the same $N_{FIN} \cdot W_{FIN}$ is assumed. It should be noted that enhancing both F_T and F_{MAX} calls for a small S_{FIN}-to-H_{FIN} ratio. This indicates that C_{PARA} has a greater impact on F_T (or F_{MAX}) than R_{SD}. When designing nanoscale FinFETs for RF/analog applications, C_{PARA} should be given more consideration than R_{SD}.

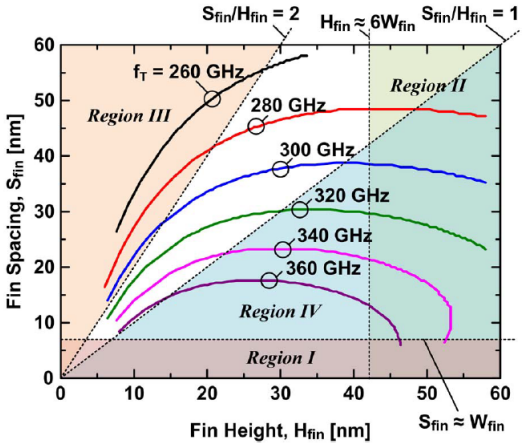


Figure 1.26. Hfin and Sfin calculated at a series of fixed fT from 260 to 360 GHz. At a given fin width (Wfin), the design window of [Hfin, Sfin] is partially screened by several concerns such as minimum Sfin (region I), maximum Hfin (region II), maximum S_{FIN}-to-H_{FIN} ratio (region III), and minimum S_{FIN}-to-H_{FIN} ratio (region IV). [;12]

At a range of fixed F_T from 260 to 360 GHz, pairs of H_{FIN} and S_{FIN} are computed. Several concerns partially obscure the design window of [H_{FIN}, S_{FIN}]. The minimum S_{FIN} ensures the layout proximity effects margin, while the maximum ensures a safe fin AR. Moreover, the FinFET layout area should be equal to or less than the planar FETs, according to the maximum S_{FIN}-to-H_{FIN} ratio. The previously-mentioned process issues lead to setting the minimum S_{FIN}-to-H_{FIN} ratio. It should be noted that while device designers are free to define their borders following their specific process requirements, region borders are picked at random. Variations in S_{FIN} and H_{FIN} inevitably alter other geometries or may impact inherent properties like channel mobility.

Chapter 2

Developments

2.1 The geometry role

Alright, let's move forward with creating these initial implementations. By now, it was obvious that geometry was essential to finFETs development in both the analog and non-analog domains. The differences produced by varying the H_{FIN} are displayed in the following subsection, which is based on [SS15]. Similarly, differences are associated with changing the W_{FIN}. In this instance, it is evident that depletion plays a crucial role, which, if full, lowers SCEs and raises gain; if incomplete, results in high I_{OFF}. FinFETs with big H_{FIN} values and lower W_{FIN} values can perform better, as can be seen by analysing the variances brought about by changing the two parameters. Linear devices have a higher F_T and finFETs with a AR $= 0.6$ exhibit the ideal balance between F_T and C_{GG}. Devices with AR $= 0.3$ and AR $= 2$ have the best power consumption, and trigates have the lowest delay.

2.1.1 The geometry role

Higher I_D and switching speed, as well as less than half the dynamic power requirement and 90% less static leakage current, are benefits of Mug-FET technology. AR is the most significant geometric parameter in FinFET technology. The FinFET (AR < 1), Trigate (AR $= 1$), and Planar (AR > 1) structural classifications apply to the device. Higher I_{ON} is shown by taller fins in the device, and SCEs immunity is established by narrower fins. There must be a trade-off with its AR between device performances.

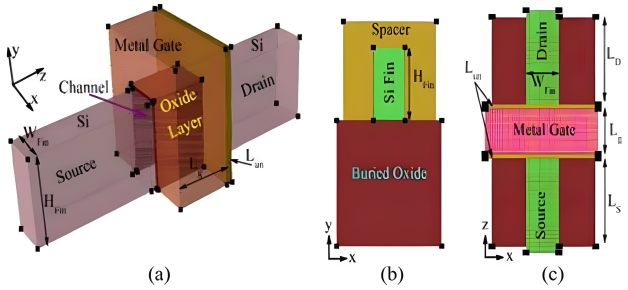


Figure 2.1. Perspective view of SOI FinFET (a) 3-D view (b) 2-D view in x-y (c) 2-D view in x-z. The metal and spacer regions are made transparent in (a). [SS15]

Design	HP	LOP	LSTP	This work FinFET/Trigate
Gate length, L_g (nm)	20	20	20	20
EOT (nm), t_{OX}	0.84	0.9	1.2	0.9
Supply Voltage, V_{DD} (V)	0.85	0.67	0.87	0.7

Table 2.1. Device Parameters as per ITRS 2013. [SS15]

A model is created for an n-channel MOSFET with an interfacial oxide of SiO_2 and a spacer of HiK material (Si_3N_4) in the underlap areas. Considered are uniform doping with ND at a density of $10^{20}cm^{-3}$ and LS/LD as 40 nm. Whereas the V_{DD} is 0.7 V, the EOT is 0.9 nm. It is expected that the gate electrode's work function is 4.5 eV. The undoped channel maximises effective mobility and boosts carrier transport from the source to the drain.

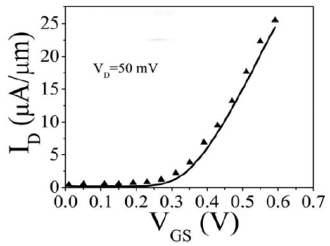


Figure 2.2. Matched ID -VGS characteristics of FinFET with the reference [SC12] and simulation result. [SS15]

Device design	H_{FIN}/L_G	W_{FIN}/L_G
	0.25, 0.6, 0.8, 1.0, 1.1, 1.3	0.25, 0.5, 0.6, 0.8

Table 2.2. Typical cases of 3D SOI-FinFET for simulation. [SS15]

2.1.2 The effects of H_{FIN}

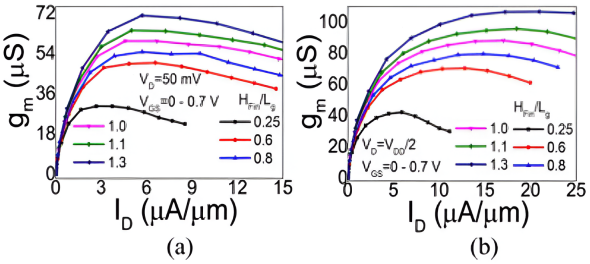


Figure 2.3. G_M as a function of I_D of the device (a) for V_{DS} = 0.05 V (b) for V_{DS} = 0.35 V. Main Device Parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, T = 300 K. [SS15]

The literature indicates that FinFETs have a more substantial access resistance issue. Nevertheless, various options like raising the H_{FIN} out of the gate region are present. Increased H_{FIN}/L_G ratios further enhance I_D and help prevent the parasitic resistance issue. When the H_{FIN}/L_G ratio rises, so do I_D and G_M. For H_{FIN} = 1.1 x L_G, higher I_D and G_M values are achieved.

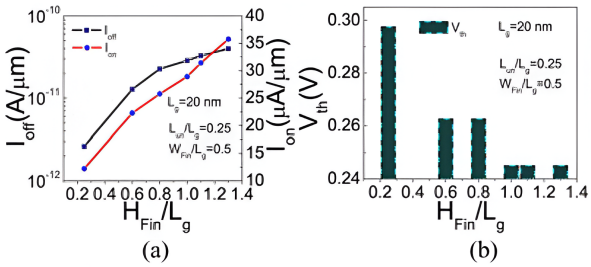


Figure 2.4. (a) I_{ON}, I_{OFF} and (b) V_{TH} of the device as a function of normalized H_{FIN} with respect to physical L_G . Main Device Parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} = V_{DS} = V_{DD} = 0.7 V, T = 300 K, H_{FIN} varied as (0.25 × L_G , 0.6 × L_G , 0.8 × L_G , 1.0 × L_G , 1.1 × L_G , 1.3 × L_G). [SS15]

The increase in H_{FIN}/L_G is accompanied by an increase in I_{ON} and I_{OFF}. This emphasises that narrow fins are recommended for improved SCE immunity and taller fins

are needed for higher current drivability. This is because narrow fins reduce the electric field in the silicon region, reducing the amount of leakage current. The best scenarios are $H_{FIN} = 0.6 \times L_G$ or 0.8 x L_G since they indicate moderate values for both I_{ON} and I_{OFF}. The MG work function typically determines and controls V_{TH} for FinFET. However, due to V_{TH}, it is exceedingly challenging to manage V_{TH} by modifying the gate work function in FinFETs. FinFET behaves like a FD-SOI MOSFET if $H_{FIN} \ll W_{FIN}$; otherwise, in the opposite situation ($H_{FIN} \gg W_{FIN}$), it acts like a DG MOSFET. Fixing the value of H_{FIN} is, therefore, more crucial for optimal device operation and improved resistance to SCEs. Higher V_{TH} roll-off and SS for high H_{FIN} values are caused by an increase in the H_{FIN}/L_G ratio, which causes V_{TH} to drop.

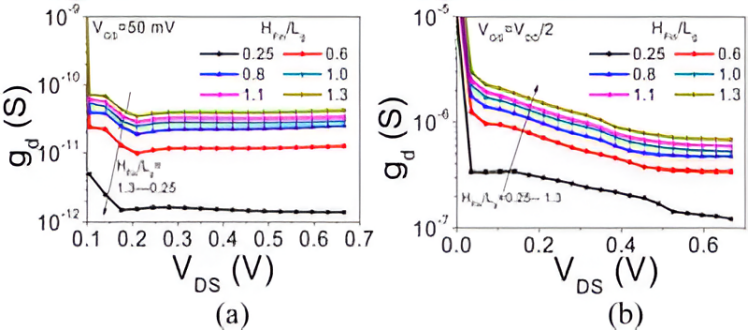


Figure 2.5. G_D of the device as a function of V_{DS} (a) for V_{GS} = 0.05 V (b) for V_{GS} = 0.35 V. Main device parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{DS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

FinFETs have stronger electrostatic control over the channel and are fully depleted due to the gate wrapping around the channel from three sides and the tiny W_{FIN}. Because of this, the drain bias dependency (depletion width at the drain side) is less and thus is the G_D. This further minimises the change in I_D. As the H_{FIN}/L_G ratio rises, G_D rises as well, which may reduce the device's gain. CMOS Transistors with low G_D are necessary for high gain in analog circuits. The low R_{OUT} is indicated by high G_D, and in the saturation regime, this leads to an increase in I_D with V_{DS}. The components, CLM and DIBL, are linked to this rise.

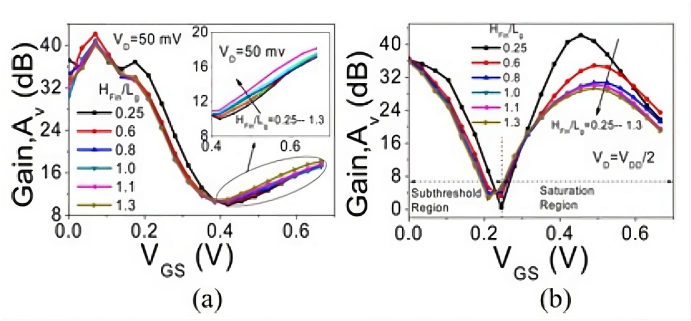


Figure 2.6. as a function of V_{GS} (a) for V_{DS} = 0.05 V (b) for V_{DS} = 0.35 V. Main device parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

An increase in A_V will be seen by a decrease in the H_{FIN}/L_G ratio. The significant decreasing G_D values for smaller H_{FIN}/L_G ratios is the cause of this.

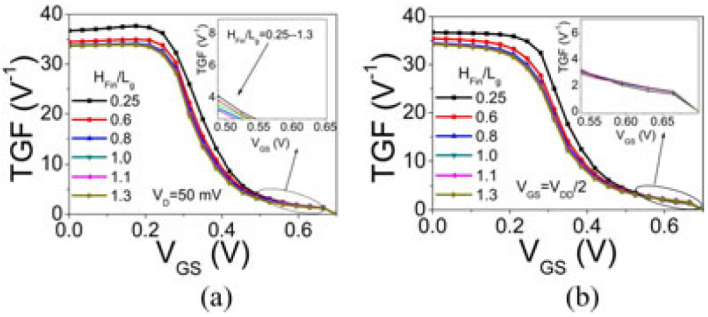


Figure 2.7. TGF as a function of V_{GS} (a) for V_{DS} = 0.05 V (b) for V_{DS} = 0.35 V. Main Device Parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

Realising analog circuits that operate at low supply voltage thanks to the high value of TGF is advantageous. Nearly the same TGF is attained in strong inversion, and the variation of TGF happens at the subthreshold region (at low V_{GS} and low V_{DS}) of operation. The degree of channel inversion is inversely proportional to this G_M/I_D ratio. High TGF values are shown by lower H_{FIN}/L_G ratios, and they progressively decline as the ratio rises in the subthreshold area of operation. The higher I_D values for greater H_{FIN}/L_G ratios are the cause of this. All that matters is the device's VEA; a low G_D propagates a higher I_D to G_{DS} ratio.

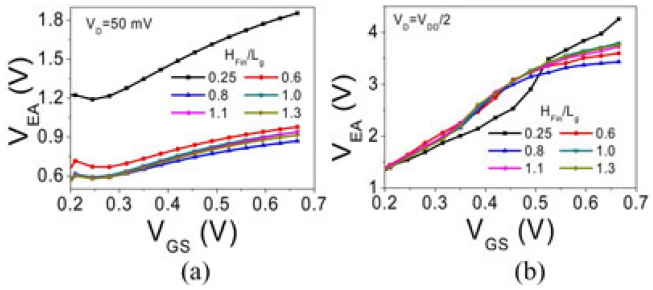


Figure 2.8. VEA as a function of V_{DS} (a) for VGS = 0.05 V(b) for V_{GS} = 0.35 V. Main Device Parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

Since the devices with small H_{FIN}/L_G ratios have low G_D values, which further enhance the VEA, they have good control over Channel Lenght Modulation (CLM) and DIBL. The VEA and A_V should be as high as feasible for optimal analog performance. In the subthreshold area (V_D = 50 mV), the VEA increases as the H_{FIN}/L_G ratio decreases; in the super-threshold region (V_D = 0.35 V), there are no such fluctuations.

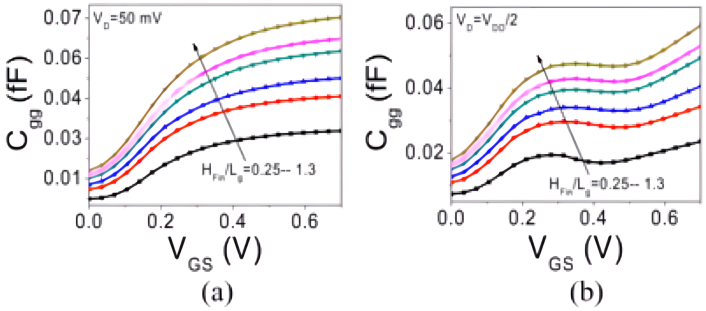


Figure 2.9. C_{GG} as a function of V_{GS} (a) for V_{DS} = 0.05 V(b) for V_{DS} = 0.35 V. Main Device Parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

As the H_{FIN}/L_G ratio rises, so does the device's C_{GG} value. The reason is higher fringing field density with the H_{FIN}/L_G ratio is the reason behind this. For greater Short Channel Effect (SCE) immunity, use H_{FIN} = 0.6 × L_G or 0.8 × L_G. The overall capacitance increases when the FinFET's stripe along the channel side walls is taller than the height of the gate electrode. The decrease in G_M with a decrease in H_{FIN}/L_G ratio further counterbalances the decrease in capacitance in the case of lower H_{FIN}/L_G ratios. The fact that selecting the ideal values for H_{FIN} and W_{FIN} is the only way to achieve the anticipated improvement in F_T with traditional scaling of a FinFET is highly noteworthy. The variation in F_T is primarily caused by G_M, with a smaller contribution from C_{GG}'s larger value. The difference between the minimum gate-drain/source capacitance and the peak of G_M is the peak point of F_T.

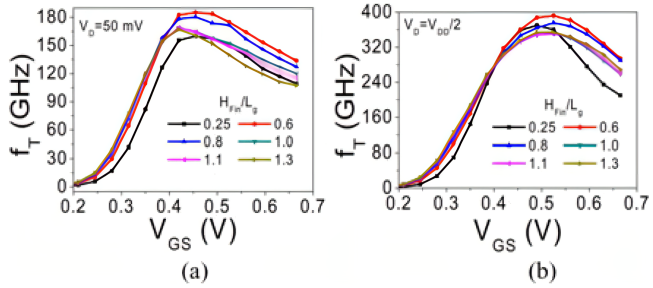


Figure 2.10. F_T as a function of V_{GS} (a) for V_{DS} = 0.05 V (b) for V_{DS} = 0.35 V. Main Device Parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

When compared to other devices in our study, the device with $H_{FIN} = 0.6 \times L_G$ has the largest F_T, indicating superior gate controllability and therefore larger G_M and lower parasitic gate capacitances.

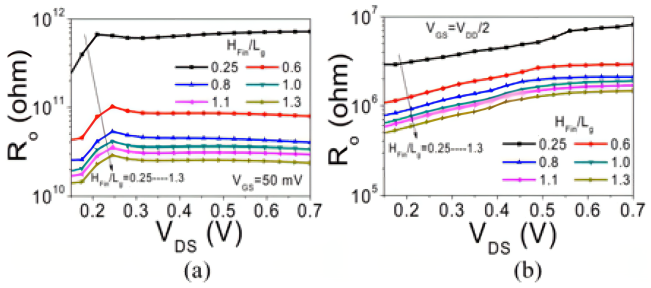


Figure 2.11. R_O of the device as a function of V_{DS} (a) for V_{GS} = 0.05 V (b) for V_{GS} = 0.35 V. Main Device Parameters are L_G = 20 nm, W_{FIN} = 10 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{DS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

Larger R_O are predicted by lower W_{FIN} devices. This can be attributed to the decrease in gd values as R0 = 1/gd for low H_{FIN}/L_G ratios and the improvement in SCEs.

2.1.3 The effects of W_{FIN}

Because numerous gates are near together, we can decrease the longitudinal electric field at the source side by selecting a smaller W_{FIN}.

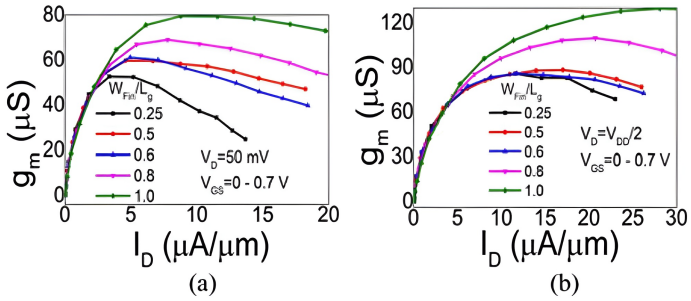


Figure 2.12. G_M as a function of I_D of the device (a) for V_{DS} = 0.05 V(b) for V_{DS} = 0.35 V. Main Device Parameters are L_G = 20 nm, H_{FIN} = 20 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

To minimize SCEs, $W_{FIN} = 0.6 \times L_G$ for FinFET and $W_{FIN} = 1.0 \times L_G$ for Trigate are needed. when expected, both I_D and G_M increase when the W_{FIN}/L_G ratio rises, reaching their maximum values at $W_{FIN} = 0.25 \times L_G$. The R_S is significantly higher for devices with low W_{FIN}.

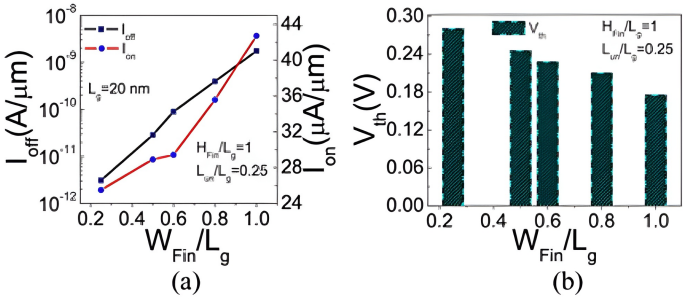


Figure 2.13. (a) I_{ON}, I_{OFF} and (b) V_{TH} of the device as a function of normalized W_{FIN} with respect to L_G. Main device parameters are L_G = 20 nm, H_{FIN} = 20 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, $V_{GS} = V_{DS} = V_{DD}$ = 0.7 V, T = 300 K, W_{FIN} varied as (0.25 × L_G, 0.5 × L_G, 0.6 × L_G, 0.8 × L_G, 1.0 × L_G). [SS15]

Each of I_{ON} and I_{OFF} grew as W_{FIN} climbed, reaching their maximum values for W_{FIN} = 1.0 x L_G. When $W_{FIN} = 0.6 \times L_G$ is the case, we obtain desirable values for $I_{ON} \simeq 30$ μA and $I_{OFF} \simeq 19^{-11}$A. The device performance is further deteriorated due to SCEs, V_{TH} roll-off, and CLM, as the V_{TH} value falls with an increase in W_{FIN}/L_G ratio. The coupling between the front and back interfaces diminishes as W_{FIN}/L_G drops, increasing V_{TH} value. This analogy suggests that we can improve the FinFET performance by taking into account thicker H_{FIN} and thinner W_{FIN}.

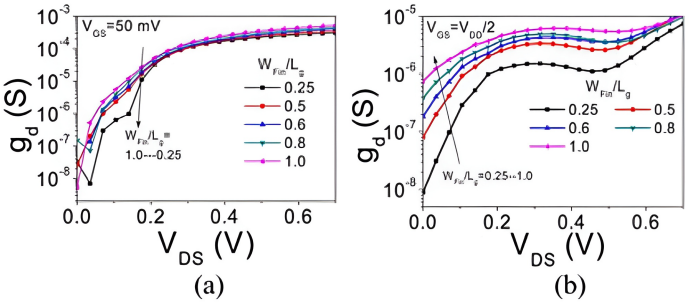


Figure 2.14. $G_D$of the device as a function of V_{DS} (a) for V_{GS} = 0.05 V (b) for V_{GS} = 0.35 V. Main Device Parameters are L_G = 20 nm, H_{FIN} = 20 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{DS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

The main device dimensions and the G_D are connected as follows: $G_D = 2H_{FIN} + W_{FIN}$. Hence, G_D and W_{FIN} are directly proportional. It is evident that in the case of higher applied voltage ($V_{GS} = V_{DD}/2$), there is a greater variation in G_D. The gadget is heating up at a greater biasing voltage, which is why. Additionally, lowering the supply voltage and thinning the W_{FIN} is sufficient to lessen the issue of body heating and, consequently, the SCEs. Because they do not experience substrate-associated degradation in the G_D, FinFETs with thinner W_{FIN} are well known for suppressing SCEs.

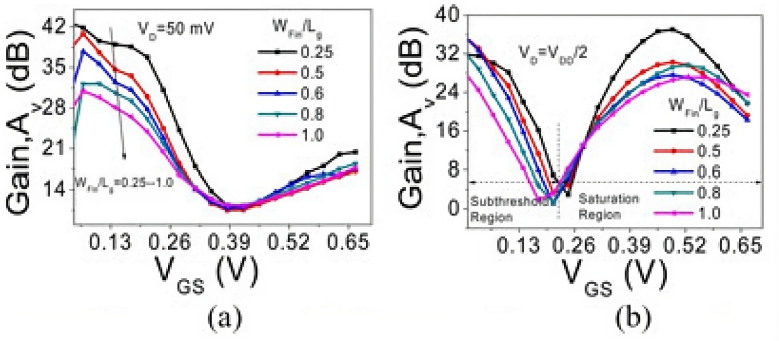


Figure 2.15. as a function of V_{GS} (a) for V_{DS} = 0.05 V(b) for V_{DS} = 0.35 V. Main Device Parameters are L_G = 20 nm, H_{FIN} = 20 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

When fins are fully depleted, G_D is significantly lower, which results in a larger gain for the FinFETs with lower W_{FIN}.

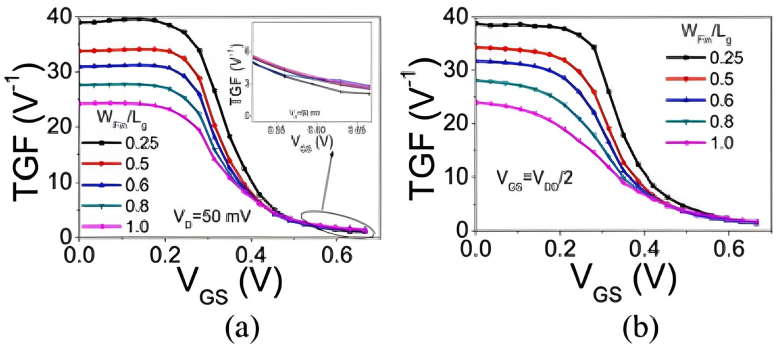


Figure 2.16. TGF as a function of V_{GS} (a) for V_{DS} = 0.05 V (b) for V_{DS} = 0.35 V. Main Device Parameters are L_G = 20 nm, H_{FIN} = 20 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

In the linear region, W_{FIN}/L_G ratio has a greater effect on G_M/I_D; in the saturation region, however, the variation appears to be considerably smaller. The dependency of R_{SERIES} on G_M/I_D is stronger than that of any other parameter. As a result, in the saturation region, $I_{D,sat}$ is less sensitive since it is a strong function of R_{SERIES}, whereas the ratio $G_M/I_{D,sat}$ is a weak function of RS. Higher VEA may also explain the decrease in G_D for low W_{FIN}.

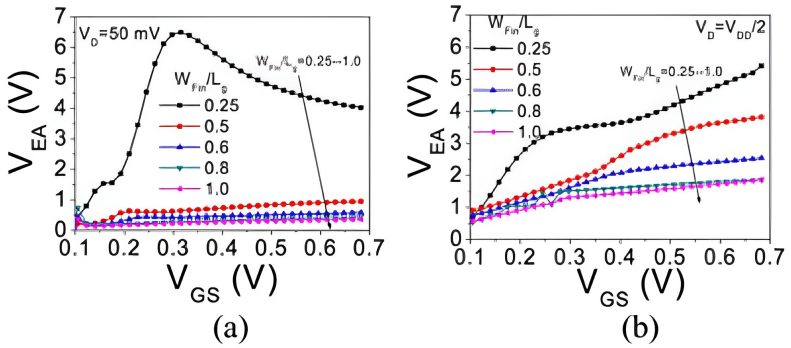


Figure 2.17. VEA as a function of V_{DS} (a) for VGS = 0.05 V (b) for V_{GS} = 0.35 V. Main Device Parameters are L_G = 20 nm, H_{FIN} = 20 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

The I_D-V_{DS} curve for BJT is often explained by VEA; however, in the case of MOSFET, it is the projected intercept of saturation output characteristics on the V_{DS} axis. We can, however, state that better VEA is predicted by lower W_{FIN}/L_G ratios because of the diminished substrate effect, the body's heating issue, and improved immunity to SCEs.

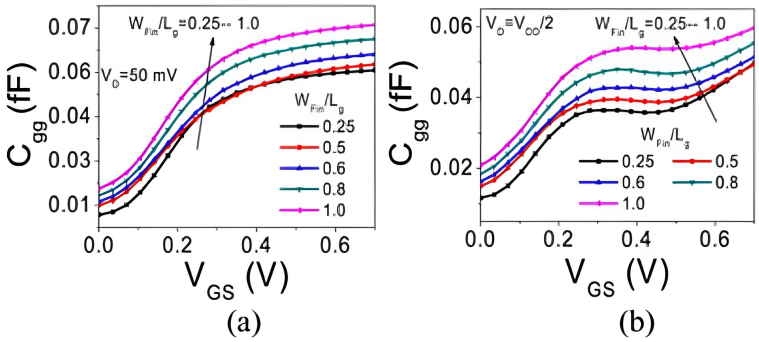


Figure 2.18. C_{GG} as a function of V_{GS} (a) for $V_{DS} = 0.05$ V (b) for $V_{DS} = 0.35$ V. Main device parameters are $L_G = 20$ nm, $H_{FIN} = 20$ nm, $T_{OX} = 0.9$ nm, $T_{BOX} = 40$ nm, $T_{SUB} = 70$ nm, $L_{un} = 5$ nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

It is quantifiable that FinFETs with low W_{FIN}/L_G ratios have substantially smaller C_{GG} values. C_{GG} decreases by 25.37% from $W_{FIN}/L_G = 1$ to $W_{FIN}/L_G = 0.25$. High G_M values are also predicted by higher W_{FIN}/L_G ratios. Hence, for all cases of W_{FIN}/L_G, an increase helps to eliminate the increment of C_{GG}, which causes a little fluctuation in F_T.

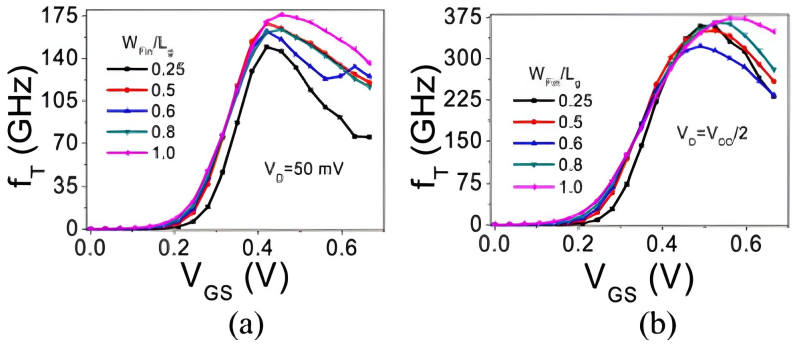


Figure 2.19. F_T as a function of V_{GS} (a) for $V_{DS} = 0.05$ V (b) for $V_{DS} = 0.35$ V. Main device parameters are $L_G = 20$ nm, $H_{FIN} = 20$ nm, $T_{OX} = 0.9$ nm, $T_{BOX} = 40$ nm, $T_{SUB} = 70$ nm, $L_{un} = 5$ nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

A slight improvement in F_T is evident when W_{FIN} rises. The variation in G_M and the larger value of C_{GG} are the primary causes of this discrepancy in F_T. The position between the minimum C_G and $G_{M,max}$ corresponds to the peak point of F_T.

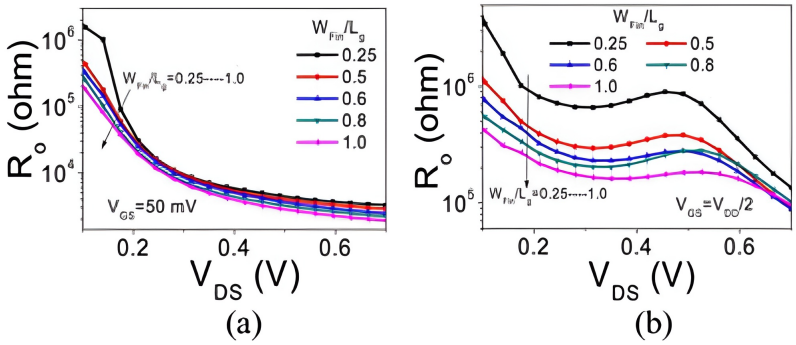


Figure 2.20. R_O of the device as a function of V_{GS} (a) for V_{DS} = 0.05 V (b) for V_{DS} = 0.35 V. Main device parameters are L_G = 20 nm, H_{FIN} = 20 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

For the lower V_{GS} example, there is no such fluctuation in R_O concerning W_{FIN}/L_G ratio. A notable difference does exist when the V_{GS}/L_G ratio is larger. This can be attributed to the bias voltage as R_O's reliance on the electric field. For thicker W_{FIN} values, where current crowding or electron pile-up effects are more severe, a low value of R_O is observed. As a result, drive current and G_M are improved. FinFETs with low W_{FIN}/L_G ratio predict high R_{SERIES}, which limits the achievable G_M, but better immunity against SCEs as it shows a higher gain. FinFETs with high W_{FIN}/L_G ratio give higher G_M, but their poor gate control results in severe SCEs (low device gain).

2.1.4 AR

While shorter fins are needed for better SCEs, taller fins are for higher current drivability and also show some improvement in high frequency of operation. Significant difficulties arise from certain fabrication limits to attain such higher H_{FIN} and narrower W_{FIN}.

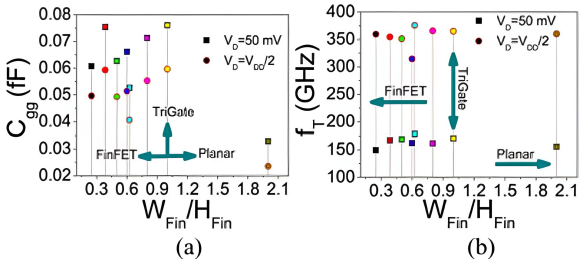


Figure 2.21. (a) C_{GG} (b) F_T as a function of Fin AR. Main device parameters are L_G = 20 nm, H_{FIN} = 20 nm, T_{OX} = 0.9 nm, T_{BOX} = 40 nm, T_{SUB} = 70 nm, L_{un} = 5 nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

The obtained C_{GG} in the case of Planar MOSFET is quite low, which improves the F_T even more. When evaluating every possible AR scenario, values for C_{GG} and F_T are

better when AR = 0.6 is used. The optimisation of delay is incorporated concerning AR to minimise the intrinsic delay, which is expressed as $(\frac{C_{GG} \times V_{DD}}{I_{EFF}})$. Where I_D for $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}/2$ and I_D for $V_{GS} = V_{DD}/2$ and $V_{DS} = V_{DD}$ are averaged to form I_{EFF}.

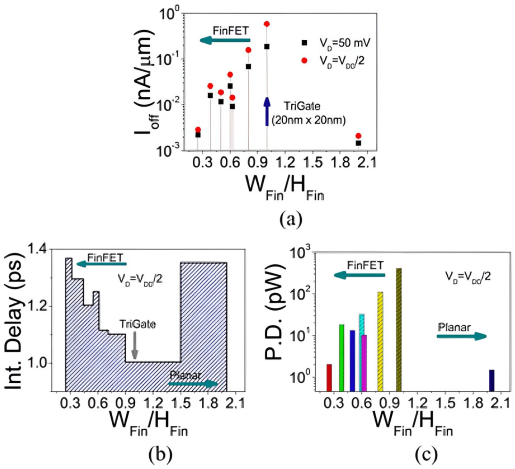


Figure 2.22. (a) I_{OFF} (b) Intrinsic Delay $(\frac{C_{GG}}{} \times V_{DD})(I_{EFF})$ (c) Static power dissipation $(V_{DD} \times I_{OFF})$ as a function of Fin AR. Main device parameters are $L_G = 20$ nm, $H_{FIN} = 20$ nm, $T_{OX} = 0.9$ nm, $T_{BOX} = 40$ nm, $T_{SUB} = 70$ nm, $L_{un} = 5$ nm, V_{GS} varied from 0 V to 0.7 V, T = 300 K. [SS15]

In comparison to other designs, such as the Trigate design (AR = 1), the I_{OFF} is lowered by a greater factor for the FinFET design with AR = 0.3 and the Planar design with AR = 2. The Trigate design (AR = 1) exhibits the least delay but the greatest power dissipation compared to its equivalents. The large Ieff in the instance of AR = 1 is the cause of this. The FinFET design with AR = 0.3 and the Planar design with AR = 2 have the best power dissipation values.

2.2 Step finFETs

After discussing geometry, we go on to the idea of step fin and step drain finFET, whose dimensions are shown in Table 2.23 and shown in Figure 2.24's schematic view.

Dimension		SF-FinFET	SD-FinFET
Width	W1,W3	3 nm	-
	W2	6 nm	-
	W4,W6	-	3 nm
	W5	-	4 nm
Height	H1,H3	5 nm	-
	H2	20 nm	-
	H4,H6	-	7 nm
	H5	-	16 nm

Figure 2.23. Dimension for SF-FinFET and SD-FinFET. [RT17]

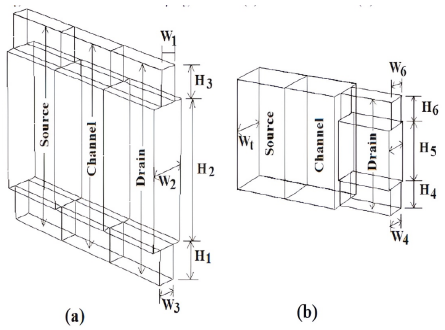


Figure 2.24. 3D schematic view of fin of (a) SF-FinFET and (b) SD-FinFET device.

All of the devices use strained silicon as their channel material. 1.19X improvement on I_{ON} and 1.34X improvement on G_{DS} are demonstrated by this suggested SD-FinFET structure. For SF-FinFET, improvements are seen in C_{GG} and F_T. Enhancement in propagation delay and noise margin is also noted in SF FinFET. The structure combines 3-D FET, silicon and strain silicon on insulator technology. The channel area uses silicon that has been strained. Strained silicon modifies the carrier transport characteristics by increasing carrier mobility. Consequently, the drive current rises. In the S/D area, silicon is used. At 1.1 nm, EOT is thought to lower the tunnelling current and thus the leakage current. As dielectric materials, SiO_2 and HfO_2 are employed here. The interface oxide layer, SiO_2, has a thickness of 0.6 nm. SiO_2 and HfO_2 have a dielectric constant of 3.9 and 22 correspondingly. Every gadget is constructed using $L_G = 20$ nm. The channel region is undoped. Doping concentrations for S/D and substrate are $1.0 \times 10^{20} cm^{-3}$ and $1.0 \times 10^{15} cm^{-3}$, respectively. As P-type and N-type dopants, active boron and phosphorus concentrations are utilised. The devices' BOX width is 30 nm. Here PolySilicon is the gate material that is used. H_{FIN} and W_{FIN}, for the standard FinFET simulated in the paper, are 30 nm and 6 nm, respectively. The SD-FinFET device exhibits identical heights H4 and H6, as similar widths W4 and W6. However, the source side (Wt) is larger than the drain side fin's width (W5). The SF-FinFET has equal widths W3 and W1, as equal heights H1 and H3.

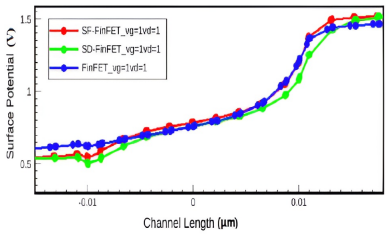


Figure 2.25. Surface Potential plot of the device along the channel length. [RT17]

Controlling the SCE requires a greater surface potential in the channel region. In the channel region, each device's surface potential is nearly equal.

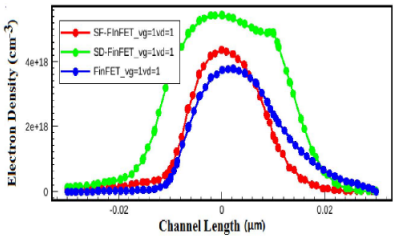


Figure 2.26. Electron Density plot of the devices along the channel length. [RT17]

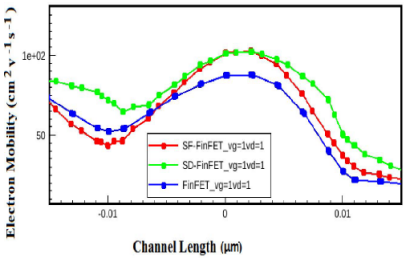


Figure 2.27. Electron Mobility plot of the devices along the channel length. [RT17]

More observations are made of the SD-FinFET's electron density and mobility than the other two devices. The structure's channel region's descending order of electric density is SD-FinFET > SF-FinFET > FinFET. At V_D = 1V and V_G = 1V, surface potential, electron density, and electron mobility are observed.

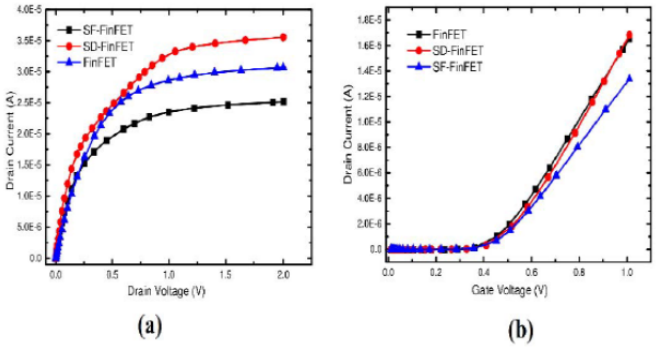


Figure 2.28. (a) Id-Vd plot and (b) Id-Vg plot of the devices. [RT17]

Elevated drain current in the SD FinFET device due to enhanced electron mobility and density in the channel area. For SF-FinFET, SD-FinFET, and FinFET, the off-state leakage currents are determined to be 2.56×10^{-13}A, $4.51 \times 10^{-13}A$, and $4.577 \times 10^{-13}A$. Every gadget displays a modest leakage current in the off state. SF-FinFET, SD FinFET, and FinFET are found to have I_{ON} values of 25µA, 35.6µA, and 30.6µA, respectively. The constant current method is used to determine V_{TH}. The values of V_{TH} for SDFinFET, SF-FinFET, and FinFET are determined to be 0.42V, 0.45V, and 0.44V, respectively.

Device	$I_{ON}(\mu A)$	SS $(\frac{mV}{decade})$	DIBL$(\frac{mV}{V})$	$\frac{I_{ON}}{I_{OFF}}$(A)
FinFET	30.6	70.89	22.15	6.68×10^7
SF-FinFET	25	71.13	23.49	9.76×10^7
SD-FinFET	35.6	73.23	32.12	5.76×10^7

Table 2.3. Comparison of device electrical parameter for N-channel. [RT17]

Device	$I_{ON}(\mu A)$	SS $(\frac{mV}{decade})$	DIBL$(\frac{mV}{V})$	$\frac{I_{ON}}{I_{OFF}}$(A)
FinFET	-21.9	71.91	30.15	1.19×10^8
SF-FinFET	-16.57	70.79	33.88	1.40×10^8
SD-FinFET	-26.89	70.36	35.83	1.224×10^8

Table 2.4. Comparison of device electrical parameter for P-channel. [RT17]

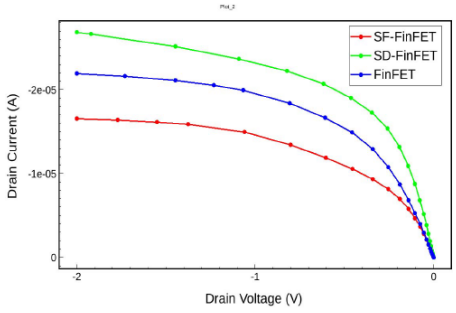


Figure 2.29. Id-Vd plot P-channel of the devices. [RT17]

For FinFET, SF-FinFET, and SD-FinFET, respectively, I_{OFF} for P-channel devices are -1.84×10^{-13}A, -1.182×10^{-13}A, and -2.197×10^{-13}A.

2.2.1 Analog parameters

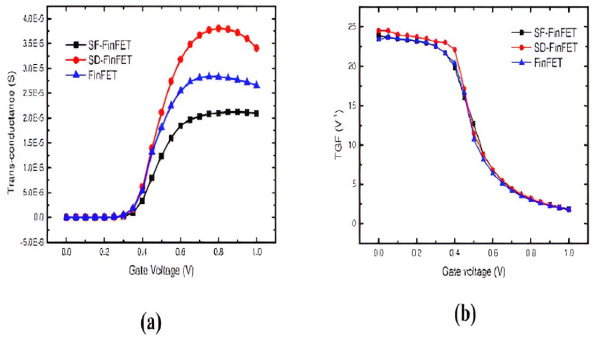


Figure 2.30. (a) G_M plot (b) TGF plot of the device Vd=1V. [RT17]

When the drain bias is applied, the SD-FinFET device has a higher G_M than the other two devices. This high G_M is attained because there is a greater variation in I_D inside a given V_{GS}, and the CLM effect in the saturation region causes it to saturate after the peak value. For a given level of I_D, the translation of G_M is represented by the quality factor TGF. The maximum value of TGF occurs at weak inversion. The SD-FinFET device achieves its maximum value of TGF at low V_G. Due to power consumption concerns, a high value of TGF results in a forfeit in a high linearity microwave system.

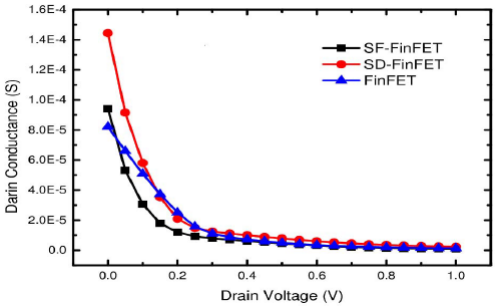


Figure 2.31. Drain-conductance plot at Vg=1V w.r.t. drain voltage. [RT17]

2.2.2 RF parameters

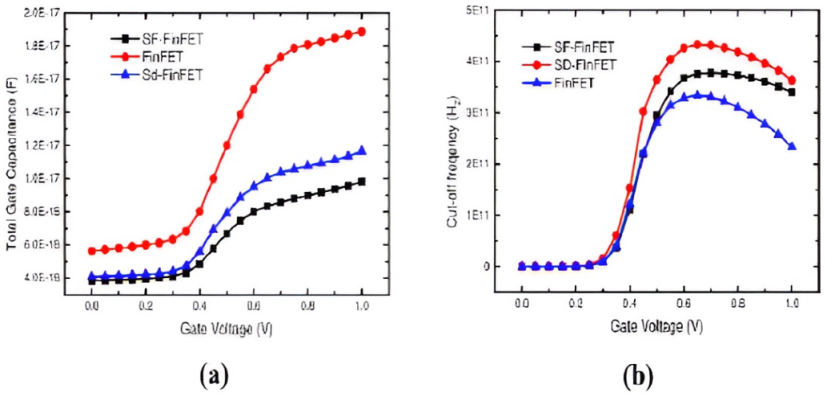


Figure 2.32. (a) C_{GG} plot (b) F_T plot w.r.t. gate voltage. [RT17]

AC small signal analysis extracts the C_{GG}. A frequency of 1MHz is used to extract capacitance, and V_G is ramped through step sizes of 0.05 V from 0 to 1 V. SF-FinFET displays a reduced C_G. C_G saturates when the device enters the saturation region because CLM occurs in this region, maintaining a constant charge in the channel region. The frequency at which the current gain is unity is F_T. F_T is lower in SD-FinFET.

$$F_T = \frac{G_M}{2\pi \cdot (C_{GS} + C_{GD})} = \frac{G_M}{2\pi \cdot C_{GG}} \tag{2.1}$$

$$GFP = \frac{G_M}{G_D} \cdot F_T \tag{2.2}$$

When using an operational amplifier in a high-frequency application, GFP is crucial.

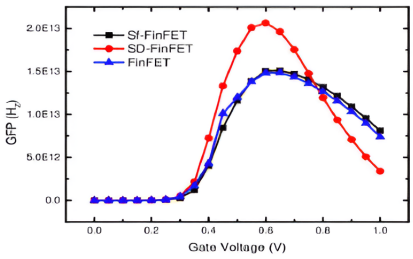


Figure 2.33. (a) GFP plot at Vd=1V with a variation of gate voltage. [RT17]

When V_G rises from the subthreshold area, it rises, finds an optimal position, and then decreases in the saturation region. SD FinFET produces superior results.

Parameter	cFinFET	SF-FinFET	SD-FinFET
$G_M(\mu S)$	28.3	21.2	38.0
$G_D(\mu S)$	82.2	94.2	114
TGF (V^{-1})	23.9	23.4	24.5
Gain (dB)	30.8	32.4	36.1
C_{GG} (pF)	1.16×10^{-2}	9.82×10^{-3}	2.33×10^{-2}
F_T (GHz)	433	378	334
GFP (GHz)	1.49×10^4	1.51×10^4	2.06×10^4

Table 2.5. Comparison of analog and RF parameters of the devices. [RT17]

2.2.3 Digital parameters

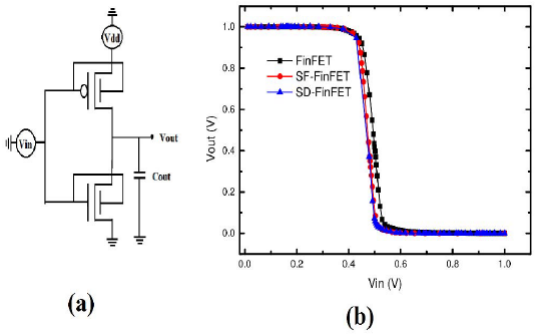


Figure 2.34. (a) Inverter Circuit using FinFET device (b) VTC curve for the devices. [RT17]

Circuit diagram for an inverter utilising PMOS and NMOS FinFET construction. Compared to a standard FinFET, the SF-FinFET has a steeper output logic switch. SF-FinFET > SD-FinFET > cFinFET is the observed descending order of steepness. Using C_{OUT} equal to 1×10^{-17}F, the results are obtained. Analysing the inverter circuit's noise margin is crucial in understanding how well the devices work in digital applications. For SF-FinFET, the lowest transition is attained.

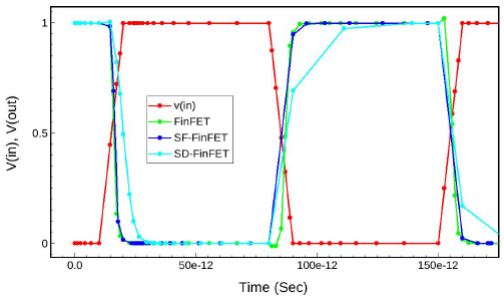


Figure 2.35. Switching characteristics plot of the devices. [RT17]

Mixed mode simulations with a pulse of 10 ps delay time, 10 ps rise time, 10 ps fall time, 60 ps ON time, and 140 ps period of one cycle for 200 ps duration at a voltage of amplitude 1V are used to assess the switching characteristics. Following the simulation tPHL, tPLH, tp, and gain are computed for a 1×10^{-17}F output capacitance or load capacitance.

Parameter	cFinFET	SF-FinFET	SD-FinFET
V_{IL} (V)	0.442	0.431	0.424
V_{IH} (V)	0.543	0.516	0.543
NM_L (mV)	441.95	425.96	423.51
NM_H (mV)	456.34	483.39	486.48
TR (mV)	100.91	85.18	89.11
τ_{PHL} (ps)	2.11	1.62	4.54
τ_{PLH} (ps)	0.49	0.3	2.27
τ_P (ps)	1.3	0.96	3.41
Gain	-14.58	-15.5	-14.5

Table 2.6. Comparison of noise margin and propagation delay for the devices. [RT17]

Comparing the SF-FinFET to the other two devices, it exhibits faster switching.

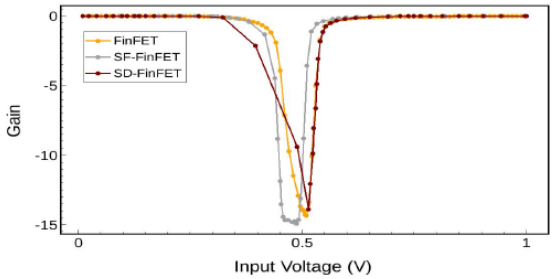


Figure 2.36. Gain plot of inverter circuit. [RT17]

2.3 14 nm RF finFETs

FinFET devices designed exclusively for the RF field are beginning to be produced. The 14 nm analog and RF technology node in detail. With V_{DD} of 0.8 V for the core (thinner oxide) and 1.2, 1.5, and 1.8 V for the I/O (thicker oxide) RF transistors, it is an expansion of the logic FinFET Platform technology based on 14 nm.

Technology	14 nm FinFET		28 nm planar FET (HiK MG)	
Device	NFinFET	PFinFET	NFET	PFET
L_G (nm)	14		30	
CPP (nm)	78		126	
V_{DD}	0.8		1.05	
$I_{D,sat}(\mu A/\mu m)$	1523	1433	670	450
$G_{M,sat}(\mu S/\mu m)$	3017	2748	985	395
F_T/F_{MAX} (GHz)	314/180	285/140	308/159	185/102
$\frac{F_T \cdot G_M}{I_D}$ (GHz/V)	2650	2053	2000	1150

Table 2.7. Comparison of key core device design and DC/AC parameters. [LS18]

Demonstrates a considerable improvement in terms of I_D and G_M over 28 nm FETs. To offer strong substrate isolation to μV level RF and analog signals, a deep n-well technique is also used.

2.3.1 Results

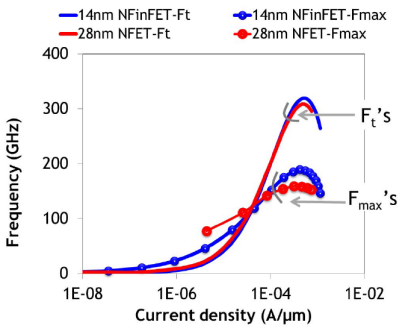


Figure 2.37. Metal-1(m1) level F_T and F_{MAX} versus Jd from a minimum Lg = 14 nm and 12-Fin NFinFET device. [LS18]

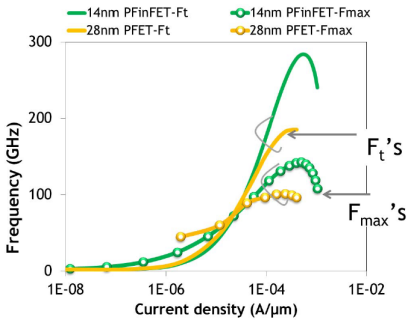


Figure 2.38. Metal-1(m1) level F_T and F_{MAX} versus Jd from a minimum Lg = 14 nm and 12-Fin PFinFET device. [LS18]

At the metal-1 level, the pad and the interconnect parasitic have been eradicated with an open, brief, and thorough de-embedding approach. FinFET's greater G_M allows it to attain a higher peak F_T. For the first time, it is thought to be comparable to the F_T of N-FinFET devices. A notable rise in P-FinFET device count is also noted compared to prior node planar P-FET device counts. Deep silicon cavities are created in the S/D region of the FinFET during fin silicon etching in the 14 nm FinFET manufacturing. The next processing step involves growing a boron-doped SiGe epitaxy stressor in the cavity area. This stressor increases the total hole carrier mobility by exerting a compressive force over the fin channel region. Consequently, a notable rise in the device G_M is noted, which is implied by the greater F_T (285 GHz) compared to the 185 GHz of the 28 nm planar P-FETs. In addition, the F_{MAX} of N and P FinFETs is substantially more than that of the planar N and PFET devices, which are 28 nm in size. The FinFET F_{MAX} performance is negatively impacted by the R_G; nevertheless, FinFET continues to perform better because of the greatly enhanced F_T and G_M.

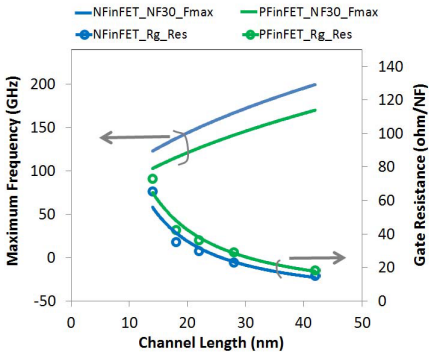


Figure 2.39. F_{MAX} and R_G relationship with N/PFinFET L_G. [LS18]

Despite having a lower F_T, FinFET with the longer L_G improves the F_{MAX}.

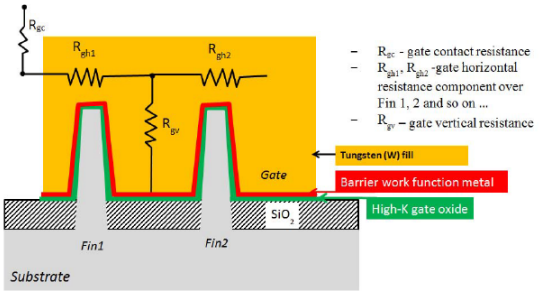


Figure 2.40. Gate horizontal and vertical resistance component in the FinFET RMG wrap-around gate structures. [LS18]

Compared to the planar 28 nm technology, the R_{GV} component is larger and more dominant.

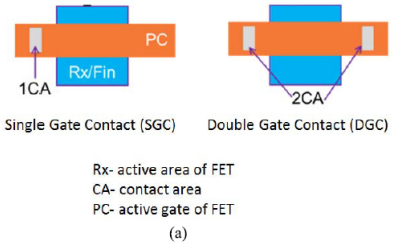


Figure 2.41. (a) Layout of the SGC and DGC device structure. [LS18]

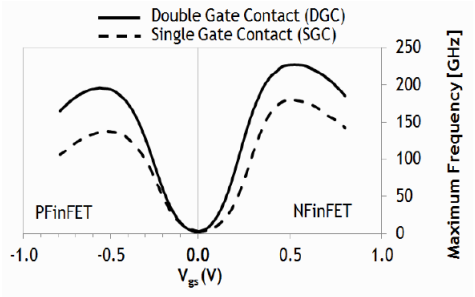


Figure 2.42. (b) Comparison of the SGC and DGC F_{MAX} performance versus V_{GS} of the N/PFinFET. [LS18]

A noteworthy F_{MAX} enhancement For N and P-FinFETs with DGC structure, it is possible to obtain 1.26 and 1.40 times that of SGC devices. While maintaining a lower device footprint, the intrinsic performance of 14-nm FinFET technology beats that of 28-nm planar FETs.

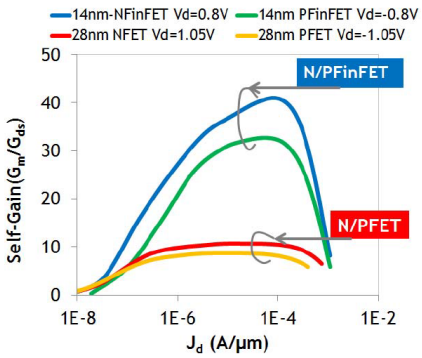


Figure 2.43. Self-gain (Gm/Gds) versus J_D of the N and PFET devices from 14 nm and 28 nm planar technologies, respectively. [LS18]

FinFET suffers full channel depletion during on-state operation, which improves electrostatic gate control over the channel region. This effectively results in a better device scaling with reduced G_{DS} and suppresses the SCEs punchthrough and DIBL. The 14-nm FinFET technology achieves more than three times as self-gain as the 28-nm technology. FinFET's three-dimensional architecture allows for a big W_{FIN} in a small device footprint, which benefits G_M.

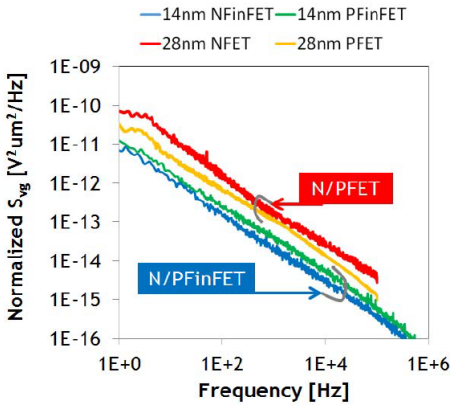


Figure 2.44. Normalized input-referred $\frac{1}{f}$ Svg versus frequency from the 28 nm planar and 14 nm FinFET technologies. [LS18]

Compared to the 171 and 106 $fV^2\mu m^2/Hz$ of the 28 nm planar N and P-FETs, the Svg of N and P-FinFET devices is 17 and 35 $fV^2\mu m^2/Hz$ at 1 kHz. Similar to core FinFETs, the 1.8 V thick gate oxide I/O N/P-FinFETs show outstanding peak F_T (50.1/53.5 GHz) and F_{MAX} (200/160 GHz).

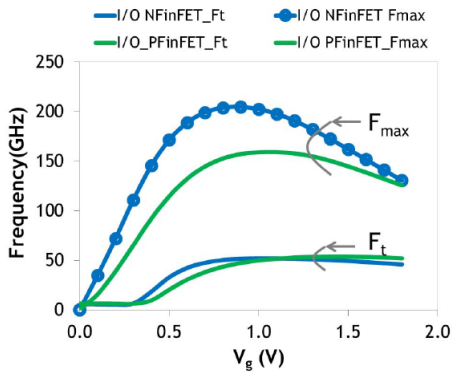


Figure 2.45. F_T and F_{MAX} of 1.8V I/O of L_G = 150 nm N/P FinFET versus Vg (gate bias voltage) characteristics. [LS18]

This I/O FETs have longer L_G, due to their higher voltage operation a high current can be drawn, which opens up possibilities for supporting RF power amplifier and cellular designs. ULVT FinFET devices with decreased V_{DD} are available for lower voltage operation. In certain RF design scenarios, these devices provide near zero V_T operation with significant power reduction. The next lowest V_T (180 mV) device designers can use is the SLVT. 30% of power is saved by the ULVT device oscillator circuit.

2.3.2 Deep N-Well analog device

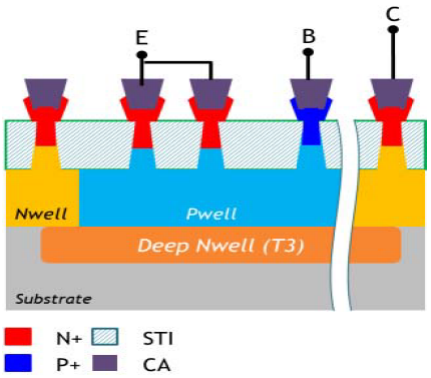


Figure 2.46. Schematic x-sectional view with label N+/P+ dopant, STI, and CA with emitter (E), base (B), and collector terminals. [LS18]

When V_{BE} is low, the VNPN device exhibits a well-behaved Gummel characteristic with a low I_B.

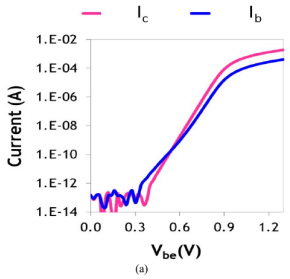


Figure 2.47. (a) Gummel characteristics I_C, I_B versus V_{BE} at 0.8 V of V_{CB} of VNPN bipolar transistor. [LS18]

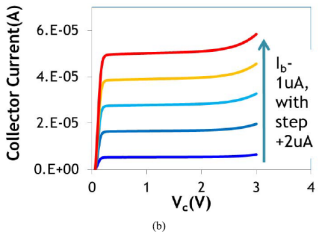


Figure 2.48. (b) I_C-V_C curve. [LS18]

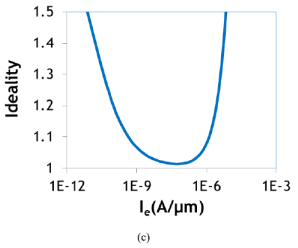


Figure 2.49. (c) Ideality characteristics of the VNPN bipolar device. [LS18]

Low carrier production and recombination levels occur at the bipolar cell's emitter and base junction. It offers a different device choice for circuits containing temperature sensors. The VNPN operate well up to 3 V, however 2.5 V is the maximum they can operate at due to device dependability. At 10 $\mu A/\mu m$, the ideality of VNPN bipolar reaches a value of 1.03, providing an additional device possibility for low circuit designs. Because these locations have less doping, the deep n-well junction with either a p-well (upper side) or p-type substrate (bottom side) can give a higher junction breakdown voltage.

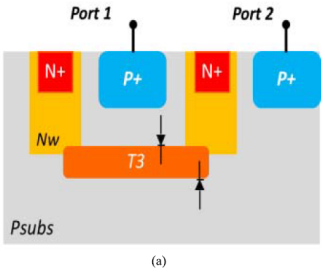


Figure 2.50. (a) Cross-sectional view of the bottom region of deep n-well isolations. [LS18]

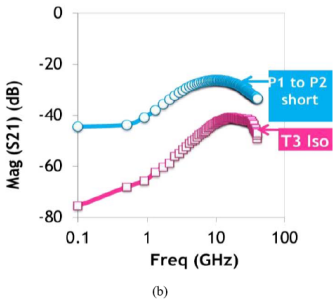


Figure 2.51. (b) Substrate coupling (S21) measured silicon results with deep n-well (T3) isolation or without T3 (P1 to P2 short) structures. [LS18]

With deep n-well isolation, noise reduction is most effective in the 0.1–10 GHz frequency region and can reach a maximum of 75 dB substrate noise reduction at 0.1 GHz.

2.4 Standard, wide and hybrid finFETs

The breakdown voltage of low-voltage FinFETs is usually less than 3 V, making them unsuitable for high-voltage or RF power applications. For devices having a drain-extension

length LD = 400 nm, the V_{BD} under the OFF-state condition is boosted beyond 6.5 V by adding a LDD extension between the channel and the drain contact. The R_{ON} = 6.9 Ω· mm is the standard finFET. The I_D increase and the hybrid device achieves the highest current by increasing WD. This smaller R_D suppresses the quasi-saturation effect.

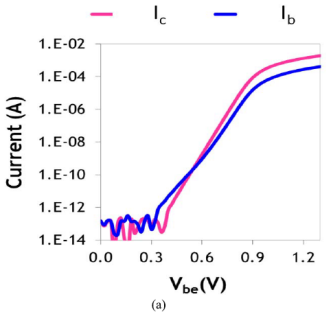


Figure 2.52. (a) Output [HC18] and

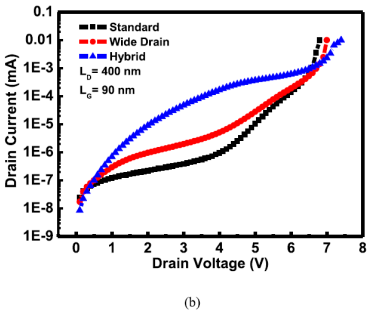


Figure 2.53. (b) breakdown characteristics of power FinFETs with different drain-extension structures. [HC18]

3.4 and 1.7 Ω· mm are the R_{ON} of wide drain and hybrid FinFETs, respectively. Wide drain extension area increase the risk of leakage current moving from drain to source beneath the low-doped fin.

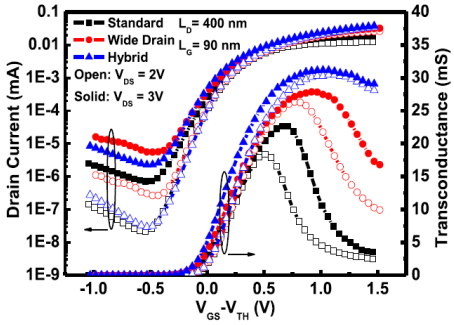


Figure 2.54. Transfer characteristics of power FinFETs with different drain extension structures. [HC18]

FinFETs with wide drain and hybrid designs exhibit superior G_{DS} properties. For analog and RF applications, higher G_Ms are necessary since they are connected to numerous significant merit parameters, including the intrinsic A_V, F_T, and F_{MAX}.

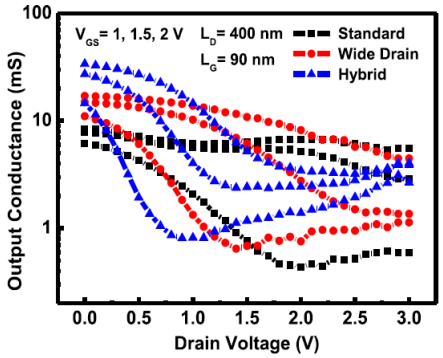


Figure 2.55. Output conductance as a function of the drain voltage of power FinFETs with different drain-extension structures. [HC18]

The wide drain and hybrid devices have larger G_{DS} in the saturation regime than the normal one at $V_{GS} = 1$ V. Conversely, the wide drain and hybrid devices show lower G_{DS} values when the gate voltage rises to 1.5 and 2 V, which may mean that they have greater intrinsic and F_{MAX}. Set the IP3 as high as possible to operate with little distortion.

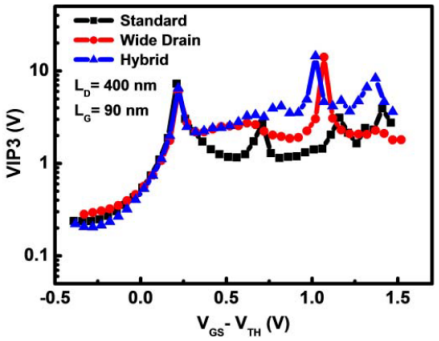
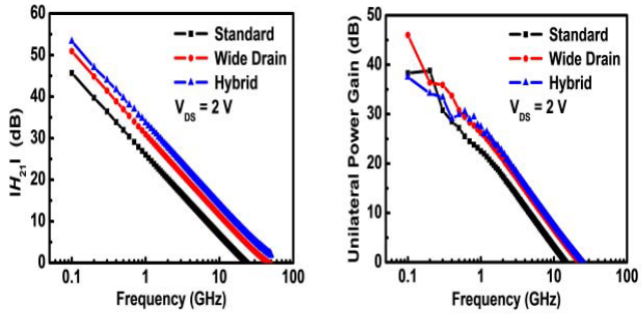


Figure 2.56. VIP3 as a function of gate voltage overdrive of power FinFETs with different drain-extension structures. [HC18]

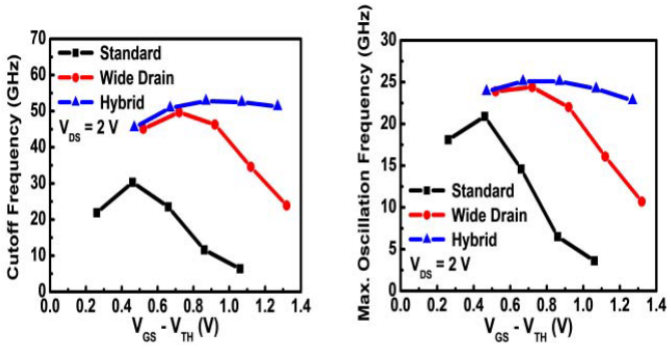
All device topologies show comparable IP3 values in the subthreshold region (V_{GS} - $V_{TH} < 0$), suggesting that the larger leakage current in the wide drain and hybrid devices does not affect the device linearity. The typical device exhibits poor linearity behaviour as devices run under the strong inversion situation because of its large G_M roll-off at high V_{GS}s. Cause signal distortion as a result. Among the several drain-extension structures, the hybrid device has the highest $3^{RD} Intercept Point$ (IP3) values because it has the most improvement in G_M features.



(a) (b)

Figure 2.57. (a) |H21| and (b) unilateral power gain as a function of the frequency of power FinFETs with different drain-extension structures. [HC18]

Because R_G is high in our devices, F_{MAX} is significantly lower than F_T. To improve F_{MAX}, it is advised to employ the multilayer metal process. As the breadth of the drain extension increases, so do F_T and F_{MAX}.



(a) (b)

Figure 2.58. (a) F_T and (b) F_{MAX} as a function of gate V_{OV} of power FinFETs with different drain-extension structures. [HC18]

When the gate V_{OV} is larger than 0.7 V, the influence of R_D makes the variations in high-frequency parameters between different drain-extended devices more noticeable. The C_{GS} and C_{GD} may also have an impact on F_T and F_{MAX}.

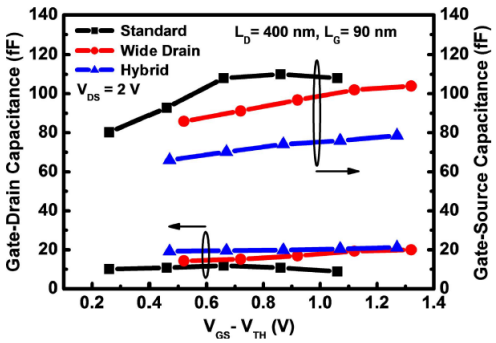


Figure 2.59. C_G as a function of gate V_{OV} of power FinFETs with different drain-extension structures. [HC18]

As the drain-extension width increases, the C_{GS} decreases. Peak F_T is enhanced by 64% and 77%, for wide drain and hybrid devices compared to normal devices, but peak F_{MAX} is only enhanced by 17% and 20%.

	Standard	Wide Drain	Hybrid
$G_M/I_D(V^{-1})$	-	1.2	1.5
A_V	-	11.6	13.7
V_EA (V)	-	9.2	9.7
Peak F_T (GHz)	30	50	53
Peak F_{MAX} (GHz)	21	24	25

Table 2.8. Summary of analog and RF parameters at $V_{DS} = 2$ V. [HC18]

Chapter 3

State of the art

3.1 Nanosheet

Nonetheless, current research has shifted to novel devices such as nanosheets, which exhibit improved A_V and comparable F_T values but worsening F_{MAX}.

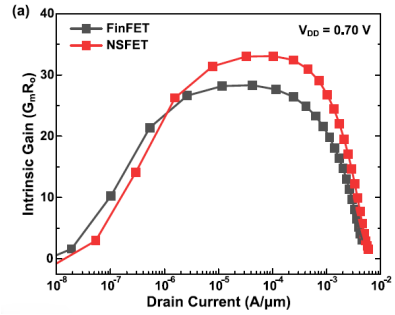


Figure 3.1. (a) G_MR_O [YB20]

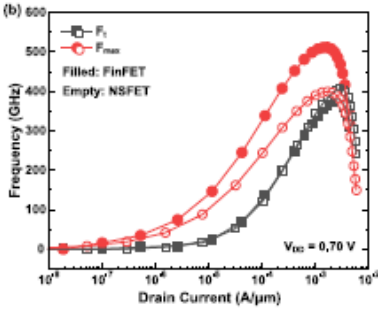


Figure 3.2. (b) F_T, F_{MAX} of FinFETs and NSFETs. [YB20]

Because NSFETs have greater W_{FIN} and better electrostatics than FinFETs within the same footprint, they have a larger G_MR_O than FinFETs. At tiny I_{DS} near $10^{-7}A/\mu$ m, there is a cross-over of G_MR_O between NSFETs and FinFETs because of the increased dopant penetration into the channel of NSFETs, which reduces the R_O. Ge intermixing promotes larger dopant penetration by aiding the diffusion of additional phosphorus dopants into the channels. Conversely, NSFETs and FinFETs have nearly identical F_T but different F_{MAX} values. FinFETs and NSFETs have reasonable G_MR_O since the reference article [YB20] had well-calibrated DC parameters. Because the parasitic RC components of metal interconnects are not included in the study, F_T and F_{MAX} were slightly larger. However, FinFETs and NSFETs have identical metal-line arrangements under the same CPP. The quantitative analog/RF FinFETs and NSFETs performances at the FEOL level are comparable too.

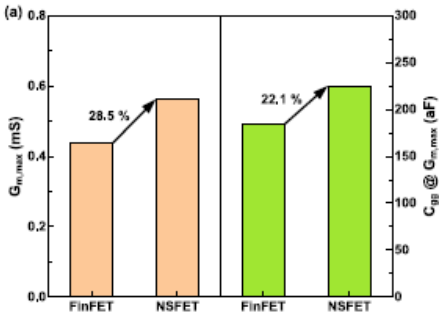


Figure 3.3. (a) $G_{M,max}$ and C_{GG} at the $G_{M,max}$ point. [YB20]

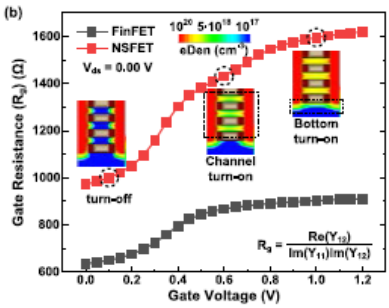


Figure 3.4. (b) R_G of 2-fin FinFETs and NSFETs under the same footprint. [YB20]

C_{GG} was extracted from the C_{GG}-V_{GS} curve at a particular V_{GS} point, and G_M was extracted from the derivative of the I_{DS}-V_{GS} curve. While F_{MAX} is inversely proportional to R_G, F_T is proportional to G_M/C_{GG}. Despite the 28.5% increase in $G_{M,max}$ from fin to NS, C_{GG} increases as well because the NSFET's large W_{NS} of 40 nm results in a bigger W_{FIN}, which raises C_{OV} and C_{OF} between the gate and S/D. Using Y parameters, R_G was derived as Re(Y12)/(Im(Y11)Im(Y12) at V_{DS} of 0 V. Although there is another way to extract R_G as Re(Y11)/Im(Y11)2, the results of these two approaches are nearly identical.

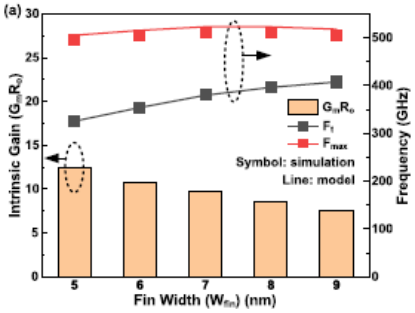


Figure 3.5. Analog/RF FoM of FinFETs having different (a) Wfin. [YB20]

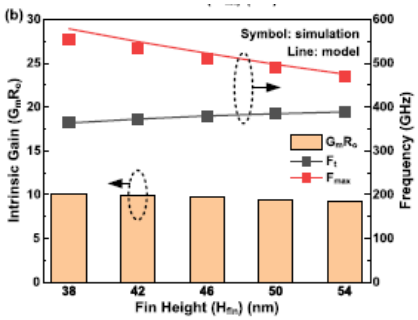


Figure 3.6. (b) Hfin splits. [YB20]

NSFETs' intricate MG arrangement that encircles the channel gives them a higher R_G than FinFETs. Moreover, the MG height is lengthened and the R_G is increased at the top-most NS spacing region. $G_M R_O$ rises when G_M falls yet R_O rises significantly as the W_{FIN} falls. In particular, smaller W_{FIN} not only decreases the SCEs, which is directly related to the G_M, but also significantly increases R_O. For F_T and F_{MAX}, the model equations are provided simply by:

$$F_T = \frac{G_M}{2\pi C_{GG}} \tag{3.1}$$

The $R_{G,int}$ is decomposed from the S/D resistance R_{SD}, G_{DS} is Output conductance, and C_{GD} is Output conductance.

$$F_{MAX} = \frac{F_T}{\sqrt{4R_{G,int}(Gds + 2\pi F_T C_{GD})}} \tag{3.2}$$

.

Metal Gate (MG) resistance and intrinsic channel resistance make up $R_{G,int}$. For any split between W_{FIN} and H_{FIN}, the simulation and model outcomes of F_T and F_{MAX} are well matched. Using the Y-function method, R_{SD} is extracted, and $R_{G,int}$ is computed as follows:

$$R_{G,int} = R_G - \frac{1}{4}R_{SD} \tag{3.3}$$

.

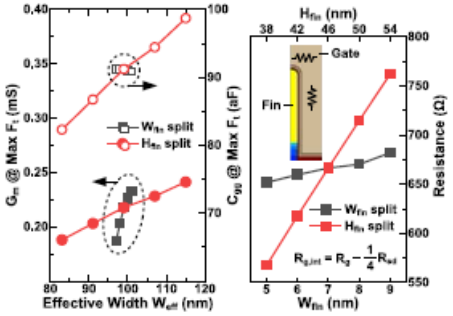


Figure 3.7. G_M and C_{GG} at the maximum F_T point (left) and $R_{G,int}$ decomposed from R_{SD} (right). [YB20]

Greater W_{FIN} raises G_M as opposed to C_{GG}, which raises F_T; however, H_{FIN} significantly shifts C_{GG} whereas W_{FIN} does not; as a result, the rise in F_T is not as substantial as that for the W_{FIN} splits. Greater C_{OV} but smaller inversion capacitance because of V_{TH} yields constant C_{GG} for bigger W_{FIN}. Depending on the S/D doping profile, this trend varies; as W_{FIN} grows, FinFETs with smaller Junction gradients increase C_{PARA} and C_{GG}. The C_{OV} associated with the Junction gradients inside the channel, the C_{OF} between the gate and S/D epi and extension, and the contact capacitance between the gate and S/D metal lines are all included in C_{PARA}. Like how the W_{FIN} declines, phosphorus from S/D is separated at the channel/oxide interface. While F_{MAX} reduces significantly as H_{FIN} increases, F_{MAX} remains rather constant regardless of W_{FIN}. The $R_{G,int}$ is the only source of F_{MAX} difference between W_{FIN} and H_{FIN} splits. Longer MG heights increase $R_{G,int}$ and hence decrease F_{MAX} as H_{FIN} increases; but, as W_{FIN} increases, larger F_T compensate larger $R_{G,int}$ by thinner MG heights, and as a result, the F_{MAX} is almost equal.

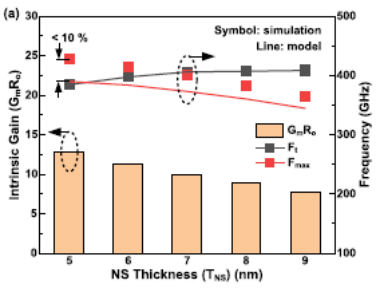


Figure 3.8. G_MR_O, F_T, F_{MAX} of NSFETs having different (a) TNS. [YB20]

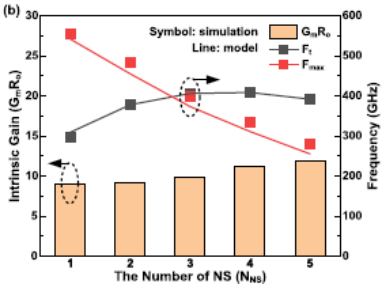


Figure 3.9. (b) NNS. [YB20]

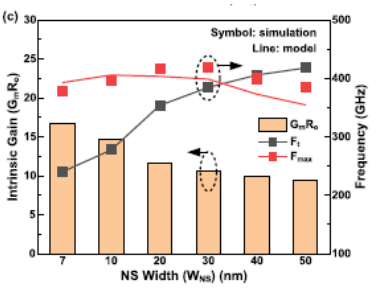


Figure 3.10. (c) WNS splits. The maximum error of Fmax is below 10%. [YB20]

Thinner T_{NS} and W_{NS} raise the G_MR_O similarly to FinFETs by improving gate-to-channel controllability and significantly increasing the R_O. Conversely, higher N_{NS} at the W_{NS} of 40 nm preserves the SCEs but significantly raises G_M instead of letting R_O drop, leading to higher G_MR_O. While F_T simulation and model results are equal, F_{MAX} is not since $R_{G,int}$ contains the bottom transistor, which has little effect on NSFET DC/AC performances because of S/D over-etching. A value for $R_{G,int}$ that does not include the bottom transistor is necessary to match the simulation results and model of F_{MAX}. The following describes F_T trends as a function of T_{NS}, N_{NS}, and W_{NS}. Bigger T_{NS} and W_{NS} raise F_T because they increase G_M instead of C_{GG}. Due to bigger W_{FIN}, more N_{NS} also raises G_M; however, they also critically increase C_{PARA} of the NS spacing regions and C_{GG}. Because longer carrier pathways are required to flow the bottom-side Nano Sheet (NS) channels, the rate of rise of the Ids and G_M is less than the rate of increase of the C_{GG} as the N_{NS} increases.

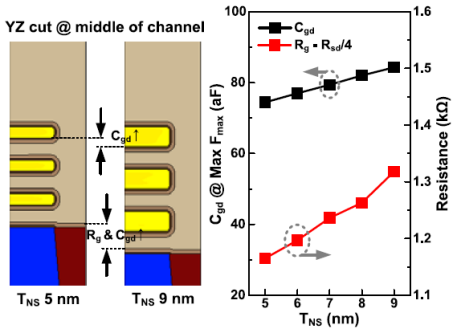


Figure 3.11. 2-D schematic views of NSFETs with TNS of 5 and 9 nm at the middle of the channel (left) and Cgd and Rg;int of NSFETs with different TNS (right). [YB20]

Greater W_{FIN} = 2(W_{NS}+T_{NS}) x N_{NS} raises C_{GD}, and longer MG height increases $R_{G,int}$ and C_{GD}, hence decreasing F_{MAX} as the T_{NS} changes from 5 to 9 nm. Larger $R_{G,int}$ and C_{GD} from longer MG height can account for the significant drop in F_{MAX} for

greater N_{NS}.

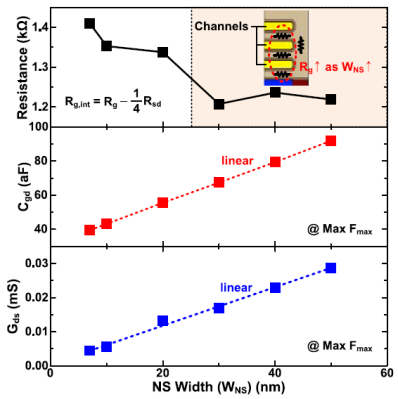


Figure 3.12. $R_{G,int}$, C_{GD} and G_{DS} of NSFETs with different W_{NS}. [YB20]

The NS spacing width is increased by W_{NS}, while the MG height remains unchanged. The $R_{G,int}$ does not drop above the W_{NS} of 30 nm because there is a compensation of $R_{G,int}$ between wider NS and longer NS spacing width. Conversely, when W_{NS} increases, C_{GD} and G_{DS} increase linearly. As a result, when the W_{NS} varies from 7 to 30 nm, the F_{MAX} grows. However, as the W_{NS} increases beyond 30 nm, the F_{MAX} falls because of the ongoing increases in $R_{G,int}$ and C_{GD}. The S/D epi size is reduced by thinner NS T_{SP}, but the channel stresses remain relatively constant; when the T_{SP} shifts from 16 to 8 nm, 0.78 GPa to 0.70 GPa. The S/D epi size has no effect on the I_{DS} since the R_{SD} is mostly affected by the S/D extension rather than the S/D epi. The NSFETs' DC performance metrics are nearly identical.

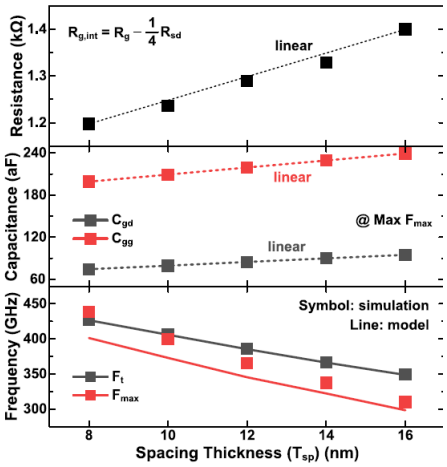


Figure 3.13. $R_{G,int}$, C_{GG}, C_{GD}, F_T and F_{MAX} of NSFETs with different T_{SP}. [YB20]

Parameters of NSFETs with varying T_{SP}, such as F_T and F_{MAX}, are analog/RF. Because of the shorter MG height, $R_{G,int}$, C_{GD}, and C_{GG} decrease linearly as T_{SP} declines. Consequently, F_T and F_{MAX} grow. By raising the ρ MG, thinner T_{SP} may raise the $R_{G,int}$. In practice, there might be a F_{MAX} bottleneck at a specific T_{SP}.

Analog/RF FoM		Device Design	Max
FinFET	$G_M R_O$	$W_{FIN} = 5nm, H_{FIN} = 38nm$	12.7
	F_T	$W_{FIN} = 9nm, H_{FIN} = 54nm$	413 GHz
	F_{MAX}	$W_{FIN} = 7nm, H_{FIN} = 38nm$	555 GHz
NSFET	$G_M R_O$	$T_{NS} = 5nm, N_{NS} = 2, W_{NS} = 7nm$	20.1
	F_T	$T_{NS} = 9nm, N_{NS} = 3, W_{NS} = 50nm$	441 GHz
	F_{MAX}	$T_{NS} = 5nm, N_{NS} = 1, W_{NS} = 40nm$	604 GHz

Table 3.1. Device design guideline for best $G_M R_O$, Ft and Fmax. [YB20]

The optimal $G_M R_O$ for FinFETs can be achieved by decreasing W_{FIN} to improve gate-to-channel controllability and by decreasing H_{FIN} to achieve bigger R_O as opposed to smaller G_M. When both W_{FIN} and H_{FIN} rise for greater current drivability, the best F_T is attained. When shorter MG height is made for smaller C_{GG} and $R_{G,int}$, the best F_{MAX} is at shorter H_{FIN}. Regarding optimal $G_M R_O$, F_T, and F_{MAX}, NSFETs and FinFETs have comparable device design regulations. To reduce C_{GG} and $R_{G,int}$ while keeping the same DC performances, T_{SP} should drop in all circumstances. It is therefore preferable to raise the $G_M R_O$, but only at the N_{NS} of 2. Thinner T_{NS} and W_{NS} increase G_M much compared to R_O reduction. The optimal F_T is achieved at the N_{NS} of 3, but only when T_{NS} and W_{NS} rise for greater current drivability. There is an ideal point for the best F_T ($N_{NS} = 3$). Greater N_{NS} raises G_M as well as C_{GG}, but the rising rate of G_M gets smaller as N_{NS} grows. By balancing between $R_{G,int}$ and F_T at the T_{NS} and N_{NS} of 5 nm and 1, respectively, when the $R_{G,int}$ is modest, the W_{NS} of 40 nm is optimal for the best F_{MAX}. With appropriate device design, NSFETs perform better than FinFETs, which is expected for analog/RF applications.

3.2 Intrinsic VS extrinsic elements

Apart from the NS, the NWs are also beginning to be assessed. Although they exhibit comparable behaviour when the width diminishes in comparison to the SCEs, they do not show the same behaviour when it increases in I_D and G_M.

3.2.1 G_M/I_D characterization technique

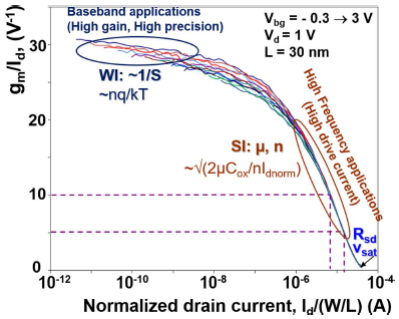


Figure 3.14. $G_M/I_D vs I_D/(W/L)$ plot for 30 nm-long FDSOI device with different V_{BG}. [RF21]

One can see that while normalised I_D is virtually constant for "long" NW MOSFET, strong improvement is noticed with NW width decrease in the case of "short" device. This behaviour, which is devoid of geometry and the V_{TH} effect, is associated with better control of SCEs in the narrow NWs. It is worth noting that these NWs are almost square/Ω-like, with a sidewall height of 10 nm, which is rather tiny compared to the NW width (the narrowest device is 17 nm wide only). In these devices with complicated 3D conduction, the typically seen improvement in I_D and G_M with a rise in NW or W_{FIN}, associated with the mobility enhancement when the top-plane concerning sidewalls dominates conduction, almost disappears. It is evident that although strain has a positive effect in the strong inversion zone (because of the focused μ improvement), there is some degradation in the weak inversion regime (because of the reduced SCE control). Thus, one would select a device with or without strain based on the intended application, which may be baseband (high-precision, gain) or high-frequency/high-current. Lowering the temperature is considered advantageous for both base-band and high-frequency applications, both in weak inversion (because of SS improvement) and in strong inversion (because of mobility improvement).

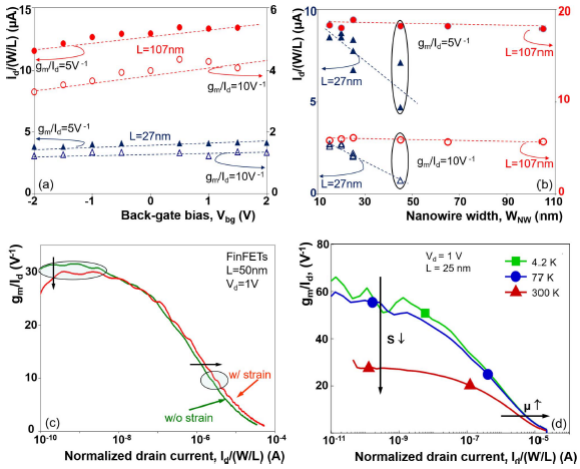


Figure 3.15. (a) Variation of Id/(W/L) in UTBB SOI MOSFET as a function of Vbg. Vd = 1 V. (b) Variation of Id/(W/L) taken at gm/Id = 10 and 5 V^{-1} in NW MOSFETs as a function of NW width. Vd = 1 V. (c) gm/Id as a function of Id/(W/L) in FinFETs with and without strain. (d) gm/Id as a function of Id/(W/L) in FDSOI MOSFET at different temperatures. [RF21]

3.2.2 $G_M - A_V$ analog metric

One wants both G_M and A_V to be as high as possible for analog applications.

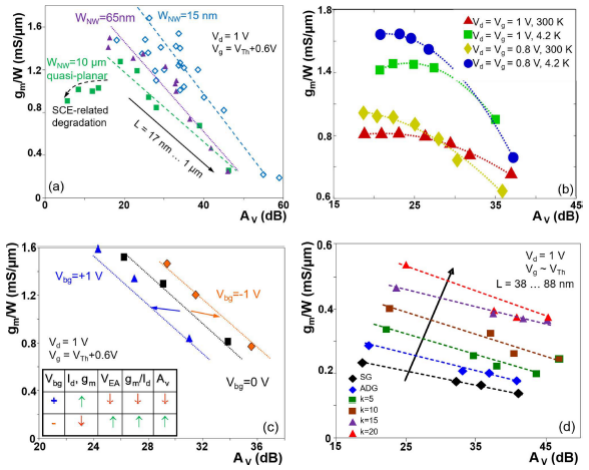


Figure 3.16. $G_M - A_V$ metric application in the case of (a) various NW MOSFETs, (b) FDSOI MOSFETs at room and cryogenic temperatures; (c) UTBB SOI MOSFETs at different back-gate biases; (d) UTBB SOI MOSFETs operating in ADG and QDG regimes. [RF21]

The performance of the device is improved in "narrow" NWs when compared to their

wide counterpart, both in terms of G_M and A_V. This is a result of the "narrow" device's "volume inversion" and "SCE" operation regimes being better controlled. This enhancement was made possible by the well-tolerated degradation effects, including higher R_{SD}, μ decrease, and interface quality, that frequently occur with NW narrowing. In short channels of wide NW devices, one can also observe a decline in performance and loss of control. Improvement in gadget performance when the temperature drops. Mobility enhancement at cryogenic temperatures leads to significant improvements in G_M values, especially in "long" channel devices; A_V values also show a minor improvement. One will select a "positive" back-gate bias for high-gain, high-precision applications or a "negative" back-gate bias for high G_M and consequently high-frequency applications, depending on the intended application. Degrading VEA and A_V is the consequence of "negative" V_{BG} drawing the channel away from the top gate and worsening control of SCE. This is done by drawing the channel to the Si/BOX interface and ensuring increased mobility. One method to achieve simultaneous biasing and sweeping of the top and bottom gates in UTBB FD-SOI devices is to improve both G_M and A_V.

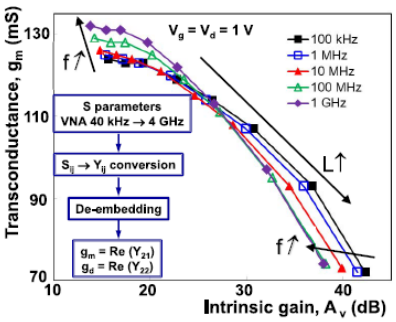


Figure 3.17. G_M- metric in FD-SOI MOSFETs extracted at various frequencies. [RF21]

As frequency increases, one may observe a decline in A_V and an improvement in G_M. The latter is the result of G_D dominating A_V due to a larger growth in G_D than G_M. Several non-stationary effects, including substrate coupling, self-heating, floating bodies, and others, manifest in distinct frequency ranges and cause frequency response dependency in G_M, G_D, and therefore A_V.

3.2.3 Non-stationary effect response

The output conductance of the MOSFET's frequency response can be seen as follows:

$$G_{DS}(f) = G_{DS,in} + \Delta G_{DS,FB}(f) + \Delta G_{DS,SH}(f) + \Delta G_{DS,SUB}(f) \tag{3.4}$$

The frequency response of G_{DS} is influenced by multiple factors. $G_{DS,in}$ is an intrinsic term associated with the DIBL and CLM that is constant with frequency in any MOSFET. The G_{DS} variation associated with the floating body effect is $\Delta G_{DS,FB}$. The SH effect is connected to $\Delta G_{DS,SH}$, whereas the frequency response of the coupling through the

substrate is related to $\Delta G_{DS,SUB}$. It is possible to add more effects. It is important to note that, depending on the device and its operating regime, ΔG_{DS} terms might have either a "positive" or "negative" sign.

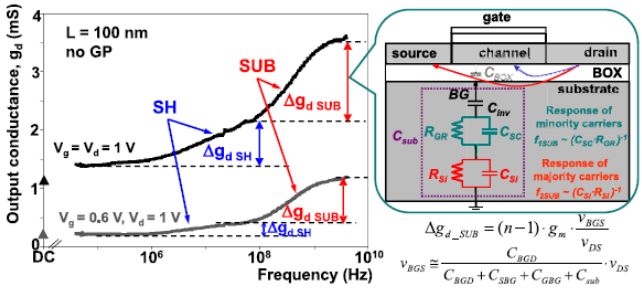


Figure 3.18. Variation of the G_{DS} vs frequency in UTBB SOI MOSFET. The schematic figure on the right introduces the frequency response of coupling through the substrate. [**trty11**]

Such thin-film FD devices allow for the first-order neglecting of floating-body effects. Nonetheless, the G_{DS} frequency response exhibits distinct transitions associated with both SH and SUB. The well-known frequency response of the SH effect is caused by the inability of lattice temperature and acoustic phonons to follow AC excitation at a specific frequency. The so-called "substrate effect," a less well-known frequency response of coupling through the substrate, is associated with the frequency variation of the C_{SUB}, whereby C_{SUB} decreases as frequency increases and minority carriers in the substrate stop following the AC signal first (in the tens-hundreds Hz range) and then majority carriers (in the GHz range). To the first order, this can be represented as two RC networks. A change in C_{SUB} causes a change in potential at the Si/BOX interface, which in turn causes a change in G_{DS}.

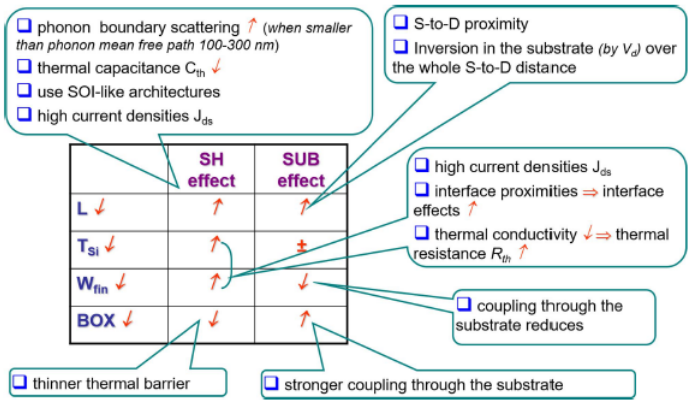


Figure 3.19. Overview of the evolution of SH and substrate effects in advanced devices. [RF21]

BOX thinning, Fin or NW width decrease, and Si film thickness on these effects. In sophisticated, deeply scaled devices, it is evident that both effects are greatly amplified. A trade-off between SH and SUB effects also exists since fin width reduction increases SH but decreases coupling through the substrate; as a result, one architectural approach may be preferred over another based on the application and bias conditions. Strong, 2-to 5-fold G_{DS} deterioration across a frequency range is a significant constraint for analog designers and applications. The transition associated with SUB was comparable in strength to that of SH, and in certain cases, it was even more so. This is because, while improving electrical connection across the substrate, BOX thinning facilitates heat evacuation towards the Si substrate.

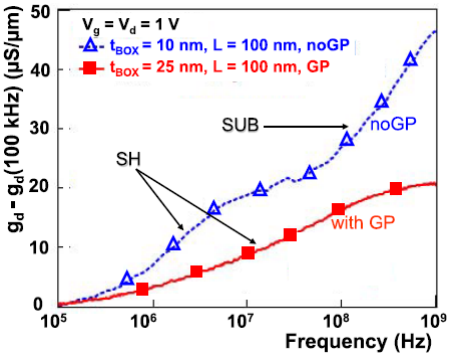


Figure 3.20. Output conductance as a function of frequency in FDSOI MOSFETs with and without the ground plane. [RF21]

It is evident that a significant reduction in the SUB-related variation of G_{DS} is possible with the introduction of a Ground Plane. With UTBB FD-SOI or SOI based FinFETs, at high bias voltage and current, power density and consequently Joule heating dissipated in the device, SH remains the primary cause of analog performance degradation in advanced devices. Beyond the usage of lower biases, alternative options such as device design modification, further oxide thinning, and the use of high thermal conductivity materials can be considered to lessen the SH effect. Additionally, it was recently shown that the usage of a sink included in the BEOL might improve SH features by 20–30%, providing greater flexibility for circuit designer optimization without requiring changes to technological processes.

3.2.4 Self Heating assesment

R_{TH} may be recovered given the following information: the amplitude of the SH-transition, $\Delta G_{DS,SH}$, low-frequency values of the G_{DS} value, and the temperature dependence of the drain current (dI_D/dT_A), where T_A is ambient temperature, acquired from complementary measurements.

$$R_{TH} = \frac{\Delta G_{DS,SH}}{(I_D + G_{LF}V_D)dI_D/dT_A} \tag{3.5}$$

Channel temperature rise can therefore be simply determined if Rth is known:

$$\Delta T = R_{TH} \cdot I_D \cdot V_D \tag{3.6}$$

The characteristic frequency $F_{TH}(= \frac{1}{2\pi \cdot R_{TH} \cdot C_{TH}}$ is inversely proportional to the volume-to-surface ratio and shifts towards higher frequencies in advanced device architectures. Thermal resistance is inversely proportional to the heat evacuation surface, whereas thermal capacitance Cth is proportional to the volume available to store the heat.

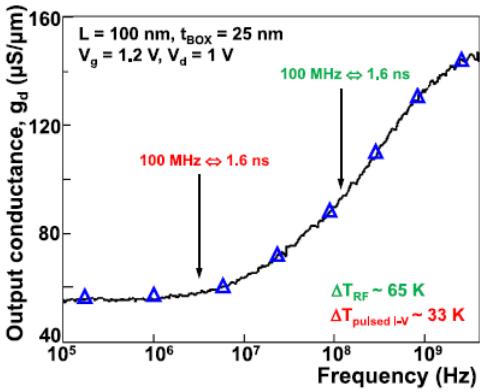


Figure 3.21. Output conductance as a function of frequency in UTBB FDSOI devices. Arrows indicate a frequency range at which RF and pulsed I-V techniques were applied for SH extraction. [RF21]

In advanced FD-SOI MOSFET, F_{TH} can reach hundreds of MHz range. An alternate pulsed I-V technique that is frequently employed for SH extraction is based on applying brief pulses to prevent device heat failures within this distinctive frequency range. To the best of the authors' knowledge, there is currently no technological solution that enables the pulse technique to be realized on a wafer with precisely controlled pulses in the 1 ns range. In sophisticated devices, the pulsed I-V method may significantly underestimate SH. Moreover, the underestimate or inconsistency would vary depending on the size, bias, and temperature conditions of the device under study. Since the characteristic SH frequency in bulk devices is lower (by about an order of magnitude) than in FD-SOI devices, benchmarking of bulk and SH features may be incorrect, even in relative values. Consequently, the pulse I-V technique can provide less underestimated values.

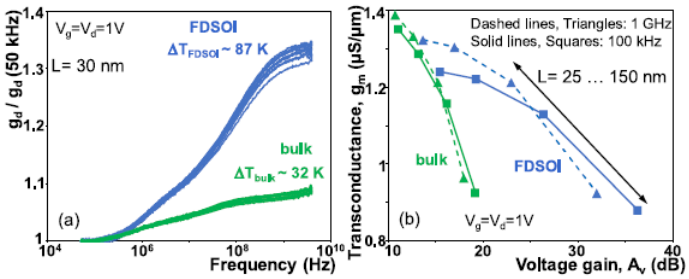


Figure 3.22. (a) Normalized output conductance as a function of frequency in FDSOI and bulk MOSFETs. L = 30 nm. (b) gm-Av metric in bulk and FDSOI MOSFETs extracted at low and high frequency. L = 25 to 150 nm. [RF21]

Throughout the whole frequency range, the FD-SOI devices outperform their bulk cousin while having stronger self-heating. Compared to high-frequency readings, FD-SOI devices offer a greater improvement when estimated from low-frequency values.

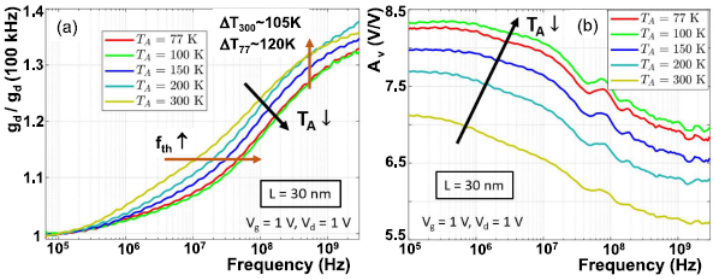


Figure 3.23. Normalized output conductance(a) and intrinsic gain (b) as a function of frequency in FDSOI MOSFETs at different temperatures. [RF21]

At cryogenic temperatures, the deterioration of analog FoM caused by SH is somewhat reduced. As the temperature drops, the thermal time constant decreases even more, making the wide-frequency technique—often referred to as the "RF technique" because it involves measurements up to the GHz range—for the extraction of SH characteristics even more pertinent. It is important to highlight that, at cryogenic temperatures, the channel temperature differs significantly from the ambient temperature, which is important for modelling. Higher-order thermal networks are required for more sophisticated and precise thermal representation and modelling.

3.2.5 Parameters extraction

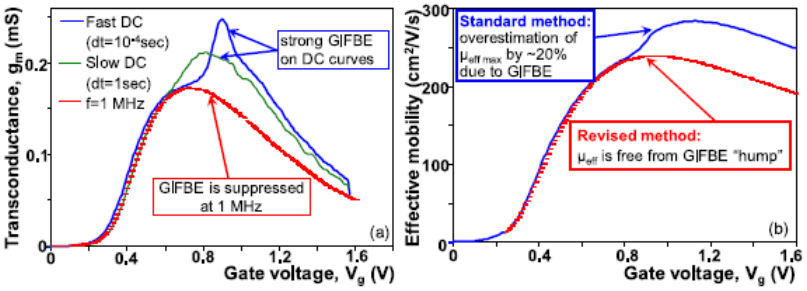


Figure 3.24. (a) gm-Vg curves of wide-fin FinFET measured at DC with short, 1 s (blue line) and long, 10 s, (green line) delay times and HF of 1 MHz (red dashes). L = 2 μm. Vd = 50 mV. (b) Effective mobility in this device was extracted using the standard and revised split C-V technique. [RF21]

The GIFBE effect has a distinctive frequency response with a cutoff frequency in the region of a few hundred kHz, according to wide-band frequency characterisation. In G_M retrieved from a 1 MHz S-parameters measurement, this effect is suppressed. Consequently, a modified split C-V technique was presented that uses capacitance measured at very high frequency and integrals of G_M (instead of DC I_D in a regular split C-V):

$$\mu = \frac{L^2}{V_D} \frac{\int_{V_G}^{V_0} G_M(V_G) dV_G + I_{D0}}{\int_{V_G}^{V_0} C_{GC}(V_G) dV_G} \tag{3.7}$$

3.2.6 RF characterization

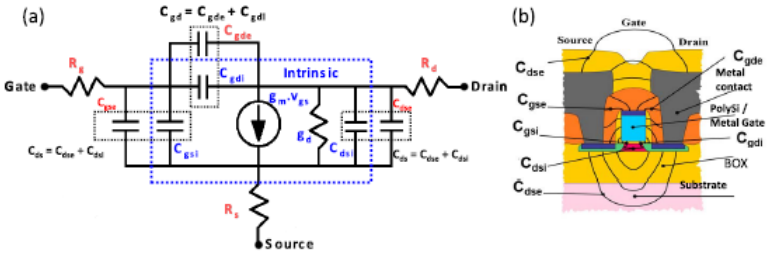


Figure 3.25. (a) MOSFET small-signal equivalent circuit including parasitic and intrinsic components; (b) schematic representation of different parasitic capacitive coupling components. [RF21]

The capacity to distinguish between "intrinsic" and "extrinsic" elements becomes essential in today's sophisticated technology because:

1. Predicting "intrinsically" feasible device/process values is made possible by it.

2. Knowing if the performance shortfall is due to "extrinsic parasitics" or "intrinsic device" is critical for process/architecture improvement. To extract an entire equivalent circuit that separates "intrinsic" and "extrinsic" components, S-parameters must be measured over a broad frequency range, up to 100 GHz. Therefore, the plan needs to incorporate suitable structures with RF access pads from the outset of the technological development.

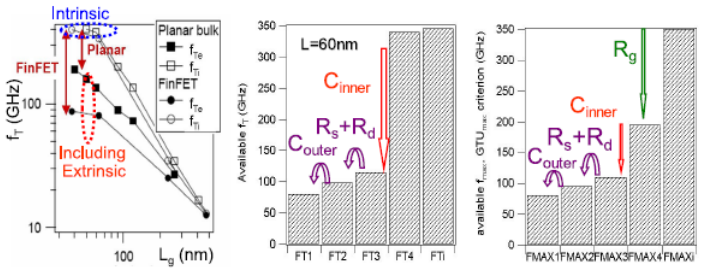


Figure 3.26. Variation of the cutoff frequency as a function of length in FinFET and planar counterparts along with analysis of the effect of different parasitic elements on the FinFET cut-off frequencies. [RF21]

First, when device length decreases, the discrepancy between "intrinsic" and "as measured" values grows, and this effect is amplified in FinFETs when compared to their bulk equivalent. Second, it's noteworthy to note that, while measurable values in FinFETs are far lower than in their planar counterparts, very similar "intrinsic" values are feasible in the case of both planar and FinFET devices. Apart from the impact of R_G on F_{MAX}, C_{INNER}—the total of fringing capacitances directly connected to the FinFET 3D architecture—is the primary cause of degradation, accounting for 30% of F_{MAX} and 60% of F_T concerning intrinsically achievable values. In these devices, the effects of the feed connection outside the active area (R_{SD} and C_{OUTER}) were comparatively minimal. It was demonstrated that the gate encircling the fin and the S/D sidewalls' 3D coupling accounted for the majority of C_{INNER}.

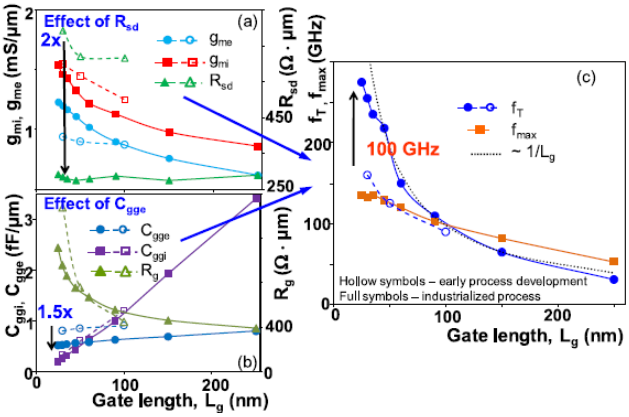


Figure 3.27. Gate length dependence of Rsd, gm, intrinsic gm (a), Rg, extrinsic and intrinsic Cgg (b) and F_T, F_{MAX} (c) in different "generations" of FDSOI MOSFETs. [RF21]

Despite having a nearly constant relationship with L, series resistance naturally has a greater effect on the G_M of shorter-L devices. The extrinsic parasitic capacitance, Cgg,e, remains relatively constant throughout a range of gate lengths, surpassing the intrinsic component, which increases in proportion to L and hence accounts for the majority of the total C_{GG}. Both the capacitive and resistive parasitic components improved as a result of process optimization: in the case of the more mature version, R_{SD} is roughly twice lower and Cgg,e is 1.5 times lower. When F_T is increased by 100 GHz, there is a significant improvement in RF performance due to the reduction of parasitics. As recently as the 30 nm long device, F_T values as high as 360 GHz.

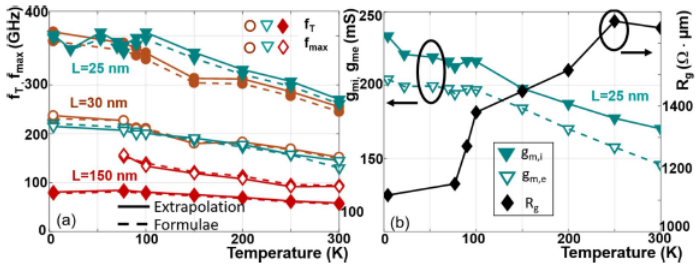


Figure 3.28. Temperature dependence of F_T, F_{MAX} (a) and Rg, intrinsic and extrinsic gm (b) in FDSOI MOSFETs. [RF21]

With temperature reduction, there is a noticeable improvement in Radio Frequency (RF) FoMs at 130 and 75 GHz for F_T and F_{MAX}, respectively, for a 25 nm-long FD-SOI device. The improvement was attributed primarily to mobility, which resulted in a 40% rise in intrinsic G_M and an additional 40

3.3 Nanowire, orientation and multi channel

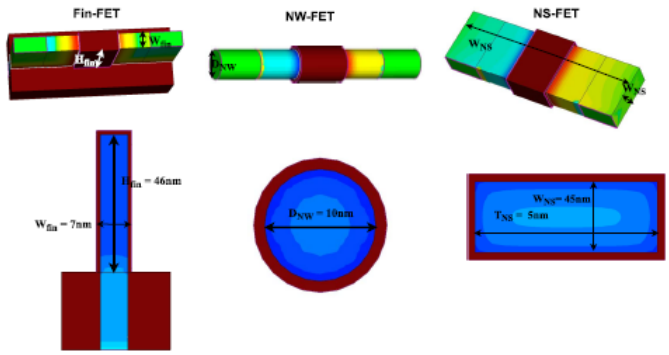


Fig. 1. Simulation geometries: cross-sectional view (top) and side view (bottom) of Fin-FET, NW-FET, and NS-FET at 5-nm technology node (18-nm channel length).

Figure 3.29. Simulation geometries: cross-sectional view (top) and side view(bottom) of FinFET, NWFET and NS-FET at 5 nm technology node (18 nm channel length). [RR22]

The final study we discuss compares fin FET, NS, and NW, with the first two having greater utility for analog and mixed-signal applications.

3.3.1 Results and discussion

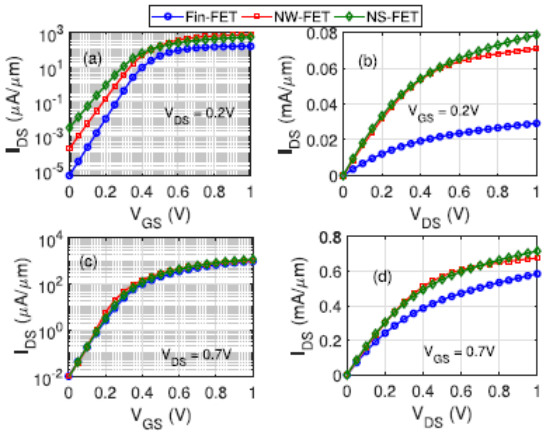


Figure 3.30. Device I–V characteristics of Fin-FET, NW-FET, and NS-FET at room temperature. Transfer characteristics (ID–V_{GS}) at (a) VDS = 0.2 V and (c)VDS = 0.7 V and output characteristics (ID–VDS) at (b)V_{GS} = 0.2 V and (d) V_{GS} = 0.7 V. [RR22]

By modifying the gate-metal work function difference, the three devices' transfer and output characteristics are achieved at a fixed I_{OFF} [I_{DS}(V_{GS} = 0 V and V_{DS} = 0.2/0.7 V)] of about 10 nA/μm for uniform performance benchmarking. Due to the significant inversion curve that is produced in the channel region by the surrounding gate on all sides, NS-FET and NW-FET offer greater driving currents than Fin-FET. For V_{GS} < 0.6 V, NW-FET shows a marginally larger drive current over NS-FET, whereas NS-FET shows a slightly higher drive current for V_{GS} > 0.6 V.

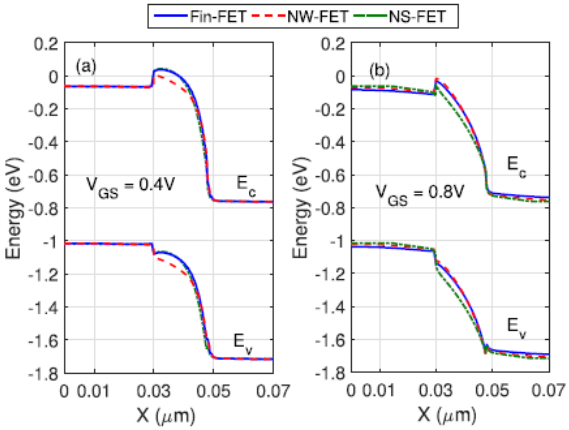


Figure 3.31. Energy band profile along the transport direction for Fin-FET, NW-FET, and NS-FET at distance 1 nm below the top oxide–semiconductor interface at V_{DS} = 0.7 V for (a) V_{GS} = 0.4 V and (b) V_{GS} = 0.8 V. [RR22]

It is observed that NW-FET increases the channel conduction band profile's gate modulation at low V_{GS}, which raises the thermionic current component's contribution. Higher gate modulation of the channel region band profile comes from a larger effective width that permits the whole V_{GS} to emerge throughout the nanosheet when V_{GS} rises over 0.6 V. As such, it causes a larger drive current at high V_{GS} for the NS-FET. It is observed that NS-FET and NW-FET have almost the same I_{DS} for all V_{DS} for V_{GS} = 0.2 V and V_{GS} = 0.7 V. Because of their lower DIBL values, the output characteristics of the NS-FET and NW-FET exhibit better saturation current than the Fin-FET. Drive current levels, therefore, imply that NS-FET and NW-FET may be more appropriate for mixed-signal and analog applications.

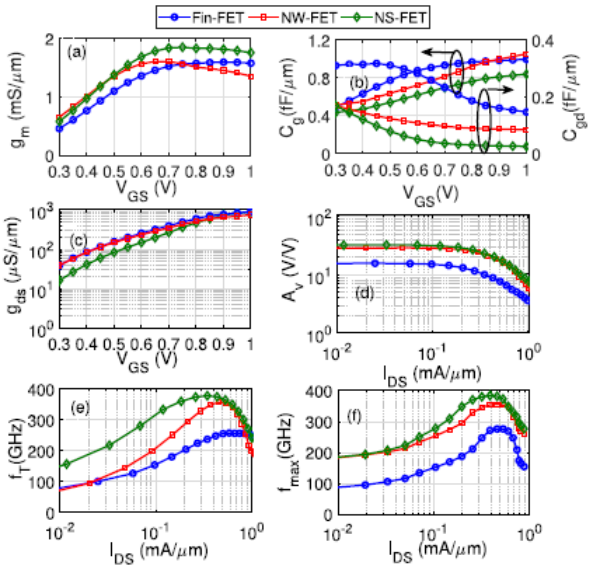


Figure 3.32. Analog/RF performance metrics of Fin-FET, NW-FET, and NS-FET atVDS = 0.7 V. (a) G_M, (b) C_G and C_{GD}, (c) G_{DS} as a function of V_{GS}, (d) vA_V = G_M/G_{DS}, (e) F_T and (f) F_{MAX} as a function of I_{DS}. [RR22]

It is noted that the transconductance G_M-V_{GS} characteristics of the three devices show a similar pattern. A peak in the G_M value occurs and drops further with increasing V_{GS}, while a linear increment in G_M is observed for low V_{GS}. The gate modulation of the channel potential is not perfect and deteriorates with rising V_{GS}, which accounts for the G_M decrements. For NS-FET, a maximum value of G_M of approximately 1.8 mS/μm is found, indicating high F_T and A_V. As V_{GS} rises, C_G rises quickly. It is discovered that for low V_{GS} values, C_{GD} drops and seems practically constant for high V_{GS} values. At high V_{GS}, Fin-FET has a greater G_M than NW-FET, but NW-FET has a higher C_G at high V_{GS}. Because the Fin-FET has a greater DIBL, which raises the G_M values, it has superior gate modulation of the channel conduction band profile than the NW-FET. The C_{GD} component in C_G is drastically increased by a greater drain charge contribution for Fin-FET. Because of their greater DIBL, Fin-FETs have higher output conductance G_{DS}, whereas NS-FETs have the lowest value of G_{DS}. The multigate device can improve performance in several ways, including by increasing the drive current, lowering C_G, and lowering G_{DS}. It does this by successfully suppressing the short-channel effects. The A_V of NS-FET and NW-FET is almost the same, but it is around 2× greater than that of Fin-FET. With the same device geometry, the NS-FET provides A_V of around 32 V/V, which is about 2.6× higher than that of planar double-gate MOSFET technology at 0.4 mA/μm I_{DS}. The multigate device architectures' improved G_M and G_{DS} values make them appear like a good option for high-gain amplifiers. It is discovered that the peak F_T of the NS-FET is approximately 1.5 x higher than that of the Fin-FET, at I_{DS} 0.4 mA/μm, or roughly 373 GHz. NS-FETs are a promising option for improving the RF performance limit at short channel length because their F_T value is about 1.6× greater at 0.4 mA/μm

I_{DS} for the same device geometry than planar double-gate MOSFET (229 GHz). The performance of multigate devices is not limited by external fringing parasitic capacitance, as indicated by a high value of F_T. The value of F_{MAX} in NS-FET is significantly higher than that of NW-FET and Fin-FET. Smaller G_{DS} and R_G values are shown by NS-FET, enabling a peak F_{MAX} of about 389 GHz. In analog/RF FoM, NS-FET performs better than Fin-FET and NW-FET, and at the 5 nm technology node, it seems to be a promising option for high-frequency applications.

3.3.2 Impact of L_G

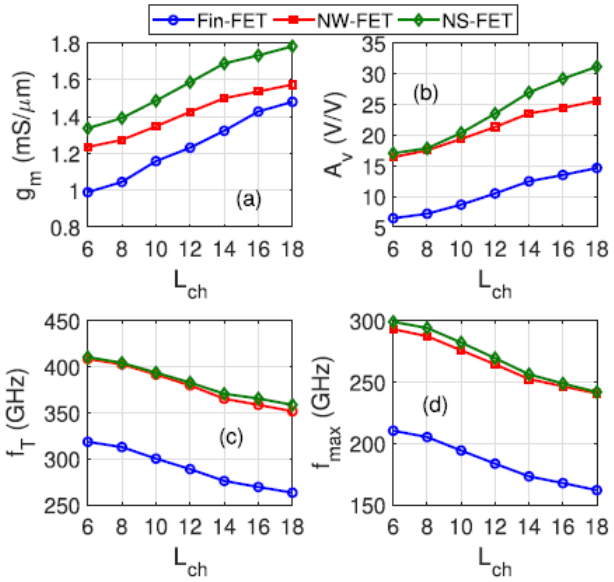


Figure 3.33. Impact of L_{CH} scaling on analog/RF performance of Fin-FET, NW-FET, and NS-FET at $V_{DS} = 0.7$ V and $V_{GS} = 0.7$ V. (a) G_M, (b) A_V, (c) F_T and (d) F_{MAX} as a function of L_{CH}. [RR22]

As the L_{CH} decreases, the G_M for the three devices also reduces significantly. This is because the source-to-channel tunnelling current at the OFF state has a significant impact on sub-14 nanometer devices. The device requires a significantly lower V_{GS} to achieve the OFF-state, and the drive current is enhanced for a fixed V_{DS} due to the increment in the source-to-channel tunnelling current. Reducing the L_{CH} results in a drop in the drive current and G_M. Crucially, when the L_{CH} is scaled down to 6 nm, NS-FET demonstrates a greater performance deterioration, but it still retains a significantly higher value of G_M. The tiny mean free path of electrons causes the mobility deterioration in the presence of more scattering events at short-L_{CH}, which results in a considerable reduction in the G_M value. For multigate devices, A_V significantly drops as L_{CH} drops. When the L_{CH} is scaled down from 18 nm to 6 nm, the A_V of NS-FET decreases from 32 V/V to 17

V/V due to a considerable reduction in G_M and G_{DS}. For $L_{CH} < 10$, it is found that NW-FET has almost the same gain as NS-FET. For amplification applications, the NS-FET and NW-FET have a A_V of around 17 V/V at 6-nm L_{CH}, making them preferable. Multigate devices can provide enough A_V even at the 6-nm L_{CH}, and in the final scaling limit, the NS-FET is superior to the Fin-FET and NW-FET. While G_M decreases, F_T of Fin-FET and NS-FET increases significantly as L_{CH} decreases. The reason for this is that there are discrete quantum states present, which cause C_G to decrease at very short L_{CH}s. Past 14 nm L_{CH}, F_T of NW-FET approaches NS-FET in almost exact proportion. Significantly less C_G over NS-FET is produced by a narrower effective width NW-FET. When L_{CH} scaled down to 6 nm, the F_T of NS-FET and NW-FET is found to be boosted by 1.14×, whereas Fin-FET demonstrates approximately 1.2× improvement. For 18–6 nm L_{CH}, NS-FET and NW-FET give roughly 1.2× greater F_T than Fin-FET. When L_{CH} decreases, F_{MAX} rises noticeably. This is because as L_{CH} decreases, F_T grows and R_G and G_{DS} drop. While NW-FET can also be preferred at very short L_{CH}s, NS-FET may be a more popular choice for high-gain and high-frequency RF circuits, according to A_V, F_T, and F_{MAX} values.

3.3.3 Impact of geometrical parameters

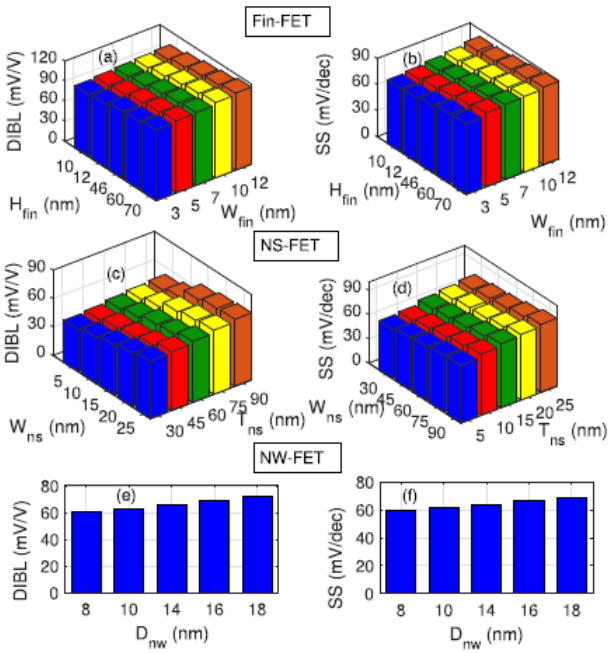


Figure 3.34. Impact of geometrical parameters on the short-channel peRFormance metrics of Fin-FET, NW-FET, and NS-FET at $V_{GS} = 0.7$ V and $V_{DS} = 0.7$ V for the fixed I_{OFF} of around 10 nA/μm. (a) DIBL and (b) SS as a function of fin width and H_{FIN}, (c) DIBL and (d) SS as a function of nanosheet width and thickness, and (e) DIBL and (f) SS as a function of nanowire diameter. [RR22]

As the H_{FIN} and width grow, the gate control over the channel region decreases, resulting in a rise in DIBL of the Fin-FET, whereas SS exhibits a marginal increment. Due to a considerable loss in gate controllability in the case of the NS-FET, DIBL grows dramatically with increasing channel width and thickness. When the NS-FET width and thickness are scaled, a marginal increment of SS is seen upward. As NW diameter increases, the SS and DIBL of NW-FET rise quickly. This is a result of the gate electrostatic control on the channel regions being weakened by a wider channel and amplifying the drain voltage's influence. Planar MOSFET has a higher minimum value of SS, which is determined to be around 72.5 mV/decade, 60.8 mV/decade, and 61 mV/decade for 3 nm W_{FIN} and 10 nm H_{FIN}, 8 nm D_{NW}, and 30 nm W_{NS} and 90 nm T_{NS}, respectively. The thermodynamic limit for MOSFET is extremely near to the SS of NW-FET due to the channel's cylindrical nature the short-channel effects are adequately suppressed. Larger sheet width and rectangular channel cross section have an impact on the switching performance of NS-FETs, necessitating much greater V_{GS} to accomplish the channel inversion. For the following values: 3 nm W_{FIN} and 10 nm H_{FIN}, 8 nm D_{NW}, 30 nm W_{NS} and 90 nm T_{NS}. The minimum DIBL is observed around 93.2 mV/V, 60.8 mV/V, and 45 mV/V. Compared to Fin-FET and NW-FET, NS-FET may be more resistant to changes in drain field effects if DIBL is smaller.

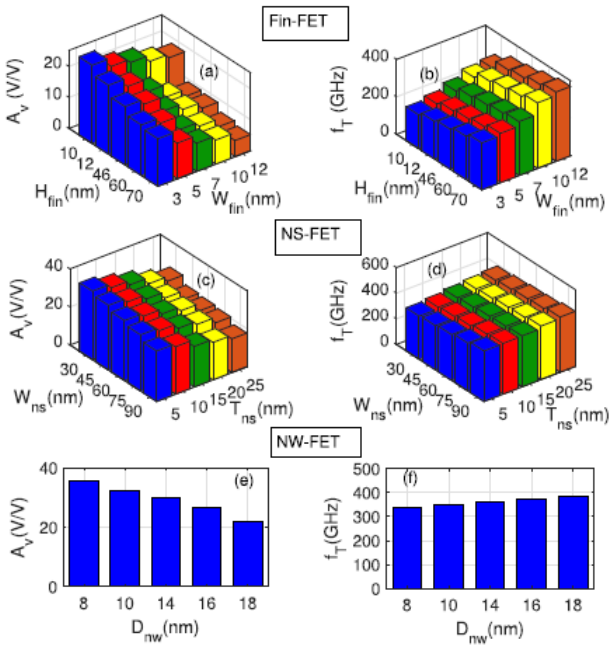


Figure 3.35. Impact of geometrical parameters on the analog/RF performance of Fin-FET,NW-FET, and NS-FET atVGS = 0.7 V andVDS = 0.7 V for the fixed OFF current of around 10 nA/μm. (a) A_V and (b) F_T as a function of fin width and fin height, (c) A_V and (d) F_T as a function of nanosheet width and thickness, and (e) A_V and (f) F_T as a function of nanowire diameter. [RR22]

When NS-FET and Fin-FET channel width and height/thickness are increased, F_T rises and A_V falls. The A_V of NS-FET decreases slightly with width, but a notable reduction is noted when sheet thickness increases. Higher G_M can be achieved with bigger NS width and thickness; however, G_{DS} increases significantly as sheet thickness grows. Greater fin height and width lower the Fin-FET's gate efficiency, which raises the G_{DS} values. It is discovered that raising the fin height and width results in an increase in G_M. A higher height causes the C_G values to drop significantly, which quickly raises F_T. A little fluctuation in C_G is observed with increasing fin width, leading to a slightly greater F_T. Due to simultaneous fluctuation in G_M and C_G, for NS-FET, a marginal increment in F_T is seen with width and thickness variation. As the nanowire diameter increases, G_M and G_{DS} increase and C_G decrease, resulting in a similar pattern in A_V and F_T of NW-FET. The highest F_T necessitates larger and thicker fin/sheet by increasing current drivability, but the best A_V can be obtained with thinner and narrower sheet/fin that improves gate controllability. Compared to the NW-FET and Fin-FET, the NS-FET provides higher A_V and F_T at about the same effective width. NW-FET provides superior A_V and F_T at the same effective width as Fin-FET. Under the same effective width, A_V and F_T of the NW-FET hA_Ve roughly 2× and 1.3×, respectively, over the Fin-FET. When the effective width is scaled from 23 nm to 152 nm, it is seen that the A_V of Fin-FET is lowered by 5×, whereas NS-FET demonstrates a marginal reduction in A_V with the factor of approximately 2× when the effective width is scaled from 70 nm to 230 nm. When scaling the effective width from 25.12 nm to 56.52 nm, NS-FET and Fin-FET show approximately 1.28× and 2.05× increment, respectively, for F_T, while NW-FET shows approximately 1.6× decrement and 1.1× increment for A_V and F_T, respectively. With geometrical parameter variation, the NS-FET has demonstrated more resilient analog/RF performance. Due to lower G_M, NW-FET exhibits greater A_V at the same DIBL as NS-FET, whereas NS-FET exhibits higher F_T due to lower C_G when compared to NW-FET. Due to significantly higher DIBL values at the chosen geometrical parameters, matching DIBL with NS-FET becomes difficult in the Fin-FET scenario. Compared to Fin-FET and NW-FET, NS-FET offers greater flexibility in optimizing geometrical parameters for improved short-channel and analog/RF performance.

3.3.4 Impact of surface orientation

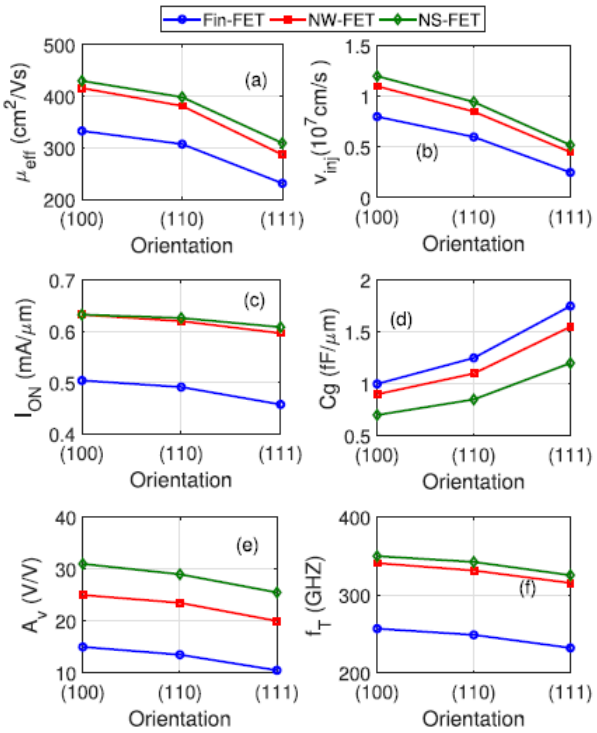


Figure 3.36. Impact of surface orientation on analog/RF performance of Fin-FET,NW-FET, and NS-FET at $V_{DS} = 0.7$ V and $V_{GS} = 0.7$ V. (a) μ_{EFF}), (b) V_{INJ}, (c) I_{ON}, (d) C_G, (e) A_V and (f) fT as a function of surface orientation. [RR22]

For n-type multigate devices, the highest μ_{EFF} is located along the (100) surface because of the lower effective electron mass and atom surface density. Because of the variance in electron masses at the different orientations, is dramatically varied in three devices with surface μ_{EFF} orientation. The μ of NS-FET and NW-FET is found to be almost equal, however, in all orientations, their mobility is around 1.29× higher than that of Fin-FET. The greater drain field in the channel region has a major impact on the Fin-FET. Higher V_{INJ} is also displayed by NS-FET with (100) surface orientation and the highest mobility, and vice versa. Around 15% and 25% more are present in NS-FETs with (100) orientation compared to NW-FETs and Fin-FETs with the same V_{INJ} surface orientation. Mobility and V_{INJ} are strongly influenced by the geometrical parameters, orientation, and bias. Because three devices are more resistant to short-channel effects, I_{ON} for each device exhibits marginal variatI_{ON} with surface orientation. Due to their almost equal μ_{EFF}, the NS-FET and NW-FET have approximately the same ON current; however, when compared to other orientations, the NS-FET with (100) orientation shows an advantage in C_G, A_V, and F_T. Because of the strong anisotropic characteristic, a bigger C_G is noticed in the (111) orientation compared to the (110) and (100) orientations. When

comparing NS-FET (100) orientation to NW-FET and Fin-FET with the same surface orientation, A_V is approximately 1.24× and 2.13× higher, respectively. Since G_{DS} values have significantly decreased, A_V of NS-FET exhibits approximately 1.14× and 1.29× degradation in (110) and (111) orientations, respectively. Because of the G_M reduction and C_G augmentation in (110) and (111) orientations, F_T does not exhibit a high reliance on orientation. Analog/RF applications, μ_{EFF}, A_V, and F_T are better suited for NS-FETs with (100) channel orientation than for those with (110) and (111) surface orientations.

3.3.5 Impact of multichannel stacks

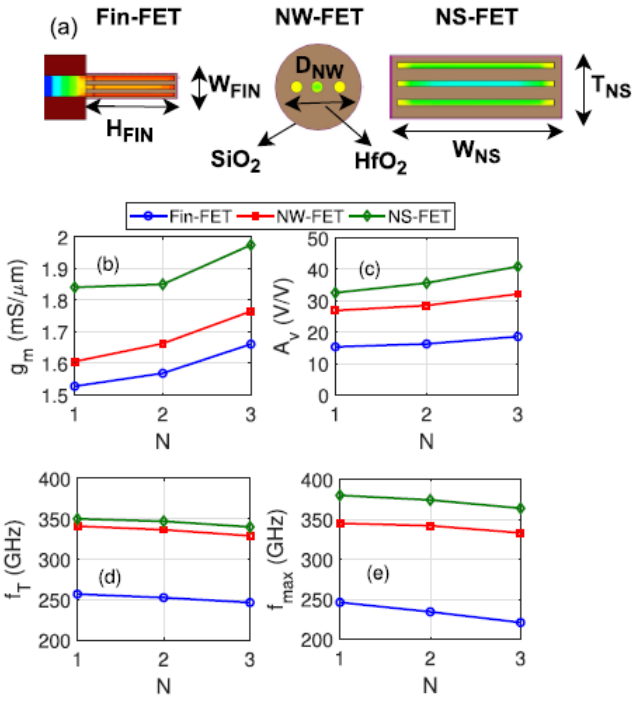


Figure 3.37. Analysis of multichannel structure on the analog/ RF performance of Fin-FET, NW-FET, and NS-FET at V_{DS} = 0.7 V and V_{GS} = 0.7 V. (a) Side schematic of the three-channel device structures of Fin-FET, NW-FET, and NS-FET, (b) G_M, (c) A_V, (d) F_T and (e) F_{MAX} as a function of number of channels (N). [RR22]

For uniform benchmarking, we increase the number of stacked channels and fins while maintaining the same area footprint. It is thought that the fin pitch and T_{SUS} are fixed at 34 and 10 nm, respectively. Because there are more electron-conducting routes when there are more channels, the G_M of multigate devices increases. Because the same width channels increase with the number of channel stacks, G_M of the NS-FET exhibits a notable improvement. When the number of channels increases, the effective channel area decreases, resulting in a marginal increment for NW-FET. For multigate devices, A_V rises

as the number of channels does. While A_V of NS-FET and Fin-FET shows 1.25× and 1.21× improvement with single to three channels increment, G_M of NS-FET and Fin-FET are boosted by 1.1× and 1.08×, respectively. The narrower sheet and W_{FIN} cause reduced drain field penetration in the channel region, which lowers the G_{DS} values, which accounts for the significant gain increment. As channel stacks increase, multigate devices' F_T decreases despite an increase in G_M. The contribution of coupling and parasitic capacitance in the C_G values is significantly increased by multichannel stacking. Due to an increase in R_G and G_{DS}, F_{MAX} for these multigate devices deteriorates as the number of channels increases. Multichannel stacks can increase G_M and A_V; however, maximizing the number of channels stacked is not the best option for improving RF performance.

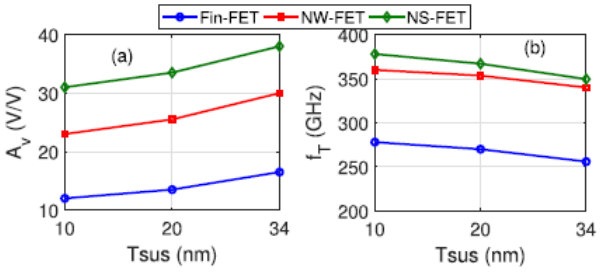


Figure 3.38. (a) Voltage gain (A_V) and (b) cutoff frequency (F_T) for three channels Fin-FET, NW-FET, and NS-FET as a function of suspension thickness (T_{SUS}) at V_{DS} = 0.7 V and V_{GS} = 0.7 V. [RR22]

As T_{SUS} grows, the channel narrows, limiting carrier scattering and raising G_M. As a result, A_V increases. Because there is less of a drain field effect in the narrower channel region, the G_{DS} likewise drops. Despite an increase in G_M, F_T somewhat lowers when T_{SUS} rises because of an increase in C_G values. A_V can be improved by optimizing T_{SUS}, however F_T demonstrates minor decline with increasing T_{SUS}.

Chapter 4

Insights

4.1 Which are the differences?

Now let's examine the key distinctions between digital and analog FinFETs.

4.1.1 Materials

Materials-wise, narrowband dielectrics like HfO_2 and gate metals like tungsten or iridium are frequently used in analog FinFETs. Conversely, highly conductive gate metals and thinner dielectrics like SiO_2 or Al_2O_3 are preferred by digital FinFETs.

4.1.2 Fabrication processes

The fabrication methods for analog FinFETs are typically more intricate, involving the utilisation of dual gates, dual dielectrics, and optimisation of channel size. They also call for more accurate stress engineering and doping management.

4.1.3 Dimensions and geometries

Increasing the channel size of analog FinFETs can achieve greater linearity and reduced distortion. The fin's height and width are maximised, with linearity being the primary consideration. Digital FinFETs have shorter gate lengths and smaller fins to reduce channel diameters. Fins and multi-fin constructions typically have a larger aspect ratio emphasising efficiency and speed.

4.1.4 Design considerations

The goals of analog FinFETs are to minimise noise, maximise linearity, and guarantee stable functioning in different scenarios.RF circuits, amplifiers, and other high-performance analog components are commonly employed with these devices. The three primary factors

for digital FinFETs are integration density, energy efficiency, and switching speed. Advanced doping tactics and multi-patterning lithography techniques are employed. They are extensively utilised in various digital logic circuits, memory, and processors.

4.1.5 Examples

This 2020 paper [YB20] provides design guidelines for FinFET and Nanosheet FET at the 5nm technology node, with analog and RF applications. A three-dimensional schematic diagram of the device is presented, highlighting key geometric parameters such as H_{FIN} and L_G, derived from TEM images. Doping of the S/D ($2 \times 10^{20} cm^{-3}$) and PTS ($2 \times 10^{18} cm^{-3}$) regions is specified, with a contact resistivity at the epi/silicide interface of $1 \times 10^{-9} \Omega \cdot cm^2$. These details are crucial for optimising performance in advanced applications.

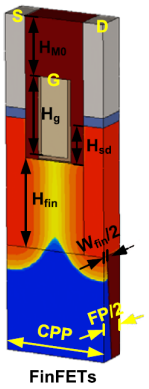


Figure 4.1. 3-D schematic diagrams of bulk FinFETs and NS-FETs. Geometrical parameters and materials are specified. [YB20]

- Geometrical parameters and materials are specified in the next frame table.
- **Hsd**, **Hg**, and $\mathbf{H}_{M0}$ are referred from several TEM images.
- S/D doping $\mathbf{2\ x\ 10^{20}} cm^{-3}$
- **PTS** doping $\mathbf{2\ x\ 10^{18}} cm^{-3}$.
- Contact resistivity at S/D epi/silicide interface = $\mathbf{1\ x\ 10^{-9}} \Omega \cdot cm^2$.

The W_{FIN} has been varied between 5 and 9 nm, while the H_{FIN} is between 38 and 54 nm. The study also includes doping data: S/D at $2 \times 10^{20} cm^{-3}$, PTS at $2 \times 10^{18} cm^{-3}$, and a contact resistivity at the S/D epi/silicide interface of $1 \times 10^{-9} \Omega \cdot cm^2$.

Geometrical parameters		Values(nm)
CPP	Contacted poly pitch	54
FP	Fin pitch	34
Lg	Gate length	18
Lsp	Spacer length	7
Hg	Gate height	40
H_{M0}	M0 height	30
Hsd	S/D height	20
Wfin	Fin width	5,6,7,8,9
Hfin	Fin height	38,42,46,50,54

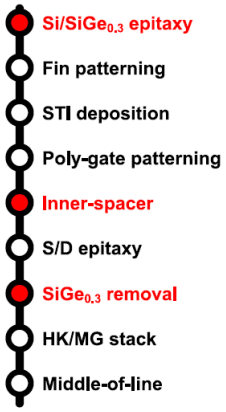


Figure 4.2. Process flows. [LB18]

A 2021 study [RF21] of FD-SOI transistors reported the following key parameters. The study also includes a TEM image that clearly shows the device structure, highlighting a narrow 25 nm SOI finger surrounded by the PVD-TiN gate stack.

- 001 **SOI** substrates **145nm BOX**.
- Minimum **Lg and Wg** by **e-beam lithography = 25nm**.
- After the active area patterning and etching **MESA isolation**
- **3nm ALD HfO2** (post-**annealed at 600°C during 15min**) + **10nm TiN** + **50nm n+** doped poly-silicon layers.
- Either a **PVD TiN (100°C, 6kWatt) or a CVD TiN (680°C with NH3 and TiCl4 as precursors)**.
- **10nm thick oxygen-free nitride spacer** prior to the **etching of HfO_2**.
- **2-steps selective epitaxy**
- **NiSi** has then been used, followed by a **standard BEOL process**.

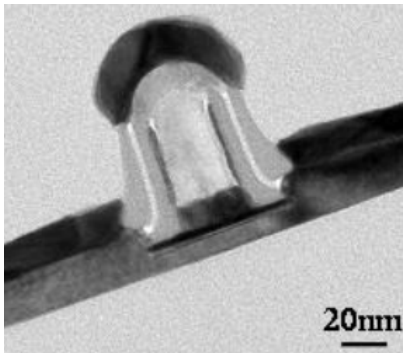


Figure 4.3. TEM cross-section of a 25nm FDSOI transistor. The film thickness is 8nm. A gate stack is 3nm HfO2 + 10nm PVD TiN + 50nm poly-Si. [MD]

The paper discusses a detailed methodology for the electrical characterisation of advanced MOSFETs for analog and RF applications. The figure shows a TEM section of a 25nm FD-SOI transistor, highlighting the gate stack.

- 100 **SOI** wafers with **TBOX** of **145 nm (UTB)** or **11.5 nm (UTBB)**.
- n-channel MOSFETs with silicon body **TSi = 11 nm, Lg = 25 nm, W = 25** μ**m**, and elevated source and drain.
- Channel **undoped** with p-type impurities **NA =** $\mathbf{10^{15}}cm^{-3}$.
- metal gate stack **TiN/HfO$_2$** with a **1.75 nm Tox**.
- About a **10-nm-thick oxygen-free nitride spacer** prior to the **etching of HfO2**.
- The substrates are p-type doped with **NA of 6.5 x** $\mathbf{10^{14}}cm^{-3}$ **(20** $\Omega \cdot$ **cm resistivity) or** $\mathbf{10^{18}}cm^{-3}$.

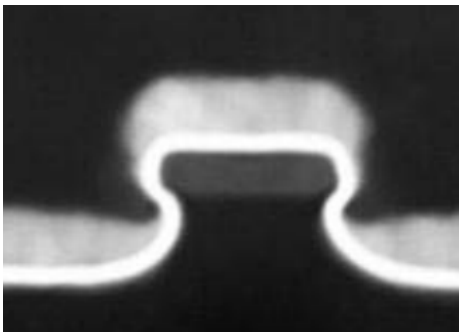


Figure 4.4. TEM performed on a 25nm narrow SOI finger with the surrounding PVD-TiN gate stack. [MD]

A 2022 study [RR22] analysed FinFETs, NW-FETs, and NS-FETs with channel lengths ranging from 18 to 1 nm. These parameters show the trend towards increasingly miniaturised devices, with precise control of fin sizes and gate oxide thickness.

- Device dimensions for 18–12 nm Lch from **IRDS 2020 projection**, **5–1 nm technology node**.
- **Lch below 12 nm** is scaled down from **low-power International Technology Roadmap for Semiconductors roadmap 2013 requirements** as IRDS specifications are limited to 1 nm technology node.
- **Wfin** and **Hfin** for Fin-FET are taken to be around **7 nm** and **46 nm**.
- **Weff** $\sim$ **99 nm (Weff**$_{fin}$ **= 2Hfin + Wfin)**.
- Stack of **0.6 nm SiO$_2$** and **1.7 nm HfO$_2$** used as gate oxide.
- **EOT = 0.9 nm**.
- The S and D regions of $\mathbf{L_{S/D}}$ **=10 nm** doped n-type with $\mathbf{N_{S/D}}$ **= 1 x** $\mathbf{10^{20}}cm^{-3}$.

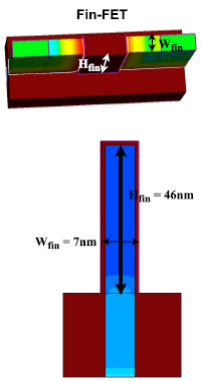


Figure 4.5. Simulation geometries: cross-sectional view (top) and side view(bottom) of Fin-FET, NW-FET, and NS-FET at a 5-nm technology node (18-nm channel length). [RR22]

Recent work from 2023 [Try] looked at U-shaped FinFET for sub-5nm technology nodes. The data highlight the further miniaturisation of FinFET devices, focusing on U-geometry that could offer performance and electrostatic control benefits for advanced technology nodes.

Specification	Values
Gate length (Lg)	12 nm
S/D length	10 nm
Height of the fin (Hfin)	50 nm
Thickness of the fin (Tfin)	5 nm
Contact resistivity	7 $\Omega \cdot \mu m^2$
Effective Oxide Thickness (EOT)	0.7 nm
Temperature	300°K
SiO_2 thickness	0.5 nm
Doping concentration	1 x $10^{18} cm^{-3}$
High-k gate dielectric (k) = HfO_2	22
Work function	4.8 eV
Spacer material (k) = SiO_2	3.9

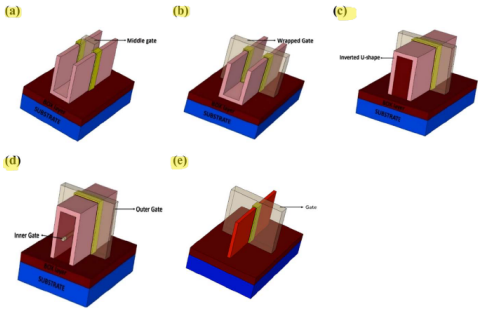


Figure 4.6. Structural variations of Junctionless FinFET (a) JL-MG-U-FinFET (b) JL-U-FinFET (c) JL-Inv-U-FinFET (d) JL-Inv-U-FinFET (e) JL-FinFET. [Try]

The diagram illustrates the fabrication process of U-shaped FinFETs, with various steps such as deposition of the BOX, removal of the substrate, isotropic etching of silicon to form fins, and formation of the gate dielectric and metal gate. This process is crucial for the development of advanced technologies in semiconductors.

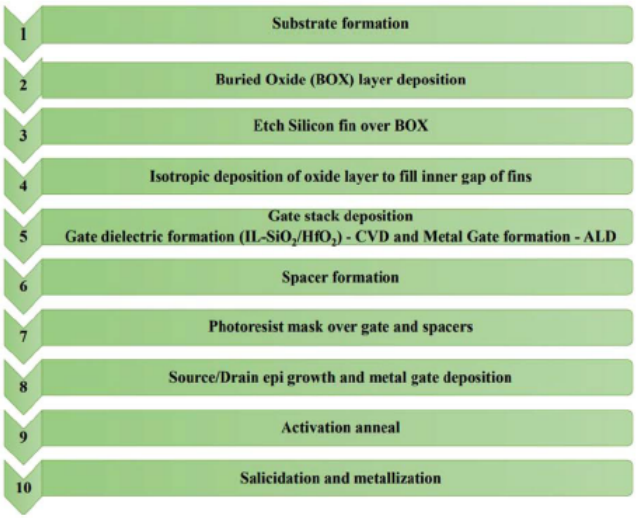


Figure 4.7. Fabrication flow of (c) and (d). [Try]

4.2 How to build an analog circuit?

Let's now examine how to use FinFETs to create analog circuits.

4.2.1 Perfomance

We compare the performance of analog and digital FinFET-based circuits. FinFET analog circuits provide better electrostatic control, which results in a higher inherent gain and improved linearity. For applications that demand accuracy and stability, this is essential. However, faster switching speeds and increased energy efficiency, two main characteristics for lowering power consumption in low-power devices are optimised into digital FinFET circuits. The device geometry must be optimised to use these FinFETs' characteristics.

4.2.2 Design considerations

There are several important considerations when creating FinFET circuits for digital or analog applications. Proper polarisation is necessary for analog circuits to minimise unpredictability and misalignment and to assure stability and energy efficiency through precise designing techniques, such as common centroid layout. Digital design guidelines for fin spacing and insulation must be followed while utilising three-dimensional methodologies to optimise efficiency and proper alignment.

4.2.3 Layout techniques

The correct operation of FinFET circuits depends on layout strategies. Accurate component matching is essential in analog circuits, necessitating the application of sophisticated methods like interdigitated or shared centroid designs. Managing parasitic capacitances and resistances is also needed, as is positioning the devices optimally to reduce unwanted effects. Reducing variability is a top priority in digital circuits, and two ways to do this are by statistically analysing variances in device parameters and using double lithographic patterning.

4.2.4 Extras

When designing FinFET analog circuits, high-frequency performance is fundamental, particularly for radio frequency applications. These devices have reduced C_G and improved G_M, which makes them perfect for high-speed applications. Using precise RF models that account for parasitic effects and high-frequency behaviour is crucial. With upgrades in SPICE models and verification tools to support simulations of phenomena like leakage and loss of gate control, EDA tools are essential in digital circuit design.

4.2.5 Examples

In advanced FinFET technology, we face limitations on the maximum gate length. To solve this problem, stacked gate designs are popular for mismatch-sensitive circuits such

as bandgaps. In this example, we replaced one long-channel device with 24 stacked short-channel devices operating at 1.8V. We require an equivalent gate length of more than 20 μm for low-current, high-precision applications. This requires exceptional process uniformity to ensure that numerous transistors operate as a single stacked gate device. The graph shows how the current mirror mismatch improves as the device's stages increase, highlighting the importance of this approach in modern analog design.

- In **advance FinFET technology**, **max Lg** will be **limited**.
- **Stacked-gate** is one of **most popular solutions** used in **mismatch-sensitive circuits**, such as **bandgap circuit**.
- In this **bandgap design**, the **long-channel device** for **current mirroring** is **replaced** by a **stacked of 24 short-channel devices operating at 1.8V**.
- For **very low current** and **high accuracy applications**, it demands the **equivalent Lg** must be **larger than 20μm**.
- This requires **high process uniformity** for a large number of transistors to work as a **single stacked-gate device**.

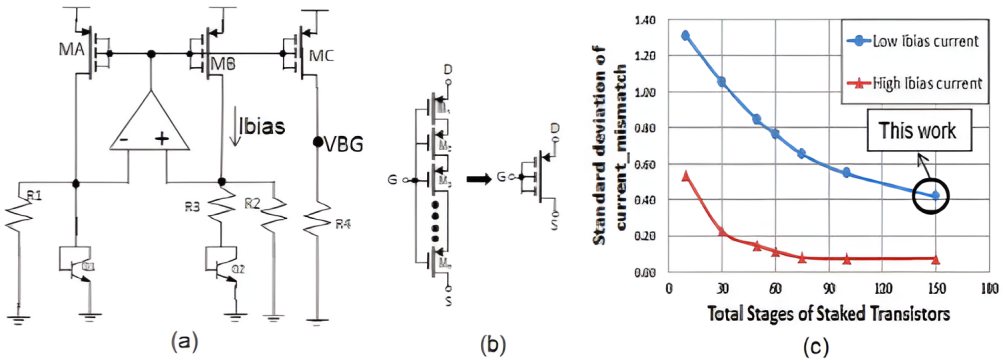


Figure 4.8. (a) Bandgap circuit, (b) stacked-gate devices representing MA, MB, and MC; (c) Current-mirror mismatch vs device stages. [Che16]

This imae illustrates the layout diagram of the bandgap circuit. Each current mirror device – MA, MB, and MC – is constructed using 150 stacked gate devices. Our simulation results, shown in the graph, reveal the relationship between the current mismatch and the total number of stacked transistors. We kept the total transistor size (W $\times$ L) constant and tested under two bias current conditions. For low-current applications, we have found that using multiple stages – up to 150 transistors – in the stack is crucial to achieving low current mismatch. This approach allows us to overcome gate length limitations while maintaining high performance in sensitive analog circuits.

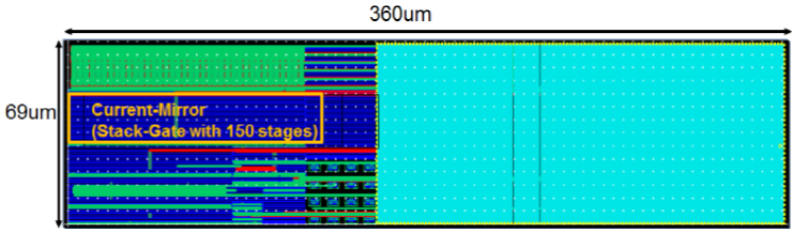


Figure 4.9. Bandgap circuit layout diagram. [Che16]

- Each of MA, MB, and MC **current-mirroring device** is constructed by **150-stacked-gate devices**.

- The simulation describing the relationship of **current mismatch** and total number of the stacked transistors assumed that **total transistor size** is kept at **same (W*L)**, at **two bias current conditions**.

- For **low-current application**, the **stacked-gate** needs more stages of transistors **up to 150** for achieving **low current mismatch**.

Layout design in FinFET-based analog circuits presents significant challenges, especially due to the uniformity of gate density. Stacked devices and interleaved transistors can be used to mitigate the negative effects of process change. However, for high-speed circuits, this can increase the load due to the complexity of metal routing. Creating a highly compact layout is therefore desirable to minimise resistances and parasitic capacitances while ensuring good alignment between the device model and the silicon.

- **Gate density uniformity** is challenging to **analog circuit layout** in **FinFET technology**.
- Using **stacked-gate**, **interleaving transistors** and **adding insensitive transistors to outer ring** of a **MOSFET array** are **possible approaches** to **overcome process penalty** in a **bandgap circuit**.
- For **high speed circuits** such kind of approaches will **increase loading** due to **complex metal routing**.
- **Highly compact layout** is desired to **minimise routing parasitic R and C**.
- Devices with **surrounding dummy pattern** and **guardring** can achieve **good device model** to **silicon correlation**.
- By adding **uniform surrounding patterns** to the **target MOSFET array**, the **device mismatch** due to **DGE can be cancelled**.
- This **layout scheme** can be applied to a group of **mismatch sensitive high speed circuits**.

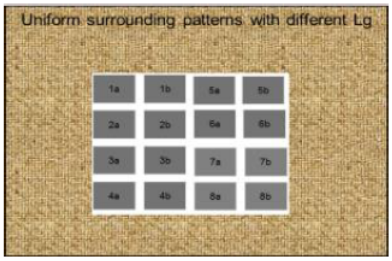


Figure 4.10. MOSFET array with 8 matching pairs (na & nb) which n = 1-8 and is surrounded by uniform patterns. [Che16]

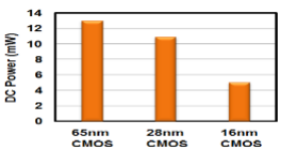
The measured performance of 5.8GHz LNA and 10GHz VCO circuits is presented, where a significant reduction in DC power of 62% and 45% respectively is observed, compared to designs made in 65 nm technology. These results highlight how 16nm FinFET technology allows for improved power efficiency without compromising high-frequency performance, making these devices ideal for modern, low-power RF applications.

	65nm CMOS	28nm CMOS	16nm CMOS
Frequency (GHz)	5.8		
V_{DD} (V)	1.2	1.05	0.8
P_{dc} (mW)	13.0 (x1)	10.9 (x0.84)	5.0 (x0.38)
Gain (dB)	16.6	17.2	17.2
NF (dB)	2.4	2.7	2.7

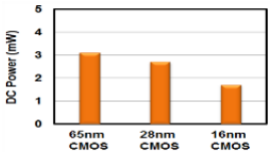
(a)

	65nm CMOS	28nm CMOS	16nm CMOS
Frequency (GHz)	10		
V_{DD} (V)	1.2	1.05	0.8
P_{dc} (mW)	3.1 (x1)	2.7 (x0.87)	1.7 (x0.55)
Phase Noise @ 1MHz (dBc/Hz)	-104.8	-104.0	-104.6

(b)



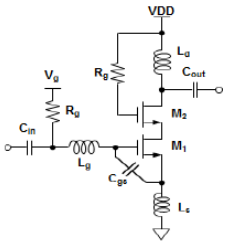
(c)



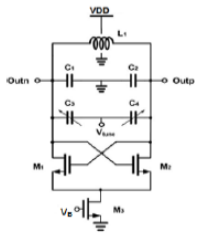
(d)

Figure 4.11. Measured circuit performance of (a) 5.8GHz LNA; (b) 10GHz VCO; and DC power driven technology trend of (c) LNA; (d) VCO from 65nm to 16nm technologies. [Che16]

- It is observed that, for **5.8GHz LNA** and **10GHz VCO** in **16nm FinFET technology**, the **DC power reduction** of **62%** and **45%** are obtained, respectively, in comparison with design in **65nm technology**.



(a)



(b)

Figure 4.12. Circuit schematic of (a) 5.8GHz LNA and (b) 10GHz VCO. [Che16]

The use of the NTV design technique, which has been successfully applied to several mixed analog-RF circuits, including LNAs and VCO operating at 2.4 GHz, is discussed. By using NTV, a significant reduction in DC power of 53% and 60% respectively was achieved for these circuits, compared to designs using higher voltages. This approach reduces power consumption and improves the device's reliability and longevity, making them ideal for low-power, high-efficiency applications.

- To achieve **more power efficiency**, the **near-threshold voltage (NTV) design technique** can be adopted.
- Actually, the **NTV** has been applied to numerous **mixed-signal** and **RF circuits**.
- A **2.4GHz LNA** and a **2.4GHz VCO** are implemented in **16nm CMOS** using **NTV design techniques**.
- It is found that, for **2.4GHz LNA** and **2.4GHz VCO** with **NTV design**, the **DC power savings** of **53%** and **60%**, respectively, are obtained.

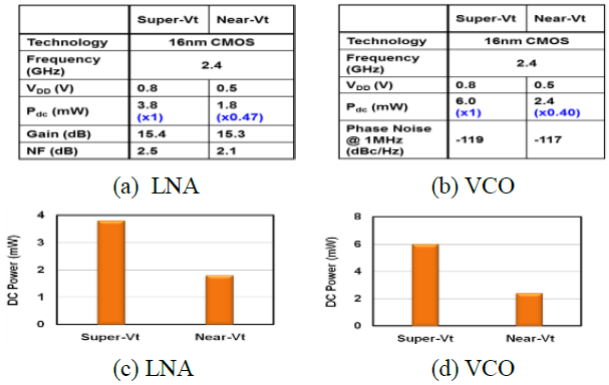


Figure 4.13. Measured circuit performance of (a) 2.4GHz LNA and (b) 2.4GHz VCO in 16nm CMOS; DC power reduction from super-Vt to near-Vt based on (c) LNA and (d) VCO. [Che16]

Figure (a) shows a graph with two waveforms representing the input and output voltages over time. Figure (b) shows various electronic components connected in a circuit configuration for transient analysis.

- A **single stage CS amplifier** is designed using **Sentaurus TCAD** and subjected to **transient analysis**.
- To analyse the **CS amplifier**, the **input voltage (Vin)** with an **amplitude of 10 mV** and a **frequency of 10 kHz**, and a **Vbias = 0.65 V**, **Vdd = 0.7 V**, **R1 = 100 Ω**, **Rd = 162 kΩ**, **CC = 3 μF**, and **RL = 1MΩ** are **fixed**.
- It is observed that the **output waveform** exhibits an **amplitude of 52 mV** and an **overall voltage gain (AV) of 5.2 V/V**.

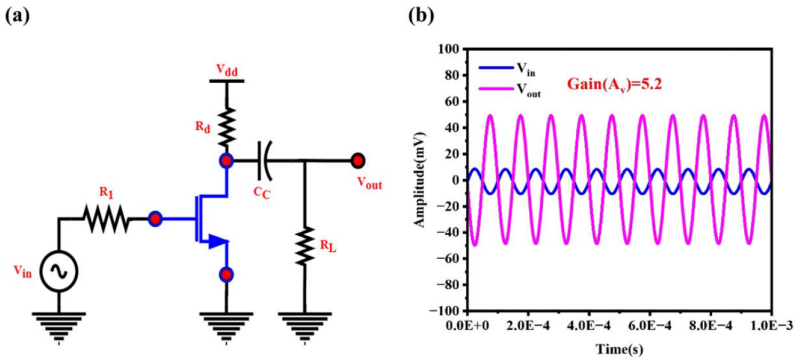


Figure 4.14. Single stage CS amplifier (a) Circuit diagram (b) Transient analysis. [Try]

4.3 How to simulate?

Let's now discuss the simulation methodologies used to study these devices. For this chapter, I also cite old papers to give the lectors an idea of the different modelling considerations due to scaling. In the paper [KA07] it is possible to read the following specifically:

- **Undoped FinFETs** simulated by **3-D simulator ATLAS**.
- **Lombardi mobility model**, which accounts for **surface roughness scattering**, **acoustic phonon scattering** and **optical intervalley scattering**.
- **Quantum effects** will not be significant in this paper as **undoped FinFETs**, with **Hfin and Tfin > 10 nm**, are **optimized** for operation in the **WI region**.
- The **source/drain profile** was modeled using the expression **NSD(x) = (NSD(x))peak exp(-x^2/σ^2)**, where **(NSD)peak** is the **peak source/drain doping**.
- σ **(lateral straggle)** defines the **roll-off** of the **source/drain profile** as $\sigma = \sqrt{2sd/ln(10)}$, where **s** is the **spacer width** and **d** is the **source/drain doping gradient**, evaluated at the **gate edge (d = 1/|dNSD(x)/dx|)** was **varied from 3 to 9 nm/decade**.
- The **lateral straggle parameter** σ was **varied from 5 to 15 nm** and the **spacer widths** corresponding to these values of σ lie in the **range of 3–90 nm**.

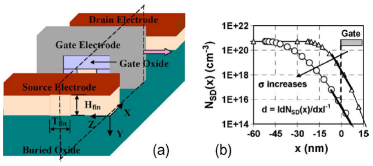


Figure 4.15. (a) Schematic diagram of a FinFET analysed in this paper, and (b) Variation of source doping profile for various σ values along the cut-plane along the channel as indicated by dashed lines. Please note that only half of the device structure is shown in (b). Notations: Δ-Δ-Δ σ = 10 nm, and °-°-° σ = 15 nm with d = 5 nm/dec. [KA07]

In [SS15] it involves the dependences between mobility, field and carrier concentration.

- **Technology parameters** and **supply voltages** used according to **analog ITRS roadmap** for **below 50 nm lg devices**.
- **VDD = 0.7 V**.
- **Work functions** of the **metal gates** are adjusted to achieve the **desired Vth value**.
- **Numerical simulation** uses the **drift-diffusion approach** and **field dependent mobility**, **concentration dependent mobility** and **velocity saturation model**.
- **Suitable empirical parameter** β is selected to calibrate the **drift diffusion transport model**.
- The **inversion layer mobility models Lombardi CVT** with **SRH** and **Auger recombination models** are included.

- The **silicon bandgap narrowing model** to determines the **intrinsic carrier concentration**.
- A set of partial differential equations solves the **discrete mesh** in an **iterative fashion**.
- The **currents**, **voltages** and **charges** for each electrode are calculated after each step of **bias ramp** through **quasi-stationary**.
- The **Poisson equation**, **continuity equations**, and the **different thermal and energy equations** are included in the simulation.
- All the **junctions** assumed as **abrupt**, **biasing conditions** are reckoned at **room temperature** and generation of **smooth mesh** is done in the simulation.
- The results of FinFETs at **low (50 mV)** and **high (0.35 V) drain biases** are analyzed further.

[RT17] includes doping and velocity saturation. The devices dimension make necessary the introduction of quantum effects.

- To consider the **mobility degradation** due to **high surface scattering** at semiconductor to insulator interface, **Lombardi mobility model** is used.
- It includes **scattering phenomenon like phonon scattering and column scattering**.
- **Mobility model** to account for **doping and velocity saturation dependency**.
- To include the **high doping concentration** in the device **Band-gap Narrowing model**.
- High doping concentration reduces the mobility of the carrier.
- So, **doping dependence mobility model** have been included in the mobility model.
- To generate results at nano-meter regime, **quantum effects** have been included.
- **Quantum drift-diffusion model** is used for accuracy of result and **Fermi- Dirac transport model** is also used in the simulation.
- We have activated **SRH generation and recombination model** to evaluate the leakage current.
- For minority carrier recombination **Auger recombination model** is used.
- The **current**, **charge** and **voltage** at every electrode can be measured at steps of **bias ramp** through **quasi-stationary simulation**.
- **Numerical technique Newton** is enabled to get the solution.

- **Temperature** during the simulation is **300K**.
- To validate our simulation , **compared the result with previous literature data**.

Quantum effects are not necessary due to the absence of junctions in [Sar18]:

- **TCAD device simulation tool Silvaco ATLAS (2011)**.
- **Drift–diffusion equations** were solved for electrons and holes.
- **Fldmob** specifies a **lateral electric field dependent model** for electrons and was used to consider the **velocity saturation effect**.
- Because of **high channel doping concentration**, the **Fermi–Dirac distribution model without impact ionization** was utilised in the simulation.
- **Electric field dependent carrier model** was used.
- Due to **highly doped channel**, **band gap narrowing effect** may arise which was taken care using **BGN**.
- This model was necessary to model the bipolar current gain.
- **SRH** and **Auger recombination/generation** account for leakage currents due to thermal generation.
- **Quantum confinement effect** is not considered as it is negligible in the case of junctionless transistors.
- **Newton and Gummel method** used at **300 K** has been fixed.

In [YB20] a Monte Carlo simulation is performed. The Quasi-ballistic effect is introduced. In the image, it is possible to see the comparison between measured and simulated data.

- **Sentaurus TCAD**.
- **Drift-diffusion transport model** was calculated with **Poisson and carrier continuity equations**.
- **Density-gradient model** to consider the quantum confinement effects within the channels.
- **Slotboom bandgap narrowing model** for doping-dependent bandgap changes.
- **Quasi-ballistic effect** was considered by including **low-field ballistic model**.
- **Mobility and generation-recombination models**, and **stress-induced modifications of bandgap**, **effective mass**, and **mobility** were equivalent.

- **TCAD parameters** were calibrated by **fitting** the Ids of the **10-nm node FinFETs**.
- **Subthreshold swing** and **DIBL** were fitted first by changing S/D doping profiles.
- **Monte Carlo simulation** was performed to fit **ballistic coefficient** and **saturation velocity**.
- **Mobility parameters** related to **surface roughness scattering** were tuned to fit the Ids in the linear region.

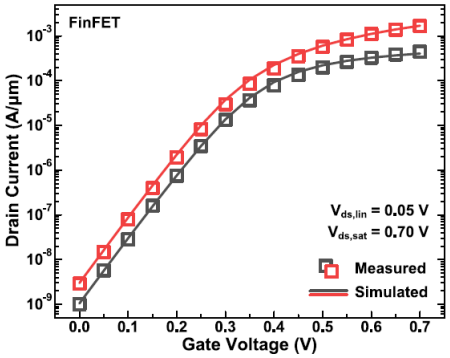


Figure 4.16. Bulk FinFETs calibrated to Intel. [YB20]

In [RR22] tunnelling effects start to be relevants.

- **3-D Sentaurus TCAD simulation** based on **drift-diffusion**, **continuity** and **Poisson's equation**.
- **Density-gradient quantization model** for **quantum confinement effect** and **source-to-channel tunnelling current**.
- **Low field ballistic model** for **quasi-ballistic transport**.
- **Slotboom bandgap narrowing model** for **bandgap narrowing** from **high doping of the source and drain regions**.
- **Lombardi mobility**, and **inversion and accumulation layer mobility models** for **mobility degradation** at the **silicon and SiO2 interface** due to **remote phonon surface** and **Coulomb scatterings**.
- **SRH recombination model** for generation and recombination in the **continuity equation**.
- For computing the analog/RF performance metrics, the devices are operated in the **mixed-mode simulation** and **small-signal equivalent circuits** are constructed from the **Y-function method**.

- A more realistic value of **fT** and **fmax** by exploiting the **short-circuit current gain (H21 = |Y12/Y11|)** and **MAG to 0 dB**.

The last analysed paper [Try] shows more recent models like hydrodynamic, MLDA, band-to-band and Philips unified. Also in this case an image is included to see the confrontation with experimental and simulation data.

- Various physics models that includes **Drift-diffusion**, **Hydrodynamic model**, **Fermi-Dirac statistics**, **MLDA model (quantum confinement effects)**, **SRH recombination**, **Band-to-band model**, **auger model**, **Philips unified** and **Lombardi mobility models**, **slotboom bandgap narrowing model** are included in simulation setup for analysis purposes.

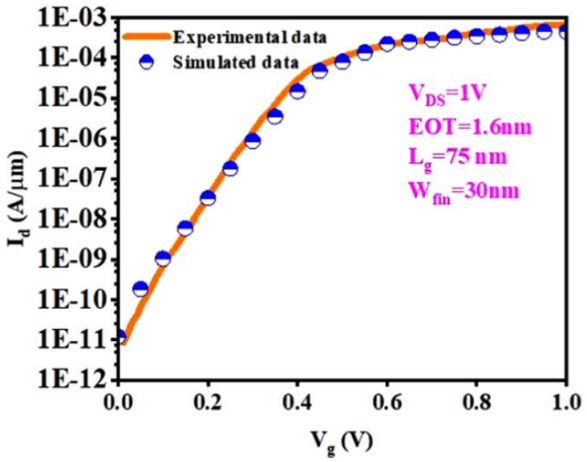


Figure 4.17. Calibration of experimental data. [Try]

Part II

Experimental

Chapter 5

Tools

For this thesis work several tools were used. In particular X2go client, Cadence Virtuoso, ADE L, model BSIM MG11.0.0.0. These tools will be analyzed in depth in the following sections.

5.1 X2go client

Figure 5.1. X2go client logo

X2Go is a remote desktop solution. The X2Go client is the user-facing component of this system, acting as a gateway to remote Linux environments. X2Go clients are available for Windows, macOS, Linux, and FreeBSD, allowing users to connect to remote Linux systems from virtually any device. Users can run and manage multiple remote sessions simultaneously, switching between them effortlessly. It allows you to disconnect from a session without closing it, enabling you to resume your work exactly where you left off, even after a network interruption. X2Go uses the NX protocol, which is highly efficient in terms of bandwidth usage. This makes it suitable for connections over slower networks or the Internet. You can access the complete remote desktop environment, run only specific applications remotely, use multiple monitors and adjust quality settings to balance performance and visual fidelity. The client includes built-in file transfer capabilities, allowing easy movement of files between local and remote systems. X2Go supports audio streaming and can even handle video playback, though performance may vary depending on network

conditions. The client can redirect local printers to the remote session, allowing you to print documents from the remote system to your local printer. For enhanced security, X2Go supports smart card authentication. Users can adjust compression settings to optimize performance based on their network conditions. All connections are secured using SSH, ensuring encrypted data transmission. X2Go's architecture allows for extensibility through plugins, enabling additional features and integrations. In addition to the graphical client, X2Go offers a command-line interface for advanced users and scripting purposes. On Linux systems, X2Go can integrate with the local desktop environment, making remote applications appear as if they're running locally. The client interface is available in numerous languages, making it accessible to a global user base. When launching the X2Go client, users are presented with a connection manager interface where they can configure and save multiple connection profiles. Each profile typically includes the IP address or hostname of the remote server, username for the remote system, SSH port, session type and additional options such as display settings, sound preferences, and shared folders. Once connected, the remote desktop or application appears in a window on the local machine, responsive and interactive as if it were running locally. The client provides a toolbar for managing the connection, accessing shared folders, and adjusting session properties on the fly. X2Go's client is particularly popular among system administrators, developers working with Linux environments, and organizations that need to provide secure remote access to Linux-based workstations or servers. Its combination of performance, security, and feature richness makes it a compelling choice for remote desktop access in the Linux ecosystem.

5.2 Cadence Virtuoso

Figure 5.2. Cadence logo

Cadence Virtuoso is a suite of EDA tools, primarily used in the semiconductor and electronics industry for designing and SoC solutions. It's a cornerstone platform for analog, mixed-signal, RF, and custom digital design. It has the capability to do schematic capture for circuit design, offers Layout tools for physical design, simulation, analysis and verification tools. It handles various process nodes, from mature technologies to cutting-edge processes, supporting different types of designs.It can also customize the layout editing, do automated placement and routing, LVS checking and DRC. It includes SPICE simulation for accurate circuit behavior prediction, fast SPICE for larger circuits, RF simulation capabilities and Mixed-signal simulation. It integrates in-design formal verification, ERC, power integrity and thermal analysis. It can be adoperated to create and employ reusable, customizable layout components. It has also tools for designing and analyzing 3D chip stacks and can interface with other Cadence tools. Cadence Virtuoso is able to manage industry-standard file format like GDSII and LEF/DEF. It supports design

data management and version control systems. It includes SKILL programming language for automating tasks and extending functionality and also supports Python scripting. It features team-based design with access control and concurrent editing. It can realize layout-dependent effects analysis, automated constraint management and assisted layout generation. It analyzes noise and mismatch and can run Monte Carlo simulations for yield estimation. Electromigration checking, IR drop analysis and ESD protection verification can be done. With the support to OpenAccess database for efficient data Handling and hardware-accelerated graphics for smooth navigation of large designs.When launching Cadence Virtuoso, users typically start with the Virtuoso ADE. This provides access to various tools such as schematic Editor, for creating circuit diagrams, layout Suite, for physical design of the , ADE Explorer, for setting up and running simulations, visualization and Analysis tools, for interpreting simulation results. The interface is highly customizable, with multiple windows and panels that can be arranged to suit the designer's workflow. Toolbars provide quick access to frequently used functions, while menus offer more comprehensive options. Designers often work across multiple views like schematic view, for logical circuit design, symbol view, for creating block representations, layout view, for physical design and simulation view, for setting up and running analyses.Virtuoso's ecosystem is vast, with numerous add-on tools and modules available for specific design tasks or technology nodes. It's deeply integrated with other Cadence tools, allowing for a seamless flow from concept to tape-out. Cadence Virtuoso is a critical tool in the semiconductor industry, used by major chip manufacturers, fabless semiconductor companies, and research institutions worldwide. Its comprehensive feature set, accuracy, and ability to handle complex designs make it indispensable for creating modern .

5.3 ADE L

ADE L is an advanced simulation and analysis environment within the Cadence Virtuoso platform, designed to streamline the process of analog and mixed-signal circuit design, simulation, and optimization. It supports various types of analyses and integrates multiple simulators like Spectre, APS, Ultrasim in a single interface. It allows easy sweeping of multiple parameters and supports corner analysis for PVT variations. It is possible to create and save reusable test setups and implement complex stimuli and measurement expressions. It has an interactive waveform display and manipulation, advanced measurement and calculation capabilities and dupport for user-defined measurements and expressions. It contains built-in optimization tools for meeting design specifications and support for yield analysis and design centering. It is possible to use organized storage and retrieval of simulation results and make comparison of results across different simulation runs or design iterations. As mention before SKILL and Python scripting are supported for automating repetitive tasks and also the creation of custom analyses and flows. Obviously, seamless connection with schematic editor and layout tools and support for in-design verification and analysis. It has the ability to simulate analog and digital portions of mixed-signal designs and offers co-simulation capabilities with digital simulators. ADE L has 2D and 3D plotting capabilities and eye diagram analysis for high-speed designs. First of all we have to define the simulation settings, analysis types, and design variables.

Then execute the simulations with specified parameters and corners. Examine results through waveforms, measurements, and calculations. If needed, adjust design parameters to meet specifications. Perform additional analyses to ensure design robustness. ADE L accelerates the design cycle by providing a comprehensive environment for simulation and analysis. it improves design quality through advanced optimization and verification capabilities, enhances productivity with reusable setups and automated workflows and facilitates collaboration through standardized processes and result sharing.

5.4 BSIM MG 11.0.0.0

Name	Unit	Default	Min	Max	Description
L	m	30e-9	1e-9	-	Designed gate length
D	m	40e-9	1e-9	-	Diameter of cylinder (for GEOMOD = 3)
TFIN	m	15e-9	1e-9	-	Body (fin) thickness
FPITCH	m	80e-9	TFIN	-	Fin Pitch
NF	-	1	1	-	Number of fingers
NFIN	-	1	> 0	-	Number of fins per finger
NFINNOM	-	1	> 0	-	Nominal number of fins per finger
NGCON	-	1	1	2	Number of gate contacts
ASEO	m^2	0	0	-	Source to substrate overlap area through oxide (all fingers)
ADEO	m^2	0	0	-	Drain to substrate overlap area through oxide (all fingers)
PSEO	m	0	0	-	Perimeter of the source to substrate overlap region through oxide (all fingers)
PDEO	m	0	0	-	Perimeter of drain to substrate overlap region through oxide (all fingers)
ASEJ	m^2	0	0	-	Source junction area (all fingers; for bulk MuGFETs, BULKMOD = 1)
ADEJ	m^2	0	0	-	Drain junction area (all fingers; for bulk MuGFETs, BULKMOD = 1)
PSEJ	m	0	0	-	Source junction perimeter (all fingers; for bulk MuGFETs, BULKMOD = 1)
PDEJ	m	0	0	-	Drain junction perimeter (all fingers; for bulk MuGFETs, BULKMOD = 1)
COVS	For F/m see CGEO1SW	0	0	-	Constant gate to source overlap capacitance (for CGEOMOD = 1)
COVD	For F/m see CGEO1SW	CVOS	0	-	Constant gate to drain overlap capacitance (for CGEOMOD = 1)
CGSP	For F/m see CGEO1SW	0	0	-	Constant gate to source fringe capacitance (for CGEOMOD = 1)
CGDP	For F/m see CGEO1SW	0	0	-	Constant gate to drain fringe capacitance (for CGEOMOD = 1)
CDSP	F	0	0	-	Constant drain to source fringe capacitance
NRS	-	0	0	-	Number of source diffusion squares (for RGEOMOD = 0)
NRD	-	0	0	-	Number of drain diffusion squares (for RGEOMOD = 0)
LRSD	m	L	0	-	Lenght of the source/drain

Table 5.1. Some of the parameters of the BSIM model.

BSIM MG 11.0.0.0 is a version of the BSIMMG (Berkeley Shortchannel IGFET Model MultiGate) transistor model, developed by the BSIM Group at the University of California, Berkeley. It's designed for accurate simulation of multigate transistor structures, particularly FinFETs. It accurately represents 3D FinFET structures, supports various fin shapes and sizes and improves the modelling of corner effects in multi-fin devices. It contains refined quantum confinement models, improved density gradient approach for carrier distribution, better modelling of DIBL, improved subthreshold swing prediction and enhanced velocity saturation modelling. Comprehensive temperature scaling for all major parameters and improved SH model for high power applications. It has advanced $\frac{1}{f}$ models and accurate channel thermal noise prediction. Updated HCI models, improved TDDB prediction. Enhanced capacitance models for multifin structures, improved S/D resistance modelling, better prediction of G_M and G_{DS}, improved modelling of GIDL, smooth transitions between different operating regions. It offers improved convergence in circuit simulations, enhanced scalability across different technology nodes and support for

various FinFET configurations. It is compatible with major SPICE-based circuit simulators, an extensive set of model parameters for finetuning, comprehensive documentation and parameter extraction guidelines. It supports single-device and circuit-level simulations and enables accurate design and simulation of advanced FinFET-based circuits. It can develop cutting-edge semiconductor processes, facilitate optimisation of device performance and power consumption and enhance reliability predictions for complex designs.

Chapter 6

Simulation

6.1 Import VerilogA models

First of all, we have to start Cadence Virtuoso. It is advisable to create a new directory before starting. An X2go client to connect to a remote machine is used for this thesis work. So, open the X2go program. The first time the "New Connection" window should open automatically, if not, open it by clicking on the "New session" icon in the top bar.

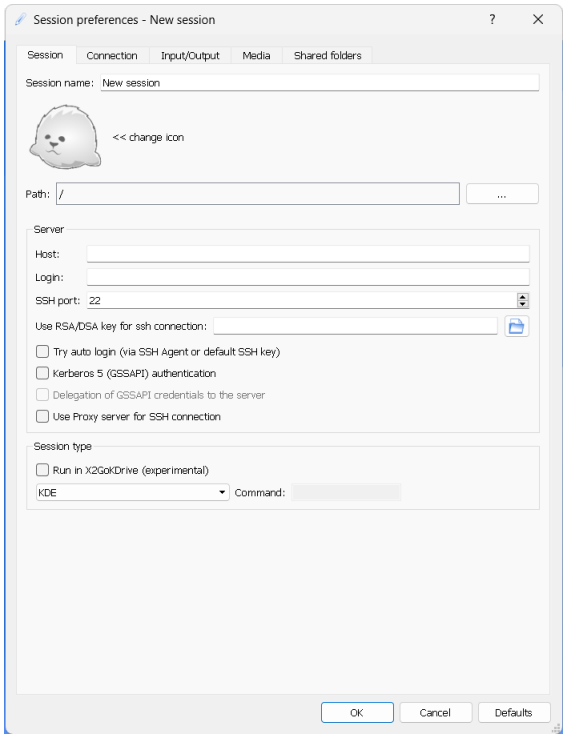


Figure 6.1. "New session" window of x2go client.

Now it's time to insert the connection parameter as the session name (it is possible to choose whatever name, desirable to pick something easy to recognise), the host, the username (under the login voice), the SSH port, the session type and then click "OK". Select the connection on the right part of the window and insert your password.

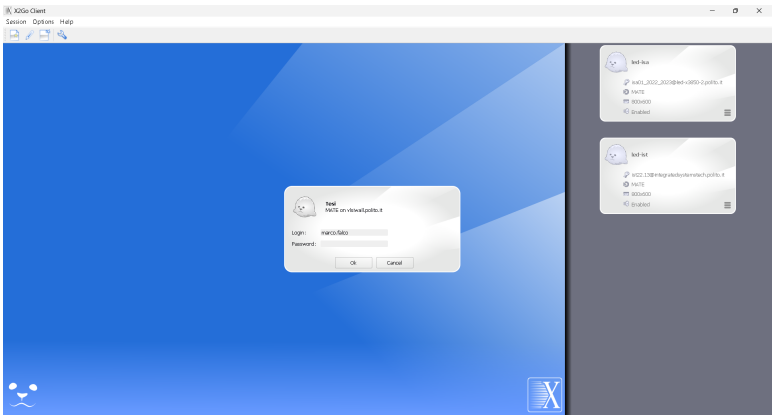


Figure 6.2. "Login" window of x2go client.

In my case, the remote machine runs Centos7, a distro Linux. To create the directory open a terminal and write "mkdir" followed by the name you want to give to it. Enter the directory by typing "cd" followed by the same name. Now you should prepare the environment for working with the Virtuoso CAD tool. I have employed the 2020/2021 edition to save resources. This is the script that I used:

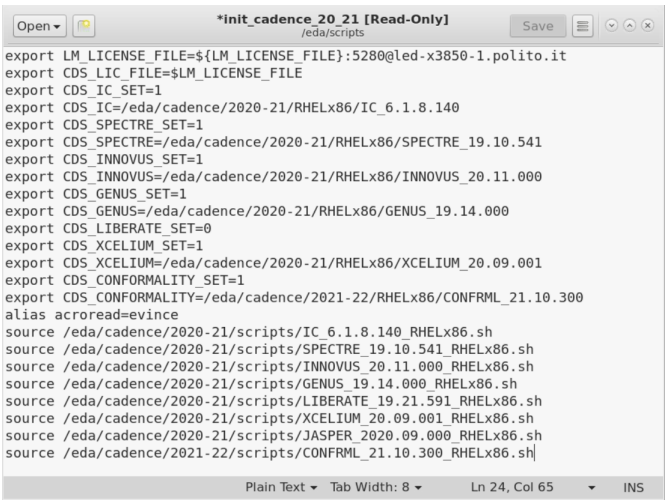


Figure 6.3. Script to set the Cadence Virtuoso environment.

Now launch the tool by typing "virtuoso". Insert a & to run the program in the

background to use the shell for other purposes. The first window that appears is called CIW.

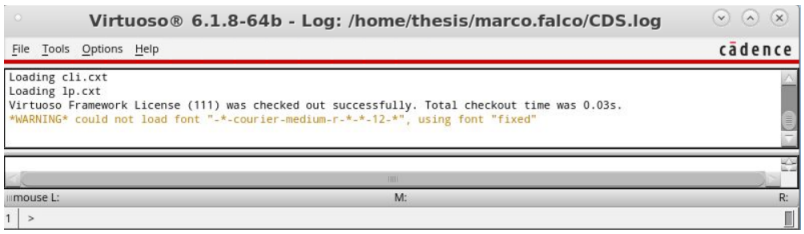


Figure 6.4. Command Interpreter Window.

To import the BSIM library open the library path editor from Tools → Library path editor.

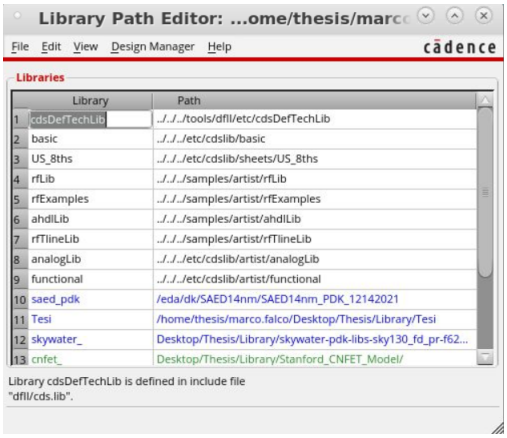


Figure 6.5. The editor to import library in Cadence Virtuoso.

Write the library name then insert the path in the right column. After you finish it should become green if there are not any problems. Now open the Library manager from Tools → Library manager in CIW menu. This window will appear.

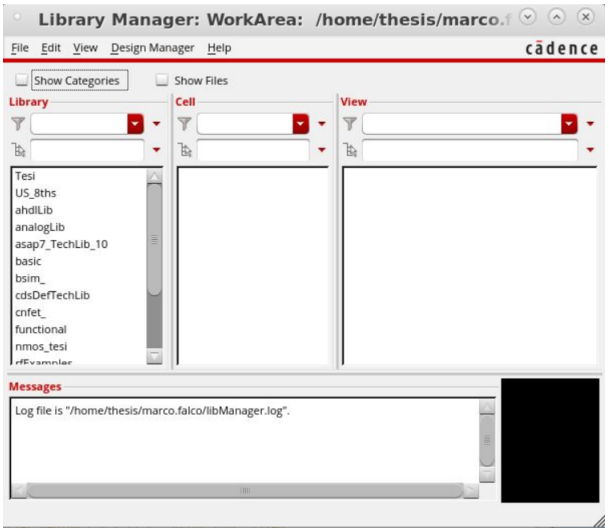


Figure 6.6. The editor to import library in Cadence Virtuoso.

You should see the library of the previous step listed on the left. Click on the library and create a new cell view selecting File → New → Cell view. Insert an explicative name and in the tab "Type" pick VerilogA as in the image and press OK.

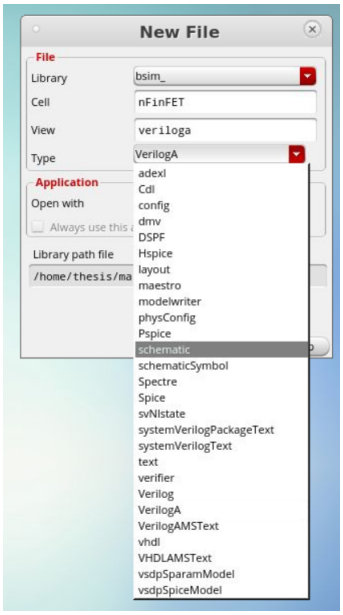


Figure 6.7. New cell window.

The VerilogA text editor will appear.

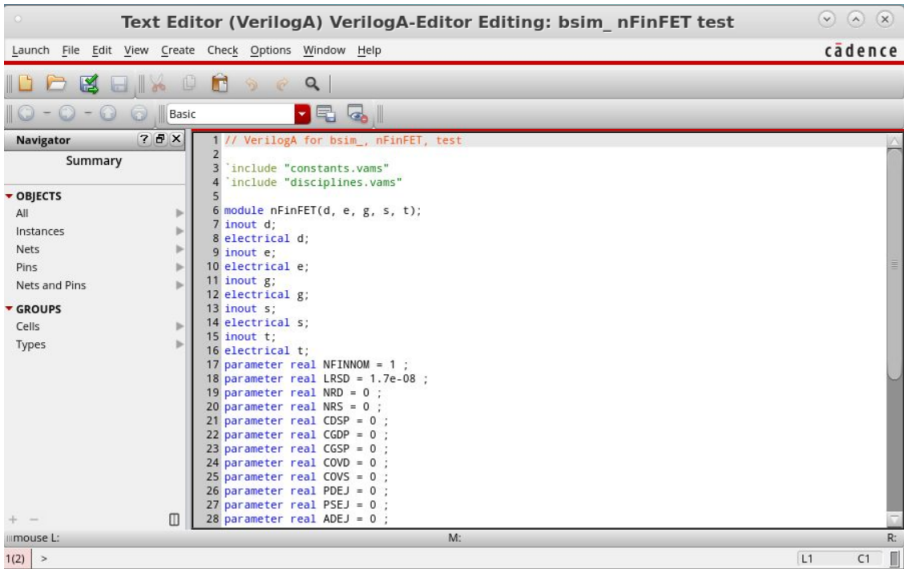


Figure 6.8. The VerilogA text editor of Cadence Virtuoso.

Delete all and copy the verilogA file describing the BSIM n-FET (bsimcmg.va).

6.1.1 Create the symbol

Modifying the module name in line 83 should be necessary to avoid conflicts. Verify that in bsim-cmg_body.include at line 159 GEOMOD is set to 1 (to model a SOI triple-gate FinFET). Correct all the errors (generally the library paths and comments). You can find them running the extract button on the top left position. If an error is encountered it is saved into View → Parser log file. Once you solve all the errors a window asking to create a symbol will appear. Say "Yes" and place the pins as shown below, then click OK.

Figure 6.9. The symbol generation options window of Cadence Virtuoso.

The symbol will appear. The t terminal is related to the activation of a thermal model and the e corresponds to the bulk terminal.

6.2 Test the n-FinFET

Close the symbol window and create a new cell view as before. Now choose the schematic as "Type" and replicate the following circuit that will appear in the editor.

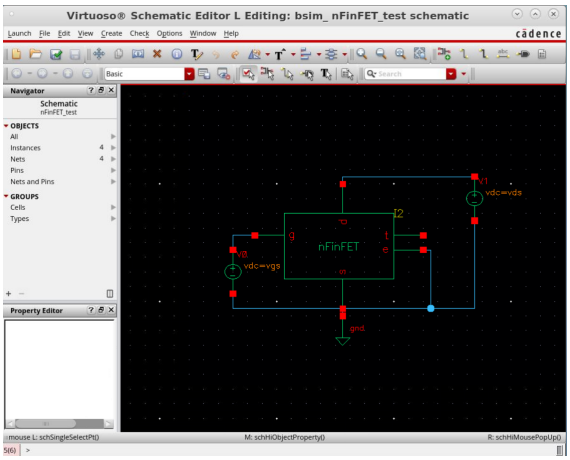


Figure 6.10. The test circuit realised into the schematic editor of Cadence Virtuoso.

To generate a schematic like this you need to press the "I" button and then the following windows will appear:

Figure 6.11. The add instance window of the Cadence Virtuoso schematic editor.

Choose the correct library and cell to insert the FinFet in the schematic. We also need two vdc and a gnd of analogLib library. To track the wires click and drag the mouse. If you change the mode use the "W" button to return to the wire insertion. For the transistor, I used the following properties:

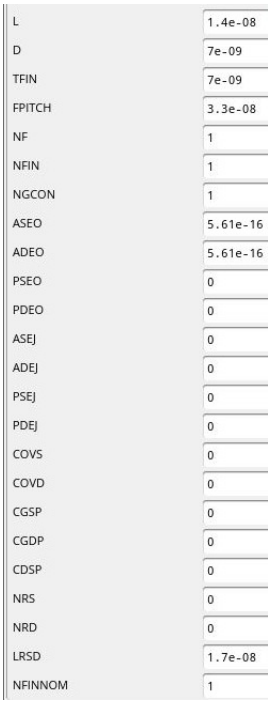


Figure 6.12. The parameters set for the BSIM n-FET.

The parameters description is in table 5.1. In particular, the selectors ADEO and ASEO are evaluated as FPITCH · NFIN · LRSD. After the circuit realisation select File → Check and save. Errors will be marked with yellow boxes on the schematic. Fix them. You will have a warning due to the floating terminal "t". Disregard it and select Launch → ADE-L. This window will appear:

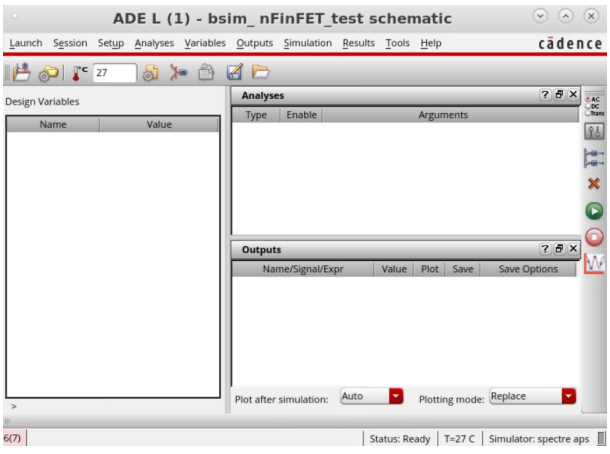


Figure 6.13. The Analog Design Environment interface.

From ADE windows select Variables → Edit and add V_{GS} and V_{DS} (right-click in the design variables area and select copy from cell view). Set them to 1 V. Now go to Analyses → Choose and copy the following setup.

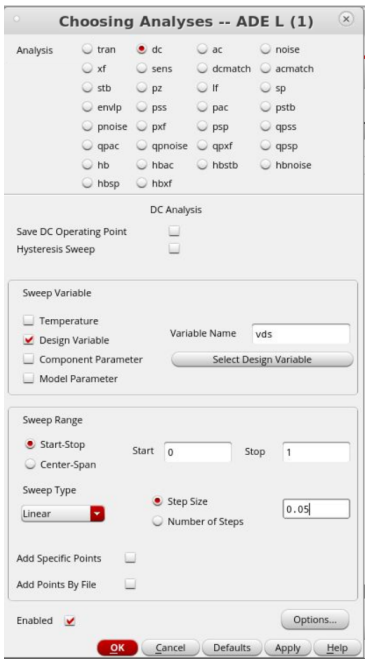


Figure 6.14. Setup for a DC analysis with sweeping V_{DS} from 0 to 1 V in steps of 50 mV .

Confirm then Outputs → To-be-plotted → Select on schematic. In the schematic window click on the drain contact. All the selected options will appear in the ADE interface. Tools → parametric analysis and in the windows that open up choose V_{GS} from 0 to 1 V in linear steps of 0.2 V. Click on the play button. This is the result.

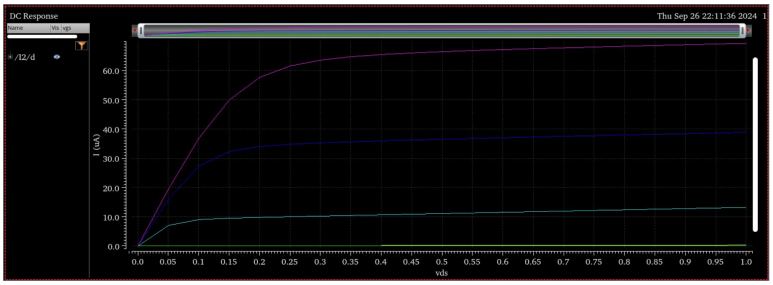


Figure 6.15. DC response with parametric analysis of V_{GS} from 0 to 1 V in steps of 0.2 V .

6.3 Single stage CS amplifier

To explore the utilisation possibility of FinFET in the analog field I tried to replicate the amplifier in Fig.4.14. This is the schematic realised with the Cadence editor.

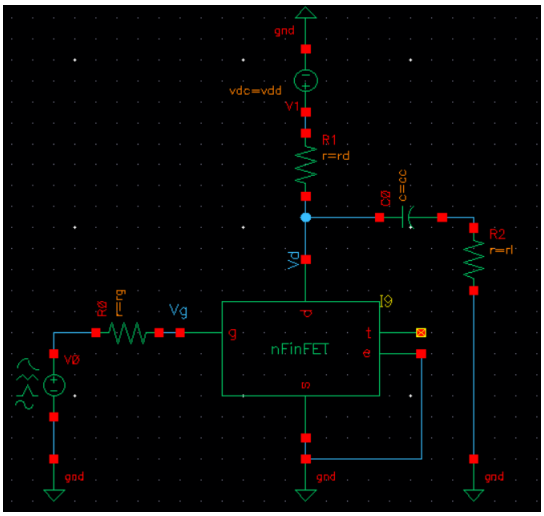


Figure 6.16. Replica of single stage CS amplifier of Fig.4.14.

With the same parameters of [Try] the following output is obtain:

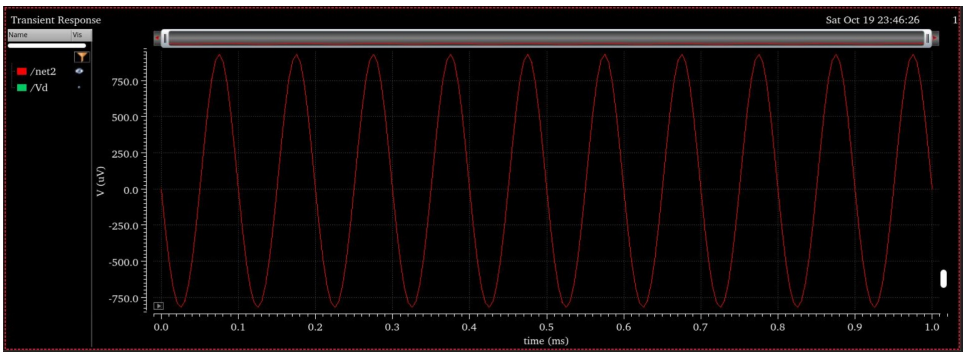


Figure 6.17. V_{OUT} of the amplifier.

We take a look at the I_D:

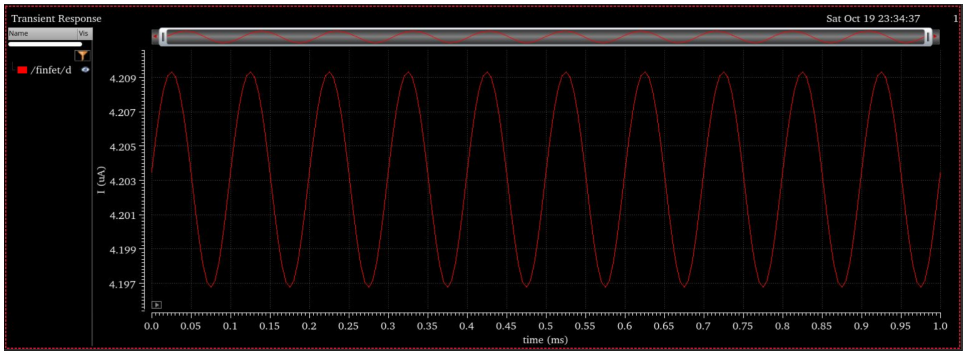


Figure 6.18. I_D of the amplifier.

Now we can run a DC analysis and save the DC Operating Point to see what is happening in our model.

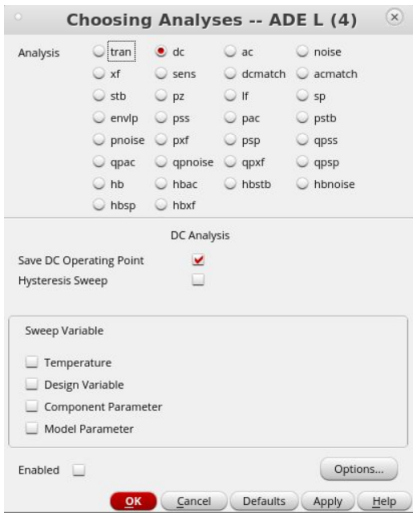


Figure 6.19. I_D of the amplifier.

This kind of analysis doesn't show any plot. To see the results select Results → Print → DC Operating Point. A list of parameters will appear. I insert those of greatest interest in a table to be more synthetic.

Parameter	Value
G_{DS}	209.3u
G_M	18.89u
I_{DS}	4.203u
I_{TH}	80.03n
$V_{DS,sat}$	75.38m
V_{FB}	-89.66m
V_{TH}	543.2m
W_{EFF}	67n

Table 6.1. DC operating point

We can also visualise DC currents and voltages on the schematic by going to View → Annotations → DC Voltages, Currents.

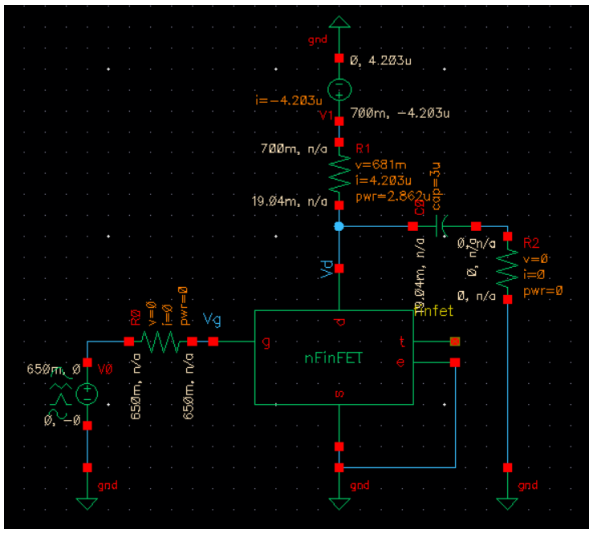


Figure 6.20. DC currents and voltages on the schematic.

The AC coupling is working correctly and from the data, we can see that $V_{GS} > V_{TH}$, but $V_{DS} < V_{GS} - V_{TH}$, so we are in the triode zone. The transistor probably can't work in the saturation zone due to a big R_L. When R_L raises, V_D is reduced until it becomes similar to V_S. Since our amplifier is a common source, the source is connected to the ground, so the voltage at the ends of R_L is almost V_{DD}. The circulating current will be limited by V_{DD} and R_L values.

$$I_D \cong \frac{V_{DD}}{R_L} = \frac{700mV}{162k\Omega} \cong 4{,}3\mu A$$

We can extrapolate the value of

$$k = \mu_0 \cdot C_{OX} \cdot \frac{W}{L} = \frac{G_M}{2 \cdot V_{DS}} = \frac{18{,}89\mu A/V}{2 \cdot 19{,}04mV} = \frac{18{,}89\mu A/V}{38{,}08mV} \cong 0{,}496mA/V^2$$

Let's deeply analyse the output voltage.

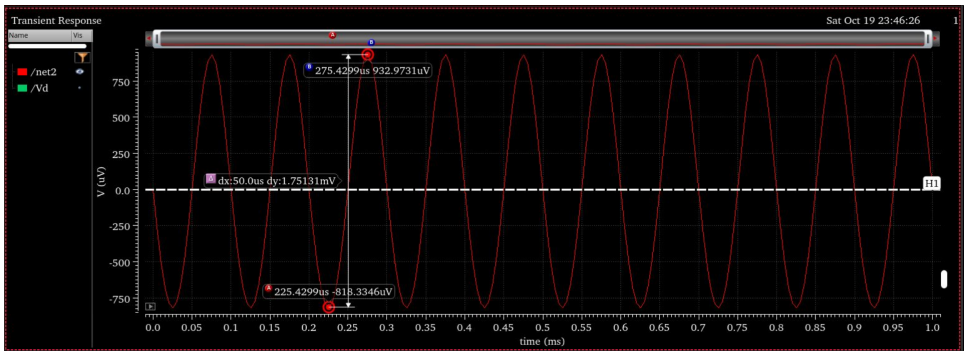


Figure 6.21. DC currents and voltages on the schematic.

We can see a distortion in the V_{DS}. We have a total y variation of about 1,751 mV so in a symmetric sinewave we expect to have two half waves of 875,5 μV of amplitude. In reality, the positive half-wave has an amplitude of 933 μV and the negative one of 818 μV. This is because the little signal variations of the current are summed to the polarisation value. This generates a quadratic term. The introduced error cannot be symmetric because the quadratic term is always positive. This brings to a lower positive half-wave and consequently a higher negative half-wave. Regarding the frequency, the period is about 100 μs as expected.

6.4 Polarisation net

We must realise a polarisation net to ensure our transistor works in the saturation region. First, a DC analysis was executed with V_{DS} sweeping from 0 to 36V and increasing V_{GS} of linear steps of 0.2V. It is possible to see the trend of the I_D improve until V_{GS} reaches 6V and then starts to fall.

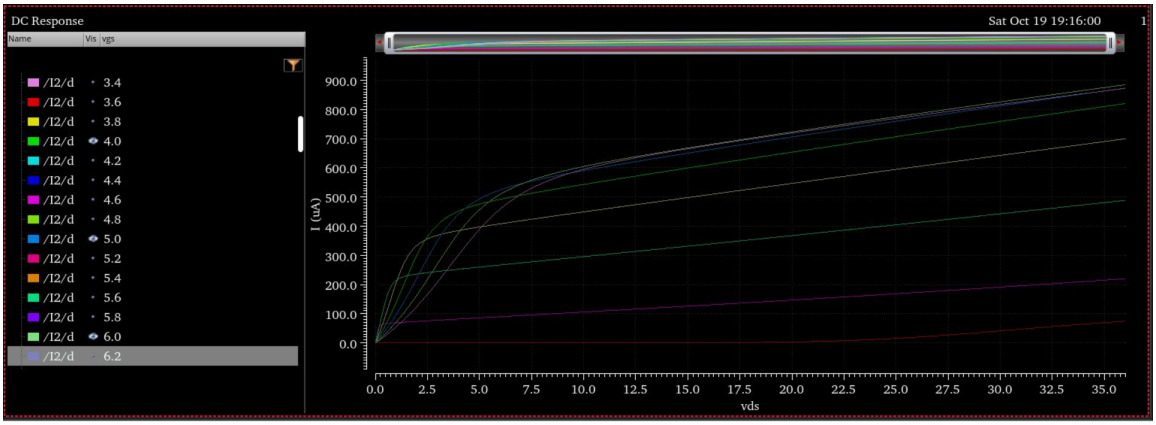


Figure 6.22. Transcharacteristic of "BSIMCMG110.0.0".

Approximately after 5V, the finFET reaches the saturation zone. Hence, we use it to simulate the glsid vs V_{GS} characteristic of the finFET, sweeping the V_{GS} parameter to find the one that best fits our needs. The sweep is performed from 0 to 36V.

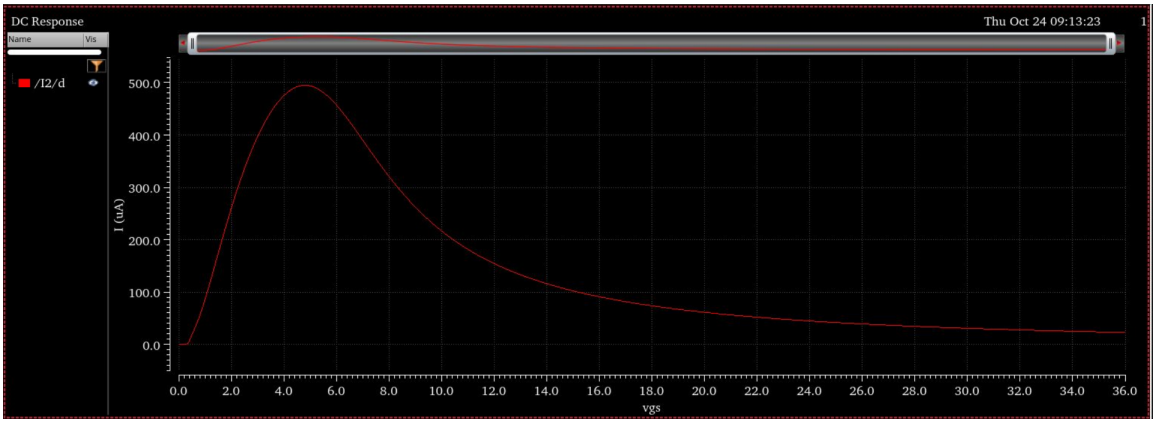


Figure 6.23. Characteristic of "BSIMCMG110.0.0".

Zooming on the V_{TH}:

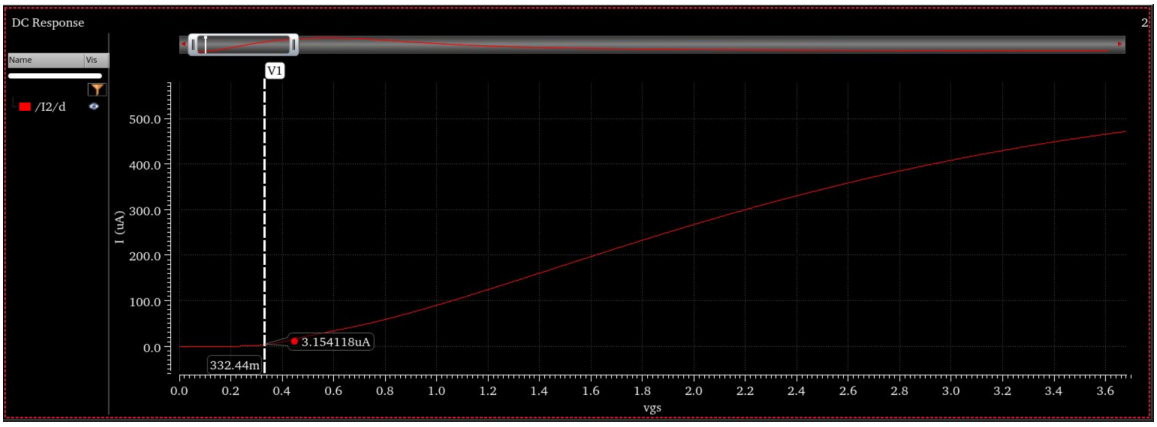


Figure 6.24. V_{TH} of "BSIMCMG110.0.0".

The value is about 332,4 mV so the V_{OV} is about V_{GS}-V_{TH} ≅ 5,6 V. The V_{DS} has to be over this value to guarantee the finFET works in saturation. It is preferable to work under 10 V because we need to set a particular option in the simulator over this value to have better results. Remembering that a lithium battery cell is about 3.6 V the value chosen is 7.2 V.

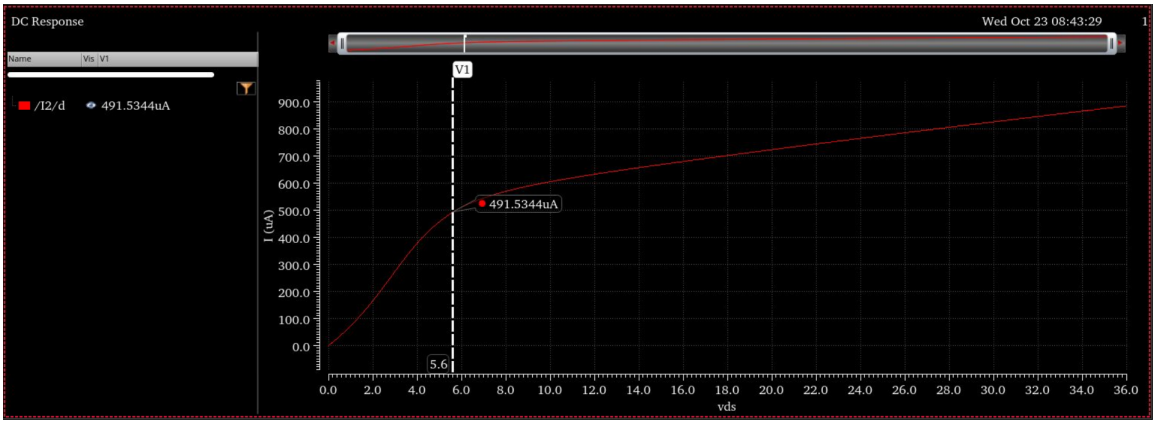


Figure 6.25. V_{OV} of "BSIMCMG110.0.0".

A DC operating point simulation was run to find the exact value of V_{TH}.

VFB	-309.9m
VTH	453.7m
WEFF	67n
WEFFCV	67n
subckt_trise__	0

Figure 6.26. Verification of "BSIMCMG110.0.0"'s V_{TH}.

The value is higher due to higher V_{DS} as expected but still guarantees to work in the saturation region. V_{OV} is about 5.5 V. To find the k of the transistor a DC response is plotted.

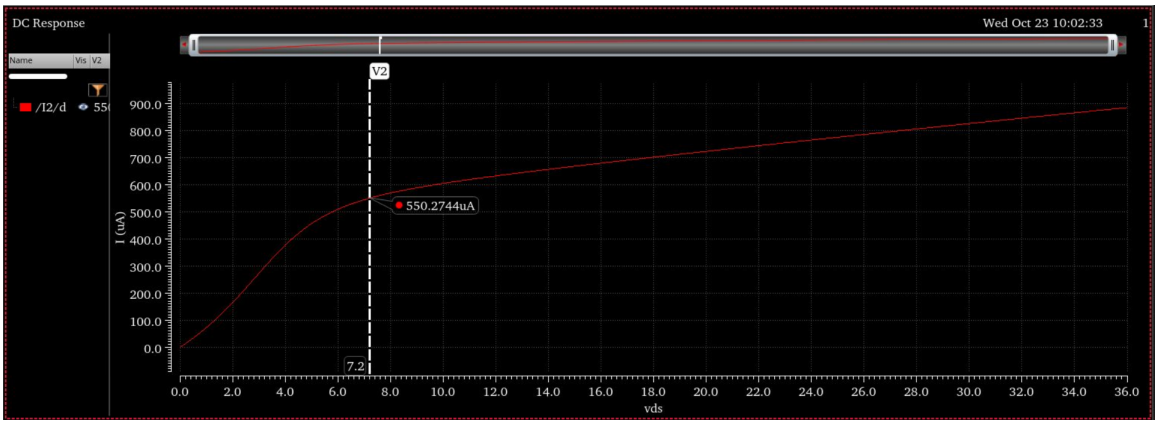


Figure 6.27. I_D of "BSIMCMG110.0.0" at V_{DS} = 7.2 V.

The value of VEA is needed to estimate the k. So the characteristic is plotted sweeping V_{DS} from -50 V to 36 V. The VEA value is the intercept of the line's extension that identifies the saturation current.

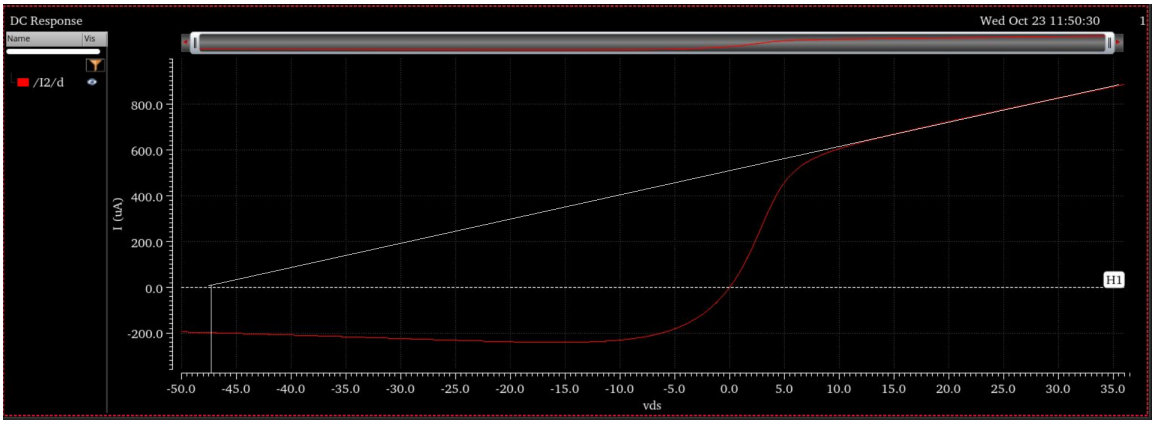


Figure 6.28. VEA of "BSIMCMG110.0.0".

The value is approximately 47.5 V. So starting from the formula to calculate the I_D in the saturation zone it is possible to find the value of k:

$$I_D = k(V_{GS} - V_{TH})^2 \cdot (1 + \frac{V_{DS}}{V_A}) \cong 34.79\mu A/V^2$$

and then the R_0:

$$\frac{V_A}{k(V_{GS}-V_{TH})^2} \cong 73{,}9M\Omega$$

which is a reasonably high value.

6.4.1 Schematic

It is expected a $I_U \cong 550\mu A$. It is preferable to have a polarization current percentage smaller than the I_D so it was chosen $50\mu A$. The choice of resistance values is not unique the designer has to consider that small values bring high polarisation current and then higher power consumption and high values bring difficult integration, higher delays and higher costs. $V_{DS} = 7.2V$ is wanted so it was decided to use a $V_{DD} = 9V$. To guarantee V_{GS} = 6V on R_1 must generate a drop voltage of 3 V and R_2 of 6V.

$$\begin{cases} I_{POL} \cdot R_1 = 3V \rightarrow R_1 = \frac{3V}{50\mu A} = 60k\Omega \\ I_{POL} \cdot R_2 = 6V \rightarrow R_2 = \frac{6V}{50\mu A} = 120k\Omega \end{cases}$$

The last thing to design is the R_L. V_{DS} has to be 7.2 V to guarantee staying in the middle of the dynamic, the load can generate a maximum voltage drop of 3.6V.

$$\frac{2 \cdot (V_{DD} - V_S)}{R_{L,MAX}} = I_U \rightarrow \frac{2(9V - 7.2V)}{R_{L,MAX}} = 550\mu A \rightarrow R_{L,MAX} = \frac{2 \cdot 1.8V}{550\mu A} = \frac{3.6}{550\mu A} \cong 6.5k\Omega$$

to find R_L:

$$R_L = \frac{R_{L,MAX}}{2} = \frac{6.5k\Omega}{2} = 3.25k\Omega$$

$3.3k\Omega$ is the nearest value of commercial resistance. The following schematic is created. A DC simulation was run and the values appear near the resistances.

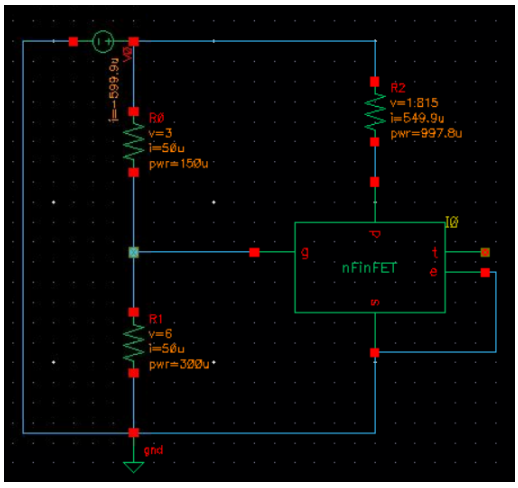


Figure 6.29. DC operating points of the polarisation net.

As it is possible to see, the current flowing into the resistor divider is 50μ A as designed. In output, there are about 550μ A. The polarisation net is working correctly.

6.5 DC or AC coupling

It is important to avoid destroying the polarisation when the input signal arrives. Two ways: a DC or AC coupling.

6.5.1 DC

In the first case, it is required to have the same potential in both the parts to be linked.

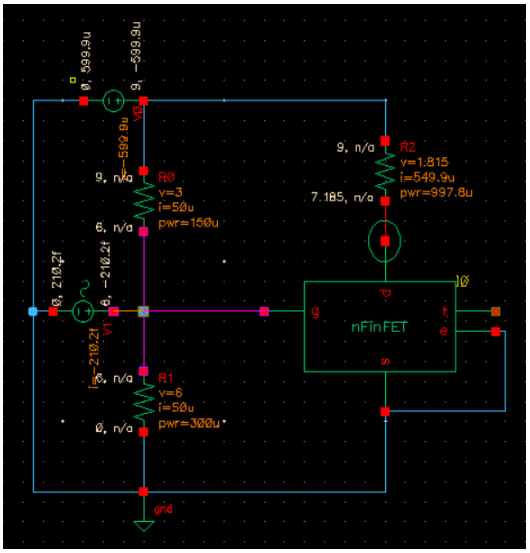


Figure 6.30. transient voltages coupling net at the same potential.

A generator referred to the ground cannot be directly connected to the gate of a MOSFET with the source to ground because if there is no signal it imposes its referred voltage to the gate.

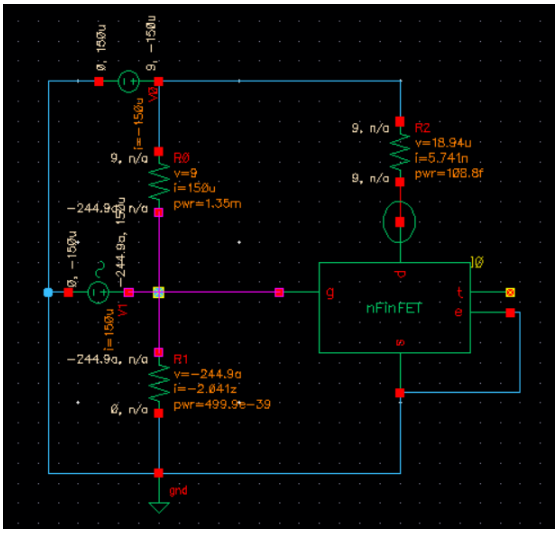


Figure 6.31. transient voltages coupling net at a different potential.

If the gate is at 0 V direct coupling could be used. An appropriate negative voltage must be supplied to the source. If the source of the signal has a resistance it must be considered. In fact:

$$V_A = V_{IN} \cdot \frac{R_{12}}{R_{12} + R_G}$$

Generally the input signal arrives from a sensor with low impedance. A 100 Ω resistance is tested.

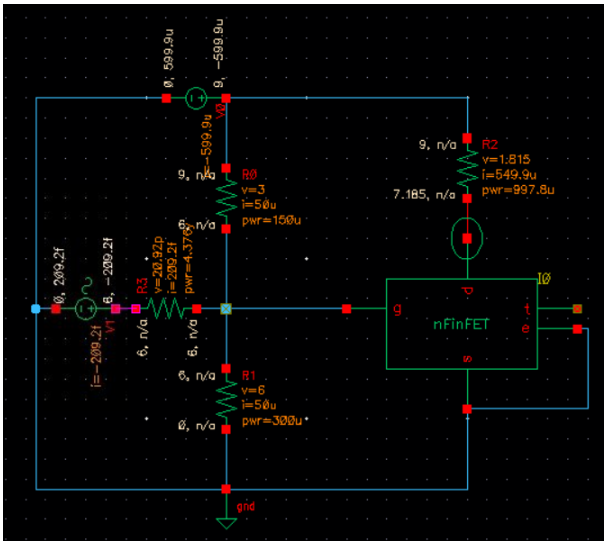


Figure 6.32. transient voltages coupling net with resistance.

Sometimes is possible to introduce some diodes to remove the potential differences.

6.5.2 ac

It is possible to separate the polarization from the signal by introducing a capacitor in series with the source of the signal. In this way we avoid the DC connection, letting pass the voltage variations. It is possible only when there is a known minimum frequency because the capacitor introduced a zero in 0, but also a pole at a frequency obtained by the product from the value of the capacitor and the total resistance seen at its ends.

$$F_{POLE} = \frac{1}{C \cdot R_{TOT}} \rightarrow C = \frac{1}{F_{POLE} \cdot R_{TOT}} \cong 400pF$$

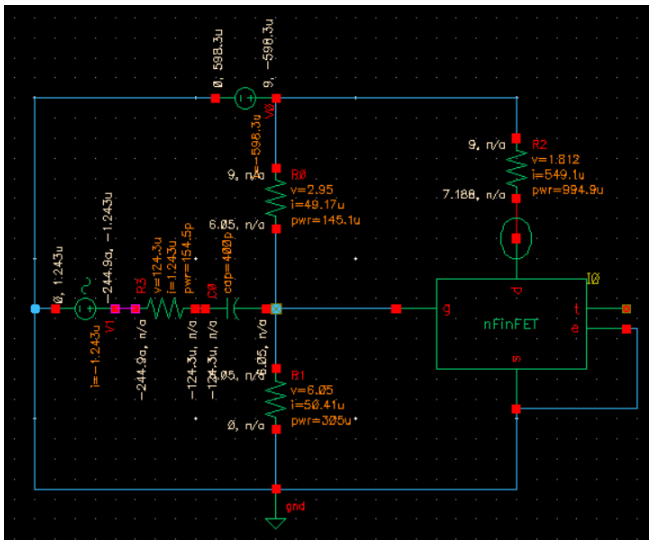


Figure 6.33. AC coupling.

6.6 Transient analysis

As an input signal is preferable to select a signal with an amplitude neither too small nor too high concerning V_{TH}. In this case 100 mV. Here the transient analysis of the V_{OUT}

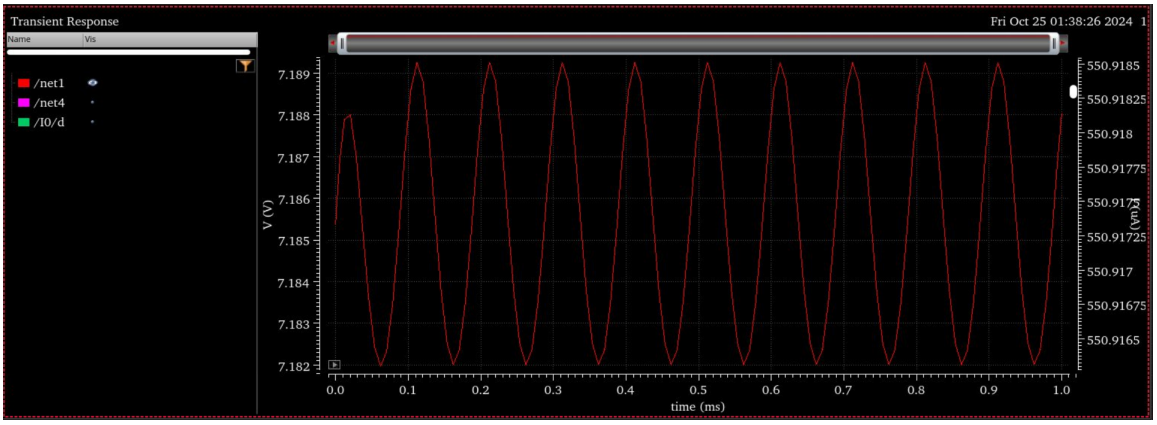


Figure 6.34. Transient analysis of V_{OUT}.

There is no amplification despite we are in the saturation region. It is possible to try to modify the channel doping.

Bibliography

[Bie04] K. Henson; R.J.P. Lander; M. Demand; C.J.J. Dachs; B. Kaczer; W. Deweerdl; T. Schram; Tokei; J.C. Hooker; F.N. Cubaynes; S. Beckx; W. Boullart; B. Coenegracht; J. Vertommen; 0. Richard; H. Bender; W. Vandervorst; M. Kaiser; J-L. Everaert; M. Jurczak; S . Biesemans. "45nm nMOSFET with Metal Gate on Thin SiON Driving 1150μA/μm and Off-state of 10nA/μm". In: *IEEE XPLORE* 35.2 (2004), pp. 1–4.

[GJM05] A. Dixit; K. G., A. Merchal; N. Collaert; S. Brusl; 0. Richard; R. Rmyacken; M. Goodwin; M. Jurczak; and K. De Meyer. "Towards Optimally Shaped Fins in P-Channel Tri-Gate FETs: Can Fin Height Be Reduced Further?" In: *IEEE XPLORE* 11.3 (2005), pp. 1–2.

[SD06] Vaidy Subramanian; Bertrand Parvais; Jonathan Borremans; Abdelkarim Mercha; Dimitri Linten; Piet Wambacq; Josine Loo; Morin Dehan; Cedric Gustin; Nadine Collaert; Stefan Kubicek; Robert Lander; Jacob Hooker; Florence Cubaynes; Stephane Donnay; Malgorzata Jurczak; Guido Groeseneken; Willy Sansen; and Stefaan Decoutere. "Planar Bulk MOSFETs Versus FinFETs: An Analog/RF Perspective". In: *IEEE TRANSACTIONS ON ELECTRON DEVICES* 53.12 (2006), pp. 1–9.

[KA07] Abhinav Kranti and G. Alastair Armstrong. "Design and Optimization of FinFETs for Ultra-Low-Voltage Analog Applications". In: *IEEE transactions on electron devices* 54.12 (2007), pp. 1–9.

[PWBVKSJBMDDLVDHD07] Geert Van der Plas; Abdelkarim Mercha; Bertrand Parvais; Cedric Gustin; Vaidy Subramanian; Nadine Collaert; Malgorzata Jurczak Piet Wambacq; Bob Verbruggen; Karen Scheir; Jonathan Borremans; Morin Dehan; Dimitri Linten; Vincent De Heyn and Stefaan Decoutere. "The

Potential of FinFETs for Analog and RF Circuit Applications". In: *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS* 54.11 (2007), pp. 1–11.

[;12] Chang-Woo Sohn; Chang Yong Kang; Rock-Hyun Baek; Member ; Do-Young Choi; Hyun Chul Sagong; Eui-Young Jeong; Chang-Ki Baek; Jeong-Soo Lee; Jack C. Lee; Fellow ; and Yoon-Ha Jeong; Fellow. "Device Design Guidelines for Nanoscale FinFETs in RF/Analog Applications". In: *IEEE ELECTRON DEVICE LETTERS* 33.9 (2012), pp. 1–3.

[SC12] M. G. C. De Andrade; J. A. Martino; M. Aoulaiche; N. Collaert; E. Simoen; and C. Claeys. "Behavior of triple-gate bulk FinFETs with and without DTMOS operation". In: *Solid. State. Electron.* 71 (2012), 63–68.

[SS15] S. K. Mohapatra; K. P. Pradhan; D. Singh; and P. K. Sahu. "The Role of Geometry Parameters and Fin Aspect Ratio of Sub-20nm SOI-FinFET: An Analysis Towards Analog and RF Circuit Design". In: *IEEE TRANSACTIONS ON NANOTECHNOLOGY* 14.3 (2015), pp. 1–8.

[Che16] Fu-Lung Hsueh; Yung-Chow Peng; Chung-Hui Chen; Tzu-Jin Yeh; Hsieh-Hung Hsieh; Chin-Ho Chang; Szu-Lin Liu; Mei-Chen Chuang; Mark Chen. "Analog/RF Wonderland: Circuit and Technology Co-optimization in Advanced FinFET Technology". In: *Symposium on VLSI Technology Digest of Technical Papers* (2016), pp. 1–2.

[RT17] Syed Samsuz Zaman; Pankaj Kumar; Manash Pratim Sarma; Ashok Ray and Gaurav Trivedi. "Design and Simulation of SF-FinFET and SD-FinFET and Their Performance in Analog, RF and Digital Applications". In: *IEEE International Symposium on Nanoelectronic and Information Systems* (2017), 1–6.

[HC18] Bo-Yuan Chen; Kun-Ming Chen; Chia-Sung Chiu; Guo-Wei Huang; Hsiu-Chih Chen; Chun-Chi Chen; Fu-Kuo Hsueh and Edward Yi Chang. "Analog and RF Characteristics of Power FinFET Transistors With Different Drain-Extension Designs". In: *IEEE transactions on electron devices* 66.10 (2018), 1–7.

[LS18] Jagar Singh; J. Ciavatti; K. Sundaram; J. S. Wong; A. Bandyopadhyay; X. Zhang; S. Li; A. Bellaouar; J. Watts; J. G. Lee and S. B. Samavedam. "14-nm FinFET Technology for Analog and RF Applications". In: *IEEE transactions on electron devices* 65.1 (2018), 1–7.

[LB18] JUN-SIK YOON; JINSU JEONG; SEUNGHWAN LEE; and ROCK-HYUN BAEK. "Systematic DC/AC Performance Benchmarking of Sub-7-nm Node FinFETs and Nanosheet FETs". In: *JOURNAL OF THE ELECTRON DEVICES SOCIETY* 6 (2018), pp. 1–6.

[Sar18] Kalyan Biswas; Angsuman Sarkar; Chandan Kumar Sarkar. "Fin shape influence on analog and RF performance of junctionless accumulation-mode bulk FinFETs". In: *Microsystem technologies* (2018), pp. 1–8.

[YB20] JUN-SIK YOON and ROCK-HYUN BAEK. "Device Design Guideline of 5-nm-Node FinFETs and Nanosheet FETs for Analog/RF Applications". In: *IEEE Access* 8 (2020), 1–9.

[RF21] VALERIYA KILCHYTSKA; SERGEJ MAKOVEJEV; BABAK KAZEMI ESFEH; LUCAS NYSSENS; ARKA HALDER; JEAN-PIERRE RASKIN and DENIS FLANDRE. "Extensive Electrical Characterization Methodology of Advanced MOSFETs Towards Analog and RF Applications". In: *Journal of the electron devices society* 9 (2021), 1–11.

[RR22] Anjali Goel; Akhilesh Rawat and Brajesh Rawat. "Benchmarking of Analog/RF Performance of Fin-FET, NW-FET, and NS-FET in the Ultimate Scaling Limit". In: *IEEE transactions on electron devices* 69.3 (2022), 1–8.

[Try] "Optimizing U-Shape FinFETs for Sub-5nm Technology: Performance Analysis and Device-to- Circuit Evaluation in Digital and Analog/Radio Frequency Applications". In: *ECS Journal of Solid State Science and Technology* (2023), pp. 1–13.

[MD] F. Andrieu; O. Faynot; X. Garros; D. Lafond; C. Buj-Dufournet; L. Tosti; S. Minoret; V. Vidal; J.C. Barbé; F. Allain; E. Rouchouze; L. Vandroux; V. Cosnier; M. Cassé; V. Delaye; C. Carabasse; M. Burdin; G. Rolland; B. Guillaumot; J.P. Colonna; P. Besson; L. Brévard; D. Mariolle; P. Holliger; A. Vandooren; C. Fenouillet-Béranger; F. Martin and S. Deleonibus. "Comparative Scalability of PVD and CVD TiN on HfO2 as a Metal Gate Stack for FDSOI cMOSFETs down to 25nm Gate Length and Width". In: *IEEE explore* (), pp. 1–4.