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Leakage currents in hafnia-based ferroelectric capacitors: modeling and validation

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To my parents and closest friends
To me
And to God

—*We've had a good ride.*
—*The best.*
Tali to Shepard, Mass Effect 3

Abstract

The recent advancements in machine learning, along with its increasingly widespread applications, have soon highlighted the limitations of the conventional Von-Neumann architecture, particularly excessive power consumption and high delay. An emerging computing paradigm inspired by the brain referred to as Neuromorphic computing promises to address these challenges. Some benefits of this new paradigm stem from the usage of innovative memory elements, such as ferroelectric capacitors (FeCaps). Hafnia-based ferroelectric memories are among the most promising emergent memory technologies due to their high endurance, high switching speed and low power consumption[1–6]. Of particular relevance for the characterization of hafnia-based FeCaps is the study and modeling of the leakage currents flowing through the capacitor stack. If leakage is not modeled properly, when the FeCap model is used in the context of circuit design, the functionality of the circuit could be severely impaired. To address this need, this work aims at modeling the leakage currents flowing through the FeCap stack. The leakage model has been implemented inside a FeCap compact model for analog circuit simulations. A compact model provides a mathematical description of the physics of a specific electronic device. The core of a compact model describes the fundamental behavior of the device, and can be enriched by including additional phenomena such as leakage currents. Compact models are fundamental for integrated circuits development, because their simplicity and high accuracy allow for the adoption of computationally intensive Monte Carlo methods, which are essential for designing scalable and reliable integrated circuits. This work started by updating the initial, resistance-based implementation of leakage to include the relevant conduction mechanisms in nanometric thin films. I evaluated the impact of three different leakage models by comparing the outputs of computer simulations with available experimental data. This comparison demonstrated that a physical leakage model incorporating three different conduction mechanisms - Poole-Frenkel, Fowler-Nordheim tunneling, and Schottky emission - provided the most accurate explanation of the leakage occurring in the FeCap stack. Subsequently, I studied the physical model in detail, highlighting how a restricted number of parameters profoundly influence the behavior of each leakage current. Quasi-static DC measurements were then conducted on existing devices with different ferroelectric thickness to validate the model. For each thickness, multiple measures were taken on different FeCaps, in order to obtain a statistically meaningful dataset for calibrating the leakage model. Considering that Poole-Frenkel was the dominant leakage mechanism, I extracted physically plausible ranges for the leakage parameters by calibrating the leakage model with experimental data. The results confirmed that Poole-Frenkel was clearly dominant, although the sample with the thinnest ferroelectric layer showed a current trend which deviated from the linear current-thickness trend seen in the other samples with thicker layers. This study provided a reliable foundation for further refinement of the model FeCaps in future research.

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Acronyms

BE Bottom Electrode

CDF Cumulative Distribution Function

CIM Compute-In-Memory

FeCap Ferroelectric Capacitor

FeRAM Ferroelectric RAM

FN Fowler-Nordheim

PF Poole-Frenkel

PUND Positive-Up Negative-Down

SE Schottky Emission

TE Top Electrode

Chapter 1

Introduction

This chapter introduces basic concepts regarding ferroelectric capacitors (FeCaps), neuromorphic computing, and their application within this novel computing paradigm. It also defines the concept of compact models and states their importance in analog circuit simulations.

1.1 A novel memory element

In the past few decades, a great deal of effort has been made in the area of memory storage to improve existing technologies, such as DRAM (volatile) and NAND flash (non-volatile). This resulted in novel memory types, one of the most promising being capacitor-type ferroelectric RAM (FeRAM). Its cell structure is similar to DRAM, employing a one-transistor one-capacitor *1T-1C* configuration. However, differently from the DRAM cell, the FeRAM employs a ferroelectric capacitor which, while being structurally similar to a conventional capacitor, employs a layer of ferroelectric material as the dielectric. The polarization of such materials can be changed by applying an external electric field and is preserved in time when external power is removed. Therefore, the FeCap acts as a non-volatile memory element.

Capacitor-type FeRAM has important advantages over other memory types, first of which being low power consumption. Other emergent memory technologies which exploit phenomena of resistance change, such as *Phase Change Memory* (*PCM*), *Resistive Switching Memory* (*RRAM*), and *Magnetoresistive Memory* (*MRAM*), need high currents to switch the resistance state[9]. On the other hand, in FeRAM, the write energy per bit needed to switch the polarization of the ferroelectric is considerably lower [1, 2]. FeRAM also exhibits extremely high endurancetypically beyond 10^9 cycles, around 10^{12} up to 10^{15} [3, 4], combined with fast switching speed. Commercial devices exhibit read/write speeds $< 50\,ns$ [5], however further scaling down to $\sim 2\,ns$ has been shown to be possible [6].

1.2 FeCaps and neuromorphic computing

Although important for conventional memory storage, FeCaps have also attracted attention for their potential in the field of *neuromorphic computing*.
Within this approach, hardware and software design is inspired by the brain, simulating its neural and synaptic processes to process information [10].

1.2.1 Basic neuron and synapse working principle

A typical neuromorphic circuit consists of a network of artificial neurons interconnected with synapses. The neuron, both biological and artificial, acts as the "decision site" of the network.

The inputs received by the neuron are integrated (summed), biologically depolarizing the neuron cell membrane [11]. When depolarization reaches a certain threshold an action potential is triggered and an output signal, called "spike", is sent. If the threshold is not reached, the integrated information conveyed by the inputs will gradually fade away, with the local potential accumulated diffusing along the nerve fibre and back out through the membrane [11]. Interestingly, the input and output signals will not have all the same strength when they reach the neuron. The signal strength of each input and output is modulated by structures called *synapses*, which enhance (*potentiation*) or hinder (*depression*) signal transmission. An artificial synapse can be implemented using devices capable of reversible and tuneable resistance change, e.g., *memristors*, to emulate potentiation and depression. A network of artificial neurons and synapses that convey information in the form of spikes is called *Spiking Neural Network* (SNN).

1.2.2 Advantages of neuromorphic computing and use cases

The recent interest in neuromorphic computing is backed by important advantages over conventional systems. Neuromorphic systems promise increased power efficiency over conventional systems because they are event-based, meaning that neurons and synapses activate only in response to other spiking neurons, while the rest of the system remains idle. Power consumption can be reduced even further using low-power devices, such as FeCaps. Neuromorphic systems can also help overcoming the *von Neumann bottleneck*. In the von Neumann architecture, the processing unit is separated from the memory and data transfer occurs via a limited number of buses, which causes a bottleneck that considerably slows computation. Neuromorphic systems solve this problem by employing *compute-in-memory* (CIM) architectures where data is processed with and stored within the network of neurons and synapses, lowering computational latency. Being brain-inspired, neuromorphic architectures have the potential to learn in real-time and to solve many different tasks in parallel, allowing them to adapt and complete tasks quickly. Although real world applications of neuromorphic architectures are still being investigated, there are several lines of research in the field of robotics, pattern recognition, and edge computing.

1.2.3 FeCaps in artificial neurons and synapses

FeCaps have been successfully used in artificial neurons as well as synapses.
In a recent work, Gibertini et al. [7] proposed a FeCap-based LIF (leaky integrate-and-fire) neuron. The schematic is shown in Figure 1.1 and comprises of three synaptic inputs (currents $I_1 - I_3$), a leaky output path (I_{leak}) which simulates membrane depotentiation, a refractory path (I_{rfr}) that emulates the refractory period of biological neurons, and comparator with a FeCap in the negative feedback loop.
The FeCap is progressively polarized as more and more input spikes are fed to the neuron. The charge accumulated in the FeCap leads to a voltage drop V_{fc}. When V_{fc} is equal to the reference voltage of the comparator, the neuron fires and the refractory path is activated. While in the refractory period, the inputs are discharged through the refractory path and do not reach the comparator. The refractory period is controlled by the refractory current I_{rfr}.

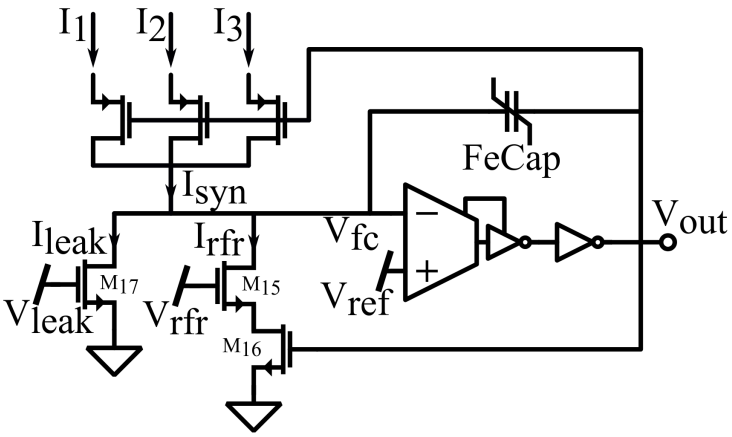


Figure 1.1: Schematic of the FeLIF neuron proposed by Gibertini et al., extracted from [7]. The three inputs currents I_{1-3} accumulate charge on the FeCap in parallel with the comparator. When the voltage drop over the FeCap equals V_{ref}, the neuron fires and the inputs are disconnected, while the refractory part is open and the FeCap is re-initialized. A leakage path has also been implemented.

Yu et al. [8] report FeCaps inside crossbar arrays for vector-matrix multiplication. As shown in Figure 1.2A, the first step of the computation consists in charging the FeCaps by raising the word-line voltage (the input vector of the multiplication), thus storing a charge in each capacitor. In this step the reference capacitors do not store any charge. Note that the matrix is represented by the FeCaps which have different capacitive weights. The second step is shown in Figure 1.2B, where along each bit-line (outputs) the charges are extracted and flow to a reference capacitor. While the positive charges are collected by the word-line inputs, the negative ones flow along the bit-lines accumulating on the reference capacitors. This creates a voltage drop over C_{Ref} which influences V_{out}. The more charges, the higher the output voltage of the bit-line. To sum up, in this case the FeCaps act as synapses with different weights and are used to process information.

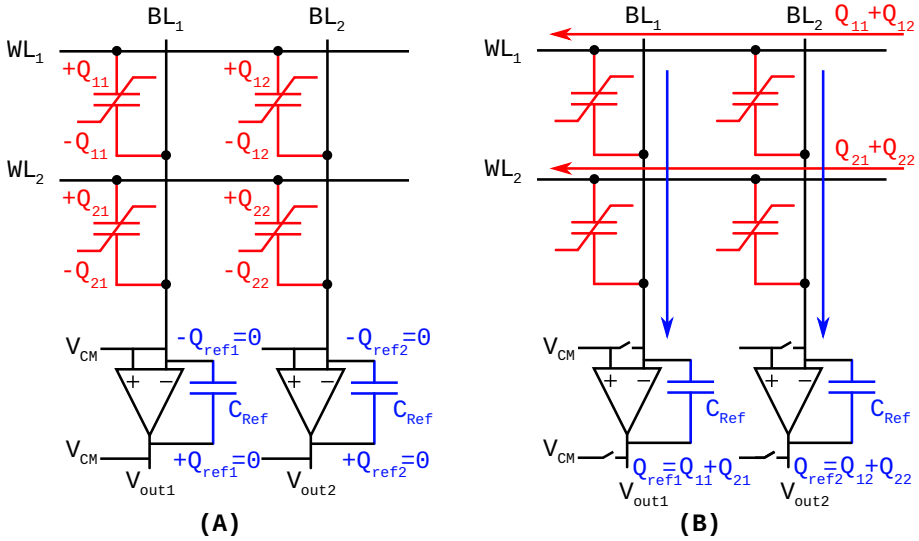


Figure 1.2: Equivalent circuit of the simplified 2×2 crossbar array as presented by Yu et al. **(A)** The circuit is programmed by raising the word-line voltage, storing charges inside the FeCaps. **(B)** The word-line voltage is turned off, and the negative charges are collected on the reference capacitors. The amount of charge influences the output voltage of each bit-line.

1.3 Compact models

A compact model is a mathematical description of the physical phenomena governing an electronic device. Compact models can be used in analog circuit simulations. The core of the compact model describes the essential physics of the device. The description provided by the core model is expanded by adding physical, geometry, structural effects, and leakage currents. The final compact model includes additional physical phenomena such as ambient temperature or layout effects[12]. Compact models are used in circuit simulation due to their low computational cost and high accuracy.

In order to be suitable for circuit simulations, a compact model must meet some important requirements. At the beginning of, or during the circuit simulation, it is possible that the voltages applied to the compact model will fall out of the operating voltage range intended for the real device the compact model emulates. Therefore, the compact model must be robust, working as intended even in unphysical operating conditions. Closely related to this aspect, the model must accurately simulate the behavior of the device in a wide range of measurements (e.g. DC, small signal AC, transient etc.). Since a compact model is experimentally calibrated to reproduce the behavior of a certain class of devices, it must be *general* as well, which means that the model must fit a certain class of devices with minimal fitting parameter variations. Finally, the mathematical formalism implemented in the compact model must be differentiable so that the simulator is able to solve the model using Newton iterations with minimal errors, which satisfy the error tolerances defined by users and in available commercial simulators.
Development of a compact model starts from a core where only the essential behavior is implemented. It is important to define some essential parameters and variables beforehand, which are extracted from literature (e.g. material parameters) and sample experimental data and devices (e.g. geometry, resistances, saturation currents and polarization). These parameters are then used in the equations that define the basic operating principle of the device. After the model has been calibrated, it is expanded and refined with additional physics and effects. After each major change, the model has to be compared with experimental data and, if needed, recalibrated. Finally, the model output is validated with additional sets of experimental data.

Chapter 2

Ferroelectric capacitors

This chapter discusses FeCaps based on hafnia-based ferroelectrics. The state-of-the-art of leakage modeling in FeCap compact models is presented, and the purpose of this work is illustrated in detail.

2.1 FeCap structure

Figure 2.1 shows the generic structure of a FeCap stack, which is similar to a traditional capacitor, but with a ferroelectric material instead of a conventional dielectric sandwiched between two metal electrodes, namely the bottom electrode (BE) and the top electrode (TE). When two different materials come into contact, they react chemically to form new compounds which create an interface layer. Therefore, possible TE and BE interfaces must be considered as part of the FeCap structure.

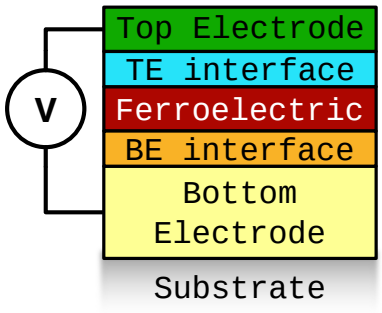


Figure 2.1: The generic structure of a FeCap stack, consisting of a ferroelectric layer sandwiched between top and bottom electrodes. The presence of parasitic interfaces at the BE/TE-ferroelectric interfaces has been considered.

2.1.1 Ferroelectric materials

Ferroelectrics are materials that exhibit spontaneous electrical polarization. In the crystalline structure of ferroelectrics, the center of positive and negative charges do not overlap, creating electrical dipoles. Clusters of dipoles with the same orientations are called domains, which can be aligned in a specific direction when a strong external electric field is applied [13, 14]. This results in a polarization hysteresis in the P-E or P-V domain (polarization-electric field or voltage). A FeCap can be operated either in current or voltage mode. Both methods create an external electric field in the ferroelectric layer, which is gradually increased to switch the polarization of the ferroelectric. For example, in current mode an external current I accumulates charges on the electrodes, which creates an electric field over the ferroelectric E (Fig. 2.3A). Initially, as the applied electric field increases, the polarization-field (P-E) characteristic is linear as highlighted by the black dashed curve in Figure 2.2A, with a slope depending on the linear capacitance of the ferroelectric C_{FE}. However, when the coercive field E_c is reached (green square in Figure 2.2A), the ferroelectric domains start to re-orient, i.e. *switch*, in the direction of the externally applied field. E_c is linked to the minimum energy necessary to switch the polarization of the majority of ferroelectric domains. The non-linear polarization of the ferroelectric attracts extra screening charges (lighter circles in

Figure 2.3B), which create an extra screening electric field E_{scr} which is added on the external field.

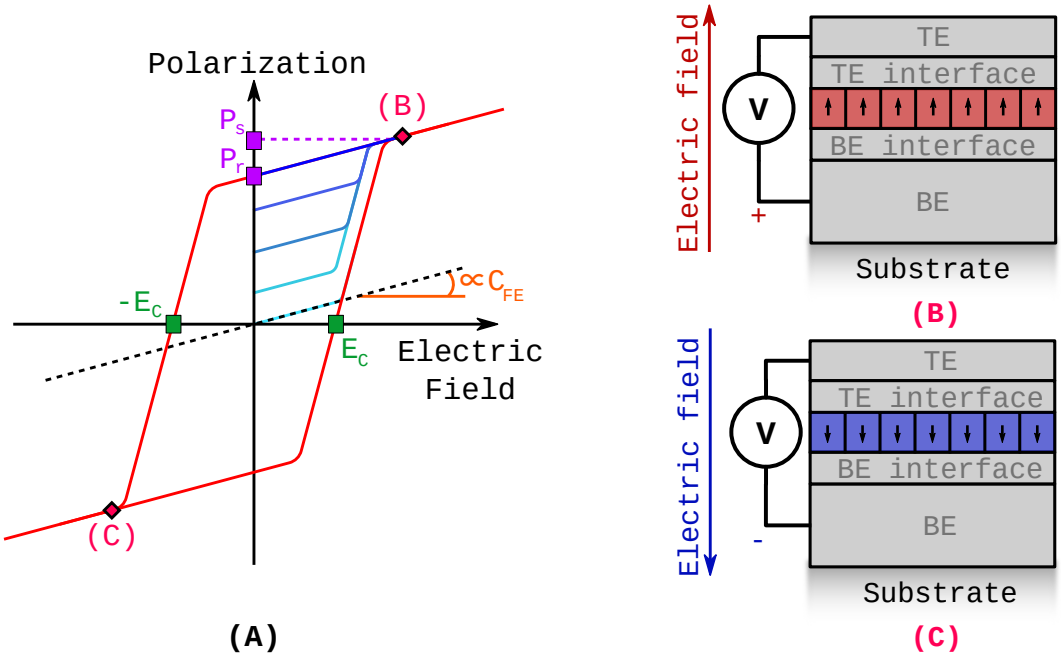


Figure 2.2: **(A)** Example of ferroelectric hysteresis plotted on the P-E plane, highlighting the saturation and remanent polarizations, the coercive field, and the slope of the linear part of the polarization curve as the linear ferroelectric capacitance. **(B)** UP and **(C)** DOWN configurations of the ferroelectric domains.

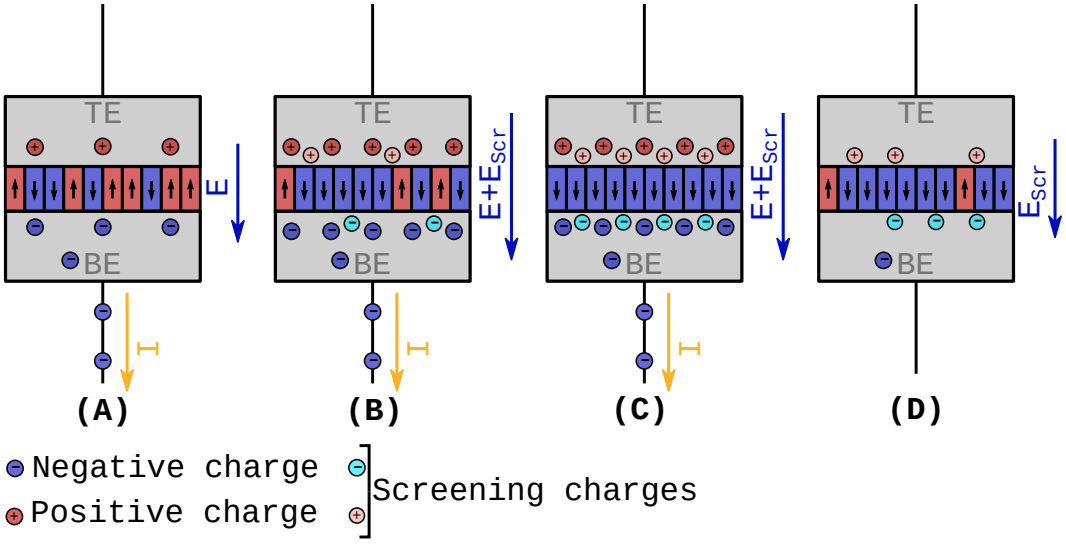


Figure 2.3: Scheme of the various phases of a FeCap operated in current mode: **(A)** Linear regime, no screening charges. **(B)** E_c is reached, switching and screening charges buildup start. **(C)** Saturation is reached. **(D)** The external current is shut off but most screening charges remain and stabilize the polarization to P_r.

When all the domains have switched, the polarization reaches the *saturation polarization* (P_s), highlighted by the magenta rhombus in Figure 2.2A. Notice, from Figure 2.3C, that at saturation even more screening charges are present. When the external field is switched off, the linear component of

the polarization discharges, while the *remanent polarization* P_r is stabilized by the screening charges accumulated on the electrodes (Figure 2.3D). The existence of a remanent polarization when no external field is applied creates the ferroelectric hysteresis. However, imperfect charge screening (also termed *imperfect compensation*) creates a depolarization field E_{dep}, which reduces P_r in time. It is also possible to store intermediate polarization states, as highlighted by the blue gradient, in which P_s and P_r lower than the maximum values possible for a certain device. The behavior of a FeCap is investigated, i.e. characterized, with different measures including PUND (Positive-Up Negative-Down), kinetics, DC, retention, endurance and their variants.
Although ferroelectrics share the same basic hysteretic behavior, conventional perovskite ferroelectrics, such as $Pb(Zr, Ti)O_3$ (lead zirconium titanate or PZT) or $BaTiO_3$ (barium titanate or BTO) exhibited limited compatibility with complementary-MOS CMOS technology, scalability issues and degraded performance for low thicknesses ($< 100\,nm$). In 2011, ferroelectricity was discovered in Si-doped HfO_2 (hafnium dioxide) [15], and shortly after in HZO as well. Differently from perovskite ferroelectrics, in which polarization switching occurs via cation displacement, in hafnia-based ferroelectrics the movement of oxygen anions causes switching [16]. However, HfO_2 has multiple phases, but the non-centrosymmetric orthorhombic phase $Pca2_1$ is regarded as the primary source of ferroelectricity [17]. Hafnia-based ferroelectrics improve on the properties of perovskites ferroelectrics. Firstly, HfO_2 is important for device scaling due to the very high permittivity (~ 30 [16]) and higher resilience to degradation when deposited in thin ($< 10\,nm$) films. Moreover, hafnia-based ferroelectrics have a higher coercive field than perovskite ferroelectrics, guaranteeing a better separation of the polarization states in thin films. Notably, hafnia-based ferroelectrics exhibit full compatibility with CMOS technology.

2.1.2 Electrodes and interfaces

The materials used for the electrodes influence the behavior of the FeCap. This influence can spur directly from the electrodes themselves, due to mechanical stress, or indirectly due to the formation of interface layers [15]. Some popular electrode materials encompass metal nitrides like TiN and TaN, pure metals like W, Pt, Ru, and Ir, and even metal oxides like IrO_2 and RuO_2[18]. The thermal expansion coefficient mismatch between HfO_2 (or HZO) and the electrode is the primary source of mechanical stress, either compressive or tensile, and deeply affects phase evolution [15, 18], which in turn influences P_r and P_s. TiN induces high tensile stress which promotes the tetragonal → orthogonal (t → o) phase transition and stabilizes the ferroelectric o-phase. The thicker the TiN layer, the higher the ferroelectric phase fraction gets [15].
The formation of interface layers is influenced by the materials involved and the fabrication process employed, which may determine an asymmetry in the top and bottom interfaces even if the same material is used for both electrodes. Due to the oxidation the BE undergoes before HZO deposition, if a TiN BE is used, a complete layer of TiO_2 forms. On the contrary, at the TE where TiN does not oxidize before deposition, the latter scavenges oxygen from HZO, creating a layer of TiO_xN_y. This interface has been shown to be thinner than 1 nm [18] hence negligible with respect to the FeCap stack. Therefore the main focus is on the modeling of the leakage current at the BE.

2.1.3 DC measurement

In the DC or quasi-static measurement, a forward and backward voltage sweeps are applied to a device-under-test (DUT) to measure the quasi-static current. The voltage sweep is typically linear and follows the staircase behavior illustrated in Figure 2.4A, where the settle time (t_{settle}) represents the delay elapsed between the beginning of each voltage step and the start of the measurement. The settle time must be long enough to filter out transient currents caused by sudden capacitive charging when the voltage is stepped to a new value. The measurement is performed during the integration time (t_{int}), in which various current samples are measured, and an average current is

obtained dividing by the integration time. Thus, the duration of each voltage step is approximately $t_{settle} + t_{int}$, not including the rise/fall time between two consecutive steps.

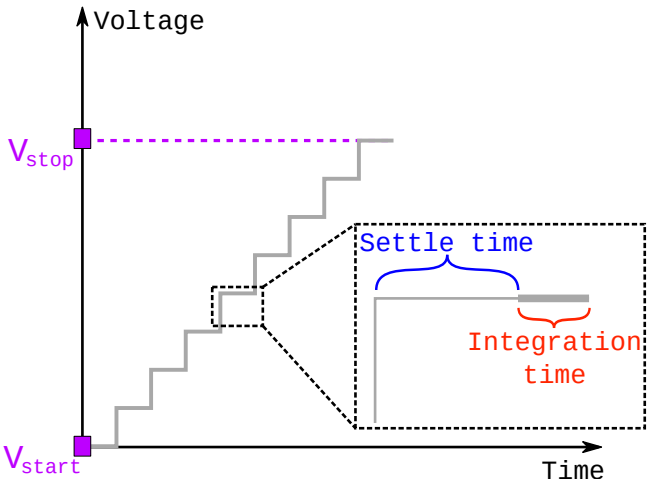


Figure 2.4: Example of DC signal trail with starting and stop voltages V_{start} and V_{stop}. The voltage is applied step by step, producing a staircase, where the duration of each step is defined by the sum of the settle and integration times.

2.1.4 PUND measurement

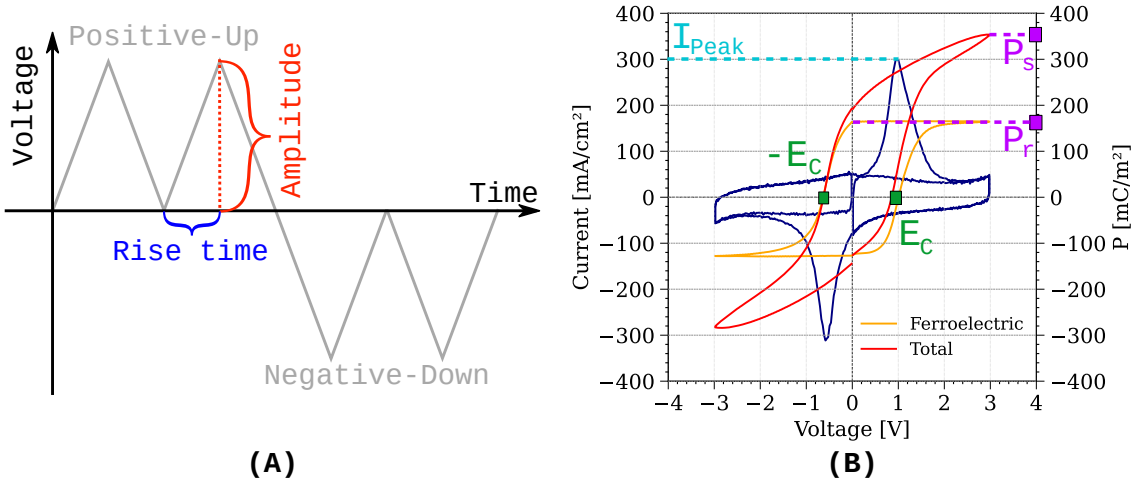


Figure 2.5: **(A)** Example of signal trail for one PUND cycle, with definite amplitude and rise time. **(B)** Sample experimental PUND data obtained from one of the available FeCaps with 6.45 nm thick ferroelectric. The blue curve is the switching current profile (left axis), while the red and orange hystereses represent the total and ferroelectric only polarization in case leakage is removed.

A single Positive-Up Negative-Down (PUND) cycle (Figure 2.5A) consists of four triangular voltage pulses, two UP and two DOWN, defined by a maximum voltage amplitude and the rise and fall time, which in this case are equal. The PUND allows to visualize the switching current peaks (blue curves in Figure 2.5B), resulting from the sudden movement of screening charges toward (or away, depending on the polarity) the capacitor plates during polarization switching. Since the

screening charge corresponds to the polarized dipole charge inside the ferroelectric, by integrating the switching current in time one obtains the P-V characteristic, showing the polarization hysteresis. In Figure 2.5B it is possible to notice that there are two different current curves for each voltage pulse pair, one corresponding to an approximately constant current value while the other exhibits the peaks. The former represents the capacitive leakage current plus other leakage phenomena that become relevant at higher voltage. These leakage components are decoupled from the entire switching current profile with the first pulse of each PUND pair. In simpler terms, the ferroelectric switches only during the first pulse, while the second reveals only the capacitive leakage current. The red hysteresis is obtained from integrating the switching current profile as is, while the orange hysteresis is obtained when the leakage component of the current is subtracted from the switching profile before integration. This second hysteresis considers only ferroelectric switching, and it is useful to obtain P_r. The PUND is particularly important to extract data regarding P_r and P_s, the coercive voltage and field, value of the switching current peak and observe possible E_c/V_c asymmetries that can be caused by *imprint*, and detect whether the device is past *wake-up*.

2.1.5 Switching kinetics measurement

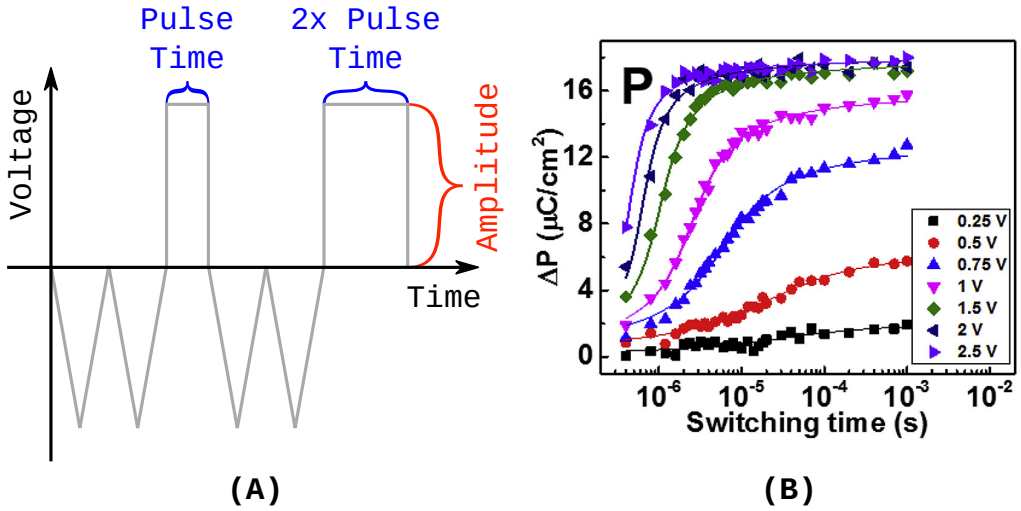


Figure 2.6: **(A)** Example of signal trail for kinetics measurement. **(B)** Switching kinetics curves extracted from [19], obtained from a $TiN - HfO_2 - TiN$ (bottom and top electrode materials are the same) FeCap stack with 8 nm thick HfO_2 after 10^3 switching cycles.

The measurement of the switching kinetics is used to visualize the polarization of the FeCap in time, in order to study its switching behavior. As shown in Figure 2.6A, the pulse sequence usually consists of *set* square voltage pulses of increasing duration separated by triangular *reset* pulses of opposite sign (half a PUND cycle). The set pulses, executed for different voltage amplitudes, polarize the capacitor to a certain degree depending on their duration - longer pulse implies higher polarization. Their duration is increased with a defined time step. The triangular pulses reset the polarization to the initial state (opposite polarization). If the set pulses are positive, then the reset pulses, and thus the initial polarization state, will be negative. This reset process produces a switching current which constitutes the output of the kinetics. Measurements are performed by capturing this switching current during the reset pulses, since their higher duration allows for easier data acquisition. Finally, the output current is integrated in time and polarization data points are produced.

2.2 Leakage modeling state-of-the-art in FeCaps

Leakage constitutes an important part of FeCap compact models for circuit simulations. The table below provides an overview of the state-of-the-art of leakage modeling:

Source	Model	Leakage model
Pešić et al.[20]	TCAD FeCap	Multiphonon Trap-assisted tunneling
Pešić et al.[20]	LK Multigrain FeCap	Resistive
Kim et al.[21]	Multidomain Preisach FeCap	Fowler-Nordheim tunneling
Asapu et al.[22]	LK FeCap	Tunneling (exponential)
Pintilie et al.[23]	Simplified FeCap	Thermionic emission

Table 2.1: Leakage models implemented in various FeCap compact models.

In their review, Pešić et al.[20] cite two different FeCap compact models. The first FeCap model is built using the Sentaurus device TCAD software, and models leakage via a Nasyrov-type, multiphonon-mediated, trap-assisted tunneling (TAT). This conduction model assumes a high density of traps, and with small trap-to-trap separation charge transport proceeds by phonon-assisted tunneling from trap to trap, without electrons emitted in the conduction band[24]. Much simpler is the model employed in the multigrain FeCap compact model where ferroelectric switching is modeled with the Landau-Khalatnikov formalism[25]. Each ferroelectric grain is modeled with a resistor and nonlinear capacitor in series, and the overall ferroelectric layer consists of a parallel of N ferroelectric grains, a linear capacitor lumping together the non ferroelectric grains, and a resistor modeling leakage. Therefore, the leakage current is simply calculated via Ohm's law, knowing the voltage drop over the ferroelectric layer and the leakage resistance value.
Kim et al.[21] follow a different approach, employing a multidomain Preisach model switching model. In the Preisach model, the ferroelectric film is divided in N units with different coercive voltages (or fields), where the coercive voltage defines the voltage at which the ferroelectric switches. Therefore, the polarization hysteresis is given by the superposition of N simpler rectangular hystereses, each of which generated by a single unit[26]. Leakage is modeled with the Fowler-Nordheim tunneling model. This model describes tunneling of charge carriers through the field-distorted triangular barrier of a dielectric, of height ϕ_B. Fowler-Nordheim is particularly important for film thicknesses below 10 nm and high electric fields [27].
Asapu et al.[22] employ a Landau-Khalatnikov based model similar to the one by Pešić et al. [20], but without a multigrain approach. Leakage is considered to be caused by charge tunneling, where the nonlinear tunnel resistance is modeled with an exponential, diode-like equation, calibrated with a pre-exponential tunnel parameter I_0.
Pintilie et al.[23] focus more on leakage in a simplified FeCap model in which the polarization hysteresis is assumed ideal and rectangular. The dominant leakage mechanism is thermionic or Schottky emission, where electrons are thermally-activated and injected over the energy barrier into the conduction band of the dielectric [27].

2.3 Purpose of this work

This work focuses on the implementation of physical conduction mechanisms to model leakage through the FeCap stack. Starting from a resistive-based implementation of the leakage, various possible causes of leakage at the nanoscale have been investigated, and physical conduction mechanisms have been implemented, transitioning to a more *physics-based* device model. Successively, the leakage model has been calibrated and validated by comparing its output with several DC measurements performed on available samples. After the calibration phase, the conduction mechanisms and their role in the device have been discussed.

Chapter 3

Compact modeling

This chapter introduces the characteristics of the FeCap samples available. Then, it focuses on compact modeling by describing the FeCap compact model used, and the implementation of a physical leakage model for the FeCap stack. In particular, the physical leakage model has been studied exploiting DC simulations run over the FeCap stack, identifying the dominant conduction mechanisms.

3.1 Available devices

The leakage model has been calibrated and fitted using sample experimental data obtained from already-fabricated FeCaps. As illustrated in Figure 3.1, these devices consist of a W/HZO/TiN stack (TE/FE/BE) with an area of $25 \times 25\mu m^2$ ($625 \times 10^{-12}\,m^2$), and different ferroelectric thicknesses of 6.45/8.37/10.63 nm referred to as device classes 30/29/28 respectively. As mentioned earlier in Subsection 2.1.2, the behavior of a FeCap is also influenced by the presence of interface layers. Drawing from various studies [18, 28], the presence of a TiO_2 BE interface has been assumed, which forms due to the exposure of TiN to oxygen before HZO deposition. Szyjka et al. [28] also remark that the thickness of TiO_2 saturates to a maximum of $3.5 - 4$ nm. Concerning the TE WO_x interface, a study [18] shows that it is thinner than 1 nm, hence negligible with respect to the overall FeCap stack, and has not been reported in Figure 3.1. However, if W were to be used as BE, the WO_x would have not been negligible, although on average thinner than the TiO_2 interface forming with a TiN BE.

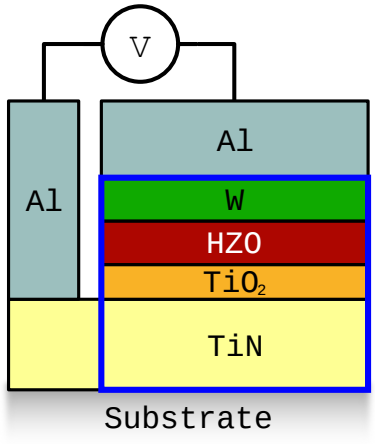


Figure 3.1: Cross section of the stack of the available FeCaps, consisting of a TiN bottom electrode, TiO_2 BE/FE interface layer, HZO (hafnium-zirconium oxide) ferroelectric layer, W top electrode, and Al contacts connecting to the bottom and top electrodes.

3.2 FeCap compact model

Figure 3.2 illustrates the equivalent circuit of the FeCap compact model used in this work. The model consists of three layers, from bottom to top - the BE interface, the ferroelectric layer, and the TE depletion capacitance.

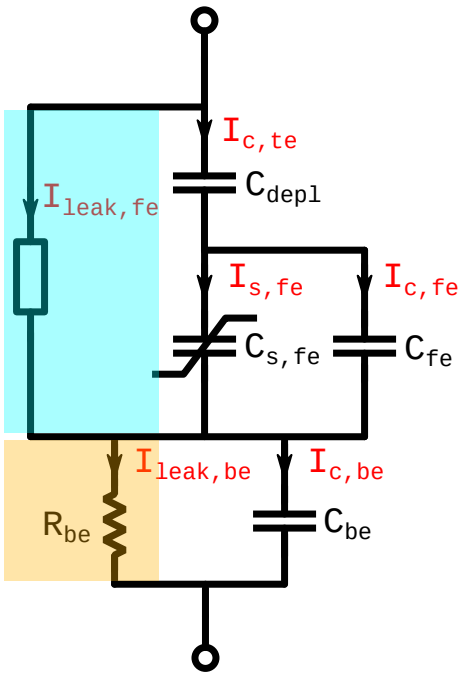


Figure 3.2: Equivalent circuit of the FeCap compact model used, extracted and modified from [29]. It consists of three layers. From bottom to top, the R_{be}/C_{be} parallel modeling the BE interface, the ferroelectric layer comprising of linear and non linear capacitances C_{fe} and $C_{s,fe}$ respectively and an element modeling leakage $I_{leak,fe}$, and the TE depletion capacitance C_{depl} with the leakage $I_{leak,fe}$ in parallel.

The BE interface is modeled with an RC parallel. The bottom electrode resistance R_{be} models the leakage current through the interface $I_{leak,be}$. The user defines the resistivity ρ_{be} and thicknesses t_{be}, from which the resistances are automatically calculated. Instead, the capacitance C_{be} models the linear capacitive behavior of the dielectric interface, and it is used to calculate the capacitive displacement current $I_{c,be}$. The ferroelectric layer is modeled with two capacitances and a leakage element in parallel. Similarly to the interface, the linear capacitance C_{fe} models the linear capacitive behavior of the ferroelectric and the displacement current $I_{c,fe}$, while the non-linear capacitance $C_{s,fe}$ models the non-linear ferroelectric switching process. Polarization switching is modeled with the Landau double-well potential formalism, in which the two possible UP and DOWN polarization states correspond to the two potential minima. The polarization evolution in time is calculated with the following equation:

$$\frac{dp}{dt} = k_{\downarrow}(1-p) - k_{\uparrow}p \tag{3.1}$$

Where p is the state variable that describes the probability of the system to be in the UP polarization state, while $k_{\downarrow/\uparrow}$ are the DOWN/UP transition rates, characterizing how frequently the domains switch in the DOWN or UP direction. The quickest transition between UP and DOWN has the highest transition rate ($1/t_{transition}$) and it is thermodynamically favorite. The switching current $I_{s,fe}$ is simply calculated as:

$$I_{s,fe} = \frac{dP}{dt} = \frac{d(2P_s p)}{dt} \tag{3.2}$$

Where P_s is the saturation polarization, and p is the polarization state variable.
The leakage current through the ferroelectric $I_{leak,fe}$ is visually represented by the rectangular element in parallel, and is calculated with a symmetric (non-rectifying), diode-like exponential equation:

$$I_{leak,fe} = \begin{cases} +(I_{0,fe} + I_{0,fe_{MC}}) \cdot \left\{ \exp\left(+\frac{V_{fe}}{V_t}\right) - 1 \right\} & V_{FE} \geqslant 0 \\ -(I_{0,fe} + I_{0,fe_{MC}}) \cdot \left\{ \exp\left(-\frac{V_{fe}}{V_t}\right) - 1 \right\} & V_{FE} < 0 \end{cases} \tag{3.3}$$

Where $I_{0,fe}$ is the pre-exponential current density parameter, $I_{0,fe_{MC}}$ is the Monte Carlo generated pre-exponential parameter in case Monte Carlo simulations are run to simulate device-to-device variability, V_{FE} is the voltage drop in the ferroelectric, and $V_t = 0.32$ is a fitting parameter. Finally, the depletion capacitance C_{depl} models the non-ideal depletion charge distribution inside the TE metal electrode, at the electrode-ferroelectric interface. Indeed, the distribution of charges in the metal occupies a finite thickness[30] as visualized in the green distribution in Figure 3.3, creating a depletion capacitance that depends on the depletion charge density and polarization direction of the ferroelectric. It has been assumed that the depletion charge does not interact with the leakage current flow, thus the ferroelectric leakage element $I_{leak,fe}$ is also in parallel with the depletion capacitance. Therefore, the ferroelectric leakage current depends on the sum of ferroelectric and depletion voltage drops $V_{FE} + V_{depl}$.

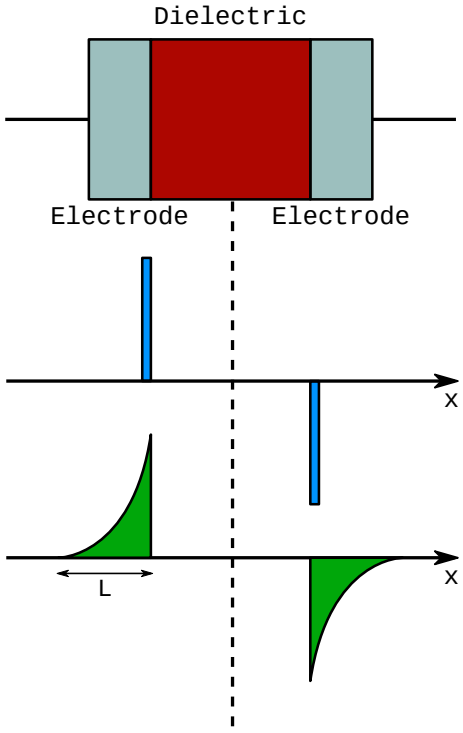


Figure 3.3: Schematic representation of the distribution of the depletion charge at the metal-dielectric interface. The ideal distribution represented with the cyan rectangles does not occupy any space along the x axis, while the non-ideal one in green occupies a finite length L.

3.3 Modelling leakage in the FeCap stack

3.3.1 Leakage models

The first model consists of the leakage mechanisms already implemented in the compact model. This leakage model applies a resistive model to the interface similar to the one implemented for the ferroelectric in the multi-grain model in [20], while leakage in the ferroelectric is modeled exponentially, similarly to [22]. As mentioned before, ferroelectric leakage is modeled with a symmetric, diode-like exponential current (eq. 3.3). The values of the pre-exponential current density factor I_0 are in the range of $10^{-5} - 10^{-3}\,\mathrm{A/m^2}$. Conversely, the BE interface leakage current is computed via a resistance R_{be} (Ohm's law):

$$J_{be} = \frac{V_{be}}{\rho_{be} \cdot t_{be}} \tag{3.4}$$

Where V_{be} is the voltage drop over the BE interface, ρ_{be} is the resistivity, and t_{be} is the thickness of the interface layer. For this reason, this model has been referred to as *resistive*. As discussed in Subsection 3.1, a TiO_2 BE interface with maximum thickness of 3.5 nm has been assumed. Regarding the resistivity of titanium dioxide, typical values for TiO_2 thin films fall in the $10^1 - 10^3\ \cdot$ m range for amorphous films and increasing with lower thickness [31]. However, higher values are possible for non-doped, stoichiometric TiO_2, around $10^{15}\ \cdot$ m [32]. Since the formation of the interface is unintentional and uncontrolled, a defect rich and non-stoichiometric TiO_2 layer has been assumed,

imposing a range of values for the resistivity slightly higher than in deposited amorphous films, but still lower than pure stoichiometric ones, around $10^3 - 10^8$ $\cdot$ m.
In the second leakage model, termed *exponential*, the exponential leakage current, described by Equation 3.3, has also been implemented for the BE interface, defining a different pre-exponential parameter $I_{0_{be}}$ and considering the voltage drop V_{tbe} on the interface layer only.
In the third and final model, named *physical*, the interface and ferroelectric leakage currents are no longer modeled with a single exponential equation, but with three leakage mechanism relevant at the nanoscale acting together. This approach is novel with respect to the state-of-the-art of leakage modeling presented in Section 2.2, where the leakage current is modeled with only one conduction mechanism, like Fowler-Nordheim tunneling [21] or Thermionic or Schottky emission [23]. The mechanisms implemented in the physical model are Fowler-Nordhem (FN) tunneling, Poole-Frenkel (PF) conduction, and Schottky emission (SE). The relevant mathematical formalism has been extracted from a study by Lim et al. [27] which surveys several conduction mechanisms that are relevant at the nanoscale. Fowler-Nordheim tunneling considers tunneling of charges through the energy barrier of an insulator that has been distorted by an external electric field, i.e. through a triangular energy barrier as shown in Figure 3.4. As mentioned in Section 2.2, it becomes relevant for dielectric thicknesses under 10 nm and for high electric fields, and it is modeled with the following equation:

$$J_{FN} = AE^2 \exp\left(-\frac{B}{E}\right) \tag{3.5}$$

$$A = \frac{1}{m_{eff}} \frac{q^3}{8\pi h \phi_B},\ B = \frac{8\pi}{3}\left(2\frac{m_0 m_{eff}}{h^2}\right)^{1/2} \frac{\phi_B^{3/2}}{q} \tag{3.6}$$

Where ϕ_B is the energy barrier height in the dielectric (here expressed in J and not in eV), m_0 and

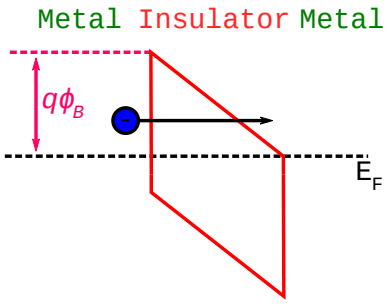


Figure 3.4: Schematic representation of Fowler-Nordheim tunneling conduction through the triangular energy barrier of a dielectric, with height ϕ_B measured from the fermi level E_F.

m_{eff} are the electron mass and effective mass respectively, h is the Planck's constant, and E is the electric field in the dielectric.

Concerning Poole-Frenkel, as highlighted in Figure 3.5A it models the transport of carriers in the conduction band via trap sites present in the insulator, and follows the relation below:

$$J_{PF} = q\mu N_C E \cdot \exp\left[\frac{-q\left(\phi_T - \sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_r}}\right)}{kT}\right] \tag{3.7}$$

Where μ is the electronic drift mobility, N_C is the density of states in the conduction band, ϕ_T is the trap depth, k is the Boltzmann's constant, and T is the temperature.
Finally, as evident from Figure 3.5B Schottky emission refers to the phenomenon of thermionic emission, occurring when thermally activated electrons "jump" over the dielectric energy barrier. The equation below models this mechanism:

$$J_{SE} = \frac{4\pi q m_0 m_{eff}(kT)^2}{h^3} \cdot \exp\left[\frac{-q\left(\phi_B - \sqrt{\frac{qE}{4\pi\varepsilon_0\varepsilon_r}}\right)}{kT}\right] \tag{3.8}$$

With ϕ_B being the junction barrier height in eV. In this study, I assumed the SE and FN junction energy barriers to be essentially the same.

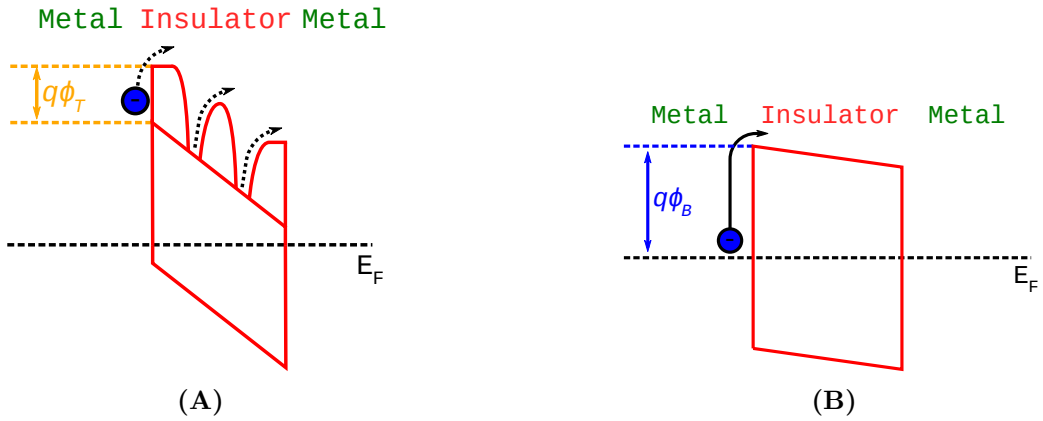


Figure 3.5: **(A)** Schematic representation of Poole-Frenkel conduction via traps present in the conduction band. **(B)** Schematic representation of Schottky emission conduction, where charges can overcome the energy barrier of a dielectric if their energy is equal or greater than the barrier height ϕ_B measured from the fermi level E_F.

The Tables below summarizes plausible ranges of leakage parameters extracted from literature:

Parameter	**Material phase**				
	Monoclinic	Tetragonal	Ferroelectric	Orthogonal	Cubic
ε_{r,HfO_2}[33]	24.1	48.7	27	-	-
$\varepsilon_{r,HZO}$[33]	22.4	45.9	29.1	22.7	36

Table 3.1: Relative permittivity of the most important phases of HfO_2 and HZO.

Parameter	Description	Unit	HZO	TiO_2
ε_r[33, 34]	Relative permittivity	1	$25-35$	$40-100$
m_{eff}[35–37]	Effective mass	1	$0.11-0.12$	$0.54-5.0$
ϕ_B[1]	Energy barrier	eV	$1.95-2.15$	$0.65-1.35$
ϕ_T[38, 39]	Trap depth	eV	$0.7 \div 6$	-
t[18]	Layer thickness	nm	$6 \div 10$	$0.5-4$
μ[2]	Electronic drift mobility	$m^2\,V^{-1}\,s^{-1}$	$1 \div 15 \cdot 10^{-4}$	-
N_C[2]	Conduction band density of states	m^{-3}	$\sim 1 \times 10^{24}$	-

Table 3.2: Plausible ranges of leakage parameters extracted from literature.

The values for the energy barrier ϕ_B have been extracted from the band diagram of the stack featured in Figure 3.6, computed by combining the data of several studies [40–44]:

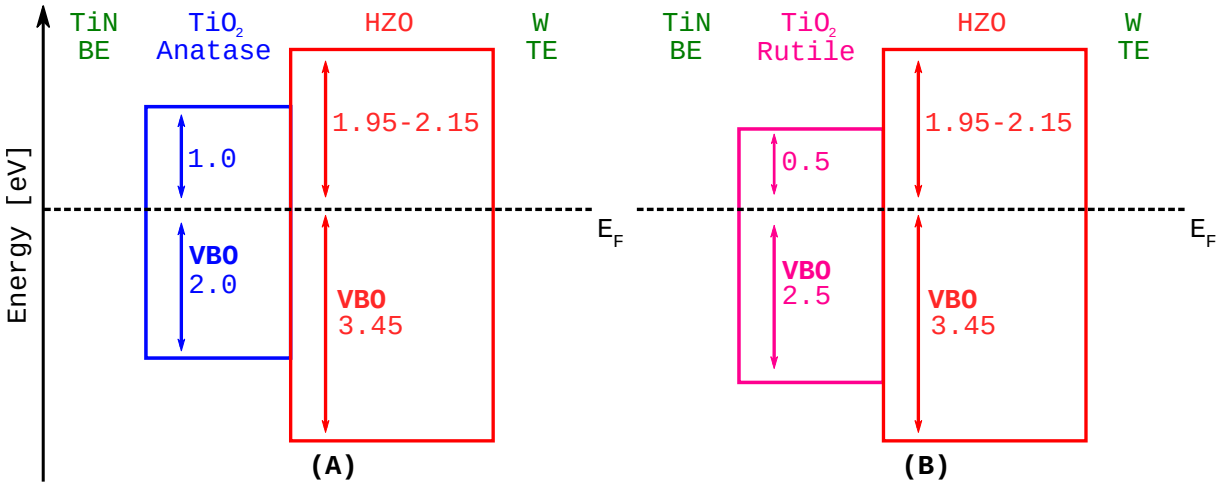


Figure 3.6: Band diagram of the FeCap stack for different phases of TiO_2. **(A)** Shows the case of anatase TiO_2, which presents a higher energy barrier than **(B)** rutile TiO_2[40, 41]. The barrier height of the HZO layer can vary based on Hf content (higher content implies wider bandgap[42], here considered $5.4-5.6\,eV$[43, 44]).

The mathematical formalism concerning the leakage mechanisms has been implemented in Python in order to compare the behavior of these currents in the ferroelectric and the interfaces. Figure 3.7 compares the *intervals* of each leakage current over voltage and thickness of the material. Each interval is obtained by changing a critical parameter of each current, i.e. a parameter whose variation greatly influences the current, while other parameters such as $\varepsilon_r = 35$, area $A = 625 \times 10^{-12}\,m^2$, $m_{eff} = 0.4$, $\mu = 15 \times 10^{-4}\ m^2\,V^{-1}\,s^{-1}$, and $N_C = 10^{24}\,m^{-3}$ remain constant and refer to the ferroelectric HZO. When plotting over voltage, the thickness has been fixed to $5\,nm$, while when varying thickness the voltage is equal to $1\,V$. Comparing both figures, it is evident that FN dominates at voltages higher than $1 \div 1.5\,V$ and thicknesses below $5-6\,nm$ and is thus ideal for thinner layers. PF stays relevant even for thicker dielectrics and grows rapidly even below $1\,V$, best fitting thicker ferroelectrics. Notice that the diode current is a good compromise between FN and PF, growing rapidly at low voltages and thicknesses, but remaining important for thicker materials and increasing steadily at high voltages, although not as steep as FN. The linear resistive current dominates

[1] Please refer to the band diagram of the FeCap stack.

[2] Since HZO is an oxide, the is a lack of studies regarding its transport and electronic properties. Therefore, a low mobility has been assumed due to the low conductivity of the ferroelectric, while the tentative value N_C is a standard/average one. Both can be treated as fitting parameters.

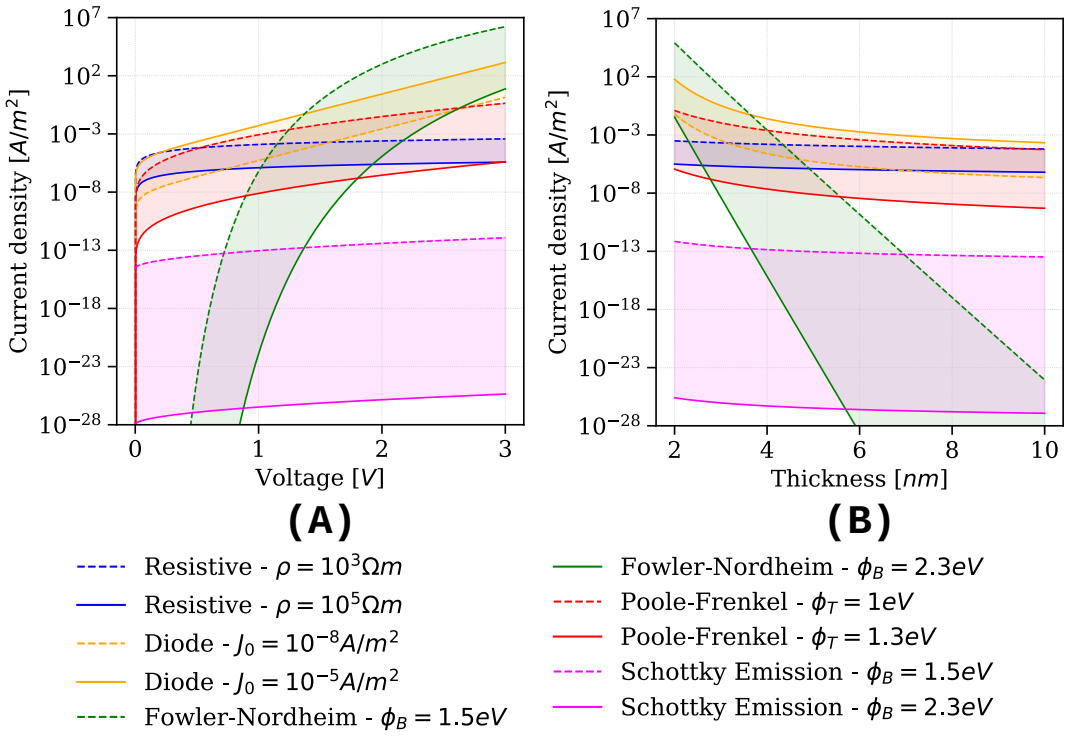


Figure 3.7: Comparison of the behavior of various leakage currents in the ferroelectric over **(A)** voltage with ferroelectric thickness fixed to 5 nm, and over **(B)** thickness with voltage fixed to 1 V. The variability of each current has been obtained by plotting corner cases for each current varying a critical parameter, such as the resistivity for the resistive, pre-exponential parameter I_0 for the exponential, barrier height ϕ_B for Schottky emission and Fowler-Nordheim tunneling, and trap depth for Poole-Frenkel.

only in the range $0 \div 0.5$ V and for higher thicknesses, where quantum conduction phenomena fade away. Finally, SE is negligible with respect to the other current components.

3.3.2 Implementation and fitting

In order to choose the model that best fits available PUND and switching kinetics experimental data, the three leakage models have been implemented in the FeCap compact model, running PUND and switching kinetics simulations. The benchmark circuit used to simulate the FeCap is shown in Figure 3.8, consisting of the FeCap, a series resistance $R_s = 50$ modeling the cables and instrumentation used for measurement, two signal generators to create the pulse trail for PUND and kinetics, and a DC source providing a baseline voltage $V_{ac} = 0$ V for the AC signals. In order to match the experimental data reported in Figures 3.9A and 3.9B, all PUND measurements have been simulated with an amplitude of 3 V and a pulse width of 1 ms (1 kHz frequency), hence with a 4 ms PUND cycle duration. The switching kinetics has been simulated for different voltage amplitudes, i.e. 0.5/1.0/1.5/2.0 V, and in the $10^{-12} \div 10^{-3}$ s time range. However, only the time window corresponding to the available experimental data, spanning from 1 μs to 1 ms, has been considered. As an arbitrary choice, device class 29 (8.37 nm thick ferroelectric) has been chosen to calibrate the PUND and kinetics fitting parameters. Table 3.3 and 3.4 illustrate the fitting parameters constant for all simulations and specific for each simulation or leakage model, respectively.

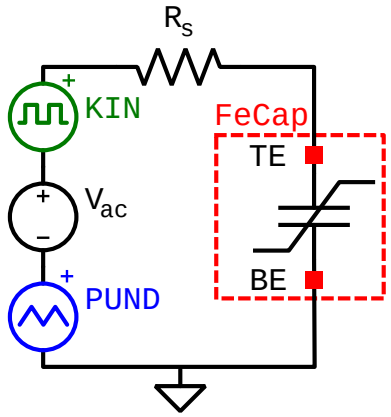
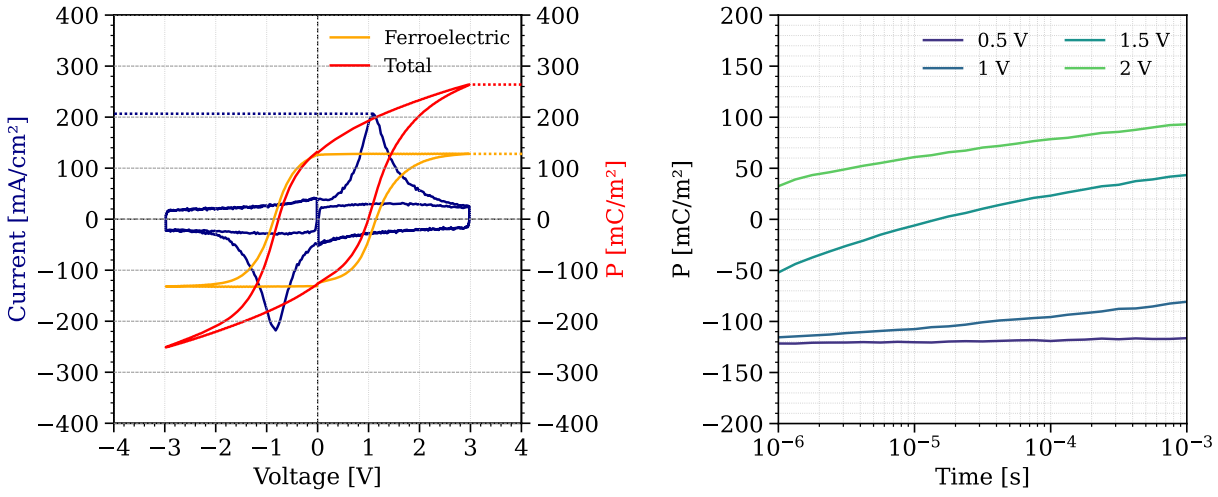


Figure 3.8: Equivalent benchmark circuit for the simulation of the FeCap compact model. The circuit consists of five elements in series - the FeCap, a series resistance modeling the cables and instrumentation used for measurement, a voltage generator (KIN) used to create the switching kinetics pulse trail, another voltage generator for the PUND pulse trail, and a DC source providing a baseline voltage for the AC signals.



(A) **(B)**

Figure 3.9: **(A)** Sample PUND data extracted from a FeCap with $t_{fe} = 8.37\,\text{nm}$ (class 29), illustrating the switching current profile in blue, and the polarization hysteresis with and without the capacitive displacement contribution, red and orange curves respectively. **(B)** Sample switching kinetics curves at four voltages 0.5/1.0/1.5/2.0 eV and in the $10^{-6} - 10^{-3}$ s time range for the same device with $t_{fe} = 8.37\,\text{nm}$ (class 29).

Parameter	Description	Unit	Value	
			PUND	Kinetics
V	Simulation voltage	V	3	0.5/1.0/1.5/2.0
T	Temperature	K	300	-
A	Device Area	m^2	$625 \cdot 10^{-12}$	-
$\varepsilon_{r_{fe}}$[3]	FE relative permittivity	1	35	-
t_{fe}	Ferroelectric thickness	nm	10.63/8.37/6.45	-
P_s	Saturation polarization	mC/m^2	110/125/145	170/125/145
W_b	Switching energy barrier	eV	1	-
d_e	Electric field action distance	nm	5	-
ε_{depl}	Polarizability of depletion layer	1	3.6	-
N_{depl}	Carrier density in depletion layer	m^{-3}	1.4×10^{26}	-

Table 3.3: Fitting parameters that remain constant for all leakage models. The switching kinetics is measured at four different voltages, hence the presence of multiple voltages. Furthermore, the saturation polarization is different for each ferroelectric thickness, thus the first value, 110 for the PUND and 170 in the switching kinetics, refers to devices with 10.63 nm thick ferroelectric, 125 to 8.37 nm, and 145 to 6.45 nm.

Parameter	Description	Unit	Value			
			Resistive		Exponential	Physical
			PUND	KIN	PUND & KIN	PUND & KIN
$\varepsilon_{r_{be}}$	BE relative permittivity	1	42.7	-	100	100
t_{be}	BE thickness	nm	2.5	-	2	1.5
ρ_{be}	BE resistivity	$\Omega \cdot m$	3.125×10^5	1×10^8	$\times$	$\times$
$I_{0,fe}$	FE pre-exponential factor	A/m^2	1×10^{-4}	-	1×10^{-4}	$\times$
$I_{0,be}$	BE pre-exponential factor	A/m^2	$\times$	$\times$	1×10^{-6}	$\times$
$\phi_{B,int}$	Interface energy barrier	eV	$\times$	$\times$	$\times$	0.8
ϕ_{B}	FE energy barrier	eV	$\times$	$\times$	$\times$	2.3
m_{eff}	FE effective mass	1	$\times$	$\times$	$\times$	0.4
$m_{eff,int}$	Interface effective mass	1	$\times$	$\times$	$\times$	1
ϕ_t	Trap depth	eV	$\times$	$\times$	$\times$	1
μ	Electron mobility	$m^2\,V^{-1}\,s^{-1}$	$\times$	$\times$	$\times$	15×10^{-4}
N_c	CB density of states	m^{-3}	$\times$	$\times$	$\times$	1×10^{24}

Table 3.4: Leakage parameters used for the fitting of each leakage model. The symbol "-" means that the parameter has not been changed, while $\times$ means that the parameters is not used in the leakage model.

Figures 3.10A and 3.10B compare the PUND fittings obtained, for device class 29 ($t_{fe} = 8.37$ nm), for the experimental switching current profile and polarization hysteresis respectively. From Figure 3.10A, it can be noted that the leakage models that better reproduce the Gaussian shape of the switching current peaks are the exponential and the physical, while the peak simulated by the resistive model appears "boxy", with abruptly increasing currents. The reason for such abruptness resides in the linear voltage-interfacial leakage current relation which has no smoothing effect when the voltage changes suddenly. On the other hand, the exponential leakage currents of the other two models smooth out abrupt changes of the voltage, consequently producing smoother peaks. Interestingly, the simulation of only one PUND cycle, with the physical leakage model, produces a very high positive current spike visible in right part of Figure 3.10A, which disappears with subsequent cycles as highlighted by the presence of a normal positive peak closer to the anomalous one. The

[3]The ferroelectric permittivity listed in the table refers to the total effective permittivity of the ferroelectric and depletion capacitances in series, whose value equal to 35 is in accordance with literature values.

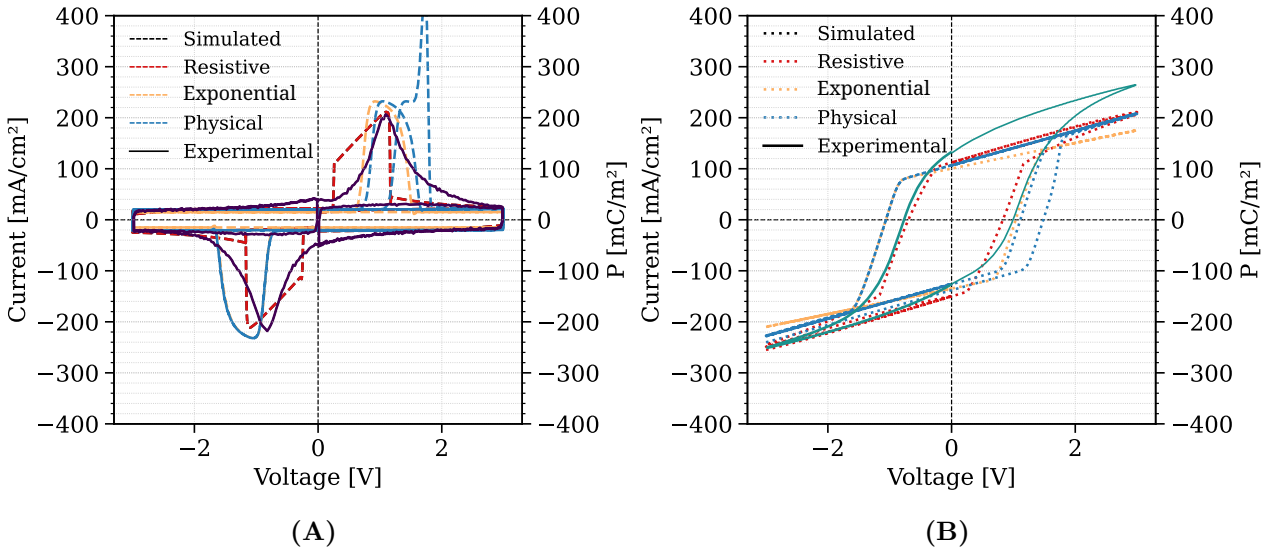


Figure 3.10: Comparison with the sample experimental data of device 29, $t_{fe} = 8.37\,nm$ of the PUND fittings. for the three leakage models discussed previously, of **(A)** the switching current profile and **(B)** the polarization hysteresis.

disappearance of the peak points out to a transient phenomenon which can be physically explained by a rearrangement of the charges inside the device the first time it switches. Conversely, the fittings of the polarization hysteresis overlap, indicating that all models are equivalent in this case (Figure 3.10B). Figure 3.11 instead compares the switching kinetics fitting of the different leakage models

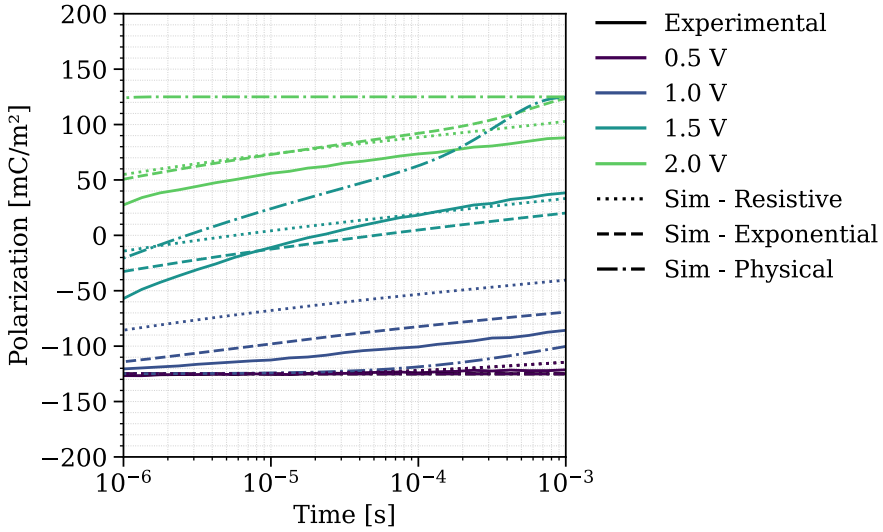


Figure 3.11: Switching kinetics experimental data compared with the fittings obtained for each leakage model, device class 29 with $t_{fe} = 8.37\,nm$. At 0.5 V and 1.0 V, the physical model (dash dotted lines) underestimates the experimental data, while the resistive (dotted) and exponential (dashed) models overestimate it. At 1.5 V the physical model fits the slope of the experimental curve, but overestimates it. The best fitting at this voltage is provided by the resistive model. At 2.0 V all models overestimate the experimental data, but the resistive model is the closest to the experimental curve.

and shows that while virtually every model follows the 0.5 V curve well, important differences are present at higher voltages. Starting with 1 V, the model that fits with the lowest overestimation of

the experimental data is the exponential, while the physical model underestimates the experimental data. At 1.5 V, although the resistive and exponential models follow the experimental curve closely, they proceed with a different slope. On the other hand, the physical model reproduces the slope better (up until 10^{-4} s, where it diverges), but overestimates the experimental curve. Finally, at 2 V all models overestimate the polarization, a consequence of an excessively rapid switching where the polarization rises earlier than expected; however, the resistive model is the most conservative, providing the best fitting.
Given the previous comparison, the *physical* model has been chosen because it fits the PUND better than the *resistive* and it showed similar performances to the other models when fitting the switching kinetics. Furthermore, in the physical model does not oversimplify leakage by defining abstract parameters such as resistivities and pre-exponential factors, but considers the physical conduction mechanisms occurring in the FeCap stack.

3.4 Parametric study of the physical leakage model

3.4.1 Scope and currents critical parameters

The behavior of the currents included in the physical model has been compared inside the ferroelectric and bottom electrode interface layers. The scope of the study is to compare corner cases of the currents over voltage, in order to determine which current and in which conditions, is dominant over the others, and therefore which conduction mechanism determines leakage. The corner cases are obtained by combining the minimum and maximum values of thickness and temperature for the layers considered, yielding four possible cases if the current depends on both variables (PF and SE), two if dependent on one only (FN).
The physical conduction model combines the contribution of three effects, namely Fowler-Nordheim tunneling, Schottky emission, and Poole-Frenkel (see Subsection 3.3.1). Each current depends differently on the electric field, temperature, the energy barrier height ϕ_{B}, and the trap depth ϕ_{T}. Fowler-Nordheim tunneling (eq. 3.6) is the most sensitive to the electric field, it is independent from the temperature, and depends on the junction barrier height. Poole-Frenkel depends on the electric field, temperature, and trap depth. Finally, Schottky emission is the least sensitive to the electric field and the most sensitive to the temperature. Similarly to FN, it also depends on the junction barrier height as. The table below summarizes these dependencies:

Current	**Dependencies**			
	Electric field	**Temperature**	**Dielectric barrier height**	**Trap depth**
Fowler-Nordheim	$E^2 \exp(-1/E)$	-	$(1/\phi_B) \exp(-\phi_B^{3/2})$	-
Poole-Frenkel	$E \exp(\sqrt{E})$	$\exp(-1/T)$	-	$\exp(-\phi_T)$
Schottky emission	$\exp\sqrt{E}$	$T^2 \exp(-1/T)$	$\exp(-\phi_B)$	-

Table 3.5: Overview of the dependency of the Fowler-Nordheim, Poole-Frenkel, and Schottky emission conduction mechanisms on the electric field, temperature, dielectric barrier height, and trap depth.

The currents have been implemented in a Python script that simulates a single layer of the FeCap stack. The outputs of the script have been validated by plotting the currents obtained for the same layer from a DC simulation run over the entire FeCap stack.

3.4.2 Ferroelectric

Starting with the ferroelectric,a voltage interval of $0-3\,\mathrm{V}$ has been considered, in order to investigate both lower and high voltage leakage contributions (similar to the positive voltage sweep that has been employed in the PUND and switching kinetics measurements). A temperature variation of $0-100\,^{\circ}\mathrm{C}$ has been employed to observe the current variability over a wide temperature range that includes typical room temperature ($20-25^{\circ}\mathrm{C}$) measurement conditions. Finally, a thickness range of $6-10\,\mathrm{nm}$ has been used to include all available device classes, whose ferroelectric thickness spans $6.45-10.63\,\mathrm{nm}$. In the DC simulation, the thickness of the BE interface has been considered constant and equal to 1 nm. All the relevant parameters used for both the Python code and the DC simulations are illustrated in the following Table:

Parameter	Description	Unit	Value
$\boldsymbol{V}$	**Simulation voltage**	$\boldsymbol{V}$	**0–3**
$\boldsymbol{t_{fe}}$	**Ferroelectric thickness**	$\boldsymbol{nm}$	**6–10**
$\boldsymbol{T}$	**Temperature**	$\boldsymbol{K}$	**273–373**
$\boldsymbol{\varepsilon_{r_FE}}$	**Ferroelectric relative permittivity**	**1**	**35**
$\boldsymbol{m_{eff}}$	**Ferroelectric effective mass**	**1**	**0.4**
$\boldsymbol{\phi_B}$	**Ferroelectric energy barrier**	$\boldsymbol{eV}$	**2**
A	Device Area	m^2	625×10^{-12}
t_{be}	BE thickness	nm	1
t_{te}	TE thickness	nm	0.1
$\varepsilon_{r_{be}}$	BE relative permittivity	1	100
$m_{eff_{int}}$	Interface effective mass	1	1
$\phi_{B_{int}}$	Interface energy barrier	eV	0.3
ϕ_t	Trap depth	eV	1
μ	Electron mobility	$m^2\,V^{-1}\,s^{-1}$	15×10^{-4}
N_c	Conduction band density of states	m^{-3}	1×10^{24}

Table 3.6: Material and device parameters used to study the leakage mechanisms operating in the ferroelectric layer. The parameters in **bold** are ferroelectric and sweep parameters.

Figure 3.12 shows the outputs of the Python code. The output of the DC simulation is the same as the Python simulation, because the majority of the voltage drop over the FeCap stack is located on the ferroelectric. Therefore the single layer Python simulation represents a good approximation of the overall behavior of the FeCap stack. The dotted lines represent currents plotted at low thickness $\mathrm{t_{fe}} = 6\,\mathrm{nm}$, while a solid line corresponds to higher thickness $\mathrm{t_{fe}} = 10\,\mathrm{nm}$. Figure 3.12A compares low and high thickness FN with PF corner cases. High thickness FN never overcomes PF, but low thickness FN can dominate low thickness and temperature PF starting from voltages $> 2\,\mathrm{V}$. At 3 V, low thickness FN is comparable to low thickness, high temperature PF, but does not dominate conduction. In Figure 3.12B, FN is compared with SE corner cases. SE currents are 8 or more orders of magnitude lower than PF, thus both low and high $\mathrm{t_{fe}}$ FN starts dominating over SE at lower voltages, in the $1-2\,\mathrm{V}$ range.
In summary, PF dominates for almost all voltages and corner cases, with exceptions occurring at high voltages, i.e. in the $2.0-3.0\,\mathrm{V}$ range, and at voltages below 0.1 V.

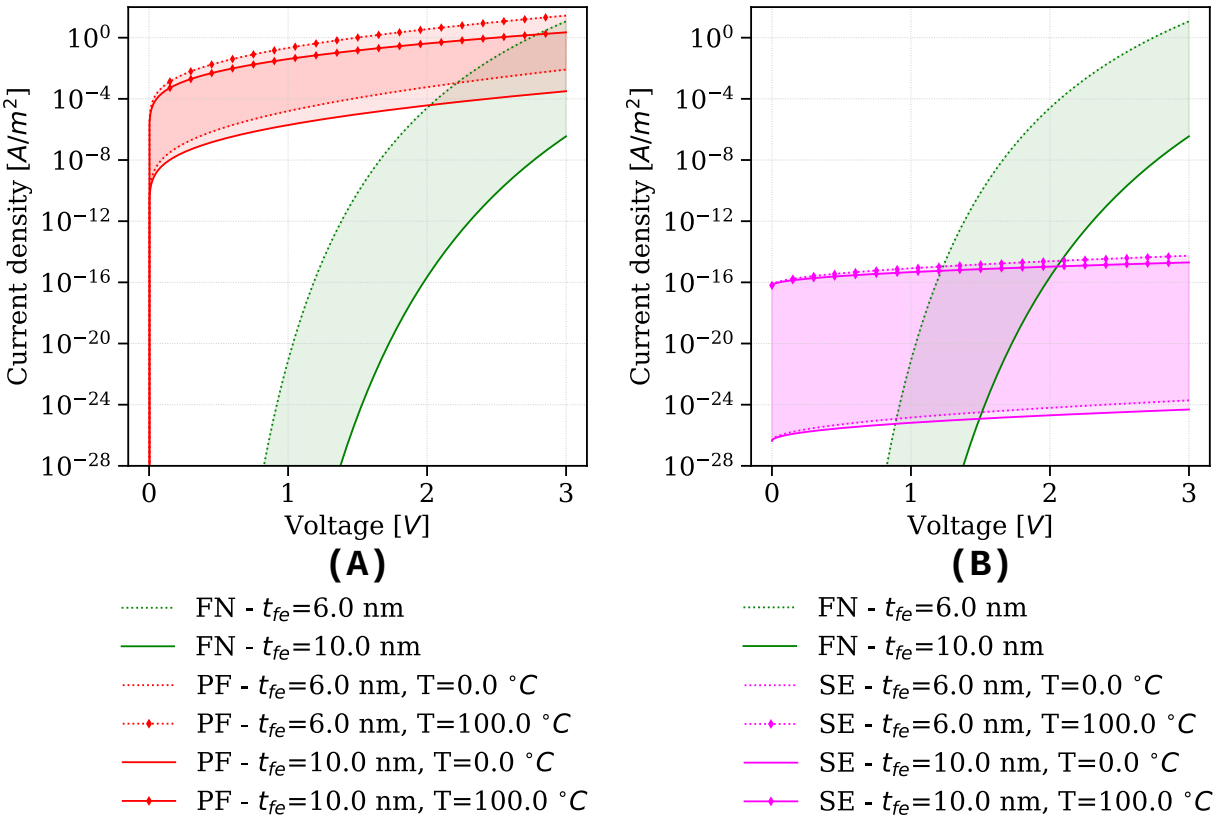


Figure 3.12: Python simulation of the ferroelectric leakage currents. **(A)** Fowler-Nordheim tunneling, at low and high thickness (dotted and solid lines green respectively), compared with four different Poole-Frankel corner cases. Notice that low thickness FN dominates over low thickness and temperature PF (dotted red line) for voltages $> 2\,V$, and is comparable to low thickness high temperature PF (dotted red line with markers) at $3\,V$. **(B)** Fowler-Nordheim tunneling compared with Schottky emission corner cases (magenta lines). The SE currents are lower than PF, thus FN begins to dominate both at low and high thickness at lower voltages in the $1 - 2\,V$ range.

3.4.3 Bottom electrode interface

Fixed junction barrier height

Regarding the BE interface, the same voltage and temperature intervals used for the ferroelectric have been considered, but the thickness range is different, spanning $0.5 - 2\,\text{nm}$. In these simulations, the value of ϕ_B has been considered constant and equal to 0.3 eV. In the DC simulation the thickness of the ferroelectric has been fixed at 8 nm, an intermediate value. The remaining parameters, already used for the ferroelectric layer (Table 3.6), have not been changed.
Figure 3.13 shows the outputs of the Python code and DC simulation respectively, and contrary to what occurs for the ferroelectric, they differ greatly, with the most notable differences being the different order of magnitudes of the currents and the absence of any FN contribution in the DC simulation.
Since interface and ferroelectric barrier heights have not been changed, V_fe is still much larger than V_be. Therefore, the DC simulation in Figure 3.13B plots the behavior of the leakage currents at very low V_be voltages. In the Python simulation, the situation depicted by the DC simulation is observed for a voltage range close to zero, where FN reduces asymptotically below SE and PF. At such low BE interface voltages, the dominant conduction mechanism is Schottky emission, which is

the least sensitive to the electric field.
By comparing Figure 3.13B with Figure 3.12A, it can be noticed that the interface SE currents and ferroelectric PF currents assume similar values, because the two layers are connected in series thus their total leakage currents must be equal.

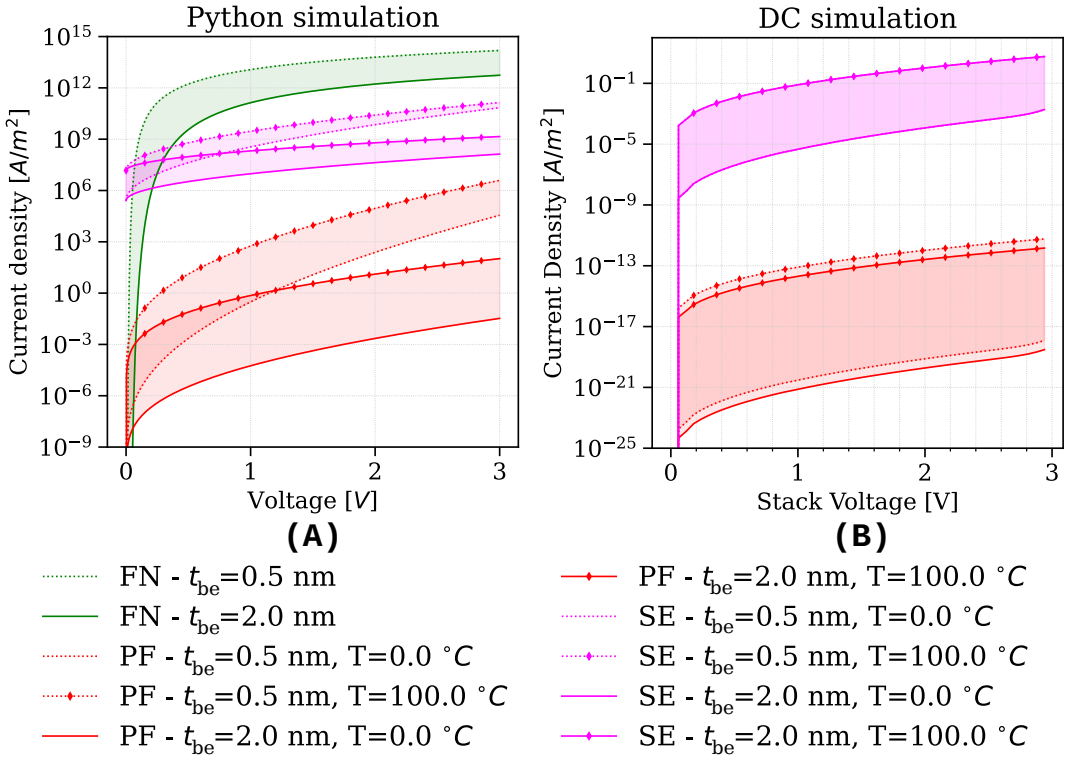


Figure 3.13: Comparison of the interface leakage currents obtained via **(A)** Python simulation of the single interface layer and **(B)** Cadence DC simulation of the entire FeCap stack. The currents obtained in the DC simulation are completely different from the Python simulation, where FN is present and is the dominant conduction mechanism, which instead is SE in the DC simulation. Furthermore, the maximum currents in the Python simulation are orders of magnitude higher than in the DC simulation, i.e. $\approx 10^{15}$ versus $\approx 10^{0}$.

Variable interface barrier height

Different electrode materials can create a wide range of interface layers which, depending on the compounds formed and phases (e.g. rutile and anatase for TiO_2, Figure 3.6) possess different barrier heights. Therefore, it is necessary to study the behavior of the leakage currents to identify which are the dominant conduction mechanisms depending on barrier height, in order to employ electrode materials that are appropriate for the operating conditions of the FeCap. In this study, the energy barrier range spans $0.3 - 1.5\,\text{eV}$, including and investigating beyond the $0.5 - 1.0\,\text{eV}$ range for TiO_2. As in previous studies, the temperature has been varied as well, in the $0 - 100°\text{C}$ interval. Interface thickness has been fixed at 1 nm, and the Python simulations have been carried out in the $0 - 1\,V$ BE voltage interval, where all the relevant transitions from one conduction mechanism to the other are shown to occur. Since the DC simulation considers the whole FeCap stack, a wider $0 - 3\,\text{V}$ stack voltage range has been considered, in line with previous studies. The remaining parameters have not been changed, and are illustrated in Table 3.6 in the previous subsection.
To track how the voltage over the interface (V_{be}) changes with barrier height, the voltages at which FN intersects and overtakes the dominant conduction mechanism, either SE or PF, have been highlighted.

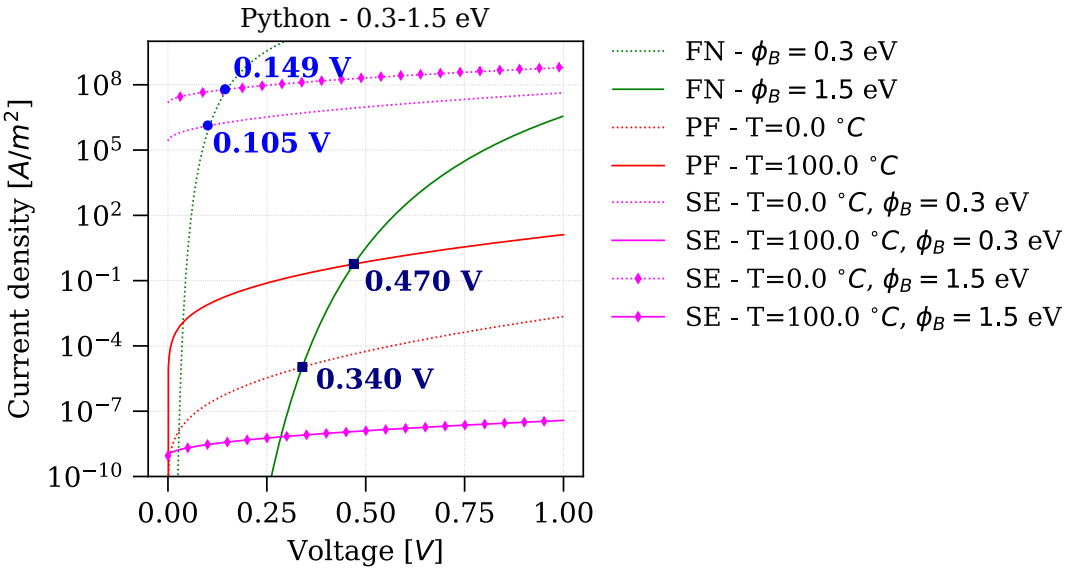


Figure 3.14: Python simulation of the BE interface leakage currents in the $0.3 - 1.5\,\text{eV}$ barrier height range. The higher ϕ_B, the higher the BE voltage at which FN (dotted and solid green curves) becomes dominant, either over SE or PF.

Figure 3.14 shows all the leakage currents, simulated with the Python code, in a $0.3 - 1.5\,\text{eV}$ barrier height range. At $\phi_B = 0.3\,\text{eV}$ the dominant conduction mechanism is initially SE, but at $V_{BE} = 0.105 - 0.149\,\text{V}$ depending on the temperature, FN overtakes Schottky emission. However, as the barrier is increased at 1.5 eV both SE and FN are reduced while PF, which does not depend on the barrier height, remains constant. Consequently, PF becomes the dominant conduction mechanism until FN takes over at $V_{BE} = 0.340 - 0.470\,\text{V}$. This simulation suggests that the interface voltage at which FN dominates increases monotonously with the barrier height.

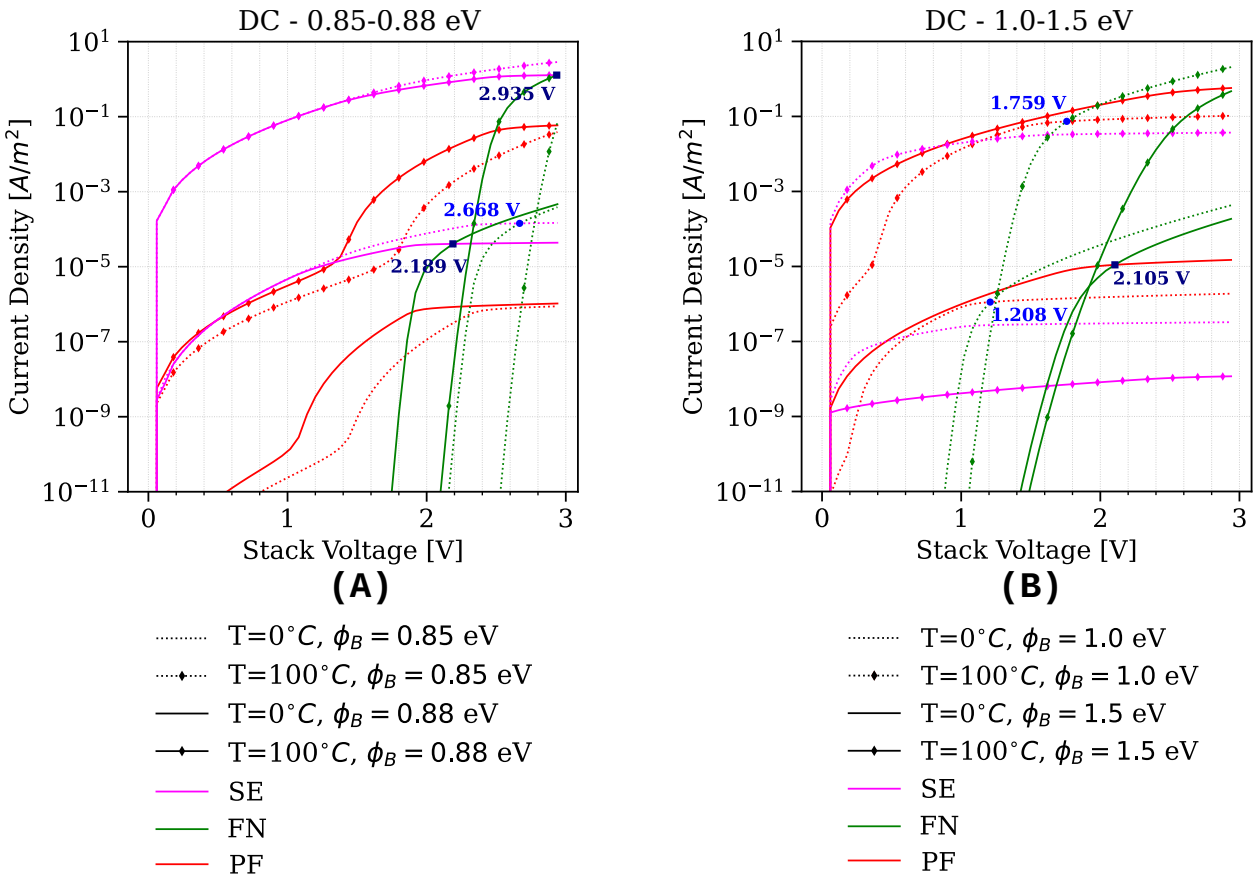


Figure 3.15: DC simulations of the BE interface leakage currents in two different barrier height ranges. **(A)** For $\phi_B < 0.85\,eV$ FN never becomes dominant, but at $\phi_B = 0.85\,eV$ FN overtakes SE, which is the dominant conduction mechanism, only at low temperature (dotted green line) and starting from $V_{stack} = 2.668\,V$. At a slightly higher barrier of 0.88 eV FN overtakes SE both at low and high temperature (solid green lines without and with markers). **(B)** In the $1.0 - 1.5\,V$ range SE decreases below PF which becomes the dominant conduction mechanism. The increase in barrier height reduces FN as well, which at $\phi_B = 1.5\,eV$ overtakes PF only at low temperature (solid green line), reverting the trend initiated at $\phi_B = 0.85\,eV$.

However, the Python simulations are run only on one layer and not the entire stack, therefore it is possible that, at a certain ϕ_B, FN does not overtake the dominant conduction mechanism as predicted, because the interface voltage is lower than required. Indeed, as shown in Figure 3.15A, the DC simulations confirm that FN overtakes SE starting from $\phi_B = 0.85\,eV$ and only at low temperature. Shortly after, at $\phi_B = 0.88\,eV$, FN overtakes SE at high temperature as well. Since the interface voltage increases monotonously with ϕ_B (Figure 3.14), and FN progressively overtakes SE the higher the barrier, it can be inferred that the voltage drop over the interface is increasing. Moreover, FN starts dominating at increasingly low stack voltages, reducing from 2.668 V to 2.189 V at low temperature.

At $\phi_B = 1.0\,eV$, as shown in Figure 3.15B, SE has decreased even further and dominates conduction only for stack voltages $< 0.5 - 0.8\,V$, after which it is replaced by PF and then FN. Notice that FN dominates at even lower stack voltages, especially at low temperature where PF and SE assume the lowest values. However, increasing the barrier at 1.5 eV decreases SE and FN even further, increasing the stack voltage at which FN dominates conduction. Consequently, Fowler-Norhdeim tunneling overtakes PF only at low temperature, reverting the trend begun at $\phi_B = 0.85\,eV$. This

suggests that the reduction of FN with ϕ_B outweighs the increase of V_{be} preventing it from dominating conduction, firstly only at high temperature, and then at low temperature as well if the energy barrier were to increase over 1.5 eV.
The following table summarizes the results of this study:

Current	Energy barrier [eV]				
	0.3 - 0.85	**0.85**	**0.88**	**1.0**	**1.5**
FN	Never dominates	Dominates at: $T = 0°C$ $V_{stack} = 2.668\,V$	Dominates at $T = 0 - 100°C$ $V_{stack} = 2.189 - 2.935\,V$	Dominates at: $T = 0 - 100°C$ $V_{stack} = 1.208 - 1.759\,V$	Dominates at: $T = 0°C$ $V_{stack} = 2.105\,V$
SE	Dominates conduction	Dominates conduction	Dominates conduction	Dominates at: $V_{stack} < 0.5 - 0.8\,V$	Never dominates
PF	Never dominates	Never dominates	Never dominates	Dominates Between SE and FN	Dominates conduction

Table 3.7: Summary of the leakage mechanisms dominating conduction in the interface at different barrier heights.

This study suggests that the interface voltage increases with barrier height. From being negligible at $\phi_B = 0.3$ eV where $V_{BE} = 0.105 - 0.149$ V is not reached since FN never dominates over SE, to almost 0.5 V at $\phi_B = 1.5$ eV. Therefore, in case FeCaps with high interface barriers are operated at voltages lower than $1 - 1.5$ V, the interfacial voltage drop could potentially halve or reduce by one third the voltage over the ferroelectric. Therefore, it is convenient to choose BE materials which create low-ϕ_B interfaces that drain away the least possible amount of voltage from the ferroelectric. For example, using W as BE creates a WO_x interface whose energy barrier is around $\approx 0.32\,eV$ [45, 46]. For barrier heights lower than 1 eV, the dominant conduction mechanism is SE, thus reducing the temperature of the samples can substantially limit interface leakage. However, this method is less effective if $\phi_B = 0.85 - 1.0$ eV because for stack voltages of $2.935 - 1.208$ V the temperature insensitive FN becomes dominant. In this case, leakage can only be reduced by substantially limiting the operating stack voltage of the FeCap. Finally, if $\phi_B > 1.0$ eV, SE and FN substantially decrease and PF becomes the dominant conduction mechanism. Consequently, leakage can be controlled both by reducing temperature and the defectivity, and thus the trap density, of the interface. However, FN still persists at $V_{stack} > 2.105$ V, and since FeCaps with high ϕ_B interfaces must be operated at voltages higher than 1.5 V, preferably higher than 2 V so that the interface voltage drop (up to 0.5 V) is less than 25% of the total stack voltage, decreasing temperature and trap density will not suppress leakage at high V_{stack}. Fowler-Nordheim can be suppressed by further increasing the energy barrier, but at the cost of a higher V_{be}. Therefore, electrode materials that form interfaces with $\phi_B \geqslant 1.5$ are recommended in case the FeCap can be operated at higher voltages.

Chapter 4

Measurements and discussion

This chapter describes the quasi-static or DC measurement campaign performed, illustrating the instrumentation and methodology used. The experimental data obtained is illustrated and discussed in detail, with a focus on device-to-device variability. The physical leakage model, implemented in the FeCap compact model, is calibrated and validated by comparing the output of DC simulations with the experimental data, discussing the fittings and leakage parameters obtained.

4.1 Measurement setup

4.1.1 Instrumentation and available samples

The DC measurement campaign has been performed using a Keithley™ 2604B Source Meter Unit (SMU) to both source the DC voltage sweep and measure the output current. The SMU has been connected to a MPI™ TS3000 probe station which has been used to contact the available samples. The SMU has been controlled with a tailored script that performed the required measurement and saved the resulting data in text files. A plotting script has also been developed to check each measurement step-by-step. As remarked in the previous chapters, the available samples are divided into three classes, depending on the thickness of the ferroelectric, referred to as devices 28/29/30 with $t_{fe} = 10.63/8.37/6.45\,\text{nm}$ respectively. On each die samples are grouped by area, and catalogued by row and contact number as "Device-Class_Row_Contacts", where for example "28_2-15_1-2" means a FeCap of class 28 in row $2-15$ and of contacts $1-2$. The FeCaps share one electrode in pairs which can either be the top or bottom electrode, and each row contains 13 devices. For this measurements, samples with an area of $25 \times 25\,\mu m^2$ have been chosen.

4.1.2 Measurement plan

As explained in Subsection 2.1.3, a DC measurement is executed by applying a staircase voltage sweep spanning a user-defined range. Each voltage step lasts for $t_{settle}+t_{int}$, where t_{settle} is the settle time that defines the delay between the beginning of the step and the start of the measurement. The latter lasts for the integration time t_{int} in which the detected current is integrated over time and then divided by the total time, yielding the average current. Both times have to be manually calibrated in order to obtain a high quality measurement. The settle time is used to filter out transient currents which can be caused, for example, by capacitance charging. Therefore, the settle time must last more than the transient phenomenon. It is also useful to employ longer integration times in order to acquire more current samples for each voltage, yielding more accurate readings. Indeed, short integration times can artificially inflate the resulting current, since a small dataset is divided by a very short time.
In this measurement campaign I have used $0-3\,\text{V}$ voltage sweeps in order to observe both pos-

sible low and high voltage leakage phenomena. The sweep has been executed back and forth, i.e. $0 \rightarrow 3 \rightarrow 0\,\mathrm{V}$, in order to check the presence of discrepancies between the two curves, which are due to capacitance charging and ferroelectric switching, and filter them out. In order to avoid discrepancies due to polarization switching, which might increase the current in the forward sweep, a shorter initialization sweep has been performed before the main one. As for the time values, I have used $t_{settle} = 1\,\mathrm{s}$ and $t_{int} = 0.5\,\mathrm{s}$, which is the maximum integration time allowed by the SMU. It has been verified that higher settle times increased ferroelectric switching. Device-to-device variability has been evaluated by performing 30 measurements for each device class, i.e. 90 measurements in total. Each of the 30 measurements per device class has been executed on 30 different FeCaps in order to specifically survey device-to-device variability.

4.2 Quasi-static leakage measurements

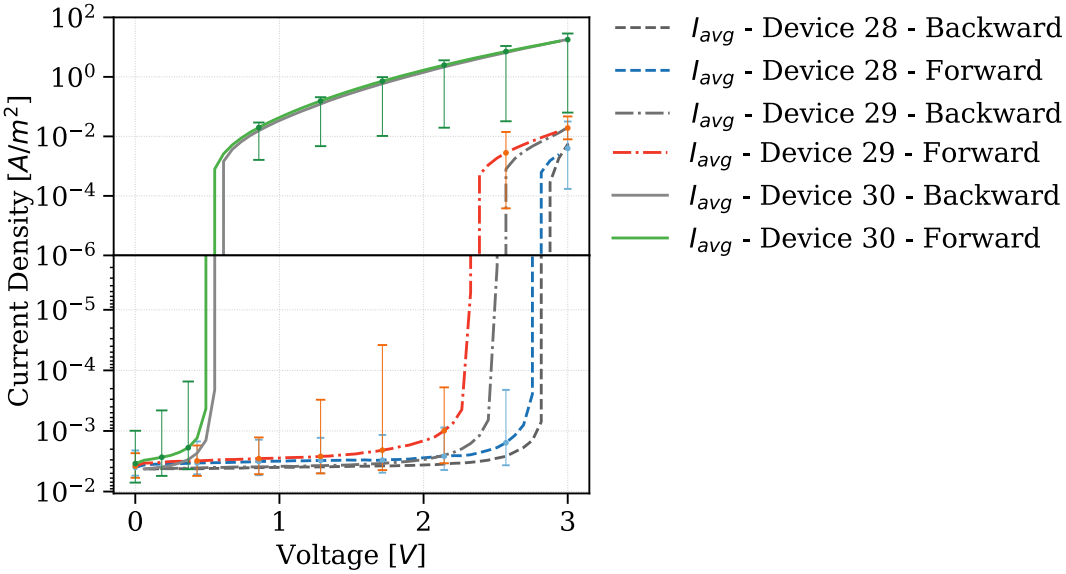


Figure 4.1: Positive and negative DC experimental data, including forward and backward sweeps, of the three device classes. The error bars highlight the device-to-device variability, ranging from the maximum to the minimum current value measured at a specific voltage.

Figure 4.1A shows the experimental data obtained for the three different device classes. The curves represent the average current and the error bars highlight the device-to-device variability. The error bars span the whole data range, from the maximum to the minimum (positive) measured value for that voltage. The average current follows the expected trend, increasing with thickness. In this Figure both forward and backward sweep data has been reported, showing a satisfactory degree of agreement. Indeed, the data of the two sweeps is in the same order of magnitude and differs less than half that order. Notice that the higher the thickness, the higher the number of negative current values. Indeed, since the current reduces with thickness, fewer values are detected above the noise floor.
Device-to-device variability has been studied by calculating the cumulative distribution functions (CDFs) for each device class at three different voltages, i.e. 2/2.5/3 V.
Figure 4.2 reports all the calculated CDFs obtained from DC measurements on FeCap with $t_{fe} = 10.63\,\mathrm{nm}$ (dashed lines), $t_{fe} = 8.37\,\mathrm{nm}$ (dash-dotted lines), and $t_{fe} = 6.45\,\mathrm{nm}$ (solid lines) at three different voltages - 2.0 V (blue gradient), 2.5 V (red gradient), and 3.0 V (green gradient). The CDFs show a clear increment of the current with voltage. In order to include negative data in the plot, the

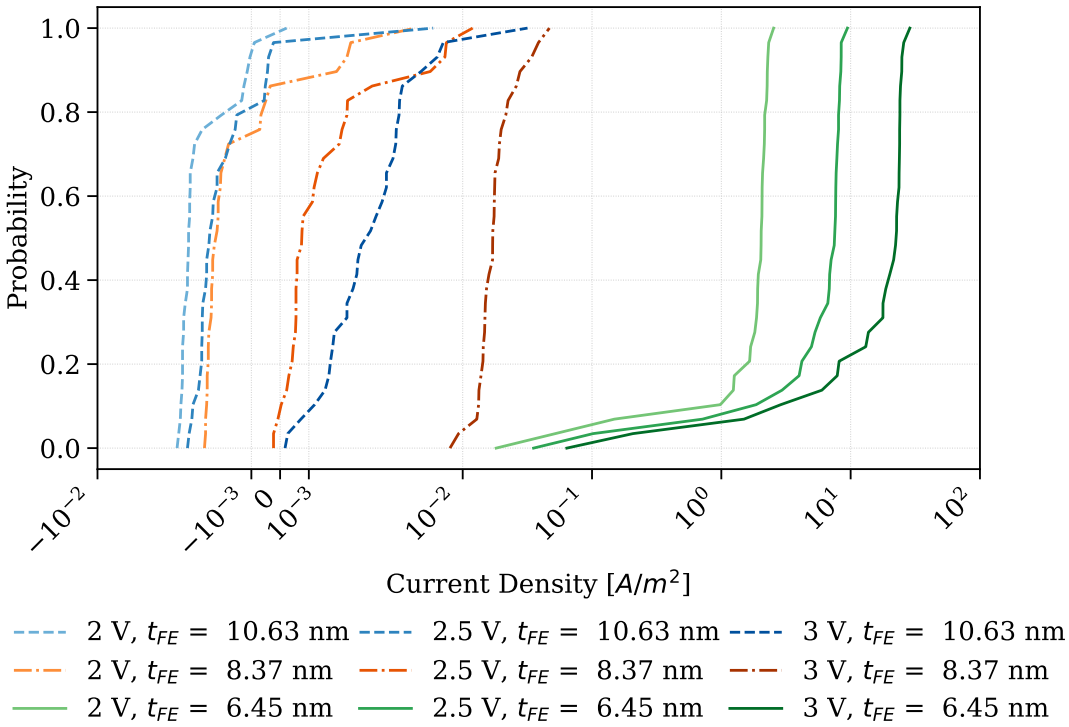


Figure 4.2: Cumulative density function obtained from DC measurements on FeCap with $t_{fe} = 10.63\,nm$ (dashed lines), $t_{fe} = 8.37\,nm$ (dash-dotted lines), and $t_{fe} = 6.45\,nm$ (solid lines) at three different voltages - 2.0 V (blue gradient), 2.5 V (red gradient), and 3.0 V (green gradient).

symlog scale has been used, which plots positive and negative data on logarithmic scale, and in the region where the logarithm crosses zero, a linear region can be defined so that this data can be represented together. The limits of the linear region are defined by the user, and in case of Figure 4.2 they span from -10^{-3} to 10^{-3}.
The current of the thinnest devices exhibits the most regular increment among other classes. The regularity of this class of devices can be explained with the measurement data reported in Figure 4.1. The current measured in the thickest devices at 2 V and 2.5 V is still close to the negative floor value, hence the small variation between CDFs. Devices of class 29 ($t_{fe} = 8.37\,nm$), which already has positive values at 2.5 V, exhibits no significant "leap" in the CDF at 3 V. There are also significant differences in the shapes of the CDFs. Contrary to the CDFs of other device classes which do not exhibit very large tails for low and high probabilities, the CDF of the thinnest devices shows a large low probability tail while the rest of the curve is extremely sloped, close to vertical. This differences are explored in greater detail in Figure 4.3 which shows the CDFs at 3 V for all ferroelectric thicknesses.
The thinnest and thickest devices show the highest absolute device-to-device variability, which spans approximately 2 orders of magnitude. On the other hand, devices with $t_{fe} = 8.37\,nm$ (class 29) exhibit the lowest absolute variability, which is less than a half order of magnitude. Therefore, class 29 will be the most restrictive when fitting the leakage model. The extremely large variability exhibited by the thinnest devices is due to the exponential increase in current when reducing thickness. As the current gets exponential higher, the variability widens exponentially as well.

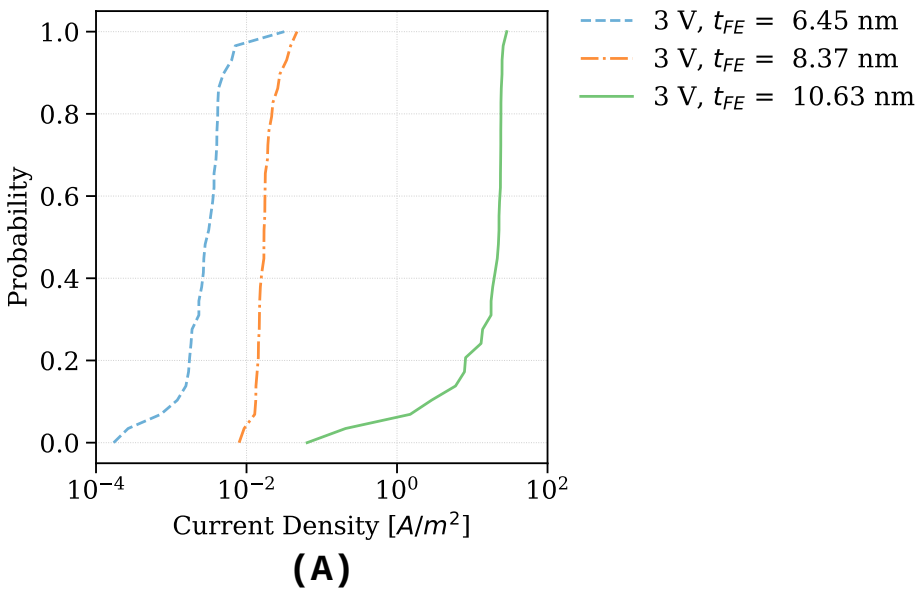


Figure 4.3: Cumulative distribution functions plotted at 3 V for all device classes.

However, although the variability in the thinnest devices is high, it is also more unlikely to occur since it is given mainly by low probability outliers. Indeed, the majority of values is located at a probability higher than $0.2 - 0.3$. The average current is closer to the maximum value, which is confirmed by the asymmetric error bars the thinnest device class exhibits in Figure 4.1, with the average curve much closer to the upper than the lower error limit. On the other hand, the thickest devices show both high and low probability tails, and most values are located closer to the average value, far from the maximum and minimum values which are outliers. Such a large variability could be caused by noise, which is much more important for lower currents. Device class 29 ($t_{fe} = 8.37$ nm), whose currents are presumably farther from the noise floor but not as exponentially higher as in the thinnest devices, exhibit the lowest absolute device-to-device variability.

4.3 Fitting the leakage model

4.3.1 Scope, method, and parameters

Parameter	Description	Unit	Value
$\boldsymbol{\phi_T}$	**Trap depth**	$\boldsymbol{eV}$	**0.9**
$\boldsymbol{t_{fe}}$	**Ferroelectric thickness**	$\boldsymbol{nm}$	**6.45/8.37/10.63**
$\boldsymbol{\mu}$	**Electron mobility**	$\boldsymbol{V^{-2}}$	$\boldsymbol{15 \times 10^{-4}}$
$m_{eff,fe}$	Effective mass	1	0.4
$\phi_{B,fe}$	Electrode/Ferroelectric barrier height	eV	2
$\phi_{B,be}$	Electrode/BE interface energy barrier	eV	1
t_{be}	BE interface thickness	nm	1.5

Table 4.1: Starting values of the leakage parameters. The parameters in **bold** are the leakage parameters that have been calibrated in this study. All remaining parameters concerning the physical leakage model and the FeCap compact model as a whole are listed in Tables 3.3 and 4.2.

The experimental data obtained has been used to calibrate the physical leakage model,implemented in the FeCap compact model. The fitting operation has been focused on four ferroelectric parameters that substantially influence leakage, namely the trap depth ϕ_T and the mobility μ which influence Poole-Frenkel emission, and the thickness of the ferroelectric layer t_{fe} that shapes all leakage currents. Firstly, the trap depth ϕ_T has to be calibrated to ensure that the total, simulated leakage currents fall within the statistical variation of their respective device, i.e. within the error bars. The simulated currents obtained will act as a baseline for the calibration of the other parameters. Subsequently, fitting ranges for the remaining leakage parameters have been computed and compared with data available in literature to check their plausibility. It is important to remark that the ranges found when fitting each parameter singularly represent their maximum variation allowed within the experimental statistical limits while keeping the other parameters constant. The final objective has been to find a set of leakage parameters that fits all devices at once. Table 4.1 summarizes the starting values for each model parameter, where the parameters in **bold** have been fitted. The values of parameters W_b, d_e, ε_{depl}, and N_{depl} are listed in Table 3.3. The remaining parameters, concerning the physical model, that have not been changed are reported in Table 4.2.

4.3.2 Calibrating the trap depth

The trap depth depends on the material, therefore it should not change with ferroelectric thickness. However, the calibration revealed that a lower trap depth was necessary to fit the thinnest devices, highlighting a possible limit of the PF model when fitting currents through dielectrics thinner than 8 nm.

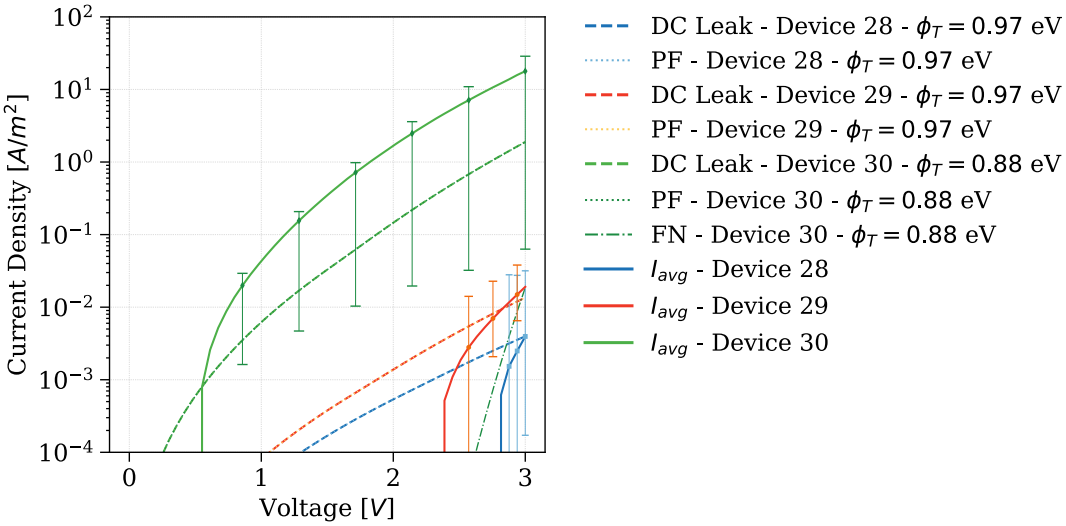


Figure 4.4: Simulated total leakage curves (dashed lines) compared to the average experimental data (solid lines) and device-to-device variation (error bars) measured, for all device classes.

Figure 4.4 plots the simulated leakage curves (dashed lines) using two different values of trap depth. For the thinnest device with $t_{fe} = 6.45$ nm, the trap depth is equal to 0.88 eV, while for the remaining device classes $\phi_T = 0.97$ eV. Both values of trap depth are plausible considering shallow traps with thermal ionization energies (trap depths) in the range of $0.7 - 1.0$ eV below the conduction band of HfO_2/HZO and densities in the order of 10^{19} cm^{-3} [39]. Deep traps are also present in the range of $2.0 - 3.5$ eV but refer to the photoionization energy, which is not an influencing factor in this study. The dominant conduction mechanism in the simulated curves is Poole-Frenkel, followed in small part by Fowler-Nordheim tunneling, especially for the thinnest devices. The simulated curves for device classes 28 and 29 (10.63 nm and 8.37 nm thick ferroelectric respectively) are also close

to the average experimental values, and reproduce how the leakage currents vary with ferroelectric thickness. However, it is evident that the thinnest device class constitutes an outlier in which the experimental current is way higher than expected. Therefore, the PF model has to be either corrected accordingly, or replaced by other more advanced models (see Section 4.5). Notice that for the thinnest device class the slope of the simulated curves is similar to the experimental data. On the other hand, the experimental curves of the other device class are much steeper than the simulated lines. A similar, steeper region can be observed in the thinnest device class at the beginning of the experimental green solid curve. This steep region is an artifact caused by the transition from negative to positive current data. Due to the few positive data points captured in device classes 28 and 29, only the beginning of the experimental curve is obtained, hence excluding the lower steepness part which is present in the thinnest device class and fits better with the slope of the simulated leakage.

4.3.3 Identification of the dominant conduction mechanism

In order to evaluate whether Poole-Frenkel is the main conduction mechanism and the quality of the fitting, both experimental and simulated currents have been plotted in Poole-Frenkel, Fowler-Nordheim, and Schottky emission plots. The total simulated leakage current comprises mainly of Poole-Frenkel emission, thus example pure FN and SE curves have been included only in the respective plots, in order to facilitate the comparison between the behavior of the experimental data and the simulated currents.

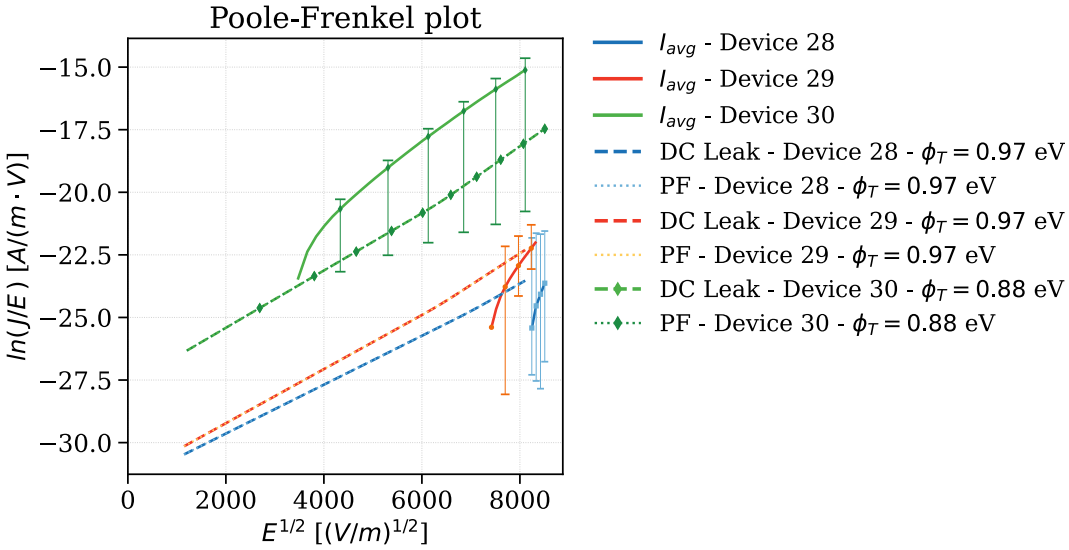


Figure 4.5: Plot of the experimental (solid lines) and simulated (dashed lines) leakage current data in a Poole-Frenkel plot. While the almost pure PF simulated curves behave as straight lines, the experimental currents present curved regions.

Figure 4.5 plots the experimental and simulated curves on a Poole-Frenkel plot. The current is plotted as ln(J/E) over $\sqrt{E}$ where E is the electric field over the entire FeCap stack. The electric field is calculated as the voltage over the stack divided by its total thickness which includes the metal electrodes but not the interface layers, i.e. $t_{tot} = t_{fe} + t_{el}$, where $t_{el} = 35\,nm$ is the total thickness of the electrodes. The device class 30, with the thinnest ferroelectric, is the only one that has sufficient positive data points for comparison. In a Poole-Frenkel plot, PF currents appear as straight lines, as clearly showed by all the simulated dashed curves. On the other hand, the average experimental current presents a curved part when transitioning from negative to positive data points, but straightens afterwards. The slope of the straight part matches the simulated one,

confirming that main mechanism in the ferroelectric layer is Poole-Frenkel.

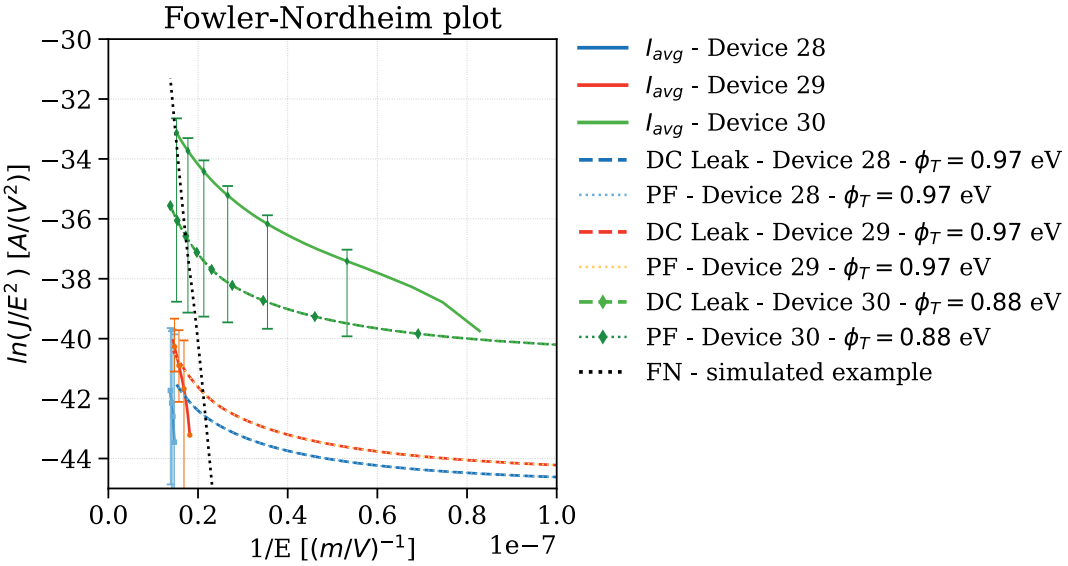


Figure 4.6: Plot of the experimental (solid lines) and simulated (dashed lines) leakage current data in a Fowler-Nordheim plot. The pure FN current (dotted black curve), obtained for the thinnest device class by reducing barrier height, is straight and very sloped, while both the experimental and simulated leakage currents are much less steep and present curved regions closer to zero.

Conversely, Figure 4.6 plots the simulated and experimental currents in a Fowler-Nordheim plot. The black dotted curve is inserted as an example of how a pure FN leakage current would behave in such a plot. This sample current has been obtained for the thinnest device class, i.e. $t_{fe} = 6.45\,nm$, and with a lower energy barrier height $\phi_B = 1.8\,eV$. In a Fowler-Nordheim plot, a pure FN current appears as an extremely steep, negatively sloped, straight curve. Its behavior is very different from the experimental data of the thinnest devices. The latter not only is less sloped, but also exhibits important non-linear regions at the beginning and end of the curve. In particular, the non-linear tail at high fields, i.e. low 1/E, is similar to the simulated leakage currents, which comprise almost exclusively of Poole-Frenkel emission (Fowler-Nordheim tunneling is at least 2 orders of magnitude lower, see Figure 4.4A, for the thinnest device). The complete absence of any behavior in the experimental data that can be related to FN tunneling confirms, as previously supposed, that FN tunneling does not dominate nor significantly influence conduction in the FeCap stack.
Figure 4.7 visualizes the simulated and experimental currents is a Schottky emission plot. The important difference of this plot from PF and FN plots is that, on the y-axis, the current density is divided not by the electric field in the ferroelectric but by the temperature squared, which has been assumed to be equal and constant to the temperature of the lab where the measurements have been performed, i.e. $T = 293\,K = 20°C$. Similarly to what has been done in the FN plot, an example SE curve (dash-dotted black line) has been inserted as reference.
The latter has been obtained for a much lower value of Schottky barrier $\phi_B \approx 0.8\,eV$ and higher $T = 200°C = 473\,K$. It is important to notice that the simulated leakage currents, given almost exclusively by PF emission, are almost straight in this plot as well, which might create confusion. Recall that, from equations 3.7 and 3.8, both PF and SE depend on $\exp(E^{1/2})$. This similar dependency on the electric field also explains why PF currents appear as almost straight lines in a SE plot as well. Still, the example curve has been obtained with totally unphysical values of energy barrier and temperature for the structure considered, and its less steep than PF. Although sample heating during measurement and Schottky barrier lowering due to the accumulation of charges at

the electrode/ferroelectric interface can occur, such high temperatures are not only implausible but also hard to detect. Furthermore, an excessive barrier lowering would also imply an important reduction of the Fowler-Nordheim barrier height, considered equal to the Schottky barrier in this study. With much lower energy barriers, the simulated FN current would increase uncontrollably, contradicting the behavior of the experimental data and the considerations made in the previous paragraph. Therefore, it is reasonable that SE does not play an important role in the FeCap leakage.

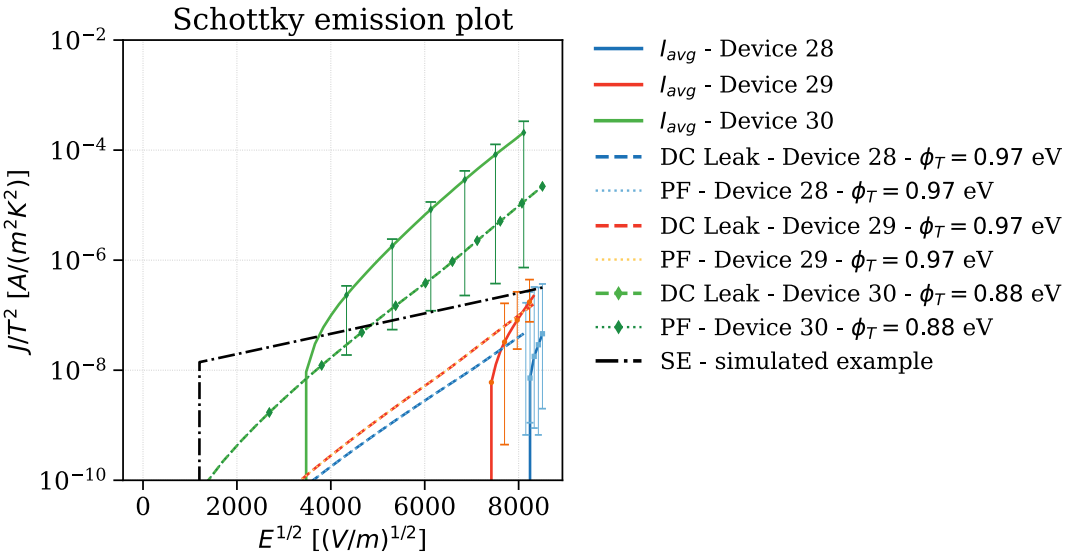


Figure 4.7: Plot of the experimental (solid lines) and simulated (dashed lines) leakage current data in a Schottky emission plot. The pure SE current (dash-dotted black curve), obtained for the thinnest device class by significantly reducing barrier height and increasing the temperature, is straight and less steep than both the experimental and simulated data.

4.3.4 Calibrating the thickness of the ferroelectric

The ferroelectric has been deposited via atomic layer deposition (ALD), which is a deposition technique that uses reactive gaseous precursors to deposit a material on a target surface. The film produces is extremely conformal, meaning that the thickness of the film remains approximately constant regardless of surface topology, and its thickness can be controlled accurately since the chemical reactions occurring on the surface are self-limiting. In order to start deposition again, the precursors must be alternated in cycles. Since each cycle deposits a certain thickness, the user can easily control the thickness of the film deposited. Calibration begins again from device class 29 with $t_{fe} = 8.37\,nm$ which exhibits the lowest device-to-device variability. Figure 4.8 plots the thickness variability range obtained for all device classes. The maximum variability has been calibrated on device class 29 ($t_{fe} = 8.37\,nm$), and resulted in a thickness variation of $\pm 10\%$, with respect to the average current. The dotted curves represent corner cases of thickness variation, and markers are used to highlight the higher thickness curve. Once again, the dominant conduction mechanism is Poole-Frenkel. According to literature, ALD thickness uniformity can be $\leqslant 4\%$ [47], which falls withing the range found.

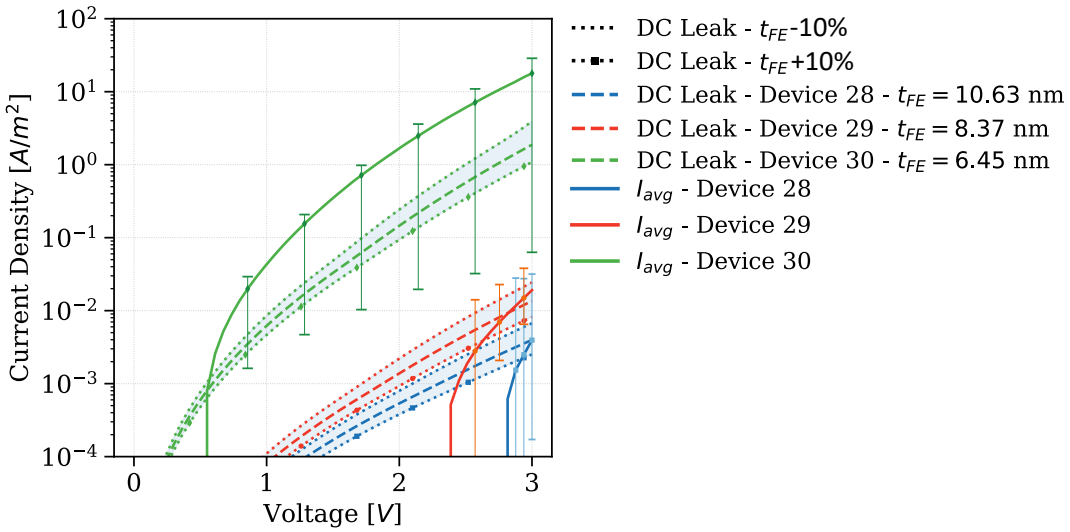


Figure 4.8: Calibration range of the ferroelectric thickness for all device classes. The range has firstly been calibrated on device class 29 with $t_{fe} = 8.37\,nm$ which has the lowest device-to-device variability (orange and red lines), imposing a maximum thickness variation of $\pm 10\%$. Dotted lines represent.

4.3.5 Calibrating the mobility

The electron drift mobility μ is a parameter that influences only Poole-Frenkel emission. Unfortunately, literature regarding the mobility inside HZO and HfO_2 is lacking due to both the recent introduction of these materials and their use as gate oxides. Indeed, since both HfO_2 and ZrO_2, which are the two binary compounds constituting HZO, have been recently popularized as gate dielectrics in MOSFETs, research focuses on the effect these materials have on the effective channel mobility in silicon. Therefore, I have decided to assume a starting value of electron mobility of $15 \times 10^{-4}\,m^2\,V^{-1}s^{-1}$ similar to $20 \times 10^{-4}\,m^2\,V^{-1}s^{-1}$ reported for SiO_2[48].

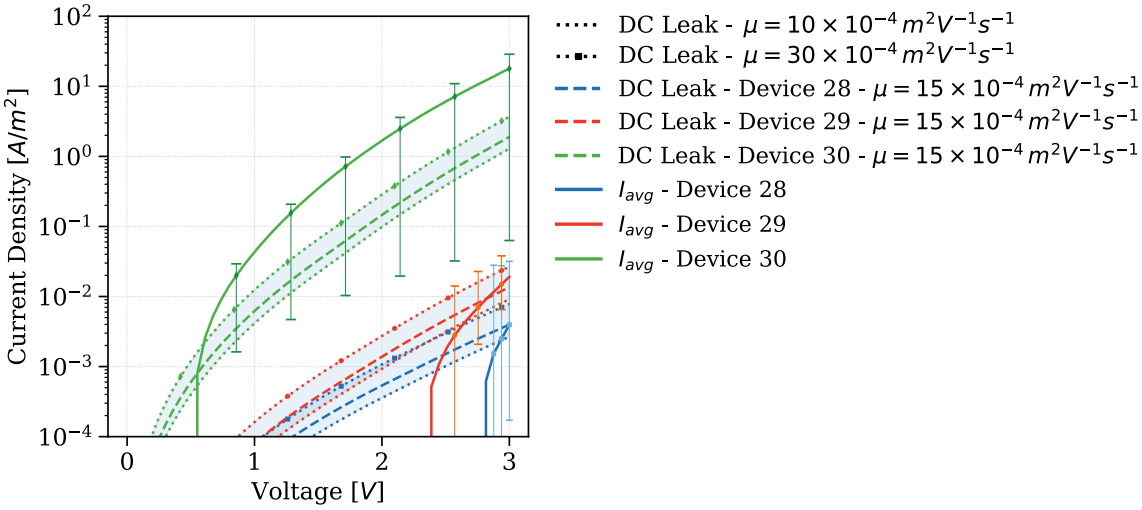


Figure 4.9: Calibration range of the electron mobility μ for all device classes. As done with the thickness, the mobility variation has been calibrated on device class 29 ($t_{fe} = 8.37\,nm$) first (orange and red lines), which exhibits the lowest device-to-device variability. The mobility range found was $10 - 30\,m^2\,V^{-1}\,s^{-1}$.

Figure 4.9 illustrates the calibration of the mobility starting from the most restrictive device class, that is 29 with $t_{fe} = 8.37\,nm$ (orange and red lines). The mobility range found is $10 - 30 \times 10^{-4}\,m^2V^{-1}s^{-1}$, which fits the remaining device classes as well (green and blue lines). Due to the absence of literature data about this parameter, the mobility can be treated as a fitting parameter.

4.3.6 Summary and further considerations

The table below summarizes the parameter ranges found and the values reported in literature:

Parameter	Description	Unit	Literature values	Fitting ranges
ϕ_T	Trap depth	eV	$0.7 - 1.0$[39]	$0.88 - 0.97$
$t_{FE,\%}$	FE thickness variation	1	$\leqslant 4\%$[47]	10%
μ	Electron mobility	$m^2\ V^{-1}s^{-1}$	-	$10 - 30 \times 10^{-4}$

Table 4.2: Leakage parameters found via fitting of the experimental data compared with the values reported in literature.

The trap depth falls within the reported values, but is not univocal for all devices because device class 30, which has the thinnest ferroelectric layer, exhibits much higher currents than expected.This discrepancy highlights the limits of the PF model when fitting currents measured in films thinner than $6\,nm$ (see Section 4.5). The ferroelectric thickness can vary up to 10% when fitting the experimental data, but the usual thickness variability is about less than one third than the fitted range, i.e. $\leqslant 4\%$[47].
Regarding carrier mobility, data from literature is lacking since both HfO_2 and HZO are recent materials adopted as gate insulators, replacing SiO_2. However, starting from a reported value of mobility similar to SiO_2[48] a reasonable range of mobility that fits the data has been obtained.

4.4 Calibration of the set of leakage parameters

Considering the leakage parameter ranges obtained in the previous section, I have calibrated a set of leakage parameters that fits the experimental data. The calibration focused on the thickness of the ferroelectric t_{fe} and the electron mobility μ. The ferroelectric thickness variability imposed has been 4% as per literature (Table 4.2). Conversely, the mobility has been treated as a fitting parameter because further literature data is absent.
The calibration of this parameter set has been carried out on FeCaps with $t_{fe} = 8.37\,nm$, part of device class 29, which exhibit the lowest absolute device-to-device variability. Using a t_{fe} variation of 4%, the calibration yielded a mobility range of $10 - 30 \times 10^{-4}\,m^2V^{-1}s^{-1}$, which is the same range found when fitting the parameter singularly (Table 4.2).
Figure 4.10 clearly shows that the set of parameters obtained fits the experimental data. The plot reports two corner cases (dotted lines, with and without markers) for the total leakage current, comprising almost exclusively of Poole-Frenkel emission, considering lowest and highest thickness values combined with the highest and lowest values of mobility respectively. The leakage parameters range also fits the remaining device classes.

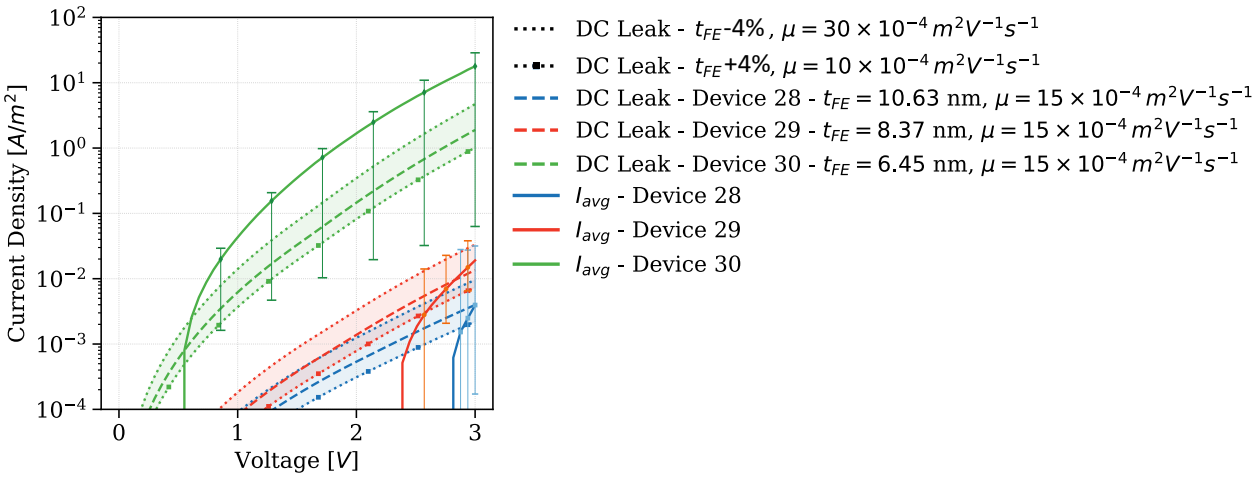


Figure 4.10: Calibration of the set of leakage parameters that fits the experimental data imposing a thickness variability of 4%, starting from device class 29 first ($t_{fe} = 8.37\,nm$) (red and orange lines).

4.5 Limits and corrections of the Poole-Frenkel model

As evidenced with this study, Poole-Frenkel emission represents the dominant leakage mechanism in the FeCap stack. However, PF underestimates the current detected in the thinnest device class. Considering the PF equation:

$$J_{PF} = q\mu N_C E \cdot \exp\left[\frac{-q\left(\phi_T - \sqrt{\frac{qE}{\pi\varepsilon_0\varepsilon_r}}\right)}{kT}\right] \tag{4.1}$$

It is possible that important parameters, such as the electron drift mobility μ, conduction band density of states N_C, and trap depth ϕ_T, are not constant as supposed but change with ferroelectric thickness, increasing PF current especially for the thinnest device. As remarked previously, studies on the dependency of these parameters on thickness are lacking in hafnia-based ferroelectrics, therefore the considerations made in this section will be based partly on studies conducted also on other non-ferroelectric oxides and semiconductors.
The trap depth and the conduction density of states could vary if the nature and concentration of traps changed with thickness. It is important to remark that the main type of defects and traps in hafnia-based ferroelectrics are oxygen vacancies[39], whose charge, concentration, and distribution depend on the deposition process and conditions, eventual doping, and electrode materials used[49], which are the same for all device classes. Therefore, it is not unreasonable to assume that the types and concentration of oxygen vacancies generated do not change with ferroelectric thickness. Since the trap depth refers to the energy levels of these oxygen vacancies, ϕ_T can be considered constant with respect to ferroelectric thickness. Interestingly, the unnatural change of trap depth necessary to fit the experimental data has been already documented in a study investigating gate leakage through a $SiO_2 - HfO_2$ gate bilayer in a MOS transistor[50]. In a much recent study, Wu et al. take inspiration from [50], suggesting to abandon PF for the more complete ITAT-MPEC model (Inelastic Trap-Assisted Tunneling Multi-Phonon Electron Coupling), which fits the experimental currents without changing the trap depths[51]. Instead, another study retains PF conduction and integrates it with ITAT[52].
Regarding oxygen vacancy concentration, a study conducted on ALD-deposited ZnO reports that

the oxygen vacancy density decreases with thickness due to improved crystallinity and reduced grain boundaries for thicker films[53]. An increase in crystallinity and grain size with thickness, thus the reduction of grain boundaries, has been reported for HfO_2 as well[54, 55]. However, these studies report that HfO_2 is mainly amorphous below a critical thickness, around $12\,nm$, which would imply that the all ferroelectric layers in our devices are amorphous, contradicting the ferroelectricity detected, typical of the polar orthorhombic crystalline phases. In fact, other studies report that the formation of crystalline ferroelectric phases in HfO_2 and HZO can be induced at thicknesses lower than the critical thickness when doping, strain due to electrodes and dopant agents, and deposition temperatures around 300°C are employed [56, 57]. Therefore, it is clear that our ferroelectric HZO thin films are not amorphous as supposed, but their crystallinity increases with thickness, reducing the available grain boundaries. These crystalline defects are critical for the formation, migration, and aggregation of oxygen vacancies in hafnia-based ferroelectrics as well[49]. Consequently, the trap density that is obtained by integrating the conduction band density of states over energy[58] is not constant because the concentration of oxygen vacancies, hence trap sites, decreases with increasing thickness. Therefore, with the thinnest device having the highest density of trap states, the conduction density of states N_C will increase as well, hence augmenting PF accordingly.
Differently from ϕ_T and N_C, the electron drift mobility is known to vary with many parameters such as temperature, electric field, and trap density. The temperature is constant, thus the mobility can vary only due to the electric field and trap density difference between device classes. Considering a thickness variation from 6.45 nm to 10.63 nm and a maximum voltage sweep amplitude of 3 V, the electric field over the ferroelectric layer decreases from 465 MV/m for the thinnest devices to 282 MV/m for the thicker ones. Therefore, we must consider the mobility to be in the high field regime (> 100 MV/m). Unfortunately, the electron drift mobility generally reduces as the field increases[59, 60]. The drift mobility also decreases with trap density[60]. Despite the reduction in electron mobility, the increase in trap conduction density of states can still be larger, prompting a net increase of the PF current. An increase of the PF current with the trap density is also physically plausible, since a higher traps density hinders conventional drift carrier transport but provides more trap sites for trap-assisted conduction[61], which includes Pool-Frenkel. Another limitation of the PF model is that assumes perfect trap compensation[62], which means that the density of donor-like traps N_{tn} is the same of acceptor-like ones N_{tp}. Considering different densities and trap energies (depths) can significantly influence the slope and the value of the PF current[62]. Taking the donor-like traps as reference, in case of under-compensation $N_{tn} > N_{tp}$, the PF current is higher than with perfect compensation. The opposite occurs in case of over-compensation, $N_{tn} < N_{tp}$. The situation is reversed for acceptor-like traps, where under-compensation implies $N_{tp} > N_{tn}$. However, assessing how oxygen vacancy formation relates to these trap types when varying the ferroelectric thickness exceeds the focus of this study. In summary, the PF model can be corrected by accounting for the increase of oxygen vacancy concentration[49, 53, 54], conduction band density of states[58], and mobility reduction with ferroelectric thickness[59, 60], and under or over-compensation of donor and acceptor-like traps[62]. Other studies propose to either integrate PF with inelastic trap-assisted tunneling (ITAT)[52] or to replace it completely with the ITAT-MPEC model[51].

Chapter 5

Conclusions and future perspectives

5.1 Summary and conclusion

This work focused on modeling and validating a conduction model that simulated the leakage currents flowing in the ferroelectric and electrode-ferroelectric interface layers of hafnia-based ferroelectric capacitors. The leakage model of choice has then been implemented in a FeCap compact model.
The ferroelectric capacitors available for this study consisted of five layers, namely a TiN bottom electrode (BE) and a BE-ferroelectric TiO_2 interface layer, a HZO ferroelectric layer, and a W top electrode (TE) with a negligible ferroelectric-TE WO_x interface layer [18]. These devices were divided in three classes depending on the thickness of the ferroelectric, with identification number 28/29/30 for $t_{fe} = 10.63/8.37/6.45\,nm$ respectively. Starting from a simplified leakage model, defined as *resistive*), in which interface leakage was modeled with resistors and ferroelectric leakage with an exponential, symmetric around zero diode-like current, two increasingly detailed leakage models, termed *exponential* and *physical*, have been implemented. The *exponential* model substitutes the interfacial leakage resistors with the same exponential current used for the ferroelectric. Conversely, the *physical* model replaces all exponential currents with three conduction mechanisms which are dominant in nanometric thin films[27], i.e. Poole-Frenkel emission (PF), Fowler-Nordheim tunneling (FN), and Schottky emission (SE). The *resistive*, *exponential*, and *physical* leakage models have been implemented in the FeCap compact model and compared by fitting available PUND and switching kinetics measurement data. The fitting parameters have been calibrated on the experimental data of a FeCap with $t_{fe} = 8.37\,nm$. Consequently, the physical model has been chosen to be implemented definitely in the FeCap compact model. The behavior of each leakage current implemented in the physical model has been studied for both the ferroelectric layer and the bottom electrode interface. Various corner cases of each leakage current, obtained varying the ferroelectric or BE interface thicknesses $t_{fe/be}$, temperature T, and the bottom electrode energy barrier $\phi_{B,BE}$, have been compared over a $0 - 3\,V$ voltage sweep. In the ferroelectric, the currents have been studied varying only the thickness and temperature, and the dominant conduction mechanism was Poole-Frenkel, although Fowler-Norhdeim can become comparable to PF or even dominant for voltages higher than 2.5 V and in the thinnest devices. In the bottom electrode interface, changing only thickness and temperature, the dominant mechanism is Schottky emission. However, changing the interface energy barrier profoundly affects the leakage currents, thus an additional study where the thickness was fixed, and temperature and interface energy barrier varied, was carried out to detect which conduction mechanisms were dominant depending on barrier height. The study unveiled that Fowler-Nordheim and Poole-Frenkel can become dominant over Schottky emission as the energy barrier increases. For $\phi_B = 0.3 - 0.85\,eV$ Schottky emission was the dominant current, but between $\phi_T = 0.85 - 0.88\,eV$ Fowler-Nordheim started to become dominant over Schottky emission. Further increasing the energy barrier, $\phi_B = 1.0 - 1.5\,eV$, gradually suppressed both Schottky emis-

sion and Fowler-Nordheim, leaving Poole-Frenkel to dominate conduction. The voltage drop on the interface increased with ϕ_B meaning that electrodes materials that form low-ϕ_B interfaces, such as tungsten[45, 46], are ideal for low voltage FeCap operations, since the majority of the voltage drop is on the ferroelectric. Moreover, since the dominant leakage mechanisms for $\phi_B < 0.85\,eV$ and $\phi_B \geqslant 1.5\,eV$ are SE and PF respectively, then leakage can be reduced by decreasing temperature, and interface defectivity (trap formation) for PF only.
The leakage model has been validated with quasi-static experimental data. Device-to-device variability has been evaluated by collecting measurements on 30 different devices per ferroelectric thickness. The measurements showed the leakage currents increasing with reducing thickness. Cumulative distribution functions have been used to study the device-to-device variability, and highlighted that device class 29, with 8.37 nm thick ferroelectric, exhibited the lowest absolute variability, closely followed by the thickest and thinnest devices (class 28). The thinnest devices (class 30) showed an exponential increase in the device-to-device variability and leakage currents, breaking the quasi-linear current-thickness trend observed in the other device classes. Critical leakage parameters, such as the trap depth ϕ_T, the thickness of the ferroelectric t_{fe}, and the mobility μ, have been fitted using the experimental data. The trap depth, calibrated first, should be independent from ferroelectric thickness, since the nature of traps (oxygen vacancies), depending on the material, should not change. Poole-Frenkel resulted as the dominant conduction mechanism, thus the simulated leakage curves acted almost as pure PF curves. The calibration quickly highlighted that, while an univocal value of ϕ_T equal to 0.97 eV can be found for device classes 28 and 29 (10.63/8.37 nm thick ferroelectric respectively), the thinnest device class requires a lower value $\phi_T = 0.88\,eV$), highlighting a possible limit of the PF model when fitting currents through dielectric thin film thinner than 8 nm. The thinnest devices act as outliers, exhibiting much higher currents and thus requiring a lower trap depth. Each remaining leakage parameter has been fitted singularly, yielding different fitting ranges that have been compared with available literature. Assuming a ferroelectric thickness variation of $\pm 10\%$, fitted the experimental data, and the literature reports a usual thickness variability, for atomic layer deposition, of 4% [47], which falls within the range found. Regarding the mobility, the calibration started from $\mu = 15\,m^2V^{-1}s^{-1}$, similar to the mobility in SiO_2[48], and found a variability range of $10 - 30\,m^2V^{-1}s^{-1}$. Possibly, the mobility can be treated as a fitting parameter. With the parameter ranges obtained from this analysis, a set of leakage parameters that fit the experimental data has been calibrated. The maximum ferroelectric thickness variability assumed has been 4%, allowing the same range of mobility found in the single parameter analysis, i.e. $10 - 30\,m^2V^{-1}s^{-1}$. However, Poole-Frenkel cannot fit the experimental data with an univocal value of trap depth, indicating that the PF model has to be corrected either by considering how its parameters vary with thickness[49, 53, 54, 58–60, 62] or integrating it with additional conduction mechanisms (like inelastic trap-assisted tunneling[52]), or substituted entirely[51].

5.2 Future perspectives

This study represents the starting point of a comprehensive study of leakage in hafnia-based ferroelectric capacitors. The leakage model showed in this study can be updated to include additional conduction mechanisms that can account for the deviations from a linear current-thickness trend that occur in thinner devices, as seen in the thinnest FeCaps. The anomalous current increase can be fitted by considering an increase in oxygen vacancy concentration, thus traps sites, for lower thicknesses. Although the electron drift mobility reduces with the trap sites density, its reduction could be outweighed by the increase in trap density, leading to a net increase in the PF current. Future studies could also focus on integrating PF with other conduction mechanisms such as inelastic trap-assited tunneling[52], or replacing it completely with a new model such as ITAT-MPEC[51]. The corrected or integrated PF model, or the the newer ITAT-MPEC, could then be validated and compared quantitatively, choosing the model that fits the data most accurately. The leakage

parameters obtained from the calibration of a refined version of the leakage model can be used to fit PUND and kinetics data, and the effect of the leakage model over these two measurements can be quantified. Additional measurement campaigns including PUND, kinetics, and endurance measurements can be carried out in order to assess the entity of device-to-device variability and the presence of other effect such as wake-up and imprint, and to study ferroelectric phase evolution with cycling, and cycle-to-cycle variability. A multi-frequency PUND can also be carried out in order to observe the effect of different pulse duration on the switching current and polarization. Multiple kinetics with different types of pulse profiles, e.g. triangular, rectangular, trapezoidal, can be executed as well to check whether different profiles influence the switching behavior of the FeCaps.

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