POLITECNICO DI TORINO

Master's Degree
in Nanotechnologies for ICTs

Master's Degree Thesis

Investigation and development of a graphene electroburning platform for reliable single-molecule electrode fabrication

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Academic Year 2023-2024

Summary

Molecular electronics has been considered a beyond-CMOS platform to pursue the scaling of electronic devices, by pushing it to the single-molecule level, and by using the paradigm in which individual molecules constitute the active components in electronic circuits, performing a variety of functions such as transistors and sensors. For many years, molecular electronics has traditionally advanced from materials such as gold electrode with nanogap formation methods such as electromigration and mechanical break junctions. Alternatively, graphene has opened a new possibility of acting as a stable electrode at room temperature for a long period of time and its unique electronic properties have been analyzed as a possible material to be the electrode for single-molecule electronics. Since atoms in graphene are stable at room temperature owing to their sp^2 C-C covalent bonds, graphene can be a natural electrode for conjugated molecules, offering, at the same time, good orbital hybridization with the molecular channel and thus more natural support to transport in molecular devices.

An established method for creating nanogaps in graphene is feedback-controlled electroburning. This method can be an effective way to form nanogaps in single or few-layer graphene if certain prerequisites are met. This approach is related to the chemical reaction of carbon atoms of graphene with oxygen, and the process evolution is controllably performed using a feedback control system.

In the first part of this work, a literature review is conducted on the graphene electroburning process, with a description of the main features and reasons for employing graphene as an electrode with its key characteristics. Additionally, the potential of graphene as an electrode is investigated through a study of its physical properties.

Then, in its second part, the thesis focuses on the development of a feedback-controlled algorithm for the graphene electroburning-based nanogap formation. The algorithm is implemented in LabVIEW for an FPGA hardware platform. The system uses analog input voltage and analog output current modules with the FPGA-based controller and it is possible to achieve fast-speed feedback controlled algorithm with resolutions up to a few µs sampling rate. Then, using simulations in Synopsys' QuantumATK® software, the graphene electroburning process is analyzed in detail through the comparison of graphene nanoribbons with different atomic configurations and their properties such as current - voltage characteristics and transmission spectrum are reported to show the graphene as an electrode with different geometries and nanogap structures.

The thesis findings are consistent with literature results from other groups, confirming the potential of electro-burned graphene electrodes as a reliable electrode for single-molecule electronics. Future works should focus on the testing and setup of the developed system on a real pre-patterned graphene sheet, addressing also higher sampling rates and time resolution.

Acknowledgements

I would like to express my gratitude to Ph.D. F. Mo and M.Sc. F. Ravera for their valuable suggestions and guidance throughout my thesis work.

I am also deeply thankful to Prof. M. Graziano and Prof. G. Piccinini for welcoming me into their research group and providing their support.

Lastly, I wish to express my heartfelt gratitude to my parents. To my mother, for her constant and unwavering support throughout my life. To my late father, whose enduring curiosity continues to inspire me, even in his absence, as I reach this achievement.

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Chapter 1

Introduction

The advancement of nanoelectronic systems and devices requires the downscaling of electronic components, such as transistors, in alignment with Moore's law. However, the miniaturization of silicon-based semiconductor devices has reached its intrinsic limitations. As a result, molecular electronics has emerged as a promising area of research. Single-molecule electronics represent a cutting-edge field in nanoelectronics, where a molecule is positioned between source and drain contacts, functioning similarly to a transistor with a three-terminal configuration. This setup enables current flow regulated by the applied bias across a pair of terminals. Therefore, it is crucial to investigate single-molecule electrodes with a focus on electron transport mechanisms.

An important factor to consider in single-molecule electrodes is the choice of electrode material, which can be conductive, such as gold or platinum. Recently, graphene has gained attention as a semiconductive material under specific conditions, exhibiting capabilities as an electrode. To enable graphene use in single-molecule electronic devices, it is necessary to create nanogaps in the graphene electrode structure, allowing the molecule to be positioned within the nanogap between the two sides of the electrode.

The creation of nanogaps with high yield is a challenge in nanoelectronic devices, both for conductive metals and semiconductive carbon-based materials like graphene. In recent years, various techniques have been developed for nanogap formation, particularly for metal contacts such as gold, to advance nanoelectronic applications.

Electroburning is a technique used to create nanogaps in graphene by generating nanoscale separations at room temperature through the reaction of graphene's carbon atoms with oxygen. This reaction takes place in localized high-temperature regions generated by Joule heating. Compared to metals like gold, graphene demonstrates superior stability at room temperature. [1]

To control the nanogap formation process in graphene and prevent the creation of large gaps, it is required to regulate the process over time. This is achieved through the feedback-controlled electroburning technique, which uses a feedback system to make the electroburning process more precise. Another critical factor in improving the yield of nanogap fabrication in graphene is the pre-design of its shape. A well-known structure, the "bow-tie" design, has been shown to significantly enhance the efficiency of nanogap formation in graphene.[2]

1.1 Organization of this work

Introduction

- Chapter 1 provided an overview of the general context of this thesis, highlighting the motivations and significance of developing a graphene electroburning platform for reliable single-molecule electrode fabrication.

Part I

- In Chapter 2, the literature review starts by discussion on two techniques for nanogap formation in metals. Then is followed by an overview of carbon-based materials, leading to a detailed discussion of the electroburning technique for creating nanogaps in graphene. The description includes the fabrication process and an explanation of the feedback-controlled electroburning algorithm as presented in the literature.
- In Chapter 3, the theoretical physical properties of graphene are discussed. Focused on its band structure, density of states, charge transport mechanisms, and the influence of edge effects in graphene nanoribbons.

Part II

- In Chapter 4, the transport properties of graphene, including I-V characteristics, transmission spectrum, and density of states, are analyzed. These analyses are performed using QuantumATK software to simulate three different atomic configurations, examining graphene's behavior as an electrode both with and without a bow-tie nanogap structure.
- In Chapter 5, the primary contribution of this thesis, the development of a feedback-controlled electroburning platform for graphene nanogap formation is presented. This involves the design of a system with an FPGA-based controller and the creation of an algorithm in the LabVIEW program, developed by the student and inspired by existing literature.

Conclusion

- Chapter 6 concludes the thesis by summarizing the key findings and contributions while offering recommendations for future research on this topic.

Part I

part one

Chapter 2

Literature review

Electronic devices are going to be smaller and smaller; Single-molecule devices, in which individual molecules are utilized as active electronic components, have blossomed into a powerful platform for exploring novel phenomena at the molecular scale and paving the way for electronic devices downscaling to the single-molecule level.[1] In recent years, graphene has become an attractive material for research in the molecular electronic field. In experiments, gold is the most preferred electrode material in metal-molecule-metal junctions, because gold is chemically inert under ambient conditions and many anchor groups can bond to the gold surface. However, the high mobility of surface atoms of gold at room temperature leads to the instability of the molecule-gold bond in ambient conditions. The covalent bond structure gives stability to graphene at room temperature. Another advantage is that it allows for a large variety of possibilities to anchor diverse molecules as compared to metallic electrodes. While for the gold electrode, thiol and amine linkage is widely used, the carbon-based materials can not only be functionalized covalently through organic chemistry techniques but also via π - π stacking interactions of aromatic rings. Another advantage is the fact that extremely thin electrodes, ranging from (few-layer) graphene to carbon nanotubes, can be prepared. Graphene, known for its excellent stability at room temperature, can serve as an electrode in devices like transistors, sensors, and switches.

2.1 Top contact junctions

2.1.1 Mechanically controlled break junction

The mechanically controlled break junction (MCBJ) technique is used to fabricate electrodes with precisely adjustable separations down to a few nanometers for metal electrodes.[3] As the name implies, the distance between the electrodes is controlled by mechanical forces. the A lithographically defined metallic bridge with a notch is attached to a flexible, elastic substrate, typically made of a phosphor-bronze sheet. This substrate, serving as a bending beam, enhances flexibility and is compatible with electron beam lithography, supporting options for metal electrode deposition. A three-point bending geometry is

used, where the substrate is bent by applying force at its center with a piezo-controlled pushing rod. The metallic wire is mechanically stretched until it breaks, creating a nano-gap between two electrodes. This design allows for sub-picometer precision in controlling the pushing rod's displacement and controllable at the nanometer scale. [4]

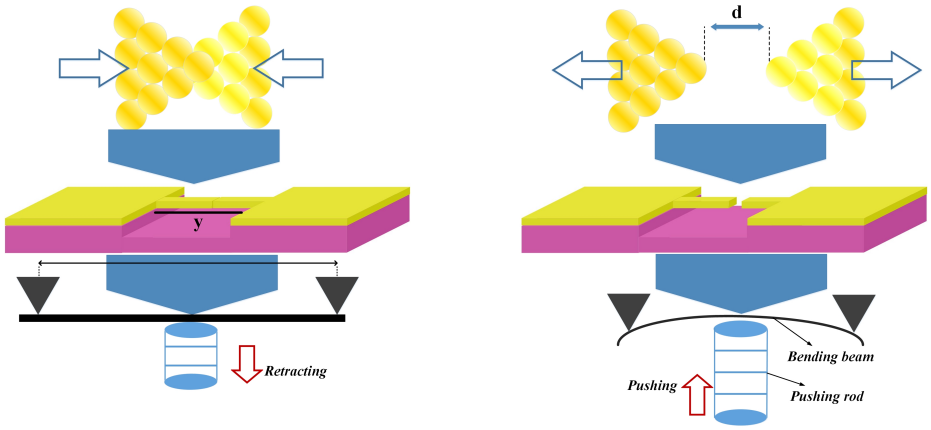


Figure 2.1. Schematic of the Mechanically controlled break junction.

The MCBJ outstanding stability enables room temperature experiments to probe stability and conductance of single molecule junctions.[4] Combined with the ability to finely adjust the nano-gap without polluting the junction, this technique allows for a large number of measurements on a target molecule, enabling statistical analysis of transport measurements.[5]

A key advantage of this system is that nano-gaps form only during the experiment, making the cleanliness requirements for sample fabrication less stringent. Molecules can self-assemble onto the gold wire before the breaking process.[6] Once the nano-gap is created, the metal electrodes are coated with a monolayer of molecules. By controlling the junction, while conductance as the nano-gap size is reduced, the formation of a single-molecule junction can be recognized. The MCBJ technique has proven useful in studying metal-molecule contact stability.[7]

Although MCBJs have led to fundamental research, they do have some limitations.[8] Developing integrated devices is challenging with MCBJs due to the constraints of bulky piezo components, which limit the larger gap size and make larger gaps difficult to create. Thermal effects are also a concern; the high electric fields applied can result in electron-phonon coupling, induce local heating, and lead to the junction instabilities.[9]

2.1.2 Electromigration

Electromigration is a process in which ions are gradually transported at high electrical current densities due to the momentum transfer from conduction electrons to lattice ions. It is well studied as a major failure mode in microelectronics[10] and has now been applied

to the fabrication of nano-gap electrode.[11, 12] A voltage ramp is applied to a lithographically defined metal constriction, and electromigration of metal atoms happens, eventually leading to the breakage. This results in the formation of two nano-electrodes separated by distances as small as 1 to 2 nm. Molecules can be introduced either before or after the nano-gap is formed. Depositing molecules before the nano-gap formation is preferred, as it helps reduce contamination within the gap.[8]

The main difference of electromigrated break junctions (EBJs) compared to mechanically controlled break junctions is the solid contact between the electrodes and the substrate, offering four main advantages. First, this setup provides excellent mechanical stability, which is important for studying electron transport in molecular junctions exposed to external electromagnetic fields.[4] Second, there are no precise requisites needed for the substrate, unlike MCBJs, which require flexible substrates. Third, the planar architecture is ideal for integrating large arrays for applications. Finally, EBJs allow for the creation of three-terminal devices by using the substrate as a gate electrode. This capability enables the fabrication of devices such as single-electron transistors. [11]

A key factor in achieving high-quality junctions is controlling the local temperature in the gap, as high current densities can cause Joule heating.[13] This can result in effects such as melting, which creates large gaps, damages molecules, and forms metal debris in the gap. These metal islands interfere with the insertion of molecules and unclear the intrinsic properties of the molecules. This issue can be mitigated by reducing the total series resistance of the system and maintaining a low temperature, as demonstrated with EBJs fabricated on free-standing transparent SiN_x membranes. When the total series resistance is minimized, the resulting nano-gaps can be clean and free of debris. [14]

Improved yield and reproducibility have been achieved through the implementation of feedback control. Instead of relying on a single voltage ramp, the bias voltage can be adjusted by feedback control based on the junction resistance. This approach prevents thermal runaway, which could create large gaps. Feedback control has enabled the parallel fabrication of a 15-junction array in a single step by ensuring that the resistance between junctions remains lower than that of the individual junctions.[15] This method evenly distributes power dissipation across the junctions, facilitating the successful fabrication of arrays and leading to the development for integrated circuits of molecular devices.

To summarize, the limitations of using metal (gold) nano-electrodes in MCBJs and EBJs are mentioned. A significant drawback of EBJs compared to MCBJs is their inability to adjust the gap size. A combination of the two techniques can minimize this limitation, but it also restricts the range of achievable gap sizes and introduces additional challenges associated with MCBJs. The high atomic mobility of gold nano-electrodes is a significant challenge for stable room-temperature device applications.[16] Replacing gold with other metals is not ideal since many metals go to oxidation in ambient conditions. Due to these fundamental challenges, carbon-based electrodes, such as graphene, have emerged as promising alternatives for molecular electronics, which will be explored in the following section.

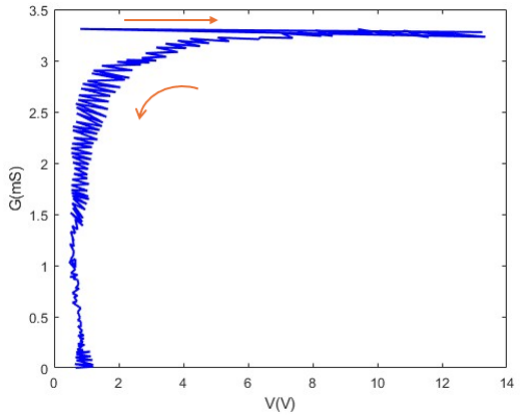


Figure 2.2. Conductance as a function of the bias voltage during the feedback-controlled electromigration process.

2.2 Carbon based electrode

Carbon-based electrodes exhibit several advantages over gold electrodes. CNTs offer a carrying current density up to 10^9 A/cm^2, which is 1000 times greater than that of noble metals.[17] Similarly, graphene demonstrates exceptional properties, including extraordinary thermal conductivity, high electron mobility, and impressive current density as well as the ability to support ballistic transport at room temperature.[18, 19] An alternative approach for creating stable electrodes with nanometer-scale separations is the use of (sp^2-) carbon-based materials. Due to their covalent bonding structure, these materials maintain stability even at high temperatures, far beyond room temperature. In contrast to more bulky metallic electrodes, these thin carbon-based electrodes minimize screening of the applied gate field, thus enhancing gate coupling. Driven by these benefits, nanogap electrodes based on carbon nanotubes have been created through oxygen-plasma etching, using a PMMA mask to define the gap, or through electrical breakdown methods. However, achieving precise control over gap sizes below 10 nm remains challenging, making it difficult to contact single molecules. Alternative methods that could lead to nanogap electrodes include atomic force microscopy (AFM), nanolithography of graphene, anisotropic etching catalyzed by nanoparticles, graphene nanogaps formed through mechanical stress, and electrical breakdown of graphene. [18]

Two main experimental techniques have been developed to create graphene nanogaps: dash-line lithographic plasma etching and feedback-controlled electroburning. The plasma etching method involves the localized cutting of graphene with oxygen plasma through an array of holes formed by dashed-line e-beam lithography in a PMMA layer. The electroburning technique, on the other hand, uses Joule heating to induce graphene breakdown in the presence of oxygen, with the process precisely controlled via a feedback system. [1]

The plasma etching approach uses chemical vapor deposition (CVD) grown graphene point contacts. By over-etching a lithographically defined pattern, this method produces

nano-gaps as small as one nanometer or less. The use of large-area CVD graphene allows for the creation of nano-gap arrays across a wafer with precise positional control, however, the yield of the plasma etched devices is only 33%. [20]

The method involves the breakdown of graphene through a current-induced process, where the nano-gap size can be controlled by using Joule heating to induce graphene breakdown with partial pressure of oxygen [1] or by using feedback-controlled electroburning, a technique similar to feedback-controlled electromigration. This feedback mechanism enables precise control over the gap size, typically in the range of 1–2 nanometers. Although electroburning achieves a high fabrication yield (92% to 95%), the placement of the nanogaps is less controlled due to the random nature of the process. [20]

Despite these advancements, challenges remain in fabricating graphene nano-electrodes. One issue is the complexity and resulting low yield of device fabrication. When combined with pre-patterning, the electroburning method can achieve precise control over gap size and positioning, reaching yields as high as 95 percent. Some groups combine both techniques to enhance the yield by optimizing certain pre-patterning steps.[20] However, the electroburning process is time-consuming, especially in applications requiring large arrays of single layer graphene (SLG) junctions.

2.3 Electroburning

2.3.1 Fabrication

We begin with a brief overview of the fabrication technique that different groups have used for the fabrication of nanogap junctions in graphene electrodes. There are two types of graphene used in this approach, some groups used few-layer graphene (FLG) while others used single-layer graphene (SLG).

Prins et al [18], used FLG material. Few-layer graphene flakes (3–18 nm thick) are deposited onto degenerately doped silicon substrates coated with 280 nm of thermal silicon oxide, using mechanical exfoliation of kish graphite. They utilize standard wafer protection tape, which minimizes adhesive residue on the substrates. Selected few-layer graphene flakes are then patterned with Cr/Au electrodes using electron-beam lithography, followed by metal evaporation and a lift-off process in cold acetone and dichloroethane. The initial device resistances at low bias range from approximately $200\,\Omega$ to $3k\,\Omega$.

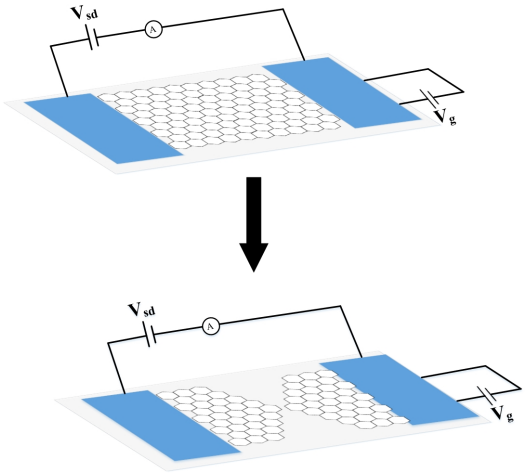


Figure 2.3. Schematic of the feedback-controlled electroburning process, before (top) and after (bottom), the formation of nanometer sized gaps in few-layer graphite flakes.

Lau et al [20], were used single layer graphene. They nano-gap fabrication approach involves a lithography process with a minimum feature size of 200 nm, followed by a feedback-controlled electroburning process that creates gaps of 0.5–2.5 nm. Out of 1079 processed devices, 776 nano-gaps were successfully formed. This study characterizes the devices before and after electroburning, examining individual nano-gap geometries through atomic force microscopy (AFM) and modeling the current density in their device structure. Graphene devices were fabricated using a passive-first, active-last process, where the graphene is transferred onto a pre-patterned silicon chip. Single-layer graphene (SLG) was grown in a chemical vapor deposition (CVD) furnace at 1090 °C, using a 1% CH4:Ar gas mixture at atmospheric pressure on a liquid copper. PMMA was spun onto the SLG/copper stack before etching away the copper with a 0.1 M ammonium persulfate solution. The PMMA/graphene stack was then rinsed in deionized water and transferred onto a pre-patterned 1 x 1 cm2 Si/SiO2 chip. Each chip contained 540 pairs of Cr/Au electrodes patterned through electron beam lithography and metal evaporation. After SLG transfer onto the metal electrodes, it was patterned into notched ribbons using electron beam lithography and oxygen plasma etching. Prior to electroburning, the devices were annealed at 350 °C for 1 hour in an Ar atmosphere to remove residual resist.

pre-patterning

As mentioned before, pre-patterning steps will lead to increase in the yield of nanogap formation. Xu et al [2], reported the differences in the yield with and without the pre-patterning considerations. They reported two methods in the process of fabricating graphene nanogap electrodes. In first method, devices are fabricated using exfoliated graphene flakes with typical widths ranging from 2 to 10 µm. In the second method, exfoliated graphene flakes are first patterned into a bowtie shape through lithography and reactive ion etching. For both methods, the subsequent steps involve depositing source and

drain metallic microelectrodes, followed by electroburning to create a gap in the graphene channel.

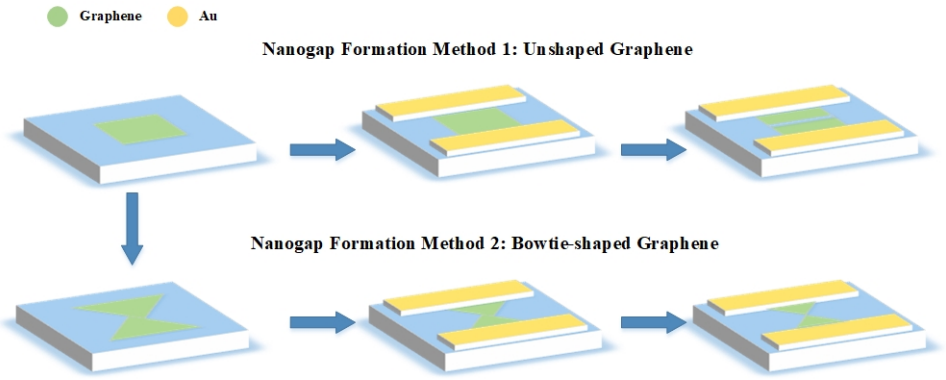


Figure 2.4. Process for fabricating of graphene nanogap electrodes. (top) device fabrication without pre-patterning. (bottom) device fabrication with pre-patterning.

Results of this group investigation[2], show that shaping a constriction in the bowtie channel dramatically increases the yield of successful nanogap formation from 30% in unshaped graphene to 80% in bowtie-shaped graphene.

2.3.2 Feedback controlled electroburning

Different approaches to feedback-controlled electroburning processes exist, varying based on the sampling rates used in the system. Here, two methods reported by scientific groups are compared, the first employs a sampling rate of 200 µs [18] while the second uses 20 µs. [1]

Feedback-controlled electroburning process with 200 µs sampling rate

The feedback-controlled electroburning process is conducted in ambient air at room temperature, utilizing a control scheme similar to methods used in metallic nanowire electromigration. A voltage ramp of 1 V/s is applied to the graphite flake (FLG), with the current (I) recorded at a sampling rate of 200 μs. Conductance ($G = \frac{I}{V}$) is monitored, and the feedback is triggered if conductance drops by more than 10 percent within the last 200 mV of the ramp. Upon detecting such a drop, the voltage is immediately reduced to zero over a 10 ms interval, and a new voltage ramp is initiated. This process is repeated, gradually narrowing the graphite flake.

During the first voltage ramp (blue trace in Figure 2.5.), nonlinear I-V characteristics appear, likely due to the removal of contaminants on the flake through current annealing.

As the voltage is further increased, the initial electroburning event is observed, characterized by a downward curvature in the I-V plot, occurring here at $V = 4.8\,\mathrm{V}$ and $I = 15\,\mathrm{mA}$. At this point, the feedback mechanism resets the voltage to zero, and a new ramp is applied. Throughout the electroburning progression, conductance decreases in discrete steps, and the voltage required to induce further electroburning events is reduced (indicated by the green arrow in Figure 2.5.). They conducted electroburning on 38 samples, of which 35 (92%) reached a low-bias resistance range between 500 MΩ and 10 GΩ. In the remaining cases, the feedback system was too slow to respond, resulting in gaps with infinite resistance ($> 100\,\mathrm{G\Omega}$). [18]

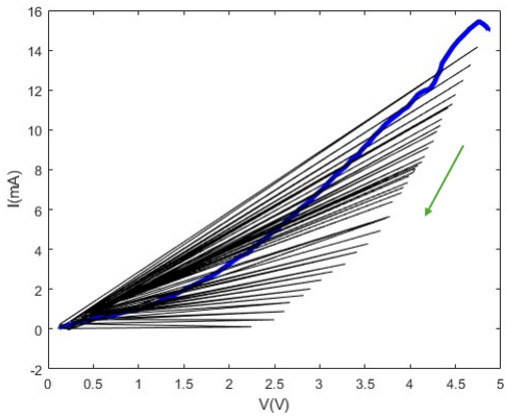


Figure 2.5. I-V traces showing the evolution (green arrow) of the feedback-controlled electroburning process with 200 µs sampling rate. The initial I-V trace is shown in blue.

Feedback-controlled electroburning process with 20 µs sampling rate

In this case, they employed an optimized fast-speed feedback-controlled electroburning process to create nano-gaps in graphene. The electroburning was carried out same as previous report in air at room temperature. A voltage ramp (1 V/s) was applied to the source-drain electrodes, while the corresponding source-drain current was continuously recorded at a sampling rate of 50 kHz. The conductance measured at 0.1 V was set as the reference value. When the conductance decreased by 5 percent, the applied bias was reduced by 20 percent immediately. The final conductance at the end of each cycle was used as the reference for the next cycle. This voltage ramping process was repeated until the target resistance (500 MΩ and 1 GΩ) was achieved. [1]

The primary difference between these two methods lies in how the applied bias is adjusted. In the first method, the applied bias is reset to zero and then increased again, while in the second method, the applied bias is reduced by 20% from the previous value.

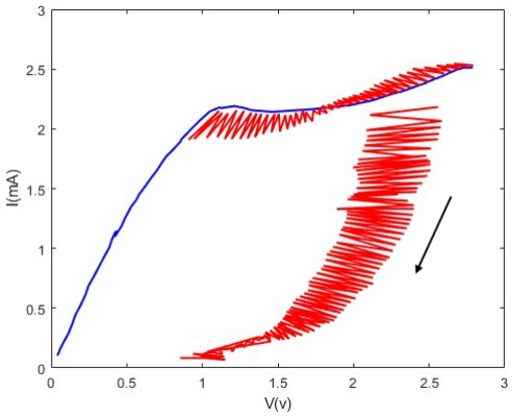


Figure 2.6. I-V traces recorded during the feedback-controlled electroburning process with 20 µs sampling rate. The initial I-V trace is shown in blue.

2.4 Conclusion

While feedback-controlled electroburning has demonstrated a high yield (>95%) for nanogap formation, precise control over the nanogap's location remains challenging. To address this, a constriction is introduced on the graphene, enabling nanogap fabrication with both accurate positioning and high yield due to the localized increase in current density and temperature at the constriction point. Specifically, single-layer graphene is first transferred onto a substrate and shaped into a bow-tie structure through electron beam lithography (EBL) and oxygen plasma etching. Next, feedback-controlled electroburning is applied to create a nanogap at the constriction. Statistical analysis indicates that this combined approach achieves 0.5–2.5 nm nanogaps with a fabrication yield of approximately 71 %. [20]

Chapter 3

Graphene

3.1 Properties

Graphene is a two-dimensional allotrope of carbon in which all carbon atoms are covalently bonded in a single plane. The structure forms a planar honeycomb lattice, characterized by a hexagonal arrangement of carbon atoms. The honeycomb lattice dedicate graphene with exceptional properties, including high electrical conductivity, mechanical strength, and thermal stability, making it a focus of extensive research in various scientific and technological fields. Graphene can transform into various forms: wrapping it into a sphere creates buckyballs, rolling it into a cylinder forms carbon nanotubes, and stacking multiple graphene layers results in graphite. Additionally, cutting graphene into narrow strips produces nanoribbons, which have become a significant focus of current research. Understanding the properties of graphene is crucial, as it provides the foundation for explaining nanoribbons' electronic behaviors. This insight is essential for exploring their potential applications in advanced materials and nanotechnology. In graphene, the 2s orbital interacts with the $2p_x$ and $2p_y$ orbitals to form three sp^2 hybrid orbitals, as illustrated in Figure 3.1. These sp^2 orbitals create three strong covalent bonds known as σ-bonds, which are localized along the plane connecting neighboring carbon atoms and provide graphene great mechanical strength. In addition to the σ-bonds, $2p_z$ orbitals form covalent π-bonds. The π-bond electron cloud is distributed perpendicular to the plane of the carbon atoms and is relatively delocalized due to the weaker binding of $2p_z$ electrons to the nuclei. These delocalized π-electrons are crucial for the unique electronic properties of graphene to understand their behavior and applications. [21]

3.2 Band Structure

Graphene is a two-dimensional material composed of carbon atoms arranged in a hexagonal lattice. This structure can be described as a triangular lattice with a basis of two carbon atoms per unit cell. The lattice vectors are defined as :

$$\mathbf{a}_1 = \frac{a}{2}(3, \sqrt{3}), \quad \mathbf{a}_2 = \frac{a}{2}(3, -\sqrt{3}),$$

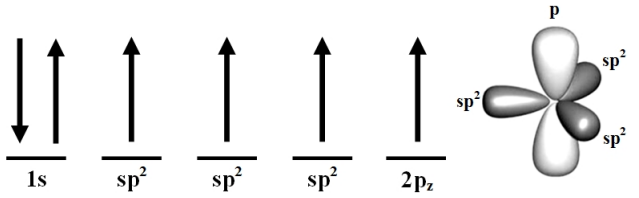


Figure 3.1. Left: The arrangement of electrons and their relative spin in graphene. Right: Illustration of the graphene orbitals.

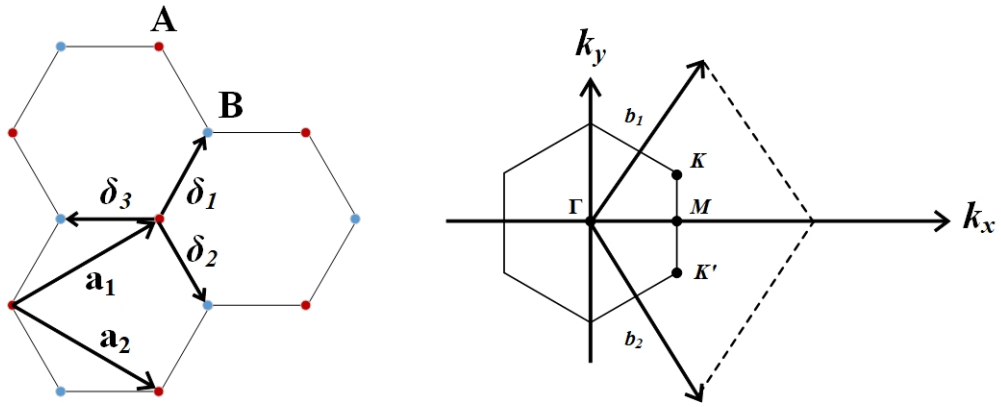


Figure 3.2. Left: Honeycomb lattice structure of graphene. Right: Corresponding Brillouin zone with the basis vectors of the reciprocal space. The Dirac cones are located at the K and K' points.

where $a \approx 1.42\,\text{Å}$ is the carbon-carbon bond length. The reciprocal lattice, critical for understanding electronic behavior, is described by the vectors:

$$\mathbf{b}_1 = \frac{2\pi}{3a}(1, \sqrt{3}), \quad \mathbf{b}_2 = \frac{2\pi}{3a}(1, -\sqrt{3}).$$

The Dirac points are particularly important, located at the corners of the graphene Brillouin zone (BZ). These points, labeled $\mathbf{K}$ and $\mathbf{K}'$, are given by:

$$\mathbf{K} = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a}\right), \quad \mathbf{K}' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a}\right).$$

The three nearest-neighbor vectors in graphene's real-space lattice, denoted by $\boldsymbol{\delta}$:

$$\boldsymbol{\delta}_1 = \frac{a}{2}(1, \sqrt{3}), \quad \boldsymbol{\delta}_2 = \frac{a}{2}(1, -\sqrt{3}), \quad \boldsymbol{\delta}_3 = -a(1, 0)$$

The Γ-point is located at the center of the Brillouin zone, while the M-points are positioned at the midpoints of the zone's edges. The K-points, including K and K', are of particular importance as they are the locations where the conduction and valence bands meet, defining the unique electronic behavior of graphene. [22]

The analytical solution for the electronic band structure of graphene can be derived using an approximation model based on the time-independent Schrödinger equation :

$$H\Psi(k,\mathbf{r}) = E(k)\Psi(k,\mathbf{r}),$$

where H is the Hamiltonian operator, representing the total energy of the system.

$$H = \frac{\hbar^2}{2m}\nabla^2 + \sum U(\mathbf{r}-\mathbf{R}),$$

The first term of the above equation corresponds to the kinetic energy, and the second term corresponds to the potential energy $U(\mathbf{r}-\mathbf{R})$ arising from the lattice atoms. The vector $\mathbf{R}$ corresponds to the position of a lattice point, indicating the shift from one unit cell to another in the periodic structure of the material. By substituting the Hamiltonian into the time-independent Schrödinger equation, we obtain a second-order partial differential equation that governs the behavior of the wave function $\Psi(k,r)$ for an electron in a periodic potential. This form leads to a more complex equation that accounts for the periodicity of the lattice and determines the allowed energy states $E(k)$ for the electron. To solve this, we must find wave function solutions that satisfy the conditions imposed by the crystal's periodic structure, involving techniques such as Bloch's theorem. Bloch's theorem states that the one-particle states in a periodic potential can be chosen so that

$$\Psi(r) = u_k(r)\exp(i\mathbf{k}\cdot\mathbf{r}),$$

where $u_k(r)$ is a periodic function with the periodicity of the lattice, and $\mathbf{k}$ belongs to the Brillouin zone. This implies that

$$\Psi(r+\mathbf{R}) = \exp(i\mathbf{k}\cdot\mathbf{R})\Psi(r),$$

The equation shows that the wave function (Ψ) at a position $\mathbf{r}$ and at a translated position $\mathbf{r}+\mathbf{R}$ is related by a phase factor $e^{i\mathbf{k}\cdot\mathbf{R}}$. [23]

The calculation of the band structure of graphene around the Fermi energy was performed using the tight-binding approximation. In the tight-binding model, only the interactions between the nearest neighbor carbon atoms are considered. Thus, taking into account that the overlap between wave functions for adjacent p_z orbitals is negligible, the energy of π band of graphene is obtained as:

$$E_{C,V}(k) = \pm\gamma\sqrt{1+4\cos\left(\frac{k_y a}{2}\right)\cos\left(\frac{\sqrt{3}k_x a}{2}\right)+4\cos^2\left(\frac{k_y a}{2}\right)}$$

where γ is a parameter representing the electronic interaction between the nearest neighbor carbon atoms in graphene, and is estimated as 3.15 eV . [24]

k_x and k_y are the wave number of the wave function representing an electronic state in π band of graphene. Positive and negative signs in above equation correspond to E_C and E_V, where C and V represent the conduction band and valence band, respectively.

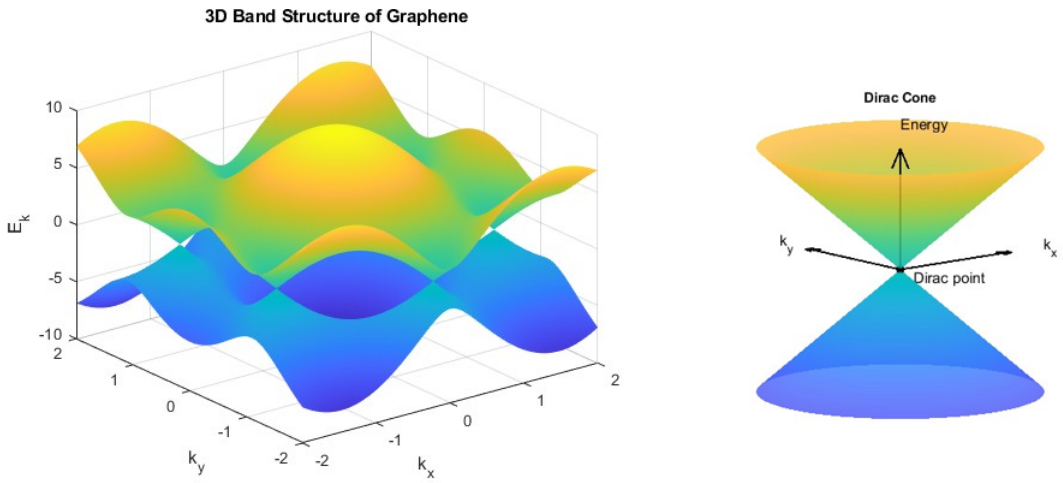


Figure 3.3. Left: The π electronic band structure of graphene obtained by the nearest-neighbor tight-binding model. Right: Dirac cone.

3.3 Density of states

Massless particles in graphene are described using Dirac's relativistic quantum mechanical wave equation. Around the Dirac points, the energy dispersion is linear and can be expressed as :

$$E(k) = \pm\hbar v_F|k| = \pm\hbar v_F\sqrt{k_x^2 + k_y^2},$$

where $\mathbf{k}$ is now expressed in spherical coordinates of the Dirac cone in the right part of figure 3.3., $\hbar$ is the reduced Planck's constant, and v_F is the Fermi velocity. The density of states (DOS), $g(E)$, represents the number of mobile electrons or holes in a material at a given temperature. In two dimensions, the total number of states between an energy E and a small interval dE is given by the differential area in k-space (dA), divided by the area of one k-state.

$$g(E)\,dE = \frac{2g_z\,dA}{(2\pi)^2/\Omega}$$

The factor of 2 is for spin degeneracy, g_z is for cone degeneracy and Ω is the area of lattice. There are six equivalent K-points, and each K-point is shared by three hexagons; therefore, $g_z = 2$ for graphene. To determine dA, consider a circle of constant energy in k-space. The perimeter of the circle is $2\pi k$, and the differential area obtained by an incremental increase of the radius by dk is $2\pi k\,dk$. Therefore, the density of states (DOS):

$$g(E) = \frac{2|k\,dk|}{\pi|dE|}$$

where $g(E)$ has been normalized to the Ω. Substituting from the energy dispersion equation yields a linear density of states (DOS) appropriate for low energies:

$$g(E) = \frac{2}{\pi(\hbar v_F)^2}|E|$$

The absolute value of E is necessary because energy can be either positive (electrons) or negative (holes). At the Fermi energy ($E_F = 0$), the DOS vanishes to zero even though there is no bandgap. This is the reason why graphene is considered a semi-metal in contrast to regular metals that have a large DOS at the Fermi energy. [21]

3.4 Charge transport mechanism

To describe the charge transport mechanisms in single-molecule devices, several theoretical models have been developed. In broad terms, coherent tunneling is explained by Landauer theory. Applying the Landauer-Büttiker theory to a nanoscale device allows expressing the steady state current as :

$$I = \frac{2q}{h} \int \gamma(E)\pi \frac{D(E)}{2} \left[f_1(E) - f_2(E)\right] dE$$

Where, q represents the charge of an electron, h is Planck's constant, $D(E)$ is the density of states, $f_1(E)$ and $f_2(E)$ are the Fermi-Dirac distribution functions corresponding to the source and drain contacts, respectively. If the channel is a single molecule, γ has a simple physical interpretation; it represents the "broadening" of the molecular energy levels due to the finite lifetimes of the electrons in a molecular level. The product $\frac{\gamma\pi D}{2}$ is dimensionless and it represents the number of conducting channels at energy E. We can rewrite the last equation as:

$$I = \frac{2q}{h} \int T(E)M(E) \left[f_1(E) - f_2(E)\right] dE$$

Where $T(E)$ denotes the transmission probability, $M(E) = \gamma(E)\pi\frac{D(E)}{2}$ specifies the number of conducting channels or modes available for transport.

The transmission probability $T(E)$ can be expressed using scattering theory in terms of the mean free path for backscattering, $\lambda(E)$, and the channel length L as:

$$T(E) = \frac{\lambda(E)}{\lambda(E) + L}$$

This equation is derived from the principles of scattering theory, which analyzes the influence of scattering on electronic transport properties. This expression for $T(E)$ is valid across different transport regimes:

- In the *diffusive limit* ($L \gg \lambda, T \approx \lambda/L \ll 1$).
- In the *ballistic limit* ($L \ll \lambda, T \to 1$).
- In the *quasi-ballistic transport regime* ($L \approx \lambda, T < 1$).

The Fermi functions at the source and drain contacts are given by $f_1 = f(E, E_{F1})$ and $f_2 = f(E, E_{F2})$, where E_{F1} and E_{F2} are the Fermi energy levels at the source and drain contacts, respectively. The Fermi function is defined as:

$$f(E, E_F) = \frac{1}{e^{(E-E_F)/k_BT} + 1}$$

where k_B is Boltzmann's constant and T is the absolute temperature. From $\Delta E_F = -qV$, substituting into the above equation:

$$I = [\frac{2q^2}{h} \int T(E)M(E) \left(-\frac{\partial f}{\partial E}\right) dE]V$$

And the conductance can be write as [25]:

$$G = \frac{I}{V} = \frac{2q^2}{h} \int T(E)M(E) \left(-\frac{\partial f}{\partial E}\right) dE$$

3.4.1 Nanogap Modelling for Graphene

To characterize the graphene nano-gaps by measuring low-bias current-voltage (I-V) curves we can exploit the Simmons model, where the current density j in a tunnel junction with a barrier in the x-direction ($\phi(x)$) is described as:

$$j = \frac{4\pi me}{h^3} \int_0^\infty [f_L(\epsilon) - f_R(\epsilon)] \, d\epsilon \int_0^\epsilon T(\epsilon_x) d\epsilon_x$$

The Fermi distribution in the leads is given by a chemical potential μ, and $T(\epsilon_x)$ represents the tunneling probability for an electron with kinetic energy ϵ_x in the x-direction.

$$f(\epsilon) = \frac{1}{e^{-\frac{(\epsilon)-\mu}{k_B T}} + 1}$$

In the low-temperature limit ($k_B T \ll \mu_L, \mu_R, f(x)$), the Fermi distribution effectively becomes a step-function, and current density can be written as:

$$j = \frac{e4\pi m}{h^3} \int_{\mu_R}^{\mu_L} d\epsilon \int_0^\epsilon d\epsilon_x T(\epsilon_x)$$

The tunneling probability for the barrier with constant hight can be derived using the Wentzel-Kramers-Brillouin approximation, which expresses it as:

$$T(\epsilon_x) = e^{-\beta d\sqrt{\phi - \epsilon_x}}$$

Where

$$\beta = \frac{2\sqrt{2m}}{\hbar}$$

and

$$d = x_2 - x_1$$

When the work function on the left electrode, ϕ_L, equals that on the right ϕ_R, j becomes:

$$j \approx \frac{e}{2\pi h d^2} \left[(\phi - \mu_L) e^{-\frac{4\pi d\sqrt{2m(\phi-\mu_L)}}{h}} - (\phi - \mu_R) e^{-\frac{4\pi d\sqrt{2m(\phi-\mu_R)}}{h}} \right]$$

This approximation can be good. [26, 18]

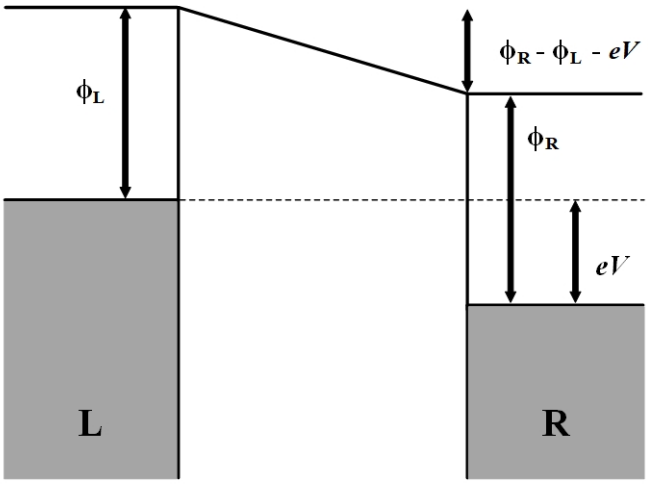


Figure 3.4. Asymmetric tunnel junction with different work functions on the left and right leads.

3.5 Graphene Nanoribbons

Graphene nanoribbons (GNRs) are narrow, rectangular structures derived from graphene sheets, with widths ranging from a few nanometers to tens of nanometers. While their lengths can extend indefinitely, their high aspect ratio classifies them as quasi-one dimensional nanomaterials. GNRs are a relatively addition to the family of nanomaterials and can exhibit either metallic or semiconducting properties.[21] The electronic structure of graphene is sensitive to structural modifications like atomic vacancies, which disrupt lattice symmetry and altering conductivity. In finite-sized graphene, edges act as one-dimensional defects, significantly affecting electronic properties of graphene. Graphene edges are classified as zigzag edge or armchair edge, with arbitrary edge shapes comprising combinations of both.[24]

Its predicted that when graphene adopts a ribbon structure with infinitely extended edges, introducing zigzag edges into the honeycomb lattice leads to the emergence of nonbonding π electronic states, referred to as "edge states," at the Dirac point. These edge states appear alongside the π valence and π^* conduction bands inherited from the ideal graphene structure. The edge states are predominantly localized at the graphene edges and significantly influence the electronic properties of these regions. In contrast, the presence of armchair edges has a negligible effect on the electronic structure near the Dirac point. [27]

The local breaking of symmetry between A and B sites (as shown in figure 3.6) at zigzag edges plays a crucial role in graphene's electronic structure. As described by the

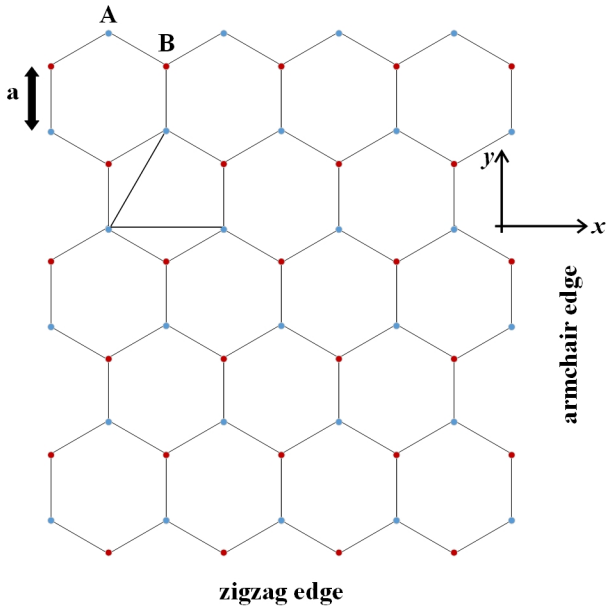


Figure 3.5. Nanoribbon geometry with both zigzag and armchair edges.

Hamiltonian equation, the electronic properties of graphene are governed by the interactions between wave functions of adjacent carbon atoms on A and B sites. The topology of the carbon atom network dictates the solutions to the Schrödinger equation.

When the symmetry between A and B sites is preserved, the electronic structure remains similar to that of ideal graphene, even in the presence of defects. However, breaking this symmetry due to defects significantly changes the electronic structure. This sublattice symmetry breaking is a fundamental reason for the emergence of edge states at zigzag edges.

Conversely, armchair edges maintain the symmetry between A and B sites. For ideal bulk graphene, with its infinite honeycomb lattice, the A and B sites are inherently symmetrical. Consequently, graphene with armchair edges exhibits an electronic structure like to that of ideal graphene, and defects that do not disrupt sublattice symmetry have minimal impact on its electronic properties. [24]

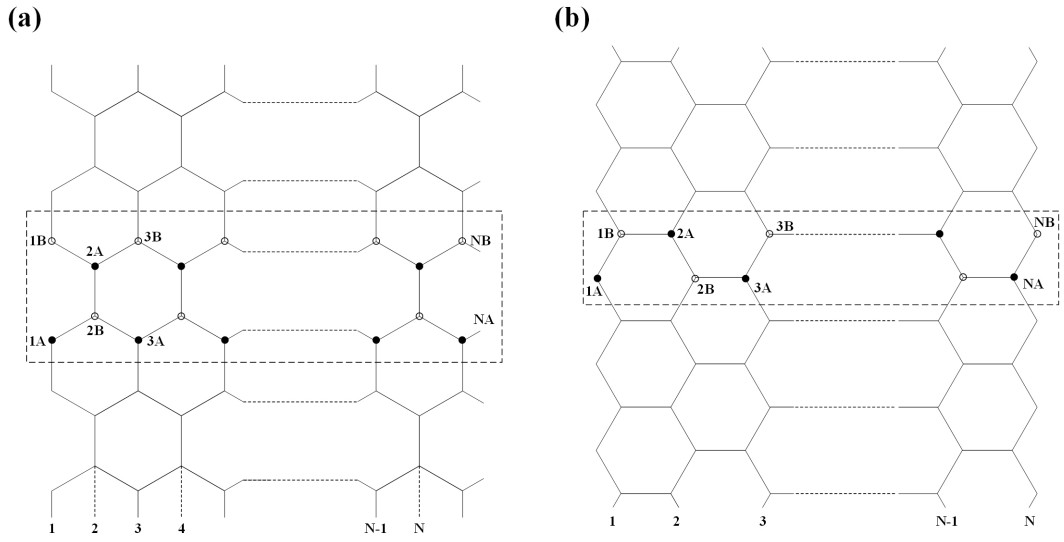


Figure 3.6. Graphene with armchair edge (a) and zigzag edge (b), where the carbon atoms belonging to sublattices are classified by labeling with A or B.

Part II

part Two

Chapter 4

Simulation by QuantumATK

In this section, we analyze the behavior of graphene as an electrode. Initially, the properties of simple graphene without a nanogap are examined, followed by an analysis of graphene with different nanogap geometries. This involves assessing the density of states (DOS), transmission spectrum, and I-V characteristics for each configuration. By comparing these results, we aim to understand how different nanogap designs impact graphene's effectiveness as an electrode in single-molecule transistors.

4.1 Computational methods

The software used for all simulations in this chapter is QuantumWise Atomistic ToolKit (ATK) by Synopsys, a platform that integrates various tools for atomic-scale modeling. It includes multiple simulation engines, such as those based on tight-binding Hamiltonians and density functional theory (DFT). For the simulations involving the density of states (DOS), transmission spectrum, and I-V characteristics of graphene electrodes with and without nanogaps, the parameters listed in Table below were applied to ensure consistency across analyses.

Table 1 presents the parameters used in the equilibrium simulations of graphene with and without nanogap for the LCAO calculator in QuantumATK. The Van der Waals correction and counterpoise correction are disabled in this simulation.

LCAO CALCULATOR	
LCAO Basis Set	Exchange correlation: GGA Functional: PBE Pseudopotential: PseudoDojo Basis set: Medium
Numerical Accuracy	Density mesh cut-off: Default setting Occupation method: Fermi-Dirac Broadening: 1000 K k-points: [9.0, 9.0, 201.0] Å
Iteration Control	Default settings
Algorithm	Default settings
Contour Integral Parameter	Default settings
Poisson Solver	Solver Type: Conjugate gradient Boundary conditions: A direction: Dirichlet B direction: Periodic boundary condition C direction: Dirichlet
Electrode Parameters	Default settings

Table 4.1. QuantumATK DFT Calculator

The graphene layer was assumed to extend infinitely in the transverse direction, using periodic boundary conditions for the B direction in the Poisson Solver. The other boundary conditions are set to Dirichlet in the Poisson Solver to account for graphene edge passivation. Tables 2 and 3 list those applied in the transmission spectrum and device density of states calculations.

Transmission Spectrum Analysis	
Energy range	E_0 = -1.5 eV E_1 = +1.5 eV Points = 301
k-point sampling	Density: K_A = 27 K_B = 27
Infinitesimal	1e-06 eV
Self-energy calculator	Recursion
Energy zero parameter	Average Fermi level

Table 4.2. QuantumATK Transmission Spectrum settings

Device Density of States Analysis	
Energy range	E_0 = -1.5 eV E_1 = +1.5 eV Points = 301
k-point sampling	Density: K_A = 15 K_B = 15
Contributions	All
Infinitesimal	1e-06 eV
Self-energy calculator	Recursion
Energy zero parameter	Average Fermi level

Table 4.3. QuantumATK Device Density of States settings

Lastly, Table 3.4. contains the parameters used in the analysis of the I-V curves.

IV curve Analysis	
Voltage Bias	V_0 = 0 V V_1 = 2 V Points = 11
Energy range	E_0 = -1.5 eV E_1 = +1.5 eV Points = 301
k-point sampling	Density: K_A = 15 K_B = 15
Infinitesimal	1e-06 eV
Self-energy calculator	Recursion

Table 4.4. QuantumATK I-V curve settings

4.2 Configuration 1

The first configuration involves the analysis of the transmission spectrum and device density of states properties of a graphene layer without nanogap. The graphene sample used in this study consists of 133 hexagons, with 7 arranged in the transversal direction and 19 in the transport direction.

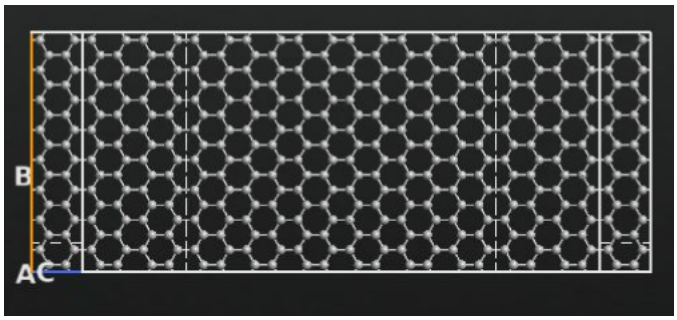


Figure 4.1. Graphene Device structure without nanogap.

The transmission spectrum analysis shows the contributions of the transmission of charge carriers across a range of energy values. The observed symmetrical pattern in the

transmission spectrum indicates an ideal graphene layer with minimal structural defects because this configuration is done for a large graphene sheet.

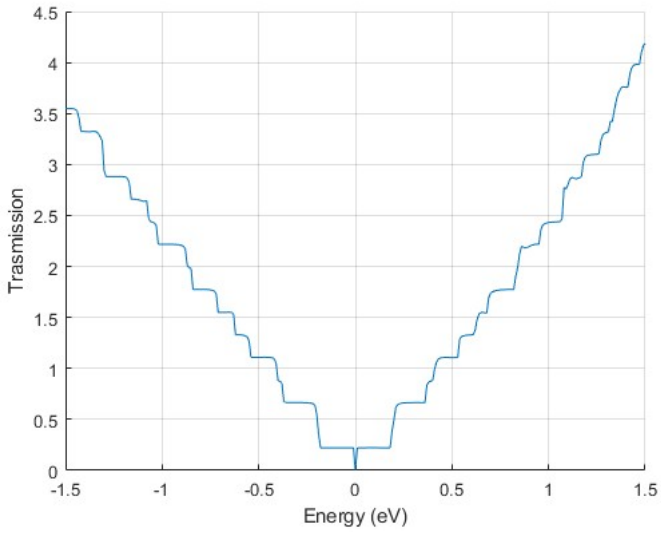


Figure 4.2. Transmission Spectrum of graphene without nanogap.

The device density of states (DOS) shows a nearly flat profile near the Fermi energy and there is a sharp peak observed around 1.4 eV.

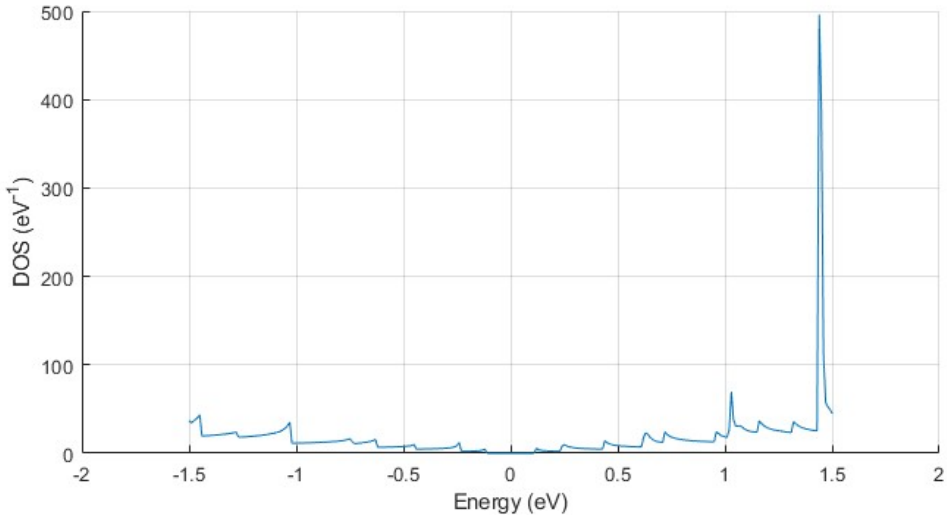


Figure 4.3. Device Density of states of graphene without nanogap.

4.3 Configuration 2

The second configuration analyzed features of a graphene nanogap in a bow-tie structure. In this structure, two central carbon atoms are retained while the atoms above and below these two are removed to form the bow-tie shape. Initially, the graphene device consisted of 75 carbon atoms, with 5 atoms along the transverse direction and 15 along the transport direction. After the removal of 9 atoms from the regions above and below the central atoms, the structure now contains a total of 66 carbon atoms.

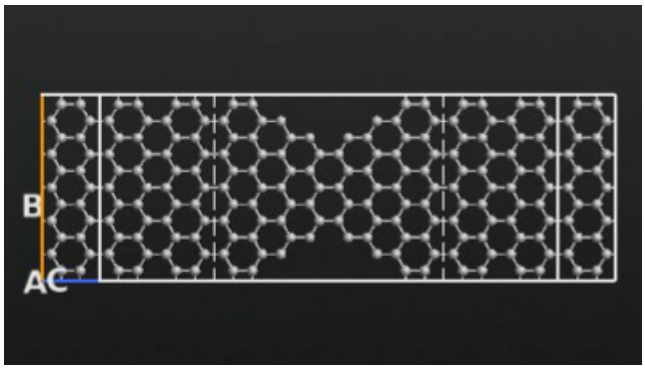


Figure 4.4. Bow-tie nanogap structure of graphene with 2 carbon atoms in the center.

To study the graphene as an electrode with a bow-tie nanogap structure, the transmission spectrum is first analyzed. The result shows that the transmission spectrum has a low value compared to the unshaped graphene layer within the same energy range. This corresponds to the band gap of the central semiconducting armchair edge ribbon. This behavior arises due to the asymmetric alignment of the electrode Fermi levels with the band edges.

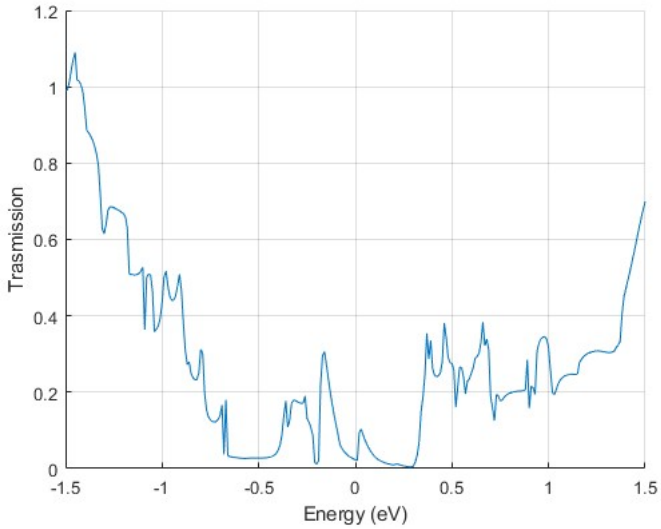


Figure 4.5. Transmission Spectrum of bow-tie nanogap graphene structure with 2 carbon atoms in the center.

The device density of states shows sharp peaks, particularly in the range of -1 to 1 eV. As observed in this structure and the corresponding transmission spectrum results, the symmetry of graphene is broken by the creation of a bow-tie shaped nanogap. This structural modification introduces localized electronic states at the edges of the nanogap, which are responsible for the observed peaks in the device density of states.

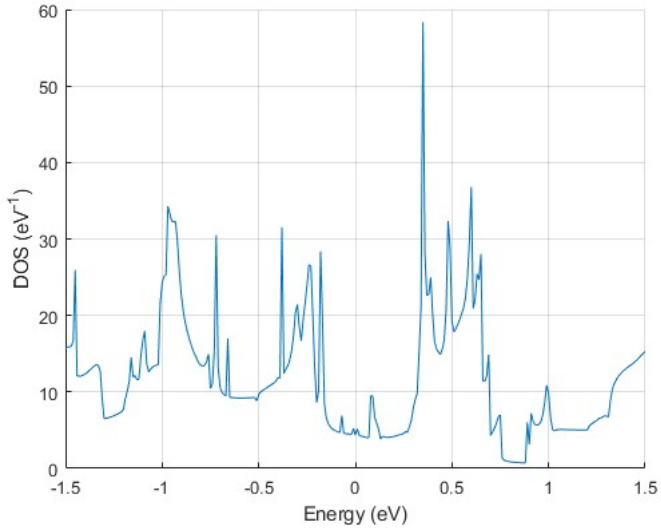


Figure 4.6. Density of states for bow-tie nanogap graphene structure with 2 carbon atoms in the center.

The I-V characteristics of the bow-tie nanogap graphene structure illustrate charge flow between the left and right electrodes, showing well match pattern with the I-V behavior (reported from [28]) of simple pure graphene.

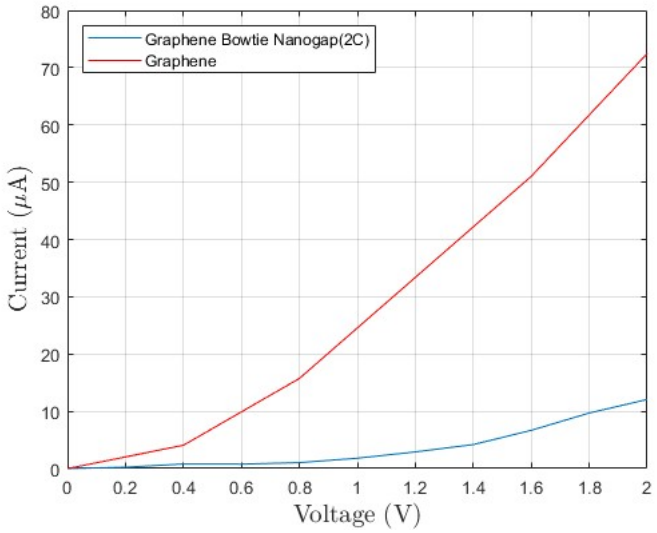


Figure 4.7. I-V curve for bow-tie nanogap graphene structure with 2 carbon atoms in the center.

4.4 Configuration 3

Another graphene electrode structure with a bow-tie shape, featuring a single carbon atom at the center, has been simulated. Initially, the graphene device consisted of 66 carbon atoms, arranged with 6 atoms along the transverse direction and 11 atoms along the transport direction. After removing 25 atoms from the regions above and below the central atom, the resulting structure contains a total of 41 carbon atoms.

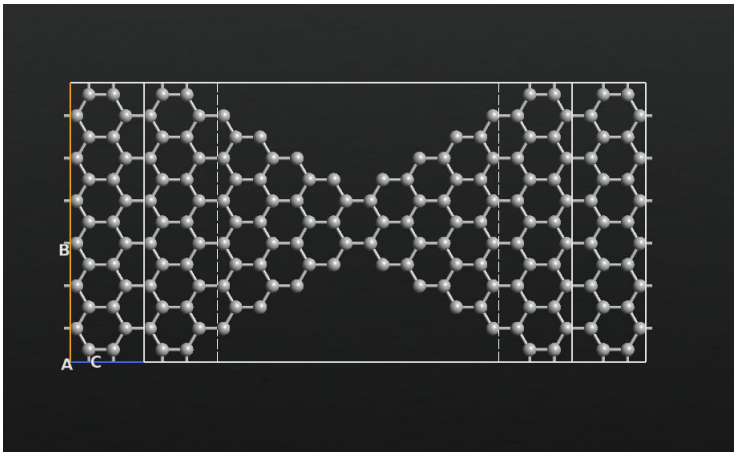


Figure 4.8. Bow-tie nanogap structure of graphene with 1 carbon atom in the center.

The transmission spectrum once again exhibits edge effects between -1 and 1 eV, corresponding to the energy range of the left and right Fermi levels, characterized by an asymmetric pattern. However, it exhibits slightly higher transmission values within the same energy range compared to the second configuration.

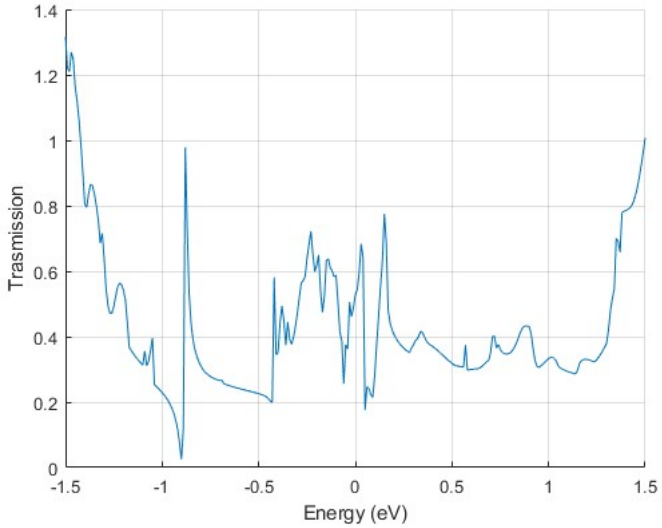


Figure 4.9. Transmission Spectrum of bow-tie nanogap graphene with 1 central carbon atom.

The density of states (DOS) for the structure with a single carbon atom in the center indicates that charge localization in the energy range of -0.5 to 0.5 eV is significantly more present compared to the second configuration. This can be attributed to the presence of only one carbon atom at the center of the graphene layer, which leads to reduced charge

delocalization. Consequently, the DOS becomes more concentrated in this case, reflecting the enhanced localization effects.

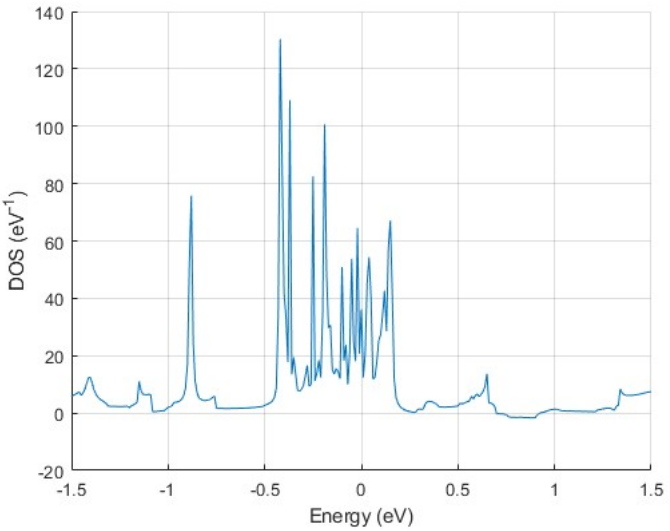


Figure 4.10. Density of states for bow-tie nanogap graphene with 1 central carbon atom.

The I-V characteristic for the graphene bow-tie shaped nanogap with a single central carbon atom clearly demonstrates the transfer of charge between the left and right electrodes.

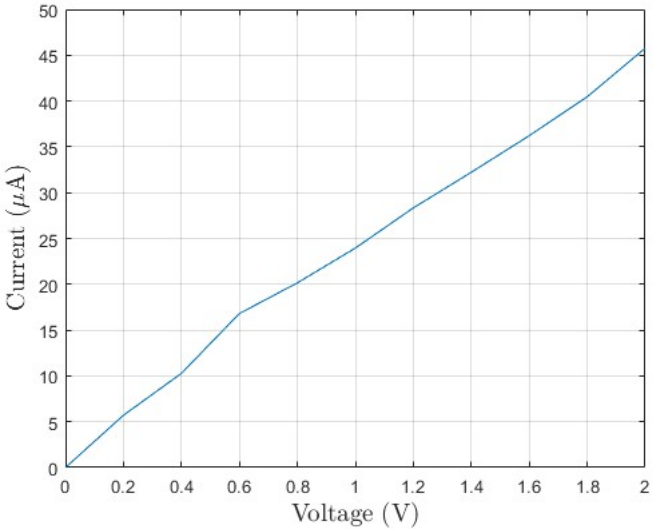


Figure 4.11. I-V curve for bow-tie nanogap graphene with 1 central carbon atom.

4.5 Charge transport comparison

The current voltage (I-V) characteristics for all three configurations are compared. By comparing the I-V curves of the graphene bow-tie shaped nanogap with one and two central carbon atoms, and the I-V characteristic of a simple graphene layer (as reported in the study conducted by another student[28], which is not included in this thesis), it is evident that both nanogap structures facilitate charge transport. However, the structure with a single central carbon atom exhibits a higher current flow compared to the two central carbon atoms bow tie nanogap. An interesting observation from the comparison between the single centered carbon atom bow-tie nanogap and simple graphene is that, between 0 and 1 volt, the nanogap structure shows higher current flow, indicating more conductive behavior. At 1 volt, the current for the nanogap structure with one central carbon atom and simple graphene structure without nanogap is 24 µA, but as the voltage increases from 1 to 2 volts, the simple graphene electrode passes more current.

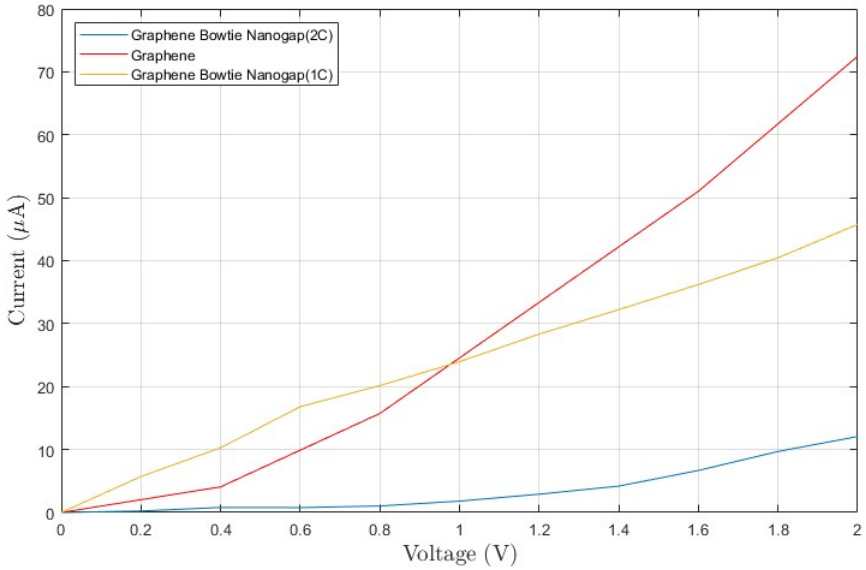


Figure 4.12. I-V curve comparison for graphene with and without nanogap structures.

4.6 Conclusion

In conclusion, the simulations show that pure graphene exhibits an ideal transmission spectrum with distinct step-like features. However, transitioning to bow-tie configurations disrupts these ideal properties. Notably, the transmission spectrum spikes observed when the graphene nanoribbon chain is opened. [29]

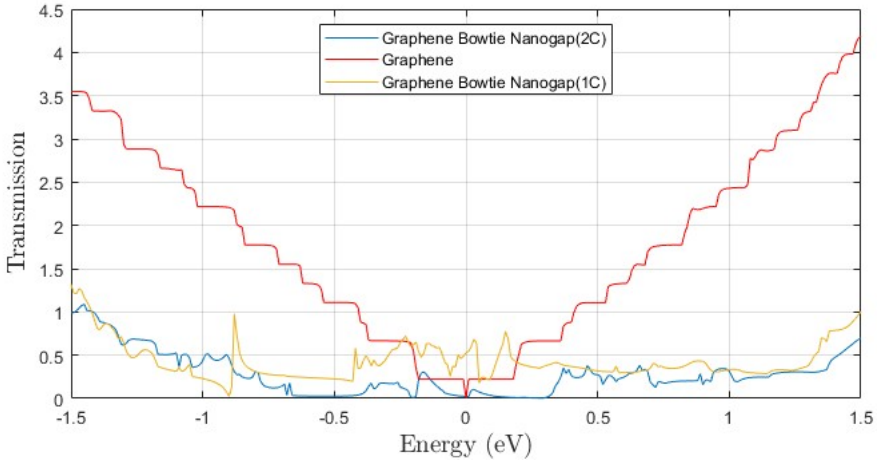


Figure 4.13. Transmission Spectrum comparison for graphene with and without nanogap structures.

Transitioning to bow-tie configurations modifies the ideal density of states of pure graphene without a nanogap, introducing non-ideal spikes. These spikes, represented as narrow peaks with minimal broadening, signify localized states. The appearance of these localized states in the density of states is attributed to the disruption of the graphene lattice's periodicity caused by the bow-tie configuration.

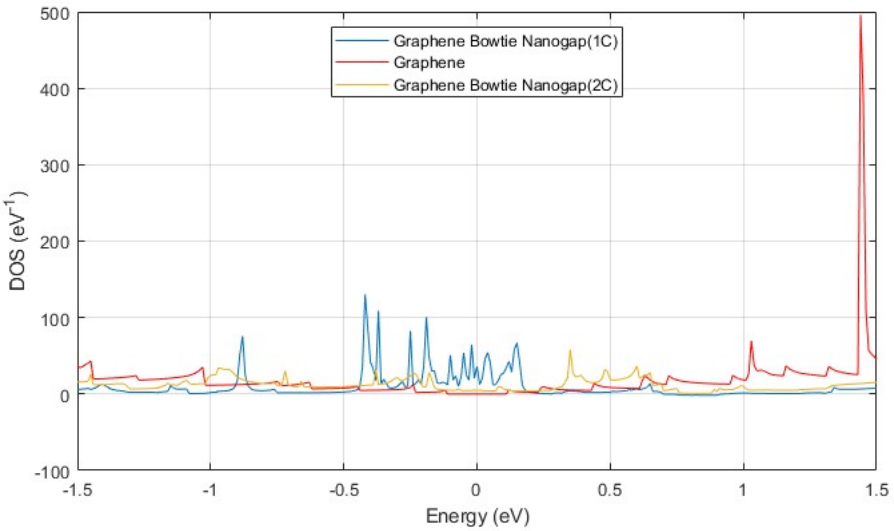


Figure 4.14. Density of states comparison for graphene with and without nanogap structures.

Chapter 5

Development of a feedback-controlled electroburning platform

As mentioned in the first chapter, the feedback-controlled electroburning process is used in this thesis for the nanogap formation in graphene material.

5.1 Hardware

In this thesis work, the feedback-controlled algorithm system has been developed by using a controller and two modules from National Instruments (NI) that are used in our work which are listed below :

1) NI cRIO-9030; FPGA core controller, host up to 4 extra modules, that two of them use in this work.

Figure 5.1. NI cRIO-9030.

2) The NI 9265 is an analog output module (current generator) with four output channels, capable of generating a maximum output current of 20 mA per channel.

Figure 5.2. NI 9265.

3) The NI 9223 is an analog input module (voltage reader) with four input channels, operating within a ±10 V range.

Figure 5.3. NI 9223.

5.2 Software

The software used in this thesis to implement the feedback-controlled algorithm was LabVIEW by National Instruments. The connection between the controller and analog input and output modules was managed through the LabVIEW-FPGA program. To transfer data between the FPGA controller (cRIO-9030), the modules (NI-9265 and NI-9223), and the host computer, an interface was established between the LabVIEW-FPGA target and the LabVIEW target. One key aspect of the feedback loop system, particularly in this test, is the sampling rate. LabVIEW-FPGA target provides the advantage of enabling a high-speed feedback control system, making it ideal for this application.

5.3 Electroburning algorithm

As mentioned in studies from other scientific groups, the system is based on a feedback-controlled loop. In this work, a potentiometer was used to simulate the behavior of the graphene electrode. Initially, since the analog output device functions as a current generator, the current is applied incrementally from 0 to 20 mA with a defined ramp speed for each step, while the voltage is measured simultaneously using an analog input voltage module. To verify that the feedback condition is applied correctly, the resistance is increased from 0 Ω to 1000Ω, and the conductance is measured in parallel. The reference parameter considered for the feedback condition is the conductance. Whenever a drop in conductance greater than 5% is detected, the current generator reduces the applied current by 20%. This loop continues until the resistance exceeds 500 $M\Omega$, at which point the system stops.

Figure 5.4. and the following flowchart illustrate the algorithm. Initially, the current is set to zero, and the ramp rate for applying current is 2 mA/s. Upon reaching 10% of the first ramp, the first reference conductance value is accepted as the baseline for subsequent steps (no feedback is applied yet), as indicated by the left red dots (First Reference) in Figure 5.4. Thereafter, if the conductance decreases by more than 5%, a new reference conductance is accepted, and the current is immediately reduced by 20%, as shown by the right red dots (Second Reference) in Figure 5.4. This process continues until the resistance exceeds 500 MΩ.

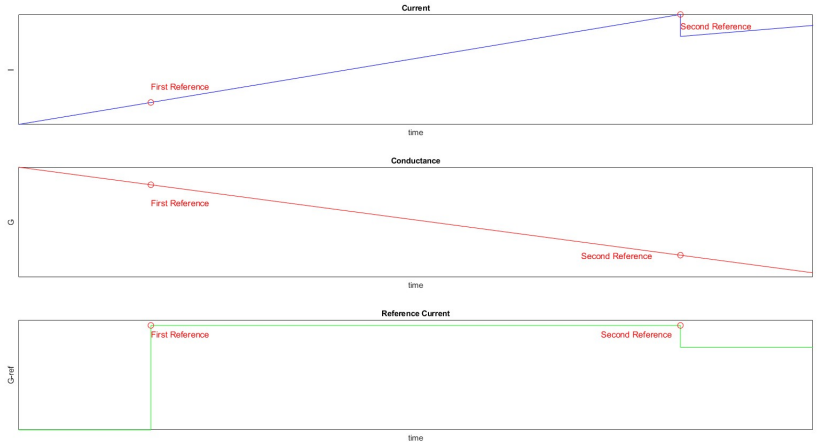
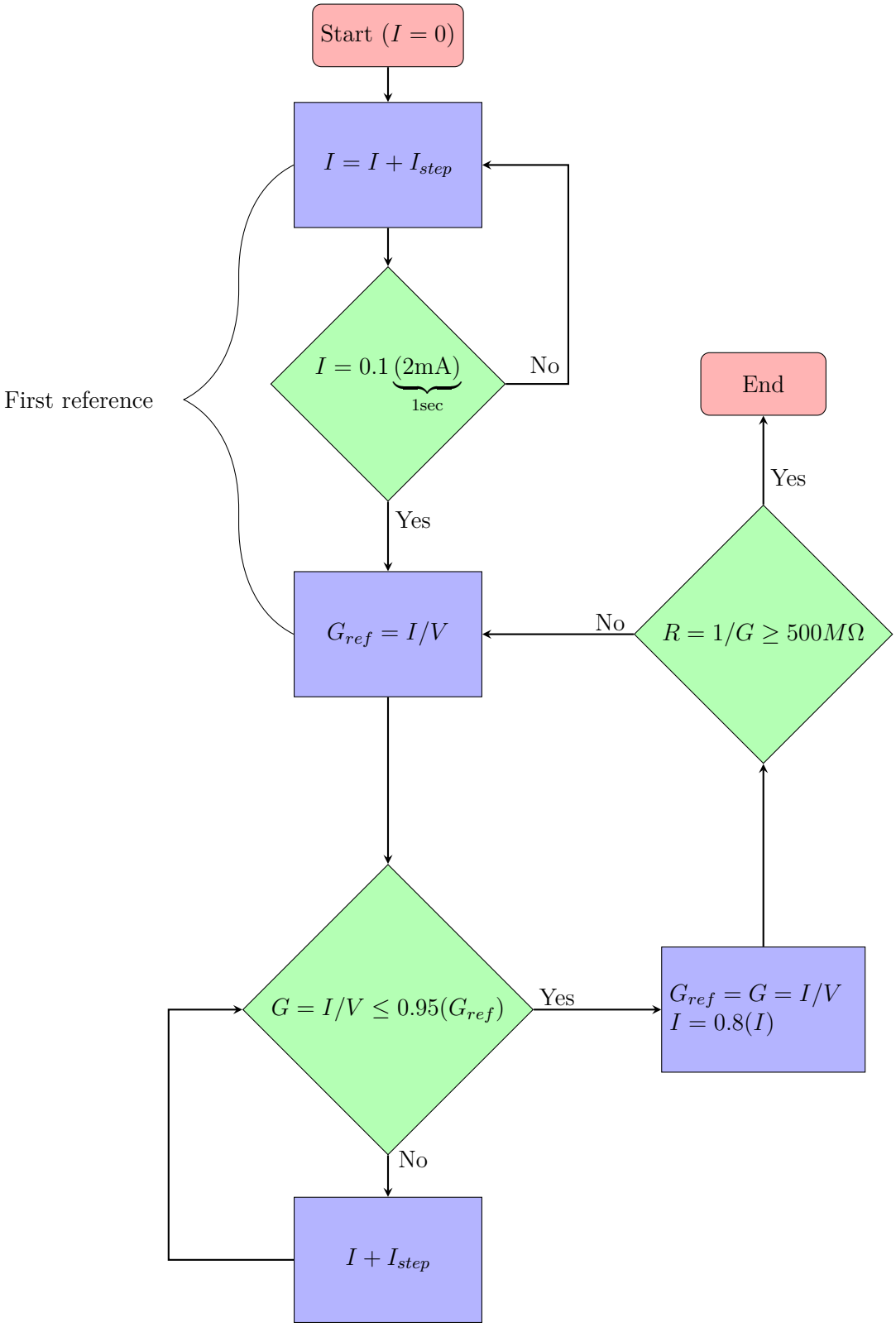


Figure 5.4. Comparison of Current, Conductance, and Reference Conductance in the Algorithm.


Start ($I = 0$)
$I = I + I_{step}$
$I = 0.1\,(\underbrace{2\text{mA}}_{1\text{sec}})$
No
Yes
First reference
$G_{ref} = I/V$
No
$R = 1/G \geq 500M\Omega$
Yes
End
$G = I/V \leq 0.95(G_{ref})$
Yes
$G_{ref} = G = I/V$
$I = 0.8(I)$
No
$I + I_{step}$

5.4 Block diagram

The following sections provide details about the algorithm and the implementation of the block diagram in LabVIEW-FPGA.

5.4.1 Current generation

As mentioned earlier, the current is applied to the system using the NI 9265 module. In the LabVIEW-FPGA target, this is achieved by utilizing an FPGA analog output node. The process of assigning the current value to this node is described in the following.

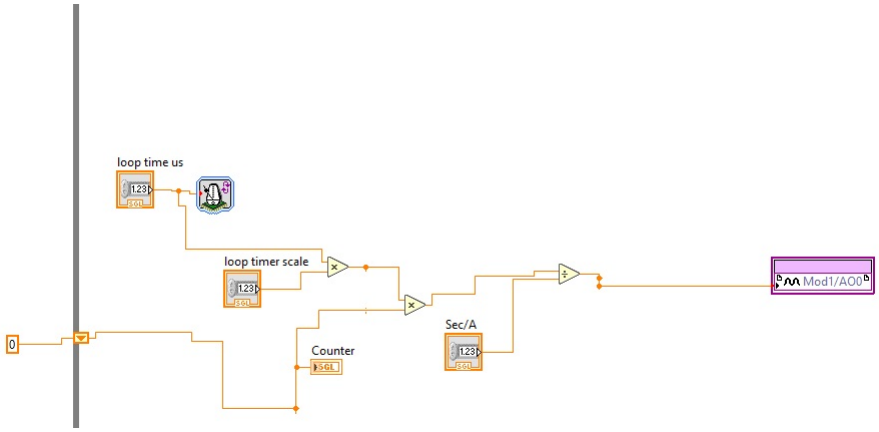


Figure 5.5. LabVIEW-FPGA block diagram for loop timing and current generation.

The FPGA loop timer is used in the system to control the duration of each loop iteration. In LabVIEW-FPGA, the loop timer can be configured in milliseconds (ms), microseconds (µs), or ticks, with microseconds (µs) chosen in this case. Since the goal is to increase the current incrementally over a defined time for each step, this can be controlled by the control block (loop time µs). For example, if the control value is set to 200, it means that each loop iteration occurs every 200 µs. This value is then multiplied by the loop timer scale block (set to 1e-6) to convert it into the 200 µ, preparing it for the following calculation that creates the current input.

The value is then multiplied by the output of a shift register, which generates an integer number and acts as a counter. This counter starts at zero and increments by 1 per each loop iteration. The resulting value is then divided by another control parameter, Sec/A, to regulate the speed of the entire ramp. This controls the rate at which the current increases per second. For example, if we want to observe the current increase over a period of 10 seconds, we need to divide 10 by 0.02 (the maximum current that can be accepted by the NI 9265, which is 20 mA). This results in a Sec/A value of 500. By dividing 200 µ over 500 the result will be 0.4 µ which means that the current generator produces 0.4 µA in each loop iteration.

It is possible to plot the analog output current in the waveform chart to see the behavior

of applied current, to visualize the chart its need to see it in the LabVIEW-FPGA VI (Virtual Instrument).

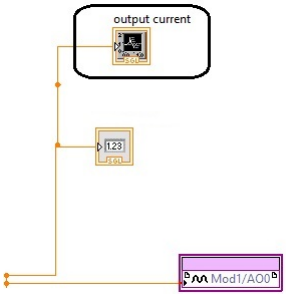


Figure 5.6. LabVIEW-FPGA block diagram for output current.

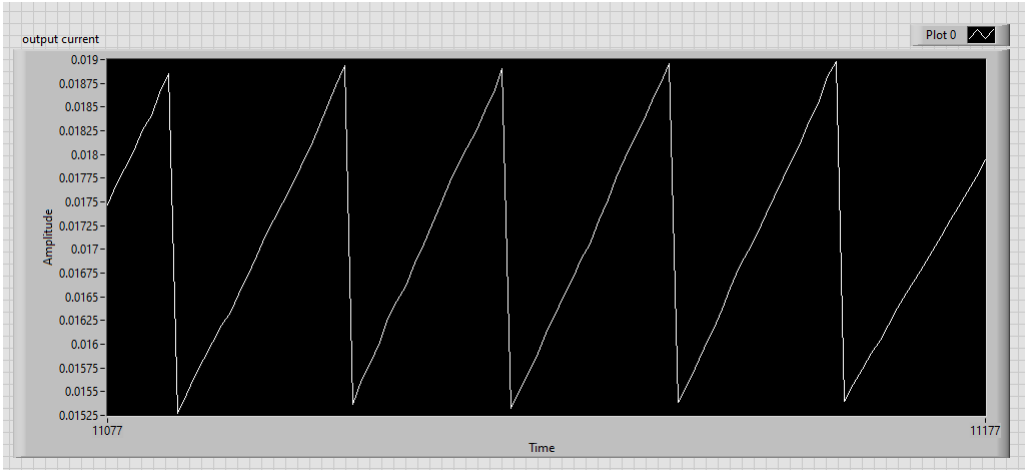


Figure 5.7. LabVIEW-FPGA VI for output current.

5.4.2 Voltage reading

As mentioned earlier, we need to measure the voltage using an analog input module (NI 9223). The following block diagram provides the details for voltage reading.

The FPGA analog input node is connected to two indicators. One displays the measured voltage on a waveform chart, and the other shows the voltage as a single precision (6-digit) number. It should be noted that a converter is connected before the indicators to convert a fixed-point number to a single precision floating-point number. Additionally, this diagram is within the same while loop as the FPGA analog output node, meaning it reads the voltage value every 200 µs, as previously defined in the loop time.

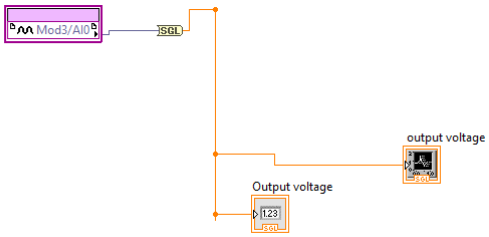


Figure 5.8. LabVIEW-FPGA block diagram for input voltage.

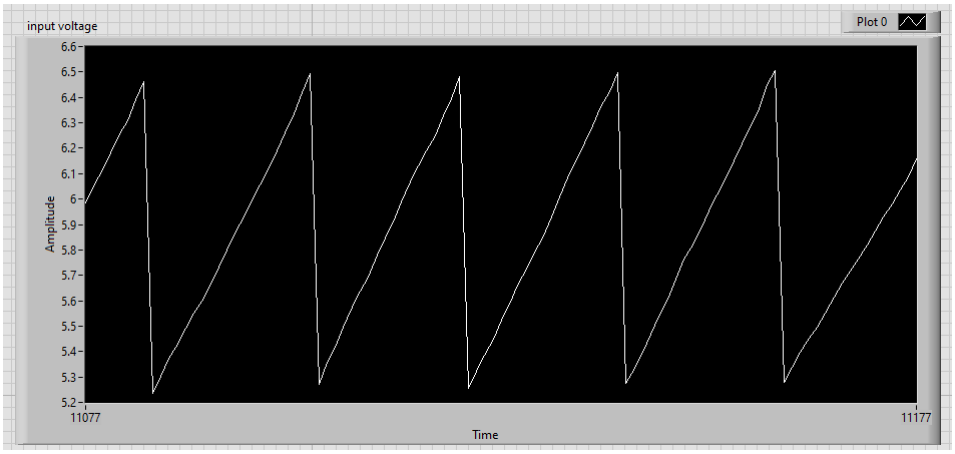


Figure 5.9. LabVIEW-FPGA VI for input voltage.

5.4.3 Conductance and Resistance

To measure the conductance in our LabVIEW-FPGA target, we divide the previously generated current value by the measured voltage. Since we do not have a current sensor and are generating the current directly in the FPGA, we use a shift register to store the previous current value. This is necessary to address the delay in updating the current input value. By using the shift register, we retain the last current value and divide it by the measured voltage to calculate the conductance. To calculate the resistance, we simply take the reciprocal of the conductance value.

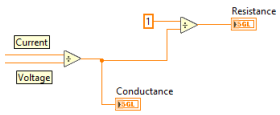


Figure 5.10. LabVIEW-FPGA block diagram for measuring Conductance and Resistance.

5.4.4 Feedback conditions

In the following, we will provide more details on the block diagram related to the conditions for applying the feedback. As specified by the algorithm, whenever the feedback condition is met, the current must be reduced to a lower value. To implement this, two feedback prerequisites are necessary:

First, we need to consider that the maximum possible value to be applied to the FPGA analog output node is 20 mA. Therefore, a comparison block is used to compare the current limit control with the generated current output to ensure the value does not exceed 20 mA. This condition is then sent as an input to an OR logic block.

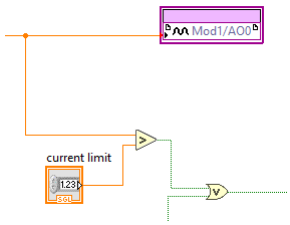


Figure 5.11. LabVIEW-FPGA block diagram for Current limit.

The other input to the OR logic block is related to the conductance. According to the algorithm, a drop in conductance must be monitored as a feedback requirement. From the literature, we know that an initial reference point for the current is needed to measure the conductance. This reference value is set to 10% of the current ramp. As previously mentioned, we generate a current ramp that increases by 0.4 µA every 200 µs. Since the process is running over 10 seconds, increasing the current from 0 to 20 mA, this corresponds to a 2 mA increment per second. The product of the loop timer scale and the loop time µs input is then divided by the reference value control (1st reference(%)), which is set to 0.1 (representing 10%). The result of this division is converted to an integer and compared with the counter value from the shift register. If these two numbers are equal, the true logic signal is sent to the OR gate of the top case structure.

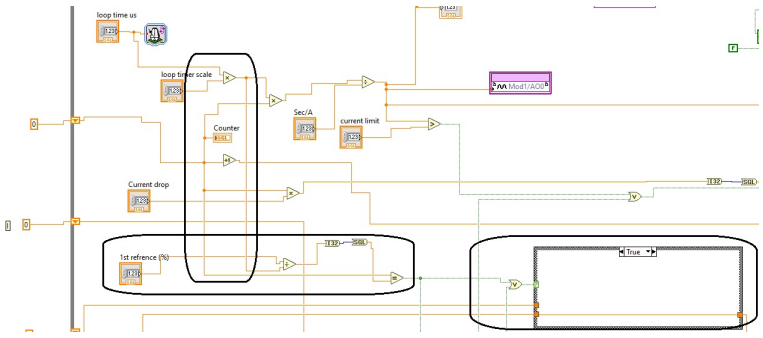


Figure 5.12. LabVIEW-FPGA block diagram for 1st reference feedback condition.

When the condition for the first reference is met, and the output is set to the ON state, we ensure that it stays ON, as we only need the first reference to be triggered once. The result of the equality comparison between the 1st reference and the counter is then passed to the bottom case structure for subsequent iterations. Inside the bottom case structure, when the constant is true, the output of the case structure is also ON, keeping the first trigger in the ON state. Conversely, when the bottom case structure is in the false state, it indicates that the first reference condition has not yet been met, and the output of the equality comparison block remains OFF. Thus, once the first reference condition is met, the bottom case structure remains in the ON state until the end of the process.

The output signal of the bottom case structure is sent to a shift register, and the same signal from the input of the shift register is forwarded to the AND logic for the top case structure. This setup ensures that when the top case structure is in the true condition, it sets G_{ref} (which is defined for catching reference conductance) equal to $G(N-1)$ (which is the previously measured conductance value). In the false condition, G_{ref} remains unchanged.

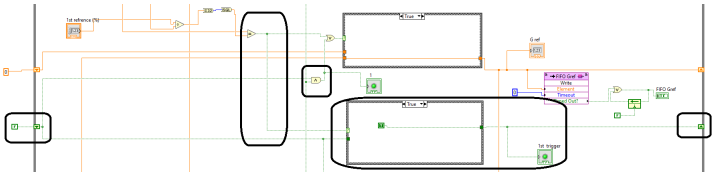


Figure 5.13. LabVIEW-FPGA block diagram for triggering reference.

This means that for the system to update G_{ref} and store the new reference conductance, the input condition for the top case structure must be in the ON state. This occurs only when the feedback prerequisite, a drop of 5% in conductance is met by the system. In this case, G_{ref} is updated to the last measured conductance value, $G(N-1)$. However, if the drop in conductance is less than 5%, the system does not accept the feedback condition, and G_{ref} remains unchanged. In order to define a reference value for conductance, we first send the latest measured conductance value to the shift register and then extract the previous value to send it to a case structure.

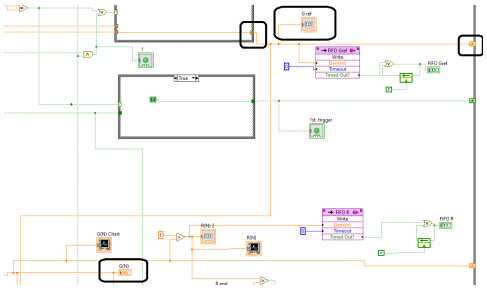


Figure 5.14. LabVIEW-FPGA block diagram for accepting reference conductance.

So we can understand that we used OR logic to separate the first reference condition from the condition of a 5% drop in conductance. Since we know that only the first time we need the first reference, and after this is passed, we only need to consider the condition of a drop in conductance (>5%).

After that, in order to set the conductance drop as the only condition for the feedback system, the AND logic is used. One terminal of the AND logic is connected to the ON signal (output logic of the first reference and the bottom case structure), and the other terminal is connected to the input from the conductance drop (>5%) to ensure that the first reference has been achieved correctly.

Therefore, we can say that overall, the bottom case structure is only used to accept and retain the first reference and first trigger, while the top case structure is used to keep G_{ref} constant until the conductance drop condition is met, at which point G_{ref} is updated to a new value.

As shown below, the measured conductance value is compared with 95% of the previous step's conductance value. If the conductance drops by 5%, the feedback condition is met and sent to the AND logical gate.

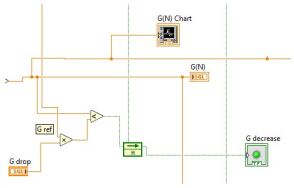


Figure 5.15. LabVIEW-FPGA block diagram for comparison of conductance.

After meeting the feedback requirements, the select logical block accepts the **true** logic, which is defined as 80% (0.8) of the counter number that generated the last step's current. This value is sent to the output of the first shift register, and the previous value is extracted from the input of the first shift register, converted to a single floating-point number, and then to an integer to be acceptable for the shift register.

Otherwise, if the feedback requirements are not met, the **false** logic is selected, and the counter of the shift register increments the integer value every 200 µs. The current increment will continue until the feedback requirements are met.

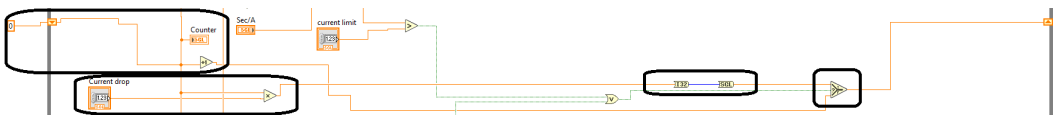


Figure 5.16. LabVIEW-FPGA block diagram for feedback selecting condition.

5.4.5 Loop end condition

In order to stop the process, the considered possible value of resistance, indicates that the gap has formed. In the literature, this value is defined by different groups as being between 500 MΩ and 1 GΩ. Here, since we are simulating the process with a potentiometer, we set this value to 10000 Ω.

Thus, if the resistance value exceeds 10000 Ω, the loop end condition will be met, and the process will stop.

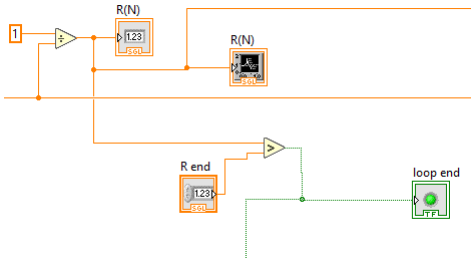


Figure 5.17. LabVIEW-FPGA block diagram to stop the loop.

5.5 Transfer data to the host

In the next step, in order to read the values on the host PC from the FPGA and observe the behavior patterns of Resistance, Conductance, Reference Conductance, Current and Voltage, we first need to write these values to the five FPGA FIFO nodes (First In, First Out) and then read them on the host computer.

5.5.1 Write to FIFO in LabVIEW-FPGA

To achieve this, we first define a buffer for the FIFO in LabVIEW-FPGA to provide enough space to store the required number of elements. It must be mentioned that the type of this FIFO is "target to host", as we are sending values from the FPGA to the host PC.

Next, we write the parameters of interest as inputs to the FIFO nodes, as illustrated below.

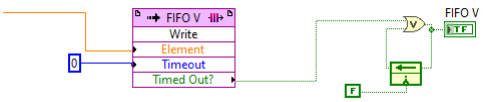


Figure 5.18. LabVIEW-FPGA block diagram to write data in FIFO.

5.5.2 Read the data from FIFO in LabVIEW

To retrieve data from the FIFO, an interface must be established between LabVIEW-FPGA and LabVIEW. The FPGA target is defined within the host program, and TDMS blocks are utilized in LabVIEW to store the data.

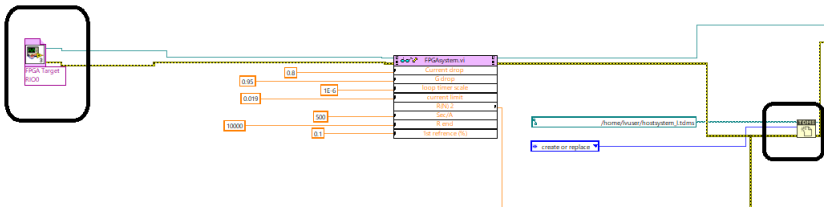


Figure 5.19. LabVIEW block diagram to open FPGA interface and TDMS.

The outputs from the FPGA interface are sent to the FIFO read blocks, and the data from the FIFO is stored using TDMS write blocks.

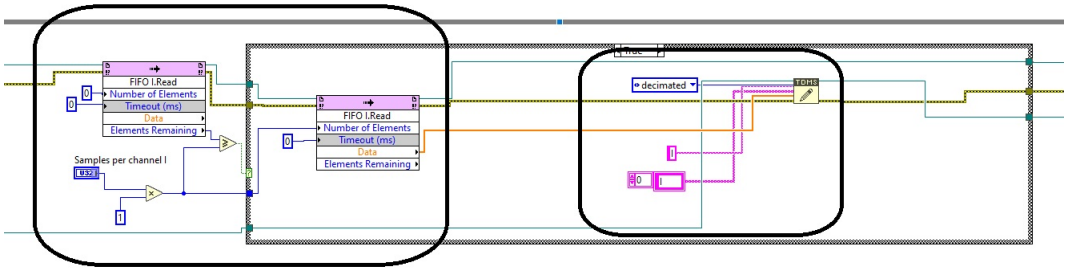


Figure 5.20. LabVIEW-FPGA block diagram to read data from FIFO and write to the TDMS.

5.6 Results of feedback-controlled system

In this part, we aim to compare the acquired data from five different parameters: Current, Voltage, Resistance, Conductance, and Reference Conductance, to analyze the behavior of the feedback-looped system.

Tests were conducted to verify that the algorithm functions properly under different sampling rates. Initially, the tests were performed with a sampling rate of 200 µs, followed by tests with sampling rates of 100 µs and 20 µs.

5.6.1 200 µs sampling rate

Firstly, we aim to set up the system to obtain results for the 200 µs sampling rate. These results are extracted from the FPGA memory, which is saved using the FIFO Read in the Host VI and written using the FIFO Write in the FPGA VI.

To read the data for the system with a 200 µs sampling rate, I defined the FIFO Write buffer size as 1023 for each of the five different FIFOs corresponding to V, I, R, G, and G_{ref}.

For reading the data using the FIFO Read block in the host VI, I set the number of samples per step to 200. Based on the runtime of the system, the FIFO stores the data in a TDMS file in the host VI. This allows us to extract the data for all five parameters V, I, R, G, and G_{ref} at intervals of 200 µs.

Since we are using a potentiometer in the process, it is not possible to achieve the gradual increase in resistance as observed in the natural behavior of graphene. Therefore, I conducted three simulations to approximate the behavior of resistance increase using the potentiometer.

First approach

In the first approach, I increased the resistance using the potentiometer in two successive steps.

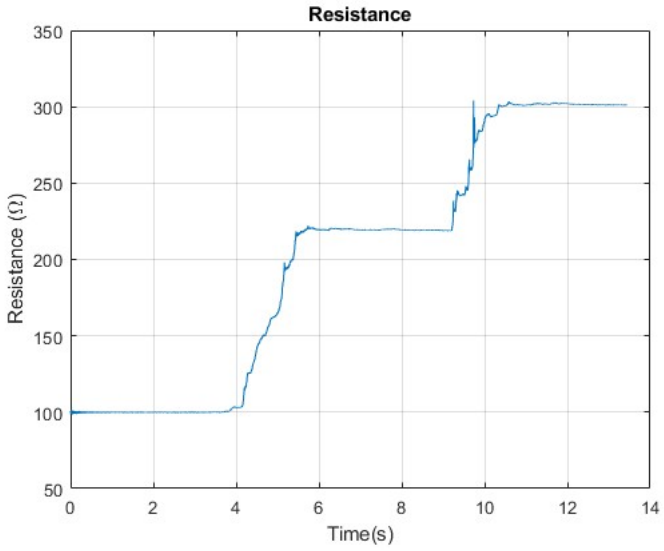


Figure 5.21. Resistance vs. Time at 200 µs sampling rate (First approach).

We can see from the resistance graph with respect to time that, at first, the resistance is equal to 100 Ω, and then it increases to 220 Ω and 300 Ω, respectively.

The conductance graph shows that, in the same time interval, there are two decreases in the conductance value.

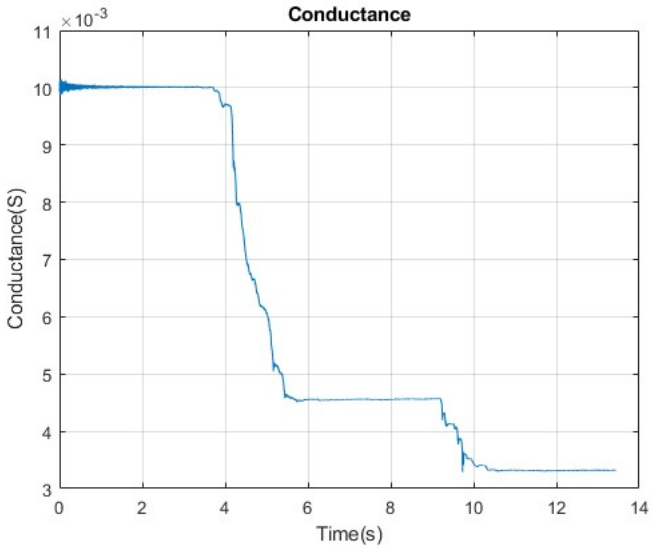


Figure 5.22. Conductance vs. Time at 200 µs sampling rate (First approach).

The plot for the current shows us that exactly at the time intervals when the resistance increases, this feedback condition is applied.

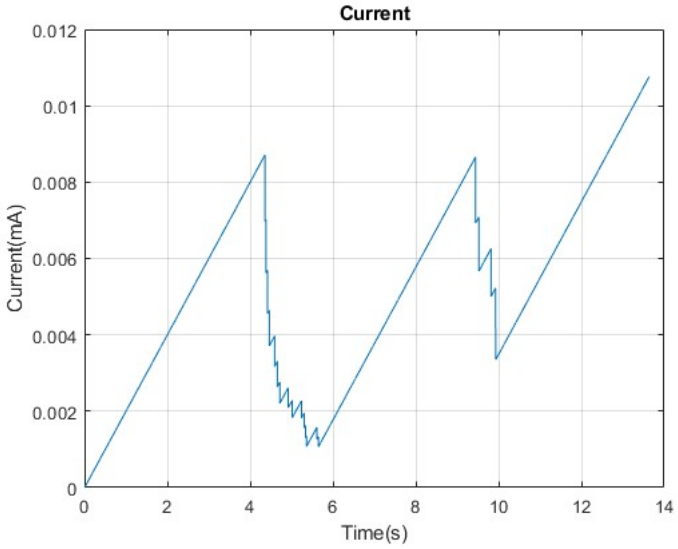


Figure 5.23. Current vs. Time at 200 µs sampling rate (First approach).

The voltage graph also shows the same behavior as the current with respect to time, and from both the current and voltage graphs, we observe two peaks occurring at the

same time intervals.

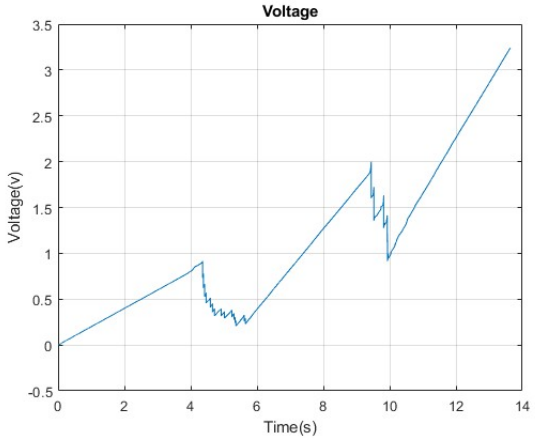


Figure 5.24. Voltage vs. Time at 200 µs sampling rate (First approach).

To provide better evidence that the feedback loop is properly adjusted, we know from the literature that the applied current must reduce by 20% when the conductance decreases by more than 5%, as defined by the reference conductance in our algorithm. Therefore, we plot the reference conductance and current on the same graph with respect to time. From the plot, we can observe that whenever the reference conductance is reduced, the applied current starts to increase.

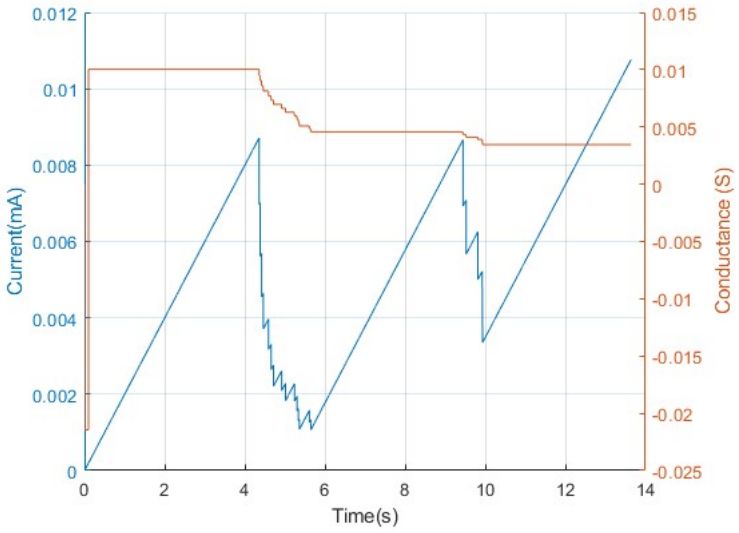


Figure 5.25. Comparison of current and reference conductance at 200 µs sampling rate (First approach).

If we examine the I-V curve of the device, we can observe two cycles of the applied feedback. In the final cycle, since there is no change in the resistance, the graph exhibits a linear behavior during the third cycle.

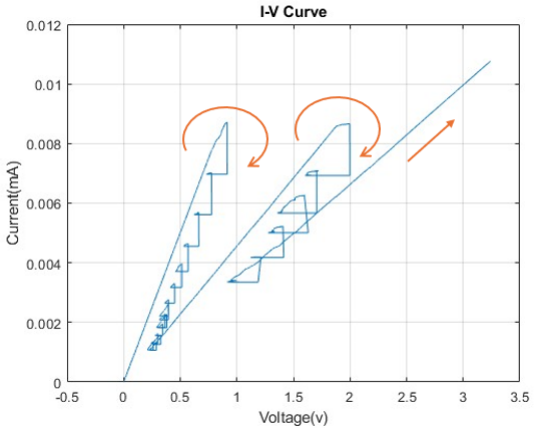


Figure 5.26. I-V plot for 200 µs sampling rate (First approach).

Second approach

In the second test for a 200 µs sampling rate, I attempted to increase the resistance four times.

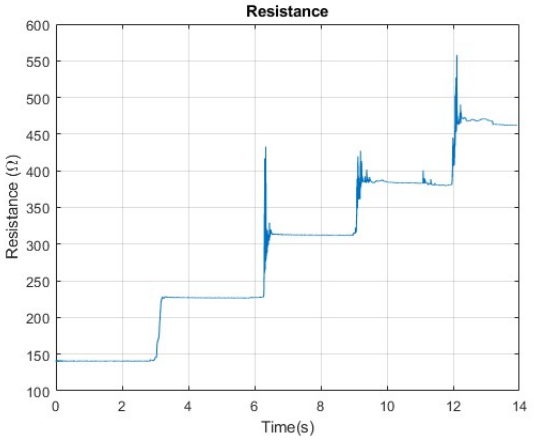


Figure 5.27. Resistance vs. Time at 200 µs sampling rate (Second approach).

We can see from the graph that the resistance increases in 4 steps from 140 Ω to 460 Ω. It needs to be mentioned that, since the voltage sensor module is highly sensitive, there are a few spikes in the resistance because we are performing the test with the potentiometer.

If we compare the conductance and reference conductance graphs, we observe that, due to the two spikes in the 2nd and 3rd steps of the resistance increase, there are corresponding downward spikes in the conductance reduction during the 2nd and 3rd steps. However, the reference conductance does not accept the 3rd conductance reduction step, as it had already recorded the value of the 2nd step spike, which was greater than the spike in the 3rd step.

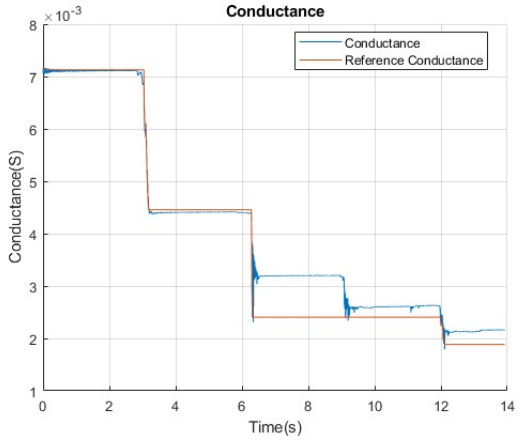


Figure 5.28. Comparison of conductance and reference conductance at 200 µs sampling rate (Second approach).

And consequently, the feedback only reacts to the reference conductance by bringing back the applied current to 20 % when the reference conductance accepts new values. If we analyze the current graph, we observe that it only responds to the changes in reference conductance and does not reduce during the 3rd step of conductance reduction.

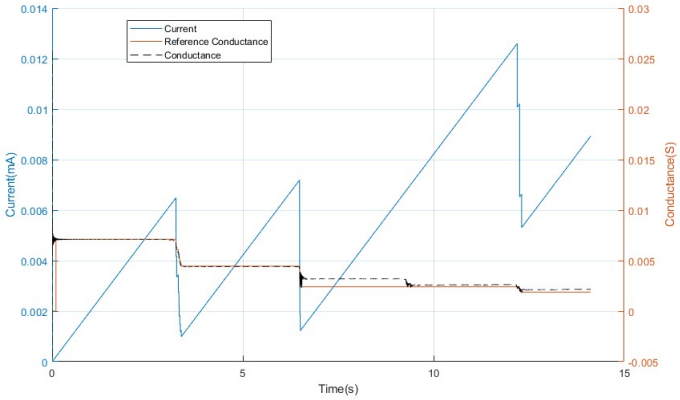


Figure 5.29. Comparison of current, conductance, and reference conductance at 200 µs sampling rate (Second approach).

While the voltage graph is consistent with the resistance values in the same time intervals.

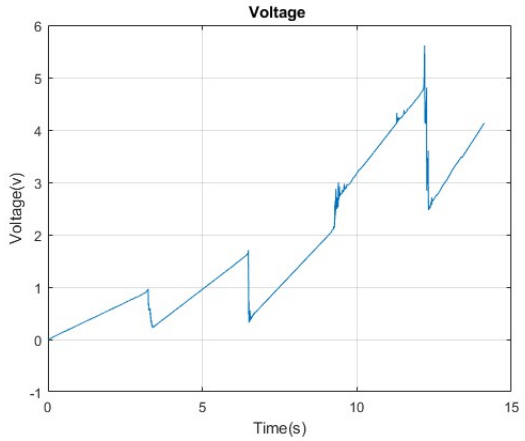


Figure 5.30. Voltage vs. Time at 200 µs sampling rate (Second approach).

From the I-V curves for the second approach, we can say that we have totally three cycles of feedback application, since the spikes between the second and fourth steps were generated and the system didn't accept the third step of increasing resistance by the potentiometer.

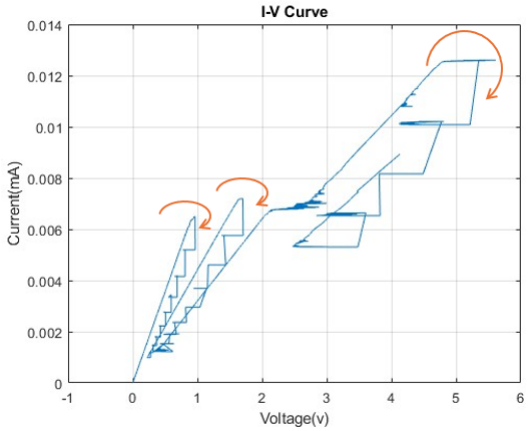


Figure 5.31. I-V plot for 200 µs sampling rate (Second approach).

Third approach

In the last approach for the 200 µs sampling rate, I increased the amount of resistance from 100 Ω to 700 Ω gradually using a potentiometer over 18 seconds. The resistance curve with respect to time shows a gradual increase.

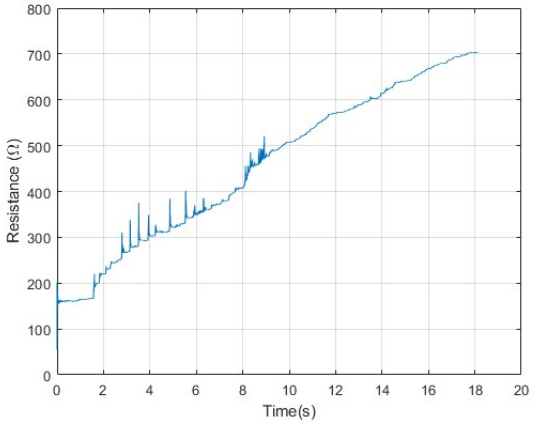


Figure 5.32. Resistance vs. Time at 200 µs sampling rate (Third approach).

We can see some small spikes in the resistance curve; these spikes are due to the high sensitivity of the voltage sensor module to the 1 kΩ potentiometer. The spikes are shorter compared to the previous test because the potentiometer rotation never stops during the entire process of this test.

By comparing the conductance and reference conductance, we observe the discretized behavior of the reference conductance, which decreases gradually as the conductance is reduced. This discretization occurs because the reference conductance only accepts variations greater than 5%.

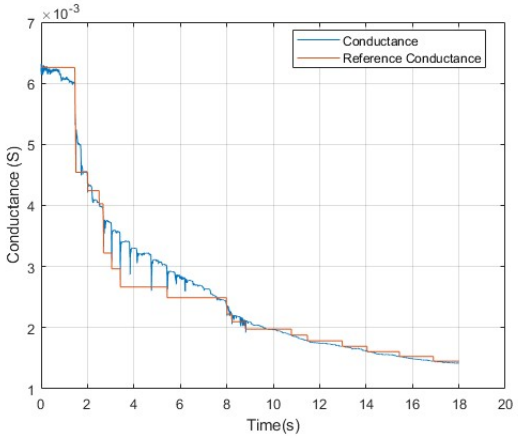


Figure 5.33. Comparison of conductance and reference conductance at 200 µs sampling rate (Third approach).

From the graphs for the current and voltage, we observe that they start to increase and decrease in multiple steps as the resistance increases. This behavior is due to the

feedback loop, which reduces the applied current by 20% each time.

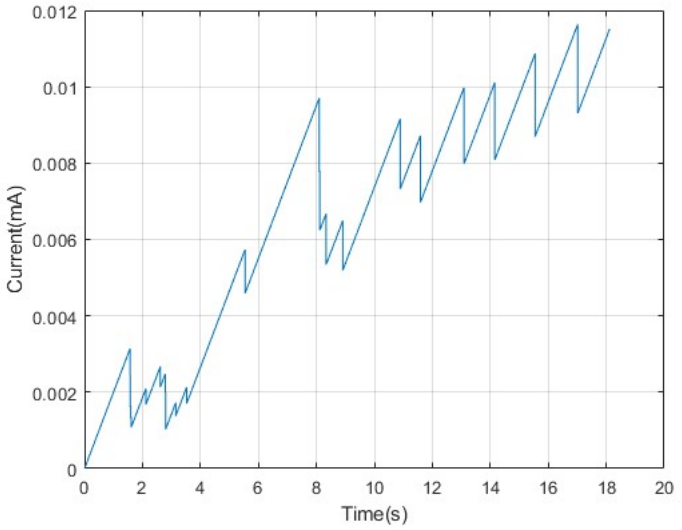


Figure 5.34. Current vs. Time at 200 µs sampling rate (Third approach).

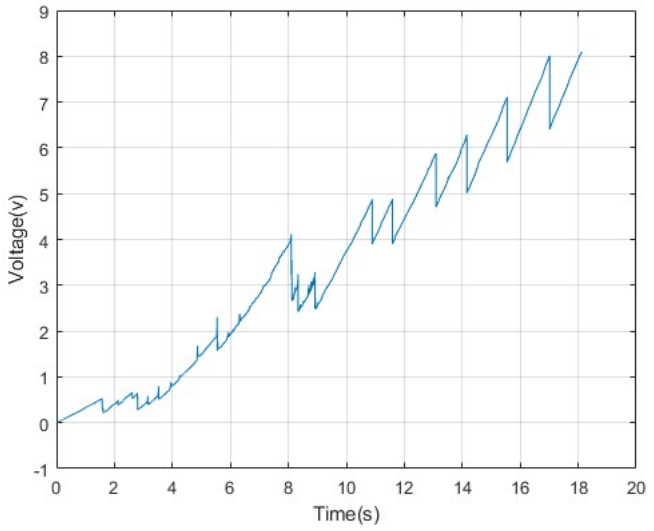


Figure 5.35. Voltage vs. Time at 200 µs sampling rate (Third approach).

At the end, the I-V curve is plotted for the entire process, and we can observe multiple cycles (triangles), which indicate that the feedback loop is adjusting repeatedly.

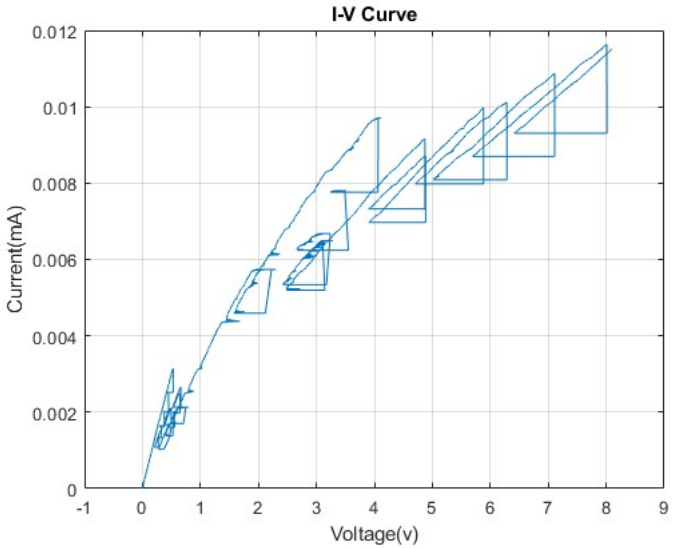


Figure 5.36. I-V plot for 200 µs sampling rate (Third approach).

5.6.2 100 µs sampling rate

For the 100 µs sampling rate, I increased the number of samples per channel in the FIFO read block in the host VI to 800, while the buffer size of the FIFO remained the same as before, equal to 1023 elements per each write in the FIFO write block in the FPGA VI. In this case, I performed two tests to analyze the behavior of the system.

First approach

Here, I tried to increase the resistance three times and extract the data. At the starting point, the resistance is equal to 102 Ω and then increased to 145 Ω, 170 Ω, and 193 Ω. From the figure 5.37. , we can see there are two spikes for the 2nd and 3rd steps of increments.

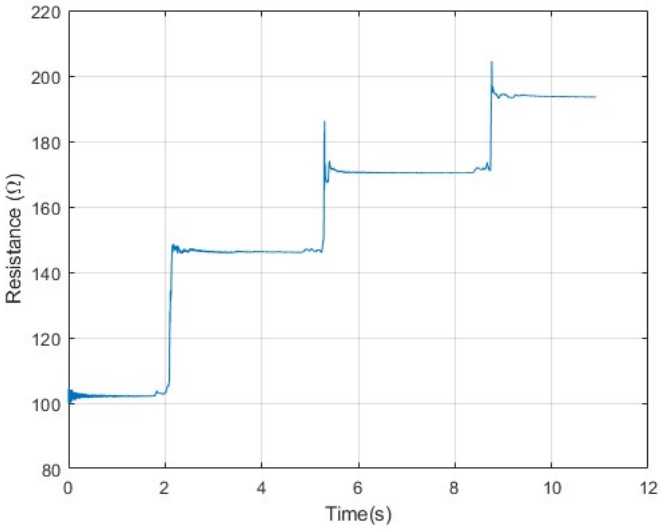


Figure 5.37. Resistance vs. Time at 100 µs sampling rate (First approach).

By comparing the conductance and reference conductance, we can see that they reduced three times as well. Although there are two spikes in the conductance reduction, since the 3rd step of conductance decrease is less than the value of the spike in the 2nd step, the reference conductance accepts this value and is also reduced in the 3rd step.

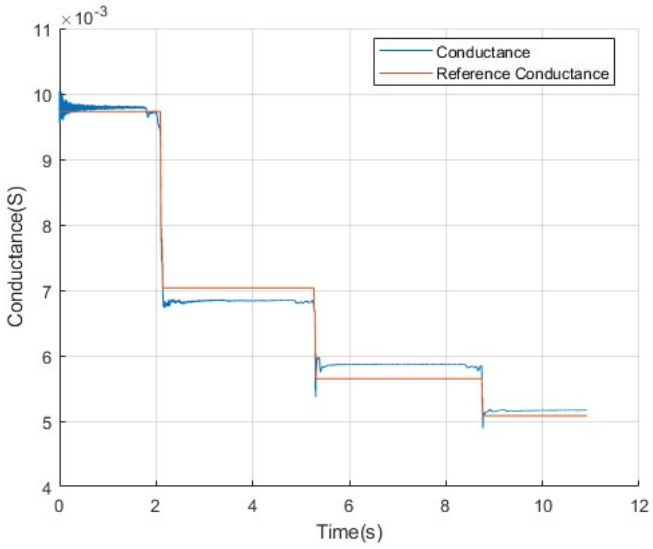


Figure 5.38. Comparison of conductance and reference conductance at 100 µs sampling rate (First approach).

We can see that in the same time intervals, the applied current is reduced and then starts to increase again. To show that the applied current returns to its 80 % value immediately, I highlight the three points in the 3rd step of resistance increase.

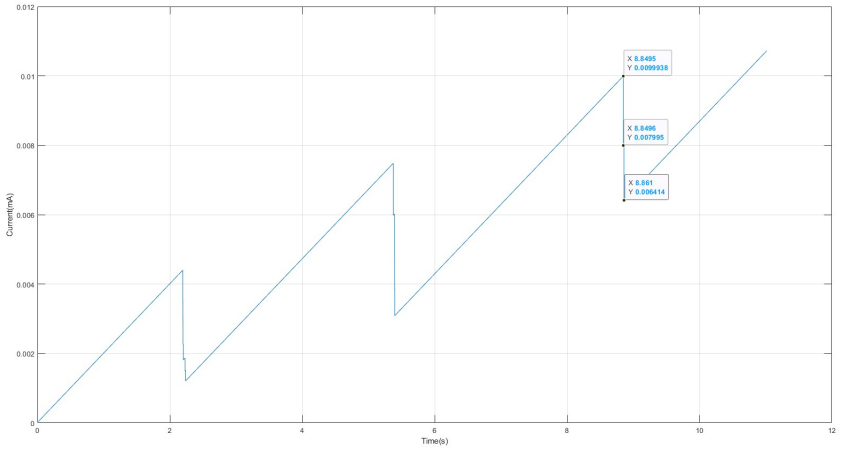


Figure 5.39. Current vs. Time at 100 µs sampling rate (First approach).

At the end, the I-V curve of this approach reveals that we have three cycles of adjusted feedback, and the I-V pattern starts increasing again linearly from the last step of resistance increase.

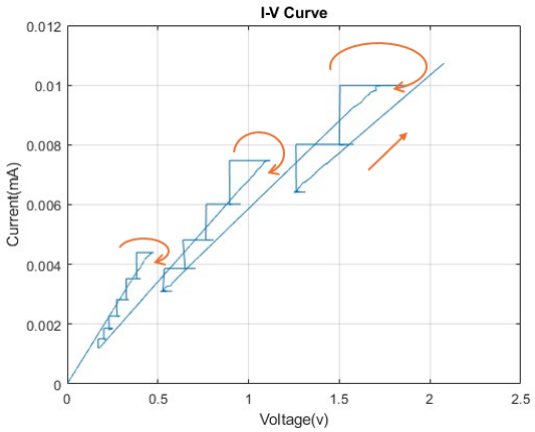


Figure 5.40. I-V plot for 100 µs sampling rate (First approach).

2nd approach

In this approach, I test the system with a one-time increase in resistance and analyze the behavior of the system.

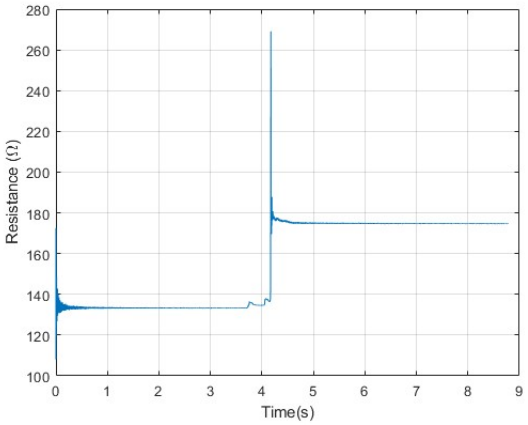


Figure 5.41. Resistance vs. Time at 100 µs sampling rate (Second approach).

As we can see, the behavior for resistance, conductance, and reference conductance is the same as in the previous tests.

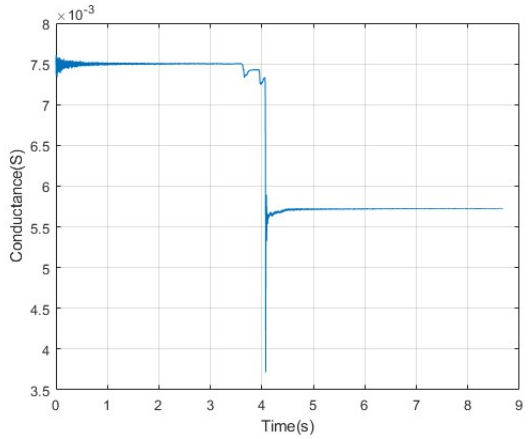


Figure 5.42. Conductance vs. Time at 100 µs sampling rate (Second approach).

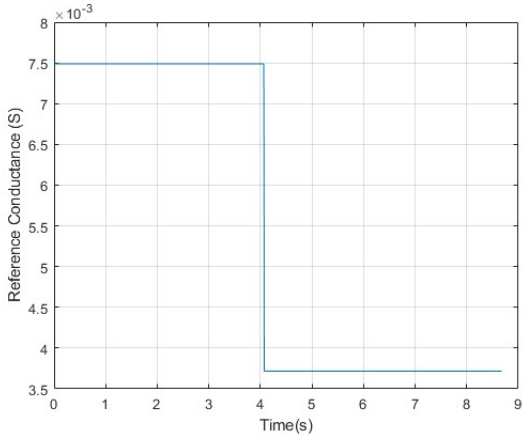


Figure 5.43. Reference conductance vs. Time at 100 µs sampling rate (Second approach).

The result shows that there is only one peak in the current and voltage plots since we only increased the resistance one time.

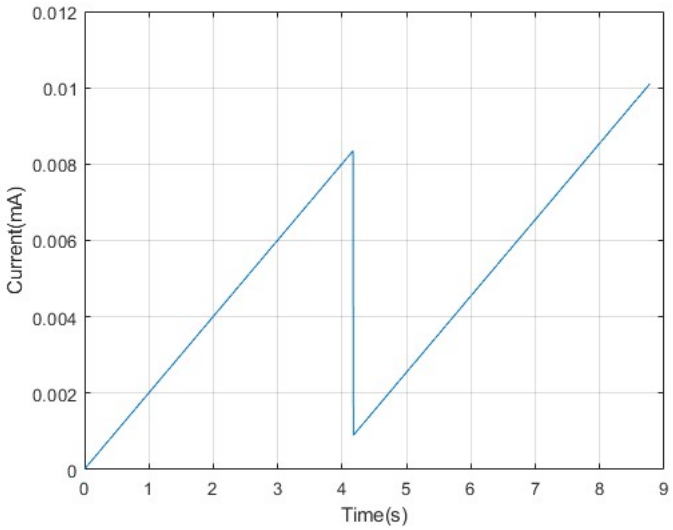


Figure 5.44. Current vs. Time at 100 µs sampling rate (Second approach).

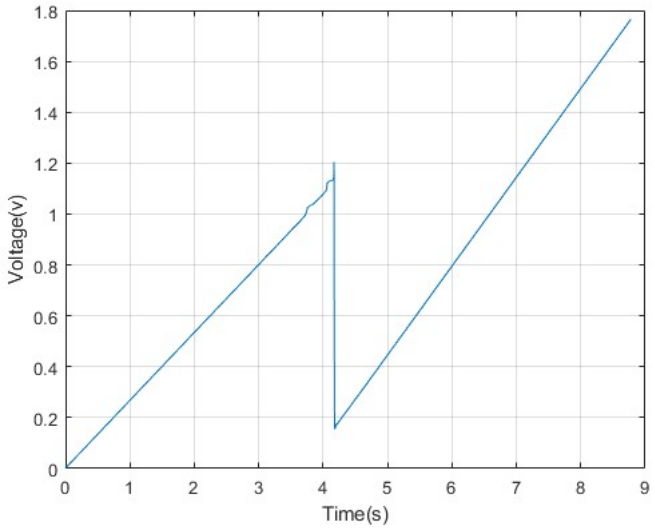


Figure 5.45. Voltage vs. Time at 100 µs sampling rate (Second approach).

The I-V curve reveals that feedback was applied for one cycle and then behaves linearly because the resistance did not change anymore.

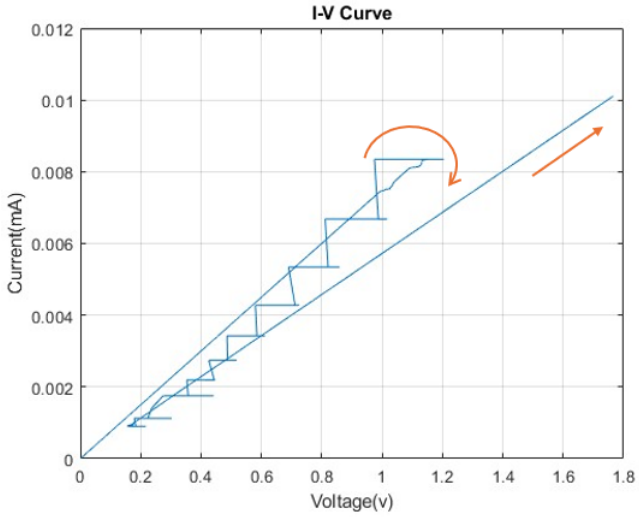


Figure 5.46. I-V plot for 100 µs sampling rate (Second approach).

5.6.3 20 µs sampling rate

At the last step, I tried to optimize the system and used the highest resolution sampling rate of 20 µs, with satisfying results that are comparable to the last two sampling rates. For the 20 µs sampling rate, I conducted two tests. When compared with the previous tests, the number of data points to be read by the FIFO is much higher since each data point is saved every 20 µs. However, the FIFO write buffer of 1023 elements in the FPGA can still support the system. The only change is that I increased the number of samples per read from each FIFO read block in the host, and as a result, the total number of data points is approximately 10 times greater than in the 200 µs sampling rate test.

First approach

In this approach, I increased the resistance using the potentiometer three times. The initial resistance value was 105 Ω, and it was increased to 130 Ω, 190 Ω, and 305 Ω respectively. The resistance chart shows that there are two noise spikes at the 2nd and 3rd increments of resistance.

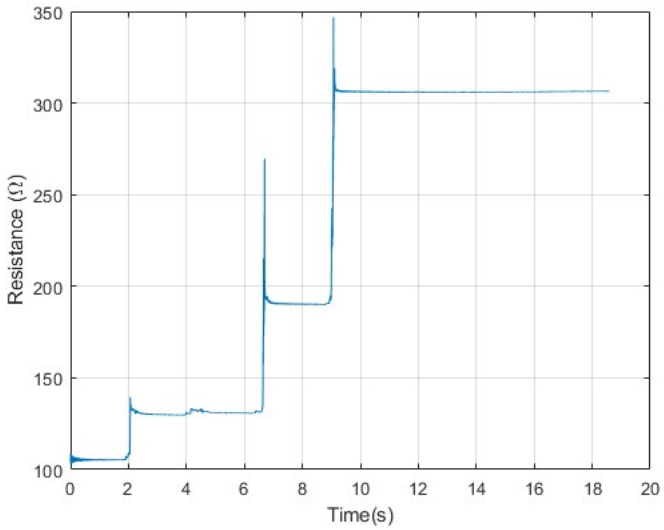


Figure 5.47. Resistance vs. Time at 20 µs sampling rate (First approach).

By comparing the conductance plots, we see that the reference conductance is accepted for the minimum values, and there are three steps of reduction in conductance occurring at the same times as the resistance increments.

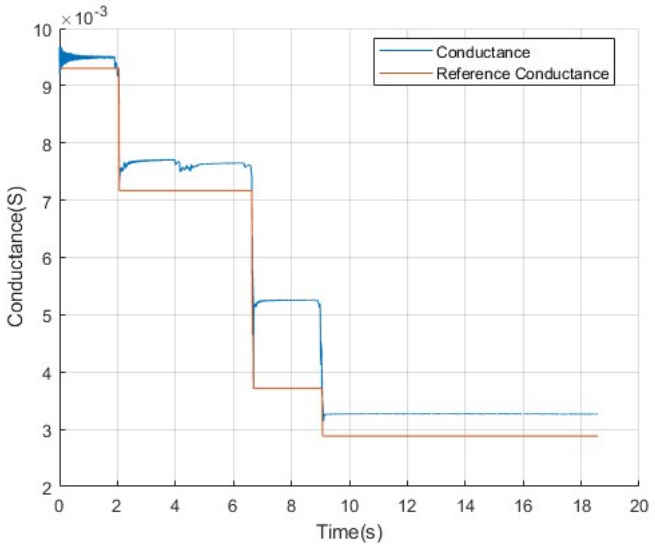


Figure 5.48. Comparison of conductance and reference conductance at 20 µs sampling rate (First approach).

The plots for current and voltage reveal three instances of applied feedback during the resistance increment between seconds 2 and 9. We can also see that at the end of the process, feedback is applied even though the resistance was not changed. This is due to the first feedback condition, which reduces the input current by 20 percent when the current limit, equal to 19 mA, is reached.

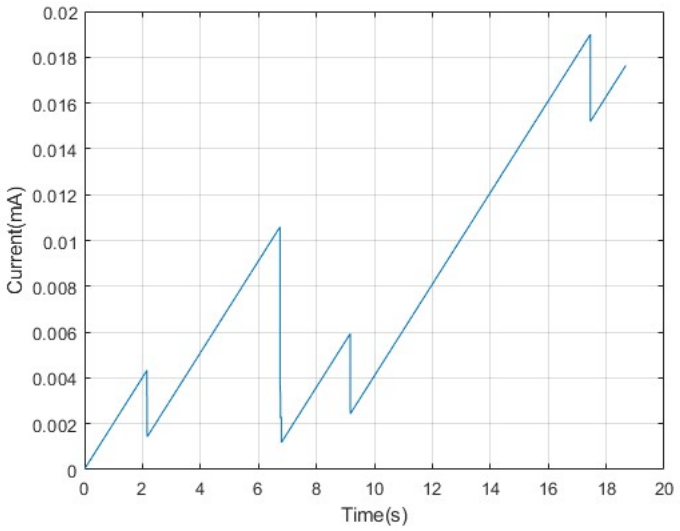


Figure 5.49. Current vs. Time at 20 µs sampling rate (First approach).

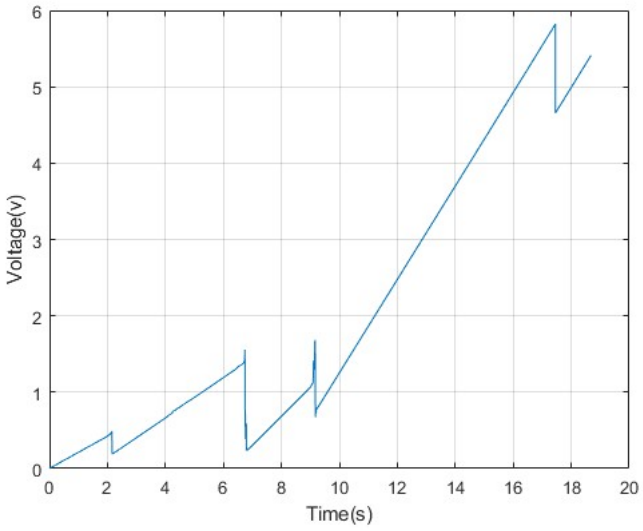


Figure 5.50. Voltage vs. Time at 20 µs sampling rate (First approach).

The I-V curve shows that we have four cycles of the feedback pattern, three of which occur initially due to the increment of resistance, and the last one is due to the current limit feedback condition.

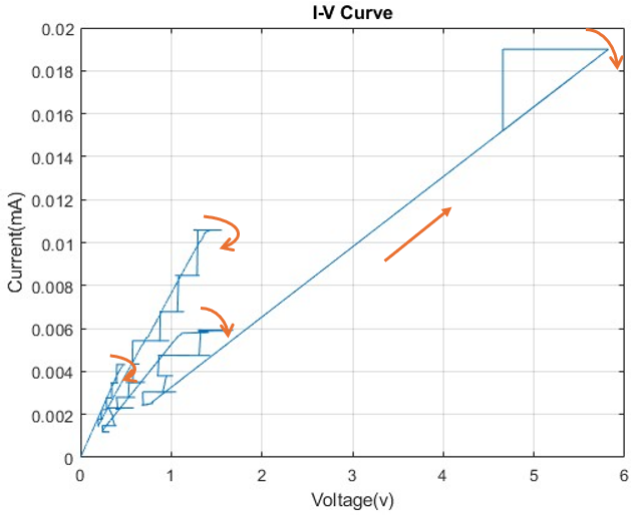


Figure 5.51. I-V plot for 20 µs sampling rate (First approach).

2nd approach

In this approach, I increased the resistance gradually for the first nine seconds. We can observe some spike noise at the last points of the increment.

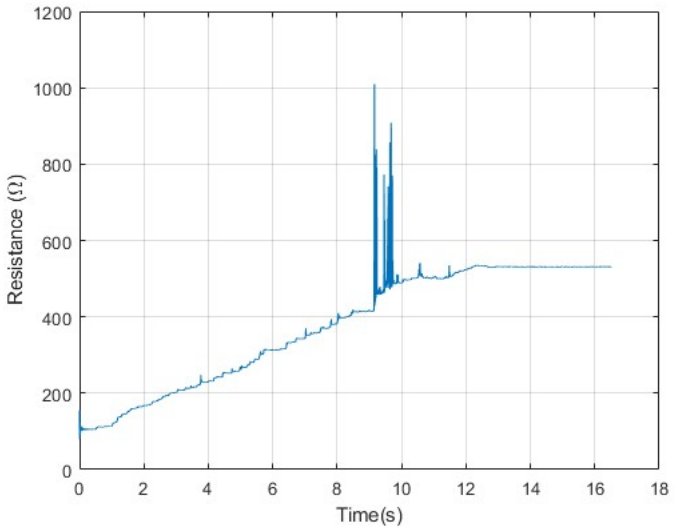


Figure 5.52. Resistance vs. Time at 20 µs sampling rate (Second approach).

The conductance plots show that the reference conductance perfectly accepts the values of the drop in conductance before the noise spikes, and the number of steps in reduction is fewer than in the main conductance plot, since it only accepts differences greater than a 5 percent drop. At the end, it reads the least amount, which is related to the noise.

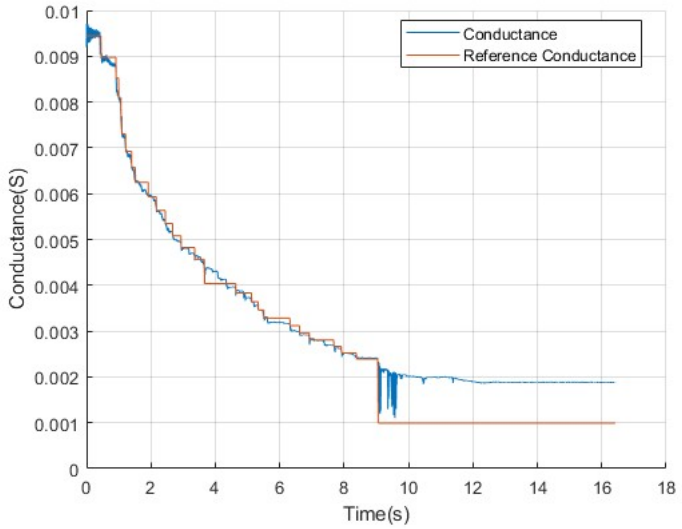


Figure 5.53. Comparison of conductance and reference conductance at 20 µs sampling rate (Second approach).

The current and voltage plots with respect to time reveal the same patterns of sawtooth increases in the first 9 seconds, and then start to linearly increase to the end of the process.

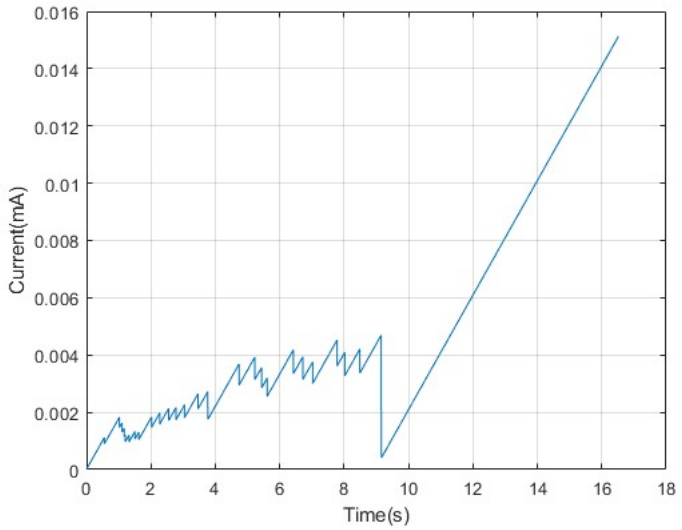


Figure 5.54. Current vs. Time at 20 µs sampling rate (Second approach).

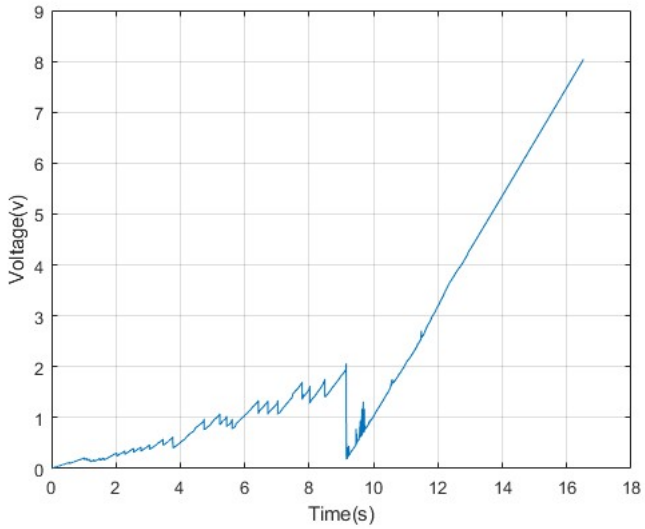


Figure 5.55. Voltage vs. Time at 20 µs sampling rate (Second approach).

At the end, we can see many cycles of applied feedback in the I-V curve between the 0 to 2 volts voltage range and the 0 to 5 mA current range, after which their pattern remains linear.

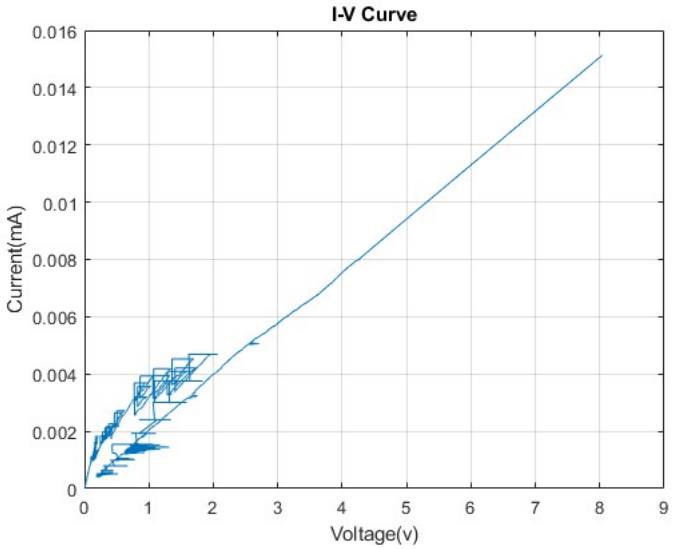


Figure 5.56. I-V plot for 20 µs sampling rate (Second approach).

5.7 Conclusion

To summarize this chapter, we investigated three different sampling rates for modeling the feedback-controlled electroburning algorithm. The reference conductance proved effective in initiating new current cycles, ensuring consistent and precise feedback application throughout the process.

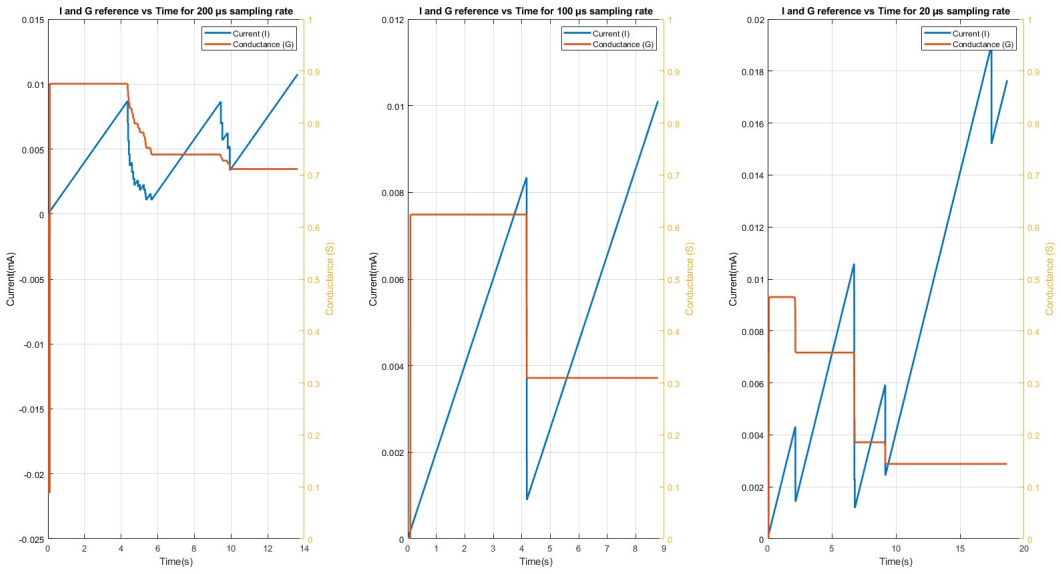


Figure 5.57. Comparison of current and reference conductance at 200 µs, 100 µs and 20 µs sampling rates.

All three rates successfully implemented the feedback mechanism. A comparison of the I-V curves for sampling rates of 200 µs, 100 µs and 20 µs showed resistance increasing in discrete steps. The observed cycles, characterized by repeating triangular patterns corresponding to each step of increasing resistance, illustrate the feedback process, where a conductance reduction exceeding 5% triggers the applied current to retract to 80% of its previous value.

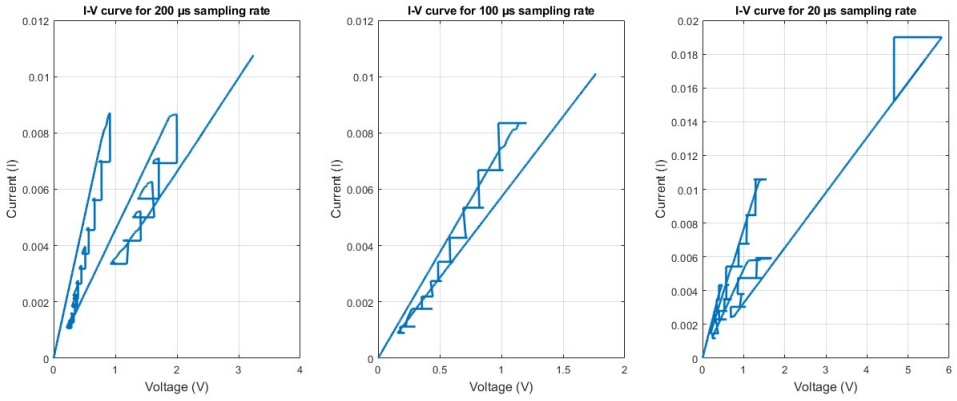


Figure 5.58. I-V plots for 200µs, 100µs and 20 µs sampling rates.

Chapter 6

Conclusion

The simulation results of graphene's electronic properties using QuantumATK demonstrate that graphene with a bow-tie nanogap structure is a viable candidate for use as an electrode for single-molecule electronic devices. However, the findings indicate that the geometry of the left and right contact leads in the molecular configuration, as well as the size of the graphene layer, play a crucial role in charge transport behavior. The simulation results indicate that introducing a single atom within the nanogap structure can enhance charge transport performance. However, the localization of states in the bow-tie configuration is highly sensitive to the precise atomic arrangement resulting from graphene patterning and electroburning. This process inherently involves a degree of randomness, making precise control at the atomic scale unachievable.

The results from the developed feedback-controlled system demonstrate the possibility of implementing a fast feedback controlled system for applying to graphene electrode. The system achieves high-resolution performance with sampling rates up to 20 µs, highlighting its effectiveness for nanogap formation in graphene electrode and it has performance comparable with literature. [1]

In future work, the complete structure of a single-molecule device can be explored, focusing on the charge transport behavior in a nanogap-separated electrode. This will involve selecting an appropriate molecule to anchor to the graphene electrode, with further analysis conducted from a simulation perspective to better understand the interactions and transport properties.

Another important consideration for future work is the use of pre-patterned graphene in a bow-tie shape to enable more precise control over the positioning of the nanogap and improve yield. This can be achieved by applying the fast feedback-controlled electroburning algorithm and analyzing the behavior of the graphene material under this process. Following the formation of the nanogap, a suitable molecule can be deposited into the nanogap, and the resulting device can be characterized to assess its potential as a single molecule device. Additionally, enhancing the yield will require careful optimization of both the nanogap positioning with the pre-patterned bow-tie structure and the fast feedback-controlled electroburning process.

Appendix A

Practical guide

This guide outlines the setup and operation of the system developed for feedback-controlled electroburning using a potentiometer.

A.0.1 Hardware

In the first step, the user must connect all the analog input and output cards to the compact-RIO chassis (cRIO 9030). These include one NI 9265 card and one NI 9223 card. In our test setup, only one channel from the NI 9265 card was used to generate current, and one input channel from the NI 9223 card was utilized to read voltage.

In the next step, the user needs to connect the power terminal of the cRIO-9030 to a voltage generator and set the system's power supply to 24 volts.

After powering the chassis, the green LED indicating the power connection should light up on the hardware.

To connect the controller to the computer, the user can use either an Ethernet cable or a USB cable. After connecting the Ethernet cable to the computer, the yellow LED on the Ethernet port should illuminate, and the green LED on the Ethernet port should start blinking.

The NI 9265, as an analog current generator, requires an external power source. Therefore, the user must supply input power from the voltage generator, set to 10 volts (or 9 volts). Pin number 8 on the NI 9265 is designated for V_{sup}, and pin number 9 is for COM.

In this system, channel one of the NI 9265 (AO0) is used. Therefore, the user must connect the wire from terminal 1 (AO0) to the output pin of the potentiometer and terminal 2 (COM0) to the GND pin of the potentiometer.

To read the voltage using the NI 9223, with channel one being utilized, the user must connect the coaxial cable to screw terminal 1 of the NI 9223.

A.0.2 Software

In the first step, the user must install the required drivers and software on the computer, which include LabVIEW, the LabVIEW FPGA Module, the Real-Time Module, and the NI CompactRIO driver. After installation, the user should activate the software.

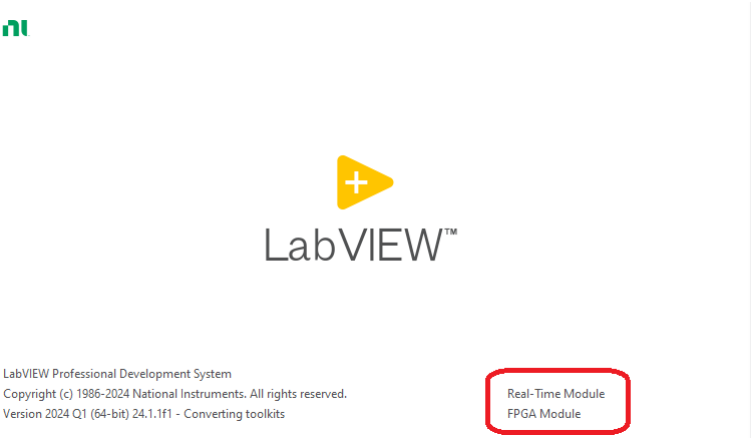


Figure A.1. LabVIEW program

The next step in setting up the system is to recognize the chassis device, which includes the controller and analog inputs and outputs, using NI MAX (Measurement and Automation Explorer).

Figure A.2. Measurement and Automation Explorer.

After opening NI MAX, expand the "Remote Systems" option. The device named "NI-cRIO-9030-01A76645" should appear in the list.

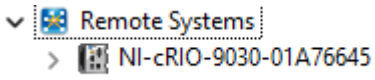


Figure A.3. Remote Systems

The user must double-click on the "NI-cRIO-9030-01A76645" icon and enter the credentials in the right window to set permissions and log in.

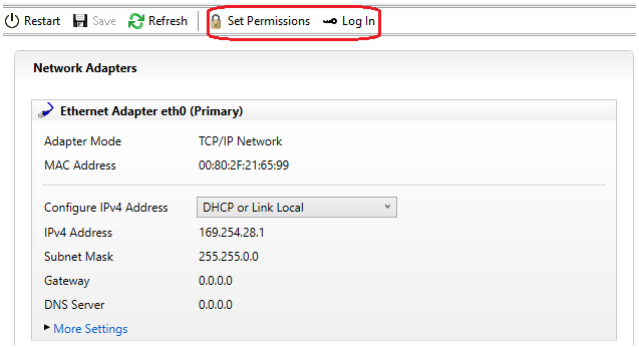


Figure A.4. Set permissions and log in

After connecting and recognizing the device, the user must open the LabVIEW project. By right-clicking on the project name, select the "New" option, and then choose "Targets and Devices."

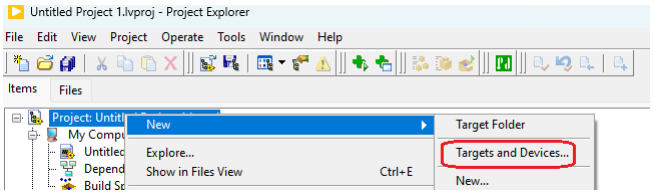


Figure A.5. LabVIEW project window

The user can discover the "NI-cRIO-9030-01A76645" in the opened window by double-clicking on the "Real-Time CompactRIO" folder.

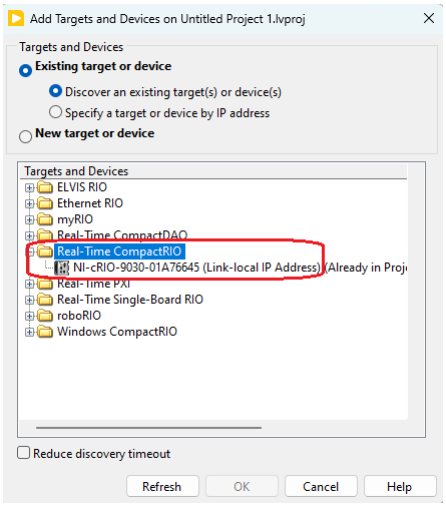


Figure A.6. LabVIEW Targets and Devices window

The user must check the FPGA interface in the opened window to enable running the FPGA target in the project.

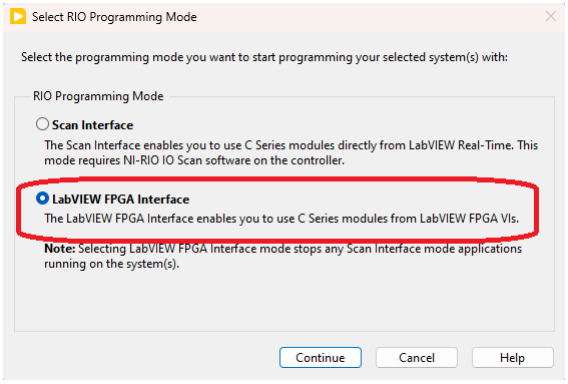


Figure A.7. LabVIEW select programming Mode window

After that, by expanding the "NI-cRIO-9030-01A76645" icon in the project tree, the "Chassis (cRIO-9030)" should appear. Expanding this will reveal the "FPGA Target (RIO0, cRIO-9030)." By expanding the "FPGA Target (RIO0, cRIO-9030)," the connected modules will also become visible in the project tree.

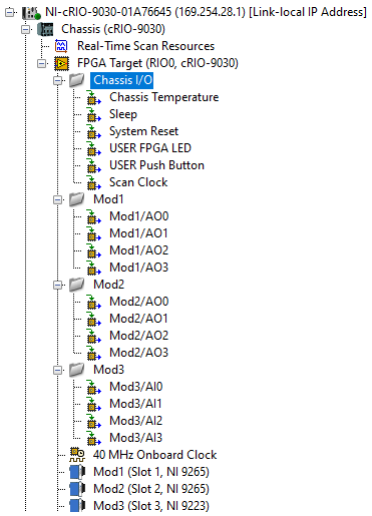
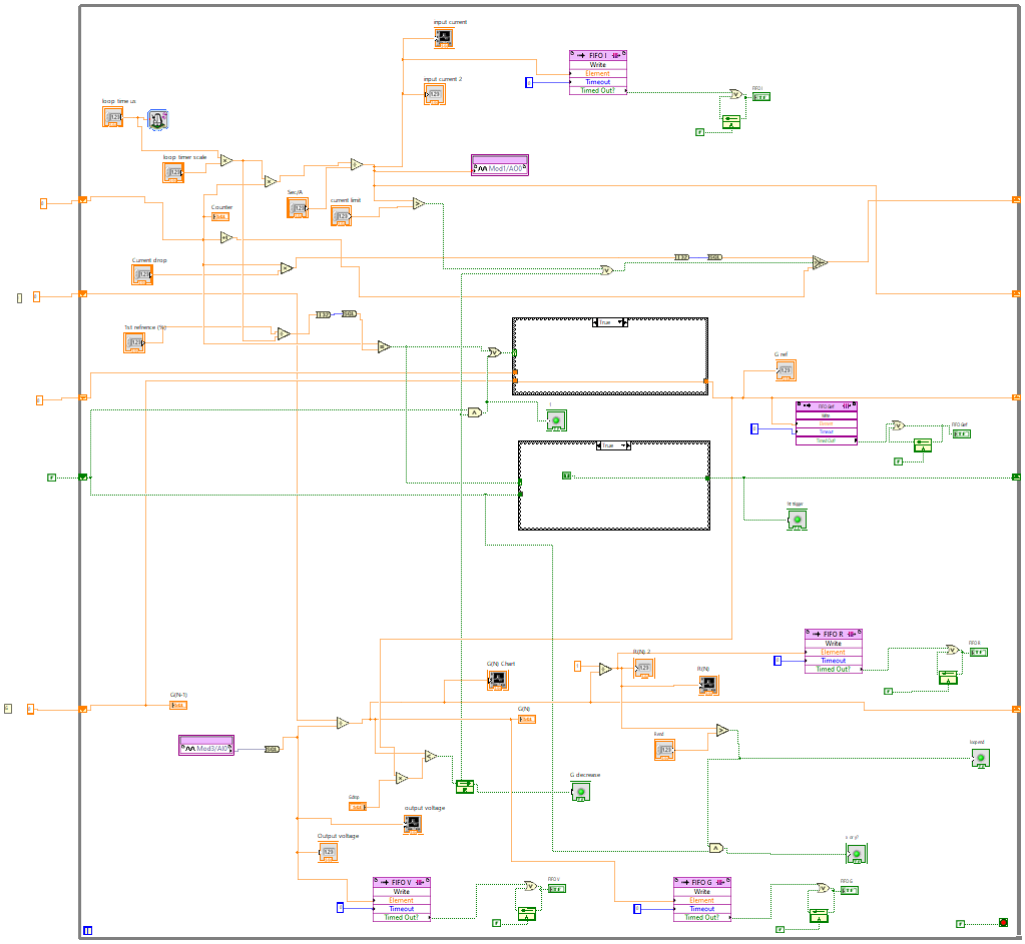


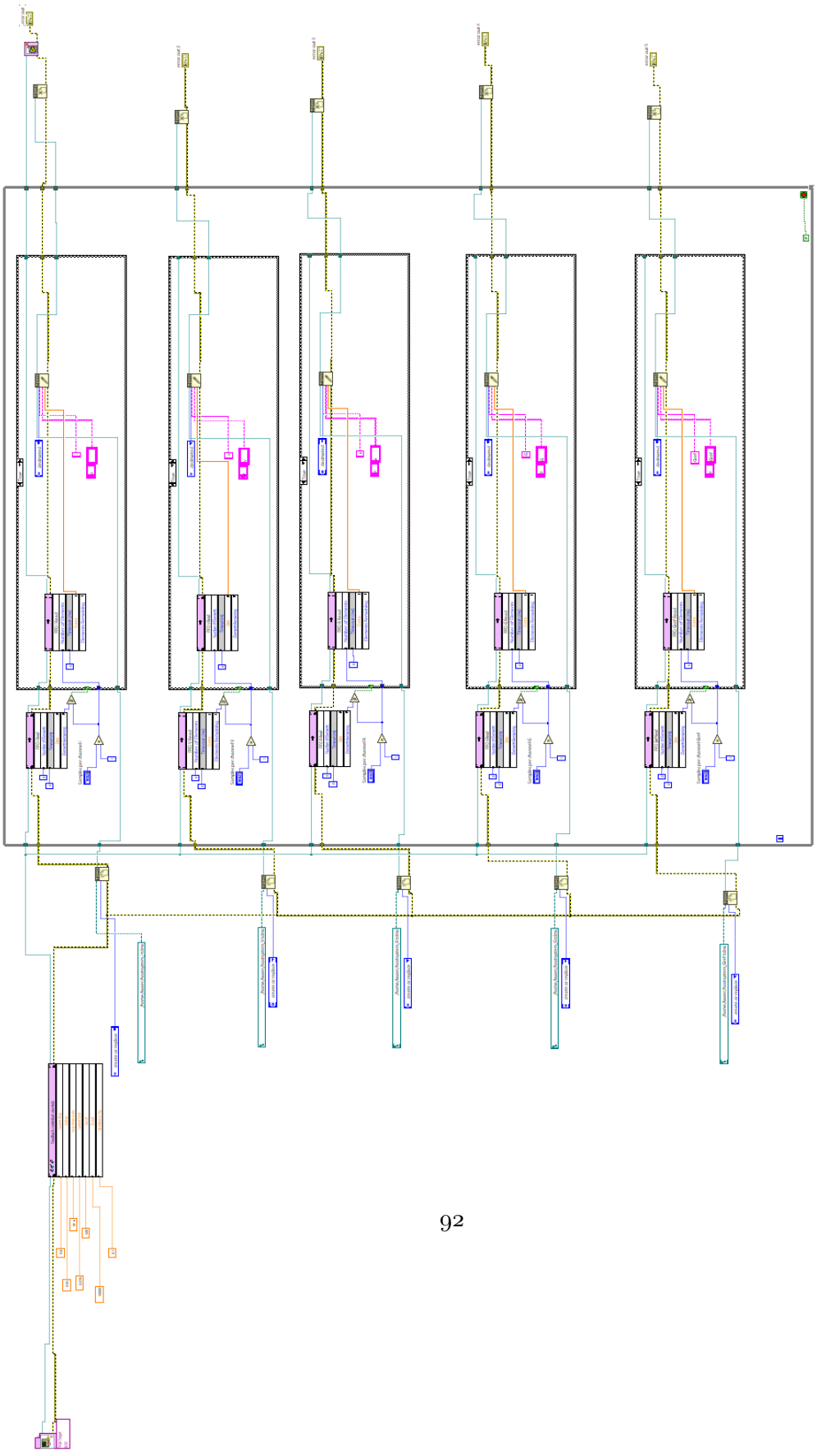
Figure A.8. LabVIEW Project tree.

Next, the user needs to add the FPGA target VI file (Feedback controlled electroburning-FPGA.vi), and compile it by clicking on the "Run" icon. Once the compilation is complete, the program will start running on the FPGA target. To transfer data to the computer, the user must add the Host VI, (Feedback controlled electroburning-Host.vi), and execute it.

A.0.3 Block diagram for the feedback-controlled electroburning, FPGA target.



A.0.4 Block diagram for the feedback-controlled electroburning, Host program.



In the next step, to import the saved data from the FPGA to the host PC, the user must open MAX, right-click on "NI-cRIO-9030-01A76645," and then click on the "file transfer" icon.

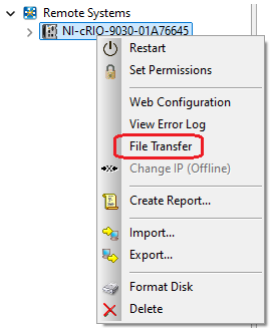


Figure A.9. Transfer data by NI MAX

Then, a credentials prompt will appear in the browser window. By entering the credentials, the user can access the saved data in the FPGA memory and download it from the directory defined for the TDMS data in the host VI.

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