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# Towards quantum devices: a study on the fabrication and measurement of $WS_2$ field effect transistors

MASTER DEGREE THESIS

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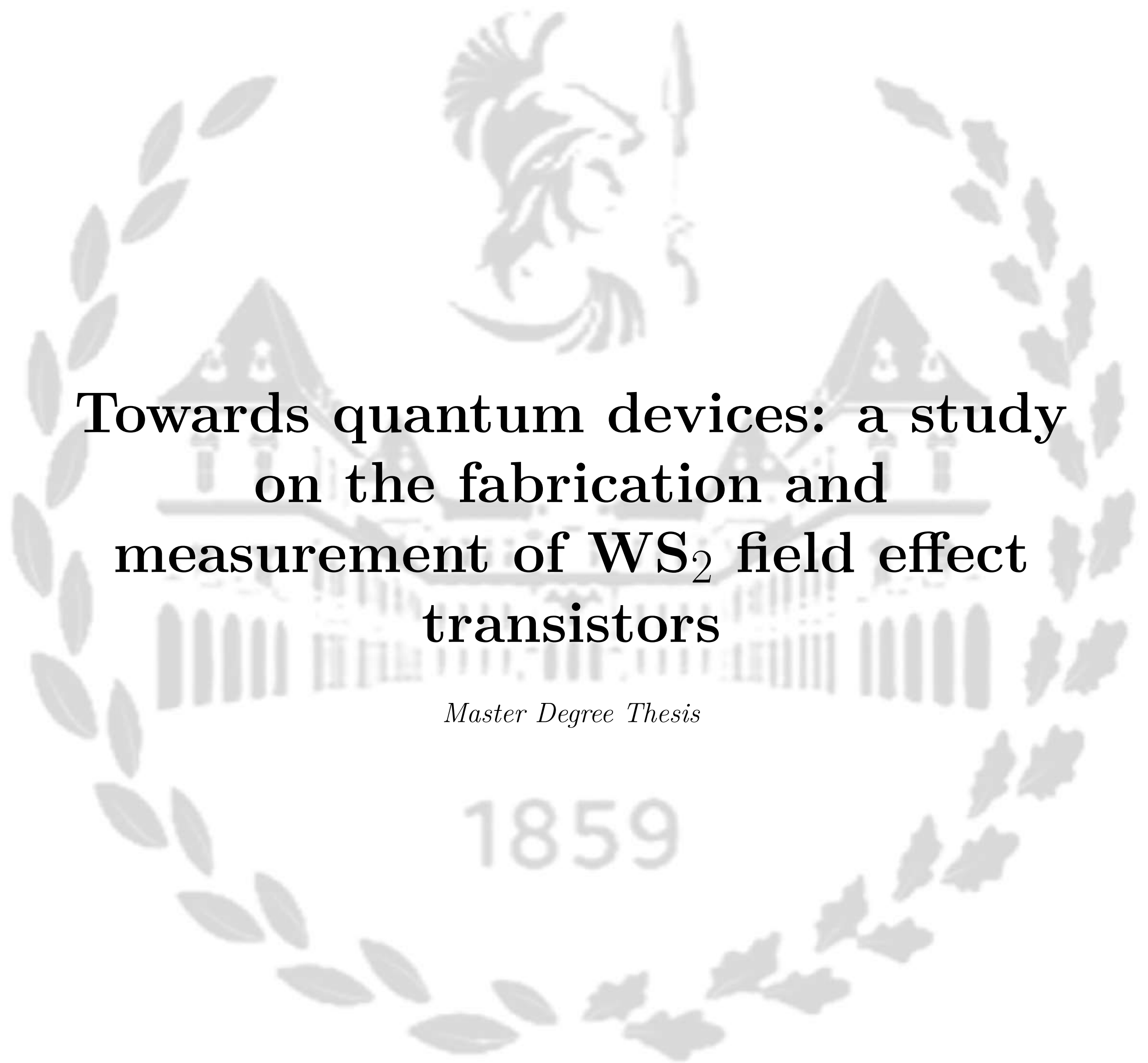


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*Master Degree Thesis*

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"*It is not our abilities that show who we truly are, it is our choices.*"

Albus Dumbledore

POLITECNICO DI TORINO

Physics of Complex Systems

**Towards quantum devices: a study on the fabrication and measurement of $WS_2$ field effect transistors**

by Alberto ROSSO

# ABSTRACT

Over the past few decades, two-dimensional (2D) transition metal dichalcogenides (TMDCs) have garnered significant attention for their exceptional electrical performance and flexibility in functional modulation. These semiconducting materials, characterized by a layered structure with weak van der Waals interlayer interactions, present a bandgap ranging from 0.5 eV to 2.0 eV, making them promising candidates for future spintronic and valleytronic applications. Unlike graphene, TMDCs possess a substantial bandgap, making them suitable for transistor fabrication. A major application of TMDCs is in field-effect transistors (FETs), where their distinct properties, such as potential immunity to short-channel effects and reduced scattering due to their intrinsic 2D confinement, are utilized to potentially outperform conventional silicon-based devices.

In this thesis, the variation of the quality of metal contacts as a function of the number of layers of each semiconductive channel is examined. Recent studies suggest that $WS_2$ may exhibit promising electrical properties, therefore it is selected as the TMDC of interest. The core of this work is devoted to the fabrication of multilayer $WS_2$ transistors on $SiO_2$. The research then moves to the more challenging fabrication of monolayer $WS_2$-based transistors on sapphire substrate. Electrical measurements highlight the poor quality of the contacts, pointing out the need of further research to optimize $WS_2$ monolayers grown by chemical vapor deposition. Photolithography is employed to produce source and drain contacts for the electrical characterization. The study emphasizes the strengths and criticalities of manipulating $WS_2$ flakes obtained by mechanical exfoliation, with specific focus on the role of the chemicals used and arrangement of metal contacts. A fully mechanized transferring technique to transfer exfoliated flakes onto gold contacts is used, and electrical characterisation at room temperature is used to assess the device performance. Finally, AFM scanning allows the estimation of the thickness and number of layers of each flake, so that the study of the respective resistance trend is allowed.

We used electrical measurements to extract transfer and output curves to measure intrinsic properties such as threshold voltage and on/off ratio. MOSFET mobility measurements are then detailed, illustrating methods to extract these parameters from experimental data. The field-effect mobility in the devices is found to be in the range of 3–9 $cm^2/Vs$ at source-drain voltage ($V_{ds}$) of 6V, which is relatively low compared to values reported in other

studies. Additionally, the devices exhibit non-linear output curves, with a few showing asymmetry around $V_{ds} = 0V$. These observations underline the complexity of achieving consistent mobility performance across devices and highlight potential areas for further optimization.

The non-linearity of output curves results from the Schottky barrier arising at the contact sides; this is expected because of the Schottky-Mott rule and the absence of a contact intermediate metal layer, e.g. indium, to decrease the barrier. Furthermore, asymmetric non-linearity may come from different Schottky barrier heights between source and drain interfaces. Achieving good ohmic metal contacts in TMDCs remains challenging, as the origins of interface phenomena, like Fermi level pinning and Schottky barrier height, are still under debate. We believe that the observations in this thesis can advance the understanding and practical application of TMDCs in electronic devices, focusing on optimizing contact properties to enhance device performance.

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# List of Abbreviations

| | |
|---|---|
| **ACMV** | **A**ir **C**onditioning and **M**echanical **V**entilation |
| **AFM** | **A**tomic **F**orce **M**icroscopy |
| **ALD** | **A**tomic **L**ayer **D**eposition |
| **BL** | **Bi** **L**ayer |
| **CBM** | **C**onduction **B**and **M**inimum |
| **CVD** | **C**hemical **V**apor **D**eposition |
| **DFT** | **D**ensity **F**unctional **T**heory |
| **DI** | **D**e-**I**onized |
| **TMDC** | **T**ransition **M**etal **D**i**C**halcogenides |
| **DOS** | **D**ensity **O**f **S**tates |
| **FET** | **F**ield **E**ffect **T**ransistor |
| **FLP** | **F**ermi **L**evel **P**inning |
| **HEPA** | **H**igh **E**fficient **P**articulate **A**ir |
| **IMRE** | **I**nstitute of **M**aterials, **R**esearch and **E**ngineering |
| **MOSFET** | **M**etal **O**xide **S**semiconductor **F**ield **E**ffect **T**ransistor |
| **PDMS** | **P**oly**D**i**M**ethyl**S**iloxane |
| **PL** | **P**hoto-**L**uminescence |
| **PPC** | **P**oly**P**ropylene **C**arbonate |
| **PR** | **P**hoto**R**esist |
| **PVD** | **P**hysical **V**apor **D**eposition |
| **RIE** | **R**eactive **I**on **E**tching |
| **RPM** | **R**evolutions **P**er **M**inute |
| **SBH** | **S**hottky **B**arrier **H**eight |
| **SCCM** | **S**tandard **C**ubic **C**entimeter per **M**inute |
| **SL** | **S**ingle **L**ayer |
| **STM** | **S**canning **T**unneling **M**icroscopy |
| **TMAH** | **T**etra**M**ethyl**A**mmonium **H**ydroxide |
| **ULPA** | **U**ltra-**L**ow **P**article **A**ir |
| **UV** | **U**ltra **V**iolet |
| **VBM** | **V**alence **B**and **M**aximum |
| **XPS** | **X**-ray **P**hotoelectron **S**pectroscopy |

# List of Symbols

| | | |
|---|---|---|
| $a$ | lattice constant | m |
| $W$ | width | m |
| $L$ | length | m |
| $t$ | thickness | m |
| $E$ | electric field | $\mathrm{V\,m^{-1}}$ |
| $I$ | electric current | A |
| $V$ | voltage | V |
| $n$ | density of carriers | $\mathrm{m^{-3}}$ |
| $R$ | electric resistance | $\Omega$ |
| $R_s$ | sheet resistance | $\Omega$ |
| $S$ | pinning factor | |
| $D$ | surface density | $\mathrm{m^{-2}}$ |
| $T$ | temperature | K |
| $g$ | conductance | S |
| $C_{ox}$ | oxide capacitance | $\mathrm{Fm^{-2}}$ |
| $Q_n$ | sheet charge density | $\mathrm{Cm^{-2}}$ |
| $F$ | Fresnel diffraction coefficient | |
| $w$ | aperture | m |
| $X$ | distance | m |
| $\rho$ | electric resistivity | $\Omega$m |
| $\chi$ | electron affinity | $\mathrm{J\,mol^{-1}}$ |
| $\Phi_M$ | metal workfunction | J |
| $\Phi_B$ | Schottky barrier height | J |
| $\varepsilon$ | dielectric constant | |
| $\mu$ | carrier mobility | $\mathrm{m^2/Vs}$ |
| $\lambda$ | wavelength | m |

*A te, che ogni giorno illuminasti e con il sorriso mi capisti. . .*

# Chapter 1

# Introduction

The rapid advancements in semiconductor technology have sparked a growing interest in exploring new materials for field-effect transistors (FETs), with particular focus on transition metal dichalcogenides (TMDCs) such as tungsten disulfide ($WS_2$).

Despite TMDCs rapid growth in the semiconductor industry, much work still needs to be done to match the performance of the commonly used silicon, surpass it and develop new, better and more efficient electronics. In particular, not much is known about the physics behind metal-semiconductor interfaces and building clean and effective junctions is still a challenge. Addressing these limitations is essential for developing high-performance $WS_2$-based FETs.

This thesis focuses on the descriptive analysis of the entire manufacturing process of a $WS_2$ transistor. The production of working devices is aimed at their electronic characterisation and the study of the correlation between their electrical properties and channel thickness, with a particular focus on the quality of the metal contacts made. An equally detailed description of the manufacturing process of $WS_2$ monolayer transistors is finally reported, analyzing critical points and differences with respect to the previous protocol.

The thesis is structured as follows: *chapter2* provides an overview of the chemistry of transition metal dichalcogenides and on the physics behind Schottky junctions; *chapter3* details the fabrication techniques used to fabricate FETs using $WS_2$ flakes on $SiO_2$, while *chapter4* presents the results of the electrical characterization. *Chapter5*, instead, describes the process to fabricate FETs with monolayer $WS_2$ on sapphire substrate.

In summary, this thesis aims to deepen the understanding of $WS_2$-based FETs by investigating the impact of device fabrication and metal contacts on their performance, ultimately contributing to the advancement of TMDC transistor technology.

# Chapter 2

# Potentials and challenges of TMDCs

## 2.1 Transition metal dichalcogenides

In the last decade, two dimensional (2D) transition metal dichalcogenides (TMDC's) have garnered significant attention due to their outstanding performances in the electrical characterization of micro- and nanoscopic devices, not to mention their flexibility for functional modulation [1]. These semiconducting materials are promising candidates for the development of spintronics and valleytronics of the future because of their distinct properties, such as potential immunity to short-channel effects and reduced scattering due to their intrinsic 2D confinement[2]. Their strength relies on their bidimensional structure, where electron transport occurs primarily within a single atomic layer, which leads to reduced scattering compared to 3D bulk materials. In silicon-based devices, for example, electrons scatter due to interactions with defects and impurities that exist throughout the bulk material. Since TMDCs have fewer bulk-like dimensions, electron mobility is less impacted by these imperfections and scattering from out-of-plane phonons is minimized.
TDMCs are described by the general formula $MX_2$, where $M$ stands for a transition metal, like Mo or W, and $X$ stands for the chalcogen, Se, Te or S. Therefore, the most common TMDC materials are $MoS_2$, $MoSe_2$, $WSe_2$ and $WS_2$.

As shown in *Fig.2.1c*, TMDCs tend to self-organize in a layered structure characterized by van der Waals (vdW) interlayer gaps. The chemical reason behind this arrangement is the presence of chalcogenide dangling-bonds-free surfaces on each layer that develop dipole interactions with the neighboring surface. These interlayer interactions are much weaker compared to the intralayer bonds, allowing the layers to easily slide over one another. Such a mechanics may remind of the famous structure of graphene; TMDCs however, do not present any Dirac electrons and display a discrete bandgap of

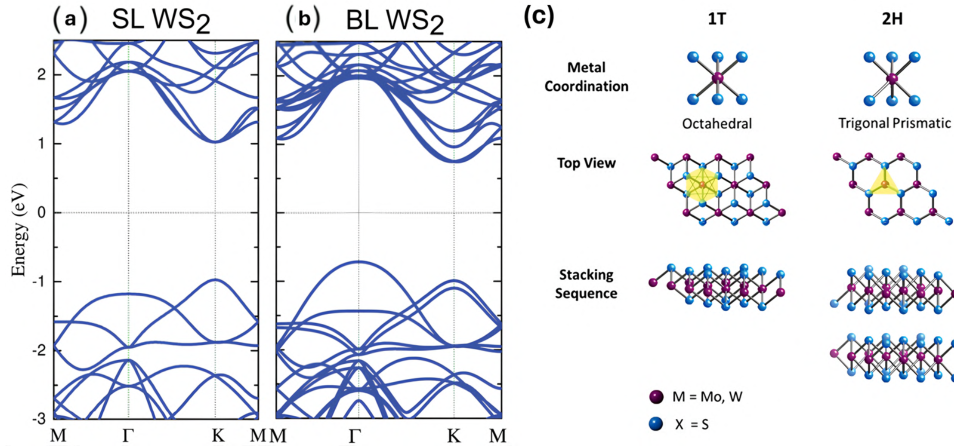


*Figure 2.1:* a)Band diagram of $WS_2$ single layer(SL). b)Band diagram of $WS_2$ bilayer(BL): one can appreciate a slight change in the energetics with respect to the single layer case. Both images are taken from [5] and were produced by density functional theory (DFT) calculations. c)Schematics of the 3D structure of typical TMDC[6].Different symmetries can be obtained in the structural unit cell. Trigonal structure (1T) presents a metallic behaviour, while more complex hexagonal (2H) symmetry characterizes the semiconducting behaviour of the TMDC. Being the 2H phase thermodynamically stable, it is the most common symmetry studied.[7]

0.68 eV - 1.58 eV [3], as shown in *Fig.2.1a,b.* Despite the large electron mobility of graphene, the lack of bandgap makes it unattractive for transistor applications, whereas TMDCs have sufficient large bandgap to allow on and off transistor activity.[4]

Among the numerous advantages of exploiting TMDCs as building materials for FET technology, there's their unique flexibility. The mechanical origins of this peculiar property have to be searched in the lattice structure of the most common TMDCs, which show strong intralayer covalent bonds, capable of providing mechanical strength, and weak vdW interlayer interactions, empowering a high flexibility. Moreover, monolayers do not show any interlayer force, allowing the material to bend and flex more easily, as shown in *Fig.2.2a.* This peculiar property was indeed explored by Zhao et al.[8] in the realization of rolled-up higher order van der Waals superlattices, shown in *Fig.2.2b.* The same research group, under the supervision of Prof. Duan, explored multiple device applications by designing FETs integrating TMDC 2D layers with 1D nanowires and nanoribbons[9][10][11]. The reasons why one should investigate the potentialities of these outstanding structures are many; as also shown by Liao et al.[12] with graphene, the transfer of synthetic nanoribbons as gate dielectric can create top-gated FETs with high mobility and large current densities.

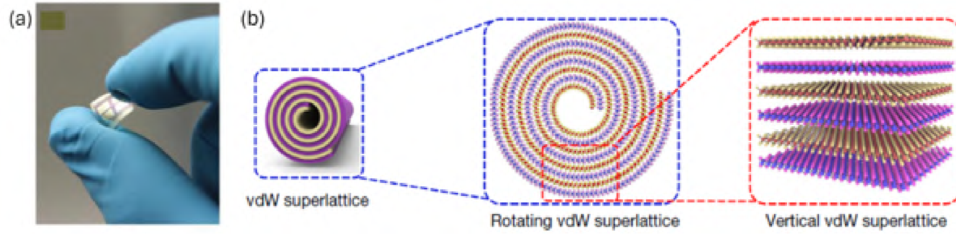


*Figure 2.2:* a) Practical demonstration of device flexibility[13]. b) Magnified schematic view of the roll-up in high-order superlattices van der Waals heterostructures[8].

### 2.1.1 TMDC field-effect transistors

One of the most common uses of TMDC materials is the design of basic 2D electronic components with the objective of testing their performance and comparing it with the ones of standard silicon devices. Although the "lab-to-fab" [14] process of TMDCs is still not as good as silicon's, the electrical performances of the latter are being caught up by the rising technology of metal chalcogenides. One common battlefield where the two materials could be compared is field effect transistors (FETs).

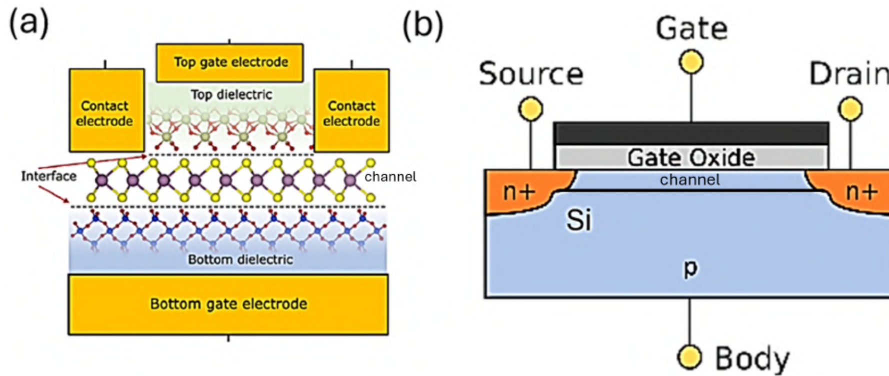


*Figure 2.3:* a)Image of a 2D TMDC FET[5]. Instead of standard Si, the device presents a thin layer of TMDC between the dielectric bulk and the contact electrodes, thus allowing for the formation of two interfaces. b) Image of a standard silicon FET, characterized by three metal contacts; drain and source are normally doped with respect to the bulk. Doping is however difficult to achieve in 2D TMDC FETs because of their dimensionality.

Invented in 1925 by Julius Edgar Lilienfeld and officially produced only in early '50s, FETs paved the way for the rapid advancement of integrated circuit technology. The simplicity of these devices is the key to their success. As shown in *Fig.2.3a*, the FET basic structure is made of three components: source, drain and gate. The current flows in a region of the device called "channel", placed between two terminals. In simple terms, carriers enter the channel from the source and leave it from the drain; the gate terminal, instead, controls the conductivity of the channel between source and drain; one thus defines the threshold voltage ($V_{th}$) as the minimum voltage required to create a conductive channel. The value of the threshold voltage, which often depends

on the choice of material and geometrical properties, is then determining the operational mode of the transistor. In other words, "enhancement-mode" transistors are normally-off devices that require a gate voltage to conduct, while "depletion-mode" transistors are normally-on devices which require a gate voltage to be turned off.

As their name itself suggests, field-effect transistors exploit the presence of an electric field created by the channel carriers attracted by the gate voltage. Such a voltage control is essential for the perfect working of the device, but it usually becomes problematic in silicon when scaling down the channel length. The drain potential could indeed influence the gate control, causing leakage currents and degraded switching characteristics. In contrast, TMDC-based FETs exhibit better immunity to short channel effects because of the natural confinement of carriers, which leads to better electrostatic control over the channel even when the channel length is reduced. Moreover, TMDCs have higher bandgaps which can compensate for the lowering of the barrier between the source and drain typical of short channel effects.

The gate voltage could be either applied on the top of the device, by depositing metal at the end of fabrication process, or on the bottom, by depositing the metal first and then proceeding with the rest of the fabrication; *Fig.2.3a* shows both of them. Standard FETs are realized in silicon, thus the different regions of the device can be created by modulating the doping concentration. In the case of TMDC mono- or bilayer transistors, instead, the three terminals can be created by metal deposition only. The most popular type of FET is the so-called metal-oxide-semiconductor (MOS)FET, which makes use of a MOS junction to control the channel conductivity. The advantage in using a thin layer of dielectric to isolate the gate contact from the channel bulk lies in the high input impedance created, which makes the input gate current practically zero and widely increases the amplification power of the transistor. Moreover, the MOS junction behaves similarly to a capacitor whose conductive plates are replaced by the two interfaces between the oxide and either the metal or the semiconductor. Thanks to this last interpretation one can better appreciate the role of the gate dielectric, whose capacitance per unit area ($C_{ox}$) will modulate the amount of charge accumulated at the semiconductor interface and thus the conductance of the FET channel.

It is precisely the current that is of most interest in the characterization of such devices. According to the carrier that drives current in the gate channel, FETs split into n-type and p-type, whose majority carriers are respectively electrons and holes. As shown in *Fig.2.4a*, in standard Si-transistors both n and p-type behavior are easy to achieve. Technologically speaking, it is sufficient to dope the bulk of the device by the implantation of electrons acceptors (III group elements, such as Boron) and electron donors (V group elements, such as Nitrogen) for p and n-type doping respectively. In the case of a 2D semiconductor, however, engineering doping is a hard task. Normal doping techniques like ion-implantation, indeed, were designed for thick bulks and their use on thin 2D semiconductors may result in the permanent damage of their structure, thus altering their electronic band structure and compromising their electrical performance. Whereas many TMDC materials intrinsically possess a n-type behavior ($MoS_2$ and $WS_2$ are just an example), achieving

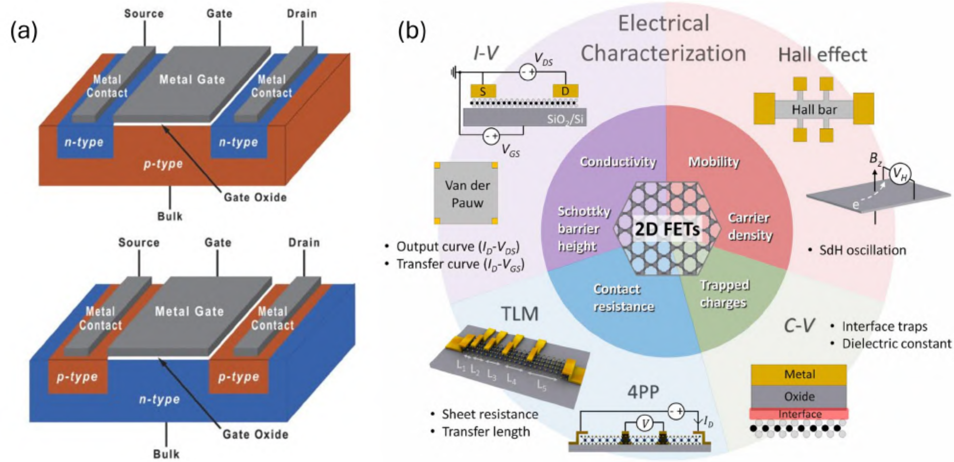


*Figure 2.4:* a)p-type and n-type metal-oxide-semiconductor(MOS)FETs[15]. One appreciates the difference in doping types in the different regions of the device. b)Electrical characterization methods of 2D FETs[16]. The Hall bar is not the only possible way to fully characterize a two-dimensional device, but it is certainly the one that better allows the determination of carrier mobility.

p-type is still an open challenge to the scientific community[17]. In the last years this topic has attracted much attention and many solutions have been proposed, though none of them has ignited the "lab-to-fab" process, yet. One major research field analyzes the role of sulfur vacancies on the top-most layer; they will ultimately introduce unoccupied defect states below the conduction band minimum(CBM) and, due to an energy offset, be more conductive and act as an electron acceptor (p-type), rather than electron donor[18][19]. A second research field has shown that the exposure of $MoSe_2$ and $WSe_2$ to some $O_2$-plasma a or UV-$O_3$ light might enhance p-type behavior by the superficial synthesis of the new chemical compound $WO_xSe_y/MoO_xSe_y$[20][21]. Moreover, surface TMDC oxidation has revealed to be a powerful technique to reduce metal contact resistivity[21]; such a behavior will be discussed further in Section 2.3.

## 2.2 Hall Bar geometry

One of the main focuses of the present research is the electrical characterization of a 2D quantum device, meaning that measurements are carried out to extract both the output and transfer characteristics and the intrinsic properties of the material such as MOSFET mobility, resistivity and differential conductivity. Therefore one needs to carefully specify the techniques and methods that are intended to be used for that purpose. In fact, experimental measurements are quite different from ideality. To begin with, we cannot directly measure the electric field or current density inside a sample, but we must indirectly derive them from measured current, geometry and voltage drops between electrical contacts. The initial choice made in this research is to adopt a Hall-bar-shaped set of devices. As presented in *Fig.2.4b*, the Hall Bar is not the only 2D FET that allows to estimate electrical properties of a 2D material; however, it is certainly one of the geometries that better helps researchers with the characterization of carrier mobility and densities. Moreover it is a geometry that allows for a simple determination of the contact

resistance, which is one of the parameters of highest interest in this research.

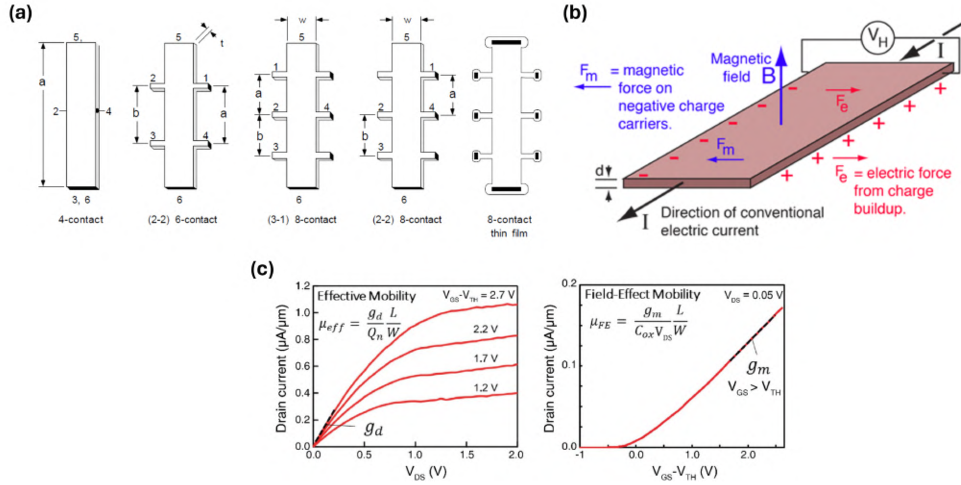

*Figure 2.5:* a) Hall bar geometries. t is the device thickness. In the 8-contacts, only the marked contacts are needed to perform measurements, the remaining two are built just for symmetry.[22] b)Classic Hall effect: the magnetic field perpendicular to the surface produces transversal Lorentz forces that induce the transversal voltage drop called Hall voltage.[23] c) MOSFET transfer characteristic highlighting effective mobility calculation and MOSFET output characteristic highlighting field-effect mobility calculation.

One relevant feature that shall be considered before realizing the device is the geometry of the Hall bar. As displayed in *Fig.2.5a*, the sample can be built with 4, 6 or even 8 contacts. Usually opposite contacts (2 and 4 in the figure) will be the terminals of the Hall voltage, while adjacent contacts (1 and 2 in the figure) will be exploited to measure current and infer electric field. The geometrical asset of this device is optimal to measure currents and voltages involved in the *classical Hall effect*. This electrodynamical phenomenon occurs whenever a magnetic field is perpendicular to the surface of a device subject to a longitudinal voltage drop, thus a longitudinal current runs through it. The magnetic field interacts with the moving carriers producing a transversal Lorentz force, as shown in *Fig.2.5b*, thus inducing the transversal voltage known as Hall voltage. Therefore, Hall bar geometries are particularly useful to characterize 2D devices because both dimensions can be fully analyzed by a discrete set of longitudinal and transverse voltages and currents. Indeed, two forms of mobility are typically extracted from Hall devices: the Hall mobility and the MOSFET mobility. Since Hall measurements, typically derived from the classical Hall effect and the application of an external magnetic field, can be conducted in A*STAR laboratories, we initially considered this approach. However, we encountered challenges in fabricating the Hall bar devices. Specifically, the Hall device using a CVD monolayer did not function, as carefully explained in CHAPTER5, and fabricating a Hall device with exfoliated multilayers requires electron beam lithography (EBL), which is currently unavailable due to heavy usage. As a result, the present research will primarily focus on the characterization of MOSFET mobility.

### 2.2.1 MOSFET mobility

The longitudinal mobility, or MOSFET mobility, can be calculated from the measured transistor characteristics. As precisely explained by Mitta et al.[16], one can distinguish between two different types of MOSFET mobilities.

**1.** The **effective mobility**, $\mu_{eff}$, is calculated by the drain conductance of a MOSFET biased in linear regime. One calculates the longitudinal current, making use of the source-drain ($ds$) parameters, as

$$I_{ds} = \frac{W}{L}\mu_{eff}Q_nV_{ds}$$

where $W$ and $L$ are the width and length of the channel, namely the dimensions of the Hall bar. $Q_n$, instead, is the sheet charge density of the channel and is calculated as the standard charge at the plate of a capacitor by $Q_n = C_{ox}(V_{gs} - V_{th})$ . $C_{ox}$ is the capacitance per unit area of the gate dielectric, while $(V_{gs} - V_{th})$ is the gate voltage subtracted by the threshold voltage. Therefore, by simple formula inversion, the effective carrier mobility for an ideal device is

$$\mu_{eff} = \frac{g_d}{Q_n}\frac{L}{W}$$

where the ratio between current and voltage, being both slowly-varying quantities, must be expressed in terms of a derivative. $g_d$ is then the drain conductance of the device and it is calculated as

$$g_d = \frac{\partial I_{ds}}{\partial V_{ds}}|_{constant V_{gs}}$$

Therefore, by recalling the expression of $Q_n$, one can write the long expression for the effective mobility:

$$\mu_{eff} = \frac{\frac{\partial I_{ds}}{\partial V_{ds}}|_{constant V_{gs}}}{C_{ox}(V_{gs}-V_{th})}\frac{L}{W}$$

**2.** The **field-effect mobility**, $\mu_{fe}$ , is calculated similarly to the effective mobility and is function of the device transcharacteristics, where $V_{gs}$ is no longer a constant parameter, but a slowly varying quantity and plays the role of $V_{ds}$ in the previous calculation.

$$\mu_{fe} = \frac{g_m}{C_{ox}V_{ds}}\frac{L}{W}$$

where $g_m$ is the device transconductance and its calculated as

$$g_m = \frac{\partial I_{ds}}{\partial(V_{gs}-V_{th})}|_{constant V_{ds}}$$

but since $\delta(V_{gs} - V_{th}) = \delta V_{gs}$,

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}|_{constant V_{ds}}$$

In conclusion, the two derived mobilities can be interpreted as the same physical quantity calculated from two different graphs, as *Fig.2.5c* correctly explains. The effective mobility is proportional to the slope of the output curve ($g_d$) at fixed $V_{gs}$, while the field-effect mobility is proportional to the slope of the transfer curve ($g_m$) at fixed $V_{ds}$. While the field-effect mobility is specific to the behavior of FETs, being the gate voltage considered as a proper variable, the effective mobility is a more general measure that applies to various types of semiconductor devices and it is thus the key quantity of interest of this thesis.

## 2.3 Transport limitations

As specified in previous sections, 2D TMDCs are promising candidates for post-Si electronics. However, the fabrication of 2D TMDC-based devices is still limited by a high contact resistance[24]. Indeed, contact resistance in TMDCs may severely limit the current flow and complicate the understanding of the device. Many experiments and most device electrical characterizations reported values of contact resistance of the order of hundreds of kΩ [25][24], while standard silicon contact resistance were of the order of hundreds of Ω[26]. Before proposing some techniques to reduce it, one first needs to understand the physics behind such a phenomenon.

Metal-semiconductor junctions are an example of what is commonly known as Schottky contact. The simplest device presenting such a structure is the well-known Schottky diode, as shown in *Fig.2.6a*. It behaves similarly to classical p-n junctions with some smaller threshold voltage and much larger rectifying behavior. The latter refers to the junction capability of directing the current flow in one way only; namely, in reverse bias ($V < 0$) the current will abruptly decrease to tiny values before breakdown. The reverse current will then be caused solely by thermionic emission, the phenomenon allowing electrons escape due to non-null temperatures[27]. The reverse current density of a Schottky junction will then be completely described by a Maxwell-Boltzmann distribution because the number of fugitive electrons is actually small:

$$j_s = AT^2 e^{-\frac{e\Phi_0}{k_b T}}$$

where $T$ is the temperature, $e$ the elemental charge ($1.602 \times 10^{-19}$ C), $\Phi_0$ the workfunction and $k_b$ the Boltzmann constant ($1.381 \times 10^{-23}\,\mathrm{J\,K^{-1}}$). Finally $A$ is typically between $\frac{1}{4}A_{th}$ and $\frac{1}{2}A_{th}$, where $A_{th}$ is a fixed constant given by

$$A_{th} = 4\pi \frac{m_e e k_b}{h}$$

where $m_e$ is the mass of the electron ($9.109 \times 10^{-31}$ kg) and $h$ the Planck constant ($6.626 \times 10^{-34}$ J s).

The forward diode current is then proportional to the reverse current and exponentially dependent on the applied voltage:

$$I = I_s(exp(\frac{eV}{k_b T}) - 1)$$

Although Wong et al.[27] demonstrated that this model does not fit well with experimental I-V curves, it is still enough to understand the junction behavior and compare it with standard ohmic contacts, characterized, instead, by the linear behavior depicted in *Fig.2.6b*. In order to exploit the best of the functionalities of the junction, one would need the characteristics to be the most ohmic possible; "ohmicity" indeed ensures a correct device functionality in reverse bias and does not present the rectifying behavior typical of Schottky junctions; moreover, it allows to minimize energy losses by offering an efficient signal transmission and controlling the current flux.

To better understand the behavior of a Schottky junction, the band-diagram representation could be useful. As shown in *Fig.2.7*, metals and

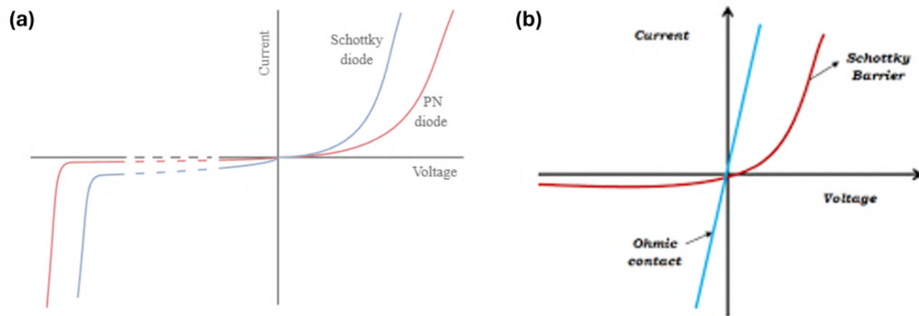


*Figure 2.6:* a) Schottky diode and PN diode comparison.[28] Schottky characteristic presents lower threshold voltage and faster current response to voltage. b) Ohmic and Schottky characteristics comparison. The linear behavior is characteristic of the ohmic contact, which does not present the rectifying behavior typical of Schottky junction.

semiconductors show two different band landscapes: in the first category, indeed, electrons are free to move because the Fermi level lies above the bottom of the conduction band; in the second group, instead, the Fermi level is found in the middle of the energy gap separating valence and conduction band. In order to promote electrical conduction, electrons must "jump" from the top of the valence band to the bottom of the conduction band, which presents available empty states.

At equilibrium, the Fermi levels of both metal and p/n-type semiconductor align, causing the bending of semiconductor valence and conduction bands. The vacuum levels ($E_0$) must indeed preserve continuity and relative distance with other band levels; in fact, they refer to the energy of an electron at rest in a vacuum, just outside the material, where it is no longer influenced by the atomic forces of the material. It is the energy required to completely remove an electron from the solid into free space. An alternative perspective on this matter is that electrons present in the conduction band of the semiconductor can transit to the vacant energy states located above the Fermi level of the metal. This transition results in a positive charge accumulation on the semiconductor side and, due to the surplus electrons, a negative charge on the metal side, thereby creating a contact potential. When a junction is established between a metal and a semiconductor, the low charge density on the semiconductor side causes electrons to be extracted not only from the surface but also from a certain depth within the semiconductor. Consequently, this process leads to the development of a depletion region within the semiconductor. As the depletion region penetrates to a specific depth in the semiconductor, it induces a bending of the energy bands on the semiconductor side.
This phenomenon causes the formation of an energetic barrier at the interface: the so-called Schottky barrier. The latter prevents holes from moving rightwards in p-type devices junctions and electrons from moving leftwards in n-type devices junctions. *Schottky barrier height* (SBH) is precisely the source of high contact resistivity at the semiconductor-metal interface and one would be interested in its reduction as a way to enhance devices performance. In order to reduce SBH, one first needs to understand which are the factors

that mostly influence it. Fortunately, these can be deduced from the band-diagram itself by simple visual inspection. *Fig.2.7b* shows that electrons SBH is simply given by: $\Phi_{Bn} = \Phi_M - \chi$ with $\Phi_M$ being the metal workfunction and $\chi$ the electron affinity, namely the energy difference between the vacuum level and the conduction band minimum. On the other hand, holes SBH appearing in p-type semiconductors depicted in *Fig.2.7a* can be calculated by means of the energy gap: $\Phi_{Bp} = E_{gap} - \Phi_{Bn}$. Both formulas show clearly the dependence of the SBH on the metal workfunction. It is of immediate understanding that SBH could be reduced by coupling n-type semiconductors with low-workfunction metals (such as Ti, In or Cr) and by coupling p-type semiconductors with high-workfunction metals (such as Pd, Sc or Bi)[29].

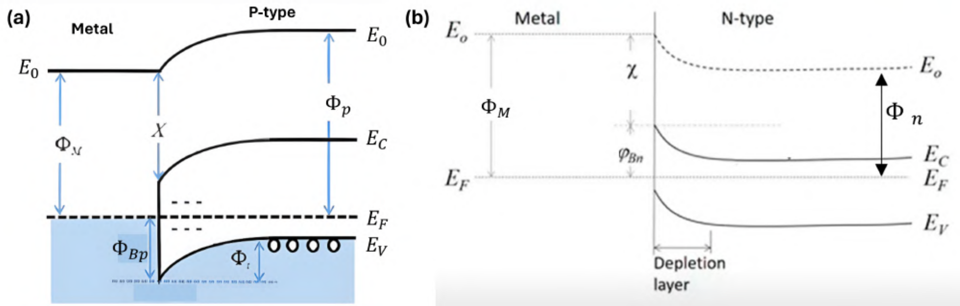


*Figure 2.7:* a) Band-diagram of p-type semiconductor-metal junction at equilibrium.[30] Bands bend to guarantee the continuity of vacuum level, thus creating an energy barrier that prevents holes from flowing smoothly from the metal to the semiconductor in direct bias. b) Band-diagram of n-type semiconductor-metal junction. Bands create an energy barrier that prevents electrons from flowing smoothly from the metal to the semiconductor in reverse bias.

Metal-semiconductor matching, or *Schottky-Mott rule*, should in principle be enough to guarantee a sensible reduction of SBH; unfortunately, most experiments show that the metal workfunction is almost ineffective on the contact resistance of the junction, meaning that some other factor must be playing an important role in the determination of the phenomenon.

Such a factor is called *Fermi level pinning* (FLP). It is a situation where the band bending in a semiconductor contacting a metal is essentially independent of the metal itself, even for large workfunction variations.[31] Despite the true origins of the phenomenon remain partially unknown, it is believed that it may originate from the parasitic dangling bonds on the surface of the TMDC layer. This means that they would deteriorate the interfacial band alignment and form high and wide Schottky barriers because of the formation of interfacial dipoles.[32] In addition, it has been demonstrated that FLP originates also from a distribution of mid-gap states at the metal-semiconductor interface, created by the presence of defects[33], as shown in *Fig.2.8a*. These MIGS (Metal-Induced Interstitial States) will weaken the TMDC layer through metal-chalcogen interactions, thereby pinning the Fermi level. *Fig.2.8b* shows the variation of the density of states (DOS) around the

semiconductor bandgap for different samples of $MoS_2$ with different percentages of surface S-vacancies. One can easily observe that for a null concentration of defects the bandgap appears well-defined and clean; as the concentration increases, though, new parasitic states begin to emerge starting from the bottom of the conduction band and moving towards the Fermi level as the concentration increases. These are the new findings of the Institute of Materials, Research and Engineering (IMRE) in Singapore, published in the paper of Bussolotti et al. in 2021[34], which could pave the way for a new understanding of the complex phenomenon of FLP.

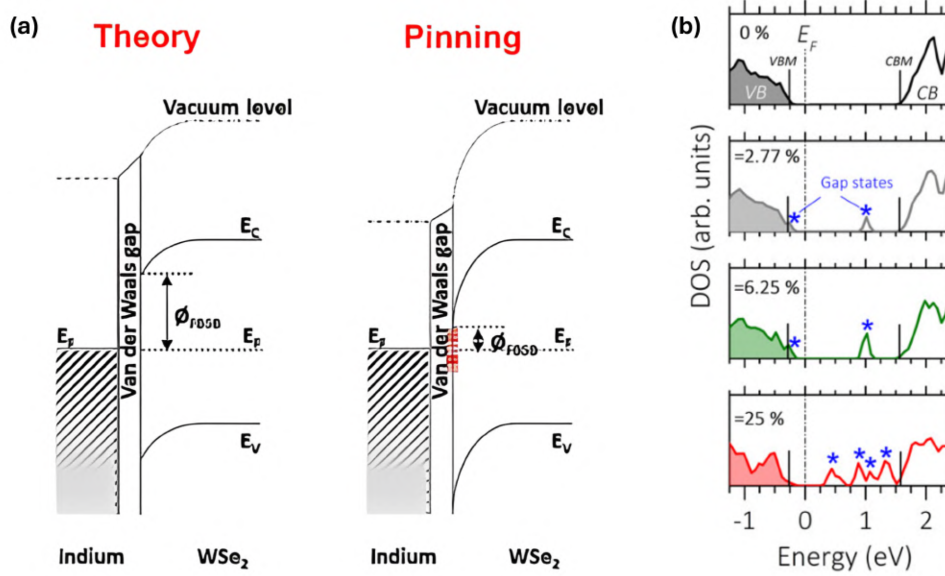


*Figure 2.8:* a) Formation of MIGS at the metal-semiconductor interface and influence on the general band-diagram[33]: the SBH increases even more due to the presence of MIGS. b) Behavior of the density of states as a function of energy as impurity states percentage is varied. One can appreciate defect states forming starting from the conduction band downwards. This phenomenon is thus responsible for pinning the Fermi level at different positions, depending on the impurities density.[34]

The whole phenomenon can be also described by a numerical factor called Pinning factor (S) ranging from 0 (maximum defect concentration) to 1 (Schottky-Mott limit).

$$S = \frac{\epsilon_i}{\epsilon_i + e^2 D_{it} \delta}$$

with $\epsilon_i$ the material electrical permittivity, $D_{it}$ the defects surface density and $\delta$ the thickness of the interlayer. S will then modify the formula for the evaluation of the SBH:

$$\Phi_B = S(\Phi_M - \Phi_{cnl}) + (\Phi_{cnl} - \chi)$$

where $\Phi_{cnl}$ is the charge intermediate performance level under a relative vacuum level and it is dependent on the electron affinity, $\chi$. Ni et al.[35] report that the usual pinning factor of defect area is observed to be about $30\% - 40\%$.

As one can appreciate from the formula, the pinning factor presents a clear dependence on the concentration of defects at the interface. Therefore, it is important to know the origins of such defects. Yan Wang and Manish Chhowalla[33] attribute the origins of interfacial defect formation to three different phenomena: chemical reactions at the interface caused by semiconductor coupling with reactive metals (such as Ti), chalcogen vacancies that introduce defect states located 0.04 eV - 0.05 eV below the minimum of the conduction band and finally defects by metal deposition, which could damage the TMDC surface if pumped at high power.

## 2.4 Possible solutions

Several are the papers dealing with reduction of SBH and presenting solutions to fight FLP. Theoretically speaking, indeed, the sole Schottky-Mott rule should be enough to guarantee a sensible interface transport by matching metal work functions according to the p or n-type behavior of the TMDC used. As shown in the previous section, however, the emergence of intergap intrusive state causes the phenomenon of FLP and thus nullifies all the efforts of the Schottky-Mott rule. Wang and Chhowalla[33], in accordance with other papers [36][37], state that one possible solution to prevent FLP effect would be the realization of ultra-clean contacts by taking small but important precautions, like avoiding reactive materials (like Ti, Cr, Ir and Sc), using metals with low vaporization temperatures (like In and Bi) and working at very low pressures ($< 10^{-7}$ torr). The latters would prevent the formation of defects by metal deposition by reducing the kinetic energy of evaporated metal atoms; the same goal could also be achieved by introducing inert gas in the evaporation chamber or by cooling the sample holder, and thus the substrate, down to the temperature of liquid nitrogen.[37]

Nowakowski et al.[38], in accordance with many others[39][40][41], investigate modifications of SBH across Schottky junctions by the introduction of buffer layers. The insertion of ultrathin layers of oxide or semimetals in the metal-semiconductor junction is indeed a candidate solution to the problem of FLP. The authors study the dependence of transport on the chosen graphene and $MoSe_2$ thicknesses and demonstrate that both materials improve the device output characteristics, even removing the rectifying behavior in the case of graphene. As elucidated by Freedy et al.[6], an interfacial metal oxide blocks the penetration of the metal wavefunction into the semiconductor, thus limiting their interactions and defects creations.

Finally, a third SBH reduction technique must be mentioned. It consists of the surface oxidation of the TMDC layer. As deeply analyzed by Cheng et al.[43] and depicted in *Fig.2.9d*, UV-$O_3$ and $O_2$-plasma are capable of oxidizing the upper layer of TMDC. Specifically, the first promotes covalent bonds between S and O, without breaking Mo-S or W-S bonds, thus producing the new species $MoS_xO_y$, while the second forms $MoO_3$/$WO_3$ by direct substitution of S with O. In addition, Santoch et al.[44] mentioned the possibility of oxygen to fill S-vacancies; O substitutional impurities would be indeed energetically favorable and together with adsorbed oxygen (S-O bonds) do not alter the electronic properties if their concentration is kept below 8%.

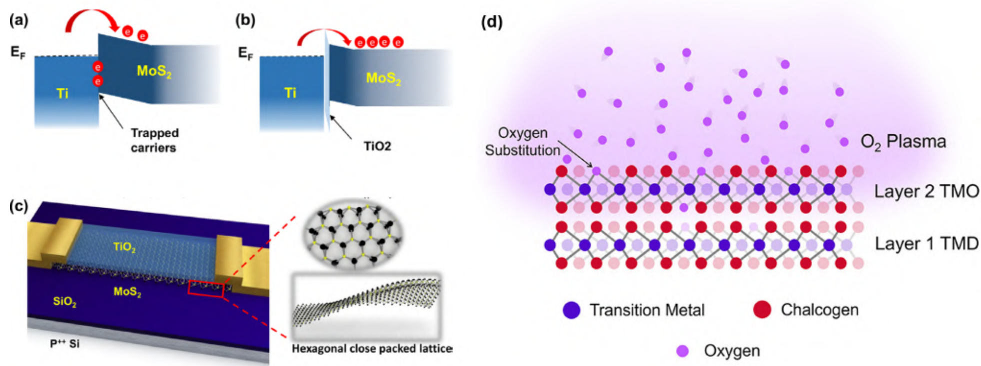


*Figure 2.9:* a)b)Band-diagram of a Schottky junction before and after the insertion of an ultrathin oxide layer[42]: the oxide prevents the formation of trapped states and therefore unpins the Fermi level, decreasing the SBH. c) 3D structure of $MoS_2$ FET with the insertion of a ultrathin oxide layer d) Oxygenation of surface layer of TMDC by oxygen plasma highlighting the substitution of sulfur by oxygen atoms.[21]

The main advantage laying underneath such a technique is the shrinkage of TMDC bandgap due to O absorbance. Engineered $MoO_x$ superficial layers would therefore show a more metallic character, enhancing junction electronic transport. The devices fabricated by Oberoi et al.[21] prove experimentally this improvement; the authors fabricated different sets of devices which had been exposed to $O_2$-plasma for different time intervals with even different metal contacts (Ni, Pt, Pd). The result is a global reduction in contact resistance as the oxidation time increases. However, the modulus of the contact resistance never decreases below some threshold value, proving the self-limiting power of the oxidation process. After 15s of plasma exposure, indeed, the oxide concentration does not change anymore because of the formation of a diffusion barrier created by the oxidized layer.

Despite device theory having studied different solutions and approaches to the problem of SBH reduction, a clean, safe and perfectly replicable fabrication process is still missing. In the next chapter one can appreciate the description of the standard steps of a microscopic 3D device fabrication aimed at its electrical characterization, with particular emphasis on the quality of the metal-semiconductor contacts.

# Chapter 3

# Fabrication of a $WS_2$ field effect transistor

The first part of the project is aimed at the fabrication of $WS_2$-based FETs by photolithography on $SiO_2$ substrate. A fully-detailed description of each fabrication step is provided by analyzing both the physics and the experimental challenges behind them. The chosen material for the FETs channels is intrinsic $WS_2$ obtained by mechanical exfoliation. Thanks to its high number of layers, each flake of $WS_2$ shows high resistance to mechanical manipulations and chemical treatment. While the bulk-like active device regions may not display the unique electrical characteristics of monolayers, they would certainly show some electrical signal and allow a complete physical characterization.

To this purpose, $SiO_2$ is chosen to be the sample substrate. Its excellent performances are reported in scientific literature, where its dielectric and thermal properties are widely analyzed[45]. Moreover, being grown on highly doped silicon (p++) , $SiO_2$ can be fully employed as a bottom gate, thus ensuring a uniform semiconductor exposure to gate voltage. The choice of exfoliated flakes and $SiO_2$ as substrate, however, forces the fabrication line to shift towards the complex technique of transferring. A fully detailed recipe to transfer $WS_2$ flakes to $SiO_2$ is described in Sec.3.7. Finally, bottom contacts are chosen in place of commonly used top contacts. As demonstrated by several authors, bottom contacts reduce the damage caused by chemicals and improve lift-off drastically[46]. To do so, pre-etched patterns must be printed on the substrate before undergoing metal deposition in order to widen the gap between gold-to-keep and gold-to-lift-off. A smooth and successful lift-off ensures the correct transfer of flakes onto the printed gold pattern. The latter is chosen to be a simple source-drain transistor. However, due to lab availability, a photolithographic mask with Hall bar patterns is adopted; what are normally considered side contacts will now be used as terminals of the new device.

In conclusion, these choices address issues related to substrate compatibility, flake integrity, and chemical damage, ultimately paving the way for a

reliable and efficient device fabrication. The entire process is illustrated in *Fig.3.1*, while the next sections will be devoted to the description of the crucial fabrication steps. The whole fabrication process is realized practically in cleanrooms. The reader can delve into cleanroom specifics and classification by reading A.

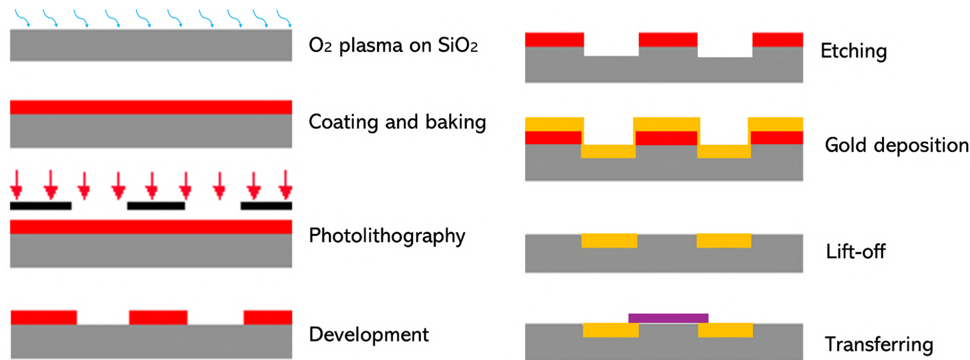


*Figure 3.1:* Schematics of the fabrication process. In gray $SiO_2$, in red photoresist, in yellow gold and in purple $WS_2$ flake.

## 3.1 Spin-coating and baking

Despite the outline of the entire process may seem similar to the fabrication of devices on standard substrates, the choice of $SiO_2$ poses new challenges that must be addressed with specific techniques. The substrate alone, indeed, does not allow for a smooth and uniform deposition of photoresist by spin coating. Indeed, materials like $SiO_2$ (in the form of quartz, glass, or silicon with a native oxide layer) and most base metals develop polar OH bonds on their surfaces after prolonged exposure to atmospheric humidity. This renders the substrate hydrophilic, leading to poor affinity for the non-polar or low-polarity resin molecules in the photoresist[47]. To make the substrate surface hydrophobic and thus more receptive to photoresist, non-polar molecules from adhesion promoters can be chemically bonded to the surface or, alternatively, a sufficient exposure of $O_2$-plasma will remove OH contaminants from the substrate surface. For this reason the diced $SiO_2$ samples must undergo a preliminary exposure to $O_2$ plasma at 50 W power, 50 sccm (standard cubic centimeter per minute) for 20 s.

The first step of a microchip fabrication consists of the deposition of a thin layer of a liquid polymer called photoresist (PR). PR is a mixture of three different substances: a lattice for 10% of the volume, a solvent for 85% and a photostarter or initiator, for the remaining 5%. The first can be an epoxy polymer with negative pH or a novolac resin with positive pH, but the latter is usually unable to react further without adding cross-link agents. The second serves the purpose of keeping the photoresist liquid influencing its viscosity; thus, it will determine some important parameters of the spin-coating such as the thickness and spreading velocity. The third, instead, is responsible for the tunable solubility of the PR: molecules that absorb UV-photons upon irradiation with light will form reactive species which will initiate consecutive

reactions and turn into a macroscopically more (or less) soluble polymer; solubility enhancement defines positive PR, while solubility diminution defines negative PR. The difference between the two is illustrated in *Fig.3.2d*, but some words may be spent to describe them more carefully. Positive PR's usually offer greater resolution because the solubility difference between exposed and non-exposed areas is of $10^2$, moreover they present high etching-resistance and greater temperature stability with respect to the negative PR. The latter, as described previously, are difficult to solve after irradiation because the polymers create higher cross-link bonds, thus reducing the solubility of the solution. Contrary to positive polymers, this last category does not offer a good resolution (usually around 2 $\mu$m) because, being at high molecular weight, it tends to swell. Independently of the kind of PR used, though, the material must have some distinctive properties that makes it suitable for its use: high sensibility to light, high contrast (no gradient between light and dark), transparency and high critical temperature. This last feature, in particular, is important to prevent PR from turning into glass or rubber while heated up.

Tunable solubility is what makes the PR so special and suitable for the photolithography step, which will involve the projection of UV light on selected areas of the wafer. The PR on these areas will change its solubility and be easily removed by a development solution. According to the typology of PR used, one must choose a different chemical to perform developing: organic compounds like benzene or toluene must be chosen for negative PR's, while water-based substances are preferred for positive PR's. The choice is in fact driven by the typology of solvent used for the two PR's: while negative uses mostly organic solvents, positive PR's are made of hydrophilic compounds like NaOH or KOH. The PR chosen for this experiment is a positive photoresist called $S1811$.

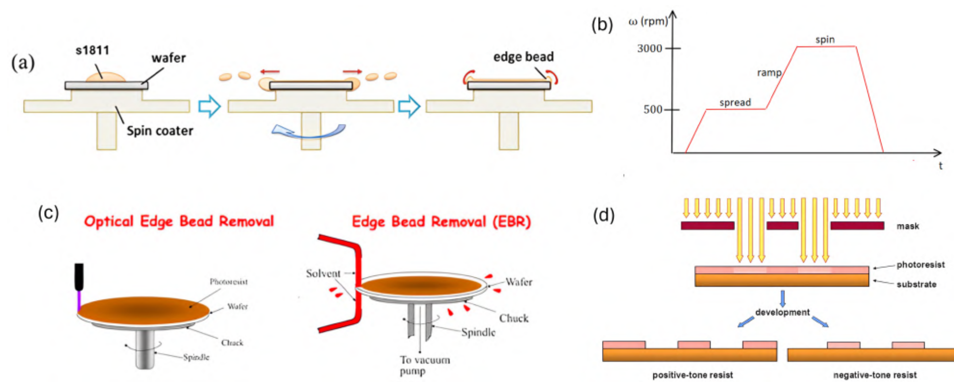


*Figure 3.2:* a)Schematics of the spin coating process: a drop of PR is deposited on the wafer placed over the spin coater, then the motor starts spinning and the PR distributes uniformly on the device; eventually some edge beads may form.[48] b)Time prospect of the spin velocity of the motor: after a first stage of PR spreading, the spin coater increases its power to bring rotation frequency to 3000 rpm in ramp and spin phases when the PR is distributed on the sample. c) Principal solution to the edge beads problem. The first image shows the use of optical lasers to remove excess PR accumulated on the edges, while the second illustrates the use of chemical solvents.[49] d) Photolithography process with positive and negative PR: in the first case illuminated PR is removed by develop solution, while in the second case remains and the remaining is removed.

In order to uniformly spread the liquid PR on the wafer, one makes use of a spin-coating machine reported in *Fig.3.3a*. A central vacuum nozzle helps maintain the device balanced while the metal support starts spinning at high frequency. Driven by the centrifugal force, the few drops of PR that are manually deposited on the sample surface will then start to spread on the top layer and gradually flatten reaching the typical thickness of 1.1 $\mu$m - 1.3 $\mu$m at 3000 rpm for 60 s.

The spin-coating process could be then summarized into four main steps. The first is called deposition and consists in the delivery of an excess of the liquid polymer onto the substrate (usually 5 ml of PR are deposited manually with a pipette). Secondly, the spin motor activates and liquid flows radially at all locations under the centrifugal force: such a spin-up is divided into two phases, which consist in a spread time when the motor rotates slowly at 500 rpm and a ramp-up when the spinning velocity increases to 3000 rpm. The prospect of the spinning velocity as a function of time is shown in *Fig.3.2b*. The third step of the spin-coating process is called spin-off and is responsible for the creation of a uniform thick film which thins slowly down to an equilibrium thickness, thanks to PR squinting. Finally the liquid solidifies due to solvent evaporation.

One major inconvenience that may occur at the end of spin-coating procedure is the formation of edgebeads, as depicted in *Fig.3.2a*. Their formation is essentially due to dynamics of fluid flow and surface tension effects. Indeed, as the PR spreads out, the surface tension tries to minimize the surface area, but edges act as a barrier causing PR piling up. The amount of material accumulated mainly depends on the viscosity of the PR itself: the higher the viscosity the thicker the edgebeads, because the liquid will resist flowing back to the center and thus accumulate at the edges. Several techniques could be implemented to reduce edgebeads effects; the two most relevant ones make use of either chemicals or lasers and are illustrated in *Fig.3.2c*. Special solvents can be indeed applied to the edge of the wafer to remove the excess of PR, or alternatively, a laser cutter removes the edgebeads. On the other hand, one simple method to eliminate this effect would be the dilution of PR with some chemical additive preventing the accumulation of PR at the edges. Such chemicals could be surfactants[50], fluorinated compounds[51] or siloxane-based compounds.

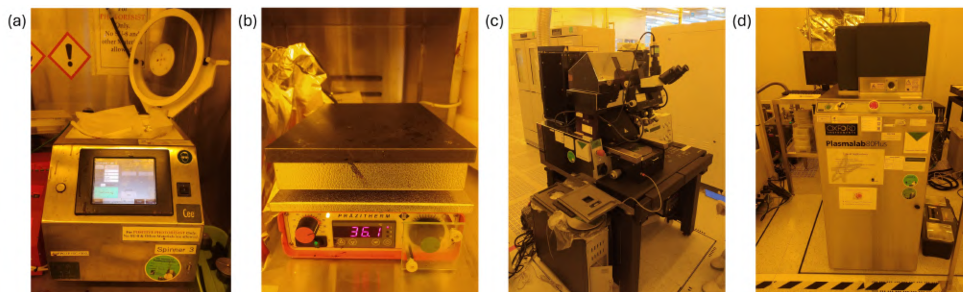


*Figure 3.3:* Pictures of a)spin-coating machine, b)hot plate, c)photolithography and d)reactive ion etching machines from A*STAR cleanroom.

At the end of spin coating the PR is however still partially liquid and one does not want to lose it while tilting the device. To harden it on the sample one makes use of a hot plate depicted in *Fig.3.3b*. The device rests there for 60 s at the temperature of 110°C. The sample is now well covered by a hardened PR, thus it is less susceptible to particle contamination and ready for the photolithography machine.

## 3.2 Photolithography: the mask alignment

Once the sample has been correctly covered by a layer of PR, it is ready to undergo photolithography, by use of the machine in *Fig.3.3c*. As the name itself suggests, photolithography is an engineering process that exploits UV light to draw specific patterns on the device. The sample is loaded on a metallic holder and automatically aligned under a quartz mask with the desired pattern. Thereafter a dark chamber is placed around the couple and UV light is projected through the mask for 7 seconds. Such light is produced by Hg-gas lamps having two peaks at 365 nm and 436 nm. Interestingly there are different methods of exposing PR according to the distance between mask and substrate. Contact mode places the mask at a distance of 0.1 $\mu$m - 1.0 $\mu$m from the sample, it offers a resolution close to the UV wavelength, but the risk of mask damage is quite high. Proximity mode, instead, has a worse resolution because it places the mask at a distance of 2.0 $\mu$m - 4.0 $\mu$m from the sample, but offers a low cost replica. Finally, projection mode places the mask far from the sample and exploits the use of lenses with small aberration to scan the entire device length. Especially in this last case, alignment is crucial: tighter overlay control means that circuit features can be packed closer together. The three photolithography methods are schematically represented in *Fig.3.4*.

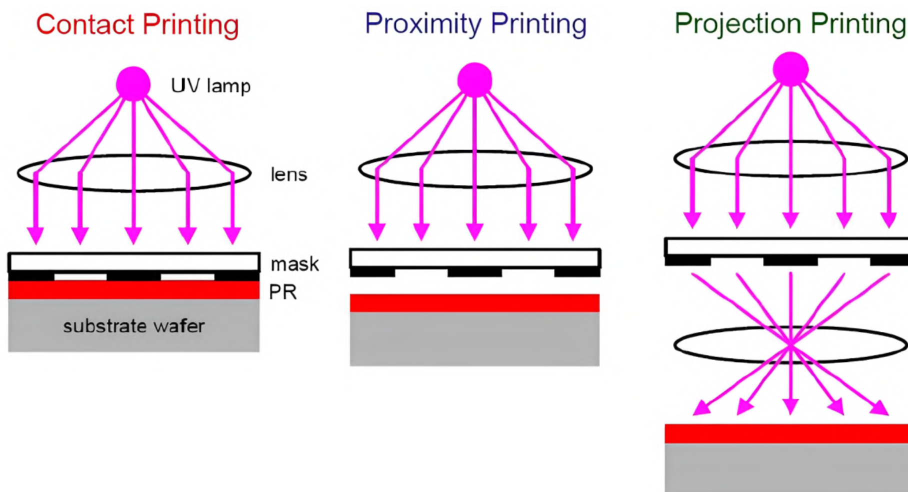


*Figure 3.4:* Three different photolithography methods: contact printing aligns mask and sample at a very narrow distance, proximity printing increases that distance, giving up on precision but preventing the device from damage. Finally, projection printing makes use of lenses to project UV light on the sample according to the mask patterns.

The distance between sample and mask plays a crucial role in the determination of the pattern resolution, which changes according to the value of Fresnel diffraction coefficient ($F$), as shown in *Fig.3.5.* The mask, indeed, can act as a diffraction grating and one can easily evaluate its Fresnel coefficient by taking into account few parameters like the size of aperture($w$), the distance of the wafer from the mask($X$) and the UV wavelength($\lambda$):

$$F = \frac{w^2}{X\lambda}$$

Fresnel coefficient, indeed, determines the kind of diffraction happening during photolithography. If the machine operates in proximity mode, the sample-mask distance is very low and $F$ turns out to be larger than one, meaning that the diffraction pattern looks pretty much like a window function, thus it is highly precise. Contrary to the so-called Fresnel diffraction, by operating in proximity mode the machine may reproduce imprecise patterns typical of the Fraunhofer diffraction, due to the combination of constructive and destructive interference phenomena.

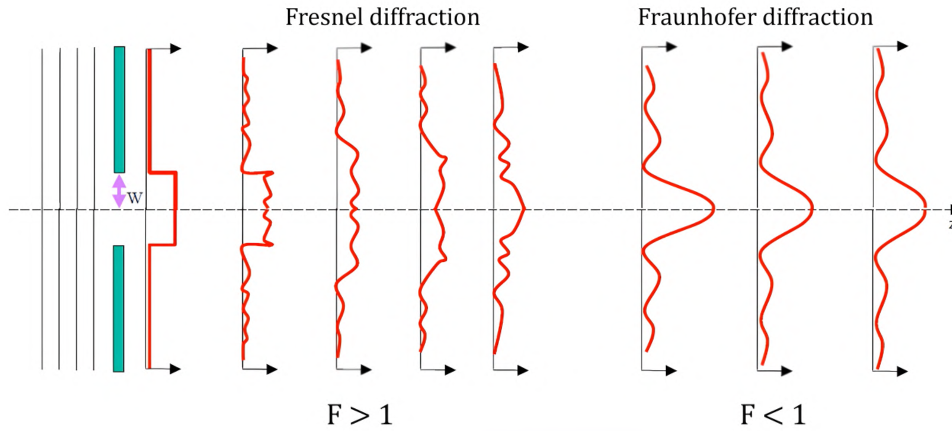


*Figure 3.5:* Diffraction patterns as a function of the sample-mask distance. When this distance is small with respect to the size of aperture $F > 1$ (Fresnel or near field diffraction). If this distance is much larger than the size aperture $F < 1$ (Fraunhofer of far field diffraction)[52].

In the present project, the first photolithographic method, the contact mode, is exploited, ensuring maximal precision and reducing alignment issues. Once the photolithography is correctly executed, the device is ready to be developed.

## 3.3 Development: a matter of seconds

As mentioned before, specific parts of the photoresist have been exposed to UV light and have therefore changed their solubility. It is time to remove them, keeping the non-exposed parts untouched. An aqueous alkaline solution named $MF319$ serves the purpose; it contains a water-soluble organic base free from metallic constituents that efficiently removes the PR with higher solubility (usually 100 times bigger than non-exposed PR). Despite the high difference in the solubility of the two sections of the PR, a prolonged exposure to the develop solution may result in the unwanted consumption of hard PR.

*Fig.3.6* shows the effect of different exposure time on a selected Hall bar pattern designed on buffer samples. To guarantee a better and smoother current flow, the developing time is set to 60 s. Once chosen the optimal exposure time, the device can undergo development and then be quickly soaked in deionized (DI) water to stop the development process and clean the device from any residual chemical.

*Figure 3.6:* Comparison between different developing times: (a)50 s, (b)60 s and (c)70 s. As time increases, one can appreciate higher curvature in the Hall bar geometries, meaning that the development solution has consumed the hard PR more. Darker areas in a),b) and grey areas in c) are substrates covered by photoresist, while the rest of the pictures show a nude substrate.

## 3.4 Reactive ion etching: digging into the substrate

In order to fabricate reliable and efficient bottom metal contacts, terminal patterns must not only be drawn on PR, as for the usual top-contact fabrication, but must be dug in the substrate as well. This will reduce the chances of lift-off issues and facilitate flake adhesion on the substrate. It is indeed clear that if metal contacts protrude from the surface for several nanometers, the flake deposited on both gold and $SiO_2$ will be forced to bend and could compromise a smooth electron flow. It is thus important to optimize etching so as to obtain an etching depth comparable to the thickness of the metal that will be deposited (approximately 30 nm). Reactive ion etching (RIE) is precisely the technique suitable to accomplish the task of removing part of the substrate. The exposure to highly energetic ion plasma is indeed capable of removing entire layers of material and dig a proper hole in the substrate.

On the other hand, one must consider the presence of spin coated PR onto the substrate. The resin will generally protect the substrate underneath from the corrosive action of the ejected gas. However, being sensitive to a prolonged exposure to ion plasma, it might burn down because of the high energy absorbed, thus compromising its solubility in acetone and ultimately harming the lift-off. Therefore, it is imperative to find a good compromise between power, flow rate and typology of gas used. Rueger et al.[101], supported by Alam[53], indicate the mixture of $CHF_3$ and Ar as the best gas cocktail to achieve this objective; flow rates are fixed to 15 sccm and 35 sccm, respectively. Nevertheless, 30 nm depth requires a prolonged PR exposure to these gases and this could still damage the resin permanently. In order to prevent PR from burning, the total etching time is split into smaller blocks with a break in between to let the sample cool down and lose some superficial energy. The optimal etching recipe is then found to be made of 6 repetitions of exposure to 80 W power for 30 s each. This procedure is done by the

reactive ion etching machine depicted in *Fig.3.3d*. It consists in a chamber where the device is carefully placed and brought to infinitesimal pressures (approximately $10^{-7}$ torr). Once all the etching cycles are over, the device looks like the one pictured in *Fig.3.7*. Air is then pumped into the chamber and the device is ready to undergo metal deposition.

*Figure 3.7:* Optical microscope image of the etched profile. Despite being only a few tens of nanometers, the Hall bar pattern etched by $CHF_3$ and Ar gas is perfectly visible and clearly stands out from the PR coated substrate.

## 3.5 Metal deposition: the physical vapor deposition

The next step of the fabrication of a FET consists in the creation of the metal contacts to properly measure currents and voltages. Since metal atoms will uniformly cover the whole sample, the presence of PR patterns printed by photolithography is essential to lift-off the unwanted metal from the substrate.

Metal deposition is performed into the so-called "glove-machine". It consists of the chamber where to realize metal physical vapor deposition (PVD), which is placed under Ar-atmosphere to prevent chemical reactions with the ions, therefore the operator must handle metal, samples and any equipment by wearing special gloves, as depicted in *Fig.3.8a*. PVD, indeed, does not involve chemical reactions, but uses only the evaporation of a metal in high vacuum. To bring the pressure to the desired values (usually below $10^{-8}$ torr), one may wait up to 10/15 h after the sample loading. Once such pressure is reached, an electron gun, consisting in a heated filament, accelerates its electrons with a voltage of 5 kV - 10 kV on the chosen metal (gold in our case). Electrons lose their energy mostly as heat, causing the evaporation of gold, which will then deposit uniformly on the sample, as shown in *Fig.3.8b*. Metal contacts are deposited with a chosen thickness of 30 nm and the device is ready to undergo lift-off.

## 3.6 Lift-off: removing unwanted gold

One of the most critical steps of the fabrication is really lift-off. Indeed, portions of gold contacts may detach from their printed channels, some others could remain joining different terminals and even more overlap on themselves. To further reduce the likelihood of this occurring, gold is not the only metal

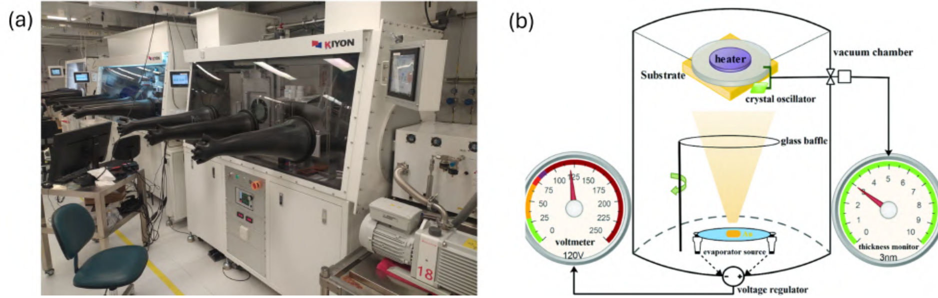


*Figure 3.8:* a)Glove machine in A*STAR cleanroom. b) Sketch of the PVD machine[54]: gold is evaporated from the evaporator source by means of a voltage source and is directed towards the sample kept fixed on a holder. Thickness is constantly monitored.

deposited on the etched patterns. A thin layer of chromium is specifically deposited before gold, right onto $SiO_2$, to increment adhesion to the substrate. 2 nm of chromium are quite enough to ensure adhesion of the remaining 28 nm of gold and despite its thermal voltage being higher, it does not damage the spin coated PR substantially.

It is the moment to lift the unwanted metal off the surface. After several trials the optimal procedure is found to be made of two main steps:

**1.** Overnight rest in a solution of acetone and 1165*remover* at the temperature of 50°C. The used remover is widely used in the semiconductor industry, particularly for positive photoresists. It is an aqueous-based solution, typically composed of tetramethylammonium hydroxide (TMAH), and is used to selectively dissolve the exposed areas of photoresist after UV exposure in photolithography processes, acting similarly to acetone.

**2.** Ultrasonication for 5 min. Ultrasonication is a process that uses ultrasonic sound waves (typically with frequencies above 20 kHz to agitate particles in a liquid medium. This technique is widely used in various applications, including cleaning and enhancing chemical reactions. It serves perfectly the purpose of removing residual unwanted metal from the surface of the device without harming the metal in the etched contacts, that is well ensured to $SiO_2$ by chromium adhesion power.

The result of this efficient technique is a clean set of metal contacts (see *Fig.3.9*) that are ready to host $WS_2$ flakes.

*Figure 3.9:* Picture of the patterned chromium-gold contacts after lift-off. The optimized recipe succeeded in obtaining a clean set of devices.

## 3.7 Transferring technique

The critical step of the whole fabrication process is certainly transferring. The transfer technique typically refers to the process of transferring thin films, nanostructures, or other materials from a generic substrate onto a targeted substrate, $SiO_2$ in this case. This is common in fields like semiconductor fabrication, optoelectronics, and microelectromechanical systems. But presents a high number of challenges; therefore, it is still an object of interest of many researchers. Hereafter, a fully mechanized transfer technique will be described with the objective of transferring exfoliated $WS_2$ flakes to $SiO_2$.

Obtained by the renowned “scotch-tape method”[55], exfoliated $WS_2$ consists in microscopical flakes of few tens of mum in diameter scattered on $SiO_2$ substrate, as shown in *Fig.3.10a*. Being several hundreds of flakes attached to the same sample, the operator must first identify the largest ones and note their position down to allow an easier orientation later on. It is advisable not to choose isolated flakes, because the process would result in a complete failure in case the targeted flake is not correctly lifted off; on the other hand, neighboring flakes may still remain attached to the gluing tape and serve the purpose in place of the original one.
$WS_2$ flakes are suitable for a controlled and mechanized procedure, which exploits the use of a mechanical manipulator with an optical microscope *Fig.3.10b*. The machine allows the user to calibrate the force used and rightfully control both the lift-off and landing areas.

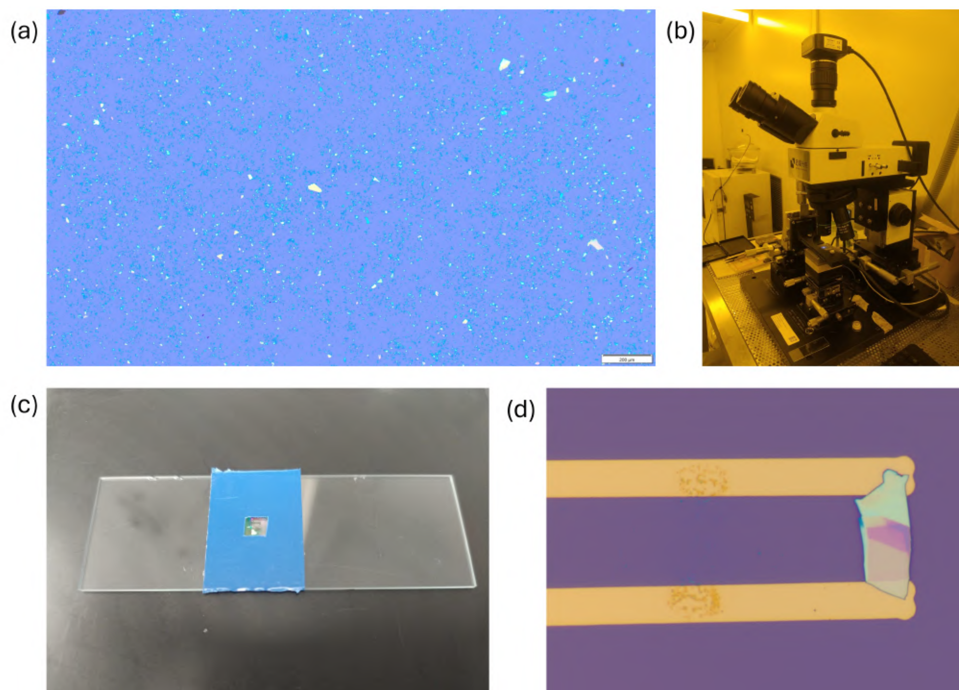


*Figure 3.10:* a) Optimal microscope image of $SiO_2$ substrate with exfoliated flakes. b) Mechanical manipulator with optical microscope from A*STAR cleanroom. c) PPC stamp prepared with 3M tape on a glass slide. d) Final device, cleaned from PPC.

The first step of such a technique is the preparation of the polypropylene carbonate (PPC) stamps. These composite objects, displayed in *Fig.3.10c*, are obtained through an elaborate procedure, which can be summarized in 5 points:

**1.** Prepare the PPC solution: dissolve a small crystal of PPC, 4% in ambient temperature chloroform. The solution must be conserved in a fridge at 4°C to inhibit chloroform fast evaporation.

**2.** Deposit a few drops of solution on a lab glass with a pipette and create a uniform and thin film of PPC by sliding two lab glasses on each other.

**3.** Cut a square hole on a 3M blue tape and use it to peel off the thin PPC film from the glass. The film will be fully attached to the tape and will also cover the square window in the middle.

**4.** Cut a small cube of poly-dimethylsiloxane (PDMS) and lodge it on a lab glass.

**5.** Deposit the 3M tape on the same glass slide so as to cover the PDMS with the PPC window.

The reason why PPC and PDMS are chosen as suitable materials for this process lies in their viscous and elastic properties. The first is an organic soft glue, whose adhesion with $WS_2$ overcomes vdW forces between the flake and the substrate, so that the semiconductor is easily lifted off $SiO_2$. The second, instead, is a highly flexible and elastic organic polymer used to soften the contact between flake and PPC.

Once the PPC stamps are ready, the transferring process may begin. The stamp is inserted inside the mechanical arm of the machine and fixed with some screws. The sample with flakes is positioned on a chuck under the optical microscope, which is essential to identify the targeted area. The PDMS-PPC sticky surface is then aligned with this area by maneuvering the mechanical arm and contact is made lowering the surface on the substrate area. In order to promote a sufficient adhesion the PDMS is pressed on the sample surface by calibrating a force knob. This initial step is carried out at ambient temperature to maximize PPC adhesion force. After carefully lifting the PPC stamp, one can appreciate the presence of the flakes onto it. The lift off is successful. At this point, the sample with the printed gold patterns is lodged on the chuck and the landing may begin. It is imperative to deposit the selected $WS_2$ flake straddling both contacts, therefore, a constant monitoring at the microscope is required. Once the flake is correctly standing on both metal stripes, the temperature of the chuck is raised to 80°C to induce PPC melting. After a couple of minutes the holder is removed and the device is ready to be cleaned from the melted PPC.

The process of cleaning is crucial to obtain a good quality of contacts with the measurement tips. For this reason, it has been carefully optimized. The sample is first left overnight soaked in chloroform at the temperature of 50°C. Then it is rinsed in isopropanol (IPA) and soaked in DI water to remove any organic residue. At this point the device will look like the one in *Fig.3.10d* and it is ready to undergo electrical measurements.

In conclusion, the fabrication of $WS_2$-based FETs by photolithography on $SiO_2$ substrate has been successfully achieved through a carefully optimized

process. This process addresses key challenges such as substrate compatibility, flake integrity, and chemical damage, ensuring reliable and efficient device fabrication. Moreover, the incorporation of bottom contacts, rather than top contacts, reduces damage caused by chemicals and improves lift-off, leading to enhanced device performance. Finally, the successful transfer of $WS_2$ flakes onto pre-etched gold patterns ensures proper contact formation and enables electrical characterization.

# Chapter 4

# Measurements and data analysis

## 4.1 Expected results

The first set of expectations concerns the electrical characterization of the fabricated devices. The classical measurements that can be done on a standard FET are synthesized in its output and transfer curves. They measure respectively the variation of the source-drain current ($I_{ds}$) as a function of the source-drain voltage ($V_{ds}$) and the change of Ids as a function of the gate voltage ($V_g$). The first takes $V_g$ as input parameter, while the second uses $V_{ds}$.

In most of the existing scientific literature $SiO_2$ is the preferred substrate for these microscopic devices. Not only has silicon oxide been better studied and analyzed in the past, but also offers quite a few additional advantages that make it the optimal insulating material on top of which a TMDC FET may be fabricated: $SiO_2$ is usually grown on top of a Si substrate, which can be highly doped ($p++$) and constitute a valid back-gate. The dielectric constant of $SiO_2$ is far smaller than sapphire's so it allows FET's channel to be opened by lower threshold voltages in case of back-gating and, finally, it offers better adhesion with the TMDC, thus reducing the probability to peel off the thin film or flake.

Moreover, the literature presents numerous results on both mono- and multi-layer $WS_2$. The performances of the two are slightly different but equally valuable. Usually there's a higher interest in monolayers because they manifest unique optical properties and a more pronounced bidimensional character, but for the purposes of this research multi-layers can play their role as well. For the sake of completeness, however, both mono- and multi-layer expected characteristics are thereafter illustrated.

Typical transfer curves of $WS_2$-based devices report source-drain currents of the order of tens of $\mu$A at fixed $V_{ds}$ of few volts. Specifically, multilayers

usually reach lower current but also higher threshold voltages, because of a normally lower carrier mobility. [56][57] However, their FET channels have dimensions of the order of 1 $\mu$m, so, being the devices of this research far larger, it is reasonable to expect a lower current due to a larger channel resistance. Typically, these FETs show an n-type behavior and are normally off, with a threshold voltage of tens of volts in absolute value. Both curves can be appreciated in *Fig.4.1a,b*.

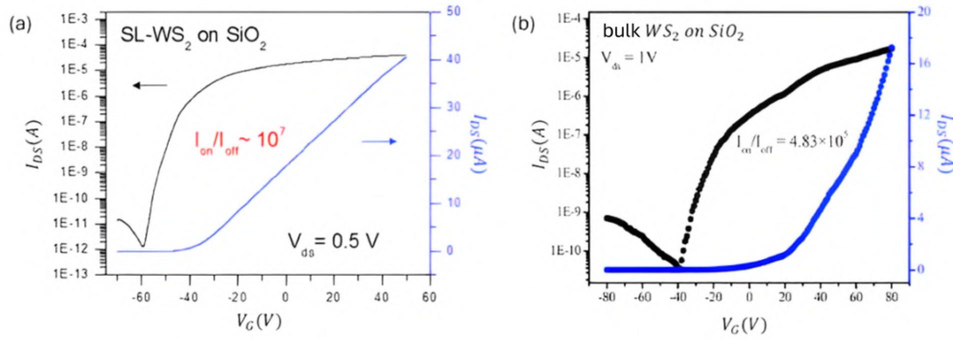


*Figure 4.1:* a) Transfer characteristic of $WS_2$ single layer (SL)[57]. b) Transfer characteristic of bulk-like $WS_2$[56]. In black the logarithmic curve.

The highest difference between mono- and multi-layers can be better appreciated by looking at the output characteristics. Monolayers, indeed, reach currents of the order of hundreds of $\mu$A, while multilayers remain around the tens of $\mu$A [56][58], as shown in *Fig.4.2a,b*. Also these curves are drawn from small devices and one expects worse results in this research. Concerning the shape of the characteristics, instead, it is reasonable to think that the solely-gold contacts will not exhibit ohmic behavior because of the workfunction mismatch (see Sec.2.3) and their output curves will bend towards the S-curve typical of Schottky junctions. However, in case higher workfunction metals (e.g. In) are adopted for the contacts, the shape of the curve may flex to a more linear behavior.

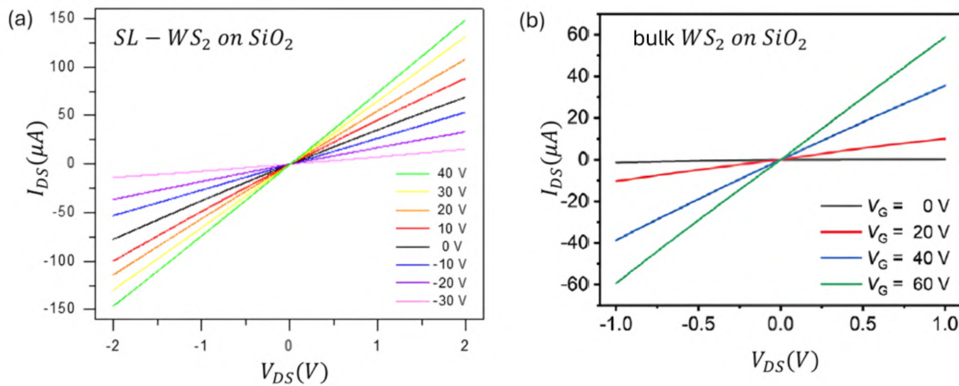


*Figure 4.2:* a) Output characteristic of single-layer $WS_2$[57]. b) Output characteristic of bulk-like $WS_2$[58]. Thanks to indium, the output curve has a prominent ohmic (linear) character.

When characterizing a FET based on new innovative materials like $WS_2$, it is important to provide enough information about its intrinsic properties, such as mobility. Some of the most acknowledged papers about TMDCs report the standard carrier mobility in $WS_2$ at room temperature to be around 20 $cm^2V^{-1}s^{-1}$, which could reach even higher values (28 $cm^2V^{-1}s^{-1}$) if the device is ambipolar[59][60]. Compared to other TMDC semiconductors such a performance may look poor: $MoS_2$, indeed, registers mobilities in the range of (10 $cm^2V^{-1}s^{-1}$ - 180 $cm^2V^{-1}s^{-1}$). In the present research, the same order of magnitude is expected for the carrier mobility because measurements are carried out at room temperature.

Additionally, it is crucial to assess the device's performance and compatibility with contemporary electronic applications. A key indicator of this is its on/off ratio. By on/off ratio one means the ratio of the highest and lowest values of $I_{ds}$ in the transfer curve. These two values are effectively associated with the on- and off-state of the device, which could be suitable for digital electronics applications if the on/off ratio is high enough. Typical on/off ratios range from $10^5$ to $10^8$ and it is reasonable to think that the fabricated devices could reach those values as well[60][61]. It is interesting to notice how the effective value of this parameter depends not only on the device, but also on the measurement machine, which could be capable of detecting even currents below $10^{-13}$ A, thus adding a couple of orders of magnitude to the parameters calculated with standard machines.

In conclusion, the electrical characterization of $WS_2$-based FETs highlights key performance metrics such as mobility, threshold voltage, and on/off ratio. Monolayers generally offer higher current and lower threshold voltages compared to multilayers, though larger device dimensions in this research may lead to increased resistance and reduced current. While carrier mobility is expected to align with prior studies, the on/off ratio remains crucial for digital applications, with values ranging from $10^5$ to $10^9$, depending on measurement sensitivity. These findings must be now compared with the actual measurement results obtained in the lab.

## 4.2 Results and discussion

The whole Chapter3 is devoted to the description of the main fabrication steps of FETs with $WS_2$ flakes on $SiO_2$ substrate. This section is devoted instead to the geometrical and electrical characterization of the fabricated devices. Time and resources available allowed the complete realization of 12 devices, among which only 9 "survived" electrical measurements. A standard nomenclature is adopted to distinguish them: "$S_xD_y$" refers indeed to the device y built on the substrate x. *Fig.4.3* shows the outlook of the working devices, while the next sessions will carefully discuss their characterization.

### 4.2.1 Geometrical characterization

The first step necessary to fully characterize a FET is the determination of its geometry. The channel length ($L$) is fixed by the photolithographic mask

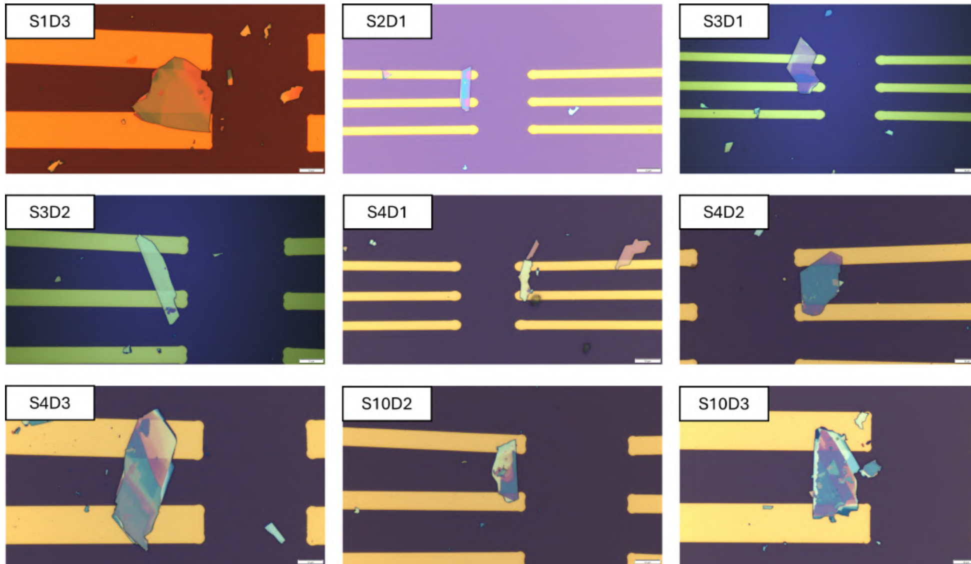


*Figure 4.3:* Outlook of the 9 working fabricated devices. All of them show different geometry, whereas channel length is fixed by the photolithographic mask used.

adopted: devices "1", "2", "3" have channel lengths equal to 8 $\mu$m, 16 $\mu$m and 19 $\mu$m, respectively. However, being the shape of each flake irregular and different from the others, AFM and optical measurements are required to establish width and thickness of each device channel. The width ($W$) is determined by approximating the shape of the whole flake to a rectangle; $W$ is then equal to the channel area, easily calculated by the optical microscope software, divided by the channel length. The thickness ($t$), instead, requires once again the use of AFM. Each AFM image is then processed by the software Gwyddion to extract the mean thickness and its associated uncertainty, computed as root mean square value. Finally, a rough estimation of the number of layers can be guessed by simple division. Indeed each layer takes approximately 1.1 nm, so it is easy to get the total number of layers, knowing the total thickness. A summary of the geometrical characterization is available in Table4.1.

| | S1D3 | S2D1 | S3D1 | S3D2 | S4D1 | S4D2 | S4D3 | S10D2 | S10D3 |
|---|---|---|---|---|---|---|---|---|---|
| $L$ ($\mu$m) | 19 | 8 | 8 | 16 | 8 | 16 | 19 | 16 | 19 |
| $W$ ($\mu$m) | 27.7 | 4.5 | 11.1 | 8.7 | 3.8 | 16.0 | 20.3 | 9.2 | 19.7 |
| $t$ (nm) | 108.5 | 86.0 | 56.8 | 54.8 | 85.1 | 92.3 | 132.9 | 73.5 | 101.1 |
| $\Delta t$ (nm) | 7.7 | 4.2 | 4.1 | 2.3 | 8.49 | 14.2 | 29.2 | 17.8 | 13.5 |
| #layers | 99 | 78 | 52 | 50 | 77 | 84 | 121 | 67 | 92 |

*Table 4.1:* Geometrical characterization of the 9 working devices.

### 4.2.2 The probe-station

Electrical measurements are aimed at the determination of transfer and output curves for each device. As for any standard FET, three probes are required: source, drain and gate. In order to be the least intrusive possible

and to do the least damage, the tips must be thin and ductile. Therefore, one has resorted to the use of the tip-probe station. The “tip-probe station” (*Fig.4.4a*) is a highly specialized piece of equipment for probing and measuring electrical characteristics. As shown in *Fig.4.4b*, it is made of several micromanipulators and a chuck, where the device is placed and connected to the back-gate terminal. Each micromanipulator consists of a mechanical arm allowed to move along X, Y and Z directions and apply voltages and probe currents by means of a tungsten tip placed at its extremity. Contrary to wire bonding, tip-probe method is far less invasive and the damage caused to the golden pad is minimal. Indeed, to apply voltages it is sufficient to lean the tip on the metal contact, without need to penetrate beneath its surface, as shown in *Fig.4.4c*. Moreover, being the tip microscopical, one can really be the least intrusive possible.

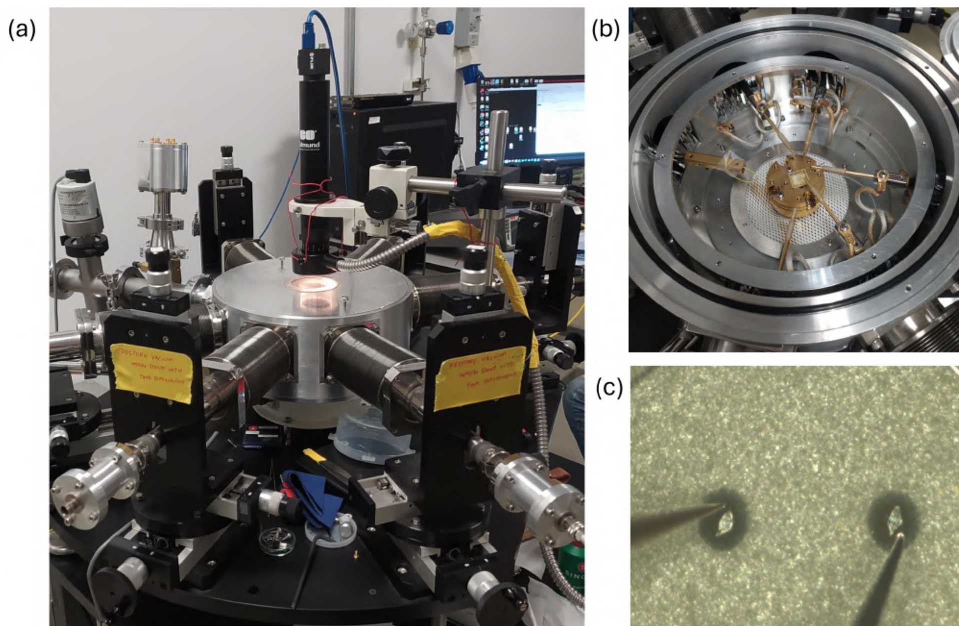


*Figure 4.4:* a) Picture of the tip-probe station from A*Star laboratories. b) Zoom in the chamber where the device is placed on the central chuck and surrounded by several micromanipulators holding tungsten tips for measurement. The position of each arm is controlled by external knobs. c) Microscope image of the contact between tips and gold pads. One can appreciate the comparison with the wire-bonding technique, which has caused the central damage in the pad.

By making use of a Python program, it is possible to draw several transcharacteristics by setting the source-drain voltage ($V_{ds}$) as a parameter. A preliminary set of measurements is run for each device in order to test its strength and robustness against voltage. To this purpose an array of $V_{ds}$ ranging from 0 V to 2 V is chosen and $V_g$ sweeps from $-60$ V to 60 V. If the leakage current remains in the order of pA, this initial test has to be considered passed and the device can undergo a more complete set of measurements, with $V_{ds}$ ranging between 1 V and 6 V, and $V_g$ sweeping from $-90$ V to 90 V.

### 4.2.3 Transfer and output curves

The main outputs of the tip-probe station are transfer and output curves. As mentioned before, they measure the relation between $I_{ds}$ and $V_g$ and $V_{ds}$, respectively. *Fig.4.5* shows both curves referred to the first device (S1D3); if the reader wants to see the complete set of measurements, they are displayed in AppendixD.

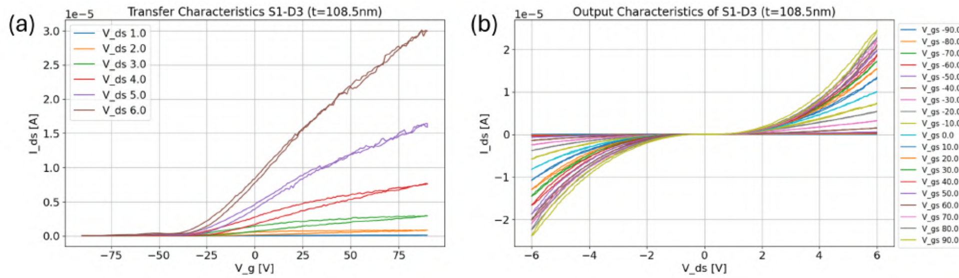


*Figure 4.5:* a) Transfer curve of device S1D3: back-gate voltage sweeps from −90 V to 90 V and $V_{ds}$ is chosen integer from 1.0 V to 6.0 V. b)Output curve of device S1D3: source-drain voltage sweeps from −6 V to 6 V and $V_g$ ranges from −90 V to 90 V.

The primary observation is the presence of minimal hysteresis in both curves, particularly noticeable in the transfer characteristics. Hysteresis occurs when the gate voltage is swept in either direction across the transfer curve, resulting in a shift in the threshold voltage[62]. This is generally considered an undesirable effect, as it causes the FET's behavior to depend on its operating history, including the direction and magnitude of the gate voltage sweep. However, this property can be advantageous for memory device applications[63] . Hysteresis is closely linked to the presence of trap states at the metal-semiconductor interface[64]. These trap states are often induced by absorbed moisture and residual oxygen from the fabrication process . Both molecules contribute to charge trapping due to their ability to polarize easily, forming dipoles that behave like capacitors at the interface. Alternatively, the same physics is observed in dangling bonds in the underlying $SiO_2$-$WS_2$ interface, which could equivalently cause the hysteretic behavior of transfer curves[65][66].

Observing the output curve, instead, one can appreciate the peculiar S-shape typical of Schottky junctions. Exactly as expected, the relation between source-drain current and voltage is not linear, but shows a steeper increase of the current for higher $V_{ds}$. The phenomenon is due to the presence of a Schottky barrier and to the increasing ability of carriers to overcome it as the voltage rises. Indeed, as the voltage increases more carriers gain higher energies and "jump" over the barrier, contributing to a larger channel current. The reason why such non-linear behavior is particularly enhanced here resides in the nature of the metal contacts chosen: gold is indeed a high workfunction metal ($\phi_m$ = 5.1 eV), which creates high SBH if coupled with a lower workfunction n-type semiconductor like $WS_2$ ($phi_s$ = 4.2/4.7 eV)[37].

An element that immediately stands out is the central flat region of the output curve. This "relatively insulating state in the low bias regime", as

it was defined by Liu et al.[60], tells us something about the entity of the SBH. At low source-drain bias, indeed, electrons possess almost solely thermal energy, which is evidently not enough to overcome the Schottky barrier. The graph clarifies that a voltage of at least 2V is required to give electrons enough energy to overcome the barrier and initiate a non-null source-drain current.

Finally, by attentively observing the whole set of data, one could notice a slight asymmetry in the output curves. Ideally, the positive and negative branches of the S-shaped curve should be symmetric with respect to the origin; however, most devices show differences between the two portions. This is normally due to a difference in the contact resistance of the two junctions, which then causes a difference in the voltage drops at the metal interface. But the phenomenon could be more complex than it appears and be caused by the presence of impurities at the interface. These factors would amplify the FLP effect and differentially modulate the two SBHs. Additionally, impurities could introduce trap charges that generate localized fields, which in turn may disrupt or alter carrier flow. Furthermore, asymmetry may be caused by an unequal gate control, due to an unbalanced deposition of the flake onto the silicon substrate[67].

### 4.2.4 Threshold voltage determination

One important parameter to determine while characterizing a FET is the threshold voltage. It corresponds to the activation voltage of the device and it is the minimum voltage required to open the FET channel and observe some source-drain current. Therefore, it is closely related to some intrinsic properties of the device, such as the material and doping. Material properties such as bandgap energy, doping concentration, and electron affinity affect how easily carriers can be moved in the channel, thus influencing $V_{th}$. Moreover, the dielectric thickness plays an important role in the definition of the threshold voltage as thicker $SiO_2$ will necessitate higher gate voltage to induce a charge in the channel. However, the determination of this pivotal parameter is not straightforward. In fact, each curve is subject to signal noise and it is far from ideal. A Python code is thus necessary to determine a suitable linear fitting and extract the threshold voltage by intersecting the calculated line with the x-axis. Starting from an array of given initial points, the algorithm tries dynamic sets of datapoints for the linear fitting, then chooses the one with the least associated standard deviation. A minimum interval of 30 datapoints is requested in order to prevent the software from choosing trivial solutions.

As most of the transfer curves show hysterisis, both the forward and the backward curves are analyzed and their associated $V_{th}$ is computed. *Fig.4.6a,b* shows such a linear fit on the set of forward and backward curves of the first device. One can appreciate a certain convergence of the calculated threshold voltages, which indicates that both the algorithm and device are functioning properly. It is also interesting to perform a comparison across the different devices to look for consistency in electrical performances. *Fig.4.6c* plots the forward transfer curves and their linear fit (at $V_{ds} = 6$ V) for each device. One

can observe a general trend of threshold voltages with values between −30 V and −20 V, with the exception of a few devices. Moreover, the algorithm seems to work fine for all of them.

Something that can be effectively analyzed is the absolute position of the threshold calculated. The latter is indeed quite negative and, despite being consistent with existing literature (see Sec.4.1), its absolute value is to be attributed to the experimental conditions of measurement[68]. Indeed, the whole set of electrical measurements has been done under high vacuum ($10^{-4}$ torr) with the help of a turbo-pump. Vacuum is responsible for dragging out superficial $O_2$ or $H_2O$ molecules that were adsorbed from the atmosphere. Recent research connected their presence to some p-type doping and thus to the right-shift of the transfer curve. P-type doping introduces more holes and a more positive gate voltage to turn the device on is required. As a result, the threshold voltage increases, shifting the transfer curve to higher voltages[69]. High-vacuum prevents this from happening and allows the measurement of the pristine n-type state of the device.

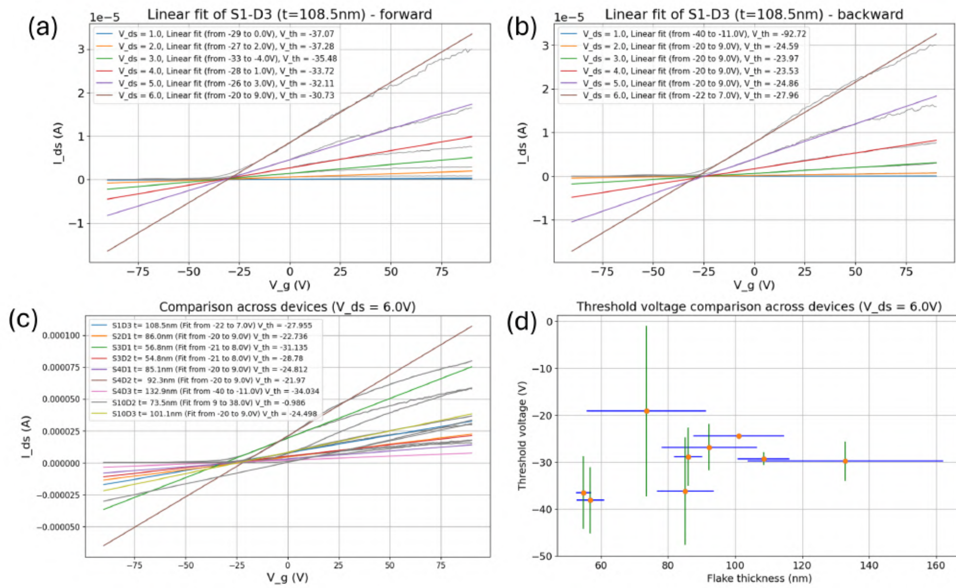


*Figure 4.6:* a) Forward and b) Backward transfer curve of device S1D3 with the plot of their linear fit. The legend reports on the $V_g$ range chosen by the algorithm for the fitting and the resulting threshold voltage. c) Plot of the forward transfer curves at $V_{ds}$=6 V for each device and their linear fit. The legend reports on the $V_g$ range chosen by the algorithm for the fitting and the resulting threshold voltage. d) Plot of the threshold voltage as a function of the flake thickness for each device at $V_{ds}$=6 V. Error bars are chosen to be the standard deviation of the threshold voltage and the root mean squared value of the thickness, calculated on the AFM images.

Finally, it is interesting to plot the obtained threshold voltages as a function of the device thickness to see if some correlation exists. *Fig.4.6d* shows the datapoints of the devices with most coherent threshold voltages and their associated error bars: the uncertainty on the threshold voltage is computed as the standard deviation on the forward and backward threshold voltages, while the error on the thickness has been computed in Sec4.2.1 . In general

one can appreciate a slight increment in the threshold voltage as a function of the thickness. This is fully justified physically by Liu et al.[70]: thicker channels prevent the gate voltage from distributing more efficiently, thus requiring a higher threshold voltage. Moreover, thicker flakes produce lower resistances and thus lower threshold voltages.

### 4.2.5 On/off ratio determination

In order to estimate the adaptability of the fabricated device to the world of digital applications, it is necessary to study the performance of each of them in terms of their on/off ratios. Such a parameter is easily calculated in absolute value as the ratio between the highest and the lowest value of $I_{ds}$ taken in the transfer curve. They should correspond respectively to the on- and off-state of the transistor device. In order to provide a graphical visualization, the logarithmic plot of the transfer curve could be used. *Fig.4.7a* shows the superposition of all the transfer curves taken at $V_{ds} = 6$ V and labeled with their identification code and thickness. Obtained on/off ratios are ranging between $10^3$ and $10^5$, a little lower than the values reported in Sec.4.1. The lower on/off ratio and the general lower performance of the fabricated devices is mainly due to the quality of the metal contact realized. Metal-semiconductor interface is indeed crucial in the achievement of good performances; the presence of impurities hinders a smooth current flow, pinning the Fermi level and raising the contact resistance. Ultimately, this will not only lower the on-state, but also raise the off-state, which will always be biased by the electric field generated by trap states. *Fig.4.7b*, on the other hand, illustrates the on/off ratio as a function of flake thickness, including the associated uncertainty. A general decreasing trend is observed, which is attributed to the higher off-current in thicker channels due to enhanced leakage paths and reduced gate control[71].

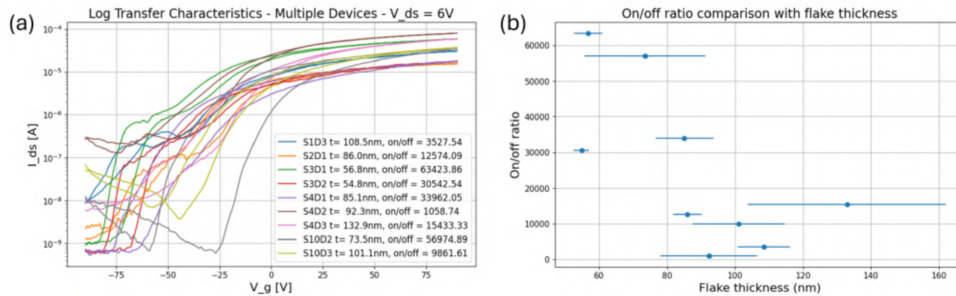


*Figure 4.7:* a) Logarithmic plot of transfer curves at fixed $V_{ds}$=6 V. In the legend both flakes thickness and calculated on/off ratios. b) Plot of the on/off ratio of each device as function of the flake thickness. The horizontal error bar is determined by AFM measurements.

### 4.2.6 Mobility determination

Finally, the last parameter to determine is the carrier mobility. As it might be guessed from the shape of the transfer curve, the main carriers are essentially electrons, coherently with the n-type behavior of $WS_2$. Typical $WS_2$

electron field effect mobilities are of the order of 20 $cm^2V^{-1}s^{-1}$, but in the present research the calculated mobilities amount to one order of magnitude less. This piece of evidence further confirms the hypothesis of bad contact quality. A high contact resistance, indeed, could hinder the flow of carriers inside the channel[72]. Moreover, any surface roughness perpetuates at the interface in terms of scatter points to lower electron velocity. In addition, as *Fig.4.8a* shows, the mobility is slightly proportional to the source-drain voltage, despite the increasing uncertainty (propagated from the fitting error on the line slope). Such a behavior is often observed experimentally and it is due to the effect of the increment of the longitudinal field, which gives higher energy to the electrons and therefore allows them to overcome the influence of scattering phenomena. Eventually carrier velocity will saturate with $V_{ds}$ and reach a plateau in the so-called "pinch-off" condition. As a sake of completeness, instead, *Fig.4.8b* plots the mobility as a function of the flake thickness. As expected no relation exists between the two quantities.

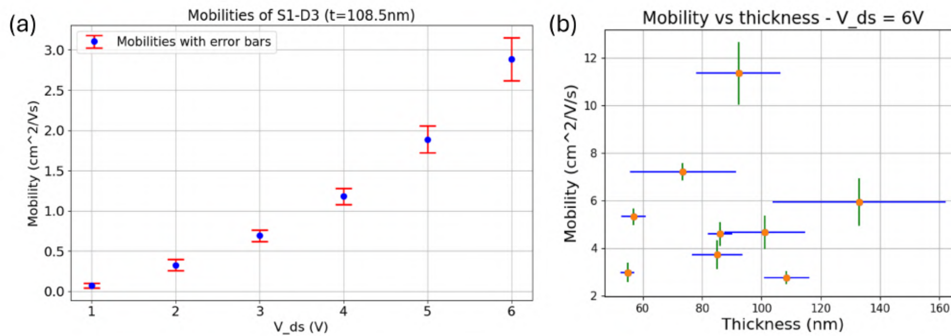


*Figure 4.8:* a) Electron mobility as a function of $V_{ds}$ for the first device. Uncertainty is given by the propagation of the uncertainty on the slope of the transfer curve linear fit. b) Plot of the mobility as a function of the flake thickness. Horizontal error bar is given by AFM measurements.

In conclusion, this chapter provides a detailed characterization of the fabricated $WS_2$-based FETs, focusing on both their geometrical and electrical properties. Geometrical analysis through AFM and optical microscopy allows for accurate measurements of the channel dimensions, including width and thickness, which varies due to the irregular shape of the $WS_2$ flakes. Electrical measurements conducted using a tip-probe station reveal important aspects of the device behavior, such as transfer and output characteristics.

Overall, the device performance is lower than anticipated, largely due to the larger channel dimensions. As shown by Acar et al.[73], longer channels introduce more scattering centers, reducing the source-drain current. Despite these challenges, the consistent trends observed across multiple devices underscore the impact of fabrication imperfections, especially at the metal-semiconductor interface. Nevertheless, the results offer a solid foundation for refining device performance, supporting further research into $WS_2$-based transistors.

# Chapter 5

# Fabrication of a 2D $WS_2$ field effect transistor

The second part of the project is aimed at the realization of Hall bar shaped 2D FETs realized by photolithography on CVD-grown $WS_2$ on sapphire substrate and at their electrical characterization. Handling monolayers requires a high level of expertise, but among all TMDCs, $WS_2$ should offer a good resistance to air-self oxidation and be quite robust against time deterioration, thus guaranteeing the highest probability of success[74]. The choice of sapphire is instead driven by the growth process of $WS_2$ itself. In fact, the highly pure and homogeneous monolayers available can be grown on sapphire only. Fabricating the device on this substrate is therefore convenient because no transferring technique is required[75]. On the other hand, metal contacts are realized in gold. The latter has been widely tested in the lab and presents high electrical stability and good performances in terms of pliability[76][77]. Despite its large work function[78], which should match well with n-type $WS_2$, gold has provided poor results in terms of electrical contacts. As explained in Sec.2.3, Fermi level pinning and high Schottky barrier do not allow for either an ohmic behavior nor low contact resistance. The latter can be so high that the device most often presents contact properties rather than channel properties[16]. It is reasonable to expect poor ohmic behavior and high contact resistances, favored by a considerable Schottky barrier. A full experimental protocol will be described hereafter with the objective of producing Hall bar devices by photolithography on $WS_2$ monolayer CVD-grown on sapphire substrate and testing their electrical performances, with particular focus on the contact resistance. The latter can be easily calculated by means of the 4-probe measurement allowed by the chosen geometry.

The first part of this section will deal with the outline of the experimental fabrication of the devices, accounting for differences in technique and protocol with respect to the previous fabrication process. The second subsection will instead focus on the measurement techniques that are intended to be used to

collect output and transfer characteristics. The last subsection will instead consider the results of the obtained measurements and describe some experimental tests aimed at optimizing and improving the quality of the fabricated FETs. The entire process of fabrication of a 2D TMDC Hall bar FET is sketched in *Fig.5.1*.

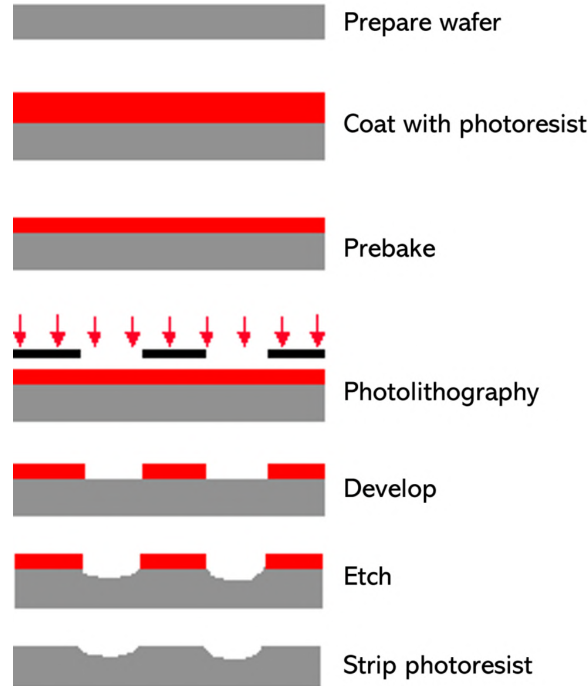


*Figure 5.1:* Generalities of the photolithographic process.[25] In gray the TMDC layers and in red the photoresist applied.

The first step of the fabrication of the 2D FET is the growth of the $WS_2$ on a sapphire substrate. Even if the growth process is not subject of interest of this report, one can mention that the samples provided were the result of chemical vapor deposition (CVD)[14][79][80], with measured thickness of 0.7 nm, corresponding to a monolayer of $WS_2$. The reader can delve into the CVD process by reading AppendixB.

Before starting the fabrication process, though, it is necessary to accurately clean the surfaces of the samples by washing them in acetone and IPA. These two chemicals are effective to eliminate any organic impurity and any salt or resin deposited on the device surface. Finally, any IPA droplet will be evaporated by a gentle nitrogen flow. The choice of nitrogen is justified by its lower reactivity compared to $O_2$ and $H_20$ - rich air, moreover it does not alter the cleanroom atmosphere composition. The sample is now ready to host the top layer of photoresist.

Positive photoresist $s1181$ can still be used in this fabrication line, with the advantage that surface $WS_2$ monolayer does not necessitate a preliminary exposure to $O_2$ plasma to ensure PR homogeneous distribution. Exactly as before, the sample is baked at 110°C for 60 s to enhance the stability of the

PR on the surface. Hall bar patterns are then printed by photolithography on the hardened PR and developed in $MF319$ for 60 s. Afterwards, each sample is cleaned in IPA and soaked in DI water to get rid of residual developer. At the end of this fabrication step, the device would look like the one depicted in *Fig.5.2a,b*. However, it is necessary to specify that, despite mandatory, the use of DI water can harm the continuity of $WS_2$ monolayer by peeling off some portions of the thin film due to the high hydrophilicity of the sapphire substrate. This issue is anyway localized to little portions of the printed patterns and at this stage of fabrication it cannot be said whether it will effectively harm future electrical measurements.

## 5.1 Reactive ion etching: getting rid of unwanted $WS_2$

After the small patterns being printed on the PR, these must be transferred into the substrate. Up to this fabrication step, the substrate has not been modified and still preserves a sapphire bulk with a uniform $WS_2$ monolayer on top. It is necessary to etch away the uncovered TMDC from the bulk to finally create the Hall Bar pattern on the $WS_2$. This procedure is done by the reactive ion etching machine. It consists in a chamber where the device is carefully placed and brought to infinitesimal pressures (approximately $10^{-7}$ torr); this is the "standby" pressure to keep the chamber clean and not contaminate the device while etching. Once the target pressure is reached, a 20 W power $SF_6$ gas is blown over the device for 15 s at a flow rate of 30 sccm; the pressure then rises to 60 mtorr. The remaining PR will protect the Hall bar-shaped TMDC from the plasma, which will instead etch away the exposed semimetal thanks to its highly reactive ions, leaving the nude sapphire exposed to air. 15 s, however, may not be sufficient to effectively etch away $WS_2$, especially at this low power. One therefore may choose to let the device undergo an additional 15 s etching cycle, still keeping the plasma pressure at 20 W, thus guaranteeing minimal PR damage. While the plasma is blown onto the surface, a tiny glow can be glimpsed from the little window on the chamber wall. Air is then pumped into the chamber and the device is ready to be stripped.

## 5.2 Stripping: to remove residual PR

The device is almost ready to host metal contacts, but first one needs to get rid of the unwanted remaining photoresist. This is usually done by a standard set of chemicals consisting in acetone, IPA and DI water. The device is left in acetone for a couple of hours, then rinsed in IPA and finally rinsed in DI water. Unfortunately, what is observed at the microscope does not quite match with the expected outcome (*Fig.5.2*).

Several trials and much research[81] have been useful to discover that DI water, if rinsed on the surface, acts as a detaching medium that pulls TMDC into nanoribbons. It sorts the same effect of soap with dirt on human skin: it is indeed due to the hydrophilic character of water and the composition of both sapphire and TMDC. To improve the stripping of photoresist it is

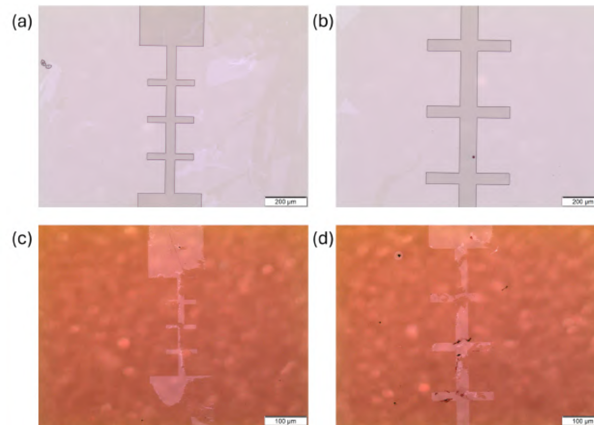


*Figure 5.2:* Control samples a)b)before etching and c)d)after stripping with acetone, IPA and DI water. Water, thanks to its hydrophilic character, has penetrated below $WS_2$ and lifted it off from the sapphire. In fig a) and b) one appreciates a darker Hall-bar shaped area consisting of $WS_2$ covered with PR on a lighter gray colored substrate of sapphire. In fig c) and d) instead, the sapphire substrate is colored in dark orange, while what remains of the $WS_2$ is in light pink; darker dots are $WS_2$ nanoribbons.

sufficient to substitute the action of "rinsing" with "soaking" in DI water; this still allows to get rid of any residual acetone molecule, but more gently. Despite some persistent imperfections, this new set of devices is now ready to host metal contacts. Metal contacts are deposited with different thicknesses (20 nm, 26 nm and 65 nm) to test and optimize the lift-off process.

## 5.3 Lift-off: a different recipe

The sample taken out of the glove-machine looks much like a golden plaque because gold has deposited uniformly on the sample. One must therefore take care of removing the unwanted gold. Unfortunately, due to the fragile nature of TMDC monolayers, ultrasonication cannot be used for this fabrication. The high-frequency wavelengths produced by the machine would damage the device permanently, preventing the process from continuing. Fortunately, by soaking the sample in acetone for a couple of hours, the chemical will react with the hidden PR and still lift off the undesired gold gradually. This simple process, however, has a drawback: some portions of gold may not lift off completely, but remain floating in acetone, especially if the thickness is large. The operator shall therefore apply a gentle flow of acetone on the sample to remove parasitic gold shreds: this bubble-jet technique can be simply done with a pipette and much carefulness. Among the thicknesses chosen, the 20 nm proved itself to be the easier to lift-off, while the 65 nm shows much unwanted gold, despite several minutes of bubble-jetting. Thicker layers of metal, indeed, have higher chances of being still joint at the etching boundaries, causing more troubles in lifting off. Once ready, the sample is dried up with $N_2$ flow and it looks like the one depicted in *Fig.5.3b*. It is now ready to start gate patterning.

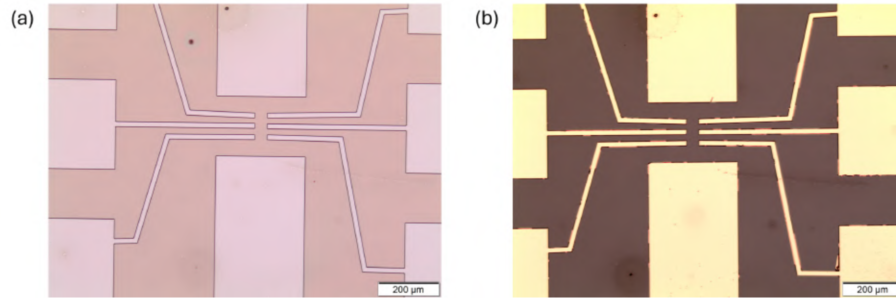


*Figure 5.3:* a)Image of metal contact pattern printed by photolithography. Upper and lower rectangles will host drain and source terminals, while side contacts will pin the lateral branches of the Hall bar for transversal current measurements. b)Image of gate contacts after lift-off. Gold was correctly deposited on the entire surface of the sample and then the latter was soaked in acetone and bubble-jetted to remove gold from "now-dark" areas of the device. The process produced a quite clean metal pattern with minimal impurities scattered in the upper region.

## 5.4 Gate patterning: the atomic layer deposition

Up to now one has dealt with the fabrication of a Hall bar device with source and drain contacts, but nothing has been said about the gate. Contrary to the previous fabrication, these devices adopt a top gate. Indeed, because of its high dielectric constant, sapphire cannot be employed as a bottom gate. A whole new gate pattern must be printed on top of the device channel. The procedure followed is identical to the one used for source and drain and it is sketched in *Fig.5.4a*. Among the three contacts in a FET, the gate presents an extra oxide layer between the semiconductor and the metal. While metal deposition occurs precisely like described above, oxide deposition requires a different engineering technique called atomic layer deposition (ALD), performed by the machine in *Fig.5.4b*.

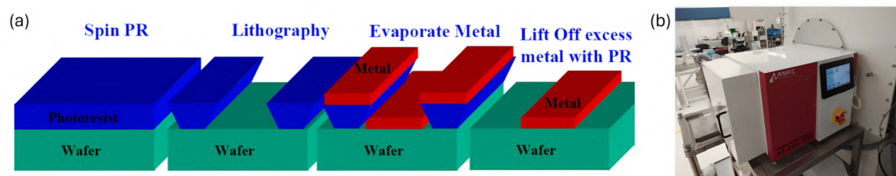


*Figure 5.4:* a) Sketch of the fabrication process to print a gate pattern by photolithography and lift-off the excessive metal[69]. b) ALD machine in A*STAR cleanroom.

ALD is a precise thin-film deposition method that applies dielectric layers at the atomic scale onto a substrate. ALD operates through a series of self-limiting chemical reactions which stop once a monolayer has formed on the device surface. The chosen oxide is $HfO_2$ and the machine deposits it through alternating exposures of the substrate to two or more chemical precursors. Hafnium precursor will be $HfCl_4$, while the oxygen source will be simply $H_2O$. Initially, the substrate is exposed to the hafnium precursor, which reacts with the surface, forming a monolayer of hafnium atoms bonded to the surface. Argon (already present in the glove-machine) is introduced

to purge the reaction chamber, removing any unreacted precursor and reaction by-products from it. The substrate is then exposed to the oxygen source, which reacts with the hafnium-containing layer on the substrate to form $HfO_2$. The ALD cycle is repeated until the desired thickness of $HfO_2$ is achieved. Each cycle typically deposits a sub-monolayer of material, while this may take a few hours, it allows for precise thickness control. The ALD machine is shown in *Fig.3.8c* and operates at a pressure of 180 mtorr at a flow rate of 28 sccm. Unfortunately though, it is impossible to remove $HfO_2$ from unwanted (non-gate) regions of the device because such oxide is capable of resisting PR lift-off by acetone. The operator will therefore deposit $HfO_2$ on the whole surface of the device knowing that later metal wires for electrical contacting will need to penetrate the oxide layer to reach source and drain. Fortunately, $HfO_2$ is quite transparent, so such an operation does not imply great difficulty. Finally, the device would look aesthetically as shown in *Fig.5.5*, where one can observe source, drain and gate contacts placed on top of a well-defined Hall bar. However, the device cannot be measured until proper wire bondings are placed on top of its metal contacts.

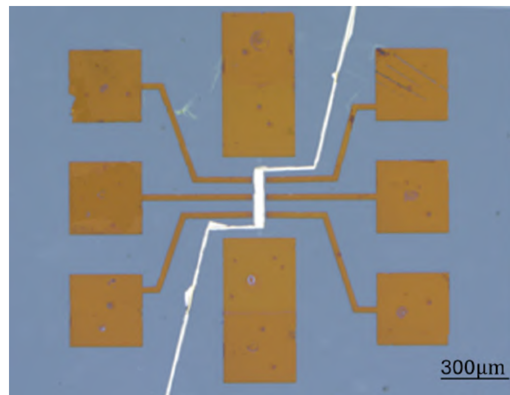


*Figure 5.5:* Final outcome of the device fabrication. One can appreciate the deposition of gold on gate patterns appearing brighter than other gold contacts because the latter are placed under the thin layer of $HfO_2$. Some imprecisions on the gate pattern are caused by lift-off.

## 5.5 Packaging and wire bonding

Finally, the sample is packaged in a standard $44-pin$ chip package, with aluminum bonding wires connecting the Hall-bar contacts to the package pins. The process of wire-bonding is quite elaborate and requires different steps and facilities. First of all, one needs to secure the device to the chip carrier by using a special silver paste, which will act as a glue if allowed to dry for a couple of hours. Then the sample and carrier will be placed in the wire bonding machine. The latter, displayed in *Fig.5.6b*, makes use of a microscope and soft moving motors to help the operator targeting the area where the aluminum wire should bond the sample surface (*Fig.5.6c,d,e*). Once the metal pin is targeted, the machine bonding head approaches the surface thanks to a *DCservo* motor and a wire clamp performs the tear and tail operation by using ultrasonic vibrations. The machine then moves toward one of the Hall

bar metal contacts, pulling the wire, and performs a second tear, thus connecting the two pads. The wire is then cut and the machine is ready to repeat the process again. The entire procedure is illustrated in *Fig.5.6a*.

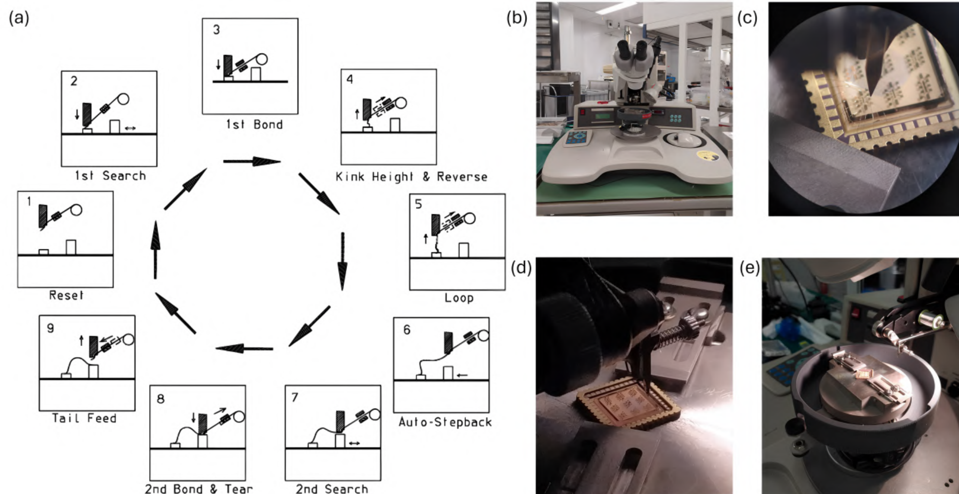


*Figure 5.6:* a)Illustrated procedure of wire bonding. 1: The head aligns with the targeted pin. 2: The head approaches the target. 3: First bond is made and aluminum wire penetrates the gold beneath. 4: The tip retreats and withdraws the wire. 5: The head lifts up, stretching the wire. 6: The head moves toward the target. 7: The head approaches the target. 8: Second bond is made and the tip tears off the superficial oxide layer to reach the gold underneath. 9: The wire is then cut and the head lifts off, feeding more wire to repeat the process[82]. b) Machine for wire bonding, model 4523*ADigital*, from A*STAR cleanroom. c) Microscope image of aluminum wires connecting the Hall bar with the gold pins of the chip carrier. d)Zoomed image of the microchip held in the wire bonding machine before wire bonding starts. e) Microchip carrier held on the machine holder under the bonding head with visible aluminum wire coil.

The advantage in using the wire bonding machine lies in its automatization. In addition to the microscope facility to better see the metal contacts, the wire bonding machine allows control of every physical parameter playing a role in the process; bonding power, force and time are only some of the controls that can be set by the machine. Naturally, these parameters do not maintain the same value between the first and the second bond. When the tip penetrates the pure gold surface of the carrier pin, indeed, less force is required and power can be low as well; on the other hand, to tear off the oxide and pin the gold contact, the tip requires higher power and higher force, which cannot be too strong otherwise the tip may tear off the gold, too, thus failing the wire bonding. Interestingly, one can also fix the tear and loop parameters, which respectively set the length of the tear movement and the height to which the bonding head moves after the first bond.

The optimal set of parameters, however, is not provided by the machine manual and the operator must perform different trials on buffer samples before finding the optimal array of values. Once the optimal set is found, wire bonding can proceed on the fabricated devices.

## 5.6 Measurements

The reason why the Hall bar geometry was chosen lies under its accuracy in the determination of electron mobility and sample resistivity. Resistivity is an intrinsic property of any material, meaning that it does not depend on its dimensions; in order to measure it, however, it is necessary to probe currents and voltages to finally determine resistances, by applying Ohm's law. Resistances, contrary to resistivity, depend on the sample geometry and, in the specifics of Hall bars, on the channel lengths between contacts. The resistance of a semiconductor channel is indeed given by:

$$R_{semi} = R_s \frac{L}{W}$$

with $L$ and $W$ the length and width of the channel between contacts and $R_s$ the sheet resistance of the sample. Such a parameter is of particular interest in experimental physics because it contains both geometrical and chemical information of the analyzed material, it is indeed calculated by

$$R_s = \frac{\rho}{t}$$

with $\rho$ the sample resistivity and $t$ the device thickness. However, $R_{semi}$ is not the only resistance that will appear in the characteristics of the measured device. The current flowing from source to drain, indeed, will move from the gold contact to the semiconductor passing through a first Schottky interface, it will then reach the second gold contact crossing a second semiconductor-metal interface. The measured resistance will then be equal to:

$$R_{tot} = 2R_m + 2R_c + R_{semi}$$

where $R_c$ is the contact resistance and $R_m$ the metal resistance, often negligible because very small compared to the others. Theoretically speaking, one should evaluate the contact resistance by considering only a small region in the vicinity of the contact, as depicted in *Fig.5.7a*. Then the contact resistance will be given by: $R_c = \rho\frac{\Delta X}{A_c}$ by the second Ohm's law, with $A_c$ the contact area. By extending this formula to infinitesimal distances, a mathematical limit appears:

$$R_c = \lim_{\Delta X \to 0}(\rho\frac{\Delta X}{A_c})$$

However, practically one cannot apply the previous formula, because it is not practicable to measure these quantities when $\Delta X$ becomes very small; therefore one must resort to its most immediate application, which resides in the expression of $R_{tot}$. By exploiting the simple geometry of a 4-contacts Hall bar as the one depicted in *Fig.5.7b*, one can play a little with the various terminals and derive some important quantities: $R_{4T}$, the "pure channel" resistance between the internal side contacts; $L_{4T}$, the longitudinal distance between the two side contacts; $L_{2T}$, the whole channel length, and, finally, $R_{2T}$, the total FET resistance. Therefore, by simply inverting the formula of the total resistance, one can easily get the expression of the contact resistance:

$$R_c = \frac{1}{2}(R_{2T} - \frac{L_{2T}}{L_{4T}}R_{4T})$$

*Fig.5.7b* also provides an insight on the measurement circuit apparatus that is used to physically measure electrical currents and voltages on a simple

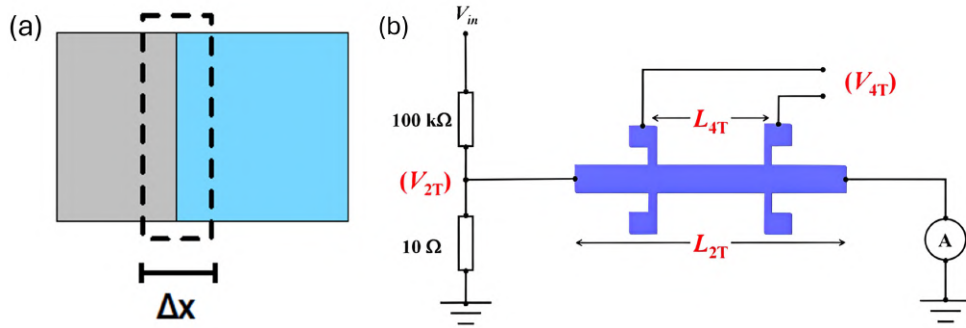


*Figure 5.7:* a)Zoom on the contact area of a device. In blue the semiconductor and in gray the metal of the contact. b)Scheme of the Hall bar measurement system. The picture highlights the channel lengths between metal contacts and provides values of the resistors that build up the measurement circuit.[83]

Hall bar geometry. The device is indeed inserted in the tank of the machine depicted in *Fig.5.8b* by means of a chip socket (*Fig.5.8a*), which integrates the chip carrier hosting the device with further metal wires connections that will allow the measurement apparatus to operate on the device. The socket is inserted in the metal tank, where measurements can be performed either at room temperature or at 77 K, by simply pouring liquid $N_2$ in the chamber. In that specific case, liquid nitrogen would not touch the surface of the device directly, but would refrigerate the sample holder, which, by thermal induction, cools down the device itself. Eventually, an electromagnet can be placed inside the chip socket to exert a magnetic field perpendicular to the device and thus induce classical Hall effect. However, prior to magnetotransport measurements, the device can be treated as a standard 2D FET, so that output and transfer characteristics may be drawn first. Measurements are performed at a constant current, whose stability is ensured by the two resistors of 100 kΩ and 10 Ω that separate output current from the lock-in amplifier that will inject the signal into the machine. The software interface allows for clear and smooth parameters setting.

The measurement performed on the fabricated devices shows a dramatic scenario. No current is indeed measured in any of the Hall bars patterned on the given $WS_2$ sample: the machine displays an indefinite current value, rapidly oscillating around 0 A, meaning that noise is the only detected signal. Even by trying different metal pads and Hall bar side contacts the output is always the same: the machine is measuring the electronic characteristics of an insulator.

Given the results obtained, the measurements cannot proceed with the determination of the transfer and output curves, nor with the calculation of the contact resistance. Indeed, it is of the utmost importance that at least a single sample works perfectly to allow a meaningful data analysis and comparison with future measurements. Therefore, the priority is to find the cause of the lack of current in the FET channel in order to proceed with the fabrication. To this purpose, a series of minor experiments are carried out and described in the next section.

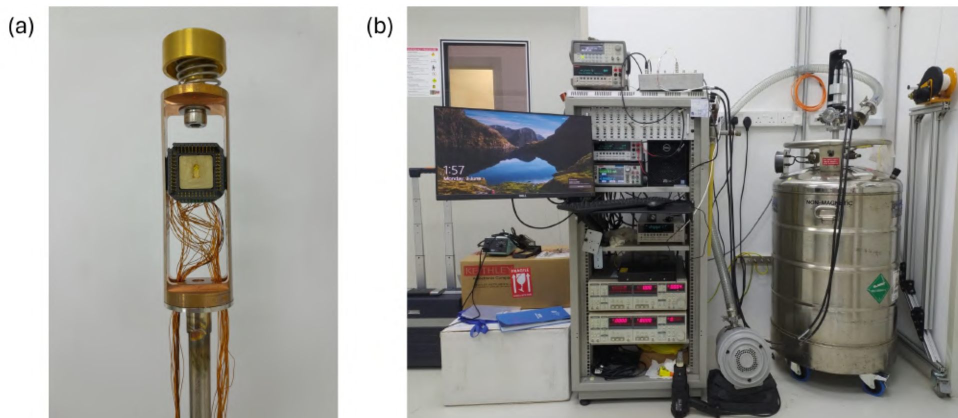


*Figure 5.8:* a) Illustration of chip socket hosting the chip carrier with a device connected by metal wires to the contact pins. The same pins are then connected to longer wires that run along the whole socket length and enter the measurement machine. b) Measurement apparatus from A*STAR laboratories. Chip socket is inserted in the metal tank on the right and copper wires connect it to the instrumentation on the left running in the plastic tube above. Measurement machines and power generators are placed at the end of the wires.

## 5.7 What went wrong: a new solution approaches

Considered the high level of difficulty involved in the fabrication of CVD-grown $WS_2$-based devices, the poor performance measured is not a surprise. However, it is interesting to identify the reason for the lack of current in order to know what to improve, change or avoid in a future fabrication phase. The possible macro-causes of this first piece of evidence could be only two: either something went wrong in one or more fabrication steps or the $WS_2$ film quality was not good. However, this last hyphothesis can be excluded a priori because of some optical tests performed by the film producer. Raman spectroscopy and photoluminescence analyses can, indeed, firmly confirm the material quality and uniformity. Moreover, despite the natural uncontrolled oxidation emerging from exposure to the atmosphere, $WS_2$ shows a quite robust resilience, compared to other TMDC films [84][74]. Therefore, the cause of the absence of current has to be searched in the experimental fabrication process.

### 5.7.1 Revision of the most critical fabrication steps

While the CVD-grown $WS_2$ film quality can be proven a priori, the same cannot be done for any of the described fabrication steps. Furthermore, one cannot exclude the possibility that even more than one step could present some irregularities or even have failed during the process.

By carefully analyzing the microscope images taken at each step of the process, one would clearly understand that some procedures could be somehow optimized. *Fig.5.9* displays two of the major criticalities of the fabrication line: development anomalous effect and lift-off problems. The latter has been briefly mentioned in Sec.5.3 and consists in the partial failure of acetone in removing the excess gold by dissolving the PR underneath. Moreover, the "bubble-jet" technique performed by the operator depends strongly on the force applied and the risk to remove the wanted gold with the monolayer

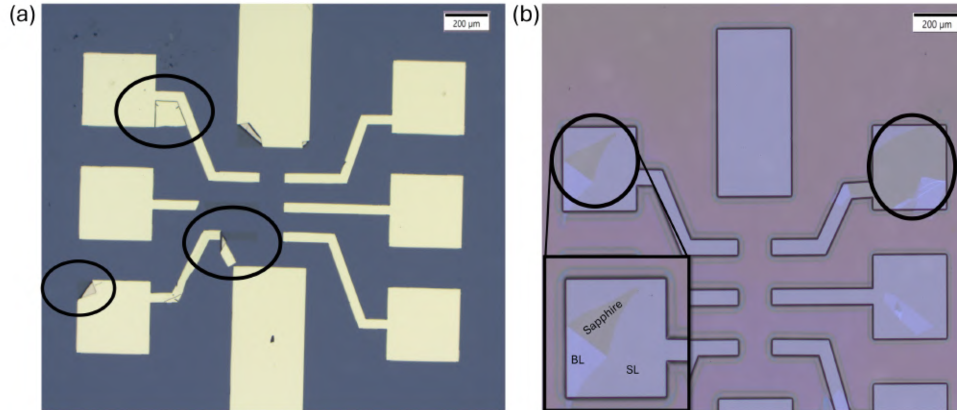


*Figure 5.9:* a) Evidence of lift-off fabrication. In the three circles one can appreciate three common issues resulting from lift-off procedure: the persistence of some gold on the sapphire substrate due to insufficient time of exposure to acetone, the break of gold contacts due to excessive lift-off and the folding of metal layer due to excessive lift-off and high adhesion within metal surfaces. b) Development issues due to hydrophilic power of DI water, which binds to the sapphire and peels $WS_2$ off. In the inset one can appreciate a typical situation of peeling off, where a portion of monolayer has been lifted by DI water and then folded on itself producing a bilayer and leaving a nude portion of sapphire to air; this particular situation could be quite dangerous for the continuity of the upcoming metal deposition and could mine the smoothness of current flow.

attached is high, if not calibrated appropriately. The first issue, instead, consists in the unwanted lift-off of the $WS_2$ film, followed by a possible successive self-folding, due to the use of DI water at the end of development phase. As explained in Sec.5.2, DI water interacts with the hydrophilic sapphire substrate underneath $WS_2$ and penetrates in their interface forcing the monolayer to take off and break. Although a rapid soaking in DI water does not remove the whole film from the substrate, thus not sensibly altering the Hall bar structure, it would be interesting to optimize this fabrication step anyway, because it can still create ribbons or foldings that might alter the smooth flux of carriers.

This issue has been addressed by Kwon et al. in a recent paper dealing with the fabrication of CVD-grown $MoS_2$ monolayer-based devices[46]. The authors fabricate a large number of devices by a fully optimized fabrication process and strongly suggest the implementation of simple strategies to prevent developing and lift-off issues from happening.

The adoption of bottom contacts would be an effective strategy to eradicate any lift-off issue. Gold would indeed be deposited in an etched region of the substrate, leaving a larger distance from the metal deposited on the PR: the mechanical force exerted by bubble-jetting can act more effectively to break the thin metal tongue separating the two metal levels and successfully lift off the unwanted gold. Moreover, the wet process of removing excess gold by acetone would be performed on the substrate directly, avoiding any chemical or mechanical damage of the $WS_2$ monolayer, which will be transferred on top of the metal later. Kwon's devices show a sizeable reduction of

the contact resistance when compared to their top-contact equivalents, sizeable enhancements where also found in the field-effect mobility and threshold voltage; these evidences are justified by the reduction of impurity density at the metal-semiconductor interface, tailored by a stronger adhesion between the two materials, which will hardly peel off in the next fabrication steps. *Fig.5.10* shows the graphical comparison between top and bottom contacts.

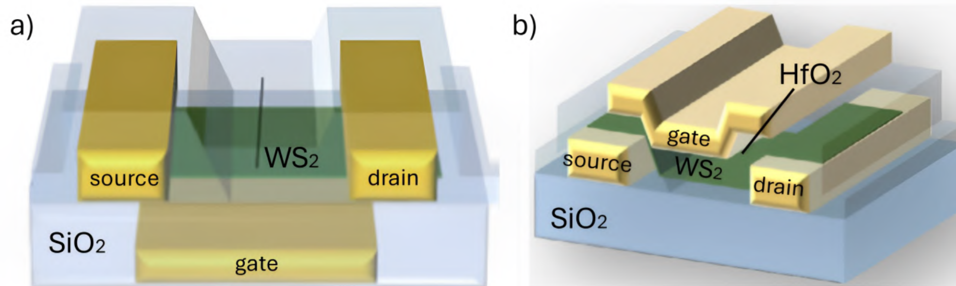


*Figure 5.10:* a) Representation of a top contact 2D FET with bottom gate: the gate contact exploits $SiO_2$ layer as dielectric and does not require additional oxide deposition. Source and drain contacts are deposited on top of the $WS_2$ monolayer, as described previously in this chapter. b) Representation of bottom contacts 2D FET with $WS_2$ monolayer on top of source and drain contacts, which have been deposited before transferring the film on $SiO_2$ substrate. Gate terminal is printed by photolithography on top of $WS_2$, which is coated with the $HfO_2$ gate dielectric.[46]

The second strategy proposed by Kwon et al. consists in the change of the substrate material. The devices built in this chapter adopts a substrate made of sapphire, which, initially, can be a convenient choice because it constitutes the wafer onto which $WS_2$ monolayer is first grown in the CVD process. However, sapphire reported many adhesion problems with $WS_2$ monolayer. It is thus necessary to move the film onto a more adhesive substrate: $SiO_2$ is a well known material, whose properties have been tested and confirmed for decades, thus it is a better alternative to sapphire.

Despite the conceptual simplicity of changing substrates, experimentally speaking this process requires a high level of expertise and precision. $WS_2$ monolayer is indeed extremely delicate and may severely damage during the transition from one surface to another. The transfer process will therefore have to be carefully studied and optimised once it is decided to proceed with it. The reader can appreciate a tentative transferring of $WS_2$ monolayer in AppendixC.

### 5.7.2 Contact quality: the use of chemicals

In parallel to the previous analysis, another measure is carried out to test the influence on the film quality of the chemicals used. Indeed, one plausible reason why current is not observed to flow in the fabricated channel is that somehow gold contacts cannot lie directly on $WS_2$, but the junction is maybe insulated by some intermediate dielectric layer. This possibility exists and it is coherent with the hypothesis of a defective developing phase. As a matter of fact, if the developing solution is not capable of removing the UV-exposed photoresist, a thin layer of PR would persist on the film surface, thus preventing gold from contacting the semiconductor. One simple way of

verifying this theory is performing atomic force microscopy (AFM) on a sample showing a clean boundary between developed and undeveloped area. The chosen sample is displayed in *Fig.5.11a* and the AFM scanning is reported in *Fig.5.11b*, which also shows the segment where the height profile is computed to measure the film height.

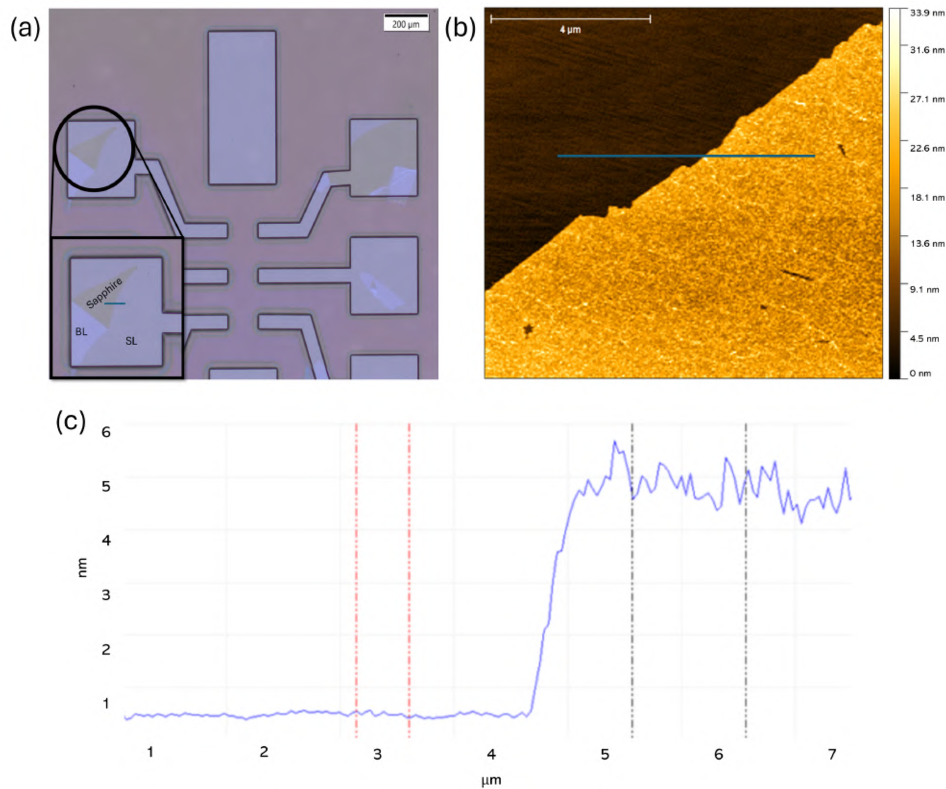


*Figure 5.11:* a) Selected device for AFM scanning. The chosen area lies in a pad where $WS_2$ has been peeled off by the DI water used to clean the sample from the developer; therefore, AFM can scan the boundary between sapphire and $WS_2$ monolayer still remaining on the pad. b) AFM direct image taken in tapping mode: one can appreciate sapphire in dark and $WS_2$ still covered with a thin PR layer in yellow. c) Height profile drawn along the blue line of the previous picture. One can appreciate a certain smoothness in the sapphire surface, while the "$WS_2$" surface appears quite rough, confirming the hypothesis of a residual PR that has developed irregularly.

A deep inspection with an AFM could indeed be quite informative on the morphology of the sample and reveal things that cannot be perceived with an optical microscope. Atomic Force Microscopy is a high-resolution technique that allows to explore and study the topographic surface of nanometric objects, such as thin films of metal, nanoparticles or, potentially, biomolecules. The key idea of AFM is to use the sensitivity of STM (Scanning Tunnel Microscopy) to measure the rise and fall of a tip mounted on a cantilever when scans a surface; not only this acknowledges on the topography, but makes it also possible to deduct some interesting spectrography. Thanks to some computer control implementation, the tip-substrate force is indeed the central quantity that provides the user with amplitude, phase, topography and

many more sample analyses. AFM can adopt different measurement strategies, based on the operational contact between tip and substrate. We analyze the thin TMDC film in tapping mode, so called because the tip lightly "taps" on the sample surface during scanning, contacting the surface only at the bottom of its swing. The amplitude of oscillation typically ranges from 20 nm to 100 nm and the cantilever oscillates close to its resonance frequency. The main advantages of this operational mode consist in the elimination of almost any lateral force and thus higher lateral resolution and less damage of the soft sample due to lower forces. The working point is chosen automatically by the software, which autotunes the cantilever frequency. It is necessary to maintain this point fixed during the scanning process, not to alter measurements. To this purpose, the AFM implements a feedback loop circuit whose control parameter (derivative, integral, proportional) is suggested directly by the software. Further optical controls have been implemented through the use of lasers, which also increase the resolution power.

The film height is expected to be approximately 1.1 nm, as a result of the typical 0.7 nm plus additional 0.4 nm of vdW distance between surface and microscope tip. However, as the height profile extracted in *Fig.5.11c* shows, the measured film height is 4.33 nm, resulting from the difference of the average heights calculated in between the red and the black dotted lines, which have been placed appositely on the nude sapphire and "TMDC" profile respectively. The measured height is 4 times larger than the expected one. This confirms the initial guess of the parasitic PR unremoved by developer solution, but unfortunately it also forces the research to a change of direction. This is indeed the second piece of evidence accusing top-contact of the absence of current in the channel, therefore it suggests to adopt bottom contacts for the next fabrication. As described in the previous section, bottom contacts would not harm the metal-semiconductor junction with the use of chemicals and they would thus produce clean contacts between the two materials.

In conclusion, the Hall bar geometry was chosen for its precision in determining key electrical parameters such as electron mobility and resistivity. Despite the accuracy of this method, the lack of current in the fabricated devices highlights significant issues in the fabrication process, especially concerning the quality of the metal-semiconductor interface. The measured characteristics suggest that contact resistance and potential fabrication errors, rather than intrinsic material properties, are responsible for the poor device performance. Future work must focus on addressing these challenges, optimizing the fabrication steps, and improving contact quality to ensure successful device functionality.

# Chapter 6

# Conclusions

This thesis is aimed to fabricate and characterize $WS_2$-based field effect transistors by making use of photolithography and reactive ion etching. In particular, the research investigates the variation of metal contact quality as a function of the channel thickness and develops a comparison with the fabrication of monolayer-$WS_2$-based devices.

The analysis revealed that the choice of bottom metal contacts is feasible in the realization of working devices, while top-contacts subject the monolayer to an excessive chemical treatment. Moreover, this suggests that bulk materials are more robust against chemicals than monolayers, which are easily peeled off due to their polarity. The low mobility and on/off ratio measured are then informative on the quality of the contact interface, while the nonlinearity of the output curves is consistent with the choice of gold as contact metal.

These findings contribute to a deeper understanding of $WS_2$ electrical properties, providing evidence that can be applied to improve TMDCs transistors scalability and general performances. Their deep characterization could indeed pave the way towards the realization of reliable ohmic devices to overcome silicon performances and go beyond Moore's law.

While this study provides important contributions to the field, it is not without limitations. The reliance on photolithography has oriented the research towards the fabrication of large channel devices, which come along with more scattering centers and lower currents. In addition, the absence of a well-defined transferring technique prevented the deposition of monolayers on optimal substrates that would have ensured the proper functioning of the devices.

The findings suggest that researchers and device manufacturers should optimize the fabrication process to reduce the impact of chemicals on the channel material and to improve the contact junction coupling, perhaps by changing the metal at the interface. Further studies are needed to better understand the physics of Schottky barriers and produce clean metal contacts, which are pivotal to bring TMDC-based transistors to market.

Overall, this research highlights strengths and criticalities of $WS_2$ transistor fabrication and sets the stage for future studies that could lead to more performant transistor technologies.

# *Acknowledgements*

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# Appendix A

# Clean room technology

Most of the hands-on experience conducted in the six-month duration of this internship took place in special laboratories where the concentration of airborne particles is controlled to specific levels. Air filtration and control over particle contaminations are two of the most important characteristics of cleanrooms, the labs where microchip fabrication and characterization take place.

The reason why microchips need to be fabricated in a controlled environment is simple: any physical or chemical contamination can seriously harm the functionalities of any microscopical device, especially if their conductive channel is made by 2D monolayers, which are particularly delicate and highly sensitive to mechanical damage. Generally speaking, however, contaminations can not only ruin devices, leading to higher costs and lower profit per chip, but also “poison” the equipment necessary to their fabrication, not to mention the human health risk that they can introduce. It is thus essential to protect the fabrication line from any contamination, either particulates like organic or inorganic dust, or films like residues deriving from inadequate rinsing or developing. Unfortunately, the sources of contamination can be numerous: even if machines and production processes can be appointed as the cause of chemical releases and dust produced by abrasion or aging plastics, humans still remain the main cause of cleanroom contaminations. Human body, indeed, continuously exfoliates skin, replaces hairs and widespreads make-ups or perfumes; it is thus necessary to wear adequate clothing both for protecting ourselves and shielding the fabrication line from contaminations coming from our own bodies. The use of face-masks, bouffant cups and nitrile or vinyl gloves is thus mandatory in all level cleanrooms; then, higher level cleanrooms must also require their operators to wear lab suits, goggles and special footwear. Nevertheless, these precautions are still not 100% sufficient; it has been estimated that a fully “shielded” human operator is still shedding 100.000 particles per minute while seated and 5 millions particles per minute walking.[85] For this reason a sophisticated air flow system is installed in any cleanroom, as stated

in the first widely accepted cleanroom standard “*Standard Functional Criteria for The Design and Operation of Clean Rooms*” published in early 1961 by the US Air Force.[86] The laminar flow is the key factor to reduce environmental particle contamination; air is flowing from the ceiling to the floor in controlled fluxes and then blown in special filters called HEPA. High Efficient Particulate Air (HEPA) filters exploit glass fiber to retain 99.97% of incident particles with diameter of 0.3 $\mu$m or larger. More sophisticated filters (Ultra-Low Particle Air, ULPA) may achieve 99.999% minimum performance level with a 0.3 $\mu$m efficiency.
Another way to limit external contamination in cleanrooms is modulating the pressure inside, setting it to a value higher than the external one, in order to force dust out of the environment and never into it. Moreover, doors always open inward, so that pressure can close them shut, if left open. However, pressure is not the only controlled parameter in these special laboratories: temperature is also fixed to $20-22°$C, as well as humidity which is blocked at 50% and constantly monitored. Controlling these last two parameters in a tropical climate like Singapore's may be costly in terms of energy: external air must be cooled down to 13° C to reduce humidity and then heated up again to the desired temperature for distribution. This is done through the Air Conditioning and Mechanical Ventilation (ACMV) system, which operates with a complex network of fume hoods departing from each cleanroom.
In addition to air setting, a constant vigilant monitoring system of sensors must be present throughout the entire volume of the cleanroom; those electronic devices are indeed essential to monitor air quality and detect any gas leakage. Gas detection sweeps from common inert gasses like argon or nitrogen, to more hazardous gasses like fluorine, hydrogen, silane and methane.[87] Even illumination is carefully controlled: as one may appreciate from *Fig.A.1b*, most environments host yellow light to protect photosensitive materials, which would be harmed by the blue components of the beams.

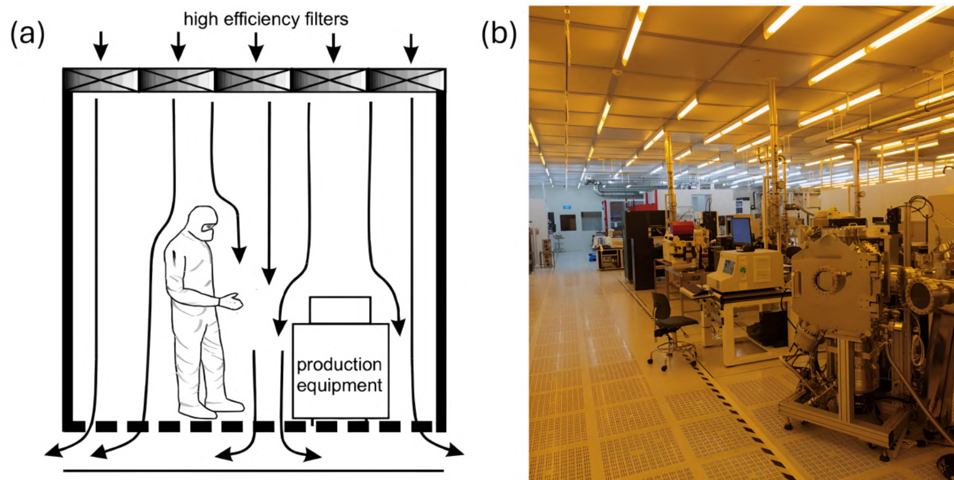


*Figure A.1:* a) Schematics of the cleanroom laminar airflow flowing from the ceiling to the floor. HEPA filters are also highlighted.[86] b) Picture taken from A*STAR C5 cleanroom.

One crucial aspect of the cleanroom environment is the floor. The latter is indeed raised from the ground to facilitate the creation of a laminar air flow

and maintain a positive pressure. Moreover, the floor allows concealment of cables and, if raised, enables easy maintenance and simplified cleaning. Finally, the raised floor helps dissipate heat and control the room temperature. *Fig.A.1a* shows a simplified scheme of cleanroom environment and its airflow coming from HEPA filters in the ceiling and directed into the raised floor.

Finally, cleanrooms are classified according to the number and size of particles permitted per volume air. Even if different classifications exist, the most common ones are the ISO cleanroom standards ( $ISO14644-1$)[88] and the Federal standard 209E ($FS209E$).[89] The latter was published by NASA in the field of space exploration in 1992 and its scope was to define classes of air cleanliness based on specified concentrations of airborne particles larger than 0.5 $\mu$m:

- Class 1: 1 particle per cubic foot.
- Class 10: 10 particles per cubic foot.
- Class 100: 100 particles per cubic foot.
- Class 1,000: 1,000 particles per cubic foot.
- Class 10,000: 10,000 particles per cubic foot.
- Class 100,000: 100,000 particles per cubic foot

On the other hand, ISO classification systems was published seven years after and provides a more elaborate cleanroom classification based on requirements for counts associated with non-viable particulates of different diameters:

| **ISO classification number (N)** | **Maximum concentration limits (particles m$^3$ of air) for particles equal to and larger than the considered sizes down below** | | | | | |
|---|---|---|---|---|---|---|
| | **0.1 $\mu$m** | **0.2 $\mu$m** | **0.3 $\mu$m** | **0.5 $\mu$m** | **1 $\mu$m** | **5 $\mu$m** |
| ISO Class 1 | 10 | 2 | | | | |
| ISO Class 2 | 100 | 24 | 10 | 4 | | |
| ISO Class 3 | 1000 | 237 | 102 | 35 | 8 | |
| ISO Class 4 | 10000 | 2370 | 1020 | 352 | 83 | |
| ISO Class 5 | 100000 | 23700 | 10200 | 3520 | 832 | 29 |
| ISO Class 6 | 1000000 | 237000 | 102000 | 35200 | 8320 | 293 |
| ISO Class 7 | | | | 352000 | 83200 | 2930 |
| ISO Class 8 | | | | 3520000 | 832000 | 29300 |
| ISO Class 9 | | | | 35200000 | 8320000 | 293000 |

*Table A.1:* ISO classification system

To conclude, despite cleanroom technology being developed more than 30 years ago, it is still the most actual protocol allowing upward and innovative scientific research. Working in a clean and safe environment is the key priority of microelectronics research and industry, thus the development of cutting-edge cleanrooms is essential to perfectioning devices fabrication and, ultimately, scientific progress itself.

# Appendix B

# Chemical Vapor Deposition

In the thesis project discussed a wide use of pre-grown samples of $WS_2$ on sapphire substrate is made. It is thus worth spending a few words on the engineering process that lies behind the growth of the 2D material that has been so widely exploited. Chemical Vapor Deposition (CVD) is the name of such a process. It involves chemical reactions occurring at the vapor phase and it is generally used to produce high-purity and high-performance solid materials, but in the last decade it has been optimized to grow 2D transition metal dichalcogenides because of their higher demand in the research environment.

The rough procedure consists of four main steps: vapor-phase transport of precursor species; adsorption and decomposition of precursors on the chosen substrate; nucleation of the crystal and final growth. The last two steps have been widely studied and perfected in the past forty years, since they come from a widely established theory from the 1980s asserting that 2D materials often align with the crystallographic orientation of the substrate even if a large lattice mismatch exists. This process, called vdW epitaxy, results in a heterostructure free of epitaxial strain, having a well-structured layer of 2D material on top.

Despite two types of CVD methods existing, as *Fig.B.1c* shows, the gas-source process shows a net advantage in the growth of TMDC with respect to the solid-source CVD. The chemical precursors involved in the reactions to produce a high-purity TMDC are better harvested in their vapor phase. The choice of these chemicals is the key to the success of the CVD, which necessitates both a volatile metal and a chalcogen precursor. Both of them can be introduced in the chamber through a mass-flow controller or bubbled using a carrier gas (usually Ar and $H_2$). $Ge_4Se_9$, $Bi_2O_2Se$ and diethyl sulfide (DES-$(C_2H_5)_2S$) are normally used as chalcogen precursors. The last is a popular choice because of its minimal toxicity and suitable volatility; nevertheless, it can introduce carbon defects, inhibiting smooth lateral growth[90]. $Mo(CO)_6$

and $W(CO)_6$ are, instead, common metal sources. They are the reason why the process takes often the name of Metal Organic CVD (MOCVD)[91][92]; the emphasis on the choice of organic compounds is highlighted because they offer good control over the partial pressure of reactants, so that a better nucleation can be achieved and, possibly, large-scale monolayers produced.
The reaction takes place because of temperature modulation operated by the machine, which can contain a hot- or cold-wall reactor, where only the substrate undergoes heating [90][93]. The reaction consists of the decomposition of the reactants into their constituent ions and their successive recomposition, which starts the nucleation phase, depicted in *Fig.B.1b*. Finally, the nucleation centers start a slow expansion which terminates when all triangles have merged together forming a uniform layer of 2D material. At this point the growth phase is terminated and the sample is ready for the fabrication process.

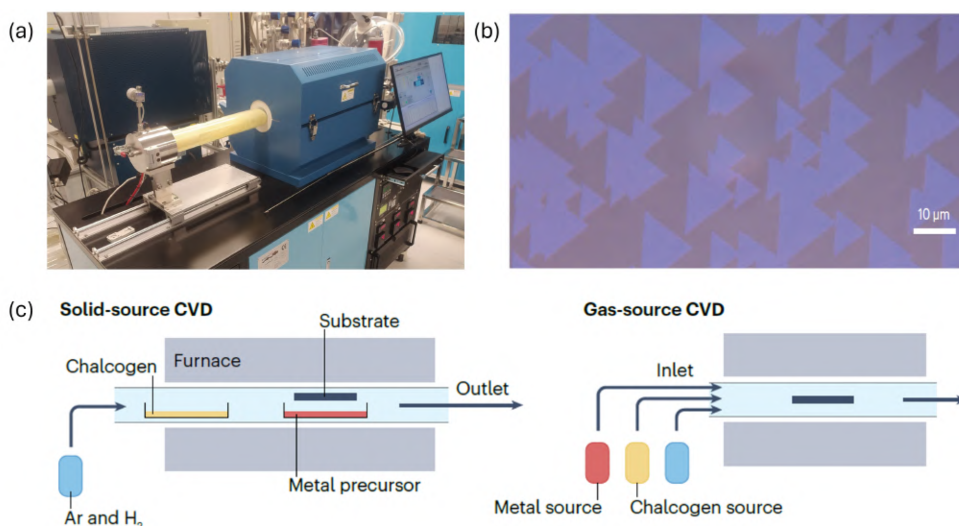


*Figure B.1:* a) Picture of the CVD furnace from A*STAR K4 cleanroom. b) Optical microscope image of the nucleation of $MoS_2$.[75] c) Schematics of the CVD process inside the machine furnace.[75]

One other important factor to consider while optimizing the CVD process is the control of point-defects. Indeed, zero-dimensional ($0D$) defects may deteriorate the quality of the 2D layer both from an electrical and optical point of view. Fortunately, some precautions can be taken to limit the creation of these defects.
One first typology of point-defects is chalcogen vacancies. To reduce their density it is sufficient to modify the kinetics of the chalconization process, so that the reaction occurs via a more energetically favorable route. By heating up to high temperatures, chalcogen monomers with higher reactivity are produced from the plate and enable a lower defect-density TMDC. A second type of defect is represented by oxygen-substituted sulfur vacancies. The exposure to $O_2$-rich atmosphere can indeed enhance the substitution of sulfur atoms with oxygen. To prevent this phenomenon from happening, a common technique to adopt is hydroxide vapor-phase deposition. Essentially, instead of using Ar and $H_2$ as carrier gas for pure tungsten, one uses simple water-vapor. In fact, W-OH bond has a lower kinetic barrier than W-O and can

provide easier dissociation and favor sulfurization. $WS_2$ film that have undergone this treatment usually show high on-current and better electronic performances.[94]

Finally, one would like to check the quality of the grown 2D material and make sure that the defect density stays below the wanted threshold. There exist different solutions to complete this task. The most common one is scanning tunneling microscopy (STM), which can provide atomic imaging of selected areas of the sample, thus producing a statistics of pointwise checks to calculate the average defect density.
A valid alternative to STM is photoluminescence (PL). TMDCs are in fact known for their optical properties and a PL test can tell immediately the density of defects, in particular sulfur vacancies. It is sufficient to analyze the PL spectrum and measure intensity and position of the peaks appearing. Usually the largest rightmost peak is located around 1.79 eV and refers to pristine $WS_2$, whose intensity can tell the difference between mono- and bilayers; while a second smaller peak around 1.7 eV refers to the sulfur vacancies density, whose value can be inferred by measuring the peak's intensity.
Other techniques, like X-ray photoelectron spectroscopy (XPS) and Raman spectroscopy, can be exploited to check the material's quality. None of them, however, allows for an immediate and simple detection of defect density like STM and PL.

# Appendix C

# Dry tranferring process of $WS_2$ monolayers

This appendix details the dry transferring process used to move $WS_2$ monolayers from a sapphire substrate to a new $SiO_2$ substrate. The process is carried out in a dry environment by making use of polypropylene carbonate (PPC), which serves as a carrier vector, and polydimethylsiloxane (PDMS), used as a solid transfer stamp. While the first is a liquid polymer that has to be spin-coated on the sapphire sample like a normal photoresist, the second is a solid organic polymer that is shaped like a stamp, attached to a glass slide and then used to pick up the monolayer covered with PPC, with which it has high adhesion. The entire procedure is sketched in *Fig.C.1a*. *Fig.C.1b*, instead, shows its crucial step, when the slide with PDMS is pressed over the $WS_2$ monolayer on top of sapphire to induce a strong adhesion between the stamp and the PPC covering the monolayer. The slide is then lifted and moved onto the new $SiO_2$ substrate, where it is pressed again and $WS_2$ released. A simple rinsing in acetone or chloroformium is enough to get rid of excess PPC. Force and pressure must be controlled at any time in order to prevent film damage; the film is indeed very delicate and the minimum excess of strength could break it severely, as shown in *Fig.C.1c*, where the image of the first transferring trial is displayed.

With some additional training the operator can master the entire transferring technique. Once fully achieved, it can effectively improve the device performances: the better adhesion between $SiO_2$ and $WS_2$, indeed, would prevent any peel off from happening after rinsing in DI water and thus guarantee a sensible reduction of film damaging during fabrication steps. Nevertheless, a trade-off exists between fabrication and transferring damages, which cannot be totally avoided because the procedure is done manually and not automatically. For such a reason we cannot reach the film quality of the devices presented by Kwon et al.[46], who exploit the use of a semi-automatic transfer machine, but we are confident enough to achieve an improvement.

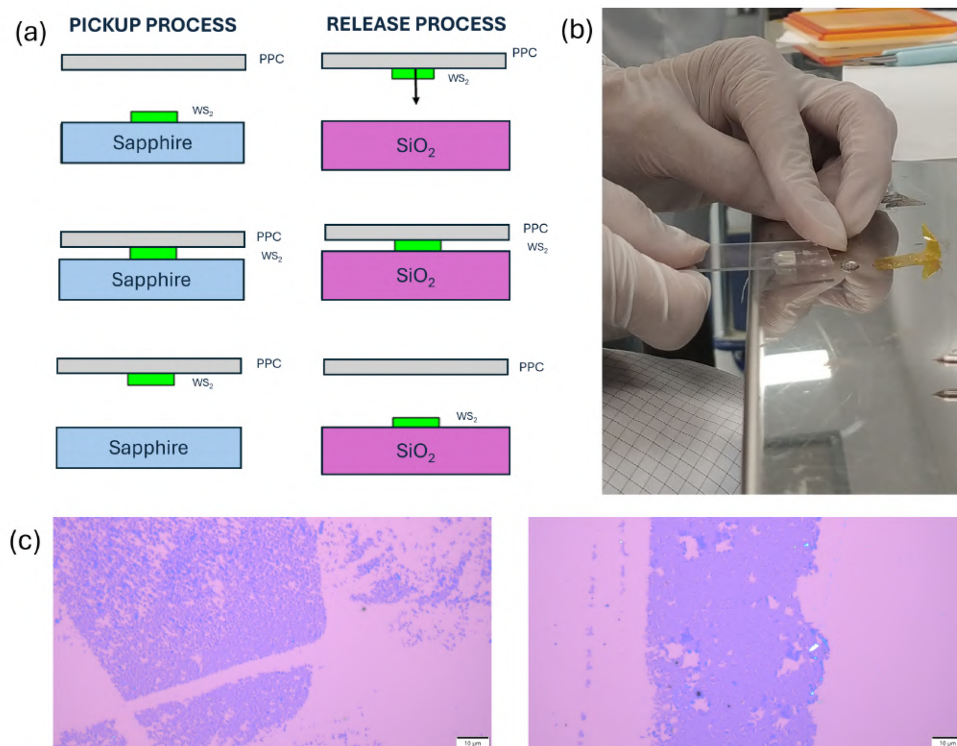


*Figure C.1:* a) Brief schematics of dry transferring technique: by making use of PPC the operator can move manually the monolayer from sapphire to $SiO_2$.[95] b) Picture of the crucial step in transferring technique: the operator is pressing the slide with PDMS on the sapphire sample with $WS_2$. The monolayer is expected to peel off the substrate thanks to water hydrophilic effect and move to the sticky PDMS, which serves as transportation vector towards $SiO_2$. c) Optical microscope images of the transferred $WS_2$ monolayer on $SiO_2$: the process has severely damaged the film, which shows highly discontinuous regions.

# Appendix D

# Complete set of electrical measurements

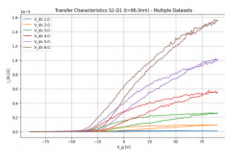
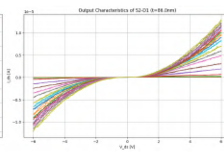

*Figure D.1:* S2D1

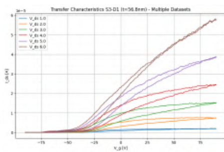
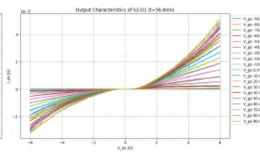

*Figure D.2:* S3D1

*Figure D.3:* S3D2

*Figure D.4:* S4D1

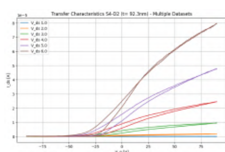
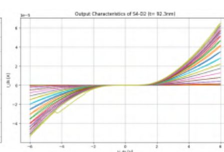

*Figure D.5:* S4D2

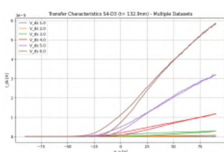
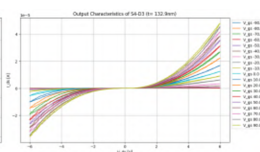

*Figure D.6:* S4D3

*Figure D.7:* S10D2

*Figure D.8:* S10D3

*Figure D.9:* Transfer and output curves of fabricated devices

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