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NANOTECHNOLOGIES FOR ICTs

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Design of radiation-tolerant analog blocks for the Control Unit of DCDC converters in High Energy Physics experiments

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MASTER'S DEGREE THESIS

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Abstract

This thesis presents the development and implementation of critical analog blocks for the control unit of DC-DC converters, designed in a commercial high-voltage 180nm technology, to be used in the upcoming High-Luminosity upgrade of the Large Hadron Collider (LHC) at CERN. Scheduled for completion by the end of the decade, this upgrade aims to achieve instantaneous luminosities 5 to 7.5 times higher than the LHC's nominal value, thereby enabling experiments to collect more data and further increase their discovery potential.
In this context, in order to properly supply the front-end circuits while limiting power losses, DC-DC converters are located close to the collision points, in a harsh environment characterized by high levels of radiations (up to 200 Mrad) and high magnetic field (up to 4T). Off-the-shelf components are inadequate to operate in such conditions, thus requiring custom ASICs to be developed.
Specifically, the focus of this thesis is on designing radiation-resistant integrated circuits for the control unit of a 48V to 5V DC-DC converter: an innovative dual-edge Pulse Width Modulator (PWM) with improved dynamic performance over conventional solutions, the control logic of a Dead Time Manager (DTM), a high-voltage comparator for an innovative resistive level shifter, and gate drivers for the power stage. Ensuring the reliable and correct operation of these designed blocks under the extreme conditions encountered in high-energy physics experiments has presented a unique and stimulating challenge, requiring the extensive application of hardening by design techniques.

Sommario

In questa tesi viene presentato lo sviluppo e l'implementazione di blocchi analogici critici per l'unità di controllo dei convertitori DC-DC, progettati in una tecnologia commerciale ad alta tensione a 180 nm, da utilizzare nel prossimo aggiornamento del Large Hadron Collider (LHC) del CERN. Previsto entro la fine del decennio, questo aggiornamento mira a raggiungere luminosità istantanee da 5 a 7,5 volte superiori al valore nominale dell'attuale configurazione del LHC, consentendo così agli esperimenti di raccogliere più dati e aumentare ulteriormente il loro potenziale di scoperta. In un simile contesto, per alimentare correttamente i circuiti del front-end limitando allo stesso tempo le perdite, convertitori DC-DC sono situati in prossimità dei punti di collisione, in un ambiente caratterizzato da alti livelli di radiazioni (fino a 200 Mrad) e un elevato campo magnetico (fino a 4T). I componenti disponibili sul mercato sono inadeguati per operare in tali condizioni, richiedendo dunque lo sviluppo di ASIC personalizzati. A tal proposito, l'obiettivo di questa tesi è la progettazione di circuiti integrati resistenti alle radiazioni da utilizzare nell'unità di controllo di un convertitore DC-DC da 48 V a 5 V: un Dual-edge Pulse Width Modulator (PWM) con prestazioni dinamiche migliori rispetto alle soluzioni convenzionali, la logica di controllo del Dead Time Manager (DTM), un comparatore per un innovativo level-shifter resistivo e i driver dei gate per lo stadio di potenza. Garantire l'affidabilità e il corretto funzionamento di questi blocchi nelle condizioni estreme che si trovano negli esperimenti di fisica delle alte energie ha rappresentato una sfida unica e stimolante, che ha richiesto l'applicazione estensiva di tecniche di tempra per progettazione.

Résumé

Cette thèse présente le développement et l'implémentation de blocs analogiques critiques pour l'unité de contrôle des convertisseurs DC-DC, conçus dans une technologie commerciale à haute tension de 180 nm, qui seront utilisés dans la prochaine mise à niveau à haute luminosité du Grand collisionneur de hadrons (LHC) au CERN. Cette mise à niveau, qui devrait être achevée d'ici la fin de la décennie, vise à atteindre des luminosités instantanées 5 à 7,5 fois supérieures à la valeur nominale du LHC, ce qui permettra aux expériences de collecter davantage de données et d'accroître encore leur potentiel de découverte. Dans ce contexte, afin d'alimenter correctement les circuits frontaux tout en limitant les pertes de puissance, les convertisseurs DC-DC sont situés à proximité des points de collision, dans un environnement difficile caractérisé par des niveaux élevés de radiations (jusqu'à 200 Mrad) et un champ magnétique important (jusqu'à 4T). Les composants disponibles sur le marché sont inadéquats pour fonctionner dans de telles conditions, ce qui nécessite le développement d'ASIC personnalisés. Plus précisément, cette thèse se concentre sur la conception de trois circuits analogiques résistants aux radiations pour l'unité de contrôle d'un convertisseur DC-DC de 48V à 5V : un nouveau modulateur de largeur d'impulsion (PWM) à double front avec une performance dynamique améliorée par rapport aux solutions conventionnelles, un comparateur haute tension pour un décaleur de niveau résistif innovant, et des pilotes de grille pour l'étage de puissance. Garantir le fonctionnement fiable et correct de ces blocs dans les conditions extrêmes rencontrées dans les expériences de physique des hautes énergies a représenté un défi unique et stimulant, nécessitant l'application extensive de techniques de durcissement par conception.

Acknowledgments

At the conclusion of this intense and fulfilling journey, I would like to take a moment to acknowledge the people who have supported and inspired me throughout these intense and challenging years.
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I would also like to extend my thanks to the entire DCDC team and the broader CERN MicroElectronics section for the stimulating and supportive environment they welcomed me in. I learned so much from being part of such a dedicated group.
I am also grateful to all my fellow Nanotech colleagues who accompanied me during my long and challenging studies across Torino, Grenoble, Lausanne and Geneva. I wish them all the success and realization they deserve.
I cannot forget to thank my friends in Caserta, my hometown. Despite the distance, their enduring friendship have been a source of strength for me. Knowing I can always count on them has made this journey more meaningful and pleasant.
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Chapter 1

Introduction

Conducted within the MicroElectronics section of the Electronic System for Experiments group at CERN, this master's thesis project focuses on designing radiation-resistant analog blocks for the control circuit of a 48V to 5V DC-DC converter which will be integrated in the power distribution scheme of the upcoming high-luminosity upgrade of the LHC.
This introductory chapter details the context and motivations for this project, starting with an overview of CERN's activities and a description of the power distribution scheme used to supply the experiments. Finally, an overview of the working principles of Switched Mode Power Supplies (SMPS) and DC-DC converters is provided.

1.1 CERN

CERN is the European Organization for Nuclear Research. Established in 1954, its mission is to advance the boundaries of human knowledge by investigating the fundamental components of matter and the forces that govern their interactions.
In order to serve this mission, a complex system of particle accelerators (Figure 1.1) is exploited to boost beams of particles to high energies before they are made to collide with each other or with stationary targets. Detectors then capture and analyze the byproducts of these collisions, measuring various parameters such as position, velocity, charge, energy, and mass of the resultant particles.

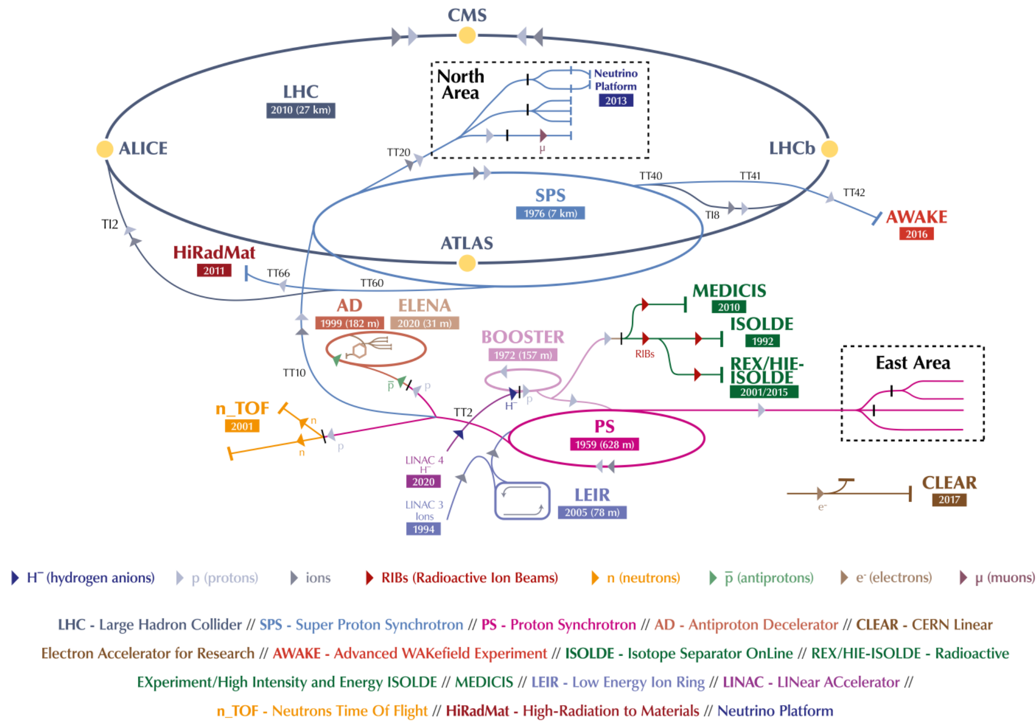


Figure 1.1: CERN's accelerator complex

Among all the accelerators, CERN hosts the Large Hadron Collider (LHC), which is the biggest and most powerful particle accelerator in the world, featuring a 27-kilometer circular tunnel where two particle beams (protons or ions) travel in opposite directions within an ultra-high vacuum. These beams are accelerated to near the speed of light by superconducting magnets and are made to collide at four points along the ring, each housing one of the primary LHC experiments: ALICE, ATLAS, CMS, and LHCb. Each of these experiments involves its own set of detection equipment and supporting infrastructure.
The high-energy collisions (up to 13 Tev) and associated beam losses result in significant radiation levels, thus requiring the electronic systems used to be robust against radiation and capable of functioning within high magnetic fields.

Scheduled for the *long shutdown 4* (2026-2029), the High-Luminosity LHC (HL-LHC) upgrade aim to dramatically increase the rate of particle collisions,

thereby expanding the volume of data collected and the discovery potential of LHC's experiments. These upgrades, however, will require electronics that can withstand even higher radiation levels while minimizing material usage to preserve collection efficiency.[1] [2]

1.2 Power distribution in LHC

If on one side the High-Luminosity upgrade will significantly increase data collection, it will also come at the cost of an increased power consumption of the front-end electronics, which means an efficient power distribution scheme is required.
The simplest and most straightforward solution would be to deliver power through long cables that carry all the current needed from the power supplies, shielded from radiations, to the front-end, control, and communication electronics. This solution, however, comes with some disadvantages that are not acceptable considered the foreseen increase in LHC power demand. First, significant power is lost in the cables due to Joule heating ($P_{\text{loss}} = R_{\text{cable}} I^2$) which means a large and power hungry cooling system is needed. Additionally, this method often fails to provide a stable voltage to the detector modules. Ultimately, the extensive use of large cables (to reduce resistance) and cooling infrastructure conflicts with the need to minimize material within the detectors, which is crucial for preserving their performance.
To solve these problems, a power distribution scheme based on Point of Load (PoL) DC-DC converters is being developed. This allows to distribute power at a higher voltage stepping it down close to where it is needed, so to reduce the current in the cables, minimizing power losses and allowing for thinner cables. In this way both power delivery efficiency and material minimization requirements are met.

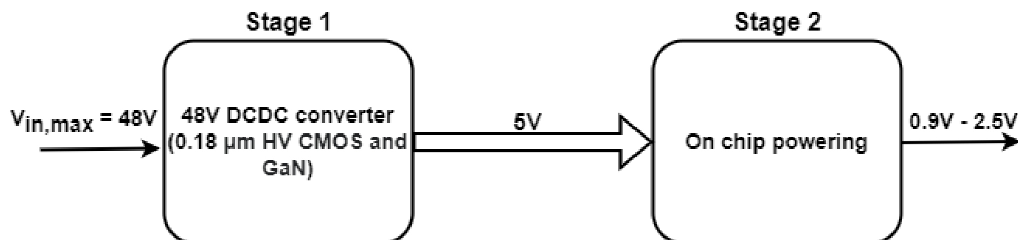


Figure 1.2: Proposed power distribution scheme.

Figure 1.2 illustrates the proposed power distribution scheme based on a two-stage conversion process that generates the required voltage levels. The first stage features a 48V to 5V DC-DC converter, for which the controller's blocks, detailed in Chapter 3, have been designed. Although the exact topology of this converter is still under discussion, its control unit is intended to be "general purpose" and adaptable to various converter topologies (such as buck or Berkeley's series capacitor buck converter) and switch technologies (including integrated high-voltage CMOS or external GaN switches). The second-stage converters then produce the specific voltages needed by the supplied circuits.

1.3 DC-DC converters

Switching converters are key components in the field of power electronics that allow to process an input power into an output power as specified by a controller (Figure 1.3). A DC-DC converter is a type of switching converter that transforms a direct current input into a direct current output with a different voltage level, which can be either higher or lower, eventually with opposite polarity or electrically isolated input and output grounds. The controller block, which is the focus of this thesis, is an essential component of any power processing system. It ensures a well-regulated output voltage, even in presence of input voltage fluctuations or changes in load current. [3]

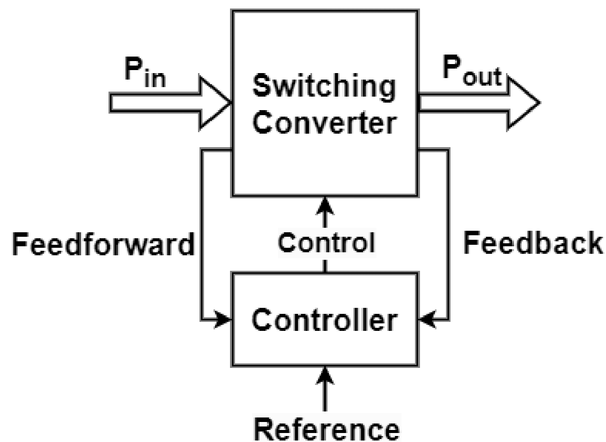


Figure 1.3: Switching converter basic scheme.

Efficiency is a key parameter when dealing with power processing.

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} \tag{1.1}$$

The difference between the input power and the output power (P_{loss}) is mostly lost into heat that needs to be dissipated by an opportunely sized cooling system.

$$P_{\text{loss}} = P_{\text{in}} - P_{\text{out}} \tag{1.2}$$

It is useful to define a quantity Q that relates the power lost in the converter and its output power:

$$Q = \frac{P_{\text{out}}}{P_{\text{loss}}} = \frac{\eta}{1-\eta} \tag{1.3}$$

This parameter serves as a quality measure for power converters, since, in most applications, the maximum output power is constrained by the cooling system's capacity to dissipate the heat associated to power losses. If significant power is lost in the circuit then a bigger and more capable cooling system becomes necessary.
Unfortunately, the previously discussed material minimization requirement in HEP experiments doesn't allow for bulky cooling systems, which would be detrimental for the detector's effectiveness. Therefore, highly efficient converters are required.

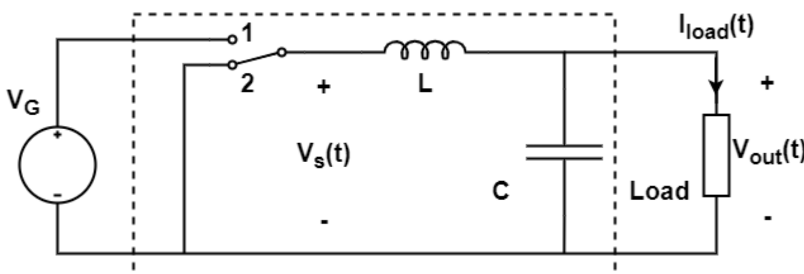


Figure 1.4: Basic scheme of a *buck* converter.

High conversion efficiencies can be achieved using a *single-pole double-throw* (SPDT) switch that periodically toggles between two nodes with different voltages. This produces a rectangular waveform V_s with a frequency f_{sw}

and a duty cycle D. By processing this square wave through energy-storing components, such as inductors and capacitors, a DC output voltage can be obtained. Since the presented scheme uses only (ideally) lossless components, conversion efficiencies approaching 100% can be achieved.
Based on the achievable conversion ratio $M(D) = \frac{V_{\text{out}}}{V_{\text{in}}}$, three main types of switching DC-DC converters can be distinguished:

- *buck* converters: $0 \leq M(D) \leq 1$;
- *boost* converters: $M(D) \geq 1$;
- *buck-boost* converters: $M(D) \leq 0$;

Figure 1.3 shows the basic scheme of a buck converter, which, in the context of this thesis, is the simplest converter topology that can be used in combination with the developed controller to step down the input voltage of 48V to an output voltage of 5V.
When the switch is in position 1, the voltage $v_s(t)$ equals the input voltage V_G; when the switch is in position 2, $v_s(t)$ becomes zero. Therefore, $v_s(t)$ forms a square wave signal with a frequency of f_{sw} and a duty cycle $D \in [0, 1]$. Fourier analysis tells us that the DC component of $v_s(t)$ is given by its average value:

$$V_{\text{out}} = \frac{1}{T_{\text{sw}}} \int_0^{T_{\text{sw}}} v_s(t)\, dt = \frac{1}{T_{\text{sw}}} (V_G T_{\text{sw}} D) = D V_G \tag{1.4}$$

An LC low-pass filter is then employed to isolate the DC component of $v_s(t)$, effectively filtering out the switching frequency and its harmonic components. To accomplish this, the filter's cutoff frequency ($f_{\text{cutoff}} = \frac{1}{2\pi\sqrt{LC}}$) must be much lower than f_{sw}.
In this way the output voltage v_{out}(t) is basically equal to the DC component of $v_s(t)$:

$$v_{\text{out}}(t) = D V_G \tag{1.5}$$

This result is valid to the extent that ideal and lossless components are used. In reality things are more complicated: the output voltage of real converters, for example, is not a perfect DC signal, but presents a small ripple caused by the incomplete attenuation of the switching harmonics by the low-pass filter. The need to minimize this ripple typically imposes limitations on the switching frequency and/or the inductance value (see *Part 1: Converters in*

Equilibrium of [3]). Moreover, the conversion ratio is never exactly equal to the duty cycle, as calculated in the earlier simplified model, due to various power losses that can occur throughout the circuit.
Setting aside these complications for a moment, the *toy model* presented here helps understanding the fundamental working principles of *switching converters* and their advantages in terms of efficiency for power distribution solutions.

Chapter 2

Radiation effects on CMOS technology and hardening techniques

This second chapter, based on Giovanni Anelli's studies [4], is dedicated to explaining the detrimental effects of radiation on MOS devices. First, an overview of the various mechanisms by which radiation degrades the electrical parameters of MOS devices will be provided. Following this, commonly adopted strategies to mitigate these effects will be presented.

2.1 Effects of ionizing radiation on MOS devices

The effect of radiation on solid matter depends on the nature of the incoming particle (its kinetic energy, charge, and mass) as well as the characteristics of the target material (atomic number, density, and mass). Charged particles like protons, ions, and electrons mainly interact through Coulomb force, whereas neutral particles act through different mechanisms: neutrons can cause nuclear reactions or elastic/inelastic collisions depending on their energy; photons can lead to photoelectric effect, Compton effect and to the creation of electron-hole pairs.
In general, the effects of radiation on solid materials, whether from charged or neutral particles, can be categorized into ionization effects and nuclear displacement:

- Ionization effects involve the creation of electron-hole pairs in a semiconductor or insulator due to radiation exposure, with the number of pairs produced being related to the energy deposited in the material by the incoming particles. This amount is typically related to the Linear Energy Transfer (LET) which quantifies the energy released by a particle per unit distance within the target material, measured in J·m^2/kg or in MeV·cm^2/mg.

$$LET = \frac{1}{\rho}\frac{dE}{dx} \tag{2.1}$$

  where ρ is the density of the target material and dE/dx is the mean energy released to the material per unit of length.

  The cumulative ionization effect is referred to as the Total Ionizing Dose (TID), which quantifies the total energy absorbed per unit mass of the target material, measured in rads (1 rad = 0.01 J/kg). On the other hand, a single, highly energetic particle can generate enough electron-hole pairs to disrupt one or more devices, potentially causing temporary or permanent errors in integrated circuits; in this case we talk about Single Event Effects (SEE).

- Nuclear displacement occurs due to the non-ionizing energy loss of impinging particles, resulting in the formation of defects in the crystal structure known as Frenkel pairs, which consist of a vacancy and a nearby interstitial defect. The cumulative damage caused by this process is known as Displacement Damage (DD), and it depends on the *fluence* of the impinging particles, which refers to the total number of particles striking the material per unit area. In semiconductors, DD can result in mid-gap defect states or changes in doping levels, however, usually DD does not significantly impact electrical performance of MOSFETs, as a very high number of Frenkel pairs would be required to affect the typically high doping levels. In Laterally-Diffused MOS transistors (LDMOS) used for high-voltage applications, displacement damage can be particularly detrimental. These devices incorporate a lightly doped drift region near the drain terminal to achieve a high breakdown voltage, as this low-doping region can sustain most of the drain-source voltage, thereby limiting the peak electric field within the bulk of the semiconductor. In LDMOS transistors, variations in doping

density caused by displacement damage lead to an increased channel resistivity that primarily impacts the slope of the Id-Vd curve in the linear region and decreases the transistor's Ion [5].

In MOSFETs, when considering the gate or the substrate, the electron-hole pairs generated by ionizing radiation rapidly recombine. Conversely, in silicon dioxide, an electric field can separate a significant fraction of these electron-hole pairs, making recombination rare. Electrons in SiO_2, due to their higher mobility, quickly drift out of the insulator, while holes migrate slowly towards the $Si-SiO_2$ interface (Figure 2.1). Near this interface, holes can become trapped into *trap-states* associated with crystalline defects, leading to an accumulation of positive charge. Even worse, radiation induces the creation of more lattice defects and *trap-states* at the $Si - SiO_2$ interface thus emphasizing this process.

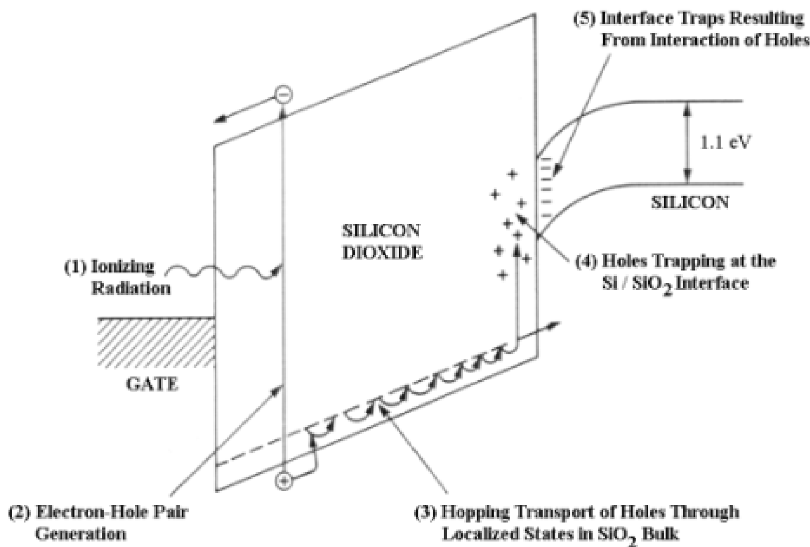


Figure 2.1: Illustration of ionizing radiation effects in MOS devices.[4]

Positive charge accumulates not only in the gate oxide but especially in the thick Shallow Trench Isolation (STI) and in the spacers (oxides positioned at the sides of the gate). As technology advances and gate oxide thickness reduces, the STI and spacers become the primary causes of TID-induced degradation in MOSFETs.

TID effects impact several MOSFETs electrical parameters, including the threshold voltage, the subthreshold slope, the transconductance and the on/off currents.
The accumulation of holes in the gate oxide together with the effect of the increased $Si - SiO_2$ interface defects lead to a variation in the flatband potential that ultimately results in an increase of the threshold voltage for both PMOS and NMOS devices. This effect is particularly strong in 3.3V devices due to the thicker gate oxide. In addition, the radiation-induced higher concentration of interface traps interferes with the channel's transport process, resulting in a reduced mobility of the inversion carriers and in a decline in the devices' transconductance and on current I_{on}. This degradation is more severe in PMOS devices because of the repulsion between the positive charges trapped in the oxide and the positively charged channel's carriers.
Radiation exposure also significantly increases leakage currents. The accumulation of positive charges in the STI oxide attracts electrons beneath the $Si - SiO_2$ interface, leading to the formation of parasitic channels parallel to the inversion layer in the active region (Figure 2.2). Although the current that can flow in these parasitic channels is typically very low, it becomes significant at low gate voltages when the main channel is turned off, leading to a substantial rise in the off-state current, I_{off} (Figure 2.7(b)). This effect is particularly pronounced in NMOS devices where electrons are the majority carriers, while PMOS devices are almost unaffected. Similar parasitic channels can also appear between two n-type diffusions of different devices due to charge accumulation in the STI oxide separating them (see Figure 2.3).
Figures 2.4, 2.5 and 2.6, curtesy of the DCDC team, illustrate the impact of TID on the I_{on}, I_{off} and the V_{th} of several devices in the 180nm CMOS technology used in this work.

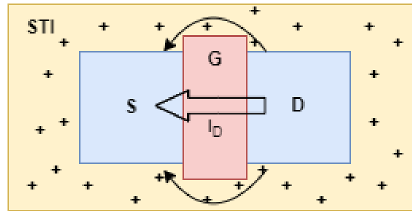


Figure 2.2: Representation of the parasitic drain-source conductive paths due to charges accumulated in the STI oxide.

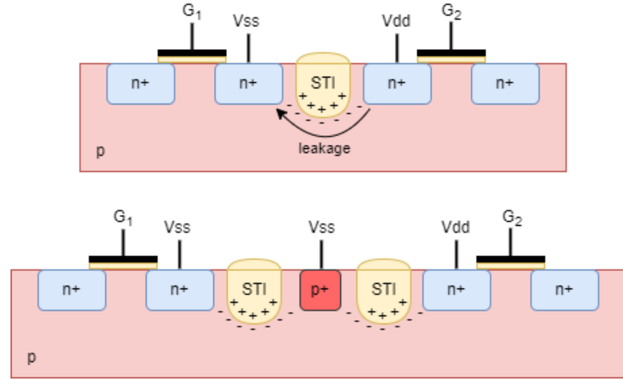


Figure 2.3: Top: STI induced parasitic paths between nwells biased at different voltages.
Bottom: p+ guard-rings used to cut radiation induced parasitic paths.

Single Event Effects (SEE) in integrated circuits can cause either reversible errors, known as soft errors, or non-reversible errors, termed hard errors. Various types of SEE exist, but the most relevant ones observed in the technology used, and noteworthy in the context of this thesis, are the following:

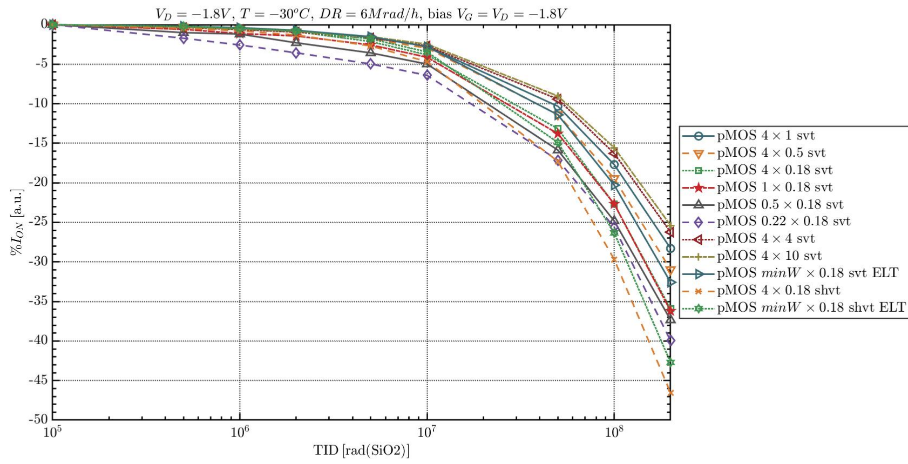
- Single Event Latch-Up (SEL) occurs when a parasitic thyristor is activated, causing a current to flow between the power lines. This error can usually be corrected by power cycling, but it can lead to the permanent failure of the circuit (thus becoming a hard error) if the latch-up current is not promptly interrupted.

- A Single Event Upset (SEU) is a reversible change of state in a logic circuit, triggered by the charge deposited by an incoming ionizing particle. It can be prevented by triplicating logic and using a majority voter to determine the output of the circuit.

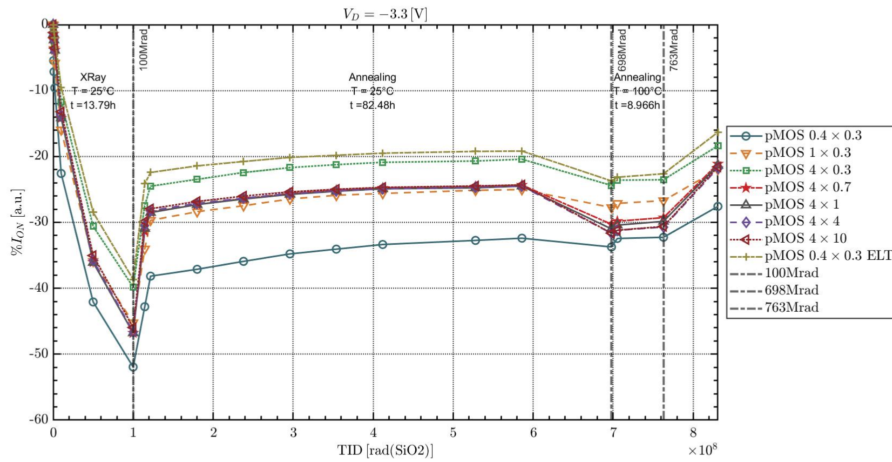
- Single Event Transients (SETs) happen when high-energy particle create a temporary fluctuation in voltage and current levels within analog or digital circuits, leading to a brief disruption in their normal operation.

- Single Event Gate Rupture (SEGR) involves the disruption of the gate oxide by an ionizing particle. This can happen especially in presence of a large gate oxide electric field, which is usually the case with power transistors.

- Single Event Burnout (SEBO) is especially observed in power MOSFETs due to the presence of parasitic bipolar transistors that can be activated by an ionizing particle, leading to significant and destructive power dissipation.

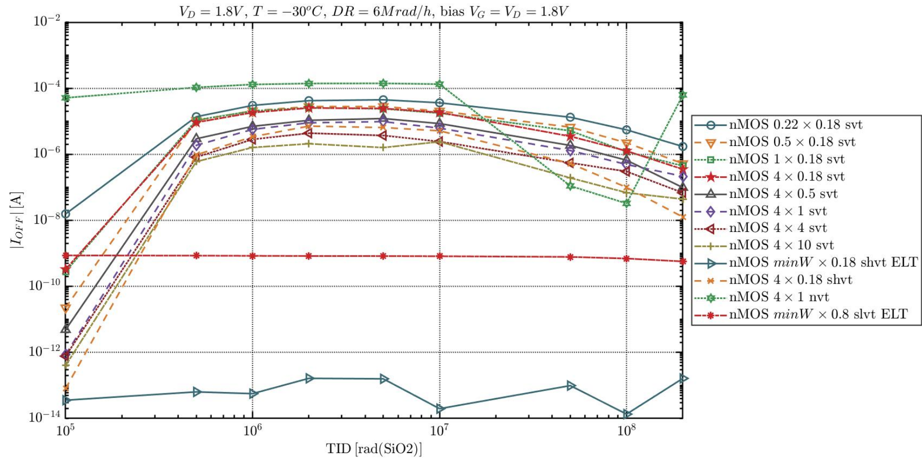


(a)

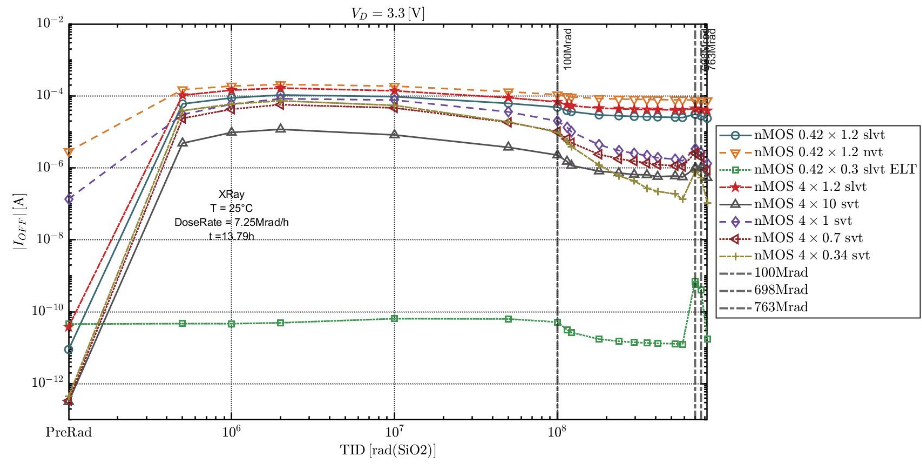


(b)

Figure 2.4: Ion vs TID. (a) 1.8V devices and (b) 3.3V devices.

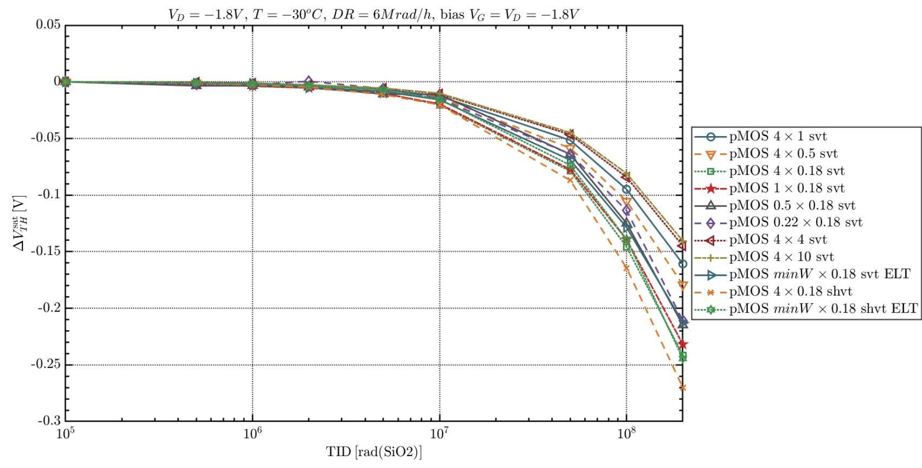


(a)

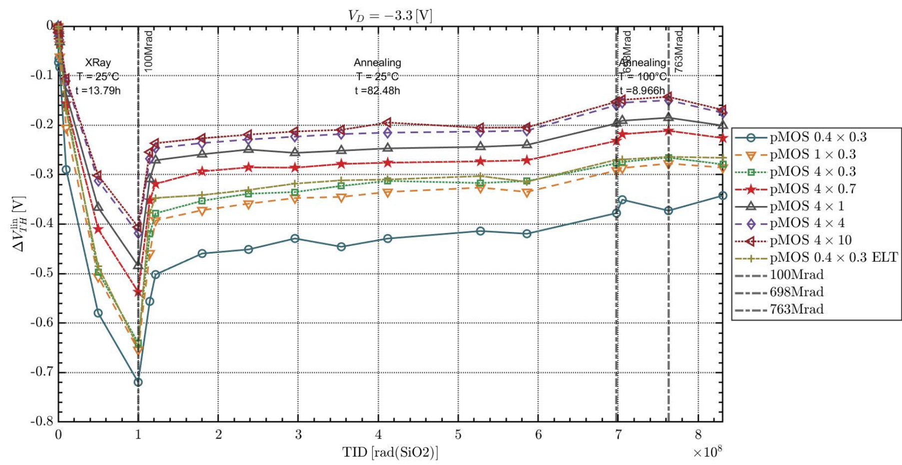


(b)

Figure 2.5: Ioff vs TID. (a) 1.8V devices and (b) 3.3V devices.



(a)



(b)

Figure 2.6: Vth vs TID. (a) 1.8V devices and (b) 3.3V devices.

2.2 Radiation hardening techniques

The blocks developed within this thesis are meant to function for ten years in the HL-LHC experiments. Given the radiation levels expected over this period in the areas where the converters will be deployed, they must endure up to 200 Mrad of Total Ionizing Dose (TID) and a fluence of 7×10^{15} n/cm^2 (1 MeV equivalent neutrons) for Displacement Damage (DD). Additionally, Single Event Effects (SEE) should not cause destructive failures for Linear Energy Transfer (LET) values up to 40 MeV·cm^2/mg. [6]
There are different ways to mitigate the effects described in the previous section, making circuits "radiation-hard". The three most commonly used techniques are:

- hardening by process: involves modifying certain process steps and technological parameters. This approach comes with higher costs and lower yields compared to using commercial CMOS technology.
- hardening by design: involves using specific design techniques allowing to mitigate the impacts of TID and SEE.
- hardening by layout: involves using specific layout techniques to mitigate the impacts of TID and SEE.

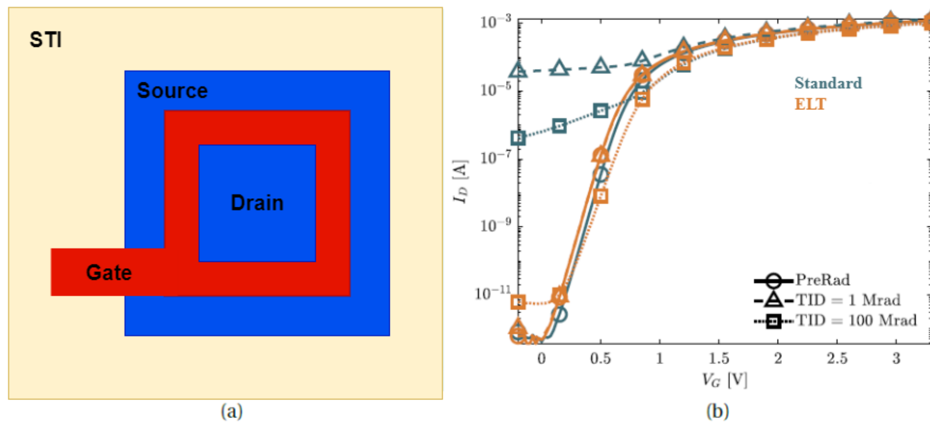


Figure 2.7: (a) Enclosed Layout Transistor illustration, and (b) typical ID-VG curves of devices before and after irradiation (1Mrad and 100Mrad).

To suppress TID-induced leakage currents in NMOS devices, an enclosed layout was used. In an Enclosed Layout Transistor (ELT), the Shallow Trench Isolation (STI) does not contact the channel, eliminating parasitic source-to-drain paths present in conventional MOSFETs. Figure 2.7 a) illustrates the general structure of an ELT, and Figure 2.7 b) shows how the leakage current of an irradiated ELT is significantly lower than a standard-layout transistor. However, using an enclosed layout has some drawbacks which make the designing process more challenging:

- ELTs occupy a larger area for the same equivalent transistor length and width, reducing the density of the integrated circuit.
- The parasitic capacitances are generally higher.
- The $\frac{W}{L}$ ratio is challenging to model and it will depend on the specific shape of the ELT. For this work the shape shown in Figure 2.8 has been used for which the following formula is valid [4]:

$$\left(\frac{W}{L}\right)_{\text{eff}} = 4 \cdot \frac{2\alpha}{\ln \frac{d'}{d'-2\alpha L_{\text{eff}}}} + 2K \cdot \frac{1-\alpha}{\frac{1}{2}\sqrt{\alpha^2+2\alpha+5} \cdot \ln \frac{1}{\alpha}} + 3 \cdot \frac{\frac{d-d'}{2}}{L_{\text{eff}}}$$

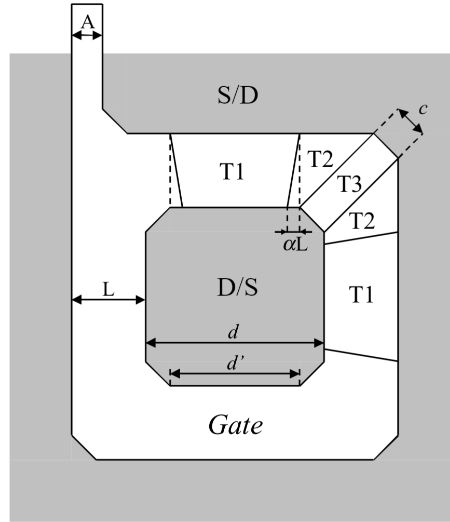


Figure 2.8: Enclosed Layout shape. Adapted from [4]

- Due to the topology of ELTs, the $\frac{W}{L}$ ratio cannot fall below a certain value dependent on L, which imposes design limitations. In this case $\frac{W}{L}_{\text{min}} \approx 2.26$
- There is a lack of symmetry which make device matching less optimal.

Other than ELT, other techniques have been employed to ensure reliable performances under radiation. To prevent parasitic currents between n-doped diffusions, p+ guard rings were placed between NMOS devices with different source potentials and between n-wells and NMOS transistors. In this way leakage paths under STI are cut (Figure2.3).
Additionally, numerous n-well and substrate contacts were placed close to any potential latch-up so that, by connecting the base of the parasitic NPN and PNP transistors to their emitters, Single Event Latch-up (SEL) is avoided (see Figure 2.9).
Finally, the impact of Single Event Transients (SETs) on the analog circuitry was minimized by lowering the impedance of the most sensitive nodes, thereby reducing the voltage fluctuation caused by the injected charge. This result has been accomplished by increasing the current or by connecting capacitors to these nodes, at the expense of area and efficiency.

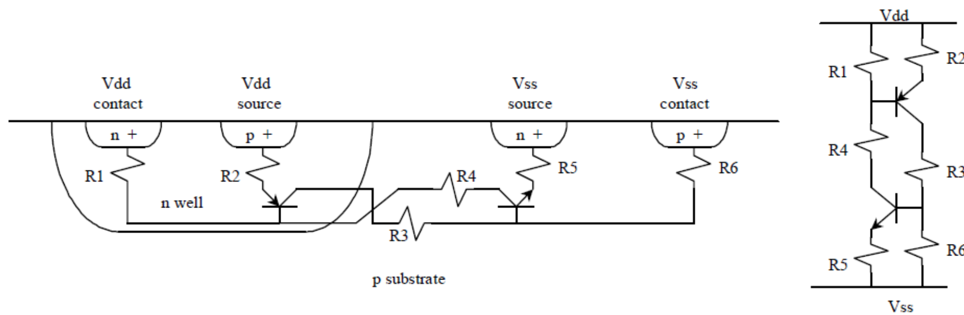


Figure 2.9: Parasitic thyristor in a CMOS process.[4]

Chapter 3

Developed blocks

As previously mentioned, the objective of this thesis has been the development of several blocks forming the control unit of the first stage DC-DC converter in the power distribution scheme proposed for the HL-LHC.
A schematic view of the fully integrated control unit currently under development is provided in Figure 3.1, with the blocks designed by the author of this thesis highlighted in red.

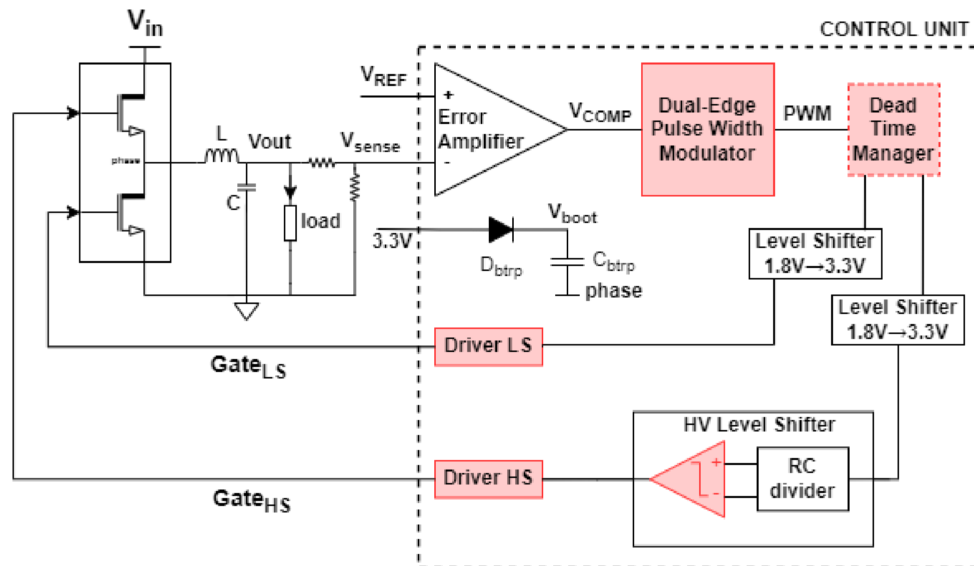


Figure 3.1: Schematic view of the developed DC-DC converter control unit. Highlighted in red the blocks that have been developed for this thesis.

The role of this control unit is to ensure tight regulation of the converter's output voltage by tuning the duty cycle of the power switches' gate signals in response to variations of V_{in} or I_{out}. In fact, differently from the ideal and lossless case presented in the introduction, when accounting for all the non-idealities of real circuits, the conversion ratio starts to show a dependence on the load current.

Voltage-mode control has been adopted for this project due to its excellent regulation performance and simplicity. In this scheme (refer to Figure 3.1), the converter's output voltage is sensed by a high-gain error amplifier and compared with a reference voltage generated internally by a bandgap reference. The control signal V_{comp} created by the error amplifier is then translated by a pulse width modulator into a duty cycle for the PWM signal, whose frequency can be regulated by an external resistor. A *dead time manager* block then manipulates the PWM signal to generate the proper input signals for the power stage switches. A "dead time", during which neither the high side switch nor the low side switch are active, is introduced to prevent dangerously large short-circuit currents from flowing from V_{in} to ground. It is important that the length of this dead time, which can be regulated by means of external resistors, is kept as short as possible to maximize efficiency by reducing the power lost due to bulk diode conduction. The dead time manager outputs are then shifted from the 1.8V voltage domain to the 3.3V one in order to drive high voltage transistors. The low side signal is then directly routed towards the LS switch driver, while the high side signal is fed to an high voltage level shifter that makes sure that it is referred to the phase node voltage. A simple bootstrap circuit consisting of a diode and a capacitor is then needed to ensure that the high side gate-source voltage difference can reach 3.3V even when $V_{\text{phase}} = V_{\text{in}}$.

In the following sections, the blocks that have been developed will be detailed: a novel dual-edge pulse width modulator, the logic part of the dead-time manager, a high voltage comparator for the high voltage level shifter, and the gate drivers for the high side and low side power switches.

3.1 Dual Edge Pulse Width Modulator

3.1.1 Theoretical background and model

The pulse width modulator is a fundamental component of the converter's control unit, determining its overall dynamic performance. The role of this block is to regulate the width of the pulses in the *PWM* signal that determines the turning on and off of the switching components, thereby varying the power supplied to the load.

There are many ways to implement pulse width modulation. The intersective method used in this work, is a straightforward and widely used technique in generating PWM signals that involves comparing a reference signal with a carrier signal (typically a triangular or sawtooth waveform). The points of intersection between these two signals determine the switching instants of the PWM signal.

Depending on the timing and positioning of the pulse transitions within each period, we can distinguish 3 main types of intersective pulse width modulation:

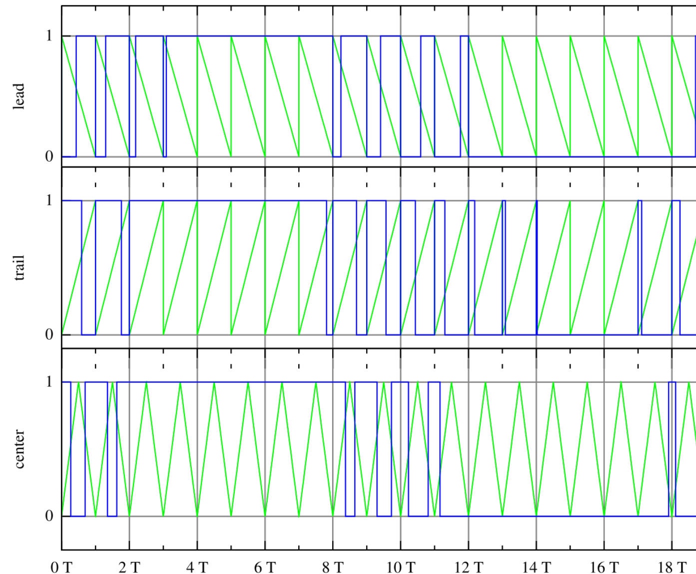


Figure 3.2: Three methods to generate an intersective pwm: leading edge modulation, trailing edge modulation or centered modulation.

- Leading edge modulation: the trailing edge of the pulse is fixed at the end of the period, and the pulse width is adjusted by varying the leading edge. This means that the pulse ends at a consistent point, but its start point changes to adjust the duty cycle.

- Trailing edge modulation: the leading edge of the pulse is fixed at the beginning of the period, and the pulse width is adjusted by varying the trailing edge. This means that the pulse begins at a consistent point, but its end point changes to adjust the duty cycle.

- Centered pulse modulation or double-edge modulation: the pulse is centered within each period. Both the leading and trailing edges of the pulse move to adjust the duty cycle, keeping the pulse symmetrical around the center of the period.

In this thesis, a novel double-edge modulator with improved dynamic performances [7] has been implemented.
Figure 3.3 shows the scheme of the proposed PWM and its steady state waveform.

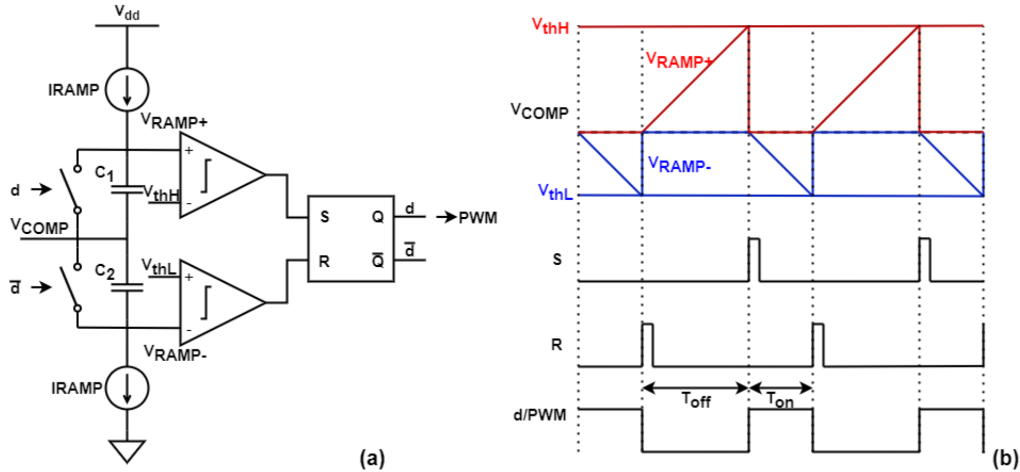


Figure 3.3: (a) Schematic and (b) steady-state waveforms of the implemented dual-edge modulator.

The control signal V_{COMP} from the Error Amplifier's output is connected to two capacitors, C_1 and C_2. When the pulse-width modulated signal, here

called d, is low, C_2 is bypassed and the current I_{RAMP} charges C_1 until the voltage $V_{\text{RAMP+}}$ reaches the threshold V_{thH}, which sets the flip-flop output d. Being d high, C_1 is bypassed, and I_{RAMP} charges C_2 until $V_{\text{RAMP}-}$ reaches the threshold V_{thL}, which resets d. To ensure a constant switching frequency f_{sw} for all duty cycle values, it is important that both capacitors are set to the same value, $C_1 = C_2 = C$.

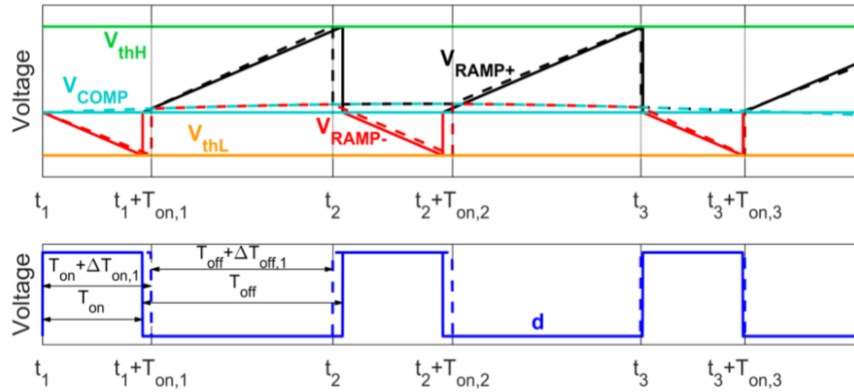


Figure 3.4: Representation of steady-state waveforms (solid lines) and perturbed waveforms (dashed lines), when a sinusoidal perturbation is applied at the input of the modulator. (Adapted from [7]).

In order to derive the small-signal response of such modulator, the *Describing Function* approach has been used [7][8].
First, lets consider a "small" sinusoidal perturbation applied on top of the DC value of V_{COMP}:

$$V_{\text{COMP}} = V_{\text{COMP,DC}} + \hat{v} sin(2\pi f_p t) \qquad \hat{v} << V_{\text{COMP,DC}} \tag{3.1}$$

At this point Fourier analysis can be used to determine amplitude and phase response of the modulator at the perturbation frequency f_p. Knowing that the output signal $d(t)$ in the ith cycle is 1 between t_i and $t_i + T_{\text{on,i}}$ and 0 elsewhere, we can calculate its first-order Fourier coefficients as:

$$
\begin{aligned}
c_m =& \frac{2jf_p}{N}\int_0^{MT_{\text{sw}}} d(t)e^{-j2\pi f_p}dt \\
=& \frac{1}{\pi N}\sum_{i=1}^{M}\left(e^{-j2\pi f_p t_i} - e^{-j2\pi f_p (t_i + T_{\text{on},i})}\right)
\end{aligned} \tag{3.2}
$$

t_i and $t_i + T_{\text{on,i}}$ can be written in a more useful form considering that the on and off times of signal $d(t)$ will now be perturbed by a small delta with respect to their DC values:

$$
T_{\text{on,i}} = T_{\text{on,DC}} + \Delta T_{\text{on,i}} \qquad T_{\text{off,i}} = T_{\text{off,DC}} + \Delta T_{\text{off,i}} \tag{3.3}
$$

From which we obtain that

$$
t_i = (i-1)\,T_{\text{sw}} + \sum_{k=1}^{i-1}\Delta T_{\text{on},k} + \sum_{k=1}^{i-1}\Delta T_{\text{off},k} \tag{3.4}
$$

$$
t_i + T_{\text{on},i} = (i-1)\,T_{\text{sw}} + T_{\text{on}} + \sum_{k=1}^{i}\Delta T_{\text{on},k} + \sum_{k=1}^{i-1}\Delta T_{\text{off},k}. \tag{3.5}
$$

Geometrical considerations (see Figure 3.6) lead to the following results:

$$
\begin{aligned}
\Delta T_{\text{on},k} &= S^{-1}\hat{v}\sin\left[2\pi f_p\left(t_k + T_{\text{on},k}\right)\right] \\
&\approx S^{-1}\hat{v}\sin\left\{2\pi f_p\left[(k-1)\,T_{sw} + T_{\text{on}}\right]\right\}
\end{aligned} \tag{3.6}
$$

$$
\Delta T_{\text{off},k} = -S^{-1}\hat{v}\sin(2\pi f_p t_{k\,+\,1}) \approx -S^{-1}\hat{v}\text{sin}(2\pi f_p k T_{sw}) \tag{3.7}
$$

Where S^{-1} is the inverse of the ramps' slope ($S = I_{\text{RAMP}}/C$).
At this point, plugging 3.4 and 3.5 in 3.2 and performing a first-order expansion of the exponential terms ($\Delta T_{\text{on},k}, \Delta T_{\text{off},k}$ are very small for the small-signal assumption) we get:

$$
\begin{aligned}
c_m = \frac{1}{\pi N}\sum_{i=1}^{M}\Bigg\{ & e^{-j2\pi f_p (i-1) Tsw}\cdot\left[1 - j2\pi f_p\left(\sum_{k=1}^{i-1}\Delta T_{\text{on},k} + \sum_{k=1}^{i-1}\Delta T_{\text{off},k}\right)\right] \\
& - e^{-j2\pi f_p[(i-1)T_{sw} + T_{\text{on}}]}\cdot\left[1 - j2\pi f_p\left(\sum_{k=1}^{i}\Delta T_{\text{on},k} + \sum_{k=1}^{i-1}\Delta T_{\text{off},k}\right)\right]\Bigg\}
\end{aligned} \tag{3.8}
$$

3.6 and 3.7 can be written in terms of complex exponential allowing to express $\sum_{k=1}^{i-1} \Delta T_{\text{on},k}, \sum_{k=1}^{i} \Delta T_{\text{on},k}, \sum_{k=1}^{i-1} \Delta T_{\text{off},k}$ into geometric summation whose value can be easily calculated. Finally, using these results in 3.8, and remembering that $\sum_{i=1}^{M} e^{-j2\pi A f_p (i-1) T_{\text{sw}}} = 0$ for $A \in Z$, we get:

$$c_m = \frac{\hat{v}}{M} \cdot \frac{e^{j2\pi f_p T_{\text{on}}} + e^{j2\pi f_p (T_{sw} - T_{\text{on}})} - 2e^{j2\pi f_p T_{sw}}}{1 - e^{j2\pi f_p T_{sw}}} \tag{3.9}$$

Dividing by the perturbation and translating the expression into the s-domain we obtain the modulator's transfer function:

$$H_{\text{mod}}(s) = = \frac{1}{M} \cdot \frac{e^{sDT_{sw}} + e^{s(1-D)T_{sw}} - 2e^{sT_{sw}}}{1 - e^{sT_{sw}}} \tag{3.10}$$

Where D is the duty cycle. This expression shows that the proposed modulator's gain is $\frac{1}{M}$, similar to the one of conventional leading-, trailing or dual-edge modulators [9]. The factor containing complex exponential introduces a phase lead in the transfer function that highlights the improved small signal response of the modulator.
Figure 3.5 shows the good correspondence between the derived model and the SIMPLIS simulations.

Another advantage of the described pulse-width modulator is its improved large-signal performance when the load current I_{load} changes suddenly. For instance, when I_{load} increases abruptly, trailing-edge modulators can experience a significant delay on the rising edge of the pulse-width modulated signal, leading to undershoots in V_{out}. Conversely, in leading-edge modulators, the delay on the falling edge of the pulse-width modulated signal can cause overshoots in V_{out}.
Conventional dual-edge modulators may exhibit both overshoots and undershoots in the output, although these effects are typically less pronounced than in the other cases. In the dual-edge modulator implemented in this work, the introduced delay and resulting over/undershoots are significantly reduced because the pulse-width modulated signal d switches immediately when the output of one of the comparators changes state.
Figure 3.6 illustrates how different types of modulators respond to a change in load current.

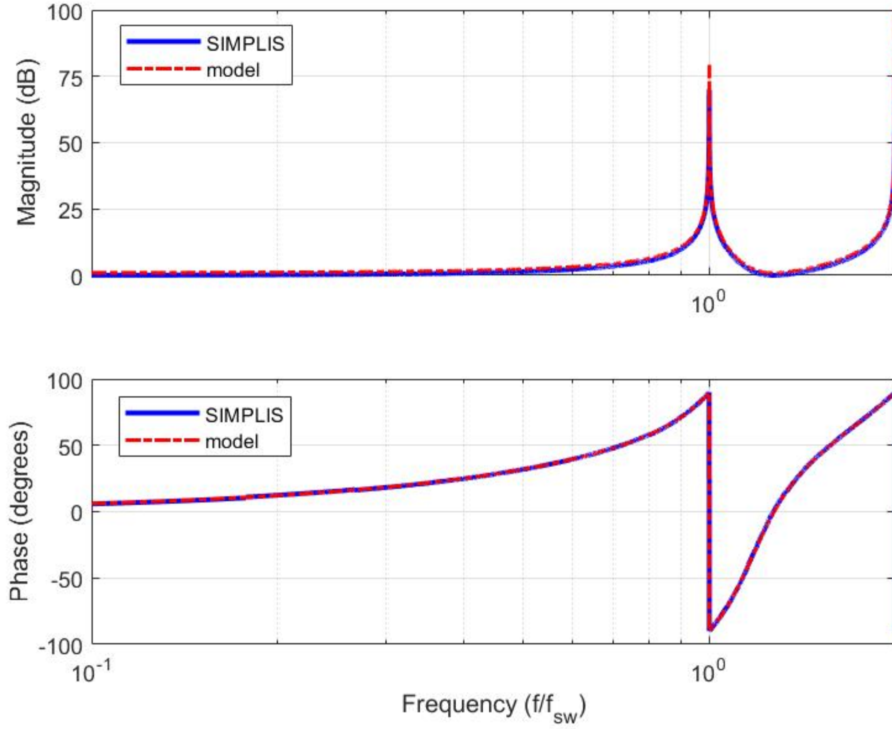


Figure 3.5: Comparison between the open-loop transfer function of the dual-edge modulator calculated using the theoretical model (blue) and the one obtained by SIMPLIS simulations (red). $D = 0.2$, $T_{\text{sw}} = 1MHz$

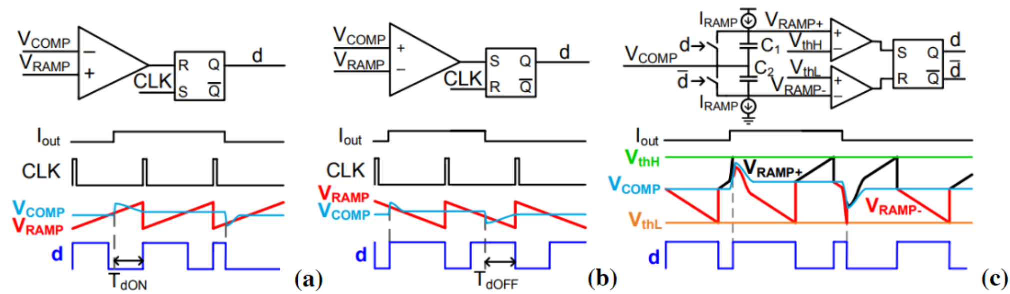


Figure 3.6: Response of (a) a trailing-edge modulator, (b) a leading-edge modulator and (c) the implemented dual-edge modulator when I_{load} is suddenly changed. Adapted from [7]

3.1.2 Implemented circuit and results

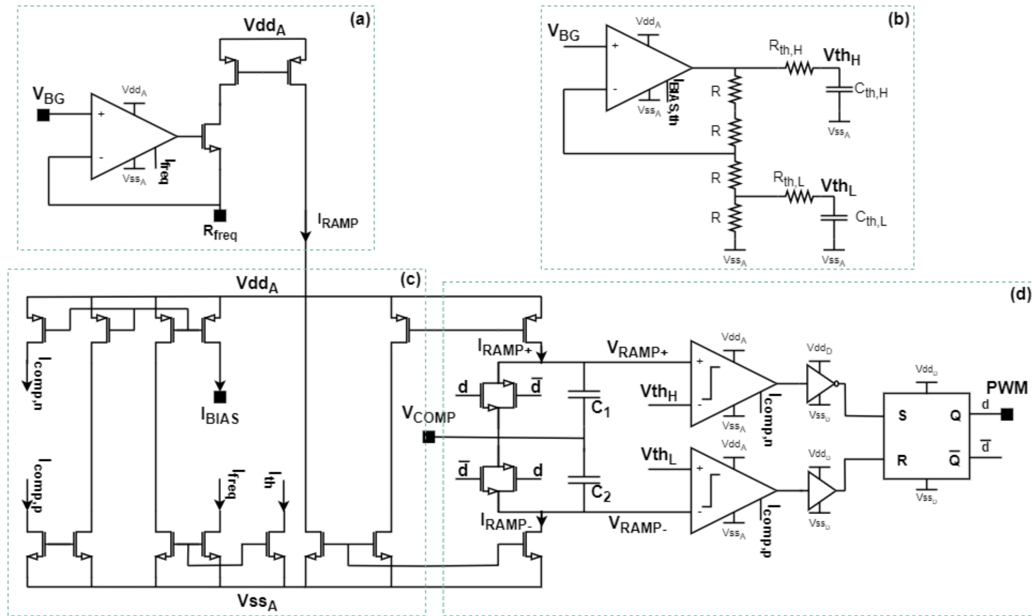


Figure 3.7: Top view of the implemented PWM circuit

Figure 3.7 shows a schematic view of the implemented dual-edge pulse width modulator circuit in which we can recognize 4 main blocks:

(a) I_{RAMP} regulator,

(b) Thresholds generator,

(c) Biasing network,

(d) Dual-Edge PWM.

Before proceeding with a detailed description of each of these blocks, it is important to note the simulation tools used to ensure the correct and reliable operation of the designed circuits: corner simulations and Montecarlo simulations.
Corner simulation consists in modelling extreme variations in fabrication parameters, supply voltage, and temperature to account for the worst/best-case operating conditions. Due to manufacturing inaccuracies, process-dependent

parameters like the oxide thickness, the diffusion/implantation depths, the doping and transistor dimensions can vary. This variation can affect transistors' electrical parameters, causing them to deviate from their nominal behavior. Additionally, supply voltage fluctuations, often caused by parasitic effects in the interconnects, can impact the design's functionality. Temperature changes also influence circuit performance. The following corners have been considered:

- Process corners for active components: typical-typical, fast-fast, slow-slow, fast-slow, slow-fast, where the first term corresponds to NMOS and the second one to PMOS.
- Process corners for passive components: high/low resistance, high/low capacitance.
- Supply voltage variations of $\pm 10\%$.
- Three temperature conditions: -30°C, 27°C, and 100°C.
- Two radiation corners: fast NMOS fast PMOS and slow NMOS slow PMOS at 200 Mrad of TID.

While corner simulations often represent the most extreme scenarios (either very pessimistic or optimistic), Monte Carlo analysis offers a statistical approach to account for fabrication-dependent parameter variations inducing device mismatches. In each run, simulations use randomly calculated parameters based on a statistical distribution model. Monte Carlo analysis is particularly useful for assessing how mismatches impact circuit's performances.
Particular attention has also been given to ensure that all devices operate within their *safe operating areas* (SOA) to achieve good reliability.

$I_{\mathbf{RAMP}}$ regulator

The current regulation circuit, depicted in Figure 3.8, is crucial for providing a stable and precise current to the ramp generation stage. This circuit is designed using a voltage follower and a PMOS current mirror to ensure the desired current regulation.

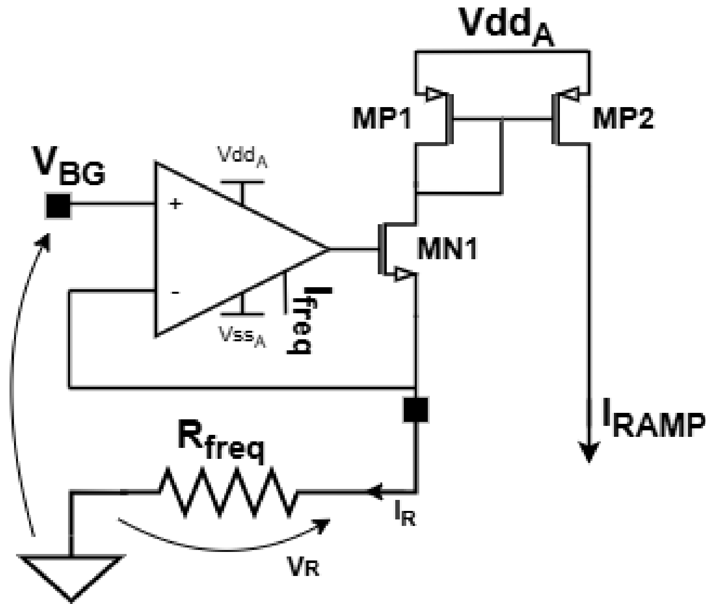


Figure 3.8: Current Regulation Circuit

At the heart of the circuit is simple two stage OTA configured as a voltage follower. Due to its high input impedance the voltage follower draws very little current from the source V_{BG}, thus eliminating load effects and allowing to virtually isolate the two stages from each other. The non-inverting input of this op-amp is connected to a bandgap reference voltage, V_{BG}, set to 0.6V. The voltage follower configuration ensures that this reference voltage is maintained also at the inverting input, thereby appearing across an external resistor, R_{freq}.
By imposing this fixed voltage of 0.6V across R_{freq}, a precise reference current, I_{R}, is established: $I_{\mathrm{R}} = \frac{V_{BG}}{R_{\mathrm{freq}}}$.
This reference current is then mirrored by a PMOS current mirror, which comprises two PMOS transistors. One transistor is situated in the reference branch, while the other is in the output branch. Assuming perfect matching

between the two transistors, that must operate in strong inversion and saturation, the current is copied from the input branch to the output branch, resulting in a stable current, I_{RAMP}, which is then supplied to the subsequent stage of the circuit.

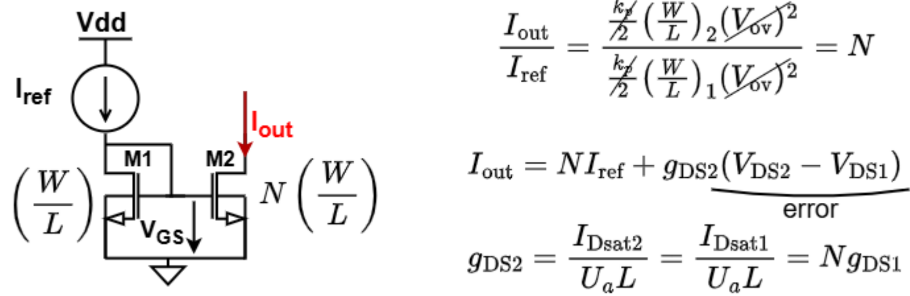


Figure 3.9: Current mirror schematic and theoretical model.

One of the significant advantages of this current regulation circuit is its precision. The voltage follower ensures that the reference voltage is precisely maintained, resulting in an accurate reference current. Furthermore, the stability of the PMOS current mirror guarantees a stable output current, which is essential for the reliable operation of subsequent stages. Additionally, the simplicity of the circuit design makes it easy to implement and integrate into larger systems.

Figure 3.10 demonstrates how the output current can be effectively controlled by adjusting R_{freq}.

The designed circuit is capable of generating stable currents ranging from 30 μA to 500 nA. The upper limit is constrained by the minimum usable resistance of 20 kΩ, while the lower limit is dictated by the PMOS current mirror moving out of its operational region (saturation and strong inversion) as a lower reference input current is provided. This results in a loss of current copying accuracy as shown by the increase in the ratio between the two branches' currrents as R_{freq} increases.

Optimal stability of the output current is also achieved in corner and Monte Carlo simulations as shown in Table 3.1.

To minimize the effects of device mismatches, common centroid layout[10] have been employed, along with large channel devices. These devices are

easier to match due to their reduced sensitivity to fabrication tolerances and exhibit lower channel conductance (g_{DS}), which diminishes the impact of channel length modulation (see formulas in Figure 3.9).

	Corners		**Montecarlo**			
	min	max	min	avg	max	σ
Ifreq	6.002 μA	6.034 μA	5.951 μA	6.022 μA	6.098 μA	24.68 nA

Table 3.1: Output current I_{freq} variation through corner and montecarlo simulation. Case $R_{\text{freq}} = 100K\Omega$, $I_R = 6\mu$.

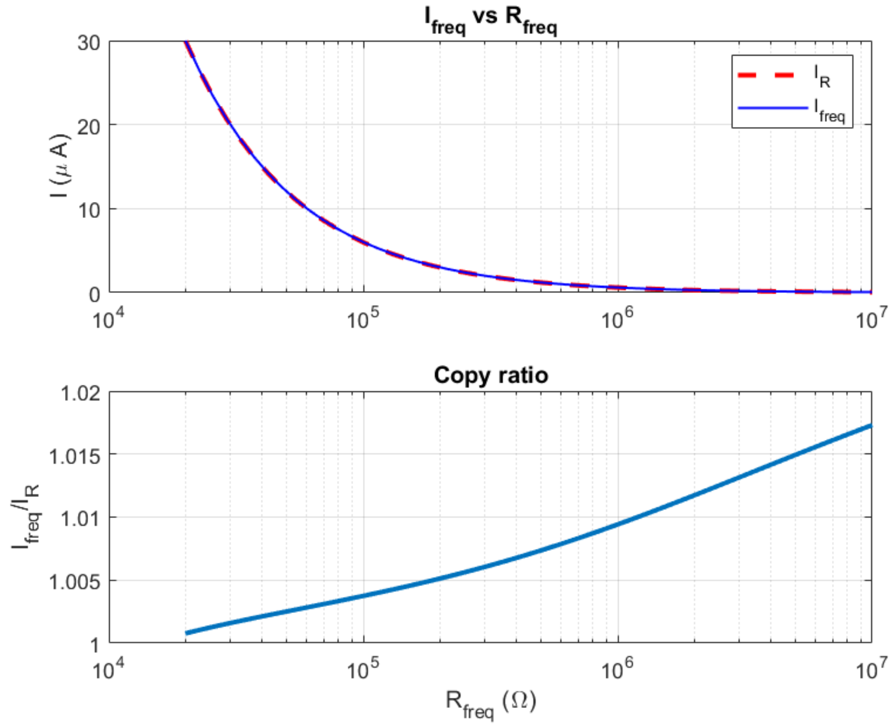


Figure 3.10: Current Regulation Circuit

Thresholds generator

The two threshold voltages V_{thH} and V_{thL} are generated by the circuit shown in Figure 3.11.

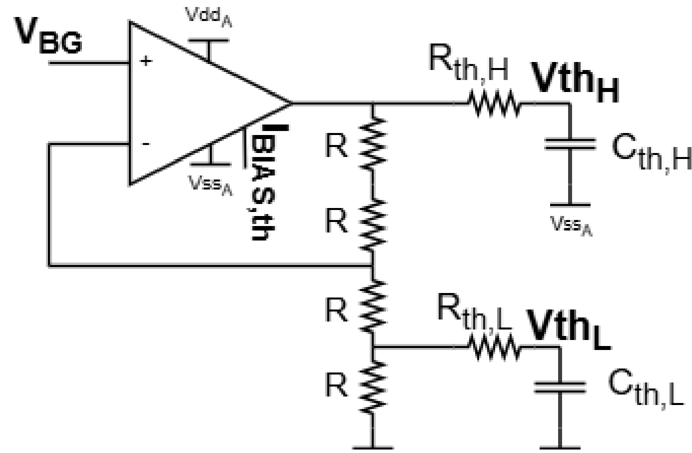


Figure 3.11: Threshold generator.

This circuit comprises a simple resistive voltage divider, where the reference voltage of 0.6V is supplied by a bandgap reference through a voltage follower OTA.
RC filters with a time constant (τ) of 5 μs are used to stabilize the two output voltages, filtering out noise and disturbances from the input voltage as well as reducing SEE.
The threshold values of 1.2V and 0.3V have been selected to ensure a good dynamic range for the ramp signals while providing sufficient "room" for the comparators' bias transistors to operate correctly, ensuring compatibility with the comparators' input range.

Since all components are integrated on silicon, particular attention has been given to the layout of this block to minimize the effects of mismatch in devices due to non-idealities of process and operating conditions. Specifically, common centroid or interdigitation techniques and dummy devices have been employed for the voltage follower as well as resistors and capacitors.

The result of corner simulations shows an incredible stability of the two thresholds against fluctiations of devices' electical and technological parame-

ters due to fabrication process tollerances or environmental factors (temperature, supply voltage, radiations).
Montecarlo simulations show great stability also against devices mismatch, as can be seen in the table below:

Montecarlo	min	avg	max	σ
V_{thH}	1.195V	1.2V	1.205V	2.008mV
V_{thL}	298.2mV	300mV	301.5mV	$579.3\mu V$

Table 3.2: Results of Montecarlo simulations for the threshold voltages.

Biasing network

A simple network of PMOS and NMOS current mirrors is used to provide the bias current to the different blocks of the circuit, as shown in Figure 3.12.

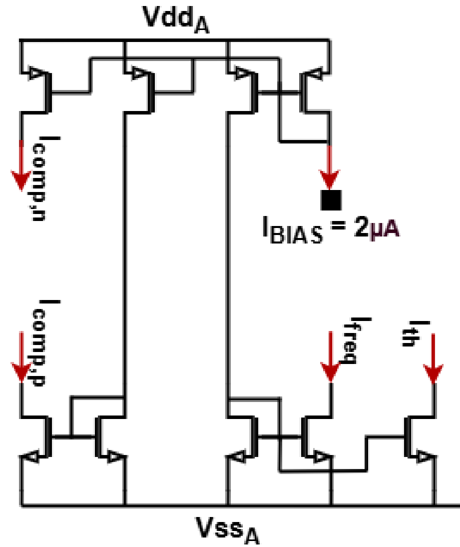


Figure 3.12: Pulse width modulator bias network.

The same considerations applied to the I_{RAMP} regulator are valid to ensure a stable bias current is provided to each block:

- Strong inversion and saturation are ensured by low $\frac{W}{L}$ ratios.

- Large channel lengths help reduce channel length modulation effects.
- Common centroid layouts and dummy transistors are employed in the layout to mitigate the effects of mismatches and fluctuations in environmental conditions.

Table 3.3 presents the results of simulations performed to validate the design, confirming the stability in the output currents that can be achieved.

		Corner		**Montecarlo**			
	target	**min**	**max**	**min**	**avg**	**max**	σ
$I_{\mathbf{Bias,th}}[\mu A]$	2	2.009	2.12	1.978	2.057	2.135	$25.04 \cdot 10^{-3}$
$I_{\mathbf{Bias,freq}}[\mu A]$	2	2.009	2.12	1.993	2.057	2.137	$23.4 \cdot 10^{-3}$
$I_{\mathbf{comp,p}}[\mu A]$	5	5.018	5.263	4.988	5.124	5.256	$41.16 \cdot 10^{-3}$
$I_{\mathbf{comp,n}}[\mu A]$	2	2.003	2.017	1.986	2.012	2.043	$11.32 \cdot 10^{-3}$

Table 3.3: Bias network output currents variation across corner and Montecarlo simulations.

Implemented dual-edge modulator

The implementation on Silicon of the dual edge modulator itself is presented in the schematic of Figure 3.13.

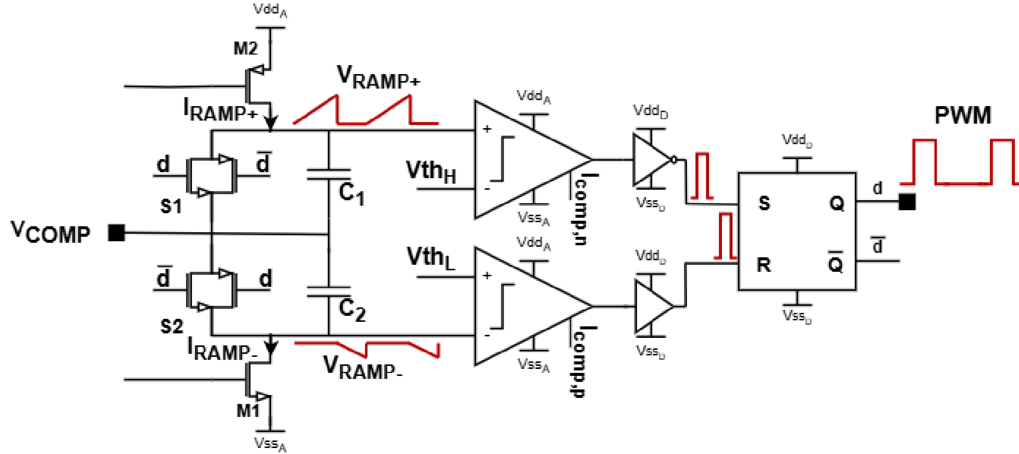


Figure 3.13: Schematic of the implemented dual edge pulse width modulator

Transistors M1 and M2 copy the output current of the I_{RAMP} regulator, providing the two equal currents $I_{\text{RAMP+}}$ and $I_{\text{RAMP-}}$ that charge and discharge the capacitors C_1 and C_2 to generate the ramp signals $V_{\text{RAMP+}}$ and $V_{\text{RAMP-}}$ which are then compared to the thresholds V_{thH} and V_{thL}.

The switches S1 and S2 that periodically shorts C1 and C2 respectively to reset the ramp signals when the threshold is reached, have been implemented by means of pass-gates (Figure 3.14).
A pass or transmission gate can selectively block or pass a voltage from the input to the output without degradation. This solid-state switch consists of a PMOS transistor and NMOS transistor biased in a complementary manner so that both transistors are either on or off.
When the control signal ϕ is high and the complementary signal $\bar{\phi}$ is low, both transistors conduct thus passing the signal from node A to node B or vice versa. When, instead, ϕ is low and $\bar{\phi}$ is high, both transistors are *off* forcing a high-impedance condition on both the A and B nodes. This design provides true bidirectional connectivity without significant degradation of the input signal.

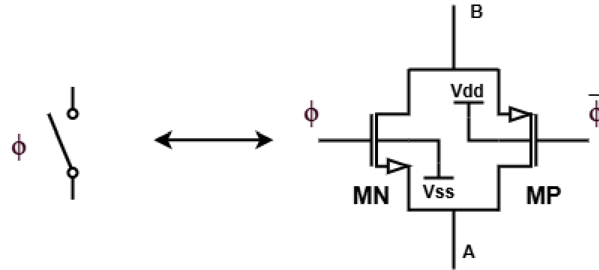


Figure 3.14: Switch implementation through pass gate

The two capacitors, C1 and C2, have been implemented using metal-oxide-metal (MOM) capacitors (Figure 3.15 (b)) consisting of a dense mesh of interdigitated metallic fingers separated by an insulating dielectric (silicon oxide). Although MOM capacitors tend to occupy a larger area on chip due to their lower capacitance density compared to metal-oxide-semiconductor (MOS) capacitors (Figure 3.15 (b)), they are less susceptible to ionizing radiation effects. This reduced susceptibility is particularly advantageous given the “floating” connection of C1 and C2 between V_{COMP} and $V_{\mathrm{RAMP+/-}}$, which limits their capability to flush excess charges.

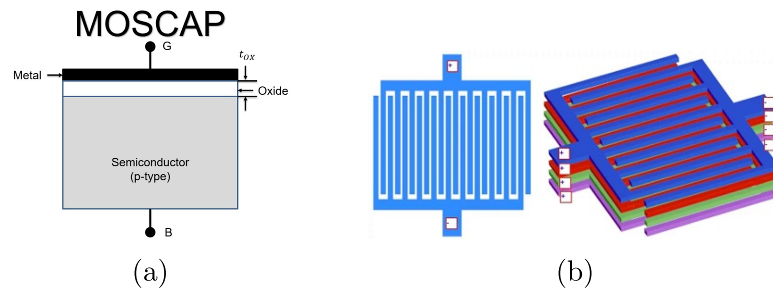


Figure 3.15: Structure of MOS capacitor (a) and Metal-Oxide-Metal (b) capacitors

The value of these capacitors (1 pF) results from a compromise between area occupancy, the error amplifier’s gain-bandwidth (GBW) specifications ($GBW \approx \frac{g_M}{2\pi C_L} > 80\,\mathrm{MHz}$), and the need to ensure good linearity of the charging curves for the ramp signals, as well as reliable modulation of the PWM signal frequency (500 kHz - 8 MHz).

The most delicate components of the whole modulator are the two continuous-mode comparators that compares the ramp signals to the thresholds thus toggling the state of the PWM signal. Both the comparators, shown in Figure 3.18, consists of a simple two stage differential amplifier driving an unbalanced inverter that rectifies the output.
The front-end OTA converts the input voltage difference ΔV_{in} into a current $I = g_m \cdot \Delta V_{\text{in}}$, and the inverter, acting as a current comparator, determines the sign of this current: positive currents fed into the inverter are integrated by the input capacitor, driving the output voltage to logic zero; conversely, negative currents bring the output voltage to logic one.
This simple topology has proven to be able of ensuring a fast switching of the output while limiting the area occupation and power consumption.
The comparator that compares the signal $V_{\text{RAMP+}}$ with the high threshold $V_{\text{thH}} = 1.2V$ uses an NMOS differential pair, while the one comparing $V_{\text{RAMP-}}$ with the low threshold $V_{\text{thL}} = 0.3V$ is made with a PMOS differential pair. This is done to optimize the performances of the comparators by taking into account the input signals' voltage ranges.

In general, the aim of a comparator is to compare two analog signals and to provide at the output a logic signal based on the result of the comparison. In this particular case, one input is the ramp signal and the other input is the threshold voltage.

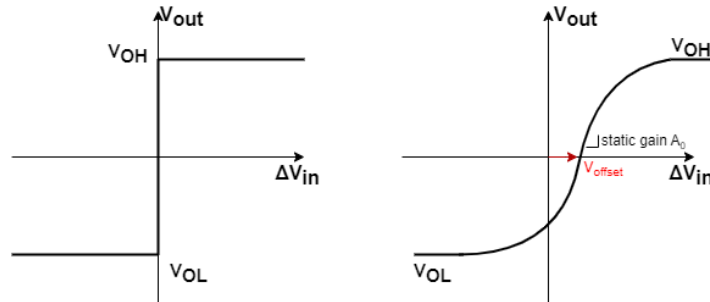


Figure 3.16: Ideal (left) and real (right) comparator transfer characteristics.

The most important parameters to take into account when evaluating the performances of a comparator are the resolution and the propagation delay. The *resolution* is defined as the minimum input signal above the threshold

that can be detected correctly determining a change in the output state; it can be mathematically represented as follows:

$$V_{\min} = \frac{V_H - V_L}{A_0} \tag{3.11}$$

where A_0 is the static gain of the circuit [11]. This is just a raw simplification since in reality a comparator is a highly non-linear component where the input signal amplitude is often large enough to make the comparator work in different operating region with respect to the linearization point. This makes predicting the dynamic behaviour of the comparator very difficult and makes simulations fundamental for the design process.
The *propagation delay*, instead, refers to the time delay between the input crossing the threshold and the output responding to this excitation, by reaching 50% of the supply voltage. Table 3.5 summarizes the performance of the designed comparators based on simulation results. This data highlights a noteworthy *speed-accuracy* trade-off: as frequency increases, the resolution of the comparators decreases.

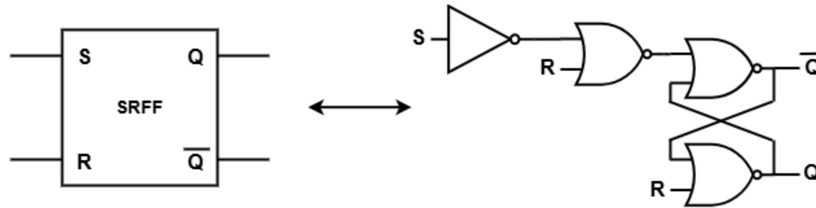
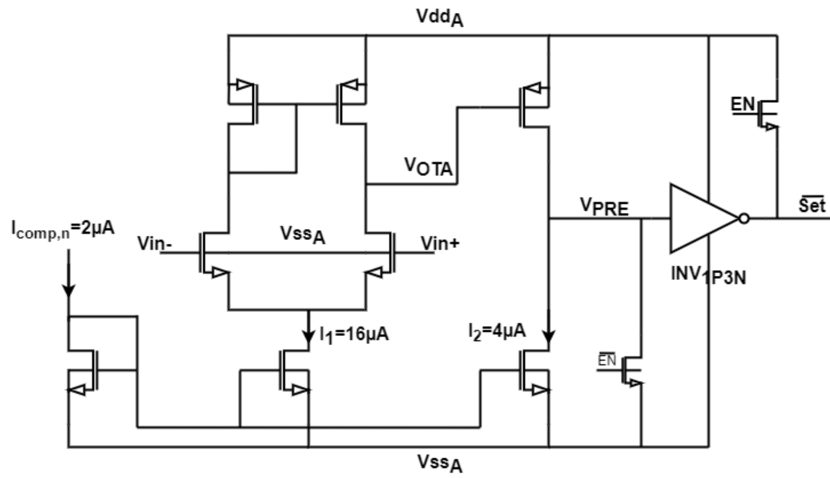
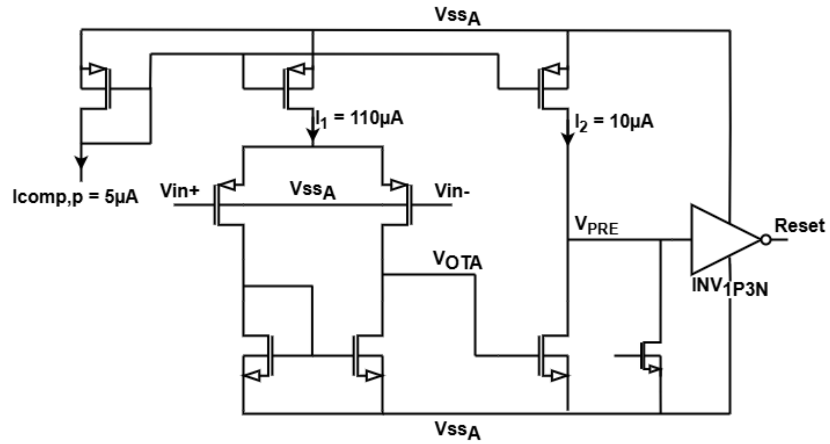


Figure 3.17: implementation of the SR flip-flop.

As illustrated in Figure 3.13, the two comparators generate pulses that drive the toggling of the internal state of a set-reset flip-flop, ultimately determining the digital value of the PWM signal. The structure of the flip-flop is shown in Figure 3.17. Specifically, it is a *reset-dominated* SR flip-flop, where additional inverters and NOR gates have been included to avoid the classical SR flip-flop forbidden state (SR = 11). In this configuration, the forbidden state is directed to the reset state. Table 3.4 clarifies the truth table for this component.



(a) High threshold comparator.



(b) Low threshold comparator.

Figure 3.18: PWM comparators.

S	R	$\bar{Q}$	Q	
0	0	$\bar{Q}$	Q	hold
0	1	1	0	Reset
1	0	0	1	Set
1	1	1	0	Reset

Table 3.4: Reset-dominated SR flip-flop truth table.

f_{sw} [MHz]	min [V]	max [V]
2	**1.301**	**1.392**
8	**1.361**	**1.482**

(a) High threshold $V_{\mathrm{th,H}} = 1.35V$.

f_{sw} [MHz]	min [V]	max [V]
2	**0.279**	**0.299**
8	**0.240**	**0.272**

(b) Low threshold $V_{\mathrm{th,L}} = 0.3V$.

Table 3.5: Comparator's real switching voltages.

Results

This section is devoted to present the main results achieved by the designed dual-edge pulse width modulator. Figure 3.6 shows the waveforms generated by the pwm. It is possible to notice how all the ramps are correctly generated as well as the Set and Reset pulses at the output of the comparators leading to a change in the state of the PWM signal. Table 3.6 shows quantitative results from the corner and Montecarlo simulation of the block.

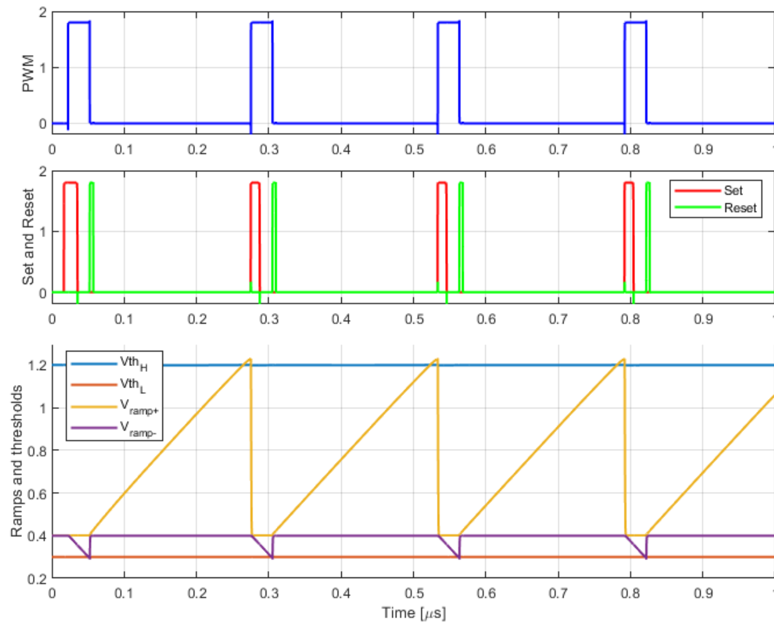


Figure 3.19: PWM wavwforms with $R_{\mathrm{freq}} = 150k\Omega$ ($I_{\mathrm{freq}} = 4\mu A$).

The observed variability of the achieved frequency is mostly due to process related fluctuations in the value of the capacitors C1 and C2, that significantly alters the slope of the ramp signals ($S \approx \frac{I_{\mathrm{RAMP}}}{C}$). From the graphs in Figure 3.20 it is possible to observe that the designed modulator can generate PWM signals with a duty cycle ranging between 0% and 100%, depending on the value of V_{COMP}, and a frequency that linearly depends on I_{RAMP}. The main limitation in the correct operation of the modulator comes from the

width of Set and Reset signals. In particular, incorrect behavior is observed when the on-time of PWM is lower than the difference between the widths of S and R signals. In this case, spurious transitions in the PWM signal may occur, compromising the circuit's operation. The dashed lines in Figure 3.20 represent the post-PEX (layout Parasitic EXtraction) simulation results of the circuit, indicating, as expected, a decline in performance when all layout parasitics are taken into account. The duty cycle increases compared to the pre-PEX case to compensate for the higher losses, while the frequency decreases by approximately 10% due to the influence of parasitic RC elements.

	Corner		**Montecarlo**			
	min	**max**	**min**	**max**	**avg**	σ
$f_{\mathbf{PWM}}[MHz]$	3.166	4.869	3.765	4.027	3.872	0.043
$D_{\mathbf{PWM}}[\%]$	10.52	12.72	10.16	12.96	11.54	0.476

Table 3.6: PWM performances.

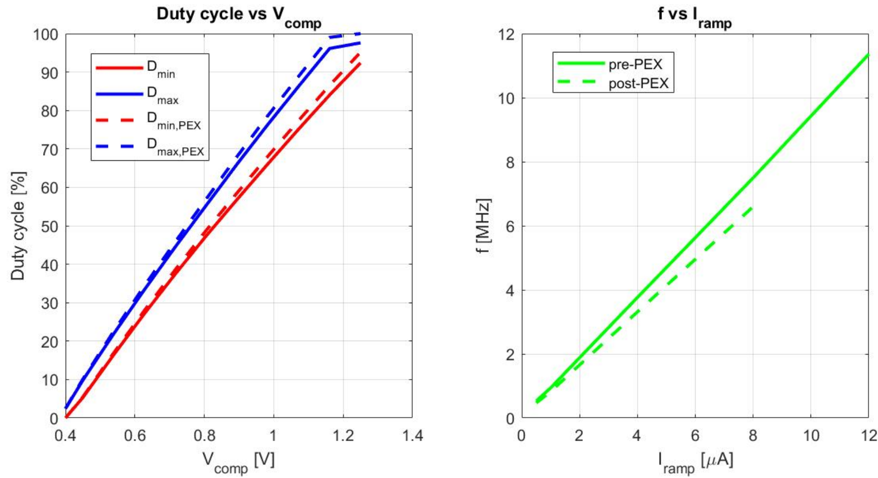


Figure 3.20: PWM Duty cycle and frequency ranges. On the left the Duty cycle maximum and minimum values obtained in corner and Montecarlo simulations are plotted against the error amplifier's output voltage V_{COMP} for $@R_{\mathrm{freq}} = 150k\Omega$ ($I_{\mathrm{freq}} = 4\mu A$). On the right the linear dependency of the PWM signal frequency on I_{RAMP} is shown for $D = 11\%$. The dashed lines represent post-PEX results.

Finally, in Figure 3.21 the layout of the proposed modulator is presented, occupying an area on Silicon 173.12 x 1174.01 μm^2.

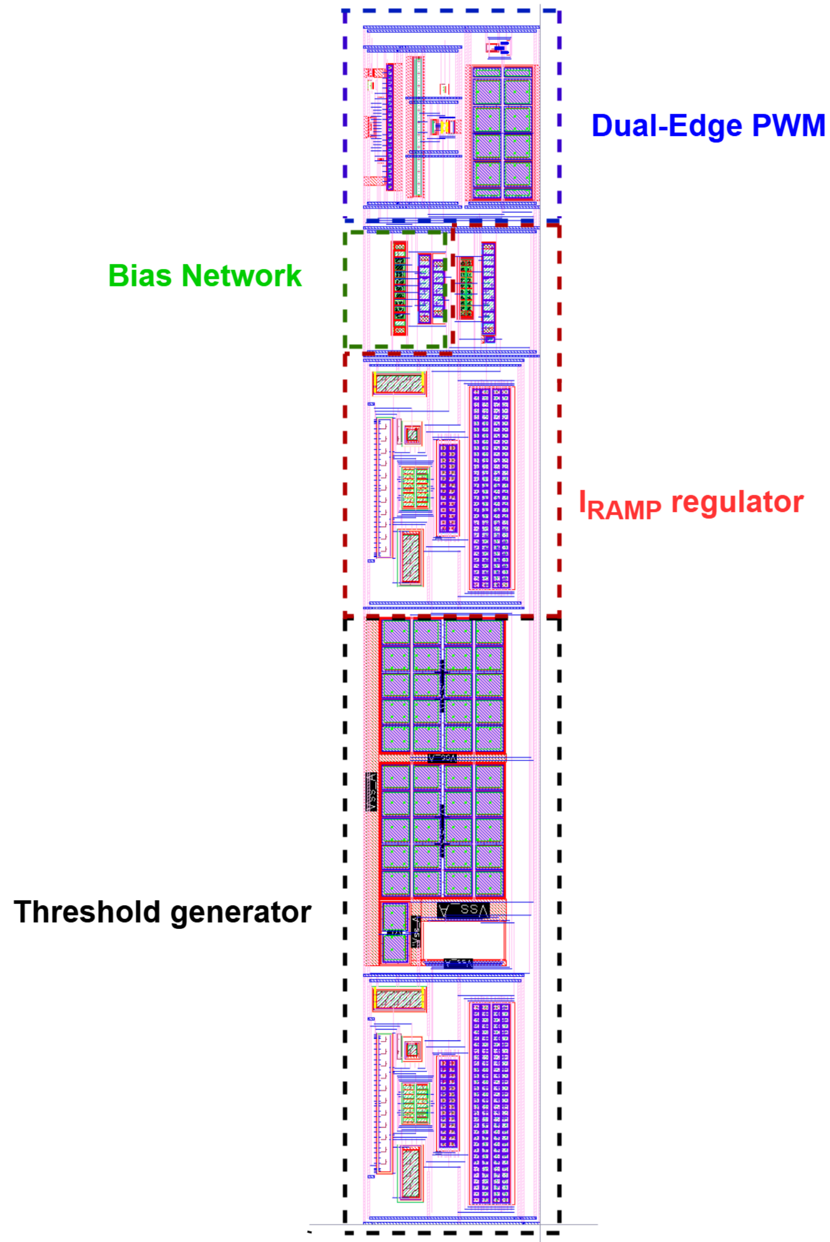


Figure 3.21: Pulse Width Modulator layout.

3.2 Dead Time Manager - control logic

As mentioned at the beginning of this chapter, dead times, during which both power switches are off, must be introduced in switching converters. This precaution is essential to prevent simultaneous activation of the High Side and Low Side transistors, which would result in a large, detrimental cross-conduction current from V_{in} to ground.
The *Dead Time Manager (DTM)* is a crucial component of DCDC converters' control circuit, responsible for introducing and regulating the dead times, τ_1 and τ_2. Figure 3.22 illustrates its working principle. The PWM signal, generated by the previously described PWM modulator, serves as a reference for determining when the Low Side and High Side transistors must be turned off (on the rising edge and falling edge of PWM signal, respectively). Using chains of starved inverters, a delay is introduced between the falling edge of the Low Side's gate signal ($Gate_{\text{LS,CORE}}$) and the rising edge of the High Side's gate signal ($Gate_{\text{HS,CORE}}$), as well as between the falling edge of $Gate_{\text{HS,CORE}}$ and the rising edge of $Gate_{\text{LS,CORE}}$.

During dead times, the inductor's current must find a path where to flow. This path is provided by the bulk diodes of the power transistors, which start conducting when the phase node is pulled below ground by a positive inductor current or when it is pushed above V_{in} by a negative inductor current. This phenomenum, however, causes power dissipation, reducing the overall efficiency of the converter. Therefore, it is crucial to control and minimize the duration of dead times. In the case of the designed DTM, such regulation is achieved by adjusting the current flowing through a chain of starved inverters using external resistors in a way similar to the one used in the I_{RAMP} *regulator*.

Figure 3.23 presents the schematic of the implemented Dead Time Manager (DTM) with a particular focus on the control logic designed in this thesis. From the input signals PWM and $\overline{PWM}$, delay blocks consisting of chains of starved inverters generate the following delayed signals:

- PWM_{3n}, with a delay of approximately 3 ns;
- $PWMd_{\text{LS}}$, $PWMBd_{\text{LS}}$, $PWMd_{\text{HS}}$, and $PWMBd_{\text{HS}}$, with delays that can be adjusted using external resistors $R_{d,\text{LS}}$ and $R_{d,\text{HS}}$.

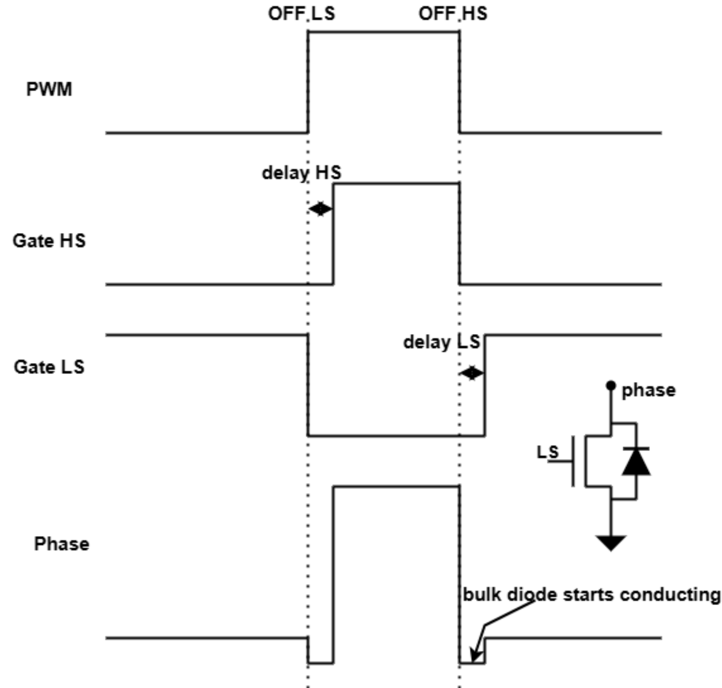


Figure 3.22: Dead Time Manager (DTM) working principle.

Focusing on the low side, a pulse signal $Pulse_{\mathrm{LS}}$ with a duration of 5 ns indicates the falling edge of $PWMd_{\mathrm{LS}}$ and sets the node Mem_{LS} to logic "1". At this point, $Gate_{\mathrm{LS,CORE}}$ can become "high" if:

- the high side is off $(toLS, B = 0)$,
- PWM_{3n} is "low",
- the control circuit is enabled $(EN = 1)$,
- the low side is not disabled $(LS_{\mathrm{disable}} = 0)$.

Otherwise, it remains "low". This configuration generates a dead time $\tau_2 = \max(0, Delay_{\mathrm{LS}} - 3\,\mathrm{ns})$.
Similarly, for the high side, the $Pulse_{\mathrm{HS}}$ signal sets $Gate_{\mathrm{HS,CORE}}$ to "high" when the low side is off $(gLS, B = 1)$ and PWM_{3n} is "high". This creates a dead time $\tau_1 = \max(0, Delay_{\mathrm{HS}} - 3\,\mathrm{ns})$.

Using PWM_{3n} as the reference signal instead of PWM allows for more flexibility in modulating the dead times, overcoming the limitation represented by the fact that the $Delay_{\mathrm{LS}}$ and $Delay_{\mathrm{HS}}$ blocks always introduce a minimum delay.

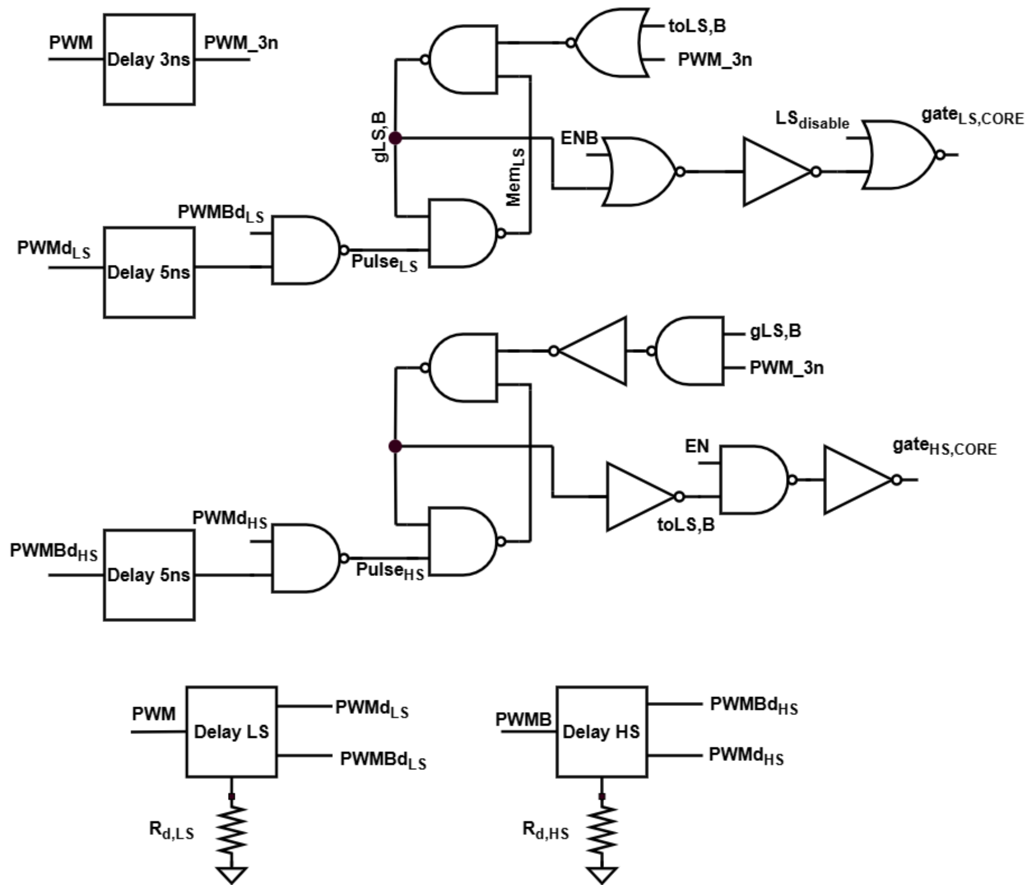


Figure 3.23: Schematic of the dead time manager control logic.

Figure 3.24 and Table 3.7 showcase the outcomes achieved by the designed Dead Time Manager block. The figure illustrates the timing diagrams and signal transitions across the DTM logic. Meanwhile, the table shows the limited impact that the control logic alone has on the introduced *dead times* across corner and Montecarlo simulations.

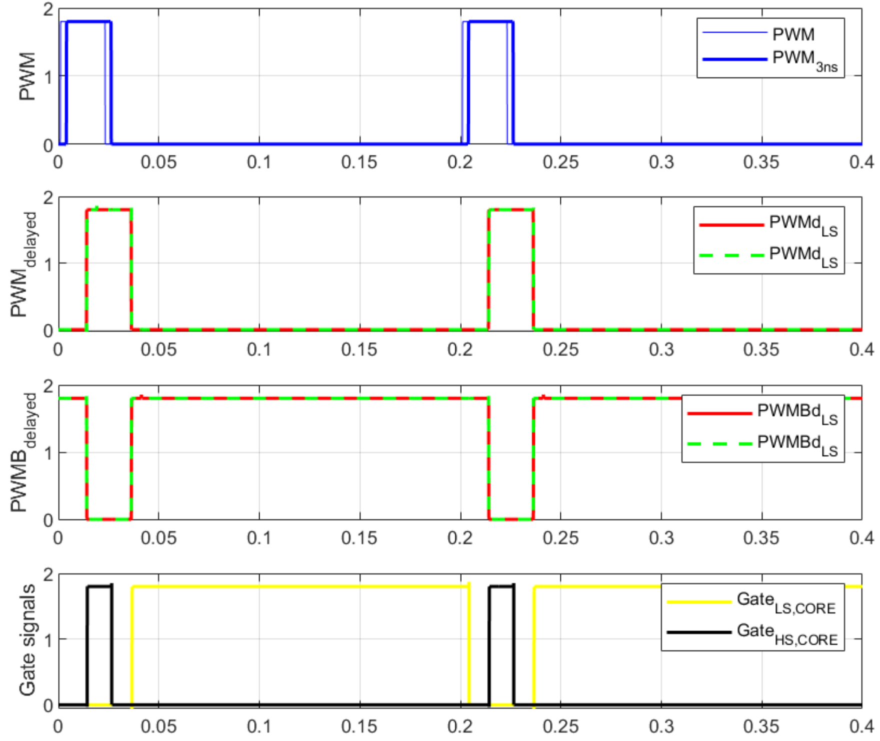


Figure 3.24: Signal transitions across the *Dead Time Manager* control logic.

	min	**max**
τ_1 **[ns]**	**9.981**	**10.31**
τ_2 **[ns]**	**10.02**	**10.28**

Table 3.7: 10 ns *dead times* fluctiation across different simulation corners.

3.3 High Voltage Comparator

There are different ways to implement the switches of *Switched Mode Power Supplies* (SMPS). The control circuit developed in this work is designed to operate with a half-bridge power stage using NMOS transistors for both the high and low sides. This choice is common because NMOS transistors have lower on-resistance per unit area compared to PMOS transistors, which helps minimize power losses and inefficiencies due to voltage drops across the power transistors. Additionally, GaN technologies do not provide good PMOS transistors, further supporting the choice of NMOS transistors.
However, using NMOS transistors for the high side has a drawback: their source node is connected to *phase*, requiring the gate voltage to surpass the input voltage V_{in}.
To translate the high side signal from the 3.3V voltage domain to the high side voltage domain referenced to *phase*, an innovative high voltage level shifter has been developed. This level shifter consists of two parts, as shown in Figure 3.25:

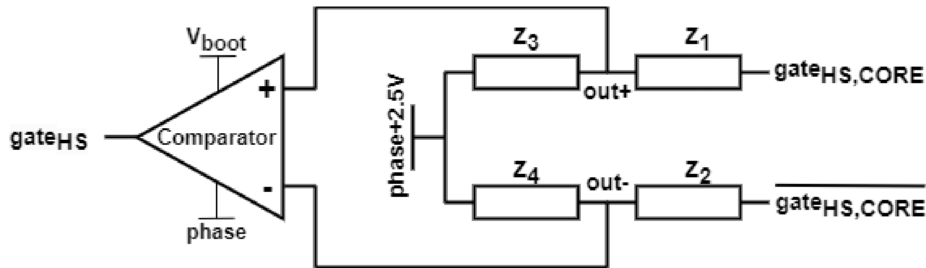


Figure 3.25: Level shifter schematic.

- A resistive voltage divider generates a differential output $(\text{out}_+ - \text{out}_-)$ with a magnitude of a few hundred millivolts. The polarity of this output depends on $\text{gate}_{\text{HS,CORE}}$: it is positive when $\text{gate}_{\text{HS,CORE}}$ is high and negative when it is low.
- A comparator that senses the differential output and encodes the result in a digital, phase-referenced signal driving the high side power switch.

The comparator developed within this thesis is shown in Figure 3.26. It consists of a *single-stage* symmetric OTA with a positive feedback loop that

ensures fast switching of the output with symmetric rise and fall times. This design has also proven necessary to guarantee correct operation under radiation. The 3.3V rated transistors used in this design, in fact, perform particularly poorly under radiation due to their thicker gate oxide, which collects more charges. Simulations have shown that the V_{th} shift for these transistors at 200 Mrad is large enough to make the comparator insensitive to input voltage differences of a few hundred millivolts.

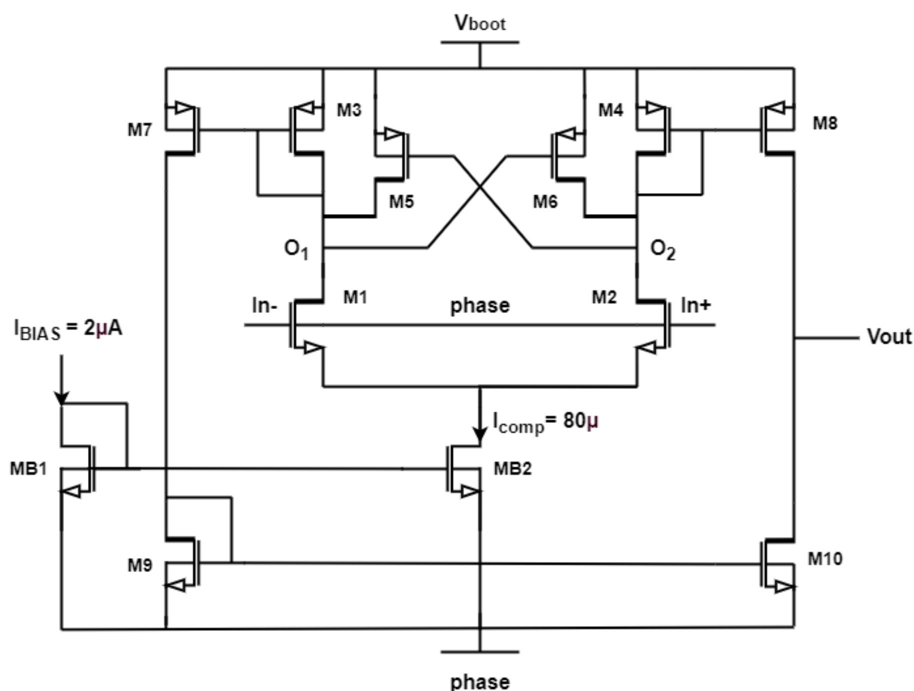


Figure 3.26: High side level shifter's comparator.

	min	**max**
$\tau_{\textbf{rising}}$ **[ns]**	0.941	1.433
$\tau_{\textbf{falling}}$ **[ns]**	0.964	2

Table 3.8: Level Shifter comparator delays.

As $In+$ becomes larger than $In-$, $M2$ starts sinking more current, thus decreasing the gate voltage of $M5$, which then starts pushing more current into

node $O1$, increasing its voltage. Simultaneously, as $O1$ increases, the gate voltage of $M6$ increases, and its drain current decreases, thus accelerating the discharging of node $O2$ operated by $M2$. A similar process occurs when instead $In-$ becomes larger than $In+$

Table 3.8 shows the results from simulations of the comparator's switching time for rising and falling transitions of the output.

3.4 Power stage driver

To validate the operation and performance of the designed blocks, we considered a test setup using a 20V to 2.5V Buck converter based on an earlier project developed by the DCDC team [12].
The integrated *half-bridge* was implemented using laterally diffused NMOS transistors rated for 30V drain voltage and 3.3V gate voltage. These transistors' sizes, detailed in Table 3.9, have been optimized to guarantee high efficiency and low losses.

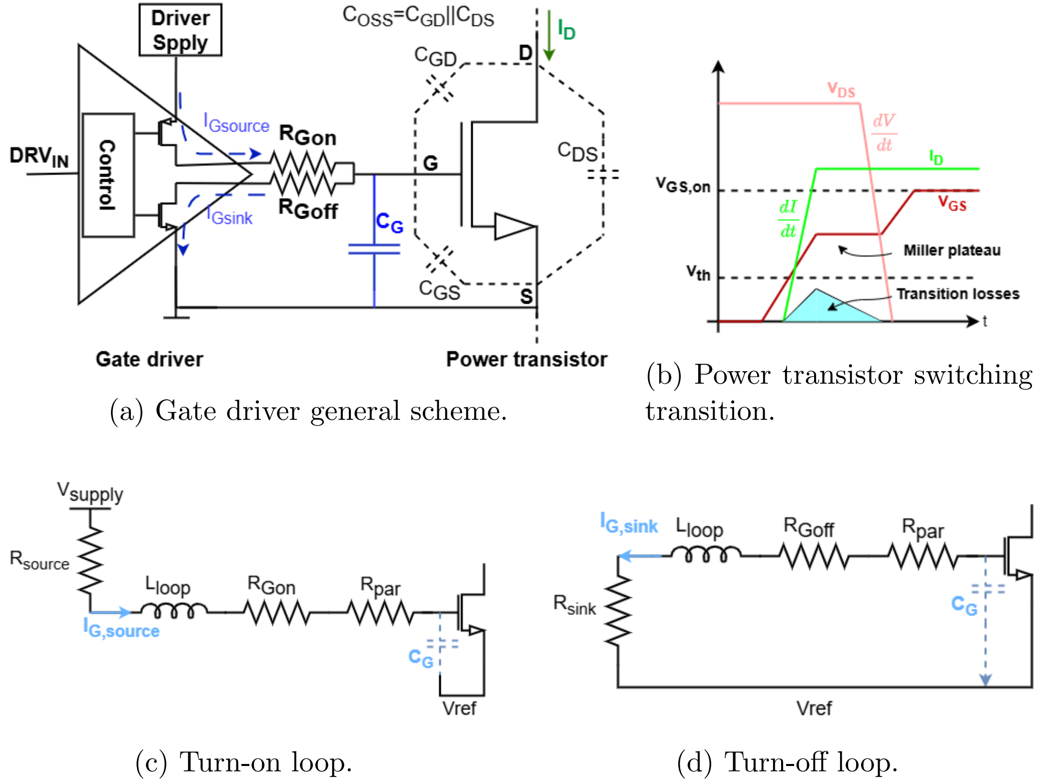
Parameter	High Side	Low Side
$W_{\mathbf{tot}}[\mu m]$	**170000**	**400000**
$L[\mu m]$	**0.6**	**0.6**
$R_{\mathbf{on}}[m\Omega]$	**70.38**	**20.94**

Table 3.9: Optimized sizes of the high and low side transistors.

Within this context, gate drivers have been designed for the low side (Figure 3.28) and high side (Figure 3.29) power transistors.
Figure 3.27 shows the typical structure of a power transistor gate driver. To turn it on, its gate gets connected to the supply voltage ($3.3V$ for the low side,$V_{\text{bootstrap}}$), while to turn it off the gate is pulled to the source potential. The gate of the large power transistor can be represented as a capacitive load C_G. The larger the currents $I_{\text{G,source}}$ and $I_{\text{G,sink}}$, the faster the rate of change of V_{GS}. The gate currents are limited by parasitic resistances in the turn-on/off loops (R_{par} and $R_{\text{G,on/off}}$ in Figure 3.27(c)(d))), but they also prevents possible ringing or gate overshoot/undershoot. As shown in the figure below, in fact, accounting for all the parassitic elements of the turnon/off loops, a resonant circuit results consisting of the gate capacitance C_G, the gate resistance $R_{\text{Gon/off}}$ and the parasitic inductance L_{loop} associated to interconnections. In order to have a stable V_{GS}, the gate loop must be dumped, meaning that the total loop resistance must be high enough that the energy stored in L_{loop} is dissipated at the end of the gate charging/discharging process. The dumping factor of the gate loop can be expressed as

$$D = \frac{R_{\text{loop}}}{2}\sqrt{\frac{C_{\text{loop}}}{L_{\text{loop}}}} = \frac{1}{2Q} \tag{3.12}$$

where Q is the quality factor. For $D = 1$ the loop is critically damped and



(a) Gate driver general scheme.

(b) Power transistor switching transition.

(c) Turn-on loop.

(d) Turn-off loop.

Figure 3.27: Gate driver.

no V_{GS} overshoot occur. In this desirable condition the minimum allowed loop resistance is

$$R_{\mathrm{loop}} = 2D\sqrt{\frac{L_{\mathrm{loop}}}{C_{\mathrm{loop}}}} \tag{3.13}$$

In the case of a monolithic integration of all components on the same die, which is the case considered in this work, the parasitic inductance is negligible, meaning that the loop parasitic resistance is large enough to ensure fast and robust switching. However, in the case of an external power stage, as when working with GaN, the loop inductance associated to interconnections can become important. In this case it could be necessary to increase the loop resistance.

In this thesis, a voltage-source controlled gate driver (Figure 3.27 (a)), or

hard-switching driver, has been implemented. It is the simplest way of driving power transistors, but unfortunately also the least efficient one.
Figure 3.27(b) illustrates the typical turn-on transient of this kind of drivers. As the gate voltage V_{GS} surpasses the threshold voltage V_{th}, the drain current I_D begins to rise until V_{GS} reaches the "Miller plateau level" at which the transistor discharges its output capacitance C_{oss} (including C_{DS}, C_{GD}, and other capacitances associated with the switching node). In this phase, the current provided by the gate driver discharges C_{GD} without charging C_{GS}, resulting in a constant V_{GS} until V_{DS} reaches its minimum value.
As previously mentioned, the hard-switching driving scheme is the simplest to implement, but it is not the most efficient due to the occurrence of several losses, known as *dynamic* or *switching* losses, during each switching cycle. The most significant of these are the following:

- Transition losses happen during the brief period when both the non-zero drain current (I_D) and V_{DS} overlap, leading to a peak in the dissipated power. These losses are particularly noticeable during turn-on and turn-off events of the power transistor but can be minimized with fast switching and an effective gate driver, which reduce the area under the power loss triangle (see Figure 3.27(b)).

- Losses are also associated to the charging and discharging of parasitic transistor capacitances.

- Reverse recovery losses occur in silicon transistors when, after the reverse conduction phase, the body diode should block the current but continues to conduct for a brief period. This can result in cross currents and additional significant losses, particularly during hard-switching transitions, where current continues to flow while the drain-source voltage (V_{DS}) is still high.

- Reverse conduction losses arise when the transistor operates in reverse conduction mode during each switching cycle.

Having this theoretical background (from [13]) it is now possible to proceed with the description of the designed drivers.
Focusing on the low side drivers, to handle the parasitic currents coming from the phase node while avoiding spurious switching of the transistors, the turning on and off is divided into several steps.

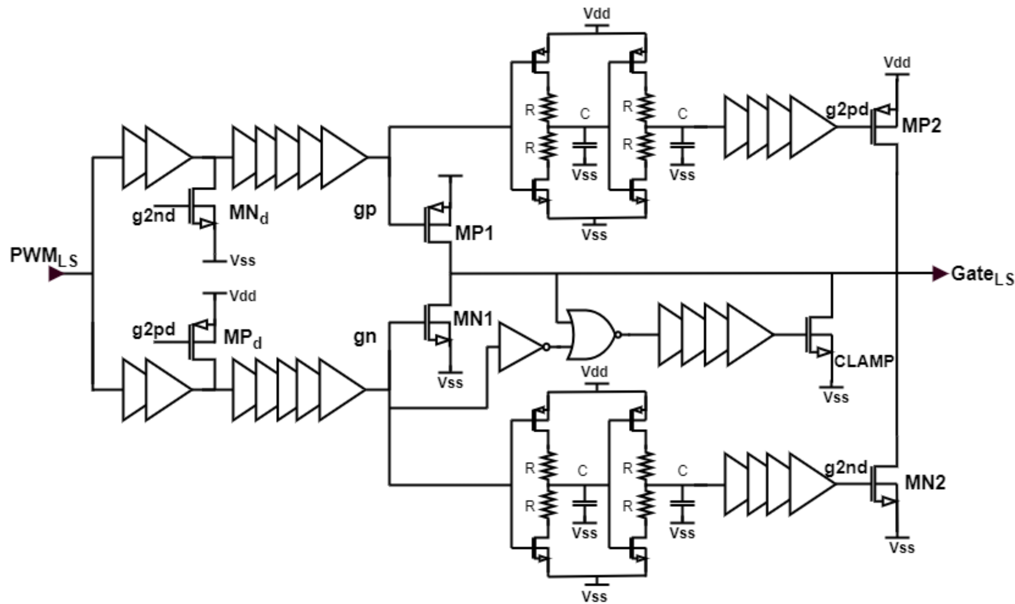


Figure 3.28: Low side switch driver structure.

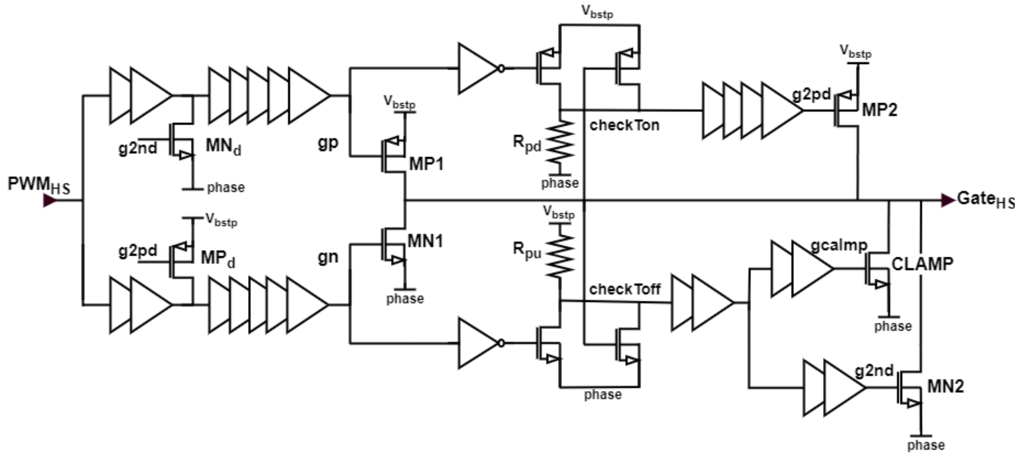
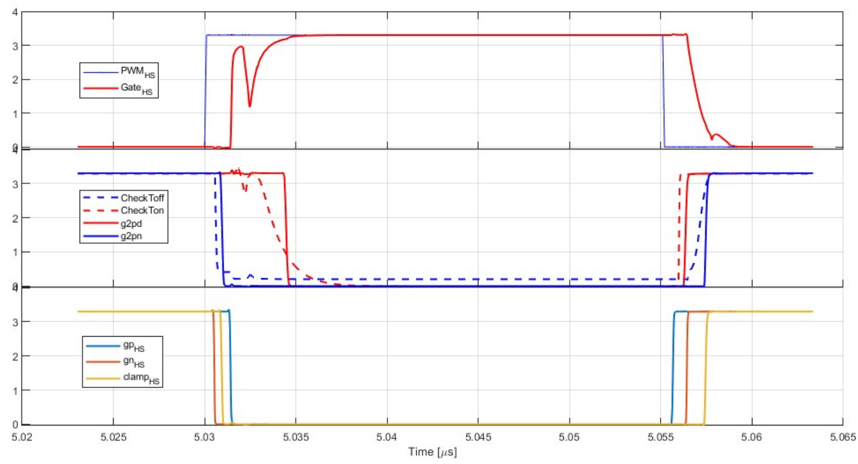


Figure 3.29: High side switch driver structure.

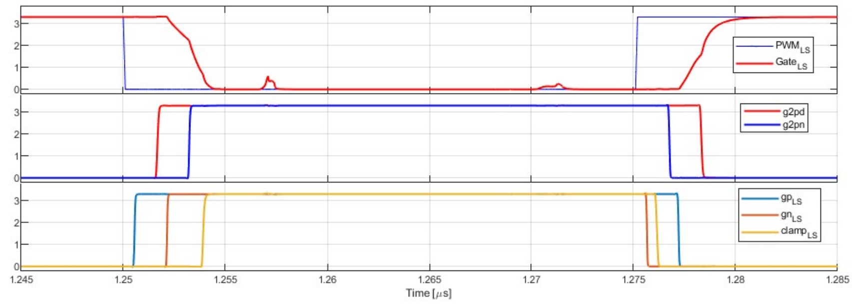
Let's consider the turning-on of the low side: as PWM_{LS} transitions from logic "0" to logic "1", MN1 is turned off, and after a delay which depends on the RC constant of the starved inverters chain, MP1 is turned on. The *dead time* introduced in this way between MN1 and MP1 serves to reduce losses,

which can be significant given the large sizes of the two transistors. As MP1 turns on, it starts driving the low side gate high. As the low side switch turns on, the gate voltage tends to saturate because of the Miller plateau effect. To counter this plateau in the gate charge characteristic, after a delay of about 2ns introduced by the two starved inverters, a larger transistor MP2 is activated to boost the low side gate charging.
When a "1" to "0" transition of PWM_{LS} is considered, MP1 is turned off, and after a dead time, MN1 is activated and starts discharging the low side gate. After a few nanoseconds, this discharging action is reinforced by the activation of MN2. To prevent charges coming from the rapidly decreasing phase, through parasitic capacitive paths, to interfere with the low side gate voltage, causing spurious turning-on, the gate is clamped by a large transistor that flushes all excess charges when the gate voltage is low enough to trigger the NOR gate output to switch.
A similar approach is used also for the high side, with the key difference being the avoidance of capacitors to prevent reliability issues related to exceeding the Safe Operating Area (SOA) limits at the bootstrap voltage.

The graphs in Figure 3.30 detail the chain of events that lead to the proper driving of the power stage transistors. In Table 3.10, some key parameters are presented, including the rising and falling times of the low and high side gates, as well as the delays introduced by the two drivers.
As a final comment, it is important to clarify that, although the drivers presented here have been tailored for a specific 20V-to-2.5V buck converter, their design still ensures the modularity and generality that are among the purposes of this thesis. By changing the length and/or size ratio of the inverter chains, the values of resistors and capacitors, as well as the sizes of the transistors, it is possible to adapt the drivers to different types of *half-bridge* based switching DC-DC converters.



(a) High side signals.



(b) Low side signals.

Figure 3.30: Signals inside the two drivers.

	min	**max**
$delay_{\mathbf{f,LS}}$ $[ns]$	**2.403**	**9.619**
$delay_{\mathbf{r,LS}}$ $[ns]$	**2.26**	**10.75**
$delay_{\mathbf{f,HS}}$ $[ns]$	**1.151**	**3.63**
$delay_{\mathbf{r,HS}}$ $[ns]$	**1.046**	**5.448**
$\tau_{\mathbf{r,LS}}$ $[ns]$	**1.296**	**5.85**
$\tau_{\mathbf{f,LS}}$ $[ns]$	**1.159**	**3.993**
$\tau_{\mathbf{r,HS}}$ $[ns]$	**0.965**	**5.117**
$\tau_{\mathbf{f,HS}}$ $[ns]$	**1.057**	**3.589**

Table 3.10: Driver's key parameters: delays introduced between the input and the output signals and rising and falling times of the output gate signals.

Chapter 4

Conclusions

This thesis addresses the challenge of designing radiation-tolerant analog blocks for the control units of DC-DC converters, which are essential for efficient power distribution in the next-generation High-Luminosity Large Hadron Collider (HL-LHC) experiments at CERN. Operating in one of the most extreme environments on Earth, characterized by exceptionally high levels of radiation and intense magnetic fields, these circuits require resilience far beyond what standard off-the-shelf components can offer.
For this reason, custom ASICs have been developed using a commercial 0.18 μm high-voltage CMOS technology: a dual-edge pulse width modulator (PWM), the control logic of a Dead Time Manager(DTM), a high-voltage comparator for an innovative level shifter, and gate drivers for power transistors. Each component was optimized not only for performance but also for radiation tolerance, which is crucial given the operational context.

The novel dual-edge PWM circuit is a particularly important achievement, offering improved dynamic response and stability compared to conventional solutions. Extensive simulations under various conditions, including those simulating radiation effects, demonstrated its exceptional robustness. The developed, validated through rigorous corner and Monte Carlo simulations, ensures reliable operation in compliance with the project's specifications.
The control logic developed for the DTM ensures the proper generation of *dead-times* between the activation of the high side and the low side, effectively preventing detrimental cross-conduction.
Equally important was the development of the high-voltage comparator, which represents the final stage of an innovative level shifter based on a

resistive divider, necessary to reference the high-side gate signal to phase. This comparator needed to balance speed with reliability and, by integrating a positive feedback loop, it successfully achieved fast switching times and precise performance, despite the poor performance exhibited by the used 3.3V transistors under radiation.
Finally, the design of the gate drivers for the power stage tansistors posed challenge due to the need to manage large parasitic currents and voltages typical of high-power devices. These drivers were engineered to ensure efficient switching and minimize power losses, an aspect particularly critical in HEP experiments, where space and material minimization constraints are particularly severe.

As previously stated, the primary challenge of this project was ensuring that these circuits could not only survive but also function effectively under the extreme radiation levels anticipated in the HL-LHC environment. This challenge was addressed through a combination of specific design and layout techniques.
In particular, the key strategy employed was “hardening by design” which involved building resilience into the circuits against radiation effects. Using enclosed layout transistors (ELTs) and incorporating guard rings were critical in mitigating these issues, ensuring functionality even as the circuits absorbed significant doses of radiation.
Computer aided simulations with tools like SIMPLIS and CADENCE-innovus played a pivotal role in this work, allowing for the modeling of extreme conditions that these circuits will face. These simulations provided a level of assurance that could not be achieved through *model-driven* design alone, especially considering the highly non-linear nature of some of the developed components, predicting how the circuits would perform under various scenarios, including different process corners, temperature variations, and voltage fluctuations in real-world settings.

While this thesis has successfully met its objectives, several avenues for future research and development could build on the foundations laid by this work. One of the possible aspects for future exploration is, for example, the integration of Gallium Nitride (GaN) technologies with the developed control blocks, that would lead to faster and more robust converters thanks to GaN advantages in terms of speed and efficiency.

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