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Master thesis project MNIS 2023-2024

Design of analog blocks in 65nm technology for calorimetry and time measurement applications

Conception de blocs analogiques en technologie 65nm pour des applications de calorimétrie et de mesure de temps

From February, 19st to August, 19st 2024

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ABSTRACT

The CMS experiment aims to explore and precise the Standard Model, the HGCAL (high granularity calorimeter) is one of the detectors used in this experiment, it requires a chip allowed to measure charges and detect time, in this context, the HGCROC3B chip was proposed. This chip has a preamplifier and ToT (Time over Threshold) discriminator for the calorimetry and a ToA (Time of Arrival) discriminator for time detection. The latest version of this circuit is HGCROC3B which was developed using 130nm Si transistors, it has 72 channels. Since the OMEGA laboratory works almost exclusively with 130nm CMOS transistors, this work consisted of starting the design of the analogue processing block (the channels and bias) of HGCROC3B on 65nm transistors. The main objective of this new design was mainly to check the feasibility of the transfer, and if possible, improve certain parts of the design. The simulation results showed that the blocks designed in 130nm could be adapted in 65nm but that careful verifications needed to be made in terms of mismatch, corners and Monte Carlo. This work therefore acts as a stepping stone for the further development of chips in 65nm with big analog blocks design done. Measurements were also done on the already existing HGCROC3B to further the understanding of the chips.

L'expérience CMS vise à explorer et à préciser le Modèle Standard. Le HGCAL (calorimètre à haute granularité) est l'un des détecteurs utilisés dans cette expérience, et il nécessite une puce capable de mesurer des charges et de détecter le temps. Dans ce contexte, la puce HGCROC3B a été proposée. Cette puce comporte un préamplificateur et un discriminateur ToT (Time over Threshold) pour la calorimétrie, ainsi qu'un discriminateur ToA (Time of Arrival) pour la détection du temps. La dernière version de ce circuit, HGCROC3B, a été développée en utilisant des transistors en silicium de 130 nm et possède 72 canaux. Étant donné que le laboratoire OMEGA travaille presque exclusivement avec des transistors CMOS de 130 nm, ce travail a consisté à commencer la conception du bloc de traitement analogique (les canaux et le biais) de la HGCROC3B sur des transistors de 65 nm. L'objectif principal de cette nouvelle conception était principalement de vérifier la faisabilité du transfert et, si possible, d'améliorer certaines parties du design. Les résultats de simulation ont montré que les blocs conçus en 130 nm pouvaient être adaptés en 65 nm, mais que des vérifications minutieuses devaient être faites en termes de mismatch, de corners (PVT) et de Monte Carlo. Ce travail sert donc de tremplin pour le développement ultérieur de puces en 65 nm avec des analogiques déjà conçus. Des mesures ont également été effectuées sur la HGCROC3B existante pour approfondir la compréhension des puces.

L'esperimento CMS mira a esplorare e a precisare il Modello Standard. L'HGCAL (calorimetro ad alta granularità) è uno dei rivelatori utilizzati in questo esperimento e richiede un chip in grado di misurare le cariche e rilevare il tempo. In questo contesto, è stato proposto il chip HGCROC3B. Questo chip ha un preamplificatore e un discriminatore ToT (Time over Threshold) per la calorimetria e un discriminatore ToA (Time of Arrival) per il rilevamento del tempo. L'ultima versione di questo circuito, HGCROC3B, è stata sviluppata utilizzando transistor al silicio di 130 nm e ha 72 canali. Poiché il laboratorio OMEGA lavora quasi esclusivamente con transistor CMOS di 130 nm, questo lavoro ha riguardato l'inizio della progettazione del blocco di elaborazione analogica (i canali e il bias) dell'HGCROC3B su transistor di 65 nm. L'obiettivo principale di questo nuovo progetto era principalmente verificare la fattibilità del trasferimento e, se possibile, migliorare alcune parti del

design. I risultati delle simulazioni hanno mostrato che i blocchi progettati a 130 nm potevano essere adattati a 65 nm, ma che dovevano essere effettuate attente verifiche in termini di mismatch, di corners (PVT) e di Monte Carlo. Questo lavoro serve quindi da trampolino di lancio per lo sviluppo ulteriore di chip a 65 nm con blocchi analogici già progettati. Sono state inoltre effettuate misurazioni sull'HGCROC3B esistente per approfondire la comprensione dei chip.

CONTENTS

GLOSSARY

OMEGA: organisation de microélectronique générale avancée

CAD: computer-aided design

ASIC: application-specific integrated circuit

HGCROC: high granularity calorimeter read-out chip

HGCAL: high granularity calorimeter

CMS: compact muon solenoid

CERN: centre européen de recherche nucléaire

LHC: large hadron collider

ATLAS: a toroidal LHC apparatus

CM: common mode

MIP: minimum ionising particle

RAM: random access memory

PLL: phase-locked loop

I2C: inter-integrated circuit

TDC: time to digital converter

IC: integrated circuit

SCE: short channel effect

MOSFET: metal oxide semiconductor field effect transistor

HKMG: high-κ metal gate

ADC: analogue to digital converter

CC: current conveyor

PDK: process design kit

PVT: process voltage temperature

DAC: digital to analogue converter

FPGA: field programmable gate array

PCB: printed circuit board

ToA: time of arrival

ToT: time over threshold

PA: preamplifier

TID: total ionising dose

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INTRODUCTION

Introduction of OMEGA Microelectronics

This training period was carried out at OMEGA (Organisation de Microélectronique Générale Avancée) located in Palaiseau, France.

OMEGA UAR3605 is a microelectronics design centre jointly supervised by CNRS/IN2P3 and Ecole Polytechnique. It is housed in building 404 Annex of the Ecole Polytechnique in Palaiseau. OMEGA is a relatively small lab comprising around fifteen people (microelectronics engineers, PhD students, CAD engineers and HR) designing sophisticated ASICs for nuclear physics, particle physics and astrophysics detectors. The reading of the detectors used in the different physics experiments requires the development of specific micro-electronic circuits including the integration of analogue functionalities (low noise amplifiers, shaping filters, comparators, etc.) and digital (digitalization of data, memory, etc.).

Introduction of the internship

The placement was carried out over six months at OMEGA Microelectronics. The main aim of the project was to transfer analogue blocks from 130nm to 65nm. The chip used as a starting block is, HGCROC3B (Fig. 1), used in calorimetry and time measurements in HGCAL - CMS experiment. Measurements and data analysis of the chip were also done during the placement. Some other tasks have also been achieved but they will not be the subject of this report.

Figure 2: The HGCROC3B chip, photograph taken by André David (CERN)

PART I

CONTEXT

As said previously, this internship was mostly focused, in different ways, on the HGCROC3B chip; this chip will be used in the HGCAL - CMS experiment. In the first place, this chapter aims to contextualise the experiment and the chip. This chapter will also introduce the advantages and inconveniences of scaling down such a chip's technology.

1 HGCAL - CMS

One of the two major general-purpose particle physics detectors constructed on the Large Hadron Collider (LHC, Fig. I.1) at CERN in Switzerland and France is the Compact Muon Solenoid (CMS) experiment. The CMS experiment (Fig. I.2) is designed to explore a broad variety of physics, including particles that potentially constitute dark matter, an extra dimension, and the search for the Higgs boson.

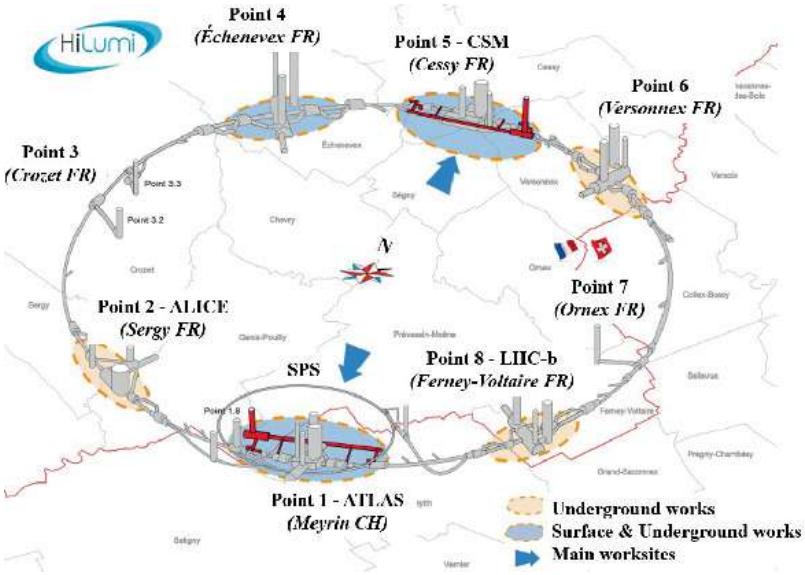


Figure I.1: The structure of the LHC

Modern collider experiments, like the Tevatron at Fermilab, the recently rebuilt Large Hadron Collider (LHC) at CERN, and the now-dimantled Large Electron Positron Collider, have yielded amazing insights into and precise testing of the Standard Model of Particle Physics. The discovery of a particle consistent with the Standard Model Higgs boson, arising from the Higgs mechanism that explains the masses of constituent

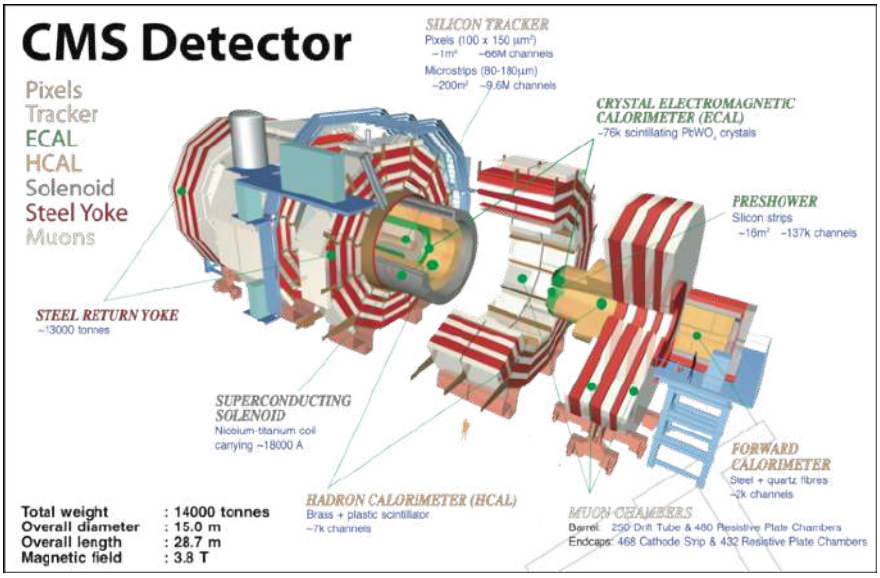


Figure I.2: The structure of the CMS detector

particles, is a primary accomplishment of these investigations (more especially, of the LHC).

Still, a lot of questions remain, which future collider experiments hope to resolve. These include tests of hypothesized dark matter theories (including supersymmetry) and the causes of the apparent imbalance between matter and antimatter in the universe, as well as uncertainty in the mathematical behaviour of the Standard Model at high energies.

The main goals of the experiment are:

- to investigate physics at the TeV scale.
- to investigate the characteristics of the Higgs boson, which CMS and ATLAS have previously found.
- to search for proof of extradimensional dimensions or supersymmetry, two examples of physics that defy the mainstream model.
- to investigate heavy ion collision-related topics.

Similar objectives guided the design of the ATLAS experiment, which is located on the other side of the LHC ring. The two experiments are meant to work in tandem to increase the scope and offer confirmation of results. To accomplish their objectives, CMS and ATLAS employ various technological approaches and detector magnet system configurations.

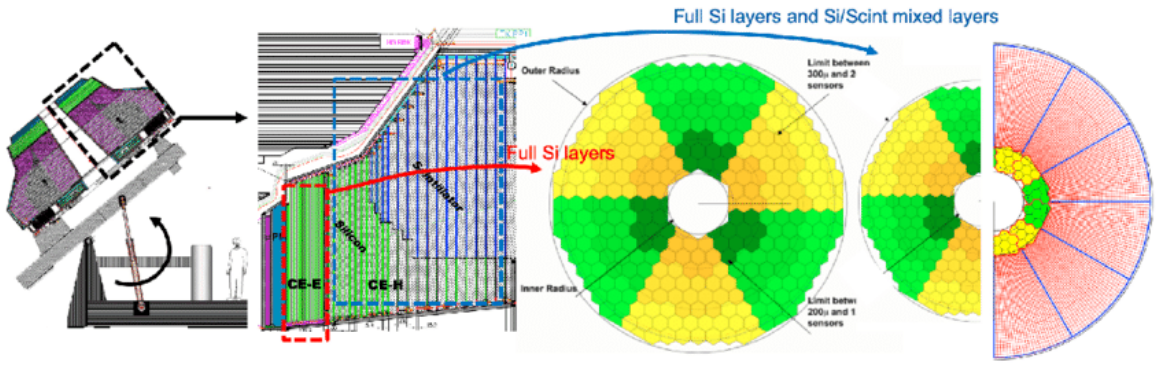


Figure I.3: The structure of the HGCAL

Because of its extremely high readout and trigger granularity, as well as the extreme radiation environment of the CMS endcaps during HL - LHC (High Luminosity Large Hadron Collider) operation, the HGCAL (High Granularity CALorimeter), Fig. I.3, is one of the most ambitious detector projects undertaken. Two materials that can withstand radiation have been chosen: plastic scintillator tiles in less harsh areas and silicon in high-radiation areas. The silicon sensors must be chilled to around $-32°C$ to minimize the effects of radiation degradation. This temperature also permits the use of on-tile silicon photomultipliers for the scintillator readout.

With 50 layers, HGCAL contains over 6.5 million detector channels. The electromagnetic portion consists of the first 28 layers and is based on hexagonal silicon sensors that are divided into hexagonal cells to maximize the useful surface of 8" circular silicon wafers. The resulting hexagonal modules are put on each side of CO2-cooled copper plates. The sensors are positioned between printed circuit boards holding the front-end electronics on one side and high-density copper-tungsten alloy baseplates on the other. The final 12 levels combine both silicon modules and scintillator tiles, while the next eight layers are identical and comprise the front portion of HGCAL's hadronic section. These layers are single-sided and utilize a lighter baseplate. Using two detection technologies maximizes the HGCAL's overall cost while preserving its superior long-term performance.

2 HGCROC3B

HGCROC3B (High Granularity Calorimeter Read Out Chip) will be one of the chips used in HGCAL for calorimetry and time detection in the CMS experiment.

The overall block diagram is described below (Fig. I.4).

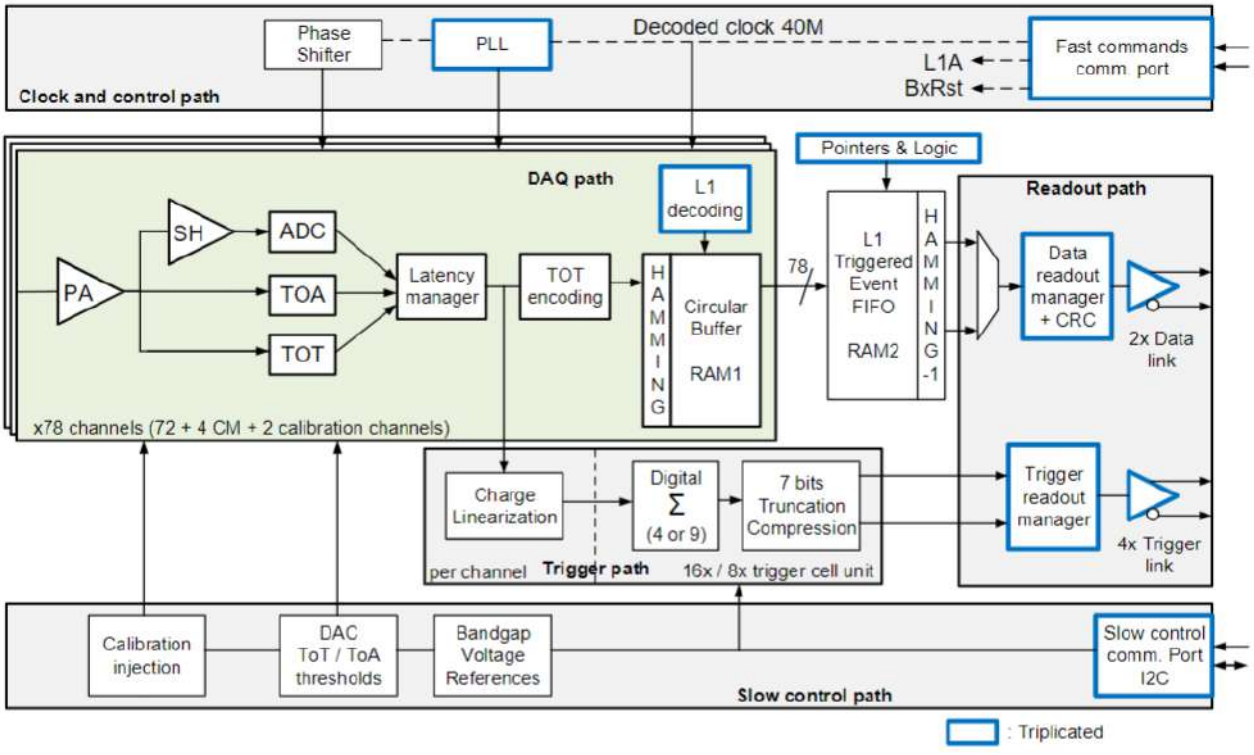


Figure I.4: Block diagram of HGCROC3B

The HGCROC3b chip is made of 72 channels of the full analogue chain providing charge and timing information, 4 common mode (CM) channels for subtracting coherent noise and 2 calibration channels for the MIP calibration. The chip (Fig. I.5) is divided into 2 symmetrical and identical parts as can be seen in the following view of the layout.

In each part, there are 36 normal channels, 2 CM channels, 1 calibration channel, 1 biasing block with its own

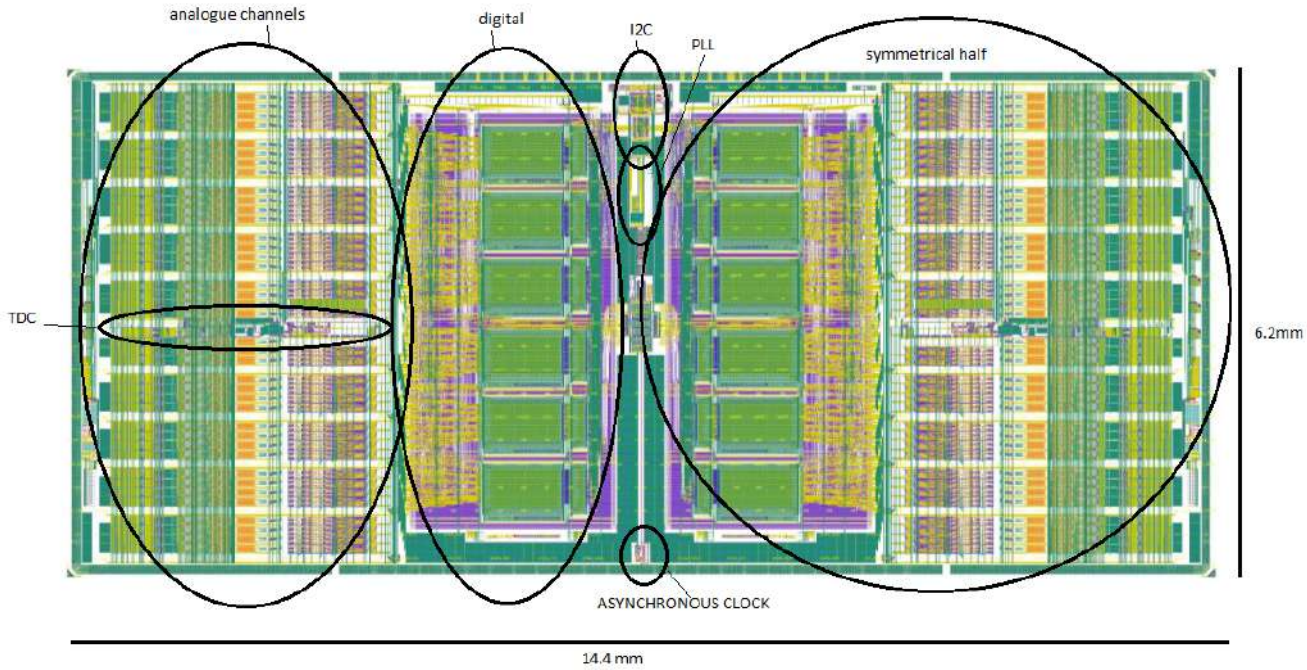


Figure I.5: Layout of HGCROC3B

bandgap and reference voltages, and 1 full digital block with the 512-deep RAM1 and 32-deep RAM2.

Common to the full ASIC are only the PLL (all the clocks used by the chip), the I2C (slow control) and FastCommand (fast control) units, the serializer and differential drivers, an asynchronous clock generator (for the TDC calibration).

Two 1.28 Gbps links are dedicated to sending out the full event information (charge and time) of selected bunch crossings after a L1A trigger request. This path is so referred to as Data path or DAQ path. A 512-deep D-RAM circular memory keeps the entire information (charge and time) for 12.5 μs. After a L1A trigger request, the selected data are sent to the RAM2 while waiting to be sent to the ECON-D concentrator chip.

Four 1.28 Gbps links are devoted to sending out an image of the deposited charge of each bunch crossing event by summing and compressing data over 4 (or 9) channels. These data will contribute to the L1A trigger generation and therefore are processed within the Trigger Path. The data are sent to the ECON-T concentrator chip.

The I2C protocol is used to set or read the more than 7900 parameters of the chip. This part is triplicated to resist the Single Event Effect (SEE). The chip is controlled by the Fast Command block which receives a clock and a command link both at 320 MHz. This allows for configuration of the operating mode of the system: link synchronization, reset, calibration, L1 request, etc. The 40 MHz clock, in phase with the LHC clock, is extracted from the 320 MHz fast command link and provides the clock to the digital part of the ASIC (digital processing, I2C) and to the PLL which generates the other clocks needed to operate the chip: the 640 MHz clock for the 1.28 Gbps links, the phase adjustable 40 MHz clock for the ADCs, the phase adjustable 160 MHz clock for the TDCs.

The front end can be divided into three main sub-parts:

- The preamplifier converts the input charge coming from the silicon diode to an output voltage. It must provide the first amplification of the signal with the best noise performance. In the linear part of the amplifier, the feedback capacitors and feedback resistors provide the gain and the shape of the output signal which is sent to the shaper. From the saturation and above, the feedback discriminator triggers and provides the charge measurement by using the Time Over Threshold technique (TOT). Another discriminator allows us to give the timing information. The preamplifier can be calibrated by injecting

a voltage step through two channel-wise selectable capacitors (0.5pF and 10pF).

- The shaper part is composed of three stages: a Sallen-Key filter, a RC2 filter and a unity gain amplifier to drive the ADC. The peaking time can be adjusted over +/- 20% around 24 ns to compensate for process variations and ensure the out-of-time pileup is below 20%.
- The two discriminators provide the TOT and TOA (Time of Arrival) pulses, each one sent to a dedicated TDC.

3 Interest of scaling

As introduced previously, the aim of this internship was mostly to transfer blocks from the 130nm technology down to 65nm. But, why?

There is a clear trend of scaling of the oxide thickness throughout the years, as illustrated in Figure I.6. We expect the minimum dimension will continue to shrink in the foreseeable future.

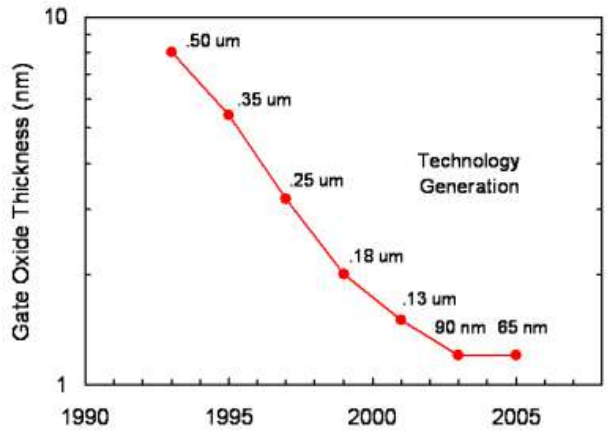


Figure I.6: Gate oxide thickness trend for Intel logic technologies [2]

The desire for scaling can be, at least in part, explained by Moores Law which states that the number of transistors in a dense integrated circuit (IC) doubles every two years (Fig. I.7). If we want the chip to stay the same size, the transistor needs to be physically scaled down to fit.

The scaling can also be for performance, notably the scaling of the oxide thickness t_{ox}. First, the objective is to avoid any problem related to short-channel effects (SCEs) by retaining control of the channel. The second objective is to allow a strong drive current I_d to go through even when the gate voltage V_g is low, thus requiring less voltage to turn the device on. A schematic of the structure of a MOSFET is given, Fig. I.8, for context.

When reducing the gate length of a MOS transistor, the width of the depletion regions around the source and drain also has to be reduced, to avoid effects such as punch-through and charge sharing, illustrated in Fig. I.9a and Fig. I.9b. To scale down the depletion regions and suppress the SCEs, Eq. I.1, the doping concentration of the channel can be increased and the biases applied can be reduced. A higher channel doping will increase the threshold voltage, as shown by Eq. I.2, which makes it more difficult to turn the device on. To control a reasonable threshold voltage, a thinner oxide is necessary.

$$\begin{aligned} x_n &= \sqrt{\frac{2\epsilon_S}{q}\frac{N_a}{N_d}\frac{1}{N_a+N_d}(\Delta V)} \\ x_p &= \sqrt{\frac{2\epsilon_S}{q}\frac{N_d}{N_a}\frac{1}{N_a+N_d}(\Delta V)} \end{aligned} \tag{I.1}$$

where x_n and x_p are the negative and positive depletion layer width with respect to the centre, N_a and N_d

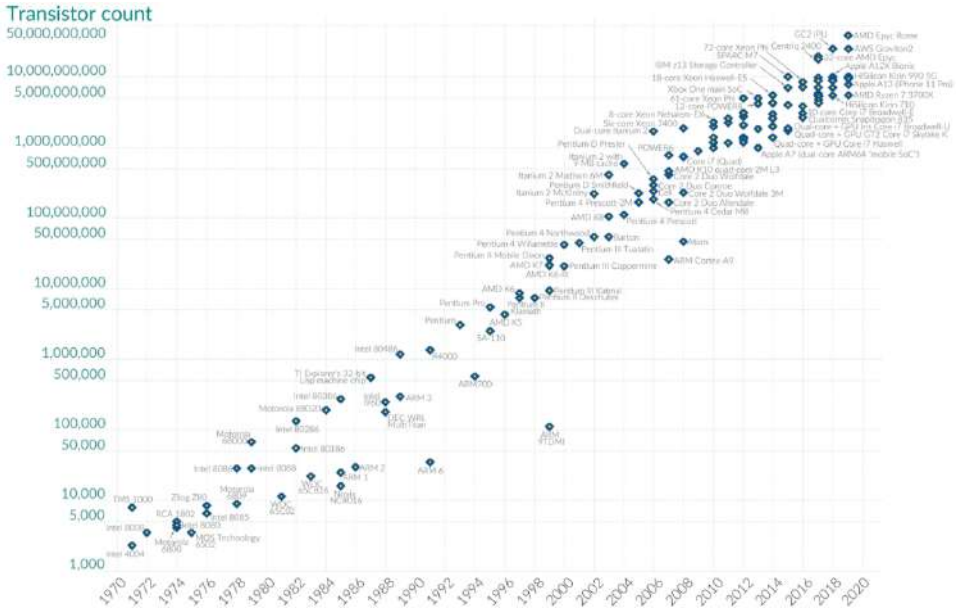


Figure I.7: Transistor counts for microprocessors against dates of introduction

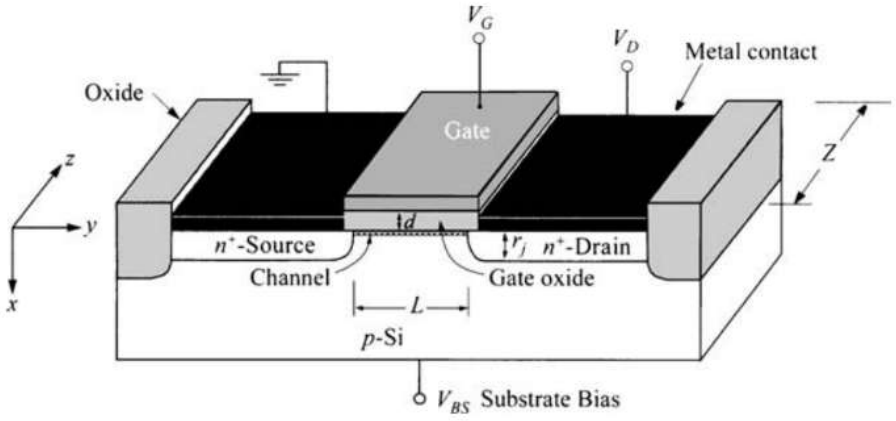


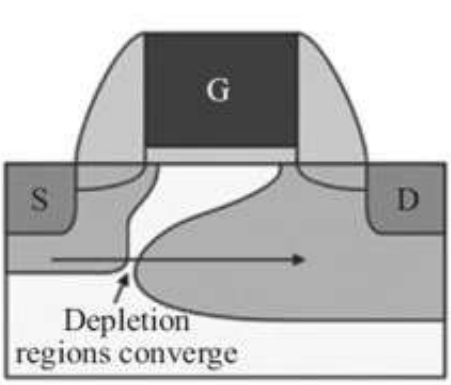
Figure I.8: Schematic diagram of a MOSFET [9]

are the acceptor and donor concentration, ϵ_S is the permittivity of the substrate, q is the electron charge and ΔV is the built-in voltage.

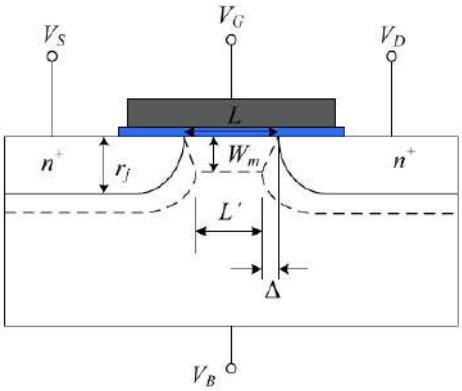
$$\begin{aligned} V_t &= V_{FB} + 2\psi_B + \frac{\sqrt{2\epsilon_S q N_a (2\psi_B)}}{C_{ox}} \\ C_{ox} &= \frac{\epsilon_{ox}}{t_{ox}} \end{aligned} \tag{I.2}$$

where V_{FB} is the flat-band voltage, $2\psi_B$ is the surface potential, ϵ_S is the permittivity of the substrate, q is the elementary charge, N_a is the substrate doping concentration, C_{ox} is the oxide capacitance.

The second objective is a matter of power consumption. Indeed, lowering the gate voltage of the transistor lowers the operating voltage of the IC which is made of an always-increasing number of millions of transistors, and as a result, the power consumption of the IC reduces as well. In theory, the drain current I_d for a MOSFET can be written (using the gradual channel approximation) as Eq. I.3, thus if the gate voltage V_g was to be reduced without any scaling of the device, the charge in the channel would be reduced and alongside it, the drive current would be. But if scaling of the oxide thickness was to be applied according to Eq. I.4 it would



(a) Punch-through effect [6]



(b) Charge sharing effect [1]

Figure I.9: Punch-through and charge-sharing effects

increase the gate capacitance and a smaller voltage would then be able to induce the same charge and the same current.

$$I_{d,sat} = \frac{W}{L}\mu C_{inv}\frac{(V_g - V_t)^2}{2} \tag{I.3}$$

where W is the width of the transistor channel, L is the channel length, μ is the channel carrier mobility, C_{inv} is the capacitance density associated with the gate dielectric, V_g is the gate voltage and V_t is the threshold voltage.

$$C = \frac{\kappa A \epsilon_0}{t_{ox}} \tag{I.4}$$

where A is the capacitor area, κ is the relative dielectric constant of the material, ϵ_0 is the vacuum permittivity and t_{ox} is the thickness of the capacitor oxide insulator.

Different ways of scaling could be used to reach certain performances; Dennard's scaling (scale down all dimensions and voltages of a MOSFET so that the internal electric fields are kept the same), constant-voltage (dimensions are scaled down but voltages remain the same), quasi-constant-voltage, and generalized scaling (dimensions and voltages are scaled down by different factors), strain engineering (use of the $Ge_xSi_{(1-x)}$ alloy system around the Si channel to improve electron and hole mobility) or high-κ dielectric and metal gate (the use of different materials than the common Si and Poly-Si with notably an oxide with a higher dielectric constant, allowing for a physically thicker oxide but better performances, Fig. I.10).

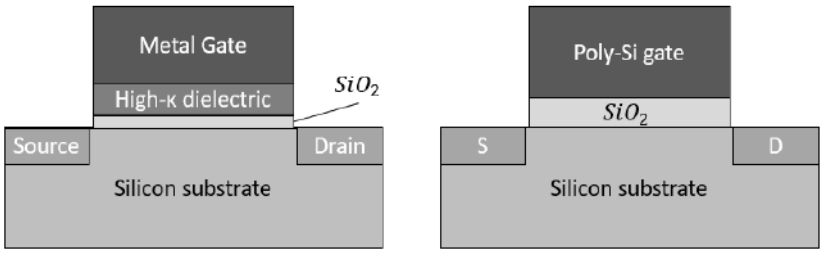


Figure I.10: High-κ/MG and SiO_2/Poly-Si structure

These scaling techniques will not be explained further, but it is worth noting that each semiconductor technology node corresponds more or less to a different technique, starting from 'happy scaling' or Dennard's scaling to strain-engineering to HKMG (high-κ metal gate) and so on, as seen in Fig. I.11.

The important nodes to keep in mind for the work presented in this report are the 130nm and the 65nm nodes.

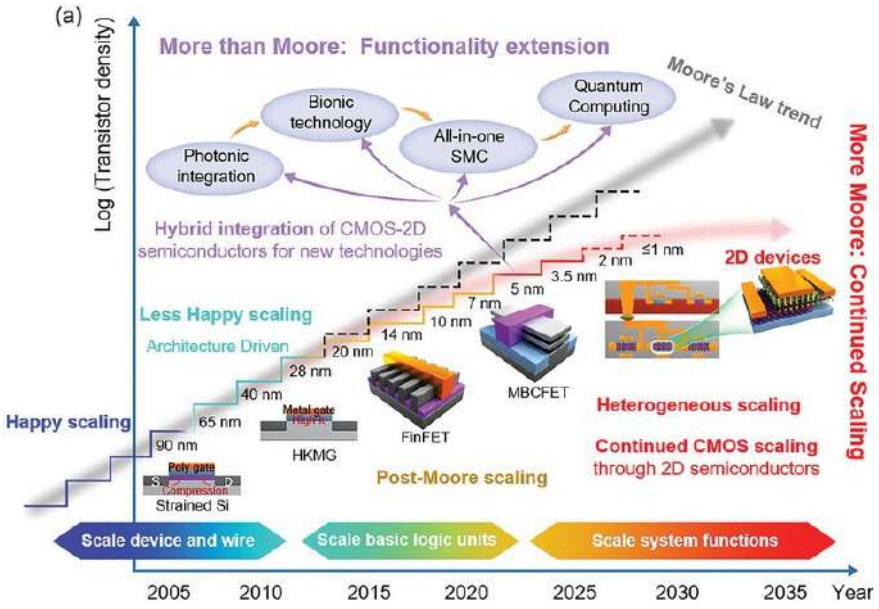


Figure I.11: Scaling trend in time

Most chips at OMEGA have been designed in 130nm, and the design work in this report will be done in 65nm. But, does it make sense to scale down the technology at OMEGA, considering that a decent amount of the chips is analogue?

To answer that question, a quick study of the advantages and inconveniences of scaling, in our specific case, can be done (Tab. I.1):

	130nm	**65nm**
Area	Less compact	Reduction in area of around 60% compared to 130nm This leaves room for more complexity in the digital part
Matching		Better matching
Rad-Hard		65nm demonstrates a better radiation hardness [3]
Speed		Higher transistor current and consequently switching speed (thinner oxide)
Maturity	Somewhat outdated in industry Introduced in 1999	Available since 2005 and used extensively for industrial/automotive
Power		Lower power
Leakage current	Less leakage current (thicker oxide) and reliability degradation	
Design Rules	Less stringent design rules	
Analog Design	Better suited for analogue designs	Smaller dynamic range (lower power supply and lower output resistance of the MOSFETs)
PVT	Less PVT (Process, Voltage, Temperature) variations [10]	
Resistances	Less metal sheet resistance [5]	Approximately three times higher (more focus on smart layout is required)
Cost	Around 300k €/run	Twice as expensive
TDC		Better performances of the TDCs
Link		Faster links

Table I.1: Limitations and advantages of the technologies

In our cases, the main advantages of using 65nm instead of 130nm are the sure availability of technology in manufacturing (130nm is starting to get a little old, and is less and less used), easier collaborations (since other labs are also slowly moving towards 65nm and under, and all of the chips at OMEGA have at least one block designed by another lab) and better radiation hardness (this might be more useful in some chips than others, but a lot of chips used in particle physics need to me rad-hard at least to a certain degree). The main inconveniences are the cost (multiplied by about two for every technology node) and the use of such a technology for mainly analogue chips (scaling is always very beneficial to the digital world but the analogue one always has to make do with it).

PART II

BLOCK DESIGNS

This chapter aims to present part of the design work achieved during this placement, the transfer of the preamplifier will be presented and a new design of a bandgap reference will be explained. Of course, other design works were achieved but introducing them would be redundant.

1 Preamplifier

a Introduction to preamplifiers

Various electronic applications can be constructed using fundamental building blocks. ASIC design typically involves connecting multiple modules, such as amplifiers, analogue-to-digital converters (ADC), discriminators, shapers, current conveyors (CC), etc.

One of the most commonly utilized modules is the amplifier. The primary purpose of an amplifier is to take an input signal and multiply it by a specified gain value. The gain of an amplifier can be set to be positive or negative, increasing or decreasing the magnitude of the input signal. Amplifiers can be configured as single-input and single-output, differential input and single-output, or differential input and output, among other configurations. Single-input, single-output amplifiers consist of a transconductance structure, such as common-source, common-drain, or cascode, with the appropriate load structure. Each amplifier is designed to meet specific requirements. Table II.1 outlines the fundamental parameters that must be characterized in an amplifier.

Performance	**Symbol**	**Unit**	**Definition**
Gain	A_v	dB	Amplifier output voltage over the input voltage.
Gain-bandwidth	f_{GBW}	Hz	Frequency at which the amplifier gain is unity.
Dynamic range			Ratio between smallest and largest signal.
Offset voltage (pedestal)	V_{os}	V	Amplifier output voltage when the input voltage is zero.
Noise (flicker or 1/f)		V/Hz	Random noise generated by trapping and release of charge carriers at the oxide-semiconductor interface.
Noise (thermal)		V/Hz	Noise generated by random thermal movement of electrons.
Power dissipation	P	W	Total power dissipated by the amplifier.
Slew rate	S_r	V/μS	Maximum current which can be delivered to the load.
Power supply rejection ratio	$PSRR$	dB	Attenuation from the power supply to the output.

Table II.1: Amplifier basic characteristics

b Design

Most of the design work done during this placement consisted of transferring blocks from the technology 130nm to 65nm and creating test benches to compare the results.

As such, the structure of the already existing (in HGCROC3B) preamplifier was not modified, and the method to adapt the design was simple:

- copy the design using the new PDK.
- create extensive test benches to test the new design and fully compare it to the one in 130nm.
- modify the sizes of the transistors to reach similar or better performances.
- change the structure if necessary (this was not needed for now).
- layout the block and test it again after extraction.

In theory, the sizes of the transistors would not need to be changed to reach the same performances, but, in reality, the transistors have slightly different characteristics, hence the necessary change of the transistors' sizes.

The design of the preamplifier is the following, Fig. II.1:

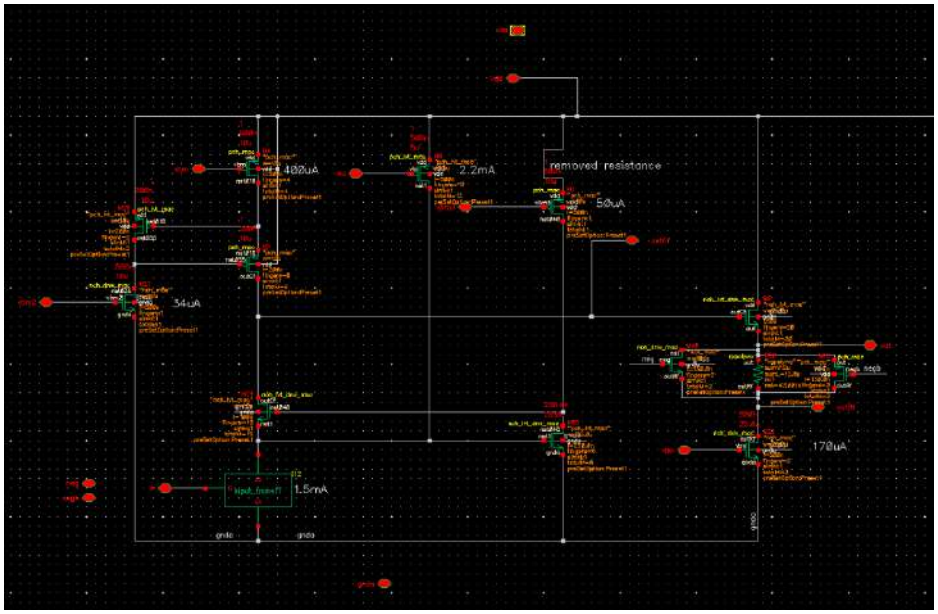


Figure II.1: Preamplifier schematic

c Simulations results

The Bode plots can be found below (Fig. II.2 and II.3), and the phase margin, gain and poles can be read from there.

The dynamic range of the preamplifier can also be seen in Fig. II.4, the dynamic range should be as large as possible.

The structure of the preamplifier was always kept identical to the one in 130nm, but many modifications in terms of transistor sizes were done to reach the following performances (Tab. II.2):

- improved speed
- reduced noise

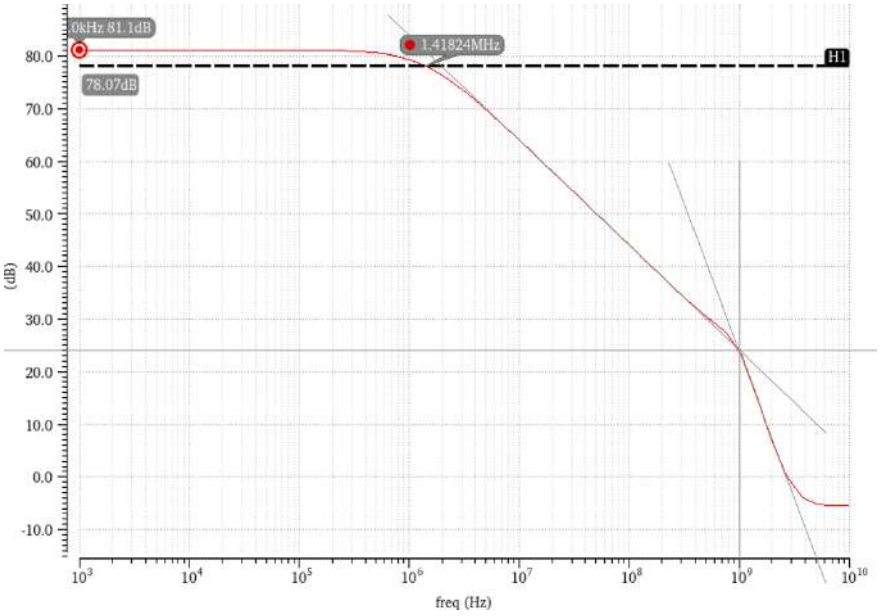


Figure II.2: Preamplifier simulations results: Gain

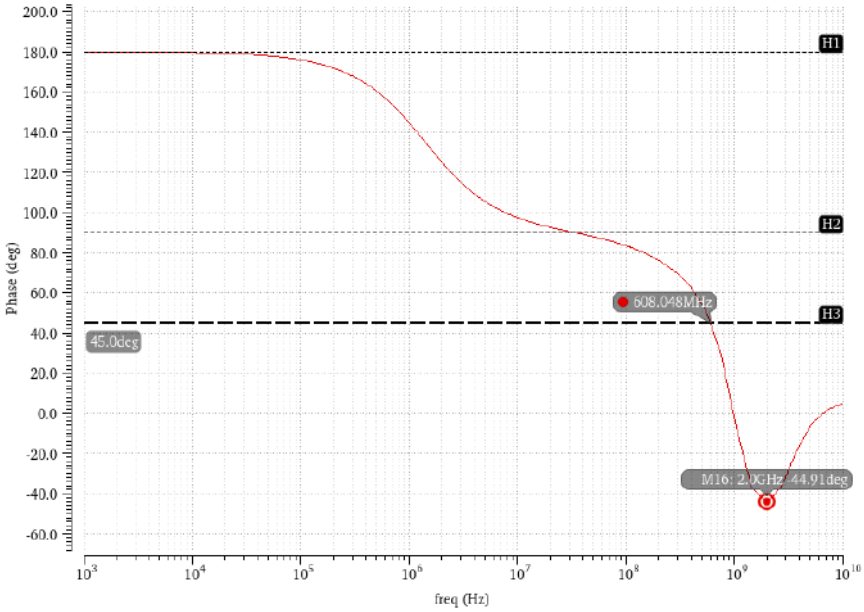


Figure II.3: Preamplifier simulations results: Phase

- gain above 80 dB
- similar dynamic range
- similar linearity
- similar power consumption
- faster rising time of output signals

Other simulations such as PVT and Monte Carlo were done to be able to design a block as stable as possible but the plots will not be shown here.

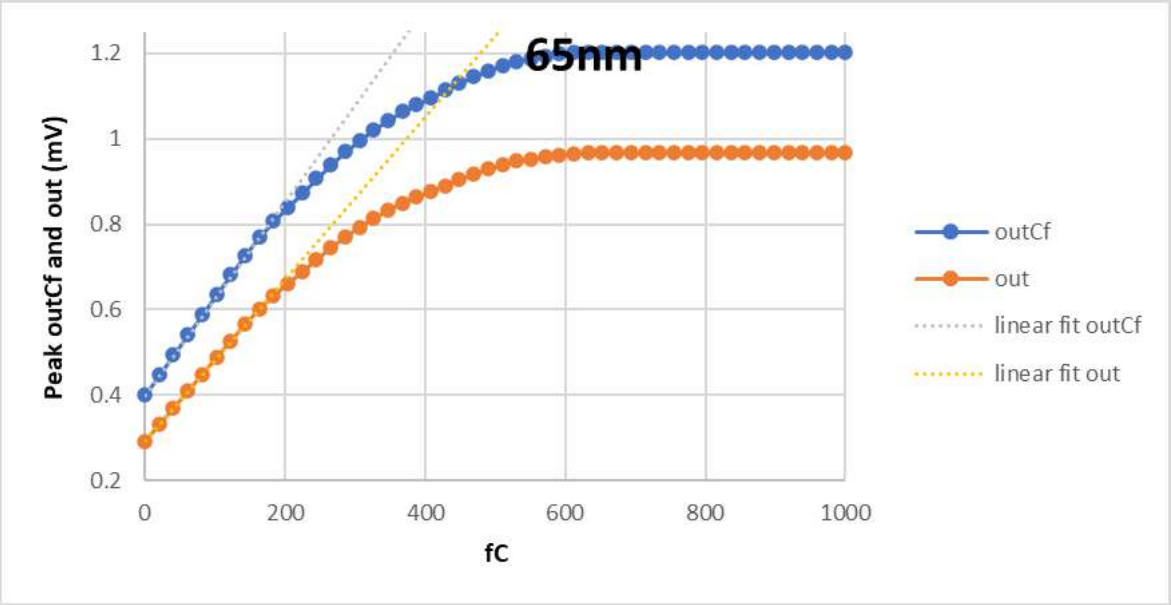


Figure II.4: Preamplifier simulations results: Dynamic range

	130nm	**65nm**
rmsNoise (μV)	822.6	749.8
Phase Margin (°)	124	141
Preamp current (mA)	2.573	2.512
Open Loop Gain (dB)	119.9	81.07
Fist pole (Hz)	11.2k	1.42M
Secong pole (Hz)	380M	1G
Rising time out (ns)	6.893	5.643
Dynamic range (outCf) (mV)	784	802
Dynamic range (out) (mV)	655	674

Table II.2: Comparison preamplifier performances 130nm/65nm

2 Bandgap

a Introduction to bandgaps

A bandgap reference or bandgap voltage reference is an electronic circuit designed to produce a stable reference voltage that is independent of temperature, power supply variations, processes and, in our case, radiations. The term "bandgap" in this context is derived from the use of the bandgap energy of silicon to create a voltage that remains relatively constant across different temperatures.

Most of the time, a bandgap reference circuit generates a voltage equal to the bandgap energy of silicon (approximately 1.25 volts) over a wide range of temperatures. The circuit exploits the predictable changes in the forward voltage drop of a diode with temperature to create a stable output voltage. Heres a simplified explanation of how it works:

1. Temperature Dependence of Diodes: The forward voltage drop of a diode decreases with increasing temperature. This effect is known as the negative temperature coefficient. Conversely, the voltage difference between two diodes operating at different current densities (proportional to their thermal voltage) increases with temperature. This effect has a positive temperature coefficient.

2. Combining Two Opposite Temperature Coefficients: By carefully combining these two effects in a circuit,

the temperature dependencies can be balanced out. Typically, one part of the circuit generates a voltage with a positive temperature coefficient, and another part generates a voltage with a negative temperature coefficient. When these two voltages are combined, the result is a temperature-independent voltage output.

3. Output Voltage: The output voltage of a bandgap reference circuit is typically around 1.2 to 1.25 volts. This is because this voltage corresponds to the theoretical bandgap of silicon at absolute zero temperature. However, practical circuits are designed to be temperature-independent at room temperature or over a specified temperature range.

Bandgap references are widely used in many electronic devices and systems where a stable voltage reference is essential, including:

- Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs): Provide a stable reference voltage to ensure accurate conversion between analogue and digital signals.
- Voltage Regulators: Maintain a constant output voltage despite changes in input voltage, load, or temperature.
- Oscillators: Provide stable voltage references for maintaining consistent oscillation frequencies.
- Sensor Circuits: Ensure that sensor readings are accurate and reliable across varying environmental conditions.

A bandgap reference is a crucial building block in many electronic circuits, providing a stable and temperature-independent reference voltage. It leverages the properties of semiconductor materials and careful circuit design to achieve its stability and precision, making it invaluable in a wide range of applications.

b Design

The other design presented in this report (preamplifier) was simply transferred from 130nm to 65nm, the structure was already chosen and did not need to be changed, but this design was made from scratch. This design was not transferred for a couple of reasons: first, this is a good learning opportunity, and second, bandgap references are extremely technology-sensitive.

The design is provided Fig. II.5:

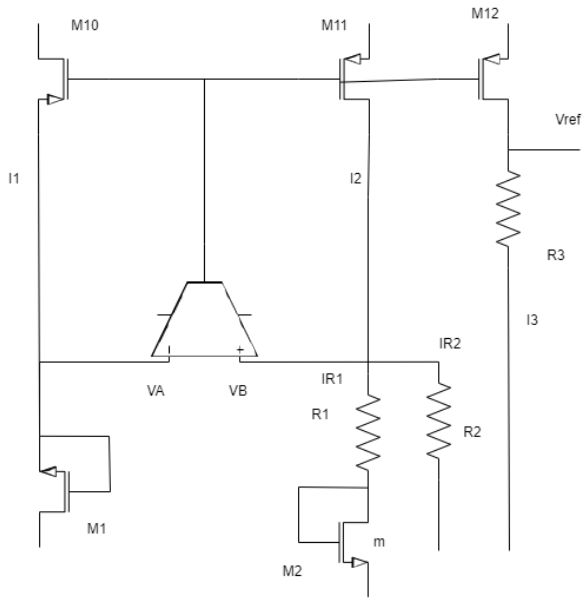


Figure II.5: Schematic of the bandgap reference

$$\begin{aligned} V_A &= V_B \\ I_{ds1} = I_1 &= I_2 = I_3 \\ I_2 &= I_{R1} + I_{R2} \end{aligned} \tag{II.1}$$

M1 and M2 are in weak inversion. The equations corresponding to weak inversion are Eq. II.2.

$$\begin{aligned} I_{ds} = I_t \frac{W}{L} exp(\frac{q(V_{gs} - V_{th})}{nkT} \\ I_t = 2n\mu C_{ox}(\frac{kT}{q})^2 \\ V_{gs} = nV_T ln(\frac{I_{ds}L}{I_T W}) + V_{th} \\ V_T = \frac{kT}{q} \end{aligned} \tag{II.2}$$

With k the Boltzmann's constant, q the electron charge, n the slope factor and V_{th} the threshold voltage.

This specifically gives Eq. II.3

$$\begin{aligned} V_{gs1} = nV_T ln(\frac{I_{ds1}L_1}{I_T W_1}) + V_{th} \\ V_{gs2} = nV_T ln(\frac{I_{ds2}L_2}{I_T W_2}) + V_{th} \end{aligned} \tag{II.3}$$

$V_A = V_B$ gives Eq. II.4

$$\begin{aligned} V_{gs1} &= V_{R1} + V_{gs2} \\ V_{R1} = \Delta V_{gs} = n\frac{kT}{q} ln(m) &= I_{R1} R1 \\ I_{R1} &= n\frac{kT}{qR1} ln(m) \end{aligned} \tag{II.4}$$

And $I_{R2} = \frac{V_B}{R2}$ gives Eq. II.5

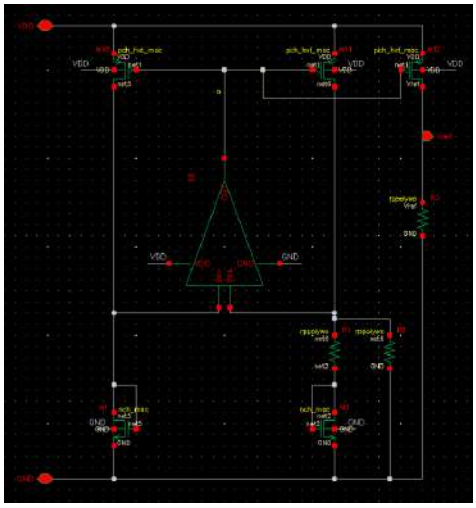
$$I_{R2} = \frac{V_B}{R2} = \frac{V_A}{R2} = \frac{V_{gs1}}{R2} \tag{II.5}$$

Hence, Eq. II.6

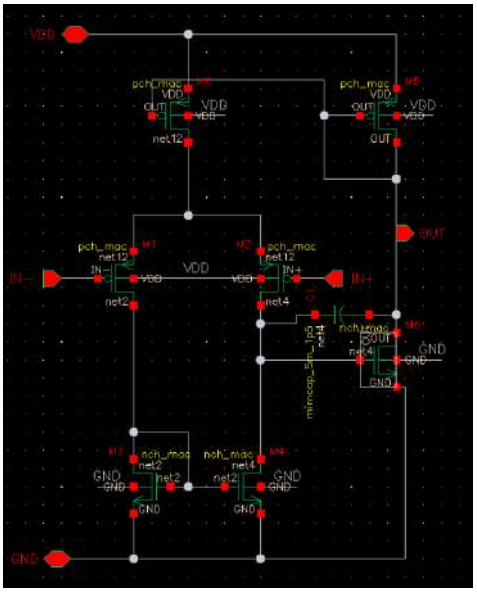
$$\begin{aligned} I_1 = I_2 = I_3 = I_{R2} + I_{R1} = \frac{V_A}{R2} + n\frac{kT}{qR1} ln(m) \\ V_{ref} = I_3 R3 = (\frac{V_{gs1}}{R2} + \frac{nkT}{qR1} ln(m)) R3 \end{aligned} \tag{II.6}$$

The different values are chosen to reach a voltage reference of 300 to 350mV.

The design in Cadence and the resulting layout can be respectively found in Fig. II.6 and II.7.



(a) Bandgap design



(b) OTA design

Figure II.6: Complete design of the bandgap reference

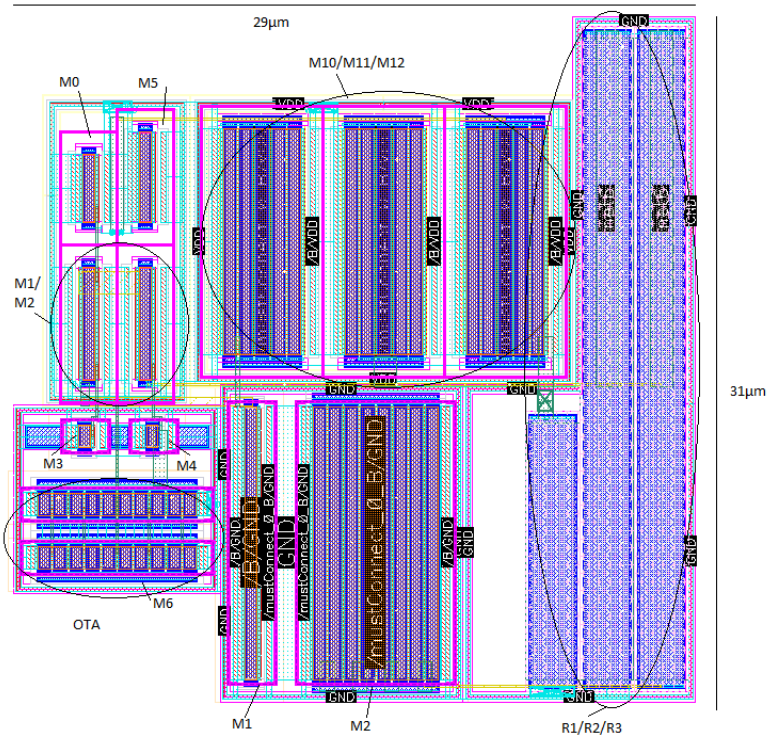
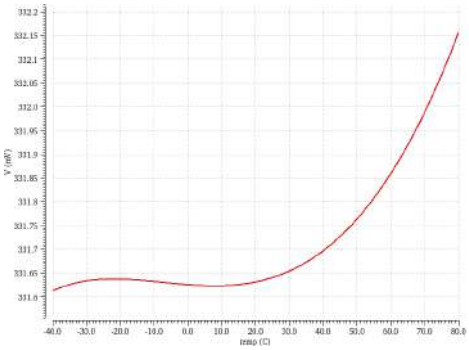


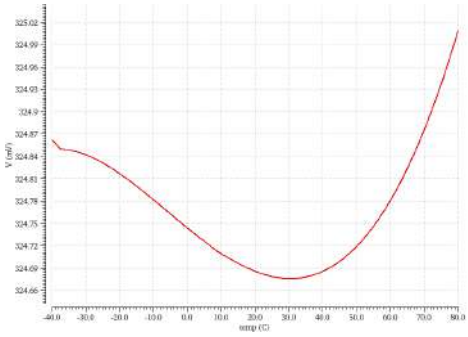
Figure II.7: Layout of the bandgap reference

c Simulations results

The supply voltage for this simulation (Fig. II.8) was set to 1.2V. The working temperature of the experiment that HGCROC is part of is -30°C, the chip should also be working at around room temperature. The sweep of temperature was set to -40-80°C to accommodate for the temperature during the experiments and to make sure that the design could also be used for different experiments at room temperature.

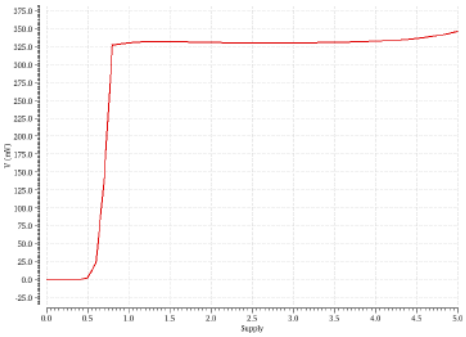


(a) Pre layout

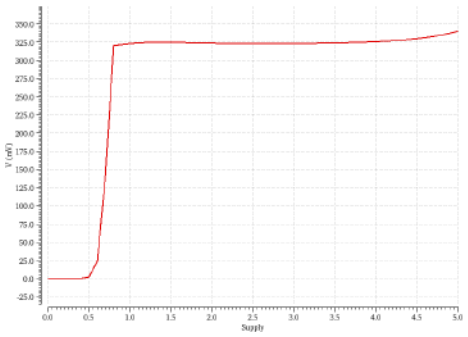


(b) Post layout

Figure II.8: Pre and Post layout simulations: temperature dependence



(a) Pre layout



(b) Post layout

Figure II.9: Pre and Post layout simulations: supply dependence

The temperature dependence can be quantified by the temperature coefficient, it is expressed in ppm/°C; with $1ppm = 1.10^{-6} \times v_{initial}$. Pre layout, the minimal value is 331.612364mV, the maximal value is 332.156277mV and the initial value (chosen has the value at 27°C and 1.2V) is 331.645301mV. This results in a temperature coefficient of 13.67 ppm/°C.

Post layout, the minimal value is 325.008591mV, the maximal value is 324.675831mV and the initial value (chosen has the value at 27°C and 1.2V) is 324.676924mV. This results in a temperature coefficient of 8.54 ppm/°C.

The temperature for this simulation (Fig. II.9 and II.10) was set to 27°C. The supply voltage of the circuit is 1.2V, the bandgap should be able to withstand variations in supply voltage around this point, it is particularly interesting to see its response on the $0.9 \times Supply - 1.1 \times Supply$ range; i.e. 1.08 - 1.32V.

The design can in no way be used below 0.8V (see the drop).

The dependence on supply voltage can be quantified by the line regulation, it is expressed in %/V.

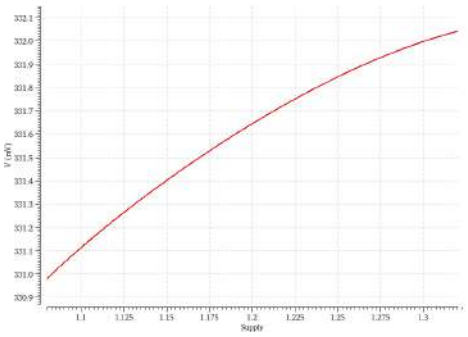
Pre layout, the minimal value is 330.980736mV, the maximal value is 332.04189mV and the initial value (chosen has the value at 27°C and 1.2V) is 331.645301mV. The resulting line regulation is 1.33 %/V.

Post layout, the minimal value is 324.01519mV, the maximal value is 325.08841mV and the initial value (chosen has the value at 27°C and 1.2V) is 324.676924mV. The resulting line regulation is 1.37 %/V.

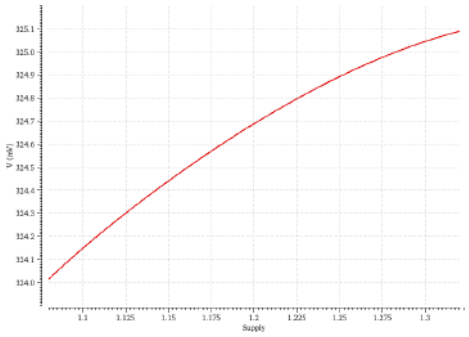
The corners simulations (Fig. II.11 and II.12) are done similarly to precedent simulations, but multiple libraries are used and looked at.

The summaries from those plot can be found Tab. II.3 and II.4:

Contextualisation of these values will be given after, with a comparison to the state-of-the-art bandgap ref-

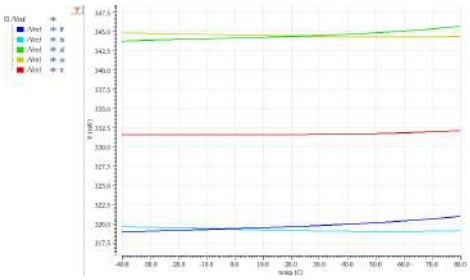


(a) Pre layout

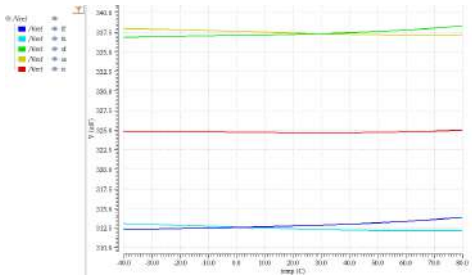


(b) Post layout

Figure II.10: Pre and Post layout simulations: line regulation

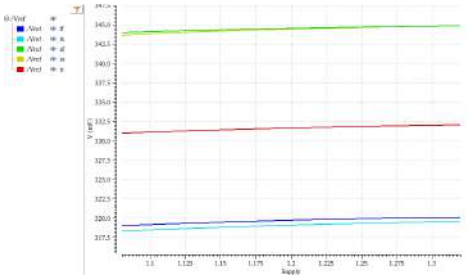


(a) Pre layout

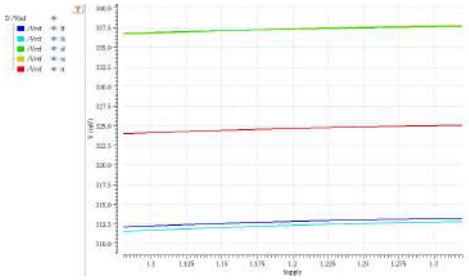


(b) Post layout

Figure II.11: Pre and Post layout simulations: temperature dependence and corners



(a) Pre layout



(b) Post layout

Figure II.12: Pre and Post layout simulations: supply dependence and corners

pre layout	ff	fs	sf	ss	tt
Temperature coefficient	53.29	16.02	47.05	12.67	13.67
Line regulation	1.40	1.61	1.04	1.50	1.33
Value (1.2V and 27°C)	319.72	319.09	344.51	344.42	331.65

Table II.3: Pre layout results from Fig. II.11 and II.12

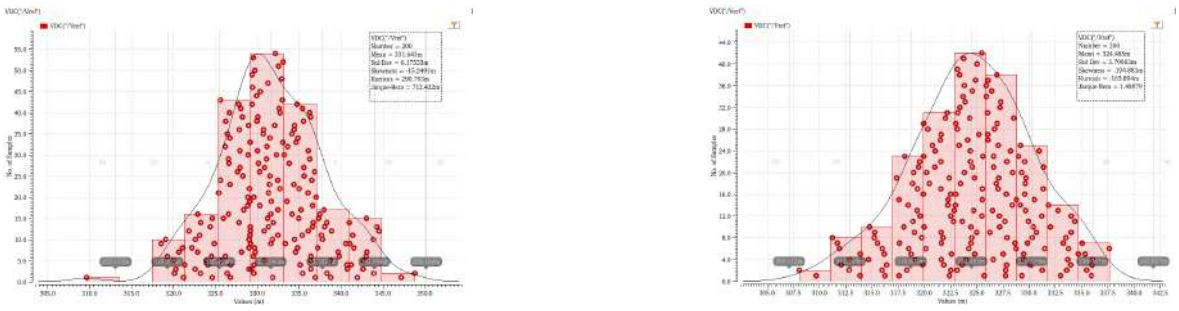
post layout	ff	fs	sf	ss	tt
Temperature coefficient	42.12	24.30	36.81	20.43	8.54
Line regulation	1.44	1.67	1.07	1.52	1.38
Value (1.2V and 27°C)	312.84	312.34	337.31	337.35	324.68

Table II.4: Post layout results from Fig. II.11 and II.12

erences.

Monte Carlo simulations to check the impact of the manufacturing process on the bandgap can also be done. They are presented in Fig II.13.

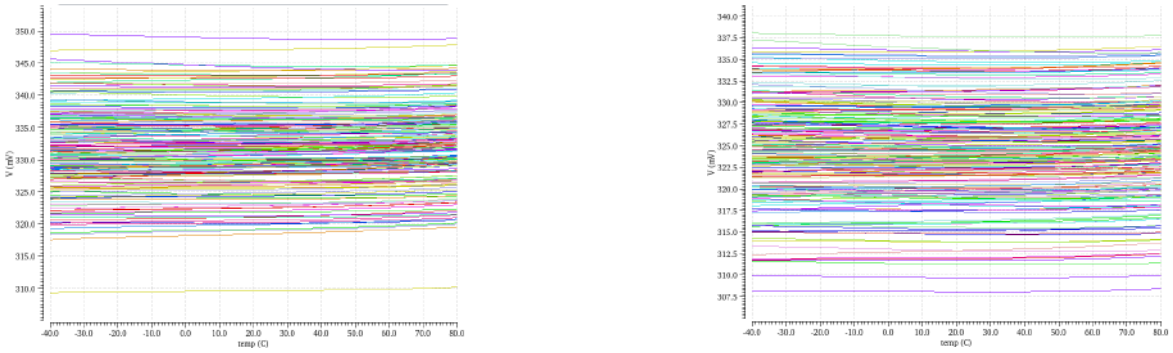
Pre-layout, the standard deviation corresponds to 1.86% of the voltage reference. Post layout, it corresponds to 1.78%. Those values are fairly similar and reasonable.



(a) Pre layout

(b) Post layout

Figure II.13: Pre and Post layout simulations: Monte Carlo in temperature



(a) Pre layout

(b) Post layout

Figure II.14: Pre and Post layout simulations: Monte Carlo with individual curves

d Comparison to state of the art

This section has for objective to compare the previously simulated and extracted values to the state of the art. Tab. II.5 and II.6 present the state of the art. And Tab. II.7 summarises the data extracted from the simulations.

130nm	**Gromov** [7]	**Cao** [4]
Supply Voltage (V)	1.2	1.2
Operating voltage range (V)	0.85-1.4	0.85-1.5
Reference voltage (mV)	405	600
Line regulation (%/V)	2.72	
Temperature coefficient (ppm/°C)	30.5	15
Temperature range (°C)	0-80	-40-125
Power consumption (μW)		60
Layout area (mm^2)	0.064	0.056
Technology	CMOS 130nm	CMOS 130nm
Measured/Simulated	Measured	Measured

Table II.5: State of the art in 130nm

65nm	**Traversi** [12]	**Traversi** [11]	**Vergine** [13]	**Jun-an** [8]
Supply Voltage (V)	1.2	1.2	1.2	1.2
Operating voltage range (V)	1.08-1.32	1.08-1.32	1.08-1.32	1.1-1.3
Reference voltage (mV)	675	400	330	468
Line regulation (%/V)	3.6	4	0.25	0.75
Temperature coefficient (ppm/°C)	230	16 (best)	130	best: 30 average: 45
Temperature range (°C)	-30-140	-40-100	-40-80	-55-125
Power consumption (μW)	46	165	240	488
Layout area (mm^2)	0.0264	0.028	0.018	0.5025
Technology	CMOS 65nm	CMOS 65nm	CMOS 65nm	CMOS 65nm
Measured/Simulated	Measured	Measured	Measured	Measured

Table II.6: State of the art in 65nm

The line regulation (Tab. II.6) ranges from 0.25 to 4%/V. The results from the simulations seem to indicate that the values of line regulation (between 1.07 and 1.67%/V) are performant.

65nm	**This work pre layout**	**This work post layout**
Supply Voltage (V)	1.2	1.2
Operating voltage range (V)	1.08-1.32	1.08-1.32
Reference voltage (mV)	331.6	324.7
Line regulation (%/V)	average: 1.38 worst: 1.61 best: 1.04	average: 1.41 worst: 1.67 best: 1.07
Temperature coefficient (ppm/°C)	average: 28.54 worst: 53.29 best: 12.67	average: 26.44 worst: 42.12 best: 8.54
Temperature range (°C)	-40-80	-40-80
Power consumption (μW)	362.2	354.8
Layout area (mm^2)		0.000924
Technology	CMOS 65nm	CMOS 65nm
Measured/Simulated	Simulated	Simulated

Table II.7: Summary of the performances of the designed BGR

The temperature coefficient ranges from 16 to 230ppm/°C. The TC of the simulations spans from 8.54 to 42.12ppm/°C which once again is good.

The power consumption in the state of the art starts at 46 and reaches 488μW. With a simulated consumption of 354.8μW, the power consumption is lacking.

Overall, the designed bandgap has pretty good performances, the main problem when designing a bandgap is that simulations are surprisingly inaccurate; hence, the actual performances of the BGR can only be judged after thorough measurements. The results simulated are encouraging but they in no way fully conclude the study of the bandgap performances.

PART III

MEASURES OF THE CHIP

This chapter aims to introduce the different measurements that can be done to test the chip's functions. It also uses those measurements to compare the various packages that could be used on the chip.

1 Test setup

The chips performance was characterised in the laboratory using two types of test benches, both controlled by an FPGA developed at CERN. These test benches communicate with the ASIC and read its response using Python scripts. Figure III.1 shows the mezzanine board with one HGCROC3B connected to a PCB, while Figure III.2 displays the socket board with one ASIC in place. The socket on the board allows for easy removal of the ASIC, enabling the interchange of ASICs and facilitating the testing of the entire production process using a robot. Figures III.1 and III.2 showcase the ZYNQ/Hexacontroller card developed at CERN. This board is used to configure and read the ASICs output. The ZYNQ is programmed with C code, enabling I2C control and fast command execution for communication through Ethernet with the PC. Subsequently, Python scripts can activate the trigger signal to inject charge internally using a DAC within the chip or introduce external charges synchronized with the trigger. All configuration parameters are modifiable through slow control via the I2C protocol.

Those boards are alimented in voltage either with 3.3V (then divided into 1.2V for analogue and 1.2V for digital) or two times 1.2V.

One of the key features of the HGCROC ASIC is its versatility in adapting to diverse scenarios. The ASIC design incorporates configurable parameters to address various aspects, including setting DC levels, mitigating radiation-induced damage, minimizing variations between channels, and establishing the minimum threshold for timing measurements. Moreover, every block of the ASIC can be configured to maintain consistent performance across channels, even in the presence of potential discrepancies resulting from the chips manufacturer and the selected technology.

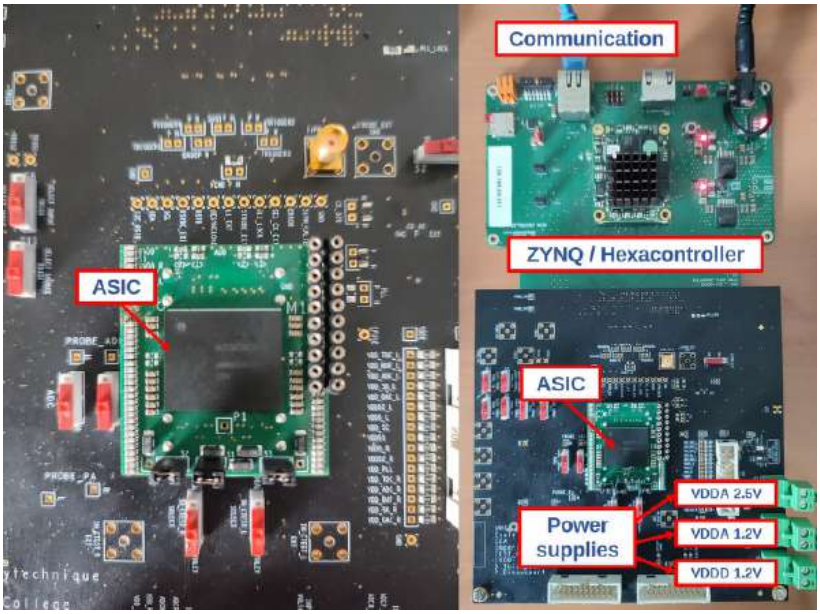


Figure III.1: Mezzanine boards

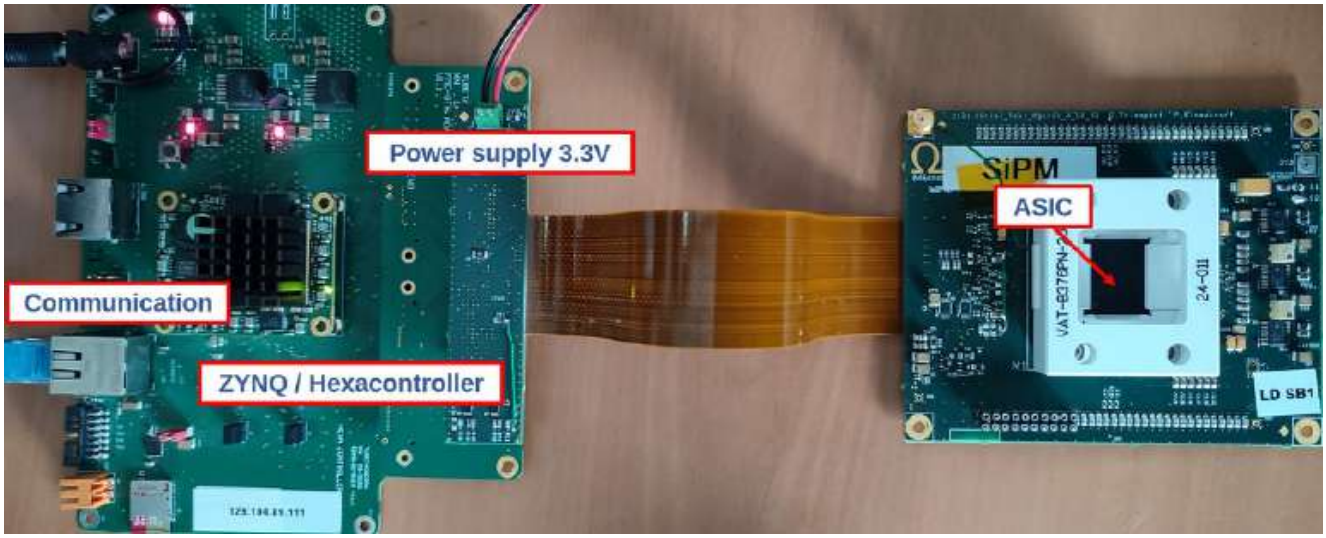


Figure III.2: Socket boards

2 Basic measures

The initial step in ASIC calibration involves setting the pedestal value for each channel to the same ADC level, minimizing noise and ensuring a lower variation between channels. The process consists of reading each channels pedestal value and using the *dacb* DAC of each channel to adjust the pedestals to fall within the same ADCs selected range.

Figure III.3 and III.4 illustrate the pedestal readings before and after calibration. The variation in the pedestal before the calibration is around 100 ADC counts and is reduced to 6 ADC counts after the calibration.

The pedestal should be constant in time but is not because of the digital clock, this variation can be observed and quantified, Fig. III.5 highlights this behaviour that is called digital noise. The variation in the pedestal is clear as the clock moves through its 15 phases, it is on average around 20 ADC counts.

A very important plot to observe is the injection of a charge in the chip and the lecture of the signal, Fig. III.6,

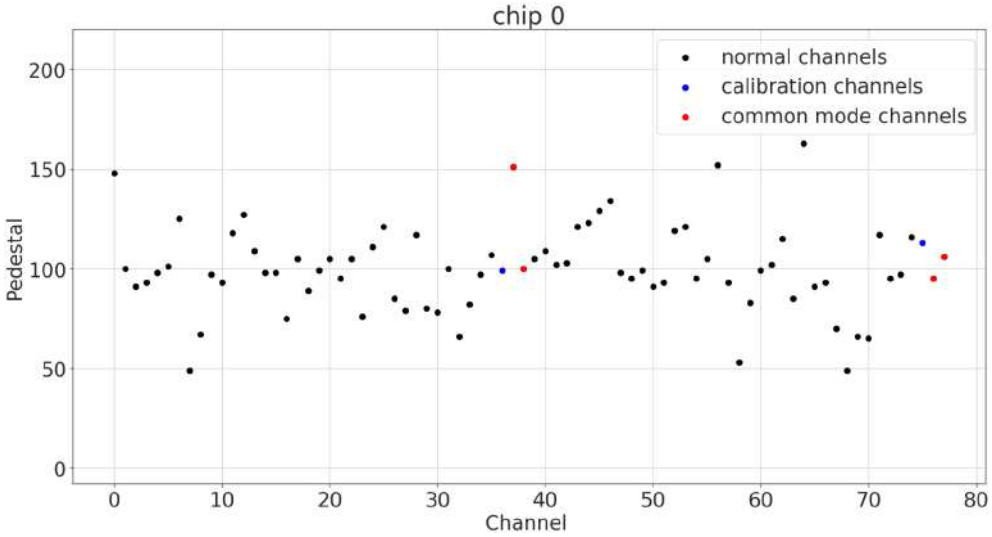


Figure III.3: Pedestal

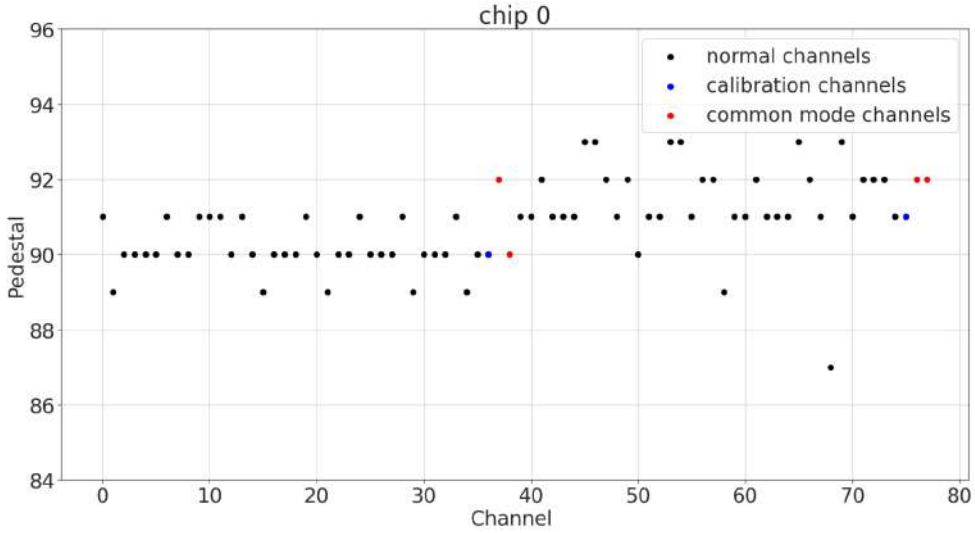


Figure III.4: Pedestal after calibration

the digital noise can once again be observed on this plot.

The measures of timing and charges are done with three components: the ADC, the ToA discriminator and the ToT discriminator. The correct behaviour of the three needs to be checked.

The ADC behaviour can be analyzed by injecting different charges and taking the pedestal for each charge. Figure III.7 provides us with the dynamic range of the ADC (this can also be compared to the simulated results), the linearity can also be checked from this plot.

When the ADC is linear, its amplitude directly correlates to the charge injected; when the ADC saturates, the ADC pulse is correlated to the charge, the ToT is then the one being used to calculate the charges, the linearities of both the ADC and the ToT are crucial to the accuracy of the charge measurement.

The discriminators (for the ToA and the ToT) work as follows: when the signal reaches the set threshold, the output of the discriminator goes to 1 (1.2V) and after a certain time (as fast as possible) it goes back to 0 (0V).

This allows for the time measurements of the ToA (Time of Arrival) and ToT (Time over Threshold).

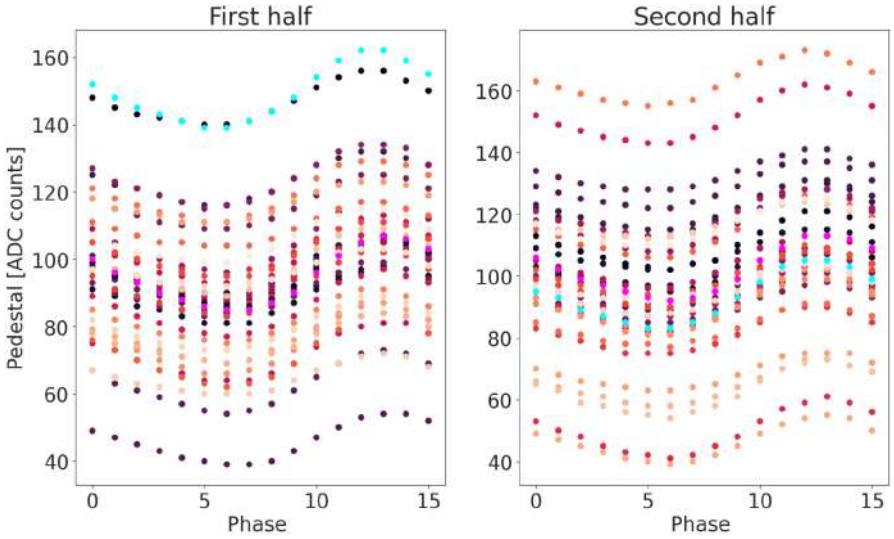


Figure III.5: Pedestal variation with clock phase

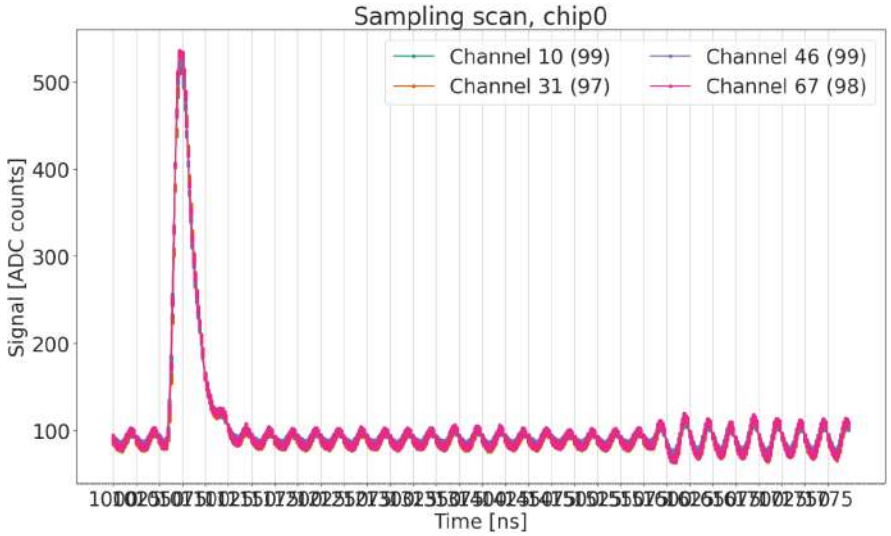


Figure III.6: Sampling

For the ToT, Fig. III.8, when the charge injected increases, the time over threshold increases as well, the relation should be linear.

For the ToA, Fig. III.9, when the charge injected increases, the time of arrival of the signal should decrease until it reaches a plateau value.

The thresholds of the two discriminators can be configured per half and adjusted channelwise to minimize dispersion among channels. The time-of-arrival (TOA) threshold should be set just above the pedestal noise level to ensure accurate data acquisition timing for most events. The time-over-threshold (TOT) threshold needs to be configured below the saturation point of the preamplifier (PA) to cover the full dynamic range of measurements. The process of establishing the threshold voltages is similar for both discriminators, but will not be presented here.

Once the thresholds are set correctly, Fig. III.11 and III.10 can be plotted. Note that the behaviours of the two plots correspond to the explained theory.

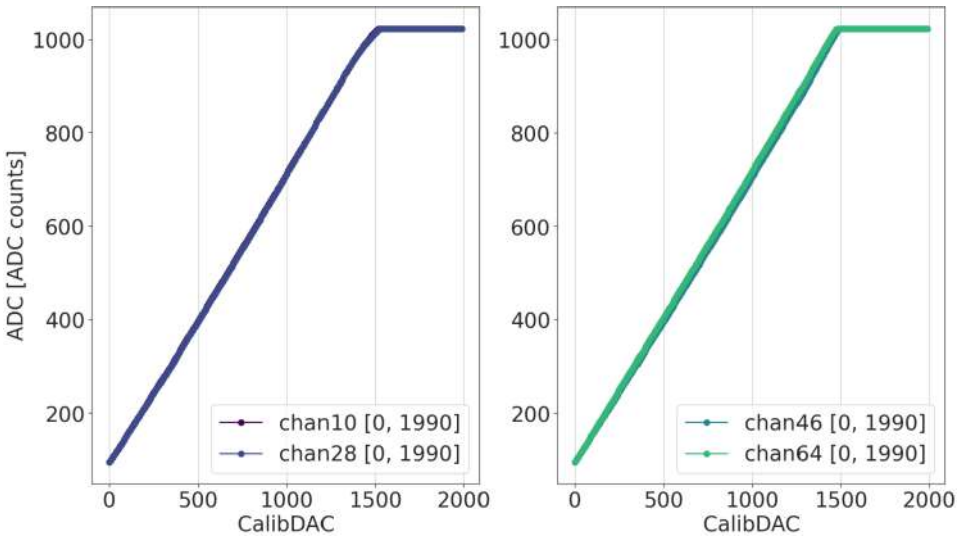


Figure III.7: ADC

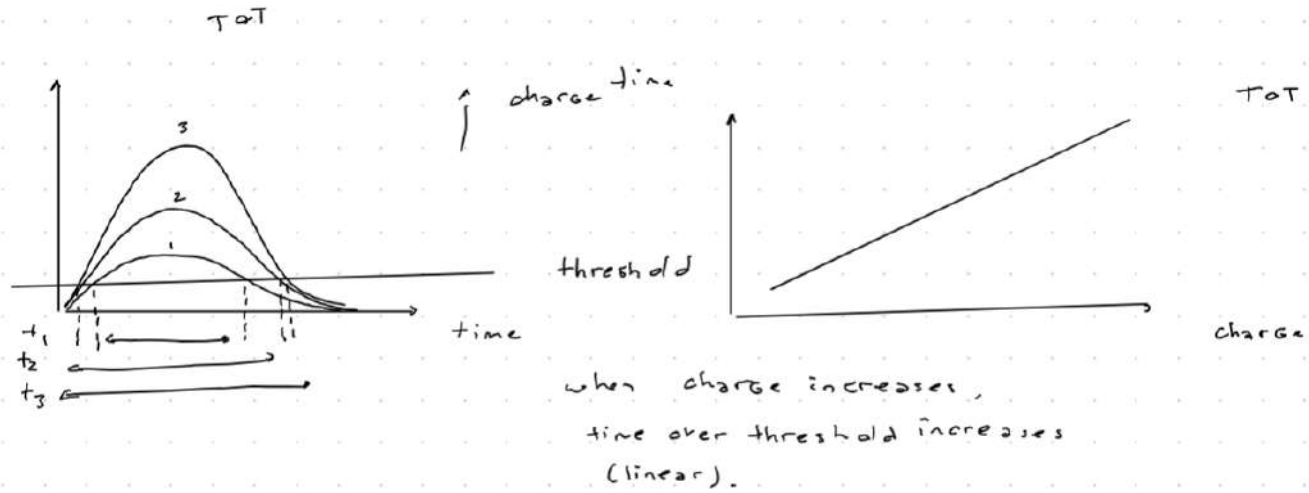


Figure III.8: Theory ToT

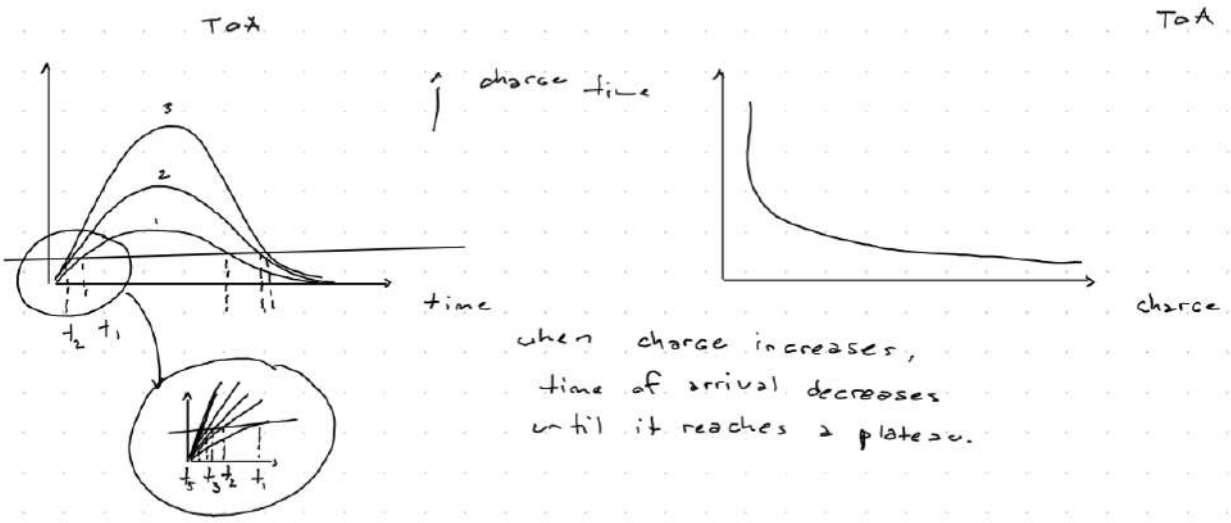


Figure III.9: Theory ToA

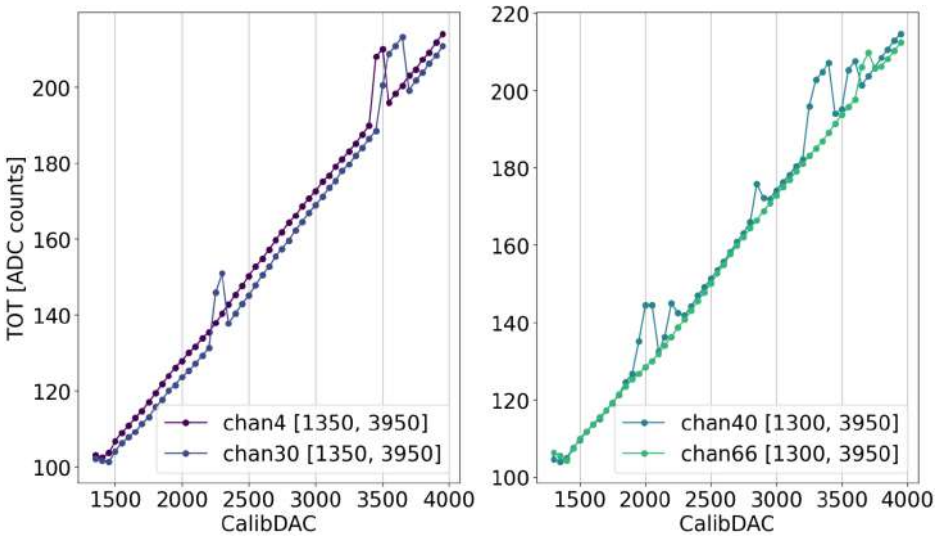


Figure III.10: ToT

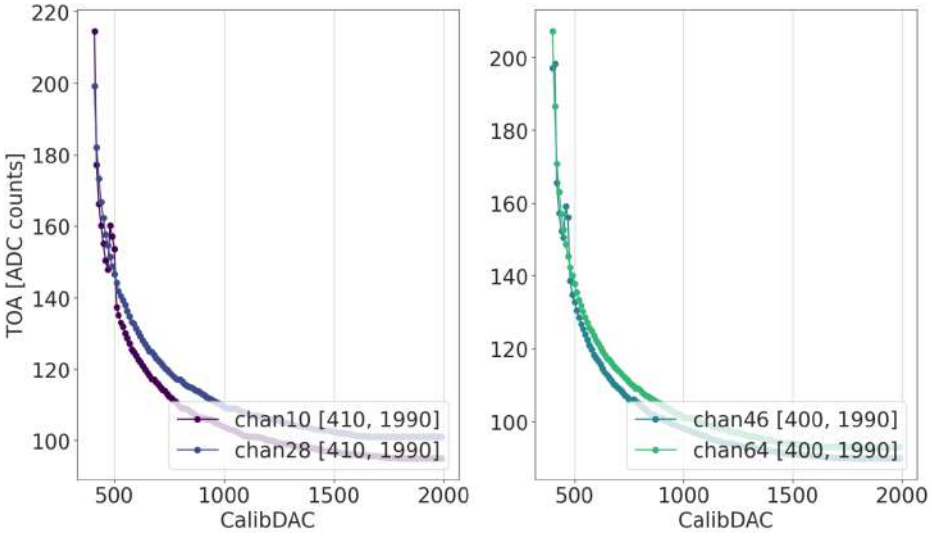


Figure III.11: ToA

3 Comparison of packages

Those measures (and others) are used to fully characterize the chips; this might allow for the classification of the chips (between bad/good/misplaced) or the comparison of the performances of different chips. In this part, the focus is on the comparison of chips that were not packaged similarly.

Multiple packages could be used for the chips, common ground or separated ground (for digital and analogue), measures of the chip with both packages can be done to be sure of the one to use.

First, the digital noise can be looked at. This can be done by looking at the pedestal in time. The pedestal is the offset value of the ADC, the pedestal should theoretically not change in time, but the digital clock has a period of 25ns and impacts the pedestal as it goes through its phases, this phenomenon is represented in Fig. III.12. The objective here is to have as little digital noise as possible.

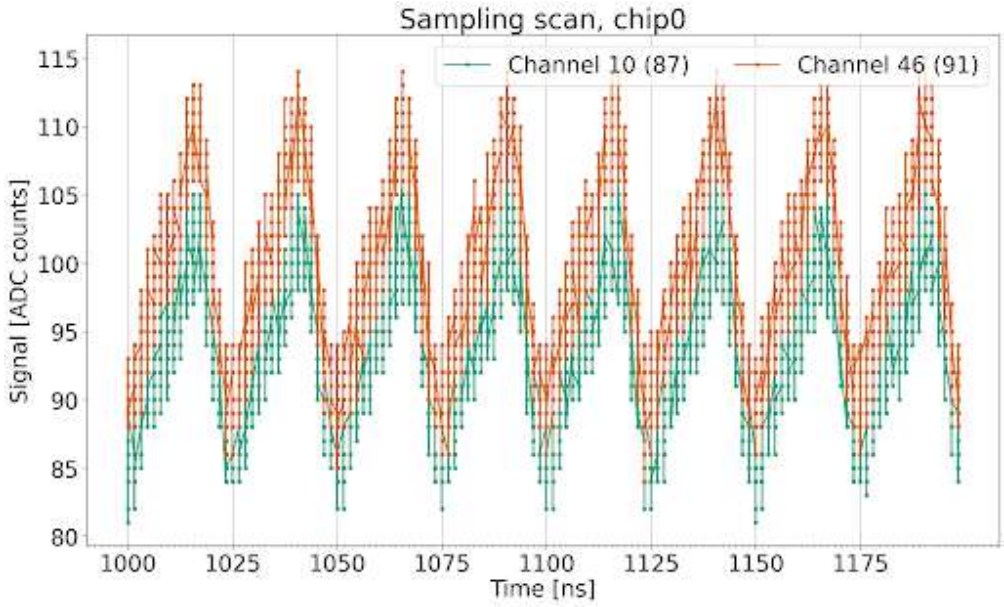
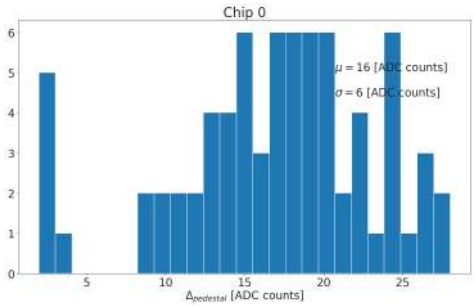


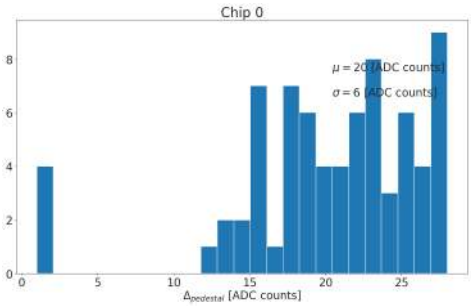
Figure III.12: Signal ADC

Fig. III.13 represents the distribution of the amplitude of pedestal variation per channel of the chip. The mean value of the variation is 16 ADC counts in common ground and 20 ADC counts in separated ground. Those values are very common. Note that the value of the pedestal is around 150 ADC counts so a variation of 20 ADC counts represents around 15%. The common ground package does slightly better on this criteria.

Then the minimum ToA (Time of Arrival) threshold can be observed (Fig. III.14). The ToA threshold should be set as low as possible, this is directly linked to the smallest charge detected. The digital noise is the main

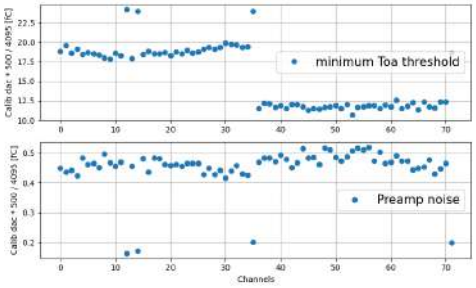


(a) Common ground

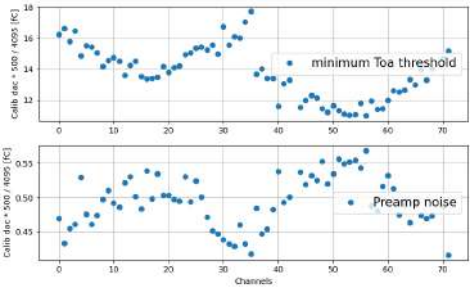


(b) Separated ground

Figure III.13: Digital noise

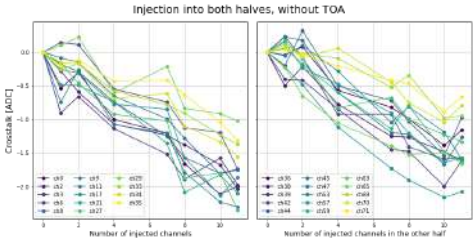


(a) Common ground

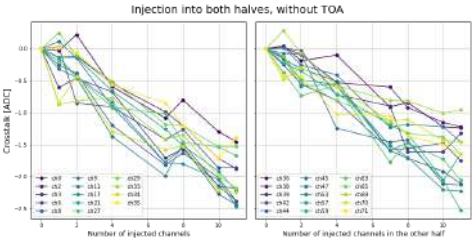


(b) Separated ground

Figure III.14: Minimum ToA threshold



(a) Common ground



(b) Separated ground

Figure III.15: Crosstalk without ToA

problem here since the threshold needs to be set above the noise.

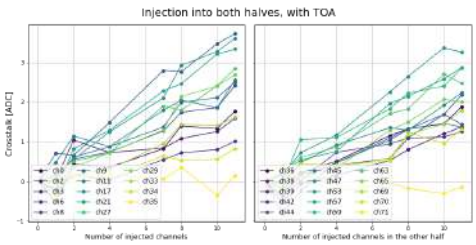
The variation of the minimum ToA threshold per chip is 12.5fC for common ground and 7fC for separated ground. The minimum ToA threshold is very similar for both packages: 10.5fC for common ground and 11fC for separated ground. The results are unclear for the minimum ToA threshold.

The crosstalk can also be measured, it depends on the presence of ToA, and the number of injected channels (Fig. III.15 and III.16). To quantify it, the pedestal is taken with no injection of channel and is compared to the pedestal when channels are injected. The crosstalk should be as small as possible, if the crosstalk was to be high, the measures of charges would be completely unreliable.

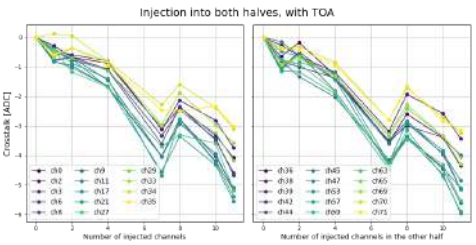
For both common and separated ground (Fig. III.15), the maximum crosstalk without ToA is 2.5 ADC counts, which is somewhat negligible compared to the 150 ADC counts of the pedestal.

In Fig. III.16, the maximum crosstalk with ToA is 4 ADC counts for common ground and 6 ADC counts for separated ground, which is once again negligible. It is worth noting that the crosstalk increases with the presence of ToA. Once again the results are somewhat similar between both packages.

Only looking at the presented figures, no clear choice can be made for which package is better. The real



(a) Common ground



(b) Separated ground

Figure III.16: Crosstalk with ToA

(a) Common ground

(b) Separated ground

Figure III.17: Hysteresis of ToA threshold

problem is the following:

Fig. III.17a shows that when the ToA threshold is set higher than the digital noise, no ToA is detected, which is perfectly normal, when the ToA threshold is dropped enough, a ToA is detected since it crosses the digital noise, but when the ToA threshold is set again to the initial value, theoretically above the digital noise, a ToA is still detected, probably because of a feedback loop increasing the noise. This is a very poor behaviour that should be avoided. Fig. III.17b shows that the same behaviour does not happen in separated ground.

This is the main reason why the separated ground package is chosen.

4 Test series

Around 120000 chips will be needed in the experiment, testing them by hand would be way too time-consuming, to help in the process a robot is used; the robot works as follows:

1. The chips are laid on trays to be processed by the robot.

2. The robot picks up the chips and places them in one of the five sockets. Multiple sockets are used to parallelise the tests and be more effective.

3. The measures are done using a script. The test series should test as many things as possible and be as reproducible as possible; most of the important tests presented earlier are in some form used in the test series and a flag is created for each test. The script is designed to test all of the important behaviours of the chips, retrieve data from those tests and fit the different data to get key fitting parameters out. Then those parameters are compared to what it should on average be and the test is deemed to be true or false.

4. The chip is then classified as either bad, good or misplaced. If the chip fails at least one test, the chip is bad, if the chip crashes, the chip is misplaced and if it passes all of the tests, it is good.

5. The data of the chip are saved in a database with a unique code corresponding to the chip tested for the sake of traceability.

Multiple tests are done on each chip (some multiple times) [1]:

- power consumption reading:
  - the current read can then be compared to the usual values.
  - Fig. III.18 highlights the normal distribution of current across the different chips. The vertical lines are the chosen thresholds that are used by the test to decide whether a value of current is acceptable or not.
- i2c reading and writing
  - for this test, a file configuring the chip is sent, and then the configuration saved on the chip is read, there should be no difference between the two files.

[1] This is a non-exhaustive list of the tests done on the chips.

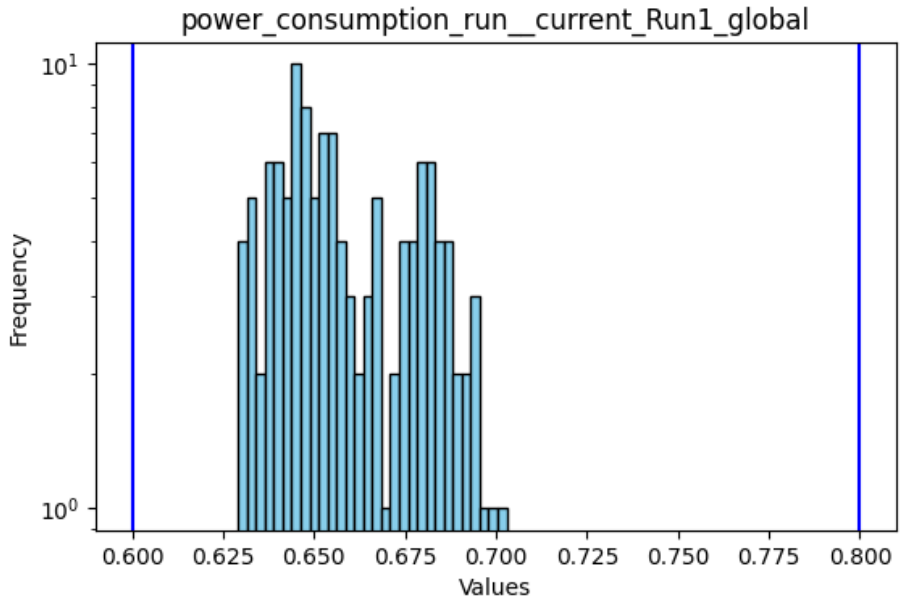


Figure III.18: Power consumption distribution of 132 chips

  - the number of differences is extracted, it should always be zero.

- pedestal reading:
  - the pedestal and the noise extracted are compared to the usual. values.

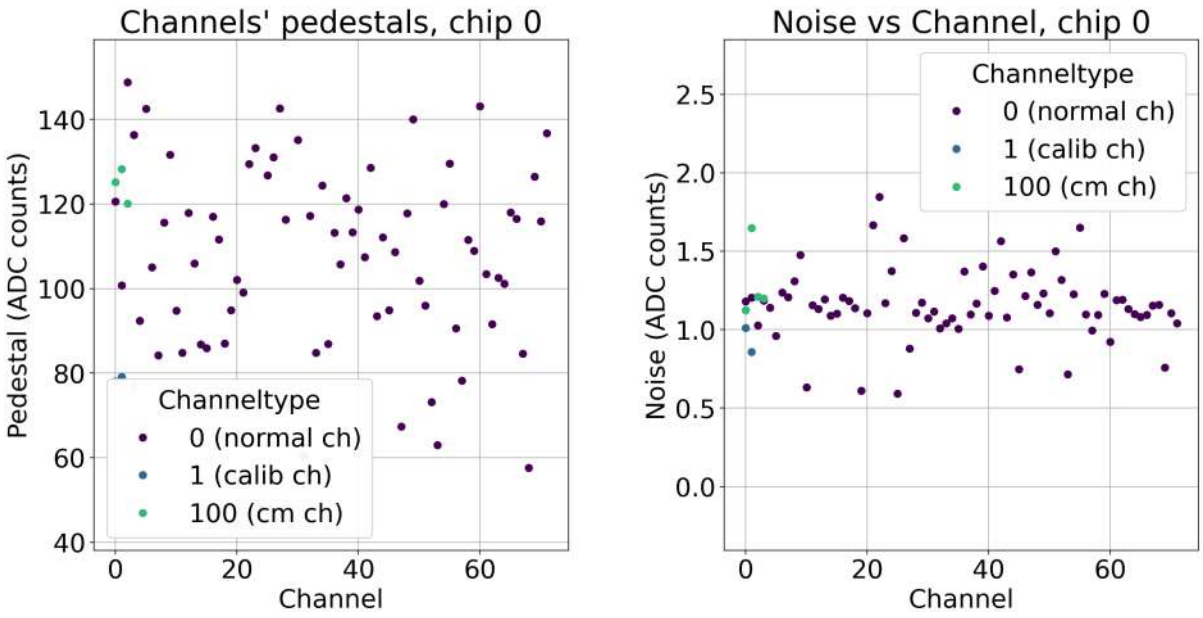
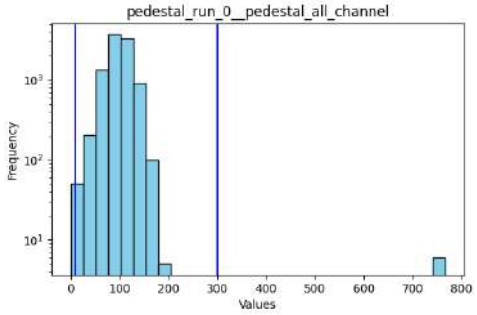


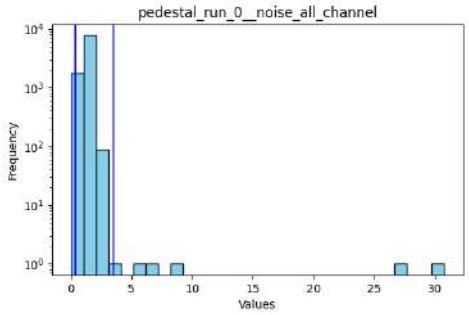
Figure III.19: Pedestal and pedestal noise of one chip

  - Fig. III.19 presents the pedestal and pedestal noise of one chip.
  - Fig. III.20a and III.20b represent the distribution of the pedestal and the pedestal noise before calibration.

- pedestal calibration: $trim\_inv$ is scanned to check that the pedestal can be calibrated, and then the pedestals are all set to more or less the same value.



(a) Pedestal



(b) Pedestal noise

Figure III.20: Pedestal and pedestal noise distributions of 132 chips

  - the data extracted are fitted with a linear function.

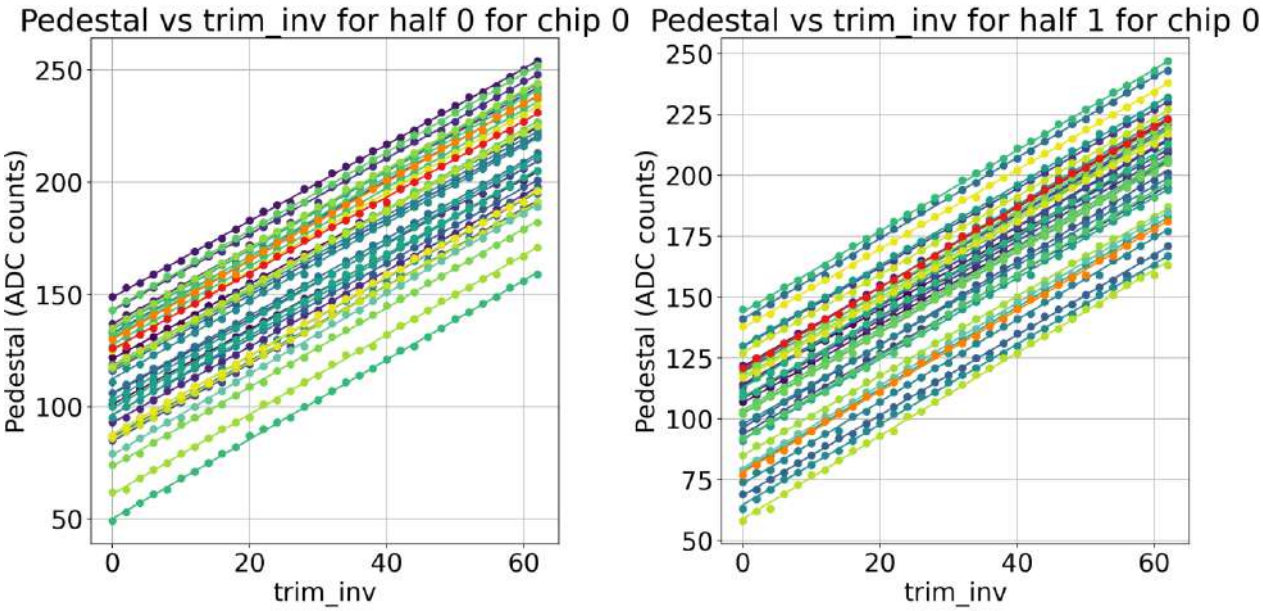
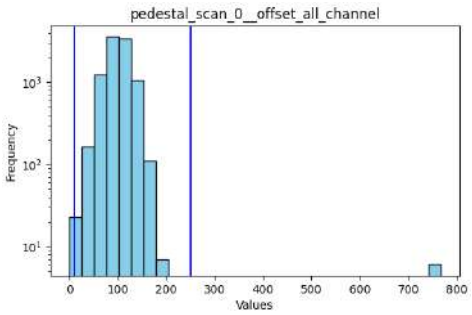


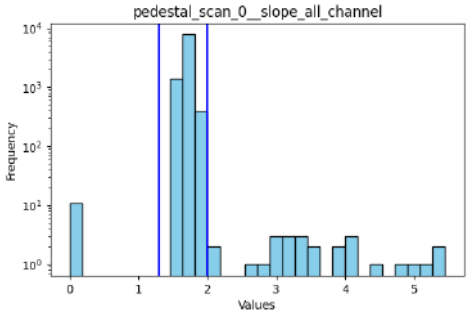
Figure III.21: Scan of $trim\_inv$ of one chip

  - Fig. III.21 shows the scanning of $trim\_inv$ in one chip. The $trim\_inv$ value of each channel will then be chosen to equalise all the pedestals.
  - Fig. III.22a and III.22b highlight the distribution of the fitting parameters of offset and slope of the curves.

- digital noise reading:
  - the amplitude of the variation and the noise are compared to the usual values.
  - Fig. III.23a and III.23b present the digital noise amplitude and the noise as the clock goes through its phases.
  - Fig. III.24a and III.24b highlight the normal distribution of the digital noise amplitude and the maximum noise reached.
- charge injection: reading of ADC, ToT and ToA (as a function of the charge).
  - the curves of the ADC and ToT are fitted with a linear function.
  - the curve of the ToA is fitted with the function $\frac{a}{x+b} + c$.

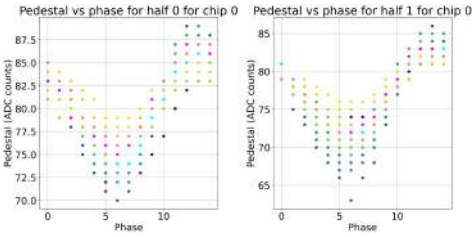


(a) Pedestal scan offset

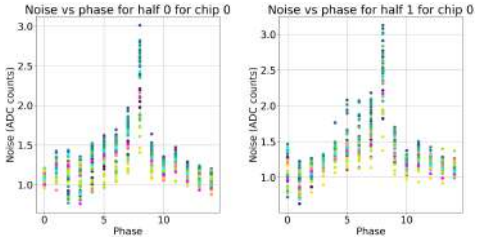


(b) Pedestal scan slope

Figure III.22: Pedestal offset and pedestal slope distributions of 132 chips

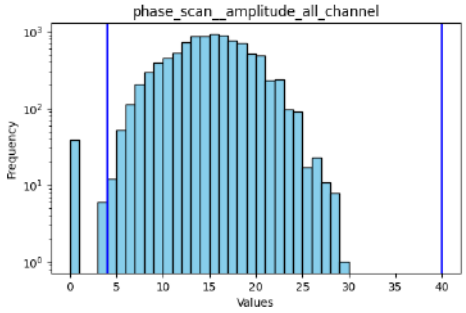


(a) Digital noise amplitude

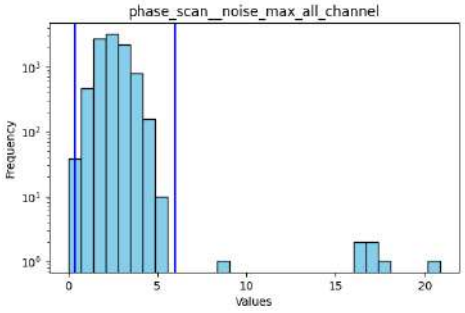


(b) Noise

Figure III.23: Digital noise amplitude and noise for one chip

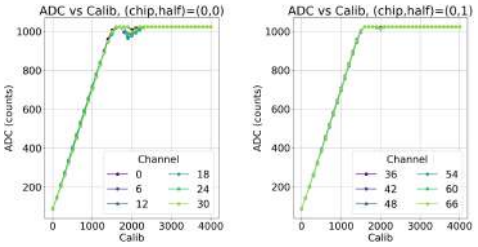


(a) Digital noise amplitude

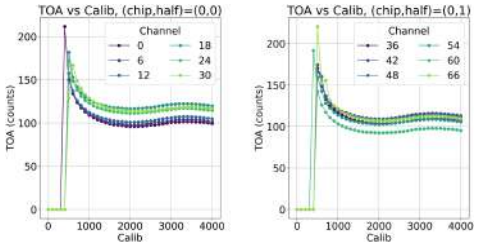


(b) Maximum noise

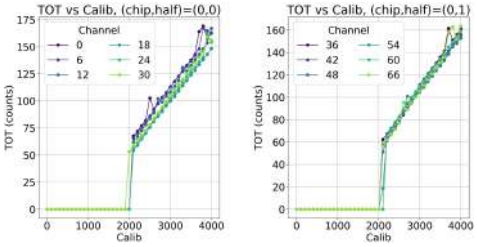
Figure III.24: Digital noise amplitude and noise distributions of 132 chips



(a) ADC as a function of charge

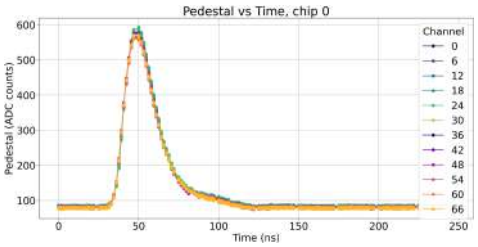


(b) ToA as a function of charge

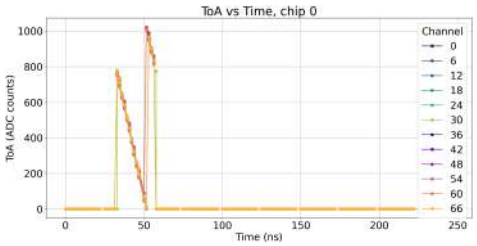


(c) ToT as a function of charge

Figure III.25: ADC, ToA and ToT as function of charge



(a) ADC signal



(b) ToA signal

Figure III.26: Signals ADC and ToA

  - Fig. III.25a, III.25b and III.25c highlight the behaviour of the ADC, ToA and ToT of one chip.
  - the distributions of the extracted parameters of these plots will not be shown for the sake of length.
- sampling: reading of ADC and ToA (as a function of time)
  - the curve of the ToA is fitted with a linear function.
  - the curve of the signal is fitted with the function: $A_0 e^{-at}(e^{-ct}(\frac{t^3}{c} - \frac{3t^2}{c^2} + \frac{6t}{c^3} - \frac{6}{c^4}) + \frac{6}{c^4})$ with $a = \frac{1}{\tau_p}$ and $c = \frac{1}{\tau_p} - \frac{1}{\tau_s}$
  - Fig. III.26a and III.26b show the signals of the ADC and the ToA response when a charge is injected.
  - the distributions of the extracted parameters of these plots will not be shown for the sake of length.

For now, the tests are lacking reproducibility. Testing the same chips a certain number of times might yield different results; this could be caused by a few things:

- the chips itself: the chips are designed to be identical, but the reality is after the manufacturing they simply are not, this explains the differences in behaviours between chips but not the differences that can be found when testing one chip multiple times.
- the material used for the measures: a lot of interconnections are present in the setup; the chips are connected to a socket, that itself is connected to the hexacontroller. The contacts between the chip and the socket could be dirty and cause problems, the connexion between the socket and the hexacontroller might be problematic as well. On top of this, the sockets are supposed to be identical but aren't, their

behaviours are slightly different, and some work better than others.

- the script: this should not cause any problem, the same data should be analysed in the same way by the script.
- the external conditions of the measures: the temperature, humidity, brightness, ... might be causing some of the discrepancies that can be observed in the tests.

More tests are being done to understand the reasons for the problem; getting reproducible tests is necessary to get these chips to production.

Even with the robot, the testing of the entirety of the chips should take around six months.

CONCLUSION

In this report, we showed part of the transfer of the blocks of HGCROC3B from the 130nm technology to 65nm. Overall, the main objective was to take the new PDK and the specific tools in hand. The second objective was to check the feasibility of such a transfer, that at first could be thought to be costly; at the end of the day, the transfer was done on the entirety of the analogue part of the chip, and the simulations were done on the critical blocks, the simulations seem to show that no problem should arise from scaling down the technology to 65nm as long as careful checks are done in terms of PVT and Monte Carlo simulations.

A similar study in a more recent node will have to be done in the future to assess the use of smaller nodes (such as 40nm or 28nm).

Measures were also made on the already existing HGCROC3B chips. Scripts used in the test series were created and help during the TID campaign was provided. The results from the tests were used to understand the chip a tiny bit better and inform the design changes needed for the chip to meet all of the requirements.

The new version of the chip, HGCROC3C, is being fabricated and will be received and tested in October.

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[1] Muhibul Bhuyan. "Analytical Modeling of the Pocket Implanted Nano Scale n-MOSFETs". PhD thesis. July 2011.

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