Politecnico di Torino

Master's Degree in Electronics Engineering

Design and Characterization of RF Power Amplifiers for Wireless Communications

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Abstract

Power amplifiers are the final stage in the transmitter chain of a communication system, and their design requires care and specific techniques since their performance has a significant effect on the overall system. Furthermore, their design becomes more challenging when very broadband operation is required. Broadband power amplifiers are necessary for several reasons, primarily due to the increasing demand for communication systems with broader frequency coverage, higher data rates, and more efficient transmission. They play a crucial role in enabling seamless and efficient wireless communication across various applications and technologies.

In this thesis work, the design and characterization of a three-octave (0.5 GHz- 4 GHz) hybrid single-stage class AB power amplifier is presented. Several figures of merit must be met when it comes to a broadband design. Among the challenges that need to be addressed, gain flatness and an appropriate trade-off between fundamental frequency and higher-order harmonics matching are two key aspects In fact, higher-order harmonics of the lower frequencies below the central frequency will fall inside the bandwidth hence proper output matching network based on the trajectory of optimum load in terms of a trade-off between output

power and efficiency over Smith chart must be designed. For this end, an output-matching network consisting of a 4-section transformer based on a Chebyshev response has been implemented. As for the input matching network, a simple topology in terms of a reasonable trade-off between minimum reflection and gain flatness is considered. Bias-T functionality over the entire bandwidth is another key challenge that must be dealt with, and finally, EMC and layout optimization are the final steps in the design procedure.

A hybrid prototype is designed and simulated based on a 25 W packaged GaN device for frequency band from 500 MHz up to 4 GHz. Over this wide bandwidth, the amplifier reaches saturated output power higher than 42 dBm with the associated transducer gain of higher than 6 dBm and power added efficiency above 55%. Measurement and verification of the manufactured prototype are still ongoing. Further developments to be carried out are linearity analysis and possibly more optimization for overall power amplifier behavior.

Acknowledgments

I would like to express my sincere gratitude to my thesis supervisors, Prof. Vittorio Camarchia and Dr. Anna Piacibello, for their guidance, support, and invaluable insights throughout the research process. Their expertise and encouragement have been instrumental in shaping the direction of this thesis.

I am also grateful to my colleagues and friends for their encouragement, support, and understanding during challenging times.

Special thanks are due to my family for their unwavering love, encouragement, and belief in my abilities. Their support has been a constant source of strength and motivation throughout this journey.

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Acronyms

PA	Power Amplifier
MN	Matching Network
EM	Electromagnetic
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
SS	Small Signal
DE	Drain Efficiency
TX	Transmitter
RX	Receiver
RF	Radio Frequency
RFC	RF Choke
PAE	Power Added Efficiency
UHF	Ultra High Frequency
OMN	Output Matching Network
IMN	Input Matching Network
ADS	Advanced Design System
LNA	Low Noise Amplifier
NF	Noise Figure
HB	Harmonic Balance

Chapter 1

Introduction

Power amplifiers (PAs) are the final stage in the transmitter chain and their design and characterization require specific care. Their performance significantly affects overall system behavior and their design becomes more challenging for operating in the ultra-broadband frequency range [5] [7] [10] [2].

Broadband power amplifiers are indispensable for several reasons, mainly because of the growing need for communication systems that offer wider frequency coverage, enhanced data rates, and improved transmission efficiency. They are pivotal in facilitating smooth and effective wireless communication across diverse applications and technologies.

In a multi-octave PA, the second harmonic load of the lower octave acts as the fundamental load of the higher octave [7], which means that in an optimization procedure, the input impedance of the Matching network (MN) is moved toward the optimum load/source impedance that the transistor needs to see at every frequency to the greatest extent possible. In a wideband design, however, it is not feasible to perfectly match the realized impedance to the optimum points, and some mismatch is

inevitable [5].

This thesis presents the broadband design and implementation of a hybrid class AB PA, maintaining good performance in terms of Gain and Efficiency over a frequency range from 500 MHz up to 4 GHz.

The thesis content is organized as follows. In the next sections of the current chapter, target performance and selection of active device are presented. In Chapter 2, the theoretical background and fundamental concepts are reviewed. The main challenges of Broadband design and circuit design steps are explained in detail in Chapter 3, while Layout planning and Electromagnetic (EM) simulation results are covered in Chapter 4. Conclusions on overall PA performance are presented in Chapter 5.

1.1 Target Performance

In this section, the desired specifications of the designed PA are presented in Table 5.1.

Frequency	Power Gain	P_{out}	Efficiency
(0.5-4) GHz	Best Effort	20 W	Best Effort

Table 1.1: Summary of the target performance

The proposed PA has a functionality over 3 octaves (from 500 MHz up to 4 GHz) and hence, the most important figure of merit in terms of Power Gain, is its flatness. Maintaining a flat gain response over the entire bandwidth is one of the challenges that must be dealt with and it is addressed in more detail in Chapter 2.

The desired saturated output power is around 20 W which can be achieved with a proper choice of active device. In this case, the 25 W CGH40025 transistor was chosen, which provides enough margin to reach the power target over a very broadband. The details about the active devices will be provided in 1.2.

A uniform and relatively flat efficiency performance over the entire bandwidth must be ensured. The efficiency level is kept as high as possible, based on the design steps described in Chapter 2.

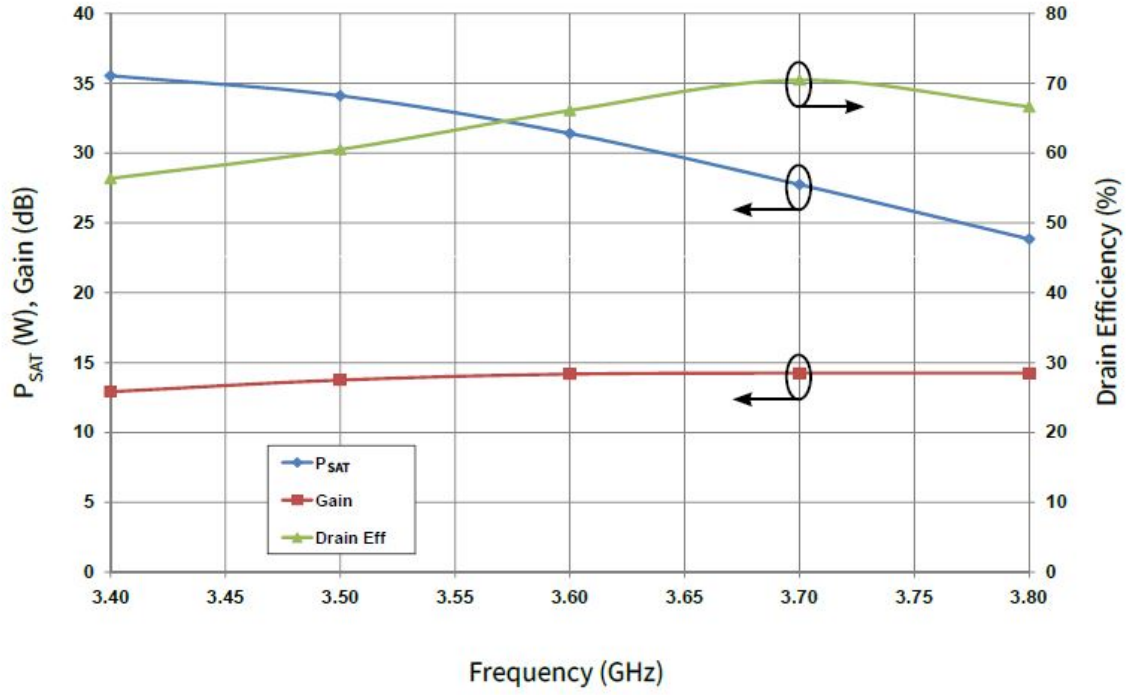
1.2 Active Device

In this thesis research, a Wolfspeed's CGH40025 25W Gallium Nitride (GaN), High Electron Mobility Transistor (HEMT), has been chosen to meet the desired specifications. GaN HEMTs offer high power density, high efficiency, high gain, and wide bandwidth capabilities, making the CGH40025 ideal for linear and compressed amplifier circuits [19].

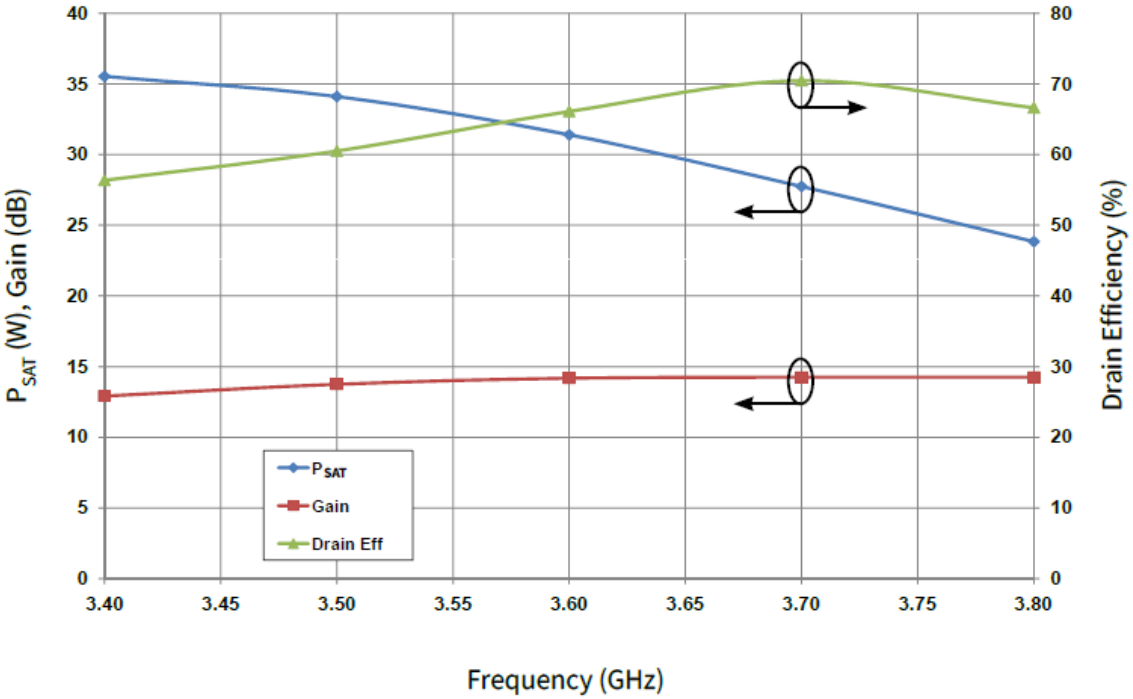
CGH40025 is capable of operating from DC up to 6 GHz, providing 30 W saturated output power and even more than 62% efficiency.

This transistor is suitable for various applications such as 2-way Private Radio, Broadband Amplifiers, Cellular Infrastructure, Test Instrumentation, etc.

In Figure 1.1 some typical performances of the active device are reported.



(a)



(b)

Figure 1.1: Typical performance of the active device, Small signal (SS) gain and Input return loss vs Frequency (a), P_{sat}, Gain, and Drain Efficiency (DE) vs Frequency (b), [19]

Chapter 2

RF Power Amplifiers

Wireless communication refers to the transmission of information without the use of physical cables or wires. It relies on electromagnetic waves to carry data between devices, making it a versatile and widely used technology in modern society.

In wireless communication systems, there are typically two main components, the transmitter (TX) and the receiver (RX) as shown in figure 2.1. The transmitter is responsible for encoding and modulating the information onto a carrier signal, amplifying it, and transmitting it through the air using antennas. On the other hand, the receiver captures the transmitted signal using antennas, demodulates it, and decodes the information to retrieve the original data.

In the TX chain of wireless communication systems, the PA plays a critical role in boosting the signal strength of the modulated radio frequency (RF) carrier before transmission. A PA needs to amplify the input signal achieving the requested output power most efficiently. moreover, the active device selected for this task must satisfy some requirements related to nonlinear large-signal behavior such as breakdown

voltage, maximum current and power [3].

In the subsequent sections, further elaboration is provided on various aspects of PA figures of merit and PA classifications.

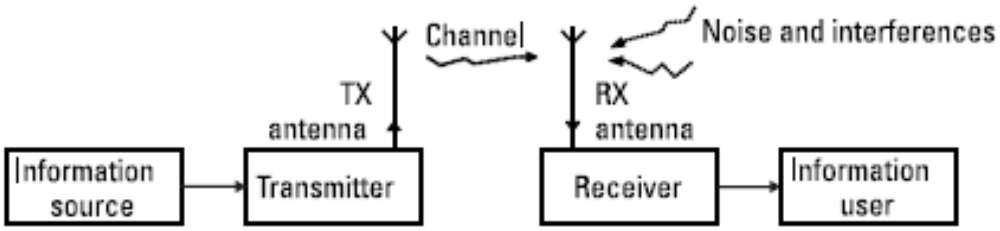


Figure 2.1: Transmitter and Receiver in Communication Systems [3]

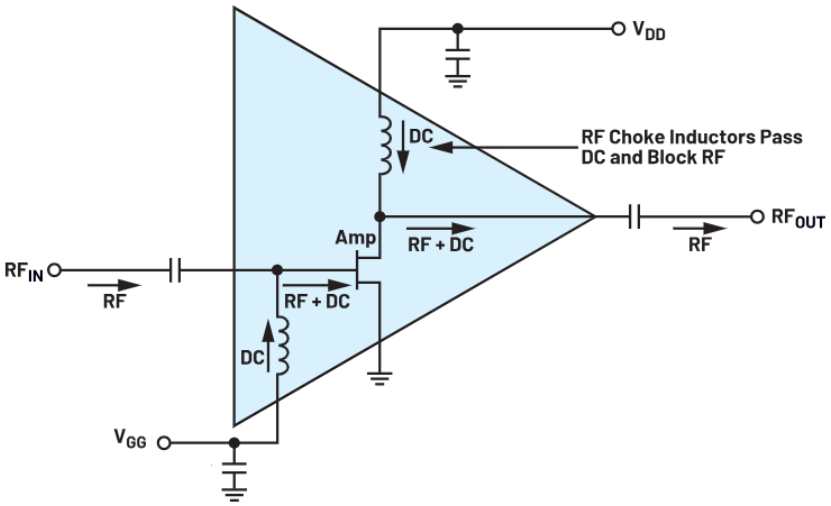


Figure 2.2: General PA schematic

2.1 PA Theory

A PA is the most power-hungry block at the end of TX chain, which increases the power level of the signal at its input at a given frequency band to a specific output level. To limit the power consumption, PA operates under large-signal conditions which make the device swing over

the whole nonlinear operation region, making output signal distorted. For this reason, a PA is considered as a nonlinear component and several trade-offs must be dealt with when it comes to PA design. such conflicting requirements can be named linearity vs. efficiency or high output power vs. low distortion. the design approach also depends on operating frequency, bandwidth, device technology, etc [12].

Figure 2.2 illustrates the block diagram of a standard PA. In this configuration, the input of the active device is sourced from two paths. One path incorporates a DC-blocking capacitor, ensuring the passage of only RF signals. Conversely, the RF choke (RFC), characterized by large inductance in the Bias line, establishes a DC route to the active device while preventing the transmission of incoming RF signals. This arrangement, known as a BiasT topology, is similarly employed in the output of the active device for the same reasons.

The PA input is normally a narrowband signal centered at frequency f_0 and there are different power definitions in PA theory. The Available power (P_{AV}) is the power that is coming from the signal source while the Input power (P_{I}) is the actual power inserted in the PA and it is not equal to (P_{AV}) due to reflections. Output power (P_{O}) is the power delivered to the load. This conversion of power from input to output is provided by DC power (P_{DC}). Figure 2.3 illustrates power flow in a typical PA. Based on these definitions several figures of merit can be defined.

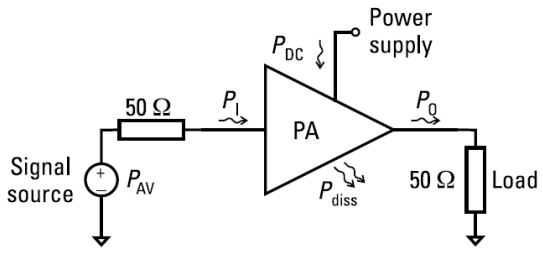


Figure 2.3: Power flow in a PA [3]

Power Gains

The ratio between output power and input power is called Power gain. There are different Power gain definitions based on the power seen in the device e.g. the power entering the PA or the available power from the source [3]. The Operative gain is:

$$G_{\mathrm{P}} = \frac{P_{\mathrm{O}}(f_0)}{P_{\mathrm{I}}(f_0)}, \tag{2.1}$$

while the Transducer gain is as follows:

$$G_{\mathrm{T}} = \frac{P_{\mathrm{O}}(f_0)}{P_{\mathrm{AV}}(f_0)}. \tag{2.2}$$

Efficiency

The ratio between output power at fundamental frequency and DC power is defined as Efficiency:

$$\eta \ = \frac{P_{\mathrm{O}}(f_0)}{P_{\mathrm{DC}}}, \tag{2.3}$$

which is also referred to as DE. A shortcoming of this definition is that it does not account for the RF power delivered at the input to the amplifier. Therefore, another way of defining the efficiency is sometimes more useful. This is is called Power-Added Efficiency (PAE):

$$PAE = \frac{P_{\mathrm{O}}(f_0) - P_{\mathrm{I}}(f_0)}{P_{\mathrm{DC}}} = \eta \ (1 - \frac{1}{G_{\mathrm{P}}}). \tag{2.4}$$

Stability

The stability issue is important in the PA design. We want a stable, non-oscillating behavior for amplifiers. There are some parameters to determine if an amplifier is unconditionally stable or conditionally stable. These criteria utilize inequalities involving a pair of parameters, which are dependent on the S-parameters of the two-port system. This includes

both the two-parameter stability criteria and those based on a single parameter, known as one-parameter stability criteria [6]. Two-parameter criteria are as follows:

$$K = \frac{1 - |S_{22}|^2 - |S_{11}|^2 + |\Delta|^2}{2|S_{21}S_{12}|} > 1 \tag{2.5}$$

while Δ must satisfy:

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| < 1. \tag{2.6}$$

One-parameter criteria can be described by any of the subsequent equations:

$$\mu_1 = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^*\Delta| + |S_{21}S_{12}|} > 1 \tag{2.7}$$

$$\mu_2 = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^*\Delta| + |S_{21}S_{12}|} > 1. \tag{2.8}$$

Maximum Available Gain

If a PA is unconditionally stable, its Maximum Available Gain (MAG) can be achieved and it is described as follows [6]:

$$MAG = \frac{|S_{21}|}{|S_{12}|}(K - \sqrt{K^2 - 1}). \tag{2.9}$$

2.2 PA Classes

PAs can be categorized based on their operational modes and classes. The classification of PAs into A, AB, B, and C is determined by the quiescent bias point [3]. Various bias points are depicted on the output and transfer characteristics of the ideal FET-like device in Figure 2.4.

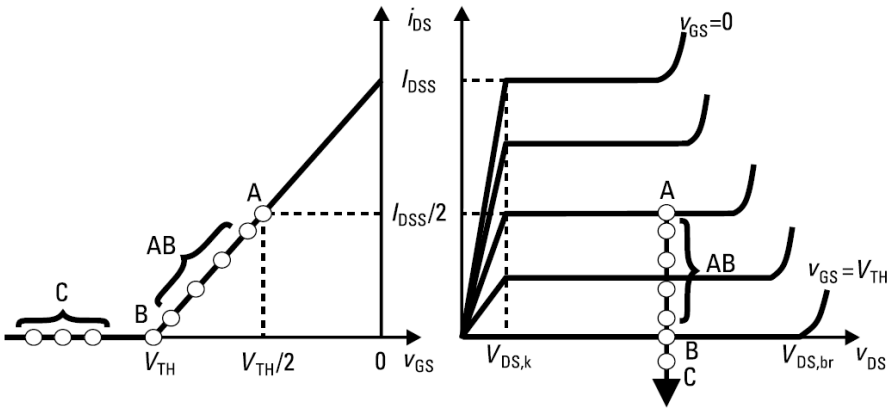


Figure 2.4: The transfer characteristics (a) and output characteristics (b) of an ideal FET vary according to different bias point classifications [3].

Class A

Class A amplifiers are characterized by their inherently linear nature, as the transistor conducts over the entire input signal cycle due to biasing. Consequently, class A amplifiers theoretically achieve a maximum efficiency of 50%. Many small-signal and low-noise amplifiers operate as class A circuits [14]. The load line and typical waveforms of a class A PA are demonstrated in Figure 2.5 and Figure 2.6.

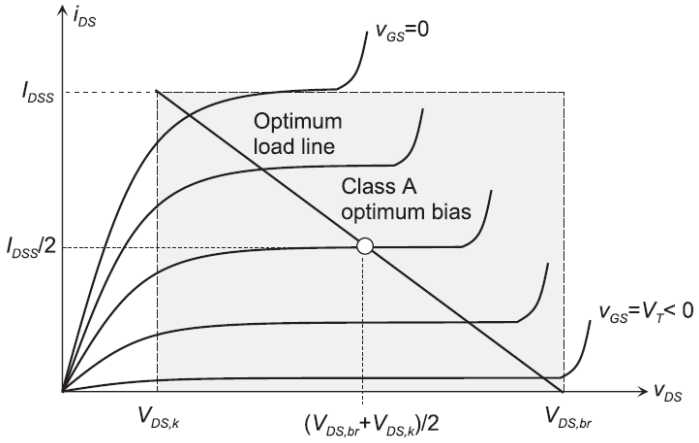


Figure 2.5: Load line of class A amplifier with optimum load [6]

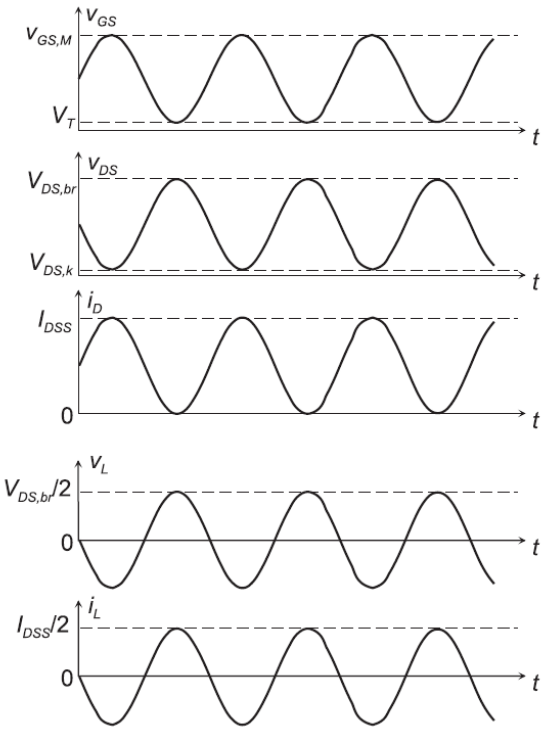


Figure 2.6: Waveforms of a class A amplifier [6]

Class B

In class B amplifiers, the transistor is biased to conduct solely during one-half of the input signal cycle. Typically, two complementary transistors are employed in a class B push-pull amplifier to facilitate amplification across the entire cycle. The theoretical efficiency of class B amplifiers stands at 78% [14]. Figure 2.7 and Figure 2.8 illustrate the load line and standard waveforms of a class B power amplifier respectively.

Class AB

Class AB amplifiers operate in between Class A and Class B in terms of conducting angle and, as a result, they can achieve a higher efficiency than Class A but lower than Class B amplifiers. They provide a balance between the two classes A and B in terms of efficiency and linearity.

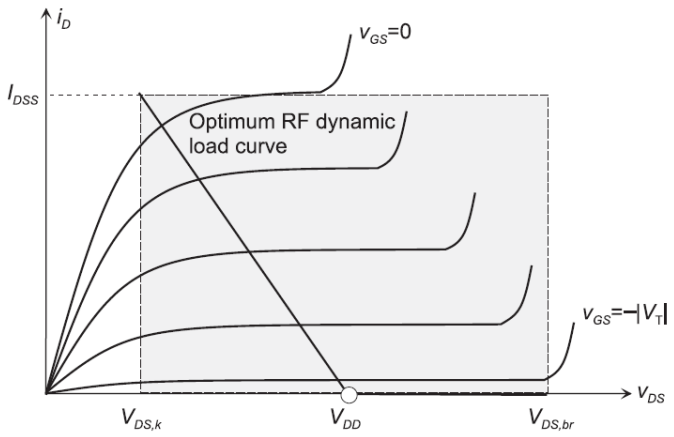


Figure 2.7: Load line of class B amplifier with optimum load [6]

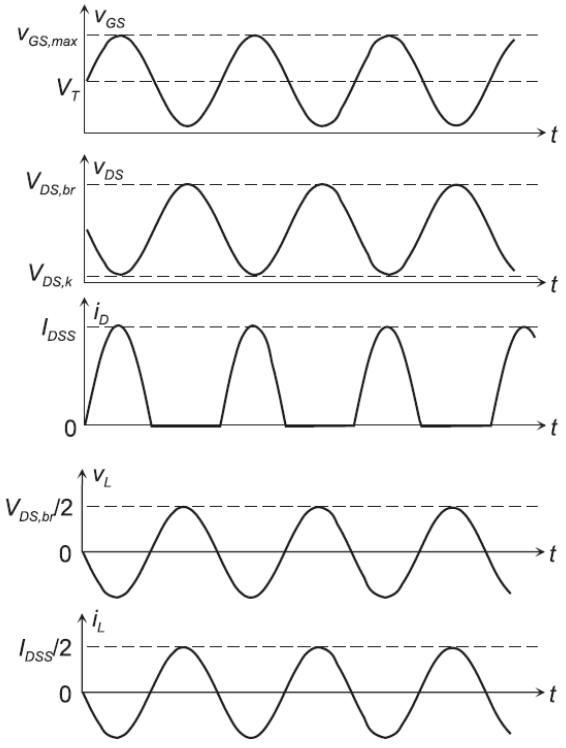


Figure 2.8: Waveforms of a class B amplifier [6]

Class C

Class C amplifiers operate with the transistor below the cutoff for more than half of the input signal cycle and typically integrate a resonant circuit in the output stage to recover the fundamental frequency. While class C amplifiers can approach efficiencies close to 100%, they are primarily compatible with constant envelope modulations [14].

Other Classes

Higher classes like class D, E, F, and S leverage the transistor as a switch to energize a highly resonant tank circuit, potentially achieving very high efficiencies. However, the majority of communication transmitters operating at Ultra High Frequencies (UHF) or higher opt for class A, AB, or B PAs due to the necessity for low-distortion products [14].

Figure 2.9 demonstrates the overall behavior of different PA classes for the Current Conducting Angle (CCA). The basic characteristics of

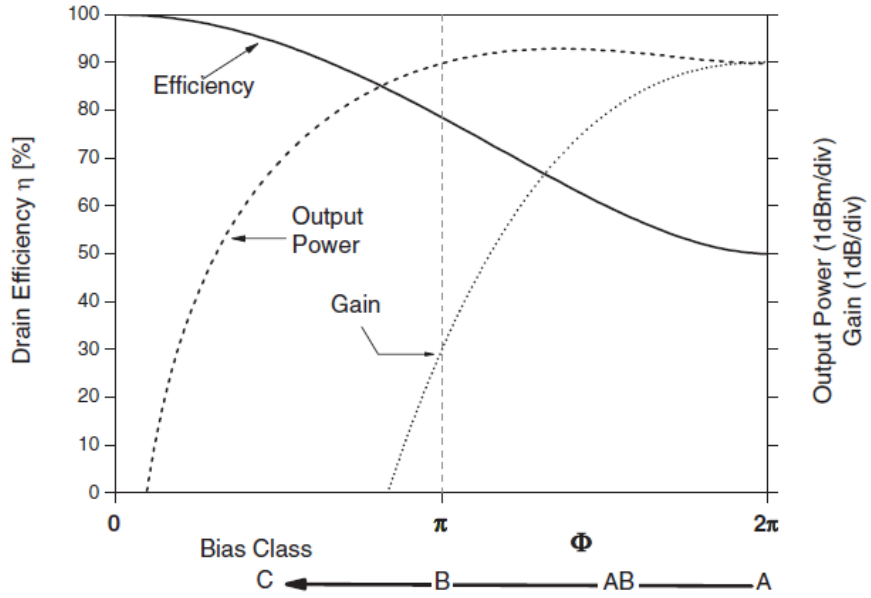


Figure 2.9: Tuned Load theoretical performance as a function of the drain CCA [12]

PA classes are written in Table 2.1.

Class	VGG	IDD	CCA	η_{max}
A	$V_{th}/2$	$I_{DSS}/2$	2π	50%
B	V_{th}	0	π	78.5%
AB	$V_{th} < ... < V_{th}/2$	$0 < ... < I_{DSS}/2$	$\pi < ... < 2\pi$	$50\% < ... < 78.5\%$
C	$... < V_{th}$	0	$... < \pi$	100%

Table 2.1: Summary on PA classes

Chapter 3

Circuit Design

In this chapter, the design procedure is introduced in detail. As mentioned in Chapter 1, the active device is CGH40025 25W GaN and the DC characteristics of the device are analyzed then the stability behavior of the device including the real bias lines is investigated. Since it is a broadband design, various Load-pull simulations for equal frequency spacing have been done, and based on the simulation results, proper Output Matching Network (OMN) and Input Matching Network (IMN) are introduced. The design environment is Keysight Advanced Design System (ADS).

3.1 Active Device Characteristics

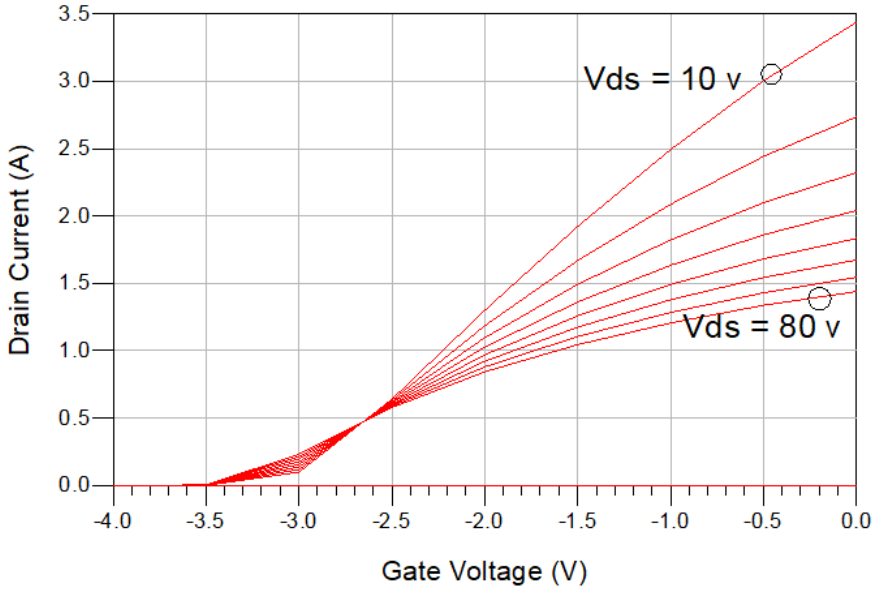
In this section, DC characteristics, stability analysis, and bias network topology are introduced. Then load-pull simulation for broadband device is investigated and an optimum trajectory for load impedance in terms of a trade-off between output power and efficiency, is obtained.

3.1.1 DC Characteristics

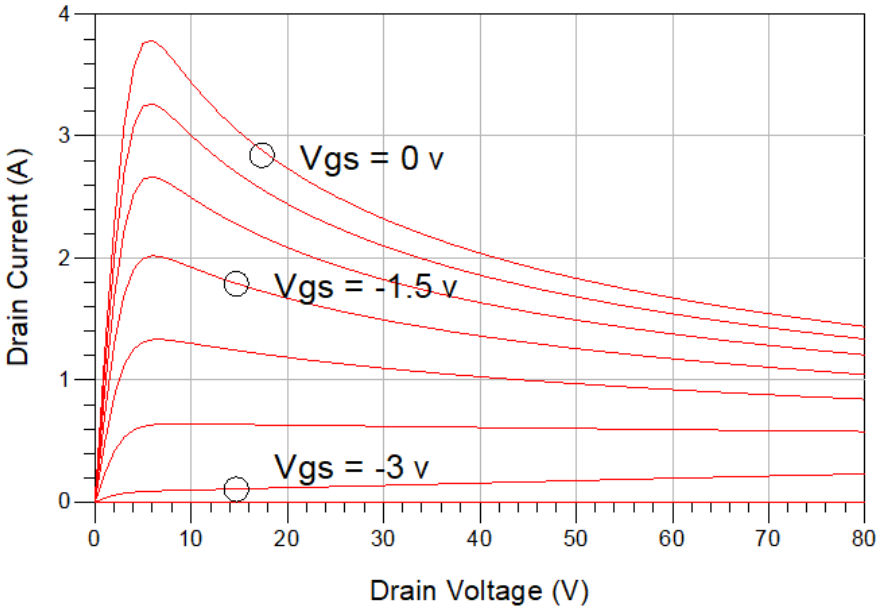
The first step in PA design is DC bias point selection. Figure 3.1 represents the active device's trans-characteristic and output-characteristic respectively. These figures show the relation between drain current and gate and drain voltages. The gate voltage is swept from -4 V up to 0 V and the drain voltage is swept from 0 V up to 80 V. To ensure that the device is operating in class AB, with the use of the data sheet, the gate voltage of -2.8 V and the drain voltage of 28 V is selected. As a result, the drain current is around 0.31 A, and its peak value is around 3.7 A.

3.1.2 Stability

Amplifiers are not always unconditionally stable in the entire design bandwidth. To avoid instabilities and oscillations, especially in lower frequency ranges, we must stabilize the circuit using passive elements either in the input or the output. Figure 3.2 illustrates a typical stabilization network. For PA design, input stabilization is mostly used so the output power and gain are not reduced, while for Low Noise Amplifiers (LNAs), for the sake of Noise Figure (NF), output stabilization is preferred.



(a)



(b)

Figure 3.1: Trans-characteristics (a) and Output-characteristics (b) of the active device

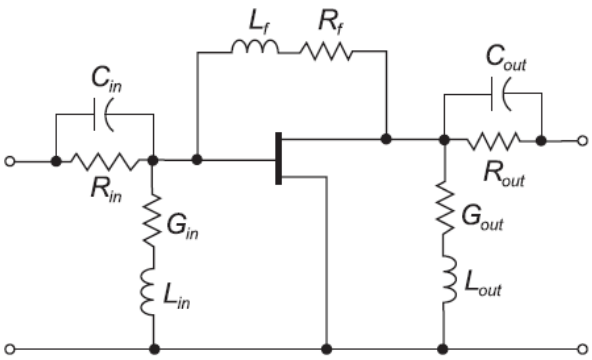


Figure 3.2: Stabilization network [6]

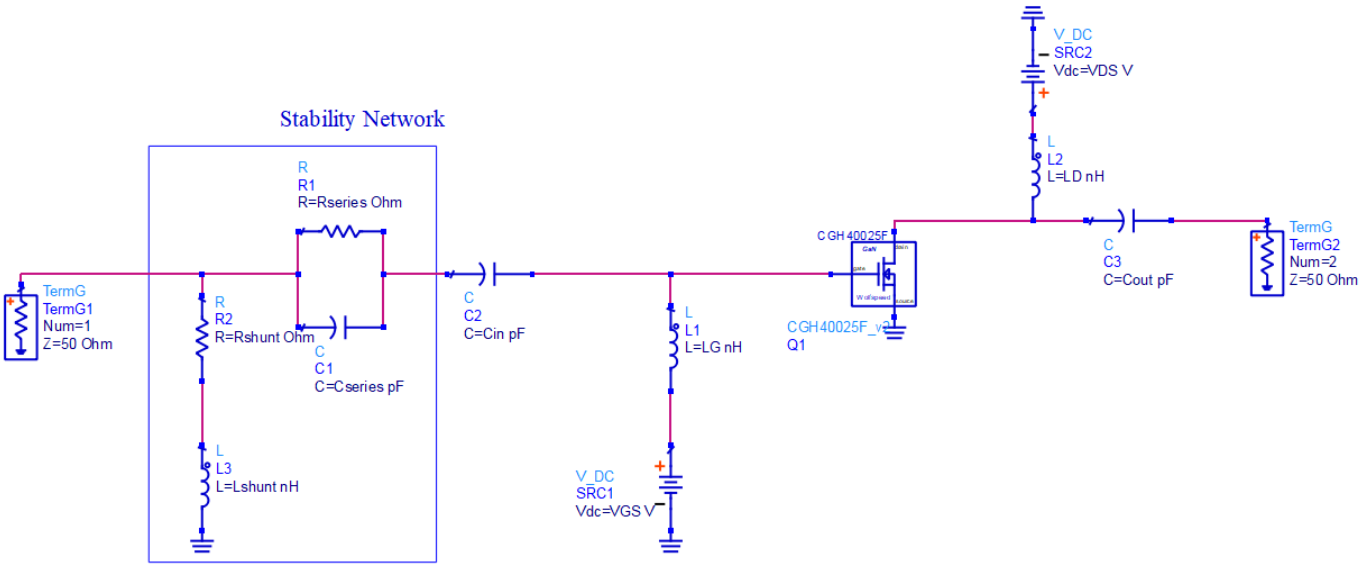


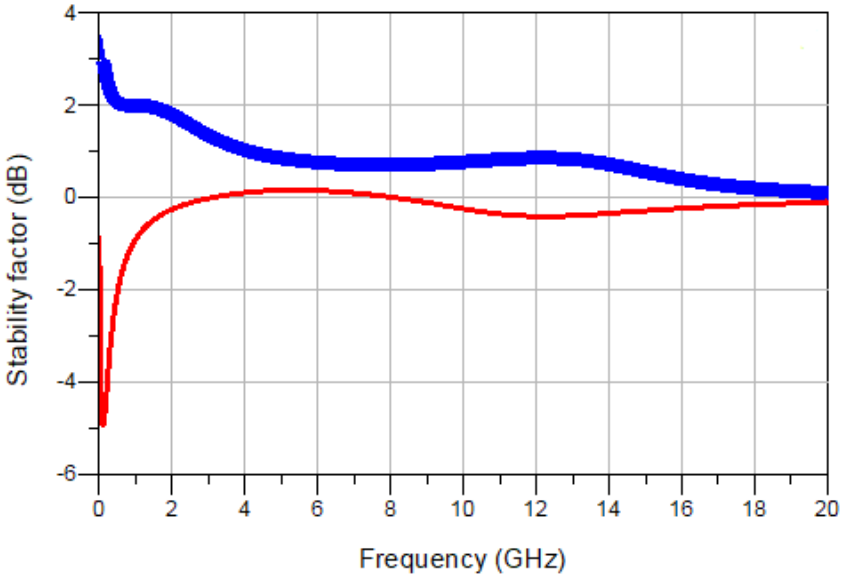
Figure 3.3: Stabilization network with ideal bias

Figure 3.3 is the schematic of the stabilized circuit with ideal bias lines. The obtained value for shunt and series resistors is 10Ω and for the series capacitor is 5 pF. These values are chosen for maximum gain and gain flatness for the entire bandwidth. As it is seen in Figure 3.4 the value of $\mu 1$ is higher than 0 dB, which indicates that the circuit is indeed stable, however MAG is inevitably lower than before.

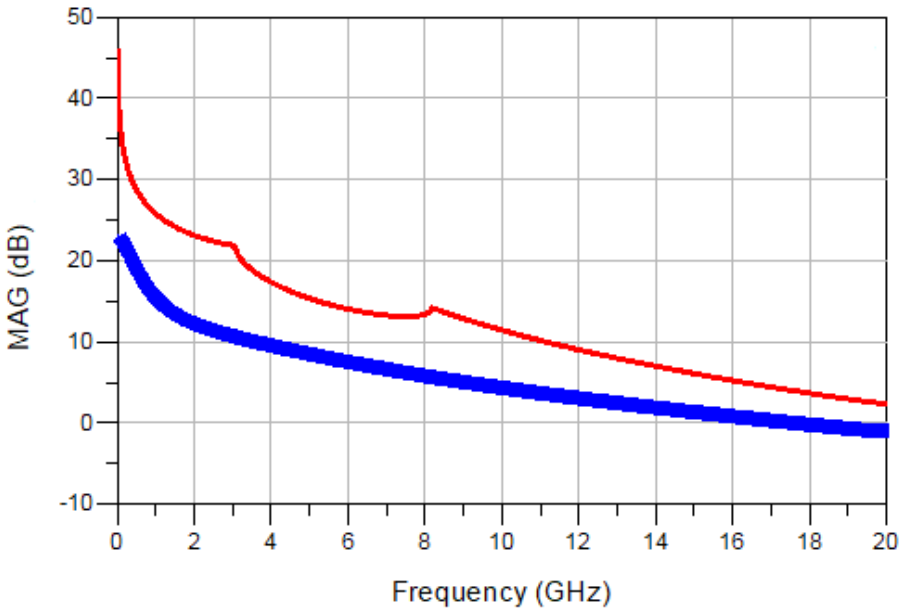
3.1.3 Bias Network

The proper DC biasing of microwave active devices requires specific attention. This involves isolating the DC bias networks from the RF circuit using dedicated circuit components known as bias Ts. The DC voltages applied to the gate and drain of a transistor are sourced from one or two DC sources through a biasing circuit. It is essential to electrically separate these biasing circuits from the RF circuit for several reasons:
1) To prevent DC current from flowing in the passive portion of the RF circuit, which could lead to power dissipation and potential damage.
2) To avoid loading the RF circuit with the DC bias circuit, as its behavior at microwave frequencies is highly unpredictable [6].

The schematic of a DC–RF decoupling network, referred to as the bias T, is illustrated in Figure 3.5 (a). In this configuration, capacitor C1 acts as a DC block while maintaining a low impedance to the RF signal. The inductor L serves as a DC short but behaves as an open circuit at RF frequencies. Additionally, decoupling capacitor C2 serves as an RF ground connected to the DC source. Essentially, the bias T enables direct connection of the DC source (via a short) to the device input or output, while presenting a high impedance (nearly an open circuit) at RF frequencies from the connecting node. Implementing inductors at high frequencies can be challenging, prompting alternative topologies based on distributed elements. The bias T depicted in Figure 3.5 (b) utilizes a lumped capacitor C1 as an RF short. At the center band, an



(a)



(b)

Figure 3.4: $\mu 1$ (a) and MAG (b) with (blue) and without (red) stability network from 0 GHz up to 20 GHz

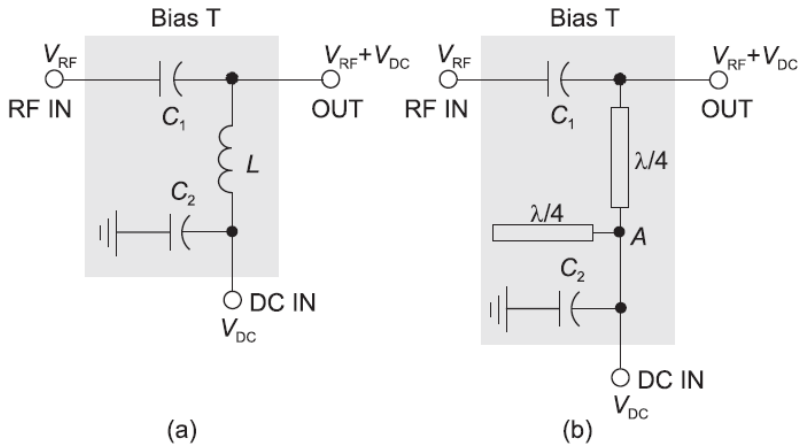


Figure 3.5: Lumped parameter (a) and Distributed parameter (b) of Bias Ts [6].

open $\lambda/4$ stub RF grounds node A, which transitions to an open circuit in the second quarter-wave section. Consequently, the RF impedance from the bias node becomes infinite. Beyond the center band frequency, RF signals are grounded through the blocking capacitor C2 [6].

In figure 3.6 the realized bias T consists of 4 capacitors of values 470 pF, 680 pf, 4.7 nF, and 10 nF. This bias T also includes two shunt resistors of value 10Ω which ensure the low-frequency stabilization. The stability results for real bias T are illustrated in Figure 3.7.

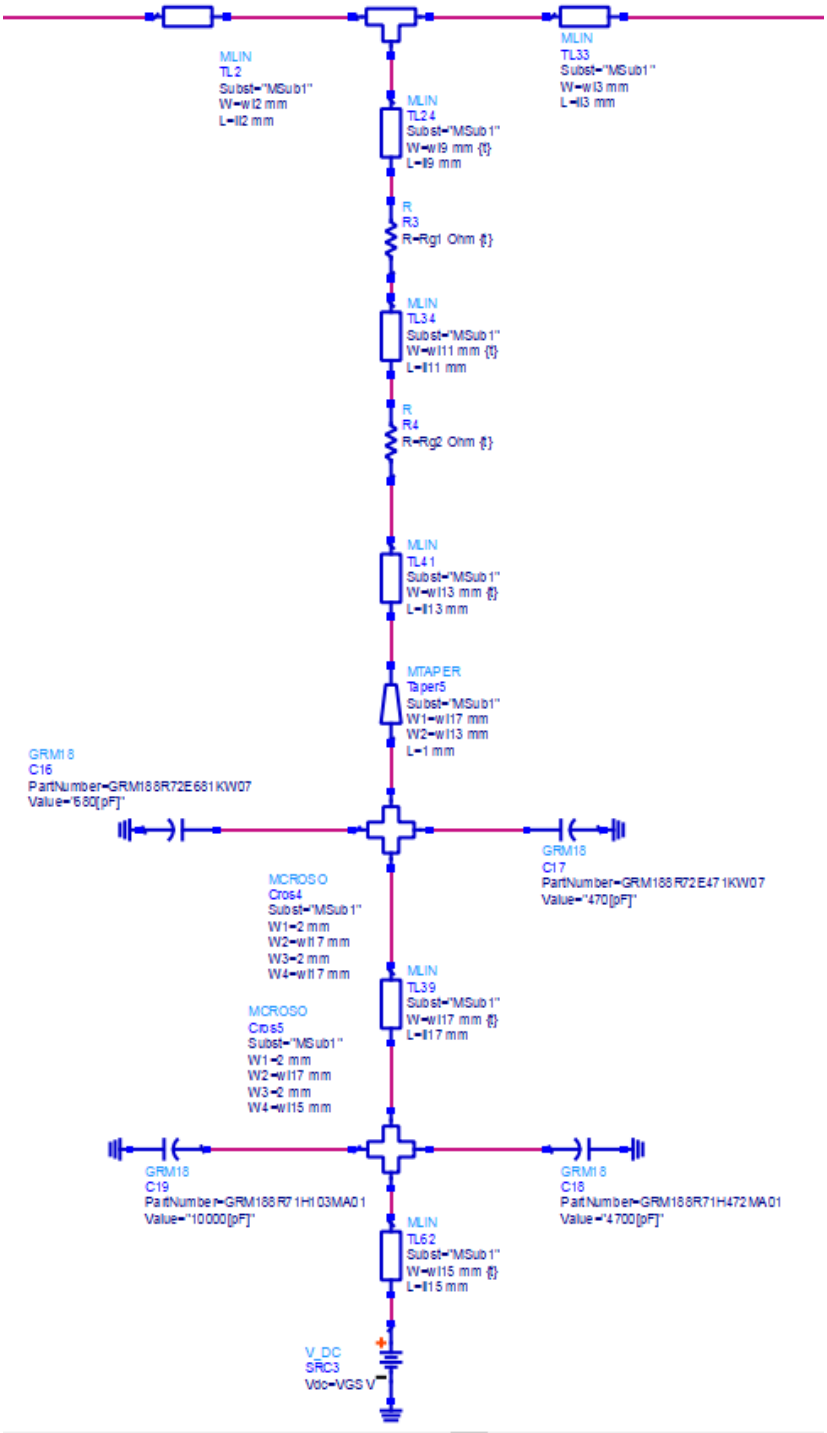
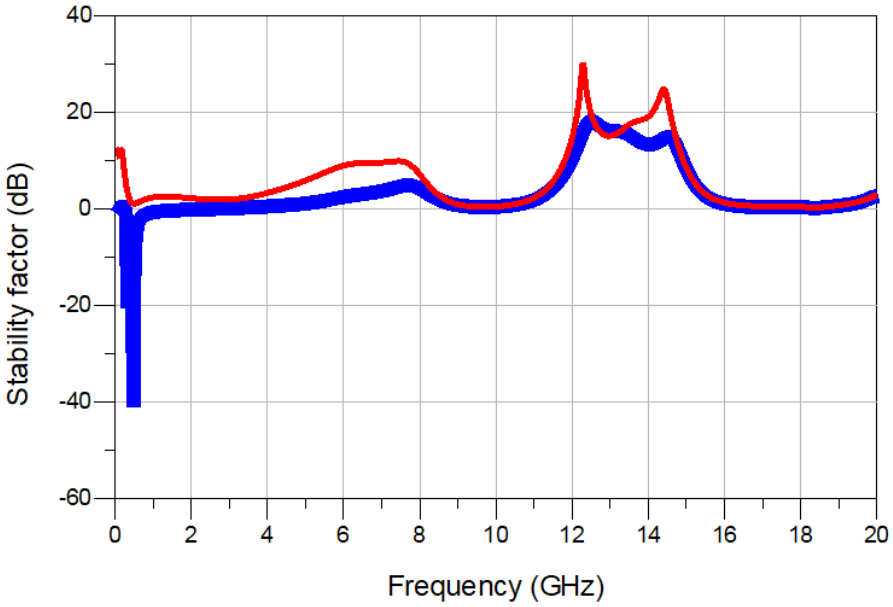
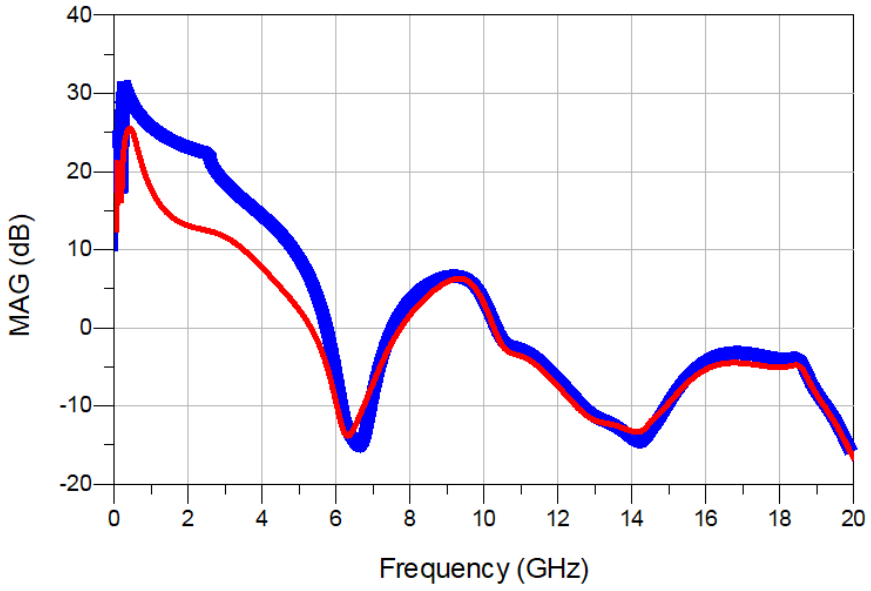


Figure 3.6: Gate Bias T



(a)



(b)

Figure 3.7: $\mu 1$ (a) and MAG (b) with (blue) and without (red) stability network from 0 GHz up to 20 GHz with real Bias T

Since this PA design targets very broadband operation, particular consideration regarding gain flatness must be taken into account. With the use of a simple topology before the gate of the transistor we can further improve gain flatness over the bandwidth (from 0.5 GHz to 4 GHz) [9] [10]. This topology, which consists of two open circuit stubs, is demonstrated in Figure 3.8. The effect of this network is shown in Figure

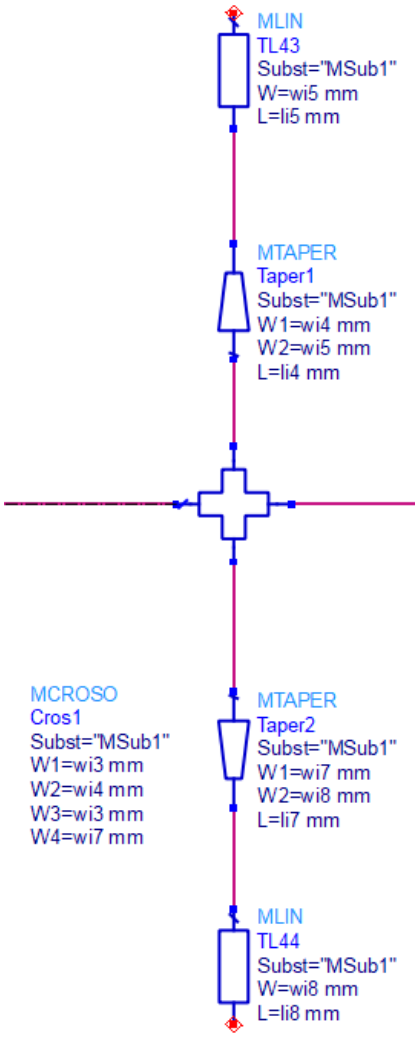
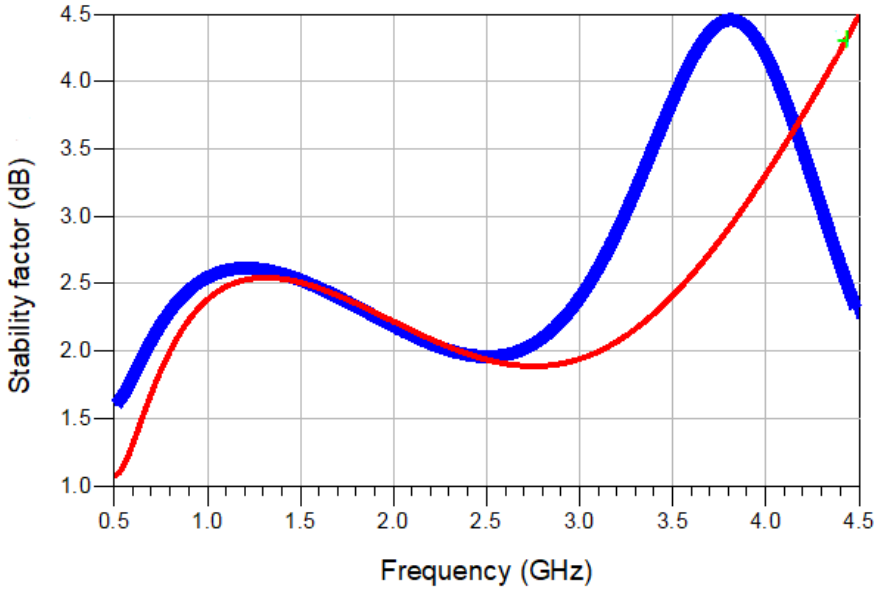


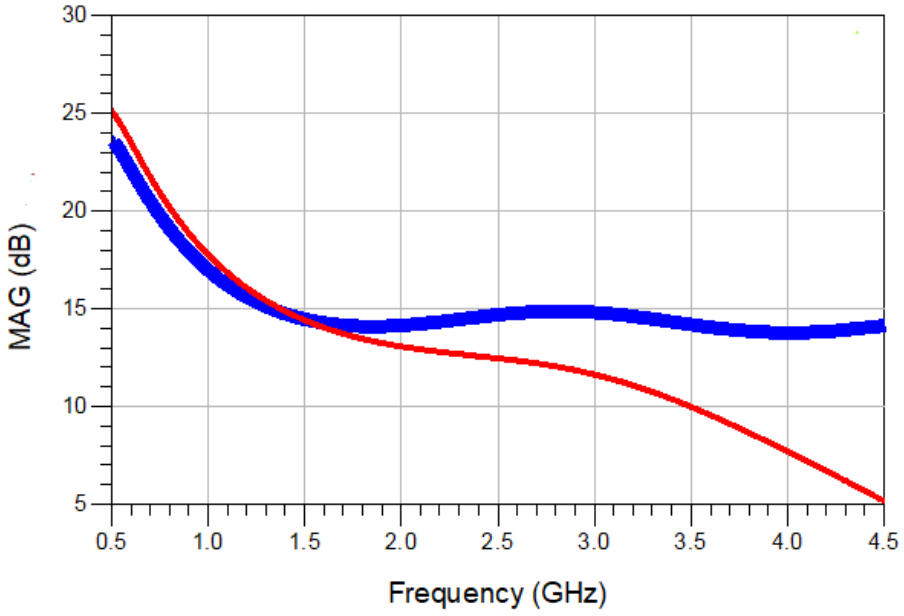
Figure 3.8: Gain Improvement Network

3.9. As it is seen in the desired bandwidth, gate flatness is improved while maintaining stability.

Finally, the full schematic of the circuit with stability network and



(a)



(b)

Figure 3.9: $\mu 1$ (a) and MAG (b) with (blue) and without (red) Gain Improvement network within the desired bandwidth

Bias Ts is illustrated in Figure 3.10

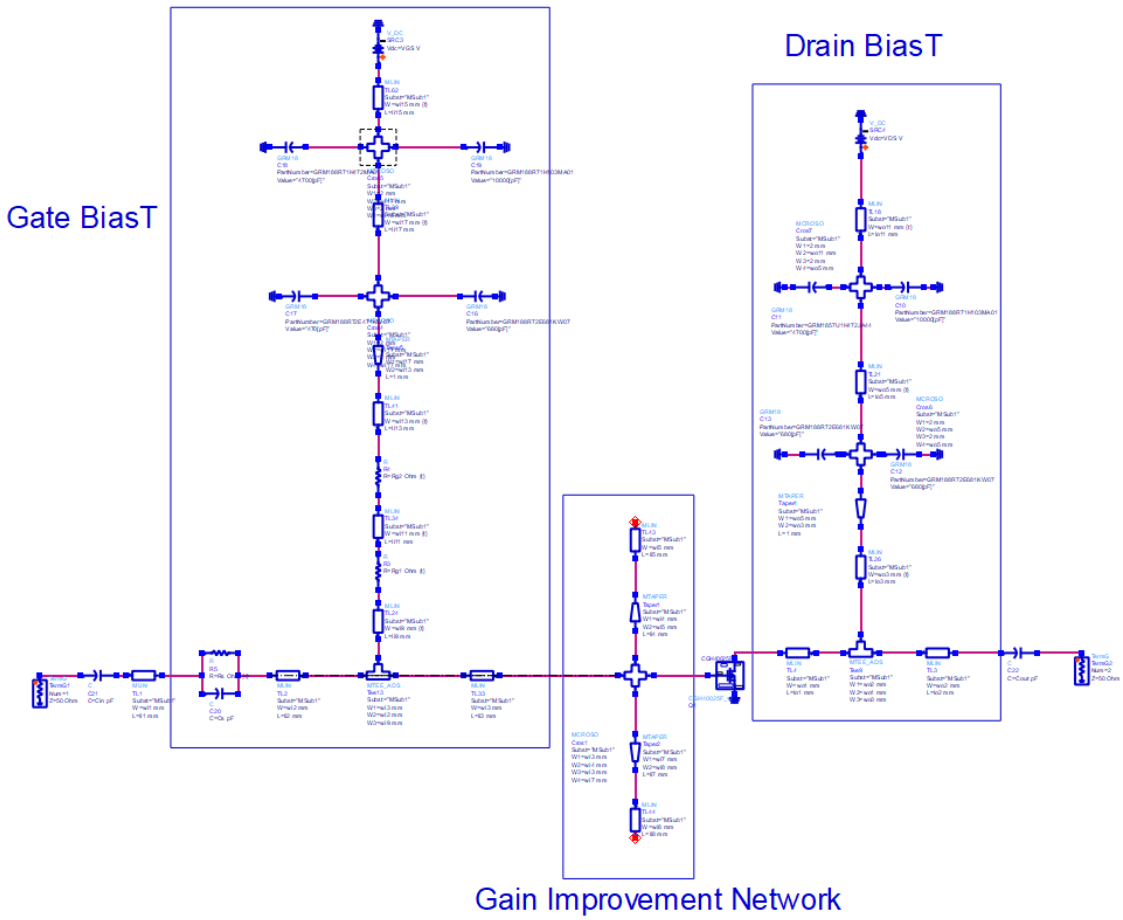


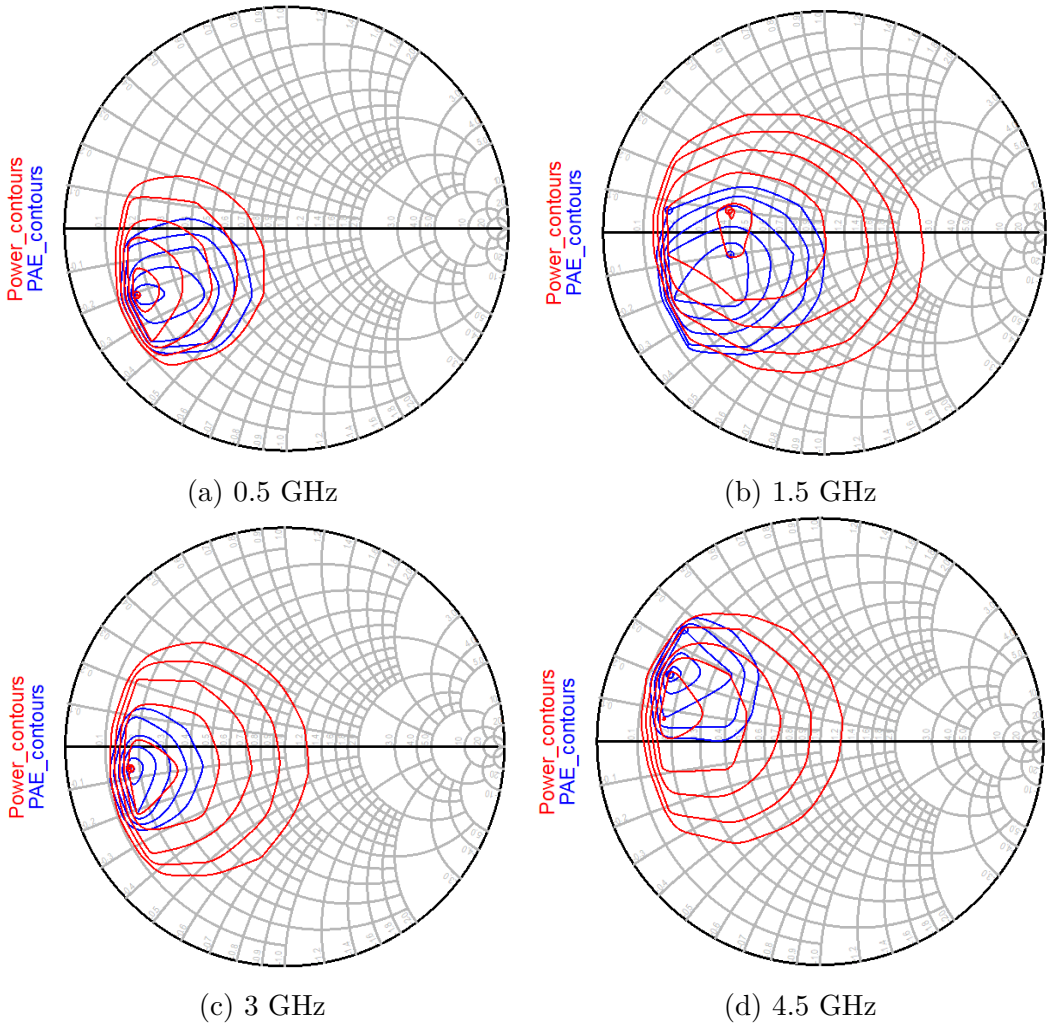
Figure 3.10: Schematic without the matching networks

3.1.4 Optimum Input and Output Terminations

As described previously, designing a broadband amplifier requires an optimum selection for Input and Output termination over the entire frequency range. This task is achieved through the Load-pull template simulation provided in ADS. Due to the device parasitics, the trajectory of optimum terminations varies over the smith-chart. Moreover, the choice of these terminations requires a trade-off between PAE and saturated output power. The optimum harmonic terminations are another aspect that must be taken into account and since for an ultra-broadband design, the harmonics of the lower frequencies fall inside the band, the optimum trajectory must follow a specific path based on the optimum terminations for higher frequencies. Figure 3.11 shows PAE and power contours for different frequencies.

The Load-pull simulation with 250 MHz spacing has been done and based on that, an optimum trajectory for output load is obtained. Moreover to have the minimum reflection in the input and as a result, an equalization between G_T and G_P, a complex conjugate match was considered for source termination [14]. Figure 3.12 shows the optimum trajectory for source and load over the Smith chart.

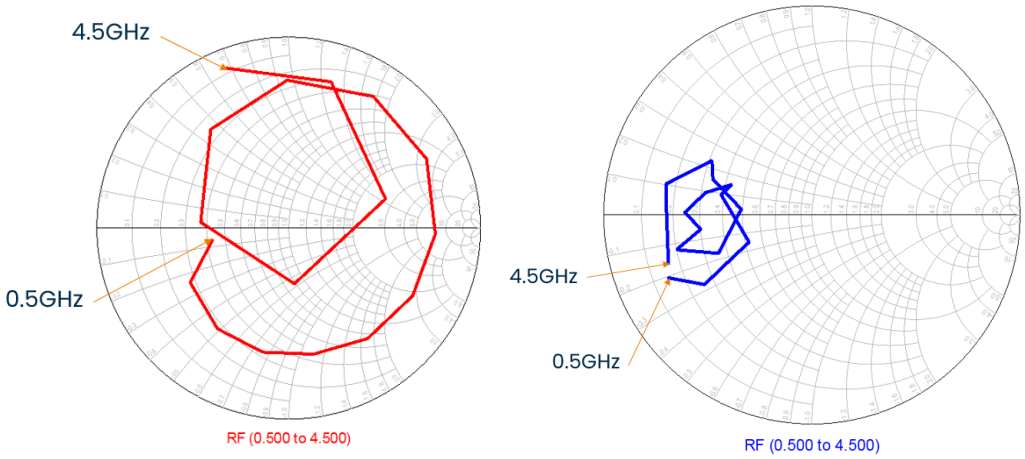
The load trajectory is more or less confined to a small region of the Smith chart. This makes the OMN design rather easier than the IMN design since the source trajectory that is based on complex conjugate varies over the entire Smith chart. Moreover, the trajectories are circulating anti-clockwise from the low frequency up to the high frequency. However, the frequency response of the matching networks is always clockwise from low to high frequency. this particular behavior makes possible mismatches in the design of the matching networks. A possible solution to tackle this problem is to implement so-called non-Foster matching networks [8] so that the trajectories of the optimum terminations will become clockwise, resulting in a lower mismatch.



(a) 0.5 GHz (b) 1.5 GHz

(c) 3 GHz (d) 4.5 GHz

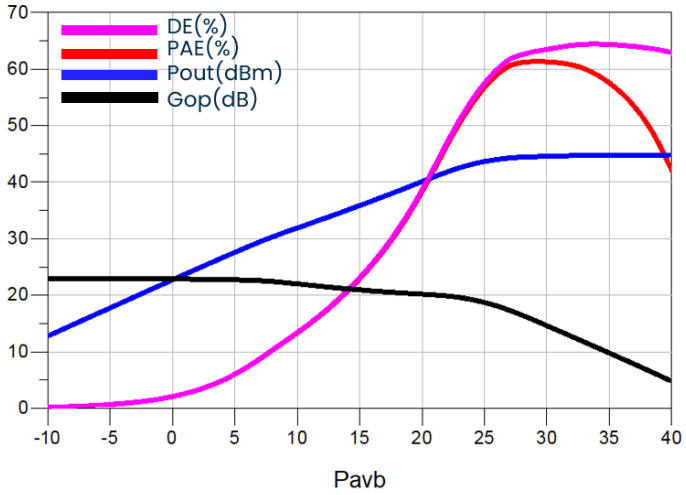
Figure 3.11: PAE and Power contours



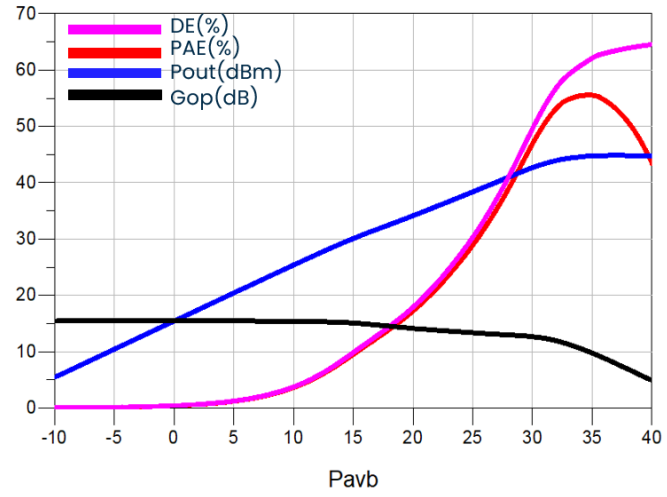
(a) Source trajectory (b) Load trajectory

Figure 3.12: Optimum termination trajectories

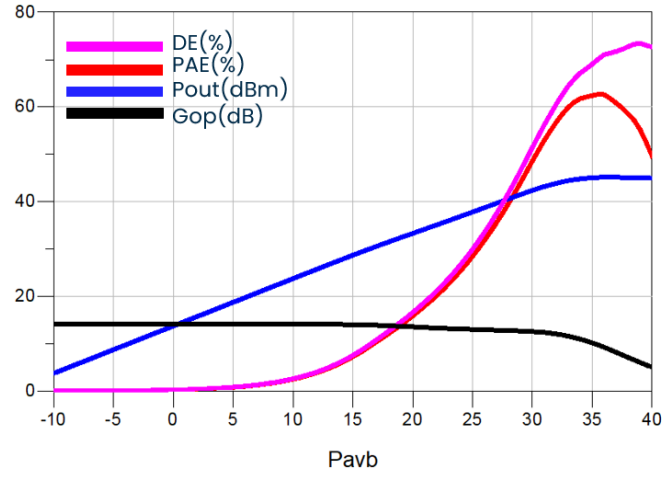
At this stage, using the Harmonic Balance (HB) simulation, we can confirm that the chosen trajectories are indeed suitable for the required circuit performance. Figure 3.13 shows HB results in different frequencies and also figure 3.14 shows the device performance at 35 dBm of input power over the entire band. The PAE is above 55% reaching 65% while the output power is around 45 dBm. due to the conjugate match of the input matching network, G_T and G_{OP} are almost identical.



(a) 0.5 GHz



(b) 2.25 GHz



(c) 4 GHz

Figure 3.13: HB simulation results

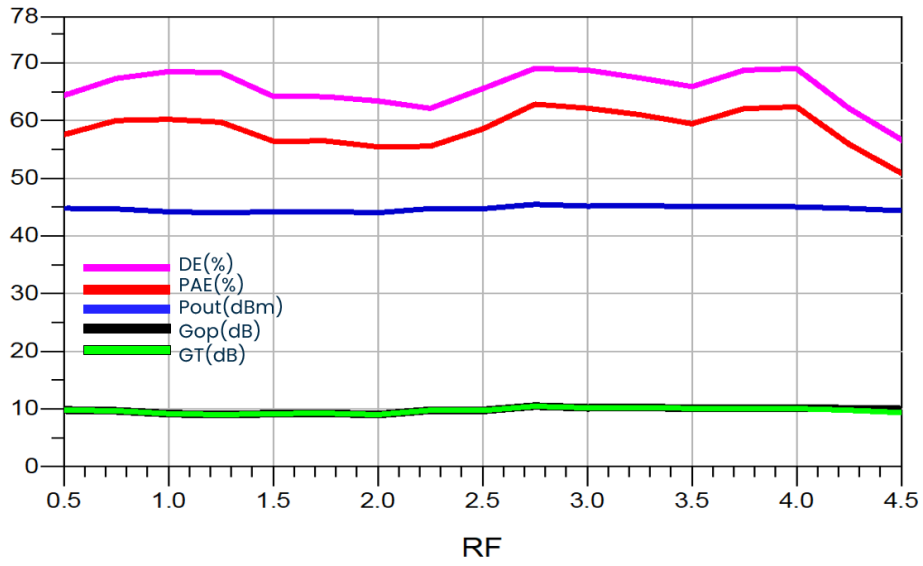


Figure 3.14: HB simulation results at 35 dBm of input power versus Frequency

3.2 Matching Network Design

Matching networks are one of the most important stages of PA design. To have fully matched conditions over the entire bandwidth extra considerations must be taken into account. In this section, the design procedure for Matching networks is explained in detail.

3.2.1 Output Matching Network

For a broadband design, the output matching network must be fully functional over the bandwidth so it is not possible to use simple stab+transmission line topology because of their narrow bandwidth. To overcome this problem a 4-section transformer based on Chebyshev response has been proposed [10].

Chebyshev response

Chebyshev matching transformer optimizes bandwidth at the expense of passband ripple [14]. By equating $\Gamma(\theta)$ to Chebyshev polynomial, we can obtain the desired OMN over the entire frequency. The first two

Chebyshev polynomials are

$$T_1(x) = x \tag{3.1}$$

$$T_2(x) = 2x^2 - 1 \tag{3.2}$$

Higher-order polynomials are obtained using the following recurrence formula:

$$T_n(x) = 2xT_{n-1}(x) - T_{n-2}(x). \tag{3.3}$$

Using the Chebyshev response and Multisection transformers, the OMN is introduced. Figure 3.15 shows the response of a multi-section transformer.

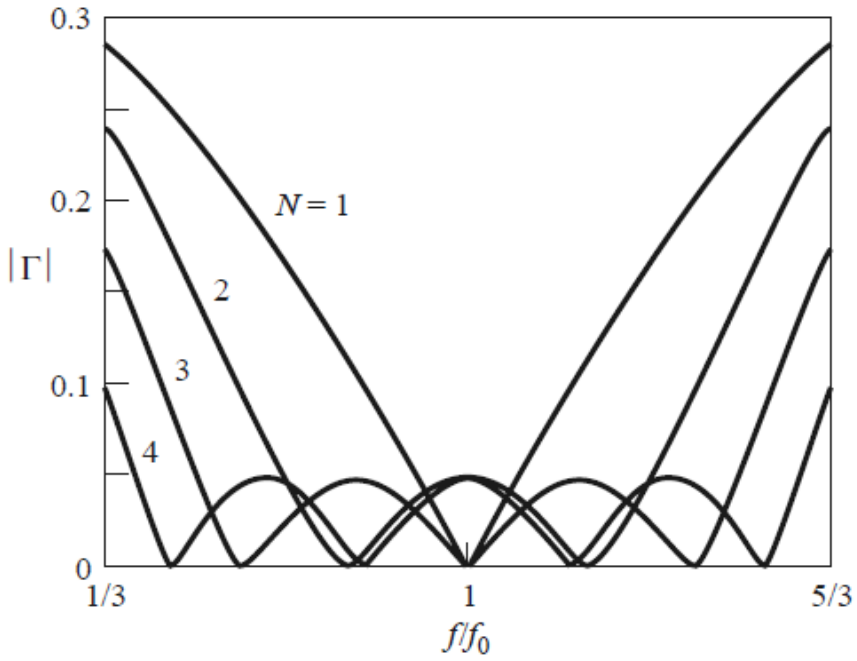


Figure 3.15: Reflection coefficient magnitude versus frequency for the multi-section transformers [14]

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The OMN schematic is proposed in Figure 3.16.

The design procedure targeted the optimum load at the central frequency (2.25 GHz) based on the results obtained from Load-pull simulations and tried to optimize the lengths and widths of transmission lines.

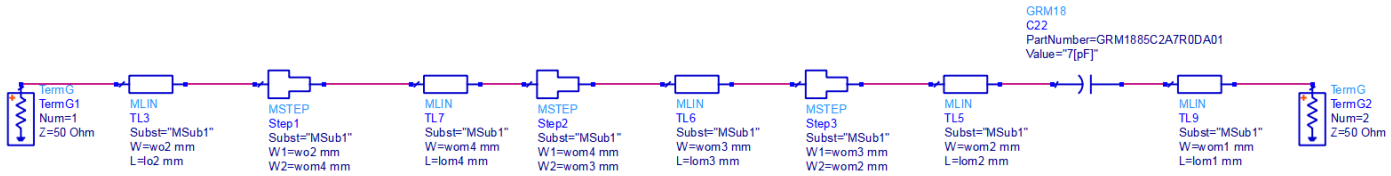

Figure 3.16: Proposed OMN

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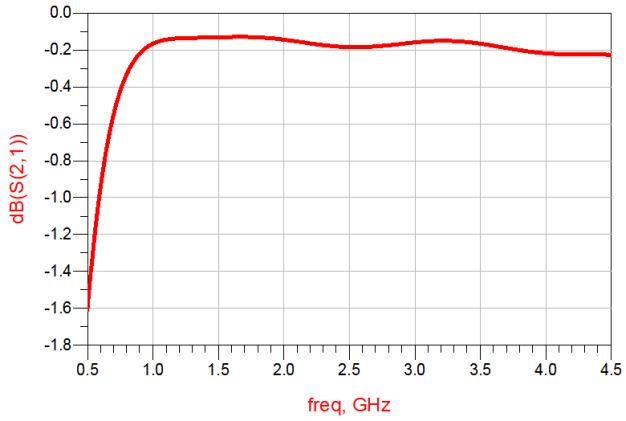
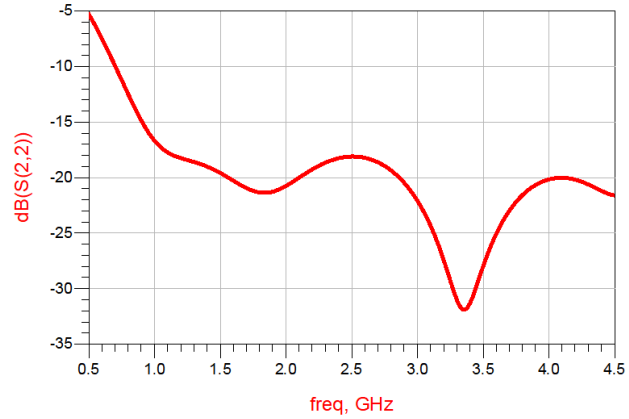
The S-parameters are shown in Figure 3.17.

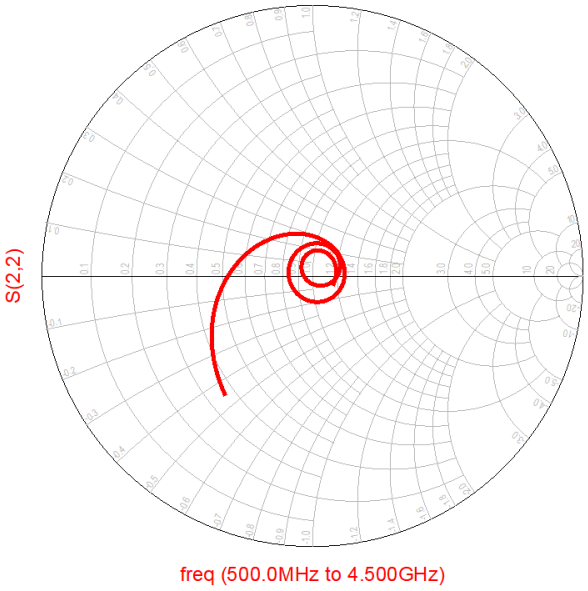
The proposed matching network is considered to be a real-to-real impedance matching and it does not consider device output parasitic variations with frequency. The complete matching network includes the Drain bias network, which compensates for parasitics. The complete OMN schematic and S-parameters are shown in Figure 3.18 and Figure 3.19 respectively.



(a)



(b)



(c)

Figure 3.17: S-parameters of OMN

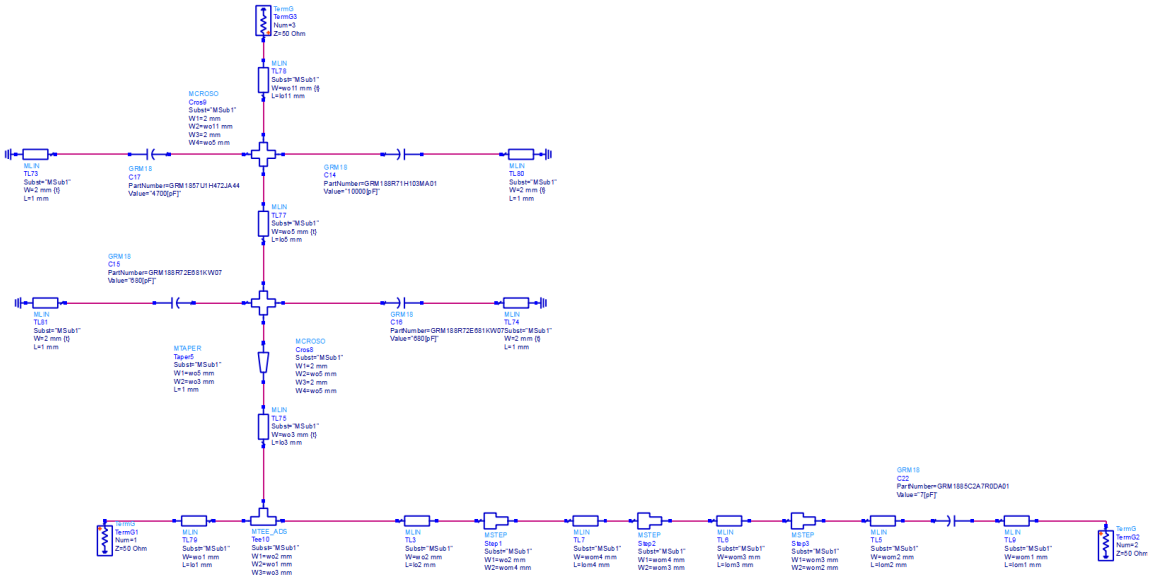


Figure 3.18: OMN with the bias line

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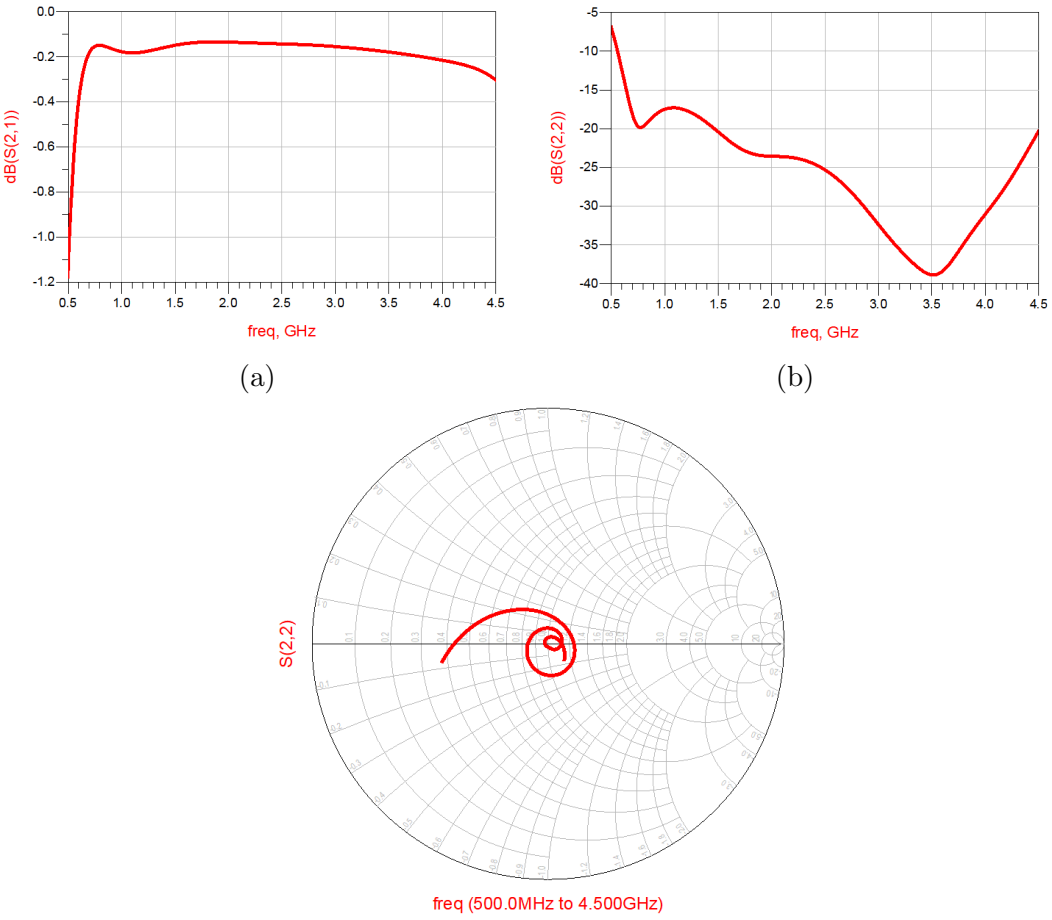
3.2.2 Input Matching Network

As discussed before, the desired match at the input is considered to be a conjugate match for the entire bandwidth however, it seems to be impossible due to the change of optimum source impedance over the whole Smith chart and not to a specific region. For this matter, a trade-off between minimum reflection and gain equality must be considered. Figure 3.20 shows the proposed IMN. this topology provides a relatively good reflection in the bandwidth and doesn't lose too much gain. Figure 3.21 illustrates the S-parameters of IMN.



(a) (b)

(c)

Figure 3.19: S-parameters of OMN with the bias line

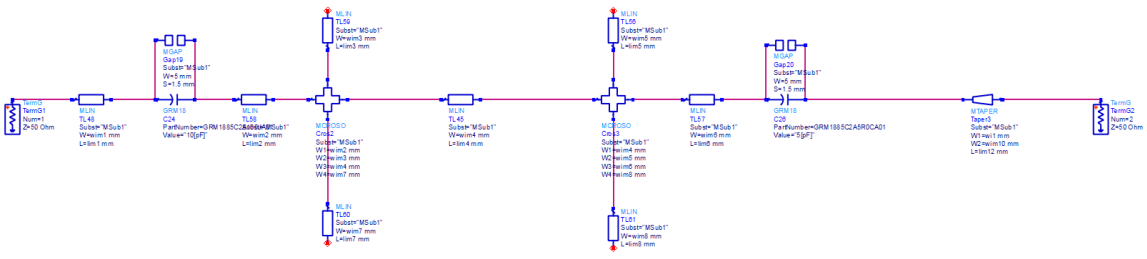


Figure 3.20: Proposed IMN

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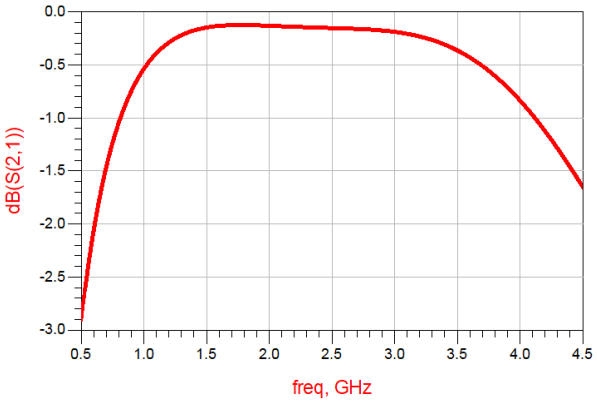
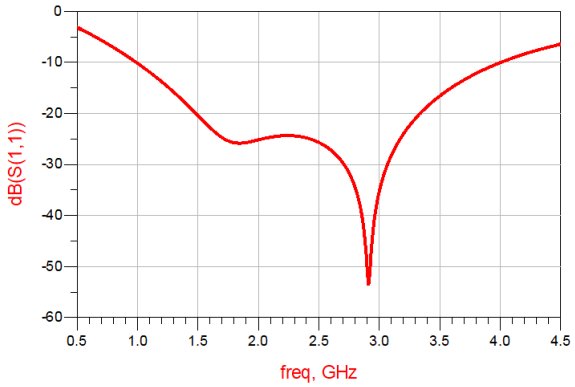
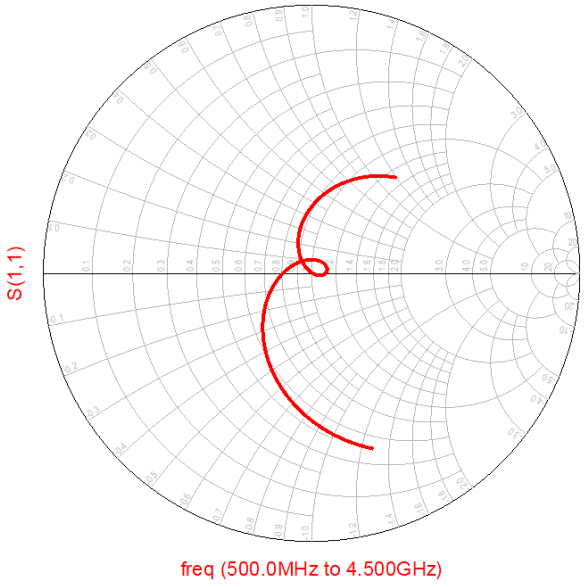


(a)



(b)



(c)

Figure 3.21: S-parameters of IMN

Having completed the design of IMN and OMN, we can finally apply them to the circuit schematic and verify whether the overall behavior of the circuit meets the requirements. Figure 3.22 shows the schematic of the entire circuit. The S-parameters and HB simulations of the circuit are shown in Figure 3.23 and Figure 3.24, respectively.

The small signal gain (S_{21}) is above 10 dB and over the bandwidth, it keeps an appropriate flatness. The input reflection (S_{11}) is roughly below -3 dB from 0.75 GHz up to 4.5 GHz. With even less reflection we could achieve higher gain and equality between G_T and G_{OP}. As for the output reflection (S_{22}), it is well below -12 dB in the entire band.

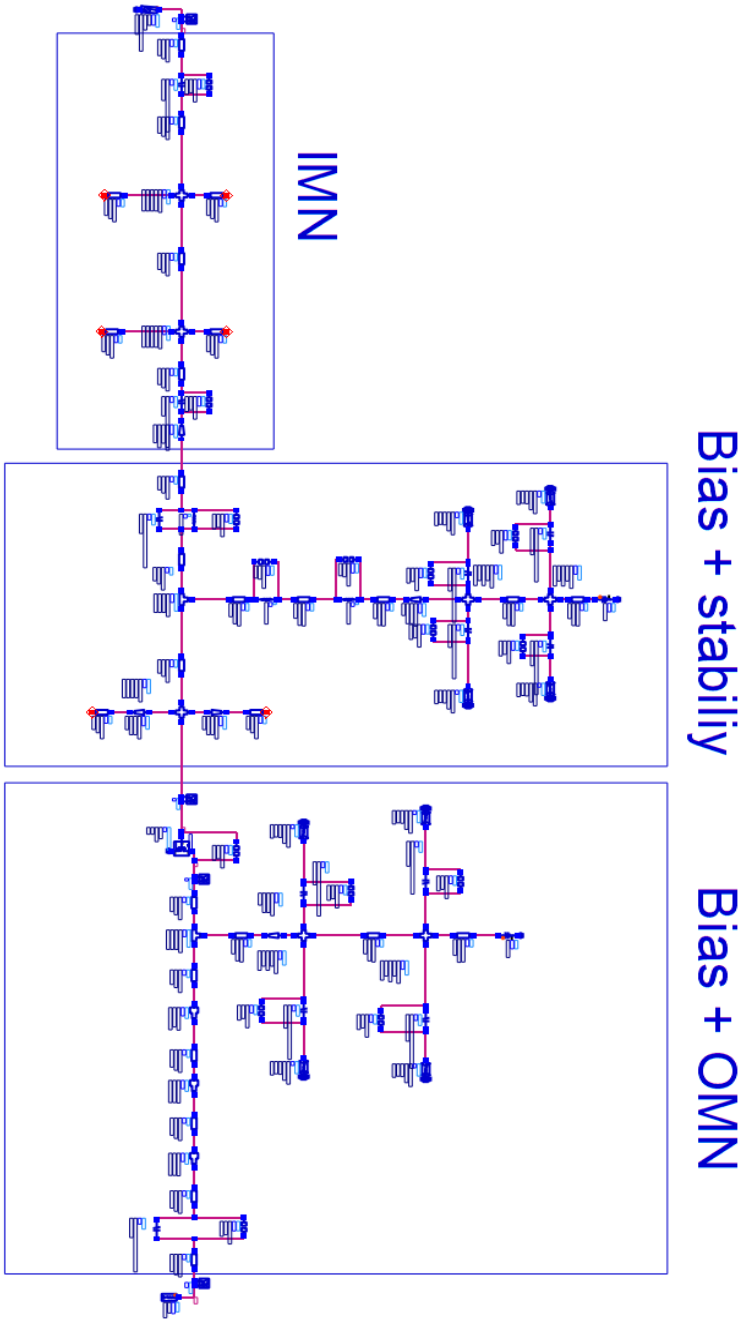


Figure 3.22: Final circuit Schematic

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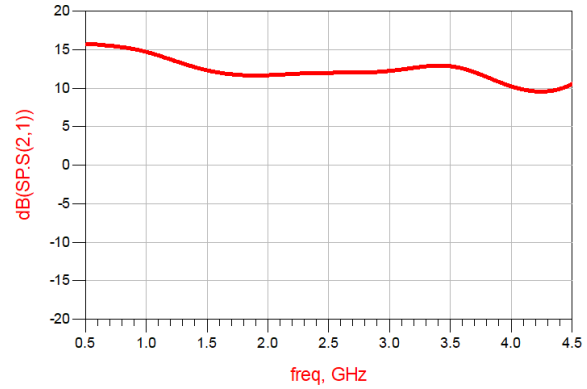
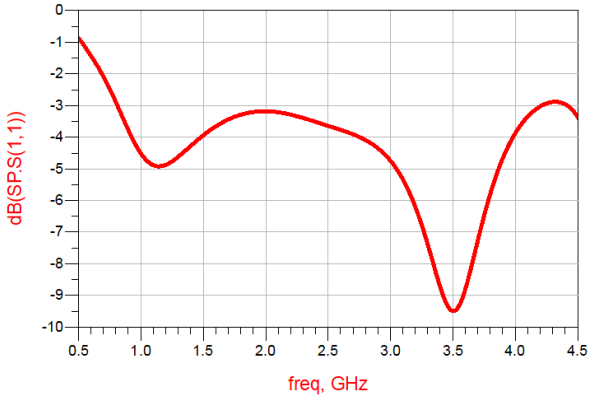


(a)



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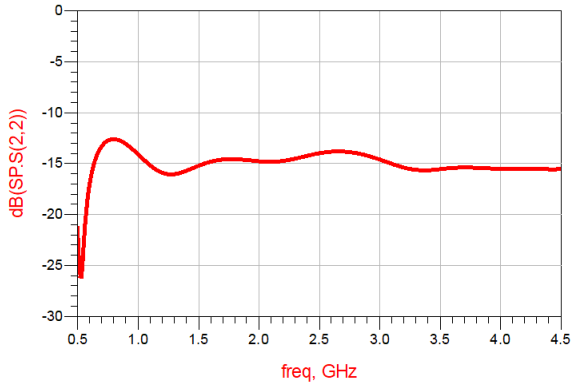

(c)

Figure 3.23: S-parameters of the entire circuit

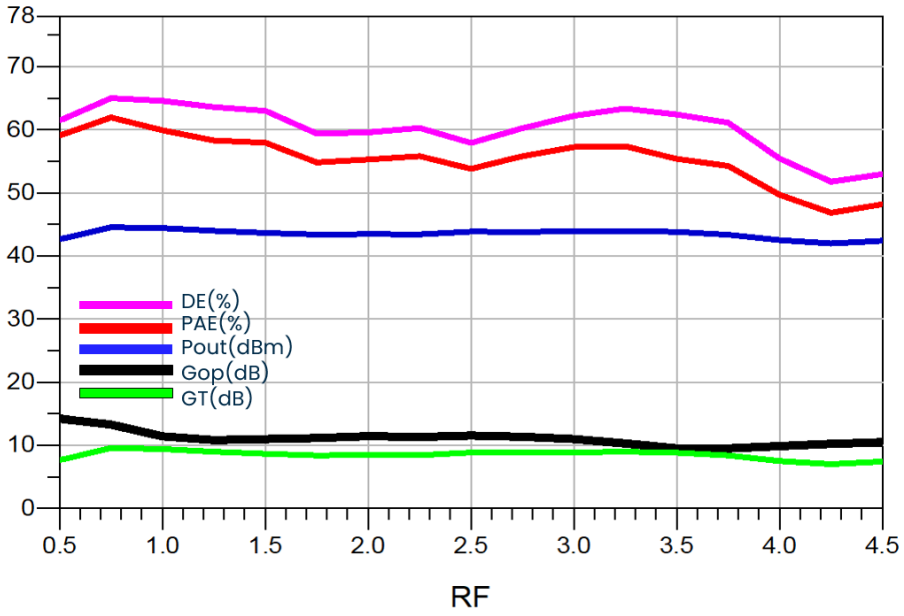

Figure 3.24: HB simulation results at 35 dbm of input power versus Frequency for circuit schematic

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The simulation results for the HB are presented with an input power of 35 dBm. However, this may not provide the most accurate depiction of the device's performance, since the gain is not exaclty the same at all frequencies. Analyzing the results at the 5 dB gain compression point is more informative, where the device reaches saturation. The results at 5 dB gain compression point are shown in Figure 3.25. These results were obtained by processing the simulation results exported from ADS with the help of the MATLAB software.

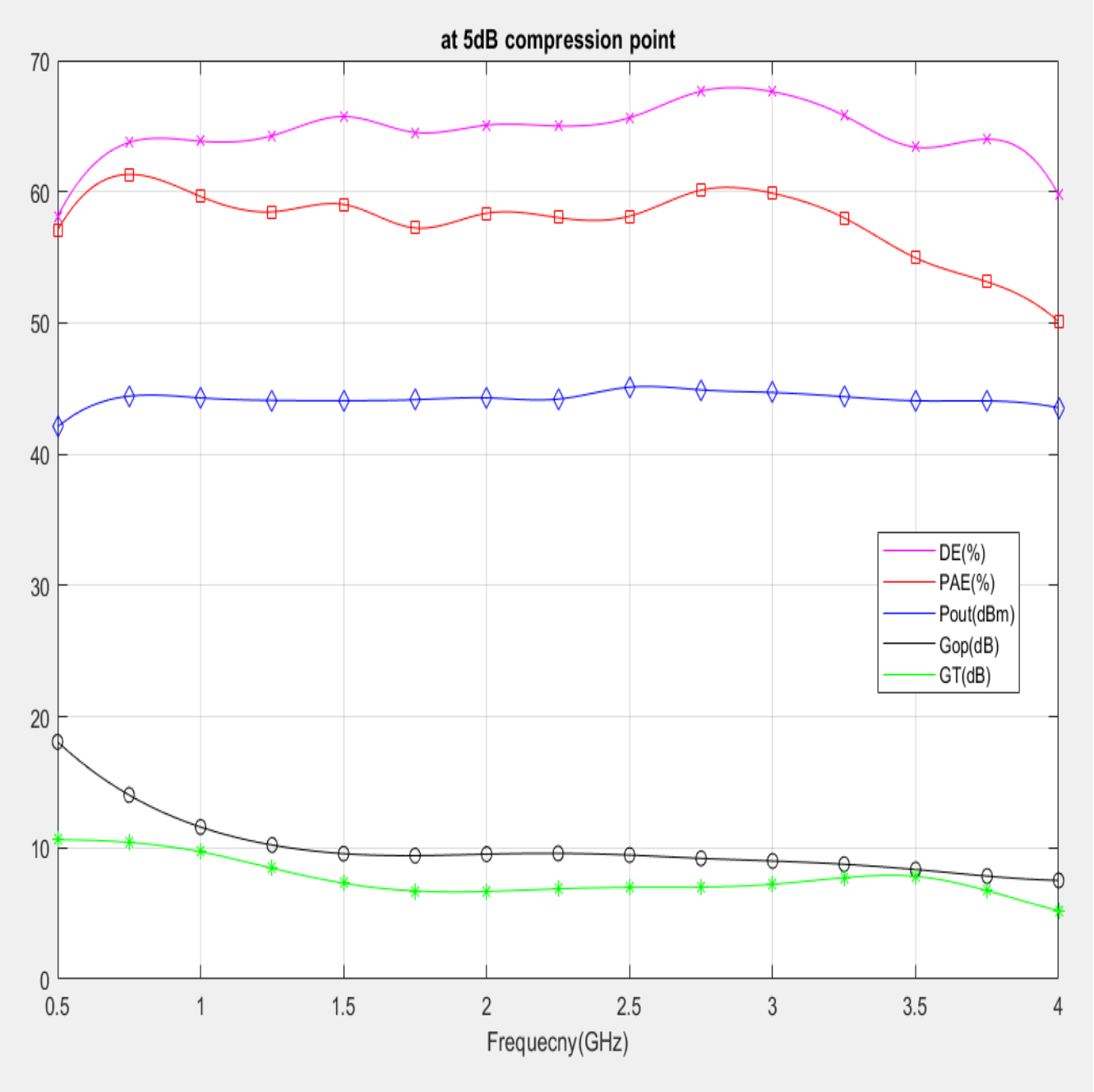

Figure 3.25: HB simulation results at 5 dB gain compression point using MATLAB

.

As shown in Figure 3.25, the results are according to the requirements. The flatness of the gain over the band is reasonable and a PAE above 50% is achieved. In Table 3.1 the device performance is introduced.

$G_{opt}(dB)$	PAE(%)	$P_{out}(dBm)$
7.52 - 18.08	50.1 - 61.32	42.08 - 45.11

Table 3.1: Circuit performance at 5 dB gain compression point

Chapter 4

Layout Implementation

In this chapter, the EM simulation and Layout planning are described. At first, a direct layout from the schematic is obtained to see how the circuit behaves. The results of the EM simulation were so far from schematic results and that's why some changes in parameters must be done to restore the same behavior as the schematic. To understand the root of the problem, the circuit is reduced into smaller parts and possible changes in parameters are adjusted. this circuit is constructed on a Roger4350B with a dielectric constant of 3.66. The microstrip line has a height of 0.76 mm and a thickness of 35 μm. The conductor is copper and its conductivity is $5.9\times10^7\frac{S}{m}$. Figure 4.1 shows a cross-section of the microstip line.

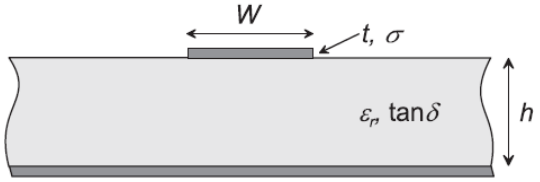

Figure 4.1: Cross-section of a microstrip line [6]

.

4.1 Input Side

The input side is composed of IMN, stability network, bias T, and gain improvement network. Figure 4.2 shows the layout of the input side. With the aid of the Co-sim tool of ADS, parametrizing the layout is possible, and by tuning of some circuit parameters, the results predicted by the circuit simulation can be obtained. The width of the bias line does not seriously affect the design because the DC path on the gate side does not need to withstand a significant amount of current. The length of the transmission line between IMN and the stability network needs to be longer to achieve better matching at the input.

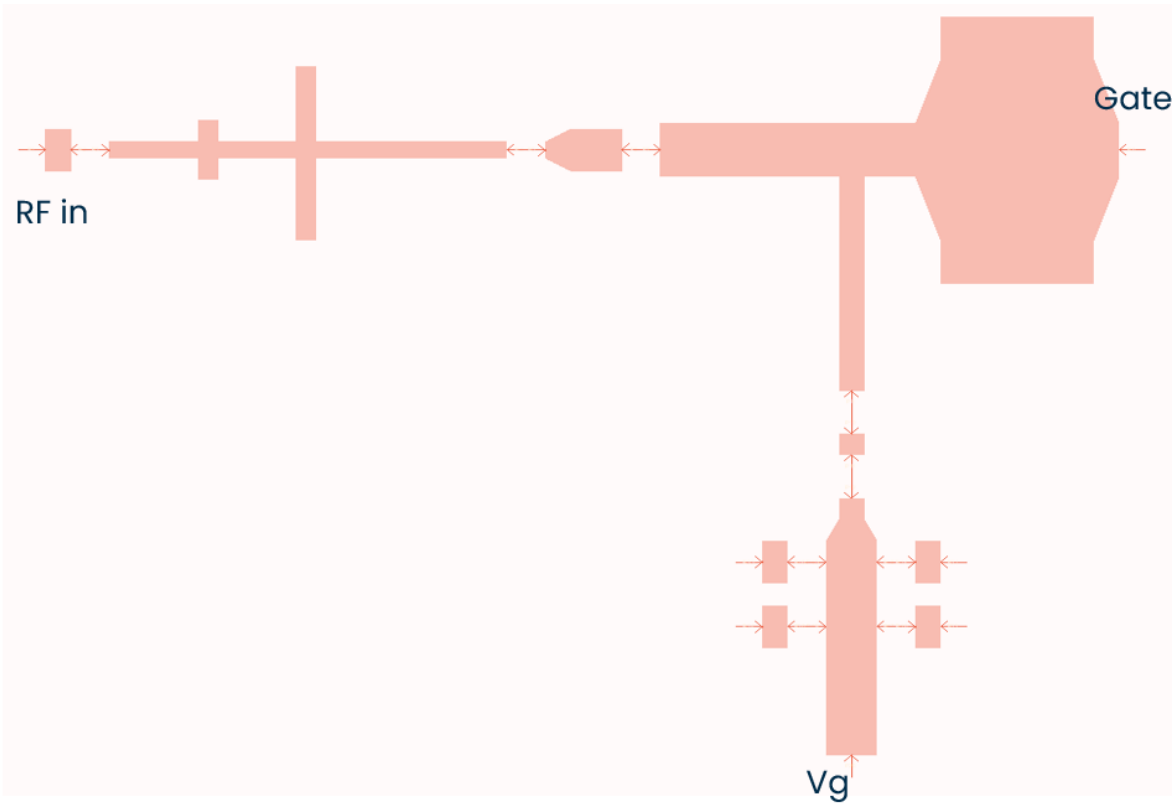

Figure 4.2: Input side layout

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4.2 Output Side

The output side is composed of the OMN and the bias network. Figure 4.3 illustrates the output side layout. The width of the bias line is designed to sustain the maximum current that the device reaches (3.5 A).

Figure 4.3: Output side layout

.

4.3 Final Layout

The entire circuit layout is shown in Figure 4.4. The Gate bias line is flipped in the same direction as the Drain line for easy wiring after manufacturing and reducing size. Two 50 Ω lines are inserted at RF in and RF out ports to fit SMA connector pins for soldering. The dimensions of the final layout are 3.3 cm × 12.4 cm.

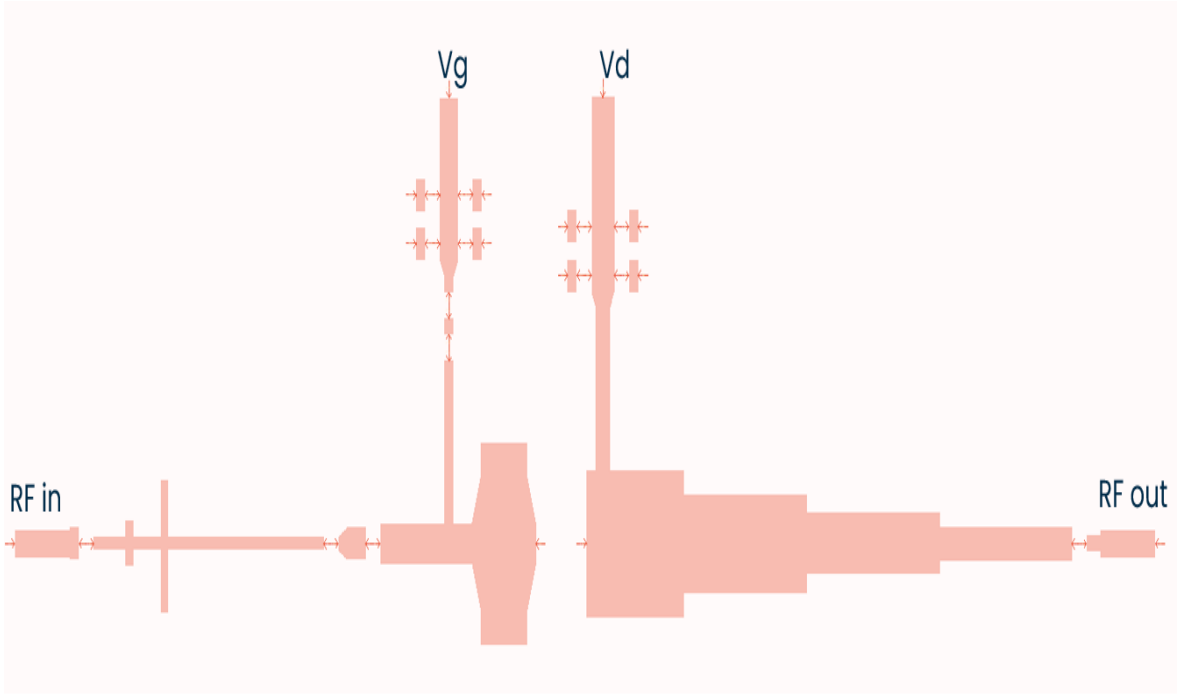

Figure 4.4: Circuit layout

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4.4 EM Simulation Results

After adjusting different parameters in the layout finally, S-parameters and HB simulation results based on the layout model shown in Figure 4.5 have been obtained. Figure 4.6 shows S-parameters of the final layout and Figure 4.7 represents HB simulation.

The S_{21} is above 10 dB except for the frequencies around 3.5 GHz. Also, the gain flatness is reduced concerning the schematic results and the reason is due to the change in the S_{11} which goes down to -9 dB at center frequency. The S_{22} is below -11 dB which is acceptable for the performance.

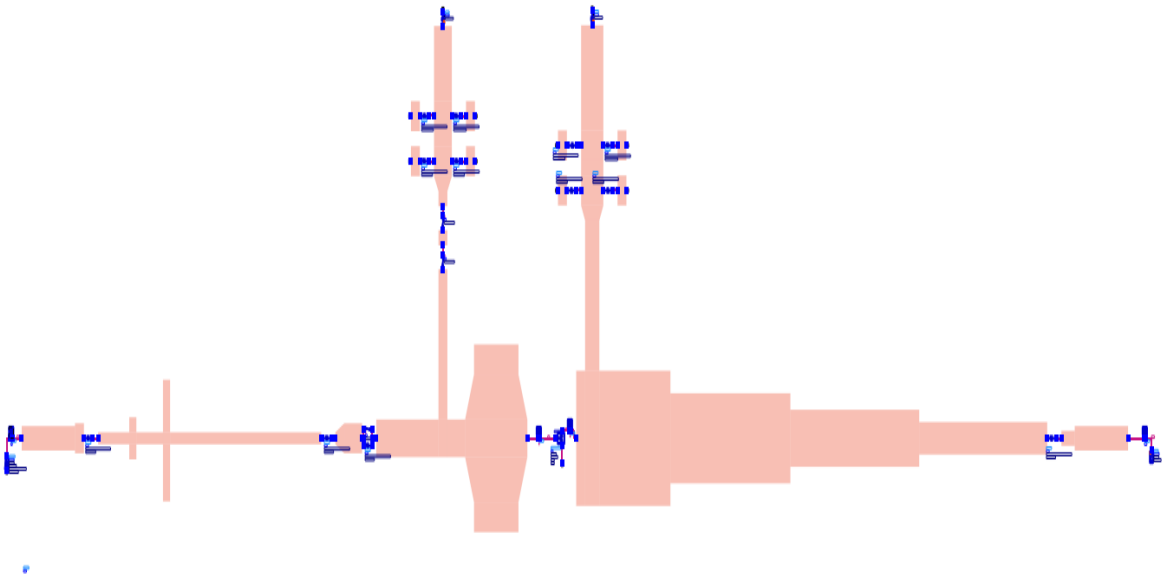

Figure 4.5: Layout symbol for simulation

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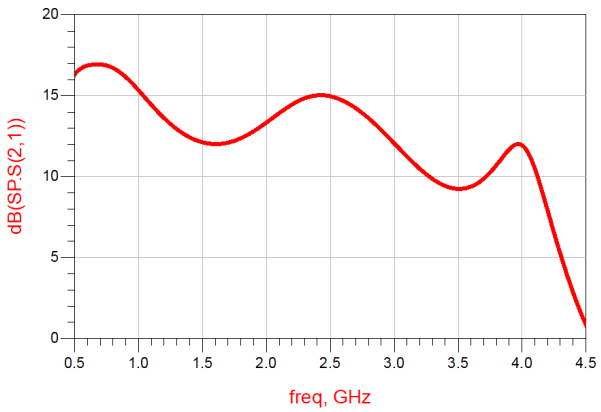
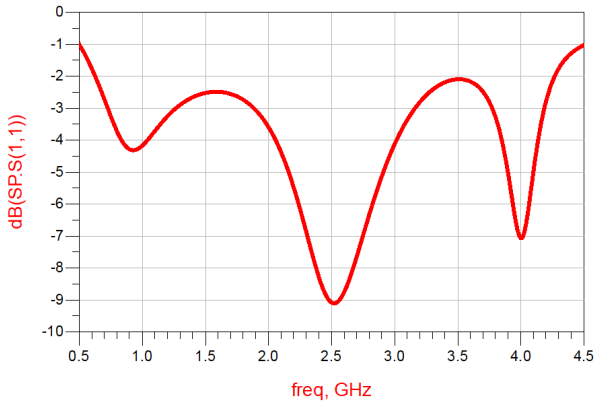
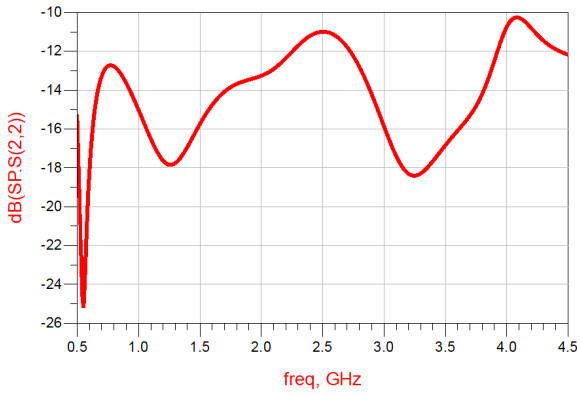
As mentioned before the more accurate way of seeing the results is to analyze the data at 5 dB gain compression point in which the device is saturated. Figure 4.8 shows the results at 5 dB gain compression point using MATLAB.



(a)



(b)



(c)

Figure 4.6: S-parameters of the circuit layout

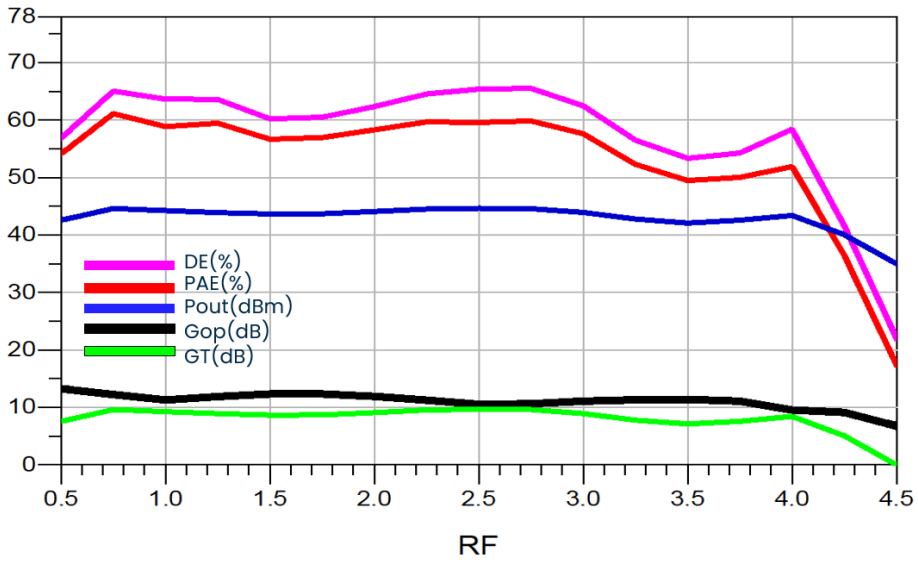


Figure 4.7: HB simulation results at 35 dBm of input power versus Frequency for circuit layout

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As evident from the graph of Figure 4.8 the results meet the specifications. The gain flatness is distorted concerning the schematic but still is acceptable. the PAE is higher than 50% in the bandwidth. The results are summarized in Table 4.1.

$G_{opt}(dB)$	PAE(%)	$P_{out}(dBm)$
7.8 - 18.1	50.54 - 60.48	42.05 - 44.67

Table 4.1: Circuit layout performance at 5 dB gain compression point

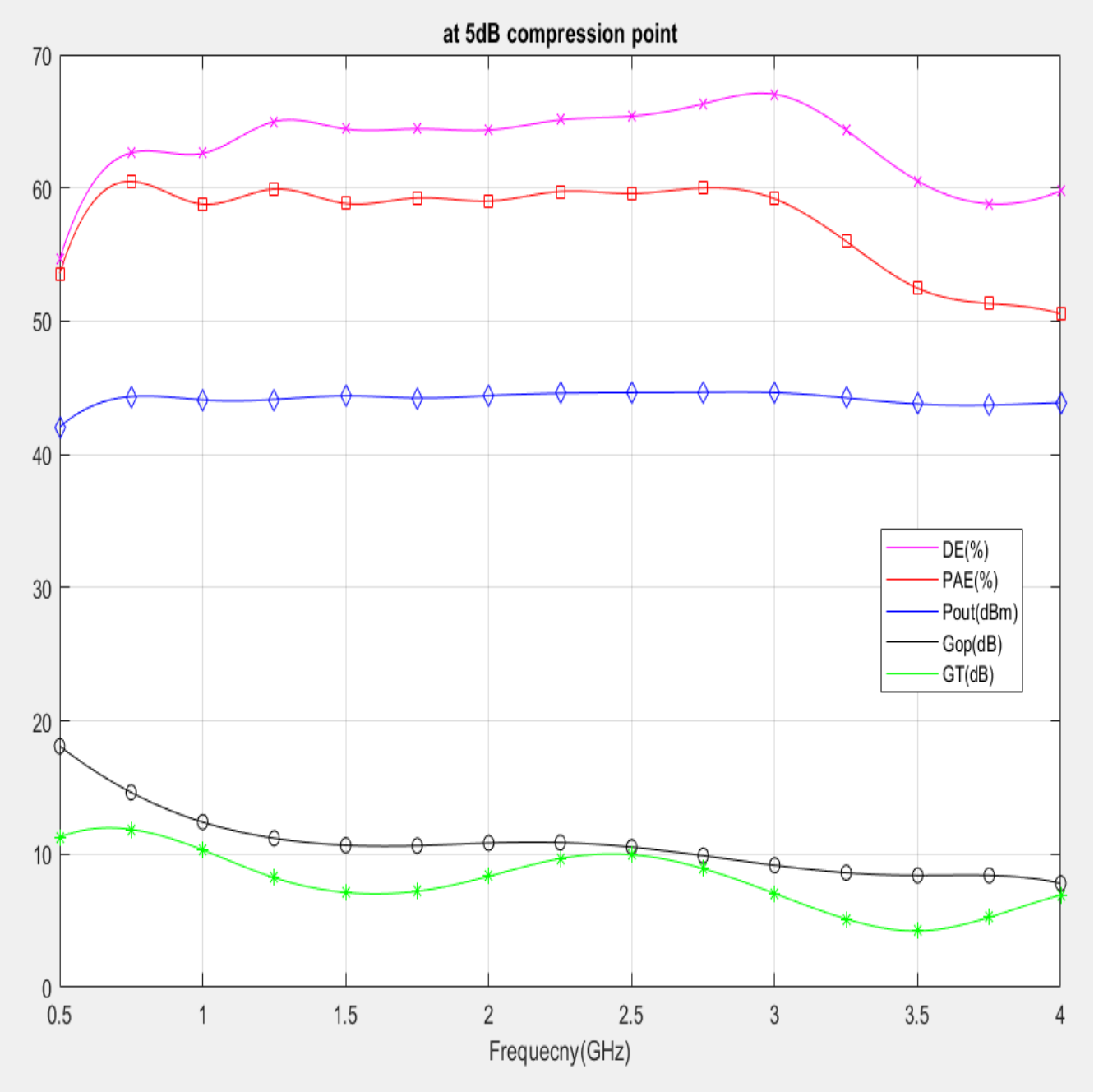

Figure 4.8: HB simulation results of the layout at 5 dB gain compression point using MATLAB

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Chapter 5

Conclusion

This thesis project presented the design and characterization of a three-octave (0.5 GHz- 4 GHz) hybrid single-stage class AB amplifier. To meet the requested specifications, optimum source, and load terminations were chosen to achieve a good trade-off between efficiency and output power. Full EM simulation on the circuit is performed and compatibility of the results with the schematic is confirmed. The proposed PA reaches a PAE of more than 50% up to 60% and maintains an output power between 16 W and 29 W. The final circuit dimension is 3.3 cm $\times$ 12.4 cm. Table **??** compares the results of this thesis work with the state-of-the-art of similar works.

The manufacturing process of the proposed circuit board is in progress and as the next stage of this thesis project, measurement and verification of the circuit performance are going to be done moreover, alternative topologies and more effective design strategies will be studied.

Ref.	BW(GHz)	BW(%)	Gain(dB)	Pout(W)	PAE(%)
[9]	0.45 - 3.4	153.2	8 - 10.5	14.1 - 26.9	54 - 70.4
[10]	0.6 - 3.8	145.5	9 - 14	10 - 15.5	46 - 75
[5]	0.8 - 3.2	120	9.5 - 13.1	47.8 - 64.5	$57 - 71^*$
[22]	0.35 - 3.55	163	8.1 - 9.6	15.5 - 26.9	$55 - 74^*$
[20]	0.4 - 2.8	150	9 - 12	7.9 - 15.8	$63 - 73.2^*$
This work	0.5 - 4	155.5	4.2 - 11.85	16 - 29.3	50.5 - 60.5

Table 5.1: Summary of Wideband PAs
* Refers to DE

Bibliography

[1] Hadi Bameri, Ahmad Hakimi, Masoud Movahhedi, and Hossein Abdollahi. A dc to 20 ghz ultra-broadband high-gain-linear distributed power amplifier with 19.5In *2010 18th Iranian Conference on Electrical Engineering*, pages 409–412, 2010.

[2] Mei-Chen Chuang, Ming-Fong Lei, and Huei Wang. A broadband medium power amplifier for millimeter-wave applications. In *2005 Asia-Pacific Microwave Conference Proceedings*, volume 3, pages 3 pp.–, 2005.

[3] Dante Del Corso, Vittorio Camarchia, Roberto Quaglia, and Paolo Bardella. *"Telecommunication Electronics"*. Artech House, 2020.

[4] Li Donglin and Yang Fei. Research on ultra-wideband high power amplifier technology. In *2022 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, pages 1–3, 2022.

[5] Mohammad Ghazizadeh and Vahid Nayyeri. "design of a 50-w power amplifier with two-octave bandwidth and high-efficiency using a systematic optimization approach". *IEEE Microwave and Wireless Components Letters*, 31(5):501–504, 2021.

[6] Marco Pirola Giovanni Ghione. *"Microwave Electronics"*. Cambridge University Press, 2018.

[7] Y. Mary Asha Latha and Karun Rawat. "design of ultra-wideband power amplifier based on extended resistive continuous class b/j mode". *IEEE Transactions on Circuits and Systems II: Express Briefs*, 69(2):419–423, 2022.

[8] Sangho Lee, Hongjong Park, Jihoon Kim, and Youngwoo Kwon. A 6–18 ghz gan phemt power amplifier using non-foster matching. In *2015 IEEE MTT-S International Microwave Symposium*, pages 1–4, 2015.

[9] Jorge Julian Moreno Rubio, Vittorio Camarchia, Roberto Quaglia, Edison Ferney Angarita Malaver, and Marco Pirola. A 0.6–3.8 ghz gan power amplifier designed through a simple strategy. *IEEE Microwave and Wireless Components Letters*, 26(6):446–448, 2016.

[10] Jorge Julian Moreno Rubio, Roberto Quaglia, Alexander Baddeley, Paul J. Tasker, and Steve C. Cripps. Design of a broadband power amplifier based on power and efficiency contour estimation. *IEEE Microwave and Wireless Components Letters*, 30(8):772–774, 2020.

[11] Abbas Nasri, Motahhareh Estebsari, Siroos Toofan, Anna Piacibello, Chiara Ramella, Vittorio Camarchia, and Marco Pirola. A 3-3.8 ghz class-j gan hemt power amplifier. In *2020 23rd International Microwave and Radar Conference (MIKON)*, pages 416–419, 2020.

[12] Franco Giannini Paolo Colantonio and Ernesto Limiti. *"High Efficiency RF and Microwave Solid State Power Amplifiers"*. John Wiley Sons Ltd, 2009.

[13] Anna Piacibello, Jorge Julian Moreno Rubio, Roberto Quaglia, and Vittorio Camarchia. Am/pm characterization of wideband power

amplifiers. In *2022 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, pages 82–85, 2022.

[14] David M. Pozar. *"Microwave Engineering"*. JohnWiley Sons, Inc., 2011.

[15] Jorge Julian Moreno Rubio, Roberto Quaglia, Anna Piacibello, Vittorio Camarchia, Paul J. Tasker, and Steve Cripps. 3–20-ghz gan mmic power amplifier design through a cout compensation strategy. *IEEE Microwave and Wireless Components Letters*, 31(5):469–472, 2021.

[16] Jaewoo Sim, Jaeyeon Lim, Myoungkyu Park, Wenwoo Kang, and Bak-IL Mah. Analysis and design of wide-band power amplifier using gan. In *2009 Asia Pacific Microwave Conference*, pages 2352–2355, 2009.

[17] H. Sledzik, R. Reber, B. Bunz, P. Schuh, M. Oppermann, M. Mußer, M. Seelmann-Eggebert, and R. Quay. Gan based power amplifiers for broadband applications from 2 ghz to 6 ghz. In *The 40th European Microwave Conference*, pages 1658–1661, 2010.

[18] Heather Song and Tanghid Rashid. A high-ip3 harmonic tuned wideband 40 dbm rf power amplifier for 5g applications. In *2023 IEEE Wireless and Microwave Technology Conference (WAMICON)*, pages 5–8, 2023.

[19] Wolfspeed. *25 W, RF Power GaN HEMT , CGH40025*, 12 2022. Rev. 4.2.

[20] Xuefei Xuan, Zhiqun Cheng, Zhiwei Zhang, Tinwei Gong, Guohua Liu, and Chao Le. Design of an extended continuous-mode class-gf power amplifier with multioctave bandwidth. *IEEE Microwave and Wireless Technology Letters*, 33(9):1329–1332, 2023.

[21] Xuefei Xuan, Zhiqun Cheng, Zhiwei Zhang, Tinwei Gong, Guohua Liu, and Chao Le. Design of an extended continuous-mode class-gf power amplifier with multioctave bandwidth. *IEEE Microwave and Wireless Technology Letters*, 33(9):1329–1332, 2023.

[22] Han Zhou, Jose-Ramon Perez-Cisneros, Björn Langborn, Thomas Eriksson, and Christian Fager. Design of a compact gan power amplifier with high efficiency and beyond decade bandwidth. *IEEE Microwave and Wireless Components Letters*, 32(12):1439–1442, 2022.