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Fabrication of CMOS-compatible Microelectrodes for Brain Stimulation and Recording in the Aid of Visual Impairment

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Summary

Cortical visual prosthesis are nowadays investigated as a promising solution for visually impaired people. Precise electrical stimulation of the visual cortex by penetrating microelectrodes demonstrated phosphene activation at specific points on the visual field, facilitating a nuanced perception of the surroundings in a grid-like manner.

The Smart Micro Neural Dot project aims at a wireless, miniaturised and large-scale cortical visual prosthesis relying on thousands of free-standing CMOS microstimulators. Penetrating microelectrodes directly stimulate the visual cortex in a one-to-one correlation with the perceived pixel in the blind visual field. The integration of such penetrating microelectrodes with CMOS implants represents a challenge in terms of assembly, reliability, repeatability, and scalability.

The aim of this thesis is developing and optimizing a post-CMOS fabrication process, enabling the integration of penetrating microelectrodes within miniaturized CMOS implants, and validating their robustness by incorporating them into phantoms that simulate brain tissue.

The system is manufactured at the Center of Micro Nano Technology (CMi) of the Ecole Polytechnique Fédérale de Lausanne (EPFL) and it is composed by a miniaturized CMOS chip of 250μm x 250μm and two shanks, strategically positioned on opposite sides of the chip. The shanks, constructed from aluminum—a material renowned for its high conductivity, compatibility with CMOS technology, and inherent flexibility, are subjected to a subsequent insulation involving SiO_2. Aluminum remains deliberately exposed exclusively at specified pad locations, facilitating potential wire connections, and at the tip of the shanks, thereby enabling precise intracortical microstimulation. Another design for simultaneous stimulation and recording is also proposed. This innovative approach involves the addition of a second metal layer, featuring four recording sites precisely aligned with the tip of each shank. The metallic layer then is insulated utilizing SiO_2, with intentional metal exposure extending to the recording sites, thereby enabling a multisite recording of the neuronal activity. Subsequent to the front-side fabrication process, a deliberate reduction in the overall thickness of the device is achieved through a sequence of deep silicon etching procedures. These procedures are designed to

comprehensively eliminate the silicon in the region of the shank adjacent to the chip, thereby allowing the 90-degree bending of the two shanks.

A systematic analysis of diverse design possibilities for the back sides is undertaken, carefully evaluating the challenges during the electrode insertion into an agarose phantom.

The resulting CMOS compatible fabrication process allows both neural recording and stimulation and represents a significant advancement in the field, offering enhanced reliability and performance for their application in miniaturized implant systems.

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Acronyms

RGC
Retinal Ganglion Cell

CNS
Central Nervous System

AV-DONE
Artificial Vision by Direct Optic Nerve Electrode

LGN
ateral geniculate nucleus

DBS
Deep Brain Stimulation

GSA
Geometric surface area

UIEA
Utah Intracortical Electrode Array

AMM
Arrays built with metal microelectrodes

PEA
Planar Electrode Arrays

SMND
Smart Micro Neural Dot

RCA

Radio Corporation of America

FFR

Fill Rinse bath

TT

Trickle Tank

SRD

Spin Rinse & Dry

PR

Photo resist

PECVD

Plasma Enhanced Chemical Vapor Deposition

EPD

End Point Detection

OES

Optical Emission Spectrometer

ICP

Inductively Coupled Plasma

RIE

Reactive Ion Etching

DRIE

Deep Reactive Ion Etching

VSI

Vertical Shift Interference

Chapter 1

Introduction

The neurological system stands out as the least comprehended among the various systems within the human body; it presents formidable challenges in the realm of curative endeavors, with the visual system being no exception [1].

Numerous attempts have been undertaken to develop assistive technologies for visually impaired people that involve translating visual images into auditory or tactile sensations. Nevertheless, the constrained efficacy of these conversion devices and the challenges associated with instructing users to interpret the converted signals, have significantly curtailed the scope of practical applications. These issues may be resolved by producing artificial vision through the visual cortex's interface with a television camera or other comparable sensor [2]. This idea first attracted a lot of attention due to the groundbreaking work of Brindley and Lewin [3].

The primary role of the ocular organ lies in the capture and precise convergence of incident light upon a specialized layer of sensory receptor cells situated along the posterior aspect of the eye. The globe of the eye is intricately linked to a sophisticated network of muscular structures, facilitating its dynamic response to environmental stimuli. Furthermore, the ocular lens, responsible for light refraction, maintains connections with muscular elements capable of modulating the lens's morphology and, correspondingly, its focal length. In the posterior region of the eye, specialized receptor cells undergo the transformation of incoming light energy into a neural signal which undergoes modification within the retinal structure, with an emphasis on detecting variations and interruptions in ambient illumination. Subsequently, the processed signal proceeds to the brain via the optic nerve [4].

Given the dependence of neurons on neural activity for survival, injury to one portion of the central nervous system (CNS) causes degeneration in distant regions, both anterograde and retrograde. In fact, the potential of visual prostheses to restore visual perception faces constraints due to the ongoing anterograde and retrograde degeneration processes taking place within the visual pathway. Electrical devices that can be used to help restore visual function fall into three major categories:

- Visual prostheses, which restore function by avoiding damaged sections and activating downstream parts of the visual system directly;
- Electric field stimulation, that seeks to restore function by encouraging injured neurons to heal themselves or directing the development and integration of transplanted neurons;
- Neuromodulation, which is being researched as a method to resynchronize neural activity. [5]

The scope of this thesis will encompass a detailed examination of visual prostheses, elucidating their pivotal role in visual rehabilitation.

1.1 Visual Prostheses

The first visual prostheses were made to communicate with the brain's visual cortex, and then, starting in the late 1980s, attempts were made to create retinal prosthetics. The first commercially available visual prosthesis was the Argus II system, followed by a sub-retinal device, the alpha AMS. Both devices, however, are no longer manufactured [6].

Visual prostheses typically use a photocell integrated into an external wearable device to capture visual input. This input is usually processed by specialized software and then sent to a lower part of the visual pathway to generate electrically induced visual sensations called phosphenes. Phosphenes with different levels of intensity are triggered at various locations on the patients' retinotopic map, enabling them to perceive their surroundings in a grid-like manner. Nonetheless, patients need to make sense of this data themselves to recognize the objects or patterns they are observing. Consequently, after receiving the implant, patients need extensive training to be proficient in interpreting phosphenes.

Visual prostheses can be categorized into the following types: retinal implants (1.1a), optic nerve implants (1.1b), thalamic implants and cortical implants (1.1c).

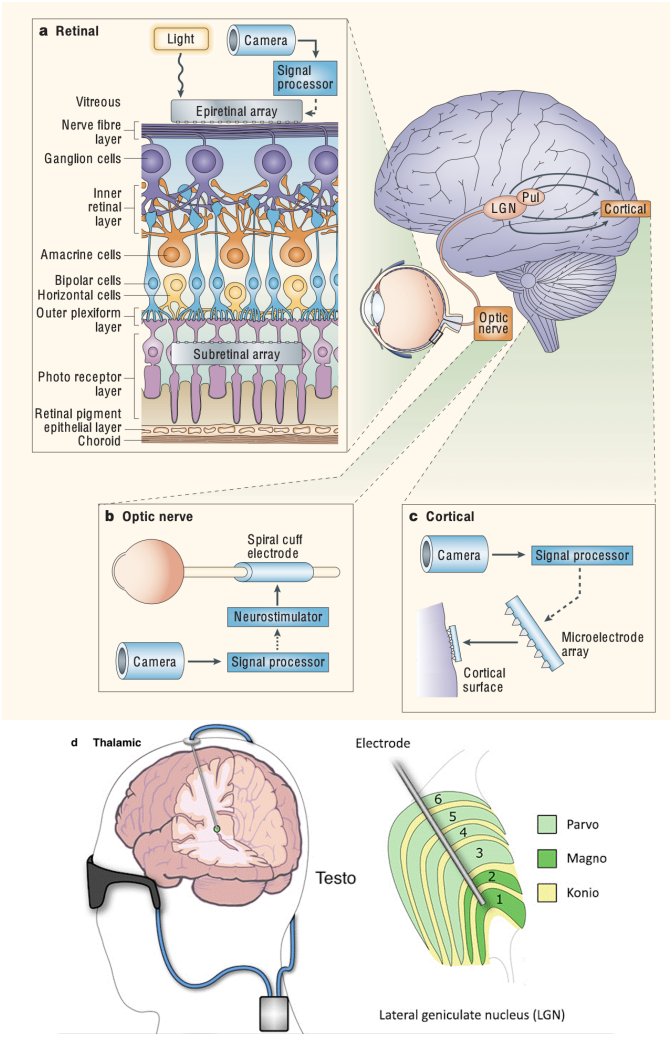


Figure 1.1: Overview of a) Retinal, b) Optic nerve, c) Cortical and d) Thalamic implants. Reprinted from [7] and [8]

1.1.1 Retinal Implants

There are three primary methods to connect electrode arrays to the retina. In the epiretinal approach, the array sits at the vitreous humor-neuroretina border, with electrodes above retinal ganglion cells. Subretinal implants instead, place the array where photoreceptors are lost, meanwhile suprachoroidal implants position the array between the sclera and choroid.

Each method faces a common challenge: supplying power and control signals to the electrode arrays, limiting the number of serial or parallel-connected electrodes and impacting spatial resolution. While attempts to use ambient light for power

have been made, they have yet to succeed in clinical trials due to insufficient intensity, requiring complex surgical procedures for cable and inductive coil implantation. Furthermore, waterproof, and biocompatible encapsulation for intraocular electronic circuits is essential, as is managing heat production from these circuits [9].

The previous mentioned Argus-II Retinal Prosthesis is a visual implant that directly interacts with the retinal ganglion cells (RGCs) of the inner retina. This approach eliminates the requirement for input from photoreceptors, particularly in neurodegenerative conditions like retinitis pigmentosa and age-related macular degeneration.

Following implantation, individuals with retinitis pigmentosa, who have experienced significant vision loss, exhibit enhanced object localization abilities. An alternative approach to address photoreceptor degeneration entails the use of the Prima System implant, which is a subretinally implanted wireless photovoltaic microchip array. Research involving non-human primate models (Macaca fascicularis) has revealed that the Prima System implant induces retinal electrical responses, as evidenced by electroretinograms (ERGs). However, these animals did not show any improvements in visual function. Nevertheless, promising outcomes have been reported in clinical trials for the Prima implant among age-related macular degeneration patients. All five patients who successfully received the implant were able to perceive visual patterns in white and yellow.

In contrast to the Argus-II implant, the Prima System implant incorporates photosensitive technology directly within the chip, eliminating the need for an external camera. Furthermore, the surgical placement of subretinal prostheses presents increased complexity when compared to epiretinal devices, and it comes with the potential risk of scleral erosion [6].

1.1.2 Optic Nerve Implants

In the decade preceding the notable enhancements in epiretinal implants, such as the Argus-II, and subretinal implants, exemplified by the Prima System, substantial focus had been directed toward the advancement of technologies designed for establishing connections with visual centers downstream.

These approaches have opened up exciting possibilities for expanding the range of clinical applications of such devices. Take, for instance, the case of direct optic nerve stimulation, which has been explored through a procedure known as Artificial Vision by Direct Optic Nerve Electrode (AV-DONE). This method involves the insertion of three wire electrodes into the optic disc, and it has demonstrated the successful generation of phosphenes in patients with advanced retinitis pigmentosa, all while keeping post-surgical complications at a minimum.

In a separate study, researchers utilized a four-contact spiral cuff wrapped around the optic nerve. This approach enabled patients to safely perceive phosphenes

and, with dedicated training, even recognize specific objects. Impressively, the recognition accuracy rate reached 63%, with an average processing time of just 60 seconds.

However, it's important to note that optic nerve devices, while capable of inducing phosphenes, tend to exhibit lower accuracy rates and longer processing times when compared to their retinal and cortical counterparts. This variance may offer insights into why further development in this direction has not been as extensively pursued [5].

1.1.3 Thalamic Implants

Exploring new frontiers, researchers have delved into the possibilities of directly stimulating the lateral geniculate nucleus (LGN) with visual prostheses. The LGN unique anatomical layout, characterized by distinct visual subdivisions, a focus on the fovea, and separate parvocellular, magnocellular, and koniocellular streams, preserves center-surround retinal fields. This configuration holds the promise of restoring not only higher visual acuity but also enhancing shape and motion perception when compared to retinal or optic nerve-based visual prostheses.

Experiments involved implanting multielectrode probes into the LGN of Wistar rats, resulting in the induction of phosphenes. Remarkably, these animals seemed capable of perceiving a broader spectrum of signals compared to those with retinal implants. This suggests that the LGN possesses the capacity to "reinterpret" external input and generate responses more akin to natural visual perceptions. The LGN direct link to the primary visual cortex is pivotal in this process. Electrical stimulation of the LGN directly induces the activation of neurons in V1, the primary visual cortex situated in the occipital lobe. This, in turn, enhances the receptive fields of the visual cortex, boosting its responsiveness to various stimuli [5].

Deep Brain Stimulation (DBS) within the thalamus has demonstrated effectiveness, although not without potential risks, particularly in cases of bilateral implantation where significant adverse effects have been documented. These risks encompass complications arising from the surgical procedure, modulation parameters, and potential side effects linked to thalamic implants [10].

Conversely, cortical implants, with a specific focus on cortical visual prostheses, present distinct advantages compared to thalamic implants. Cortical visual prostheses play a pivotal role for individuals with entirely compromised retinas, optic nerves, or lateral geniculate bodies, offering a viable solution for blindness stemming from diverse conditions.

1.1.4 Cortical implants

The key advantage of cortical implants in visual prosthetics lies in their capacity to activate neurons beyond impaired areas along the visual pathways, rendering them beneficial for individuals with incurable blindness and diminished visual acuity. Extensive work has gone into the development of visual prostheses designed to directly stimulate the primary visual cortex situated in the occipital lobe. These endeavors draw inspiration from experiments conducted during the 1960s, which demonstrated that electrical stimulation of the occipital lobe could provoke phosphenes—visual sensations. In comparison to alternative visual prosthesis approaches, cortical prostheses hold a distinct advantage in their potential to offer restored visual perception to a wider range of medical conditions. Cortical implants come in different forms, including the Intracortical Visual Prosthesis Project (IVCP, United States) that employs a floating microelectrode array, equipped with 16 microelectrodes, strategically positioned on the dorsolateral surface of the human occipital lobe. Additionally, the Cortical Visual Neuroprosthesis for the Blind (CORTIVIS, Spain), situated on the lateral occipital cortex, utilizes the FDA-approved Utah electrode array.

Studies conducted on patients with these implants have yielded promising results. These individuals have demonstrated the ability to perceive various phosphenes that vary in size and color, showcasing the potential of cortical implants in restoring visual perception [5].

Current research and development efforts are dedicated to addressing the main obstacles associated with cortical implants such as:

- Large-scale Cortical Interfaces:
  The current state of large-scale cortical interfaces presents obstacles for dynamic implants due to the intricacy of effectively integrating them [11].

- Biocompatibility Investigations:
  Elements such as damage induced by micromotion and implant density impact biocompatibility, requiring meticulous consideration in the design of neural implants [12].

- Microscopic Tissue Formation:
  Brain implants may induce the formation of microscopic cerebral tissue, underscoring the requirement for solutions to diminish this problem, leading to improved long-term results.

- Stability and Material Challenges:
  Embeddable neural prostheses face issues associated with inadequate material properties, continuous expansion during water absorption, and overall instability that require resolution to attain optimal performance [13].

1.2 Smart Micro Neural Dot Project

The Smart Micro Neural Dot project aims to advance the field of vision restoration without depending on externally powered implantable units or wired connections and using electrodes that integrate CMOS technology [14][15][16][17].

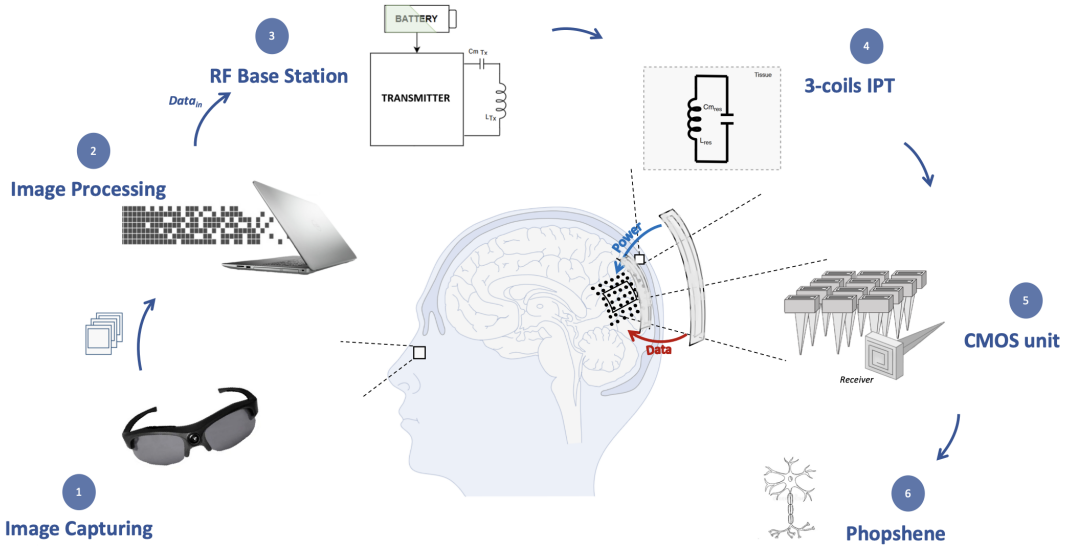


Figure 1.2: Schematic representation of the concerned visual prosthesis.

The envisioned visual prosthetic entails an external camera for capturing black-and-white images of the surrounding environment. Subsequently, the captured image is transmitted to an external Video Processing Unit (VPU), which transforms the grayscale floating-point pixel values into a binary format. The information associated with the image is then wirelessly transmitted from an external transmitter to an array of free-floating penetrating electrodes through an inductive coil, along with the required power supply for the implants. In this phase of the project, our focus will be on the clean room fabrication of microelectrodes that will enable direct stimulation of the visual cortex, bypassing any damaged sections of the visual system and inducing phosphenes generation [18]. Each microelectrode, one for each pixel of the image that will be generated, will be then furnished with its integrated CMOS circuitry. In the realm of semiconductor and nano/micro-technology, recent progress has facilitated the downsizing of these devices to sub-millimetric dimensions but the weak link in the system lies in the junction between the CMOS and the corresponding microelectrode. Nowadays, microelectrodes are commonly affixed to CMOS pads manually. This approach presents various drawbacks, including diminished reliability and repeatability, restricted scalability

for miniaturized implants, and reliance on conductive silver paste with suboptimal electrical properties. To tackle this challenge, this thesis proposes an alternative method, hinging on the creation of a pioneering CMOS-compatible microfabrication approach for electrodes directly on the CMOS chip during a subsequent processing stage. But, first and foremost, to accomplish this objective, it is imperative to take into account various factors, such as:

- Functional stability;
- Long-term stability;
- Mechanical integrity;
- Risk reduction;
- Biocompatibility.

A potential solution to enhance biocompatibility involves minimizing the contact of materials with biological tissue, thus advocating for the miniaturization of implants and leveraging wireless communications.

1.2.1 Thesis Objectives

The objective of this thesis is to develop probes for brain stimulation and recording. Following a careful bending operation, these probes will be implanted in the visual cortex, where stimulation will occur in a one-to-one correlation with the pixels perceived in the blind visual field. The need to manage limited space while ensuring proper functionality and defining an adequate interface between various MEMS components and CMOS chips exemplifies the significant challenge associated with integrating miniaturized probes with CMOS chips.

Currently, microelectrodes are manually attached to CMOS pads, a process with disadvantages primarily related to manual imprecision leading to issues of reliability, repeatability, and low scalability toward miniaturized implants. The thesis critically engages with challenges concerning material limitations to ensure compatibility with CMOS technology, as well as methods for probe release following fabrication on the wafer. In this context, various thickness values and designs are systematically evaluated to ensure both proper probe release and adequate bending, mitigating the risks of breakage or deformation. A significant challenge pertains to the bending methodology, which must preserve the probe's integrity and achieve a precise 90-degree bend of the shank. Deliberations on stress application points for bending the shanks inform the definition of the bending system. The correct bending and robustness of the probe are meticulously assessed following implantation in an agarose gel designed to simulate brain tissue.

Thesis Outline

- **Chapter 2: Electrodes for neural interfaces - State-of-the-art.**
  In this chapter, an in-depth exploration of the current state-of-the-art in neural probe technologies is undertaken. Various probes employed for neural stimulation and recording are comprehensively examined, drawing meaningful comparisons among the available options. Through a meticulous review, this chapter aims to elucidate the strengths and limitations inherent in diverse neural probe technologies. By providing a detailed comparative analysis, the groundwork is laid for subsequent chapters, contributing to a comprehensive understanding of the existing landscape in neural research.

- **Chapter 3: Microelectrodes Fabrication.**
  In this chapter, a thorough exploration of the stepwise microfabrication processes for crafting 2D neural probes from a silicon wafer is provided. Each microfabrication step is examined, emphasizing the technological nuances inherent in the manufacturing process. This chapter establishes a theoretical framework, offering insightful comprehension of the complexities involved in microfabrication techniques. Within this chapter, is provided also an explication regarding the methodology employed for bending the probes, delineating both the design specifications of the fabricated device and the procedural intricacies involved in the 3D printing process.

- **Chapter 4: Results.**
  The fifth chapter serves as a culmination of the preceding chapters, reporting both intermediate and final results pertaining to the fabrication, bending, and subsequent validation of the implanted probes. The outcomes of the microfabrication processes, bending methodology, and the validation of implants in an agarose gel, simulating brain tissue, are thoroughly discussed. Through a comprehensive presentation of results, this chapter offers valuable insights into the success and challenges encountered during the entire process, contributing to the overall understanding of the study's outcomes.

- **Chapter 5: Conclusions**
  This concluding chapter encapsulates the key findings and proposals presented in the thesis. It highlights the introduction of a post-CMOS fabrication method for cortical visual prosthesis probes, addressing challenges related to the manual integration of the CMOS chip onto implantable devices. Overall, the chapter serves as a succinct summary, providing a glimpse into the achievements of the proposed fabrication method, future directions for research, and areas requiring refinement for the development of effective cortical visual prosthesis probes.

Chapter 2

Electrodes for neural interfaces: State-of-the-art

2.1 Probes for neural stimulation

2.1.1 Electrical stimulation working principle

Electrical stimulation acts as a trigger for functional responses by inducing the depolarization of excitable cell membranes. This depolarization relies on the orchestrated exchange of ionic currents between electrodes, with at least one electrode strategically positioned in immediate proximity to the target tissue. In the context of neural applications, the exploitation of electrical stimulation takes the form of a series of biphasic current pulses, each carefully tuned with cathodal and anodal phases. These phases are meticulously calibrated in terms of current amplitudes and durations to ensure an overall neutral charge (charge-balance).

The cathodal phase, characterized by a reduction effect at the stimulation electrode, witnesses electrons flowing from the electrode to the tissue. In contrast, the anodal phase initiates an oxidizing effect, with electron flow directed in the opposite direction. The charge delivered is succinctly expressed as the time integral of the current, represented by $ic \cdot tc$, denoting the magnitude (ic) and pulse width (tc) of the cathodal constant-current pulse. Achieving charge-balance, particularly with intramuscular and peripheral nervous system electrodes, may involve the incorporation of a capacitor discharge circuit, resulting in a monophasic, capacitor-coupled waveform.

Modifications to biphasic current waveforms are diverse and open to exploration. From a physiological standpoint, the conventional preference is to initiate with the cathodal phase. However, there's merit in investigating anodal-first pulsing for potentially more efficient activation of specific neural elements. While historical

emphasis has been on aligning charges in the cathodal and anodal phases, the practical realization of this ideal has proven to be variable.

2.1.2 Charge Injection Mechanisms: Capacitive and Faradaic Processes

The intricate process of the transition from electron flow within the electrode to ion flow within the tissue is governed by distinct reactions classified into two principal categories: capacitive and faradaic.

Within the domain of capacitive reactions, the focal point is the dynamic interplay of charging and discharging within the electrode-electrolyte double layer. Electrostatic capacitive charging manifests with the distinctive separation of ions and electrons within the double layer, harmonized with the alignment of electrolyte dipoles. Conversely, electrolytic capacitive charging entails the storage of charge across a slender, high-dielectric-constant oxide positioned at the electrode-electrolyte interface.

Faradaic reactions, in stark contrast, entail the oxidation and reduction of confined species on the electrode surface. This intricate process mandates the transfer of electrons across the electrode-electrolyte interface, contingent upon specific species undergoing a consequential shift in valence, be it oxidation or reduction.

2.1.3 Electrical stimulation side effects

The primary goal of charge-balance remains centered on maintaining the electrode potential within a range that forestalls irreversible reduction and oxidation reactions, thus safeguarding against electrode degradation, tissue harm, or restrictions on charge deliverability during stimulation pulses.

Even within the domain of charge-balanced stimulus pulse pairs, the risk of electrode polarization looms during pulse delivery. This polarization could potentially lead to irreversibility and consequential damage to either the tissue or the electrode. Consequently, beyond achieving charge balance, it becomes imperative for stimulus waveforms to comply with limits on current and charge densities. This compliance ensures charge injection occurs through reversible processes, mitigating the risk of undesirable rates of irreversible cathodic or anodic charge injection. The practical efficacy of a neural prosthesis reliant on electrical stimulation hinges on its consistent capacity to deliver therapeutic stimulation at safe levels over prolonged durations. In diverse applications for both animals and humans, electrical thresholds have been established.

2.1.4 Electrode Classification: Distinctions between Micro and Macro Electrodes

In a broad classification, electrodes utilized in neural stimulation can be grouped into two primary categories. Macroelectrodes, situated on the surface of the target tissue, typically display high charge/phase thresholds and low charge density thresholds. These electrodes boast a geometric surface area (GSA) surpassing approximately 100,000 μm^2. (0.001 cm^2).
Conversely, microelectrodes exhibit an inverse behavior, featuring low charge/phase thresholds but high charge density thresholds. Engineered to penetrate the target tissue, microelectrodes possess surface areas smaller than approximately 10,000 μm^2. A distinct advantage of microelectrodes lies in their ability to stimulate a relatively confined tissue volume, potentially enhancing the selectivity and spatial resolution of functional responses when deployed in sufficient numbers. Unlike macroelectrodes, which generally resist corrosion and stimulation-induced electrode degradation at clinically relevant charge levels due to their modest charge-injection densities, they may pose a risk of inducing tissue damage owing to their elevated charge/phase levels. Conversely, microelectrodes, marked by high charge densities, grapple with challenges linked to both electrode degradation and tissue damage.

2.1.5 Materials for Electrode Fabrication

When it comes to fabricating electrodes for neural stimulation within the human body, the critical task lies in selecting the most suitable material, involving a comprehensive examination of diverse criteria. Optimal materials are those that not only operate efficiently and safely but also have minimal power requirements [19].

Platinum stands out as the most frequently employed material for electrodes. In the study referenced as [20], it was determined that the charge injection limit for platinum electrodes reached 400 $\mu C/cm^2$, meanwhile in [21] it was found to be 75 $\mu C/cm^2$. Recent investigations have concentrated into the potential of iridium oxide (IrOx) and titanium nitride (TiN) in delivering a higher charge per unit area than platinum electrodes. An exploration of both materials through a cyclic voltammogram (depicted in figure 2.1) clarifies the process of charge transfer within the electrode.

The elevated points depicted in the IrOx graph reveal that most of its charge emanates from redox reactions intricately connected with the oxidation and reduction phenomena inherent in the iridium oxide itself. The cyclic voltammogram enclosed area serves as a metric for the material maximum charge, with only a fraction available for electrostimulation due to chemical reaction rate limits and pore resistance. Comparative analysis indicates that IrOx can store more charge

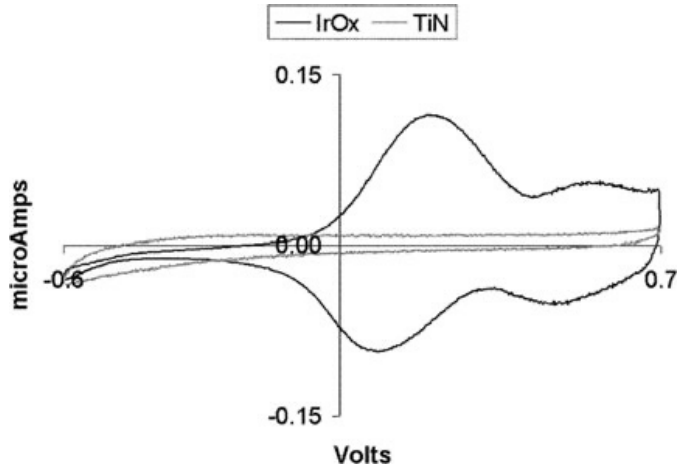


Figure 2.1: Cyclic voltammogram for IrOx and TiN, the reference electrode was a saturated calomel electrode. Reprinted from [22]

than TiN, exhibiting superior charge delivery per unit area, albeit with exceptions at high frequencies.

The redox reactions occurring on the IrOx surface were determined to be fully reversible. The safety thresholds for charge injection concerning electrode integrity were established based on the presumed water window. When the electrode potential falls within this range, theoretically, potentially hazardous hydrolysis does not occur. As documented in [21], the safe limit for iridium oxide was identified as 4 mC/cm^2. TiN demonstrated the ability to convey 950 μC/cm^2 in case of anodic current and 550 μC/cm^2 with cathodic current pulses. These values were obtained using a 0.2 ms current pulse and 4,000 μm^2 electrodes [22]. Consequently, both TiN and IrOx boast higher charge injection capacities in comparison to platinum. PtIr emerges as another material displaying significantly increased charge injection capacity when contrasted with platinum [19]. Additionally, a key consideration is the design of electrodes to be as compact as possible, allowing the implanted chip to maximize performance while minimizing any disruption to the patient.

2.1.6 Electrodes design and current distribution

Two distinct electrode factors should be taken into consideration: geometric surface area and real surface area. Geometric surface area follows traditional measurements, such as the product of length and width for rectangular electrodes or π times the square of the radius for circular ones. However, practical application introduces a nuanced perspective. In cases where the electrode surface displays roughness or porosity, the actual contact area between the electrode and electrolyte surpasses the confines of geometric surface area. This extended interaction area is termed

the real surface area, or electrochemical surface area, accounting for the electrode's surface roughness and potentially resulting in an area that could be many times greater than the geometric surface area. When dealing with faradaic current flow, a rough electrode has the potential to facilitate a greater number of surface chemical reactions compared to its smooth counterpart, even when possessing an equivalent geometric surface area. The characterization of the real surface area often involves a surface roughness factor, denoting the ratio between the real surface area and the geometric surface area. This factor can occasionally exceed 2,000.

The charge injection capacity, indicating the quantity of charge a material can inject before undesirable redox reactions occur, is a critical parameter. Elevating the real surface area contributes to an augmentation in the double layer capacitance of the electrode. Consequently, the voltage across the electrode-electrolyte capacitance is reduced for a given injected charge amount. This voltage reduction acts as a preventive measure against undesired redox reactions, which tend to occur more readily at higher voltage drops across the electrode-electrolyte interface. Notably, in the realm of porous electrodes, the quest for increased charge injection capacity encounters a geometric constrains imposed by pore resistance, placing limits on the feasible enhancement obtained by increasing the ratio between the "electrochemical surface area (ESA)" and the "geometric surface area (GSA)". Experimental determination of the surface roughness factor involves quantifying the adsorption capacity of chemicals onto the electrode surface. With an escalation in electrode porosity, the real surface area increases meanwhile the surface impedance experiences a reduction. Similarly, an augmentation in the thickness of porous metal contributes to an increase in the real surface area of the porous electrode. Favorable outcomes are linked to lower impedances for both stimulating and recording electrodes. The initiation of stimulation requires a specific current density. Higher electrode impedance results in increased voltages, potentially triggering electrochemical reactions that can harm both the electrode and the adjacent tissue. In recording scenarios, where signals are exceedingly small, ranging from microvolts to millivolts, insufficient electrode impedance may obscure these signals within the noisy ionic environment.

The inclination toward larger electrodes in recording situations arises from the reduced total resistance of the solution around the electrode, thereby mitigating thermal noise associated with the resistance in series with the electrode double layer capacitance.

For extracellular signal recording, where the signal lacks direct current and spans frequencies from hundreds to thousands of Hertz, electrodes must possess substantial interface capacitance to maintain low impedance in this frequency range. Consequently, electrodes with increased porosity are advantageous [19].

When utilizing recording electrodes, it is imperative to operate within an input voltage amplitude range that preserves linearity. Nonlinearity has the potential to

distort the shape of the recorded signal, compromising the accuracy of the recorded data.

The distribution of electrical current is significantly influenced by the shape of the electrode. Achieving a consistent primary current distribution across a surface is best exemplified by utilizing a hemispherical metal electrode placed on a flat insulator with infinite dimensions. Conversely, opting for a rectangular shape proves to be suboptimal when considering current distribution. Iain Henly et al. [23] highlighted that the current density at the corners of a rectangular electrode can substantially surpass that of other points along the sides, particularly those away from the corners. This discrepancy arises from a higher voltage drop at the electrode-electrolyte interface, more pronounced at the edges and corners, and less significant in the middle when the electrode potential undergoes abrupt changes.

To promote a more even surface current density, hence reducing susceptibility to corrosion and enhancing patient safety, several modifications can be applied:

- Introducing a recess for the electrodes into insulating wells. For disk electrodes, a recession of 0.1–0.4 times the disk radius has demonstrated significant positive effects, with a deeper recession yielding better results. Although literature does not specify the required depth for rectangular electrodes, the favorable influence of recession on current distribution holds true.
- Opting for a disk-shaped design over a square configuration.
- Incorporating gentle curvature into the electrodes, steering clear of sharp convex corners.

However, the safest and most conservative approach to mitigate adverse reactions at the electrode surface caused by non-uniform current distribution is to confine the electrode potential within the water window. This involves neglecting the impact of access voltage effects, focusing instead on limiting the electrode potential while disregarding the voltage drop across the interface capacitance.

2.2 Probes for neural recording

Advancements in neurophysiology have significantly enhanced our comprehension of neurons and their functional attributes through the utilization of individual microelectrodes. This tool not only facilitates understanding the biophysics governing neuron action potential generation but also establishes the groundwork for comprehending the network properties of the nervous system, revealing the cortex's role as a parallel information processor. Due to their limited diameter (50–100 μm), the functionality of the examined brain regions remains minimally affected by the microelectrode insertion. Furthermore, given that the electrode active area

resides at the inserted shank's tip, the neurons in immediate vicinity encounter reduced interference from both the microelectrode and the implantation procedure. Nevertheless, since the nervous system processes information through the coordinated spatial and temporal activity of extensive neuron assemblies, constraints imposed by single microelectrode electrophysiology have hindered advancements in fundamental brain research. Therefore, to gain a more comprehensive insight into cortical information processing, researchers turn to multielectrode investigations, enabling simultaneous evaluation of neural responses at multiple locations [24] [25]. Neural probe technology has advanced significantly, employing various tools across several scales. Patch clamps, for instance, excel in capturing single-cell electrical activities, particularly in studying ion channel behavior. The evolution of microelectromechanical systems (MEMS) technology has led to the successful implementation of high-density silicon-based microelectrode arrays (MEAs). These MEAs demonstrate the capability to record brain electrical signals with high throughput and temporal precision. Nevertheless, reducing the size of electrode recording sites results in diminished capacitance and heightened impedance at the electrode/tissue interface, significantly impacting recording resolution.

Multiple electrode materials give rise to various microelectrode types, including glass micropipette electrodes, metal microwire electrodes, and semiconductor substrate electrodes. Glass micropipette electrodes, commonly known as patch clamps, serve to record ion channel electrical activity on biological membranes. Contrasting with micropipette electrodes fashioned from high-temperature drawn capillary glass tubes, microwire electrodes showcase reduced high-frequency impedance, an improved signal-to-noise ratio, and superior mechanical characteristics, enabling them to detect voltage variations without adversely affecting cellular activity. While microwire electrodes were among the first implantable microelectrodes for extended brain activity recording, increasing the number of channels poses several challenges. Achieving precise spacing control between microwire electrodes becomes problematic, affecting electrode performance uniformity. The assembly of electrode arrays becomes intricate due to this lack of precision. Advancements in photolithography and silicon etching techniques have led to the substitution of metal microwire microelectrodes by silicon counterparts. Silicon microelectrodes, boasting favorable mechanical properties and biocompatibility, have become prominent. The Utah Intracortical Electrode Arrays (UIEA) and Michigan probes stand out as the foremost examples of silicon-based microelectrode arrays [26].

2.2.1 Recording basic requirements

The human brain's neural network comprises around 86 billion neurons, working collaboratively to transmit information through intricate temporal patterns within the neuronal framework [26]. Comprehending the factors influencing the activation

or inhibition of individual neurons stands as a pivotal inquiry within the realm of neuroscience. Therefore, the optimal detection instrument should encompass the entire spectrum, from the solitary neuron to its intricate web of interconnections, in order to grasp the manner in which a specific 'cell type' processes information. [27]

High quality recording

The primary role of implantable microelectrodes revolves around capturing electrophysiological signals emitted by neurons, particularly spikes, which constitute the fundamental components of neural electrical activity. The precision of recorded signals holds paramount importance in the accurate assessment of neuronal behavior. Various metrics, such as the signal-to-noise ratio (SNR), the capacity for single-unit recording, and the capability for prolonged recording, serve as indicators of signal quality. Notably, both single-unit recording and the ability for long-term recording are intricately linked to SNR, calculated with the following formula, where RMS denotes the voltage's root mean square value across the trace:

$$SNR = \frac{V_{\max} - V_{\min}}{2 \cdot RMS} \tag{2.1}$$

The SNR undergoes its initial modulation through the amplitude of the recording signal, especially within the realm of extracellular spike signals, typically registering around 100μV. A consequential determinant in SNR variation is the amplitude of background noise, encapsulating not only electrode thermal noise but also biological noise. Striking a delicate balance, the cumulative noise baseline necessitates a stringent limit below 20 μV, ensuring a minimum SNR threshold of 5:1.

Diverse factors, both organic and inanimate, exert their sway over SNR. Concerning the device itself, SNR intricately ties itself to the material composition, size dimensions, and structural morphology of the electrode sites. These elements, in turn, mold SNR by influencing the impedance interface at the junction of the electrode and brain tissue. A recurring concern pertains to the precipitous reduction in electrode-tissue interface impedance as the electrode size expands. However, direct augmentation of the electrode encounters dual constraints. Firstly, for enhanced recording selectivity and the attainment of a distinct single-unit signal, the electrode cannot exceed a certain size. An optimal electrode size is vital to enhance recording selectivity and procure a reliably distinct single-unit signal. Compliant with extracellular recording principles, an increase beyond a specific electrode size tends to average out signal amplitude, resulting in discernible local field potential (LFP) signals reflecting neural population activity. Secondly, adherence to size constraints is crucial for implantable devices with a compact footprint to minimize potential damage. Navigating these constraints, modifications to the electrode

interface frequently become imperative to attain a more expansive exposed surface area within confined dimensions.

Materials commonly employed for modifying interfaces encompass metals like gold and platinum, metal nitrides such as titanium nitride, carbon materials including carbon nanotubes, carbon nanofibers, and graphene, metal oxides like iridium oxide, and conductive polymers such as poly(3,4-ethylene diox-ythiophene) and polypyrrole. Metals, metal nitrides, and carbon materials serve the purpose of enlarging electrode surface areas through the construction of micro/nanostructures, thereby enhancing the electrochemical properties and maintaining the original geometric size, resulting in reduced impedance and heightened charge storage capacity. Titanium nitride, in particular, stands out for its commendable conductivity, mechanical resilience, and stability. Carbon-based nanomaterials, characterized by substantial electrical conductivity and extensive surface area, present a unique set of considerations. When employed independently, they encounter challenges in forming secure bonds with electrodes, thus limiting advancements in electrochemical properties. Conversely, specific conductive polymer variants demonstrate positive biocompatibility and a pronounced attraction to neurons, thereby aiding in minimizing potential tissue harm. However, these advantages are counterbalanced by persistent concerns about the durability of conductive polymers, coupled with their inadequate bonding to metallic substrates.

Stable and long term recording

In the realm of in vivo applications, an implantable electrode must exhibit prolonged and dependable functionality. This endurance comprises two key aspects. Firstly, the electrode itself must maintain stability within the extracellular fluid environment, necessitating a robust fusion of insulation and conductive materials. Potential pitfalls such as cracking, delamination, peeling, and degradation may all contribute to device failure. Common occurrences include cracking and delamination at the tip of microwire electrodes, where the insulation layer peels away, exposing the recording site. Delamination is also evident between distinct layers of planar electrodes. Adhesive coatings, including Ti, Cr, and silane, are frequently integrated to bolster adhesion between the conductive material and insulation. Surface processing methodologies, encompassing thermal annealing and functionalized surface treatments, are routinely employed to elevate adhesion while mitigating delamination. The second crucial aspect of ensuring stability revolves around the compatibility of the device with biological tissue. Achieving biocompatibility necessitates the exclusive use of materials during manufacturing that pose no biotoxicity risks. The act of inserting the device runs the inadvertent risk of causing harm or even the demise of neurons directly interacting with the device, establishing what is informally known as a "kill zone" marked by a substantial reduction in

neuronal density. Throughout this phase, macrophages (microglia) aggregate around the electrode, contributing to localized neuronal toxicity. The subsequent stage in tissue response transitions into the chronic immune phase due to prolonged exposure to the device. Chronic responses primarily originate from tethering modes, brain micromotion, and mechanical disparities. While implanted electrodes are conventionally affixed to the skull, the inherent mobility of brain tissue within the cranial cavity introduces a great complexity. Even minimal brain movements can induce asynchronous motion between electrodes and brain tissue, potentially causing damage due to the mechanical discrepancies introduced by the electrode. Sustained and ongoing damage triggers the gathering of macrophages and astrocytes around the electrode, gradually compacting over time and culminating in the formation of a glial scar zone spanning approximately 100 μm, the typical maximum range for neural microelectrode recording. The emergence of glial scarring serves to isolate electrodes from the neighboring tissue, augment the distance between recording sites and neurons, and modify the diffusion properties of brain tissue, potentially elevating recording resistance. Softness is a term employed to convey the pliability of a material and denotes its capacity to withstand localized pressure from a rigid object. Flexibility, on the other hand, characterizes the rigidity of a material and alludes to its ability to resist elastic deformation when subjected to external forces, often quantified by Young's modulus. Consequently, the mechanical incongruity between brain tissue and electrodes encompasses two inherent material attributes: hardness and stiffness. The stiffness discrepancy gives rise to forces acting between brain tissue and electrodes during asynchronous movement. Simultaneously, the hardness incongruity culminates in damage to the brain tissue caused by electrodes under these applied forces. Both stiffness and hardness are intrinsic material traits, unaffected by shape or size. Flexibility in materials is characterized by compliance, which represents the inclination to deform under external forces, especially relevant to elastomers. The measure of bending stiffness can be estimated through the formula:

$$Bending\ Stiffness = \frac{E \cdot w \cdot h^3}{12} \tag{2.2}$$

In this expression, E denotes Young's modulus, w signifies the width of the electrode, and h represents the thickness of the electrode. It's essential to note that the bending stiffness isn't exclusively determined by material rigidity; rather, it is influenced also by the electrode's footprint. Consequently, electrodes labeled as compliant may not universally translate to flexibility. Elevating electrode compliance offers the potential to alleviate forces between the electrode and tissue, while amplifying softness assists in reducing tissue damage caused by forces exerted by the electrode, ultimately diminishing the immune response from the tissue. Enhancing compliance can be approached through soft tethering, a technique predominantly employed in Utah arrays and hybrid integrated electrodes with a combination of rigidity and

flexibility. Take the Utah array, for instance, constructed primarily from silicon boasting a high Young's modulus. The enhancement of compliance involves the incorporation of pliant ribbon cables, connecting the unyielding electrodes nestled within softer brain tissue to the rigid head stage affixed to the skull. The flexibility of these cables enables encapsulation without disrupting the electrodes embedded within it and the design enables the rigid electrodes to harmoniously move with the fluctuating brain tissue during micromotion, thereby diminishing tissue-electrode interaction and advancing the stability of the long-term interface.

Ultrasmall electrodes exhibit a marked reduction in damage upon implantation and provoke minimal tissue response. Nevertheless, the difference in Young's modulus between conventional rigid electrode materials and soft biological tissues amplifies the rejection of invasive probe, leading to diminished electrode functionality. To address this issue, a viable solution is to apply a softer biocompatible coating to the surface of a rigid electrode. Opting for polymer materials with a lower Young's modulus as the substrate for the electrode enhances both its softness and flexibility and such electrodes fall into the category of flexible electrodes. These compliant electrodes effectively alleviate the repercussions of brain micromotion, thereby diminishing chronic tissue responses. Additionally, they enhance charge storage capacity and lower interfacial impedance, consequently boosting the signal-to-noise ratio (SNR) in detecting electrophysiological signals. Despite these advantages, their buckling strength tends to be low, presenting a challenge in the smooth implantation into the brain, as they are more predisposed to bending than to be inserted. [26][28].

Utah Intracortical Electrode Arrays (UIEA)

Originating from a silicon monocrystalline block, the Utah electrodes, taking their name from the University where they were developed, underwent intricate micromachining using a diamond dicing saw and subsequent chemical etching. The array structure featured a 4.2 mm by 4.2 mm substrate, approximately 200 μm thick, hosting 100 needle-like electrodes projecting in a 10 x 10 array with 400 μm spacing. Each needle, approximately 1.5 mm in length, tapered from an 80 μm base diameter to a pointed tip. Situated on the opposite side of the substrate from each needle was an aluminum pad, enabling contact with the electrode. Coatings of platinum or gold were applied to the tips, and the entire array (excluding the tips) was encased in polyimide during encapsulation. In the initial manufacturing approach, *Jones et al. [29]* utilized a unique method, termed thermomigration, to achieve electrical isolation among individual electrodes within the array before any micromachining phase. This process enabled the creation of electrode arrays, ensuring separation between any two electrodes by employing a pair of opposing p-n junctions. The leakage currents of these p-n junctions were observed at an average

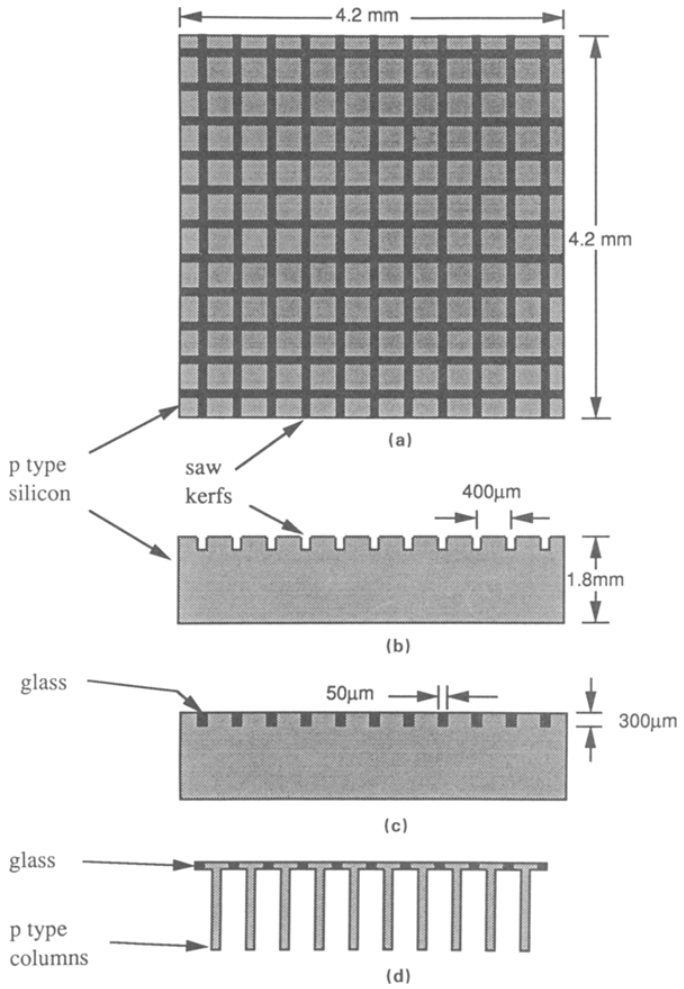


Figure 2.2: Silicon die illustration: A) top view, displaying perpendicular rows of incised grooves on the surface; B) profile view of the die with 50 μm grooves; C) incorporating molten glass into the grooves and smoothing the surface; D) creating columns in the die through a diamond dicing saw. Reprinted from [29]

of 3.3 nA under a 1V condition. As a result, effective electrical isolation among the electrodes within the array was achieved. In [29] the current method of array production enables the construction of a "structure in which long, tapered electrodes are essentially suspended in a sea of glass substrate". This involves fusing frit glass into shallow saw kerfs on one side of a silicon substrate and removing a significant portion of the silicon material through deep saw kerfs cut from the opposite side of the silicon chip. This method produces elevated silicon columns connected at their bases by the glass. This glass segment isolates each array electrode, establishing a remarkably effective insulating layer between neighboring electrodes. [29]

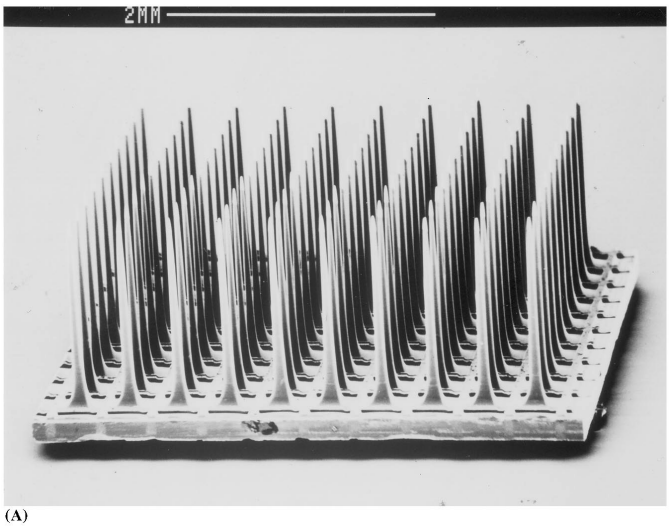


Figure 2.3: SEM image of Utah Intracortical Electrode Array. Reprinted from [30]

Arrays built with metal microelectrodes (AMM)

Given the efficacy and simplicity of single metal microelectrodes, early devices designed to interface with multiple neurons integrated several metal electrodes into a unified multi-electrode array. An illustrative instance of this approach is the

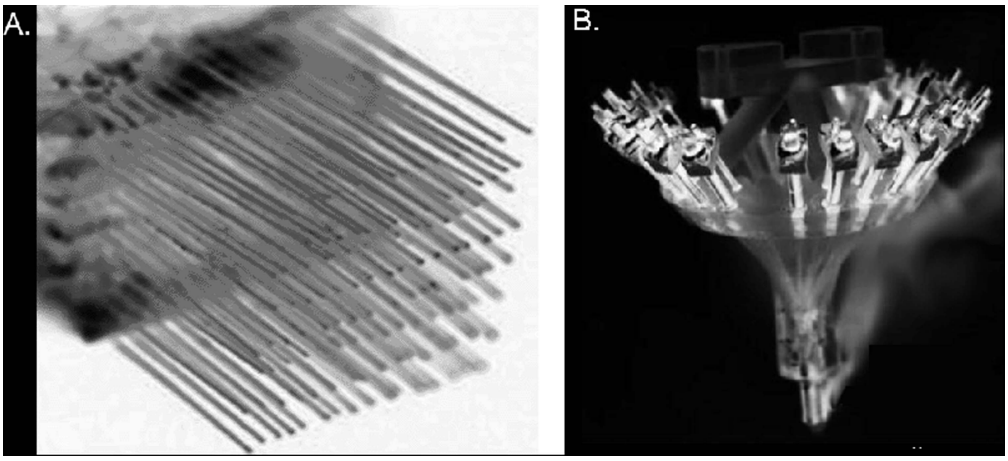


Figure 2.4: (A) Handcrafted penetrating microelectrode array assembled from several insulated wires with trimmed ends.). (B) Microwire array designed for long-term utilization in small animal experiments. Reprinted from [25]

microwire array depicted in figure 2.4A. Typically crafted by bonding the proximal

ends of numerous insulated metal wires onto a single substrate. A modified version of this architecture involves attaching individual metal microelectrodes to separate micromanipulators, enabling the advancement of each microelectrode to a specific cortical depth or fine-tuning the depth for optimal recording of single-unit activity. The device in figure 2.4B exemplifies a compact and lightweight design, facilitating direct mounting on the skulls of small animals (NeuroTek, Toronto, Canada). Noteworthy is the repositioning capability of microelectrodes, allowing for recording new neurons as the recording quality of previously captured sites diminishes as time passes. A straightforward yet potent penetrating electrode array can be created by twisting several distinct wire elements into a unified, wider-diameter electrode configuration, exemplified by the tetrode. Focusing multiple elements within a compact cortical area enables researchers to leverage the amplitudes of responses on each individual element for triangulating the recorded elements' positions.

Tetrode

Extensively employed in neural systems, the tetrode serves as a tool for recording extracellular electrical potentials. Marked by the prefix (tetr-), it embodies four electrodes detecting neuronal signals from different spatial points originating from a common source. Typically crafted from a platinum–tungsten alloy and insulated with a quartz coating, these electrodes expose their metal ends to acquire electrical signals. The diameter of each electrode at the metallic terminus is usually under 30 μm, potentially extending up to 100 μm at the coated terminus. The coating purpose is to curtail interference of electrophysiological signals across electrodes. Figure 2.5 illustrates that a lone tetrode can gauge extracellular potentials from approximately 1,100 neurons within a 140-μm radius in the rat cortex [31]-[32]. A primary benefit of employing this technique instead of individual-channel electrodes lies in the ability for users to categorize extracellular potentials from neighboring neurons through a clustering methodology [33]-[34]. The tetrode four electrodes detect distinct temporal points and waveforms of each neuron's extracellular potentials, attributed to variations in spatial distances between electrodes and neurons. This enables the separation of spikes from multiple neurons during post-processing. Nevertheless, a single tetrode lacks the capability to directly measure spatially multi-dimensional extracellular potential distributions. Achieving this would require precise implantation and arrangement of multiple tetrodes at regular intervals.
[35].

Michigan Probe

Both the Utah array and the tetrode enable the recording of neural activity from diverse cortical regions. Nevertheless, their effectiveness is constrained when it comes to accessing deep neural structures along the axial dimension [36][37]. By

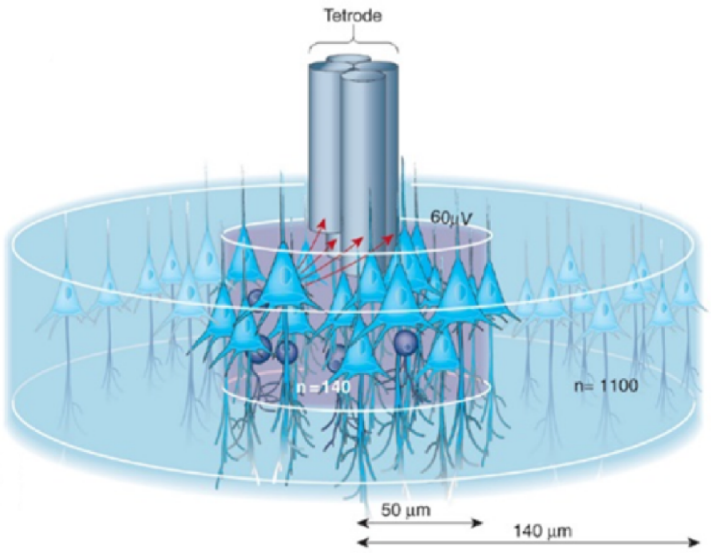


Figure 2.5: The tetrode and its detecting area. With improved clustering and spike sorting, the tetrode can identifie neural activities in assemblies with 280 μm diameters. Reprinted from [35]

the close of the 1970s, the initial iteration of the Michigan probe, a prototype for a multi-channel depth electrode, materialized through the application of electron-beam lithographic techniques. Multiple preclinical investigations with small animals have affirmed the prolonged safety of Michigan probe implantation. These findings imply the potential utilization of such probes in BMI systems. Notably, the electrodes within the Michigan probe measure between 2 to 15 mm, surpassing the lengths found in the Utah array (typically 0.5 to 1.5 mm in research settings). Consequently, the Michigan probe emerges as a potentially preferable choice for recording activities in correspondence of substantial depths within the cortex. [35]. Michigan probes exhibit a range of beneficial characteristics such as production in batches, ensuring consistent reproduction of both geometric and electrical attributes. Moreover, these devices are compact, facilitating seamless integration with silicon ribbon cables and the inclusion of on-chip electronics for effective signal conditioning. The platform's flexibility is evident in its adaptability for customized designs across a spectrum of applications. One instance is the assembly of planar probes into multiplane arrays, precisely situating recording sites in the brain's three-dimensional space. Additionally, hybrid assemblies are achieved by coupling probes with polymer ribbon cables, offering increased mechanical flexibility. Unique probe designs feature microchannels along the shanks, allowing controlled

microscale fluid delivery through the blood-brain barrier. The first step of the Michigan probe fabrication process involves the targeted introduction of boron into a silicon wafer, defining the device's shape and thickness. Insulation from the conductive boron-doped substrate is provided by subsequent deposition of silicon dioxide and silicon nitride dielectric layers. The application of a conductive interconnect material (typically polysilicon) follows, with deposition, patterning, and insulation using upper dielectrics. To establish recording sites, a combination of wet and dry etching is employed for selective access through the upper dielectrics to the polysilicon layer. Following this, metal is deposited and patterned, utilizing a lift-off technique to create the electrode sites and bond pads. Dielectrics in the field area are removed using a dry etch. This process uses eight photolithographic masks and enables the design of a wide variety of planar probes, with specific site configuration and physical layout customized to the targeted neural structure [38].

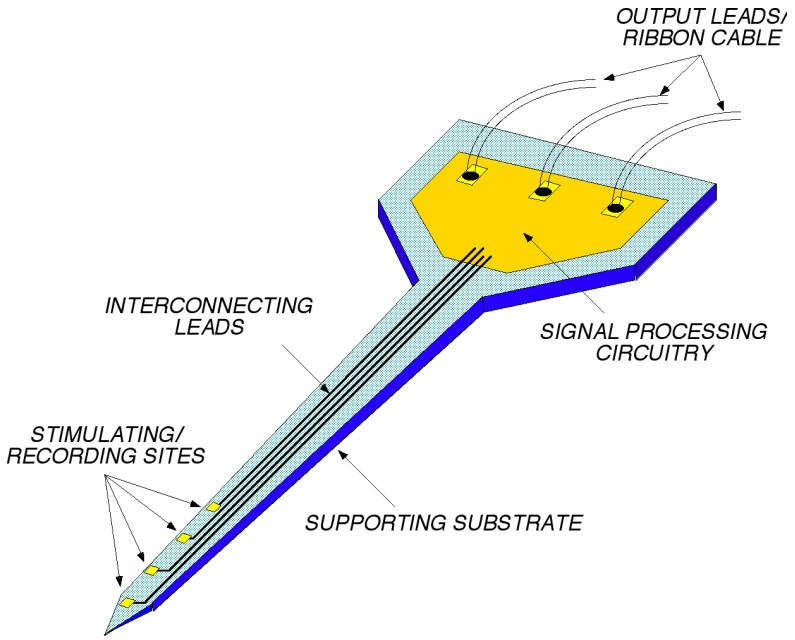


Figure 2.6: Michigan probe. Reprinted from [39]

Planar Electrode Arrays (PEA)

Microfabrication techniques developed for integrated circuitry and micro-electro-mechanical devices now shape recent microelectrode arrays.

Rooted in planar photolithography, early arrays were primarily one and two-dimensional with a single shaft figure 2.7A or 'pitchfork' geometry. In the early stages, planar arrays employed gold or platinum on penetrating shafts crafted via

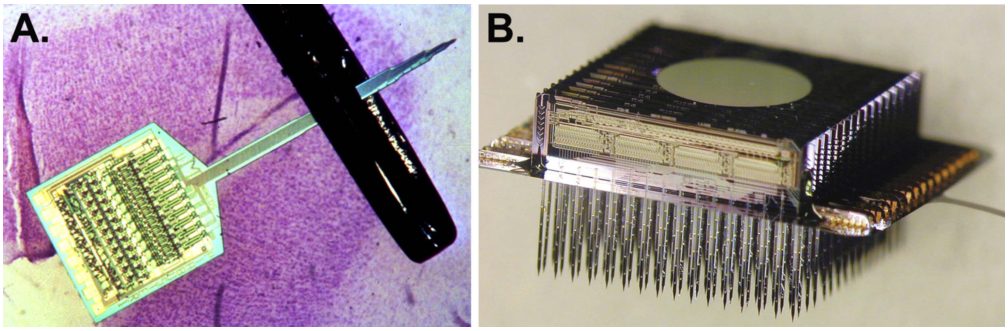


Figure 2.7: (A) Illustration of a four-tine fork featuring two rows of microelectrodes on each prong. The probe base's contact pads serve for interconnections or cable assemblies. (B) A NeuroProbe array in three dimensions, featuring multiple recording sites connected to a pliable ribbon cable. Taken from [25]

photolithography and acid etching on sapphire or silicon wafers. High-resolution photolithography facilitated depositing numerous microelectrodes on the shafts, connecting them with gold traces to bond pads or integrated circuitry on the array's substrate. However, this flat design confines researchers to planar sections of nervous tissues, limiting neural access. Hoogerwoff and Wise (1994) creatively linked planar arrays to break this constraint, creating a genuine 3D recording structure figure 2.7B.
Table 2.1 provides a comprehensive overview of various types of probes discussed in current literature, offering a detailed examination of their advantages and disadvantages. To simplify writing, we will use the following abbreviations:

- Utah Intracortical Electrode Arrays (**UIEA**)
- Arrays built with metal microelectrodes (**AMM**)
- Planar Electrode Arrays (**PEA**)

Probe Type	**Advantages**	**Disadvantages**
UIEA	• High spatial resolution • Flexibility and precision • Reliable signal acquisition	• High cost • Complexity in usage
AMM	• High conductivity • Good precision and resolution in stimulation • High durability	• Rigidity • High cost
TETRODE	• Greater sensitivity in recording • Comprehensive view of brain activity • Noise reduction	• Operational complexity • Dimensions • High cost
MICHIGAN	• Detailed mapping of neural signals • Reliability • Compatibility with advanced technologies	• Operational complexity • High Cost
PEA	• Compact configuration • Lower invasiveness • Compatibility with advanced technologies	• Limited resolution • Risks of interference • Technical complexity

Table 2.1: Advantages and disadvantages of different probes.

Chapter 3

Microelectrodes Fabrication

Despite the variety of probe types documented in the literature, none currently meet the requirements to obviate the reliance on powered implantable external units and wired connections. The strength of the probes proposed in the following chapter lies in the integration of CMOS technology, which enables the incorporation of advanced electronic circuits onto small probes, facilitating the development of compact and minimally invasive devices. This is critical for minimizing surgical impact and enhancing the precision of brain stimulation. CMOS integration also serves to minimize power consumption and reduce electromagnetic interference and noise in recorded or stimulated signals.

The realization of probes for cerebral stimulation and recording entails a series of specific microfabrication steps, originating from a silicon wafer, ensuring the precision and reliability of subsequent implantable devices.

Following the initial 2D fabrication (figure 3.1a), the probes undergo a critical release process and are subsequently subjected to a bending procedure (figure 3.1b) using a custom made nano-device. This deliberate bending is essential not only to align the probes with their designated functions of stimulation and recording but also to achieve a configuration optimized for seamless implantation. The choice of this methodology is driven by a meticulous consideration of the practical requirements and challenges associated with implantable devices in neurological applications.

Moreover, identifying the challenges previously discussed concerning the integration of CMOS technology with implantable microelectrodes, this thesis introduces and refines an alternative paradigm. This alternative approach is rooted in the post-CMOS fabrication of the probes, offering a pragmatic solution to the intricate integration challenges faced in contemporary neural interfaces.
The electrodes microfabrication was conducted at CMi (Center of Micro and Nanotechnology) in Lausanne, which is equipped with clean rooms designed to ensure

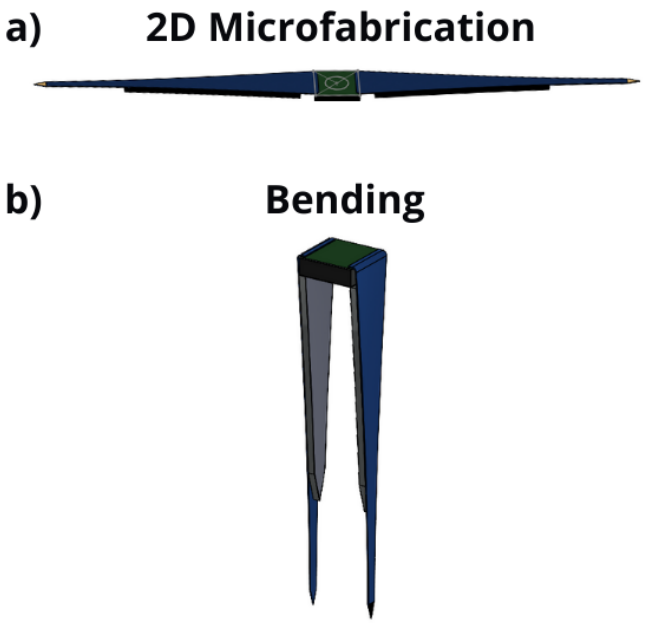


Figure 3.1: Schematic representation illustrating the final fabrication result in 2D a) and subsequent to the bending process b).

the secure execution of various microfabrication steps while mitigating the risk of contamination. A clean room is a enclosed environment featuring continuous air supply through filters with laminar flow from top to bottom and meticulous control of working conditions, including temperature, humidity, and UV-light exposure. The air purification system plays a vital role since it hinders external microorganisms or dust particles from infiltrating, thus preserving the internal environment as entirely sterile and aseptic. The different zones within the clean room can be divided into nine ISO classes according to the maximum permitted number of airborne particles present in a given volume of air; in table 3.1 division in different classes is shown. This controlled and sterile environment is essential for the precision and reliability of the microfabrication processes.
A process flow was meticulously developed to guide the fabrication of microelectrodes. Following a comprehensive evaluation by the CMi staff, the proposed process flow received approval, marking the initiation of the manufacturing process. This process flow furnishes a meticulous roadmap, delineating the sequential steps and specifying the machines to be employed. Its approval is pivotal in averting errors stemming from potential incompatibilities between machines and materials or among various procedural steps. Throughout the manufacturing process, certain steps were modified or added to the initial version to enhance overall performances.

Prior to initiating the microfabrication procedures, the electrode design must be conceived using technical drawing software, such as *AutoCAD (version 2024, Autodesk Inc.)*. This phase encompasses the delineation of individual layer designs that will subsequently be transferred onto the wafer through various photolithography processes. The design specification must also consider specific constraints associated with the machinery employed, such as the machine's resolution for the photolithography exposure step, which is approximately 1 μm. Hence, a certain margin of error must be considered during the realization of the design.

ISO classification number	Maximum concentration limits (particles/m^3 of air)					
	0.1 μm	0.2 μm	0.3 μm	0.5 μm	1 μm	5 μm
ISO Class 1	10	2	–	–	–	–
ISO Class 2	100	24	10	4	–	–
ISO Class 3	1,000	237	102	35	8	–
ISO Class 4	10,000	2,370	1,020	352	83	–
ISO Class 5	100,000	23,700	10,200	3,520	832	29
ISO Class 6	1,000,000	237,000	102,000	35,200	8,320	293
ISO Class 7	–	–	–	352,000	83,200	2,930
ISO Class 8	–	–	–	3,520,000	832,000	29,300
ISO Class 9	–	–	–	35,200,000	8,320,000	293,000

Table 3.1: Maximum concentration limits for particles equal to and larger than the reported size according to the different ISO classes.

3.1 Overview of Materials Employed

The starting material is a silicon wafer, specifically selected from those offered at the CMi facility and detailed in the accompanying table 3.2. The chosen substrate is a p-doped <100> wafer, with 380 μm of thickness, a 100 mm diameter, and a bulk resistivity falling within the range of 0.1-0.5 $\Omega \cdot$ cm, low enough to increase stimulation precision. The notation <100> specifically defines the orientation of the crystal plane, indicating perpendicular alignment with the x-axis and parallel alignment with the z- and y-axes. The wafer's orientation stands as a pivotal parameter within the semiconductor industry, exerting influence over the operational efficiency and characteristics of the electronic devices produced on the wafer. In the realm of microelectronics, <100> wafers are prevalent. However,

when it comes to Bipolar Transistors, <111> wafers are the preferred choice, while <110> wafers are specifically utilized to achieve particular orientations for etching processes. The notation "p-doped" specifically indicates the type of dopant employed. Indeed, silicon wafers undergo a process known as doping, where various elements are introduced to modify their electrical characteristics. The primary objective behind doping silicon wafers is to enhance energy flow by minimizing resistance, thus facilitating a smoother current passage through the material. This becomes imperative for the optimal operation of diverse electronic devices, including transistors, solar cells, and rectifiers. Doping incorporates a range of elements, such as boron, fluoride, arsenic, phosphorus, antimony, and nitrogen. The specific dopant utilized has a direct impact on the conductivity and other electrical properties of the silicon wafer. Introducing boron, for example, leads to the formation of p-type silicon, a critical component in the fabrication of various electronic devices. [40] The concentration of the dopant plays also a crucial role in determining the bulk resistivity of the silicon wafer, i.e. the property that governs silicon ability to conduct electricity. As the concentration of dopants rises, the resistivity of the silicon wafer decreases, causing a shift in its electrical conductivity [41] as shown in the reported figure 3.2.

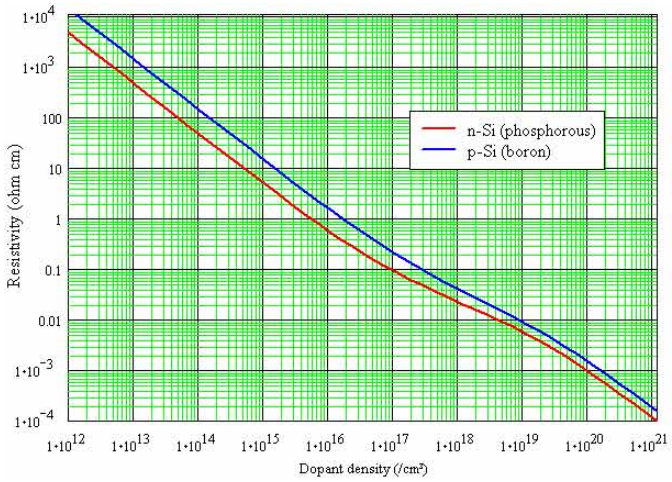


Figure 3.2: Relationship between Dopant Concentration and Resistivity in Silicon. Reprinted from [41].

For this application, opting for wafers with low bulk resistivity is preferable, as it ensures:

- Improved Electrical Performance: enhanced electrical conductivity is facilitated by low resistivity, offering advantages across a spectrum of electronic applications, including integrated circuits, transistors, and diodes;

- Minimized Power Consumption: utilizing wafers characterized by reduced resistivity results in electronic devices that demand lower power consumption, thereby contributing to heightened energy efficiency [42];
- Improved Signal Propagation: wafers with diminished resistivity offer benefits in scenarios demanding swift signal transmission, particularly in high-frequency devices and communication systems.
- Augmented Sensitivity: within specific sensor applications, wafers characterized by reduced resistivity can provide heightened responsiveness, enhancing the ability to detect and measure minute electrical signals [41].

Name	**Diameter**	**Thickness**	**Orientation**	**Doping**	**Resistivity** [$\Omega \cdot$ **cm**]
100/P/SS/01-100	100	525	<100>	P or N	0.1 – 100
Single side polished	± 0.5 mm	± 25 μm			
100/P/DS/1-10	100	380	<100>	p	1 – 10
Double side polished	± 0.2 mm	± 10 μm			
100/P/SS/01-05	100	525	<100>	p	0.1 – 0.5
Single side polished	± 0.2 mm	± 20 μm			
100/P/DS/01-05	100	380	<100>	p	0.1 - 0.5
Double side polished	± 0.2 mm	± 10 μm			
150/P/SS/15-25	150	675	<100>	p	15 – 25
Single side polished	± 0.2 mm	± 20 μm			

Table 3.2: Characteristics of wafers available at CMi.

The materials employed in the diverse stages of manufacturing must adhere to biocompatibility standards. This is crucial as the electrodes are intended for implantation in the brain and must ensure sustained stimulation over an extended duration. Consequently, post-implantation, the electrodes should not induce inflammatory reactions, undergo degradation, and must assure long-term safety by minimizing performance deterioration. The involved materials and their main characteristcs, together with biocompatibility and biostability, are:

- Titanium:
  - It serves as adhesive layer;

  - Light weight;
  - Wear resistant;
  - High strength;
  - Low density [43][44][45].

- Aluminum:
  - Low cost;
  - Corrosion resistant;
  - Light weight;
  - Good conductivity ($\sim 3.5 \cdot 10^7$ S/m);
  - CMOS compatible [43].

- SiO_2:
  - Easy surface modification;
  - Low conductivity ($\sim 10 \cdot 10^{-10}$ S/m) [46].

- Parylene:
  - Flexible;
  - Absolute conformance to substrate topography;
  - Pinhole-free coverage even in very thin applications;
  - Effective capability to infiltrate and cover intricate geometries;
  - It forms a strong barrier against contaminants, resisting corrosion [47].

- SiC:
  - Low dissolution rate;
  - High Power densities;
  - Low energy losses;
  - Light weight;
  - Robust [48][49].

3.2 Electrodes Design

The electrodes were meticulously designed using AutoCAD, a robust computer-aided design (CAD) software. This tool allows for the meticulous definition of distinct electrode layers, contributing to the creation of a matrix comprising four electrode arrays, each characterized by a consistent design tailored for this specific application. Within each array, electrodes share a consistent design. The organized structure of each array consists of 20 rows and 5 columns, resulting in a comprehensive total of 400 electrodes per wafer.
One of the primary considerations in electrode manufacturing, as previously discussed, refers to biocompatibility. In biomedical domain, biocompatibility denotes a material capability to seamlessly integrate into biological tissue without inducing adverse reactions. Consequently, a potential approach to enhance biocompatibility is to minimize the amount of material that will be in contact with brain tissue following electrode implantation, requiring so a miniaturization of the electrodes and a wireless communication system.
Probes are designed with precision, featuring a compact structure consisting of two elements: an square-shaped pad with a side length of 250 μm and two shanks with a length of 1.6 mm. The specific dimensions are illustrated in the accompanying figure 3.3, underscoring the meticulous attention to size and form in alignment with the overarching theme of miniaturization.

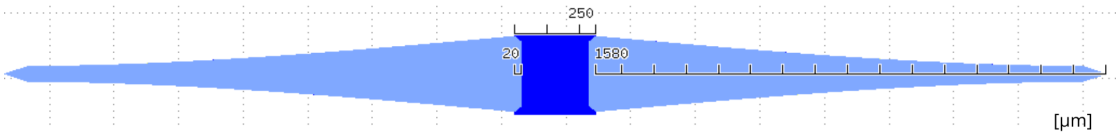


Figure 3.3: Illustration of the probe design with respective dimensions.

As depicited in the reported figure, a 20 μm length of the shank is intentionally overlapped with the pad to ensure a robust mechanical connection between these two distinct elements.
Figure 3.4 instead, displays a segment of the printed design, featuring probes fabricated within a rectangular structure measuring 450 by 3610 μm. This avoids during all the etching procedures to decrease the wafer thickness in the whole wafer, isolating the thickness reduction only within that rectangle and reducing the risk to break or damage the wafer during handling. As shown, the spacing between various structures is determined to ensure a minimum aspect ratio of 1:2 mitigating potential clamping issues arising from the non-uniformity of the Parylene-C layer employed for front-side protection.

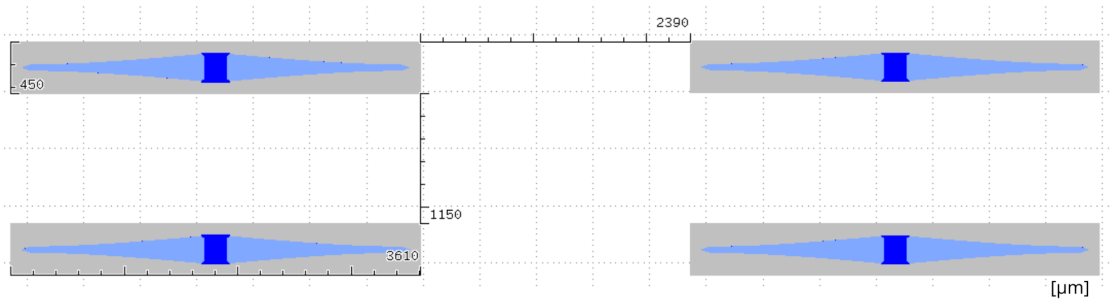


Figure 3.4: Illustration of portion of the design.

3.3 Microfabrication Methods

The subsequent section will delineate the procedural steps and machinery involved in the fabrication process leading to the development of the microelectrodes.

3.3.1 RCA and WetOxidation service

The initial stage in the process flow involves a service provided by CMi, specifically RCA cleaning and wet oxidation on both sides of the wafer (figure 3.5.

Figure 3.5: Wafrer section after Wet Oxidation

The Plade RCA wet bench is exclusively designated for the cleaning of wafers and samples before subjecting them to high-temperature processes in the Centrotherm furnaces. This adheres to the procedure established by W. Kern et al in 1970, whose steps are summarized below:

1. RCA 1 for the elimination of the organic elements. The processing temperature is 75°C and the processing time 15 min.

2. Rinse 1 min

3. HF (Can be optional) for the removal of the silicon oxide generated during the RCA 1 step. The removed thickness is 70A for 15 s on thermal oxide. This step can be skiped for blanket silicon wafers with oxide on it.

4. Rinse 1 min

5. RCA 2 for the elimination of the metallic elements. The processing temperature is 75°C and the processing time 15 min.

6. Full rinse 15 min with the Fast Fill Rinse bath (FFR) and the Trickle Tank (TT) bath .

7. Drying of the wafers with the Spin Rinse & Dry (SRD) system [50].

The key details concerning the three RCA baths are succinctly presented in table 3.3 below

Step	**Solution**	**Temperature**	**Duration**
RCA-1	H_2O:NH_4OH:H_2O_2 (5:1:1)	75°C	5 to 15 min
HF	HF:H_2O (1:10)	20°C	15s
RCA-2	H_2O:HCl:H_2O_2 (6:1:1)	75°C	5 to 15 min

Table 3.3: RCA cleaning steps [50].

After being adequately cleaned, wafers undergo a thermal growth process of SiO_2 in Centrotherm furnaces. The thermal growth of SiO_2 can be achieved through two methods: dry oxidation and wet oxidation. In dry oxidation, only pure O_2 is introduced into the tube at elevated temperatures. Conversely, in wet oxidation, a regulated mixture of O_2/H_2 is injected. Wet oxidation is typically employed for thicker layers (200 nm or more) due to its faster processing (known as the rapid process oxidation). On the other hand, dry oxidation is generally utilized for thin oxide layers ranging from 0.1 nm to 200 nm to ensure precise thickness control [51]. In this specific application, a 200 nm layer of SiO_2 is deposited, enabling the wet oxidation process and streamlining this phase. The presence of SiO_2 is crucial because constructing structures directly on bare silicon (a semiconductor) would result in all elements being short-circuited together, rendering the application ineffective.

3.3.2 Aluminum layer - Frontside

Metal deposition

The initial stage of the process involves the deposition of metals (figure 3.6), specifically 10 nm of Ti and 4 μm of Al. In this context, Ti is utilized to enhance the adhesion of Al to the silicon substrate, addressing the inherent poor adhesion between Silicon and Aluminum.

Figure 3.6: Wafer section after metal deposition

The metal deposition process employs the *Spider 600 (Pfeiffer-Vacuum, Germany)* machine, which relies on sputtering method. In sputtering, energetic particles collide with the target (i.e. the metal intended to be deposited), leading to the ejection of atoms that subsequently cover the wafer surface [52]. To prevent metal deposition on the backside, a dummy wafer is strategically used by placing the substrate on top of it, thereby safeguarding the backside of the Si wafer from coating. Both metals are deposited at room temperature with a power of 1kW, employing two distinct process modules. PM1 is employed for Ti, whereas PM4 is utilized for Al, and the corresponding parameters are outlined in table 3.4. The deposition time is determined by the ratio of the desired thickness to the deposition rate: this calculation results in a deposition time of 7 s for Titanium and 18 min 36 s for Aluminum, as illustrated in formula 3.1:

Material	Target	Film	Source	Power [kW]	Gas [sccm]	V [nm/min]
Ti	Ti_r	Ti	RF	1	Ar(15)	90.0
Al	Al	Al	DC	1	Ar(15)	215.0

Table 3.4: Metal deposition parameters [53].

$$t_{Ti} = \frac{10\,\text{nm}}{90\,\text{nm/min}} = 7\,\text{s} \quad \text{e} \quad t_{Al} = \frac{4000\,\text{nm}}{215\,\text{nm/min}} = 18\,\text{min}\,36\,\text{s} \tag{3.1}$$

Photolithography

The following step consists in the precise imprinting of a specific pattern onto a photosensitive material on the wafer surface through a process called photolithography. This process comprises three distinct phases: Photoresist (PR) coating, exposure, and photoresist development.

1. **Photo resist coating**
   Coating is performed with *ACS200 (SÜSS MicroTec, Germany)*, enabling the rapid covering of the desired resist type and thickness onto the wafer surface (figure 3.7). In this instance, a quick application of 5 µm of *AZ ECI 3027* (positivce photoresist) is achieved, completing the entire process in approximately 8 minutes.

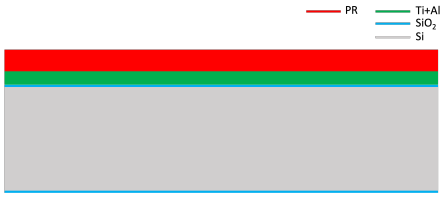


Figure 3.7: Spin coating technique [54].

Prior to the actual coating, *ACS200* conducts a surface preparation tailored to the resist type and surface material as depicted in table 3.5. In this case, with the surface material being Al, the preparation involves thermal dehydration, aiming to eliminate humidity and other impurities from the wafer by heating it.

Surface material (larger area)	**Vapor HMDS**	**Plasma O_2**	**Thermal dehydration**
Si	✓✓	✓	✓
SiO_2, Fused s Silica, SiN, Si3N4	✓✓	✓	✓
Float glass, Pyrex	✓	✓✓	✓
Metals: Al, Au, Pt, Ti	...	✓	✓✓
Metals: Ag, Cu, Cr, Fe	...	X	✓✓
III/V Semiconductors (GaN, GaAs)	...	X	✓✓

Table 3.5: Surface Preparation Details. Legend: ✓✓ Strongly recommended / ✓ Alternative process / ... Not effective / X May affect or destroy under laying material [55].

Following surface preparation, the coating process proceeds to spin coating. In spin coating, a liquid is applied to a flat substrate and then rapidly spun, creating a thin, uniform film through centrifugal force, as shown in figure 3.8 [56].

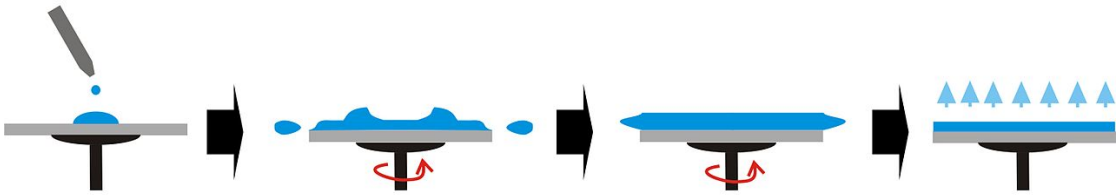


Figure 3.8: Spin coating technique [54].

Consequently, as the rotation speed increases, the thickness of the photo resist diminishes, as indicated by the spin curve in figure 3.9 that correlates film thickness with rotation speed. Given the desired photo resist thickness of 5 μm, the machine configures the rotation speed to 1020 RPM, as determined by the spin curve.
Subsequent to the coating process, a thorough cleaning of the wafer surface is conducted to eliminate any residuals of photoresist. Two alternatives are available: edge bead removal and edge clean. The avoidance of the edge bead removal function is deliberate, as its implementation has been observed to potentially induce parylene detachment in the latter stages of the process flow. Consequently, the edge clean option is selected, complemented by backside rinsing to mitigate the risk of contaminations. The edge clean procedure involves the meticulous removal of any surplus material deposited on the wafer's edge during the spin coating phase.

2. **Exposure**

   The exposure process is executed utilizing *MLA 150 (Heidelberg, Germany)*, a mask less aligner facilitating the direct printing of a design without the necessity of procuring or manufacturing a mask (figure 3.10).

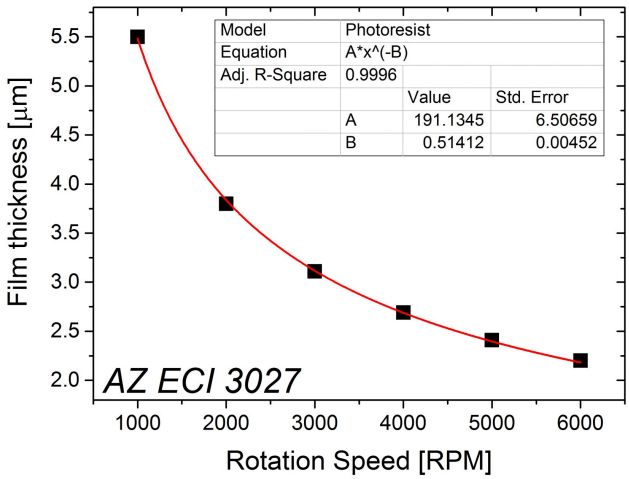


Figure 3.9: Spin curve for *AZ ECI 3027* [55].

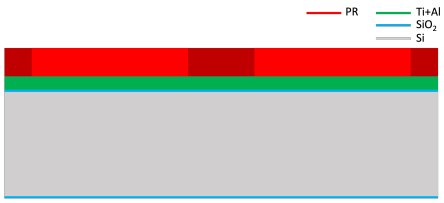


Figure 3.10: Wafer section after PR coating.

Initially, the design is converted into the *.gds* format, and the specific layers are selected for exposure through the application of logical operators (*or* or *cut*). Preceding the initiation of the exposure process, the design intended for use is shown, wherein the black pixels delineate the areas that will be exposed by the machine as shown in figure 3.11.
Being a positive resist, the exposed regions experience a chemical alteration, thereby increasing their solubility in the developer solvent. In contrast, the unexposed areas demonstrate unchanged and limited solubility.

During this phase, it is imperative to include the exposure of alignment marks (figure 3.12, as they play a crucial role in aligning the designs in the subsequent photolithography steps.

Following the conversion of the design, the machine necessitates the configuration of several parameters, including laser power (set at 100% since no

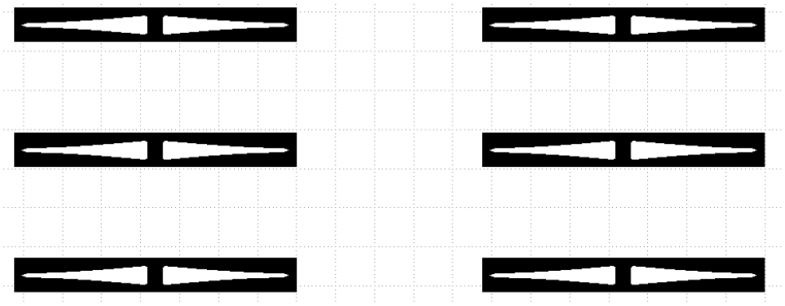


Figure 3.11: Design for Al photolitography.

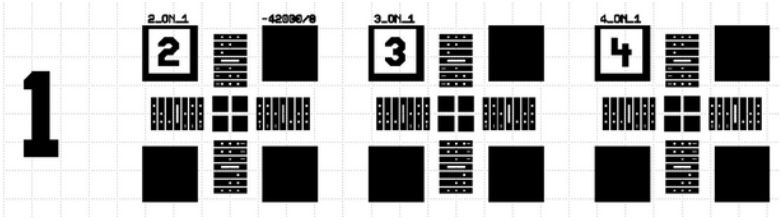


Figure 3.12: Alignment crosses for the first photolithography.

grayscale exposure is performed), laser wavelength, dose and defocus. The laser wavelength can be either 405 or 375 nm, determined based on the type of resist employed, with a similar consideration applied to the dose. The defocus parameter enables the adjustment of focus to center it within the resist instead of the top as shown in figure 3.13. A positive defocus (and this is the case) will move the focus downwards inside the resist and a step corresponds to a movement of approximately 600 nm [57].

The CMi staff supplies some tables containing recommended dose and focus values, contingent upon the type of resist employed. However, owing to the substantial influence of the exhibited design on these parameters, an initial dose test is imperative to ascertain the correct combination of dose and defocus. Consequently, guided by preceding tests, a dose of 400 mJ/cm^2 and a focus of +2 were established.
After placing the wafer on the *MLA150* holder, the machine conducts an edge detection to locate the wafer and a rotation detection. This preliminary step enables the selection of rotation correction before initiating the exposure, adjusting the design by the detected rotation angle.
Two distinct exposure modes are available for selection:

1. Fast exposure: Lower overlap of the exposure stripe;

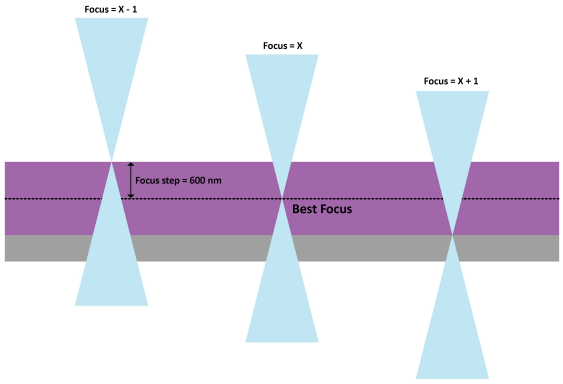


Figure 3.13: Effect of the defocus value. [57]

2. Quality exposure: Bigger overlap of the strip ($\approx$ 1.5x slower) [57].

In determining the exposure mode, several considerations were taken into account, specifically focusing on the resolution of the *MLA150* and the critical dimension of the design. The critical dimension, denoted as the width of a feature printed in resist at a specific height above the substrate [58], is approximately 3 μm at the tip, where the design tends to become more delicate. Given that the *MLA150* has a resolution of 1 μm, the decision was made to employ the quality exposure mode. This choice aims to prevent inaccurate exposure in specific areas of the wafer, ensuring precision, particularly in regions where the design is more intricate and susceptible to thinning.

3. **Photo resist development**

In the development phase, *ACS200* is employed once again. Preceding the actual development stage, a post-exposure bake is conducted, a step highly recommended for this particular type of photoresist. This bake, executed at 110°C for a minimum of 90 seconds with minimum proximity gap [55], serves to create a solubility differential between exposed and unexposed parts of the resist [59]. Following the bake, the authentic development process ensues, employing a combination of spray dispense and puddle development methods (figure 3.15). The recommended developer for AZ ECI 3027 is MF CD 26 (or AZ 726 MIF), an organic solution based upon TMAH [55]. This approach facilitates the dissolution of the exposed resist regions, yielding the final structures wherein the resist shields and safeguards certain areas from the subsequent aluminum etching process (figure 3.14).
Following the development process, the wafers undergo a thorough washing and drying procedure using a Spin Rinser and Dryer (SRD). This step is crucial for removing any developer residues on the backside of the wafer, as

these residues have the potential to cause clamping issues in subsequent steps. Before advancing to the etching phase, it is imperative to conduct an overnight baking of the resist at 85 °C using the *HeraEUS oven (HeraEUS, Germany)*. This process is designed to eliminate all traces of solvent from the resist, ensuring its thorough dryness. This meticulous preparation significantly enhances the accuracy and overall quality of the ensuing etching procedure.

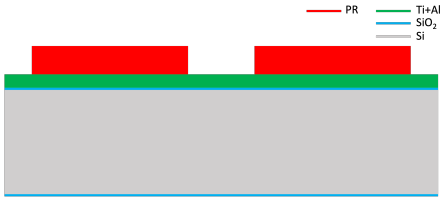


Figure 3.14: Wafer section after PR development.

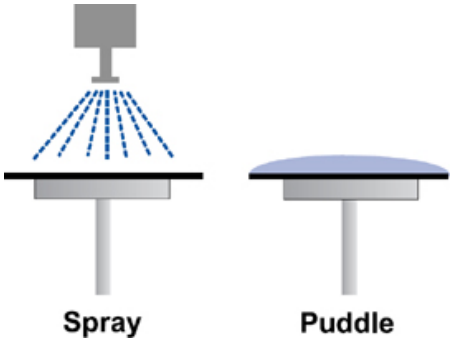


Figure 3.15: Illustration of spray dispense and puddle development method.

Aluminum etching

The *etching* term specifically denotes the selective removal of material through a reaction with chemically active radicals. In this specific application, dry etching is employed to etch all 4 μm of aluminum (figure 3.16). This method, known for being dry and clean, streamlines processes and enhances dimensional tolerances in semiconductor IC fabrication compared to traditional wet-chemical etching [60]. The aluminum etching is executed with the *Cobra PlasmaPro100* by *Oxford Instruments, UK*. This equipment provides a broad range of material etching options utilizing high-density plasma of the ICP (Inductively Coupled Plasma) type. Chlorinated gases are popular for efficient aluminum etching. Nonetheless, the etching process for aluminum faces a challenge posed by its inherent aluminum oxide layer, providing protection against gases like Cl_2, Br_2 and HCl, rendering them ineffectual in aluminum removal. BCl_3, along with its plasma-generated fragments

efficiently eliminate oxygen and water vapor. Consequently, the plasma chamber can contain significant amounts (a few percent) of oxygen without hindering aluminum etching. In fact, minimal oxygen quantities enhance the plasma etch rate of aluminum in BCl_3. Therefore, gas mixtures for aluminum etching commonly include BCl_3 to assist in scavenging oxygen and water vapor [60].

Considering the substantial thickness requiring etching, the selected recipe among

Material to etch	**Process name**	**Mask**	**Etch rate (nm/min)**	**Chemistry**
Al Ti TiN	Al_Ti_TiN_etch	PR	Al 340 Ti 250 PR 300	Cl_2/BCl_3
Al Ti TiN	Al_etch_w-breakthrough	PR	Al 510 PR 250 SiO_2 50	BCl_3 (BT) Cl_2 (main)
Si	Si_etch	PR SiO_2	Si 370 PR 430 DUV42P 120	Cl_2
SiO_2 Si_3N_4	SiO_2_Si_3N_4_etch	PR	SiO_2 175 Si 220 PR 332	CF_4
SiO_2 Si_3N_4	SiO_2_Si_3N_4_RIE	PR	SiO_2 45 Si 55 PR 25	CF_4/Ar
Polyimide	PI_etch_O_2-Ar	SiO_2	PI 2'550 SiO_2 20	O_2/Ar

Table 3.6: List of etching recipes for *PlasmaPro100 Cobra* [61].

the available ones (table 3.6) is `Al_etch_w-breakthrough`. This selection is based on its notable etching rate (510 nm/min) and high selectivity towards photoresist, ensuring that only 490 nm of photoresist is removed for every micron of aluminum etched.

After aluminum etch, corrosion is an issue because of trapped Chlorine (a corrosive gas) at patterns' sidewalls: HCl creation will locally initiate as soon as the sample is at atmosphere and in contact with ambient humidity. In order to avoid slow corrosion of the Aluminum, it is necessary to get with no delay the wafers rinsed in a high volume of DI water. This will force create HCl but will dilute it right away from the wafers.

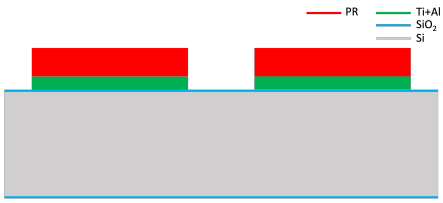


Figure 3.16: Wafer section after Al etching.

Photo resist stripping

The process then advances to photo resist stripping, involving the removal of any lingering PR layers from the wafer surface (figuree 3.17).

Figure 3.17: Wafer section after PR stripping.

This task is accomplished through the utilization of two machines: *GiGAbatch (PVA TePla America, LLC, California)* that uses O_2 plasma, and the *UFT Resist wetbench*. This combination ensures a thorough and comprehensive resist-stripping process.

1. *TePla GiGAbatch*
   The Tepla GiGAbatch employs high-frequency oxygen plasma to assist in the removal of photoresist, generating perforations in the resist and thereby enhancing the effectiveness of the subsequent remover application. Users have the option to select between two modes: high power and low power.

   - **Resist Strip High Power/Flow**

     - Power: 600 W
     - O_2 flow: 400 sccm
     - Pressure: 0.8 mbar
     - Uniformity: 20% to 30% depending on process time

Positive resists etch rate 250 nm/min to 1.2 μm/min depending on process time (tool heating up) and the number of wafers to be processed in the batch (chemical "loading").

- **Resist Strip Low Power/Flow**

  - Power: 200 W
  - O_2 flow: 200 sccm
  - Pressure: 0.5 mbar
  - Uniformity: 20% to 30% depending on process time

  Positive resists etch rate 100 nm/min to 500 nm/min depending on process time (tool heating up) and the number of wafers to be processed in the batch (chemical "loading") [62].

2. *UFT Resist wetbench*

The UFT wet bench comprises four sequential baths, culminating in a Spin Rinser Dryer dedicated to the drying of wafer, as shown in figure 3.18. In the initial two baths, Remover 1165 is employed for five minutes, and the solution is heated to a minimum of 70°C to enhance its effectiveness. The third bath serves as a rapid Dump Rinse, facilitating the removal of any remaining Remover residue. The fourth bath operates as a cascade tank, ensuring thorough and precise rinsing of the substrate. Finally, the Spin Rinser employs a Dry-only recipe, leaving the substrate ready for subsequent fabrication steps.

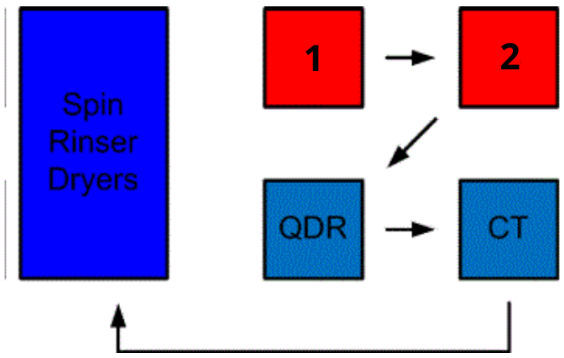


Figure 3.18: UFT Resist wetbench sequence: 1 & 2: baths of REM1165 at 70°C (min); QDR: Quick Dump Rinse (rough rinsing); CT: Cascade Tank (fine rinsing) [63].

3.3.3 SiO_2 layer - Frontside

Until this stage in the process flow, the aluminum component has been exclusively situated within the shanks of the microelectrode. Consequently, it is advisable to proceed with the application of a SiO_2 layer (1μm to ensure insulation for the frontside structures. This layer will selectively expose only the tip (dedicated to stimulation) and the portion of the shank overlapped with the pad: in this specific region, aluminum will remain uncovered. As elucidated in the preceding section, the notable conductivity of aluminum is pivotal, as in this case it facilitates the connection of this microelectrode segment with wires, a critical aspect for enabling communication between the brain and the external environment.

$Si0_2$ deposition

The deposition of SiO_2 (figure 3.19) was carried out utilizing plasma-enhanced chemical vapor deposition (PECVD) at elevated temperatures with the *Corial D250L (Plasma-Therm, United States)* system.

Figure 3.19: Wafer section after SiO_2 deposition.

Given the high temperature employed in this process, it is imperative to ensure the complete removal of photoresist prior to SiO_2 deposition.
Chemical vapor deposition is renowned for its commendable step coverage; however, it is noteworthy that the growth temperature typically exceeds 800 °C. Consequently, the adoption of PECVD becomes imperative in order to reduce the deposition temperature while maintaining both optimal step coverage and deposition rate [64]. In terms of deposition precursors, various gas combinations containing silicon and oxygen are applicable for achieving the desired SiO_2 deposition. PECVD utilizes plasma to enhance the chemical reactions of precursor gases, depositing a thin film on the exposed wafer surface. The plasma is generated through radio-frequency (RF) alternating current discharge between two electrodes. Its presence ionizes the precursor gases, forming reactive species that interact with the substrate's surface. These species undergo chemical reactions, resulting in the formation of a solid, thin film. The remaining gaseous byproducts are removed through the pumping line. This meticulous approach ensures precision and reliability in the fabrication process. The *Corial D250L* comes with an optical emission spectrometer (OES) dedicated to end-point detection (EPD). The primary role of EPD is to autonomously conclude

in-situ plasma cleaning, ensuring reactor cleanliness and avoiding an unnecessary increase in its temperature.

Throughout deposition processes, the OES spectrometer can function in interferometry mode, allowing for the supervision of film thickness and the automatic cessation of deposition upon achieving the desired thickness [65].

Among the suggested recipes (table 3.16), `A_SiO2_Fast` is employed due to its elevated deposition rate and the minimal stress it imparts on the wafer. The deposition time is computed by dividing the desired thickness by the deposition rate, yielding a brief duration of only 2 minutes and 28 seconds.

$$t_{SiO2} = \frac{1000\,\text{nm}}{405\,\text{nm/min}} = 7\,\text{min} \quad 28\,\text{s} \tag{3.2}$$

Recipe Name	**Film**	**Dep. Rate [nm/min]**	**n @ 677 nm**	**Unif [%]**	**Stress [MPa]**
A_SiO_2_Fast	SiO_x	405	1.47	0.5	-190
A_SiO_2_High_Density	SiO_x	22.7	1.47	0.5	-318
A_Si_3N_4_Fast	Si_xN_y	191.2	2	1.9	+24
A_Si_3N_4_High_Density	Si_xN_y	57.6	1.97	0.6	-100
A_a-Si:H	a-Si:H	69	3.74	0.6	-280
A_SiC	SiC	30	2.68	1.36	-328
A_aC	a-C	35.6	1.88	2.2	-242

Table 3.7: List of PECVD deposition recipes for *Corial D250L* [65].

Alternatively, SiO2 deposition using sputtering (*Spider 600*) could have been employed, requiring approximately 17 minutes (deposition rate = 58 nm/min). This is approximately seven times longer compared to the PECVD method.

Photolithography

During the photolithography steps (figure 3.21), the deposition and isolation of photo resist occur in regions where SiO_2 is intended to be retained, as it will undergo etching in areas lacking PR protection.

Photo resist coating

Regarding the coating process, the same equipment, resist, and thickness as before are utilized. The procedural steps remain consistent, with the only variation being

in surface preparation, involving *HMDS Vapor*. This adjustment is necessary due to the altered surface material, transitioning from aluminum to SiO_2.

Exposure

The subsequent exposure phase is conducted using the maskless aligner *MLA150* to replicate the design involving the aforementioned rectangle, the SiO_2 layer, and partially mentioned alignment marks (figure 3.20).

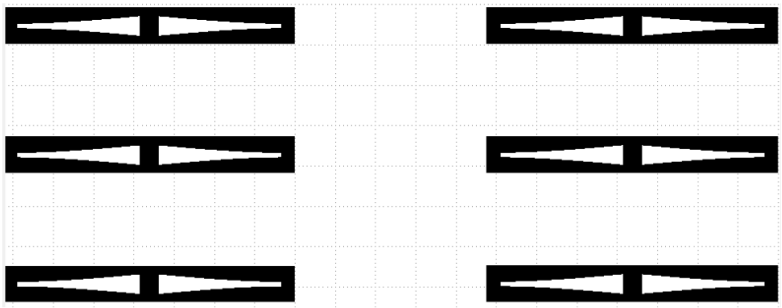


Figure 3.20: Design for SiO_2 photolitography.

In this scenario, given that it is not the initial exposure, it becomes imperative, as part of the preparation for the upcoming exposure, to execute an alignment procedure ensuring the accurate alignment of the first and second layers. During this phase, the coordinates of the alignment markers, exposed in the first photolithography, are initially inputted (x=42000 μm and y= 0 μm for marker 1, and x=-42000 μm and y=0 μm for marker 2). Subsequently, the *MLA150* camera is positioned at the cross points, proposing an automatic alignment, which, however, necessitates user confirmation. This approach allows for the assessment of the deviation between the actual and theoretical positions of the markers by implementing a rotation correction, typically on the order of ten mrad. Indeed, the alignment marks serve not only for alignment confirmation but also to gauge its success. A correct alignment manifests as an external cross (imprinted during the second photolithography) enclosing a smaller cross, the one imprinted during the initial photolithography.

The exposure parameters remain identical to the previous step, and the exposure time is approximately the same, given the minimal design alterations from the aluminum configuration, primarily involving the trimming of the two sides of the shanks.

Photo resist development

The development process remains consistent with the preceding photolithography step, and the wafer undergoes washing and drying using a centrifuge.
In this instance, it is recommended to undertake an overnight bake at 85°C, a practice previously applied to aluminum.

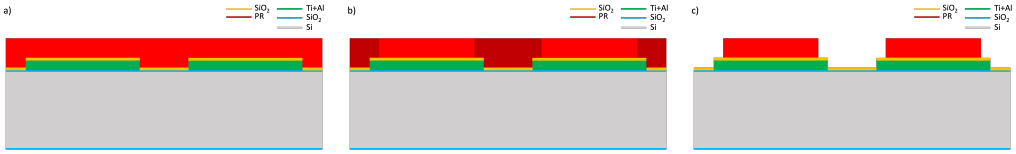


Figure 3.21: Wafer section after: a) PR coating; b) Exposure; c) PR development.

SiO_2 etching

Now that photo resist is located only in the wanted areas, one can proceed with SiO_2 etching (figure 3.22), performed using *SPTS APS (SPTS Technology, UK)*, an ICP-based high density plasma source. This system was optimized for etching dielectrics (e.g. SiO_2, Si_xN_y, SiC, Al_2O_3, glass types...) which pose challenges for conventional reactive ion etching (RIE) or ICP sources [66].
The choice of the SiO_2 etching recipe is guided by careful consideration of the etching selectivity between SiO_2 and the photo resist, as well as the desired etched thickness and the thickness of the resist acting as a mask. In this particular scenario, where the objective is to etch 1 μm of SiO_2 with a 5 μm layer of photoresist to protect specific areas of the wafer from etching, there are no restrictive criteria influencing the selection of the etching recipe. Hence, a recipe with a SiO2:PR selectivity of 3:1 was chosen as the most effective option.

Material	SH Temp (°C)	Process Name	Chemistry	Mask Material	Etch Rate (nm/min)
SiO_2 Si3N4	10	SiO_2_PR_3:1	$C_4F_8/H_2/He$	PR ZEP/CSAR	WetOx: 380 Si_3N_4: 255 SiN LS: 190 Si: 35 ZEP / CSAR: 130

Table 3.8: SPTS APS recipe used for SiO_2 etching [66].

The targeted etch thickness for SiO_2 is 1.2 μm, aiming to remove the additional 200 nm of SiO_2 resulting from the initial Wet Oxidation process, thereby exposing bare silicon in the pad region.

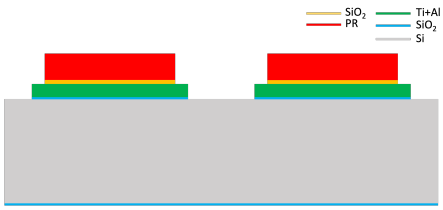


Figure 3.22: Wafer section after SiO_2 etching.

The calculation of the etching time is given in the formula 3.3:

$$t_{SiO2} = \frac{1200\,\text{nm}}{380\,\text{nm/min}} = 3\,\text{min} \quad 10\,\text{s} \tag{3.3}$$

Nevertheless, in the machine preparation phase, the etching time was extended to 3 minutes and 30 seconds. This adjustment was made to incorporate end-point detection and execute a final over-etching step, thereby guaranteeing the complete and uniform removal of the SiO_2 layer at the specified locations. This approach aims to minimize any disparity between the center and the edges of the wafer.
Prior to advancing to subsequent stages, *Filmetrics-F54 XY-200 (Filmetrics a KLA Company, US)* was employed to verify the thorough removal of the SiO2 layer from the targeted areas. *Filmetrics F54* is employed to precisely measure the thickness of thin films, encompassing both dielectric and inductive materials, ranging from 4 nm to 115 µm. This measurement is conducted through spectral reflectometry, utilizing either a highly accurate mapping technique or by assessing random points across the entire surface of the wafer. When light interacts with the boundary between two materials, a portion of it is reflected. The wave-like nature of light causes reflections from multiple interfaces ($\varphi 1$, $\varphi 2$) to interfere, leading to oscillations in the reflected light spectrum (figure 3.23). By analyzing the frequency of these oscillations, we determine the distance between different interfaces, providing the thickness (d) of the thin film – an increased number of oscillations indicating a greater thickness. Additionally, various material characteristics such as refractive index and surface roughness are assessed.

In the analysis of spectra, our FILMapper software employs two distinct modes: Spectrum-Matching and FFT. The Spectrum-Matching mode enables the analysis of both thickness and refractive index, while the FFT mode is dedicated solely to thickness analysis, and is often considered more robust for thicker films [67].

If Filmetrics F54 yields results indicating the presence of SiO_2, it is necessary to repeat the etching process. The duration of etching should be determined based on the measured thickness of SiO_2 and the etching rate. Once SiO_2 has been effectively removed, the subsequent step of stripping can be carried out.

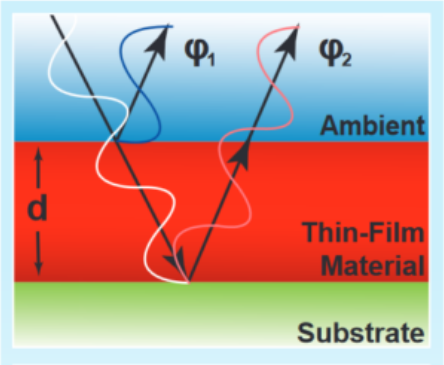


Figure 3.23: *Filmetrics F54* working principle [67].

Photo resist stripping

The stripping process is executed using the same method as previously described: a combination of O_2 plasma with *TePla* and 20 minutes in the *UFT Wet bench*, heated to a minimum of 70 °C.

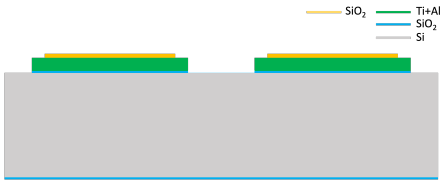


Figure 3.24: Wafer section after PR stripping.

3.3.4 Grinding - Backside

Having concluded the front side processes, the subsequent phase involves a precision grinding step. This meticulous grinding endeavor aims to diminish the wafer's thickness by 150 μm, strategically mitigating potential aspect ratio challenges during the subsequent silicon backside etching, which assumes critical importance, particularly due to the narrow 70-30 μm trench and the substantial depth of etching required.

CMi provides grinding services using the *DAG810 (Disco, Japan)*, an automatic and compact grinder capable of efficiently grinding various materials, including Si and SiO_2. Given the presence of a 200 nm layer of SiO_2 deposited during wet oxidation on the backside, the grinding process focuses on removing this SiO_2 layer along with approximately 150 μm of silicon to achieve a final silicon thickness of 230 μm. The wafers are affixed to a rotating chuck table, where a diamond wheel

in motion sweeps across its center (figure 3.25). A descending spindle with the wheel removes material from the wafers surface.

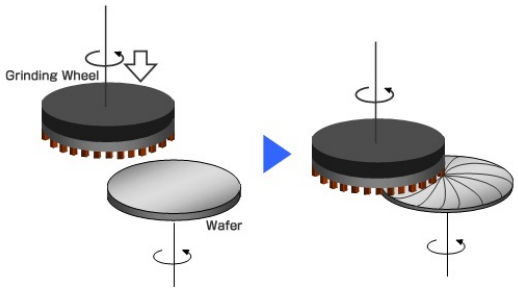


Figure 3.25: Grinding mechanism [68].

Water is utilized for cooling and clearing debris during the grinding process. Initially, wafer edges exhibit a rounded shape, but as they are ground, these edges acquire a sharp form (figure 3.26), resulting in diminished mechanical strength: the cooling water and grinding conditions in this weakened edge area may pose a risk of breakage. To prevent damage to the edge area, acceleration at the chuck table rotation speed and deceleration at the spindle rotation speed are employed [68].

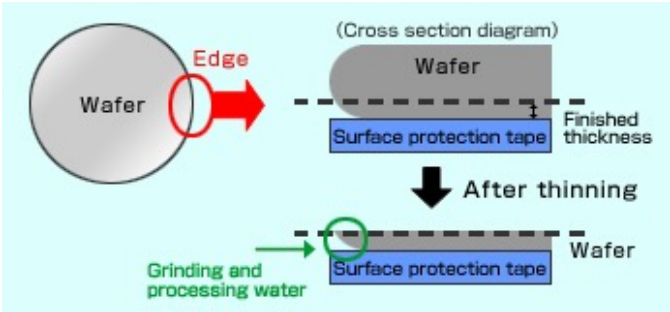


Figure 3.26: Edge thinning outline [68].

During the grinding process, it is imperative to note that the wafer is secured on its front side. Given the highly aggressive nature of the grinding action, precautionary measures become essential. In this regard, the utilization of protective elements, such as UV-tape (considered the standard choice) or a suitably thick layer of photo resist, is recommended. These protective measures aim to mitigate the risk of damage to the front side of the wafer.

- UV-tape:
  UV tape serves as an adhesive tape extensively employed for safeguarding the wafer surface during various processes, including dicing and grinding.

Additionally, it is used to shield one side of the wafer to prevent any impact during specific procedures such as Parylene deposition. The composition of UV tape includes a Polymer Base, Oligomer, and Photo Initiator. Notably, its adhesive capacity diminishes upon exposure to UV light, as illustrated in the accompanying figure. This reduction in adhesive strength occurs because the oligomers undergo a polymerization reaction, forming a cross-linked structure upon UV irradiation. Consequently, the adhesive undergoes a hardening process, leading to a decrease in adhesive strength [69]. Nevertheless, it is not recommended to use UV tape in situations in which the design of the front side imposes significant mechanical stress during the UV-tape removal. This is particularly relevant in cases involving tall and narrow structures, such as the one under consideration, as it may result in the breakage of the wafer.

- Photo Resist:
  To address the mentioned issue, a potential solution involves substituting the UV-tape with a thick layer of photo resist. This alternative ensures the protection of the front side, and the removal process does not involve mechanical means. Instead, it follows the standard UFT remover stripping method, which is a chemical process that avoids inducing stress on the wafer. Nonetheless, this procedure carries inherent risks. In cases where the adhesion of the photor esist is insufficient, there exists a potential hazard of wafer detachment during the grinding process.

- UV-tape + Photo Resist:
  The best solution, in the case of complex designs, is a combination of UV-tape + photo resist. In this case, the thick layer of photo resist will make the surface flatter, reducing the stress generated during its removal.

Post-grinding etching

Post-grinding, the wafers surface is invariably altered and can be categorized into various zones. The first zone displays roughness associated with the utilized wheel. The second zone, typically 2 μm to 10 μm thick, contains micro-cracks inducing stress in the workpieces. Subsequently, a zone with crystal dislocations is observed before the material reverts to its typical arrangement. Surface roughness can be minimized, and stress induced by micro-cracks can be alleviated by removing a few microns of material using dry or wet etching or polishing techniques [68].
To alleviate stress produced during grinding and enhance the purity of the backside surface, an etching process of a few microns of silicon on the ground surface was chosen. This specific step can be executed using either the *SPTS Rapier (SPTS Technology, UK)* or the *Cobra PlasmaPro100 (Oxford Instruments, UK)* machines, both serving the same purpose.

- *SPTS Rapier*
  By choosing the `Si_thinning` recipe, *SPTS Rapier* enables isotropic silicon etching with a uniformity of ±3.5% and an etching rate of approximately 4.4 μm/min, employing SF_6-based chemistry [70]. In this particular recipe, the sole adjustable parameter is the etching time, currently set at 2 minutes. This duration results in an additional etching of about 9 μm, crucial for relieving the mechanical stress induced during grinding, with potential adverse effects if not addressed.

- *Cobra PlasmaPro100*
  When utilizing the Cobra machine, it is imperative to execute this procedure in two distinct steps:

  1. Implement the `STS-Pyralin` process for 1 minute, wherein O_2 is employed to cleanse the surface of ground silicon.
  2. Implement the `STS-W-etch` process for 5 minutes, facilitating an SF_6 etch of silicon to alleviate stress.

  These specific procedures derive from the predecessor machine of Cobra, the *STS Multiplx ICP (Surface Technology Systems, UK)*, and are characterized by the key features outlined in the subsequent table.

Material to etch	**Process name**	**Mask**	**Etch rate (nm/min)**	**Chemistry**
Polyimide	STS-Pyralin	SiO_2	»1	O_2
W	STS-W-etch	PR	0.5	SF_6

Table 3.9: Selected recipe for post-grinding etching on *PlasmaPro100 Cobra*

  In this scenario, the etched thickness measures approximately 2.5 μm, indicating a significantly reduced thinning [71].

3.3.5 SiO_2 deposition - Backside

The primary step in backside processing entails depositing 1 μm of SiO_2 (figure 3.27) through PECVD at 320 °C, employing the identical procedure outlined in section 3.3.3 with *Corial D250L* and recipe `A_SiO2_Fast`. In this instance, the SiO_2 layer serves as a hard mask for the subsequent deep etching of silicon, which will create the design of the probes on the backside.

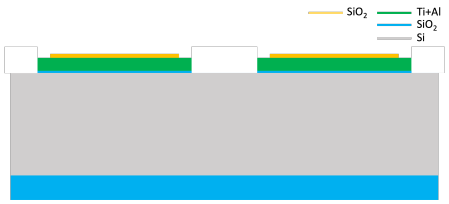


Figure 3.27: Wafer section after SiO_2 deposition.

To achieve a deposition of 1 μm of SiO_2 with a deposition rate of 405 nm/min, the deposition time is equal to 2 minutes and 28 seconds, computed using the following formula 3.4:

$$t_{SiO2} = \frac{1000\,\text{nm}}{405\,\text{nm/min}} = 7\,\text{min} \quad 28\,\text{s} \tag{3.4}$$

3.3.6 Parylene coating - Frontside

Before commencing the backside processing, the front side structures were safeguarded with a 5 μm layer of Parylene, one of the most commonly employed polymers in CMOS fabrication. This precautionary measure was taken to shield the front side structures from potential damage during the subsequent backside steps, where the front side is clamped and maintained in close contact with the support in different machines.
Since Parylene-C melting temperature results to be 290 °C [72], it is impractical to execute this step before depositing SiO_2 on the backside, as PECVD is carried out at 320 °C, posing the risk of Parylene melting. Consequently, owing to the inherent incompatibility of Parylene with PECVD processes, the initial backside step is undertaken without the protection of the front side structures.

Parylene coating

Parylene coating is a service offered by CMi involving the use of *Comelec C-30-S* machine by *Comelec SA, Switzerland*, allowing users to select from a range of available thickness options: 50 nm; 100 nm; 200 nm; 500 nm; 1 μm; 2 μm; 2.5 μ; 3 μm; 5 μm; 7 μm; 10 μm

Parylene deposition occurs in a vacuum chamber at room temperature (few µbar pressure). The raw material, initially a solid dimer, undergoes vaporization by heating at around 150 °C. It transitions to a vapor phase, then diffuses to a pyrolysis chamber at 670 °C, where it dissociates into a monomer. The monomer subsequently diffuses to a process chamber maintained at room temperature or

slightly heated (80 °C), condensing to form the Parylene layer. Residual monomers are captured in a cryogenic device before pumping.

The thickness of the Parylene layer is contingent on the solid load placed in the vaporization boat. Factors such as total surface area and arrangement within the processing chamber influence layer thickness and uniformity. On a 100 mm silicon wafer scale, the layer exhibits uniformity of less than 1%. To prevent Parylene deposition on one side of the wafer, UV-tape can be applied to cover the undesired side. This ensures that Parylene adheres to one side of the wafer while attaching to the UV-tape on the other side. Subsequently, after removing the UV-tape along with the deposited Parylene layer, an unaffected side is revealed. In situations where the use of UV-tape is to be avoided (and this is the case), Parylene coating is performed on both sides of the wafer (figure 3.28) and then it is removed from the backside at a later stage. Due to the deposition mechanism, achieving uniform deposition on both sides is impractical. This limitation arises from the support structure during coating, where the wafer is held by three pins, effectively preventing coating in the area they occupy. Therefore, if coating is applied to both sides, only one side will exhibit uniform coating, while the other will have three small holes as a result of the pins placement. In this scenario, to ensure uniform frontside protection, the pins were strategically positioned on the backside.

Figure 3.28: Wafer section after Parylene-C coating.

Parylene etching - Backside

The process of Parylene etching (figure 3.28) on the backside involves utilizing O_2 plasma with the *PlasmaPro100 Cobra* machine. The chosen recipe is `STS-Pyralin`, and the key parameters are detailed in the following table 3.10.

Material to etch	**Process name**	**Mask**	**Etch rate (nm/min)**	**Chemistry**
Polyimide	STS-Pyralin	SiO_2	»1	O_2

Table 3.10: Selected recipe for Parylene etching on *PlasmaPro100 Cobra*

Figure 3.29: Wafer section after Parylene-C etching on backside.

O_2 plasma effectively removes Parylene, leveraging a principle similar to the one employed in *TePla* for photo resist stripping, while ensuring no damage to the underlying layers. The existence of "naked" SiO_2 in the regions where the pins were positioned, devoid of Parylene, does not pose a problem as O_2 exclusively targets Parylene.

An additional advantage lies in the ability to set an adequately extended etching time and terminate the process based on end-point detection. The Cobra laser plays a crucial role in this aspect by assessing material reflectivity using a wavelength of 670 nm. If Parylene is present, the detected signal exhibits a sinusoidal pattern due to the laser penetrating the Parylene layer. However, once the Parylene is completely etched away, the signal becomes flat as the laser encounters no layer, indicating the thorough removal of Parylene.

3.3.7 SiO_2 layer - Backside

First Photolithography - Backside

With the front-side structures now fully shielded to prevent damage in the final stages of the process flow, it is possible to proceed with the initial backside photolithography. This step impacts the previously deposited SiO_2 layer and seeks to establish an SiO_2 hard mask that will play a crucial role in the subsequent stage, where the silicon is slated for etching.

1. **Photo resist coating**:
   For the first backside photolithography, given the high selectivity of SiO_2:PR during etching, a single micron of photoresist is sufficient to achieve the desired aim. In this case, the chosen resist is AZ ECI 3007 coated using the *ACS200*. Since the coating needs to be applied to a SiO_2 layer, the recommended surface preparation is Vapor HMDS, improving adhesion between the resist and the underlying layer. Additionally, in the final stage of the coating, edge bead removal with a backside rinse option is performed to eliminate residual resist on the edge and backside of the resist.

2. **Exposure**:

During the exposure phase, the *MLA150* with 405 nm laser source is used to expose the parts of resist that will later be removed during development, making that portion of the wafer vulnerable to the gases used during etching. The exposed design is confined to the rectangular region, where SiO_2 will be entirely removed (figure 3.30. Within this area, the silicon thickness will be reduced by up to 30 μm, adhering to a precise design outlined during the second photolithography.

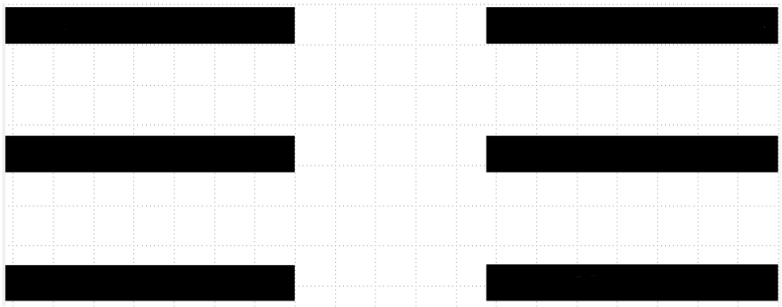


Figure 3.30: Design for SiO_2 photolitography.

A crucial aspect during the initial backside exposure involves aligning the front side with the backside. In this first photolithography, achieving proper alignment is imperative to ensure the accurate positioning of the backside design in relation to the front side. To facilitate subsequent backside photolithographies, alignment markers on the backside are also exposed. The front-to-back alignment process employs a specialized camera known as "backside camera". While aligning, the infrared camera captures a real-time low-resolution image of the design on the front side. The provided theoretical coordinates of the markers are then compared with the actual coordinates determined during this phase. This comparison allows for the evaluation of the wafer's rotation and ensures alignment consistency between the front and backside designs. Since the wafer is positioned with the backside facing up and the alignment markers are on the front side, their coordinates are mirrored along the x-axis due to the rotation around the y-axis. The first marker is located at x = -42000, y = 0, and the second marker at x = 42000, y = 0. Consequently, due to the rotation around the y-axis, it becomes essential to mirror the design along the x-axis, given that the design is not centered at (0,0). The critical nature of this step stems primarily from the low resolution of the backside cameras, which may pose challenges in accurately identifying the markers.

3. **Photo resist development**
   Development is performed again using *ACS200*, with the same procedure

mentioned for the other photolithographies. Following development, the photoresist will cover the entire wafer surface, providing protection during etching, except for the designated rectangle area where the SiO_2 will be selectively removed.

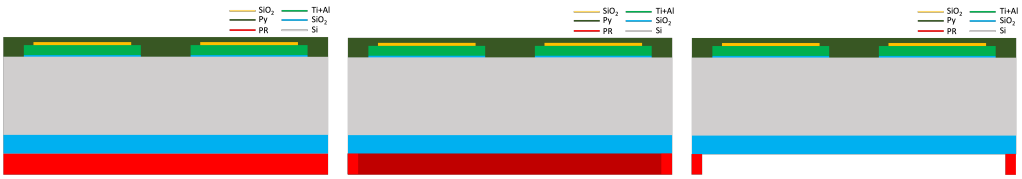


Figure 3.31: Wafer section after: a) PR coating; b) Exposure; c) PR development.

SiO_2 etching

The SiO_2 etching process occurs within the rectangle, where the front-side structures are situated, utilizing the *SPTS Advanced Plasma System (APS) (SPTS Technology, UK)*, an ICP-based high-density plasma source. This system is specifically designed for etching dielectrics, a task that can be challenging with conventional RIE or ICP sources [73].

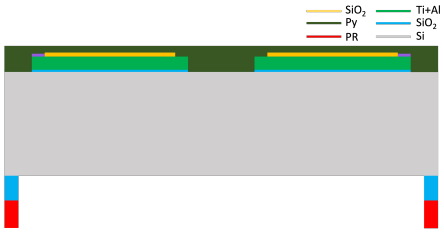


Figure 3.32: Wafer section after SiO_2 etching.

Given the similar thicknesses of the SiO_2 to be etched and the photoresist (PR) mask, careful consideration is required when selecting the etching recipe. Ensuring that the PR is not completely removed, even in the over-etching phase, is crucial. Consequently, the chosen recipe exhibits a SiO_2:PR selectivity of 3:1. This signifies that, following the complete etching of SiO_2, approximately 0.7 μm of PR will remain. The parameters associated with the selected recipe are outlined in the following table 3.11

The duration of the etching process is determined using the following formula 3.5:

$$t_{SiO2} = \frac{1000\,\text{nm}}{320\,\text{nm/min}} = 3\,\text{min} \quad 8\,\text{s} \tag{3.5}$$

Material to etch	Process name	Mask	Etch rate (nm/min)	Chemistry
SiO_2, Si_3N_4	SiO_2_PR_3:1_SOFT	SiO_2	WetOx: 320 Si_3N_4: 70 SiN LS: 60 Si: 35	C_4F_8/He

Table 3.11: Selected recipe for SiO_2 etching on *SPTS APS*

However, considering the potential variation in etching rates due to various factors and the imprecise knowledge of the exact thickness of the SiO_2 layer, the initial etching time is conservatively set at 3 minutes and 30 seconds. The process is then halted using endpoint detection, introducing an over-etching phase that corresponds to approximately 7% of the total time. This approach aims to achieve a more uniform etching across the entire wafer surface.

Photo resist stripping

To remove the photo resist mask post SiO_2 etching, a combination of dry and wet treatments is employed:

1. Initiate an oxygen plasma treatment using the *Tepla GiGAbatch*.
2. Proceed with a wet remover treatment using the *UFT wetbench*.
3. If needed, conduct a secondary treatment with the *Tepla GiGAbatch* to eliminate any remaining residues.

Figure 3.33: Wafer section after PR stripping.

3.3.8 Second photolitography - Backside

The objective of the second photolithography is to imprint the backside design of the probes onto the wafer.

1. **Photo resist coating**:
   For the photolithography on silicon surface, 2 μm of resist are used, given the substantial amount of silicon to be etched. *ACS200* is used to coat the defined thickness of AZ 10XT-20, a high-performance resist recommended for dry etching and not requiring overnight stabilization.

2. **Exposure**:
   The exposure is performed using the *MLA150* with 405 nm laser. In this photolithography step, the alignment marks exposed in the preceding photolithography process are employed to align the design of the backside probes. In contrast to the backside camera, the conventional camera is utilized in this instance, making the identification of markers less challenging owing to its higher resolution. The exposed design comprises a 250 · 250 μm pad and two shanks, featuring three distinct configurations, stemming from prior considerations regarding mechanical stress and positioned separately from the pad (figure **??**). The trench dimensions range from 73.5 to 79.5 μm for one wafer and from 33.5 to 39.5 μm for other wafers. This arrangement facilitates backside silicon etching in the shank region adjacent to the pad, enabling controlled bending.

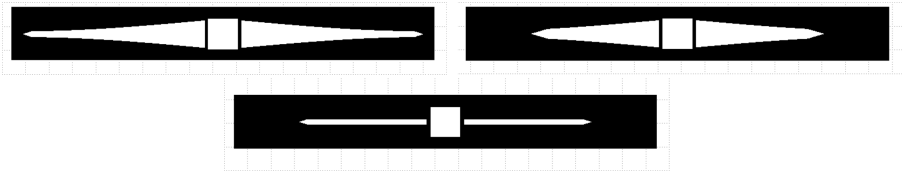


Figure 3.34: Overview of the silicon backside design.

3. **Photo resist development:**
   For this particular type of resist, recommended developer is AZ 400K, a KOH organic solution that gurantees sharper edge profile, diluited in water with volume ratio 1:3.5. Development with *ACS200* combines spray and puddle methods with intermediates spin-clean steps. No Softbake is applied in order to preserve vertical PR side walls [74].

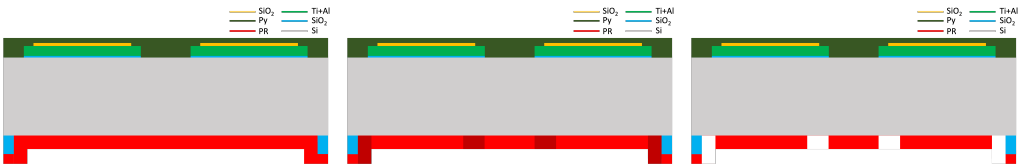


Figure 3.35: Wafer section after: a) PR coating; b) Exposure; c) PR development.

3.3.9 Deep silicon etching - Backside

The trench value assumes significant importance as it directly influences the ultimate thickness of silicon. Defined as the distance between the shank and the pad, maintaining a final silicon thickness less than or equal to this value becomes imperative. This ensures that the backside silicon etching process does not impede the bending of the probes.

To achieve a specific silicon thickness of approximately 30 or 70 μm at both the pad and shanks, with a complete absence of silicon in the other regions within the rectangle to facilitate probe detachment, a two-step silicon etching process is essential.

First deep silicon etching

The initial deep silicon etching on the backside utilizes a photo resist mask and aims to remove silicon in an amount precisely aligned with the trench value (figure 3.36).

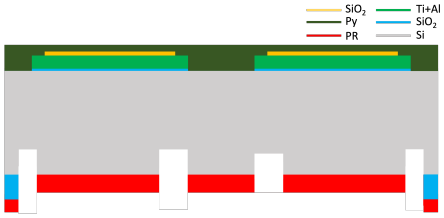


Figure 3.36: Wafer section after first deep silicon etching.

This approach allows for the precise determination of the thickness difference between the pad and the fins. Subsequently, the entire remaining silicon can be effectively etched in the subsequent etching phase. The *SPTS Rapier (SPTS Technology, UK)*, an optimized Deep Reactive Ion Etching (DRIE) system designed for Silicon and Silicon on Insulator wafers, is employed in this step. This system facilitates a high-performance Bosch process, which is an anisotropic dry etching technique. The Bosch process achieves deep structures with vertical profiles through a sequence of three distinct steps: film deposition, bottom film etching, and silicon etching (figure 3.37).

- **Film deposition**:
  The passivation phase involves depositing a fluorocarbon-based protective film on the sidewalls and base of the trench. This film provides protection throughout the etching phase and ensures the creation of a vertical profile.
- **Bottom film etching**:
  In this subsequent phase, the passivation film undergoes etching at the bottom

of the trench using O_2 plasma, exposing this area to the etching process while still safeguarding the sidewalls, defining the anisotropic characteristics of the etch profile.

- **Silicon etching**:
  In the final stage of the cycle, the silicon exposed at the trench base undergoes etching, employing gases like SF_6. Throughout the etching process, a portion of the polymeric sidewall material, deposited in prior steps, is removed from the sidewall due to off-vertical ion impacts.

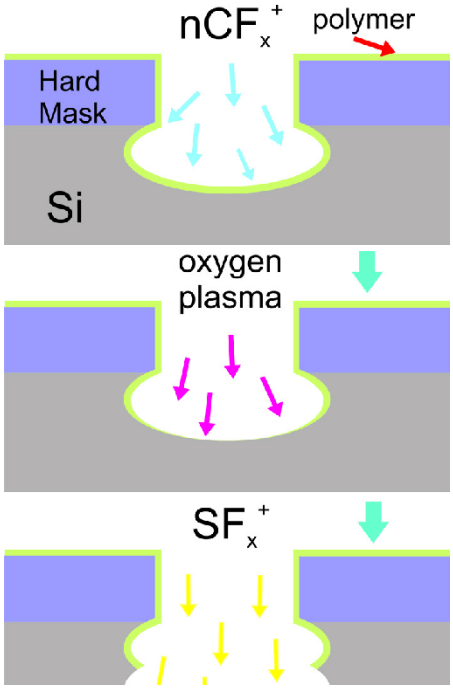


Figure 3.37: Overview of Bosch process steps [75].

These three steps are iterated through multiple cycles, progressively depositing the passivation film deeper. This progress ensures a local anisotropy in the etching that would otherwise be nearly completely isotropic. Consequently, only a slight lateral roughness persists as an indication of the discontinuous process [76]. In the process of deep silicon etching, which consists of two distinct phases - passivation and etching, the critical parameter to be configured is not the etching time but rather the number of cycles. This is done to prevent terminating the etching process during the passivation phase, which would result in an oscillating etching rate. While there are tables available that provide an estimate of the etching rate based on the number of cycles and trench dimensions, due to a significant dependence on the specific design, it is advisable to approach the etching process conservatively.

The preferred method involves conducting iterations, inspecting the wafer with a profilometer or a standard microscope at each stage, and determining the variations in etching rates.

Trench (μm)	Etching Rate (μm/loop)		
	100 loops	200 loops	300 loops
2	39	68	92
5	47	83	112
10	54	97	133
20	62	113	155
50	70	133	186
100	74	143	206
200	76	147	217
500+	78	149	223

The procedure for the initial deep silicon etching includes an initial descum phase utilizing O_2 plasma, ensuring complete removal of the resist in uncovered areas of the wafer that might obstruct the covered regions. In this stage, the photo resist is removed at a rate of 10 nm/sec. Subsequently, in the actual etching phase, the photo resist undergoes etching at a rate of 6 nm/cycle.

Photo resist stripping:

Following the initial deep silicon etching, the photo resist removal process involves a combination of O_2 plasma with *Tepla GiGAbatch*, and *UFT Remover*. However, considering that O_2 plasma removes both the photo resist and Parylene, and since it has already been utilized in the prior stripping stage, potentially affecting Parylene adhesion, it is advisable to limit *TePla GiGAbatch* exposure to no more than 30 seconds. If the photo resist is successfully removed after *UFT Remover* step, a visual and microscopic inspection of the Parylene adhesion is recommended, as detachment may occur due to the effect of O_2 plasma.

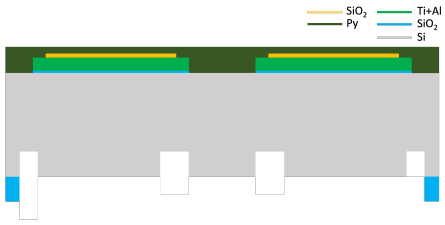


Figure 3.38: Wafer section after PR stripping.

Second deep silicon etching

In the second phase of deep silicon etching, once again utilizing the *SPTS Rapier*, the objective is the complete removal of silicon, confining it solely to the backside design of the probes and beyond the rectangle (figure 3.39.

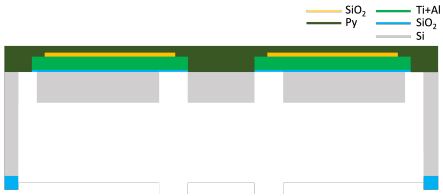


Figure 3.39: Wafer section after second deep silicon etching.

The mask facilitating selective silicon etching is embodied by the SiO_2 layer, a frequently employed hard mask in these applications, affected during the etching proces with a rate equal to 2.5 nm/loop. Here, the thickness of the silicon to be etched ($thick_2$) is contingent on the quantity of silicon removed ($thick_1$) in the preceding step and the overall thickness of the silicon wafer ($thick_{Si}$), and it is calculated by the following formula 3.6:

$$thick_2 = thick_{Si} - thick_1 \tag{3.6}$$

Nevertheless, in this concluding etching phase, it is pivotal to include an over-etching step to guarantee thorough silicon removal in the pertinent areas across the whole wafer, enabling the subsequent release of probes. Over-etching, in this case, is not deemed a critical step, owing to the presence of Parylene and SiO_2 on the front side. These materials serve as a robust mask, arresting silicon etching without adversely impacting adjacent layers.

3.3.10 Insulator coating - Backside

Before proceeding with the release of the probes, a backside coating is imperative, ensuring isolation and biocompatibility while minimizing the response of brain tissue. Viable coating alternatives that meet the requirements encompass SiO_2, SiC, and Parylene. However, SiO_2 and SiC may pose challenges related to adhesion and adaptation to topography characterized by significant thickness variations. In contrast, Parylene circumvents these issues as a plastic material, effortlessly adapting to complex topographies, provided the deposited layer remains sufficiently thin.
As a first test, it was decided to deposit 1 μm of Parylene, covering both the front and backside while aligning the pins with the front side to ensure a uniform coating on the backside.

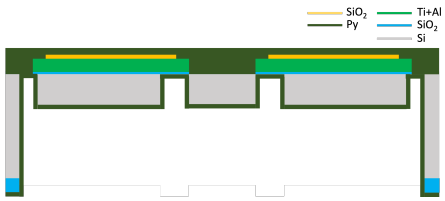


Figure 3.40: Wafer section after backside Parylene coating.

3.3.11 Parylene etching - Frontside

The final step in the process flow involves etching the 5 μm of Parylene on the frontside, deposited for the protection of structures, along with an additional 1 μm resulting from the latest coating. The wafer containing the probes is positioned on a dummy wafer, where cavities approximately 80 μm in size, matching the dimensions of the rectangle containing the probes, have been created. The two wafers are bonded together using a quick stick, melted on a hot plate at 135 °C. Once the wafers are bonded, the etching of the Parylene on the front side can proceed, releasing the structures that will fall into the cavities of the dummy wafer. The etching process is carried out using the *PlasmaPro100 Cobra*.

Endpoint detection in this phase proves highly beneficial. By positioning the laser on the inner part of the rectangle but outside the probes—where all 6 μm of Parylene need to be removed—one can assess, from the laser reflectivity plot, when the Parylene has been completely etched. This allows for the release of the probes. An overetching phase is necessary to ensure the complete removal of Parylene, even at the wafer's edge. Following the identification of a flat signal, an overetching of approximately 15% is performed. This overetching, involving only O_2 plasma, preserves the integrity of the probes but ensures their release.

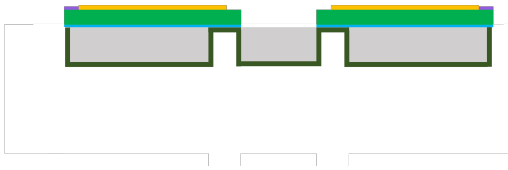


Figure 3.41: Wafer section after probes release.

3.4 Probes for neural recording

The fabrication process also involved the development of probes designed not only for stimulation through the aluminum layer but also for recording neural activity. To achieve this objective, two additional layers were added to the probes originally intended for stimulation. Following the aluminum layer to ensure proper stimulation and the silicon dioxide layer for isolation, a metal (either aluminum or platinum) was once again deposited. Subsequently, using successive steps of photolithography and etching, a pattern suitable for brain recording was created. This pattern featured four circular recording sites with a diameter of 5 μm, connected by 4 μm-wide traces to the pad. In this case as well, the final layer serves as insulation, aiming to isolate the entire shank except for the portion overlapping with the pad and the recording sites, where exposed metal will be present.

Figure 3.42: Design for Aluminum layer (4 μm, stimulation).

Figure 3.43: Design for SiO_2 layer (1 μm, insulation).

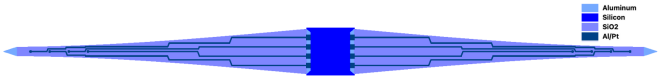


Figure 3.44: Design for Al/Pt layer (500 nm, recording).

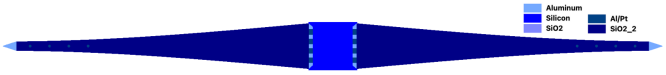


Figure 3.45: Design for SiO_2 layer (500 nm, insulation).

3.5 Neural Probe Bending Methodology

Following the release of the probes, the shanks undergo a 90-degree bending process to achieve a configuration conducive to implantation. For the successful bending of the probes, it is imperative that the final thickness of the silicon chip be smaller than the value of the trench, which represents the distance between the chip and the shank in the backside design of the probe. Failure to meet this requirement would impede the completion of the bending process due to the bulkiness of the silicon. To facilitate the bending, a specialized device was constructed. The intricate details of this device necessitated the use of *Nanoscribe Photonic Professional*

GT+ (Nanoscribe GmbH & Co. KG, Germany), a 3D printer with nanometric precision, as conventional 3D printers lacked the required accuracy. The printing process involved the precision polymerization of IP-Q resist on a silicon substrate, utilizing a 10x objective selected based on the dimensions involved. Subsequent to the exposure process, the substrate and partially polymerized resist underwent development in PGMEA, followed by rinsing in IPA. This procedure facilitated the removal of excess resist, revealing the structure of the targeted device.

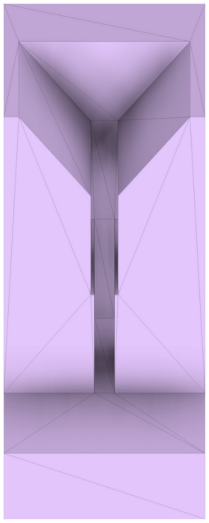


Figure 3.46: Bending device used for probes bending.

After development and drying, the device was detached from the silicon substrate through the generation of thermal stress via gradual heating from 25°C to 190°C on a hot plate. This thermal stress facilitated the separation of the device from the silicon substrate using a blade. The device, depicted in Figure XX, consists of three distinct sections. The probe must be positioned with the backside facing upward in the upper part of the device, centering the chip over the central cavity. Using an additional element (figure 3.47) printed with the *Nanoscribe* following the same procedure (IP-Q resist polymerization on a silicon substrate), pressure is generated over the chip. In this manner, the walls of the bending device exert pressure on the fins, inducing an initial 45-degree bend.

The design of the device ensures that stress is applied to a sufficiently solid portion of the shank (near the chip) to prevent damage to the probe from manually applied force. This approach minimizes the applied force moment compared to applying force near the tip, which is challenging to control precisely. The initial 45-degree bending stabilizes the probe before proceeding to the second bend, after which the shanks will be fully bent to 90 degrees. The opening of the tunnel for

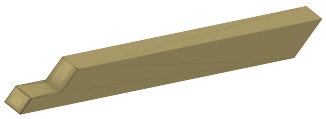


Figure 3.47: Lever used for the application of force.

this second and final bending is 270 μm, slightly larger than the 250 μm chip size, facilitating its movement within the tunnel. The third region of the device has an opening of 200 μm, smaller than the chip size to prevent its insertion but allowing the insertion of a needle. By sliding the probe upwards, the needle separates it from the device, preparing it for implantation.

Chapter 4

Results and Discussion

In the following section, the results obtained at various intermediate steps and at the end of the manufacturing process are analyzed, interpreting images and data derived from metrology instruments such as the optical microscope (*Leica*), Scanning Electron Microscopy (SEM) (*Zeiss Merlin*), mechanical profilometer (*Bruker Dektak*), optical profilometer (*Bruker Contour X*), and the film thickness mapper (*Filmetrics F54*). The optical microscope was employed to assess the results derived from various photolithography steps following resist development, ensuring the correctness of the design and alignment before proceeding with the etching step. Additionally, the optical microscope can provide an indication of the height step between two points. By selecting two points and adjusting the focus for each to achieve optimal clarity, the step height can be evaluated as the difference in the z-coordinate that yields the best focus. This method provides a rapid indication of the etching rate on the specific design.

On the other hand, SEM allows the generation of high-quality images by scanning the surface with a focused ion beam of electrons. This enables a detailed examination of the separation between different layers and a more in-depth assessment of the design compared to the optical microscope. The optical and mechanical profilometers, in turn, are used to evaluate the step height between different points in the design, allowing considerations regarding the actual deposited material thickness and the profile of various layers. The mechanical profilometer employs a stylus in physical contact with the substrate, reflecting the design profile through stylus movement. However, in cases involving deep and narrow holes where the stylus cannot reach the depth, the results from the mechanical profilometer may be unreliable. In such instances, the optical microscope with Vertical Shift Interference (VSI) mode is preferred, relying on vertical scanning interferometry. This method, once again, provides insights into the design profile without contact with the substrate (with the added advantage of avoiding wafer damage).

The thin film mapper is used to assess the thickness of specific materials, allowing

for precise mapping by selecting measurement points. Based on criteria such as layers to study and the type of material on which the film thickness mapper operates, it defines the film thickness according to the procedure outlined in Section XX.

4.0.1 Aluminum layer - Frontside

The design transferred onto the wafer following the initial photolithography, specifically on the aluminum layer, has been evaluated in terms of shape and dimensions using an optical microscope. It is crucial to perform this assessment both before and after the etching process to proceed with resist stripping in case the photolithography does not yield the expected results. The images below (figure 4.1) were obtained from an inspection executed immediately after the resist development, with the darker portions representing the resist. This delineates protection for the underlying aluminum in the subsequent etching step, which aims to remove the aluminum in areas not shielded by the resist.

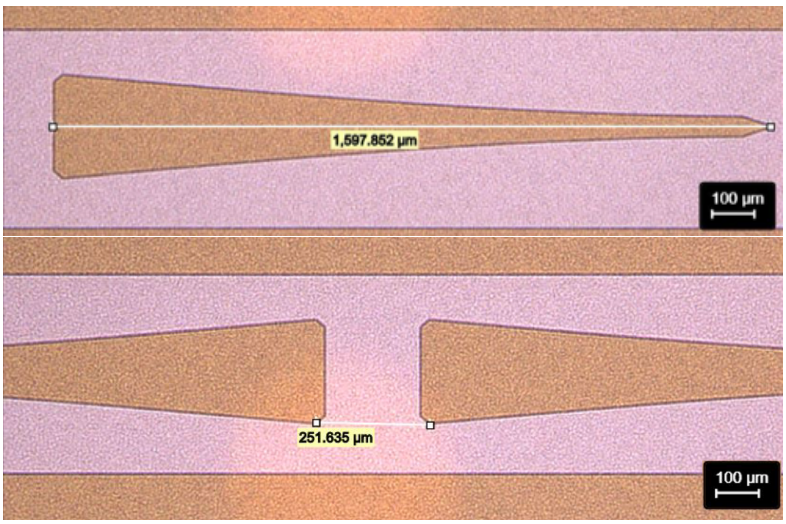


Figure 4.1: Probes after Aluminum photolithography.

The resulting structures are re-examined under the microscope after resist stripping to assess the need for additional treatment with O_2 plasma due to incomplete resist removal, as depicted in figure 4.2.

4.0.2 SiO_2 layer - Frontside

Before proceeding with the backside processing, following the photolithography on the SiO_2 layer, the structures were meticulously examined under the microscope to verify the alignment between the two layers (Aluminum and SiO_2), resulting in the

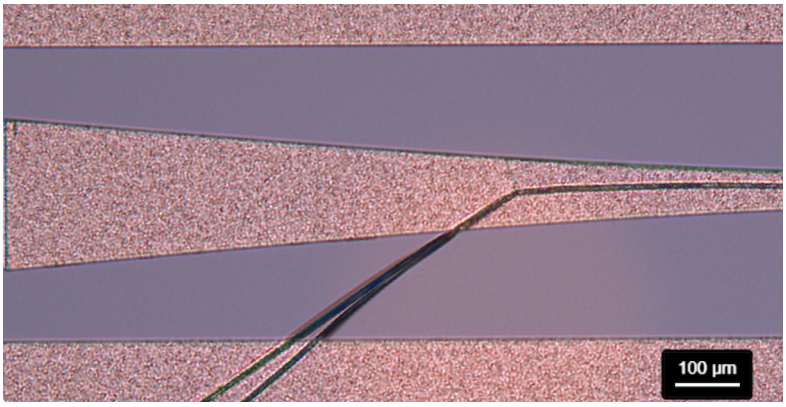


Figure 4.2: Example of unsuccessful stripping with photo resist residuals.

configurations depicted in figure 4.3. In the provided images, the photoresist covers the entire shank, excluding only the tip used for stimulation and the portion of the shank overlapping the chip. This ensures the maintenance of a specific surface area of exposed highly conductive aluminum.

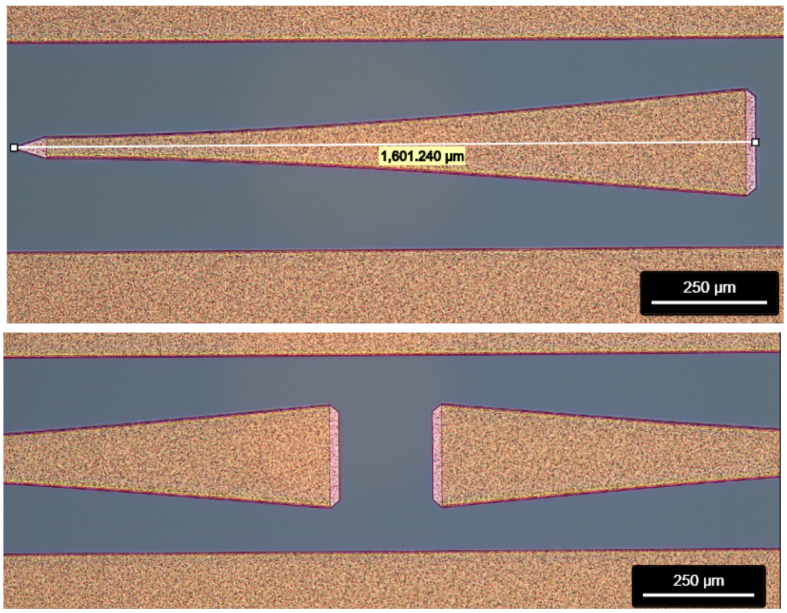


Figure 4.3: Probes after SiO_2 photolithography.

Subsequent to the etching and stripping steps, the structures underwent further inspection using the optical profilometer.

In this instance, utilizing the provided section in figure 4.4, an anticipated step height of nearly 5 μm is expected. This projection arises from the transition

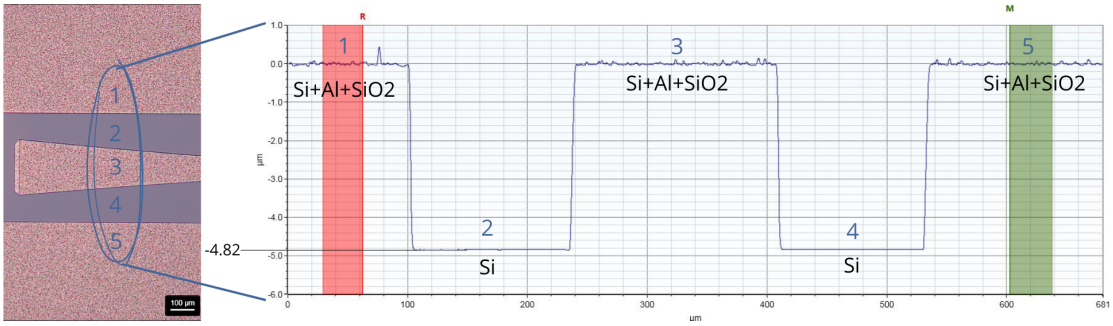


Figure 4.4: Probes profile obtained from optical profilometer after SiO_2 etching.

between regions featuring both Al and SiO_2 layers (regions 1, 3, and 5) to regions exclusively comprising Si due to the etching of both Al and SiO_2 layers (regions 2 and 4). Commencing from region 1, characterized by the simultaneous presence of Al and SiO_2 depositions on the wafer, the initial thickness value is established as 0, as a starting point. Progressing to the second region, a step height of 4.82 μm is measured for this specific sample, closely aligning with the expected value. From this sectional analysis, isolating the individual contributions of Al and SiO_2 is not feasible, preventing identification of the component responsible for the observed deviation from the anticipated total value of 5 μm (comprising 4 μm from Al and 1 μm from SiO_2).

In the third area, situated at the shank location, the stylus measures an identical thickness to that of the first region, as expected. In the fourth area, characterized by exposed Si, a thickness reduction of approximately 4.8 μm is observed, consistent with the findings in region 2. The final region, positioned outside the rectangle and featuring both Al and SiO_2 layers, yields the same thickness as regions 1 and 3. Considering the alternative section of figure 4.5, Al and SiO_2 contributions can be distinctly delineated.

The thickness of the initial region is denoted as 0, pertaining to the concurrent presence of both Al and SiO_2. In the subsequent region, where SiO2 has undergone etching, an anticipated thickness reduction of 1 μm (equivalent to the SiO_2 thickness) is expected and duly observed. This elucidates that the Al thickness is not precisely 4 μm but marginally lower, by approximately 200 nm in this specific sample.

In the third region, coinciding with the chip, both materials have been etched, reaching the minimum thickness. The cumulative delta for wafer 4 corresponds to 4.82 μm, as detailed in the preceding section. Region 4 exhibits a thickness increment attributed to the presence of the Al layer, albeit slightly thinner than expected. Subsequently, in region 5, the maximum thickness is attained due to an additional μm contributed by the SiO_2 layer.

The SEM has been employed for the examination of the morphological features

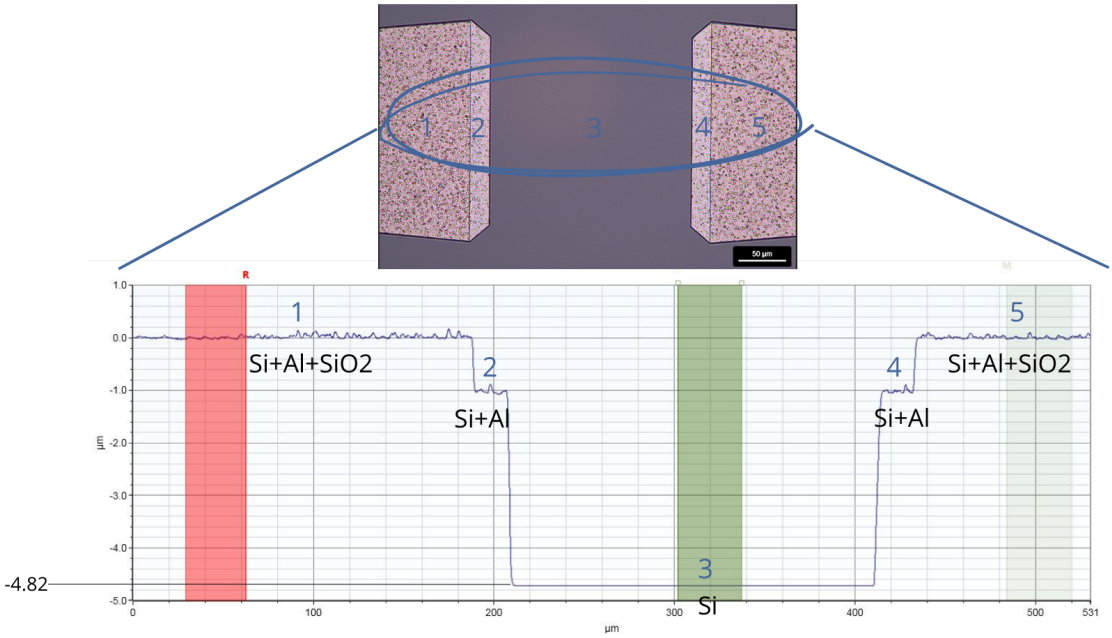


Figure 4.5: Probes profile obtained from optical profilometer after SiO_2 etching.

of the structures, specifically focusing on the pad and the tip. This choice was dictated by the fact that other segments of the probes are shielded by an insulating material, which complicates the process of surface scanning. The SEM images have

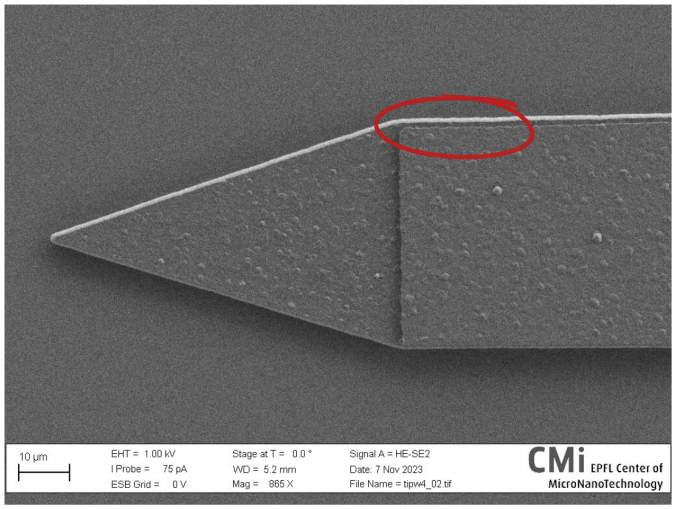


Figure 4.6: Tip morphology obtained by SEM analysis.

unveiled a notable concern related to the SiO_2 layer, as it fails to uniformly cover the shank as shown in figure 4.6.

This issue appears to stem from a combination of errors during photolithography exposure and the influence of scattered ions during SiO_2 etching. Consequently,

Figure 4.7: Scattering of ions during etching.

there are instances of SiO_2 removal beneath the resist, a phenomenon exacerbated by the presence of a thick layer of aluminum as demonstrated in figure 4.7.

Despite this challenge, SEM images attest to the proper morphology of both the chip and the tips. Notably, these structures demonstrate a high degree of precision in terms of shape and thickness step, showcasing exceptionally vertical sidewalls as demonstrated in figure 4.8.

4.0.3 Grinding - Backside

The grinding process proved to be a critical step as it revealed issues related to the chosen front side protection, leading to wafer breakage in certain instances. In the initial attempt, UV-tape was employed to safeguard the structures on the front side. However, following the grinding process, the wafer broke during the UV-tape removal due to the high mechanical stress exerted on the thick (4 μm of Al and 1 μm of SiO_2) and narrow structures.

To address this issue in the second attempt, UV-tape was replaced with a 15 μm layer of photo resist deposited on the front side, and edge bead removal was performed to prevent resist residues at the edge from hindering the grinding process. This approach proved successful for 2 out of 3 wafers. Subsequently, for the next wafer, a combination of UV-tape and photo resist was utilized. In this configuration, UV-tape adheres more smoothly to the surface due to the substantial resist thickness, as illustrated in figure 4.9. Consequently, the stress generated during UV-tape removal does not pose a threat to wafer integrity, while the photo resist is chemically removed through a standard treatment with *UFT remover*.

4.0.4 SiO_2 deposition - Backside

Following the deposition of 1 μm of SiO_2 on the backside through PECVD, the layer's uniformity was evaluated using the *Filmetrics F54*. In previous versions

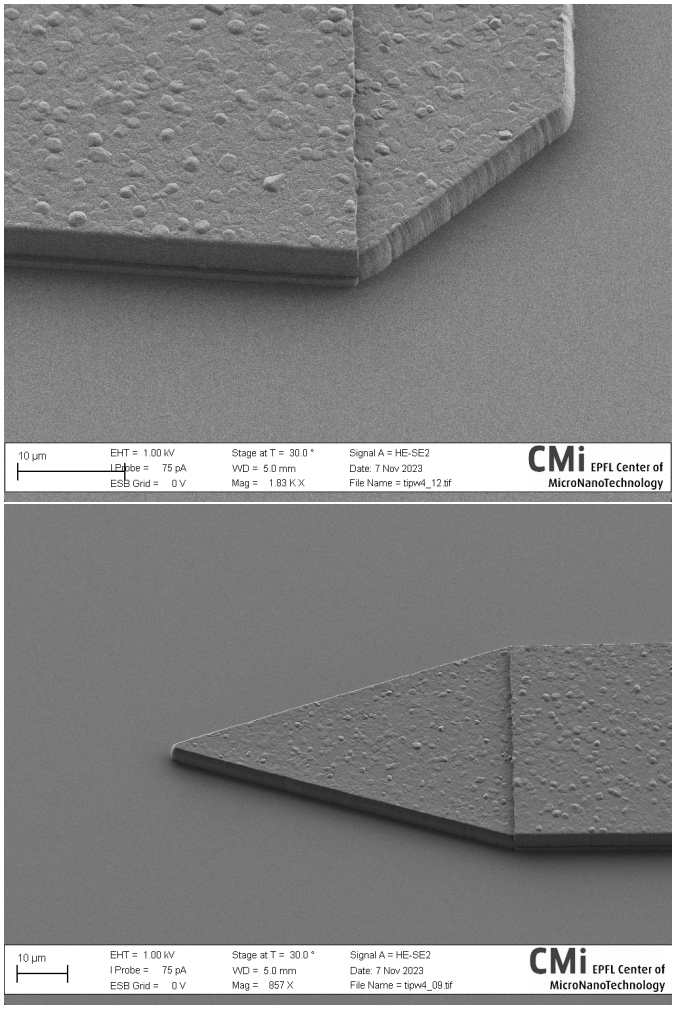


Figure 4.8: SEM images.

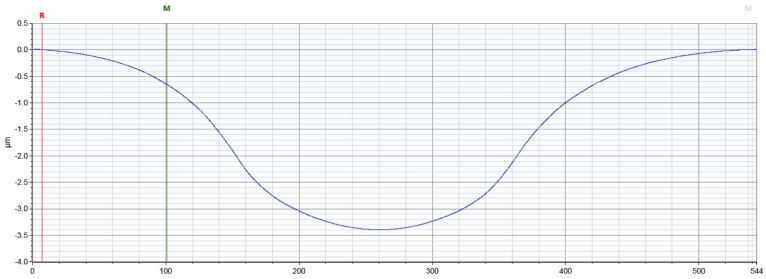


Figure 4.9: Thickness evaliuation after 15 μm PR coating using mechanical profilometer.

of the process flow, this step was executed through sputtering, resulting in non-uniform SiO_2 deposition (with an error of approximately 10%). The uniformity achieved with PECVD, on the other hand, is significantly higher, with an error of around 1%, as demonstrated by conducting measurements with the *Filmetrics F54*.

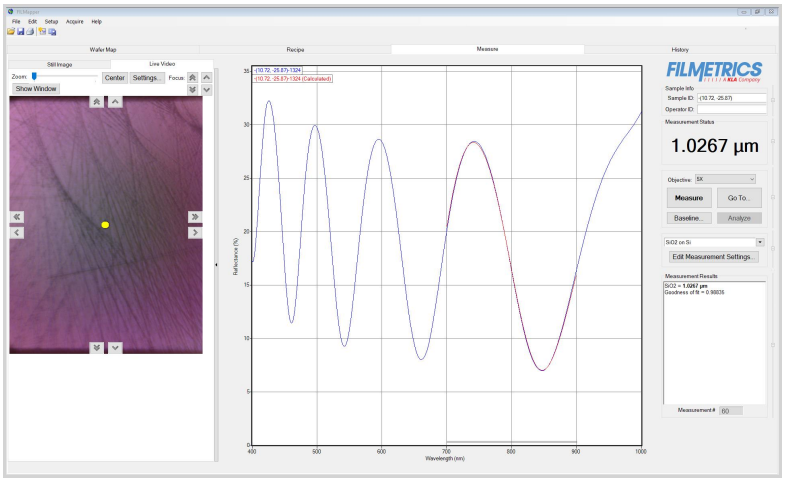


Figure 4.10: SiO_2 thickness in the center measured with *Filmetrics F54*.

These measurements detected a SiO_2 thickness of approximately 1.0267 μm at the center as shown in figure 4.10.

4.0.5 Parylene coating - Frontside

Following the parylene coating, the structures were examined under an optical microscope, revealing a significant disparity between the structures at the wafer edge and those towards the center. In the former, an incomplete adhesion of Parylene is evident, as indicated by the iridescent region observed around the edge of the structures and the rectangle, where a depth variation is noticeable. However, this issue is observable exclusively at the wafer's periphery, specifically along the first and last rows and columns. In contrast, for the other structures situated closer to the center, the Parylene adhered adequately, as illustrated in the accompanying figure 4.11.

This issue arises from the utilization of the edge bead removal function during the resist coating on the frontside, a necessary step to ensure protection during grinding. However, since this problem is confined to structures at the wafer's edge, it does not pose an impediment to subsequent steps in which Parylene will be employed solely to stop the deep silicon etching step and to bond the frontside structures together.

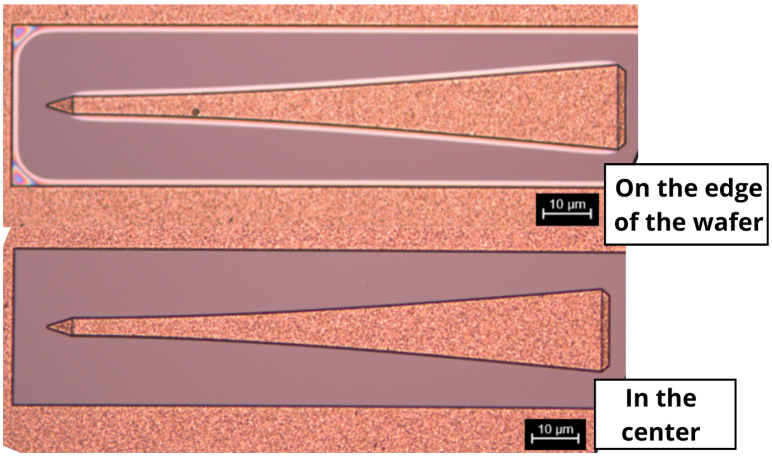


Figure 4.11: Parylene adhesion inspection, comparison between structures at the edge and in the center.

4.0.6 SiO_2 layer - Backside

The initial step of backside photolithography aims to isolate the photoresist to enable the etching of SiO_2 within the rectangle containing the structures, thus creating a hard mask for the subsequent silicon etching step. To assess the alignment between the backside and front side, it is necessary to employ a glass support that allows irradiation of the wafer backside with infrared light. Infrared light, with longer wavelengths than visible light, can penetrate more effectively through the glass support, reaching the wafer.

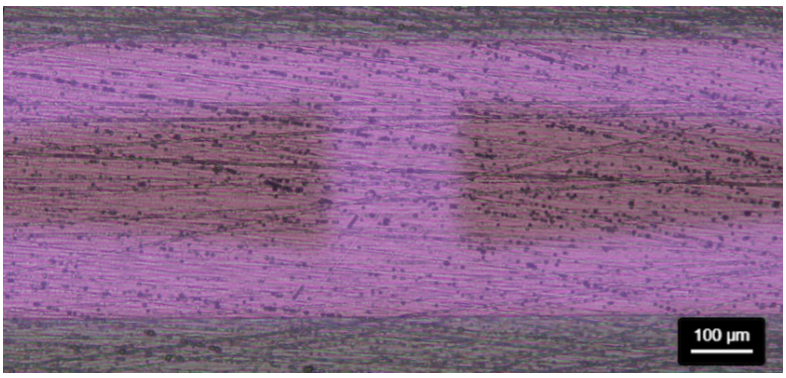


Figure 4.12: Frontside and backside microscopic inspection.

By adjusting the intensity of the backside infrared light and the frontside visible light, the design of both the frontside and backside can be visualized in the same image as shown in figure 4.12, where the brighter part represents the backside,

where the infrared light brights the wafer.

4.0.7 Second photolithography - Backside

Microscopic inspection following the second backside photolithography must be conducted with considerable precision, as even a slight misalignment could compromise the release and bending of the probes.

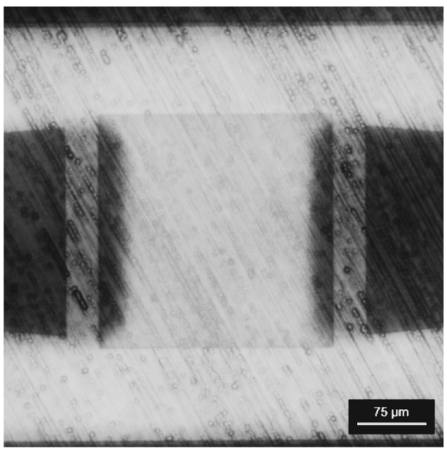


Figure 4.13: Frontside and backside microscopic inspection in corrispondance of the chip.

Special attention must be paid to the overlap between the shank and the chip (figure 4.13), ensuring the proper connection between these two elements even when the probes are bent.

Another critical aspect to consider is the alignment of the shanks tip, which must ensure consistency between the design of the frontside and backside, as shown in figure 4.14

Figure 4.14: Frontside and backside microscopic inspection in corrispondance of the tip.

4.0.8 First deep silicon etching - Backside

The deep silicon etching is carried out iteratively, carefully monitoring the relationship between the number of cycles performed and the etched depth. The etching rate is calculated accordingly, and it tends to decrease as the depth of the step increases. This reduction is attributed to the unfavorable gas loading and unloading conditions caused by the considerable depth of the trench.

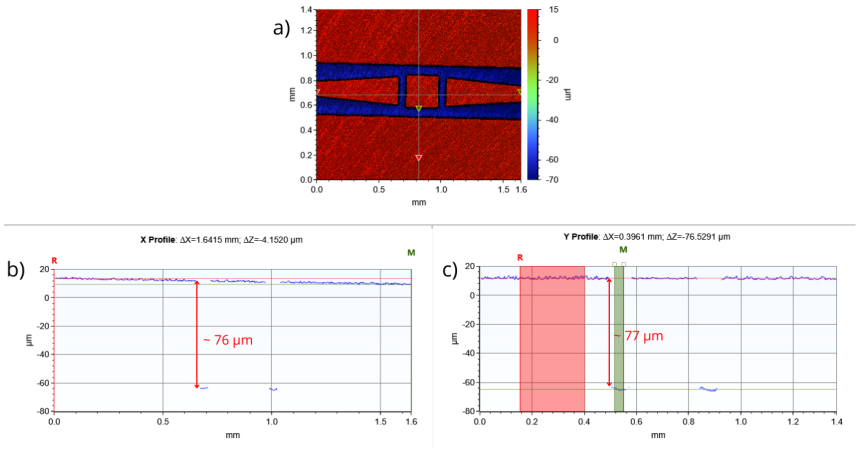


Figure 4.15: Optical profilometer profile evaluation after the first deep silicon etching step. a) probe backside design, b) depth x-profile, c) depth y-profile.

For the wafer with trench of 70 μm for example, a singular iteration involving 105 cycles proved adequate, resulting in etching from 73 μm up to 77 μm. The optical profilometer is employed to assess the etched thickness without causing damage to the wafer, given its critical design. The x-profile plot provides insights into the step between the shank and the chip, nearly equal to 76 μm for this specific chip. Conversely, the y-profile plot enables the evaluation of the step between the rectangle (or the rest of the wafer without any design) and the chip, resulting in a step height of 77 μm, consistent with the previous plot.

4.0.9 Photo resist stripping

Following the photoresist stripping, specifically after the use of O_2 plasma with *Tepla*, the detachment of the Parylene on the frontside was observed (figure 4.16, as anticipated. Consequently, as the structures on the frontside were no longer adequately protected, impeding the continuation of the fabrication process, the decision was made to completely remove the Parylene on the frontside following the mentioned steps:

- 10 min O_2 plasma with *Tepla*

- Cleaning with IPA and acetone to remove visible burnt Parylene residuals
- 10 min O_2 plasma with *Tepla*
- 3 min O_2 plasma with *PlasmaPro100 Cobra*

Subsequently, a new coating of 5 μm of Parylene was applied to ensure the protection of the structures.

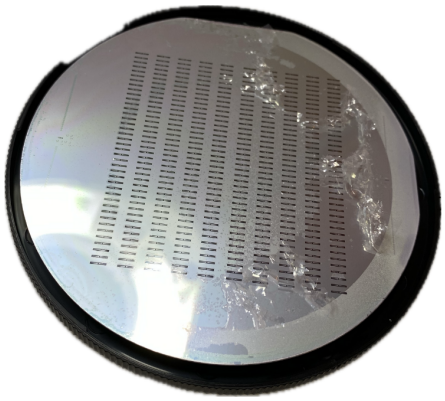


Figure 4.16: Parylene detachment after *Tepla* use.

4.0.10 Second deep silicon etching - Backside

For wafer with a 70 μm trench, the second and final deep etching process was completed through multiple iterations, coupled with optical profilometer analysis. Following the first iteration, the step height between the shank and the chip remained at 73 μm (figure **??**b), identical to the previous etching step. This indicates a uniform reduction in thickness for both the silicon under the shank and the silicon under the chip, aligning with our expectations. Utilizing the y-profile (figure **??**c), the step between the rest of the wafer and the internal portion of the rectangle was measured, resulting in a depth of 147 μm—higher than the 77 μm found in the same portion after the initial etching (figure 4.15c). However, the step height between the chip and the rectangle remained nearly constant at 75 μm. This consistent behavior confirms the proper etching of silicon.

Multiple iterations were performed for this final etching, revealing a diminishing etching rate as the process progressed. The last 15 cycles served as overetching to ensure complete silicon removal for subsequent probe release. Overetching, in this case, is not deemed critical due to the presence of Parylene and SiO_2 on the front side, acting as a hard mask to stop the etching. After the final 15 overetching cycles, thinning was observed only in correspondence of the shank and of the chip.

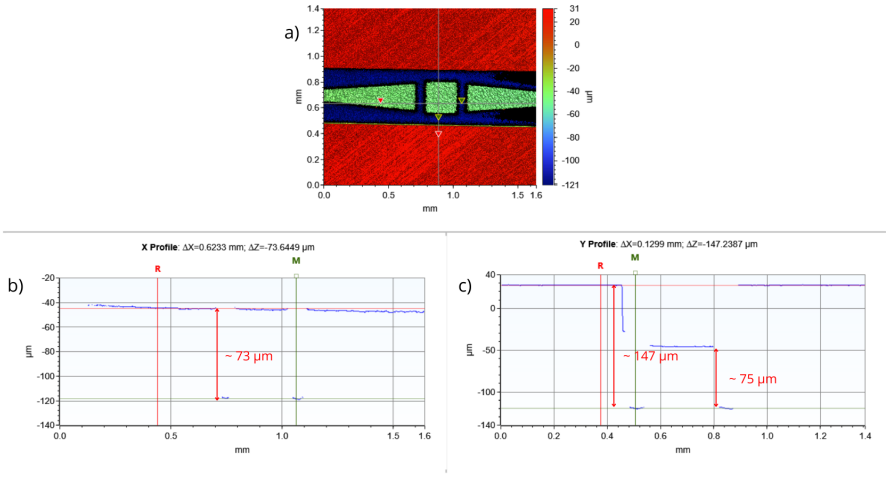


Figure 4.17: Optical profilometer profile evaluation after the first iteration of the last deep silicon etching step. a) probe backside design, b) depth x-profile, c) depth y-profile.

Iteration	Number of Cycles	Etched Thickness (μm)	ER (nm/cycle)
1	105	75	$\sim$ 714
2	105	65/70	$\sim$ 650
3	15	Overetching	-

Table 4.1: Summary of Deep Silicon Etching Iterations

As the etched depth increases, the influence of the design becomes more pronounced. Towards the end of these final cycles, variations in the etched thickness became evident based on the probe design. For designs 1 and 2, which are very similar, the step height between the shank and the rectangle is the same as that between the chip and the rectangle, equal to 50 μm, as observed in the y-profile (figure **??**c). As this represents the final etching, it is crucial to study the step between the rectangle and the rest of the wafer, ideally equal to the total silicon wafer thickness since complete silicon removal is necessary in this area. In this case, the mentioned step is 217 μm (figure **??**c), but it was higher for the second-to-last iteration (147 μm, figure **??**c), confirming an overetch of silicon during the final cycles, resulting in a reduction in the remaining silicon thickness.

For design 3 (figure **??**a), the x-profile (figure **??**b) indicates different depths for the shank and chip, with the chip being more etched due to its elementary and larger shape, facilitating the loading and unloading of etching gases. In contrast, the y-profile (figure **??**c)shows that the depth between the rectangle and the rest

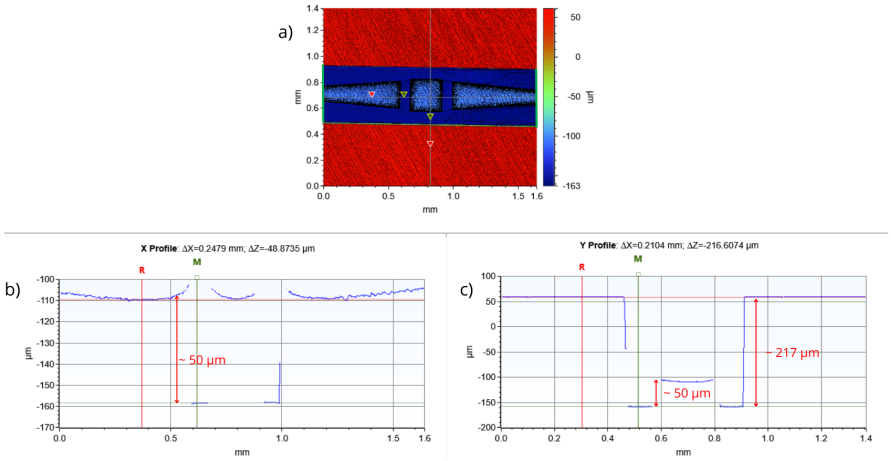


Figure 4.18: Optical profilometer profile evaluation at the end of the last deep silicon etching step for designs 1 and 2. a) probe backside design, b) depth x-profile, c) depth y-profile.

of the wafer is 217 μm, lower than the value found in the previous iteration.

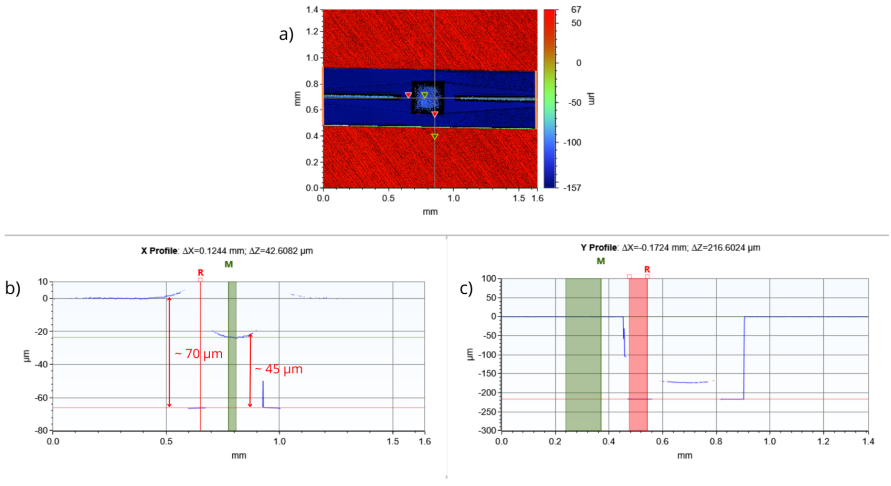


Figure 4.19: Optical profilometer profile evaluation at the end of the last deep silicon etching step for design 3. a) probe backside design, b) depth x-profile, c) depth y-profile.

3D images further highlight the distinctions between the designs, particularly the thinner chip compared to the shanks for design 3, while designs 1 and 2 exhibit both elements at the same level.

Probes were also inspected under a microscope, and thanks to the reduction

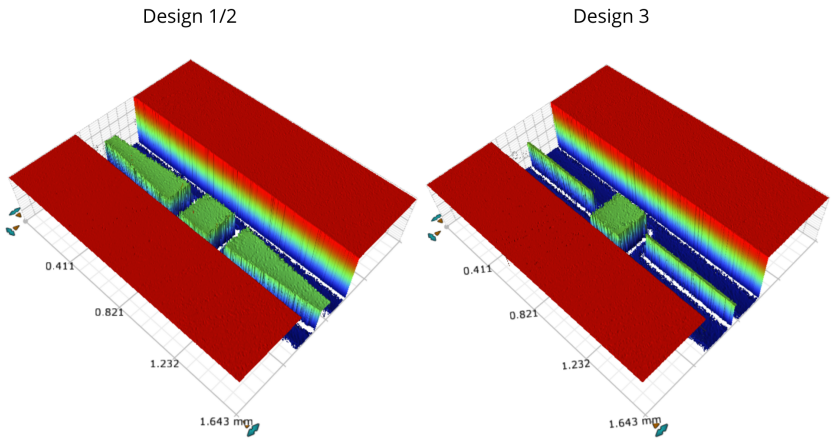


Figure 4.20: Optical profilometer 3D evaluation for both designs.

in silicon thickness, it is now easier to visualize both the front side and backside designs simultaneously.

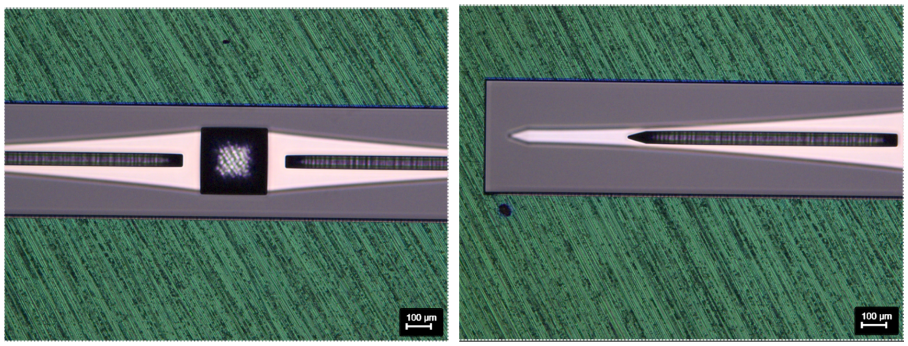


Figure 4.21: Optical microscope inspection at the end of the last deep silicon etching step.

4.0.11 Insulator coating - Backside

A coating is imperative to ensure insulation and biocompatibility, given its direct contact with the brain. The choice for the backside coating is narrowed down to parylene and SiO_2. However, for the initial trial, parylene has been selected due to its advantageous role in facilitating a smoother release of the probes.

A 1 μm parylene coating has been applied to both sides of the wafer to avoid the use of UV tape, due to the fragility of the wafer. Consequently, after the CMi service, there is 1 μm of parylene on the backside and a total of 5+1 micrometers

on the frontside, with the additional 5 micrometers originating from the preceding coating to ensure frontside protection.

The utilization of parylene presents both merits and drawbacks. The primary advantages include:

- Uniformity in coating: The parylene deposition process involves material sublimation under vacuum conditions, ensuring even coverage on intricate and irregular three-dimensional surfaces;
- Controlled thickness: The process allows for precise control over the thickness of the coating;
- Flexibility: This ensures comprehensive coverage, even on complex components;
- Low-temperature deposition: This reduces the risk of thermal damage to sensitive components.

However, the parylene coating on the backside is not without its disadvantages, including:

- Cost: Parylene is a high-cost material.
- Risk of cross etching: The need to etch parylene on the frontside for structure release poses a challenge, as the only layer keeping the probes together is also present on the backside. This introduces the potential for partial parylene etching on the backside due to the flow of O2 plasma.

4.0.12 Parylene etching - Frontiside

Before initiating the actual etching process, a dummy wafer with cavities aligned with the probe locations was manufactured. Subsequently, the wafer containing the probes is placed on top of the dummy wafer and bonded using a quick stick. For wafer 2, featuring a 70 μm trench, the cavity depth was set at nearly 90 μm. This depth allows the probes to descend and securely stabilize within the cavities at the conclusion of the etching process.

This method provides an additional advantage as it ensures that the released probes are systematically arranged inside the cavities, maintaining the same positions they occupied on the original wafer. This organizational structure greatly aids in distinguishing probes based on their respective designs.

The probes were then successfully released, falling into the cavities of the dummy wafer through a Parylene etching on the front side lasting approximately 9 minutes.

4.0.13 Released probes inspection

Wafer with 70 μm trench

After probes release, some problems for the wafer with 70 μm trench emerged. Despite the very good quality of the bosh process quite evident in the very vertical sidewalls, the final silicon thickness was higher than what expected and what measured using the profilometer, not allowing the probes bending since the final silicon thickness is higher than the trench. This was not expected because at the end of the last deep silicon etching step, the silicon thickness was evaluated using the profilometer, resulting in a final thickness of 50 μm for both the shank and the chip. It is quite evident in this case that the information provided by the optical profilometer cannot be considered reliable, due probably to the irregular surface (since this is a ground wafer, a significant portion of it has a notably rough surface), multiple reflection, non uniformity in the reflective index distribution etc.

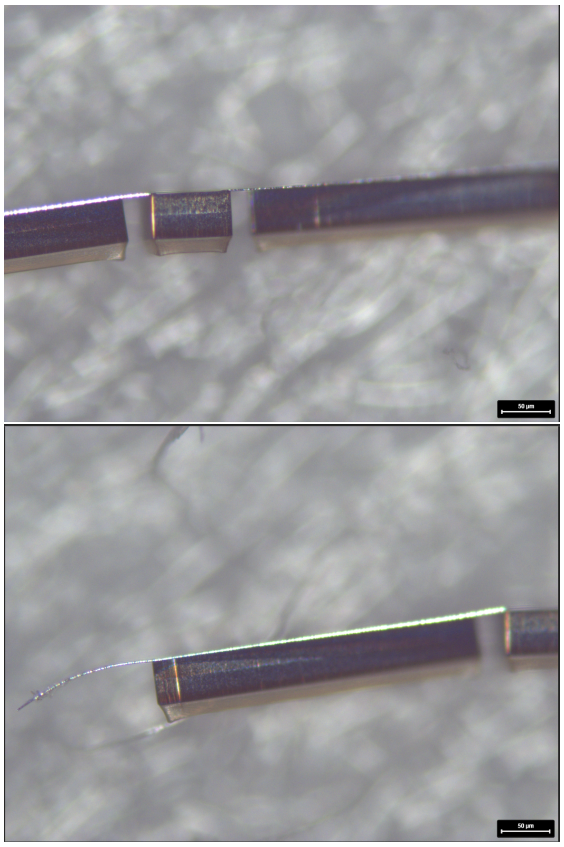


Figure 4.22: Optical microscope inspection of the released probe with 70 μm trench.

Two noticeable issues are evident in figure 4.22: tip bending and parylene

detachment. A partial bending of the final segment of the shank is observed for some backside designs, and this is likely attributed to stress resulting from the deposition of multiple layers. Throughout the various fabrication steps, the wafer may accumulate stress due to factors like temperature variations, pressures, or chemical processes. More specifically, the deposition of SiO_2 as the final insulating layer, aimed also at improving biocompatibility, induces deformation that remains in the material due to the employed PECVD process. Upon the release of the probes, these stresses indeed result in bends or deformations in the tips of the shanks.

The detachment of parylene instead, can be attributed to the aforementioned cross etching. In the concluding step of the process flow, an etching of parylene is performed to facilitate the release of probes. However, the precise positioning of the probes within the cavities is not guaranteed. Probes may deviate from a straight descent, adhering to the lateral wall rather than the base, or release may occur from one side as shown in 4.23. In such cases, the O_2 plasma flow could potentially impact the uniformity and adhesion of the parylene layer on the backside.

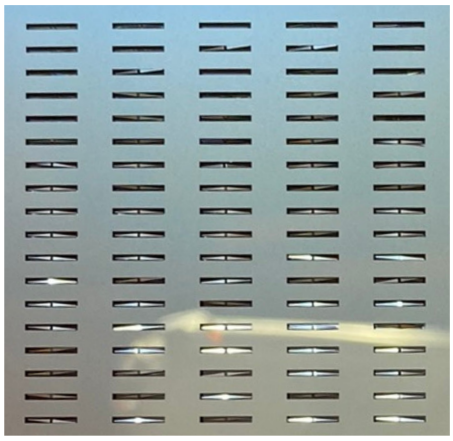


Figure 4.23: Optical microscope inspection of the cavities after probes release.

An insightful microscope photo (figure 4.24) enhances the understanding of probe positioning within the cavity. It is observed that, in this specific case, probes descend into the cavity with the backside facing upward, thereby allowing the O_2 plasma, utilized during the final etching, to contribute to parylene removal. An intriguing aspect discerned from the microscope photo is the varied coloring on the backside of the probes, indicating different positions that lead to a different reflection of light. Simple considerations about the color variations readily demonstrate that the location of probes within the cavity is not consistently uniform. Additionally, the photo illustrates instances where the tip of the probe on the left is positioned outside the designated cavity, while the cavity on the right encompasses both the

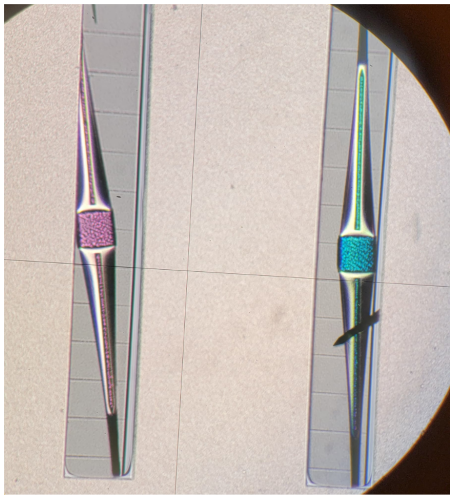


Figure 4.24: Optical microscope inspection of the released probes inside the cavities.

tip of one probe and the base of another.

Wafer with 30 μm trench

The microscope image in figure 4.25 pertain to wafer 3, specifically focusing on probes with a trench of 30 μm.

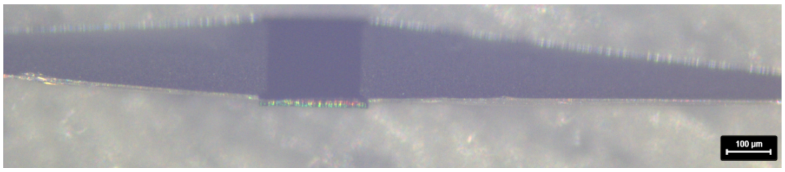


Figure 4.25: Optical microscope inspection of the released probe with 30 μm trench.

As discernible from figure 4.25, in this particular case, no issues pertaining to the uniformity of the final silicon thickness were encountered, thereby mitigating concerns associated with probe bending.

Despite this, other problems connected to the design appeared: first, also for this trench and final thickness value, the tip of the shank is partially bent for all the designs in which silicon is not present till the end of the shank, and second, for a design in particular, silicon has not been completely etched. The tip bending issue can be addressed or avoided by integrating a silicon support beneath the shank, as seen in the design case 1. The silicon support functions as a structural

reinforcement, offering increased strength and support to the shank.

Silicon is recognized for its stiffness and robustness, and introducing a silicon support beneath the shank can absorb a portion of the mechanical stress during manufacturing. This aids in upholding the structural stability of the probe and lowers the chances of the tip bending or undergoing damage. The incomplete etching problem instead, arises for designs 1 and 2, in which the space between the edge of the rectangle and the central (and also larger) portion of the probe is reduced. This hinders the loading and unloading of gases that are used during the etching process, leading to a not completed silicon etching in this part of the probe even if only in correspondence of the wafer edge.

Design considerations

Following the considerations made upon the release of the probes for all three backside designs, it has been possible to identify the pros and cons of each proposal.

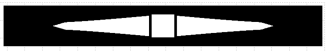
Design	Pro	Con
	- Straight tip	- Etching not completed
		- Etching not completed - Bent tip
	- Etching completed	- Bent tip

Table 4.2: Advantages and disadvantages of the proposed backside designs

In light of the concerns regarding the bending of the shank tip identified during the initial testing, it has been concluded that the most advantageous design is the first one. This is attributed to its extension of the silicon material to the tip, offering support to the overlying aluminum layer and mitigating tip bending. Addressing the sole issue associated with this design, pertaining to incomplete silicon etching in the center, may be remedied by enlarging the rectangle on the backside, thereby providing additional space for the gases responsible for the etching process.

4.1 Probes for neural recording

4.1.1 Recording layer photolithography

The "additional" photolithography that should be carried out compared to stimulation probes, specifically pertaining to the recording layer, has revealed challenges

arising from the surface topography. The photoresist coating is performed using a spin coating technique and, due to the substantial height difference between the thinnest and thickest parts of the wafer, which is approximately 5 μm (4 μm of aluminum and μm of SiO_2), issues have arisen. The challenge in coating the photoresist arises from its difficulty in effectively covering the terminal part of the shank. This difficulty is attributed to the region where the amplitude between the outer part of the rectangle and the design of the probe is greater, resulting in a wider thickness gap. Consequently, the photoresist faces obstacles in depositing smoothly onto the terminal section of the shank. As a result, the thickness of the resist in this specific area is found to be lower than the expected value. Given the complexity of the design in terms of trenches and depth, the results obtained from the profilometer may not always be deemed reliable in the definition of the photoresist thickness. Therefore, to assess the feasibility of proceeding with the etching step based on the amount of resist in the relevant areas, SEM images have been acquired. Through these images (figure 4.26) and with some straightforward calculations, it is possible to determine the thickness of the resist.

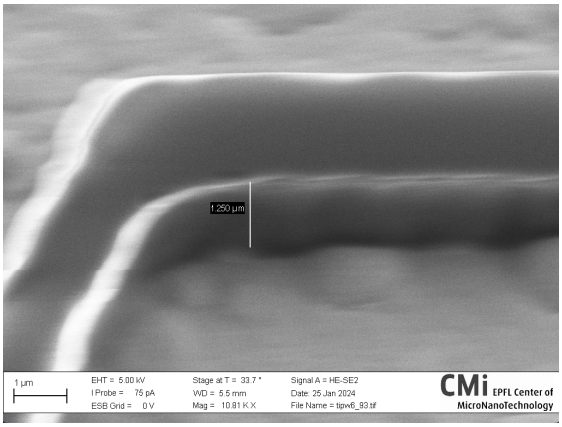


Figure 4.26: SEM image before the etching of the recording layer.

In this scenario, the determination of resist thickness involves considerations regarding the inclination angle (α) applied during image acquisition and the measured length (l). The resist thickness (h) can be expressed as:

$$h = \frac{l}{\cos(\alpha)}$$

and so

$$h = \frac{1.250\,\mu\text{m}}{\cos(33.7°)} = 1.5\,\mu\text{m}$$

SEM images have facilitated a comprehensive evaluation of the design transferred onto the wafer through the photolithography process, as depicted in the following

figure 4.27. This in-depth analysis has allowed for an examination of both the morphology and precision of the structure achieved before proceeding with the etching step.

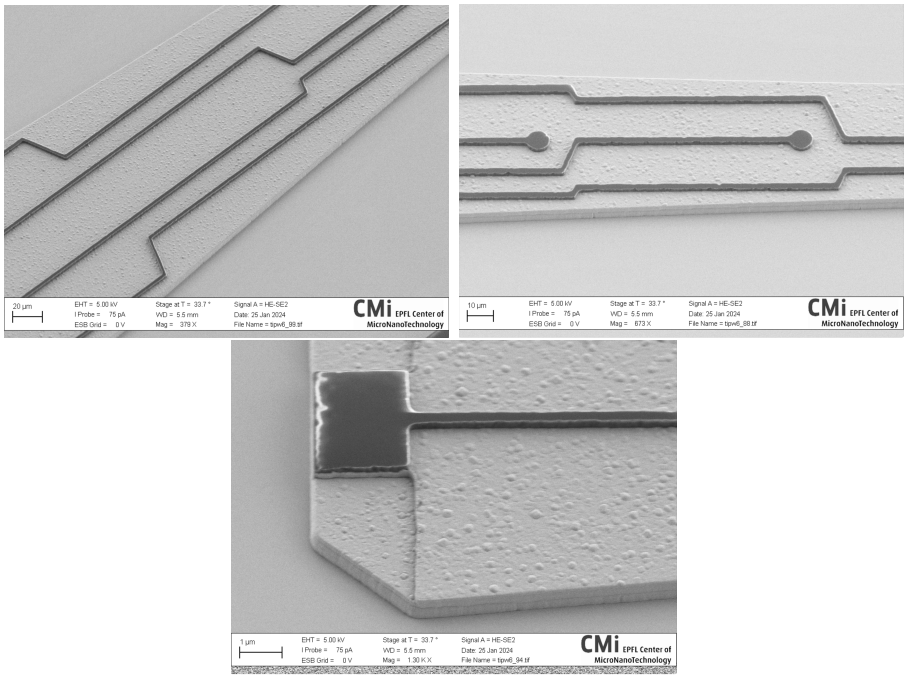


Figure 4.27: SEM images before the etching of the recording layer.

4.1.2 Recording layer etching

In the context of platinum layer etching, ion beam etching is employed rather than dry etching, as is the case with aluminum, due to the necessity of achieving high selectivity and directionality in the material removal process. Ion beam etching involves the use of ionized inert gas ions, such as argon, to selectively and directionally remove the material. In contrast, dry etching may exhibit less selectivity and directionality.

Due to the purely physical nature of the sputtering mechanism in the etching process, which involves no volatile byproducts, redeposition of etched materials occurs in areas not directly exposed to ions. The sidewalls of the photoresist mask, typically mostly vertical, are impacted by this redeposition of etched materials.

To mitigate this effect, it is recommended to optimize the shape of the photoresist patterns by performing a reflow process. This helps tilt the sidewalls, exposing them to ions and thereby preventing material redeposition [77].

The resist reflow process precedes etching to ensure the accurate delineation of structure details. During the reflow, a portion of the heated resist liquefies and is drawn inward by the surface tension force, facilitating the attainment of desired profiles, such as lenses or sidewall structures. This step is indispensable for ensuring the accurate definition of structure details before proceeding with the etching process [78].

Following the ion beam etching performed using the *Nexus IBE350 (Veeco United States)* and subsequent stripping, the structures were inspected using the scanning electron microscope (SEM), which identified issues related to the redeposition of removed ions during the etching process on the sidewalls of the platinum traces, as illustrated in figure 4.28.

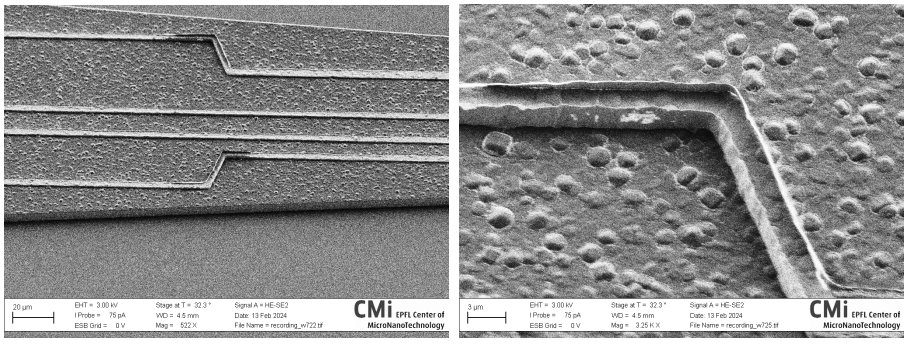


Figure 4.28: SEM images after the etching of the recording layer.

4.2 Probes bending

The bending process assumes a pivotal role in the overall procedure, primarily due to the inherent delicacy of the probes involved. The strategic application of force to a relatively resilient segment of the probe emerges as a crucial technique, mitigating the potential hazards associated with shank breakage or unintended detachment from the pad.

In the initial phase, characterized by a 45-degree bend, the objective transcends mere angular adjustment. This deliberate bend not only imparts a measure of stability but also ensures uniformity in the angular relationship between the two shanks and the chip. This nuanced approach is a deliberate departure from a hasty, one-shot bending process, which could compromise the structural integrity of the probe.

However, the initial bending stage introduces its own set of challenges. The imperative of precision in probe placement, centering the chip within the central part of the opening, and orchestrating a uniform bend across both shanks underscores the intricacies inherent in this critical step. The avoidance of a unilateral shank bend becomes paramount, requiring a meticulous approach to guarantee a harmonious and symmetrical outcome.

As the procedure progresses to the second and final bending phase (refer to figure 4.29), the landscape shifts. With a foundation of stability and uniformity established in the previous step, this subsequent stage assumes a less critical stance. The culmination of efforts in the earlier phase manifests in a more manageable and controlled execution, marking a notable contrast to the intricacies encountered in the initial bending process.

The bent probes were subsequently subjected to SEM inspection. Placing the probes on a carbon pad facilitated SEM imaging, despite the limited practicality in inserting the micrometric probe into the chamber. Through SEM images, the outcomes of the bending process were assessed, focusing on the integrity of the shank and the consistency of silicon thickness at the tip and pad.

From SEM images (figure 4.30), several important points regarding the bending of the shanks, can be highlighted.

Firstly, the aluminum material used for the shank proved to be sufficiently flexible, which is one of its primary characteristics. This flexibility enabled the complete bending of the shank without detachment from the pad (figure 4.31). The inherent flexibility of aluminum is advantageous in this context as it allows the shank to undergo the necessary bending without compromising its structural integrity or causing detachment from the pad.

Moreover, the absence of observed problems at the pad region indicates the effectiveness of the bending process. This suggests that the bending procedure was executed with precision and care, ensuring that the shank maintained its connection

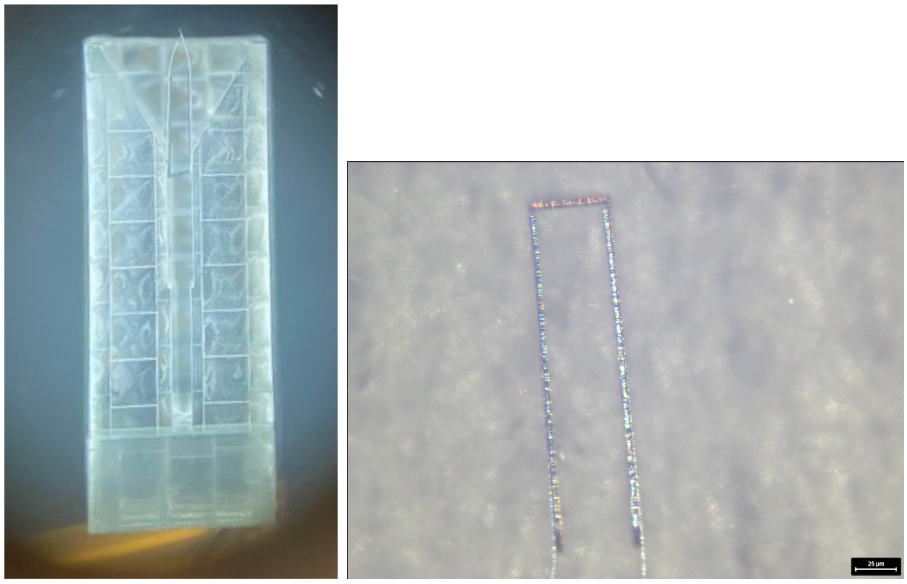


Figure 4.29: Final probe bending.

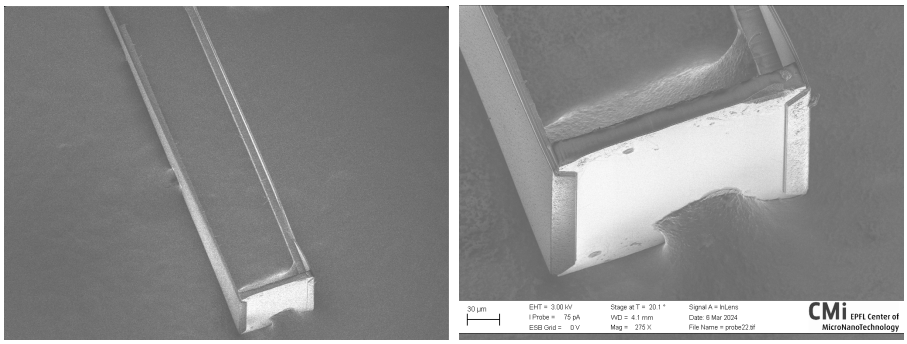


Figure 4.30: SEM images of the bent probe.

with the pad throughout the bending process. The successful integration of the shank with the chip at the pad region is crucial for the overall functionality and reliability of the probe.

This approach provides a crucial visual assessment of the bending process quality, thereby contributing to the understanding of the reliability and compliance of the bent probes.

In Figure 4.32, an image of the bent probe is presented, providing a visual comparison with the size of a human finger.

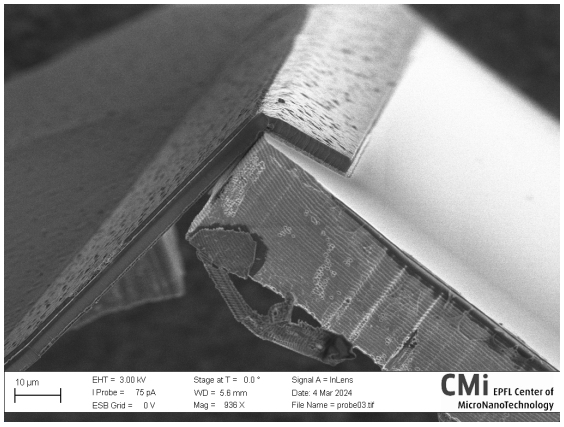


Figure 4.31: Optical microscope inspection of the released and bent probe with 30 μm trench.

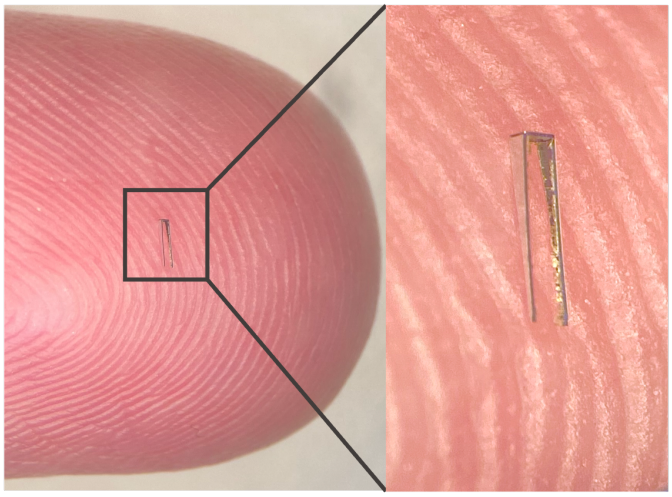


Figure 4.32: Bent probe compared with human finger.

4.3 Probes Implantation

Following the bending phase, the robustness of the probes was assessed by inserting them into an agarose phantom, created by boiling and subsequently solidifying a 0.6% agarose in DI water. The agarose phantom serves as a simulation of brain tissue, with the probe inserted into it while applying uniform pressure at the pad. The implantation procedure proved successful, as no deformations, breakages, or deflections of the shank were observed.

The choice to employ an agarose phantom for robustness evaluation stems from its ability to mimic the properties of brain tissue, providing a realistic environment for

assessing the probe's performance. Agarose, being a biocompatible and transparent material, allows for visualization and inspection of the probe within the phantom. The 0.6% concentration in DI water ensures a gel-like consistency, replicating the soft and pliable nature of brain tissue.

The success of the implantation is crucial in affirming the structural integrity of the probes post-bending. The absence of any noted deformations, breakages, or deflections in the shank during the robustness evaluation suggests that the bending process did not compromise the overall stability of the probes. This outcome reinforces the reliability of the bending technique employed, as it demonstrates the probes' ability to withstand realistic conditions without adverse effects.

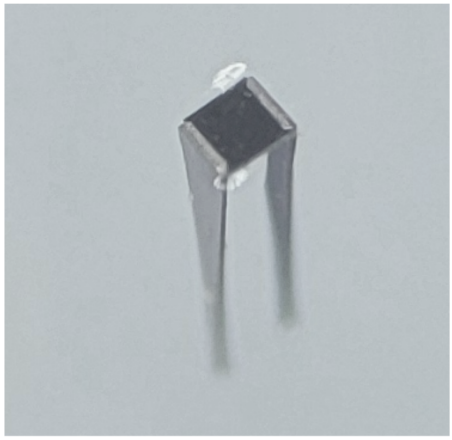


Figure 4.33: Optical microscope photo of the bent probe after implantation.

Chapter 5

Conclusions

Brain stimulation emerges as one of the most effective methodologies for treating blind patients. In addition to external electronics processing images captured by a camera into pulses, cortical visual prostheses also require the fabrication of microelectrodes to be implanted in the visual cortex. This thesis introduces a post-CMOS fabrication method for cortical visual prosthesis probes, addressing challenges associated with manually integrating the CMOS chip onto implantable probes.

The initial part of the thesis focuses on the microfabrication of the probes, featuring a silicon chip mimicking the CMOS chip and two shanks positioned on opposite sides of the chip, adhering to requirements for miniaturization, integrity, and biocompatibility. Following microfabrication, the shanks were bent by 90 degrees using a custom-designed device, which I engineered and manufactured using a nanometric precision 3D printer. The design of the device necessitated careful analysis regarding the area where force is applied to prevent probe breakage.

Upon completion of probe fabrication and bending, their robustness was successfully validated and confirmed through implantation in agarose gel mimicking brain tissue, substantiating potential in vivo applications of these probes.

5.1 Limitations and Unconsidered Factors in Fabrication

One of the primary limitations in the microfabrication of electrodes is the significant amount of silicon wastage. From a 380 μm silicon wafer, electrodes around 30 μm thick are typically produced by removing a considerable portion of the silicon through grinding and deep silicon etching steps. Additionally, the absence of using a mask during photolithography steps poses challenges in achieving precise alignment between the different layers. This alignment is crucial due to the small size of the

electrodes, where even minor misalignments can become problematic. Furthermore, the lack of techniques to release stress during layer deposition on the front side often results in partial bending of the electrode tips. To address this issue, backside designs with silicon support extending to the tip are employed to provide stability and alleviate bending concerns.

To fully achieve the objectives of the project, it is essential to initiate the fabrication process using a wafer containing CMOS chips. This initial step ensures the incorporation of advanced electronic functionalities into the microelectrode probes, which is crucial for their effective operation. However, it is important to note that this aspect was not addressed in the development of this thesis.

While starting the fabrication process with a CMOS wafer offers advantages such as streamlined integration and compatibility with existing CMOS processes, the focus of this thesis was on post-CMOS fabrication. This decision was motivated by the aim to demonstrate the feasibility and potential of this alternative approach.

Acknowledging the omission of consideration for starting with a CMOS wafer highlights a limitation in the scope of this project. Nevertheless, this limitation provides valuable insights for future research endeavors. It emphasizes the significance of exploring methods to integrate CMOS technology into the fabrication process, which holds promise for enhancing the performance and functionality of cortical visual prosthesis probes in future applications [79].

5.2 Future Developments

This section explores potential avenues for future developments and advancements in the field. Key areas for improvement and innovation will be identified, aiming to enhance the performance, reliability, and applicability of cortical visual prosthesis probes. Through targeted research and technological advancements, solutions to existing challenges will be sought, paving the way for transformative breakthroughs in neuroprosthetics

- **Substitution of Parylene backside coating with SiO_2**
  The substitution of Parylene with another insulating material can solve the problem releated to the cross etching. However, using only SiO_2 would make the release of the probes too complex. An alternative approach involves the combination of both SiO_2 and parylene. To address the issue of probes sticking during release due to naked parylene on the backside during frontside etching, a protective layer of 50 nm SiO_2 can be applied. This additional SiO_2 layer prevents parylene etching on the backside, allowing the frontside etching to proceed. However, complications arise in the coating process. PECVD, known for ideal uniformity, is unsuitable due to its incompatibility with the parylene on the frontside. Sputtering should be utilized, but challenges may arise in

achieving uniformity while depositing a very thin layer.

- **Bending System**
  The current bending system relies heavily on the operator, resulting in poor reproducibility and being a time-consuming method.

- **Study of the Force needed and generated during the implantation**
  Studying the force required and generated during implantation can be useful for optimizing the process and considering the design of the probes, allowing for the optimization of geometry to minimize the required force and consequently the damage to brain tissue.

By addressing these challenges, the thesis sets the stage for advancing and optimizing the proposed method in the fabrication of cortical visual prosthesis probes. These innovations not only overcome existing hurdles but also chart a promising trajectory for the development of reliable and effective implantable probes. Such advancements hold the potential to significantly contribute to the field of neuroprosthetics, aligning with the broader goal of restoring vision in individuals with visual impairments. The proposed method, refined through the resolution of identified challenges, emerges as a crucial step towards realizing tangible benefits for patients and fostering continuous progress in the realm of visual prosthetics not relying on powered implantable external units and wired connections.

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