Master's degree in
Micro and Nanotechnologies for Integrated Systems

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Design of radiation-tolerant linear regulators in a high-voltage 0.18um technology

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Master's degree thesis

Supervisors:
Dr. Stefano Michelis
Prof. Adil Koukab
Prof. Gianluca Piccinini

Candidate:
Roberto Musio

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Acronyms

DD Displacement damage.

ELT Enclosed-layout transistor.

LDMOS Laterally-diffused metal-oxide semiconductor.

MOSFET Metal-oxide semiconductor field effect transistor.

OTA Operational trans-conductance amplifier.

PSRR Power supply rejection ratio.

SEE Single event effects.

TID Total ionizing dose.

UVLO Under-voltage lockout.

Abstract

The power management within the Large Hadron Collider (LHC) is a particularly challenging task due to the power demands, the cooling capabilities and the constraints on area and volume. Notably, the DCDC team ([1]) at CERN works on power converters which are able to withstand extremely high levels of radiations and high magnetic fields.

This thesis contributes to the R&D efforts aligned with the forthcoming *long shutdown 4 (LS4)*, which is scheduled for approximately a decade from now and which will allow for a technological upgrade of CERN experiments. An increased luminosity for the accelerator is targeted and larger supply currents are required for front-end circuits: in order to mitigate power losses, DC/DC converters are placed in close proximity to the front-end stage, where radiation levels are expected to reach $\approx 200\ Mrad$. Therefore, commercial components are not suitable for such a harsh environment and custom ASICs (Application Specific Integrated Circuits) must be tailored to CERN's unique requirements.

The project developed in this thesis revolves around the design of three linear regulator in the $48\ V \rightarrow 5\ V$ DC/DC buck module, ensuring optimal power distribution across its distinct voltage domains. The linear regulators step down the supply voltage through the following conversion sequence: $48\ V \rightarrow 5\ V$, for the GaN (Gallium Nitride) switches of the buck converter; $5\ V \rightarrow 3.3\ V$, for the gate drivers; $3.3\ V \rightarrow 1.8\ V$, for the control circuitry.

The impact of radiation-induced degradation on the transistors (i.e., total ionizing dose, displacement damage, leakage) has been considered through the creation of dedicated radiation corners, which were subsequently integrated into the simulation environment of the CAE tools. Experimental measurements informed this process, also leading to the development of behavioral Verilog-A modules designed to describe these phenomena.

Finally, the layout process exploited enclosed-layout transistors (ELTs) and a model describing their electrical characteristics, i.e., their $\frac{W}{L}$ ratio, has been proposed. This model was introduced to address situations involving transistors with large channel lengths (L), such as those where precise matching is paramount.

Abstract

La distribuzione di potenza all'interno del Large Hadron Collider (LHC) è un compito particolarmente impegnativo a causa dei livelli di potenza richiesti, delle capacità di raffreddamento e dei vincoli di area e volume relativi ad ogni modulo. In particolare, il team DCDC ([1]) presso il CERN lavora su convertitori di potenza in grado di resistere a livelli estremamente elevati di radiazioni e a campi magnetici intensi.

Questa tesi si colloca nell'ambito del R&D (ricerca e sviluppo) relativo al *long shutdown 4 (LS4)*, previsto tra circa dieci anni e che permetterà un miglioramento tecnologico degli esperimenti del CERN. In questa prospettiva, si punta ad un aumento della luminosità dell'acceleratore e son richiesti livelli di corrente più elevati per i circuiti di front-end. I convertitori DC/DC saranno posizionati in una zona nella quale si prevede che i livelli di radiazioni raggiungano i 200 $Mrad$. Per questo motivo, i circuiti integrati (IC) che vengono impiegati in queste condizioni devono essere realizzati specificamente sulla base delle esigenze tecniche del CERN.

Questo lavoro di tesi si concentra sulla progettazione di tre regolatori lineari, che faranno parte del convertitore buck da 48 V a 5 V, garantendo una distribuzione ottimale della potenza ai diversi domini di tensione. Gli stadi di conversione relativi ai regolatori lineari sono i seguenti: da 48 V a 5 V, per gli interruttori GaN (nitruro di gallio) del convertitore; da 5 V a 3.3 V per i driver dei gate; e da 3.3 V a 1.8 V per il controllore.

Le radiazioni inducono una degradazione dei transistor (total ionizing dose, displacement damage e leakage current) e, a partire da dei dati sperimentali, si sono sviluppati dei modelli specifici per descrivere questi fenomeni attraverso dei moduli in Verilog-A. Successivamente, questi ultimi sono stati integrati nell'ambiente di simulazione del tool CAE (computer-aided engineering).

Infine, si è curata anche la fase di layout dei circuiti citati e si è proposto un modello che descriva le caratteristiche elettriche equivalenti dei cosiddetti "enclosed-layout transistor" (ELT), ottenendo una modellizzazione accurata anche nei casi di alti valori di lunghezze di canale (L) dei transistor.

Résumé

La gestion de la puissance au sein du Grand Collisionneur de Hadrons (LHC) représente une tâche particulièrement exigeante en raison des demandes en puissance, des capacités de refroidissement et des contraintes en termes d'espace et de volume inhérentes à chaque module. Notamment, l'équipe DCDC ([1]) au CERN travaille sur des convertisseurs de puissance capables de résister à des niveaux extrêmement élevés de radiations et de champs magnétiques intenses.

Cette thèse s'inscrit dans le cadre des efforts de Recherche et Développement (R&D) liés à la future *long shutdown 4 (LS4)*, prévue dans environ une décennie, et qui permettra une amélioration technologique des expériences menées au CERN. Dans cette perspective, l'accent est mis sur l'augmentation de la luminosité de l'accélérateur et des courants d'alimentation plus élevés sont requis pour les circuits en amont. Les convertisseurs DC/DC seront positionnés dans une zone où les niveaux de radiation atteindront environ 200 $Mrad$. Pour cette raison, les circuits intégrés (CI) utilisés dans de telles conditions doivent être spécifiquement conçus pour répondre aux besoins techniques du CERN.

Ce travail de thèse se concentre sur la conception de trois régulateurs linéaires, qui feront partie du convertisseur buck de 48 V à 5 V, assurant une distribution optimale de la puissance dans les différents domaines de tension. Les étapes de conversion liées aux régulateurs linéaires sont les suivantes : de 48 V à 5 V, pour les interrupteurs GaN (nitrure de gallium) du convertisseur ; de 5 V à 3.3 V pour les pilotes de gates ; et de 3.3 V à 1.8 V pour le régulateur.

Les radiations induisent une dégradation des transistors (total ionizing dose, displacement damage et leakage current) et, à partir de données expérimentales, des modèles spécifiques ont été développés pour décrire ces phénomènes à l'aide de modules Verilog-A. Ensuite, ces derniers ont été intégrés dans l'environnement de simulation de l'outil CAE (ingénierie assistée par ordinateur).

Enfin, la phase de layout a également été prise en compte, et un modèle décrivant les caractéristiques électriques équivalentes des transistors "enclosed-layout" (ELT) a été proposé, obtenant ainsi une modélisation précise même dans les cas de valeurs élevées de longueurs de canal (L) des transistors.

1 Introduction

1.1 CERN

CERN (*Conseil Européen pour la Recherche Nucléaire*) stands globally as a leading institution of particle physics research. It was established in 1954 in Meyrin, a Swiss city close to the French border.

CERN's particle accelerators propel charged particles to nearly the speed of light in order to explore the fundamental components of matter and the forces that govern their interactions.

Central to CERN's arsenal is the Large Hadron Collider (LHC), which is characterized by a 27-kilometer circular pathway. As a collider, it is used to accelerate two opposing particle beams through the employment of superconducting magnets and other accelerating components. When the beams reach the required energy, they are led to collision at designated collision points within CERN's experiments (ALICE, ATLAS, CMS, and LHCb). The aftermath of these high-energy collisions is meticulously captured by detectors, providing great insights about the subatomic world: data on the position, charge, speed, mass, and energy of the particles created by the collisions is collected.

The detectors work in a high-radiation and high magnetic field environment, so that they demand a stable and radiation-resistant power distribution. The DCDC Team ([1]) in the Microelectronics section at CERN takes care of the intricate network of switching converters, carefully engineered to minimize the power losses and minimizing the area consumption of their modules, following the stringent requirements for the CERN's experiments. GaN (Gallium Nitride) devices are exploited as power switches due to their advantages with respect to silicon in terms of on-resistance, voltage ratings and switching speed, ultimately leading to reduced power losses. Moreover, they are characterized by optimal radiation characteristics.

The $48\ V \rightarrow 5\ V$ step-down converter stage represents the framework in which this work is carried out. Specifically, this thesis focuses on the analog blocks developed by the author (i.e., the linear regulators), while it is to be acknowledged that the final buck converter module will be the result of the endeavors of many others contributors and team members (the controller, the band-gap circuit, the beta-multiplier circuit, the gate driver circuits and so on).

1.2 Buck converter

Figure 1 illustrates the schematics of a switching regulator (buck converter) module. Two switches (HS and LS) are driven with opposite phases and with a certain duty cycle. The phase node (Ph) is then periodically shorted either to ground or to the supply voltage through the switches, so that its average value V_{Ph}^{DC} is

$$V_{Ph}^{DC} = V_{buck}^{DC} = \frac{1}{T_s} \int_0^{T_s} V_{Ph}(t)\ dt\ = D \cdot V_{in} \tag{1}$$

where D represents the duty cycle, T_s is the switching period and V_{in} is the supply

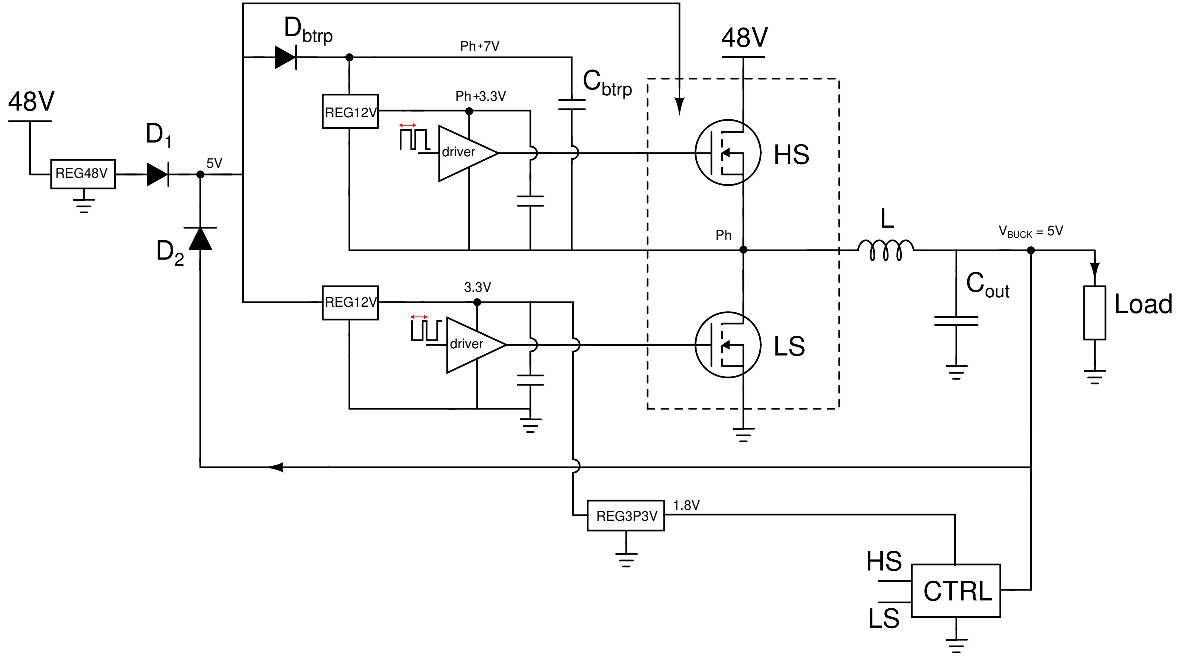


Figure 1: Buck converter

voltage. The inductor L and the output capacitor C_{out} form a low-pass filter with a cut-off frequency much smaller than the switching frequency $f_s = \frac{1}{T_s}$, hence the DC component of the output node V_{buck}^{DC} (here $5V$) is the same as that of the phase node. It is clear from eq. 1 that the output voltage may be controlled through the duty cycle. However, given a fixed duty cycle, the output voltage may vary due to perturbations on the supply voltage or variations in the load. Therefore a controller circuit (CTRL) is needed, so that these sources of variation are compensated for. The regulation mechanism is the following: when the V_{out} is lower than it should be, the high-side transistor (HS) is kept on for a longer period of time (increased duty cycle) and some energy may flow from the power supply (48V) to the output node through the inductor, charging the output node (V_{buck}); conversely, the duty cycle is reduced in order to discharge the output node.

In order to reduce the switching losses of the system and to increase its power efficiency, the switches are commercial HEMT-GaN (gallium nitride) transistors. They are also well-suited for their intrinsic radiation hardness. A bootstrap circuit (D_{btrp} and C_{btrp}) enables the high-side gate driving, given that the phase node (PH) is around 48V when HS is on.

The linear regulators (Reg) provide the voltage and current to the circuits within the buck converter module, but they are quite inefficient due to the high conversion ratios they have to handle, as it will be explained later. Therefore, the diodes D_1 and D_2 represent a simple (passive) solution of *recirculating* the current within the system, so that the load current of the lossy linear regulators is rather provided by the efficient switching regulator as soon as the nominal output voltage is reached, increasing the overall power efficiency.

As it is clear from figure 1, at least three different linear regulators are needed for the

operation of the the switching regulator and they are the focus of this thesis. The input supply voltage is 48V, which is still under the ELV (extra-low voltage) specification for safety handling. The recent trend aims at increasing the input voltage to the system so that the cables that distribute the power from the outside to the radiation-intensive environment contribute to a lesser degree to the (resistive) losses, by decreasing the current through them.

The conversions achieved by the three regulators designed during this thesis are the following:

1. REG48V, $48\ V \rightarrow 12\ V$(or $5\ V$) with a maximum current load of $I_{load} = 100\ mA$. It allows for the recirculation of current through D_1 and D_2, and it feeds the internal circuitry of the GaN chip.

2. REG12V, $12\ V$(or $5\ V$) $\rightarrow 3.3\ V$ (either with respect to ground for the LS or to the phase node Ph for the HS), with a maximum current load of $I_{load} = 10\ mA$. It supplies the drivers.

3. REG3P3V, $3.3\ V \rightarrow 1.8\ V$ with a maximum current load of $I_{load} = 10\ mA$. It feeds the analog and digital circuitry inside the controller.

Every linear regulator must ultimately have a large capacitor attached to the output node, in order to reduce the voltage fluctuations that would take place as a response to the large dynamic currents drawn by the downstream circuitry.

Due to the high-voltage handling, a commercial 180 nm HV technology has been employed, exploiting both LDMOS (laterally-diffused MOS) and low-voltage MOSFETs. Moreover, a very good insulation is required between the voltage domains and, conveniently, the chosen technology provides DTIs (deep trench insulation) and back to back pn junctions between insulated devices (the simplified device structure is sketched in figure 8).

1.3 Linear regulators

A linear regulator is a feedback-loop circuit that steps down the input supply voltage V_{in} and provides a stable V_{out}, regardless of the noise on V_{in} and its current load conditions. Only series regulators are taken into account in this thesis, due to superior efficiency performance with respect to the shunt topology. This circuit exploits the so-called *pass element* as a means to keep the output voltage V_{out} constant, driving accordingly the pass transistor.

Figure 2 shows a simplified schematics of a linear regulator. If the OTA is considered to be ideal, then the feedback loop adjusts the overdrive of the pass transistor (transistor M1), so that the output voltage mirrors the accurate reference voltage V_{ref} through an up-scaling factor that is provided by the resistive network. The working principle of the feedback loop is the following: when V_{out} is smaller than it should be, then $V_{fb} < V_{ref}$, the output of the OTA decreases, increasing the V_{sg} of M1 and allowing a large current to charge the output node. A simplified DC analysis is proposed:

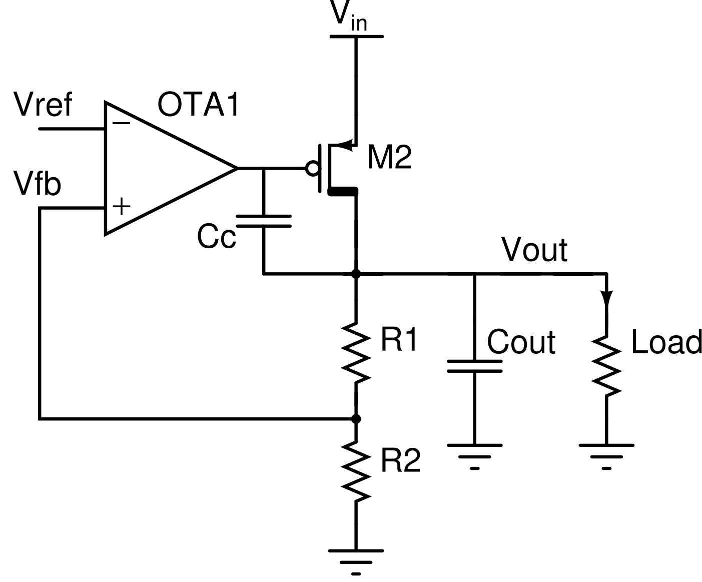


Figure 2: Schematics of a linear regulator employing a p-type pass transistor.

$$V_{out} = A_{OTA} \cdot (V_{ref} - V_{out} \cdot \frac{R_2}{R_1 + R_2})$$
$$V_{out} = V_{ref} \cdot \left(1 + \frac{R_1}{R_2}\right), \quad if\ A_{OTA} \rightarrow \infty \tag{2}$$

A large output capacitor C_{out} provides a stable output of the system, i.e., a low impedance node in AC, so that the power supply is as ideal as possible from the point of view of the load circuit, i.e. it resists ripples. The *line regulation* represents the shift in the V_{out} given a change in the V_{in}, i.e. $\frac{\Delta V_{out}}{\Delta V_{in}}$. The load regulation describes what happens to the output voltage when a change in the current load takes place, i.e. $\frac{\Delta V_{out}}{\Delta I_{load}}$.

Stability analysis The small-signal model of the open-loop linear regulator is presented in figure 3. The nodal equations regarding *net 1* and *net 2* are:

$$-gm_I v_y + v_x g_{dsI} + v_x s C_{n1} + (v_x - v_{out}) s C_c = 0$$
$$g_{mII} v_x + (v_{out} - v_x) s C_c + \frac{v_{out}}{R_{load}//(R_1 + R_2)} + v_{out} s C_{out} = 0 \tag{3}$$

where the OTA is modeled through a trans-conductance g_{mI} and a finite output conductance g_{dsI}. The channel length modulation of the pass transistor is neglected since the output is a low impedance node.

By solving the system of equations 3, by assuming $g_{dsI} \ll g_{mII}$ and $C_{n1} \ll C_{out}$ and C_c, the following transfer function is obtained, which is the loop gain of the system.

$$\frac{v_z}{v_y} = \frac{R_2}{R_1 + R_2} \cdot \frac{g_{mI} r_{oI} g_{mII} r_{oII} (\frac{s}{\omega_z} - 1)}{s^2 C_{out} C_c r_{oI} r_{oII} + s(g_{mII} C_c r_{oI} r_{oII} + C_c r_{oI} + C_{out} r_{oII}) + 1} \tag{4}$$

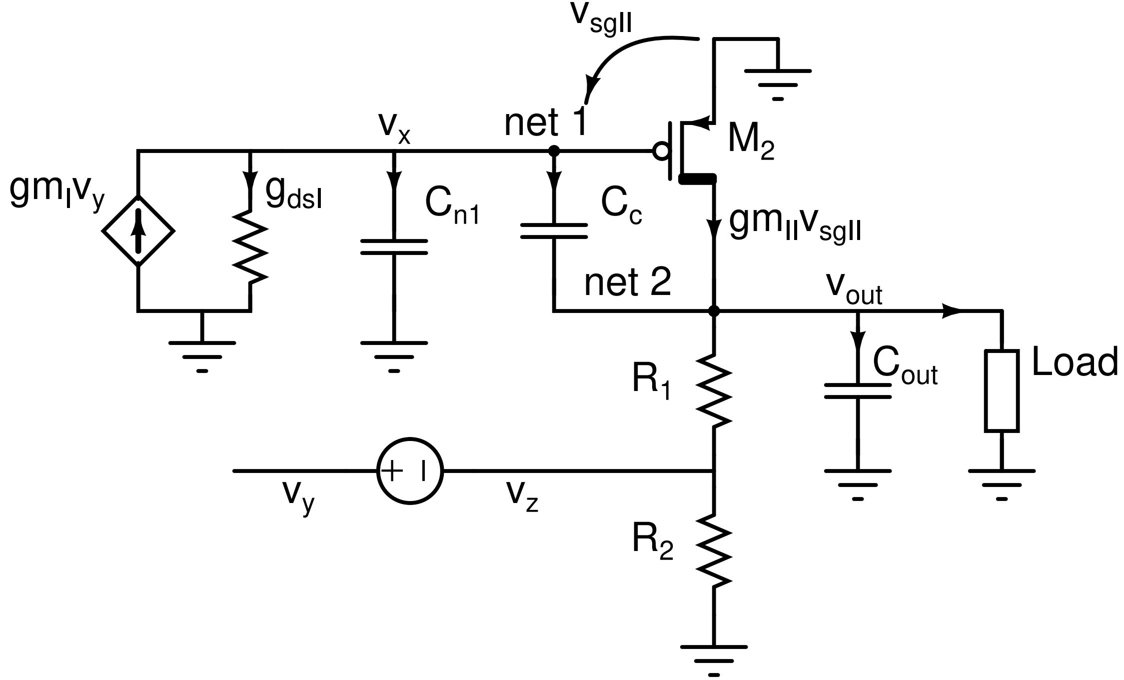


Figure 3: Small signal circuit of the open-loop linear regulator in figure 2.

where ω_z is a positive zero and it is equal to

$$\omega_z = \frac{g_{mII}}{C_c} \tag{5}$$

and where $r_{oI} = \frac{1}{g_{oI}}, r_{oII} = (R_1 + R_2)//R_{load}$.

The positive zero in eq. 5 is critical for the stability of the system, as it would tend to decrease the phase margin in the case it is contained within the unit-gain bandwidth (ω_{BW}) of the circuit. Indeed, the positive-zero frequency should be sufficiently high so that $\omega_z \gg \omega_{BW}$. Nevertheless, as the trans-conductance of the pass transistor (g_{mII}) is degraded during the radiation exposure, the zero would be shifted towards lower frequencies and it might have a negative impact on the stability. Along the same line of reasoning, the scenario when $I_{load} = 0$ should be considered carefully, as the g_{mII} is at its minimum.

By assuming the two poles of the systems are sufficiently far apart from each other,

$$\begin{aligned} \omega_{dom} &= \frac{1}{r_{oI} C_c (g_{mII} r_{oII} + 1) + C_{out} r_{oII}} \\ \omega_{non-dom} &= \frac{r_{oI} C_c (g_{mII} r_{oII} + 1) + C_{out} r_{oII}}{C_{out} C_c r_{oI} r_{oII}} \end{aligned} \tag{6}$$

It is clear from eq. 6 that the dominant pole is the result of competing contributions, i.e., the output capacitance and the Miller compensation capacitance. When no current load is present at the output of the linear regulator, the amplification factor due to the

pass transistor is small, so that the dominant pole is predominantly determined by the large output capacitor, i.e., the Miller effect is negligible. More precisely, the time constant associated with the large C_{out} is larger than that associated with the gate of the pass transistor. As a limiting case, the Miller capacitance is completely neglected, while the C_{n1} is taken into account. Under these assumptions, the poles of the system are easily found by inspection as follows (see eq. 7):

$$\begin{aligned} \omega_{dom}(I_{load} = 0) &\approx \frac{1}{C_{out} r_{oII}} \\ \omega_{non-dom}(I_{load} = 0) &\approx \frac{1}{C_{n1} r_{oI}} \end{aligned} \tag{7}$$

In a real scenario, both C_c and C_{n1} would influence the poles, but it has been observed from simulations that, when no load is attached and when $C_{out} \approx 1\ \mu F$, the C_{n1} represents by far the predominant contribution to the non-dominant pole.

Conversely, when the current load is maximum, the Miller compensation is the most influential contribution (see eq. 8).

$$\begin{aligned} \omega_{dom}(I_{load} \approx 10mA) &\approx \frac{1}{r_{oI} r_{oII} g_{mII} C_c} \\ \omega_{non-dom}(I_{load} \approx 10mA) &\approx \frac{g_{mII}}{C_{out}} \end{aligned} \tag{8}$$

Since stability is to be achieved throughout all the operating conditions, this design methodology has been followed for the three regulators: firstly, the system is analyzed with no load and the output resistance of the OTA is adjusted so that the non-dominant pole is sufficiently far from the dominant one; secondly, the C_c is adjusted so that the system is stable with the maximum current load ($I_{load} \approx 10mA$). As the C_c is increased, the two poles of the system tend to drift apart from each other, resulting in the well-known phenomenon of *pole splitting*. It is to be noted that these two methodological steps are independent from each other at the first order of approximation, due to the previous observations.

It is interesting to note that, in general, the radiation effects would tend to decrease the stability of the circuit, since the trans-conductance of the pass transistor is severely degraded, reducing the Miller amplification.

Power consumption A linear regulator by itself is extremely power inefficient, even more so when high conversion ratios between the V_{in} and the V_{out} are considered. In fact, if we neglect the bias current (quiescent current) related to the inner workings of the linear regulator itself, the dissipated power is

$$P_{diss} = P_{in} - P_{out} \approx (V_{out} - V_{in}) \cdot I_{out} \tag{9}$$

while the power efficiency is

$$\eta = \frac{P_{out}}{P_{in}} \approx \frac{V_{out}}{V_{in}} \tag{10}$$

An example would hopefully make it clearer. If $V_{in} = 48\ V$, $V_{out} = 12\ V$ and $I_{out} \approx 80\ mA$, just like in the case of the REG48V regulator, the estimated dissipated power would be $\approx 2.88\ W$ and the power efficiency would be 25%. This would impose severe conditions on the heat dissipation system and it would drastically decrease the overall power efficiency of the buck converter module, which is expected to have $\eta > 90\%$. This is the reason why the *recirculating* mechanism for the current was employed.

PSRR analysis The power supply rejection ratio (PSRR) represents the capability of the circuit to not be affected at its output upon perturbations on the input supply voltage V_{in}. It is defined as a small-signal figure of merit and, as a reference, its usual frequency dependence is shown in figure 28. The low frequency part of the PSRR is mainly due to the OTA amplification. For mid frequency range, the PSRR follows OTA frequency response, it reaches a minimum and, then, for the high frequency range the time constant of the output stage (i.e., pass transistor and C_{out}) starts to kick in. Intuitively, for high frequency the output capacitor resists variations of the V_{out}, improving the rejection capability, while the feedback loop cannot compensate for the perturbations since it is usually beyond its unit gain bandwidth.

Since the dip in the PSRR response happens at high frequency, the time constant related to the output node is relevant and it characterizes the charging/discharging process of the output capacitor. Therefore, it is interesting to note that this figure of merit is significantly better when no load is present. In fact, the pass transistor would be characterized by a large equivalent resistance, effectively filtering the V_{in} perturbation.

On the other hand, a large load yields a smaller equivalent resistance for the pass transistor, thus leading to a worse rejection capability (the output stage follows readily the variations in the supply voltage, with a less pronounced RC filtering).

Bandgap reference Any variation on the reference voltage V_{ref} directly affects the output voltage V_{out}, so that a stable, precise V_{ref} is needed: a bandgap reference circuit is thus employed. It consists of a feedback circuit with a stable ON operating point which is ideally not sensitive to PVT variations. This circuit has been developed by the DCDC Team and its inner workings are outside the scope of this thesis.

Beta multiplier The OTA needs a precise current reference internally: this is achieved through a beta multiplier circuit. The topology that has been developed by the DCDC Team reasonably compensates for the power supply and temperature variations, but its simple structure is strongly affected by process variations, most prominently the ones related to the resistances available in the employed technology. The description of this circuit is outside the scope of this thesis.

2 Radiation effects and models

The radiation effects can be divided in two main categories: the cumulative effects, either ionizing (*total ionizing dose*) or non-ionizing (*displacement damage*) effects, and the stochastic (ionizing) effects (*single event effects*) [2].

Ionizing radiation, such as charged particles (e.g. protons, heavy ions, electrons) and certain neutral particles (e.g. photons) can interact with the semiconductor material of a transistor. These interactions result in the creation of electron-hole pairs within the material, degrading the transistor's electrical characteristics. The *Total Ionizing Dose* (TID) is a parameter that describes the cumulative effect of ionizing radiation, by quantifying the amount of energy absorbed by the target material, normalized by the density of the material. It is typically expressed in *rads*, where 1 rad equals $0.01\frac{J}{Kg}$.

The amount of energy deposited in the material by the impinging particle per unit path length is the LET (linear energy transfer).

$$LET = \frac{1}{\rho} \cdot \frac{dE}{dx} \tag{11}$$

where ρ is the density of the material and E is the transferred energy. It is measured in $\frac{MeV \cdot cm^2}{mg}$. The LET parameter is related to the single event effects (SEE), as it determines the amount of electron-hole pairs that are created within the material.

On the other hand, displacement damage affects the crystalline structure of the material. When high-energy particles (e.g. neutrons, silicon and tungsten atoms) interact with the semiconductor lattice, they can impart enough energy to displace atoms from their original positions. This displacement of atoms results in the creation of the so-called Frenkel pairs, which consist of an interstitial atom (an atom located in an unintended position within the crystal lattice) and a vacancy (an empty site where an atom should be).

2.1 Total ionizing dose effects

Trapping mechanisms in oxides The critical area for ionizing radiation in a transistor are the oxides, both the gate oxide and the field oxide (LOCOS or STI). When electron-hole pairs are created, they quickly disappear due to the low substrate resistance. Conversely, when they are created within the gate oxide (see figure 4), electrons have a much larger mobility with respect to holes, differing by five to twelve orders of magnitude. As a consequence, the electric field across the oxide separates the carriers and the electrons drift to the gate in an extremely short time (at the order of ps), while the holes move slowly towards the silicon-oxide interface through a hopping phenomena involving localized states [2]. This phenomenon leads to the trapping of holes near the low-potential edge of the gate oxide, causing an accumulation of positive charge within the gate oxide. Thus, electrons are electro-statically attracted close to the interface on the channel side, increasing the conductivity of n-type transistors and turning off

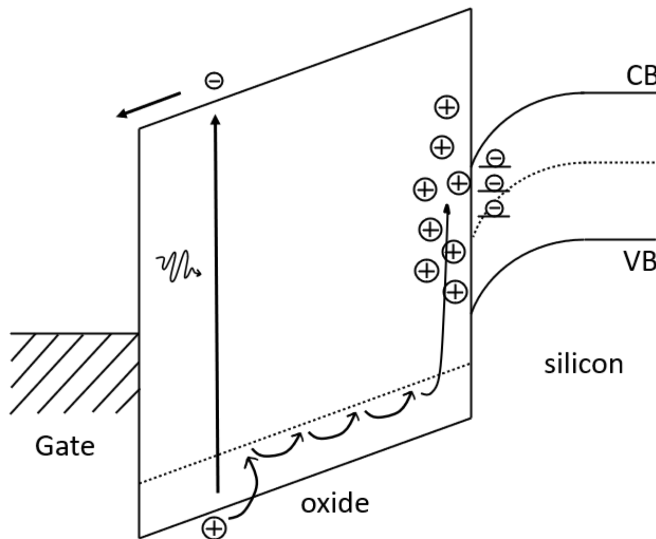


Figure 4: The figure shows the band diagram of a n-type MOS structure, highlighting the hopping transport mechanism of holes within the oxide, the hole accumulation near the Si/SiO_2 interface and the acceptor traps at the interface. Adapted from ref [2].

p-type ones.

Moreover, the radiation also leads to the increase by several orders of magnitude of the number of traps at the Si/SiO_2 interface: a hole may react with a hydrogen atom within the oxide bulk and form H^+, which starts to move through the oxide and de-passivate the interface traps between $Si - SiO_2$. Thanks to experimental results, we can safely assume that the traps below the midgap are donors (when above the Fermi level they release an electron into the valence band, becoming positively charged), while the ones above the midgap are acceptors (when above the Fermi level they accept an electron from the conduction band, becoming negatively charged). Therefore, the later trapping mechanism tends to turn-off the transistors (both p- and n- types), but it is characterized by a very long time constant.

TID degradation The TID effects lead to a shift in the threshold voltage, to a reduction in the I_{on} and to an increased leakage current in n-type devices. The decrease in the threshold voltage is due to the combined effect of the hole accumulation within the oxide and the dynamics of the interface traps. In fact, these two phenomena would lead to a variation in the flat band voltage of the devices, due to the extra charge. The ΔV_{TH} is clearly shown in figure 14, where a p-type LDMOS device has been irradiated with a TID dose of $200 Mrad$. By considering the $I_D - V_D$ characteristics of the same device, figure 14 highlights the degradation of its I_{ON}.

Moreover, the increased presence of interface traps interferes with the transport in the channel, effectively decreasing the mobility of the inversion carriers: this also leads to a degradation of the trans-conductance of the devices.

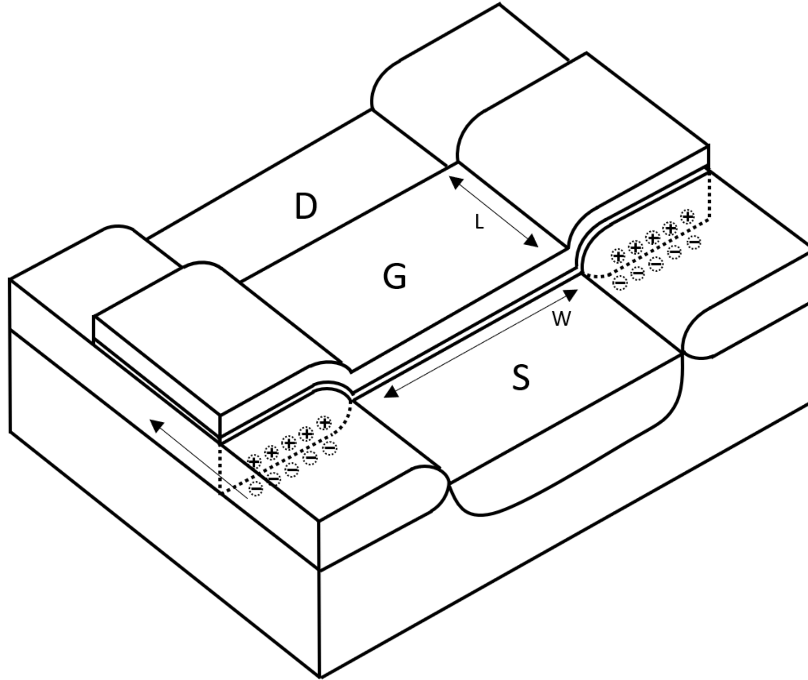


Figure 5: The radiation-induced leakage current path is illustrated. The electric field of the gate results in the accumulation of electrons right below the field oxide (here represented as LOCOS). Adapted from [2].

Leakage current Figure 5 illustrates the origin for the increased leakage current. In fact, the positive charges that accumulate within the STI (or LOCOS in the figure) oxides attract some electrons below the Si/SiO_2 interface creating a parasitic channel in parallel to the inversion layer in the active area. The parasitic channel is weakly controlled by the gate due to the thickness of the STI (or LOCOS), but it becomes relevant at low gate voltages, when the main channel is turned off, thus contributing to the overall leakage. This is the so-called FOXFET (Field OXide FET).

This issue is to be addressed both at the design and layout level. At the design level, it is important to always provide a path to the leakage current towards a low-impedance node, so that no over-voltages might take place when the circuit is turned off. This technique has been employed in all the regulator circuits that are discussed in this thesis and, for instance, it is shown in figure 20, where the diodes effectively clamp the source nodes of transistors $M6, M7$. Nevertheless, this design effort is only due when dealing with high-voltage LDMOS devices, because the leakage phenomenon is completely solved for low-voltage devices at the layout-level.

A layout-level solution for this issue is represented by the *enclosed-layout technique* or *ELT technique* (see figure 6). The source is drawn to surround the poly-silicon and the drain terminal in a central symmetry. As a consequence no field oxide is present between the source and drain. Experimentally, ELT transistors have been observed to present very little leakage current, comparable to the pre-rad levels.

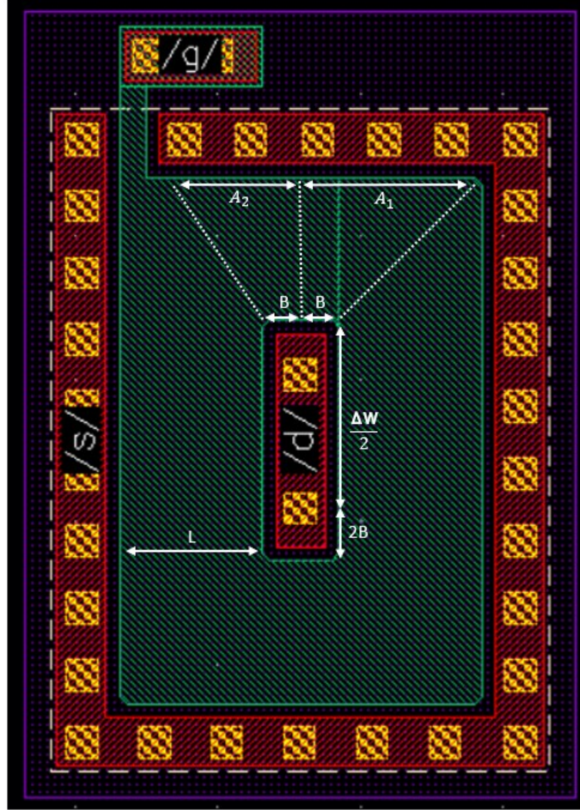


Figure 6: The enclosed layout technique is illustrated, considering a low- voltage nmos device. The purple layer represents the n-type implantation, the red layer the first level of metal, the green layer the poly-silicon, the yellow squares the contacts (either to poly-silicon or to the n-wells) and the white square delimits the active area of the device. STI insulation surrounds the device. B represents half the minimum geometrical dimension of the central hole edge due to DRC (Design Rule Check) constraints. The gate length is L, W_{min} is the minimum achievable equivalent width and $\Delta W = W_{design} - W_{min}$. This layout has been generated automatically by programming a PCell (parametrized cell) in the CAE tool environment.

Nevertheless, the are few disadvantages to their employment ([2], [3]):

1. The modeling of the $\frac{W}{L}$ is challenging;
2. Geometrical limitations to the minimum obtainable $\frac{W}{L}$ ratio, given a fixed L;
3. Tendency to a larger area consumption with respect to a standard transistor, given the same $\frac{W}{L}$ ratio;
4. The device is not symmetrical with respect to the source and the drain;
5. Large parasitic capacitances.

The model of their $\frac{W}{L}$ with respect to the geometrical dimensions has been developed in ref. [2], by differentiating some device sections based on the unequal distribution of the current density and the peculiar flow paths. On the other hand, the minimum

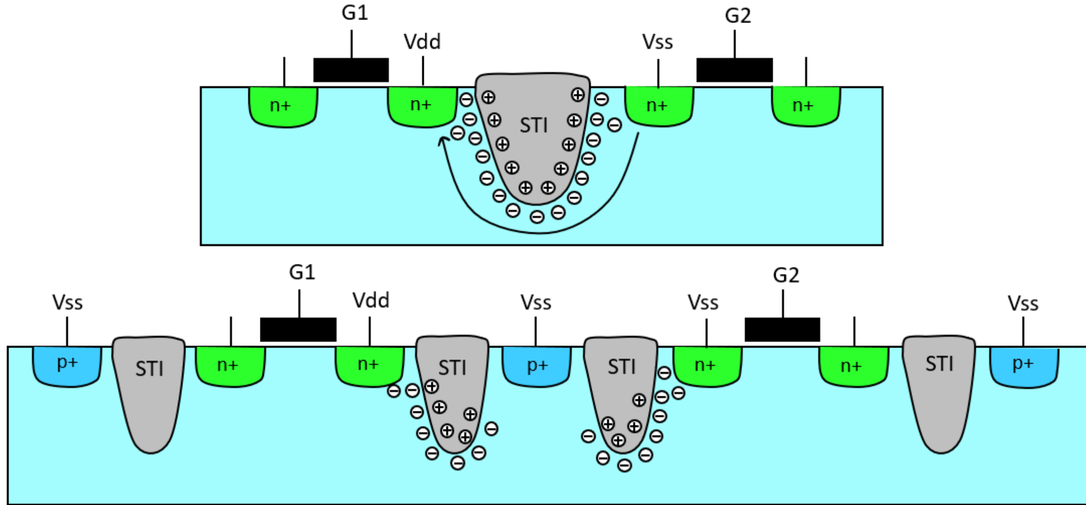


Figure 7: The guard ring technique is illustrated. The guard rings (blue p+ implantations in the bottom figure) enclose the whole devices, it guarantees a good contact to the bulk and it cuts any parasitic path.

metal width, which is fixed by the specific technology, results in a lower limit for the achievable $\frac{W}{L}$.

Here are few detail for the model. The width of the poly-silicon represents roughly the L of the device, while the W is related the perimeter of the gate (see figure 6). The model provides an empirical formula in order to compute the minimum achievable $\frac{W}{L}$ ratio and W_{min} given a fixed L (which corresponds to the smallest possible metal square for the inner drain contact). The required W_{design} is obtained by increasing the perimeter by $\Delta W = W_{design} - W_{min}$ (by stretching either side of the minimum sized cell or both). The check against the provided formula is handled automatically by the LVS (layout versus schematics) tool of the CAE environment and it has been achieved by feeding it some custom rule files. This procedure has been improved throughout the course of this master thesis, by developing a flexible PCell (parametrized cell) using the SKILL script language: when instantiating the cell, the tool automatically creates the layout of the ELT transistor with the right geometrical dimensions so that they correspond to the $\frac{W}{L}$ ratio, W_{design}, L that the user specifies in the schematics.

The model in ref. [4] proves to be accurate when the L of the transistors is relatively small. Nevertheless, large L devices are needed when matching and noise constraints are paramount. For this reason, taking inspiration from this, during this thesis a new model has been developed in order to provide a better description of the device for large L conditions. A brief explanation of this newly developed model is provided in chapter 6.

The experimental data regarding the employed technology was available before this project started and the results have shown the effectiveness of exploiting ELT devices for low-voltage nmos transistors (both 1.8V and 3.3V rated devices). Conversely, the same technique has not been proven to be useful for high-voltage LDMOS transistors, since the ELT ones systematically failed at handling voltages much lower than their

ratings. This phenomenon has also been observed in ref. [5]: test results show how the ELT configuration interferes with the high-voltage handling capability of the LDMOS devices and should be avoided.

Finally, there may also be parasitic paths between two different devices, as it is shown in figure 7. In fact, some electrons are attracted under the STI oxide due to the hole accumulation after the irradiation of the devices. When two n-type terminals of two neighboring devices are at different voltages, the carriers in the parasitic channel are induced to flow, creating a leakage path. This can also happen between n-type tubs (e.g., n-well in a pMOSFET) at different voltage levels. No p-type channel can be created under the STI because only holes can be accumulated within the oxides. A guard ring structure surrounding all the n-type devices solves the mentioned issue as the p+ implantation cuts the leakage path.

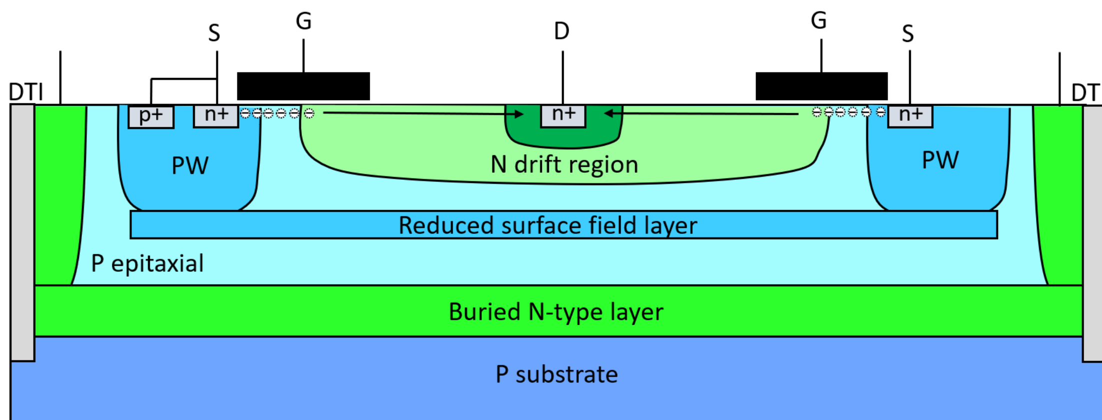
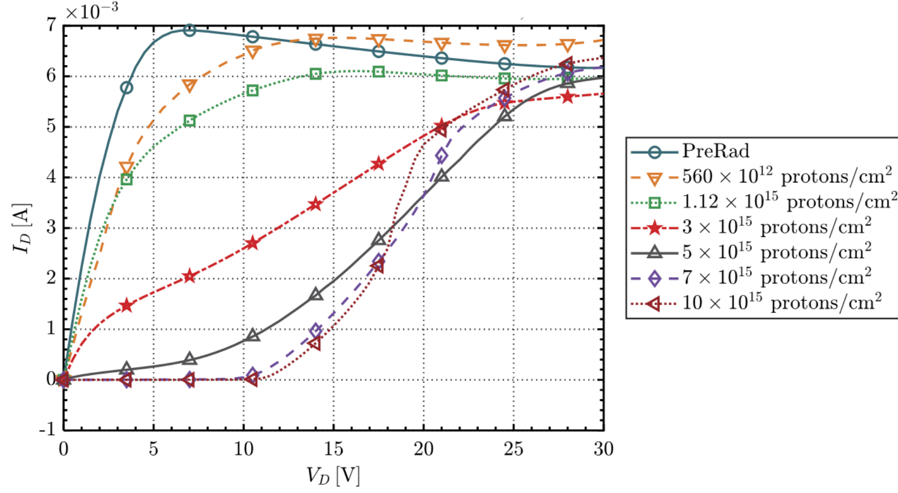


Figure 8: The device structure of a n-type LDMOS devices is depicted. Every isolated device is fabricated within a local P-type pocket (P epitaxial), which is separated from the substrate through a buried N-type layer. Through a positive gate voltage, the electrons are accumulated right below the gate oxide and they drift through a low-doping N-type region before they reach the drain contact.

2.2 Displacement damage

The displacement damage (DD) is related to the damage to the crystalline structure of silicon, as the doping impurities are kicked out of their substitutional site within the semiconducting crystal. This is usually not an issue for advanced nodes, as the doping levels are reasonably high, but it becomes detrimental for high-voltage LDMOS devices (see figure 8). The later devices need a low-doping drift region close to the drain terminal in order to allow for a high breakdown voltage of the transistor: in fact, the low-doping region is able to sustain most of the voltage across the drain and source terminals, limiting the peak of the electric field within the bulk. The displacement of dopants results in an increased resistive behaviour of the transistor, mostly affecting the slope in linear regime of the $I_d - V_d$ characteristics and the I_{on} of the transistor.

This phenomenon has been discussed in ref. [5], where the distortion of the $I_D - V_D$ characteristics of the LDMOS devices is highlighted. Figure 9 shows this behaviour for the transistors employed in this project and figure 10 represents the fitted model for high-voltage transistors. The displacement damage appears to have a more dramatic impact on n-type LDMOS with respect to their p-type counterpart. The damages result in a greatly increased saturation voltage for the transistors with respect to the pre-rad behaviour.



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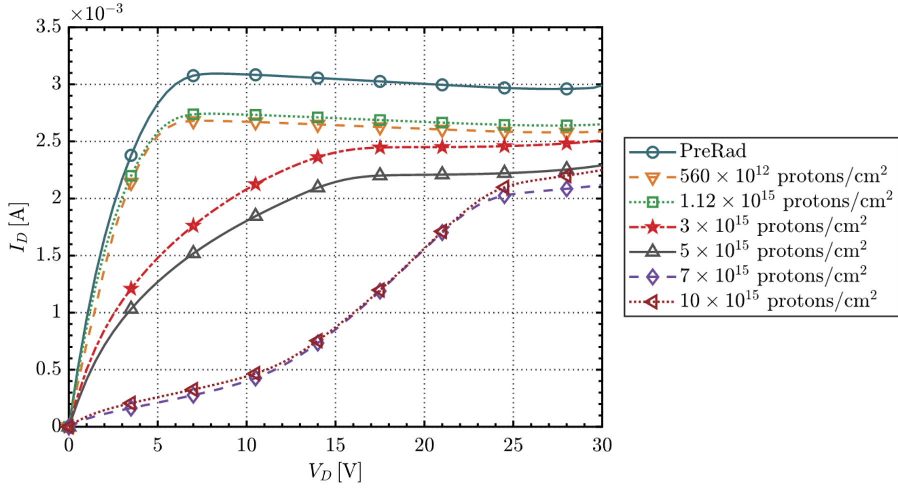
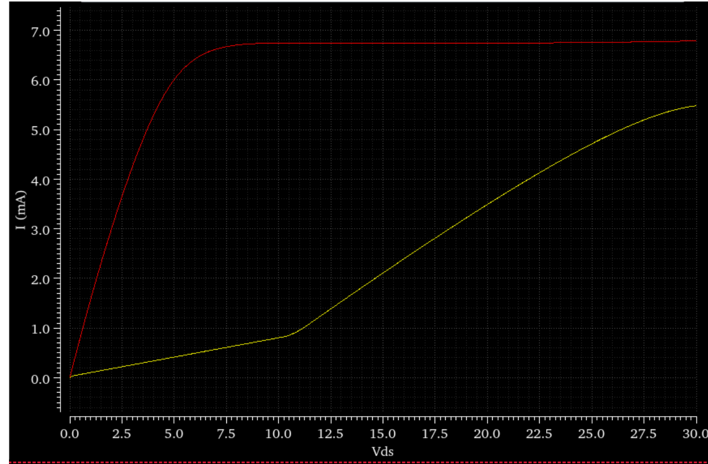


(b)

Figure 9: The measurement results of the $I_D - V_D$ characteristic of the n-type (a) and p-type (b) LDMOS transistors are presented. These results have been obtained by the DCDC team prior to this thesis. The figure shows how the electrical characteristic of high-voltage transistors is distorted at various fluence levels for the displacement damage (DD) phenomenon. The gate bias voltage is $|V_G| = 3.3\ V$. The circuit designed in this thesis can withstand up to $5 \cdot 10^{15} \frac{protons}{cm^2}$ (grey curve). The fitted results are shown in figure 10.



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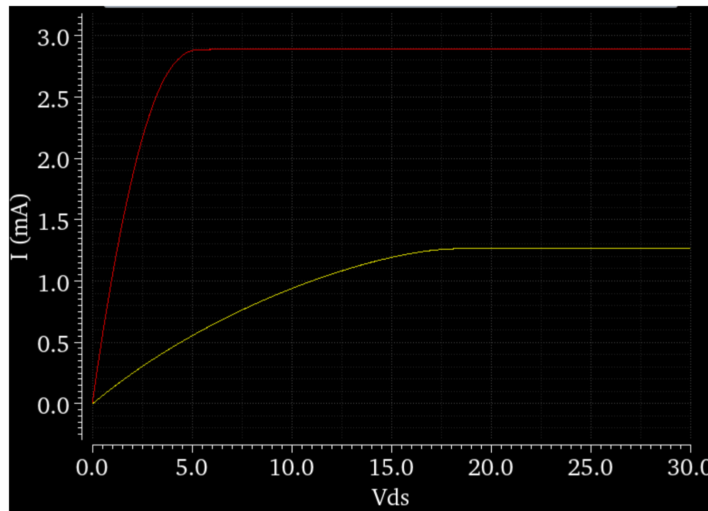


(b)

Figure 10: The figure shows the $I_{DS} - V_{DS}$ characteristics of a n-type (a) and p-type (b) LDMOS transistor. The yellow curve represents the effects of radiations on the electrical parameters with respect to the standard conditions (red curve). In subfigure (a) it is shown that the additional resistive effect introduced by the DD is dominating up to $V_{DS} \approx 28V$. The simulation takes into account a bias $V_{GS} \approx 3.3V$ for n-type and $V_{SG} \approx 3.3V$ for p-type transistors. A displacement damage of $5 \cdot 10^{15} \frac{protons}{cm^2}$ has been considered. Since the irradiation has been carried out with protons, the model takes into account both the TID ($\approx 136 Mrad$) effects and the DD ones.

2.3 Single event effects

A n-type LDMOS transistor is considered as an example for analyzing the so-called *single event transients* (SET). The latter are temporary, short-lived and non-destructive changes in the output of an electronic device, which manifest as transient voltage or current fluctuations that can propagate through the circuit.

When an energetic particle impinges on a device, many electron-hole pairs are created. In the quasi-neutral region of the transistor, the electric field is approximately zero and most of the pairs have enough time to recombine before they separate . Close

to the n-type diffusion well of the drain, a space charge area is present and the electric field is intense, so that it separates the carriers: specifically, in a n-type transistor the electrons drift towards the drain, while the holes towards the source, which is connected to the bulk (low impedance node). As a consequence, the parasitic capacitance between the drain and the bulk is discharged, since the newly created electron-hole pairs compensate the stored charges in the depletion capacitance: instantaneously, the voltage at the drain node decreases.

Analogously in the case of a p-type transistor, this phenomenon tends to increase the voltage at the drain node.

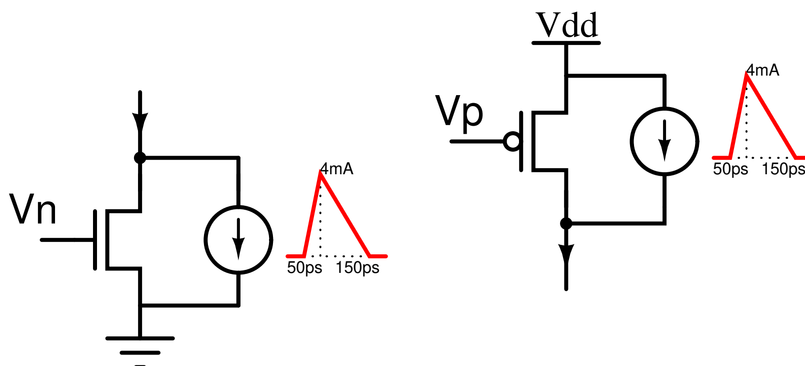


Figure 11: The method for simulating SEE is shown. A triangular current pulse with a peak of 4 mA and duration of 200 ps is injected. The pulse tends to decrease the $|V_{DS}|$ in both n- and p-type transistors, thus decreasing the drain voltage in the n-type transistor and increasing it in the p-type one.

From the simulation point of view, every node of the circuit is independently tested for SET, exploiting a current source with the proper direction shown in figure 11. A SEE would induce an impulsive response on the V_{out} of the regulators, as it is shown in figure 12, due to instantaneous charging/discharging of the gate node of the pass transistor as a consequence of a single event on some other node. It is worth noting that the time response of the feedback loop is much slower than the impulsive single event, so that the latter induces a very fast transient on the voltages of the parasitic capacitances in the circuit. The peak (dip) of the overshoot (undershoot) and the time it takes for the feedback loop to bring the circuit back to steady-state both depend on the operating conditions: when no load is present, the overshoot is the worst condition, because the feedback loop would tend to turn off the pass transistor, opposing the effect of the SEE impulse, and the small feedback current (flowing through R_1, R_2 in figure 2) has to discharge the large C_{out}; on an analogous line of reasoning, when the load is maximum, the undershoot of the output voltage is the worst condition.

The specific shape of the impulse has been extrapolated from experimental data and it is the following: the rise time of the triangular impulse is 50 ps; the peak current value is set to 4 mA; the fall time is 150 ps. The rise and fall time are different because of the different underlying transport mechanisms of the carriers: the fast rising edge is due to

the drift current and to the high electric field, while the slower falling edge is mostly due to a diffusion component of the generated electron-hole pairs. The peak current of the impulse is strictly related to the linear energy transfer (LET) of the impinging particle: the peak of 4 mA has been used for a $LET \approx 40\ \frac{MeV\ cm^2}{mg}$. Due to a certain degree of uncertainty in the shape of the current pulse, also the following scenario is simulated: the total charge is set to be the same as before, while the peak current value is decreased by a factor of ten (400 μA), hence the pulse duration is stretched to 2 ns in total.

Figure 12: Example of a SEE simulation. This specific example considers the REG12V regulator and the graph shows his V_{out}. Every node in the circuit is tested with the proper current direction.

In the case of high voltage devices, the so-called *single event burnout* (SEB) may also take place. The latter is a destructive form of SEE. The electron-hole pairs may multiply in the regions of intense electric field and a self-sustaining avalanche effect might onset. There exists a critical field that a device can sustain without such a breakdown mechanism and it depends on the LET of the impinging particle. The p-type LDMOS devices that have been used in this thesis do not suffer from this issue in the voltage range that has been examined. On the other hand, the n-type ones have been observed to undergo a SEB for $V_{DS} > 30\ V$: nevertheless, this critical voltage stands right at the edge of the safe-operating area of the transistors.

A quenching mechanism may be easily employed at the design level, connecting a series resistance: the large avalanche current induces a significant voltage drop on the resistance, bringing the field within the transistor below SEB critical field value.

2.4 Radiation corner analysis

In order to take into account the radiation effects on the transistors, a describing model has been developed, considering TID and DD effects. The radiation effects are known to

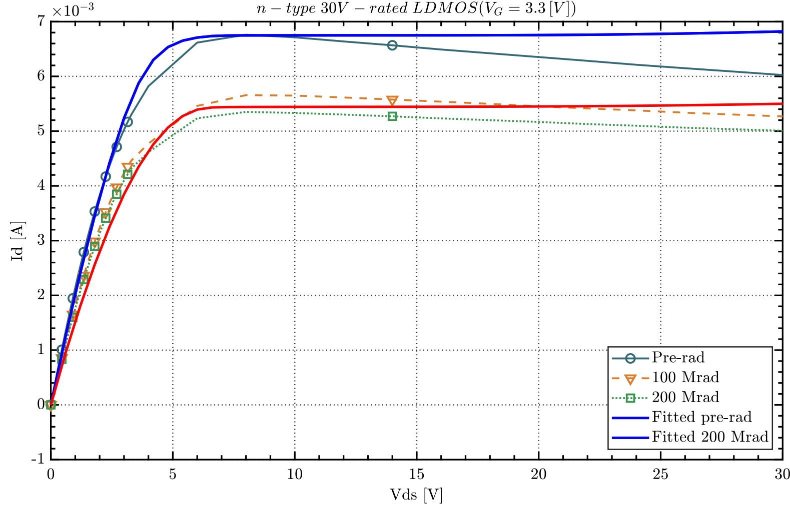
be subject to a large variability among different production lots or even among different foundry production sites: hence, these models just attempt to sketch a worst-case scenario, keeping in mind the limited amount of available data, given how time consuming and financially demanding it is to carry out such measurements.

The variations of the electrical parameters have been fitted from experimental data and inserted into the BSIM4 model that the CAE (computer-aided engineering) software environment exploits for the simulations. The latter is a widely used compact model for MOSFETs and it comprises around 300 parameters [6]. The BSIM4 model also allows for more degrees of freedom, as separate W and L ranges may be described independently. In the light of this, the data coming from devices with different dimensions has been analyzed, extracting the radiation-induced degradation parameters and these values have been exploited to modify the existing process corners and, finally, take into account radiations. The results are considered reliable in that the correction coefficients are reasonably coherent throughout all the devices.

Measurement procedure The measurements were carried out prior to this master thesis by the DCDC team. All the transistors that have been characterized have been irradiated with fixed bias voltages, with $|V_{gs,\,irrad}| = |V_{ds,\,irrad}| = 3.3\ V$. The radiation exposure was temporarily interrupted at specific TID doses, in order to electrically characterize the transistors and track the development of the radiation-related degradation: hence, the $I_D - V_D$ and $I_D - V_G$ characteristics were measured. In the real circuit, no bias voltage is fixed and, for instance, the V_{gs} would follow the V_{th} and attempt to maintain the same current level in the case of cascoded transistors.

TID fitting procedure The fitting procedure that has been considered is the following: firstly, the shift in the threshold voltage is extracted from the measured $I_D - V_G$ characteristics, focusing on the sub-threshold exponential region of the current; then the trans-conductance of the transistors is artificially reduced in order to match the variations in the I_{ON}: this can be achieved either by varying the mobility μ (used for LDMOS device) or through a change in the W and L of the transistor (used for 3.3V-rated p-type devices). Since the process corners of the fabricated device are superimposed on the radiation-related degradation, both the pre- and post-radiation curves are fitted. This methodology provides a well-defined baseline for the fitting process. As a counterexample, if only the post-radiation curves were fitted, then the $|\Delta V_{th}|$ would be misrepresented, as $\Delta V_{th} \approx \Delta V_{th,\,process} + \Delta V_{th,\,radiation}$. In the following paragraphs, only the relative degradation with respect to the pre-rad characteristics is reported and commented. This procedure successfully managed to fit the available data to a reasonable degree of accuracy.

LDMOS TID fitting results Table 1 shows the results related to the LDMOS devices. 30V-rated devices (both n- and p- type) and 45V-rated devices (only p-type) have been considered: regarding the 45V flavour, the n-type devices have been neglected



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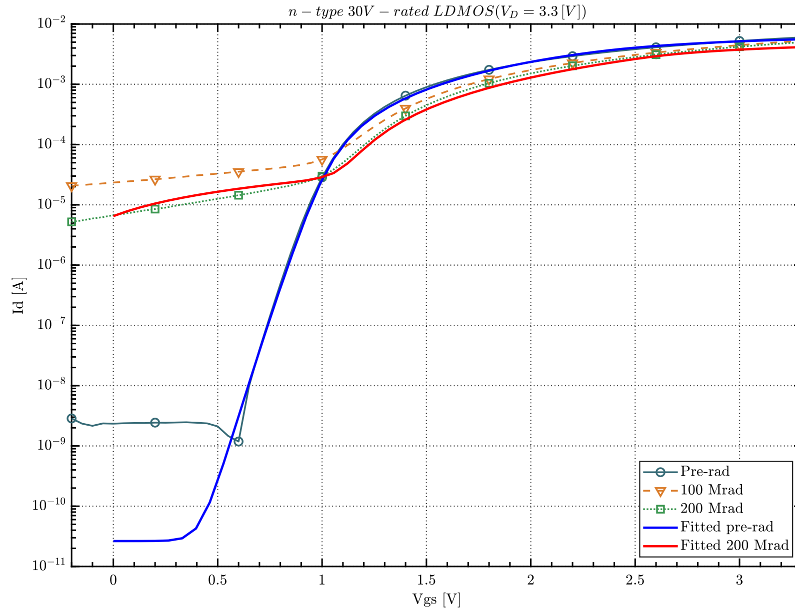
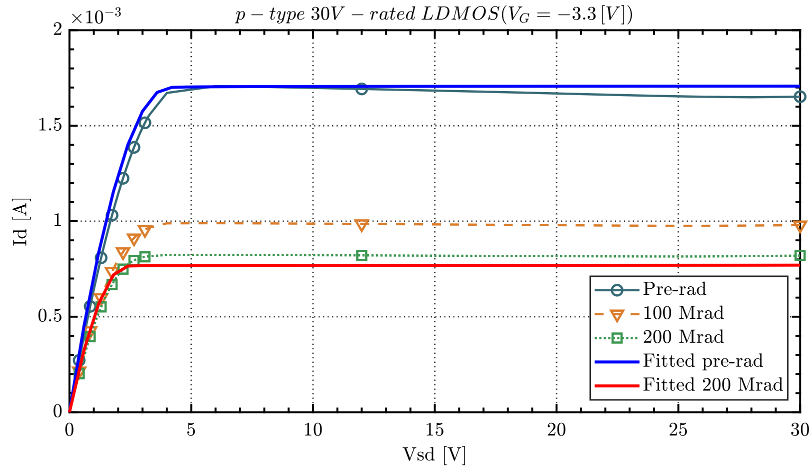


(b)

Figure 13: The $I_D - V_D$ (a) and $I_D - V_G$ (b) characteristics of a 30V-rated n-type LDMOS device are presented, considering both the pre- and post-irradiation scenarios.

Device	$\Delta V_{th}\ [V]$	$\frac{\Delta\mu}{\mu}$
30V-rated n-type LDMOS	$+0.1$	-40%
30V-rated p-type LDMOS	-0.7	0
45V-rated p-type LDMOS	-0.71	0

Table 1: The correction factors for the high-voltage LDMOS devices are presented. ΔV_{TH} represents the shift in the threshold voltage upon exposure to radiations and $\frac{\Delta\mu}{\mu}$ represents the relative degradation of the mobility of the carriers. The TID level is 200 $Mrad$. The V_{th} for p-type devices is considered to be negative.



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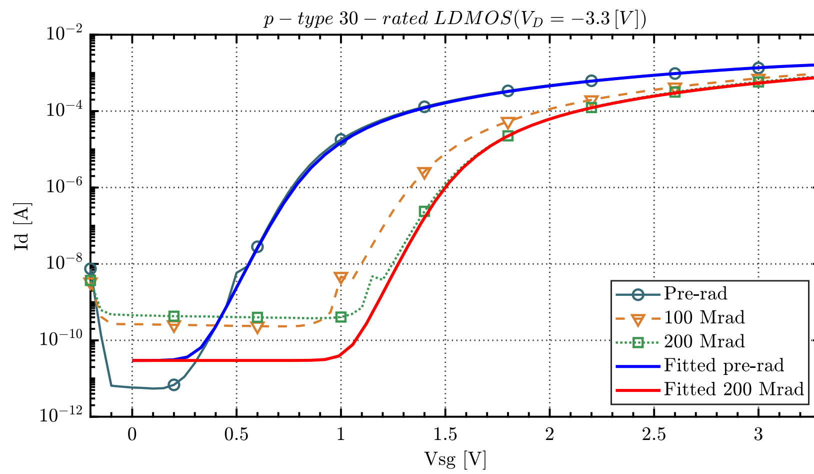
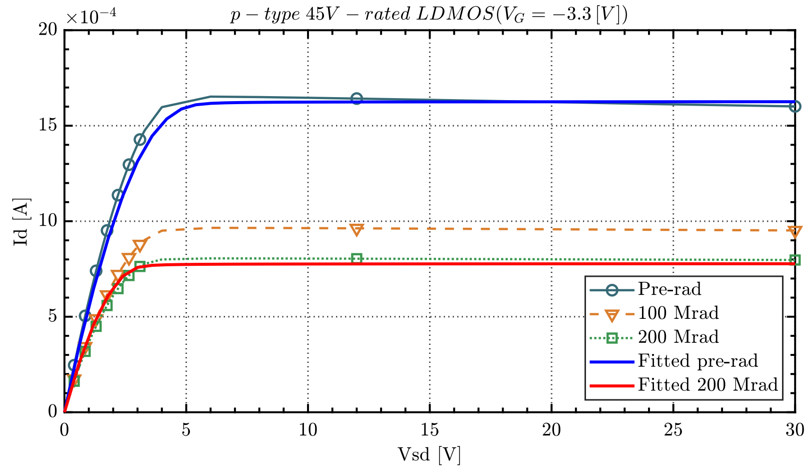


(b)

Figure 14: The $I_D - V_D$ (a) and $I_D - V_G$ (b) characteristics of a 30V-rated p-type LDMOS device are presented, considering both the pre- and post-irradiation scenarios.



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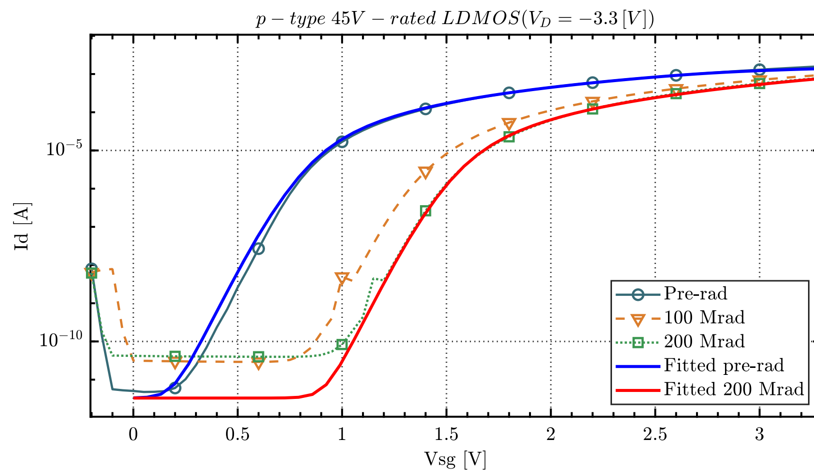


(b)

Figure 15: The $I_D - V_D$ (a) and $I_D - V_G$ (b) characteristics of a 45V-rated p-type LDMOS device are presented, considering both the pre- and post-irradiation scenarios.

as they are not robust with respect to single event effects.

The I_{on} degradation has been modeled through a multiplicative factor on the mobility of the carriers. Another option would be to artificially decrease the dimensions of the transistors, but, as a side consequence, this would also lead to a large variation in the capacitances of the devices. The latter scenario is not acceptable since the high-voltage transistors are employed in the Miller compensation loop and in the output stage: therefore, a change in the capacitance values would fictitiously affect the stability of the system or the PSRR, respectively.

The results show that the p-type device experience a negative threshold shift, i.e., the radiations tend to turn off the inversion channel. The large shifts ($\Delta V_{th,\,p} \approx -0.71\ V$) observed in p-type LDMOS when compared to 1.8V-rated devices (not presented in this thesis and modeled by another colleague in the DCDC group) are to be referred to their thick gate oxide, which is rated for 3.3V. In fact, thin oxide would accumulate a smaller amount of holes, leading to a less detrimental degradation. Such a threshold voltage degradation has also proved to completely explain the degradation of the I_{ON} for p-type devices, so that no mobility correction was necessary.

Analogously, the threshold voltage of n-type devices tends to increase at 200 $Mrad$. This result is explained by the combined effect of the two carrier trapping mechanisms that have been discussed earlier: it is clear that at such doses in a n-type transistor, the SiO_2/Si interface trapping mechanism starts to become dominant. The latter phenomena are also responsible for the small threshold variation $\Delta V_{th,\,n} \approx +0.1\ V$, since there is a competition and compensation between them.

The final fitted results are shown in fig. 13, fig. 14 and fig. 15.

Leakage modeling for n-type LDMOS device In the case of n-type LDMOS devices the leakage phenomenon is to be considered and a Verilog-A module was developed, describing the transistor-like behaviour of the parasitic FOXFET at a dose of 200 $Mrad$. The latter Verilog-A module is then instantiated within the device's model in the specific radiation-related corners. The leakage current is defined as the value of the current when $V_{gs} = 0\ V$ (see figure 13).

The scenario where $V_{gs,\,irrad} \approx 3.3\ V$ is observed to be the worst case for the leakage phenomenon (at $V_{gs} = 0\ V$) and it is taken as a reference for all transistors, regardless of their actual bias in the regulator. However, in principle, the radiation-induced degradation should be bias-dependent, as the charges are distributed according to the electric field lines. Both the V_{sg} and V_{ds} dependences have been implemented in a transistor-like fashion. Thus, given a certain parasitic current, the gate voltage may help accumulating charges in the parasitic channel. Moreover, the leakage current may flow in both direction, according to the sign of V_{ds}. When $V_{ds} = 0$, no leakage is present. When $V_{gs} \leq 0$, but $V_{ds} \neq 0$, a residual leakage path is still present and it is strictly determined by the irradiation conditions (i.e., $V_{gs,irrad} = 3.3\ V$ here). A saturation region has been described within the Verilog-A module and the parasitic saturation voltage has been arbitrarily set to a small value of $V_{dsat,parasitic} = 100\ mV$, as a conservative assumption.

Nonetheless, the actual peak in the leakage current takes place when the TID dose

is relatively low, when the hole accumulation in the oxides is the dominant contribution in n-type transistors. Given the dose rates that were used during the measurements, the peak took place at around 1 $Mrad$. The peak value is clearly a function of the voltage bias during the irradiation: it has been measured to be 5 μA when $V_{gs,\,irrad} \approx 1\ V$ and 100 μA when $V_{gs,\,irrad} \approx 3.3\ V$. Hence, a separate simulation corner has been developed so that this phenomenon may be taken into account. As a worst-case assumption, it is assumed that the parasitic channel has no gate modulation, keeping the current at its maximum value. Experimentally, the gate modulation has been observed to turn off the parasitic channel for $V_{gs} < 0\ V$ when $V_{gs,\,irrad}$ is small, but not when $V_{gs,\,irrad} \approx 3.3\ V$. A Verilog-A module similar to the aforementioned one has been created, implementing the dependence on the $V_{gs,\,irrad}$ and the V_{ds}.

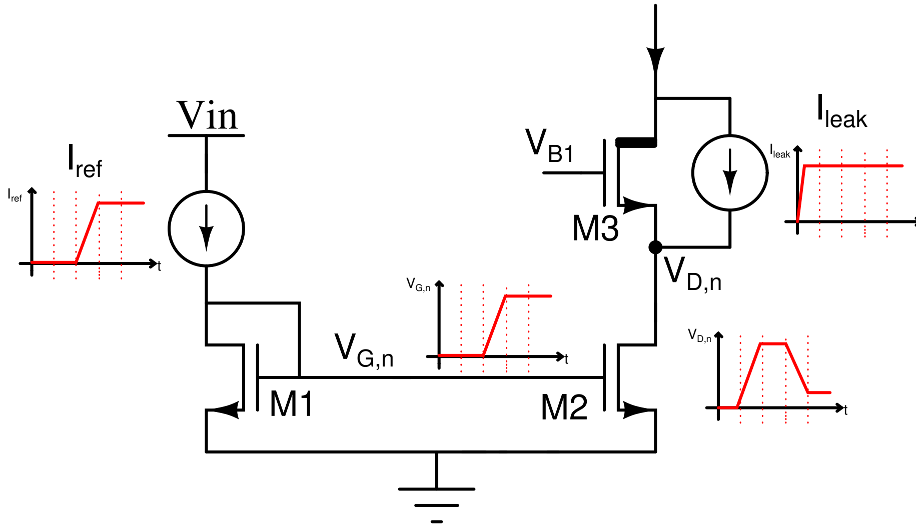


Figure 16: Example of a leakage-induced over-voltage, namely on transistor M2 (see the voltage $V_{D,n}$ on the drain of M2). The transient behaviour of I_{leak}, I_{ref}, $V_{G,n}$ and $V_{D,n}$ are shown next to the corresponding nodes.

A possible chip failure may be due to a turn-off/turn-on cycle at relative low TID dose values, as the peak leakage current during the start-up phase may exacerbate the over-voltage issue when the circuit is not fully on.

For the sake of clarity, an example is shown in figure 16. Four distinct time steps are shown and the V_{in} is considered to be rising from 0 V to its nominal value. At first, the beta-multiplier circuit (I_{ref}) is off due to the low V_{in}. On the other hand, the leakage current (I_{leak}) is readily present as soon as few hundreds of millivolts drop on $V_{ds}(M3)$ (it has been observed that the accumulation of electrons in the parasitic channels may be independent from the $V_{gs}(M3)$).

In the second time step, it is assumed that the $V_{G,n}$ is still low: it is a reasonable assumption, since the beta multiplier circuit has been designed by the DCDC team to work when V_{in} is larger than few volts. Therefore, the transistor M2 is off and its drain node is characterized by a high equivalent impedance. The leakage current charges the parasitic capacitances at the drain of M2, increasing $V_{D,n}$: thus, an overvoltage on transistor M2 takes place, possibly exceeding its V_{ds} rating. The peak of the over-

voltage is determined by the value of the leakage current and it gets worse as the latter increases: for low TID doses ($\approx 1\ Mrad$), the leakage current reaches its maximum, representing the worst-case for over-voltages during the start-up.

In the third time step, the beta-multiplier delivers the nominal current and $V_{G,n}$ increases, exceeding the threshold voltage of M2. Electrons start to accumulate in the channel of M2.

In the forth step, the highly conductive inversion channel is formed and the $V_{D,n}$ decreases, since a smaller voltage drop on M2 is necessary to sustain the flow of current: in other words, the high $V_{D,n}$ induces a large current through M2 and the parasitic capacitances at the drain of M2 are discharged. Finally, all the electrical quantities reach their steady state value.

In the light of the previous example, a path to a low voltage node should be always provided in the case of leakage, as it will be discussed in the following chapters. In fact, considering figure 16, if a low-impedance path (e.g., to ground) were available in parallel to M2 when the over-voltages happen, the drain of M2 would be clamped and would not experience any overshoot.

The line of reasoning presented above underlies few assumptions. During the irradiation, the transistors bias voltage V_{gs} is not fixed as in the measurement procedure previously described. In fact, the V_{gs} would follow the V_{th} variation as to provide the same current level, given that all the other devices are correctly in their saturation region. In the case of a n-type LDMOS transistor, the additional presence of the leakage current would further reduce the $V_{gs,\,n}$, as the current is gradually redistributed to the parasitic channel. In the light of this, in the real circuit the peak leakage current would have a milder effect on the circuit with respect to the simulation.

Displacement damage modeling for LDMOS devices Since the displacement damage effects lead to an increased resistance in the low doping region of the LDMOS transistors, it has been described as an additional series resistor within the transistor's model. In the case of p-type LDMOS transistors, the "RDW" parameter in the BSIM4 model has been modified, increasing the low-doping region resistance by a factor of 30. In the case of n-type LDMOS transistors, the $I_D - V_D$ characteristics is severely distorted, as it is shown in figure 10. Hence, a piece-wise linear resistor has been instantiated within the transistor's model for the radiation corners. Two values of resistances are used: the slope in figure 10 is 12 $k\Omega$ for $V_{ds,\,n} < 10\ V$ and 2.5 $k\Omega$ for $V_{ds,\,n} > 10\ V$. Eventually, the transistor saturates for $V_{ds} > 30\ V$ and the saturation current value is not influenced by the additional resistor. The series resistance value is normalized with respect to the dimensions (W) and the number of gates: when the transistor is larger, the local damage in the low-doping region is assumed to be the same, but it has a milder absolute impact on the device.

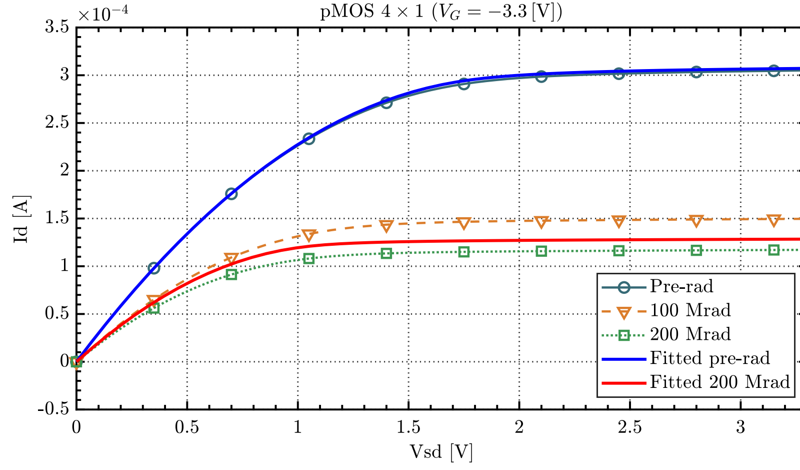
3.3V-rated p-MOSFET TID fitting results The results in table 2 show the extracted parameters for 3.3V-rated pmos transistors. In this case, the mobility μ is considered as not perturbed in the model and the degradation of the I_{on} is obtained by changing the width and the gate length L. The ΔW is to be attributed to the partial depletion of the inversion channel due to the accumulation of holes close to the edge of

$Dimensions\left(\frac{W}{L}\right)$	ΔW	ΔL	ΔV_{th}
$1\ \mu m/300\ nm$	$-50\ nm$	$+40\ nm$	$-0.83\ V$
$4\ \mu m/300\ nm$	$-50\ nm$	$+40\ nm$	$-0.83\ V$
$4\ \mu m/700\ nm$	$-50\ nm$	$+40\ nm$	$-0.90\ V$
$4\ \mu m/4\ \mu m$	$-50\ nm$	$+40\ nm$	$-0.93\ V$
$4\ \mu m/10\ \mu m$	$-50\ nm$	$+40\ nm$	$-0.93\ V$
$4\ \mu m/1\ \mu m$	$-50\ nm$	$+40\ nm$	$-0.93\ V$
$400\ nm/300\ nm$	$-50\ nm$	$+40\ nm$	$-0.80\ V$

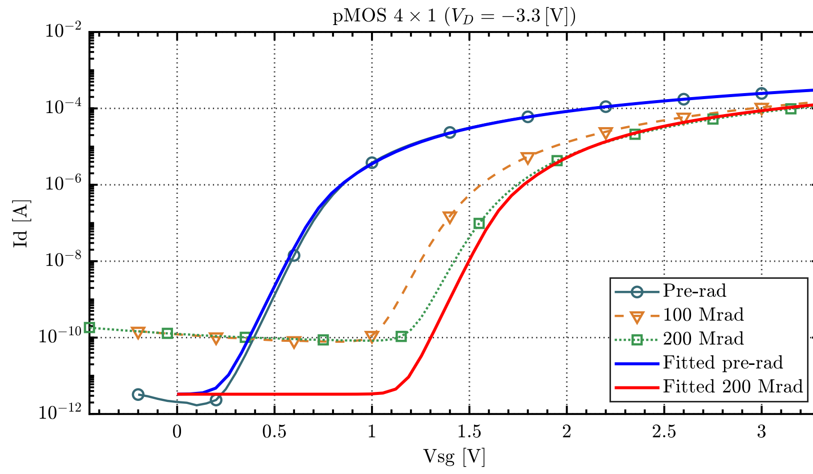
Table 2: The extracted corrections of the parameters of the 3.3V-rated pmos transistor upon radiation with a TID of 200 $Mrad$ are presented. The V_{th} for p-type devices is considered to be negative.

the transistor (see figure 5). Additionally, the ΔL has been considered since it allows for a reasonable fitting of the data. The ΔL has been extracted by considering devices with a small L and a large W, in order to single out the contribution of the variation of the gate length: the device with dimensions $\frac{4\ \mu m}{300\ nm}$ has been considered. By fixing ΔL, the ΔW has been extracted with an analogous rationale, using the devices with dimensions $\frac{1\ \mu m}{300\ nm}$ and $\frac{400\ nm}{300\ nm}$. The extracted results have been extended to all the other dimension ranges, as it is shown in table 2. It is interesting to notice that these parameters are comparable (or slightly worse) with respect to those of the p-type LDMOS devices (table 1). Some fitted curves are shown in figure 17 and 18.

3.3V-rated n-MOSFET TID fitting results The ELT 3.3V-rated n-type devices were damaged during the measurement procedure and no experimental data is present. As a consequence, the fitting procedure has been applied to the standard devices. Nevertheless, the dimensions of the standard transistors that were characterized are not compatible with the ELT geometrical constraints (minimum achievable width of an ELT transistor), expect for one device. Therefore, it has been decided to consider a conservative worst-case scenario in the experimental data, extending it to all the sections of the BSIM4 model. The $\Delta V_{th} \approx +175\ mV$, while $\frac{\Delta \mu}{\mu} = -25\%$.

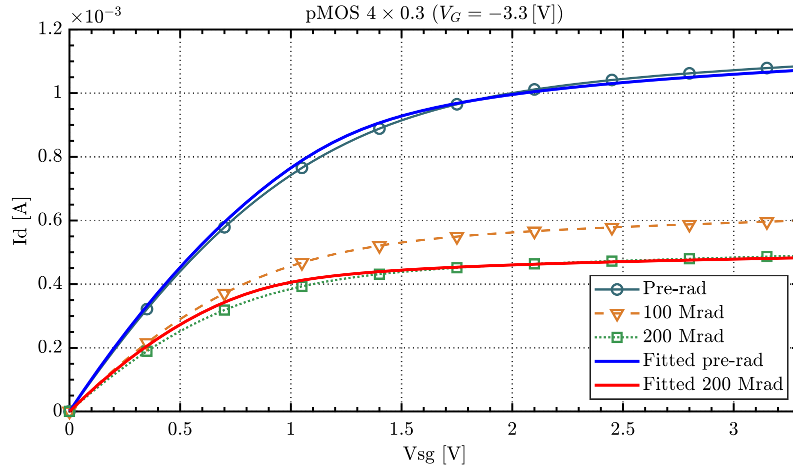


(a)

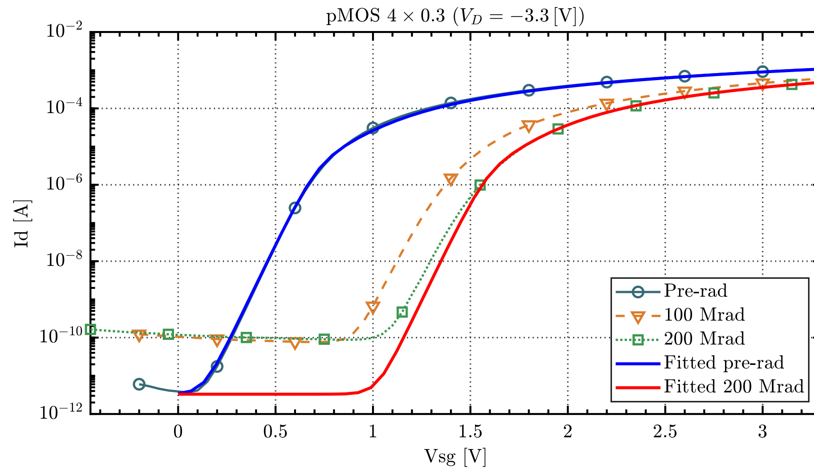


(b)

Figure 17: The $I_D - V_D$ (a) and $I_D - V_G$ (b) characteristics of a low-voltage pmos device are presented, considering both the pre- and post-irradiation scenarios. The dimensions are $\frac{W}{L} = \frac{4\,\mu m}{1\,\mu m}$.



(a)



(b)

Figure 18: The $I_D - V_D$ (a) and $I_D - V_G$ (b) characteristics of a low-voltage pmos device are presented, considering both the pre- and post-irradiation scenarios. The dimensions are $\frac{W}{L} = \frac{4\,\mu m}{0.3\,\mu m}$.

3 Linear regulator REG48V

The primary focus of the design of this regulator (alongside REG12V and REG3P3V) is to ensure its *reliability*. The most demanding aspect is to ensure its proper functionality across a wide spectrum of operating conditions, both prior to and following exposure to radiation. Given that these circuits are intended for use in CERN experiments, it would be highly undesirable for them to require frequent replacement, resulting in substantial time and financial wastage: for instance, the access to CERN experiments is complicated due to the radioactive materials. The targeted reliability of the DCDC converter chip, and consequently these circuits, is set to be approximately 10 years.

The circuit REG48V that is examined in this chapter is part of the chain of regulators in figure 1. A simplified schematics is shown in figure 19. Its purpose is mainly to feed the chip for the GaN switches.

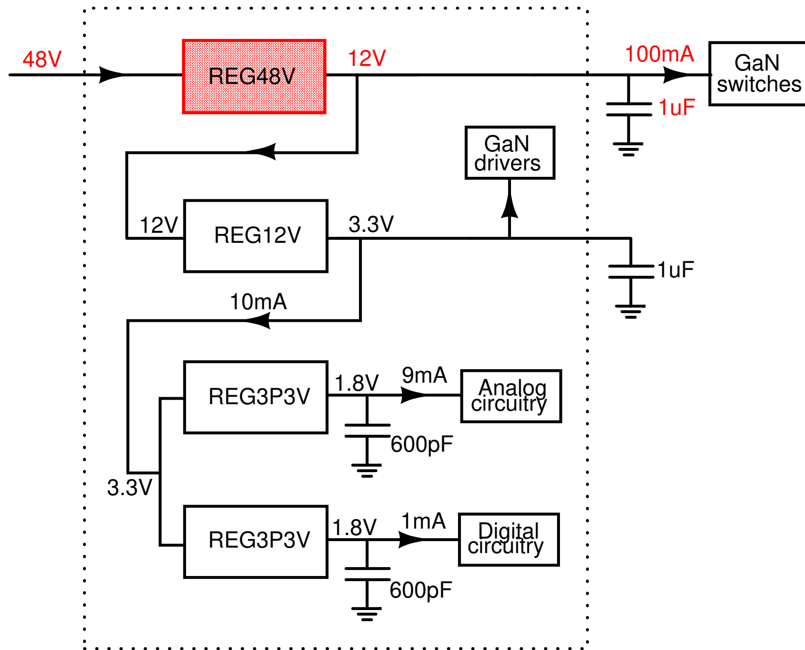


Figure 19: A simplified schematics of the module in figure 1 is presented and REG48V is highlighted.

3.1 Specifications

This chapter describes the linear regulator *REG48V*. This circuit has been designed to work in an extremely broad range of operating conditions and flexible specifications (table 3).

In addition to the conditions that are highlighted in table 3, the PVT corners (process, voltage, temperature variations) have to be considered, with a sufficient margin of design.

Specifically, a variation of $\pm 20\%$ in the values of the resistances has to be considered due to process and temperature variations if no temperature compensation is present.

Specifications	Value
Temperature	$-30°C$ - $100°C$
Output load I_{load}	0 - 100 mA
Input supply voltage V_{in}	$< 55V$
Output voltage V_{out}	$3.3V$ - $12V$
$\left\lvert \frac{\Delta V_{out}}{V_{out}} \right\rvert$	$< 3.5\%$
Total ionising dose	$< 200\ Mrad$
Displacement damage fluence	$< 5 \cdot 10^{15}\ \frac{protons}{cm^2}$
n-type LDMOS I_{leak}	$< 5\ \mu A$
Single event LET	$< 40\ \frac{MeV \cdot cm^2}{mg}$
Output filter capacitance C_{out}	$1\ \mu F \pm 30\%$
Phase margin	$> 45°$
PSRR	$> 30\ dB$
$\Delta V_{out,SEE}$	$< 20\ mV$
$T_{startup,rise}$	$> 1\ ms$

Table 3: This table shows the specifications of the REG48V circuit.

These variations severely affect the voltage references (bandgap reference) and the beta multiplier circuits (see section 1.3). Indeed, the beta-multiplier circuit, which has been employed to provide a reference current to the regulator, is affected up to 50% with respect to its nominal output current $I_{ref} = 20\ \mu A$ (see fig.20): this happens because it relies on a resistor, which can be compensated for regarding the temperature variations, but not easily with respect to process variations. Along the same lines of reasoning, the bandgap reference providing the $V_{ref} = 1.2\ V$ has a $\approx 2.5\%$ tolerance on its output.

Analogously, the process variations of the employed capacitances and the transistors are taken into account. Moreover, the specifications on the C_{out} take into account a $\pm 30\%$ tolerance on the nominal value for the following reasons. First of all, this capacitor is a commercially available component and it is mounted at the PCB level: such components usually have significant tolerance windows on their value. Secondly, the C_{out} should be able to sustain a relatively large voltage ($\approx 12V$): most often, there is a trade-off between the accuracy of their capacitance value and the high-voltage rating. This should be taken into account for the stability, as the output node determines the bandwidth of the feedback loop in standard operating conditions. Finally, the temperature range that is considered is a reasonable choice despite the large currents involved thanks to the efficient cooling system at the PCB level.

The circuit should be stable in all the operating conditions and a phase margin greater than 45° is set as the absolute lower bound for stability. The power supply rejection ratio (PSRR) is one of the most important parameters for the linear regulator and the lower bound that meets the specs is set to be 20dB of rejection (the performance of the regulator is $> 30dB$, as it is shown in table 3). The mismatch of the regulator should be less than 3.5% with respect to the output voltage, using real bandgap and beta-multiplier circuits (1% when considering ideal reference circuits). The minimum

drop-out of the linear regulator should be minimized, carefully considering the trade-off with respect to the area consumption. During a single event, the variation on the output voltage should be minimized (here, $\Delta V_{out,SEE} < 20\ mV$). The voltages within the circuit should be within the SOA specifications of every device when the input power supply goes from $0\ V$ to $55\ V$ with a rise time $T_{rise} > 1\ ms$.

3.2 Circuit description

In the following paragraph, a qualitative analysis of the circuit in fig.20 is provided. The final sizing of the whole circuit required the cross examinations of all the operating conditions, a heavy use of the simulation results and a large dose of experience on the supervisor's side. Moreover, the design choices are markedly conservative, since modeling the radiation-induced degradation of transistors is tricky and it can only provide a worst-case scenario. In light of this, it is thought that a purely analytical discussion would be too complex and less helpful in a practical design, so that the focus in this section is on an intuitive understanding of the design challenges.

The system consists of a single-stage OTA driving the pass transistor. This very simple topology has been selected in order to guarantee reliability in the long-term operation of the circuit and to minimize the number of high-voltage transistors (LDMOSs) that are employed, since they drastically impact on the area. Moreover, also multiple-stage OTAs have been thoroughly investigated through simulations, but all the examined circuits resulted unstable in some corners: further analysis took place and the issue was identified as the interplay between the outer feedback loop (comprising the multiple stages of buffering or amplification) and the inner Miller compensation loop. Therefore, these circuit topologies have been discarded.

OTA analysis Since the input power supply may reach 55V, at least two high-voltage (p-type LDMOS) transistors are necessary to sustain such a voltage drop, since the rating of each one is for 30V between drain and source. Moreover, the employment of two LDMOS transistors prevents the SEB phenomenon from happening, since the SEB critical electric field is around $30\ V$. The transistor $M6 - M9$ and $M23 - M24$ are needed in order to protect the low voltage nmos current mirror ($M2, M3, M21$), while $M14, M15$ protect the low-voltage pmos current mirror ($M16, M17$) that provides the bias current to the pmos differential pair ($M12, M13$). Moreover, due to the large degradation of the n-type LDMOS transistors related to the displacement damage (see fig.10), an additional low-voltage cascode stage ($M4, M5$) is introduced.

The bulk terminals of the transistors in the differential pair are not connected to their sources because of the SEE effects: when a huge amount of electron-hole pairs are created within the devices, it is better to have a low impedance node to evacuate them, so that the bulk is connected to V_{B1}.

The bias voltages V_{B0}, V_{B1} and Vin_half are produced through series resistors and diode-connected low-voltage transistors, since they should be available even for small values of the supply voltage. Moreover, they have large integrated capacitances in parallel ($\approx 8pF$), so that they are characterized by a low impedance during fast transients (e.g, during a SEE burst of current).

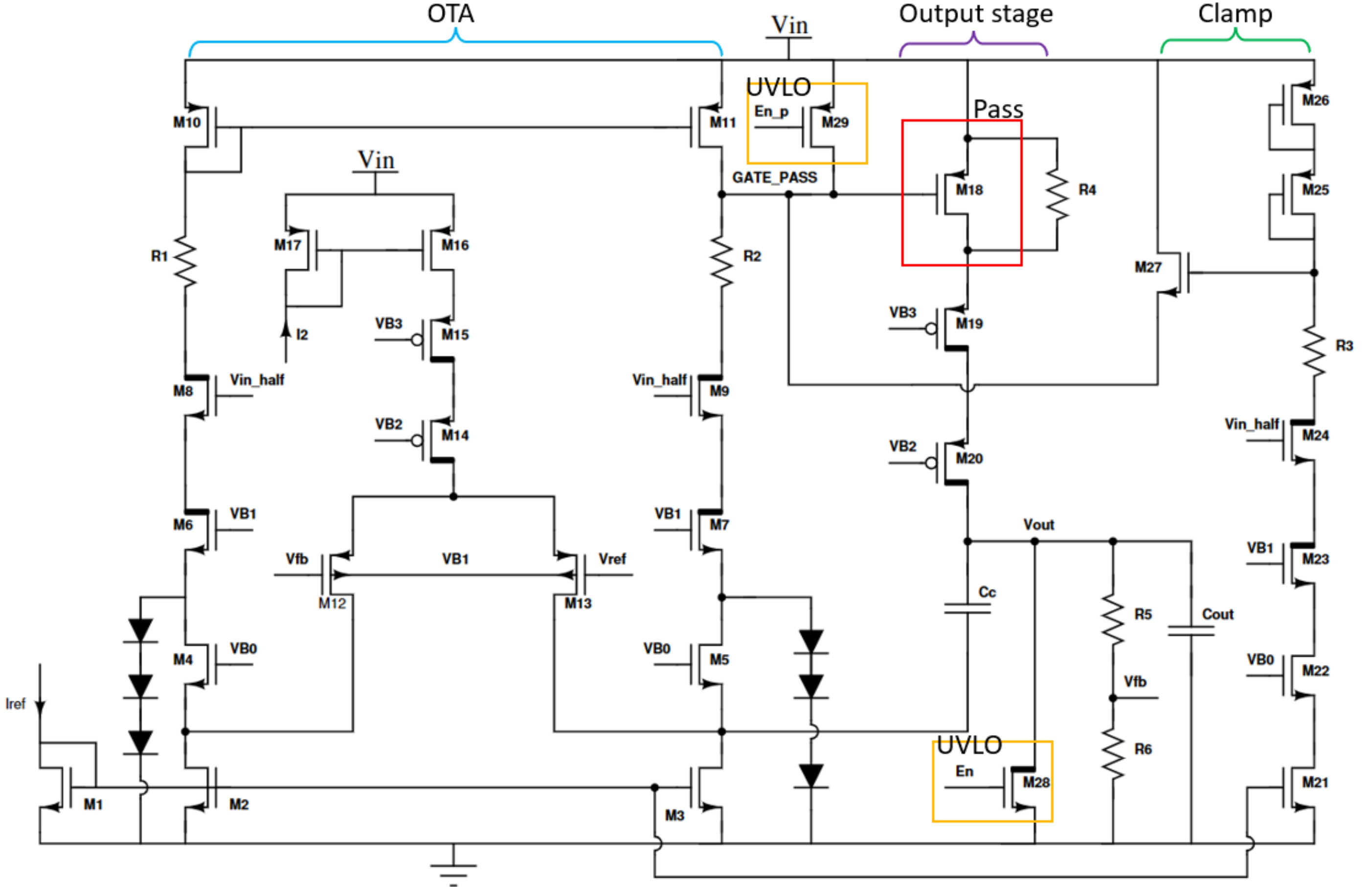


Figure 20: The simplified final schematics of the designed regulator *REG48V* is presented. A folded-cascode structure (cyan, M1-M17) is connected to the pass transistor (red, M18). The gate of the pass transistor is protected against over-voltages through a clamp structure (green, M21-M27). The biasing circuits are not shown. The UVLO (under-voltage lock-out) enabling signals are represented as En and En_p (yellow, M28 and M29).

The series resistors $R_1, R_2 \approx 1\ k\Omega$ are introduced in order to provide a quenching mechanism to the single event burnout phenomenon (SEB) on transistors $M6 - M9$: in fact, when a large current is induced by an impinging high-energy particle, the additional voltage drop due to such resistances brings the V_{DS} below the critical value ($\approx 30V$ for these n-type LDMOS, see 2.3), effectively quenching the effect.

The diodes in the schematics serve to provide a parallel path towards a low impedance node in the case of leakage current during the start-up phase of the circuit. In fact, it has been shown that the leakage current induced by radiations may not have a strong dependence on the V_{gs} of the transistor (see figure 5 and the related discussion), while a V_{ds} dependence is present as expected. With such premises, as the power supply increases starting from $0V$, a leakage current is injected into the rest of the circuit, while it is still not fully operative. This phenomenon would lead to the charging of the small parasitic capacitances of the devices and thus to severe over-voltages on the transistors

$M4 - M5$, which would exit their safe operating area (SOA). The diodes are able to redirect the leakage current towards the ground node, which would not be affected.

Pass transistor Since the pass transistor has to handle $100mA$ of load current, it is one of the dominant contributions to the overall area of the whole circuit. Therefore, its size has been computed in order to minimize the area consumption, while keeping the transistor within its safe-operating area. In order to do that, a IO transistor (3.3V-rated transistor) has been chosen and the $\frac{W}{L} = 50 \cdot \frac{26\mu m}{0.3\mu m}$. the number of fingers has been computed in order to reduce the electro-migration effects on the device, as it will be explained later.

A core transistor (1.8V-rated transistor) is also a reasonable choice for the pass transistor, but it is characterized by the following issue. Since $V_{sg}(M18) = V_{sd}(M11)$ as it is shown in figure 30, considering the large output load range (up to 100 mA) and taking care of the SOA for the core transistor ($V_{sg}(M18, core) < 2\ V$), this option would tend to have $M11$ in triode region when no load is present at the output, due to the oversize of $M18$. This condition would introduce a significant mismatch in the OTA structure, leading to a non accurate output voltage V_{out}.

It could also be sensible to employ a (either p-type or n-type) LDMOS as the pass transistor, but this option has been discarded in the light of the following considerations.

1. The LDMOS transistors are characterised by large parasitic capacitances due to their device structure (see fig.8). This leads to worse PSRR performances of the circuit with respect to the low-voltage counterpart.

2. These devices experience a detrimental degradation due to the displacement damage, on top of the V_{th} shift and the I_{ON} reduction (see fig.10). It is then not thoughtful to employ such transistors as active elements in the feedback loops (rather than just cascaded protection transistors), since the loop gain would be dramatically affected.

Another possibility could be to use a n-type transistor as the pass element, as exemplified in figure 21. The n-type pass transistor has to be driven in a way such that both its gate and source nodes are referred to the same voltage domain. This is done in order to protect the pass transistor and keep it within its SOA specifications at all times: in this specific example, it is achieved by folding the OTA branches so that $M22, M26$ are referred to the output node. This topology has been investigated through simulations. Nevertheless, the degradation due to the DD is even more significant than the one the p-type high-voltage transistors experience (see fig.10). Moreover, the leakage current is an unsolvable problem for n-type LDMOSs (the ELT structure cannot be properly adapted and it has been proved experimentally): during the start-up, this could cause the charging of high-impedance nodes, since the current is injected into a circuit which is not fully on, thus leading to over-voltages that could destroy the transistors themselves. In the light of these considerations, this topology has been discarded.

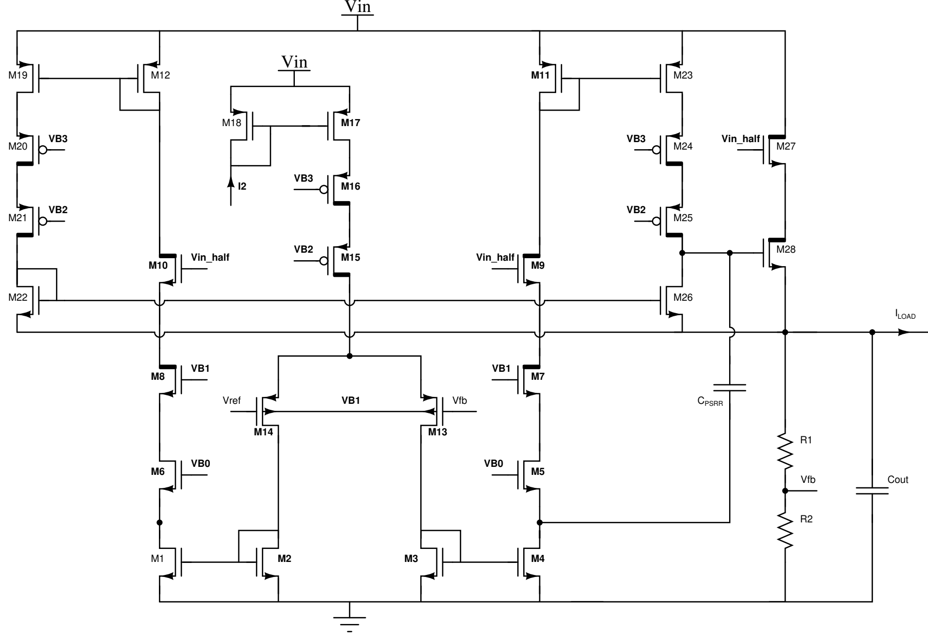


Figure 21: A simplified schematics of a regulator employing a n-type pass transistor is shown. The high-side driving of the pass transistor is achieved by referring the n-type current mirror $M22, M26$ to the output node.

Output stage analysis The transistors $M19, M20$ serve to sustain the voltage drop on the output stage. The voltage V_{B3} has to allow the pass transistor to be in saturation throughout all the operating conditions and, specifically, taking care of the load: in fact, when the load is maximum, the V_{sg} of the pass transistor is maximum and the saturation voltage is increased accordingly. The circuit in fig.22 has been designed so that the bias voltage is adjusted according to the output load through a voltage follower stage. By referring the bias voltage to the gate of the pass transistor, a simple way of compensating the radiation-induced degradation of the V_{th} of the p-type LDMOS $M19$ is achieved. Indeed, the transistors try to provide the same amount of current even after the exposure to radiations, a shift in the threshold voltage is directly mirrored in the same shift of the V_{sg} at the first order of approximation. Since the p-type IO devices (e.g., $M18$) and the p-type LDMOS (e.g., $M19$) devices have a very similar V_{th} degradation, the V_{B3} is optimally adjusted, making the design of the bias circuit easier. The diodes connected to V_{B3} aim at limiting the V_{DS} voltage of the pass transistor, since it has to be lower than 3.6V.

The dimensions of the transistors $M19, M20$ has been chosen as a trade-off between the minimum drop-out and the area consumption. This is because due to the displacement damage effects, the p-type LDMOS transistors experience a detrimental shift in the saturation voltage (due to the increased resistivity of the transistor). The chosen dimension for both transistors is $120 \cdot \frac{100\mu m}{1\mu m}$: this is by far the most significant contribution to the area consumption in the circuit, since the isolation DTI and electro-migration concerns also have to be taken into account.

A precise tuning of the V_{B2} is needed in order to equally distribute the headroom voltage between $M19, M20$. The bias circuit for the voltage V_{B3} has been designed as

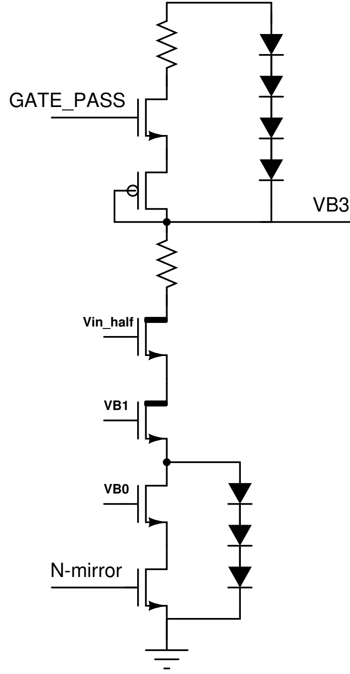


Figure 22: The bias circuit providing V_{B3} to the circuit in fig. 20 is presented.

a voltage divider between the input supply voltage and the output voltage of the linear regulator. This is done because the V_{out} is between $3.3V$ and $12V$, while also the V_{in} is quite flexible.

It has been simulated that, in order to work properly in every possible operating condition, the V_{sd} of the high-voltage transistor should be larger than their saturation voltage, which is estimated to be $V_{sat} \approx 5; V$ given their dimensions (see fig. 10). Therefore, this would imply a minimum dropout of $V_{dropout} = V_{dsat}(M20) + V_{dsat}(M19) + V_{dsat}(M18) \approx 11\ V$. This is a quite conservative condition and it refers to the worst possible case, which is when $I_{load} = 100\ mA$, at $T = 100°C$, after radiation exposure and considering the displacement damage effect. When no load is present, it has been simulated that the regulator works with a minimum dropout of $2\ V$. On the other hand, if only the pre-rad condition is of interest, the minimum V_{in} is around $15\ V$ (with max load). If the transistors in the output stage operate in their triode region (relatively small V_{sd}), their V_{gs} may go outside their SOA if not be able to sustain large loads.

The resistor R_4 in fig.20 aims at providing a small bias current to the output stack (M_{19}, M_{20}) during the start-up phase of the circuit: without that resistance, the current flowing through $M18$ would be the same as that flowing through the output stack. In the latter scenario, since two different transistor technologies are employed (3.3V technology and p-type LDMOS), the two I_{off} ($V_{gs} = 0, V_{ds} \neq 0$) currents are significantly different, so that the V_{SG} of M_{20} would become negative when the regulator is disabled ($En = 1$), thus pushing the pass transistor out of its safe operating area. The current through R_4 is $\approx 500nA$ in steady state.

Finally, the feedback resistors $R5, R6$ guarantee that when $V_{out} = 12\ V$, the feedback

current is around 48 μA. This is only necessary for the inner workings of the feedback system and does not contribute to the power delivered to the load: hence, a higher value of resistance value would in principle minimize the power loss, but it would lead the $M10, M11$ current mirror into triode region, due to the reduced V_{sg} of the pass transistor $M18$.

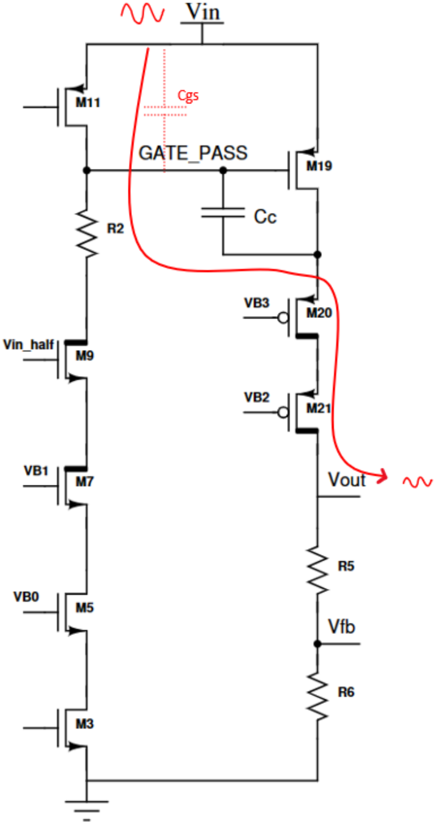


Figure 23: This figure represents a portion of the circuit in figure 20 where, instead, the Miller compensation capacitance has one of its ends attached to the gate of the pass transistor. A direct path for the noise from the power supply to the output node is highlighted.

Compensation loop Coming to the compensation capacitor, it has been connected to the drain of $M3$ (see figure 20) since it represents a low-impedance node that is reasonably stable with the variations on the input supply voltage V_{in}, unlike the gate of the pass transistor. In fact, in the latter situation, the Miller capacitor would represent a direct AC path from the supply to to output node, leading to poor PSRR performance (see figure 23). In order to make the system stable with and without load, a compensation capacitance of $\approx 40\ pF$ has been employed. This has a huge impact on the area consumption of the chip, since a MOS capacitor (MOSCAP, with capacitance density $\approx 5\frac{fF}{\mu m^2}$) cannot be employed due to the relatively high voltages ($V_{out} = 12\ V$ in the worst case). It is then mandatory to exploit a metal finger capacitor (capacitance density $\approx 0.5\frac{fF}{\mu m^2}$), which is specifically designed to withstand such a voltage: unfortunately, they are characterized by a much smaller capacitance density with respect to

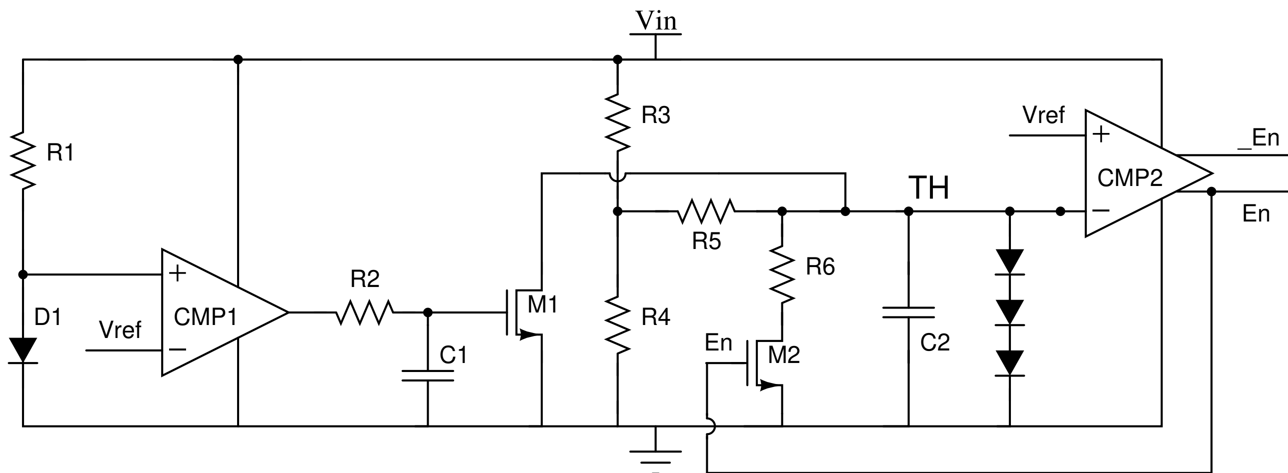


Figure 24: The UVLO (under-voltage lock-out) circuit is represented. The *REG48V* circuit is disabled until the input supply voltage reaches a certain threshold, given by the node *TH_25V*. A preliminary check takes place through the comparator *CMP1*, by making sure the reference voltage V_{ref} has reached its nominal value during the start-up phase. A hysteresis is inserted through the feedback involving the transistor M2.

MOSCAPs.

Clamp protection A clamp is needed for the gate node of the pass transistor, as its V_{SG} is only controlled by the output current that the attached load draws from the regulator. Transistor $M27$ has its gate biased by $M25, M26$ and when the gate of the pass transistors decreases too much, $M27$ starts conducting, pushing the node back up. This allows the clamp to be extremely reactive with respect to voltage variations. Such a good reactivity has been observed to also improve the SEE response. Conversely, in the structure in fig. 22, the voltage drop is divided equally among the series diodes, so that it is characterized by a lower sensitivity to over-voltages. During the standard operation of the circuit, the clamp protection is off. The over-current condition (leading to an over-voltage in the V_{SG} of the pass transistor), has been simulated by shorting the output node to ground: by doing so, the OTA is maximally unbalanced at its inputs and the feedback attempts to provide as much current as it is capable of (outside of its design specifications). The sizing of $M25$ - $M27$ clamps the $V_{SG}(M18) < 3.6\ V$. This exact condition is what happens during the start-up phase, when the V_{ref} is readily available, while the V_{out} is forced to $0\ V$ by the UVLO system.

Under-voltage lock-out (UVLO) The UVLO system is necessary in order to disable the linear regulator when the input supply voltage is too small. It is triggered during the start-up phase and the threshold above which the regulator is enabled is set by a voltage divider. An idealized implementation is shown in fig.24. It consists of a comparator ($CMP2$), which is triggered when the node TH reaches the level of V_{ref}. This comparator provides the signals En and En_p to the regulator (respectively, to $M28$ and $M29$ in fig.20): the En signal is provided by the ground-referred output of the comparator, while the En_p is obtained through a node which is referred to the supply. TH is a scaled version of the supply voltage and it is determined through an

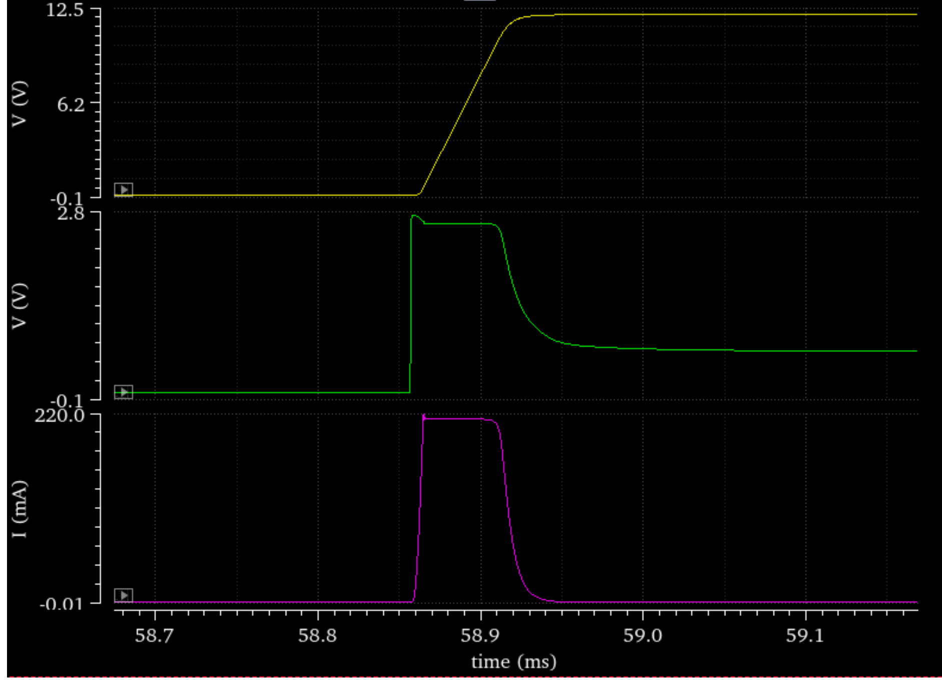


Figure 25: Example of a start-up where no soft start is implemented. V_{in} rises from $0\ V$ to $55\ V$ with a $T_{rise} = 100\ ms$. The regulator is turned on at around $V_{in} \approx 18\ V$. The considered corner is the slow one, with no radiation effects. The yellow curve represents the V_{out}, the green curve is the V_{sg} of the pass transistor and the purple one is the current that charges C_{out}.

hysteresis ($M2$ in fig.24). The UVLO circuitry has to be implemented in a high-voltage technology, since during the start-up no low-voltage domain is readily available.

$$\begin{aligned} V(TH)(En=0) &= V_{in} \cdot \frac{R_4}{R_4 + R_3} \\ V(TH)(En=1) &= V_{in} \cdot \frac{R_4//(R_5+R_6)}{R_3 + R_4//(R_5+R_6)} \cdot \frac{R_6}{R5+R6} \end{aligned} \tag{12}$$

The hysteretic behaviour of circuit can be characterized by two thresholds V_{TH}^1 and V_{TH}^2 on V_{in}, when the voltage divider is such that $V(TH) = V_{ref}$. Supposing that $V_{TH}^2 > V_{TH}^1$ and $R_5 + R_6 \gg R_4$ in order to have $\Delta V_{TH} = V_{TH}^2 - V_{TH}^1$ small (of the order of $1\ V$). Hence, the analytical expressions of the threshold are the following:

$$\begin{aligned} V_{TH}^1 =& V_{ref} \cdot \left(1 + \frac{R_3}{R_4}\right) \\ V_{TH}^2 =& V_{TH}^1 \cdot \left(1 + \frac{R_5}{R_6}\right) \end{aligned} \tag{13}$$

It is interesting to note that the two threshold only depend on ratios of resistances, so that their values are as accurate as the V_{ref} is, since the process variations on R_3, R_4, R_5, R_6 mostly cancel out.

Given eq.12 , for very low V_{in}, the $En = 1$ (the V_{out} is kept at 0V) and when TH reaches V_{ref} (threshold V_{TH}^2), it is quickly increased, so that there is no ambiguity in the transition due to noise or perturbations (e.g., SEEs). Analogously, if the V_{in} is high (above V_{TH}^2 and $En = 0$), when it decreases below V_{TH}^1 the regulator is quickly turned off, in order to prevent it from working in an unsuitable range of voltages, since it could be damaged. It is shown in eq. 13 that the two thresholds can be set independently. Moreover, $R_3 + R_4$ is around $\approx 2\ M\Omega$, in order to reduce the power consumption of the circuit. The specific values of the two thresholds are set by the minimum dropout of the regulator: for instance, considering the configuration such that $V_{out} = 12\ V$, since the minimum dropout is at least $2\ V$ when no load is present (i.e., during the start-up phase), the V_1^{TH} is set to $\approx 14\ V$ and V_2^{TH} to $\approx 15\ V$. It is important to point out that during both the start-up and the turn-off stages, no load current should be present: if it is the case, the regulator might not be able to sustain high currents with such low supply voltages.

$CMP1$ is used to have a preliminary check on the value of the voltage reference: in fact, for very small values of V_{in} it is reasonable that the bandgap reference block cannot output the proper nominal value $V_{ref} = 1.2\ V$, so that the comparison taking place with $CMP2$ would be meaningless: moreover, it could also happen that the UVLO switches at a lower voltage than predicted, depending on the erroneous value of V_{ref}. In the light of this consideration, when the bandgap circuit is not ready, the node TH is shorted to ground through $M1$: the diode D_1 is taken as a readily-available less precise voltage reference for $CMP1$.

An quick overview of the start-up phase is here presented. The V_{in} rises from $0V$ to its nominal value. Starting at very low voltages, the UVLO system immediately turns off the regulator by shorting the output to ground and by forcing the gate node of the pass transistor to the supply node: by doing so, the V_{out} of the regulator is guaranteed to stay at $0\ V$, keeping safe the circuitry that is attached to this block. As soon as the V_{in} exceeds the chosen threshold, the En signal becomes low and the output voltage is allowed to rise, through the charging of C_{out} by the pass transistor.

Since the V_{ref} reaches its steady state at low voltages, when the regulator is first turned on, it is maximally unbalanced: in fact when the UVLO is disabled, $V_{fb} = V_{out} = 0\ V$ and $V_{ref} = 1.2\ V$. Therefore, the regulator tries to provide as much current as it is capable of, beyond its design specifications, so that the so-called *inrush current* phenomenon takes place. This behaviour is unwanted, as over-voltages may permanently ruin the transistors in the output stage. In order to address this issue, a *soft start* is implemented and the maximum current that is delivered is limited. The reference voltage V_{ref} is only allowed to rise (slowly) to its nominal value when the regulator is enabled. Moreover, a RC circuit controls its rise time. As a consequence, the rise times of V_{ref} and V_{out} roughly match together, thus the charging of the output capacitor is a much more controlled process.

For instance, figure 25 shows what would happen without the soft start implementation. The current (and equivalently the V_{sg} of the pass transistor) are only limited by the clamp protection. It is worth noticing that the in figure 25 the peak current is around $220\ mA$, which is more than twice the design value. Moreover, the inrush phenomenon takes around $60\ \mu s$ to complete, so that it may seriously affect the circuit

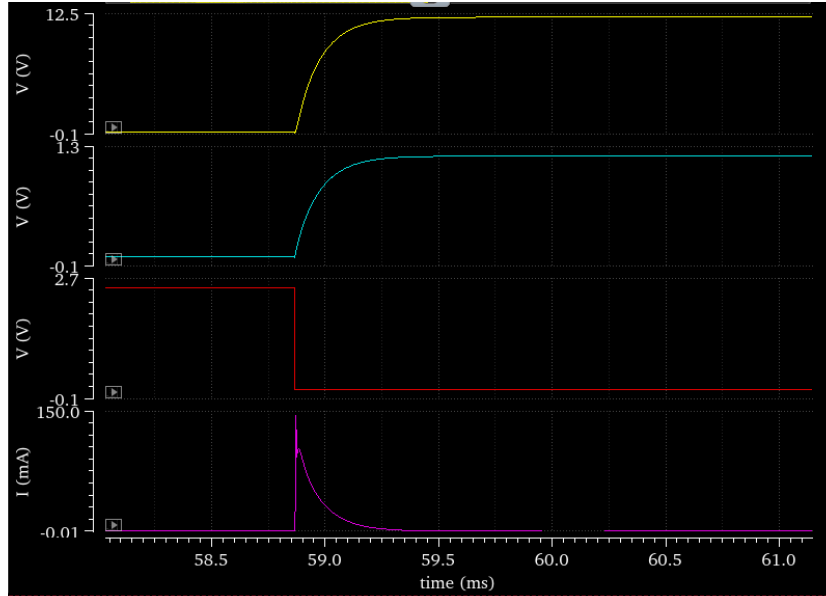


Figure 26: The transient simulation of the start-up phase is presented. The V_{in} rises from 0 V to 55 V with a rise time $T_{riswe} = 100; mA$. The V_{out} (yellow curve) is set to 12 V. In this case, the UVLO system enables the regulator $V_{in} \approx 25\ V$ through the enabling signal En (red curve). The reference voltage V_{ref} (cyan curve) is filtered through a RC and fed into the regulator: this feature determines the *soft start* feature. The inrush current (purple curve) is also plotted. During the start-up phase the load current is set to zero, i.e., the downstream circuitry is still off.

in terms of electro-migration and of long-term reliability.

Conversely, a proper soft-start is shown in fig.26. The slow rise time of the V_{ref} is limited by the the area consumption of the large capacitor ($\approx 25\ pF$) and the large resistance ($\approx 4\ M\Omega$) that are needed for such RC circuit.

3.3 Simulation results

In the following sections, the figures of merit of the circuit in fig.20 are highlighted and discussed.

DC simulation The circuit output voltage is expected to have a certain tolerance depending on the specific operating condition. The systematic mismatch results are highlighted in table 4. The source of this mismatch is twofold: both extrinsic (i.e., V_{ref} and I_{ref}) and intrinsic factors (i.e., the inherent structure of the regulator) play a role. It is worth noticing that the main contribution is due to the reference circuits. Thus, the max output variation $|\Delta V_{out}| \approx 400\ mV$ when $V_{out} = 12\ V$, while $|\Delta V_{out}| \approx 100\ mV$ when $V_{out} = 3.3\ V$.

Referring to figure 20, the V_{sg} of the pass transistor ($M18$) varies significantly according to the load. Since the it has to handle a large output current in the worst case, it has been particularly oversized in order to stay within its safe operating area. Consequently, when no load is attached, the pass transistor just provides a small current to the feedback loop (i.e., through R_5, R_6), which is of the order of 30 μA. Thus

Vout (nominal)	Vin	load = 0	load = 100mA
3.3V	24V	3.3% (1.12%)	2.5% (0.63%)
	55V	3.48% (1.33%)	3.1% (0.63%)
12V	24V	3.41% (1.25%)	2.8% (0.58%)
	55V	3.58% (1.33%)	3.2% (0.58%)

Table 4: The relative variation of the V_{out} is presented, with respect to the nominal value, throughout all the operating conditions described in table 3. The values in parenthesis represent the mismatch component which is only due to the intrinsic structure of the regulator. The corners are quite conservative and consider a 5σ variation on the electrical parameters. These results include - and are mostly influenced by - the DC variability of the V_{ref} and I_{ref}. This is the representation of a systematic mismatch in the whole circuit, as it does not involve the Monte Carlo statistical analysis.

$V_{sg}(M18) \approx 200\ mV$, pushing the p-type current mirror $(M10, M11)$ towards the triode region, usually leading to a higher V_{out}. This is the reason why the (intrinsic) mismatch is worse in the case of $I_{load} = 0$. Analogously, when the load is maximum the $V_{sg}(M18) \approx 3\ V$, so that the channel length modulation effect of $M11$ starts kicking in ($L_{mirror} = 0.75\ \mu m$), leading to a lower V_{out}. This issue could be solved by increasing the gate length of the p-type current mirror, but this has detrimental effects on the stability of the system with no load, as it will be detailed in the following sections. As a consequence, this represents a fundamental limitation in the topology that has been chosen.

Figure 27 shows the results of the Monte Carlo simulations. It shows that the corner analysis results that have been previously analyzed represent a quite pessimistic extreme condition: in fact, in the case of figure 27, the standard variation on the output voltage is around 154 mV, while the corner analysis predicted a 3.5% tolerance. It has been observed that the n-type current mirror $M2, M3$ represents the dominant contribution to the mismatch. Thus, their dimensions have been set in order to keep them in saturation and in strong inversion (the chosen L is 4 μm). Analogously, the differential pair in the OTA $(M12, M13)$ has been kept in weak inversion.

Stability analysis The results of the stability analysis are presented in table 5. These results comprise any possible operating condition in which the circuit may be operated. It is shown that when the $I_{load} = 0$, the circuit has a better phase margin with a larger output capacitor C_{out}. Conversely, when the load is maximum, the phase margin benefits from a smaller C_{out}. This is completely in accordance with eq.6 and the related theoretical discussion: in fact, when no load is present, the C_{out} determines the dominant pole, while it represents the non dominant pole when the load is maximum.

It is worthy of attention that the stability is affected when the V_{out} is chosen to be lower (3.3 V). The explanation is related to the return ratio of the feedback loop. It is the case that the follower configuration for an op-amp is the worst scenario for its stability, since the output signal is directly fed back into the system with no attenuation: analogously, the small V_{out} configuration for the regulator is characterized by the lowest

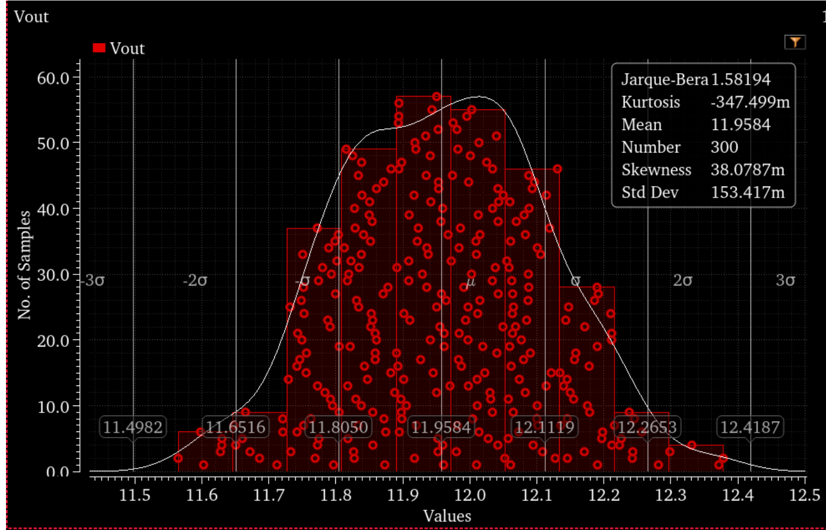


Figure 27: This figure shows the results of a Monte Carlo analysis for the $REG48V$. The simulation conditions are the following: nominal PVT conditions, $I_{load} = 80\ mA$, $V_{in} = 48\ V$, $V_{out} = 12\ V$. The number of points for the simulation is 300. These results are sufficiently general and can be extended to the other operating conditions. In this case, the mean value is 11.96 V, while the standard deviation is around $\approx 154\ mV$. These results take into account the bandgap and the beta-multiplier circuits (not ideal references).

		$I_{load} = 0$		$I_{load} = 100\ mA$	
V_{out}	Vin	$C_{out} = 0.7\ \mu F$	$C_{out} = 1.3\ \mu F$	$C_{out} = 0.7\ \mu F$	$C_{out} = 1.3\ \mu F$
3.3V	24 V	51°	62°	58°	46°
	55 V	59°	69°	61°	47°
12V	24 V	75°	81°	79°	73°
	55 V	78°	83°	83°	77°

Table 5: This table summarizes the stability results of $REG48V$ as a function of the $V_{out}, V_{in}, I_{load}$ and C_{out}. For each entry, it is only specified the worst case throughout the PVT corners, also taking into account the radiation-induced degradation of the transistor. The corners are quite conservative and consider a 5σ variation on the electrical parameters.

		$I_{load} = 0$		$I_{load} = 100\ mA$	
V_{out}	Vin	$C_{out} = 0.7\ \mu F$	$C_{out} = 1.3\ \mu F$	$C_{out} = 0.7\ \mu F$	$C_{out} = 1.3\ \mu F$
3.3V	24 V	>59dB	>59dB	>29dB	>43dB
	55 V	>60dB	>58dB	>31dB	>45dB
12V	24 V	>51dB	>51dB	>37dB	>46dB
	55 V	>49dB	>49dB	>38dB	>48dB

Table 6: This table shows the minimum values of the PSRR as a function of the frequency, considering real bias circuits and the real bandgap reference circuit. This table is quite conservative, because, for instance, these results are not representative of the PSRR in DC, which is better than what is shown here.

attenuation, since the output node is already close to the voltage level of the V_{ref} (see fig.2).

PSRR results The results for the min values of the PSRR with respect to frequency are shown in table 6. The circuit is guaranteed to work with a PSRR larger than $29dB$ in any operating condition and at any frequency. When no load is present a better PSRR is clearly observed, as it is expected from the theoretical considerations. The dip in the rejection function happens at high frequencies, usually close to the operating frequency of the buck converter system around which this regulator has to be employed.

Figure 28 shows the frequency dependence of the PSRR, by considering ideal current and voltage references. The DC rejection capability of the regulator exceeds 120 dB when the load is present (as it is commonly employed), while it is larger than 70 dB with no load. When real reference circuits are employed, the PSRR of the regulator is shaped by the bandgap and beta-multiplier frequency response.

Transient analysis Figure 26 shows the results of the simulation regarding the start-up phase of the regulator. The V_{in} rises from 0 V to 55 V with a rise time of 100 ms, which is coherent with the characteristics of the power supplies that will be employed with the regulator. A soft start is also displayed. The charging time of the output node is always around 0.5 ms. The V_{sg} of the pass transistor is kept under 3.6 V by the clamp protection circuit. The peak in the current is only due to a slight mismatch in the rising slope of both V_{out} and V_{ref}, so that that the OTA is initially significantly unbalanced. Nonetheless, the inrush process is well controlled.

SEE analysis The SEE analysis has been carried out on each individual node of the REG48V, considering the typical PVT corner for the sake of simplicity. Since a large capacitance is present at the output of this regulator ($C_{out} \approx 1\ \mu F$), the single events do not have a much effect on V_{out}. When no load is present, the worst condition is $|\Delta V_{out}| \approx 3\ mV(\left|\frac{\Delta V_{out}}{V_{out}}\right| \approx 0.03\%)$.

When the load is maximum ($I_{load} = 100\ mA$), $|\Delta V_{out}| \approx 16\ mV(\left|\frac{\Delta V_{out}}{V_{out}}\right| \approx 0.12\%)$.

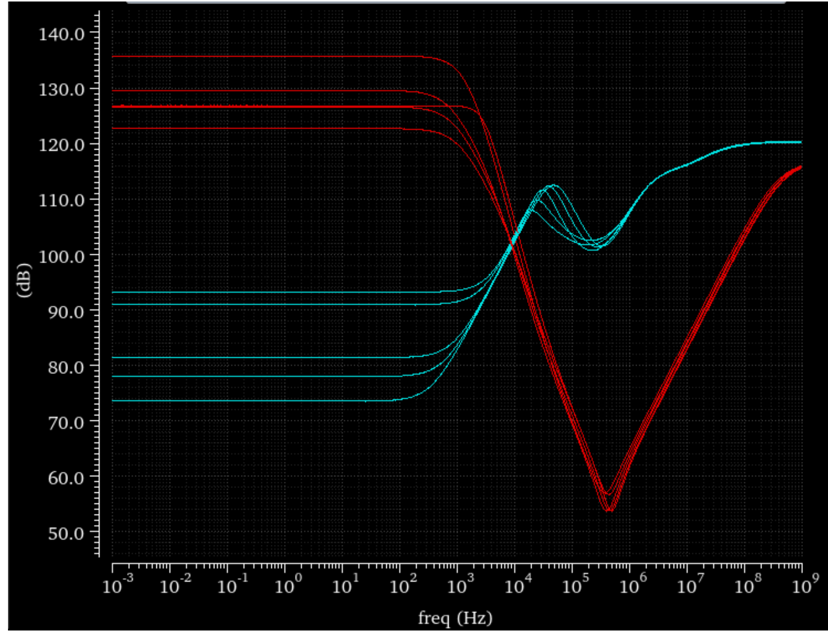


Figure 28: The PSRR figure of merit of $REG48V$ is presented. For the sake of clarity, just a few representative corners are displayed, including the radiation ones. The family of red curves refers to $I_{load} = 100\ mA$, while the cyan one to $I_{load} = 0$. The $V_{in} = 48\ V$ and $C_{out} = 1\ \mu F$. Real V_{ref} and I_{ref} references are considered. When the non-ideal bandgap reference is inserted, its finite PSRR limits the DC value in this graph. At the switching frequency of the buck converter ($f_{BUCK} \approx 2\ MHz$), the PSRR $> 60dB$.

The most sensitive nodes are the following (see figure 20): the gate of the pass transistor; those in the symmetrical branches of the OTA and, notably, the source of $M5$, due to the large C_c capacitance connecting that node directly to the output. The gate of $M27$ in the clamp circuit would be a sensitive node (most prominently when the load is maximum) but a capacitor (not shown in figure 20) has been attached there, in order to limit the voltage excursion and to avoid the undesirable turning on of $M27$.

4 Linear regulator REG12V

This chapter focuses on the design of the regulator REG12V. In the DCDC converter module, it is employed in order to feed the gate drivers, regulating their input supply voltage that could be subject to noise due to the switching phase node in the buck converter.

The circuit REG412V that is examined in this chapter is part of the chain of regulators in figure 1. A simplified schematics is shown in figure 29. Its main purpose is to feed integrated GaN driver circuit at 3.3V and the next stage of regulation (REG3P3V).

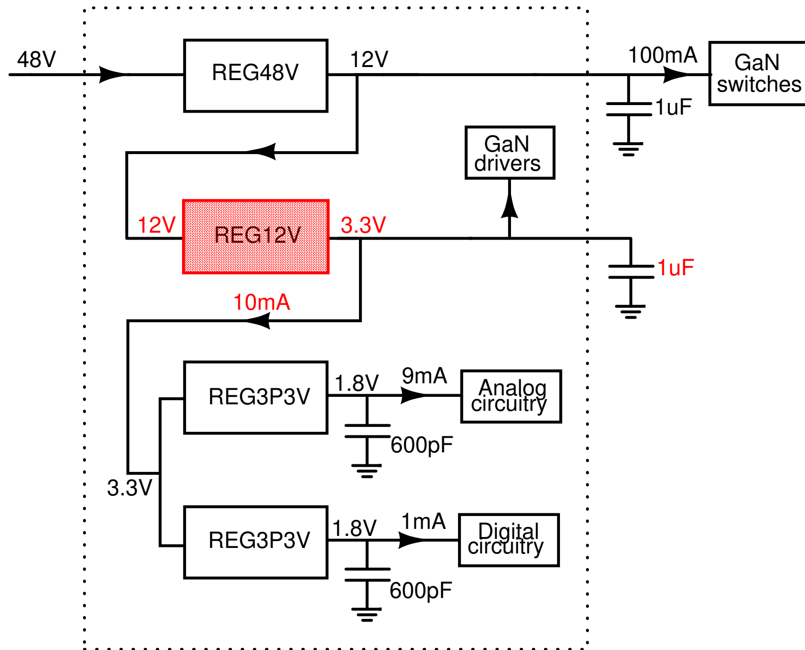


Figure 29: A simplified schematics of the module in figure 1 is presented and REG12V is highlighted.

4.1 Specifications

The operating conditions under which the regulator has to operate are shown in table 8. The radiation requirements are the same as those in $REG48V$, just like the temperature range.

On top of these operating conditions, the PVT and radiation corners are considered, along with the Montecarlo analysis.

The circuit should be stable in all the operating conditions and a phase margin greater than 45° is set as the absolute lower bound for stability. The power supply rejection ratio (PSRR) is one of the most important parameters for the linear regulator and the lower bound that meets the specs is set to be 20dB of rejection (the performance of the circuit is $> 60\ dB$, as it is shown in table 7). The mismatch of the regulator should be less than 3.5% with respect to the output voltage (usign real bandgap and

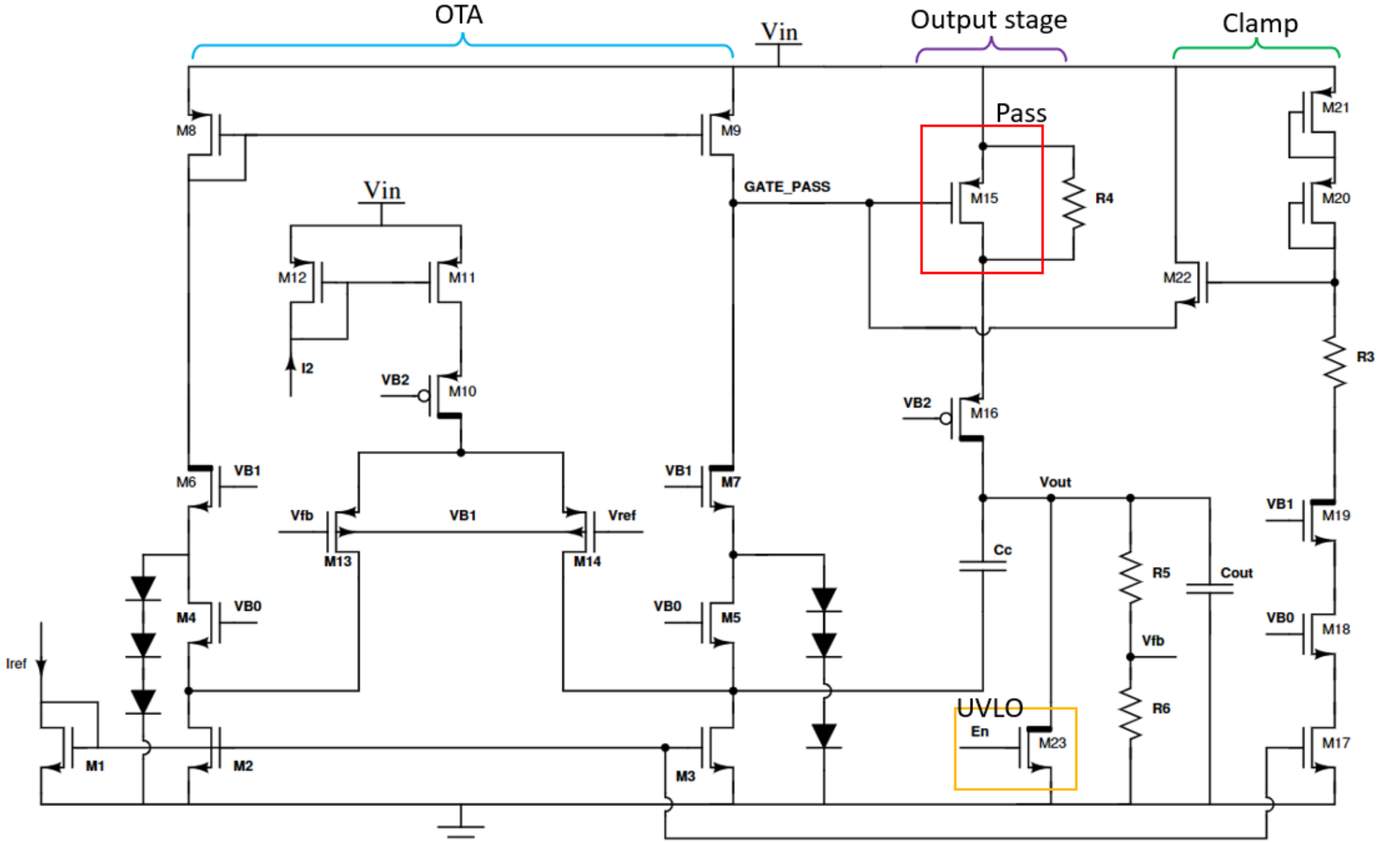


Figure 30: The simplified final schematics of the designed regulator *REG12V* is presented. A folded-cascode structure (cyan, M1-M14) is connected to the pass transistor (red, M15). The gate of the pass transistor is protected against over-voltages through a clamp structure (green, M17-M22). The biasing circuits are not shown. The UVLO (under-voltage lock-out) enabling signal is represented as En (yellow, M23).

Operating conditions	Value
Temperature	-30 $°C$ - 100$°C$
Output load I_{load}	0 - 10 mA
Input supply voltage V_{in}	4.5 V - 30V
Output voltage V_{out}	3.3 $\pm$ 3.5%
Output filter capacitance C_{out}	1 $\mu F \pm 30\%$
Phase margin	$> 45°$
PSRR at f_{SW}	> 60 dB
Total ionising dose	< 200 $Mrad$
Displacement damage fluence	$< 5 \cdot 10^{15} \frac{protons}{cm^2}$
Single event LET	$< 40 \frac{MeV \cdot cm^2}{mg}$
n-type LDMOS I_{leak}	< 5 μA
$\Delta V_{out,SEE}$	< 10 mV

Table 7: This table shows the specifications of the REG12V circuit.

	$I_{out} = 0$	$I_{out} = 10\ mA$
$V_{in} = 30\ V$	3.3%(0.36%)	3.15%(0.24%)
$V_{in} = 4.5\ V$	3.3%(0.36%)	3.15(0.24%)

Table 8: The relative variation of the output voltage ($\frac{\Delta V_{out}}{V_{out}}$) of REG12V is presented. The values within parenthesis represent the mismatch considering ideal reference voltage V_{ref} and current I_{ref}. These are the summarizing results of the whole corner analysis. The values in parentheses represent the percentage variation when considering ideal voltage and current references.

beta-multiplier circuits). During a single event, the variation on the output voltage should be minimized (here, $\Delta V_{out,SEE} < 10\ mV$). No over-voltage must take place during the start-up phase.

4.2 Circuit description

The schematic of the circuit is shown in figure 30. This circuit is constituted by a folded-cascode OTA structure and a 3.3V-rated pmos-type pass transistor ($M15$, in figure 30). Thanks to the analogous considerations in the REG48V regulator (paragraph 3.2), a IO transistor has been employed as a pass transistor. Since the circuit must be able to operate with a minimum dropout of 1.2 V ($V_{in,min} = 4.5\ V, V_{out} = 3.3\ V$, as shown in table 7), both the pass transistor $M15$ and the cascode transistor $M16$ have been oversized: the pass transistor's $\frac{W}{L}$ ratio is $\frac{200\mu m}{0.3\mu m}$, while $M16$'s one is $100 \cdot \frac{100\mu m}{1\mu m}$. This allows both transistors to stay in saturation even after the radiation effect (most prominently, after the displacement damage effects on $M16$) throughout all the operating conditions.

The OTA structure of this regulator is very similiar to the one in REG48V, but, most notably, only one LDMOS device per OTA branch is needed in order to sustain the power supply voltage (see $M6, M7$ in figure 30). This characteristic is particularly advantageous layout-wise, because it guarantees the maximum re-usability of the layout block that have been already developed for REG48V.

The clamp system ($M17$ - $M22$) is the same as that in REG48V.

The UVLO system comprises $M23$ in order to keep the output node to ground when the voltage is below the established threshold. The rise time during the start-up phase is dictated by the charging process of the output capacitor of REG48V, which takes around $\approx 500\mu m$. This system has been observe to be enough to avoid over-voltages within the circuit.

The compensation capacitor is $C_c = 30\ pF$.

4.3 Simulation results

DC analysis Table 8 shows the percentage variation of the output voltage with different load conditions of the circuit. The PVT corners have been considered, alongside the radiation corners, as it has been explained in section 2.4. It can be seen that the mismatch is mostly due to the voltage reference provided by the bandgap and beta-

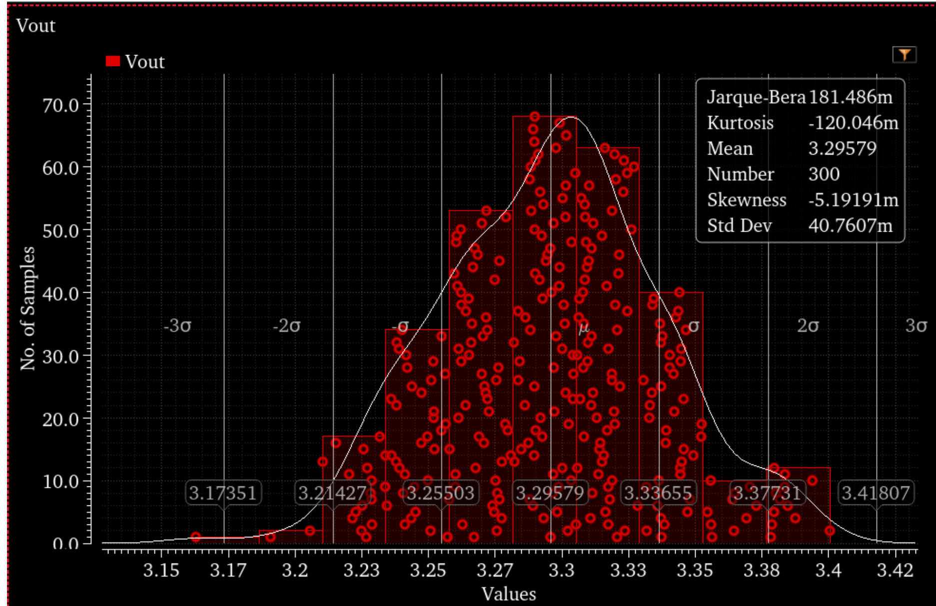


Figure 31: The results of the Montecarlo simulation for REG12V are presented. The simulation conditions are the following: nominal PVT conditions, $I_{load} = 10\ mA$, $V_{in} = 12\ V$, $V_{out} = 3.3\ V$. The number of points for the simulation is 300. The mean is 3.296 V and the standard deviation of the V_{out} is $\approx 41\ mV$. These results take into account the real band-gap and beta-multiplier circuits.

multiplier circuits, while the systematic mismatch of the circuit amounts to less than 0.4%.

Stability analysis The stability results are shown in table 4.3. These represent the worst-case scenarios regarding the PVT and the radiation corners: in fact, the lower bound of the phase margin refers specifically to the radiation corner at $TID = 200\ Mrad$ superimposed onto the slow process corner for the transistors (with a 5 sigma variation of electrical parameters). Hence, these results guarantee the system be stable in all operating conditions.

		$I_{load} = 0$	$I_{load} = 10\ mA$
$V_{in} = 4.5\ V$	$C_{out} = 700\ nF$	$> 79°$	$> 56°$
	$C_{out} = 1.3\ \mu F$	$> 83°$	$> 54°$
$V_{in} = 30\ V$	$C_{out} = 700\ nF$	$> 74°$	$> 53°$
	$C_{out} = 1.3\ \mu F$	$> 80°$	$> 48°$

Table 9: The results of the stability analysis for REG12V are shown. These represent the worst-case scenario with respect to PVT and radiation corners. The real bandgap and beta-multiplier circuits are employed for this simulation.

PSRR analysis The following scenario has been considered for the PSRR analysis: a regulator REG12V is connected in cascade to a REG48V regulator, just like in figure 1. The quantity that is ultimately simulated is at the first order of approximation

		$I_{load} = 0$	$I_{load} = 10\ mA$
$V_{in} = 4.5\ V$	$C_{out} = 700\ nF$	$> 59.7\ dB$	$> 61.7\ dB$
	$C_{out} = 1.3\ \mu F$	$> 59.7\ dB$	$> 58.5\ dB$
$V_{in} = 30\ V$	$C_{out} = 700\ nF$	$> 59.6\ dB$	$> 62.9\ dB$
	$C_{out} = 1.3\ \mu F$	$> 59.6\ dB$	$> 60\ dB$

Table 10: The results of the PSRR analysis of REG12V are shown. These represent the worst-case scenario regarding the PVT and radiation corners and across all frequencies. The real bandgap and beta-multiplier circuits are considered in the simulation.

$$\delta V_{out,\ 3.3\ V} = \left(\frac{\partial V_{out}}{\partial V_{in,12\ V}} \cdot \frac{\partial V_{in,\ 12\ V}}{\partial V_{in,\ 48\ V}} + \frac{\partial V_{out}}{\partial V_{ref}} \cdot \frac{\partial V_{ref}}{\partial V_{in,\ 48\ V}} + \frac{\partial V_{out}}{\partial I_{ref}} \cdot \frac{\partial I_{ref}}{\partial V_{in,\ 48\ V}} \right) \cdot \delta V_{in,\ 48\ V} \tag{14}$$

where $V_{in,48V}$ is the input of the REG48V, $V_{in,12V}$ is the output of REG48V and the input of REG12V, and V_{out} is the ouput of REG12V (see figure 1). At the level of simulation, a perturbation is injected into $V_{in,\ 48\ V}$, since it represents the noisy power supply: experimentally, the oscillations in its value may reach few volts. The input voltage perturbation $V_{in,12\ V}$ is the result of the filtering of the $\delta V_{in,48\ V}$, thanks to the power-supply rejection of the REG48V regulator: as a consequence, the first term in eq. 14 is completely negligible (the yellow curve in figure 32 remains unchanged when the input of REG12V is fed by an ideal generator instead of the output of the REG48V). The high-voltage bandgap and the beta-multiplier circuits must be connected to the 48 V power supply ($V_{in,48V}$) and the overall perturbation at their output (V_{ref}) is directly affected by $V_{in,48\ V}$ (second and third term in eq. 14 and red and cyan curve in figure 32). It is observed that the latter terms dominate the output perturbation of the overall chain: when considering the non-ideal bandgap and beta-multiplier circuits, the regulator is guaranteed to work with at least 58 dB of attenuation at all frequencies, at any input voltage, with a ±30% tolerance on the output capacitor C_{out} and throughout all process corners (see figure 4.3).

SEE analysis The SEE analysis, as it has been detailed previously, has been carried out on each individual node, considering the typical PVT corner. The impulsive response of the V_{out} when no load is present are shown in figure 12. Just like the REG48V, the single events do not have much effect on the output voltage due to the large C_{out}. When no load is present, the worst condition is represented by the overshoots in V_{out}, leading to a $\Delta V_{out} \approx 2\ mV(\frac{\Delta V_{out}}{V_{out}} \approx 0.06\%)$.

When the load is maximum ($I_{load} = 10\ mA$), also the undershoots in the V_{out} are not negligible. A $\Delta V_{out} \approx \pm 8\ mV(\frac{\Delta V_{out}}{V_{out}} \approx \pm 0.25\%)$.

The most sensitive nodes are the following (see figure 30): the gate of the pass transistor; those in the symmetrical branches of the OTA and, notably, the source of $M5$, due to the large C_c capacitance connecting that node directly to the output; the gate of $M22$ in the clamp circuit.

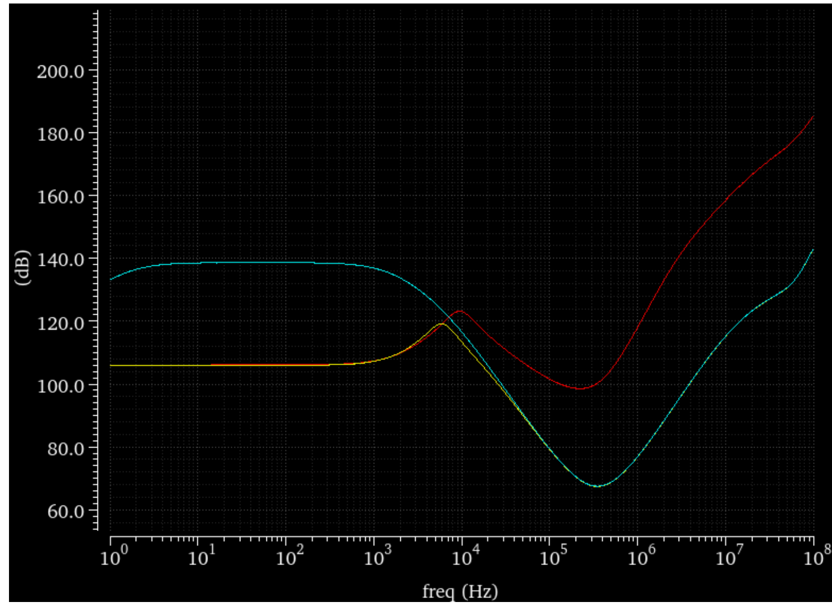


Figure 32: An example of the PSRR of the REG12V circuit is presented, considering a typical corner with maximum load. The yellow curve represents the PSRR with the real bandgap and beta-multiplier circuits. The red curve represents the perturbation in the output voltage due to the variation in the V_{ref} (second term in eq.14), while the cyan curve refers to the variation in the I_{ref} (third term in eq.14). The transfer functions for the different contributions have been singled out through large capacitors ($\approx 1\ \mu F$) at the outputs of the bias circuits.

5 Linear regulator REG3P3V

The circuit REG3P3V that is examined in this chapter is part of the chain of regulators in figure 1. A simplified schematics is shown in figure 33. In the chip two REG3P3V regulators are employed and they separately feed the analog and the digital circuitry of the controller for the buck converter. The current rating of this type of regulator is 10 mA, but the analog and digital parts have different current requirements, i.e., 9 mA and 1 mA respectively.

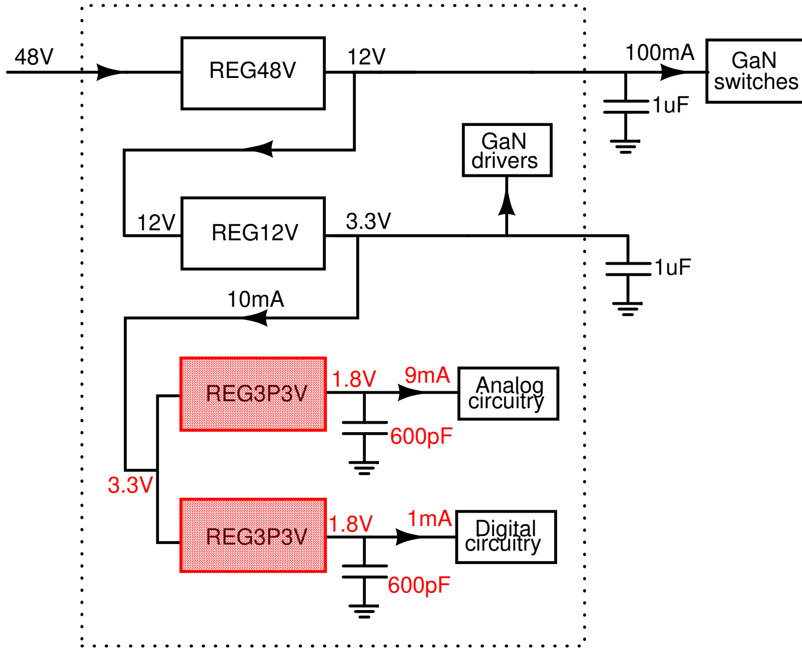


Figure 33: A simplified schematics of the module in figure 1 is presented and REG3P3V is highlighted.

5.1 Specifications

This chapter deals with the linear regulator REG3P3V, which is used in order to feed the 1.8‘; V controller circuit. The specifications are shown in table 11.

The radiation requirements are the same as those in REG48V , just like the temperature range. On top of these operating conditions, the PVT and radiation corners are considered, along with the Montecarlo analysis.

This circuits is characterized by a fully-integrated output capacitor $C_{out} = 600\ pF$, which is implemented employing MOSCAP capacitors (capacitance density of $\approx 5\frac{fF}{\mu m^2}$), due to the low-voltage output voltage. Since the capacitive load of this regulator REG3P3V is lower than the one in REG48V and REG12V, which are carachterized by $C_{out} \approx 1\ \mu F$, the stability requirements are achieved more easily through the employment of a Miller compensation capacitor.

The circuit should be stable in all the operating conditions and a phase margin greater than 45° is set as the absolute lower bound for stability. The lower bound on PSRR that meets the specs is set to be 20dB of rejection (the performance of the circuit

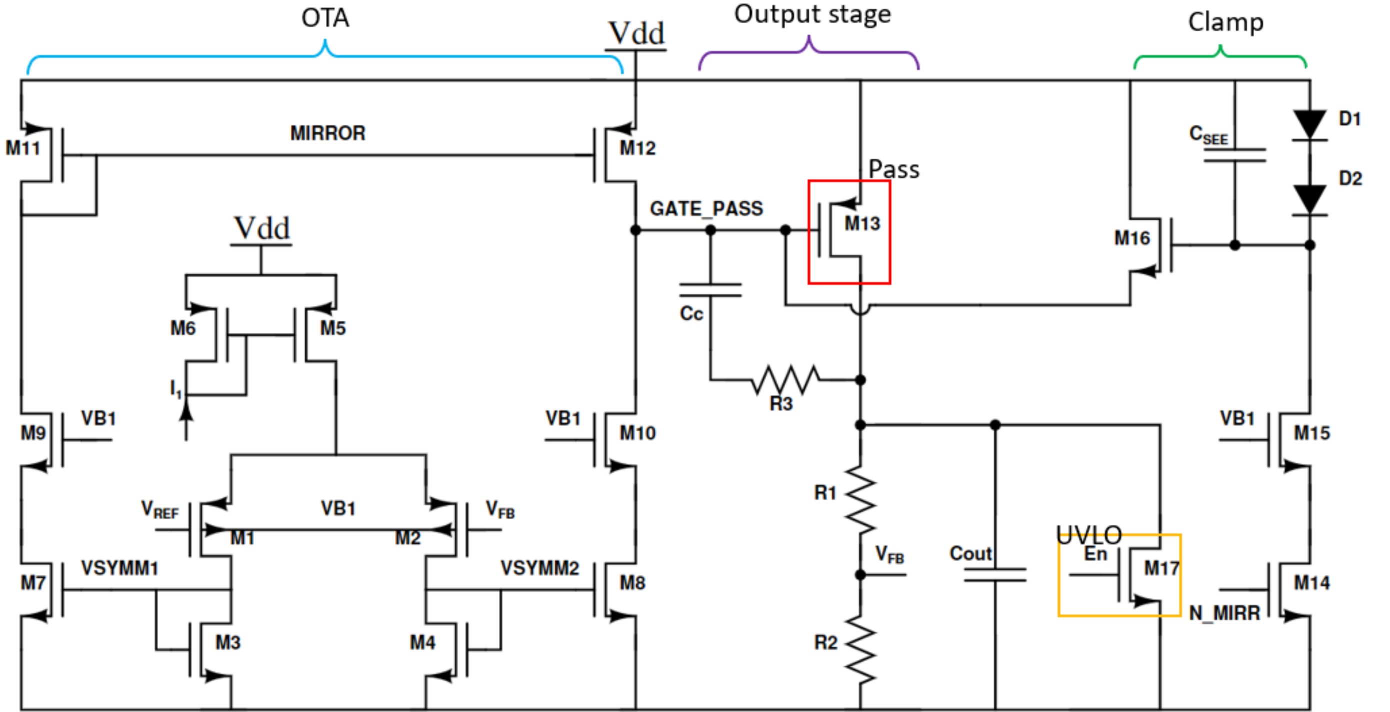


Figure 34: The simplified final schematics of the designed regulator *REG3P3V* is presented. A symmetrical OTA structure (cyan, M1-M12) is connected to the pass transistor (red, M13). The gate of the pass transistor is protected against over-voltages through a clamp structure (green, M14-M16). The biasing circuits are not shown. The UVLO (under-voltage lock-out) enabling signal is represented as En (yellow, M17).

Operating conditions	Value
Temperature	-30 $°C$ - 100$°C$
Output load I_{load}	0 - 10 mA
Input supply voltage V_{in}	3.3 $\pm$ 10%
Output voltage V_{out}	1.8 $\pm$ 3.5%
Total ionising dose	$<$ 200 $Mrad$
Displacement damage fluence	$< 5 \cdot 10^{15} \frac{protons}{cm^2}$
n-type LDMOS I_{leak}	$<$ 5 μA
Single event LET	$< 40 \frac{MeV \cdot cm^2}{mg}$
Phase margin	$>$ 45°
PSRR	$>$ 60 dB
$\|\Delta V_{out,SEE}\|$	$<$ 160 mV

Table 11: This table shows the specifications of the REG3P3V circuit.

is $>$ 60 dB, as it is shown in table 11). The mismatch of the regulator should be less than 3.5% with respect to the output voltage (using real bandgap and beta-multiplier circuits). During a single event, the variation on the output voltage should be less than 10%. No over-voltage must take place during the start-up phase.

5.2 Circuit description

A 3.3V-rated low-voltage p-type pass transistor has been selected. Due to the large variation in the load condition of the regulator and also considering the SOA specification for the maximum gate voltage, this choice allows to have enough margin on the voltage swing of $V_{sg}(M13)$ in order not to push the current mirror $M11, M12$ into triode region: if this were not the case, a detrimental offset would affect the regulator and it might damage the delicate 1.8V-rated circuitry connected to it. Following an analogous line of reasoning, the previously-mentioned p-type current mirror cannot be upgraded to a cascoded version.

In this regulator, the feedback current is set by $R1, R2$ to be around 30 μA.

The schematics of the regulator REG3P3V is shown in figure 34. In order to minimize the mismatch and, consequently, the offset on the output V_{out}, a fully symmetrical topology for the OTA has been designed.

Since the output capacitor C_{out} is an integrated MOSCAP capacitor, the SEE are of concern, conversely to what happened with REG48V and REG12V. Therefore, the compensation capacitor C_c has been connected directly on the gate of the pass transistor $M13$, in order to increase the capacitance at that node and to reduce the voltage swing. In fact, ΔV_{out} can be estimated as

$$\Delta V_{GATE_PASS} = \frac{1}{C_{GATE_PASS}} \cdot \int I_{PULSE}(t)\, dt \tag{15}$$

where I_{PULSE} is the impulsive current injection due to the SEE and shown in figure 12. The issue with this solution is that the PSRR is degraded, as it is shown in figure 23, since C_c provides a direct path for AC perturbation in the supply voltage to the output node. The resistor R_3 is connected in series to C_c, in order to generate a relatively high-frequency zero and, by doing so, improving the stability of the circuit: nevertheless, the series resistance has a negative impact on the PSRR and the SEE response, so that a trade-off is to be found. The value for the C_c is 20 pF, while R_3 is 15 $k\Omega$.

The clamp system ($M14$ - $M16$) is designed in a similar fashion with respect to REG48V and REG12V, just like the UVLO control ($M17$).

5.3 Simulation results

	$I_{out} = 0$	$I_{out} = 10\ mA$
$\frac{\Delta V_{out}}{V_{out}}$	3.3%(0.2%)	3.2%(0.1%)

Table 12: The DC results of the REG3P3V are shown. Specifically, the table highlights the relative variation of the V_{out} with respect to its nominal value 1.8 V throughout all the PVT and radiation corners. These values represent the worst-case scenario throughout the PVT and radiation corners. The value within parenthesis are related to the ΔV_{out} when the voltage and current reference circuits are ideal.

DC results As it is shown in figure 12, the output voltage of the regulator has a maximum variation of 3.3%, considering every PVT and radiation corners. It is interesting to notice that such variation is mostly due to the accuracy of the band-gap reference circuit: if an ideal one is considered, the percentage variation at the output drops to 0.2% in the worst case. The Montecarlo results are shown in figure 35. The mean V_{out} is observed to be 1.798 V and the standard deviation is around $\approx 23\ mV$.

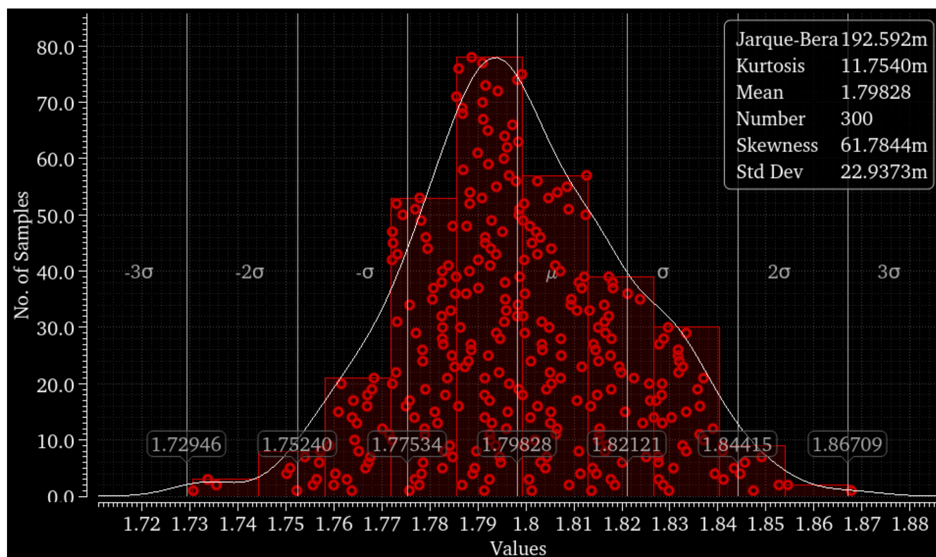


Figure 35: The Montecarlo simulation result of the V_{out} of REG3P3V. The simulation conditions are the following: nominal PVT conditions, $I_{load} = 10\ mA$, $V_{in} = 3.3\ V$, $V_{out} = 1.8\ V$. The number of points for the simulation is 300. The mean V_{out} is $\mu = 1.789\ V$ and the standard deviation is $\sigma \approx 23\ mV$. These results take into consideration the real reference voltage and current circuits.

STB results The results of the stability analysis are shown in table 13. The results represent a worst-case scenario and they guarantee that the circuit does not suffer from reliability issues.

	$I_{out} = 0$	$I_{out} = 10\ mA$
Phase margin	$> 45.6°$	$> 66.5°$

Table 13: The stability analysis of the REG3P3V are shown. The real reference circuits for V_{ref} and the current reference are considered. These results represent the worst-case scenario throughout all the PVT and the radiation corners.

PSRR results The PSRR simulations show that the the minimum rejection capability of the regulator is $> 64.3\ dB$, which is at least a factor of 1600. It is interesting to note that the PSRR value here is close to result obtained for the regulator REG12V: this is a reasonable consequence of the fact that the PSRR is dominated by the bandgap reference and by the beta multiplier circuits, as the input voltage V_{in} perturbations are already attenuated by two stages of regulation.

SEE analysis As it has been stated before, the SEE have a detrimental on this circuit, due to the relatively-small value integrated C_{out}. As it was the case for the other regulators, the most sensitive nodes are the ones in the OTA, the $GATE_PASS$. Moreover, the gate of $M16$ is observed to be critical, so that a MOSCAP-type capacitor $C_{SEE} = 2\ pF$ has been attached to it, in order to limit the voltage swing, which could potentially turn off the pass transistor and, consequently, induce an undervoltage on the output node: this is the most critical condition for the digital low-voltage circuitry attached to this regulator.

The results of the SEE analysis are the following: when no load is present, the peak overvoltage is $55\ mV(\frac{\Delta V_{out}}{V_{out}} \approx 3\%)$ and the peak undervoltage is $-21\ mV(\frac{\Delta V_{out}}{V_{out}} \approx -1.2\%)$; when the load is present the peak overvoltage is $156\ mV(\frac{\Delta V_{out}}{V_{out}} \approx 8.7\%)$ and the maximum undervoltage is $-80\ mV(\frac{\Delta V_{out}}{V_{out}} \approx -4.5\%)$.

6 ELT transistor modeling

This chapter aims at describing a simple model which has been developed during this thesis and which has been proven to provide a useful description of the equivalent electrical parameters of ELT transistors. Further work and more measurement data are needed to ultimately assess its effectiveness.

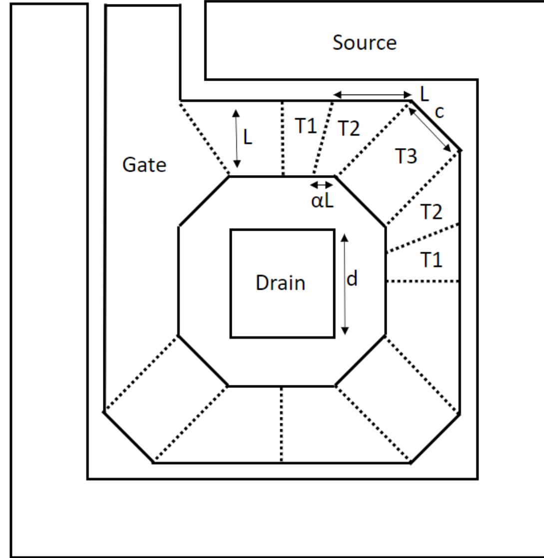


Figure 36: The figure represents the layout of an ELT (enclosed-layout) transistor. Here are highlighted the portions in which the channel is divided in the work of [4].

There have been valuable contribution in the modeling of the ELT transistor's electrical parameters ([4], [3], [2]) and the minimum ratio $\frac{W}{L}$ can be described by eq. 16 (ref. [4])

$$\left(\frac{W}{L}\right)_{eq}^{min} = 4 \cdot 2\frac{\alpha}{\log(\frac{d}{d-2\alpha L})} + 4 \cdot 2\frac{1}{\Delta(\alpha)}\frac{1-\alpha}{-\log(\alpha)} + k \cdot \frac{c}{L\sqrt{2}} \tag{16}$$

where α and k are an empirical parameters, d is the minimum size of the drain contact and c is the length of the oblique corner of the transistor (see figure 36). In the work in ref. [4], three distinct portions of the channel are identified: the region where the electric field is parallel to the channel length L (T1), where it bends due to the corners (T2), while the T3 region is related to the oblique corners. Each term in eq.16 is associated with one of these three regions. It is assumed that the the distance from the corner at which the electric field is influenced by it is $\alpha \cdot L$ [4]. Moreover, the parameter K takes into account the fact that the source implantation in the upper-left corner is interrupted by the presence of the poly-silicon, so that it is accounted for with a fractional contribution.

The width of the transistor is intuitively proportional to the perimeter of the contact. Given the minimum W_{min} that the geometrical constraints impose, due to the minimum dimensions of the first metal contact (DRC rules for the technology), the required W_{design} can be obtained by stretching correspondingly the dimensions in the

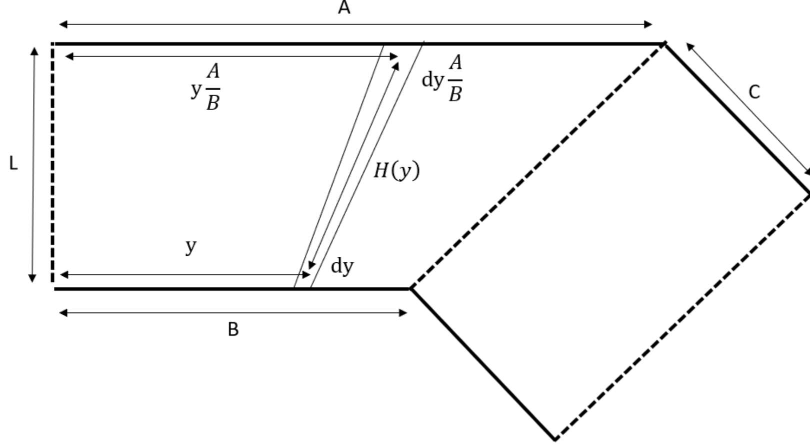


Figure 37: All the relevant parameters of the derivation are represented. Only the poly-silicon gate is shown and the source and drain contacts are omitted.

layout. This process is implemented automatically in the PCell (Parametrized Cell) that has been developed for this thesis.

Nevertheless, large Ls are required when tight matching is crucial. The previously-discussed model has an issue when $\alpha \cdot L \approx B$ (see figure 37), since the short edge of T1 is reduced to a single point, so that the current associated with that region drops to zero: from this point on, the first term in eq. 16 becomes negligible. During this master thesis, a simple model for large values of L has been derived, following the lead of ref. [4].

At first a simple correction to the model has been applied, by saturating the αL distance from the corner to some maximum value for large Ls, so that the region T1 always keeps having a significant contribution: this model is referred to as "model 2".

Nevertheless, another approach has been followed, in order to be able to reduce the number of empirical parameters and in order to have a continuous function throughout all the range of L. This model merges together the regions T1 and T2 in fig 36, so that the dependence on the fitting parameter α is avoided. Such a simple derivation is now presented.

Given a large L and the minimum width W_{min}, it is reasonable to assume that the equi-potential curves in the ELT transistor are closer to circles than to squares. Thus, the electric field lines are considered as radial. In reality, the field lines have the tendency to be parallel to the channel L close to region T1, so that the drift current takes the least resistance path. Moreover the electric field lines must be perpendicular to the high-doping implantations for the source and drain, deviating from the radial path.

Both the A and B edges are divided into small slices Δy and the current contribution of each slice is computed. The current flow is parallel to the electric field lines and the length of the path of each slice is $H(y)$ (eq. 17)

$$H(y) = \sqrt{\left(y\frac{A}{B} - y\right)^2 + L^2} \tag{17}$$

From the fundamental MOSFET equation 18, we consider the differential current contribution of each slice (namely $I(y)$).

$$\int_{x=0}^{x=H(y)} \frac{I(y)\ dy}{W(x,\ \Delta y)}\ dx = \int_{\phi=Vs}^{\phi=Vd} \mu \cdot Q(\phi)\ d\phi \tag{18}$$

where ϕ is the electrical potential, $Q(\phi)$ is the superficial density of (inversion) charge, μ is the (effective) mobility of the carriers and $W(x,\ \Delta y)$ provides a linear mapping between the short and long edges of the trapezoidal shape, serving to properly scale the differential element dy along $H(y)$. The current is assumed to be perpendicular to this direction, which is a reasonable assumption as the width of the slice is infinitesimal in the limiting case in which the electric field lines are distributed radially.

$$W(x,\ \Delta y) = \Delta y \cdot \frac{A}{B} + \Delta y \cdot \frac{1 - \frac{A}{B}}{H(y)} \cdot x \tag{19}$$

Since the electric field is assumed to be radial, all the slices can be considered as many transistor in parallel. This assumption tends to overestimate the total current and it will be checked experimentally: this is because the field will strongly bend close to the corners, so that in principle the parallel transistors that have just been defined should not be considered as independent from each other. The equivalent $\frac{W}{L}$ ratio can be expressed as follows (eq. 20)

$$\left(\frac{W}{L}\right)_{eq}^{T1,\,T2} = \sum_{\Delta y} \frac{1}{\int_{x=0}^{x=H(y)} \frac{dx}{W(x,\,\Delta y)}} \tag{20}$$

By solving the integral with respect to the variable x and as $\Delta y \to 0$, it follows that

$$\left(\frac{W}{L}\right)_{eq}^{T1,\,T2} = \int_{y=0}^{y=B} \left(1 - \frac{A}{B}\right) \frac{1}{H(y)} \frac{1}{\ln\left(\frac{B}{A}\right)}\ dy \tag{21}$$

and, finally,

$$\left(\frac{W}{L}\right)_{eq}^{T1,\,T2} = \frac{1}{\ln\left(\frac{A}{B}\right)} \cdot asinh\left(\frac{A-B}{L}\right) \tag{22}$$

where $asinh$ is the inverse function of the hyperbolic sine.

It is worth highlighting that when $A - B \approx L$ (see figure 36), eq. 22 becomes

$$\left(\frac{W}{L}\right)_{eq}^{T1,\,T2} \approx 0.88 \cdot \frac{1}{\ln\left(\frac{A}{B}\right)} \tag{23}$$

coherently with the results shown in ref. [3]. Nevertheless, eq. 22 is much more general and allows for flexibility in the description of the transistor geometry.

Equation 22 represents the contribution to the current of the T1 and T2 regions in figure 36 and there are eight such regions. Moreover, the T3 contribution is simply taken from the model in ref [4]. The final expression for the equivalent $\frac{W}{L}$ ratio is

$$\left(\frac{W}{L}\right)_{eq}^{min} = 2 \cdot k \cdot \left(\frac{W}{L}\right)_{eq}^{T1,\, T2} + k \cdot \frac{C}{L\sqrt{2}} \tag{24}$$

The derived expression only relies on the assumption that the field in the channel is radial and it is always continuous throughout the range of values for L. The parameter k is not mandatory to this model, as long as the detailed geometry of the ELT layout is considered in eq. 16 through A and B, discriminating among the different regions: thus, k is not to be considered a fitting parameter, as it will be shown later.

In order to establish the accuracy of the proposed model, measurement data on a 65nm technology has been analysed (see figure 38): "model 1" is from [4]; "model 2" is considerably similiar to model 1 and it only comprises few corrections, i.e., saturation of $\alpha \cdot L$ for large values of L; "model 3" is the newly proposed model that has been discussed. The measured $I_D - V_D$ characteristics of minimum-sized ELT transistors were exploited in order to obtain their equivalent min $\left(\frac{W}{L}\right)_{eq}^{min}$. A simple statistical analysis has been carried out considering many test chips and many devices within the same chip, in order to correct for inter- and intra-chip variability. For each value of L, different biasing conditions have been considered: $V_{gs,\, bias} = 600\ mV, 800\ mV, 1\ V$ and $1.2\ V$, which are all plotted in figure 39: the extracted $\left(\frac{W}{L}\right)_{eq}^{min}$ with different $V_{gs,\, bias}$ are observed to slightly differ from each other. Moreover, the measurement data regarding the $I_D - V_G$ characteristics of the ELT transistors has been taken into consideration to guarantee good fitting results. Then, the obtained equivalent $\frac{W}{L}$ of the fabricated devices were compared with the theoretical models.

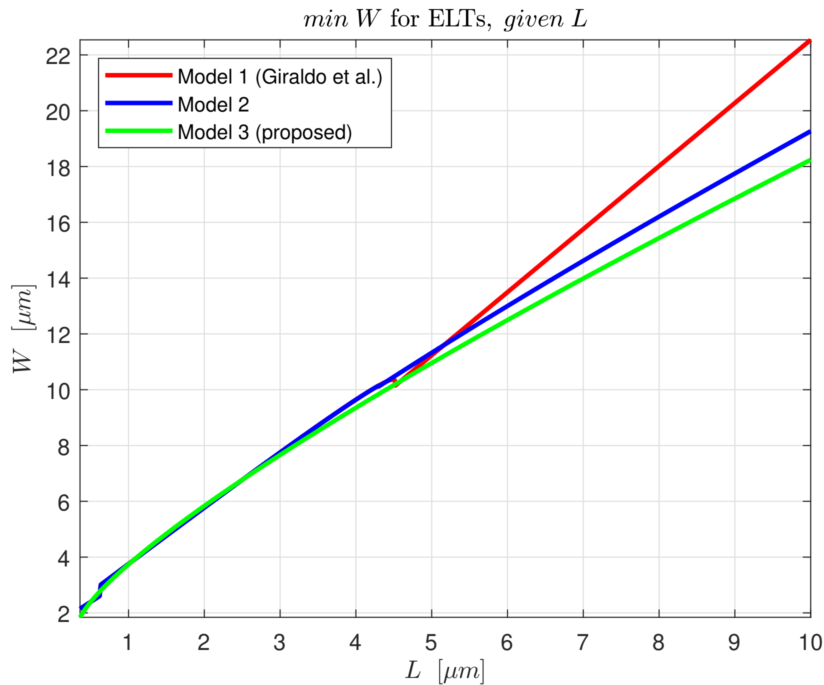
It is interesting to observe that the new model accurately describes the electrical characteristics of the ELT transistors at $L = 4\mu m$, with an error of 6% with respect to the measurement data (see figure 39). On the other hand, model 1 from ref. [4] presents an relative error of 20%. For small values of L, the three models do not differ significantly, yielding a maximum error of 9% for $L < 120\ nm$. Unlike models 1 and 2, no fitting parameters have been exploited to obtain the green curve for the new "model 3" in figure 38: the different geometrical regions of the ELT layout have been accurately described through eq. 22; neither the k parameter nor the α one have been used; no effective correction of the channel length has been considered.

On a final note, the equivalent length L_{eq} does not precisely correspond to the L in figure 37, due to the longer path the current would follow towards the corners of the ELT layout within the frame of the proposed model. In order to account for this phenomenon at the first order of approximation, a correction factor is proposed, based on the harmonic average of the length of the current paths: using such an average, smaller values of $H(y)$ have a larger impact on the final result L_{eq}, reflecting the fact that the current preferential path is the shortest one. Referring to figure 37,

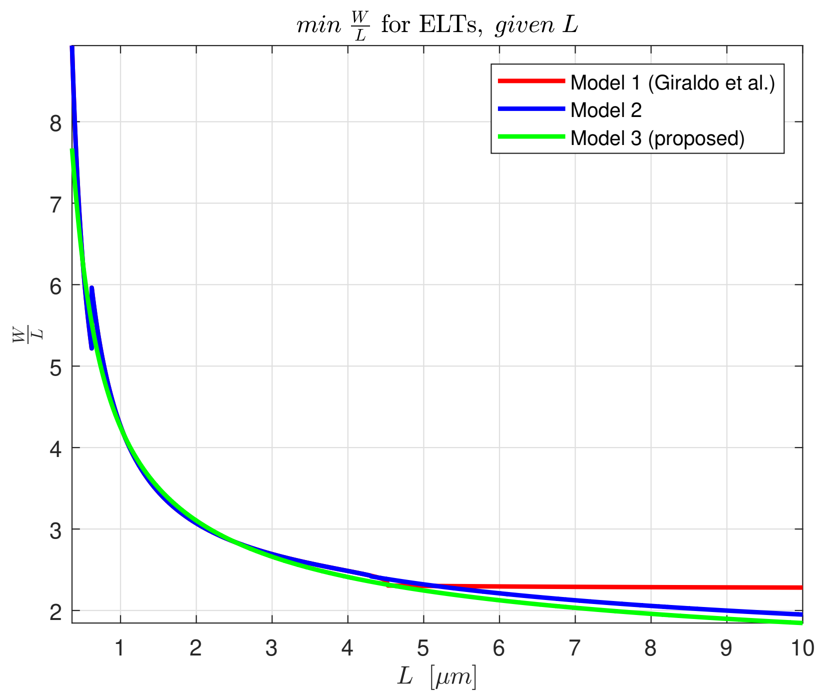
$$\frac{1}{L_{eq}} = \frac{1}{B} \cdot \int_{y=0}^{y=B} \frac{1}{H(y)}\, dy, \tag{25}$$

which would lead to

$$L_{eq} \approx 1.13 \cdot L \tag{26}$$

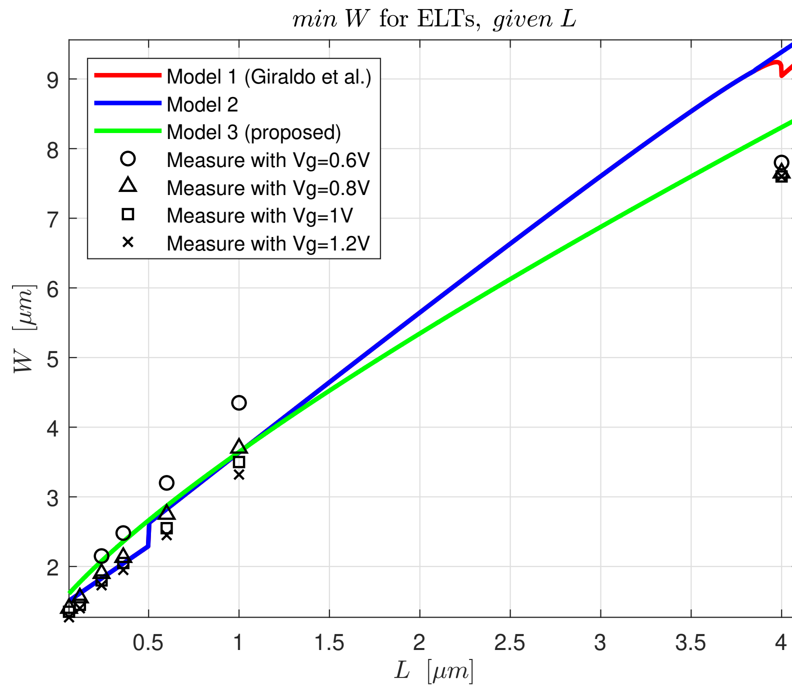


(a)

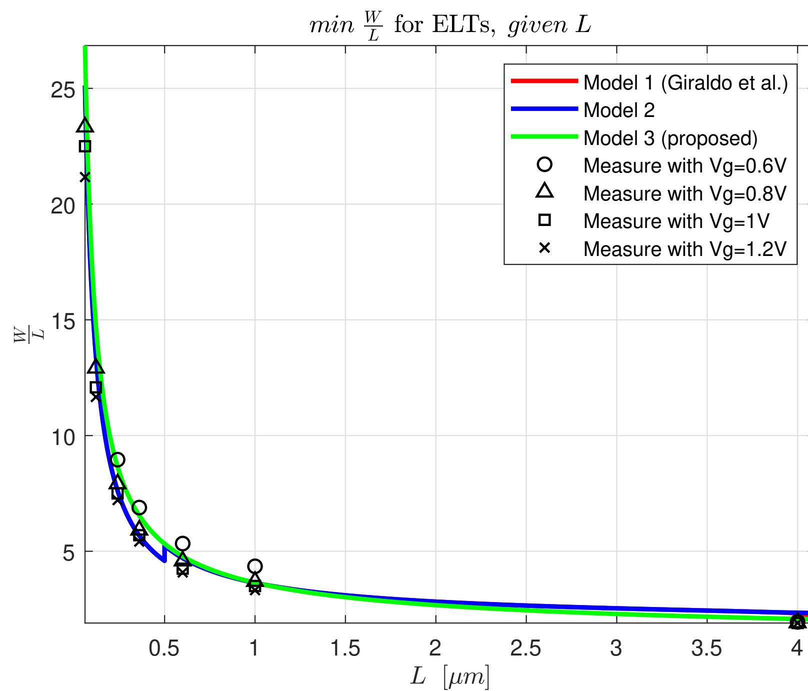


(b)

Figure 38: The minimum $\frac{W}{L}$ and W achievable given a certain L are presented, considering three distinct models for the electrical behaviour of ELT devices. The red curve is the original model proposed by ref. [4]. The model related to the blue curve implements additional corrections on top of the original one. The green curve is the result of the newly developed model.



(a)



(b)

Figure 39: The measurement data on a 65nm technology are presented (purple points) and compared to the theoretical models. The data points have been extracted from measurement with diverse bias conditions. The red curve is the original model proposed by ref. [4]. The model related to the blue curve implements additional corrections on top of the original one. The green curve is the result of the newly developed model.

Finally, the min W_{eq}^{min} can be obtained as

$$W_{eq}^{min} = \left(\frac{W}{L}\right)_{eq}^{min} \cdot L_{eq} \tag{27}$$

7 Conclusion

In this work, rad-hard analog blocks for a DC/DC (buck) converter module have been developed for LHC experiments at CERN. Specifically, the design, the simulations and the layout of a chain of three linear regulators (REG48V, REG5V, REG3P3V) constitute the main focus of this thesis. LDMOS (30V-rated), IO (3.3V-rated) and core (1.8V-rated) transistors have been exploited in the design.

Radiation effects have been taken into account, considering a TID dose $< 200\ Mrad$, a displacement damage (DD) fluence $< 5 \cdot 10^{15}\ \frac{protons}{cm^2}$ and single events SEE with LET $< 40\ \frac{MeV \cdot cm^2}{mg}$. In order to do so, radiation models have been developed and employed in the CAE simulation environment, on top of the standard PVT corners and the Montecarlo analysis. The parameters to this models have been extracted from experimental data. The threshold voltage shift ΔV_{th}, the I_{on} degradation, the leakage current and the increased resistivity of high-voltage devices due to DD have been modeled.

All the circuits have been successfully designed to work in a broad range of operating conditions, comprising process, temperature, radiation corners and V_{in}, V_{out} and I_{load} ranges: as a final result, their output voltage is affected overall by a maximum of $\pm 3.5\%$ offset with respect to the nominal value. The designed UVLO (under-voltage lockout) system ensures that the regulators are not operated when the input supply voltage is too low, in order to avoid unpredictable and improper outcomes. Moreover, reliability issues have been carefully addressed, in order to allow a 10-year operation: electro-migration, radiation-induced degradation and SOAs (safe operating area) have been taken into account.

REG48V is able to withstand a 100 mA load current, when the V_{in} varies in the range 23 V - 55 V (14 V - 55 V pre-rad) and the output voltage V_{out} is configurable to be in the range 3.3 V - 12 V.

REG12V is able to withstand a 10 mA load current, when $V_{out} = 3.3\ V$ and V_{in} ranges from 4.5 V to 30 V (1.2 V minimum dropout).

REG3P3V is able to withstand a 10 mA load current, when $V_{in} = 3.3\ V \pm 10\%$ and $V_{out} = 1.8\ V$. When impulsive single events happen, the V_{out} has been observed to vary by 8% in the worst case.

These regulators circuits will be integrated in a ASIC in the near future, as the building blocks for a new 48 $V \rightarrow 5\ V$ DC/DC rad-hard buck converter.

A model of the electrical parameters of the ELT (enclosed-layout transistors) devices has been proposed, in order to improve the physical description of the minimum $\left(\frac{W}{L}\right)_{eq}^{min}$ allowed given a certain L. Considering the measurement data for a 65 nm technology, this model aligns well with the those in the literature for small values of L (less than 9% error) , while introducing a significant improvement of 13.5% for large Ls. It is interesting to note that no fitting parameters are present. Further work should be carried out in order to assess the accuracy of this new model.

The final period for this thesis was dedicated to the layout of the aforementioned

blocks, ensuring good matching, keeping the current density under control in every section of the devices (electro-migration issues) and developing a PCell using the SKILL language in order to make the layout process of ELT (enclosed-layout transistor) devices easier.

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