Politecnico di Torino

Master's Degree course in Micro- and Nanotechnologies for Integrated Systems

Master's Degree Thesis

Design of radiation-tolerant current and voltage reference circuits in a 0.18 µm high-voltage CMOS technology

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Abstract

At the forefront of particle physics research lies CERN, the European Organization for Nuclear Research. Here, thanks to the presence of cutting-edge particle accelerators (mainly Large Hadron Collider (LHC)) and detectors, scientists are constantly extending the knowledge of the universe.

The upgrade of the LHC (HL-LHC) will lead to an increase of the amount of data collected by the detectors, requiring higher power consumption in the front-end circuits. In this context, efficiently providing different supply voltages to the front-end circuits while minimizing power consumption becomes a challenging task. Currently, the power distribution scheme for the HL-LHC upgrade is based on different stages of DC-DC converters placed close to the collision point, constantly subjected to high levels of radiation. Within this innovative environment, this master thesis project contributes to the advancement in the development of radiation-tolerant electronic circuits employed in CERN's converters.

The heart of this project is the design of two radiation-hard voltage reference circuits. These blocks are crucial to provide a reference voltage to the other circuitry of the controller of a $48\,\mathrm{V} \rightarrow 5\,\mathrm{V}$ buck converter. In particular, a low-voltage circuit is designed to generate the reference voltage for the control circuitry and a high-voltage version instead necessary for the chain of linear regulators present in the controller block. Additionally, two high-voltage and low-voltage current reference circuits are designed.

Since the circuits must withstand extreme radiation conditions, it is crucial to intervene already in the design phase. Thus, different models are developed to forecast transistors' behavior in response to radiation, allowing the early simulation of the circuits in radiation conditions.

Sommario

All'avanguardia nella ricerca sulla fisica delle particelle si trova il CERN, l'Organizzazione Europea per la Ricerca Nucleare. Qui, grazie alla presenza di innovativi acceleratori di particelle (principalmente il Large Hadron Collider (LHC)) e di rivelatori, gli scienziati stanno costantemente ampliando la conoscenza dell'universo. Il potenziamento dell'LHC (HL-LHC) porterà a un aumento della quantità di dati raccolti dai rivelatori, richiedendo un maggiore consumo di energia nei circuiti front-end. In questo contesto, fornire in modo efficiente diverse tensioni di alimentazione ai circuiti front-end riducendo al minimo il consumo di energia è complicato. Attualmente, lo schema di distribuzione dell'energia per l'HL-LHC si basa su diversi stadi di convertitori DC-DC posizionati vicino al punto di collisione delle particelle, costantemente sottoposti a livelli elevati di radiazioni. All'interno di questo ambiente innovativo, questo progetto di tesi contribuisce allo sviluppo dei circuiti elettronici resistenti alle radiazioni impiegati nei convertitori del CERN. Il cuore di questo progetto è lo sviluppo di due circuiti di riferimento di tensione resistenti alle radiazioni. Questi blocchi sono cruciali per fornire una tensione di riferimento agli altri circuiti del controllore di un convertitore buck 48 V $\rightarrow$ 5 V. In particolare, un circuito a bassa tensione genera la tensione di riferimento per il circuito di controllo, mentre una versione ad alta tensione è necessaria per la catena di regolatori lineari presenti nel controllore. Inoltre, sono stati progettati anche due circuiti di riferimento di corrente ad alta e bassa tensione. Poiché i circuiti devono resistere a condizioni di radiazione estreme, è fondamentale intervenire giá in fase di progettazione. Pertanto, sono stati sviluppati diversi modelli per prevedere il comportamento dei transistor in risposta alle radiazioni, consentendo la simulazione dei circuiti irraggiati.

Résumé

Le CERN, l'Organisation européenne pour la recherche nucléaire, est à la pointe de la recherche en physique des particules. Ici, grâce à la présence d'accélérateurs de particules (principalement le Large Hadron Collider (LHC)) et de détecteurs, les scientifiques ne cessent d'approfondir la connaissance de l'univers. La mise à niveau du LHC (HL-LHC) entraînera une augmentation de la quantité de données collectées par les détecteurs, ce qui nécessitera une plus grande consommation d'énergie dans les circuits de front-end des détecteurs. Dans ce contexte, la fourniture efficace de différentes tensions d'alimentation aux circuits de front-end tout en minimisant la consommation d'énergie est une tâche difficile. Actuellement, le schéma de distribution de l'énergie dans les détecteurs du HL-LHC est basé sur différents stades de convertisseurs DC-DC placés à proximité du point de collision, constamment soumis à des niveaux élevés de radiation. Dans cet environnement innovant, ce projet de thése de master contribue à l'avancement des circuits électroniques tolérants aux radiations utilisés dans les convertisseurs du CERN. Le coeur de ce projet est le développement de deux circuits de référence de tension résistants aux radiations. Ces blocs sont essentiels pour fournir une tension de référence aux autres circuits du contrôleur d'un convertisseur abaisseur de tension 48 V $\rightarrow$ 5 V. En particulier, un circuit basse tension est conçu pour générer la tension de référence pour le circuit de contrôle et une version haute tension nécessaire pour la chaîne de régulateurs linéaires présente dans le circuit de contrôle. En outre, deux circuits de référence de courant haute tension et basse tension sont conçus. Comme les circuits doivent résister à des conditions de rayonnement extrêmes, il est crucial d'intervenir dés la phase de conception. Ainsi, différents modèles sont développés pour prévoir le comportement des transistors en réponse au rayonnement, ce qui permet de simuler rapidement les circuits irradiés.

Acknowledgements

At the end of this long journey, I extend my deepest gratitude to my supervisor, Dr. Giacomo Ripamonti, whose constant support and guidance were vital throughout my thesis internship. I owe special thanks also to Dr. Stefano Michelis, who played an essential role alongside Giacomo in guiding and mentoring me. I would also like to acknowledge Professor Koukab and Professor Piccinini for their contribution.

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My friends in Belluno, my hometown, hold a special place in my heart. Among them, I want to mention Anna, whose strong friendship remains dear to me, despite spending less time there now.

Last but certainly not least, heartfelt thanks go to my family. Their encouragement has been a constant source of motivation, continuously urging me to strive for the best and never lose sight of my goals.

To everyone mentioned, thank you for being integral parts of my university journey and significant presences in my life.

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Acronyms

ALICE A Large Ion Collider Experiment. 1

ASIC Application-Specific Integrated Circuit. 2, 3

ATLAS A Toroidal LHC ApparatuS. 2

BGR BandGap Reference. vi, vii, 5, 29, 37, 45, 48, 49, 56–62, 64, 65, 67, 68

CERN Conseil Européen pour la Recherche Nucléaire. iii, 1–4

CLM Channel Length Modulation. 31

CMS Compact Muon Solenoid. 2

CTAT Complementary To Absolute Temperature. 47, 48, 56

DD Displacement Damage. v, 12

ELT Enclosed Layout Transistor. v, 17, 26, 27

FOXFET Field OXide FET. 9, 18, 19, 69

HEMT High Electron Mobility Transistors. 3

HL-LHC High-Luminosity Large Hadron Collide. i, 2, 3

LDD Lightly Doped Drain/Source. 8

LDMOS Laterally Diffused MOS. iii, v, 11, 15, 17, 20, 36, 37, 39, 63, 69

LEP Large Electron-Positron. 1

LET Linear Energy Transfer. 21, 22

LF Low Frequency. 50

LHC Large Hadron Collider. i, 1–3, 69

LHCb Large Hadron Collider beauty. 1

MBU Multi-Bit Upset. 13

OPAMP OPerational AMPlifier. iv, vi, 29, 34, 37, 47, 49, 51–55, 57, 59–61, 65, 66, 70

OTA Operational Transconductance Amplifier. iv, 49, 50, 52, 53, 70

PDK Process Design Kit. 15

PSR Power Supply Rejection. iv–vi, 31, 33, 34, 40, 41, 48, 58, 61, 65

PTAT Proportional To Absolute Temperature. 47, 48, 56

RINCE Radiation Induced Narrow Channel Effect. 10, 15

RISCE Radiation Induced Short Channel Effect. 10, 16

SEBO Single Event Burn Out. 14

SEE Single Event Effects. iii–vi, 13, 14, 20–25, 27, 48, 57, 59, 73–76

SEGR Single Event Gate Rupture. 14

SEL Single Event Latchup. 13, 27

SET Single Event Transient. 13

SEU Single Event Upset. 13

SOA Safe Operating Area. 36, 39, 63

STI Shallow Trench Isolation. 8–10, 15, 26, 27, 69

TC Temperature Coefficient. 32, 46–48, 56, 70

TID Total Ionizing Dose. iii, vii, 7, 14–20, 35, 42, 60, 65, 66, 69, 70

Chapter 1

Introduction

1.1 CERN

This master thesis project has been carried out at the MicroElectronics section of the Electronic System for Experiments group of CERN. CERN, short for "Conseil Européen pour la Recherche Nucléaire", is today the forefront organization for particle physics research. It was established in 1954 in Geneva, Switzerland as a way to foster nuclear research in Europe. From the beginning the focus was on the development of particle accelerators to deepen the knowledge on the properties of matter. Its first accelerators were the Synchrocyclotron and the Proton Synchtotron, which became operational respectively in 1957 and in 1959. In 1983, the construction of the Large Electron-Positron (LEP) was approved, and after some years it evolved into the most powerful accelerator of that time, making electrons and positrons collide at a maximum energy of 209 GeV in 2000. The LEP was then replaced by new Large Hadron Collider (LHC), which became operational in 2008. It extends for 27 kilometers in an underground tunnel at the French-Swiss border and it is still the largest particle accelerator in the world. Inside the accelerator there are two beams of very high energy particles travelling close to the speed of light. The LHC is the last element of a chain of other systems that accelerate the particles at higher and higher energy. The two beams flow in opposite directions and they are made collide in four different sites (Figure 1.1), where particle detectors capture the products of the collisions:

- A Large Ion Collider Experiment (ALICE), which aims to recreate the same phase of matter as after the Big Bang, the quark-gluon plasma, to investigate fundamental properties of matter.

- LHCb, whose main goal is deepening the knowledge on the differences between matter and antimatter.

- ATLAS (A Toroidal LHC ApparatuS), tasked with studying different physics branches like the Higgs boson, extra dimensions, dark matter.
- CMS (Compact Muon Solenoid), with the same research goals as ATLAS but using different equipments.

Thanks to the collaboration between the last two experiments in the analysis of the proton-proton collisions, in 2012 the discovery of the Higgs boson was announced, which can be considered a milestone for the research on particle physics and cosmology.

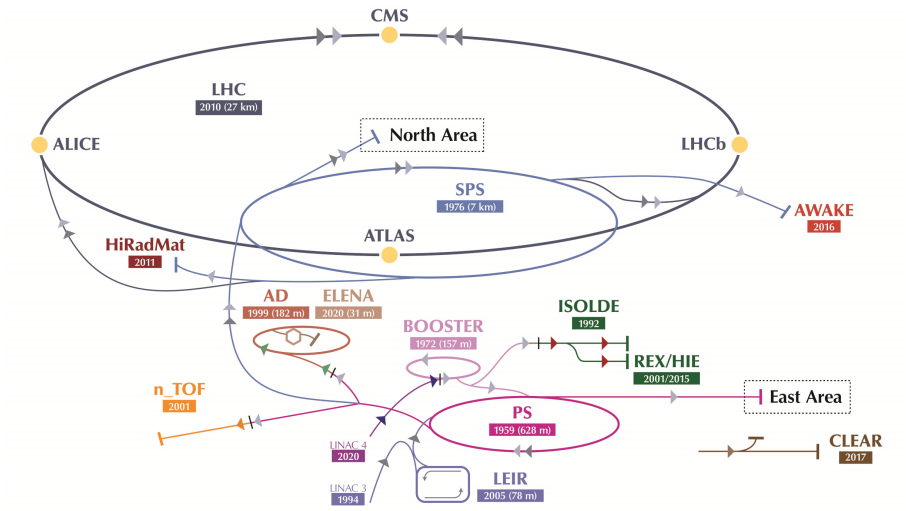


Figure 1.1: CERN's accelerators complex with all experiments sites.

However, these are not the only experiments in the complex, there are several other experimental sites for experiments with lower energy beams. In the next years, it is foreseen to increase the performance of the LHC with the so-called High-Luminosity Large Hadron Collide (HL-LHC) project. Luminosity is used as an indicator proportional to the number of collisions in a given amount of time. An increase of this performance indicator leads to a larger amount of data to be analyzed. The project should be operational by 2029, enabling scientists to discover particles and phenomena still unreachable with current technology [2].

1.2 Power distribution at CERN and DCDC converters

This work is part of the DC-DC project, which focuses on the development of DC-DC converters based on ASICs (Application-Specific Integrated Circuits) for

application in the LHC and HL-LHC detectors [3].
Providing different supply voltages to the front-end circuits in the detectors keeping low power consumption is not straightforward. Indeed, since they are located close to the collision sites and the power supplies are placed at a distance of approximately 100 m from them, it is important to keep the supply voltage as high as possible until the very end point of the power distribution network: this allows to have a lower current in the cables and consequently also a lower power dissipation ($P \propto RI^2$), or conversely to reduce the size of the cables. Considering the increased power consumption of the front-end circuits that will be employed in the HL-LHC detectors and the material minimization constraints (the minimum amount of material must be used in the detectors to avoid affecting their physics performance), it is mandatory to introduce on-detector DC-DC converters. They step down the voltage in close proximity to the front-end ASICs, allowing the employment of thin cables without compromising the system efficiency. In particular, different stages of DC-to-DC conversion are used to create the different voltage domains required by the front-end circuits from a single line. As the converters are placed close to the collision points, they are subject to high levels of radiation (up to hundreds of Mrad of total ionizing dose, see subsection 2.1.1). This is why common electronics cannot be used in this context and specific radiation-hard ASICs are needed, which are designed at CERN for the harsh environment application.

Research and development on new power distribution systems are in progress, in particular for the upgrades of the LHC detectors (HL-LHC). Currently, the adoption of GaN power devices is being explored. GaN devices are particularly interesting for application in DC-DC converters because they are High Electron Mobility Transistors (HEMT) and thus they present a higher electric field strength compared to silicon devices. Consequently, for the same dimensions GaN transistors can have a significantly lower value of R_{ON}. Moreover, they are characterized by very fast switching property thanks to their low input capacitance, which leads to a lower power dissipation [4]. In addition, GaN devices show increased radiation tolerance compared to their silicon counterparts. As the radiation hardness of silicon devices decreases for a higher voltage rating, it is very challenging to design a DC-DC converter with an input voltage larger than 12 V using such devices that is compatible with application in the HL-LHC detector. With GaN devices, it is instead possible to significantly increase the input voltage of the converter (thus further reducing the power dissipation in the cables and/or the cable size), while maintaining a high tolerance to radiation. Therefore, 48 V-input DC-DC converters using GaN switches are currently being developed at CERN. They use commercial GaN devices, together with a radiation-hard silicon controller developed at CERN. The chosen topology for the converters (*buck*) is introduced in the following Section, together with a more detailed explanation of the architecture of the radiation-tolerant GaN-based converter.

1.2.1 Buck converter

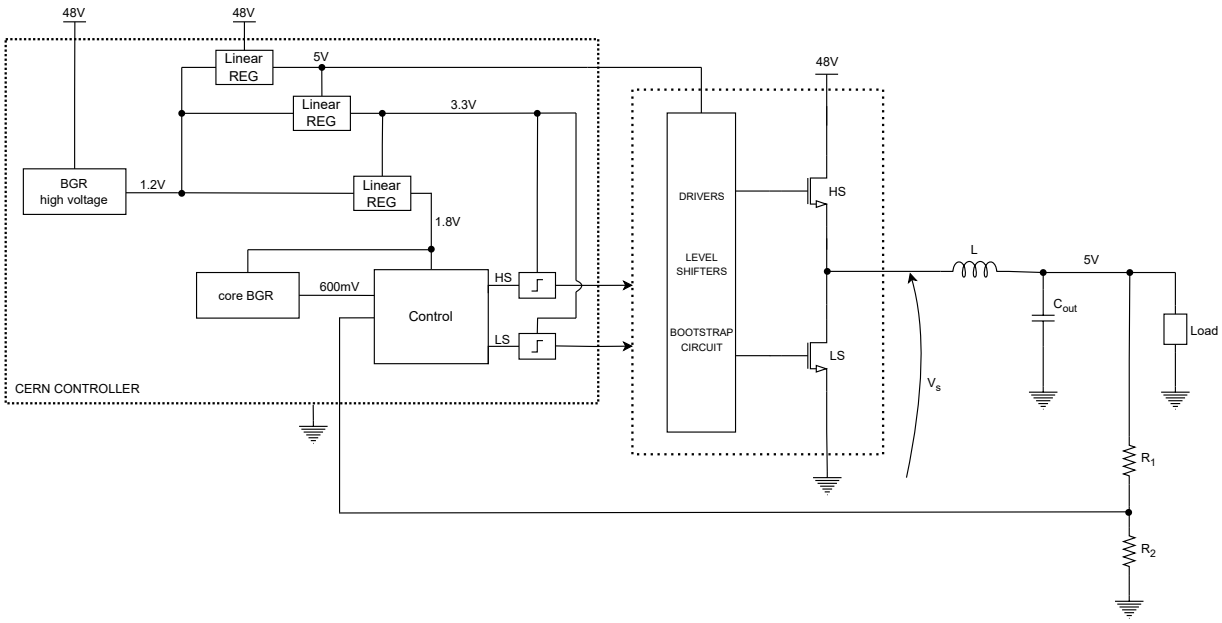


Figure 1.2: Buck converter schematic. Besides the core stage composed of the switches and the L-C filter, also the CERN controller block diagram is represented.

Figure 1.2 represents the schematic of a buck converter. It is a type of DC-DC converter which takes a defined input voltage and steps it down to a lower voltage. It is a switching circuit, with two switches that work in phase opposition. When the HS switch is ON, V_s is equal to the input voltage of the converter (in this case 48 V), whereas when the LS switch is in the ON state, V_s is equal to zero. HS and LS are switched periodically with period T and a specified duty cycle D, defined by the amount of time the HS switch is in the ON state compared to the total period. From the Fourier analysis it is known that the DC component of a periodic waveform is equal to its average value, hence:

$$V_{s,DC} = \frac{1}{T}\int_0^T Vs(t)dt = DV_{in}. \tag{1.1}$$

To remove the harmonic components of the signal, a L-C low pass filter is introduced, with a corner frequency sufficiently lower than the switching frequency. [5] As for the two switches, a commercial GaN component is used. It features internal level shifters, a bootstrap circuit and gate drivers that control the GaN FETs. This block is supplied by 5 V and it accepts at its inputs 3.3 V or 5 V logic levels.
To regulate the output voltage, a control circuit is implemented. It has the task of adjusting the duty cycle D depending on the value of the output voltage, which can change because of variations on the input voltage or on the load. A scaled version of

the output voltage is compared to a given reference and the duty cycle is adjusted accordingly. This control block belongs to the controller circuit for the GaN component, which is being designed by the DC-DC group at CERN using a 0.18 µm high-voltage CMOS technology. The main control blocks are supplied by 1.8 V, therefore two level shifters are needed to convert the digital voltage level of the HS and LS signals from 1.8 V to 3.3 V. It was decided to supply the Control block at 1.8 V because in this way both the circuits inside the block and the bandgap reference employed for its reference voltage can be designed with low-voltage transistors (1.8 V N/PMOS). These devices are featured with high radiation hardness compared to high-voltage transistors. The different voltage domains needed to supply the circuits are generated through a chain of linear regulators that convert their supply voltage to a lower output voltage. In particular, three linear regulators are needed:

1. 48 V $\rightarrow$ 5 V, which generates the supply voltage for the drivers component inside the GaN component.
2. 5 V $\rightarrow$ 3.3 V, which generates the supply voltage for the two level shifters and output drivers of the HS/LS signals.
3. 3.3 V $\rightarrow$ 1.8 V, which generates the supply voltage for the control block.

Two radiation-hard voltage reference circuits are then essential to provide the reference voltage to the linear regulators and to the control block. The development of these circuits is the purpose of this project.

1.3 Project overview

This project deals with the design of two different BandGap Reference (BGR) circuits in a 0.18 µm high-voltage CMOS technology. The first is a BGR circuit with 1.8 V supply voltage and 600 mV output reference voltage, whereas the second one is a high-voltage circuit that must work with a supply voltage between 12 V and 55 V and provides a reference of 1.2 V. The output of the first circuit is used as a reference to determine the output voltage of the DC-DC converter, and it is therefore designed using exclusively 1.8 V-rated devices: the higher radiation-tolerance of these transistors compared to high-voltage devices helps in achieving an accurate reference voltage even at ultra-high doses of radiation, leading to a stabler output voltage of the converter. The second BGR circuit is instead used to provide the reference to the linear regulators presented in the previous Section. Together with the main schematic of the BGR circuit, also the fundamental blocks necessary to its operation were designed i.e. the operational amplifier and the current reference circuits (beta multiplier).

Chapter 3 deals with the design of both the low- and high-voltage versions of the current reference circuits. On the other hand, chapter 4 focuses on the design of both low- and high-voltage versions of the voltage reference circuits. Both chapters also include different simulation results to assess the performance of the circuits. Particular attention is paid on the robustness of the circuit to radiation effects. The most relevant effects on transistors due to the high levels of radiation are described in chapter 2, together with the main techniques adopted to strengthen the electronic circuits, from both a circuital and a physical point of view. Some models of the transistors are developed in this work to simulate the circuits also in conditions similar to the actual radiation environment, allowing to harden the circuit already in the design phase.

Chapter 2

Radiation influence on transistors

As mentioned in chapter 1, the designed DC-DC converter will be situated in a region highly exposed to radiation resulting from particle collisions. For this reason, it is indispensable to know possible effects of radiations on the utilized electronics to properly study different techniques to harden the circuitry. This chapter presents different types of radiation effects that are relevant in electronics, hence that can modify the normal behavior of the device. Along with a theoretical overview on radiation effects [1] [6], this chapter also presents the different hardening techniques. A particular focus is put on the work carried out during this Master thesis project: the development of radiation models for Total Ionizing Dose (TID) effects and of a Verilog-A cell to automatize the injection of Single Events.

2.1 Radiation effects on matter and MOS devices

The way radiation influences matter's properties involves the presence of different incident particles, mainly photons, neutrons (neutral particles), protons, heavy ions and electrons (charged particles). The main effects can be grouped into three categories: TID effects, displacement damage, single event effects.

2.1.1 Total Ionizing Dose effects

Ionization refers to the process in which a high energy incident particle collides with an atom and transfers enough energy to remove one or more electrons. The result is the presence of an ionized atom and free electrons (electron-hole pairs). The cumulative ionization effects are expressed as TID, which represents the total energy released per unit of mass during the interaction between radiation and the material. While the standard SI unit for the absorbed total dose is the gray (Gy), where 1 Gy = 1 Jkg^{-1}, the rad, with 1 rad = 0.01 Gy, is still commonly used. In principle, MOS devices are more significantly affected by ionizing effects. In particular, the

incident particles cause the generation of electron-hole (e-h) pairs in the device. In SiO_2, the e-h pair creation energy is around 17eV (X/γ rays) and it is the only region where e-h pairs do not quickly recombine, as its insulating properties result in significantly different mobilities for electrons and holes: electrons drift rapidly, while holes migrate towards the gate or the silicon-oxide interface (whether the device is an NMOS or a PMOS). Consequently, some positive charges accumulate in the gate oxide due to their entrapment in defects. At the same time, holes may bind to hydrogen in the oxide creating ions H^+ that tend to de-passivate the interface traps. At the end, interface traps store negative charge for NMOS and positive charge for PMOS. This latter process occurs at a slower rate compared to the charge accumulation in the oxide.
In CMOS technology, transistors include not only the gate oxide but also other thicker and lower-quality oxides. These oxides are more affected by defects, which can trap holes. As shown in Figure 2.1, there are also spacers oxides, to create Lightly Doped Drain/Source (LDD) regions, and Shallow Trench Isolation (STI) oxides, to isolate from the nearby transistors.

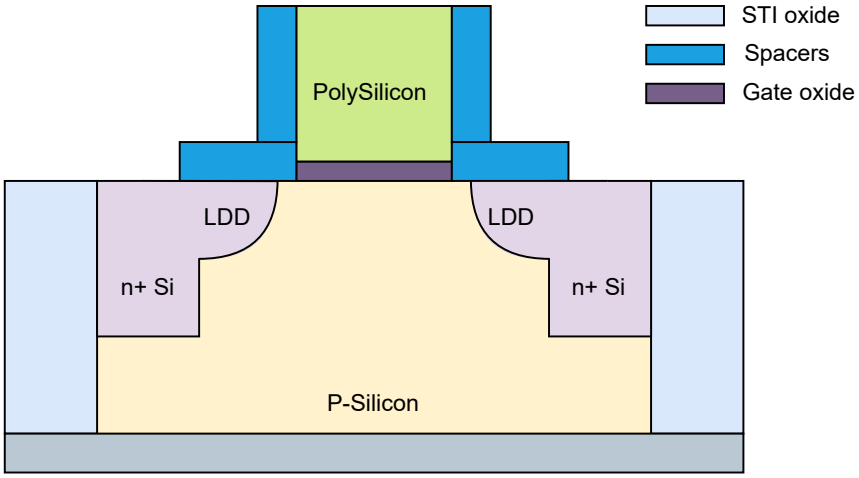


Figure 2.1: Cross section of an NMOS transistor in CMOS technology. All the oxides employed in the fabrication are depicted: the gate oxide, the spacers and the STIs. Adapted from [6].

The effect of these phenomena is a variation on several electrical parameters of the transistors.

Voltage threshold shift due to gate oxide traps

The holes trapped in the oxide alter the electric field distribution across the MOSFET channel. Consequently, the shift in the electric field modifies the threshold voltage. For a PMOS device, the positive charge trapped in the oxide repulses holes

in the channel, hence the threshold voltage increases in absolute value. In NMOS devices instead the reasoning is opposite and the threshold voltage decreases.
As regards the charges at the $SiO_2 - Si$ interface, in NMOS transistors radiation exposure typically results in a net negative charge accumulation, causing the threshold voltage to shift positively. In PMOS devices, the opposite occurs, with a net positive charge accumulation leading to a negative shift: both PMOS and NMOS experience in this case an increase of the threshold in absolute value [1].

Leakage current increase

Leakage current I_{OFF} is the current that flows between source and drain of a transistor even when it should be in the OFF state, and in particular it is defined as the drain current of a FET when its V_{GS} is equal to 0 V. Leakage current can have significant implications for circuit performance and power consumption (static power consumption P_S is proportional to I_{OFF}). Irradiated NMOS transistors experience an increase of leakage current that can be explained with mainly two effects:

1. The main contribution is given by **STI parasitic paths**. As it can be seen in Figure 2.2, the STI oxide sorrounding the device entraps always positive charges. In the case of an NMOS transistor, electrons are attracted from the bulk and an electric field is created capable of inverting lateral channels. This effect can be modeled with the presence of two parasitic transistors (the so-called Field OXide FET (FOXFET)) in parallel to the main one. This

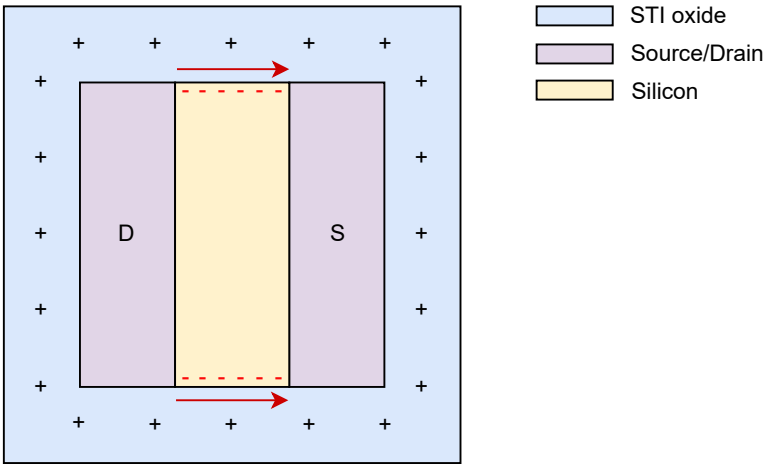


Figure 2.2: Parasitic paths for the leakage current due to the presence of the STI oxide in an NMOS transistor.

effect can be seen only in NMOS transistors, since electrons are the majority

carriers. In PMOS, where holes are the majority carriers the effect of electrons accumulation near in the lateral channels is less pronounced and the leakage current increase is not significant.

2. There is also a contribution that comes from the decrease of the subthreshold slope and the threshold voltage shift induced by irradiation. However, this is not the dominant one compared to the parasitic currents influence.

I_{ON} degradation

The I_{ON} of a transistor can be defined as the drain current when the transistor is in saturation and with maximum V_{GS}. Both in NMOS and PMOS transistors a variation of I_{ON} is observed as a radiation response. The degradation is higher in PMOS devices, because the charge trapped in the oxide and at the interface have the same positive sign. In NMOS they have instead opposite sign, thus there is a compensation between the two effects. This degradation is found to be strongly dependent on the channel width and this effect was called **Radiation Induced Narrow Channel Effect (RINCE)** [7]. This dependence can be explained by the fact that the amount of charge trapped in the STI oxide is always the same, therefore the effect on the sides of the channel does not change, regardless the channel width. However, transistors with lower channel widths experience, in percentage, a more relevant effect.
Channel width is not the only parameter which influences the I_{ON} degradation. Some measurements were recently performed on transistors with widths large enough to no longer be relevant and different lengths [8]. The result is that shorter transistor are more affected by radiation induced degradation. This phenomenon was first observed by Faccio et al. in [9] and it was called **Radiation Induced Short Channel Effect (RISCE)**. It is related to the presence of the spacers oxides, that as the other oxides can entrap positive charges and release hydrogen ions. Consequently, the series resistance increases leading to a decrease in transconductance. When the channel length is reduced, the current I_{DS} rises causing an increase in the voltage that drops over the resistance.

2.1.2 Displacement Damage

Displacement damage is another phenomenon which derives from impinging high energy particles. If the particles have sufficient energy they can break the atomic bonds, displacing atoms from their original position in the lattice. This creates structural defects in the material and can alter the doping level. In general MOS transistor are not very affected by displacement damage, whereas it can be significant for high-voltage CMOS transistors, where low-doped regions are used [10], as presented in subsection 2.1.3.

2.1.3 Laterally Diffused MOS (LDMOS)

Particular transistors are employed for high-voltage applications, capable of withstanding larger values of V_{DS} compared to conventional MOSFETs. The most common device, employed also in the design of the high-voltage blocks in this project, is the LDMOS, used both in power and RF applications. A general schematic of an n-channel device is depicted in Figure 2.3.

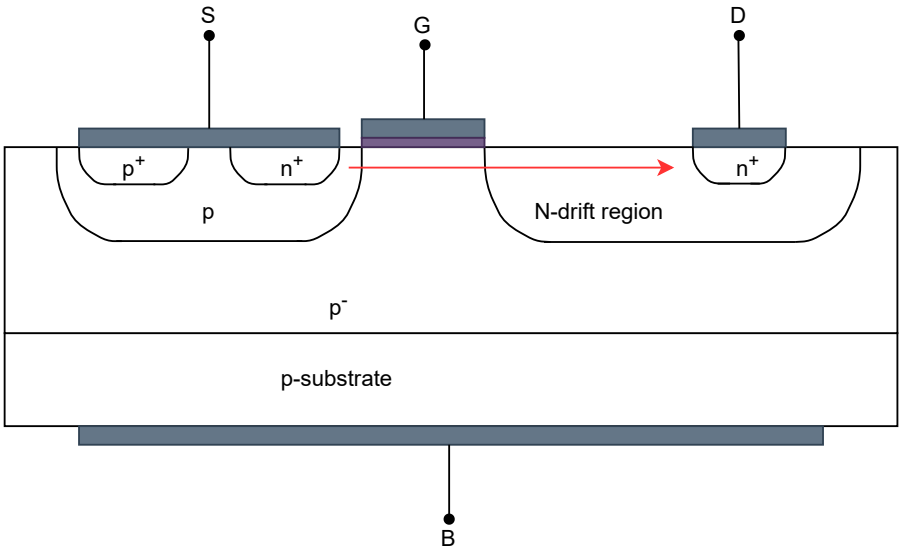


Figure 2.3: Schematic drawing of an N-LDMOS transistor.

The N-LDMOS is built over a p-type silicon substrate, over which a p-epitaxial layer with a lower doping concentration is grown. The critical component of its structure is the presence of an N-drift region with a lower doping concentration compared to the source and drain regions. It spreads out the electric field across a larger area, preventing the formation of localized high electric field areas that could damage the transistor. In this way this type of transistors can withstand high voltage levels.

LDMOS devices generally feature a thickness of the gate oxide that is not as low as that of CMOS low voltage transistors. Since they are characterized by these thicker oxides, they can experience a large shift of the V_{th} and a relevant increase of leakage current.

LDMOS of both n-type and p-type are strongly affected by displacement damage than conventional MOSFETs, due to the presence of regions with lower doping levels that can be more easily altered by nuclear displacement. This causes a distorsion on the output characteristic that is more evident in N-LDMOS transistors (see Figure 2.4).

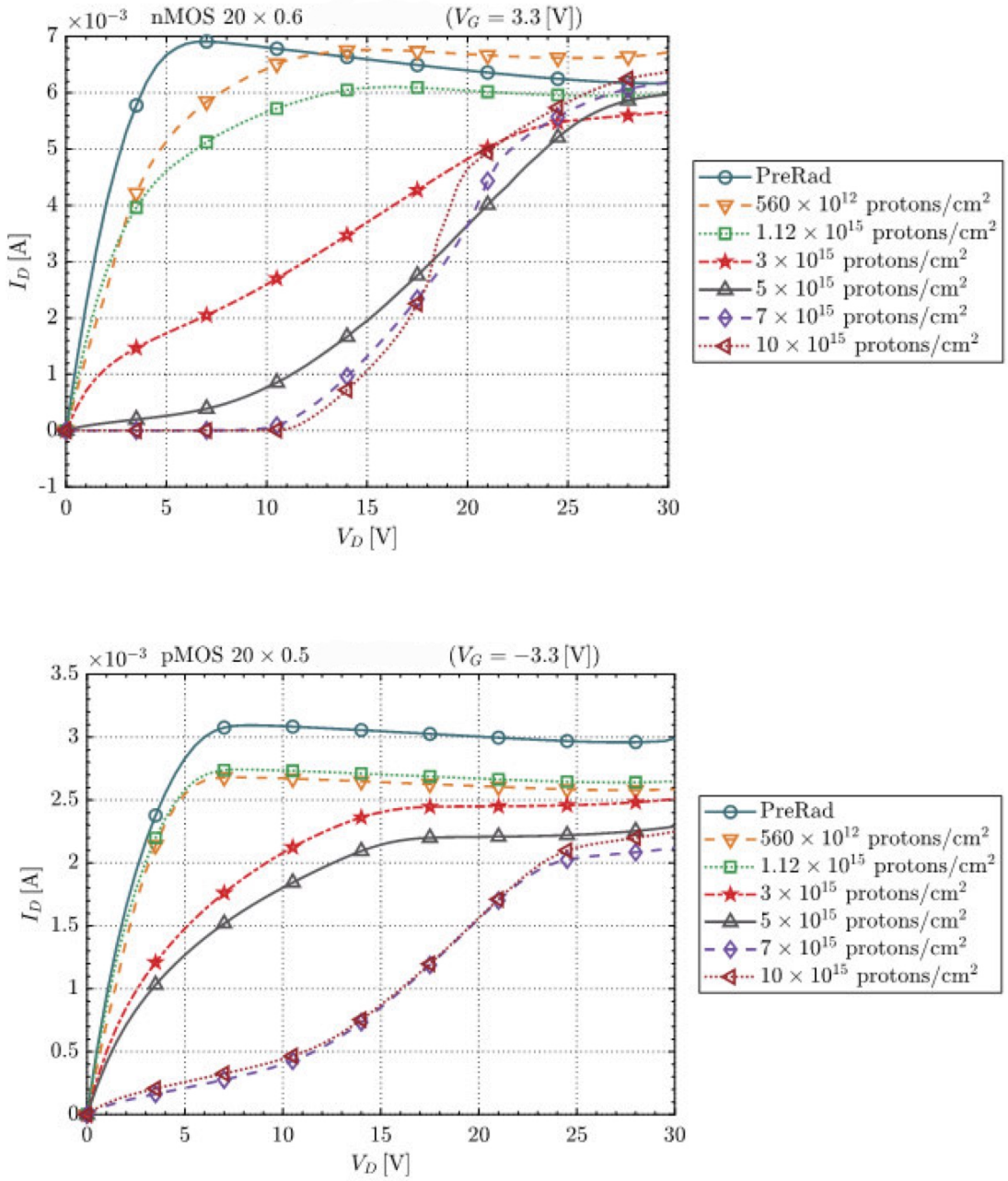


Figure 2.4: N-type and P-type LDMOS characteristics at different proton irradiation levels to see DD distorsion effects.

2.1.4 Single Event Effects (SEE)

Single Event Effects are caused by a *single* high-energy particle, such as a proton or a heavy ion, which hits a transistor or a similar electronic device altering its normal behavior. They can be divided into two main categories based on the reversibility of their effect. These two categories are presented below, along with the most relevant errors belonging to each.

1. Non-destructive SEE:
    - *Single Event Upset (SEU)*: change in the value of a bit stored in a memory cell due to a particle strike. This type of error concerns more digital circuits and it can be solved writing again the correct information. Usually the main technique to prevent SEU is the triplication, which consists of the parallel operation of three copies of the same component. The outputs of these three modules are sent to a voting block which selects the output usually with a majority voting criterion. Nevertheless, this type of solution does not preserve from the simultaneous upset of more than one bit (*Multi-Bit Upset (MBU)*). However, it was observed that a larger physical distance among the modules significantly reduces the failure probability.
    - *Single Event Transient (SET)*: the high energy particle causes a transient disturbance in voltage and current levels in both analog and digital circuits, provoking a deviation from normal operation.
2. Destructive SEE
    - *Single Event Latchup (SEL)*: this is a typical CMOS effect, where a parasitic structure can be formed causing high current flow leading to a damage of the device. In particular, a PNPN structure called thyristor (Figure 2.5) can be switched on, allowing the flow of current from V_{dd} to V_{ss}.

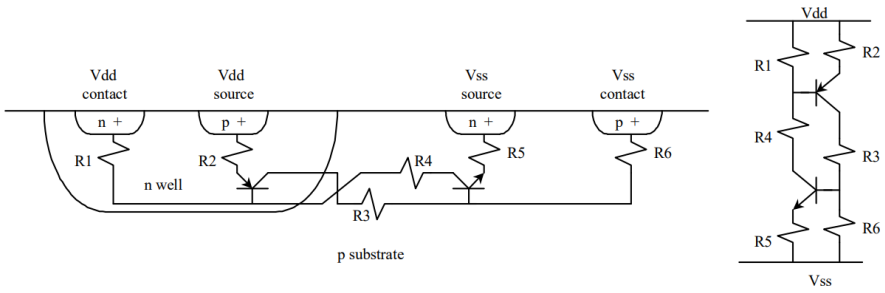


Figure 2.5: Schematic drawing of the thyristor in n-type CMOS technology [1].

- *Single Event Gate Rupture (SEGR)*: this phenomenon occurs when an ionizing particle causes the destruction of the gate oxide. Typically, it happens under conditions of high electric field on the gate oxide, as in power MOSFET devices.
- *Single Event Burn Out (SEBO)*: this effect is seen in power MOSFET and bipolar transistors because they include the presence of a parasitic bipolar transistor. A ionizing particle may activate the bipolar transistor, which starts to conduct a certain amount of current. This can lead to a significant power dissipation, possibly causing the melting of the MOS transistor.

2.2 Circuits radiation-hardness

There are different techniques to make circuits radiation-hard, acting at different levels. In particular, it is possible to intervene at the physical, circuit or process level.

- *Process* hardening techniques: in principle the process flow for the fabrication of the transistors can be customized to make the device rad-hard. For example, some relevant parameters such as the thickness of the gate oxide could be modified. Nevertheless, typically commercial CMOS technologies are used, otherwise customized fabrication would be too expensive.
- *Circuit* hardening techniques: it is possible to make some modifications on the topology of the circuit to make it more radiation-tolerant. The simulation of radiation effects on circuits is important to guide the design choices to achieve the target radiation hardness. In order to make such simulations possible in the used 0.18 μm HV-CMOS technology, TID effects and SEE on the employed transistors have been modeled in this thesis work. As for the TID effects, the goal is to model the characteristics of the circuits after being irradiated. Then, some additional corners are introduced to simulate the circuit as if it were exposed to radiation. In the SEE case instead, a tool to automatize the injection of single events is developed.
- *Layout* hardening techniques: it is also possible to adopt some layout strategies to improve circuit hardness, in particular to reduce leakage current and minimize the impact of single events.

2.2.1 Modeling of the TID effects

In order to simulate the circuits under radiation conditions, some radiation models for the transistors are developed in this work. This allows to account for TID

effects on transistors already in the design phase. In this project, TID models are developed for low-voltage transistors (1.8 V-rated transistors used in the low-voltage blocks). Some considerations to correctly model the leakage current for high-voltage transistors (LDMOS) are also presented. As already mentioned, low-voltage transistors are less affected by radiation compared to LDMOS because of the different technology characteristics.
The electrical parameters of transistors are specified in the model files included in the Process Design Kit (PDK) of the technology. In particular, BSIM4 MOSFET model is used to model transistors. It is a physics-based model featuring accurate predictions of MOSFET behavior also at sub-micron dimensions. Each transistor model is divided into different sections according to the values of its length and width. The general approach for the radiation modeling is modifying some electrical parameters in the model, according to physical effects, trying to fit the $I_D - V_D$ and $I_D - V_G$ characteristics measured after irradiation. A TID of 200Mrad is considered for all the models, as it is the target value of TID for the application.

1.8 V **transistors modeling**

Concerning 1.8 V NMOS and PMOS transistors, three parameters are adjusted: the threshold voltage V_{th}, the effective width W_{eff} and the effective length L_{eff}. Threshold voltage shift can be physically explained by the effect introduced in Section 2.1.1.1. Table 2.1 summarizes the threshold voltage shifts for both transistors types, according to their dimensions. It can be noticed that for PMOS devices the threshold shift tends to decrease increasing the width value. This can be justified by the RINCE effect, which states that narrower channels transistors are more affected by radiation-induced degradation of their I_{on}. All NMOS transistors models instead present the same value of threshold shift, regardless their dimensions. This is probably because RINCE effect is experimentally significantly more evident in PMOS devices. Also the models of hvt (high V_{th}) and lvt (low V_{th}) devices are modified, since some experimental data are available. However, they will not be used for the scope of this project. The voltage threshold shift is not reported in the table, but for PMOS hvt transistors is very similar to the values reported for standard-V_{th} PMOS transistors. As regards NMOS hvt and lvt transistors, the threshold shift value is respectively of 0.05 V and 0.02 V.

RINCE effect can be seen also as a reduction of the effective width of a transistor. Indeed, charges accumulated in the STI oxide prevent the channel inversion in those areas, reducing W_{eff} of the channel. A ΔW parameter is subtracted from the value of the effective width reported in the model. Since the ΔW is approximately always the same regardless the width and length values of the transistors, narrower transistors will be more impacted by this change. NMOS transistors do not seem to be significantly affected by this effect, thus their ΔW is kept to zero.

		$0 < L < 0.42\,\mu m$	$0.42\,\mu m < L < 10\,\mu m$	$10\,\mu m < L < 100\,\mu m$
$0 < W < 0.3\,\mu m$	PMOS	0.2 V	0.25 V	0.25 V
	NMOS	0.05 V	0.05 V	0.05 V
$0.3\,\mu m < W < 1\,\mu m$	PMOS	0.2 V	0.2 V	0.2 V
	NMOS	0.05 V	0.05 V	0.05 V
$1\,\mu m < W < 10\,\mu m$	PMOS	0.17 V	0.17 V	0.17 V
	NMOS	0.05 V	0.05 V	0.05 V
$10\,\mu m < W < 100\,\mu m$	PMOS	0.17 V	0.17 V	0.17 V
	NMOS	0.05 V	0.05 V	0.05 V

Table 2.1: Threshold voltage shift due to TID radiation effects (200Mrad) on 1.8 V N/PMOS transistors, divided into different sections according to their values of width W and length L.

Analogously, RISCE effect can be seen as an increase of the effective length. Indeed, it leads to an increase of the channel series resistance which corresponds to a longer effective channel length. Also in this case, the longer the channel is, the less affected the transistor is.

W_{eff} and L_{eff} parameters are reported in the BSIM4 model [11] as:

$$W_{eff} = \frac{W_{drawn}}{NF} + XW - 2dW, \tag{2.1a}$$

$$L_{eff} = L_{drawn} + XL - 2dL, \tag{2.1b}$$

with NF number of fingers, XL and XW parameters that account for the offset due to mask and etching inaccuracies. dW and dL represent instead statistical variations. With the introduction of the new radiation parameters, Equation 2.1 becomes:

$$W_{eff} = \frac{W_{drawn}}{NF} + XW - 2dW - \Delta W, \tag{2.2a}$$

$$L_{eff} = L_{drawn} + XL - 2dL + \Delta L. \tag{2.2b}$$

Table 2.2 summarizes the values of ΔL and ΔW parameters introduced for N/PMOS transistors.

Figure 2.6 shows an example of the comparison between the measured PMOS $I_D - V_G$ and $I_D - V_D$ characteristics and the simulated ones with the modified transistor models. These measurement data specifically refer to a PMOS transistor with $W = 4\,\mu m$ and $L = 1\,\mu m$. The model accurately fits the experimental data, in both Figure 2.6a and Figure 2.6b. There is only a leakage component that is not included in the model because it can be considered negligible (less then 10^{-10} A).

	NMOS	NMOS hvt	NMOS lvt	PMOS	PMOS hvt
ΔW [nm]	0	0	0	30	30
ΔL [nm]	0	30	30	25-35	25-35

Table 2.2: Effective width and effective length shifts due to TID radiation effects (200Mrad) on 1.8 V N/PMOS, hvt/lvt transistors.

Figure 2.7 shows instead an example concerning NMOS transistors, with minimum width and length of 0.18 µm. In this case also the pre-irradiation simulated characteristics is plotted since they already slightly differ from the measured ones. However, also in this case the result is quite accurate. Measurements were performed directly on ELT NMOS that, as will be explained in subsection 2.2.3, do not feature the leakage problem. Since all the 1.8 V NMOS transistors used in this project are laid out with this configuration, the radiation models are built according to these leakage-free experimental data.

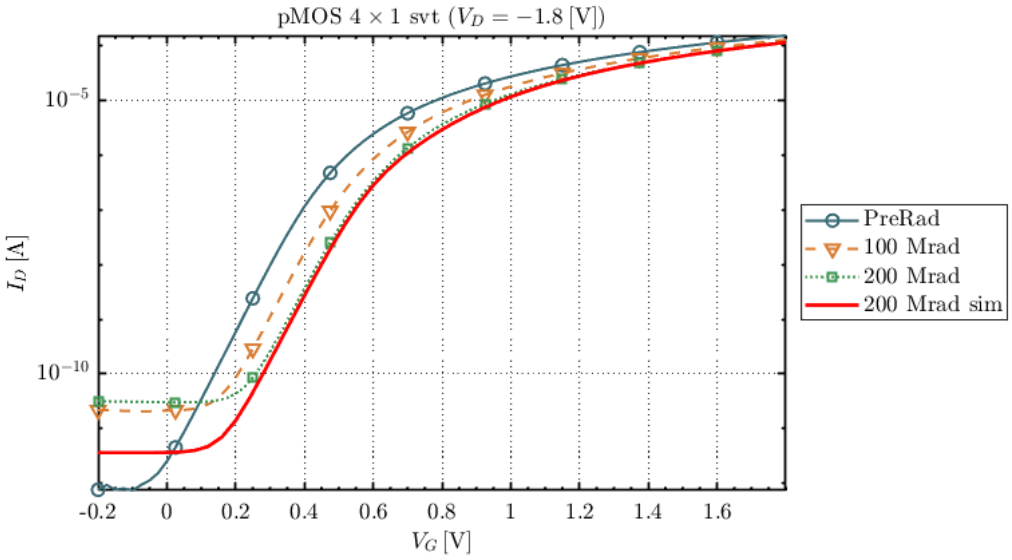
LDMOS modeling

The modeling of LDMOS transistors is challenging since they are consistently more affected by radiation effects compared to 1.8 V-rated transistors. All available experimental results were obtained irradiating transistors with fixed bias conditions for $|V_{GS,bias}|$ and $|V_{DS,bias}|$. Then, after reaching a certain amount of TID, the electrical characteristics $I_D - V_G$ and $I_D - V_D$ of the transistors were measured.
The fitting of the experimental curves modifying model parameters related to displacement damage and TID effects are not carried out in this project, and they have been the subject of a different Master thesis project. The following paragraphs present the considerations used to model LDMOS devices.

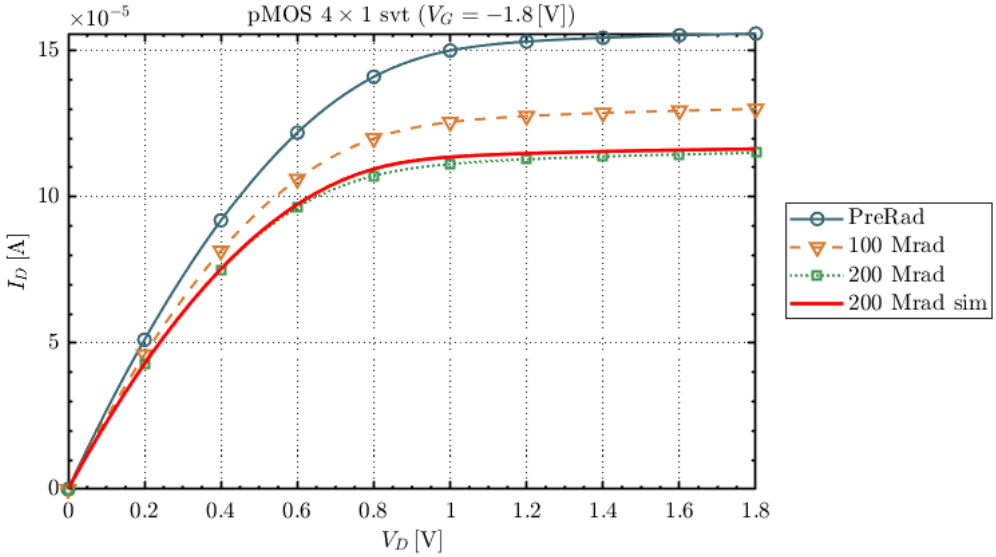
The TID modeling includes a change in the carriers mobility to model the I_{ON} degradation and a shift of the threshold voltage. The latter is significantly higher than the 1.8 V-rated transistors in the case of p-type devices (around 0.7 V). This is due to the presence of thicker gate oxides in LDMOS structures. Conversely, for the n-type counterpart, there is a compensation mechanism between charges in the gate oxide and interface traps, which leads to a less significant impact on the threshold voltage shift.

It was experimentally verified that the radiation-induced leakage current in n-type devices is strongly affected by the value of $V_{GS,bias}$ used during the irradiation (see Figure 2.8).

This effect is challenging to model, as a different value of leakage current should be introduced in the simulations according to the biasing conditions. On the other



(a) I_D-V_G characteristic.

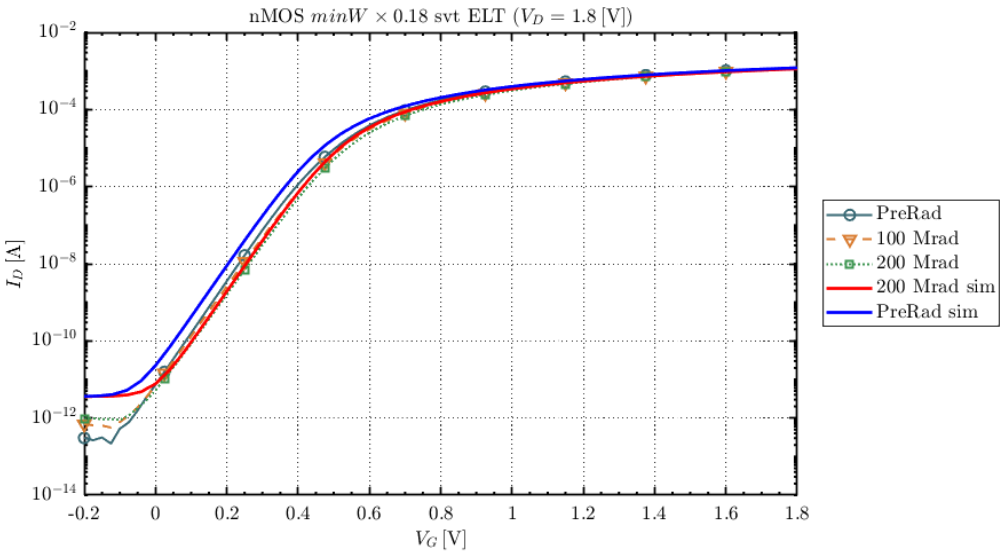


(b) I_D-V_D characteristic.

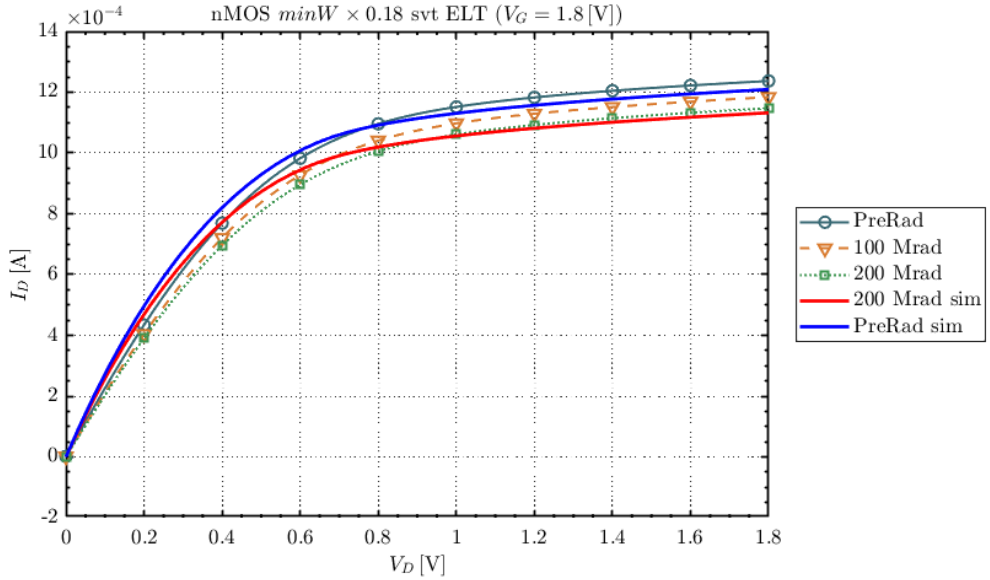
Figure 2.6: 1.8 V-PMOS $I_D - V_G$ and $I_D - V_D$ characteristics, both measured and simulated. Both pre-irradiation and post-irradiation characteristics are plotted. The simulated post-irradiation characteristics correspond to a TID of 200Mrad.

hand, the leakage problem has to be accurately managed since it could lead to overvoltages in the high-voltage circuitry and possible device failures.

Along with the developed TID models, a Verilog-A block is implemented to describe the transistor-like behavior of the parasitic FOXFET. It is then instantiated within the model file, specifically in the radiation-corner section.



(a) I_D-V_G characteristic.



(b) I_D-V_D characteristic.

Figure 2.7: 1.8 V-NMOS $I_D - V_G$ and $I_D - V_D$ characteristics, both measured and simulated. Both pre-irradiation and post-irradiation characteristics are plotted. The simulated post-irradiation characteristics correspond to a TID of 200Mrad.

The current of the parasitic FOXFET is modulated with both V_{gs} and V_{ds} (dynamic electrical parameters of the transistors during the transients):

- V_{gs} modulation: for a fixed leakage condition, a larger gate-to-source voltage

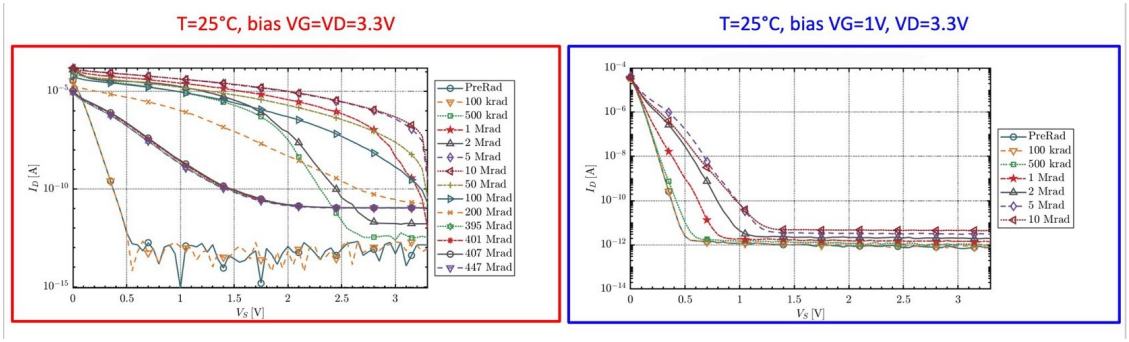


Figure 2.8: Behavior of the I_{OFF} current over a sweep on the source voltage at room temperature at different bias conditions for a n-type LDMOS. $V_{DS,bias}$ is the same in both cases and it is equal to 3.3 V. $V_{GS,bias}$ is equal to 3.3 V in the red picture, 1 V in the blue one.

helps accumulating charges in the parasitic channel.

- V_{ds} modulation: the direction of the current changes according to the sign of V_{ds}. If $V_{ds} = 0$, no leakage current flows in the device.

If $V_{ds} \neq 0$ and $V_{gs} < 0$ there is still a residual leakage current depending on the irradiation conditions. Saturation is arbitrarily fixed at $V_{ds} = 100\,\text{mV}$.

The peak in the leakage current is found at a TID lower than 200Mrad (around 1Mrad), since there is not yet the compensation mechanism caused by the negative charges accumulated at the interface. For the sake of simplicity, for the 200 Mrad corner the worst case biasing for the leakage current $|V_{GS,bias}| = 3.3\,\text{V}$ is considered for all transistors, which correspond to 6.5 µA. It is nevertheless important to simulate also the circuit behavior in correspondence of the peak in the leakage current. This particular situation is simulated in a dedicated corner, using a Verilog-A component similar to the previous one. However, in this case the dependence of the peak leakage current on $|V_{GS,bias}|$ is considered in the simulations, as considering the worst-case peak leakage would lead to unrealistic results. According to measurement results, the peak value of the leakage current is 5 µA when $|V_{GS,bias}| = 1\,\text{V}$ and 100 µA when $|V_{GS,bias}| = 3.3\,\text{V}$. In the experimental data it is observed that when $|V_{GS,bias}| = 3.3\,\text{V}$ the current is not modulated by the gate voltage, whereas in the case of $|V_{GS,bias}| = 1\,\text{V}$ a V_{gs} modulation is observed. As a worst case, is is assumed that the leakage current remains independent of V_{gs} in each scenario.

2.2.2 Modeling of the SEEs

The effect of single events on CMOS devices is the generation of electron-hole pairs that can alter the device normal behavior. This charge injection can be modeled using a triangular shape current pulse.

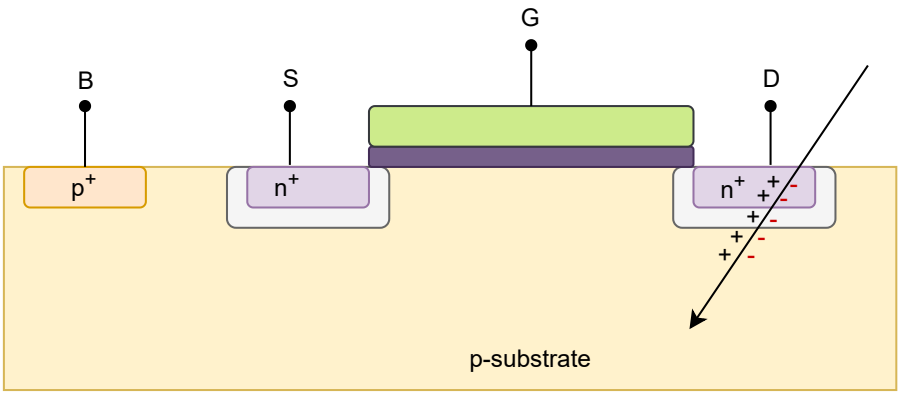


Figure 2.9: Schematic drawing of an NMOS transistor in CMOS technology. The impact of a highly-energetic single particle generating e-h pairs is highlighted.

A schematic of a NMOS transistor in CMOS technology is depicted in Figure 2.9 . When a high energetic particle hits the circuit, it generates e-h pairs within the device, as represented for the drain node. Pairs generated in the substrate or in the n+ regions rapidly recombine whereas in the depletion region they are separated due to the presence of a high electric field. In this case, positive charges are attracted to the lower potential node, which is the bulk contact, typically connected to the V_{ss} power rail. Some of these holes recombine in the substrate but the majority flows towards the contact with negligible impact on its potential value due to its low impedance, being connected to a power rail. Electrons instead are attracted to the node at higher potential which is the drain in this case. This results in a discharging current from the drain to the bulk, leading to a temporary decrease of the drain potential.
As for the PMOS counterpart, there is an analogous mechanism. In this case, negative charges are attracted to the bulk contact, connected to the V_{dd} power rail. Positive charges instead flow towards the drain contact that corresponds to the lower potential node, increasing temporarily its potential and resulting in a charging current from bulk to drain.
In principle, also the source contact is subjected to the same phenomena but it is typically connected to the bulk, then it does not have any influence.
Given these considerations, usually only some specific nets of the circuit are checked. In particular, only nets corresponding to transistors terminals are meaningful. If the source is connected to the bulk, the set reduces to only drain nodes. According to the mechanisms presented earlier, the additional current sources to model SEE are schematically represented in Figure 2.10.

The quantity of e-h pairs generated by the incident particle is proportional to the amount of energy deposited by that particle per unit distance, which is usually measured in terms of Linear Energy Transfer (LET). In particular, this quantity

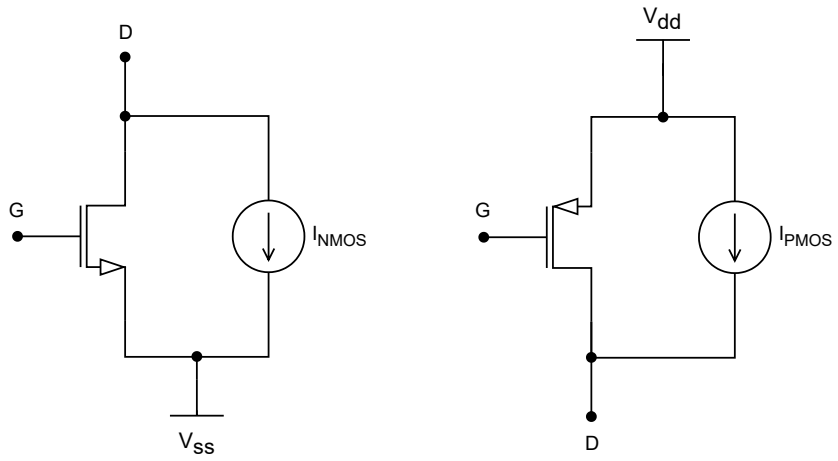


Figure 2.10: Ideal current sources used to model SEE. SEE in NMOS transistors are modeled with a current pulse flowing from the drain to V_{ss}, whereas in PMOS transistors they are modeled with the same current pulse between V_{dd} and the drain.

can be expressed as an energy per unit distance, and then normalized using the density of the material: $\frac{eV}{cm} \cdot \frac{cm^3}{mg} = \frac{eV \cdot cm^2}{mg}$. The value of Linear Energy Transfer (LET) can be correlated with the amount of charge deposited in the sensitive area of the device, and previous works have demonstrated that for $LET = 1\frac{eV \cdot cm^2}{mg}$, the corresponding injected charge is approximately $10fC$. In this project, circuits are hardened up to a LET of $40\,\mathrm{eV\,cm^2\,mg^{-1}}$. As the duration of the charge injection is not known, it has been modeled using two current pulses with different duration:

- $I_{peak} = 4\,\mathrm{mA}$, $t_{rise} = 50\,\mathrm{ps}$, $t_{fall} = 150\,\mathrm{ps}$.
- $I_{peak} = 400\,\mu\mathrm{A}$, $t_{rise} = 500\,\mathrm{ps}$, $t_{fall} = 1.5\,\mathrm{ns}$.

These two possibilities represent fast and slow injection conditions. Since the event altering the node voltage has a very limited duration, in several cases it does not significantly influence the circuit behavior. Nevertheless, the effect on some sensitive nodes can be relevant, thus proper techniques must be adopted to make them robust to SEE. In general, to limit this effect, their high-frequency impedance is reduced with the addition of capacitances. The main techniques to contrast SEEs are listed below:

1. Addition of a capacitor between the node under consideration and a power rail.
2. Addition of an R-C filter.

3. Addition of a normally-off clamp transistor. It tends to turn on when the node is kept down (up) in the presence of a single event, allowing a fast recovery of the original voltage. This approach just shortens the duration of the event.

Figure 2.11 provides a graphical overview of the three techniques.

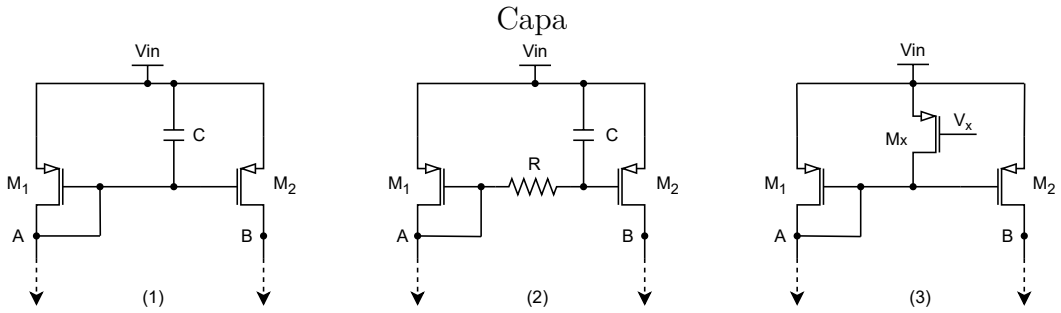


Figure 2.11: Schematic representations of the three main techniques used to harden circuits against SEEs. In all cases node "A" represents the node hit by the particle. In the third circuit, V_x represents a bias voltage properly generated to ensure the correct functionality of the clamp transistor M_x.

SEE injection cell development

Prior to this work, SEE injections were tested manually for analog circuits in the team hosting this Master thesis, instantiating in the schematics different current sources according to the configuration shown in Figure 2.10. Such sources are triggered at different times, in order to allow the testing of each injection independently from the others. This proves to be quite time-consuming, thus an alternative solution is used in this project. The idea is the development of a VerilogA module to be instantiated in the schematic cell of the component under test. The Verilog-A code is reported in the following:

```
1  `include "constants.vams"
2  `include "disciplines.vams"
3  `define NUMBITS 100
4
5  module SEE_INJECT(
6          input input_i,
7          input [`NUMBITS-1:0] in_nets_neg,
8          input [`NUMBITS-1:0] in_nets_pos,
9          inout VSS);
10
11         parameter starting_point=10e-6, interval=1e-6;
12         electrical input_i, VSS;
```

```
13          electrical [`NUMBITS-1:0] in_nets_neg;
14          electrical [`NUMBITS-1:0] in_nets_pos;
15
16          analog begin
17                  generate i (`NUMBITS-1,0) begin
18                          V(input_i,VSS)<+0;
19                          I(in_nets_pos[i],VSS)<+absdelay(I(
                               input_i,VSS)*(-1),starting_point+
                               interval*i);
20                          I(in_nets_neg[i],VSS)<+absdelay(I(
                               input_i,VSS),starting_point+
                               interval*(`NUMBITS+i+1));
21                  end
22          end
23
24  endmodule
```

A quick overview of the code functionality is given below, and a graphical representation of the cell symbol is provided in Figure 2.13. The cell presents three input ports:

- *input_i*: this is an electrical input that corresponds to the reference current signal to be injected in the circuit nodes (see Figure 2.12).
- *in_nets_pos*: this is an array of the positive injection nets, that means injection into the node (current entering the node).
- *in_nets_neg*: this is an array of the negative injection nets, that means charge withdrawal from the node (current exiting the node).

The time intervals can be customized thanks to the presence of two parameters in the module: *starting_point* defines the starting point of the injection current whereas *interval* specifies the time interval between each net injection. Figure 2.14 shows the positive and negative injections on the nets associated to the *in_nets_pos* and *in_nets_neg* input arrays.

The next step is the development of a SKILL script which allows the automatic extraction of the nets of a specific schematic cell and connects them to the positive and negative inputs of the SEE injection cell. In this way, instantiating the SEE injection cell in the schematic of the cell under test, all nodes are automatically perturbed. Here a brief description of the script purposes is reported, then the complete code is detailed in Appendix A. It is composed of two procedures:

- *SEEinjection()*: this procedure extracts all nets of an input cell schematic and generates a list with such nets. It ensures also that multiple nets (those connected together) are added to the list only once. Since the input arrays of the SEE injection cell have 100 elements, the remaining ones are left floating.

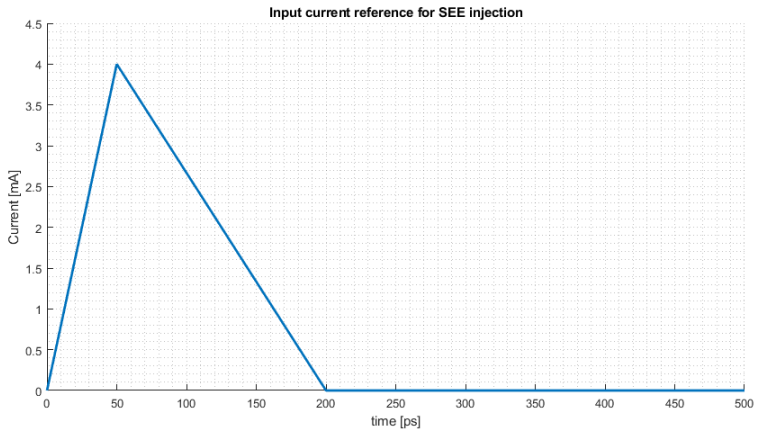


Figure 2.12: Current signal injected in the circuit's nodes. This is the case of a fast injection with 4 mA peak amplitude.

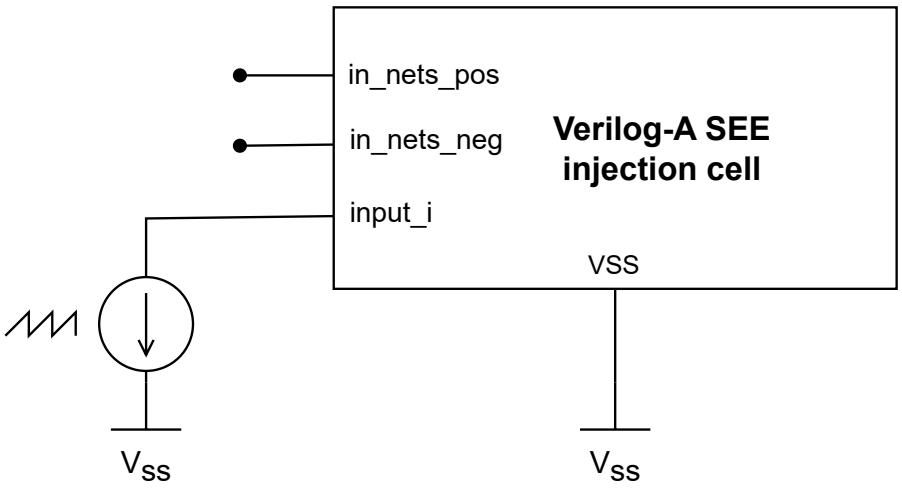


Figure 2.13: Graphical drawing of the symbol of the implemented Verilog-A module for the single events injection. To the *input_i* port a triangular current source with the shape previously described is connected.

- *ChangeNetLabel()*: this procedure takes in input the list of nets generated in the previous procedure and modifies the labels of the input arrays of the SEE injection cell.

Using this script, it is only necessary to instantiate the cell in the same schematic of the cell under test and simulate the circuit. It must be noted that the script is useful to both inject and withdraw current from all nodes, although only a subset of them is meaningful due to the reasons previously mentioned.

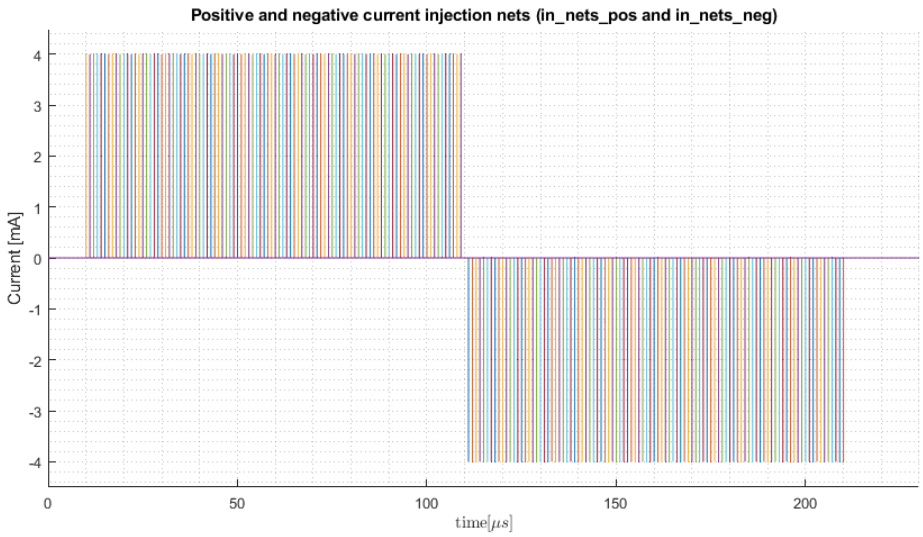


Figure 2.14: Positive and negative injection nets in the Verilog-A injection cell. In this particular case, a starting point of 10 µs and a time interval of 1 µs are set.

2.2.3 Layout techniques

The most relevant layout strategy to make circuits more radiation-tolerant is the implementation of NMOS transistors as Enclosed Layout Transistor (ELT) [12]. This is a layout strategy that completely eliminates the parasitic paths for the leakage current caused by the presence of the STI oxide (see Figure 2.15). The source terminal is arranged to surround both the polysilicon gate and the drain terminal in a centrally symmetrical manner. As a result, there are no parasitic paths at the edges of the channel.

Nevertheless, this techniques presents some disadvantages to be taken into account:

- The modeling of W/L ratio is challenging and imposes limitations in the range of usable W/L ratios.
- Increased area consumption with consequent density reduction.
- Higher gate and source/drain capacitances.

However, due to their high leakage degradation, it is a good practice using this strategy in the layout of NMOS transistors, whereas it is not used for PMOS transistors since they do not present this leakage problem. In this project, an enclosed layout could be adopted for low-voltage devices, while that was not possible for LDMOS due to Design Rules violations. The radiation-induced leakage of LDMOS had therefore to be included in simulations, as presented in Section 2.2.1.

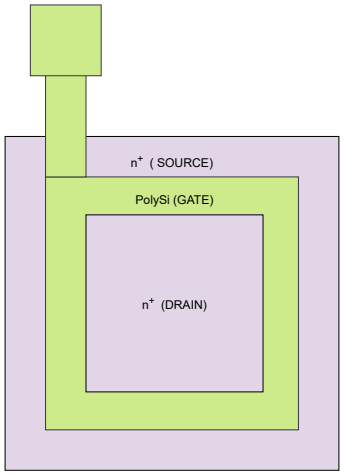


Figure 2.15: Schematic drawing of an Enclosed Layout Transistor (ELT).

Another layout method to improve the tolerance to radiation effects consists of sorrounding neighbouring NMOS devices with different source connections with a p+ guard ring, solving the leakage parasitic paths under the STI oxide between different devices. The same has to be done between a NMOS devices and n-wells. Also in this case, the area consumption increases.
Several layout approaches are adopted also to prevent SEEs, particularly SEL. Referring to Figure 2.5, the number of substrate and well contacts are maximized to minimize resistances R_1 and R_6. Furthermore, the distance between the p+ diffusion in the n-well and n+ diffusion in the substrate is increased. Finally, besides NMOS devices also PMOS are sorrounded by n+ guard rings. P+ guard rings are used to reduce the gain of the parasitic NPN bipolar transistor by creating a highly doped region in the base, which efficiently connects the base to the ground. Similarly, n+ guard rings serve the same purpose for the PNP bipolar transistors.

Chapter 3

Current Reference

The first part of the project consists of the design of two current references needed for other internal blocks of the DC-DC converter, including the OPAMP used in the BGR circuit. The first is a low-voltage current reference circuit, supplied by a voltage of 1.8 V and with an output current of 2 µA. In the design of this block core transistors with maximum V_{DS} and V_{GS} of 1.8 V are used since it is not necessary to handle high voltages. The second block instead is a high-voltage current reference, with supply voltage up to 55 V and output current of 20 µA. The latter includes instead high-voltage transistors in the design, which are able to withstand a V_{DS} up to 30 V.

3.1 Working principle

The configuration chosen for the current reference is a beta multiplier circuit. The schematic of the latter is shown in Figure 3.1.

Analyzing the circuit schematic, the equation of the output current can be derived. From the PMOS network:

$$I_{ref} = k \cdot I_{out}. \tag{3.1}$$

I_{ref} and I_{out} can be written respectively as:

$$I_{ref} = \frac{\beta_n}{2}(V_{GS1} - V_T)^2, \tag{3.2a}$$

$$I_{out} = \frac{\beta_n}{2}(V_{GS2} - V_T)^2, \tag{3.2b}$$

where $\beta_n = k_{p,n} \cdot \frac{W_n}{L_n}$, $V_{GS1} = V_G$ and $V_{GS2} = V_G - R_S I_{out}$. $V_G - V_T$ can be derived from Equation 3.2a and it can be substituted in Equation 3.2b. Using also the relationship between I_{ref} and I_{out} given by Equation 3.1, it results:

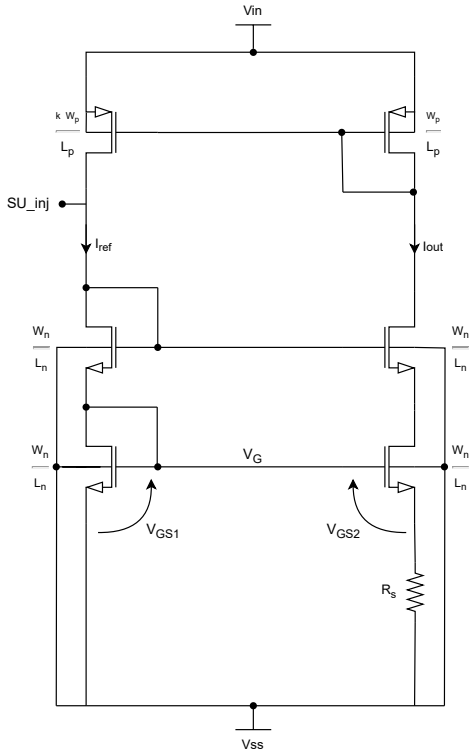


Figure 3.1: Schematic of the low-voltage Beta Multiplier.

$$\sqrt{I_{out}} = \sqrt{\frac{\beta_n}{2}} \cdot \left(\sqrt{\frac{2k}{\beta_n}} - R_S \sqrt{I_{out}} \right). \tag{3.3}$$

At this point, the final expression of I_{out} can be extracted, and two solutions can be obtained. The solution $I_{out} = 0$ can be discarded thanks to the adoption of a start-up circuit (presented in subsection 3.2.1), so the output current of the circuit results:

$$I_{out} = \frac{2}{\beta_n \cdot R_S^2} (\sqrt{k} - 1)^2. \tag{3.4}$$

The temperature coefficient (TC) of the output current can be obtained as:

$$TC(I_{out}) = \frac{1}{I_{out}} \frac{\delta I_{out}}{\delta T}. \tag{3.5}$$

Looking at Equation 3.4, the only two terms that must be considered as dependent on temperature are R_S and k_p. Thus, applying the chain rule, Equation 3.5 becomes

$$TC(I_{out}) = \frac{\delta I_{out}}{\delta R_S}\frac{\delta R_S}{\delta T} + \frac{\delta I_{out}}{\delta k_p}\frac{\delta k_p}{\delta T} = -(2TC(R_s) + TC(k_p)), \tag{3.6}$$

where $TC(R_s)$ can be shortened with "TCR".

3.1.1 Design strategy

The specifications for the current reference circuit under consideration are the following:

- Output current (I_{out}): the desired output current is 2 µA.
- Temperature Coefficient (TC): the circuit should have a constant behavior with respect to temperature variations. The TC of the current should not exceed 10% of relative variation.
- Power Supply Rejection (PSR): the circuit should have good PSR capabilities, with a minimum of 130dB at low frequencies. This ensures that the output current remains stable also if there are fluctuations on the supply voltage. Moreover, the PSR should remain high enough also around the switching frequency of the converter, which is between 1 MHz and 5 MHz.

The value of the output current is fixed by Equation 3.4. The used 1.8 V-rated NMOS device features a value of $k_{p,n}$ of around 200 $\frac{\mu A}{V^2}$ for V_{DS} between 0.1 V and 1 V. To choose the values of the other parameters in the equation to meet the specification on the output current, several considerations must be taken into account. First of all, the value of k is fixed to *4*. Then, NMOS and PMOS transistors are sized. In this circuit transistors are used in current mirror configurations, where ideally the copied current should always be equal or a multiple of the input current. Actually they have slightly different characteristics due to mismatch. To compensate for these errors, the lenghts of the transistors are chosen sufficiently large to reduce the variations due to mismatch. Moreover, the length is chosen large enough also to mitigate the Channel Length Modulation (CLM) of the transistors that can cause deviations from the ideal value of the output current. Cascode adopted for the NMOS transistors contributes to minimize CLM. Due to headroom limitations, a cascode could not be used for the PMOS, and L_p is chosen to be larger than L_n to minimize the impact of mismatch. In particular $L_p = 5\,\mu m$ and $L_n = 2.5\,\mu m$. Taking into account also the predefined value for the output current, $I_{out} = 2\,\mu A$, W_n/L_n and W_p/L_p are chosen to be respectively 1 and 4 to make the transistors remain in the strong inversion region. This ensures reduced sensitivity to mismatch and linearity in the current relationship (indeed, Equation 3.2 is true only in strong inversion conditions). Having both the W/L ratio and the length of the transistors defined, the width can be derived: $W_n = 10$ and $W_p = 5$.

The values of W_n/L_n and k (both equal to 4), can be used to find the value of the resistance R_S reversing Equation 3.4:

$$R_S = \sqrt{\frac{2}{\beta_n I_{out}}(\sqrt{k}-1)^2} \simeq 35\,\text{k}\Omega. \tag{3.7}$$

To improve the behavior of the current with respect to temperature the resistance R_S must be optimized. Analyzing Equation 3.6, the TC of k_p is the same as the TC of the mobility of the transistor μ, being $k_p = \mu \cdot C_{ox}$. Increasing temperature also scattering increases, leading to a decrease of the mobility. Consequently $TC(k_p)$ is always negative, in this case $TC(k_p) = -\frac{1.34}{T}$. Thus, to compensate the temperature behavior a resistance with a positive TCR is needed. However, the total resistance is split to include also a negative TCR resistance, in order to have a further degree of freedom to tune $TC(I_{out})$ until reaching approximately zero. An overview of the selected values for the circuit parameters is presented in Table 3.1.

W_p $[\mu m]$	L_p $[\mu m]$	W_n $[\mu m]$	L_n $[\mu m]$	k	R_S $[k\Omega]$
5	5	10	2.5	4	35

Table 3.1: Summary of the sizing choices for the current reference circuit.

3.2 Core Beta Multiplier

3.2.1 Start-up circuit

A start-up circuit for the Beta Multiplier is needed to avoid the solution $I_{out} = 0$ of Equation 3.3. In this way, the circuit will start working at the right operating point without getting stuck at zero. The schematic of the employed start-up circuit is shown in Figure 3.2.

When the circuit is started-up (Power supply is switched on) there is no current flowing in the circuit, then $V_G = 0$ (see Figure 3.1). Since the gate of M_2 is connected to V_G, the transistor is initially turned off. Thus, the input of the inverter composed of transistors M_3, M_4 is at a high value, and the gate node of transistor M_5 is low. M_5 will inject current to SU_inj node (see Figure 3.1) until V_G will be high enough to turn M_2 on and reverse the configuration. As for the sizing choices of the start-up circuit, it is important to have a small W/L ratio on transistor M_1 to limit its current in steady-state. The same choice applies also to transistor M_5 to limit the initial injection current, that can impact on the output current steady-state value. Therefore, they are both fixed to 0.1. In order to reach a working

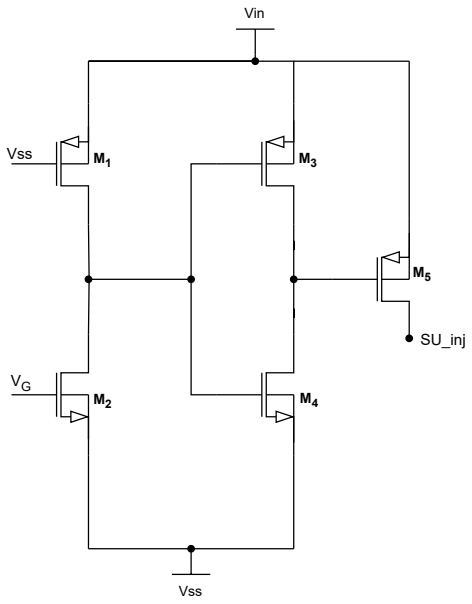


Figure 3.2: Schematic of the start-up circuit of the low-voltage Beta Multiplier.

operating condition, the sizing of the other transistors is carefully optimized and a summary of the selected transistor parameters is reported in Table 3.2.

	M_1	M_2	M_3	M_4	M_5
Width $[\mu m]$	1	10	20	20	1
Length $[\mu m]$	10	1	1	1	10

Table 3.2: Summary of the sizing choices for the current reference start-up circuit.

3.2.2 PSR

The output current of the reference circuit must have a good PSR, which means it must be quite independent on the variations of the supply voltage. The NMOS network of the circuit is cascoded to improve the Power Supply Rejection (PSR). In this way, the cascoded structure fixes the V_{DS} voltages of the NMOS transistors keeping them independent on the variations of V_{in}. A better result would be reached cascoding also the PMOS network to ensure a precise current copy, but being the supply voltage quite low (1.8 V) the headroom is not enough to make the circuit work in the correct way. The resulting PSR at the typical process corner is shown in Figure 3.3. It is approximately equal to 152dB at low frequencies, then it starts to worsen at higher frequencies due to the presence of parasitic capacitances.

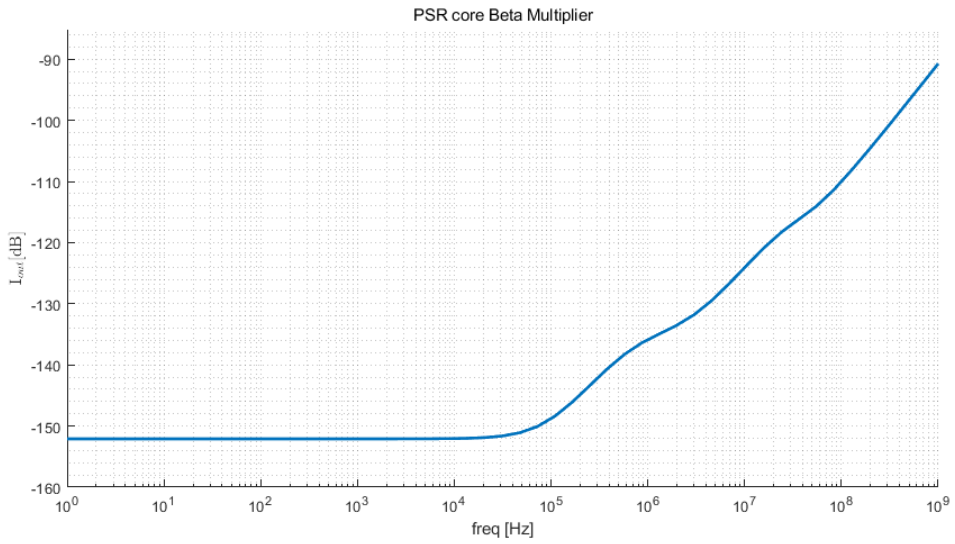
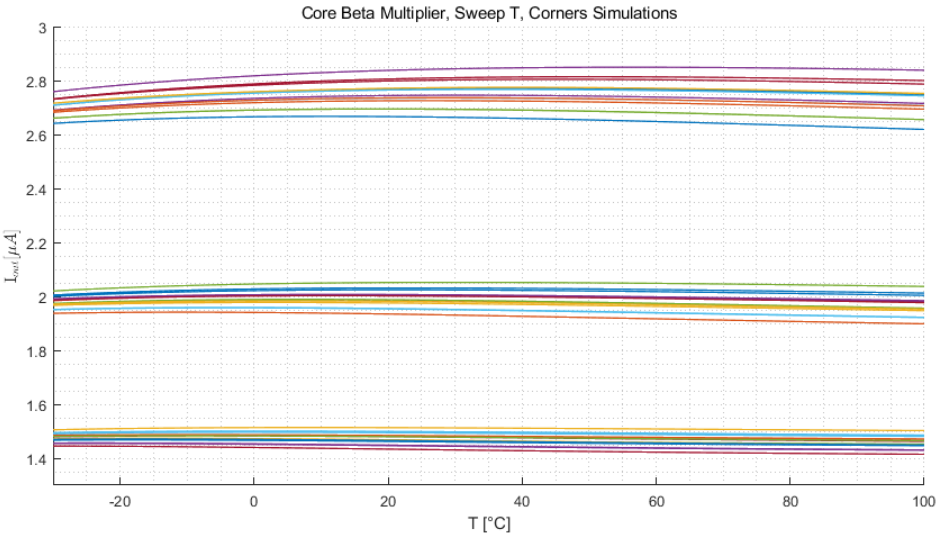


Figure 3.3: PSR of the output current in the low-voltage Beta Multiplier.

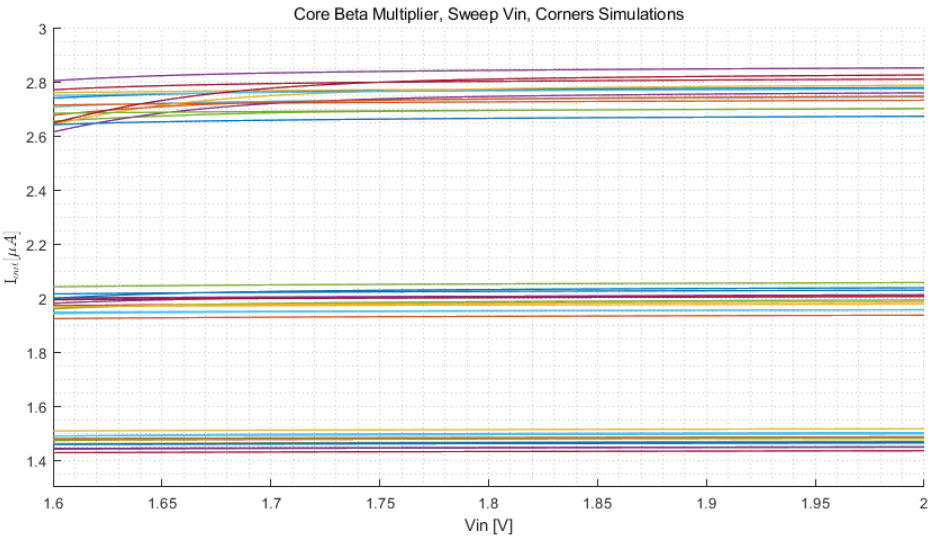
3.2.3 Final core current reference circuit simulations

The circuit is simulated over a set of corners that take into account supply voltage, temperature and process changes on both transistors and resistors. Also radiation corners for a TID of 200Mrad are included. The output current of the Beta Multiplier features three different bands of values, due to the high process variations of the resistance in this technology (see Figure 3.4). In particular, the lowest band refers to corners "high" of resistance, the middle band to the typical corners, whereas the highest band to the corners "low" (output current is quadratically inversely proportional to the resistance). These variations among the three bands result acceptable for the OPAMP used for the bandgap reference circuit, since it was properly designed to work also at different values of current references.
However, taking into account a single band of values, it results very constant with Temperature (Figure 3.4a) and supply voltage (Figure 3.4b), with around 100 nA of absolute variation.

Also, Monte Carlo simulations are performed to ensure a stability of the output current with mismatch variations. Results are reported in Figure 3.5. I_{out} has an absolute variation of about 100 nA that corresponds to 5% deviation from the expected value.



(a) Sweep of the Temperature T from −30°C to 100°C.



(b) Sweep of the Supply Voltage V_{in} from 1.6V to 2V.

Figure 3.4: Behavior of the output current of the core beta multiplier sweeping temperature and supply voltage. Both process corners on transistors and resistors and TID radiation corners are simulated.

3.3 Circuits adjustment for a high-voltage application

The high-voltage version of a generic circuit can be implemented with the same topology as the low-voltage one. However, since the power supply voltage may

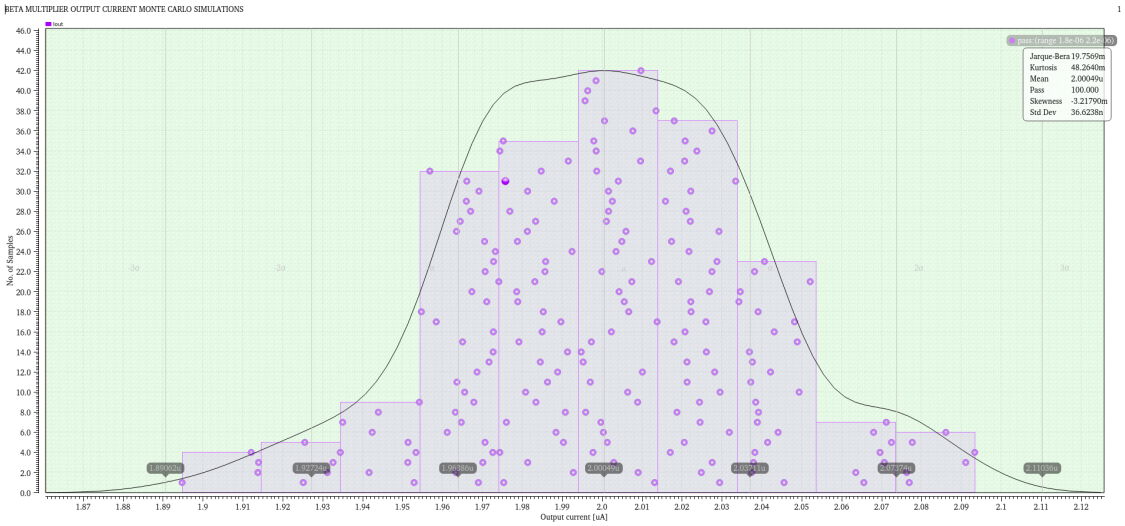


Figure 3.5: Monte Carlo mismatch simulations of the low-voltage beta multiplier output current. 200 runs at room temperature with supply voltage of 1.8 V are performed.

reach up to 55 V, the schematic must be extended through the addition of clamping high-voltage transistors (LDMOS). The employed LDMOS transistors can withstand values of V_{DS} up to 30 V, thus a series of two of them for each branch is needed to sustain the input voltage also in the worst case. These transistors must be accurately biased to act as clamping devices and make sure that the low-voltage transistors keep working in their Safe Operating Area (SOA). SOA refers to the set of conditions associated to a specific model of transistor that define the limits under which it properly work without experiencing degradation or damage. Since the employed transistors in the design have a V_{DS} rating lower than the power supply, it is essential to check if they operate in their SOA. Besides supply voltage, temperature and process corners on both active and passive devices, also radiation corners are simulated. High voltage circuits are more susceptible to radiation-induced variations compared the low-voltage counterpart. This is due to the presence of LDMOS transistors, featured with high radiation-induced degradation (see subsection 2.1.3). Moreover, the correct biasing of LDMOS transistors is challenging thus they typically operate with tight design margins. The confluence of these factors makes the circuit design critical in maintaining optimal operating conditions, ensuring that all transistors work properly and within their specifications.
Another issue that should be taken into account designing high-voltage circuits is that n-type LDMOS device feature high values of leakage current (details were presented in subsection 2.2.1). Consequently, in the branches with a N-LDMOS a current at least equal to the its leakage current should flow to ensure the correct functionality of the circuit.

3.4 High-voltage Beta Multiplier

The high-voltage version of the current reference circuit has the same specifications as the previously described low-voltage circuit, except for the reference current which must be increased to 20 µA.

3.4.1 High-voltage schematic

In the specific case of the current reference circuit adjustment, PMOS and NMOS transistors which are not in the diode connected configuration need to be protected. For this purpose, two high-voltage p-type LDMOS transistors ($LD_{1,2}$) are added to protect the low-voltage pmos current mirror. Analogously, two high-voltage n-type LDMOS transistors ($LD_{3,4}$) are used to protect the nmos part. Figure 3.6 shows the new high-voltage schematic, including LDMOS devices.

Moreover, in the context of high voltage applications, it is crucial to review the design parameters since a reference current of 2 µA cannot be feasible to ensure proper circuit functionality. For this purpose the values of the k parameter and of the resistances R_S are adapted for a current I_{ref} of 10 µA, which is then copied and doubled through parallel transistor to achieve 20 µA, required by specifications. Table 3.3 summarizes the final sizing of the adapted circuit.

W_p $[\mu m]$	L_p $[\mu m]$	W_n $[\mu m]$	L_n $[\mu m]$	k	R_S $[k\Omega]$
5	5	10	2.5	8	23.2

Table 3.3: Summary of the sizing choices for the high-voltage current reference circuit.

3.4.2 High-voltage biasing branches

High-voltage transistors need to be accurately biased to ensure that the system remains always in an optimal operating condition. In Figure 3.7 the employed biasing configuration is represented. These biasing voltages will be used also for the high-voltage transistors needed in the extension of the design of the other blocks in this project (OPAMP, BGR circuit).

The bias voltages VB_1, VB_{1_h}, VB_2, VB_{2_h}, VB_{2_hh} are generated through series resistors and diode connected transistors. These voltages must be available immediately even before the start-up phase is ended, in order to ensure that all the devices operate in their safe operating area. For the biasing of PMOS high-voltage transistors, two diode-connected transistors and a resistor voltage divider are used. On the other hand, the biasing for the NMOS transistors involves three

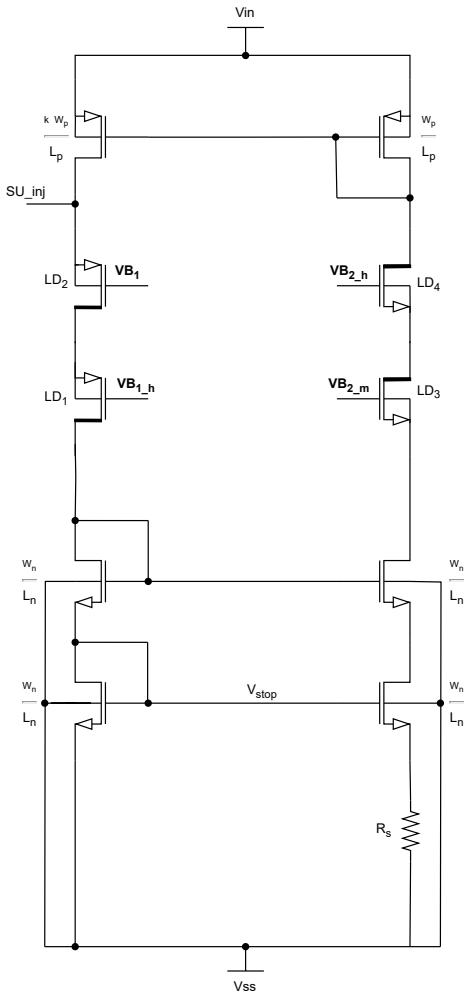


Figure 3.6: Schematic of the high-voltage Beta Multiplier.

diode-connected transistors. This different configuration is necessary because in some cases the low-voltage transistors to be protected are in cascode configuration, requiring a higher voltage margin. To ensure a correct functionality also in radiation corners, both low- and high-voltage transistors are employed for the diode-connected series transistors. In fact, with this approach the degradation of the biasing branches follows the one of the main branches.

3.4.3 New start-up circuit

Along with the current reference circuit itself, also its start-up circuit should be revised for a high-voltage application. In particular, the new start-up configuration is depicted in Figure 3.8.

During the start-up phase, when the power supply voltage is still close to 0,

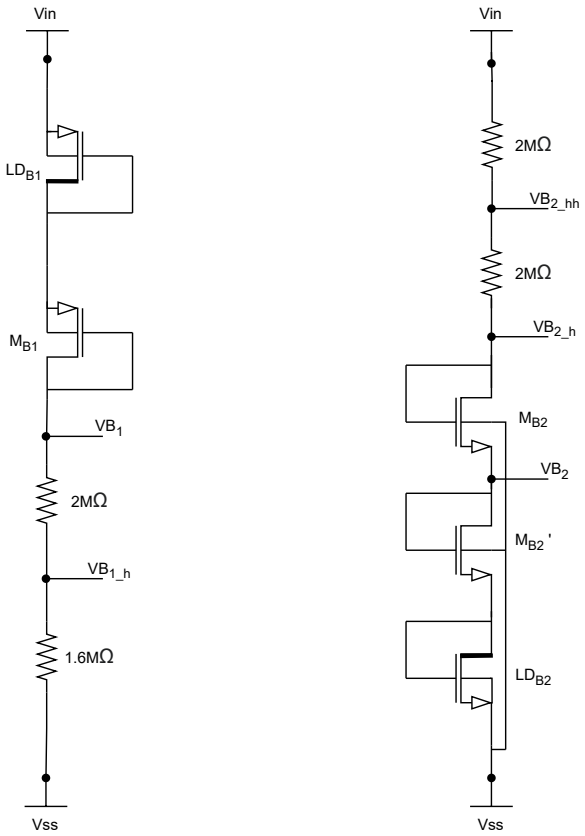


Figure 3.7: Schematic of the biasing branches for the high-voltage transistors.

no current flows in the circuit thus node V_{stop} is near V_{SS}. As a consequence, M_{S1} remains in an off-state and no current flows in this branch. M_{S2} also stays off, allowing M_{S3} to inject current into the beta multiplier. Once V_{stop} rises, M_{S1} turns on causing the gate voltage of M_{S2} to decrease, enabling it to turn on as well. This leads to an increase in the gate voltage of M_{S3} and the current injection stops.
To ensure that the SOA conditions are satisfied, transistors $M_{S4,5,6}$ act as clamps for the V_{GS} of M_{S3} and M_{S2} when they are in the on-state. These clamping transistors should be accurately sized to ensure a sufficiently large V_{GS} of M_{S3} and M_{S2} when they should conduct, without exiting SOA specifications.
LD_{B1}, LD_{B2} transistors are added to protect M_{S1}. These transistors are n-type LDMOS, thus they experience an increase in their leakage current due to radiation. Given these considerations, R_C is accurately chosen to maintain a proper voltage drop that keeps M_{S2} in the on-state in all corners. At the same time it is also essential to limit the voltage drop caused by the leakage current in the start-up phase to prevent M_{S2} from turning on prematurely, ceasing the current injection. According to simulation results, the value of R_C is fixed to 70 kΩ. Moreover, R_A needs to be carefully sized. It is used to limit the current in the steady-state

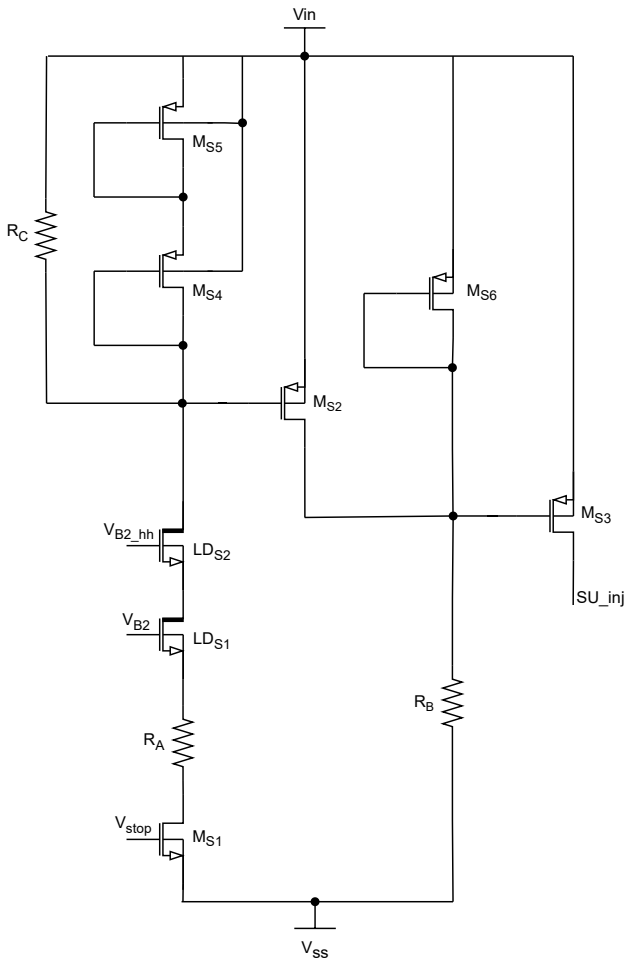


Figure 3.8: Schematic of the high-voltage start-up circuit.

condition, when M_{S1} is turned on. This current should be high enough compared to the leakage current of high-voltage transistors. Furthermore, together with the value of R_C, fixing the current of the branch contributes to fix the voltage drop across R_C. Again based on simulations, R_A value is set at 10 kΩ.
Resistance R_D instead should be high enough to limit the current flow in its branch, since it experiences the voltage drop of the total supply voltage except for the V_{DS} of M_{S6}. For this purpose, it is fixed to 2 MΩ. All the sizing choices are summarized in Table 3.4.

3.4.4 Final high-voltage current reference circuit simulations

Figure 3.9 illustrates the PSR of the high-voltage current reference circuit, for two different supply voltages. Decreasing the power supply voltage also PSR at

	M_{S1}	M_{S2}	M_{S3}	$M_{S4,5}$	M_{S6}
Width $[\mu m]$	5	24	1	40	72
Length $[\mu m]$	1	0.5	1	0.18	0.5

R_A $[k\Omega]$	R_B $[M\Omega]$	R_C $[k\Omega]$
10	2	70

Table 3.4: Summary of the sizing choices for the high-voltage current reference start-up circuit.

low frequencies decreases. However, it is still significantly higher than the value required by the specifications (130 dB).

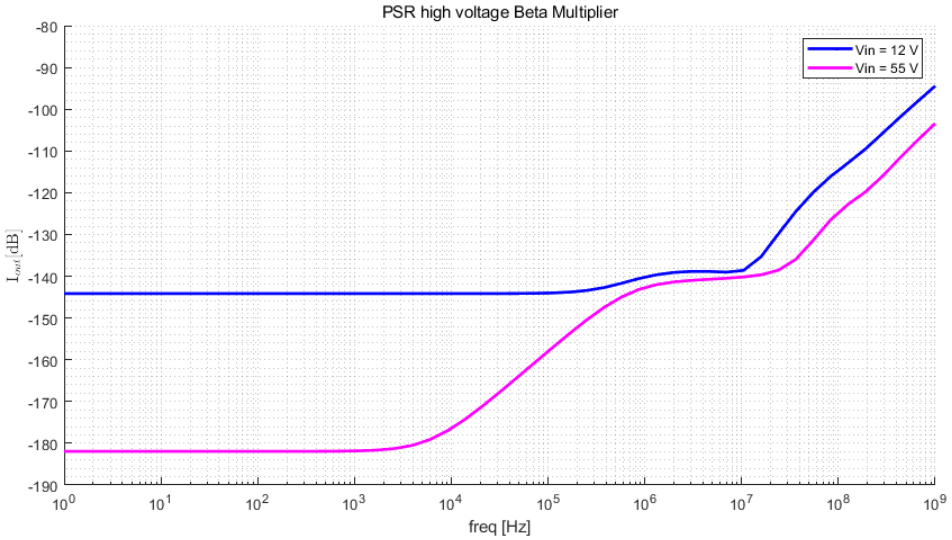
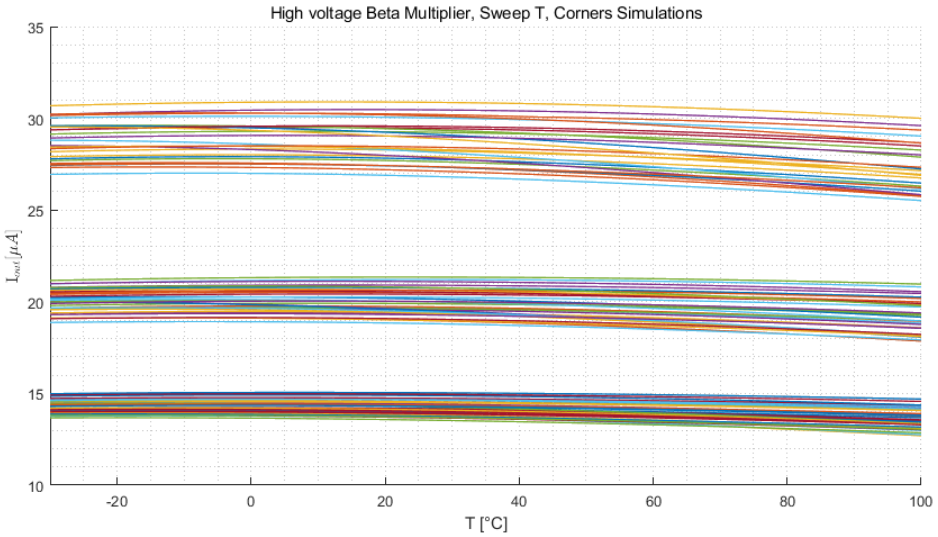


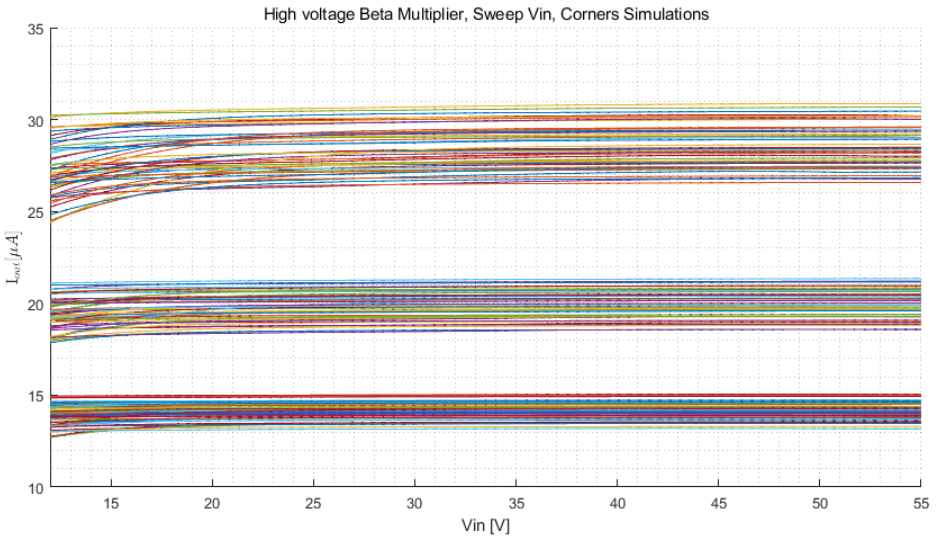
Figure 3.9: PSR of the output current of the high-voltage Beta Multiplier for a supply voltage equal to 12 V and 55 V.

The high-voltage circuit is simulated over the same set of process and radiation corners as the low-voltage version. Figure 3.10 displays the value of the reference current over a sweep in temperature (Figure 3.10a) and supply voltage (Figure 3.10b). Also in this case it is clear the presence of the three bands due to the resistance corners. The absolute variation between bands is quite large, but still acceptable for the application. Nevertheless, considering only a specific band of values, the relative variation remains less than the 5% with respect to the nominal value.

To conclude, Monte Carlo simulations are performed to verify that the value



(a) Sweep of the Temperature T from −30°C to 100°C.



(b) Sweep of the Supply Voltage V_{in} from 12 V to 55 V.

Figure 3.10: Behavior of the output current of the high-voltage Beta Multiplier sweeping Temperature and Supply Voltage. Both process corners on transistors and resistors and TID radiations corners are simulated.

of the new reference current still meets the specifications. Results are depicted in Figure 3.11. In this case, the worst case sample deviates from the nominal value of less then the required 3% relative variation.

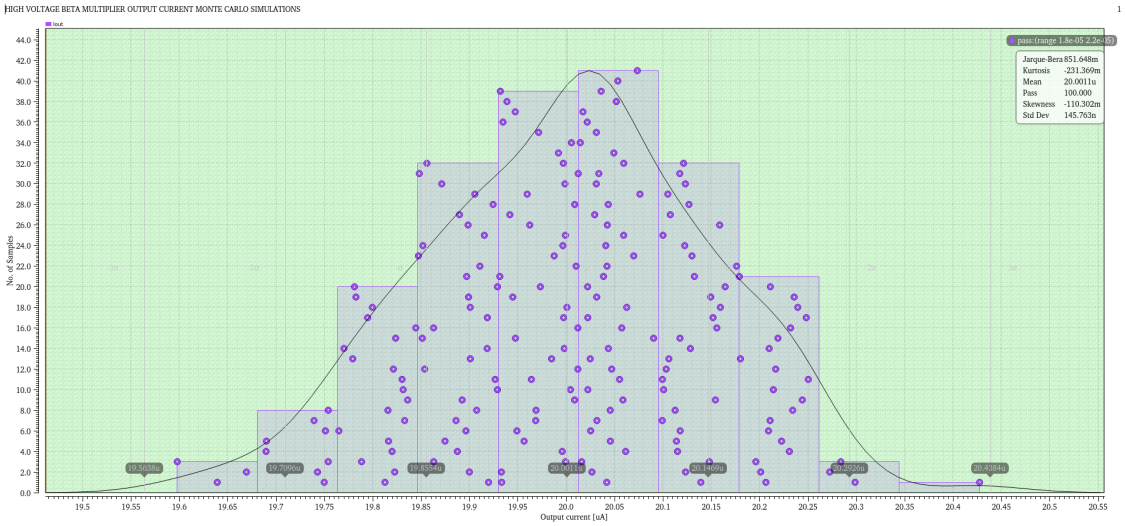


Figure 3.11: Monte Carlo mismatch simulations of the high-voltage beta multiplier output current. 200 runs at room temperature with supply voltage of 48 V are performed.

Chapter 4

Bandgap Reference

The second part of this master thesis project concerns the design of two bandgap reference circuits, a low-voltage and a high-voltage variant. A BGR circuit is used to provide a stable voltage reference. This reference should be almost constant with temperature and supply voltage. The first BGR is used as a reference voltage for the control part of the DC-DC converter. It is supplied with 1.8 V and outputs a reference of 600 mV. The second one serves as a reference voltage for all the linear regulators placed in chain in the DC-DC converter. It works with supply voltages between 12 V and 55 V and has an output voltage of 1.2 V. As in the design of the current references, the low-voltage bandgap reference circuit includes only low-voltage transistors, whereas the high-voltage one implies the use of also high-voltage transistors that withstand a V_{ds} up to 30 V.

4.1 Choice of the configuration and working principle

In order to generate a suitable reference voltage that is tunable according to the application, the conventional OPAMP-based BGR circuit (whose schematic is presented in Figure 4.1) cannot be used, since it outputs a reference which is the sum of two voltages and cannot be tuned.

The expression of the output voltage can be derived by analyzing the circuit. The current that flows in a diode can be expressed as a function of the voltage:

$$I_{diode} = I_s \cdot (e^{\frac{qV_{diode}}{kT}} - 1) \simeq I_s \cdot e^{\frac{qV_{diode}}{kT}}, \tag{4.1}$$

with $\frac{kT}{q} = V_T$ and $V_{diode} \gg V_T$. Considering the $\frac{W}{L}$ to be the same for M1 and M2, the currents in the two diodes I_{D1} and I_{D2} are equal, and V_{D1} and V_{D2} can be expressed as:

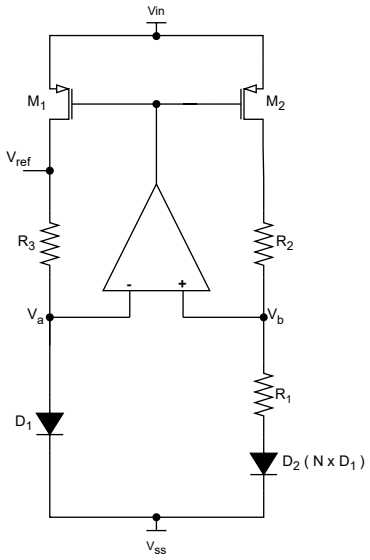


Figure 4.1: Schematic of the conventional OPAMP-based bandgap reference circuit.

$$V_{D1} = V_T \cdot ln\left(\frac{I_{D1}}{I_S}\right), \tag{4.2a}$$

$$V_{D2} = V_T \cdot ln\left(\frac{I_{D2}}{I_S}\right) = V_T \cdot ln\left(\frac{I_{D1}}{N \cdot I_S}\right). \tag{4.2b}$$

The high gain OPAMP forces its input nodes to the same voltage, hence $V_a = V_b$ that means $V_{D1} = V_{D2} + I_{R1}R_1$. As a consequence I_{R1} is equal to:

$$I_{R1} = \frac{V_{D1} - V_{D2}}{R_1} = \frac{V_T ln(N)}{R_1}. \tag{4.3}$$

The circuit output voltage is therefore:

$$V_{ref} = V_{D1} + I_{R1}R_3 = V_{D1} + \frac{R_3}{R_1}V_T ln(N) \tag{4.4}$$

In this case, V_{D1} has a negative TC of about -1.85mV/°C, extracted from simulations, whereas V_T has a positive TC of 0.086mV/°C. Consequently, the Temperature Coefficient of V_{ref} can be zeroed choosing the appropriate resistor ratio. In this way, V_{ref} can be only a fixed value and cannot be tuned. In order to introduce a further degree of freedom on its value and make it suitable for different applications, resistances R_2 and R_3 are moved in parallel to the diodes branches. In this way, the output reference voltage is generated through the sum of two currents, not two voltages anymore as in the conventional circuit. The advantage is that the conventional output voltage equation is multiplied by a further factor that can be used to tune its value. Figure 4.2 shows the schematic of the chosen topology [13].

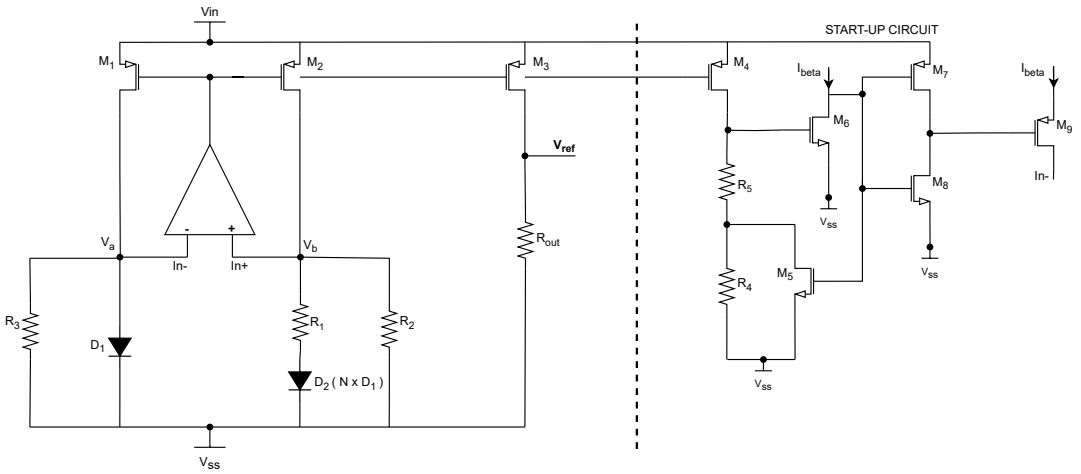


Figure 4.2: Circuit schematic of the employed OPAMP based bandgap reference circuit with its start-up circuit.

Also in this case $R_2 = R_3$ and $V_a = V_b$ thanks to the presence of the OPAMP, $I_{R2} = I_{R3}$ and therefore $I_{D1} = I_{R1} = NI_{D2}$. Due to the current mirror configuration, also currents in M_1, M_2, M_3 are the same. Given these considerations, looking only at the branches connected to the positive input of the OPAMP, the Complementary To Absolute Temperature (CTAT) and Proportional To Absolute Temperature (PTAT) branches can be distinguished:

- The branch with the D_2 diode is the PTAT branch, since in Equation 4.3 only the positive TC of V_T contributes.
- R_2 branch instead is the CTAT one, since $I_{R2} = \frac{V_{D1}}{R_2}$ and as mentioned before V_{D1} has a negative TC.

Then, the expression of V_{ref} is derived:

$$V_{ref} = R_{out} \cdot I_{M3} = R_{out} \cdot (I_{R1} + I_{R2}) = R_{out} \left(\frac{V_T ln(N)}{R_1} + \frac{V_{D1}}{R_2} \right). \tag{4.5}$$

Equation 4.5 shows that fixing the ratio between R_1 and R_2 to minimize the variations with temperature, the value of V_{ref} can be tuned by adjusting the output resistance (R_{out}).

4.2 Sizing

General specifications for the bandgap reference circuit are:

- Output reference voltage V_{ref}: the desired reference voltage is 600 mV for the low-voltage bandgap circuit, while it is 1.2 V for the high-voltage version.
- Temperature coefficient TC: the output voltage should feature a behavior with temperature variations as constant as possible. The TC should be at most less then 1% of relative variation.
- Power Supply Rejection (PSR): the circuit should have a minimum PSR of 50dB at low frequencies, to ensure the reference voltage is not influenced too much by the variations on the supply voltage. Furthermore, the specified value of PSR should not be exceeded around the switching frequency of the converter, which is between 1 MHz and 5 MHz.
- Mismatch variation: the circuit should also withstand mismatch variations, without exceeding 2-3% of relative variation.
- SEE robustness: the circuit must be stable in the presence of single events. It means that V_{ref} also in this case should not exceed 2-3% of relative variation.

Transistors M_1, M_2, M_3, M_4 are in a current mirror configuration, thus they have to be matched to one another. Their length is fixed at 3 µm to improve matching and achieve better mirroring, ensuring that the copied current accurately follows the input current. In general, to reduce mismatch effects their area must be kept from being too small, thus their width is set to 20 µm. This choice also allows them to work in the strong inversion region.
The only other important design consideration is the sizing of the resistances to make the behavior of the reference voltage as constant as possible with temperature. As can be deducted from Equation 4.5, V_{ref} depends only on the ratio between resistances. Therefore, if resistors of the same kind and multiple of the same segment (with fixed dimensions of length and width) are chosen, the temperature coefficient of the reference voltage should not depend on the TCR of the resistors. A segment of 2 kΩ is used as the basic unit, with $W = 0.5$ µm and $L = 161$ µm.
At this point, the only way to tune V_{ref} TC is changing the value of the resistances on the PTAT and CTAT branches. In this way, the values of the PTAT and CTAT currents is modified until they compensate each other. Then, the output resistance is adapted to mantain the correct absolute value of the reference voltage. The best combination is found through simulations and it is reported in Table 4.1.

R_1 $[k\Omega]$	$R_{2,3}$ $[k\Omega]$	R_{out} $[k\Omega]$
8.7	80	26

Table 4.1: Summary of the selected values for the resistances of the BGR circuit.

4.3 Core Bandgap Reference

4.3.1 OPAMP

To keep V_a equal to V_b, an OPAMP circuit is designed. This is an important step to make the bandgap circuit work in the correct way. Specifications for the circuit are:

- DC Gain: the circuit must exhibit a DC gain of at least 80dB.
- Offset voltage: the voltage difference between the two inputs of the amplifiers should be minimized, keeping the 3σ variation of the offset voltage lower than $\pm$ 2 mV.
- Loop gain stability: to ensure a good stability of the circuit, the phase margin should remain above 45 degrees in all conditions.

Comparison between Symmetric and Folded Cascode OTA

A comparison is performed between two different configurations of an operational amplifier. In both cases, it is a two-stages amplifier: the first stage is a PMOS differential pair and the second stage is a PMOS common source amplifier to allow maximum swing at the output. In this way, a second low frequency pole is added to the circuit, which makes it more difficult to stabilize. A Miller capacitance is then introduced for frequency compensation. The bias current for the circuit is taken from the previously designed core beta multiplier. In order to choose the proper configuration for the first amplification stage, the comparison between a symmetric and a folded cascode OTA has been carried out (see Figure 4.3).

In both cases, the OTA has a cascode configuration chosen to boost the gain. The same simulations are performed for both configurations using the same total area of transistors and eventually the folded cascode configuration is selected. The symmetric configuration has more transistors that must be kept large for the offset minimization, therefore for the same transistors area the offset is significantly better in the folded cascode OTA configuration. With Monte Carlo simulations, symmetric OPAMP reaches values of 3σ offset voltage greater than $\pm$ 15 mV compared to the $\pm$ 3 mV of the folded one. This parameter is particularly important for this design, since the offset voltage strongly impacts the value of the reference voltage of the BGR circuit.

The complete schematic of the final chosen OPAMP is shown in Figure 4.4.

Small signal analysis

Figure 4.5 shows the small signal schematic of the folded cascode OTA.

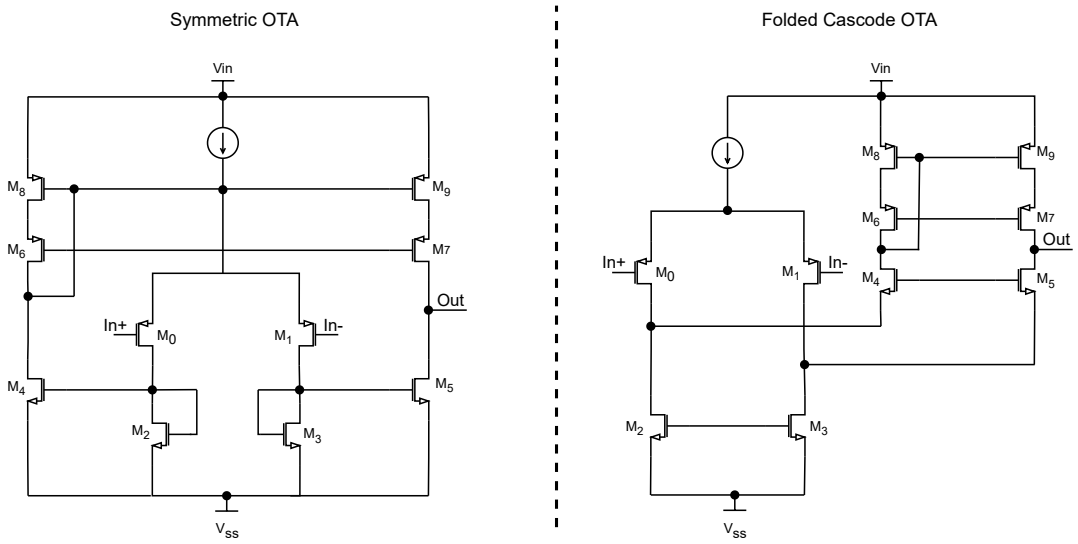


Figure 4.3: Circuit schematics of two different topologies for a cascode OTA. In particular, on the left the symmetric cascode configuration is depicted, on the right the folded cascode counterpart is proposed.

The output resistance R_{out} is the parallel between R_{out1} and R_{out2}:

$$R_{out1} = \frac{1}{g_{ds9}}\left(1 + \frac{g_{m9}}{g_{ds11}}\right) \simeq \frac{g_{m9}}{g_{ds9} \cdot g_{ds11}}, \tag{4.6a}$$

$$R_{out2} = \frac{1}{g_{ds7}}\left[1 + \left(\frac{1}{g_{ds5}} \parallel \frac{1}{g_{ds3}}\right) g_{m7}\right] \simeq \frac{g_{m7}}{g_{ds7}} \cdot \left(\frac{1}{g_{ds5}} \parallel \frac{1}{g_{ds3}}\right). \tag{4.6b}$$

Since typically in a transistor $g_m \gg g_{ds}$, for an overall study all transconductances g_{mx} and drain-source conductances g_{dsx} can be approximated to the same value of g_m and g_{ds}. Thus, the expressions can be re-written as:

$$R_{out1} = \frac{g_m}{g_{ds}^2} = g_m r_0^2, \tag{4.7a}$$

$$R_{out2} = \frac{2g_m}{g_{ds}^2} = g_m \frac{r_0^2}{2}, \tag{4.7b}$$

and R_{out} of the OTA becomes then:

$$R_{o,1} = R_{out1} \parallel R_{out2} \simeq \frac{1}{3} r_0^2 g_m. \tag{4.8}$$

As it can be seen from Equation 4.8, with the cascode configuration the Low Frequency (LF) gain $A_{0,1}$ of the OTA is boosted compared to a conventional OTA, since it is proportional to r_0^2 instead of only r_0. The LF gain results then

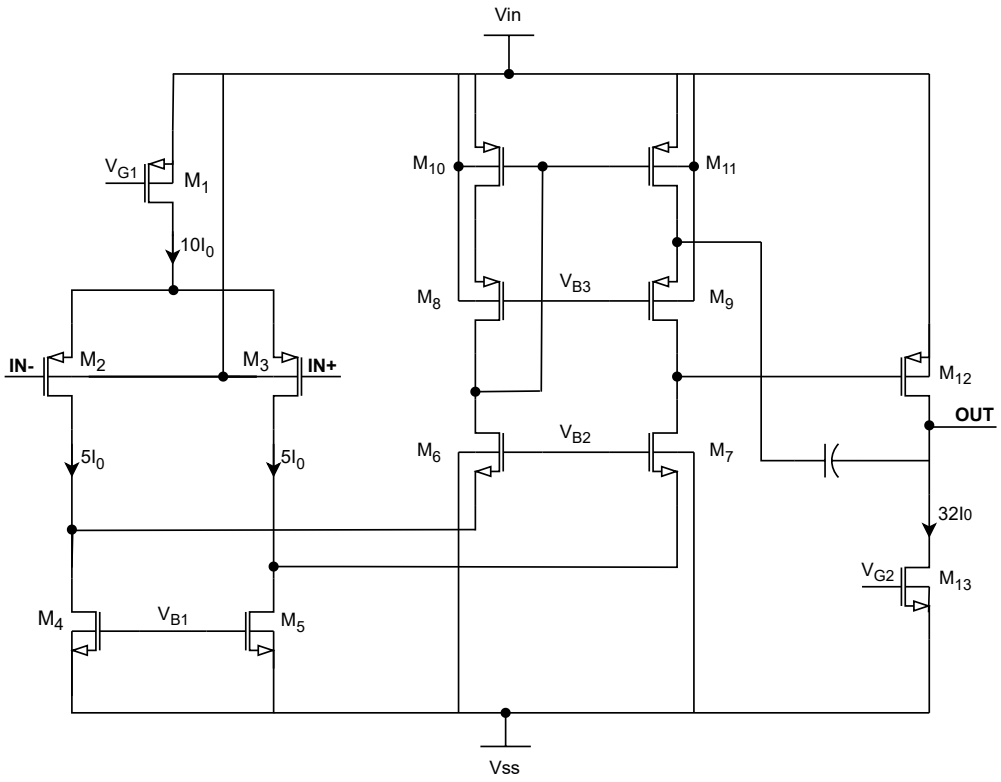


Figure 4.4: Circuit schematic of the definitive low-voltage folded cascode OPAMP.

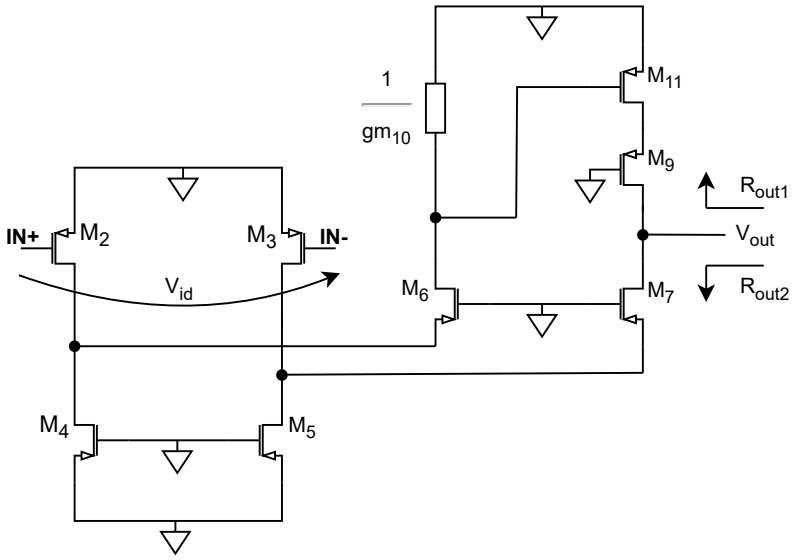


Figure 4.5: Small signal folded cascode OTA circuit schematic.

$$A_{0,1} = \frac{V_{out}}{V_{id}} = g_{m2,3} \cdot R_{o,1}. \tag{4.9}$$

Including also the common source stage, the gain $A_{0,1}$ is multiplied by the common source gain $A_{0,2}$, which is:

$$A_{0,2} = g_{m12} \cdot r_{012} \parallel r_{013} \simeq g_m \frac{r_0}{2}. \tag{4.10}$$

For a frequency analysis of the circuit, a simplified small signal model of the two-stages OPAMP is represented in Figure 4.6.

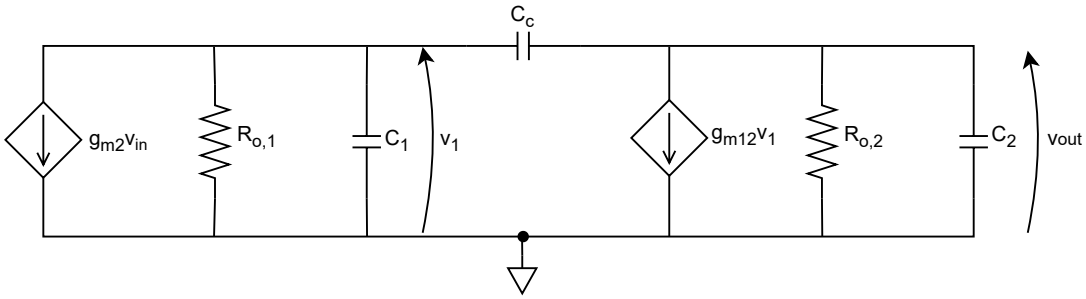


Figure 4.6: Small signal two-stages OPAMP circuit schematic.

With the addition of the common source amplification stage, the circuit becomes a multi-pole system since it introduces another high impedance node. It is then necessary to compensate adding a Miller capacitance C_c between the output of the OTA and the output of the common source. The idea is creating a large capacitance $C_c \cdot A_{0,2}$ by Miller effect at the output of the OTA, which implies the shift of the first pole to lower frequencies and also the second pole to higher frequencies (pole splitting). Writing the nodal equations at nodes 1 and 2:

$$\text{Node 1: } sC_c(v_1 - v_{out}) = -g_{m2}v_{in} - \left(\frac{1}{R_{o,1}} + sC_1\right) v_1. \tag{4.11a}$$

$$\text{Node 2: } sC_c(v_1 - v_{out}) = g_{m12}v_1 + \left(\frac{1}{R_{o,2}} + sC_2\right) v_{out}. \tag{4.11b}$$

Solving Equations 4.11a and 4.11b, the transfer function can be derived:

$$\frac{v_{out}}{v_{in}} = A_{0,1} \cdot A_{0,2} \cdot \frac{1 - s\frac{C_c}{g_{m12}}}{1 + s\left[\frac{(C_2+C_c)}{g_{o,1}} + \frac{(C_1+C_c)}{g_{o,2}} + \frac{C_c g_{m12}}{g_{o,1}g_{o,2}}\right] + s^2 \frac{(C_1C_c+C_1C_2+C_2C_c)}{g_{o,1}g_{o,2}}}, \tag{4.12}$$

where $g_{o,1}$, $g_{o,2}$ are respectively equal to $\frac{1}{R_{o,1}}$, $\frac{1}{R_{o,2}}$. Some terms can be neglected since $\frac{(C_2+C_c)}{g_{o,1}}$, $\frac{(C_1+C_c)}{g_{o,2}} \ll \frac{C_c g_{m12}}{g_{o,1} g_{o,2}}$ and typically $C_1 \ll C_2$, C_c. Given these considerations, the two poles of the system can be derived:

$$f_{p1} = \frac{g_{0,1} \cdot g_{0,2}}{2\pi \cdot C_c \cdot g_{m12}}, \tag{4.13a}$$

$$f_{p2} = \frac{g_{m12}}{2\pi \cdot C_2}. \tag{4.13b}$$

The gain-bandwidth product can thus be written as:

$$GBW = A_0 \cdot 2\pi f_{p1} = \frac{g_{m2}}{C_c}. \tag{4.14}$$

In this way also a resistance in series to the capacitance would be needed because C_c introduces also a positive zero that must be avoided:

$$f_z = \frac{g_{m12}}{2\pi \cdot C_c}. \tag{4.15}$$

Since the employed OTA has a folded cascode configuration, the capacitance can be connected to the node between the two PMOS M_{11} and M_9, so that the feed-forward path will see a high impedance node (drain of M_9), whereas the feedback path a low impedance node (source of M_9). In this way, the feed-forward is avoided and the positive zero eliminated without the addition of a resistance.

Sizing of the amplifier

First of all, fixing $GBW \simeq 3.5\,\text{MHz}$ and Miller capacitance not higher than 5 pF, it is possible to derive the transconductance of the differential pair from Equation 4.14, $g_{m2,3} = GBW \cdot C_c = 110\,\mu\text{S}$. Fixing the current to $10I_0$, where I_0 is the output current of the current reference circuit, the inversion factor is approximately equal to 4, indicating that the differential pair works in moderate inversion. This is a good trade-off becuase strong inversion operation would imply a lower area and higher gain but weak inversion helps to reduce mismatch effects between the transistors. It is found that such a performance can be achieved with a W/L ratio equal to 28. From the topology of the bandgap reference circuit it is known that the output capacitance is $C_2 \simeq 2\,\text{pF}$. In order to ensure stability in the system the condition $f_{p2} \geq 3GBW$ must be satisfied, then f_{p2} is fixed to $4GBW$. Using Equation 4.13b g_{m12} is calculated to be equal to $176\,\mu\text{S}$, which leads in this case to a W/L ratio of 160. Once fixed g_{m12}, lengths of the transistors M_{12}, M_{13} must be appropriately chosen since they are strictly related to the gain of the second stage. The folded cascode stage is sized to achieve a gain of 70dB for the first stage. Therefore, the lengths of M_{12}, M_{13} are set to $1\,\mu\text{m}$ since they are not needed to be excessively large. In this way, a gain of 30dB is obtained for the second stage, and the total gain of the OPAMP reaches 100dB.

Amplifier simulations

The frequency behavior of the designed OPAMP is simulated and the results are reported in Figure 4.7 and Figure 4.8. Open-loop gain and phase are simulated for three different temperatures (−30°C, 27°C, 100°C) and three different supply voltages (1.6 V, 1.8 V, 2 V). Changing the supply voltage both loop gain and phase remain almost constant (same color in the graphs). Increasing temperature the Loop gain presents a slight decrease, but the phase margin is almost the same so it does not influence the stability of the circuit.

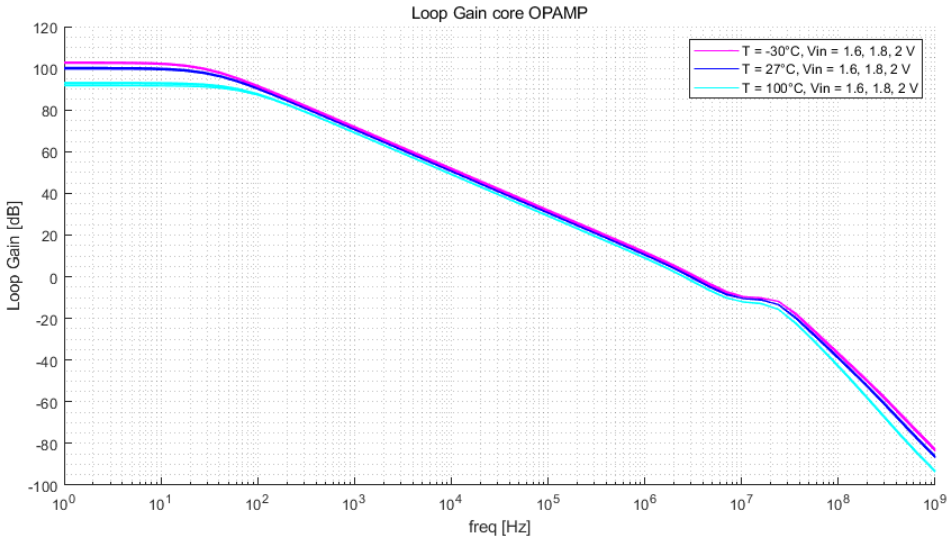


Figure 4.7: Open-loop gain of the designed OPAMP.

Figure 4.9 shows instead Monte Carlo simulations on the variations of the offset voltage of the developed OPAMP due to mismatch. The simulations are made of 200 runs at room temperature and 1.8 V supply voltage. Green area corresponds to an offset lower than 2 mV as the specifications require and almost all the samples satisfy this requirement.

4.3.2 Start-up circuit

A bandgap reference circuit needs a startup circuit in order to ensure that the desired operating point is obtained, avoiding that the ouput of the bandgap voltage reference circuit is stuck at zero. The start-up circuit designed for this block is shown on the right part of Figure 4.2. This circuit takes the current of the current reference (I_{beta}) to bias transistors M_6 and M_9. At the beginning, when the power is turned on the supply voltage is still low so there is no current flowing in the branches and transistor M_6 is switched off. Consequently, the input of the inverter composed

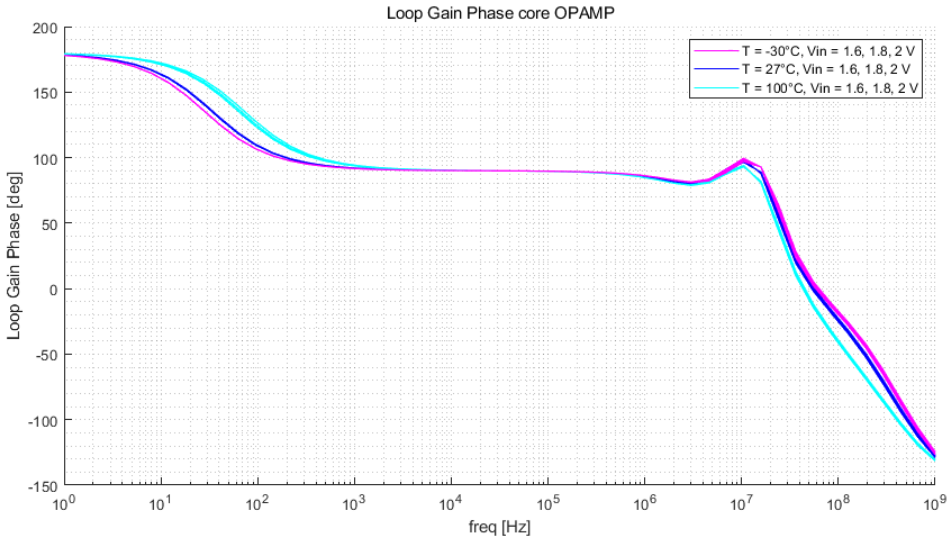


Figure 4.8: Open-loop gain phase of the designed OPAMP.

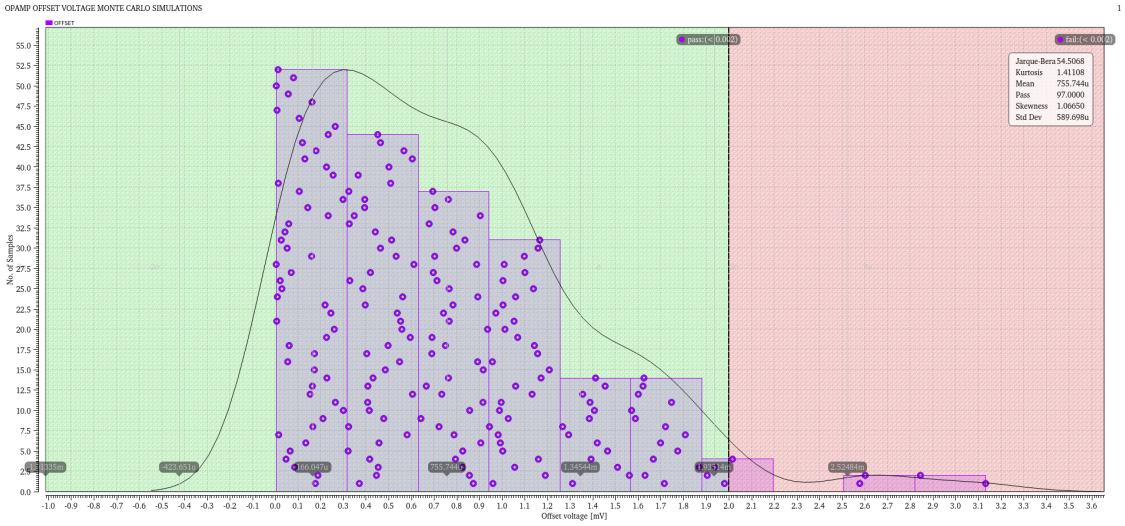


Figure 4.9: Monte Carlo mismatch simulations of the low-voltage OPAMP offset voltage. The absolute value of the offset is shown. 200 runs at room temperature with supply voltage of 1.8 V are performed.

of transistors M_7 and M_8 is high, which means that gate of M_9 is low. Hence, the PMOS transistor is on and inject current to the negative input of the OPAMP. Once the circuit reaches the steady-state, the situation is reversed and transistor M_9 is turned off, thus it stops the injection. Whenever the reference voltage were to lower under a certain threshold, transistor M_6 would switch off again in order to restart the injection. Since random fluctuations could make it switch off even

if there is no need of inject current, a hysteresis system is built through transistor M_5: at the beginning it is switched on, so it short circuits resistance R_4. Then, at steady-state resistance R_4 adds to R_5, preventing M_6 to become operational in presence of only a small fluctuation.

4.3.3 Trimming circuits

In order to precisely adjust the output voltage to a desired value, trimming circuits are employed in BGR circuits. Here, trimming is used also to adjust the temperature coefficient of the bandgap reference voltage. The purpose is allowing an accurate selection of the output voltage and of the temperature coefficient in the test phase. Designing the circuit in a customizable way, the BGR could work with the exact output voltage characteristics previously established by specifications despite simulation inaccuracies and process variations.
There are different techniques to perform trimming on a circuit, here a digital method is employed. Both output resistance and resistances on PTAT and CTAT branches effective values are set by means of external digital control signals. In principle output resistance R_{out} is tuned to adjust the value of the output voltage whereas resistances R_1, R_2, R_3 (see Figure 4.2) are responsible for the tuning of the Temperature Coefficient. Actually, as it can be seen in Equation 4.5, the values of R_1 and $R_{2,3}$ affect also the value of the reference voltage, therefore a combination of the two circuits is necessary even if only a temperature adjustment is needed.
In particular, three different trimming circuits are added to the BGR schematic (see Figure 4.10), each composed by a series of resistances controlled by the switches.

Seven different external digital signals are used, four for the output resistance tuning (O_1, O_2, O_3, O_4) and three for the TC tuning (T_1, T_2, T_3). Every signal controls an NMOS switch in parallel to a resistance. In this way, if the digital value is "1" the resistance is short-circuited. The series of resistances have binary weighted values in order to get a linear scale of possible values with binary signals. Tables 4.2 and 4.3 summarize all possible values that the trimming resistances can assume, according to the binary code of the related switches.

In principle only one of R_1, $R_{2,3}$ could be adjusted to tune the temperature behavior of the reference voltage. However, changing both resistances at the same time but in opposite direction allows limiting the impact on the reference voltage absolute value. For this reason temperature digital signals (T_1, T_2, T_3) control the value of $R_{2,3}$ and inverters are used to swap their value to control the value of R_1.

Tuning is permitted in both directions, thus the binary values of the digital signals that correspond to the ideal case are in the middle, as it can be seen in Table 4.4.

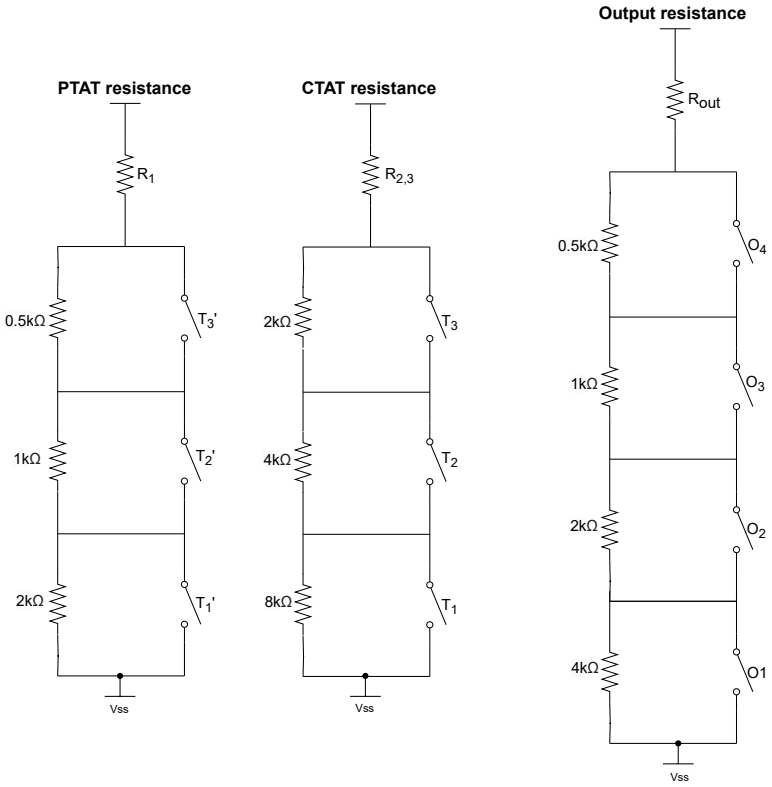


Figure 4.10: Trimming circuits schematic implemented to tune resistances R_1, $R_{2,3}$, R_{out} in the implemented BGR circuit.

4.3.4 Single events circuit hardening

Simulations performed with the injection of current on the sensitive nodes as described in subsection 2.2.2 demonstrate that certain nodes in the circuit require a SEE protection. As discussed in the mentioned section, there are various techniques to enhance circuit robustness to single events. In this particular case, R-C filters are implemented on the most sensitive nodes to ensure that the reference voltage stays within the 3% of relative variation. First of all, a large R-C filter is implemented on the output node, with a capacitance $C = 30\,\text{pF}$ and a resistance $R = 275\,\text{k}\Omega$, that means a cutoff frequency equal to 19 kHz. This already solves almost all the issues related to single events. Nevertheless, two further small R-C filter are added to the OPAMP current mirrors. In particular, in this scenario $R' = 10\,\text{k}\Omega$ and $C' = 500\,\text{fF}$, that results in a cutoff frequency of about 32 MHz. Figure 4.11 and Figure 4.12 show the implemented SEE-hard configurations. Results of the single events simulations are presented in the following section.

O_1	O_2	O_3	O_4	R'_{out} $[k\Omega]$
0	0	0	0	7.5
0	0	0	1	7
0	0	1	0	6.5
0	0	1	1	6
0	1	0	0	5.5
0	1	0	1	5
0	1	1	0	4.5
0	1	1	1	4
1	0	0	0	3.5
1	0	0	1	3
1	0	1	0	2.5
1	0	1	1	2
1	1	0	0	1.5
1	1	0	1	1
1	1	1	0	0.5
1	1	1	1	0

Table 4.2: Possible values of the trimming resistance R'_{out} in series to R_{out} in the implemented BGR circuit.

T_1	T_2	T_3	R'_1 $[k\Omega]$	R'_2 $[k\Omega]$
0	0	0	0	14
0	0	1	0.5	12
0	1	0	1	10
0	1	1	1.5	8
1	0	0	2	6
1	0	1	2.5	4
1	1	0	3	2
1	1	1	3.5	0

Table 4.3: Possible values of the trimming resistances R'_1 and R'_2 in series to R_1 and $R_{2,3}$ in the implemented BGR circuit.

T_1	T_2	T_3	O_1	O_2	O_3	O_4
0	1	1	0	1	1	1

Table 4.4: Ideal case values for all digital signals in the implemented BGR circuit.

4.3.5 Final core bandgap reference circuit simulations

Figure 4.13 shows the behavior of the output reference voltage of the BGR circuit versus temperature. The plot includes all simulated corners results. The variation of the voltage concerning a single band of values is pretty low, less than 0.5 mV in the nominal corner, and up to 5 mV considering the worst case, that is still in the specifications requirements.

PSR is simulated for different temperature and supply voltage conditions (Figure 4.14). It tends to decrease with both the temperature and the supply voltage. However, also in the worst case (Vin = 1.6 V, T = -30°C) it never drops under 49dB which is still acceptable.

Also, Monte Carlo simulations are carried out to check variations on the reference voltage caused by mismatch. As can be seen in Figure 4.15 there is a variation of ± 15 mV that corresponds to about 1% variation from the nominal value.

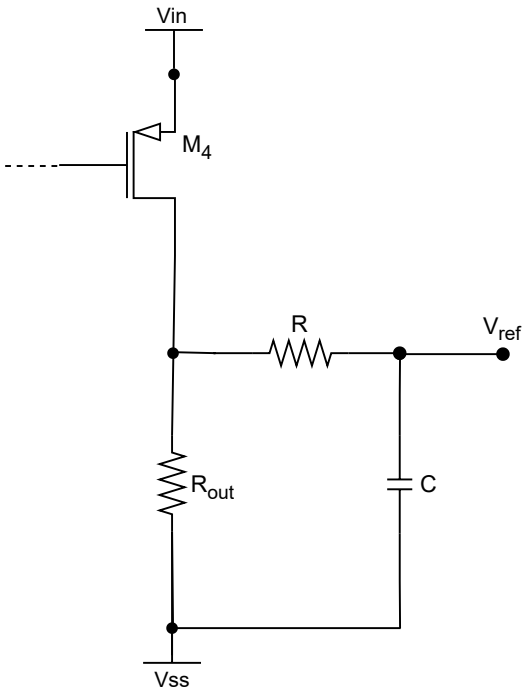


Figure 4.11: R-C filter implemented at the output of the BGR circuit for the single events hardening.

At the end, Single Event Effects are simulated using the SEE cell developed in subsection 2.2.2. In particular, it is checked that the reference voltage remains constant, with a maximum relative variation of about the 3%.

The reference voltage is controlled injecting current pulses in BGR, OPAMP and beta multiplier nets. As an example Figures 4.16 and 4.17 show the results of the BGR injection, for only significant nets. V_{ref} remains constant all along, without reaching ±5 mV of total variation.

4.4 High-Voltage bandgap reference

As for the current reference circuit, also the high-voltage version of the bandgap reference circuit is adapted from the low-voltage one. In this case, the desired reference voltage is increased to 1.2 V. Furthermore, the other specifications remain the same.

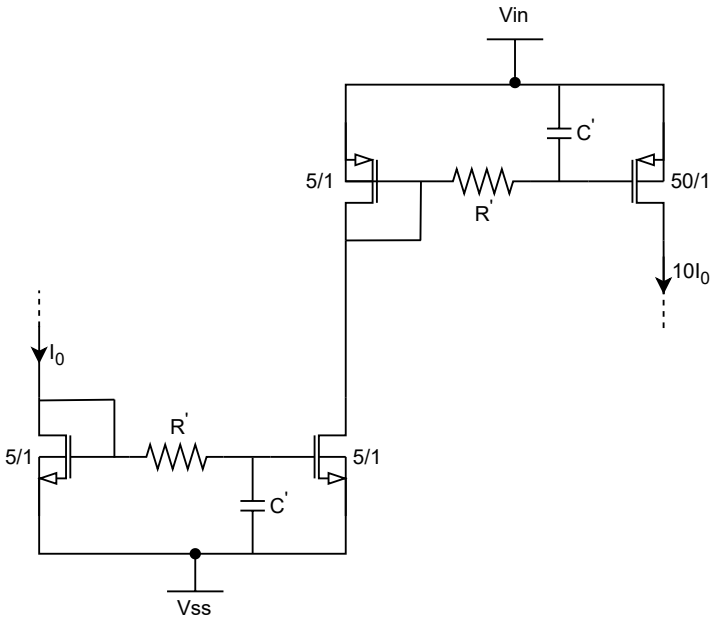


Figure 4.12: R-C filters implemented for the single events hardening of the OPAMP current mirrors. I_0 is the output current of the current reference circuit. Also, W/L ratios of the transistors are displayed in the figure.

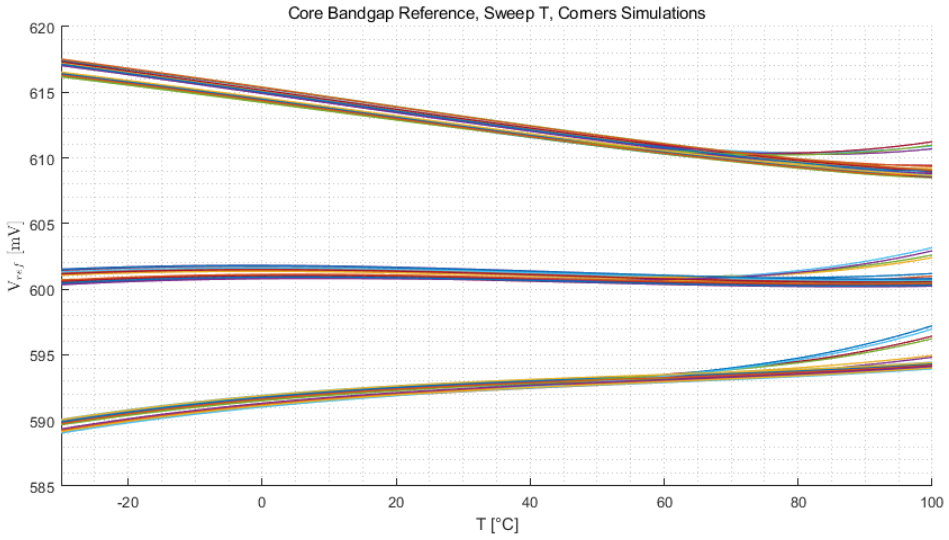


Figure 4.13: Reference voltage behavior of the low-voltage BGR circuit over a Temperature sweep from -30°C to 100°C. Process corners on transistors, resistors and capacitors and TID radiations corners are simulated.

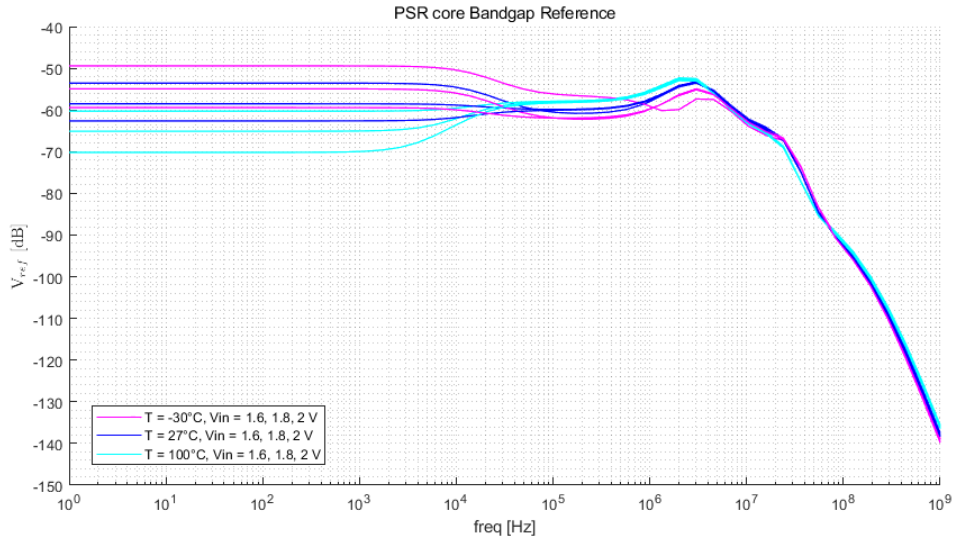


Figure 4.14: PSR of the reference voltage of the core BGR circuit. Results are shown for three different tempertures (−30°C, 27°C, 100°C) and three different supply voltages (1.6 V, 1.8 V, 2 V). Colors define the temperature of the simulation and supply voltage is lower for lower values of PSR.

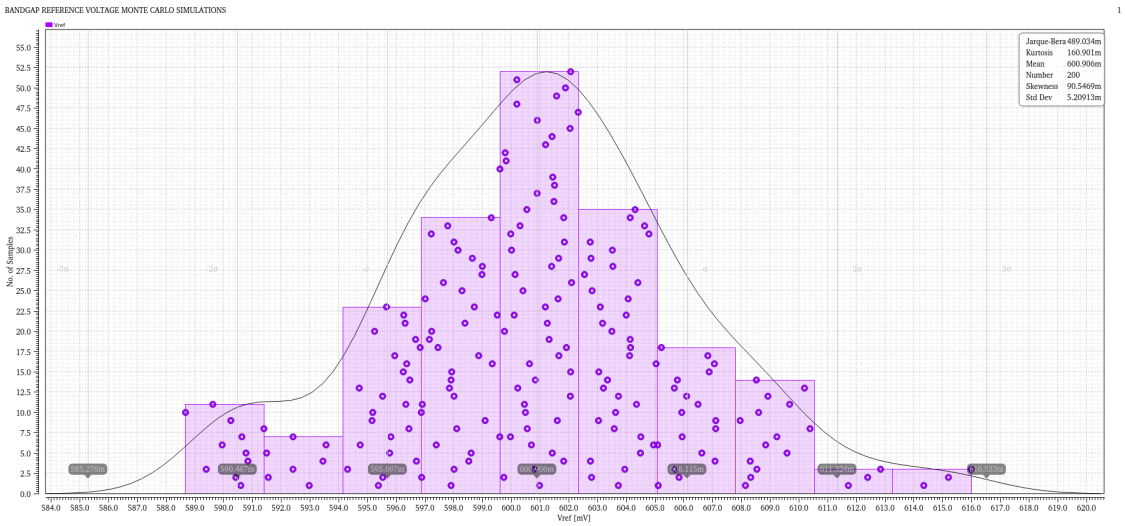


Figure 4.15: Monte Carlo mismatch simulations of the low-voltage BGR circuit output voltage. 200 runs at room temperature with supply voltage of 1.8 V are performed.

4.4.1 High-voltage OPAMP schematic

First of all, the schematic of the amplifier is adapted (Figure 4.18). In this case, the biasing current of the differential pair is taken directly from the high-voltage current reference circuit, without prior multiplication. Additional transistors ($LD_{2,4}$,

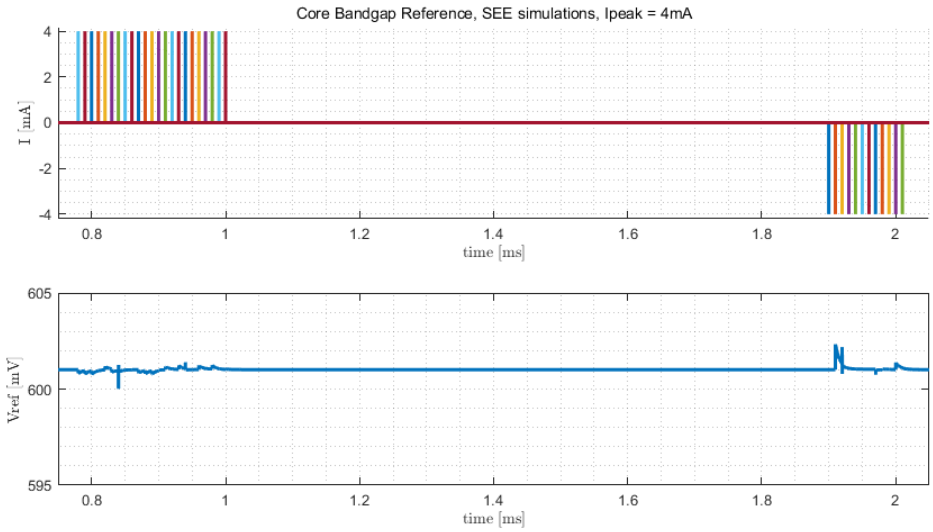


Figure 4.16: Reference voltage variations under Single Events current injection in significant nets of the BGR circuit. Here the current pulse has a peak of 4 mA. The simulation is performed at room temperature with a supply voltage of 1.8 V.

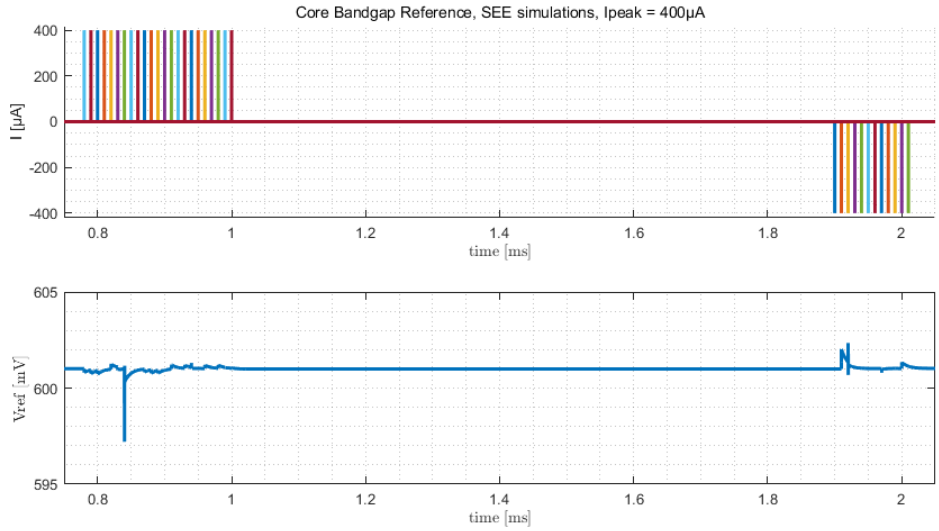


Figure 4.17: Reference voltage variations under Single Events current injection in significant nets of the BGR circuit.Here the current pulse has a peak of 400 µA. The simulation is performed at room temperature with a supply voltage of 1.8 V.

$LD_{1,3}$) are included to ensure protection from overvoltages of $M_{4,6}$ and $M_{5,7}$ respectively. $M_{8,10}$ do not need protection measures because they correspond to a diode-connected transistor configuration, whereas $M_{9,11}$ are safeguarded by diodes

$D_{1,2}$, which will be presented later. Furthermore, on the second stage $LD_{5,6}$ are introduced for M_{13} and the V_{DS} of M_{12} is clamped by means of diodes $D_{3,4}$. Transistors' sizing is kept unchanged with respect to the low-voltage amplifier. Concerning biasing voltages for the LDMOS transistors, the same biasing branches as the current reference circuit are utilized (see Figure 3.7). Besides offering a protection to the mentioned transistors, diodes D_{1-4} are useful in the start-up phase of the circuit to provide an alternative path to a low impedance node (V_{in}). In fact, when the power supply is switched on a small value of V_{DS} in the n-type LDMOS transistors (set by the models at around 100 mV) triggers the flow of a leakage current in the radiation corners. In this way, some current flows in the circuit before it has achieved its functional operation, that may result in an overshooting voltage on some nodes that brings transistors out of their SOA.

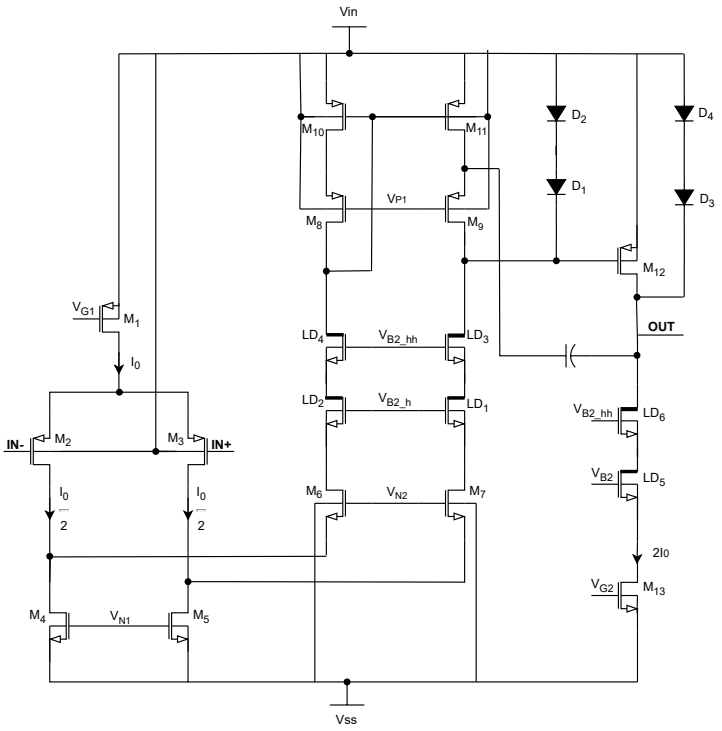


Figure 4.18: Circuit schematic of the employed high-voltage amplifier.

4.4.2 High-voltage bandgap reference circuit schematic

The left part of Figure 4.19 depicts the schematic of the high-voltage version of the voltage reference circuit. Also in this case transistors $LD_{1,2}$, $LD_{3,4}$, $LD_{5,6}$, $LD_{7,8}$ are included as clamps for M_1, M_2, M_3, M_4 respectively. Then, values of resistances are tuned to meet the new output voltage specification. Table 4.5 indicates the new resistance values.

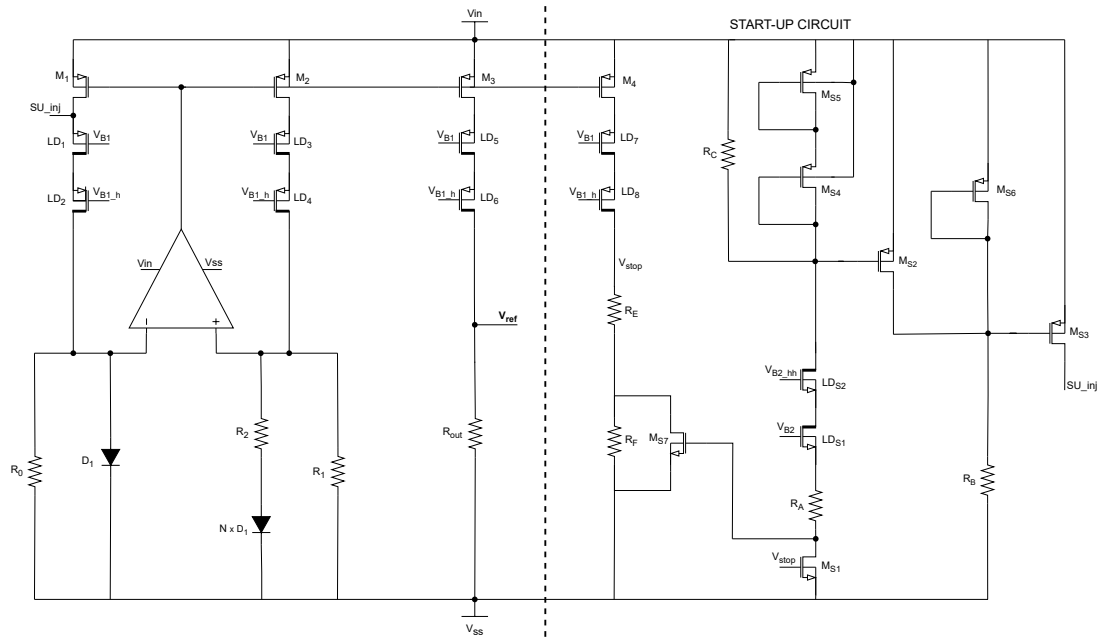


Figure 4.19: Schematic of the employed OPAMP based high-voltage bandgap reference circuit with its start-up circuit.

R_1 $[k\Omega]$	$R_{2,3}$ $[k\Omega]$	R_{out} $[k\Omega]$
8.6	79	52

Table 4.5: Summary of the selected values for the resistances of the high-voltage BGR circuit.

4.4.3 Start-up circuit

The updated start-up circuit, displayed in the right part of Figure 4.19, shares a similar topology to the one used for the start-up of the current reference circuit, previously described in subsection 3.4.3. Therefore, a repetitive description of the circuit's functionality and the sizing choices will be omitted. However, it should be noticed that in this case the hysteresis mechanism already implemented in the low-voltage version is replicated using resistance R_F and transistor M_{S7}. This hysteresis mechanism aids in ensuring a proper circuit functionality.

4.4.4 Final high-voltage bandgap reference circuit simulations

AC simulations are performed on the high-voltage block to ensure that the reference voltage is still stable with variations on the supply voltage (see Figure 4.20).

Changing both the power supply voltage and the temperature of the simulation, the DC value of the PSR varies between 105dB ad 130dB, meeting the specifications requirements. It is still acceptable also in the switching frequency range.

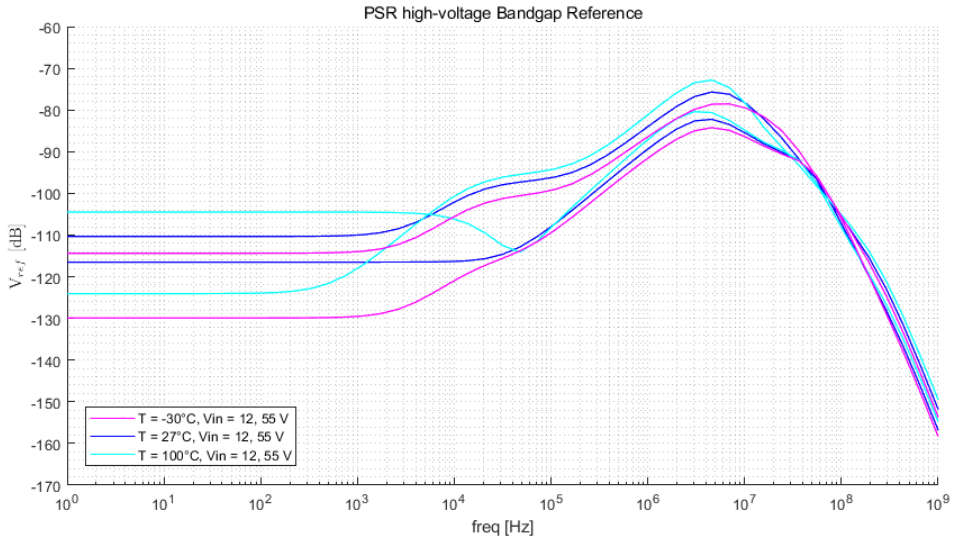


Figure 4.20: PSR of the reference voltage of the high-voltage BGR circuit. Results are shown for three different temperatures (−30°C, 27°C, 100°C) and two different supply voltages (12 V, 55 V). Colors define the temperature of the simulation.

Figure 4.21 illustrates the behavior of the reference voltage in response to temperature variation. The sweep simulation includes: standard process corners, TID radiation corners (TID = 200Mrad) and leakage radiation corners (peak in leakage current value). Leakage corners are almost superimposed to the standard ones, which is why they are not visible in the figure. Indeed, if the current on each branch is higher than the leakage current, it should not change anything in the DC simulations. Three bands for the three resistors' corners values are still perceptible although they tend to merge in the TID corners.

Additionally, Monte Carlo simulations are carried out for both the offset voltage of the new version of the OPAMP and the output reference voltage of the high-voltage bandgap reference circuit. Figure 4.22 shows that the offset voltage is a bit worse than the low-voltage Monte Carlo simulations, but it can still be considered acceptable.

Reference voltage varies between 1.16 V and 1.24 V that corresponds to the 2% of relative variation with respect to the nominal value (Figure 4.23).

To conclude, single events simulations are performed. Results are shown in Figure 4.24 and Figure 4.25, respectively for a current peak of 4 mA and 400 µA. Also in this scenario, the response of the reference voltage to the current injections is satisfactory, with an absolute variation of ±15mV in the worst case (1.3% relative

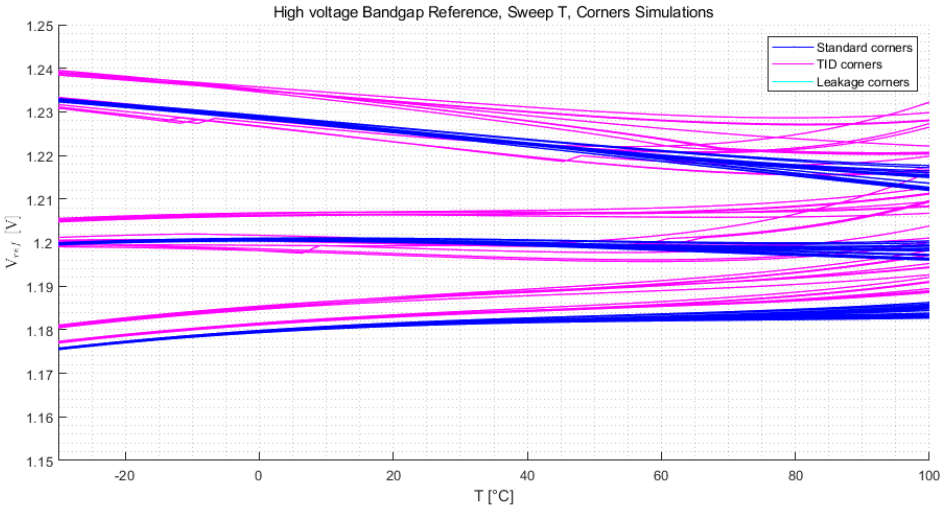


Figure 4.21: Reference voltage behavior over a Temperature sweep from −30°C to 100°C. Process corners on transistors, resistors and capacitors, TID radiations corners and peak leakage radiation corners are simulated.

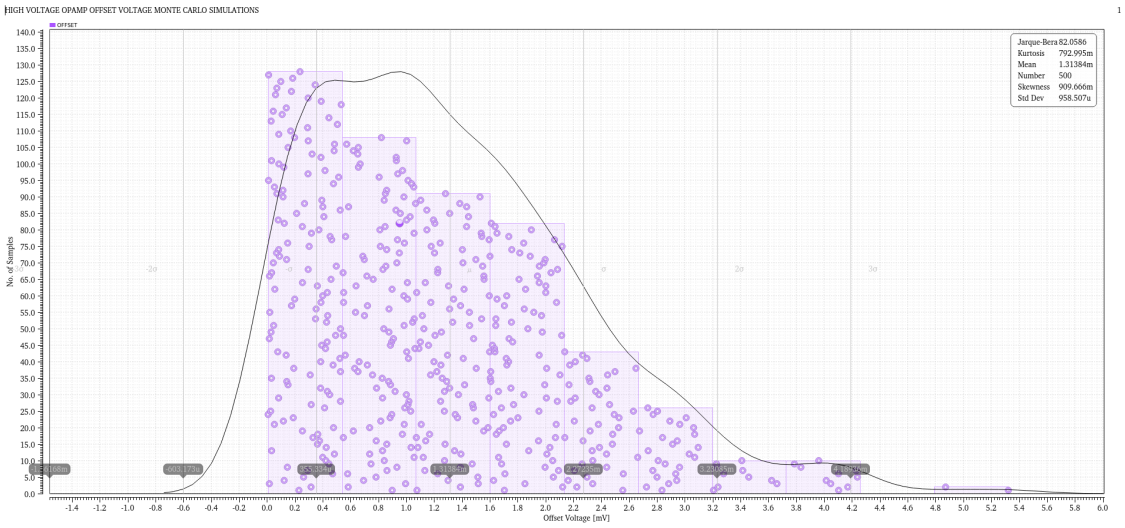


Figure 4.22: Monte Carlo mismatch simulations of the high-voltage OPAMP offset voltage. The absolute values of the offset are shown 200 runs at room temperature with supply voltage of 48 V are performed.

variation).

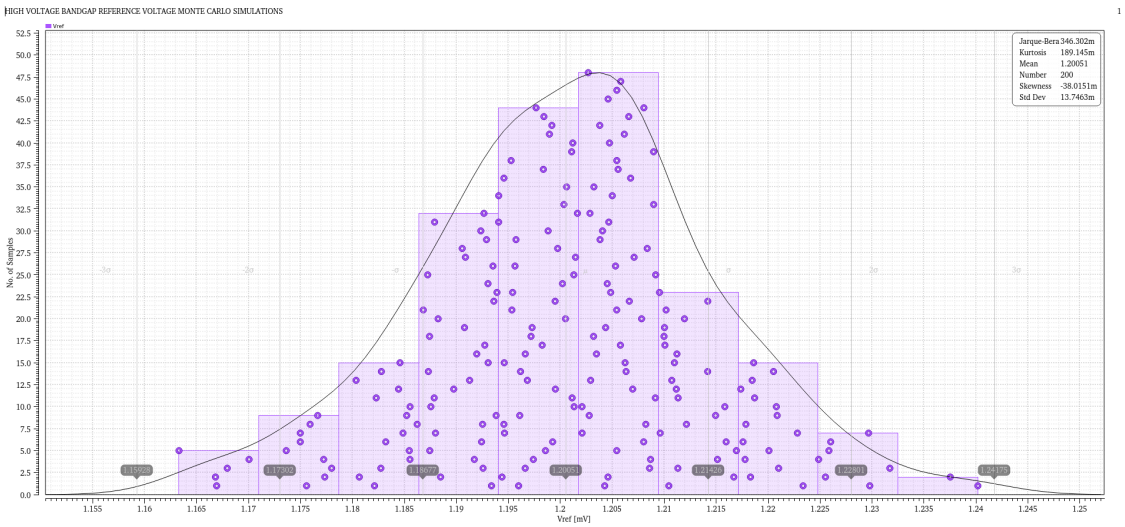


Figure 4.23: Monte Carlo mismatch simulations of the high voltage BGR output voltage. 200 runs at room temperature with supply voltage of 48 V are performed.

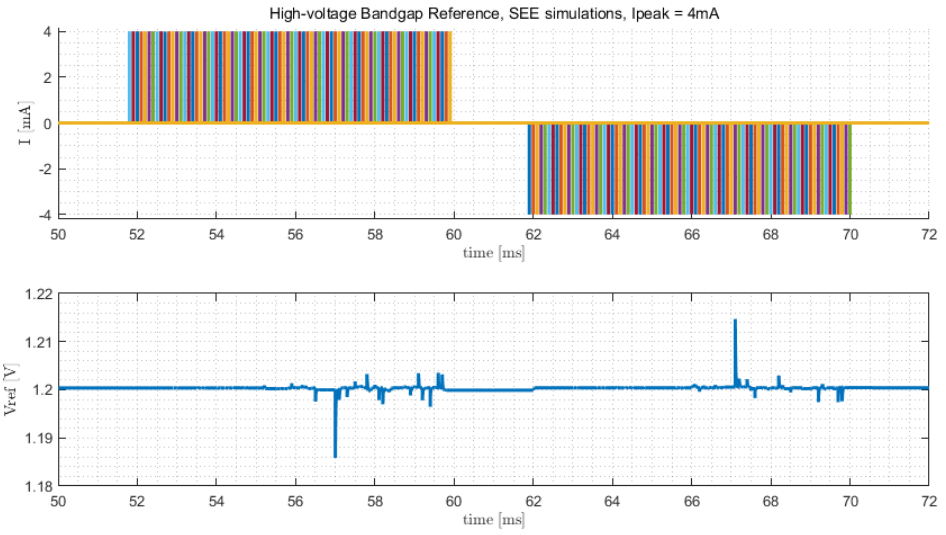


Figure 4.24: Reference voltage variations under Single Events current injection in significant nets of the high-voltage BGR circuit. Here the current pulse has a peak of 4 mA and a duration of 200ps. The simulation is performed at room temperature with a supply voltage of 48 V.

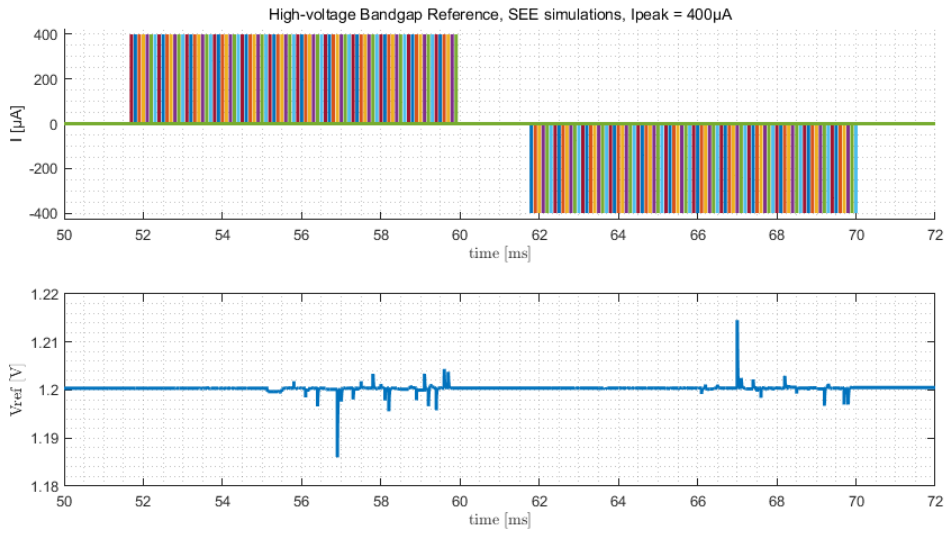


Figure 4.25: Reference voltage variations under Single Events current injection in significant nets of the high-voltage BGR circuit. Here the current pulse has a peak of 400 µA and a duration of $2ns$. The simulation is performed at room temperature with a supply voltage of 48 V.

Chapter 5

Conclusion

In conclusion, this thesis reports the design of radiation-tolerant current and voltage reference circuits. These circuits will be integrated into the controller of a buck DC-DC converter designed at CERN, which will be employed in the LHC upgrades.

Since the designed DC-DC converter will be situated close to the particles collision sites, the primary challenge of this project was ensuring the circuits' robustness to the harsh radiation environment. To address this, radiation models were developed to account for the effects of Total Ionizing Dose. Concerning 1.8 V-rated transistors, adjustments were made for three parameters in the model files: the threshold voltage V_{th}, the effective width W_{eff} and the effective length L_{eff}. Each of these modifications can be physically explained with the presence of traps in the different oxides employed in CMOS technology (the gate oxide, the spacers and the STIs). In this way, the modeled $I_D - V_D$ and $I_D - V_G$ characteristics fit almost perfectly the measured ones. On the other hand, also LDMOS transistors characteristics were modeled, in particular the leakage degradation in n-type devices. A Verilog-A block was also implemented to describe the transistor-like behavior of the parasitic FOXFET, under maximum TID and leakage conditions, respectively at 200Mrad and 1Mrad. Along with TID models, a tool composed of a Verilog-A cell together with a SKILL script to automatize the injection of single events in the circuits was developed. Using such tool, automatically all the nets are extracted from a given schematic of a cell under test. Then, the nodes are perturbed either by injection or withdrawal of current, based on the shape of an input current source. Thanks to these strategies, the simulation of transistors in radiation conditions was made possible, allowing to harden the circuit already in the design-phase.

The design flow started with the development of two current reference circuits. The first is a low-voltage circuit supplied at 1.8 V and with an output current of 2 µA. The second is a high-voltage version, fed by a supply voltage ranging from 12 V to 55 V and an output current of 20 µA. Both circuits were simulated over an

extensive set of corners including supply voltage, temperature and process changes on both active and passive devices. Radiation corners were also simulated for TID of 200Mrad and, exclusively for the high-voltage circuit, for the peak value of the radiation-induced leakage current. The output current remained stable in both circuits, never overcoming $\pm 5\%$ of relative variation from the nominal values.

Furthermore, two bandgap reference circuits were designed, one for low-voltage (1.8 V supply) and another for high-voltage (up to 55 V) applications. The first circuit is used to generate the reference voltage for the control part of the DC-DC converter. The high-voltage bandgap circuit instead provides a reference to the chain of linear regulators in the controller. Additionally, two OPAMP circuits are designed to be employed in the bandgap circuits. A two-stage amplifier is selected with a folded cascode configuration for the OTA, which proved to be the best solution for the minimization of the input offset. Also in this case, simulations of the circuits demonstrated that the reference voltage met the specifications in both low- and high-voltage circuits. In particular, at a fixed resistance process corner, the TC of the output voltage does not exceed the 1% of relative variation.

The project is still under development, with the layout of all blocks being designed. In the upcoming months, all other components required to complete the controller block of the buck converter will also be designed. Then, the circuits must be fabricated and tested to ensure their correct functionality, particularly in a radiation environment.

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Appendix A

SKILL code for the modeling of SEEs

The complete SKILL code used to automatize the process of generating injection current sources to test single events is reported below.

```
/*
SKILL script to extract the nets of a schematic and set
   them as inputs of a SEE injection cell.
Usage:
Load the SKILL code in CIW:
                        load "SEEinjection.il"
1) With the source schematic cellview open:
                        SEEinjection()
2) For a specific cellview referred by its name:
                        cv = dbOpenCellViewByType("
                           LibName" "CellName" "schematic
                           ")
                        SEEinjection(?cv cv )

Notes:
- Inputs of the second procedure should be adapted to the
    specific Library being used
- The modified SEE injection cell must be then copied and
    pasted in the schematic of interest
- !All the nets to be extracted must have a non-default
   name!

*/

procedure(SEEinjection(@key (cv geGetEditCellView()))
```

```
net_list = ""
tot_nets = 0
foreach(netId cv~>nets~>name ; get the name of all nets
   in the schematic
if( getchar(netId 1) != '\074 ; ignore multiple nets
   connected together ( <*X>net )
then                                          ; '\074 = \<
;addition to the list of nets
net_list = strcat(net_list netId)
net_list = strcat(net_list ",")
;total nets number update
if( getchar(netId strlen(netId)) == '\076       ;
   multiple nets ( net<0:X> ) '\076 = \>
then
str_to_add = strpbrk(netId ":")
str_to_add = substring(str_to_add 2 strlen(str_to_add)-2)
tot_nets = tot_nets + atoi(str_to_add) + 1
else
tot_nets = tot_nets + 1
) ; end if
) ; end if
) ; end foreach
; Since the SEE injection cell has 100 inputs, the
   remaining ones are left floating
sprintf(str_to_append "VSSfloat<0:%d>" 100-tot_nets-1)
net_list = strcat(net_list str_to_append)

; Change the labels of the inputs of the SEE injection
   cell with the list of nets just extracted
ChangeNetLabel("em_I4T" "schematic" "GR_SEE_INJECT_tb"
   net_list tot_nets) /******* LIBRARY NAME TO BE CHANGED
    *******/

) ; end proc

/*
The following procedure is used to change the label of
   the net inputs of the SEE injection cell.
INPUTS: library name, view name, cell name, new label for
    the inputs, total number of nets of the source cell
*!*!* The procedure works only if the net inputs have
   already a specified label *!*!*
```

```
*!*!* The labels of the nets "VSS" and "VSSfloat" must
   not be changed!!
*/
procedure(ChangeNetLabel(libName viewName cellName
   newLabel tot_nets)
let((cv libId cellId cellList newNet)
libId = ddGetObj(libName)
cellId = ddGetObj(libName cellName)
foreach(view cellId~>views
if( view~>name == viewName &&
(cv = dbOpenCellViewByType(libName  cellId->name view~>
   name "" "a"))
then
printf("\nOpened␣view␣%L␣from␣cell␣%L␣of␣library␣%L␣for␣
   edit.\n"
 cv~>viewName cv~>cellName cv~>libName) ; get the
    cellview with the correct view
foreach( net cv~>nets ; scrolling all the nets of the
   cell
newNet = dbMakeNet(cv net~>name)
dbMergeNet(newNet net)
 foreach( fig newNet~>figs
 when( fig~>objType == "label" ; if the net has already a
    label
myLabel = fig~>theLabel
if( substring(myLabel 1 4) == "VSSf" ; change the label
   attached with floating net connected to the remaining
   inputs
then
sprintf(str_float "VSSfloat<0:%d>" 100-tot_nets-1)
fig~>theLabel = str_float
else
if( myLabel != "VSS"
then
fig~>theLabel = newLabel ; change the label attached with
    net inputs
) ;if
) ;if
) ; end when
 ) ;end foreach
 ) ; end foreach
```

```
; change also the name of the resistance needed for the
   floating net
foreach( instance cv->instances
if( instance->cellName == "res"
then
sprintf(res_name "R0<0:%d>" 100-tot_nets-1)
instance->name = res_name
) ; end if res
) ; end foreach instances
dbCheck(cv)
dbSave(cv)
dbClose(cv)
);end if
);end foreach view
ddReleaseObj(libId)
);let
printf("Job␣Done...\n")
);proc
```