Politecnico di Torino

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Master's Degree in Electronic Engineering
Master's Degree Thesis

Analysis and design of a power converter for high-power density adapters

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A mia sorella,
per esserci sempre stata.

"C'è una forza motrice più forte del vapore, dell'elettricità e dell'energia: la volontà."
ALBERT EINSTEIN

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Chapter 1

Introduction

The growing demand to reduce the size of chargers/adapters for mobile electronic devices such as laptops, tablets, smartphones, etc., motivates the increasing interest in the research for the development of high-power density adapters. Another important need of today's society is to minimize the waste of energy. To guarantee this request, high efficiency adapters must be designed.

The most used circuit topology for this type of application is the conventional flyback power converter. It has been widely used for low power application due to its simple design, as it requires few components, low cost, and insulation feature. However, in this topology, switches operate in hard-switching mode resulting in increased switching losses and high electromagnetic interference (EMI) noise [1]. In this case, snubbers are needed to protect primary and secondary switches from voltage spikes and to reduce the EMI noise.

To overcome these problems, three main solutions have been presented in literature: Active Clamp Flyback converter, Asymmetrical Half Bridge Flyback converter and LLC resonant power converter [1][2][3]. All these circuit topologies can work under soft-switching mode making snubbers no more needed. Moreover, the dimensions of the electronic parts present in the power converters can be reduced by operating them at high switching frequency to reduce the size of the transformer, the volume of the capacitors and the size of the switches. As an example, Figure 1.1 shows the increase in power-density of adapters over the years [4].

To operate the converters at high switching frequency (i.e., larger than MHz), Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) devices are adopted because they are more suitable for these applications than Silicon MOSFETs and this help to improve the power-density as well as the performance of power converters.

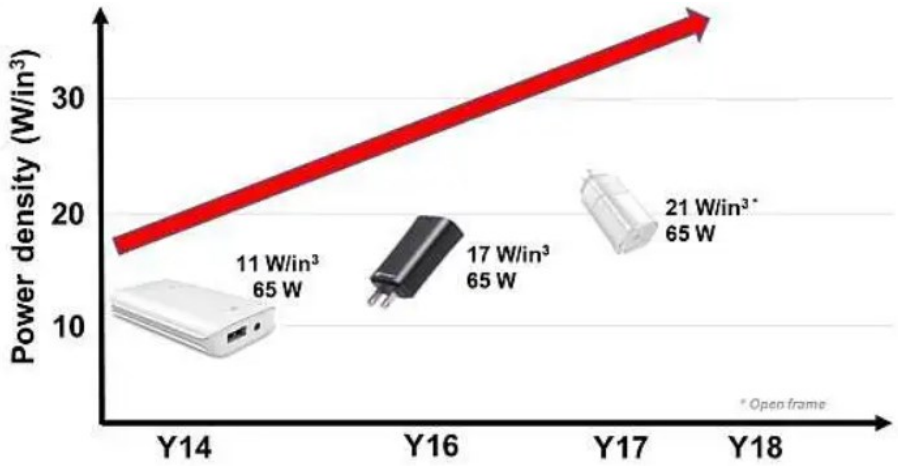


Figure 1.1: Power-density improvements in the adapters [4].

1.1 Aim of the thesis and outline

The aim of this thesis work is to identify the most suitable converter topology among the three solutions mentioned before and then, improve it in terms of efficiency, stress of the components, size reduction and control method.
To achieve this goal, a detailed study has been done on the available literature on the resonant power converters, on the most suitable devices to be used at high operating frequency and on the hard-switching and soft-switching techniques. Furthermore, several papers about the three power converter topologies previously mentioned have been studied. Then, these power converters have been analysed, designed, and simulated by using circuital simulators. As a next step, the best topology in terms of efficiency and stress of components has been selected and improved by exploiting a resonant scheme. Simulations with both ideal and real component models have been carried out to observe the behaviour of the current and voltage waveforms and to verify the theoretical analysis. Then, a programmable digital controller from Texas Instruments has been properly selected to implement the control method. Finally, a printed circuit board (PCB) prototype has been designed to validate the proposed approach.

The thesis is organized into six chapters where the first one contains this Introduction. In **Chapter 2**, the state of the art of the high power-density and high frequency adapter is presented. In particular, the main characteristics of the power converters used to implement these devices are described. More precisely, hard-switching, and soft-

switching techniques are reviewed, the operation of the resonant converters is analysed and the most used power converter topologies for adapters are presented.
In **Chapter 3**, the analyses of the converters are described in detail and the design for each topology with the obtained improvement is explained. After the design, simulations results that verify the theoretical analysis are shown and discussed.
In **Chapter 4**, the chosen power converter topology is discussed, highlighting the reasons for which it was preferred among the others, and the advantages obtained with respect to the other topologies. Then, the selected controller is described in details and adapted to the chosen topology.
In **Chapter 5**, the design of the PCB is reported starting from the implementation of the schematic up to the realization of the layout.
Finally, in **Chapter 6**, the conclusion of this thesis work together with the achieved results are discussed and possible future works are suggested.

Chapter 2

High power density and high frequency adapter: state of the art

In this chapter the main features of the power converters used to implement the high-power density and high-frequency adapter model will be presented. In particular, Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) techniques are reviewed, an overview of how resonant converters work and the most common power converter topologies are presented.

2.1 Soft switching

One of the most important issue and limit that affects any power converters is related to their switching losses. When the converter operates at high frequency, switching losses occur during the turn-on and turn-off of the switches present in the converter due to the superposition of the drain current flowing through the switch and drain-to-source voltage. Since during the turn-on and turn-off switching delays the drain current and the drain-to-source voltage are different from zero, the power dissipated by the switch is high and consequently this leads to an efficiency reduction. This mechanism of operating the switches is the so-called Hard Switching and in Figure 2.1 are depicted the voltage across the switch, the current flowing through it and the power.

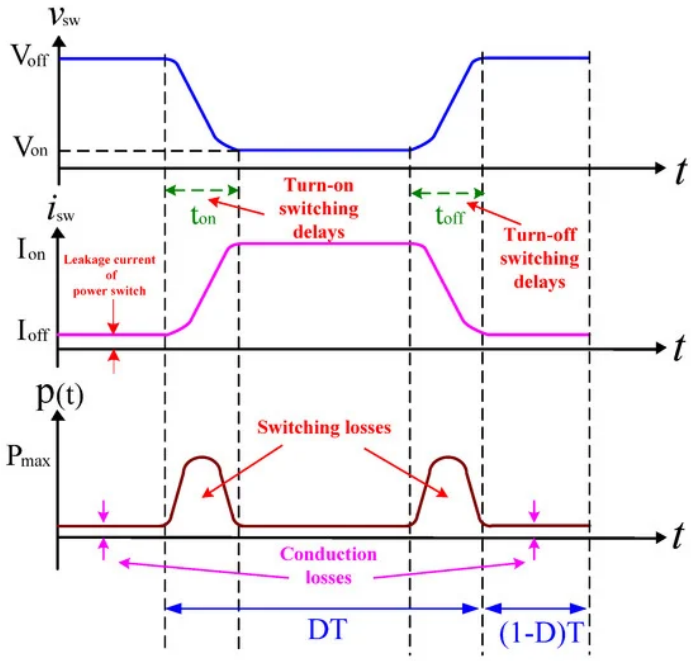


Figure 2.1: Hard switching waveforms.

The most significant components of switching losses in the transistor are the losses induced by the diode reverse recovery process and the losses related to the energy stored into the output capacitance of the transistor [5].

Resonant power converters overcome this limit related to the Hard Switching because they operate under the so-called Soft Switching mechanism.

The aim of the soft switching method is to attenuate the switching loss during turn-on and turn-off transitions avoiding the overlap between drain current and drain-to-source voltage. Furthermore, this portion of energy that with the hard switching method is lost, now it is recovered and transferred to the converter source or load with a consequently efficiency improvement. This is possible thanks to the presence of the resonant elements in the resonant power converter.

In fact, the resonant elements make possible the ZCS and the ZVS operation of the switch, in this way, switching losses are reduced or completely eliminated.

ZCS occurs during the turn-off and turn-on transitions when the current flowing through the switch is equal to zero when the drain-to-source voltage of the switch increases or decreases. Similarly, ZVS occurs during the turn-off and turn-on transitions when the drain-to-source voltage is equal to zero when the current flowing through the switch is different from zero.

An example of ZVS Buck converter [5] with the schematic of the circuit and both current and voltage waveforms is shown in Figure 2.2.

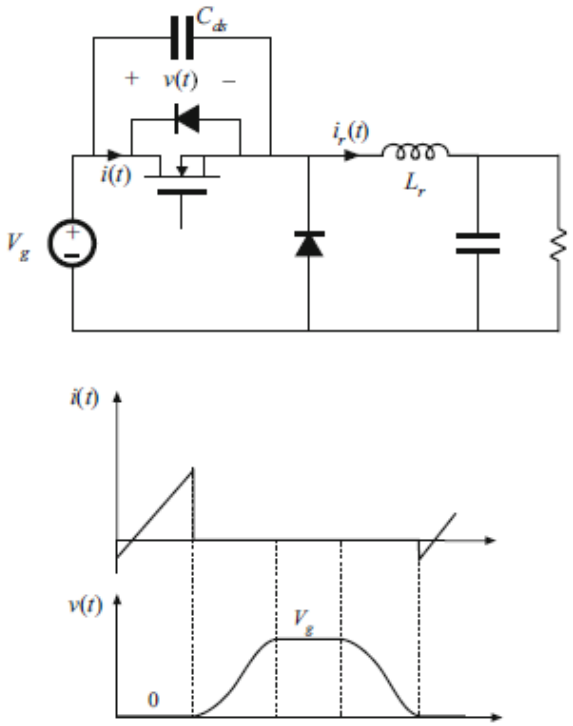


Figure 2.2: ZVS Buck converter, schematic and waveforms [5] .

The circuit in Figure 2.2 represents an example of how ZVS can prevent both diode reverse recovery current spike and switching losses related to the energy stored in the output capacitance of the transistor.
In this case the Buck converter circuit is able to discharge the energy stored into the output capacitance before the transistor is switched on. When the drain-to-source voltage waveform passes through the zero, the body diode of the transistor becomes forward biased, and the transistor is turned on with zero voltage and hence without switching losses. It is important that the turn on transition is completed before the current though the inductor becomes positive otherwise this transition becomes lossy. The transistor turn-off follows the same mechanism and it is also lossless. Furthermore, ZVS of the transistor eliminates the switching loss related to the reverse recovery of the body diode because it forces it to operate under ZVS condition [5].

2.2 Resonant power converters

The generic topology of a DC-DC resonant power converter that can be found in the literature includes a resonant inverter and a high-frequency rectifier. The inverter and the rectifier must be compatible with each other, which means that:

- an inverter with a current output must be connected to a current-driven rectifier;
- an inverter with a voltage output must be connected to a voltage-driven rectifier.

Let's consider in what follows the second situation, in which the inverter has a voltage output and hence it is coupled with a voltage-driven rectifier.
The resonant inverter typically consists of a full-bridge or a half-bridge configuration that generates a square wave voltage from the DC input voltage. Then, the generated square wave becomes the input of a resonant LC tank that produces a sinusoidal voltage signal.
The high-frequency rectifier can be connected to the resonant inverter through a transformer in order to guarantee a galvanic isolation between the two stages.
The goal of the rectifier is to converter the AC voltage generated by the resonant inverter to the output DC voltage. The rectification can be achieved by using one of the following rectifiers:

- half-wave rectifier;
- center-tapped rectifier;
- bridge rectifier.

However, it is preferable to choose a synchronous rectifier (SR) instead of a power diode rectifier to improve the converter efficiency.
The conversion ratio of the resonant power converter is obtained by the product between the voltage transfer function of the inverter and voltage transfer function of the rectifier. The efficiency is retrieved similarly to the voltage transfer ratio. In Figure 2.3 a block diagram of a DC-DC resonant power converter is shown.

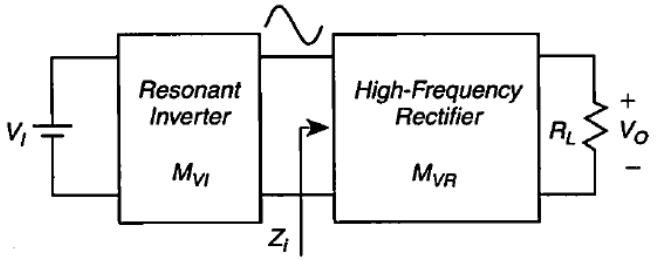


Figure 2.3: Block diagram of a DC-DC resonant power converter [6].

In many resonant converters, power switches operate under soft-switching conditions, more precisely, ZVS and ZCS that will be considered in the next section.
Resonant power converters can be classified in three main topologies:

- series-resonant converter (SRC);
- parallel-resonant converter (PRC);
- series-parallel-resonant converter (SPRC).

2.2.1 Series-resonant converter

The primary side of the SRC with a half-bridge configuration, as shown in Figure 2.4, consists of two switches, *S1* and *S2*, and a series resonant circuit composed of a capacitor *C*, an inductor *L* and a resistor R_i that represents the AC load and it could be replaced by one of the rectifiers mentioned previously to get the DC-DC converter. Each switch is composed by a transistor and an antiparallel diode and therefore they are bidirectional in conducting current.
If the transistor is ON, a positive or a negative current can flow through the transistor. If the transistor is OFF, only a negative current can flow through the switch and, in this case, it is the diode that conducts.
The two switches are driven in a complementary way by two rectangular wave voltages with duty cycle of 50% and dead time.

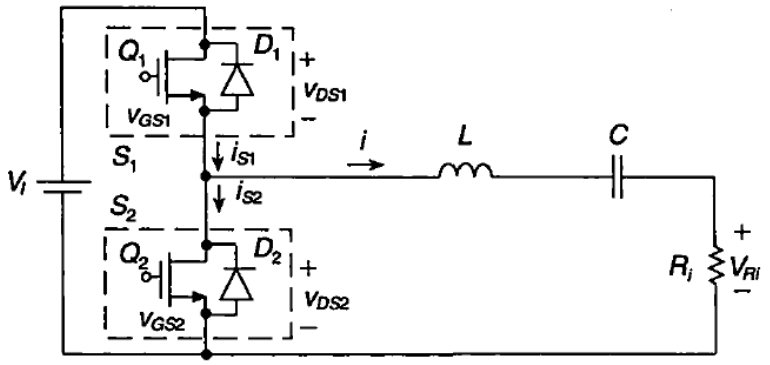


Figure 2.4: Resonant inverter of the SRC circuit [6].

The most important parameters that characterize the SRC are defined as follows [6]:

- The resonant frequency

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{2.1}$$

- The characteristic impedance

$$Z_o = \sqrt{\frac{L}{C}} = \omega_o L = \frac{1}{\omega_0 C} \tag{2.2}$$

- The loaded quality factor

$$Q_L = \frac{\omega_o L}{R} = \frac{1}{\omega_o C R} = \frac{Z_o}{R} = \frac{\sqrt{\frac{L}{C}}}{R} \tag{2.3}$$

- The unloaded quality factor

$$Q_o = \frac{\omega_o L}{r} = \frac{1}{\omega_o C r} = \frac{Z_o}{r} = \frac{\sqrt{\frac{L}{C}}}{r} \tag{2.4}$$

where

$$r = r_{DS} + r_L + r_C \tag{2.5}$$

and

$$R = R_i + r \tag{2.6}$$

where r is the unloaded resistance or parasitic resistance composed by the transistor on-resistance r_{DS}, the equivalent series resistance (ESR) of the inductor r_L and equivalent series resistance of the capacitor r_C.
R is the total resistance composed by the load resistance R_i and the parasitic resistance r.
If the loaded quality factor Q_L is high enough, the current flowing through the series-resonant circuit can be considered to be sinusoidal.

Depending on the value of the switching frequency with respect to the resonant frequency, the SRC converter operates in three different regions:

- if $f > f_o$, SRC operates above resonance;
- if $f = f_o$, SRC operates at resonance;
- if $f < f_o$, SRC operates below resonance.

The three working regions of the SRC can be identified in Figure 2.5, which shows the magnitude of the conversion ratio of the resonant inverter as a function of the switching frequency normalized with respect to the resonant frequency.
For $f > f_o$, the SRC operates above resonance and the series-resonant circuit represents an inductive load because the inductive reactance is higher than the capacitive reactance. Under this operating mode, the current i that flows through the series-resonant circuit lags the fundamental component of the input voltage applied to the resonant circuit with reference to Figure 2.4, the conduction sequence of the switches is *D1*, *Q1*, *D2*, *Q2*.

When the transistor *Q1* is turned on by the drive voltage, the current *i* is equal to zero and the current that flows through *Q1* is the same of *i*, hence *Q1* turns on with zero current and zero voltage.

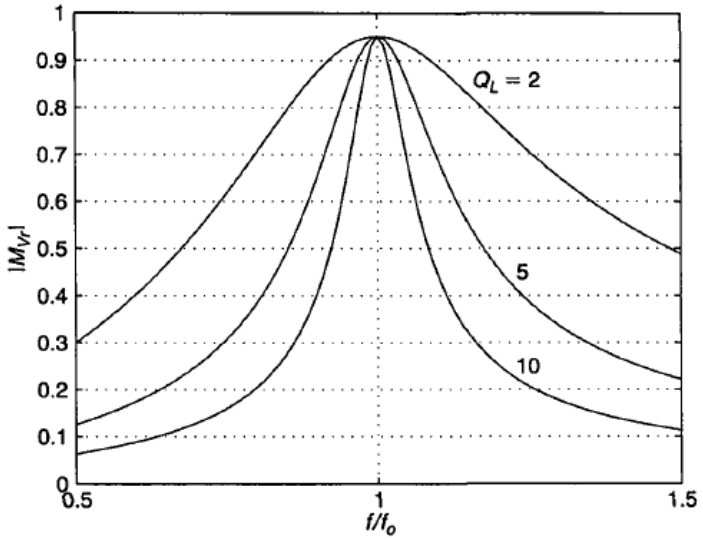


Figure 2.5: Magnitude of the conversion ratio of the resonant inverter of the SRC versus normalized operating frequency [6].

When the transistor *Q1* is turned off by the drive voltage, the V_{DS1} voltage increases and the V_{DS2} voltage decreases. When the V_{DS2} voltage reaches the forward voltage of the diode, *D2* turns on and the current continues to flow through it since during the dead time both transistors are OFF.
The turn-on switching loss is zero because both voltage and current are zero, but turn-off switching loss is present due to the overlap of the voltage across the switch and the current flowing through it.
It is interesting to notice that only the turn-off of the switch is directly controllable by the driver, while the turn-on happens after the turn-off of the complementary switch.
Another important consideration is related to the Miller's effect. During this operating mode, since the turn-on switching loss is zero, the Miller's effect is absent at the turn-on, and the input capacitance of the transistor is reduced. Consequently, the speed of the turn-on transition is high. While the Miller's effect is considerable during turn-off due to the switching loss [6].

For $f < f_o$, the SRC operates below resonance and the series-resonant circuit represents a capacitive load because the capacitive reactance is higher than the inductive reactance. Under this operating mode, the current *i* that flows through the series-

resonant circuit leads the fundamental component of the input voltage applied to the resonant circuit. The conduction sequence of the switches is *Q1*, *D1*, *Q2*, *D2*.
When the transistor *Q2* is turned on by the drive voltage, the V_{DS2} voltage decreases and the V_{DS1} voltage increases. Therefore, the current that flowed through the diode *D1* continues to flow through the transistor *Q2* turned on by the respective drive voltage.
This operating mode is characterized by a considerable drawback that is the diode reverse recovery stress when the diode turns off because of the turning on of the opposite transistor. The diode turns off when the current flowing through it is very high generating a high reverse recovery current spike. This current spike is diverted from the diode to the transistor since it cannot flow through the resonant circuit due to the presence of the inductor. Consequently, it may destroy the transistors and increases the switching loss.
When the transistor *Q2* is turned off, the current *i* continues to flow through the diode *D2*. Then, at the turn-on of the transistor *Q1*, the high reverse recovery current spike is due to the diode *D2* causing a high current spike in the switch current of the transistor *Q1*. Hence, operation below resonance should be avoided.
In this case, the turn-on of the switch is directly controllable by the driver, while the turn-off happens after the turn-on of the complementary switch.
Furthermore, as in the operating mode discussed previously, another drawback is the Miller's effect present both at the turn-on and turn off because of the switching loss. Consequently, the speed of the turn-on and turn-off transitions is high [6].

For $f = f_o$, the SRC operates at resonance. Only during this operating mode, transistors turn on and turn off when the current flowing through them is equal to zero. Therefore, switching losses are very low and this increases the efficiency of the resonant power converter. Moreover, antiparallel diodes never conduct.
The waveforms corresponding to each operating principle of the SRC described above are reported in Figure 2.6.

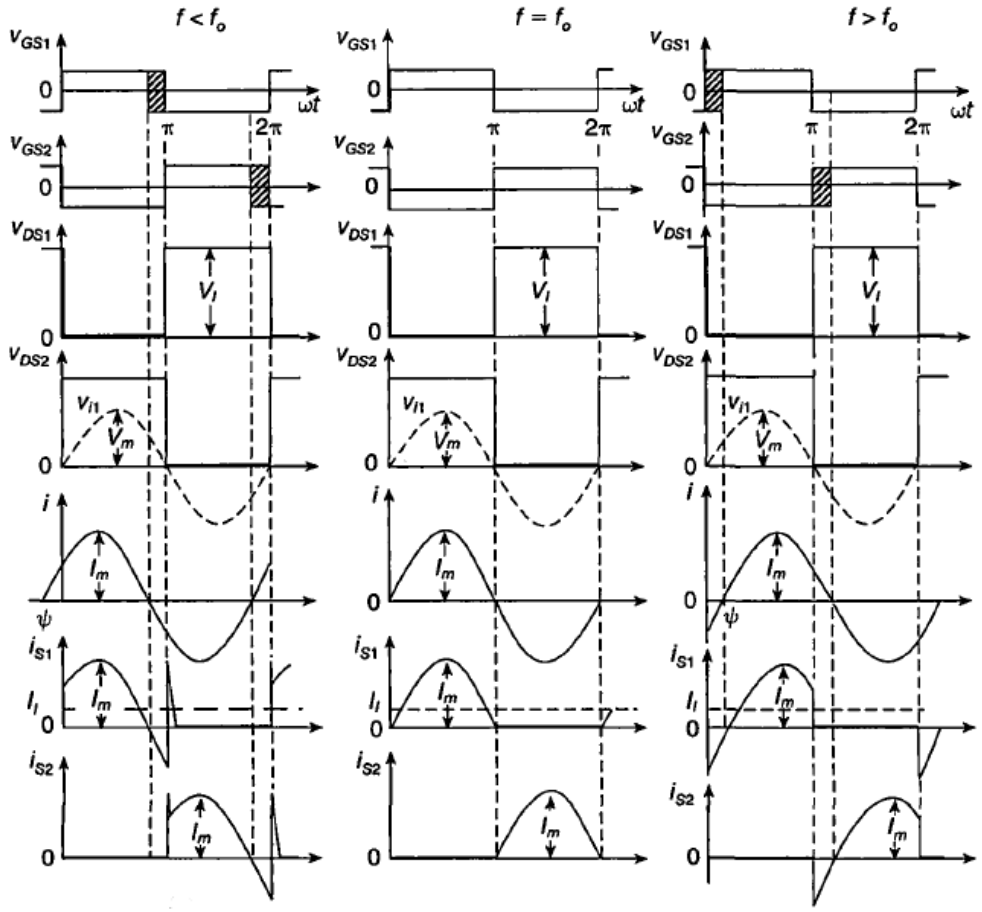


Figure 2.6: Waveforms of the SRC operating principles [6].

2.2.2 Parallel-resonant converter

The second topology which is shown in Figure 2.7 is the PRC. The primary side of a PRC with a half-bridge configuration consists of two switches, *S1* and *S2*, and a parallel resonant circuit composed of an inductor L, a DC-blocking capacitor C_c to avoid DC current flowing through the AC load, a capacitor C and a resistor R_l. The resistor represents the AC load and, as in the previous topology, it should be replaced by one of the rectifiers mentioned previously to get the DC-DC converter. Each switch is composed by a transistor and an antiparallel diode and therefore they are bidirectional in conducting current.

As in the SRC topology, the two switches are driven in a complementary way by two rectangular wave voltages with duty cycle of 50% and dead time.

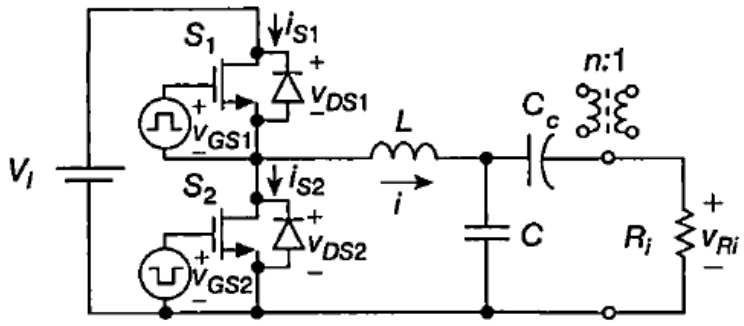


Figure 2.7: Resonant inverter of the PRC circuit [6].

To simplify the analysis of this resonant converter, usually the parallel combination of the of the AC load resistance R_i and capacitor C is transformed into a series combination of the new resistance R_s and capacitor C_s. This new combination is shown in Figure 2.8.

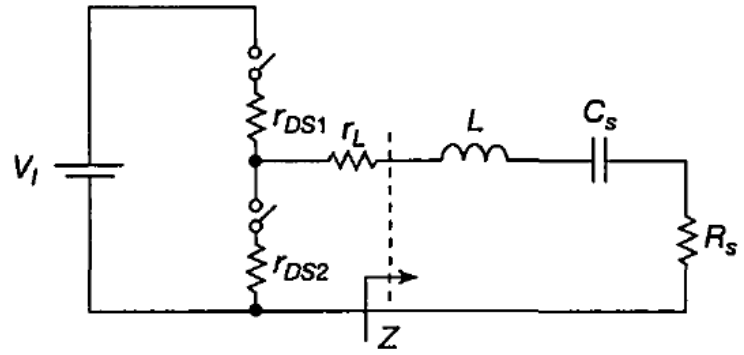


Figure 2.8: Series combination of the load resistance and capacitance in the PRC [6].

The resonant circuit of the PRC topology is a second order low pass filter and hence the parameters that characterize the PRC are the following [6]:

- The undamped natural frequency

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{2.7}$$

- The characteristic impedance

$$Z_o = \sqrt{\frac{L}{C}} = \omega_o L = \frac{1}{\omega_0 C} \tag{2.8}$$

- The loaded quality factor at the undamped natural frequency

$$Q_L = \omega_o C R_i = \frac{R_i}{\omega_o L} = \frac{R_i}{Z_o} \tag{2.9}$$

- The resonant frequency

$$\omega_r = \frac{1}{\sqrt{LC_s}} \tag{2.10}$$

- The unloaded quality factor at the resonant frequency

$$Q_r = \frac{\omega_r L}{R_s} = \frac{1}{\omega_o C_s R_s} \tag{2.11}$$

where R_i is the parallel AC load and R_s is the series AC load obtained from the transformation of the R_i-C circuit into the R_s-C_s circuit.
If the loaded quality factor Q_L is high enough, the current flowing through the parallel-resonant circuit is sinusoidal.

Depending on the value of the switching frequency with respect to the resonant frequency, the PRC converter operates in three different regions:

- if $f > f_r$, PRC operates above resonance;
- if $f = f_r$, PRC operates at resonance;
- if $f < f_r$, PRC operates below resonance.

The three working regions of the PRC can be identified in Figure 2.9 which shows the magnitude of the conversion ratio of the resonant inverter as a function of the switching frequency normalized with respect to the undamped natural frequency for several values of the loaded quality factor.

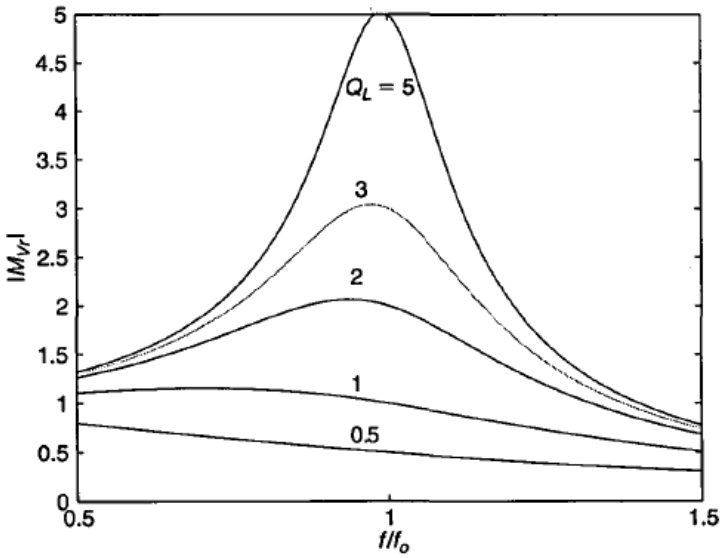


Figure 2.9: Magnitude of the conversion ratio of the resonant inverter of the PRC versus normalized operating frequency [5].

For what concerns the operating principles of the PRC, they are exactly the same described previously for the SRC and which waveforms are shown in the Figure 2.6.
To perform a comparison between series-resonant converter and parallel-resonant converter, the main advantages and disadvantages are highlight below.
The principal features of the SRC are [7]:

- this converter is able to generate waveforms in the frequency range of 200 Hz to 100 kHz;
- increasing the output voltage is quite difficult when the variation of the load is wider, as a consequence the efficiency is low;
- it can operate safely with an open circuit at the output but not with a short circuit.

The principal features of the PRC are [7]:

- this converter generates a continuously controlled current and hence it also gives short circuit protection;
- it is able to increase and decrease the output voltage without negative consequences on the efficiency;
- the output voltage is controlled from full load to no load conditions by working at the operating frequency higher than the resonance frequency;
- the conduction losses of the switches are considerable even for light loads and therefore, in this case, the efficiency is low.

2.2.3 Series-parallel-resonant converter

The last topology of resonant power converters described in this thesis is the series-parallel-resonant converter, and it combines the features of both SRC and PRC. Many configurations of SPRCs can be obtained combining the resonant capacitor and resonant inductor differently: LCC, LLC, LCLC and LCCL.
The LLC resonant converter, which topology is shown in Figure 2.10, has several advantages such as high efficiency, low electromagnetic interference and high power density [7], so it is one of the topologies examined in this work to achieve and to improve the adapter.
The primary side of a LLC resonant converter with a half-bridge configuration consists of two bidirectional switches, *S1* and *S2*, and a resonant circuit composed of an inductor L_1, an inductor L_2 and a capacitor *C*. The AC load resistor R_i is connected in parallel with the L_2 inductor, and it should be replaced by a rectifier.

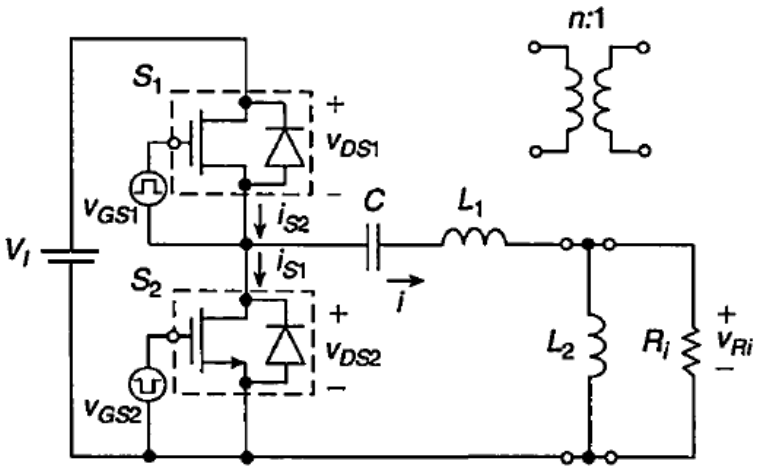


Figure 2.10: Resonant inverter of the LLC resonant converter [6].

The L_2 inductance can be replaced by a transformer and it becomes the magnetization inductance of the transformer, while the leakage inductance of the transformer is included in the L_1 inductance.
It is useful to notice that the topology of the transformer version of the SRC is identical to that LLC converter, the only difference being the value of the magnetizing inductance that in the SRC is large while in the LLC topology it is small [6].
As in the PRC topology, the parallel combination of the of the AC load resistance R_i and the inductance L_2 can be converted into a series combination of the new resistance R_s and inductance L_s.
The resonant circuit of the LLC topology is characterized by the following parameters [6]:

- The inductance ratio

$$A = \frac{L_1}{L_2} \tag{2.12}$$

- The equivalent inductance of L_1 and L_2 in series

$$L = L_1 + L_2 = L_1\left(1 + \frac{1}{A}\right) = L_2(1 + A) \tag{2.13}$$

- The undamped natural frequency

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{2.14}$$

- The characteristic impedance

$$Z_o = \sqrt{\frac{L}{C}} = \omega_o L = \frac{1}{\omega_0 C} \tag{2.15}$$

- The loaded quality factor at the undamped natural frequency

$$Q_L = \omega_o C R_i = \frac{R_i}{\omega_o L} = \frac{R_i}{Z_o} \tag{2.16}$$

- The equivalent inductance of L_1 and L_s in series

$$L_{eq} = L_1 + L_s \tag{2.17}$$

- The resonant frequency

$$\omega_r = \frac{1}{\sqrt{L_{eq} C}} \tag{2.18}$$

- The unloaded quality factor at the resonant frequency

$$Q_r = \frac{\omega_r L_{eq}}{R_s} = \frac{1}{\omega_o C R_s} \tag{2.19}$$

where R_i is the parallel AC load and R_s is the series AC load obtained from the transformation of the R_i-L_2 circuit into the R_s-L_s circuit.

For what concerns the operating principles of the LLC resonant converter, they are exactly the same as those of the SRC and PRC described previously and which waveforms are shown in the Figure 2.6.

Accordingly, the operation in the region above the resonance is preferred because the reverse recovery of the transistor antiparallel diode does not affect adversely the circuit operation. The diode turns off with low current and it does not generate reverse-recovery current spikes, hence the switching losses are reduced.

The three working regions of the LLC resonant converter can be identified in Figure 2.11.

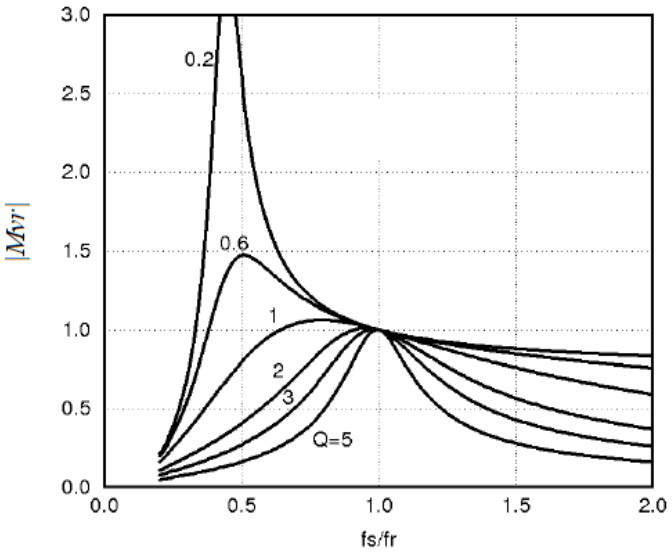


Figure 2.11: Magnitude of the conversion ratio of the resonant inverter of the LLC converter versus normalized operating frequency.

Finally, it is interesting to summarize the most important features [7], both advantages and disadvantages, of the LLC resonant power converter useful for the design that will be done in the next chapter:

- high efficiency;
- low electromagnetic interference;
- high power density;
- operation at resonance with a nominal input voltage;

- ZVS and ZCS over the entire operating range, so this means low switching losses;
- ZVS also at no load condition;
- both step up and step down operations;
- further improvement of the efficiency by using a synchronous rectifier instead of a diode rectifier;
- at no load the output over voltage protection and over current protection are not obtained.

2.3 Power converter topologies

The most common power converter topologies used for high-power density and high-frequency adapters are based on the flyback converter and LLC resonant converter architectures.
The standard flyback converter is easy to design but it does not allow to reach high-power density while high-frequency operation is difficult to obtain due to the high output capacitance and high gate charge of the Silicon MOSFET [8]. Since the main goal is to increase the power density and to reduce the size of the adapter, optimizations have been applied to the standard flyback converters in recent years.
In this context, increasing the operating frequency is significative because it allows to reduce the size of the components of the circuit, and this means a reduction of the size of the adapter.
In literature, several kinds of improved flyback converters for adapter applications can be found. More precisely, the studied topologies include:

- Active Clamp Flyback (ACF) converter;
- Asymmetrical Half Bridge Flyback (AHBF) converter;
- LLC resonant power converter.

The ACF converter [9] is an improved flyback converter topology which is able to recover the energy stored into the leakage inductor. This topology is shown in Figure 2.12 and it consists of two switches *S1* and *S2* at the primary side with a clamp capacitor C_r connected in series with the high-side switch *S2*. The presence of the clamp capacitor in series with the high-side switch is one of the main differences between the ACF converter and the standard flyback converter. Furthermore, the power supply V_{in} is not connected to the drain of the switch *S2* as in the standard two-switch architecture, but it is connected to the negative pole of the clamp capacitor. The transformer's leakage inductance L_r acts as resonant inductor and together with the magnetization inductance L_m constitute the elements for storing energy.
The secondary side of the ACF converter preserve the standard flyback converter configuration with the secondary rectifier switch *S3* and the output capacitor C_o is needed to filter the output voltage ripple.

An important feature to mention is the ability of the ACF converter to achieve ZVS turn-off and turn-on of primary side switches and ZCS turn-off of secondary side switch. Thanks to these techniques, the switching losses are greatly reduced and consequently the efficiency increases.

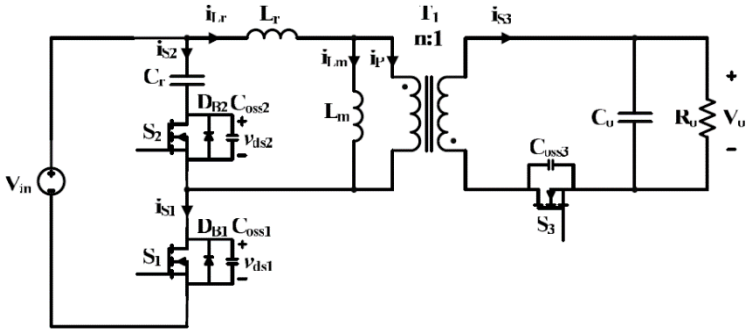


Figure 2.12:Active Clamp Flyback converter schematic [2].

The second topology shown in Figure 2.13, the AHBF converter [8], is similar to the ACF converter from the architectural point of view. The only difference between the two architectures is that in the AHFB converter the power supply V_{in} is connected to the drain of the high-side switch *Q1* and no more to the negative pole of the primary side capacitor C_r. Therefore, the primary side of this circuit consists of a half-bridge driving a LC tank circuit made of a blocking resonant capacitor C_r, the leakage inductance L_r of the transformer and the magnetization inductance L_m.
The secondary side of the AHBF converter is exactly the same of the ACF converter, therefore the complete architecture consists of an LLC inverter with a flyback secondary rectifier.
This topology has several advantages with respect to the ACF converter that will be shown in the next chapter. However, one of the main advantages is the presence of multiple energy storage elements: the leakage inductance, the magnetizing inductance and the blocking resonant capacitor store energy when the secondary side switch is turned off. As a consequence of the presence of multiple energy storage elements, the size of the transformer can be reduced [1].
Also, the ZVS turn-on and turn-off of the primary side switches and the ZCS turn-off of the secondary side switch are achieved in order to reduce the switching losses and improve the efficiency.

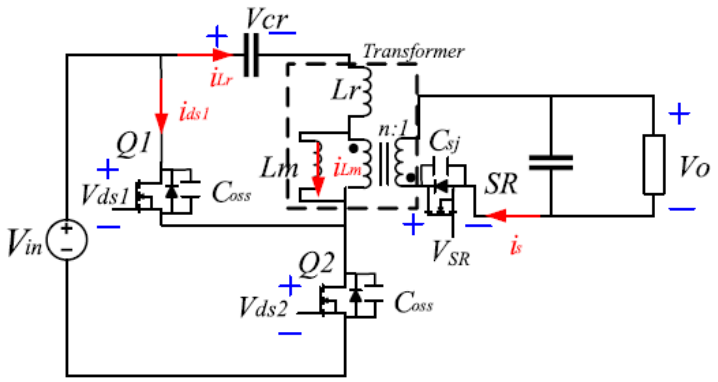


Figure 2.13: Asymmetrical Half Bridge Flyback converter schematic [8].

The last considered topology is the LLC resonant converter which is shown in Figure 2.14.

This topology is quite different than the previous mentioned topologies both in terms of operating principle and in terms of architecture, a detailed study will be done in the next chapter.

For what concerns the architecture, the primary side of this converter is equal to the one of the AHBF converter, therefore it consists of a half-bridge driving a resonant LC tank.

The secondary side is a center tapped rectifier which uses a center tapped transformer and two diodes to convert the AC signal coming from the LLC inverter into DC signal.

This type of converter is also able to achieve ZVS and ZCS as in the previous topologies. Unlike the other two converters, it does not work properly for a wide input voltage range because the optimal operating point of the LLC resonant converter is reached for a given input voltage and load resistance. If the input voltage or the load change, the operating frequency must be adjusted by a feedback loop to keep the output voltage properly regulated [3].

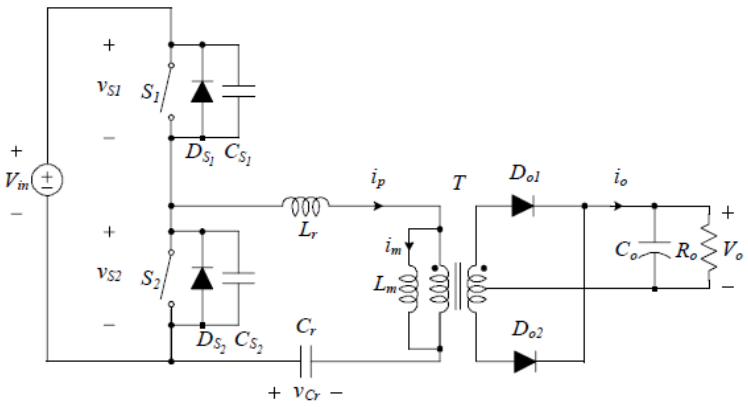


Figure 2.14: LLC resonant power converter schematic [3].

Chapter 3

Analysis and design of resonant power converters

The aim of this chapter is to identify an improved solution in term of efficiency and electrical stresses of components of the resonant power converters employed in the realization of high-power density adapters.
In order to operate at very high frequency, such as 1 MHz, GaN HEMT devices are adopted as primary switches because they are more suitable to work at high frequency than the traditional approach with Silicon MOSFET devices. Therefore, before proceeding with the circuit analysis, GaN HEMT devices highlighting the advantages compared to Silicon MOSFETs are presented.
First of all, in order to design the circuits, the current and voltage waveforms of the three topologies that are available in the literature and mentioned in the Chapter 2 have been analysed. Then, a generic design of each topology has been retrieved with possible improvements such as the resonant current dip phenomenon and the secondary side resonance scheme.
After the design, simulations to verify the theoretical solutions have been carried out by using the LTspice and PowerSim softwares. These first simulations were performed by using the ideal models of the elements that constitute the power converters.

3.1 GaN HEMT devices overview

High switching frequency operation is the first strategy to achieve high power density and size reduction. In order to meet this requirement, GaN HEMT devices have proved to be more suitable for working at high frequency than Silicon MOSFETs.
HEMT devices can be built by using several types of junction materials such as GaN and AlGaN or GaAs and AlGaAs, but anyway GaN material results the most widely

used in the fabrication of these devices due to its performance for high frequency and high-power density applications.
Gallium Nitride is a III-V semiconductor with direct wide bandgap equal to 3.4 eV, while Silicon has 1.12 eV bandgap, this means that GaN requires more energy to excite a valence electron in the conduction band of the semiconductor than Silicon. For this reason, GaN presents a lot of merits such as larger breakdown electric field, high electronic saturation velocity, high electron mobility but lower thermal conductivity.
A bar chart in Figure 3.1 is reported to compare Silicon and GaN properties [10].
Moreover, also Silicon Carbide (SiC) offers great performance at high frequency operation, in fact its features are quite competitive with those of GaN material. Looking at Figure 3.1, it is possible to notice that the thermal conductivity is much greater for the SiC material than for GaN material. However, the GaN electron mobility is higher than SiC so that GaN can be considered the most suitable device for very high frequencies. Furthermore, the material employed for SiC devices is limited than the one used for GaN devices and therefore their cost is quite high [10].
Focusing on the structure of a GaN HEMT device, it is typically composed of a thick silicon substrate, a AlGaN-GaN heterostructure, a Schottky metal-semiconductor junction for the gate contact and ohmic contacts for the source and the drain like the one shown in Figure 3.2.

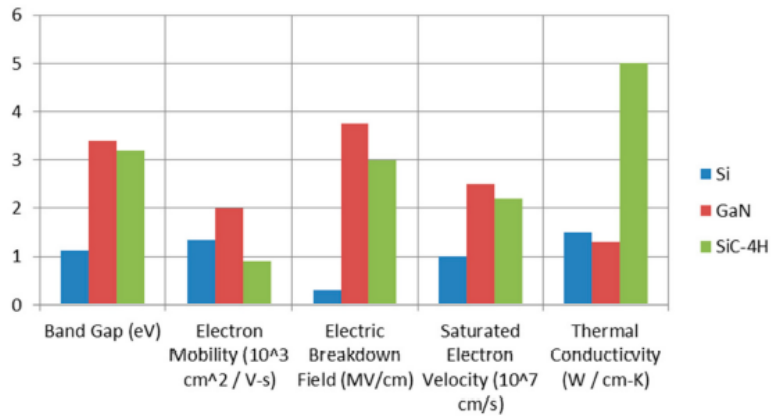


Figure 3.1: Comparison between Silicon (Si), Gallium Nitride (GaN) and Silicon Carbide (SiC) properties [10].

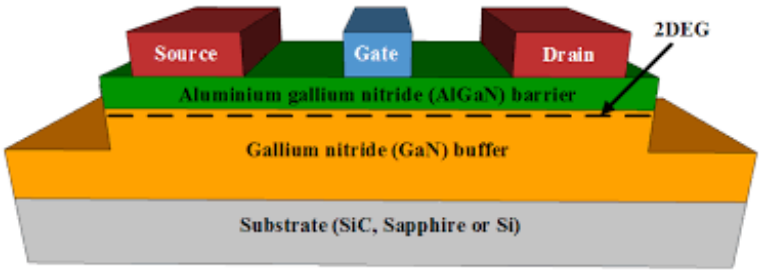


Figure 3.2: Structure of the GaN HEMT device.

To define the working principle of these devices, the behaviour of a heterostructure must be investigated [11]. To this purpose, the structure of the energy band between the two materials, i.e. the intrinsic GaN semiconductor and the highly n-doped AlGaN semiconductor is analysed in what follows.

The vertical section of AlGaN-GaN heterostructure and the band diagram of the heterostructure is reported in Figure 3.3.

When the intrinsic GaN semiconductor and the highly n-doped AlGaN semiconductor are separated, they are characterized by their own conduction band and valence band levels. When the two semiconductors form a junction ($x = 0$ in Figure 3.3), the level of the conduction band of the first material and the one of the second material are aligned, and the same happens for the levels of the valence band.

In this context, electrons that come from the highly n-doped AlGaN semiconductor move towards the conduction band in the intrinsic GaN semiconductor. This phenomenon ends when the charge difference between the two semiconductors produces a high electric field that is able to interrupt the flow of electrons moving from one region to the other. When this strong electric field is achieved, the thermal equilibrium is reached.

Furthermore, from the band diagram shown in Figure 3.3, it is possible to observe that at the interface between the two semiconductors (at $x = 0$) a discontinuity point is formed. This creates a triangular Quantum Well (QW) in which electrons are trapped and it forms a Two-Dimensional Electron Gas (2-DEG) channel.

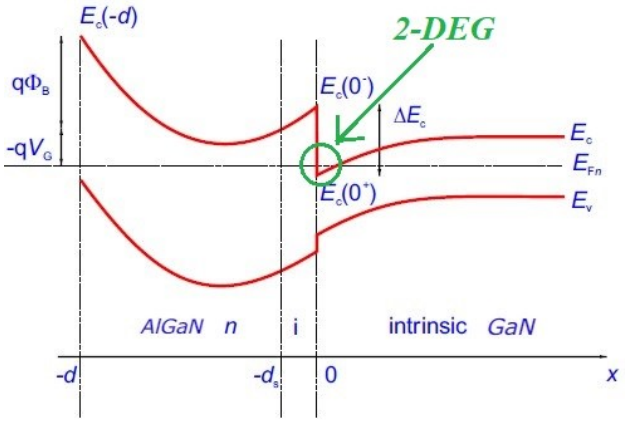


Figure 3.3: Band diagram of the AlGaN-GaN heterostructure.

According to value of the voltage applied to the gate of the GaN HEMT device, the conduction channel is differently modulated. Consequently, if the intensity of the gate voltage is increases, the number of electrons in the 2-DEG channel increases and hence the current flowing into the device increase. This leads to saturation phenomenon and it limits the maximum current that can flow through the device. This is represented in Figure 3.4.

It is possible to distinguish between two types of devices: depletion mode (*d-mode*) transistor and enhancement mode (*e-mode*) transistor.

The first one, *d-mode*, leads to normally-ON transistor, therefore without applying any voltage to the gate of the device the conduction channel is already formed. Then, this conduction channel is modulated according to the intensity of the gate voltage as mentioned previously.

The second one*, e-mode*, leads to normally-OFF transistor, therefore without applying any voltage to the gate of the device, the conduction channel is not formed. So, only when a positive gate voltage is applied the conduction channel is formed and the current starts flowing into the transistor. For this reason, it is better to use *e-mode* device in power conversion to prevent short circuits.

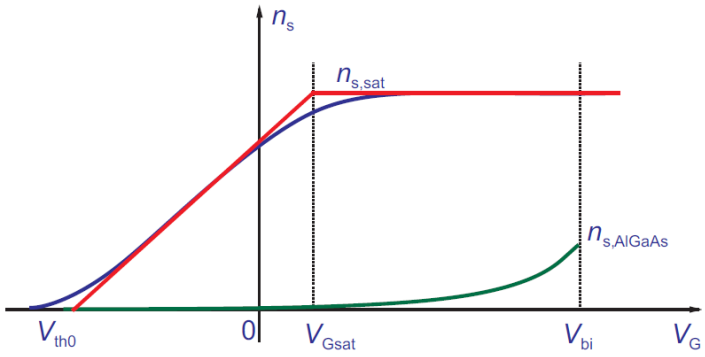


Figure 3.4: Electron concentration per unit area versus the gate voltage.

Finally, the advantages of the GaN HEMT devices with respect to Silicon MOSFET devices that make them preferable for high frequency applications and to enhance the performances of power converters are the following:

- ability to sustain higher temperatures than Silicon devices;
- higher mobility thanks to the insertion of the undoped layer at the interface between the two semiconductors;
- larger saturation velocity and faster switching times;
- low on-resistance;
- high breakdown voltage;
- very low output capacitance;

- low input capacitance due to the lower capacitance of the Schottky metal-semiconductor junction for the gate contact;
- ability to conduct current in reverse direction without exploiting an intrinsic diode in the structure.

However, not only the advantages should be denoted but also the drawbacks. The main limitation of the GaN HEMT device is the lower thermal conductivity than Silicon MOSFET device. This is a crucial factor that affects the device because it means more heat accumulation and hence increased temperature and power dissipation. But thanks to the previously mentioned properties of the GaN devices, such as low output capacitance, higher mobility and so on, the power dissipated is very low and it is able to maintain an adequate temperature without negatively affecting the efficiency.

3.2 Active Clamp Flyback converter

As discussed in the previous chapter, the ACF converter is one of the topologies that is employed to meet the requirements of high-power density in the adapter design. In what follows the analysis is detailed for what concern the working principle and the design equations.

The ACF converter schematic [12] that will be considered throughout this section is shown in Figure 3.5. For what concerns the primary side of the circuit, *S1* is the main switch and *S2* is the auxiliary switch. Both *S1* and *S2* are GaN HEMT switches, and their body diodes and output capacitances are considered. V_{in} is the DC input voltage. Then, C_r is the resonant clamp capacitor, L_r is the resonant inductance that also includes the leakage inductance of the transformer and L_m is the magnetizing inductance.

Now, focusing on the secondary side of the converter, S*3* is the synchronous rectifier (SR) switch and it is a Silicon MOSFET device. Its output capacitance C_{oss3} is also considered.

Finally, C_o is the output capacitor and R_o represents the equivalent load resistance.

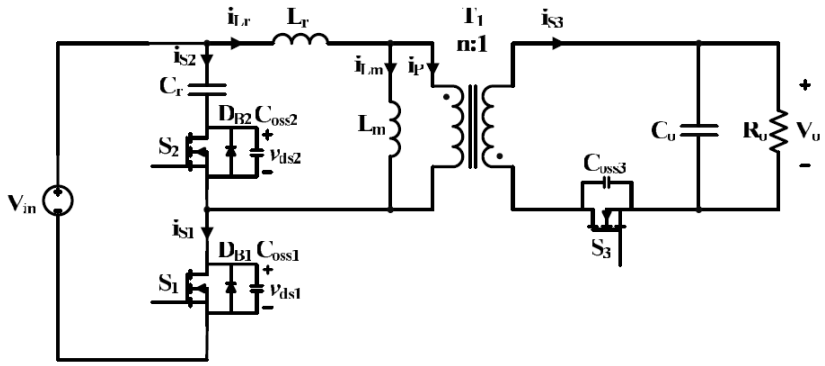


Figure 3.5: Active Clamp Flyback converter schematic [12].

3.2.1 Circuit analysis

Before proceeding with the circuit analysis, it is meaningful to define the following assumptions [12] in order to simplify the study of the converter:

- steady state operation;
- the magnetizing inductance L_m is greater than the resonant inductance L_r, and the secondary leakage inductance is neglected;
- the output capacitor C_o is considered large enough such that the output voltage can be a constant DC voltage with negligible ripple.

As a first step in circuit analysis, it is necessary to derive the conversion ratio of the ACF converter. To compute it, two intervals must be considered while dead times are ignored.

- **T1 period**: *S1* transistor is ON, *S2* and *S3* transistors are OFF.
- **T2 period**: *S1* transistor is OFF, *S2* and *S3* transistors are ON.

The **T1 period** is the charging phase during which the magnetizing inductance L_m is charged and no energy is transferred to the secondary side.
During this period, the drain-to-source voltage across the *S2* transistor can be defined through the following equation:

$$V_{DS2} = V_{in} + V_{Cr} \tag{3.1}$$

However, the same voltage is also defined by the equation below under the $L_r << L_m$ assumption:

$$V_{DS2} = V_p(T1) + V_{Cr} \tag{3.2}$$

where V_{Cr} is the voltage across the resonant clamp capacitance C_r.

By combining Equation (3.1) and Equation (3.2), the voltage across the primary winding $V_p(T1)$ during this phase is equal to the input voltage V_{in} as reported in the following equation.

$$V_P(T1) = V_{in} \tag{3.3}$$

The **T2 period** is the discharging phase during which the magnetizing inductance L_m is discharged and the energy is transferred from the primary side to the secondary side of the isolated resonant power converter.
As done before, the drain-to-source voltage across the *S1* transistor can be defined by the following equation:

$$V_{DS1} = V_{in} + V_{Cr}\,. \tag{3.4}$$

The voltage across the primary winding during the T2 time interval $V_p(T2)$ can be derived by the equations below:

$$V_p(T2) = -V_{Cr} \tag{3.5}$$

$$V_p(T2) = nV_s \tag{3.6}$$

$$V_s = -V_o \tag{3.7}$$

where n is the turns ratio of the coupled inductors equal to N_p/N_s, V_s is the voltage across to the secondary winding and V_o is the DC output voltage.
First of all, Equation (3.7) is substituted in the Equation (3.6) in order to obtain the voltage across the primary winding during T2 period.

$$V_p(T2) = -nV_o\,. \tag{3.8}$$

Then, Equation (3.8) is substituted in the Equation (3.5) in order to obtain the voltage across the resonant capacitance:

$$V_{Cr} = nV_o\,. \tag{3.9}$$

Finally, by substituting Equation (3.9) in the Equation (3.1) and (3.4), the drain-to-source voltage of both *S1* and *S2* transistors is obtained:

$$V_{DS1} = V_{in} + nV_o \tag{3.10}$$

$$V_{DS2} = V_{in} + nV_o\,. \tag{3.11}$$

From Equation (3.10) and (3.11), it can be noted that the voltage stress of the main and auxiliary switches depends on the input voltage and on the output voltage reflected to the primary side. Therefore, this means less margin for the selection of the primary switches.
Moreover, the voltage stress of the synchronous rectifier *S3* transistor can be computed during T1 period as follows:

$$V_{DS3} = V_S + V_o = \frac{V_p(T1)}{n} + V_o = \frac{V_{in}}{n} + V_o \,. \tag{3.12}$$

Similarly, V_{DS3} depends on the output voltage and on the input voltage reflected to the secondary side, as well as for the primary switches this means less margin to select the secondary switch.
The next step regards the derivation of the conversion ratio of the ACF converter. To perform this computation, the volt-second balance is applied to the voltage across the primary winding during the time intervals T1 and T2.
The procedure for obtaining the conversion ratio is reported in what follows, where *D* is the duty cycle of the transistor S1 and *T* is the whole period.

$$\begin{cases} V_p(T1)T1 + V_p(T2)T2 = 0 & (3.13) \\ D = \dfrac{T1}{T} = \dfrac{T1}{T1 + T2} & (3.14) \end{cases}$$

$$V_{in}T1 - nV_oT2 = 0 \tag{3.15}$$

$$V_{in}T2 = nV_o(T - T1) \,. \tag{3.16}$$

Finally, the expression of the conversion ratio of the ACF converter is the following:

$$\frac{V_o}{V_{in}} = \frac{1}{n}\frac{T1}{T - T1} = \frac{1}{n}\frac{1}{\frac{T}{T1} - 1} = \frac{D}{n(1 - D)} \tag{3.17}$$

Focusing on the working principles [12], it is easier to consider eight intervals from t_0 to t_8 separately. The current and voltage steady-state waveforms of the ACF converter are shown in Figure 3.6.

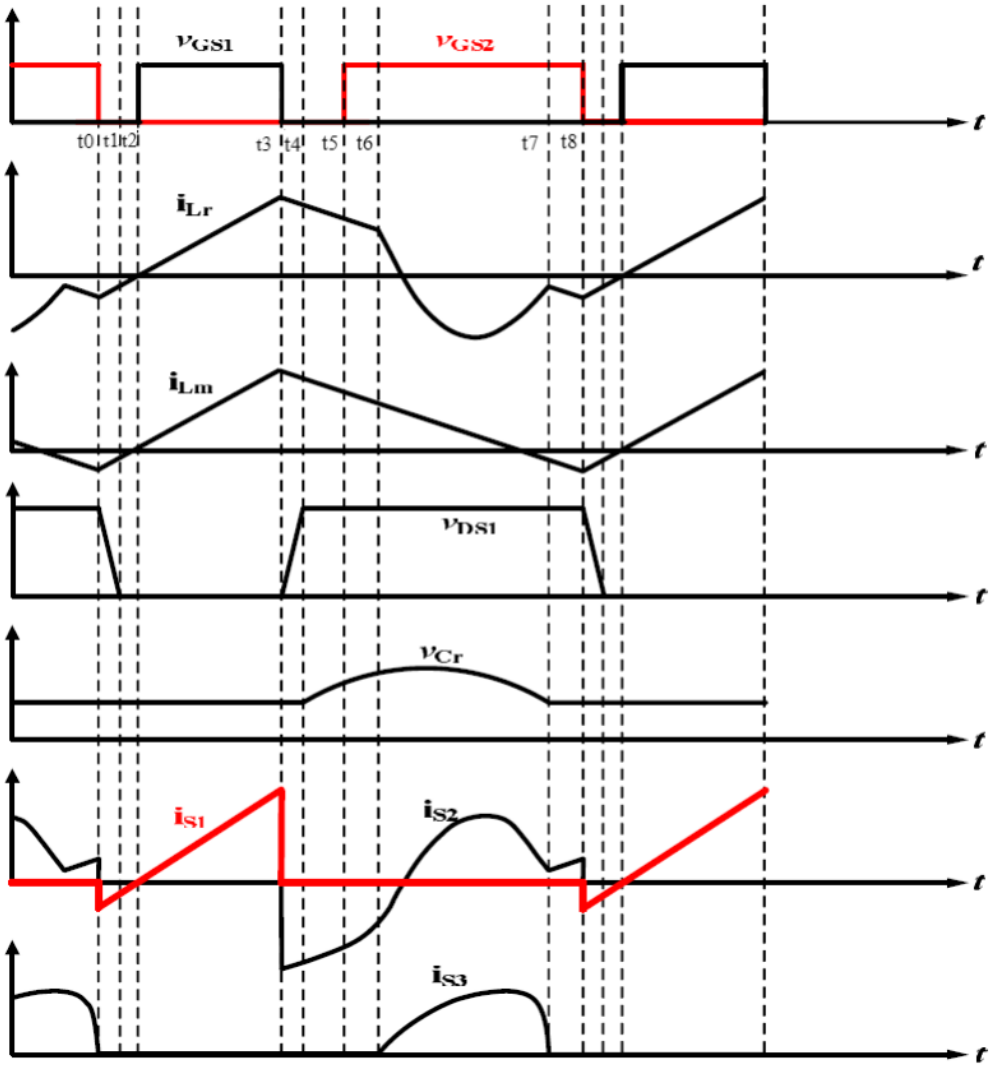


Figure 3.6: Current and voltage steady-state waveforms of the ACF converter [12].

Interval 1 [$t_0 - t_1$]: during this time interval, all the transistors are off. The current i_{Lm} discharges the output capacitance C_{oss1} of the transistor *S1*. Therefore, the drain-to-source voltage V_{DS1} decreases from its maximum value $V_{in} + nV_o$ to *0 V*.
Since the output capacitance of a GaN HEMT device is very small, it discharges quickly and hence this time interval is quite short.
At the same time, i_{Lm} is able to charge the output capacitance C_{oss2} of the transistor *S2* and the drain-to-source voltage V_{DS2} increases from *0 V* to its maximum value $V_{in} + nV_o$.
Furthermore, since at t_0 instant the *S2* transistor is turned off, the i_{Lm} current increases linearly and this means that the input voltage V_{in} starts to charge the magnetizing inductance L_m.
During this time interval, the resonant current i_{Lr} and the i_{S1} current follow the magnetizing current i_{Lm}, while the other transistor currents are equal to zero.

Figure 3.7 shows the current path in the ACF converter during this interval.

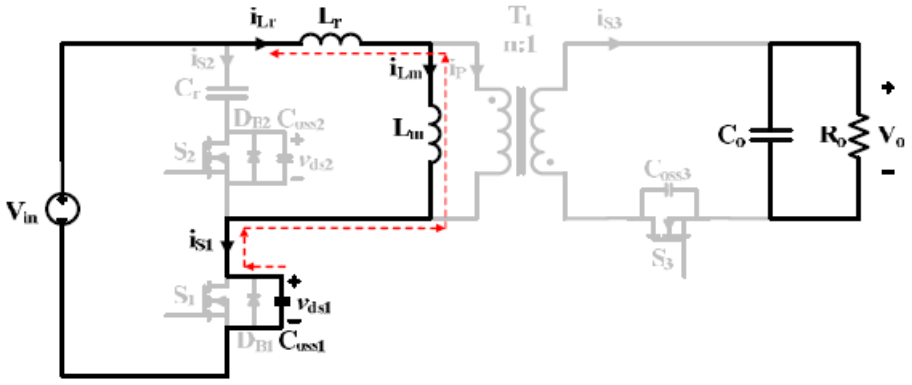


Figure 3.7: ACF during interval 1 [12].

Interval 2 [$t_1 - t_2$]: during this time interval, the transistors are still off.
The magnetizing current i_{Lm} continues to increase linearly. Since both the *S1* and the *S2* transistors are off, i_{Lm} flows through the body diode D_{B1} of the *S1* transistor.
At t_1, the C_{oss1} is fully discharged and V_{DS1} ha reached *0 V*, hence the *S1* transistor will be switched on with ZVS.
The resonant current i_{Lr} and the current i_{S1} continue to follow the magnetizing current i_{Lm}, while the other transistor currents are still zero.
The i_{Lm} equation during this operating stage is the following:

$$\begin{aligned} i_{Lm}(t) &= i_{Lm}(t_1) + \frac{1}{L_m}\int_{t_1}^{t} v_{Lm}(\tau)\, d\tau \\ &= i_{Lm}(t_1) + \frac{V_{in}}{L_m + L_r} t\,. \end{aligned} \tag{3.18}$$

Under the $L_m >> L_r$ assumption, the Equation (3.18) can be simplified as follows:

$$i_{Lm}(t) = i_{Lm}(t_1) + \frac{V_{in}}{L_m} t\,. \tag{3.19}$$

Figure 3.8 shows the current path in the ACF converter during interval 2.

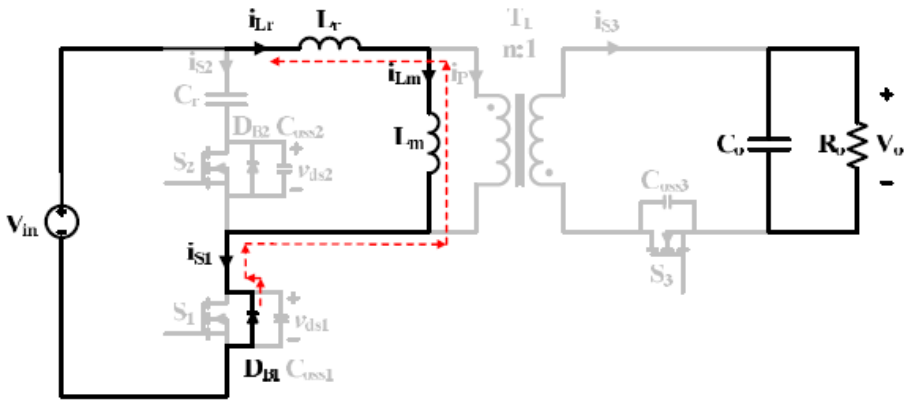


Figure 3.8: ACF during interval 2 [12].

Interval 3 [$t_2 - t_3$]: At t_2, *S1* turns on with ZVS. The input voltage continues to charge the magnetizing inductance up to the time instant t_3 and the i_{Lm} becomes positive following the same equation valis in the previous interval, Equation (3.19).

As in the previous interval, the resonant current i_{Lr} and the current i_{S1} continue to follow the magnetizing current i_{Lm}, while the other transistor currents continue to be zero.

Since the resonant current i_{Lr} and the magnetizing current i_{Lm} are equal, the primary current i_p, that is the difference between i_{Lr} and i_{Lm}, is equal to zero. Therefore, the current i_{S3} in the secondary winding is equal to zero and no energy is transferred from the primary to the secondary side of the converter.

Moreover, during this period, the voltage across the primary winding V_p is equal to the input voltage V_{in} and then the voltage stress of the transistor *S2* is equal to $V_{in} + nV_o$.

Figure 3.9 shows the current path in the ACF converter during interval 3.

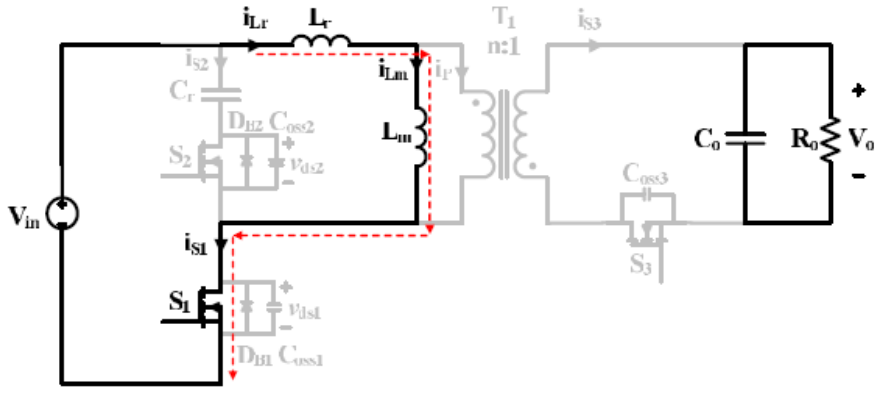


Figure 3.9: ACF during interval 3 [12].

Interval 4 [$t_3 - t_4$]: At t_3, *S1* is tuned off with ZVS and the magnetizing current starts to decrease following the Equation (3.20).

The output capacitance C_{oss1} is charged by the magnetizing current and V_{DS1} increases from *0 V* to $V_{in} + nV_o$, while C_{oss2} is discharged by the magnetizing current and V_{DS2} decreases from $V_{in} + nV_o$ to *0 V*.
Since these two capacitances are very small because of GaN devices, this time interval is short and it is possible to consider a linear charging and discharging behaviour.
The magnetizing current i_{Lm} equation can be expressed as follows, where nV_o is the voltage across the resonant capacitor and the assumption $L_m >> L_r$ is considered:

$$\begin{aligned} i_{Lm}(t) &= i_{Lm}(t_3) + \frac{1}{L_m}\int_{t_3}^{t} v_{Lm}(\tau)\, d\tau \\ &= i_{Lm}(t_3) - \frac{nV_o}{L_m} t\,. \end{aligned} \tag{3.20}$$

During this period, the resonant current i_{Lr} follows the magnetizing current i_{Lm}, the i_{S1} and the i_{S3} currents are equal to zero, and, finally, the i_{S2} current is equal to the opposite of the resonant current i_{Lr}. Therefore, no energy is transferred from the primary to the secondary side of the converter.
Figure 3.10 shows the current path in the ACF converter during interval 4.

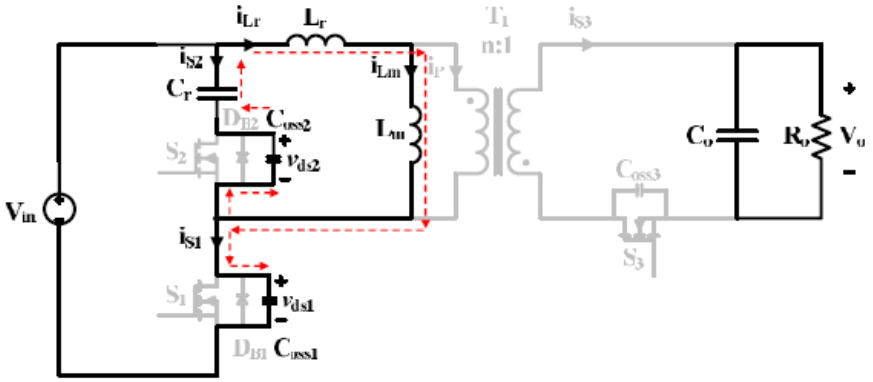


Figure 3.10: ACF during interval 4 [12].

Interval 5 [$t_4 - t_5$]: At t_4, C_{oss2} is fully discharged and V_{DS2} has reached *0 V*, hence the *S2* transistor will be turned on with ZVS.
The body diode of the *S2* transistor conducts because the i_{Lm} current is positive but the *S2* transistor is still off.
Moreover, the resonant capacitor C_r is charged by the magnetizing current and the voltage across C_r starts to increase following the Equation (3.25) until it reaches nV_o. The V_{Cr} voltage is obtained as follows:

$$\begin{cases} i_{Cr}(t) = C_r \dfrac{dV_{Cr}(t)}{dt} & (3.21) \\ i_{Cr}(t) = i_{Lm}(t) = i_{Lm}(t_4) - \dfrac{nV_o}{L_m} t & (3.22) \\ i_{Lm}(t_4) = I_{Lm4} = constant & (3.23) \end{cases}$$

$$\frac{dV_{Cr}(t)}{dt} = \frac{1}{C_r}\left(I_{Lm4} - \frac{nV_o}{L_m} t\right) \quad (3.24)$$

$$V_{Cr}(t) = \frac{1}{C_r}\int_{t_4}^{t}\left(I_{Lm4} - \frac{nV_o}{L_m}\tau\right) d\tau$$

$$= \frac{1}{C_r}\left[I_{Lm4}\,(t - t_4) - \frac{nV_o}{2L_m}(t - t_4)^2\right]. \quad (3.25)$$

Figure 3.11 shows the current path in the ACF converter during interval 5.

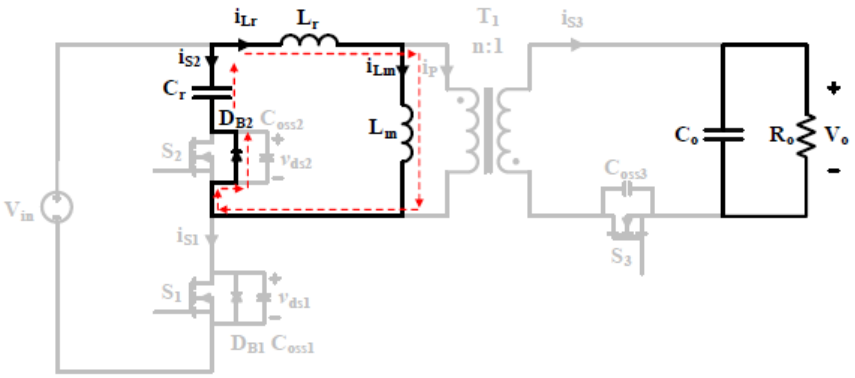


Figure 3.11: ACF during interval 5 [12].

Interval 6 [$t_5 - t_6$]: At t_5, *S2* is turned on with ZVS. The magnetizing current i_{Lm} flows through the *S2* transistor and it continues to charge the resonant capacitor C_r.
Therefore, the resonant current i_{Lr} follows the magnetizing current i_{Lm} and the i_{S2} current is equal to the opposite of the magnetizing current i_{Lm}. Since the S3 transistor is still off and the i_{Lr} and i_{Lm} currents are equal, the secondary current i_{S3} is equal to zero and no energy is transferred to the secondary side of the converter.
Figure 3.12 shows the current path in the ACF converter during interval 6.

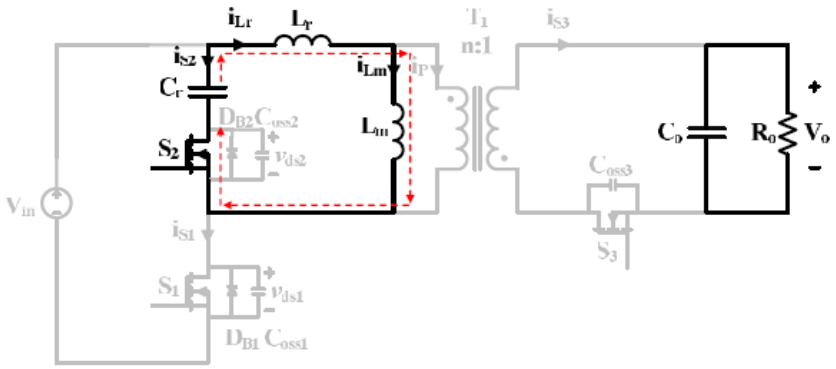


Figure 3.12: ACF during interval 6 [12].

Interval 7 [$t_6 - t_7$]: At t_6, the voltage across the resonant capacitor C_r reaches nV_o and the *S3* transistor is turned on with ZCS.
During this time interval, the positive energy accumulated into the C_r capacitor is transferred to the secondary side of the converter through the transformer.
Furthermore, the resonant inductor L_r and the resonant capacitor C_r forms a series resonant circuit, while the magnetizing inductance L_m does not participate to the resonant process because the voltage across the primary winding V_p is clamped by a constant value equal to nV_o.
The magnetizing current i_{Lm} is described by the equation obtained previously, Equation (3.20), up to the time instant t_8.
Concerning the resonant current i_{Lr}, the Equation (3.26) is obtained:

$$i_{Lr}(t) = i_{Lr}(t_6)\cos\omega_r t + \frac{V_{Lr}}{Z_r}\sin\omega_r t \tag{3.26}$$

where V_{Lr} is the voltage across the resonant inductor L_r, ω_r is the resonant frequency and Z_r is the resonant impedance computed as follows:

$$V_{Lr} = -V_p - V_{Cr} = nV_o - V_{Cr}(t_6) \tag{3.27}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{3.28}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}}. \tag{3.29}$$

The secondary current i_{S3}, which is the same of the current flowing through the *S3* transistor, is obtained in the following way:

$$i_{S3} = -ni_p = -n(i_{Lr} - i_{Lm}). \quad (3.30)$$

Finally, the i_{S2} current is now equal to the opposite of the resonant current i_{Lr}.
Figure 3.13 shows the current path in the ACF converter during interval 7.

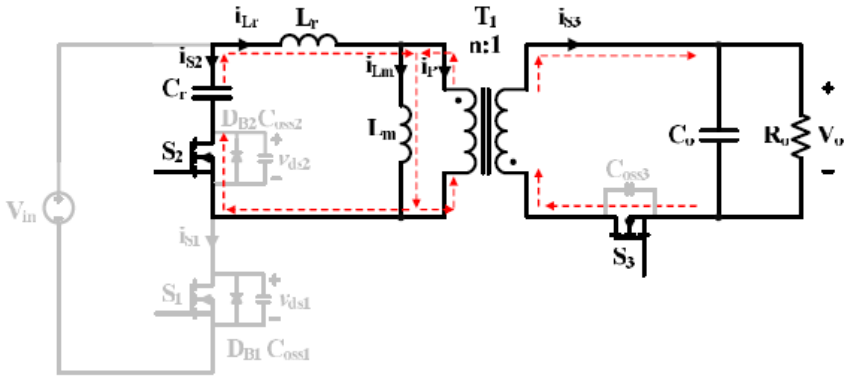


Figure 3.13: ACF during interval 7 [12].

Interval 8 [$t_7 - t_8$]: At t_5, *S3* is turned off with ZCS.
In this time interval, both the resonant current and the magnetizing current are negative. This provides both the ZVS turn-on for the *S1* transistor and the ZCS turn-off for the *S3* transistor.
Therefore, no more energy is transferred from the primary side to the secondary side of the converter.
Figure 3.14 shows the current path in the ACF converter during interval 8.

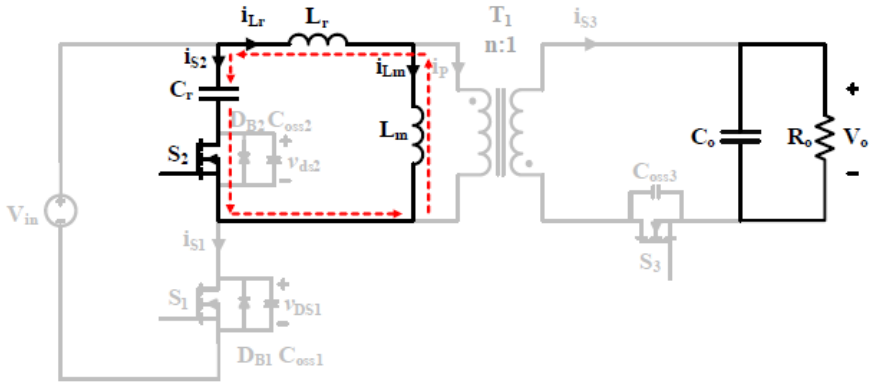


Figure 3.14: ACF during interval 8 [12].

The last consideration to conclude the generic analysis of the ACF converter is related to the last stage of the working principle. More precisely, this topology is able to cover both the SRC and the LLC region [12]. Typically, the converter operates in the SRC

region under low input voltage conditions and without considering the last time interval, while it operates in the LLC region under high input voltage conditions and considering the last time interval.
Without considering the last stage, the secondary side transistor *S3* is turned off simultaneously with the primary side transistor *S2*.

3.2.2 General design

Once the ACF converter analysis has been described in detail, a general design of this topology can be realized considering the specifications reported in Table 3.1.

P_o	65 W
V_o	19.5 V
ΔV_o	0.1 V
V_{in} (AC)	90 – 250 V
f_{sw}	1 MHz
D_{MAX}	0.45

Table 3.1: ACF design specifications.

The components that need to be selected are:

- transformer;
- primary and secondary transistors;
- resonant inductor;
- resonant capacitor;
- output capacitor.

It is necessary to define the main electrical parameters associated with each component of the converter.
The first step is to define the value of the turns ratio *n* between the transformer primary side and secondary side according to the following equation:

$$n = \frac{V_{in}}{V_o}\frac{D}{1-D} \tag{3.31}$$

where D is the duty-cycle, V_o the DC output voltage and V_{in} the DC input voltage.
The turns ratio is selected considering the maximum duty-cycle and the minimum input voltage since the maximum duty-cycle happens when the input voltage is the minimum one, hence it can be computed as follows:

$$n = \frac{V_{in,min}}{V_o}\frac{D_{MAX}}{1 - D_{MAX}} \cong 5. \tag{3.32}$$

As a next step, the magnetizing inductance L_m is derived by the equality below:

$$P_{Lm} = \frac{P_s}{\eta_{magn}} \tag{3.33}$$

where P_{Lm} is the magnetizing power, P_s is the power coming out from the secondary side of the transformer and η_{magn} is the efficiency due to the magnetic core. Typically, the value of η_{magn} is between 90% and 95%.
The expression of the maximum magnetizing power is defined as follows:

$$P_{Lm(MAX)} = \frac{1}{2} L_m I_{Lm(MAX)}^2 f_{SW} \tag{3.34}$$

where L_m is the magnetizing inductance *and* $I_{Lm(MAX)}$ is the maximum current flowing through L_m reported in the following equation:

$$I_{Lm(MAX)} = \frac{V_{in,min} D_{MAX}}{L_m f_{SW}}. \tag{3.35}$$

Then, the power coming out from the secondary side of the transformer can be defined as follows:

$$P_s = I_o(V_o + V_{DS3}) \tag{3.36}$$

where I_o is the output current, V_o the DC output voltage and V_{DS3} the drain-to-source voltage of the transistor *S3*. This last electrical parameter is defined in the following equation:

$$V_{DS3} = \frac{V_{in,min}}{n} + V_o. \tag{3.37}$$

At this point, it is possible to derive the magnetizing inductance expression reported in the Equation (3.38) by combining the expressions defined from Equation (3.33) to Equation (3.37).

$$L_m = \frac{V_{in,min}^2 D_{MAX}^2 \eta_{magn}}{2 f_{SW}(P_o + I_o V_{DS3})} \tag{3.38}$$

According to the Equation (3.38), L_m = 7 μH has been chosen.
Once the magnetizing inductance has been computed, the stress of the primary and secondary transistors can be defined. More precisely, the maximum drain-to-source voltage and the maximum drain current are needed to select the transistors from catalogues.
The maximum drain-to-source voltages for *S1* and *S2* are defined as follows:

$$V_{DS1,MAX} = V_{in,MAX} + nV_o \cong 451\ V \tag{3.39}$$

$$V_{DS2,MAX} = V_{in,MAX} + nV_o \cong 451\ V\ . \tag{3.40}$$

Then, the maximum drain current of the transistor *S1* is equal to the maximum magnetization current as follows:

$$I_{S1(MAX)} = \frac{V_{in,min}D_{MAX}}{L_m f_{SW}} \cong 8\ A\ . \tag{3.41}$$

Concerning the transistor *S2*, its maximum drain current is equal to that of the transistor *S1*, hence:

$$I_{S2(MAX)} = \frac{V_{in,min}D_{MAX}}{L_m f_{SW}} \cong 8\ A. \tag{3.42}$$

According to these electrical parameters related to the primary and secondary transistors, the GaN HEMT GS0650111L from GaN Systems has been chosen.
The main parameters of this device extracted from the datasheet are reported in Table 3.2.

$V_{DS,MAX}$	650 V
$R_{DS,ON(MAX)}$	190 mΩ
$I_{D,MAX}$	11 A
C_{OSS}	20 pF

Table 3.2: GS0650111L GaN HEMT parameters.

The maximum drain-to-source voltage of the transistor *S3* can be defined as follows:

$$V_{DS3,MAX} = \frac{V_{in,MAX}}{n} + V_o \cong 90\ V \tag{3.43}$$

and the maximum drain current is reported in the following equation:

$$I_{S3(MAX)} = \frac{2I_o}{(1 - D_{MAX})} = \frac{2P_o}{V_o(1 - D_{MAX})} \cong 12\ A\ . \tag{3.44}$$

As done for the primary side transistor, the Silicon MOSFET BSC320N20NS3 from Infineon has been chosen.
The main parameters of this device extracted from the datasheet are reported in Table 3.3.

$V_{DS,MAX}$	200 V
$R_{DS,ON(MAX)}$	32 mΩ
$I_{D,MAX}$	36 A
C_{OSS}	180 pF

Table 3.3: Silicon MOSFET BSC320N20NS3 parameters.

The next component to design is the resonant inductor L_r. It is important to highlight that the resonant inductor also includes the leakage inductance of the transformer.
In order to ensure the ZVS operation for the primary transistor *S1*, the energy stored in the resonant inductor must be higher than the energy stored in the total output capacitance $C_{oss,TOT}$ of the transistors. The total output capacitance $C_{oss,TOT}$ is equal to the parallel combination of the output capacitance of the transistor *S1* and the output capacitance of the transistor *S2* [13].
The value of the resonant inductance can be derived as follows:

$$L_r > \frac{C_{oss,TOT}\left(V_{in,MAX} + nV_o\right)^2}{I_{S1,MAX}^2} > 130\ nH. \tag{3.45}$$

The chosen value of the resonant inductance according to the Equation (3.45) is L_r = 150 nH.
The resonant capacitance C_r is chosen based on the considerations discussed below.
For first, it is necessary to consider that the i_{Lr} current, when the transistor *S2* conducts, has a resonant period equal to the following relation:

$$T_r = 2\pi\sqrt{L_r C_r}\ . \tag{3.46}$$

The resonant period reported in the Equation (3.46) should be lower than the *S2* on-time in order to accelerate the resonant current i_{Lr} to merge with the magnetizing current i_{Lm} that is negative during that period. In this way, the ZCS condition for the transistor *S3* is achieved. Therefore, the resonant capacitance C_r is computed in the following way:

$$T_r < (1 - D_{min})T_{SW} \tag{3.47}$$

$$2\pi\sqrt{L_r C_r} < (1 - D_{min})T_{SW} \tag{3.48}$$

$$L_r C_r < \left[\frac{(1 - D_{min})T_{SW}}{2\pi}\right]^2 \tag{3.49}$$

$$C_r < \frac{(1 - D_{min})^2}{(2\pi f_{SW})^2 L_r} < 103\ nF \tag{3.50}$$

where D_{min} is the minimum duty-cycle at the maximum input voltage given by:

$$D_{min} = \frac{nV_o}{V_{in,MAX} + nV_o} \cong 0.22\ . \tag{3.51}$$

The chosen normalized value of the resonant capacitance according to the E12 series is $C_r = 82$ nF.
The last component that must be designed is the output capacitor C_o and it is designed with the aim to minimize the output voltage ripple ΔV_o.
The output voltage ripple ΔV_o is given by:

$$\Delta V_o = \frac{V_0\ D\ T_{SW}}{R_o C_o} = \frac{P_0\ D\ T_{SW}}{V_o C_o} \tag{3.52}$$

and to get $\Delta V_o \leq 0.1$ V, the output capacitance C_o value can be computed as follows:

$$C_o \geq \frac{P_o D_{MAX}}{V_o f_{SW}\ 0.1V} \geq 15\ \mu F\ . \tag{3.53}$$

Finally, the chosen normalized value of the output capacitance according to the E12 series is $C_o = 22$ μF.
To conclude the generic analysis of the ACF converter, the minimum dead time can be computed:

$$t_d = \frac{\pi}{2}\sqrt{L_m C_{oss,TOT}} \cong 27\ ns \tag{3.54}$$

The dead time t_d is of greater importance to ensure the correct circuit operation and to achieve the ZVS turn-on and turn-off for the primary side switches. Furthermore, it should be long enough to allow the discharging and the charging of the output

capacitance of the transistor before the complementary one turns on or turns off. In order to meet these constraints, the dead time must be at least equal to ¼ the time period of the resonance between the magnetizing inductance and the parallel combination of the output capacitances of the primary transistors [14].

3.2.3 Primary resonant current dip effect

The primary resonant current dip, shown in Figure 3.15, is a phenomenon that affects the resonant current i_{Lr} after the *S1* turn-off. The equivalent circuit of the ACF converter after the *S1* turn-off is shown in Figure 3.16, where the output capacitance C_{oss3} of the transistor *S3* defined as C_j and the output voltage V_o are reflected to the primary side.

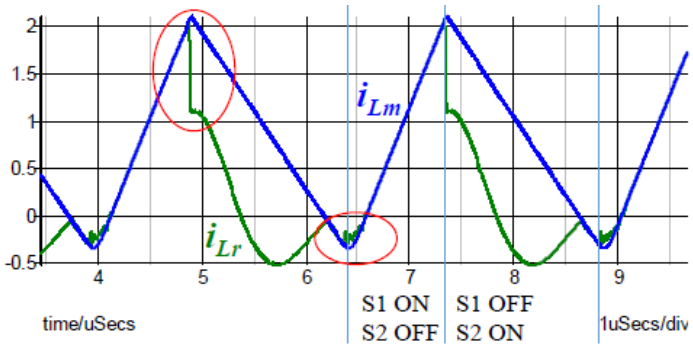


Figure 3.15: Primary resonant current dip effect [9].

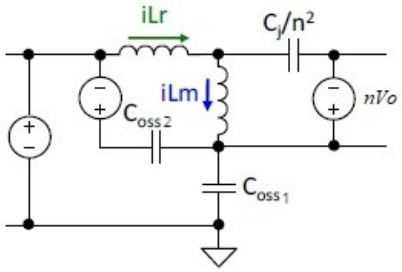


Figure 3.16: Equivalent circuit of the ACF after the S1 turn-off [15].

At *S1* turn-off, the resonant current i_{Lr} is equal to the maximum magnetizing current $I_{Lm,max}$ and i_{Lm} can be considered constant during this small transition [5].
Under the $L_m >> L_r$ assumption, the current i_{Lm} is splitted into two branches in order to charge the output capacitance C_{oss1} and to discharge the output capacitance C_{oss2}. The resonant current i_{Lr} at S1 turn-off is derived as follows [9]:

$$i_{Lr} \approx I_{Lm(\max)} \frac{2C_{oss}}{2C_{oss} + \frac{C_j}{n^2}} + (I_{Lm(\max)} \frac{\frac{C_j}{n^2}}{2C_{oss} + \frac{C_j}{n^2}}) \cos(\omega_r t) \tag{3.55}$$

where $C_{oss} = C_{oss1} = C_{oss2}$ and ω_r is the resonant frequency given by:

$$\omega_r = \frac{1}{\sqrt{\frac{2C_{oss}\frac{C_j}{n^2}}{2C_{oss} + \frac{C_j}{n^2}} L_r}}. \tag{3.56}$$

Only the output capacitances of the transistors are considered, while the other parasitic capacitances related, for example, to the transformer are not taken into account in this current dip analysis. Furthermore, this resonant phenomenon ends when the C_{oss2} is fully discharged and C_{oss1} is fully charged or when C_{oss3} is fully discharged [9].
The resonant current i_{Lr} resonates following a cosine function and the maximum current dip can be obtained by the following equation [9]:

$$I_{Lr(dip,max)} = I_{Lm(\max)} \frac{2\frac{C_j}{n^2}}{2C_{oss} + \frac{C_j}{n^2}}. \tag{3.57}$$

From Equation (3.57), it can be noted that the maximum current dip in the resonant current i_{Lr} occurs when the output capacitance of the secondary side transistor *S3* reflected to the primary side is greater than the parallel combination of the output capacitances of the primary transistors *S1* and *S2*. Therefore, in order to maximize the current dip, GaN HEMTs are more suitable for the primary switches than Silicon MOSFETs due to their low output capacitance while Silicon MOSFET is selected for the secondary switch to meet the following constraint:

$$C_j > C_{oss}. \tag{3.58}$$

The resonant primary current dip effect has good consequences in the ACF converter behaviour because it allows to reduce the conduction losses of the *S2* transistor. This happens because the current dip sets an initial condition for the resonant process during the *S2* on period. In fact, higher current dip means lower RMS resonant current i_{Lr} and, during the *S2* on period, it is equal to the current that flow through this transistor. Therefore, the conduction losses related to the *S2* transistor can be significantly reduced.

Another positive effect of the current dip is related to the transfer of energy to the secondary side. More precisely, if $I_{Lr(dip,max)}$ is very large, the RMS resonant current i_{Lr} is lower and a large amount of current is delivered from the primary side to the secondary side during the resonant process.
To take advantage of these effects, the $(C_j/n^2)/C_{oss}$ ratio is set equal to 3. Therefore, since the MOSFET chosen in the previous section has a typical output capacitance C_j equal to 135 pF and the primary side GaN devices have an output capacitance C_{oss} equal to 20 pF, an extra capacitance with a value equal to 1.32 nF in parallel combination with the MOSFET must be added. In this way, the total output capacitance of the secondary side MOSFET is approximately equal to 1.5nF and the current dip effect significantly affects the primary resonant current i_{Lr}.

3.2.4 Secondary side resonance scheme

The ACF efficiency and the conduction losses related to the switches can be further improved by implementing the secondary side resonance scheme [9],[15]. This method consists in involving the output capacitance C_o in the resonant process during the conduction period of the transistors *S2* and *S3*.
A small output capacitance C_o is used as the resonant element, typically a ceramic capacitor with a low ESR. The resonant clamp capacitance C_r, instead, is larger with respect to the conventional primary side resonance scheme and the voltage across it is considered constant. Moreover, the reflected output voltage to the primary side is lower than the voltage across the resonant clamp capacitance C_r.
During the *S1* on period the operation of the converter is the same as the conventional case while, during *S2* and *S3* on period, the resonant inductor L_r resonates with both the output capacitance C_o and the resonant clamp capacitance C_r. At the beginning of the *S2* and *S3* on period, the resonant current i_{Lr} further dips down with respect to the current dip effect still reducing the RMS resonant current i_{Lr} and the conduction losses related to the transistor *S2*. Moreover, during this period, the resonant current i_{Lr} is always lower than the magnetizing current i_{Lm} and hence the secondary current i_{S3} will not double dip to zero. This effect allows to reduce the conduction losses related to the transistor *S3* and to improve the whole efficiency of the ACF converter.
The equivalent resonant capacitance that participates in the resonance is given by:

$$C_{eq} = \frac{C_r \frac{C_o}{n^2}}{C_r + \frac{C_o}{n^2}}. \tag{3.59}$$

The ACF converter current and voltage waveforms with the secondary side resonant scheme are shown in Figure 3.17.

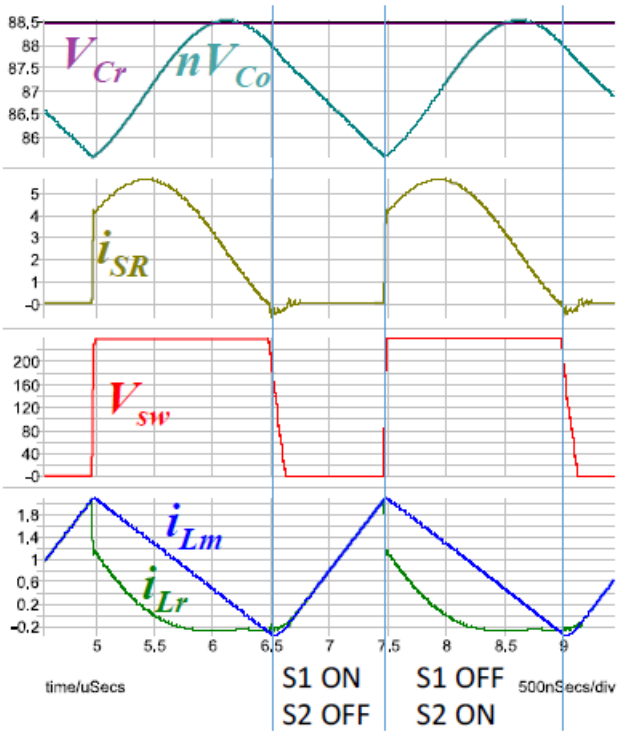


Figure 3.17: ACF converter waveforms with secondary side resonance scheme [9].

Finally, to implement the secondary side resonant scheme in the general design of the ACF converter, the following values of the converter elements have been computed:

- C_r = 560 nF;
- L_r = 5.6 nH;
- C_o = 22 uF.

The resonant clamp capacitance C_r has been increased with respect to the general design in order to involve the output capacitor C_o in the resonance according to the Equation (3.59).
Then, the resonant inductance L_r value is derived from the Equation (3.50), knowing the value of the resonant clamp capacitance C_r.

3.2.5 Ideal circuits simulations

In this section, the *LTspice* software is used to perform ideal circuit simulations and to analyse their results with respect to the theoretical analysis done in the previous section.
All simulations are performed with a transient analysis (*.tran*) and the ideal model of the converter components are considered except for the primary and secondary side transistors. The latter are implemented by considering the output capacitance, the body

diode, the on resistance, the off resistance and the threshold voltage extracted from the datasheet of the selected component. The main values that characterize the transistors are reported in Table 3.4 and the chosen values for the other components are reported in Table 3.5.

	Primary side transistors (GaN HEMT)	*Secondary side transistor (Silicon MOSFET)*
$V_{DS,MAX}$	650 V	200 V
$R_{DS,ON}$	150 mΩ	27 mΩ
C_{oss}	20 pF	135 pF

Table 3.4: Primary and secondary side transistors parameters.

	Transformer	*Resonant Clamp Capacitor* C_r	Output Capacitor C_o
General design	L_m =7 µH L_r = 150 nH N = 5	C_r = 82 nF	C_o = 22 µF
Design with current dip effect and secondary side resonance scheme	L_m =7 µH L_r = 5.6 nH N = 5	C_r = 560 nF	C_o = 22 µF

Table 3.5: ACF component values.

Figure 3.18 shows the schematic of the general design of the ACF converter implemented in *LTspice* for the simulations, while Figure 3.19 shows the schematic of the ACF converter with both current dip effect and secondary side resonance scheme.

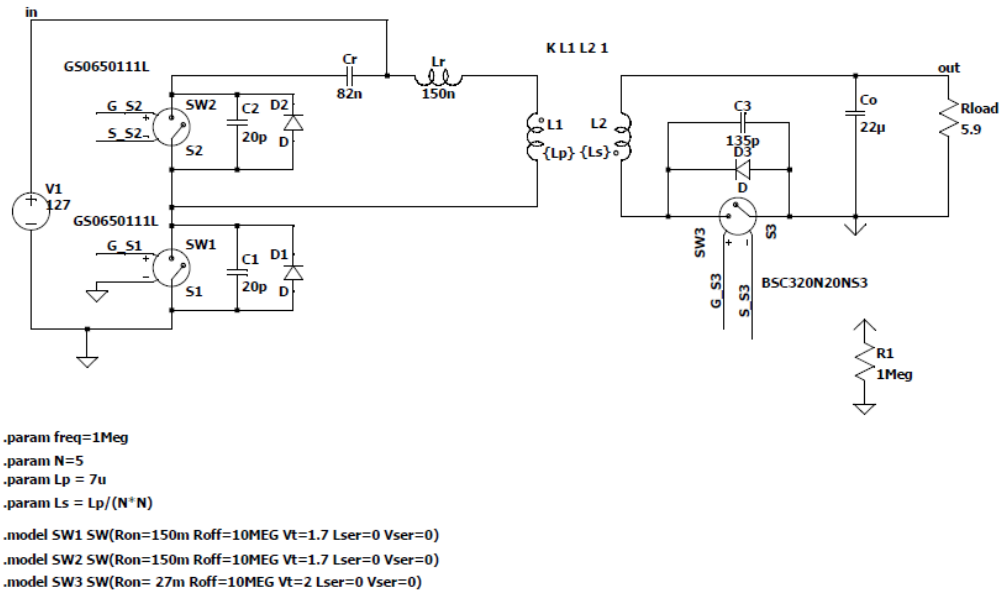


Figure 3.18: Schematic of the general design of the ACF converter implemented in LTspice.

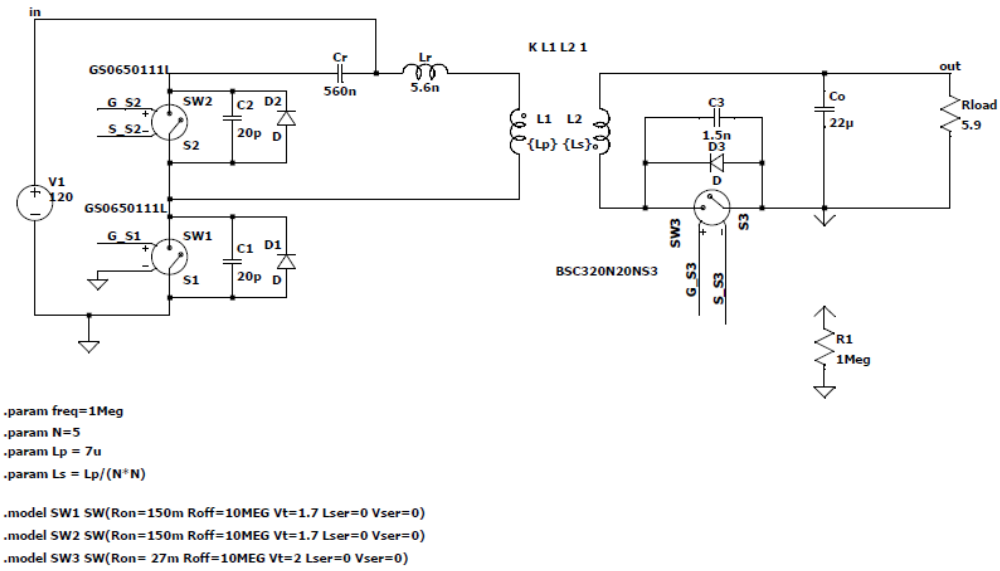


Figure 3.19: Schematic of the ACF converter with both current dip effect and secondary side resonance scheme implemented in LTspice.

Table 3.6 shows the simulations results of the four different designs of the ACF converter focusing on the efficiency and on the RMS resonant current measurements. It confirms how the current dip effect and the secondary side resonant scheme

combination reduces the RMS resonant current and consequently the efficiency of the ACF increases.

	ACF general design	*ACF with the current dip effect*	*ACF with the secondary side resonance scheme*	*ACF with both current dip effect and secondary side resonance scheme*
Efficiency	97 %	97.7 %	97.4 %	98 %
$I_{Lr(RMS)}$	2.8 A	2.68 A	2.27 A	2.24 A

Table 3.6:Efficiency and RMS resonant current results from the ACF ideal circuit simulations.

In the following, the current and voltage waveforms of the circuit simulations are reported. Figure 3.20 shows the simulation results of the ACF converter general design, while Figure 3.21 shows the simulation results of the ACF converter with both current dip effect and secondary side resonance scheme.
As it can be seen in both figures, the *S1* and *S2* transistors are turned on and off with ZVS thus eliminating the switching losses related to them.
Furthermore, in the Figure 3.20, the *S3* transistor is turned on with ZCS when the voltage across the resonant capacitor has reached its maximum value and also turned off with ZCS when the capacitor has been completely discharged. Figure 3.21, instead, shows that the ACF design with both the current dip effect and the secondary side resonance scheme has been performed by turning on and off the *S2* and the *S3* transistors simultaneously to transfer more energy to the secondary side of the converter. Also in this case, the switching of the transistor occurs with ZCS eliminating the switching losses.
Moreover, in Figure 3.21 it is possible to see a dip in the resonant current i_{Lr} after the *S1* turn off, the current dip reduces the RMS resonant current $i_{Lr,rms}$ and more current is transferred from the primary side to the secondary side increasing hence the efficiency of the converter.

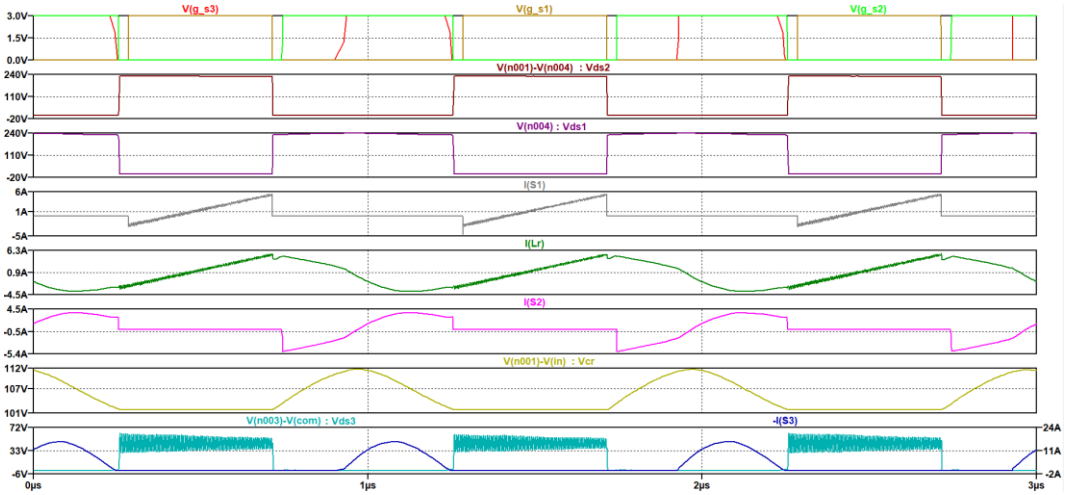


Figure 3.20: Ideal circuit simulation results of the general design of the ACF converter.

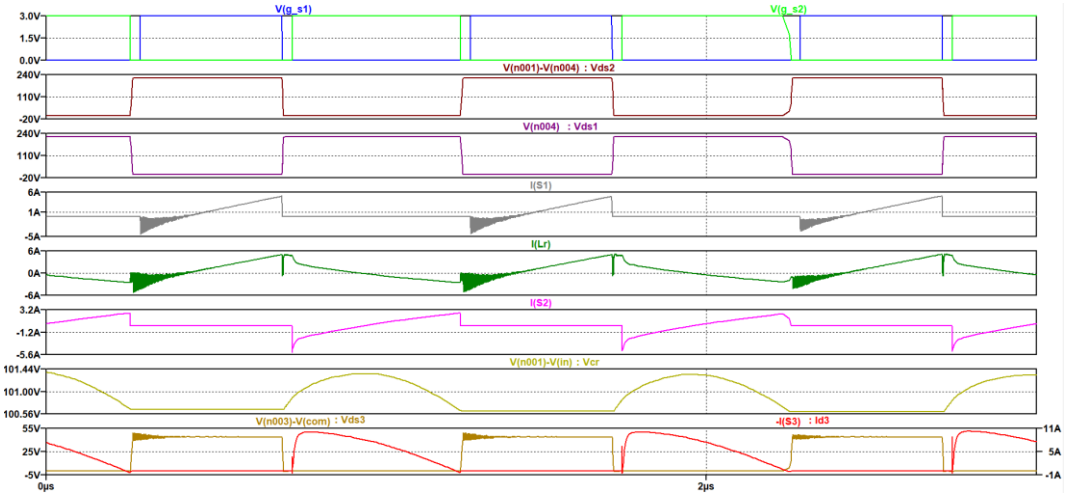


Figure 3.21: Ideal circuit simulation results of the ACF converter with both current dip effect and secondary side resonance scheme.

3.2.6 Simulations with real component models

After the ideal circuit simulations, the ACF converter schematic is completed with the real *LTspice* models of all the components that constitute the circuit. However, only the coupled inductors are still considered ideal since during its design it is difficult to estimate their parasitic elements.

Before proceeding with the real simulations, the real components have to be selected from catalogues. Then, the *LTspice* model can be extracted and imported in the software to design the circuit and to execute the simulations.
The primary and secondary side transistors have already been selected in the Section 3.2.2.
Then, the resonant clamp capacitor and the output capacitance must be selected.
Concerning the resonant clamp capacitor, the voltage across the capacitor is equal to output voltage reflected to the primary side, hence $V_{Cr} = 97.5$ V.
Focusing, now, on the output capacitor, the maximum voltage across it and the ESR must be derived. The maximum voltage across C_o is equal to the output voltage and the ESR is computed as the ratio between the output voltage ripple and the maximum current that flow through the secondary side transistor ($ESR = \Delta V_o / I_{S3(MAX)}$). Therefore, the computed ESR is equal to 3.7 mΩ.
Since this ESR value is very small for an electrolytic capacitor, a ceramic capacitor must be chosen. Compared with an electrolytic output capacitor, the advantage of the ACF using an output capacitor with a low ESR like a polymer or ceramic capacitor is to minimize the output voltage ripple.

According to these considerations, the resonant clamp capacitor C_r can be chosen:

- The KEMET X7R C1825C563K2RAC with a capacitance value equal to 56 nF rather than 82 nF was chosen for the general design, after several value adjustments during the simulations, in order to obtain ZCS turn-off for the secondary side transistor.
- The KEMET X7R C1210C823K2RAC with a capacitance value equal to 82 nF was chosen for the ACF design with the current dip effect.
- The KEMET X7R C2220C564K2RAC with a capacitance value equal to 560 nF was chosen for the ACF design with the secondary side resonance scheme and for the design with both the current dip effect and the secondary side resonance scheme.

Now, focusing on the output capacitor C_o, the following models can be chosen:

- The Wurth Elektronik X5R 885012109014 WCAP-CSGP with a capacitance value equal to 22 μF, was chosen for the ACF general design, for the design with the current dip effect and for the design with the secondary side resonance scheme. The ESR of this component is equal to 2.7 mΩ and its maximum working voltage is equal to 25 V.
- The KEMET X5R C1210C825K3PAC with a capacitance value equal to 8.2 μF was chosen for the design with both the current dip effect and the secondary side resonance scheme. The ESR of this component is equal to 6.8 mΩ and its maximum working voltage is equal to 25 V. Two capacitors in a parallel

combination are used to have a total capacitance higher than 15 μF and a ESR value close to 3.7 mΩ. This choice was adopted after several C_o value adjustments during simulations to achieve ZCS turn-off for the secondary side transistor.

Moreover, to implement the current dip, since the secondary side transistor which was chosen has an output capacitance equal to 180 pF, an extra capacitor with a value equal to 1.32 nF must be added in parallel combination with the transistor.
Table 3.7 shows the real simulations results of the four different designs of the ACF converter focusing on the efficiency and on the RMS resonant current measurements.

	ACF general design	*ACF with the current dip effect*	*ACF with the secondary side resonance scheme*	*ACF with both current dip effect and secondary side resonance scheme*
Efficiency	95.2 %	96.3 %	96.7 %	97%
$I_{Lr(RMS)}$	2.7 A	2.1 A	2.3 A	2.2 A

Table 3.7: Efficiency and RMS resonant current results from the ACF real circuit simulations.

In the following, the current and voltage waveforms of the circuit simulations are reported. Figure 3.22 shows the real simulation results of the ACF converter general design, while Figure 3.23 shows the real simulation results of the ACF converter with both current dip effect and secondary side resonance scheme.
The waveforms reported in these figures confirm the results obtained with the ideal circuit simulations regarding the ZVS turn on and turn off for both the *S1* and the *S2* transistors. In addition to the ideal circuit simulations, the real ones show that the ACF design with both current dip effect and secondary side resonance scheme eliminates the double switching of the secondary side switch shown in the I_{d3} waveform in Figure 3.22. This has a positive impact on the efficiency since it eliminates the losses associated with that double switching.

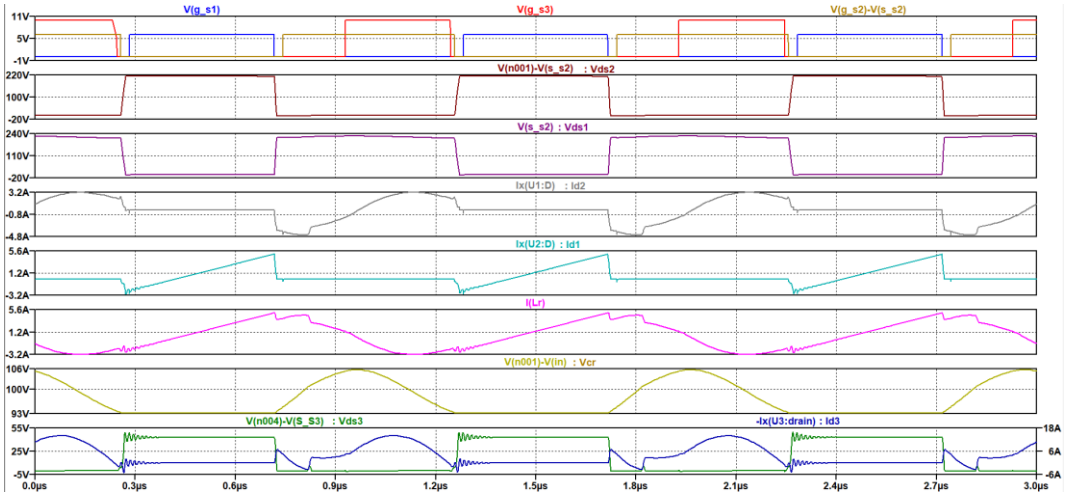


Figure 3.22: Real circuit simulation results of the general design of the ACF converter.

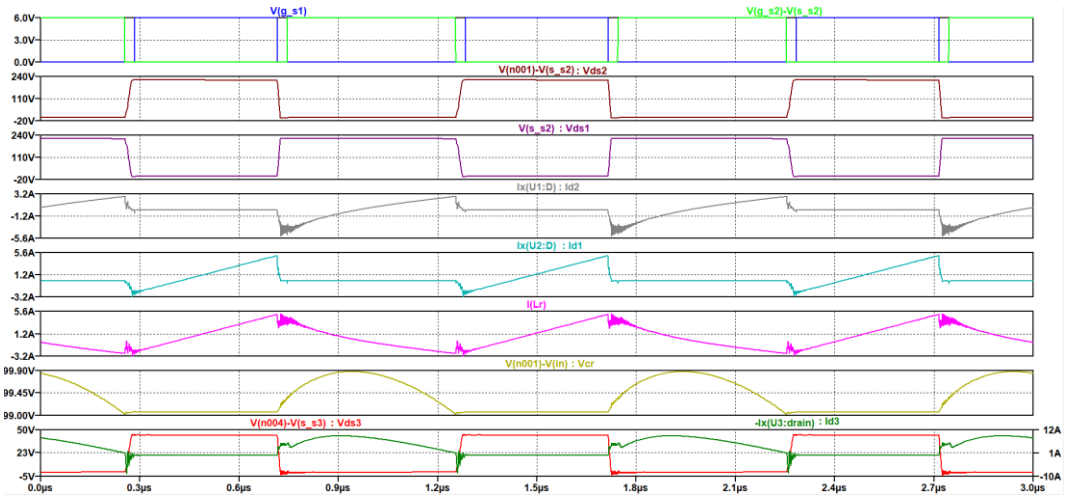


Figure 3.23: Real circuit simulation results of the ACF converter with both current dip effect and secondary side resonance scheme.

Figure 3.24 shows the schematic of the general design of the ACF converter implemented in *LTspice* with the real models. The other circuits are realized in the same way.

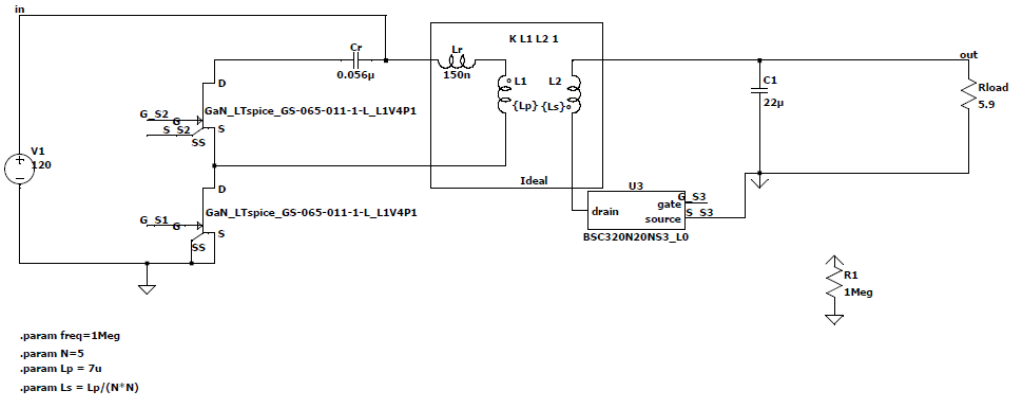


Figure 3.24:Schematic of the general design of the ACF converter implemented in LTspice with real component models.

At this point, considerations about the power dissipation by each component of the circuit can be done. The power dissipated by each element is computed directly from the *LTspice* software and the results are shown in Figure 3.25 and Figure 3.26. The pie charts reported in these figures show that the component that dissipate the most power is the secondary side transistor, that is the MOSFET S3. This is due to the high RMS current and its on resistance, therefore the solution to reduce the power dissipation related to this transistor is to select a device characterized by a lower on resistance. In this way, the efficiency of the
ACF converter can increase.

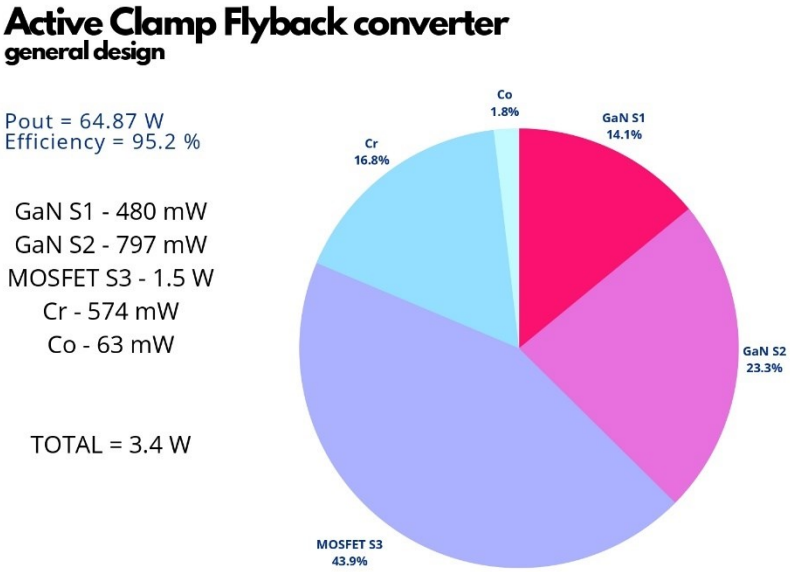


Figure 3.25: ACF general design power dissipation.

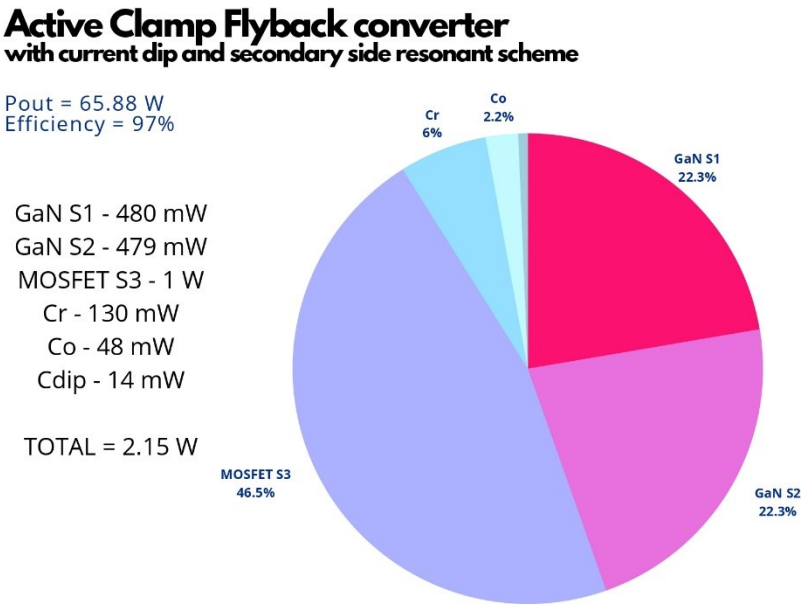


Figure 3.26: ACF with current dip and secondary side resonance scheme power dissipation.

3.3 Asymmetrical Half Bridge Flyback converter

The other improved flyback converter topology found in the literature is the AHBF converter shown in Figure 3.27. The working principle and the design equations are reported in detail in this section.

The primary side of the circuit is composed by the main switch *S2* and the auxiliary switch *S1*. Both *S1* and *S2* are GaN HEMT switches, and their body diodes and output capacitances are considered. V_{in} is the DC input voltage.

Then, C_r is the resonant capacitor, L_r is the resonant inductance that also includes the leakage inductance of the transformer and L_m is the magnetizing inductance.

The secondary side of the converter is composed by the synchronous rectifier (SR) switch *SR* that is a Silicon MOSFET device. Its output capacitance C_{sj} is also considered. Finally, C_o is the output capacitor and R_o represents the equivalent load resistance.

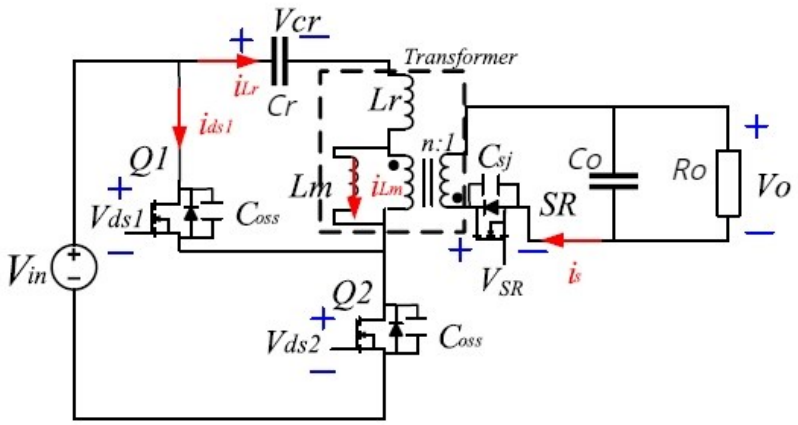


Figure 3.27: Asymmetrical Half Bridge Flyback converter schematic [8].

3.3.1 Circuit analysis

First of all, the circuit analysis is carried out on the basis of the following assumptions [8]:

- steady state operation;
- the magnetizing inductance L_m is greater than the resonant inductance L_r, and the secondary leakage inductance is neglected;
- the resonant capacitor C_r is considered a constant voltage source;
- the output capacitor C_o is considered large enough such that the output voltage can be a constant DC voltage with negligible ripple.

As a first step in circuit analysis, it is necessary to derive the conversion ratio of the AHBF converter. To compute it, two intervals must be considered while dead times are ignored.

- **T1 period**: *S2* transistor is ON, *S1* and *SR* transistors are OFF.
- **T2 period**: *S2* transistor is OFF, *S1* and *SR* transistors are ON.

The **T1 period** is the charging phase during which the magnetizing inductance L_m is charged and no energy is transferred to the secondary side.
During this period, the drain-to-source voltage across the *S1* transistor can be defined through the following equation:

$$V_{DS1} = V_{in} \tag{3.60}$$

The same voltage can be also defined by the equation below under the $L_r << L_m$ assumption:

$$V_{DS1} = V_p(T1) + V_{Cr} \tag{3.61}$$

where V_{Cr} is the voltage across the resonant capacitance C_r.
By combining Equation (3.60) and Equation (3.61), the voltage across the primary winding $V_{p(T1)}$ is given by:

$$V_P(T1) = V_{in} - V_{C_r}. \tag{3.62}$$

The **T2 period** is the discharging phase during which the magnetizing inductance L_m is discharged and the energy is transferred from the primary side to the secondary side of the isolated resonant power converter.
The drain-to-source voltage across the *S2* transistor can be defined by the following equation:

$$V_{DS2} = V_{in}. \tag{3.63}$$

The voltage across the primary winding during the T2 time interval $V_{p(T2)}$ can be derived by the equations below:

$$V_p(T2) = -V_{Cr} \tag{3.64}$$

$$V_p(T2) = nV_s \tag{3.65}$$

$$V_s = -V_o \tag{3.66}$$

where n is the turns ratio of the coupled inductors equal to N_p/N_s, V_s is the voltage across to the secondary winding and V_o is the DC output voltage.
At this point, Equation (3.66) is substituted in the Equation (3.65) in order to obtain the voltage across the primary winding during T2 period.

$$V_p(T2) = -nV_o. \tag{3.67}$$

Then, Equation (3.67) is substituted in the Equation (3.64) to obtain the voltage across the resonant capacitance:

$$V_{Cr} = nV_o. \tag{3.68}$$

From the Equation (3.60) and (3.63), it can be noted that the voltage stress of the main and auxiliary switches depends only on the input voltage V_{in}. This means much more margin for the selection of the primary switches with respect to the ACF converter, therefore this represents a clear advantage of the AHBF topology.
Moreover, the voltage stress of the synchronous rectifier *SR* transistor can be computed during T1 period as follows:

$$
\begin{aligned}
V_{DSR} &= V_S + V_o \\
&= \frac{V_p(T1)}{n} + V_o \\
&= \frac{V_{in}}{n} - \frac{V_{C_r}}{n} + V_o \\
&= \frac{V_{in}}{n} - \frac{nV_o}{n} + V_o \\
&= \frac{V_{in}}{n}.
\end{aligned}
\tag{3.69}
$$

V_{DSR} depends only on the input voltage reflected to the secondary side, as well as for the primary switches this means much more margin to select the secondary switch.
To compute the conversion ratio of the AHBF converter, the volt-second balance is applied to the voltage across the primary winding during the time intervals T1 and T2. The conversion ratio is derived as follows, where *D* is the duty cycle of the transistor *S2* and *T* is the whole period.

$$
\begin{cases}
V_p(T1)T1 + V_p(T2)T2 = 0 & (3.70) \\
D = \dfrac{T1}{T} = \dfrac{T1}{T1 + T2} & (3.71)
\end{cases}
$$

$$(V_{in} - V_{C_r})T1 - V_{C_r}T2 = 0 \tag{3.72}$$

$$(V_{in} - nV_o)D = nV_o(1 - D) \tag{3.73}$$

$$V_{in}D = nV_o\,. \tag{3.74}$$

Finally, the expression of the conversion ratio of the AHBF converter is the following:

$$\frac{V_o}{V_{in}} = \frac{D}{n}. \tag{3.75}$$

The analysis of the working principle is based on six intervals from t_0 to t_6. The current and voltage steady-state waveforms of the AHBF converter are shown in Figure 3.28.

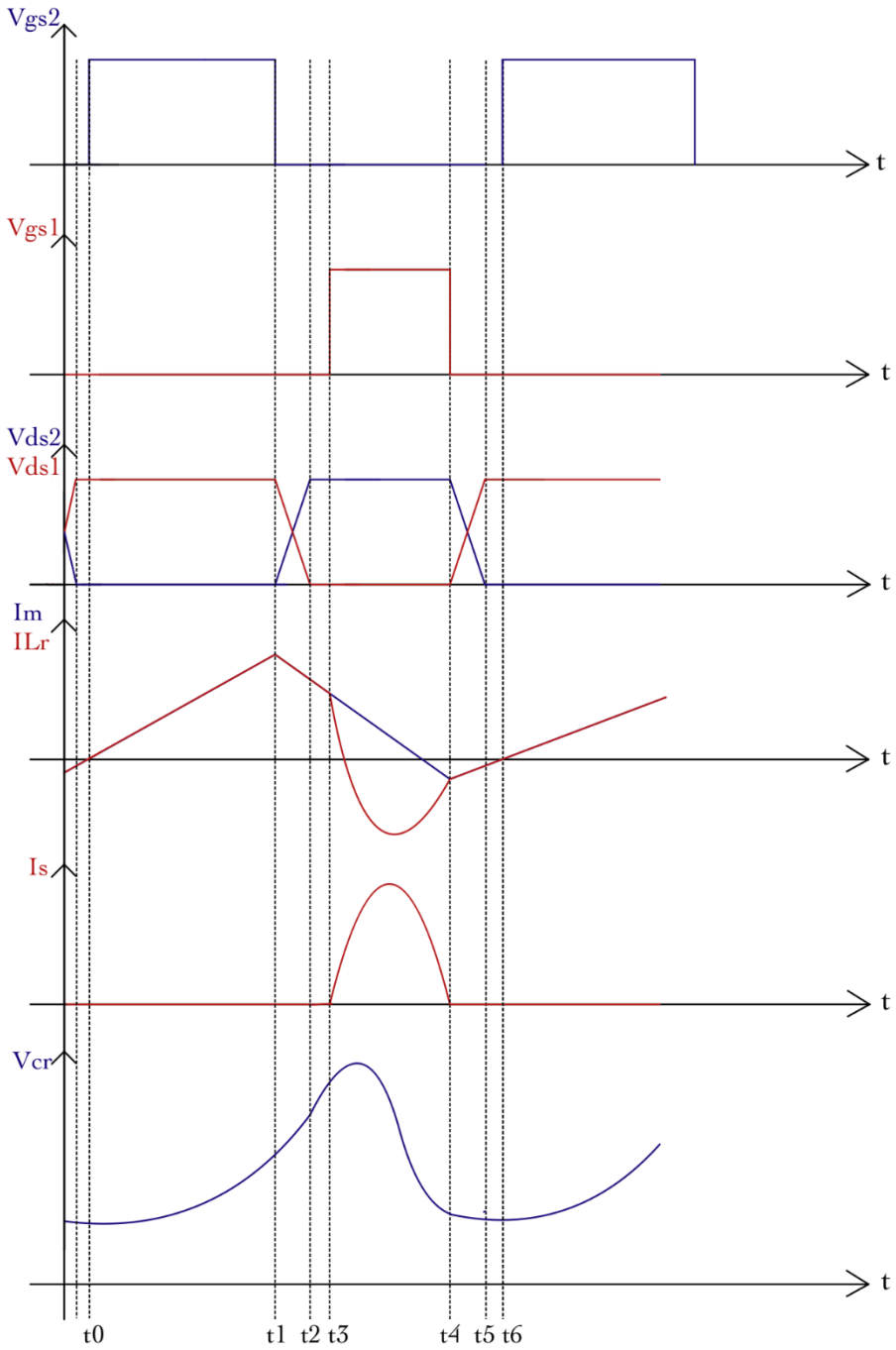


Figure 3.28: Current and voltage steady-state waveforms of the AHBF converter.

Interval 1 [$t_0 - t_1$]: At t_0, *S2* turns on with ZVS and both the *S1* and the *SR* transistors are off. During this period, the input voltage V_{in} charges the magnetizing inductance L_m and the magnetizing current i_{Lm} increases linearly according to the following equation:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{1}{L_m}\int_{t_o}^{t} v_{Lm}(\tau)\, d\tau$$
$$= i_{Lm}(t_0) + \frac{V_{in} - V_{C_r}}{L_m + L_r} t\,. \tag{3.76}$$

Under the $L_m >> L_r$ assumption, the Equation (3.76) can be simplified as follows:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_{in} - V_{C_r}}{L_m} t\,. \tag{3.77}$$

The resonant current i_{Lr} and the current i_{S2} follow the magnetizing current i_{Lm}, while the current i_{S1} is equal to zero. Since the resonant current i_{Lr} is equal to the magnetizing current i_{Lm}, the primary current i_p, that is the difference between i_{Lr} and i_{Lm}, is equal to zero. Therefore, the current i_{SR} in the secondary winding is equal to zero and no energy is transferred from the primary to the secondary side of the converter.
Moreover, the voltage across the primary winding V_p is equal to:

$$V_p = V_{L_m} = V_{in} - V_{C_r} \tag{3.78}$$

then, the voltage stress of the transistor *S1* is equal to V_{in} and the voltage stress of the transistor *SR* is equal to V_{in}/n.
The voltage across the resonant capacitor C_r can be computed as follows [16]:

$$V_{C_r}(t) = V_{in} - [V_{in} - V_{C_r}(t_0)]\cos(\omega_{r_1}(t - t_0)) \tag{3.79}$$

where

$$\omega_{r_1} = \frac{1}{\sqrt{(L_m + L_r)C_r}} \tag{3.80}$$

Figure 3.29 shows the equivalent circuit of the AHBF converter during interval 1.

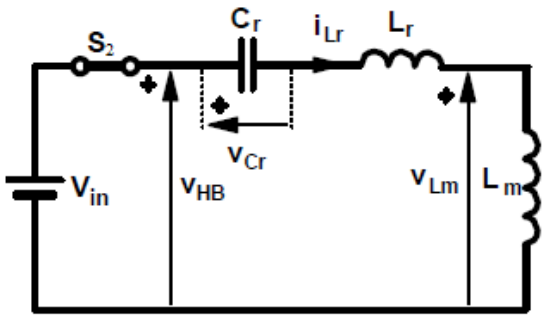


Figure 3.29: AHBF during interval 1 [16].

Interval 2 [$t_1 - t_2$]: At t_1, *S2* is turned off with ZVS and the magnetizing current starts to decrease following the Equation (3.81). Both the *S1* and the *SR* transistors are still off.
The output capacitance C_{oss2} is charged by the magnetizing current and V_{DS2} increases from *0 V* to V_{in}, while the output capacitance C_{oss1} is discharged by the magnetizing current and V_{DS1} decreases from V_{in} to *0 V*.
The primary transistors are GaN HEMT devices with very small output capacitances, therefore the charging and the discharging times are short and it is possible to consider a linear charging and discharging behaviour.
During this time interval, the magnetizing current i_{Lm} equation is given by:

$$\begin{aligned} i_{Lm}(t) &= i_{Lm}(t_1) + \frac{1}{L_m}\int_{t_1}^{t} v_{Lm}(\tau)\, d\tau \\ &= i_{Lm}(t_1) - \frac{nV_o}{L_m}t\,. \end{aligned} \tag{3.81}$$

The resonant current i_{Lr} continues to follow the magnetizing current i_{Lm} and no energy is transferred from the primary to the secondary side of the converter.
Figure 3.30 shows the equivalent circuit of the AHBF converter during interval 2.

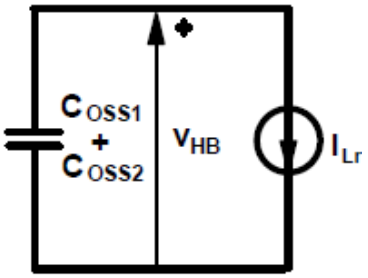


Figure 3.30: AHBF during interval 2 [16] .

Interval 3 [$t_2 - t_3$]: At t_2, C_{oss1} is fully discharged and V_{DS1} has reached *0 V*, hence the transistor *S1* will be turned on with ZVS. Conversely, C_{oss2} is fully charged and V_{DS2} has reached V_{in}.
During this period, all the transistors are still off.
The body diode D_{S1} of the *S1* transistor starts to conduct because the voltage V_{gs1} is equal to zero. Moreover, the resonant capacitor C_r is charged by the magnetizing current and the voltage across it slightly increases up to t_3.
The resonant current i_{Lr} continues to follow the magnetizing current i_{Lm}, while the current i_{SR} is still equal to zero and no energy is transferred from the primary to the secondary side of the converter.

Figure 3.31 shows the equivalent circuit of the AHBF converter during interval 3.

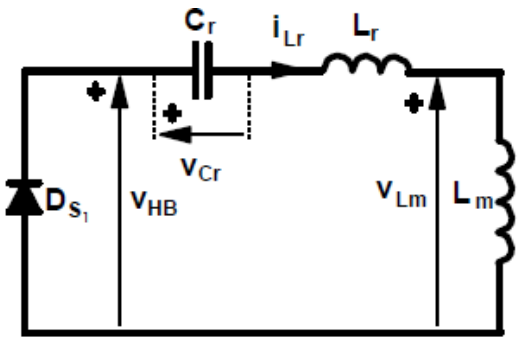


Figure 3.31: AHBF during interval 3 [16].

Interval 4 [$t_3 - t_4$]: At t_3, *S1* is turned on with ZVS and SR is turned on with ZCS. During this time interval, the positive energy accumulated into the resonant capacitor C_r is transferred to the secondary side of the converter through the transformer and the voltage across it starts to decrease.
The resonant inductor L_r and the resonant capacitor C_r forms a resonant circuit, while the magnetizing inductance L_m does not participate to the resonant process because the voltage across it is clamped by a constant value equal to the output voltage V_o reflected to the primary side.
The magnetizing current i_{Lm} continues to decrease according to the previous Equation (3.81), while the resonant current i_{Lr} is no more equal to i_{Lm} and it is obtained by the following equation:

$$i_{L_r}(t) = I_{Lr}(t_3)\cos(\omega_{r2}t) + (nV_o - V_{Cr}(t_3))\sqrt{\frac{C_r}{L_r}}\sin(\omega_{r2}t) \tag{3.82}$$

where

$$\omega_{r2} = \frac{1}{\sqrt{C_r L_r}}. \tag{3.83}$$

The i_{S1} current is now equal to the opposite of the resonant current i_{Lr}.
Finally, the secondary current i_{SR}, which is the same of the current flowing through the *SR* transistor, is obtained in the following way:

$$i_{SR} = -ni_p = -n(i_{Lr} - i_{Lm}). \tag{3.84}$$

Figure 3.32 shows the equivalent circuit of the AHBF converter during interval 4.

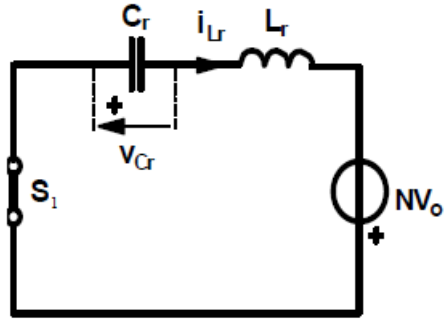


Figure 3.32: AHBF during interval 4 [16].

Interval 5 [$t_4 - t_5$]: At t_4, *S1* is turned off with ZVS and *SR* is turned off with ZCS. The *S2* transistor is still off.

Furthermore, at t_4, the input voltage V_{in} starts to charge the magnetizing inductance L_m and the magnetizing current i_{Lm} increases following the Equation (3.77) with a different initial condition.

The output capacitance C_{oss1} is charged by the magnetizing current and V_{DS1} increases from *0 V* to V_{in}, while the output capacitance C_{oss2} is discharged by the magnetizing current and V_{DS2} decreases from V_{in} to *0 V*.

This interval ends when C_{oss2} is fully discharged and hence the transistor *S2* will be turned on with ZVS.

During this period, the resonant current i_{Lr} follows the magnetizing current i_{Lm}. Since the resonant current i_{Lr} is equal to the magnetizing current i_{Lm}, the primary current i_p is equal to zero and no energy is transferred from the primary to the secondary side of the converter.

Figure 3.33 shows the equivalent circuit of the AHBF converter during interval 5.

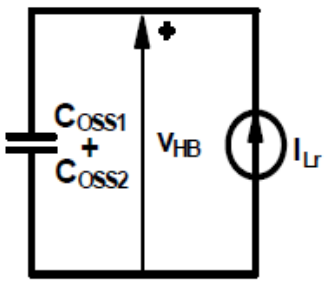


Figure 3.33: AHBF during interval 5 [16].

Interval 6 [$t_5 - t_6$]: during this time interval, the transistors are still off.

The magnetizing current i_{Lm} continues to increase linearly. Since both the *S1* and *S2* transistors are off, i_{Lm} flows through the body diode D_{S2} of the *S2* transistor because the voltage V_{gs2} is equal to zero.

The resonant current i_{Lr} follows the magnetizing current i_{Lm}, the current flowing through D_{S2} is equal to -i_{Lr}, while the i_{S1} and i_{SR} currents are zero.
The i_{Lm} equation during this interval is the same as the Equation (3.77) with different initial condition as follows:

$$i_{Lm}(t) = i_{Lm}(t_5) + \frac{V_{in} - V_{C_r}}{L_m} t \,. \tag{3.85}$$

Figure 3.34 shows the equivalent circuit of the AHBF converter during interval 6.

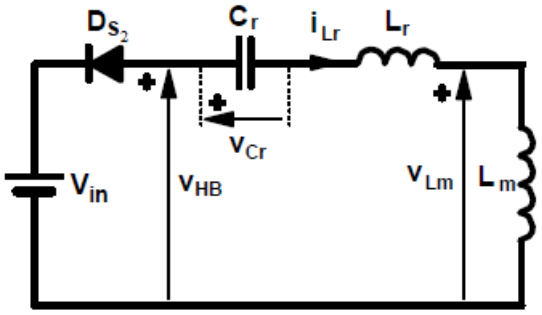


Figure 3.34: AHBF during interval 6 [16].

3.3.2 General design

As done in the previous section, once the AHBF converter analysis has been described in detail, a general design is carried out considering the specifications reported in Table 3.8.

P_o	65 W
V_o	19.5 V
ΔV_o	0.1 V
V_{in} (AC)	90 – 250 V
f_{sw}	1 MHz
D_{MAX}	0.75

Table 3.8: AHBF design specifications.

The components that need to be selected are:

- transformer;
- primary and secondary transistors;
- resonant inductor;
- resonant capacitor;
- output capacitor.

In this section, the main electrical parameters associated with each component of the converter will be defined.
Firstly, the value of the turns ratio n between the transformer primary side and secondary side is computed according to the following equation:

$$n = \frac{V_{in}}{V_o} D \tag{3.86}$$

where D is the duty-cycle, V_o the DC output voltage and V_{in} the DC input voltage.
The turns ratio is selected considering the maximum duty-cycle and the minimum input voltage since the maximum duty-cycle happens when the input voltage is the minimum one, hence it can be computed as follows:

$$n = \frac{V_{in,min}}{V_o} D_{MAX} \cong 5. \tag{3.87}$$

The next step is to derive the magnetizing inductance L_m. In order to achieve ZVS turn on for the transistor *S2*, L_m must be designed to provide enough negative magnetizing current i_{Lm} [16], therefore the minimum value of i_{Lm} has to be negative:

$$I_{Lm_{min}} < 0\,. \tag{3.88}$$

The maximum and the minimum expressions of the magnetizing current are obtained as:

$$I_{Lm_{MAX}} = I_{Lm_{AVG}} + \frac{\Delta I_{Lm}}{2} = \frac{I_o}{n} + \frac{nV_o}{2L_m}(1-D)T_s \tag{3.89}$$

and

$$I_{Lm_{min}} = I_{Lm_{AVG}} - \frac{\Delta I_{Lm}}{2} = \frac{I_o}{n} - \frac{nV_o}{2L_m}(1-D)T_s \tag{3.90}$$

where ΔI_{Lm} is the peak-to-peak value of the magnetizing current.
Using the Equation (3.88) and the Equation (3.90), the magnetizing inductance L_m is obtained as follows:

$$L_m < \frac{n^2 V_o (1-D_{MAX})}{2 I_0 f_{SW}} < 18\,\mu H \tag{3.91}$$

The value of the magnetizing inductance L_m needed to achieve ZVS turn-on for the transistor *S2* and chosen according to the Equation (3.91) and is L_m = 10 μH.
Once the magnetizing inductance has been computed, the stress of the primary and secondary transistors can be defined to select the transistors from catalogues.

The maximum drain-to-source voltages for *S1* and *S2* are defined as follows:

$$V_{DS1,MAX} = V_{in,MAX} \cong 354\ V \tag{3.92}$$

$$V_{DS2,MAX} = V_{in,MAX} \cong 354\ V\ . \tag{3.93}$$

Then, the maximum drain current of the transistor *S2* is equal to the maximum magnetization current as follows:

$$I_{S2(MAX)} = \frac{I_o}{n} + \frac{nV_o}{2L_m}(1 - D_{min})T_s \cong 4.2\ A\ . \tag{3.94}$$

Concerning the transistor *S1*, its maximum drain current is equal to that of the transistor *S2*, hence:

$$I_{S1(MAX)} = \frac{I_o}{n} + \frac{nV_o}{2L_m}(1 - D_{min})T_s \cong 4.2\ A \tag{3.95}$$

where D_{min} is the minimum value of the duty cycle equal to

$$D_{min} = \frac{nV_o}{V_{in_{MAX}}} = 0.27. \tag{3.96}$$

According to these electrical parameters related to the primary and secondary transistors, the GaN HEMT GS0650111L from GaN Systems has been chosen.
An advantage of this topology is to select GaN HEMT devices with lower voltage ratings with respect to 650 V and also lower on-resistance to reduce the conduction losses and to improve the performance of the converter. However, they are not yet available in the market.
The main parameters of this device extracted from the datasheet are reported in Table 3.2.
The maximum drain-to-source voltage of the transistor *SR* can be defined as follows:

$$V_{DSR,MAX} = \frac{V_{in,MAX}}{n} \cong 71\ V \tag{3.97}$$

and the maximum drain current is given by:

$$I_{SR(MAX)} = \frac{2I_o}{(1 - D_{MAX})} = \frac{2P_o}{V_o(1 - D_{MAX})} \cong 27\ A\ . \tag{3.98}$$

The Silicon MOSFET BSZ240N12NS3-G from Infineon has been chosen.
The main parameters of this device extracted from the datasheet are reported in Table 3.9.

$V_{DS,MAX}$	120 V
$R_{DS,ON(MAX)}$	24 mΩ
$I_{D,MAX}$	37 A
$C_{OSS,MAX}$	230 pF

Table 3.9: Silicon MOSFET BSZ240N12NS3-G parameters

Subsequently, the resonant inductor L_r has to be designed which also includes the leakage inductance of the transformer.
In order to ensure the ZVS operation for the primary transistors, the energy stored in the resonant inductor must be higher than the energy stored in the total output capacitance $C_{oss,TOT}$ of the transistors.
The value of the resonant inductance L_r is typically 1% or 2% of the magnetizing inductance L_m [16]. Therefore, L_r = 1% of L_m = 100 nH.
The resonant capacitance C_r is chosen based on the considerations discussed below. Firstly, it is necessary to consider that the i_{Lr} current, when the transistor *S1* conducts, has a resonant period equal to:

$$T_r = 2\pi\sqrt{L_r C_r}\ . \tag{3.99}$$

The resonant period reported in the Equation (3.99) should be lower than the *S1* on-time in order to accelerate the resonant current i_{Lr} to merge with the magnetizing current i_{Lm} achieving ZCS condition for the transistor *SR*. Therefore, the resonant capacitance C_r is computed in the following way:

$$T_r < D_{MAX} T_{SW} \tag{3.100}$$

$$2\pi\sqrt{L_r C_r} < D_{MAX} T_{SW} \tag{3.101}$$

$$L_r C_r < \left(\frac{D_{MAX} T_{SW}}{2\pi}\right)^2 \tag{3.102}$$

$$C_r < \frac{(D_{MAX})^2}{(2\pi f_{SW})^2 L_r} < 142\ nF. \tag{3.103}$$

The chosen normalized value of the resonant capacitance according to the E12 series is C_r = 39 nF.
Then, the output capacitor C_o is designed with the aim to minimize the output voltage ripple ΔV_o.
The output voltage ripple ΔV_o is given by:

$$\Delta V_o = \frac{V_0\, D\, T_{SW}}{R_o C_o} = \frac{P_0\, D\, T_{SW}}{V_o C_o} \tag{3.104}$$

and to get $\Delta V_o \leq 0.1V$, the output capacitance C_o value can be computed as follows:

$$C_o \geq \frac{P_o D_{MAX}}{V_o f_{SW}\, 0.1V} \geq 25\mu F\,. \tag{3.105}$$

The chosen normalized value of the output capacitance according to the E12 series is C_o = 33 µF.
Finally, following the same considerations made for the ACF converter, the minimum dead time can be computed as:

$$t_{d(\min)} = \frac{\pi}{2}\sqrt{L_m C_{oss,TOT}} \cong 32\, ns\,. \tag{3.106}$$

3.3.3 Primary resonant current dip effect

The primary resonant current dip effect explained in the previous section can be also considered in the AHBF converter at the *S2* turn-off as shown in Figure 3.35.

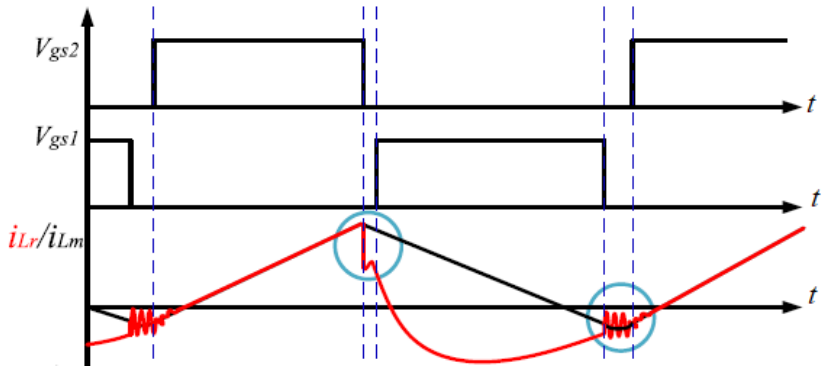


Figure 3.35: Primary resonant current dip effect in the AHBF converter [8].

The AHBF converter takes advantage from the resonant primary current dip effect because it allows to reduce the conduction losses of the *S1* transistor. This effect

happens because the current dip sets an initial condition for the resonant process during the *S1* on period. Higher current dip means lower RMS resonant current i_{Lr} and, during the *S1* on period, it is equal to the current that flow through this transistor and hence the conduction losses related to the *S1* transistor are significantly reduced.
Another positive effect of the current dip is related to the transfer of energy to the secondary side. If the current dip is very large, the RMS resonant current i_{Lr} is lower and more current is delivered from the primary side to the secondary side during the resonant process.
To take advantage of these current dip effects, the $(C_j/n^2)/C_{oss}$ ratio is set equal to 2. Since the secondary side MOSFET chosen for this topology has a typical output capacitance C_j equal to 170 pF and the primary side GaN devices have an output capacitance C_{oss} equal to 20 pF, therefore an extra capacitance with a value equal to 820 pF in parallel combination with the MOSFET must be added. In this way, the total output capacitance of the secondary side MOSFET is approximately equal to 1 nF, and the current dip effect significantly affects the primary resonant current i_{Lr}.

3.3.4 Secondary side resonance scheme

The AHBF converter efficiency and the conduction losses related to the switches can be further improved by implementing the secondary side resonance scheme. As explained in the previous section related to the ACF, this method consists in involving the output capacitance C_o in the resonant process during the conduction period of the transistors *S1* and *SR*.
In order to implement the secondary side resonance scheme, a small output capacitance C_o with low ESR is used as the resonant element and the resonant capacitance C_r must be larger with respect to the conventional primary side resonance scheme. Furthermore, the reflected output voltage V_o to the primary side is lower than the voltage across the resonant capacitance C_r.
During the *S2* on period the operation of the converter is the same as the conventional case while, during *S1* and *SR* on period, the resonant inductor L_r resonates with both the output capacitance C_o and the resonant capacitance C_r. At the beginning of the *S1* and *SR* on period, the resonant current i_{Lr} further dips down with respect to the current dip effect still reducing the RMS resonant current i_{Lr} and the conduction losses related to the *S1* and *SR* transistors. As a consequence, the whole efficiency of the AHBF converter is improved.
The equivalent resonant capacitance that participates in the resonance is equal to:

$$C_{eq} = \frac{C_r \frac{C_o}{n^2}}{C_r + \frac{C_o}{n^2}}. \tag{3.107}$$

Finally, to add the secondary side resonant scheme in the general design of the AHBF converter, the following values of the converter elements have been derived:

- C_r = 3.3 μF;
- L_r = 5.6 nH;
- C_o = 33 μF;

As done for the ACF converter, the resonant capacitance C_r has been increased with respect to the general design to involve the output capacitor C_o in the resonance according to the Equation (3.107). The resonant inductance L_r value is derived from the Equation (3.103), knowing the value of the resonant capacitance C_r.

3.3.5 Ideal circuits simulations

The next step is to use the *LTspice* software to perform the ideal circuit simulations and to analyse their results with respect to the theoretical analysis already done.
All simulations are performed with a transient analysis (*.tran*) and, as done for the ACF converter, the ideal model of the converter components are considered except for the primary and secondary side transistors. The latter are implemented by considering the output capacitance, the body diode, the on resistance, the off resistance and the threshold voltage extracted from the datasheet of the selected component. The main values that characterize the transistors are reported in Table 3.10 and the chosen values for the other components are reported in Table 3.11.

	Primary side transistors (GaN HEMT)	*Secondary side transistor (Silicon MOSFET)*
$V_{DS,MAX}$	650 V	120 V
$R_{DS,ON}$	150 mΩ	21 mΩ
C_{oss}	20 pF	170 pF

Table 3.10: AHBF primary and secondary side transistors parameters.

	Transformer	*Resonant Clamp Capacitor* C_r	Output Capacitor C_o
General design	L_m =10 μH L_r = 100 nH N = 5	C_r = 39 nF	C_o = 33μF
Design with current dip effect and secondary side resonance scheme	L_m =10 μH L_r = 5.6 nH N = 5	C_r = 3.3 uF	C_o = 33 μF

Table 3.11: AHBF component values.

Figure 3.36 shows the schematic of the general design of the AHBF converter implemented in *LTspice* for the simulations, while Figure 3.37 shows the schematic of the AHBF converter with both current dip effect and secondary side resonance scheme.

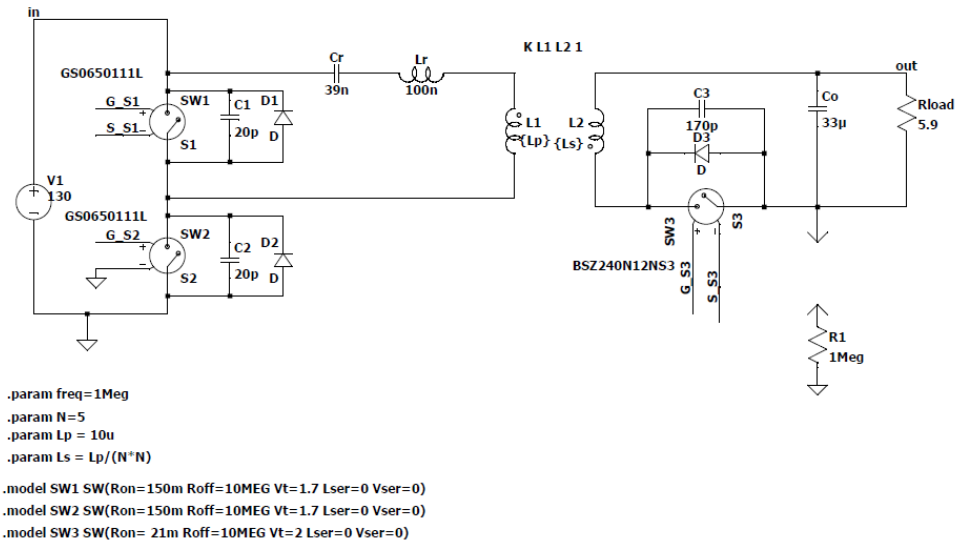


Figure 3.36: Schematic of the general design of the AHBF converter implemented in LTspice.

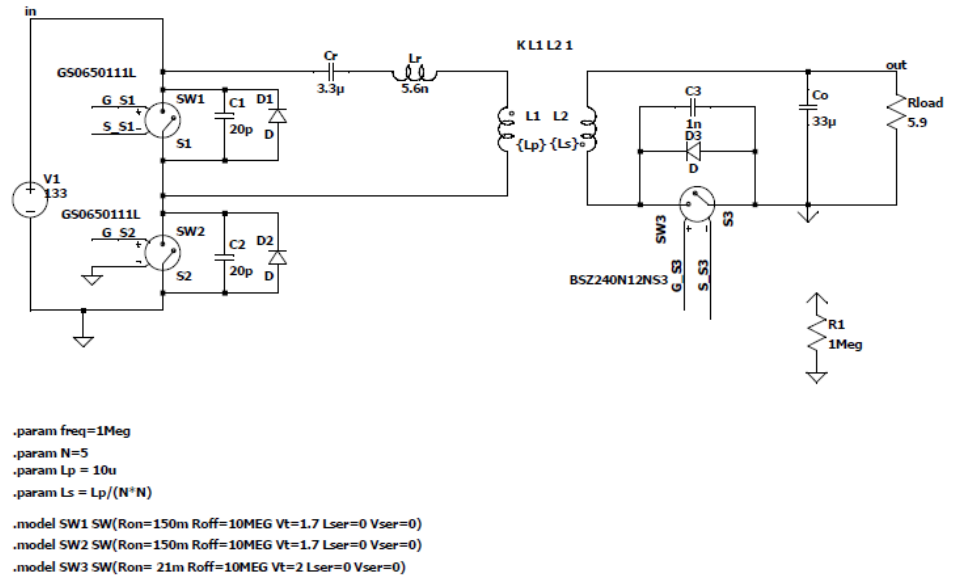


Figure 3.37: Schematic of the AHBF converter with both current dip effect and secondary side resonance scheme implemented in LTspice.

Table 3.12 shows the simulations results of the four different designs of the AHBF converter focusing on the efficiency and on the RMS resonant current measurements. It confirms how the current dip effect reduces the RMS resonant current and increases efficiency of the converter.
Furthermore, the current dip effect combined with the secondary side resonance scheme has a good result on the efficiency that increases considerably compared with the other designs. Therefore, the latter improved design of the AHFB converter will be considered and analysed in detail, also with the control method, in the next chapters.

	AHBF general design	*AHBF with the current dip effect*	*AHBF with the secondary side resonance scheme*	*AHBF with both current dip effect and secondary side resonance scheme*
Efficiency	97.2 %	97.3 %	98.7 %	98.9 %
$I_{Lr(RMS)}$	1.54 A	1.52 A	1.56 A	1.53 A

Table 3.12: Efficiency and RMS resonant current results from the AHBF ideal circuit simulations.

In the following, the current and voltage waveforms of the circuit simulations are reported. Figure 3.38 shows the simulation results of the AHBF converter general design, while Figure 3.39 shows the simulation results of the AHBF converter with both current dip effect and secondary side resonance scheme.
From the voltage waveforms shown in Figure 3.38 and in Figure 3.39, it is possible to see that the *S1* and *S2* transistors are turned on and off with ZVS thus eliminating the switching losses related to them. Moreover, the AHBF designs have been performed by turning on and off the *S1* and the *S3* transistors simultaneously.
Figure 3.38 shows that the transistor *S3* is turned off with ZCS and, at this point, the resonant capacitor has completely discharged. Also in this case, the ZCS of this transistor eliminates the switching losses.
Furthermore, from Figure 3.39 it is possible to see a dip in the resonant current i_{Lr} after the *S2* turn off, the current dip reduces the RMS resonant current $i_{Lr,rms}$ and more current is transferred from the primary side to the secondary side increasing the converter efficiency. Compared to the AHFB general design, the AHFB design with both current dip and secondary side resonance scheme loses the ZCS turn off for the transistor *S3* at low input voltage as it can be seen in Figure 3.39. However, the drain-

to-source voltage of this transistor is equal to zero both at the turn on and turn off and therefore the switching losses are equal to zero.
Moreover, at higher input voltage such as $V_{in,rms}$ equal to 230 V, the transistor *S3* turns off with ZCS as shown in Figure 3.40. This is due to the increase in the input voltage and therefore to the to the increase in the on time of the transistor *S3* which allows the current flowing through it to reach zero when it is switched off.

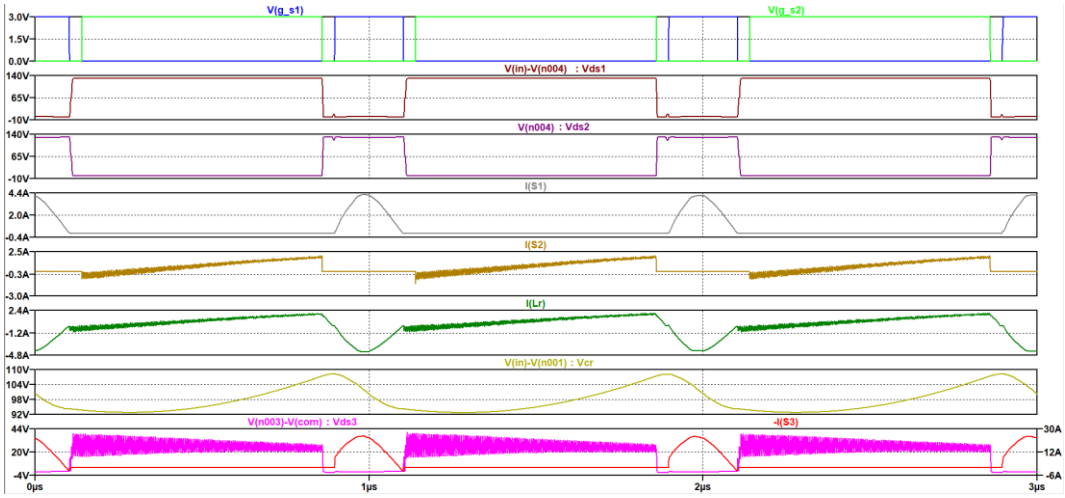


Figure 3.38: Ideal circuit simulation results of the general design of the AHBF converter.

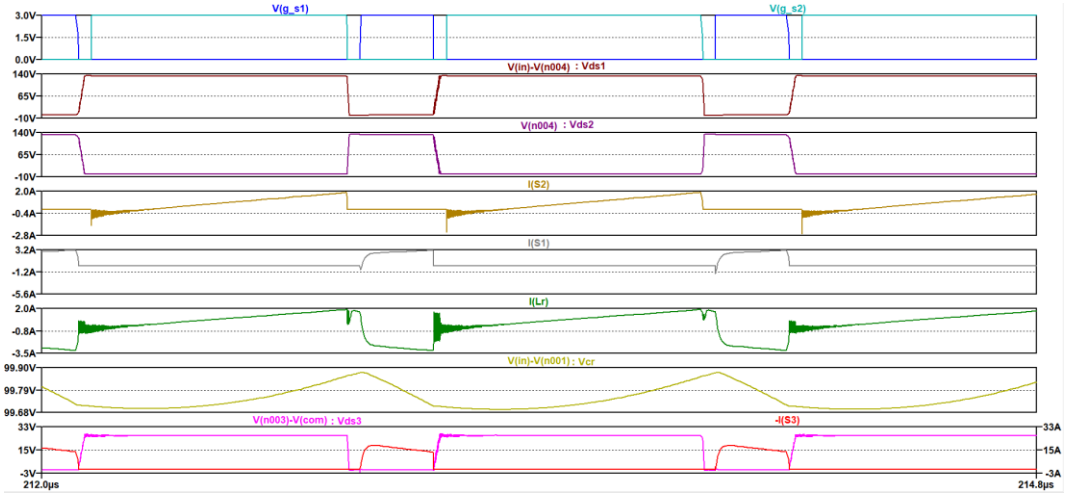


Figure 3.39: Ideal circuit simulation results of the AHBF converter with both current dip effect and secondary side resonance scheme when $V_{in,rms}$ = 90 V.

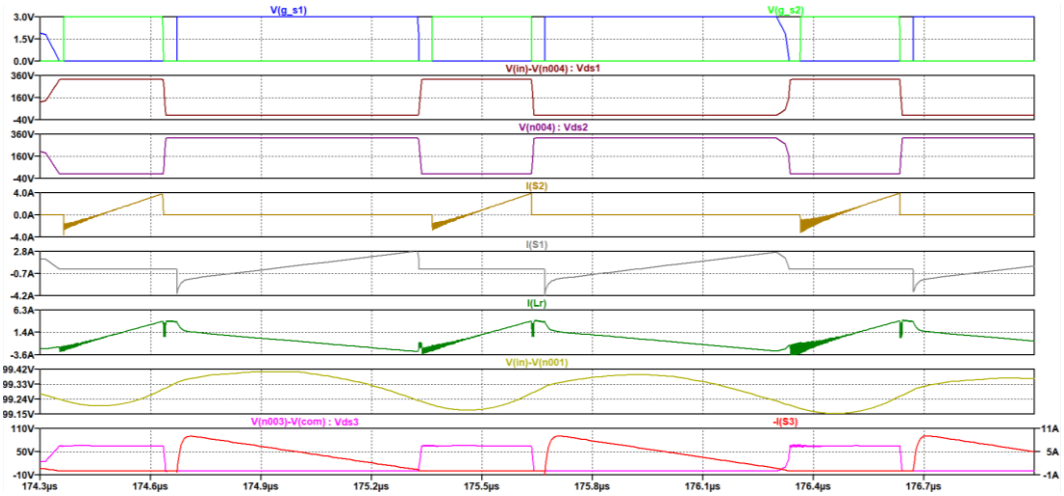


Figure 3.40: Ideal circuit simulation results of the AHBF converter with both current dip effect and secondary side resonance scheme when $V_{in,rms}$ = 230 V.

The simulation results about the AHBF converter design with both current dip effect and secondary side resonance scheme obtained by using the *LTspice* software were also confirmed by the simulations performed with the PSIM software. The current and voltage waveforms of the latter simulation are shown in Figure 3.41.

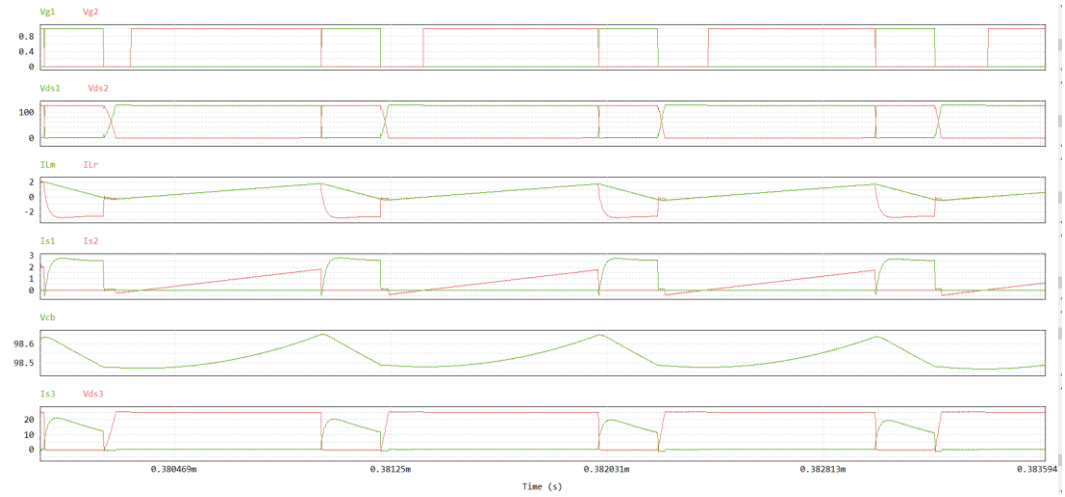


Figure 3.41: AHFB with current dip and secondary side resonance scheme ideal PSIM simulation.

3.3.6 Simulations with real component models

After the ideal circuit simulations, the AHBF converter schematic is completed with the real *LTspice* models of all the components that constitute the circuit, but only the coupled inductors are still considered ideal since during its design it is difficult to estimate their parasitic elements.
Before proceeding with the real simulations, the real components must be selected from catalogues. Then, the *LTspice* model can be extracted and imported in the software to design the circuit and to execute the simulations.
The primary and secondary side transistors have already been selected in the Section 3.3.2.
Then, the resonant clamp capacitor and the output capacitance must be selected.
Focusing on the resonant clamp capacitor, the voltage across the capacitor is equal to output voltage reflected to the primary side, hence V_{Cr} = 97.5 V.
Focusing, now, on the output capacitor, the maximum voltage across it and the ESR must be derived. The maximum voltage across the output capacitance is equal to the output voltage and the ESR is computed as the ratio between the output voltage ripple and the maximum current that flow through the secondary side transistor (ESR = ΔV_o / $I_{S3(MAX)}$). Therefore, the computed ESR is equal to 3.7 mΩ, as in the ACF converter.

According to these considerations, the resonant clamp capacitor C_r can be chosen:

- The KEMET X7R C1825C393K2RAC with a capacitance value equal to 39 nF was chosen for the AHBF general design and for the design with the current dip effect.
- The KEMET X7R C1825C105K2RAC with a capacitance value equal to 1 μF was chosen for the design with the secondary side resonance scheme and for the design with both the current dip effect and the secondary side resonance scheme.

Now, focusing on the output capacitor C_o, the following models can be chosen:

- The Wurth Elektronik X5R 885012106031 WCAP-CSGP with a capacitance value equal to 10 μF was chosen for all the AHBF designs. The ESR of this component is equal to 10 mΩ and its maximum working voltage is equal to 25 V. Three capacitors in a parallel combination are used to have a total capacitance close to 30 μF and a ESR value close to 3.7 mΩ.

To implement the current dip, since the secondary side transistor which was chosen has an output capacitance equal to 180 pF, an extra capacitor with a value equal to 820 pF must be added in parallel combination with the transistor.

Table 3.13 shows the real simulations results of the four different designs of the ACF converter focusing on the efficiency and on the RMS resonant current measurements. The real circuit simulations of the AHBF converter improved design in terms of efficiency with both the current dip effect and the secondary side resonance scheme will be considered in detail in the next chapter, underlining the improvements and all the design choices of this topology.

	AHBF general design	*AHBF with the current dip effect*	*AHBF with the secondary side resonance scheme*	*AHBF with both current dip effect and secondary side resonance scheme*
Efficiency	96.5 %	96.6 %	96.8 %	97.56 %
$I_{Lr(RMS)}$	1.52 A	1.51 A	1.49 A	1.48 A

Table 3.13: Efficiency and RMS resonant current results from the AHBF real circuit simulations.

In the following, Figure 3.42 shows the real simulation results of the AHBF converter general design.
The waveforms reported in this figure confirm the results obtained with the ideal circuit simulation regarding the ZVS turn on and turn off for both the *S1* and the *S2* transistors. Moreover, the I_{d3} waveform shows that the transistor *S3* turns off with ZCS also reducing the switching losses related to it.
Finally, the theoretical analysis is confirmed by the simulations with real model components.

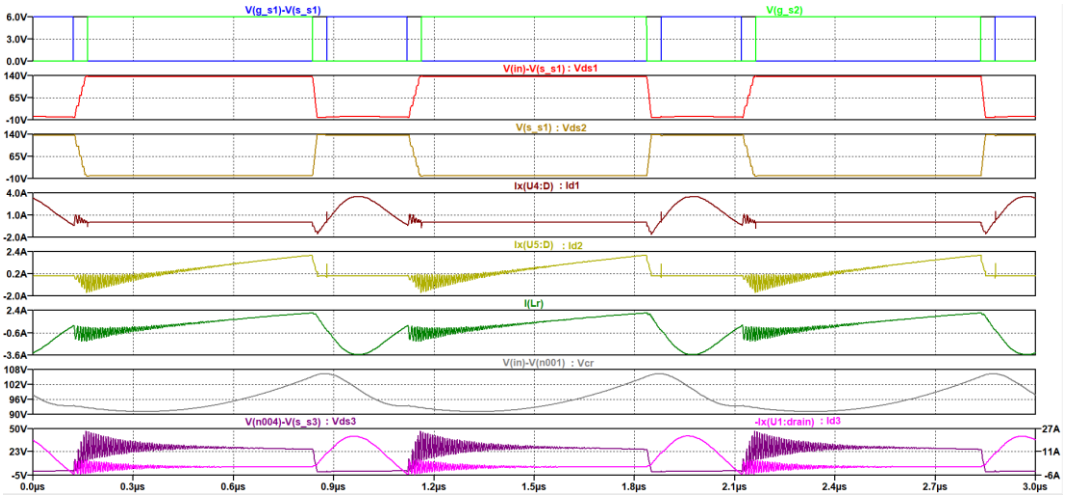


Figure 3.42: Real circuit simulation results of the general design of the AHBF converter.

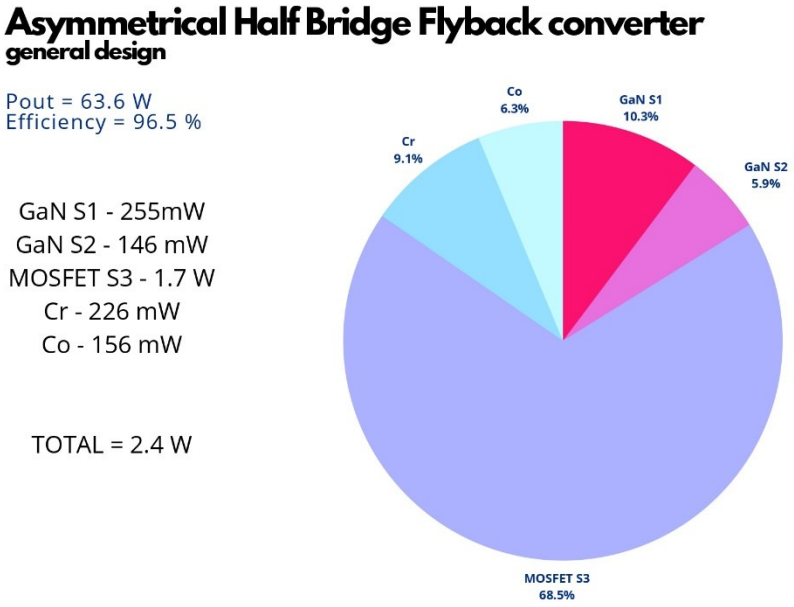


Figure 3.43: AHBF general design power dissipation.

Now, considerations about the power dissipation by each component of the circuit can be done. The power dissipated by each element is computed directly from the *LTspice* software and the results are shown in Figure 3.43. The pie chart reported in this figure show that the component that dissipate the most power is still the secondary side transistor because of the high RMS current and its on resistance. To reduce the power

dissipation related to this transistor and hence to increase the efficiency of the converter, a device with a lower on resistance must be selected.

3.4 LLC resonant power converter

The last power converter topology analysed in this work to implement high-power density and high-frequency adapters is the LLC resonant power converter shown in Figure 3.44.

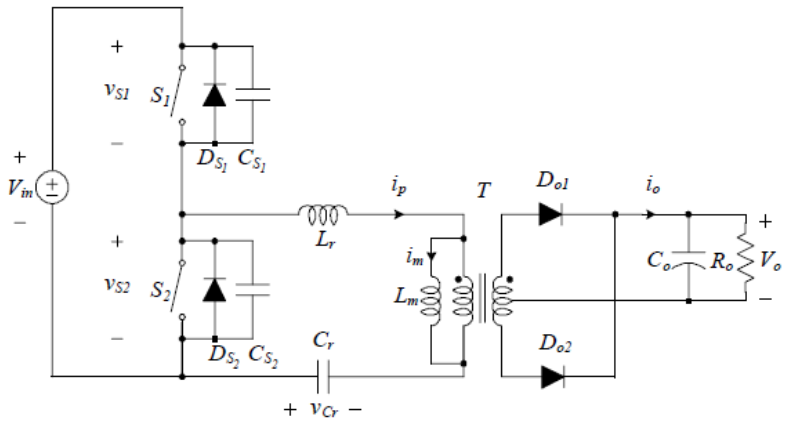


Figure 3.44: LLC resonant power converter schematic [3].

The primary side of the circuit is composed by the main switch *S1* and the auxiliary switch *S2*. Both *S1* and *S2* are GaN HEMT switches, and their body diodes (D_{s1} and D_{s2}) and output capacitances (C_{s1} and C_{s2}) are considered. V_{in} is the DC input voltage. Then, C_r is the resonant capacitor, L_r is the resonant inductance that also includes the leakage inductance of the transformer and L_m is the magnetizing inductance.
The secondary side of the converter is a center tapped rectifier composed by a center tapped transformer and two diodes D_{01} and D_{02}. Finally, C_o is the output capacitor and R_o represents the equivalent load resistance.

3.4.1 Circuit analysis

The working principle and the design equations of this converter topology are reported in detail in this section. The DC characteristic and the input-output response in the frequency domain are derived from the equivalent circuit obtained by the first harmonic approximation (FHA) method [3].
In the LLC resonant power converter, two resonant frequencies f_{r1} and f_{r2} are defined in the following way:

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.108}$$

and

$$f_{r2} = \frac{1}{2\pi\sqrt{(L_m + L_r)C_r}}. \tag{3.109}$$

Then, the quality factor Q_S is defined as follows:

$$Q_S = \frac{\sqrt{L_r/C_r}}{n^2 R_o} = \frac{Z_{r1}}{n^2 R_o} \tag{3.110}$$

where $n = N_p/N_s$ is the turns ratio, Z_{r1} is the resonant impedance of f_{r1} and R_o is the load resistance.

The DC gain characteristic of the LLC converter is shown in Figure 3.45. From the DC gain characteristic, it is possible to notice that the peak gain changes according to the load variations through the direct dependence on the quality factor. Under light load conditions, the peak gain is close to the resonant frequency f_{r2}. Under heavy load conditions, instead, the peak gain is close to the resonant frequency f_{r1}. However, Figure 3.45 shows that the gain at f_{r1} is independent on the load variations.

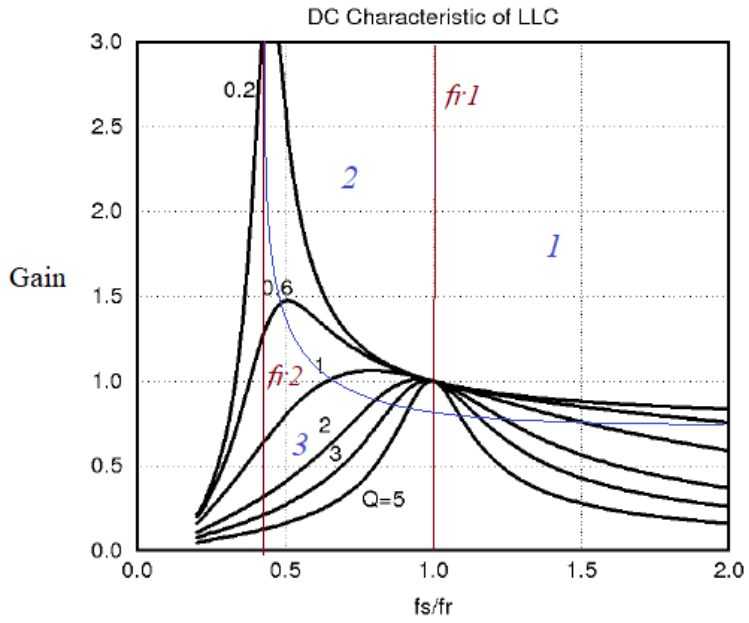


Figure 3.45: DC gain characteristic of the LLC resonant power converter.

Furthermore, the DC gain characteristic of the LLC converter can be divided into three regions:

- The *region 1* is the SRC operation region, where the switching frequency f_s is higher than the resonant frequency f_{r1}. In this operation region, the magnetizing inductance L_m does not participate in the resonance and the ZVS operation is achieved [3].
- The *region 2* is the multi-resonant operation region, where the switching frequency f_s is between the two resonant frequencies f_{r1} and f_{r2}. In this operation region, the load determines the operation of the converter under ZVS and ZCS conditions [3].
- The *region 3* is the overloaded operation region. In this area, the operation of the converter under ZCS condition is achieved [3].

The converter has to be designed to operate in region 1 and in region 2 in order to ensure ZVS operation. Moreover, to be sure that the ZVS condition will be achieved, the switching frequency f_s must be higher than the resonant frequency f_{r2}.
At this point, the analysis of the AC equivalent model of the LLC resonant power converter [3], shown in Figure 3.46, can be done.

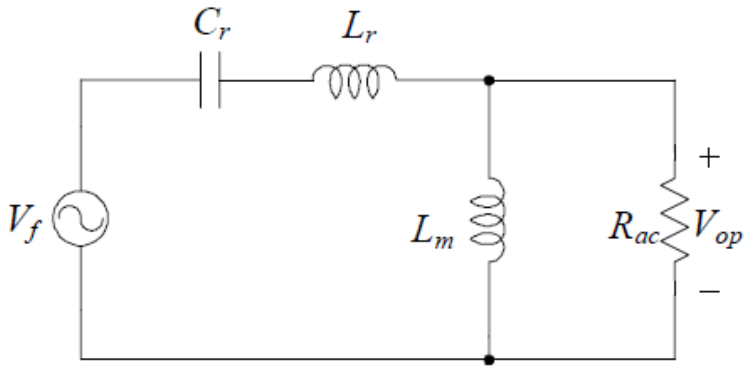


Figure 3.46: AC equivalent model of the LLC resonant power converter [3].

The power requirement defines the operating point of the LLC converter. Under low power conditions, the switching frequency f_s is higher than f_{r2}. On the contrary, under high power conditions, the switching frequency is close to f_{r1} and a control loop is needed to reduce the f_s approaching it to f_{r2} in order to deliver the necessary amount of current to the load. Moreover, near f_{r2}, the LLC converter can be considered to operate as a bandpass filter with a square wave excitation coming from the half bridge. Using the FHA method, the square wave excitation is replaced with its fundamental value V_f given by [3]:

$$V_f = \frac{2V_{in}}{\pi} \tag{3.111}$$

where V_{in} is the AC input voltage.
Then, the secondary side components are transferred to the primary side. In fact, in Figure 3.46, R_{ac} is the equivalent load resistance that represents the secondary side of the converter and it is given by:

$$R_{ac} = \frac{8n^2 R_o}{\eta\pi^2} \tag{3.112}$$

where n is the turns ratio, is the output load of the secondary side and η is the efficiency due to the magnetic core of the transformer.
The average output current I_o is equal to:

$$I_o = \frac{\eta\pi V_{op}}{4R_o} \tag{3.113}$$

where V_{op} is the is the voltage across R_o.
Then, the DC output voltage V_o can be computed by combining the Equation (3.113) and the turns ratio n of the transformer as follows:

$$V_o = \frac{\eta\pi V_{op}}{4n}. \tag{3.114}$$

The conversion ratio of the converter can be derived by combining the Equation (3.114) and the Equation (3.111):

$$\frac{V_{op}}{V_f} = \frac{4nV_o}{\pi\eta} \cdot \frac{\pi}{2V_{in}} = \frac{2nV_o}{\eta V_{in}} \tag{3.115}$$

and, by using the Laplace transformation, the conversion ratio in the s-domain is given by:

$$\frac{V_{op}}{V_f}(s) = \left| \frac{sL_m \,//\, R_{ac}}{sL_r + \frac{1}{sC_r} + sL_m \,//\, R_{ac}} \right|. \tag{3.116}$$

In the frequency domain, by using the equivalence $s = j\omega$ and under no-load condition $R_{ac} = \infty$, Equation (3.116) becomes:

$$\frac{V_{op}}{V_f}(\omega) = \left| \frac{\frac{j\omega L_m R_{ac}}{j\omega L_m + R_{ac}}}{j\omega L_r + \frac{1}{j\omega C_r} + \frac{j\omega L_m R_{ac}}{j\omega L_m + R_{ac}}} \right| \cong \frac{L_m}{L_m + L_r - \frac{1}{\omega^2 C_r}}. \tag{3.117}$$

Finally, the expression of the conversion ratio is the following:

$$\frac{V_o}{V_{in}} = \frac{\eta}{2n} \cdot \frac{L_m}{L_m + L_r - \frac{1}{\omega^2 C_r}} \cong \frac{\eta}{2n} \cdot \frac{L_m}{L_m + L_r}. \tag{3.118}$$

Focusing on the working principles, it is assumed that the LLC converter is operating at switching frequency f_s close to the resonant frequency f_{r1}. Therefore, the operation of a switching cycle is divided into six intervals from t_0 to t_6. The current and the voltage steady-state waveforms of the LLC converter are shown in Figure 3.47.

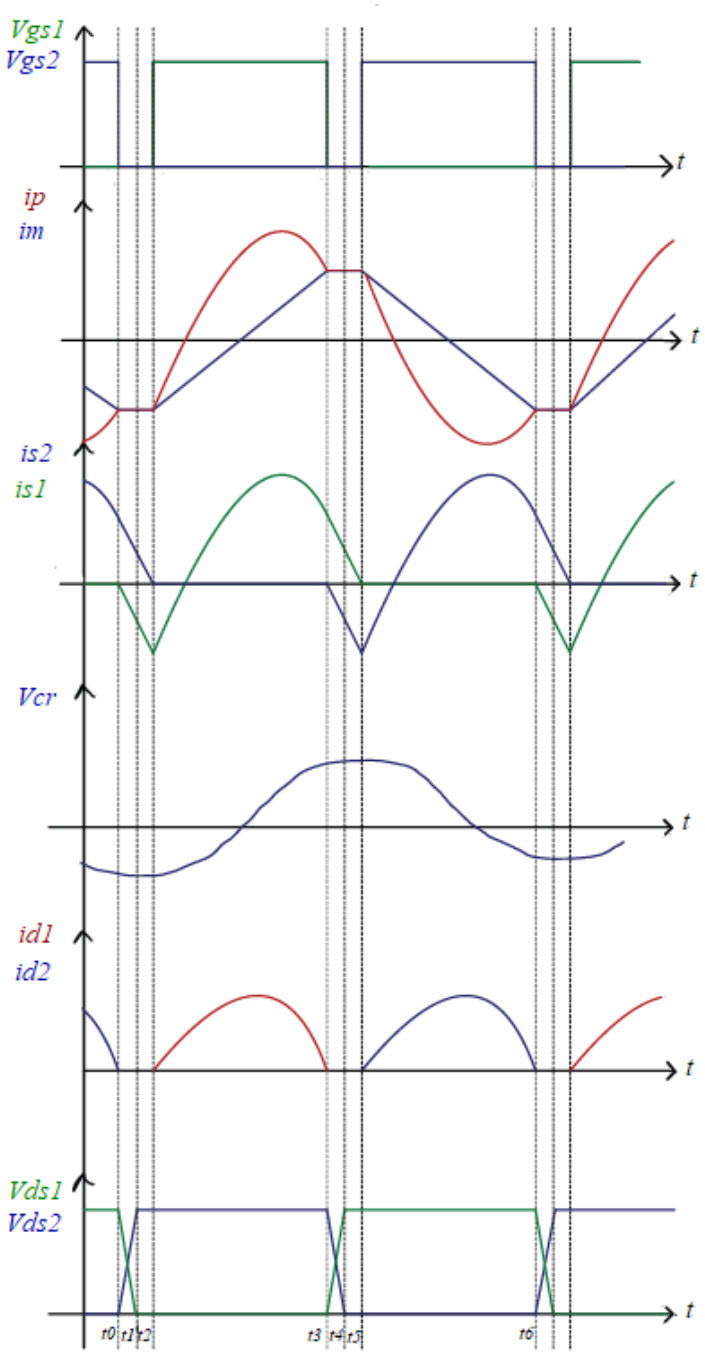


Figure 3.47: Current and voltage steady-state waveforms of the LLC resonant power converter.

Interval 1 [$t_0 - t_1$]: Att_o, the *S2* transistor is turned off with ZVS and the *S1* transistor was already off.

The primary resonant current i_p discharges the output capacitance C_{s1} of the transistor *S1* and charges the output capacitance C_{s2} of the transistor *S2*. Therefore, the drain-to-

source voltage V_{DS1} decreases from its maximum value V_{in} to $0\ V$, while the drain-to-source voltage V_{DS2} increases from $0\ V$ to V_{in}.
Since the output capacitance of a GaN HEMT device is very small, they charge and discharge very quickly, hence this time interval is quite short and the current i_{Lm} can be considered almost constant.
During this time interval, the primary resonant current i_p follows the magnetizing current i_{Lm} and no power is delivered from the primary side to the secondary side of the converter.
Figure 3.48 shows the current path in the LLC resonant power converter during interval 1.

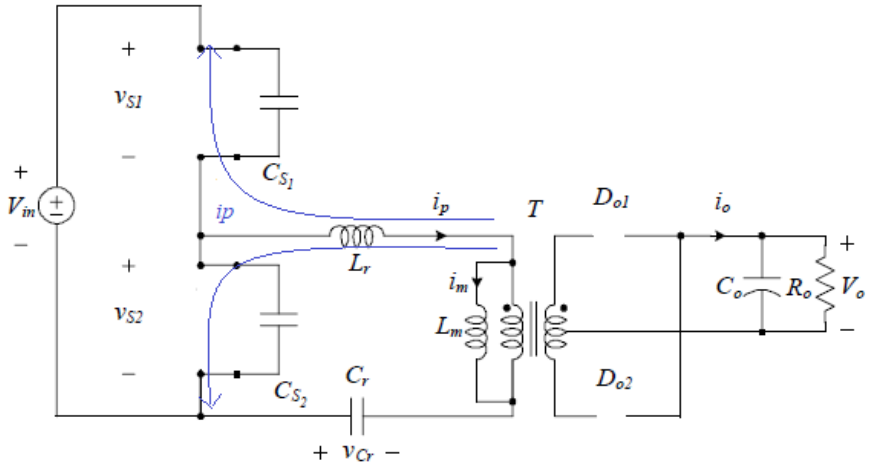


Figure 3.48: LLC during interval 1.

Interval 2 [$t_1 - t_2$]: during this time interval, the transistors are still off.
The magnetizing current i_{Lm} is still considered almost constant and the primary resonant current i_p flows through the body diode D_{s1} of the transistor $S1$.
Moreover, the primary resonant current i_p continues to follow the magnetizing current i_{Lm} and no energy is delivered from the primary side to the secondary side of the converter.
At t1, the output capacitance C_{s1} of the transistor $S1$ is fully discharged and the output capacitance C_{s2} of the transistor $S2$ is fully charged. Therefore, the voltage V_{DS1} has reached $0\ V$ which creates the ZVS condition for the $S1$ turn-on.
Figure 3.49 shows the current path in the LLC resonant power converter during interval 2.

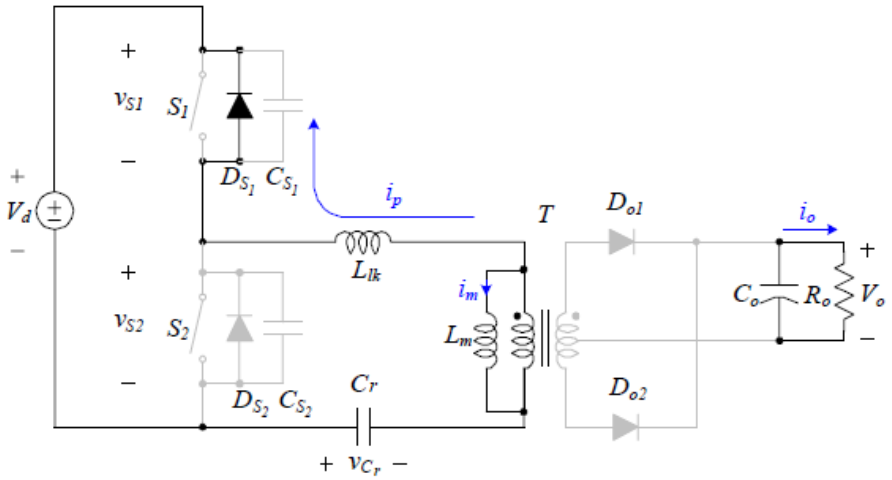


Figure 3.49: LLC during interval 2 [3].

Interval 3 [$t_2 - t_3$]: at t2, the *S1* transistor turns on with ZVS and hence the current i_p continues to flow through *S1*.
During this interval, the input voltage V_{in} starts to charge the magnetizing inductance L_m and the magnetizing current i_{Lm} increases linearly. The primary resonant current i_p increases following a cosine function and it force the secondary side diode D_{o1} to conduct since the difference between the current i_p and the current i_{Lm} is different from zero. Therefore, there is a transfer of energy from the primary side to the secondary side of the converter.
The expression of the magnetizing current i_{Lm}, under the $L_m >> L_r$ assumption, is given by:

$$i_{Lm}(t) = i_{Lm}(t_2) + \frac{n(V_o + V_{Df})}{L_m}(t - t_2) \tag{3.119}$$

and the expression of the primary resonant current i_p is the following one:

$$i_p(t) = i_p(t_2)\cos(\omega_{r1}(t - t_2)) + \frac{V_b}{Z_{r1}}\sin(\omega_{r1}(t - t_2)) \tag{3.120}$$

where ω_{r1} is resonant frequency and V_b is equal to:

$$V_b = V_{in} - V_{Cr}(t_2) - n(V_o + V_{Df}) \tag{3.121}$$

where V_{Df} is the forward voltage drop of the output diodes and V_{Cr} is the voltage across the resonant capacitor.

Furthermore, the voltage across the magnetizing inductance L_m is constant and equal to nV_o, hence L_m does not participate in the resonant process during this period.
Then, the resonant capacitor C_r is charged by the primary current and the voltage across it increases reaching its maximum value almost equal to nV_o at t_3.
Finally, this period end when the primary resonant current is equal to the magnetizing current at t_3 and the output current i_o, that is equal to the diode D_{o1} current i_{D1}, reaches zero.
Figure 3.50 shows the current path in the LLC resonant power converter during interval 3.

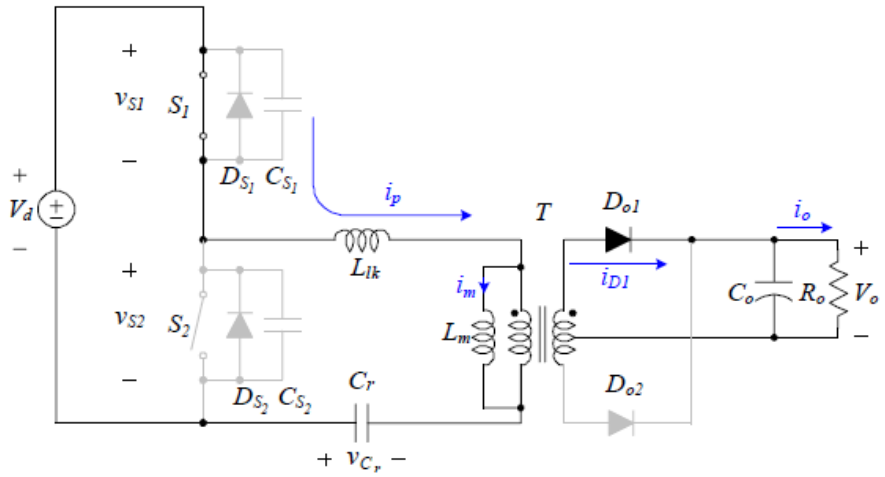


Figure 3.50: LLC during interval 3 [3].

Interval 4 [$t_3 - t_4$]: during this time interval, all the transistors are off.
At t_3, *S1* is turned off with ZVS and the magnetizing current remains almost constant at its maximum value.
The primary resonant current i_p discharges the output capacitance C_{s2} of the transistor *S2* and charges the output capacitance C_{s1} of the transistor *S1*. Therefore, the drain-to-source voltage V_{DS2} decreases from its maximum value V_{in} to *0 V*, while the drain-to-source voltage V_{DS1} increases from *0 V* to V_{in}.
During this time interval, the primary resonant current i_p follows the magnetizing current i_{Lm} and no power is delivered from the primary side to the secondary side of the converter.
Figure 3.51 shows the current path in the LLC resonant power converter during interval 4.

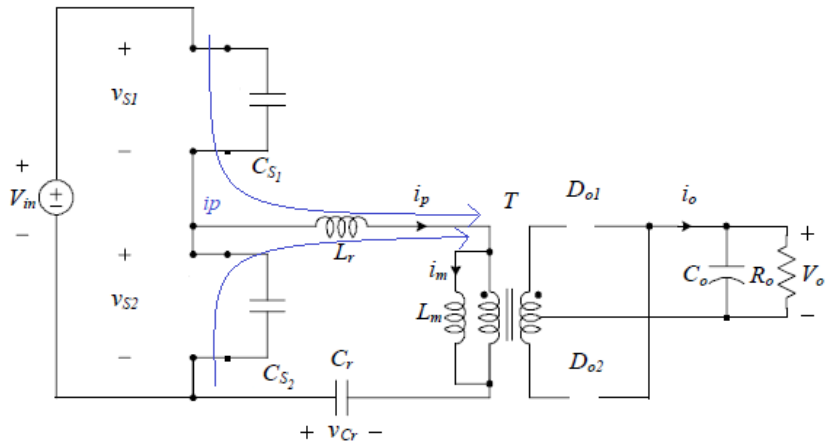


Figure 3.51: LLC during interval 4.

Interval 5 [$t_4 – t_5$]: during this time interval, the transistors are still off.
The magnetizing current i_{Lm} is still considered almost constant and the primary resonant current i_p flows through the body diode D_{s2} of the transistor *S2*.
Moreover, the primary resonant current i_p continues to follow the magnetizing current i_{Lm} and no energy is delivered from the primary side to the secondary side of the converter.
At t4, the output capacitance C_{s2} of the transistor *S2* is fully discharged and the output capacitance C_{s1} of the transistor *S1* is fully charged. Therefore, the voltage V_{DS2} has reached *0 V* which creates the ZVS condition for the *S2* turn-on.
Figure 3.52 shows the current path in the LLC resonant power converter during interval 5.

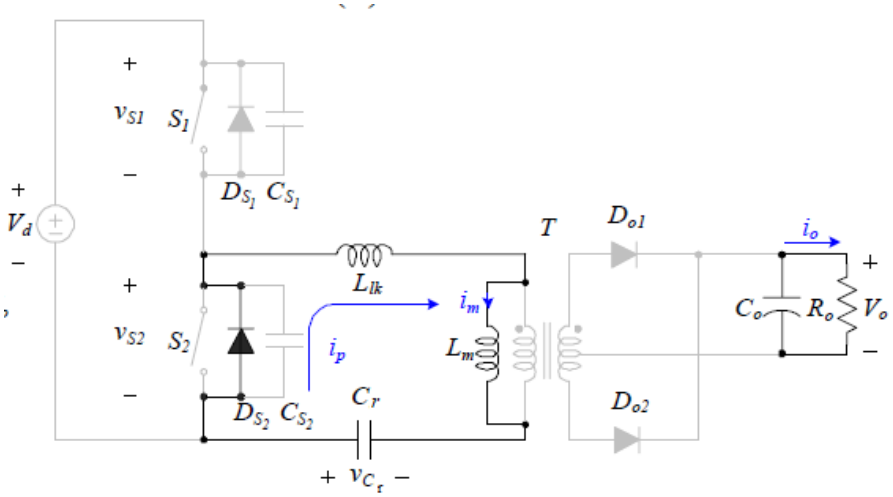


Figure 3.52: LLC during interval 5 [3].

Interval 6 [$t_5 - t_6$]: at t5, the *S2* transistor turns on with ZVS and hence the current i_p continues to flow through *S2*.
During this interval, the energy is transferred from the primary side to the secondary side of the converter and hence the magnetizing current i_{Lm} decrease linearly. The primary resonant current i_p decreases following a cosine function and it force the secondary side diode D_{o2} to conduct since the difference between the current i_p and the current i_{Lm} is different from zero.
The expression of the magnetizing current i_{Lm}, under the $L_m >> L_r$ assumption, is given by:

$$i_{Lm}(t) = i_{Lm}(t_5) - \frac{n\left(V_o + V_{Df}\right)}{L_m}(t - t_5) \tag{3.122}$$

and the expression of the primary resonant current i_p is the following one:

$$i_p(t) = i_p(t_5)\cos\left(\omega_{r1}(t - t_5)\right) - \frac{V_r}{Z_{r1}}\sin\left(\omega_{r1}(t - t_5)\right) \tag{3.123}$$

where ω_{r1} is resonant frequency and V_r is equal to:

$$V_b = V_{Cr}(t_5) - n(V_o + V_{Df}) \tag{3.124}$$

where V_{Df} is the forward voltage drop of the output diodes and V_{Cr} is the voltage across the resonant capacitor.
Moreover, the voltage across the magnetizing inductance L_m is constant and equal to nV_o, hence L_m does not participate in the resonant process during this period.
During this period, the resonant capacitor C_r is discharged by the primary current and the voltage across it decreases reaching its minimum value.
Finally, this period end when the primary resonant current is equal to the magnetizing current at t_6 and the output current i_o, that is equal to the diode D_{o2} current i_{D2}, reaches zero.
Figure 3.53 shows the current path in the LLC resonant power converter during interval 6.

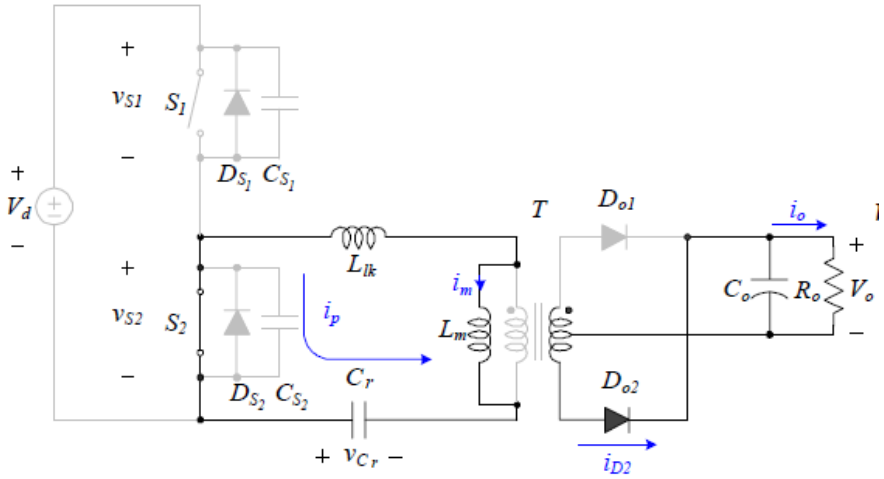


Figure 3.53: LLC during interval 6 [3].

3.4.2 General design

Once the LLC resonant power converter analysis has been described in detail, a general design [17] of this topology can be realized considering the specifications reported in Table 3.14.

P_o	65 W
V_o	19.5 V
ΔV_o	0.1 V
V_{in} (AC)	90 – 250 V
f_{sw}	1 MHz
D_{MAX}	0.5

Table 3.14: LLC design specifications.

The components that need to be selected are:

- transformer;
- primary and secondary transistors;
- resonant inductor;
- resonant capacitor;
- output capacitor.

It is necessary to define the main electrical parameters associated with each component of the converter.
The design of the resonant components must be performed by ensuring a good compromise among load variations, maximum acceptable switching frequency

excursion, maximum input voltage range and short circuit characteristic. In fact, the optimal operating point is achieved only for a given load resistance, a given switching frequency and a given input voltage. Therefore, when the input voltage decreases and the load increases, a feedback loop is needed to reduce the switching frequency and to maintain the output voltage always regulated [3] according to the following equation:

$$Q_s = \frac{\omega_{r1} L_r}{\frac{\eta^2}{4} \frac{V_{in}^2}{V_o^2} R_o} \tag{3.125}$$

Moreover, the switching losses are low if the LLC resonant power converter operates at the switching frequency f_{sw} equal to the resonant frequency f_{r1}.
The first step is to define the value of the transformer turns ratio n according to the following equation:

$$n = \frac{\frac{V_{in,min}}{2}}{V_o} = 3.25 \rightarrow 5 \tag{3.126}$$

where V_o the DC output voltage and $V_{in,min}$ is the minimum DC input voltage.
Then, the maximum gain M_{g_max} and the minimum gain M_{g_min} are obtained as follows:

$$M_{g\_max} = \frac{n(V_0 + V_D)}{\frac{V_{in,min}}{2}} \cong 2.24 \tag{3.127}$$

and

$$M_{g\_min} = \frac{n(V_0 + V_D)}{\frac{V_{in,max}}{2}} \cong 0.81 \tag{3.128}$$

where V_D is the secondary side diode voltage drop and it is assumed to be equal to 0.7 V.
Furthermore, to maintain the operation of the converter within the inductive region with an overload current capability of 110%, the maximum gain M_{g_max} must be increased [17]:

$$M_{g\_max} = \frac{n(V_0 + V_D)}{\frac{V_{in,min}}{2}} x\ 110\% \cong 2.46\,. \tag{3.129}$$

The next step is to select the inductance ratio L_n and the quality factor Q_s from the graph in Figure 3.54.

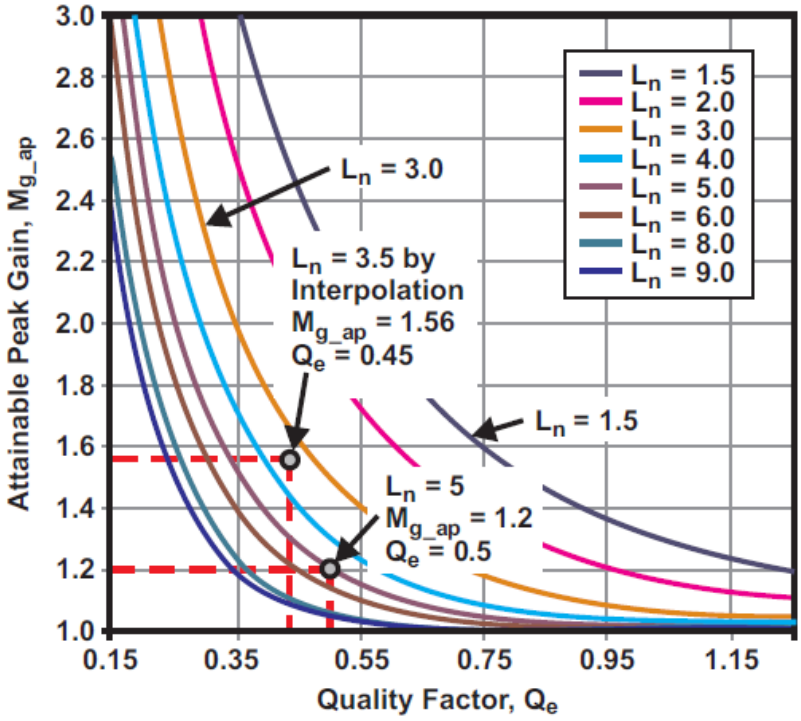


Figure 3.54: Attainable peak gain with respect to quality factor graph.

The inductance ratio L_n is chosen equal to:

$$L_n = \frac{L_m}{L_r} = 3.5 \tag{3.130}$$

and, in order to obtain the attainable peak gain M_{g_ap} higher than the maximum peak gain M_{g_max}, the quality factor Q_s is selected from the graph:

$$Q_s \cong 0.25\,. \tag{3.131}$$

In this way, the attainable peak gain M_{g_ap} is equal to 2.6 that is higher than the maximum peak gain M_{g_max} equal to 2.46.
As a next step, the equivalent load resistance R_{ac} is derived by the expression below:

$$R_{ac} = \frac{8n^2V_o}{\pi^2 I_o} = 119\ \Omega. \tag{3.132}$$

At 110% overload, the equivalent load resistance R_{ac} is equal to:

$$R_{ac} = \frac{8n^2V_o}{\pi^2 I_o} \cdot \frac{1}{110\%} = 108\ \Omega. \tag{3.133}$$

Then, the resonant circuit components C_r and L_r values are defined as follows, at the switching frequency equal to 1 MHz:

$$C_r = \frac{1}{2\pi Q_s f_{SW} R_{ac}} \cong 5.35\ nF \tag{3.134}$$

and

$$L_r = \frac{1}{(2\pi f_{SW})^2 C_r} \cong 4.52\ \mu H. \tag{3.135}$$

The value of the resonant inductance L_r was approximated to $L_r = 4.7$ µH.
The chosen normalized value of the resonant capacitance C_r according to the E12 series is $C_r = 5.6$ nF.
At this point, it is possible to derive the magnetizing inductance value by combining the Equation (3.130) and the Equation (3.135):

$$L_m = L_n \cdot L_r = 16.5\ \mu H. \tag{3.136}$$

At this point, it is necessary to verify the resonant circuit design. In particular, it is important to check the switching frequency, the inductance ratio and the quality factor both at full load and at 110% overload by substituting in the following equations the values just computed:

$$f_{sw} = \frac{1}{2\pi\sqrt{L_r C_r}} \cong 981\ kHz \tag{3.137}$$

$$L_n = \frac{L_m}{L_r} \cong 3.51 \tag{3.138}$$

$$Q_s = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \cong 0.24 \tag{3.139}$$

$$Q_s = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \cdot 110\% \cong 0.27. \tag{3.140}$$

From Equation (3.137) to Equation (3.140), it is possible to notice that the design of the resonant components meets the initial requirements of the inductance ratio and quality factor.
Once the resonant circuit components values have been computed, the stress of the primary and secondary side of the converter can be defined.
The RMS primary side current is given by:

$$I_{p(RMS)} = \frac{\pi I_o}{2\sqrt{2}\, n} \cong 740\ mA\ . \tag{3.141}$$

The RMS magnetizing current is given by:

$$I_{Lm(RMS)} = \frac{2\sqrt{2}\, nV_o}{\pi \omega_{r1} L_m} \cong 847\ mA\ . \tag{3.142}$$

Then, the transformer RMS primary winding current is given by:

$$I_r = \sqrt{I_{Lm(RMS)}^2 + I_{p(RMS)}^2} \cong 1.12A\ . \tag{3.143}$$

The RMS secondary side current is given by:

$$I_{s(RMS)} = nI_{p(RMS)} \cong 3.7\ A\ . \tag{3.144}$$

Moreover, since the transformer secondary side has a center tapped configuration, the secondary side current can be equally divided into two transformer windings in the secondary side. Therefore, the current of each winding is equal to:

$$I_w = \frac{\sqrt{2}}{2} I_{s(RMS)} \cong 2.6\ A\ . \tag{3.145}$$

The resonant capacitance C_r voltage stresses are defined in the following equations.
The AC resonant capacitance voltage is given by:

$$V_{Cr} = \frac{I_r}{\omega_{r1} C_r} \cong 32\ V. \tag{3.146}$$

The RMS resonant capacitance voltage is given by:

$$V_{Cr_{RMS}} = \sqrt{\left(\frac{V_{in,\max}}{2}\right)^2 + V_{Cr}^2} \cong 180\ V\ . \tag{3.147}$$

Then, the resonant capacitance peak voltage is given by:

$$V_{Cr,peak} = \frac{V_{in,MAX}}{2} + \sqrt{2}\,V_{Cr} \cong 222\ V. \tag{3.148}$$

The next step is to define the stress of the primary side transistors to select them from catalogues.
The maximum drain-to-source voltages for *S1* and *S2* are defined as follows:

$$V_{DS1,MAX} = V_{DS2,MAX} = V_{in,MAX} \cong 354\ V \tag{3.149}$$

Then, the RMS drain current of the *S1* and *S2* transistors are equal to I_r as follows:

$$I_{S1(RMS)} = I_{S2(RMS)} = I_r = 1.12\ A\ . \tag{3.150}$$

According to these electrical parameters related to the primary transistors, the GaN HEMT IGLD60R190D1 from Infineon has been chosen.
As already said for the AHBF topology, GaN HEMT devices with lower voltage ratings with respect to 600 V can be selected to take advantage of this characteristic ad hence to improve the performance of the converter when they are commercially available.
The main parameters of this device extracted from the datasheet are reported in Table 3.15.

$V_{DS,MAX}$	600 V
$R_{DS,ON(MAX)}$	190 mΩ
$I_{D,MAX}$	10 A
C_{OSS}	28 pF

Table 3.15: GaN HEMT IGLD60R190D1 parameters.

The stresses of the center tapped rectifier diodes are derived.
The diode voltage rating is defined as follows:

$$V_D = \frac{\frac{V_{in,MAX}}{2}}{n} x2 \cong 71\ V \tag{3.151}$$

and $V_D = 85$ V is chosen.

Then, the diode current rating is computed as follows:

$$I_D = \frac{\sqrt{2} I_{s(RMS)}}{\pi} \cong 1.7\ A\ . \tag{3.152}$$

The last component that must be designed is the output capacitor C_o and it is designed with the aim to minimize the output voltage ripple ΔV_o.
The output voltage ripple ΔV_o is given by:

$$\Delta V_o = \frac{V_0\ D\ T_{SW}}{R_o C_o} = \frac{P_0\ D\ T_{SW}}{V_o C_o} \tag{3.153}$$

and wanting to main $\Delta V_o \leq 0.1V$, the output capacitance C_o value can be computed as follows:

$$C_o \geq \frac{P_o D_{MAX}}{V_o f_{SW}\ 0.1V} \geq 17\mu F\ . \tag{3.154}$$

Finally, the chosen normalized value of the output capacitance according to the E12 series is $C_o = 22\ \mu F$.
Then, the RMS output capacitor current is given by:

$$I_{Co} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_o\right)^2 - I_o^2}\ \cong 1.6\ A\ . \tag{3.155}$$

The maximum ESR of the output capacitor is computed as follows:

$$ESR_{max} = \frac{\Delta V_o}{I_{Co}\sqrt{12}} \cong 18\ m\Omega. \tag{3.156}$$

The maximum voltage across C_o is equal to:

$$V_{Co,max} = V_o = 19.5\ V. \tag{3.157}$$

To conclude the generic analysis of the LLC resonant power converter, the dead time t_d can be computed [17]:

$$t_d \geq 16\ \cdot\ 2C_{oss}\ \cdot\ L_m\ \cdot f_{SW}\ \geq 15\ ns \tag{3.158}$$

where $2C_{oss} = C_{oss1} + C_{oss2}$ is the sum of the primary side transistor output capacitances. The dead time t_d should be large enough to allow the discharging and the charging of the output capacitances of the primary side transistors before the complementary one

turns on or turns off. This is important to ensure the correct circuit operation and to achieve the ZVS turn-on and turn-off for the primary side transistors.
This topology has the drawback that the optimal operating point, and hence the maximum efficiency, is obtained only for a given input voltage and for a given load resistance. Indeed, it is typically designed under a switching frequency close to the resonant frequency f_{r1} and full load conditions [3].
Moreover, to achieve high peak voltage gain M_{g_ap}, a small inductance ratio L_n is needed. A small value of L_n means a small value of the magnetizing inductance L_m and high value of the resonant inductance L_r, which results in high primary current, high conduction losses and high switching losses of the primary side switches. However, small L_m guarantees the ZVS for the primary switches and hence a compromise is needed. A typical value of L_n is chosen between 3 and 7 [3].
As a consequence of these considerations, the other two topologies analysed in this chapter are preferred for the adapter mainly because they are able to reach high efficiency for a wide input voltage range [3], [8], [12].

3.4.3 Ideal circuits simulations

In this section, ideal circuit simulations are performed by using the *LTspice* software in order to compare their results with the theoretical analysis done previously. All simulations are performed with a transient analysis (*.tran*) and the ideal model of the converter components are considered except for the primary transistors as done in the other ideal simulations.
The main values that characterize the transistors are reported in Table 3.16 and the chosen values for the other components are reported in Table 3.17.

	Primary side transistors (GaN HEMT)
$V_{DS,MAX}$	600 V
$R_{DS,ON}$	190 mΩ
C_{oss}	28 pF

Table 3.16: LLC converter primary transistors parameters.

	Transformer	*Resonant Clamp Capacitor* C_r	Output Capacitor C_o
General design	L_m =16.5 uH L_r = 4.7 μH N = 5	C_r = 5.6 nF	C_o = 22uF

Table 3.17: LLC converter component values.

Figure 3.55 shows the LLC resonant power converter schematic implemented in *LTspice* for the simulations.

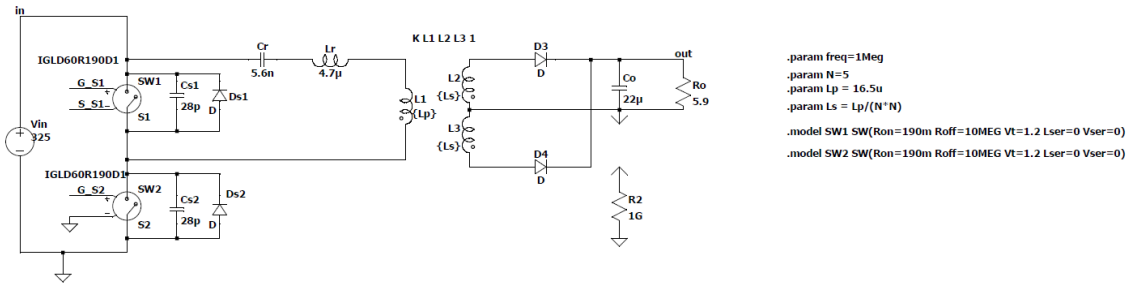


Figure 3.55: LTspice schematic of the LLC resonant power converter.

Two kinds of simulations are performed to measure how the efficiency changes according to the variation of the input voltage and then the variation of the load resistance.
Table 3.18 shows the efficiency measurements from the circuit simulations performed by varying the input voltage.

DC input voltage V_{in}	*Efficiency*
127 V	94 %
254 V	91.7%
325 V	96.1%
354 V	95.3%

Table 3.18: Efficiency results from the LLC ideal circuit simulations with different input voltages.

From Figure 3.56 to Figure 3.59, the current and voltage waveforms of the simulation results can be observed.
These figures show that the *S1* and the *S2* transistors are turned on and off with ZVS and the secondary side diodes ZCS turn off is always achieved. Therefore, the switching losses related to them are eliminated. Then, when the input voltage increases, the peak values of the current increases as well and the peak-to-peak voltage of the resonant capacitor increases.

Finally, according to the Table 3.18 which is obtained on the basis of these simulation results, the maximum efficiency is achieved for the DC input voltage V_{in} equal to 325 V and the load resistance R_o equal to 5.9 Ω.

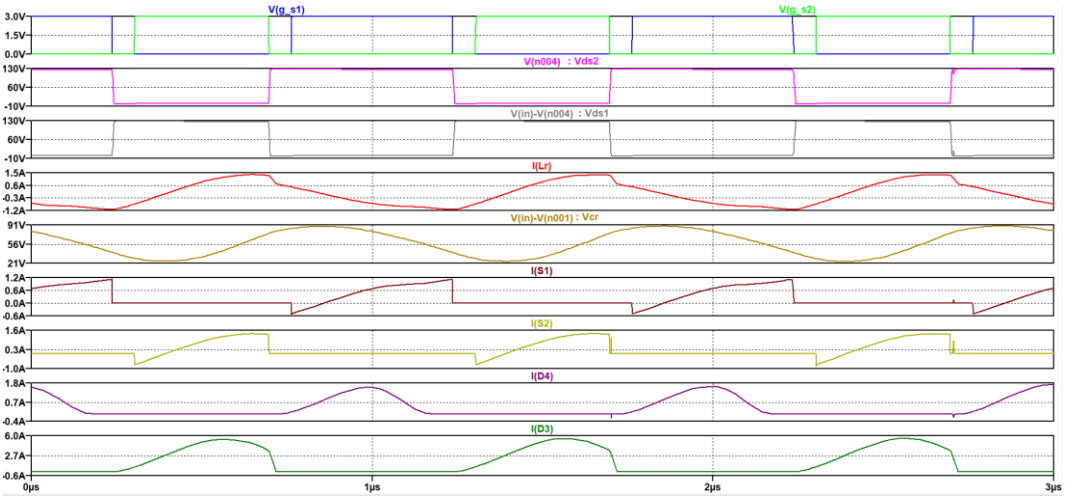


Figure 3.56: LLC simulation results with $V_{in\,(DC)}$ = 127 V and R_o = 5.9 Ω.

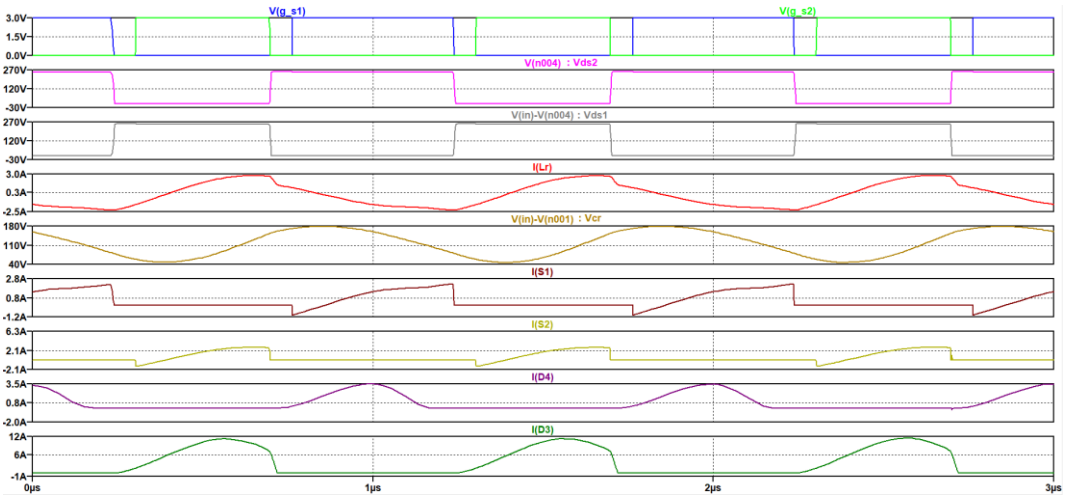


Figure 3.57: LLC simulation results with $V_{in\,(DC)}$ = 254 V and R_o = 5.9 Ω.

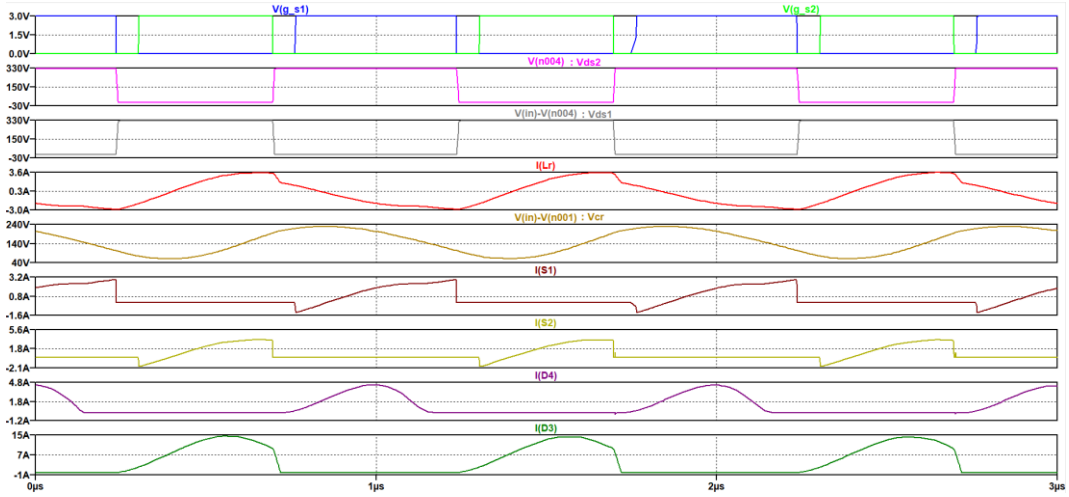


Figure 3.58: LLC simulation results with $V_{in\,(DC)} = 325V$ and $R_o = 5.9\ \Omega$.

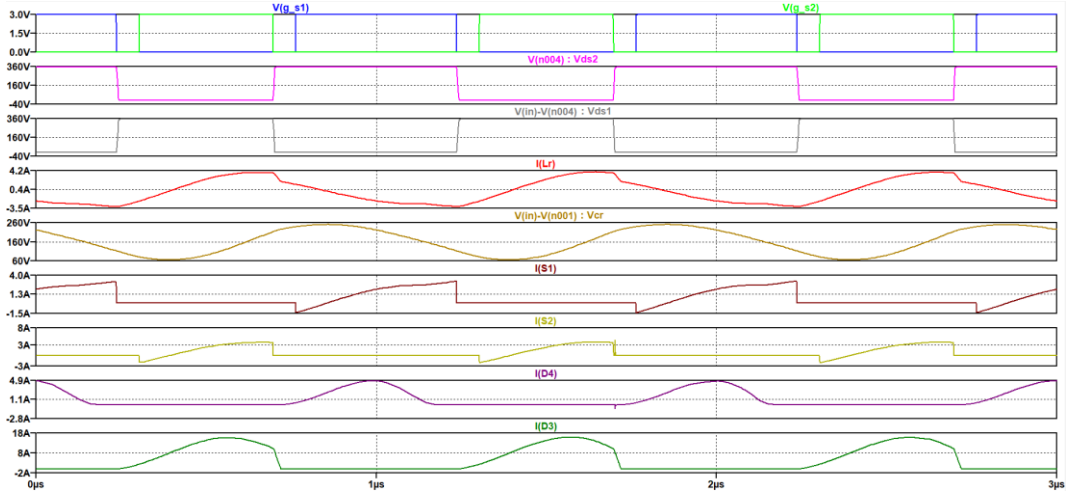


Figure 3.59: LLC simulation results with $V_{in\,(DC)} = 354V$ and $R_o = 5.9\ \Omega$.

The next step is to perform the circuit simulation increasing the load resistance of 50% with the input voltage V_{in} equal to 325 V. Under these conditions, the efficiency drops from 96.1% to 92.7%.

Therefore, the optimal operating point is obtained for the DC input voltage V_{in} equal to 325 V and the load resistance R_o equal to 5.9 Ω.

Chapter 4

AHBF converter with secondary side resonance scheme and primary current dip effect

This chapter is devoted to the AHBF converter topology with both secondary side resonance scheme and primary current dip effect.
Firstly, the reasons why this topology was preferred to others converters in this thesis work will be explained. Then, an overview of the real components already selected in the previous chapter and the procedure for the design of the coupled inductors will be reported. The next step is related to the simulation results, considerations about the power dissipation and the discussion of possible design improvements. Finally, a programmable digital controller from Texas Instruments has been properly selected to generate the control signals for the switching operation of the primary and secondary side transistors.

4.1 Motivations for selecting the AHBF topology

The AHBF converter topology has several advantages compared with the ACF converter and LLC resonant power converter topologies.
A considerable benefit of this topology is related to the electrical stress of the transistors. The maximum drain-to-source voltage of the primary side transistors is reduced by a factor equal to nV_o (being n the turn ratio of the coupled inductors and V_o the output voltage) while that of the secondary side transistor is reduced by V_o with respect to the ACF. This represents a good feature of the AHBF because it allows to have a larger safety margin for the choice of the transistors. Furthermore, transistors with lower rated voltages and consequently with a lower on-resistance can be selected, thus reducing the amount of dissipated power during their operation.

Another advantage with respect to the ACF topology deals with the presence of multiple energy storage elements, such as the leakage inductance, the magnetizing inductance, and the resonant capacitor. These elements store energy when the secondary side transistor does not conduct.
Moreover, compared to the LLC resonant power converter, the AHBF converter can operate correctly for a wide input voltage range, also achieving higher efficiency.
Finally, further improvements in terms of efficiency on the AHFB topology were made by implementing the secondary side resonance scheme and the current dip effect as previously discussed. The simulation results with the ideal component models and those with the real component models showed that the latter design increased the efficiency of the converter from 97.2% to 98.9% in the ideal case and from 96.5% to 97.6% in the real case.

4.2 Components selection

In this section a summary of the components chosen to implement the converter shown in Figure 4.1 is provided.

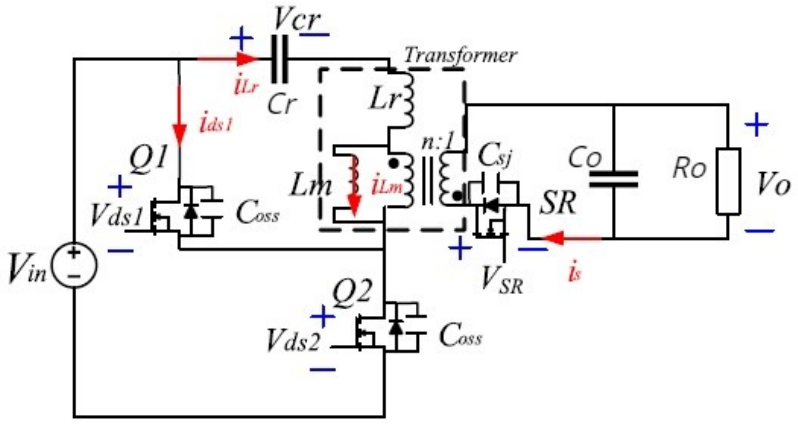


Figure 4.1: AHBF converter schematic [8].

4.2.1 Half-bridge GaN HEMTs

The GaN HEMT GS0650111L from GaN Systems has been chosen for the primary side transistors *S1* and *S2*.
Table 4.1 provides the characteristics of the selected component according to the maximum working voltage and the peak current previously computed.

Computed values	*GaN HEMT GS0650111L*
$V_{DS,MAX} = V_{IN,MAX} =$ 354 V $I_{SW,MAX}$ = 4.2 A	$V_{DS,MAX}$ = 650 V $I_{D,MAX}$ = 11 A C_{oss}= 20 pF $R_{DSon(MAX)}$ = 190 mΩ $R_{DSon(TYP)}$ = 150 mΩ

Table 4.1: AHFB primary side transistors parameters.

As already explained, this topology allows to choose a GaN HEMT device with lower rated voltage than 650 V since the maximum calculated is equal to 350 V, but a device with a lower rated voltage is not yet present in the market. Therefore, this topology can be further improved in the future.

4.2.2 Secondary side MOSFET

The Silicon MOSFET BSZ240N12NS3-G from Infineon has been chosen for the secondary side transistor *SR*.
Table 4.2 provides the characteristics of the selected component according to the maximum working voltage and the peak current previously computed.

Computed values	*Silicon MOSFET BSZ240N12NS3-G*
$V_{DS,MAX} = V_{IN,MAX}/n$ = 71 V $I_{SW,MAX}$ = 27 A	$V_{DS,MAX}$ = 120 V $I_{D,MAX}$ = 37 A $C_{oss(MAX)}$ = 230 pF $C_{oss(TYP)}$ = 170 pF $R_{DSon(MAX)}$ = 24 mΩ $R_{DSon(TYP)}$ = 21 mΩ

Table 4.2: AHFB secondary side transistor parameters.

To implement the current dip effect, as explained in the previous chapter, a capacitor with a value equal to 680 pF in a parallel combination with the secondary side transistor is needed. Therefore, the GCM21A5C2E821JX01 ceramic capacitor from Murata has been chosen to this purpose.

4.2.3 Resonant capacitor

The C1825C105K2RAC X7R multilayer ceramic capacitor from KEMET has been chosen for the resonant capacitor C_r to meet the specifications needed to implement the secondary side resonance scheme.
Table 4.3 provides the characteristics of the selected component according to the computed voltage across the resonant capacitor.

Computed value	*C1825C105K2RAC X7R*
$V_{Cr} = 97.5$ V $C_r = 3.3$ µF	$V_{rated} = 200$ V $C_r = 1$ µF

Table 4.3: AHBF resonant capacitor parameters.

4.2.4 Output capacitor

The 885012106031 X5R WCAP-CSGP multilayer ceramic capacitor from Wurth Elektronik has been chosen for the output capacitor C_o. Three capacitors in a parallel combination are used to have a total capacitance close to 30 µF and a ESR value close to 3.7 mΩ.
Table 4.4 provides the characteristics of the selected component according to the maximum working voltage and ESR.

Computed values	*885012106031 X5R (x 3)*
$V_{Co,MAX} = V_o + \Delta V_o = 19.5$ V + 0.1 V $C_o = 30$ µF ESR = 3.7 mΩ	$V_{rated} = 25$ V $C_o = 10$ µF ESR = 10 mΩ

Table 4.4: AHBF output capacitor parameters.

4.2.5 Coupled inductors

Magnetic components are difficult to design since several factors must be considered to design them correctly, such as the parasitic elements, size, etc. Also, quantifying copper losses and core losses adds more difficulty to the design. For these reasons, it

is usually difficult to find catalogues containing already designed magnetic components, therefore they must be designed ad hoc for each project.
Concerning the materials used in the construction of the core, for frequencies higher than a few tens of kHz, two types of materials are usually employed: ferrites and powders [18].
Ferrites are ceramic materials composed of iron oxides and other metal oxides. The most commonly used types of ferrites are the following:

- Ferrite Zinc-Manganese (ZnMn);
- Ferrite Zinc-Nickel (ZnNi).

The main feature of these materials is to have a high resistivity and therefore they are considered insulating materials. Moreover, ZnMn ferrites are employed for frequencies close to few MHz and they are characterized by a high relative permeability around 10^3-10^4. Instead, ZnNi ferrite are employed for frequencies up to a few tens of MHz and they are characterized by a lower relative permeability around 50-500 [18].
Powders are obtained from powders of natural magnetic materials such as iron, nickel, and carbon monoxide. It is an insulating material because the granules of magnetic material are isolated from each other, moreover the relative permeability is quite low because there is air among the granules of magnetic material. Compared to ferrites, powders are characterized by a higher saturation magnetic flux density [18].
Focusing now on core shapes, different types can be found:

- E cores;
- Pot cores;
- Cubic cores (RM);
- Toroids.

The toroidal and E shaped cores can be found in both powders and ferrite, while the pot and cubic cores are made of ferrite material only.
At this point, the design of two different coupled inductors will be presented to compare some results such as the wire losses and the relative copper losses. Other results, such as the estimation of parasitic parameters, can be obtained through experimental measurements or they can be provided by the manufacturer.
The first design is carried out with a ferrite material and RM shaped core.
The chosen material is the SIFERRIT material N49 from TDK, it is a ZnMn ferrite, and it is typically used for high frequency power transformers between 300 kHz and 1 MHz.
The main parameters extracted from the datasheet of the material and useful for the design are shown in Table 4.5.

	N49 ZnMn Ferrite
Sat. flux density B_s @25°	490 mT
Resistivity	17 Ω·m
Relative initial permeability	1500

Table 4.5: N49 Ferrite material parameters.

The chosen core shape is the RM8 from TDK. The dimensions of the core are reported in Table 4.6.

	RM8 core shape
Window area A_w	0.30 cm^2
Minimum core area A_c	0.55 cm^2
Core volume V_e	1.86 cm^3
Average length of turns MLT	4.2 cm

Table 4.6: RM8 core shape parameters.

Before proceeding with the magnetic design, the maximum magnetizing current, the primary and secondary RMS currents, and the total RMS current must be defined.
The maximum magnetizing current, which was computed in the previous chapter, is $I_{Lm,MAX} = 4$ A.
The primary and secondary RMS currents are obtained as follows:

$$I_{P,RMS} = I_{P,MAX}\sqrt{\frac{D_{MAX}}{3}} = 2 \text{ A} \tag{4.1}$$

$$I_{S,RMS} = I_{S,MAX}\sqrt{\frac{1 - D_{MAX}}{3}} = 8 \text{ A} \tag{4.2}$$

where $I_{P,MAX}$ is the maximum primary current equal to 4.2 A, $I_{S,MAX}$ is the maximum secondary current equal to 27 A and D_{MAX} is the maximum duty cycle equal to 0.75.
The total RMS current reflected at the primary side is given by:

$$I_{TOT,RMS} = I_{P,RMS} + \frac{1}{N} I_{S,RMS} = 3.6 \text{ A} \tag{4.3}$$

where N is the primary to secondary turns ratio equal to 5, as computed in Chapter 3 Section 3.3.
Another parameter needed for the design is the fill factor K_u, that represents the portion of the core window area filled with copper. Its value is between 0 and 1, and typical values of K_u for this application is approximately equal to 0.3 [5].

The maximum power dissipated by the coupled inductors is considered equal to the 1% of the output power P_{out}, therefore $P_{D,MAX}$ = 650 mW.
The maximum magnetic flux density is computed as follows:

$$B_{MAX} < B_S \frac{V_{in,min}}{V_{inMAX}} < 176\ mT. \tag{4.4}$$

Therefore, B_{MAX} = 50 mT has been chosen.
The next step is to compute the core geometrical constant K_g to check if the chosen core meets this requirement.
The core geometrical constant K_g is given by [5]:

$$K_g \geq \frac{\rho L_m^2 I_{TOT,RMS}^2\ I_{Lm,MAX}^2}{B_{MAX}^2 K_u P_{D,MAX}} x10^8 \geq 0.0073\ cm^5 \tag{4.5}$$

where ρ is the resistivity of the copper wire equal to $1.724 \cdot 10^{-6}$ Ω·cm.
K_g can also be computed as follows:

$$K_g = \frac{A_c^2 A_w}{MLT}. \tag{4.6}$$

From the Equation (4.6) and by considering the parameters reported in the Table 4.6, the RM8/N49 core has a core geometrical constant K_g equal to 0.029 cm^5 which meets the constraint defined with the Equation (4.5).
Relative core losses are obtained in the following way:

$$P_V = \frac{\frac{1}{2} P_{D,MAX}}{V_e} \cong 175\ \frac{kW}{m^3}. \tag{4.7}$$

The dimensions of the wires must be defined to compute the losses in the wires. The number of the primary winding turns n_1 and of the secondary winding turns n_2 can be achieved as follows [5]:

$$n_1 = \frac{L_m I_{Lm,MAX}}{B_{MAX} A_c} 10^4 = 14.5\ turns\ \rightarrow 15\ turns \tag{4.8}$$

$$n_2 = \frac{1}{N} n_1 = 3\ turns\ \rightarrow 3\ turns. \tag{4.9}$$

The portions of the window area assigned to primary winding 1 and secondary winding 2 are selected as follows [5]:

$$\alpha_1 = \frac{I_{P,RMS}}{I_{TOT,RMS}} = 0.55 \tag{4.10}$$

$$\alpha_2 = \frac{n_2 I_{S,RMS}}{n_1 I_{TOT,RMS}} = 0.44. \tag{4.11}$$

Therefore, the wire gauges can be computed [5]:

$$A_{wire1} \leq \frac{\alpha_1 K_u A_w}{n_1} \leq 0.33\ mm^2 \tag{4.12}$$

$$A_{wire2} \leq \frac{\alpha_2 K_u A_w}{n_2} \leq 1.3\ mm^2. \tag{4.13}$$

According to Equation (4.12) and Equation (4.13), #23 AWG (0.259 mm^2) for wire 1 and #17 AWG (1.04 mm^2) for wire 2 can be suitable.
The wire resistance can be obtained according to the following equation:

$$R_w = \frac{\rho MLTn}{A_{wire}}. \tag{4.14}$$

By combining Equation (4.14) with the previous computed values of the wire gauges and the number of winding turns, the primary wire resistance R_{wp} = 42 mΩ and the secondary wire resistance R_{ws} = 2 mΩ are obtained.
At this point, the losses in the wires can be determined from the wire resistances and primary and secondary RMS currents:

$$P_{wire} = R_{wp} i_{p,RMS}^2 + R_{ws} i_{s,RMS}^2 = 296\ mW. \tag{4.15}$$

The second design is carried out with a powder material and E shaped core.
The chosen material is the MIX 18 material from Micrometals, it is a carbonyl iron powder mix material, and it is typically used for high frequency power transformers up to 1.3 MHz.
The main parameters extracted from the datasheet of the material and useful for the design are shown in Table 4.7.

	MIX 18 powder
Sat. flux density B_s @25°	1.78 T
Relative initial permeability	55

Table 4.7: MIX 18 powder material parameters.

The chosen core shape is the E137 shape from Micrometals. The dimensions of the core are reported in Table 4.8.

	E137 core shape
Window area A_w	1.54 cm^2
Effective core area A_c	0.907 cm^2
Core volume V_e	6.72 cm^3
Average length of turns MLT	6.99 cm

Table 4.8: E137 core shape parameters.

The same procedure previously followed is resumed for this design.
The maximum magnetic flux density is computed according to the Equation (4.4) and it must be lower than 640 mT.
From the datasheet of the material, B_{MAX} is approximately equal to 14 mT thus satisfying the constraint imposed by the Equation (4.4).
The next step is to compute the core geometrical constant K_g to check if the chosen core meets this requirement. K_g is computing by using the Equation (4.5) and it must be higher than 0.094 cm^5.
From the Equation (4.6) and by considering the parameters reported in the Table 4.8, the E137/18 core has a core geometrical constant K_g equal to 0.18 cm^5 which meets the constraint defined with the Equation (4.5).
As done previously, relative core losses are computed according to the Equation (4.7) and $P_v = 48$ kW/m^3 is obtained.
The dimensions of the wires must be defined to compute the losses in the wires. The number of the primary winding turns n_1 and of the secondary winding turns n_2 can be achieved following Equation (4.8) and Equation (4.9), deriving $n_1 = 35$ and $n_2 = 7$.
The portion of the window area assigned to primary winding 1 and secondary winding 2 are the same as the previous design since the turn ratio has not changed.
The wire gauges can be computed from the Equation (4.12) and (4.13) obtaining $A_{wire1} \leq 0.726$ mm^2 and $A_{wire2} \leq 2.9$ mm^2. Therefore, #20 AWG (0.518 mm^2) for wire 1 and #15 AWG (1.65 mm^2) for wire 2 can be suitable.
The wire resistance can be obtained by combining Equation (4.14) with the previous computed values of the wire gauges and the number of windings turns, the primary wire resistance $R_{wp} = 81$ μΩ and the secondary wire resistance $R_{ws} = 5$ μΩ are obtained.
At this point, the losses in the wires can be determined from the wire resistances and primary and secondary RMS currents, getting $P_{wire} = 0.64$ mW.
Finally, it is possible to make a comparison between the two coupled inductors designs highlighting how the relative core losses are reduced from 175 kW/m^3 to 48 kW/m^3 and the wire losses are reduced from 296 mW to 0.64 mW.

4.2.5.1 Real coupled inductors

The electrical specifications of the coupled inductors required for this project have been provided to the Italtras manufacturer with the aim of building them.
The coupled inductors specifications are reported in Table 4.9 and the required schematic is shown in Figure 4.2.

Figure 4.2 shows the presence of two auxiliary windings, necessary for the controller and gate drivers power supplies. This aspect will be described in detail in the next chapter.

Output power	P_o = 65 W
Operating frequency	f_{SW} = 1 MHz
Magnetizing inductance	L_m = 10 µH
Leakage inductance	L_{lk} = 5.6 nH
Primary-to-secondary turns ratio	$N_{ps} = N_p/N_s = 5$
Primary-to-primary auxiliary turns ratio	$N_{p\_ap} = N_p/N_{ap} = 7$
Secondary-to-secondary auxiliary turns ratio	$N_{a\_as} = N_a/N_{as} = 2$
Primary side	V_{pMAX} = 256.5 V V_{pmin}= -97.5 V I_{pMAX}= 4.2 A I_{pRMS}= 2 A
Secondary side	V_{sMAX}= 51.3 V V_{smin}= -19.5 V I_{sMAX}= 27 A I_{sRMS}= 8 A
Primary auxiliary side	V_{MAX}= 13.9 V V_{min}= -36.6 V I_{MAX}= 100 mA
Secondary auxiliary side	V_{MAX}= 51 V V_{min}= -25.7 V I_{MAX}= 100 mA

Table 4.9: Coupled inductors specifications.

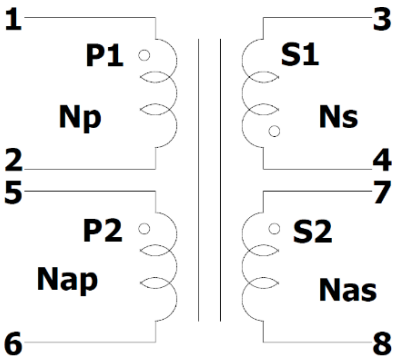


Figure 4.2: Coupled inductors schematic.

The coupled inductors realized by the manufacturer present the following characteristics:

- $L_m = 10.9\ \mu H$;
- $L_{lk} = 2\ \mu H$;
- $N_p = 13$;
- $N_s = 2.6 \cong 3$;
- $N_{ps} = 4.33$;
- $N_{ap} = 1.8 \cong 2$;
- $N_{as} = 1.3 \cong 1$.

The L_m and turns values satisfy the specifications since the magnetizing inductance L_m must be lower than 18 μH and the primary-to-secondary turns ratio N_{ps} value must be close to 4.8, as computed in Chapter 3. Therefore, these values can be acceptable.
However, the value of the obtained leakage inductance L_{lk} equal to 2 μH is too high to achieve a good circuit behaviour implementing the resonance scheme discussed in the previous chapter. This happens because this leakage inductance value implies a value of the resonant capacitor C_r lower than 7 nF, following the reasoning discussed in Chapter 3 and according to the Equation (3.103). Since the output capacitance C_o must be higher than 25 μF to satisfy the required output voltage ripple, the value of the resonant capacitor C_r is low to involve the output capacitor C_o in the resonance process. The value of the resonant capacitor C_r must be a few μF and the desired leakage inductance L_{lk} must be lower than 14 nH to achieve the optimal resonance scheme.
Until now, it has been difficult to fabricate the coupled inductors with the leakage inductance almost equal to 5.6 nH. A method for obtaining a lower leakage inductance value at high frequency (i.e., MHz), which is discussed in literature, consists of interleaving primary and secondary windings. For example, the winding configuration 1S1P (1-Secondary-1-Primary) allows to obtain leakage inductance of the order of nH [19]. The 1S1P winding configuration is shown in Figure 4.3.

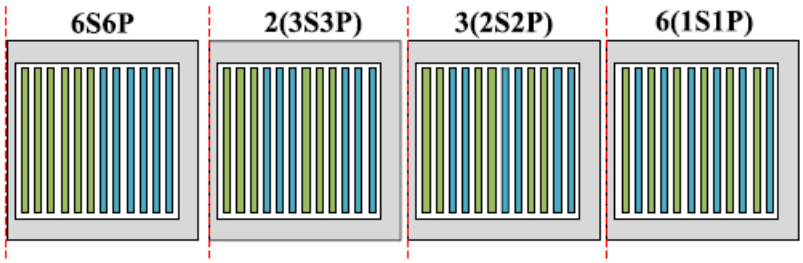


Figure 4.3: 1S1P winding configuration [19].

However, the coupled inductors realized by implementing the interleaved winding configuration may not meet the requirements imposed by the electrical safety norm IEC 62368-1, since the primary and the secondary windings are very close to each other. To comply with the IEC 62368-1 standard, a minimum distance must be guaranteed between the primary and the secondary windings or each winding must be covered by an insulating material to ensure insulation.
The IEC 62368-1 norm applies for the verification of the safety of electrical and electronic devices in the audio, video, information and communication technologies [20]. Concerning the transformer, for a maximum RMS input voltage equal to 250 V, the peak insulation test voltage must be approximately 3 kV[1].

4.3 Simulations with real component models and design improvements

After defining the components necessary to implement the improved design in terms of efficiency of the AHBF converter, the simulation results with the real component models are presented below.
Figure 4.4 shows the current and voltage waveforms of the circuit simulations when the RMS value of the input voltage V_{in} is equal to 230 V.
The waveforms reported in this figure confirm the results obtained with the ideal circuit simulation regarding the ZVS turn on and turn off for both the *S1* and the *S2* transistors. The transistor *S3* turns off with ZCS thus contributing to the switching losses reduction.
Furthermore, from the i_{Lr} current waveform, the dip in the resonant current i_{Lr} immediately after the *S2* turn off can be observed. This current dip reduces the RMS resonant current $i_{Lr,rms}$ and more current is transferred from the primary side of the converter to the secondary one thus increasing the efficiency.
The simulation results also confirm the value of the output voltage ripple ΔV_o which remains below 0.1 V.
Finally, the theoretical analysis and the ideal simulation results are confirmed by the simulations with real model components.

[1]https://ulstandards.ul.com/wp-content/uploads/2021/02/iec62368-1_draft_4b.pdf, page 249, Table G.4.

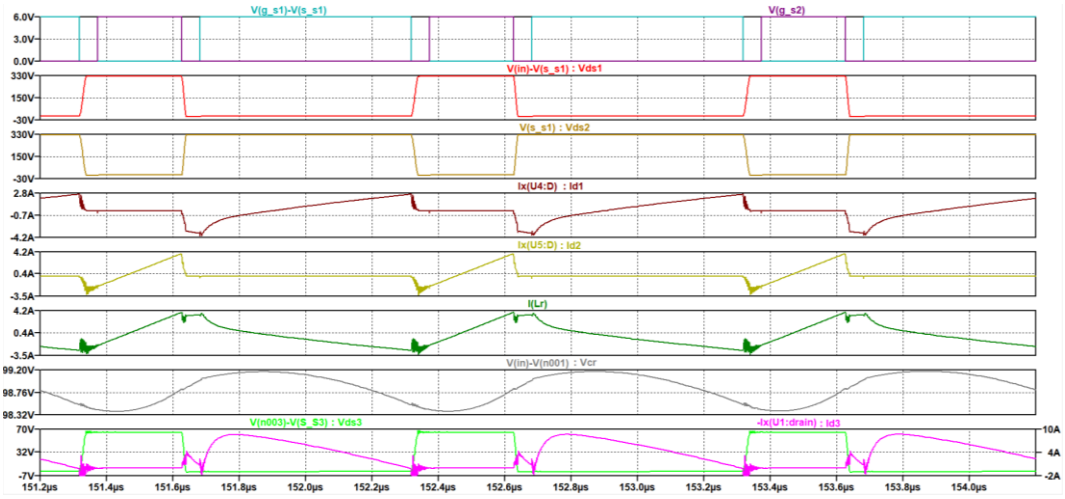


Figure 4.4: Circuit simulation results with real component models of the AHBF converter with both current dip effect and secondary side resonance scheme.

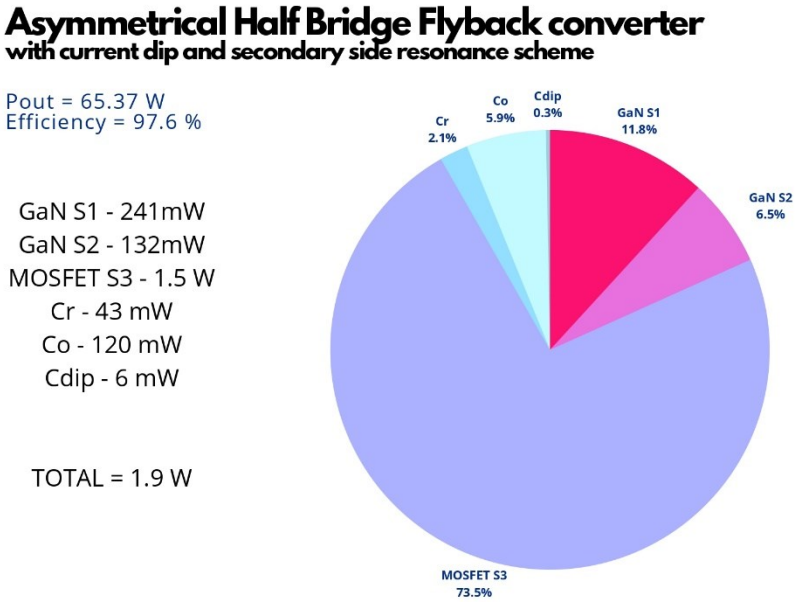


Figure 4.5: AHBF with current dip and secondary side resonance scheme power dissipation.

The power dissipated by each element is computed directly from the *LTspice* software and the results are shown in Figure 4.5. From the pie chart reported in this figure it is possible to notice how the component that dissipate the most power is the secondary side transistor due to the high RMS current and its on resistance. Therefore, the power

dissipation related to this transistor can be reduced by selecting a device with a lower on resistance.
To improve the AHFB converter design, the Silicon MOSFET IPA105N15N3-G from Infineon has been selected. This device has a lower typical on-resistance equal to 9.1 mΩ which allows to reduce the dissipated power.
Table 4.10 provides the characteristics of the selected component.

$V_{DS,MAX}$	150 V
$R_{DS,ON(MAX)}$	10.5 mΩ
$R_{DS,ON(TYP)}$	9.1 mΩ
$I_{D,MAX}$	37 A
C_{OSS}	378 pF

Table 4.10: Silicon MOSFET IPA105N15N3-G parameters.

Moreover, the output capacitance is higher with respect to the previous selected transistor, but it is suitable for this design because the current dip effect has to be implemented. Also, the value of the capacitor in a parallel combination with this transistor can be reduced from 820 pF to 680 pF and the 12062A681KAT2A ceramic capacitor from Kyocera AVX is chosen.
Figure 4.6 shows the simulated current and voltage waveforms of the circuit with the new secondary side transistor. These simulations are performed with the input voltage $V_{in,rms}$ equal to 90 V. The theoretical analysis and the results of the previous simulations are confirmed: the *S1* and the *S2* transistors turn on and off with ZVS, the dip in the resonant current i_{Lr} immediately after the *S2* turn off is present and the transistor *S3* turns off without ZCS at low input voltage. However, this is not a big issue because, when the transistor is turned off, the drain-to-source voltage is equal to zero and consequently the switching losses are also zero.
Instead, at higher input voltage such as $V_{in,rms}$ equal to 230 V and $V_{in,rms}$ equal to 250 V, the transistor *S3* turns off with ZCS as shown in Figure 4.7 and Figure 4.8. This happens because as the input voltage increases, the turn-on time of the transistor *S3* also increases and the current flowing through it reaches zero when it is switched off. Then, the value of the output voltage ripple ΔV_o is lower than 0.1 V.
The schematic of the simulated circuit is shown in Figure 4.9.

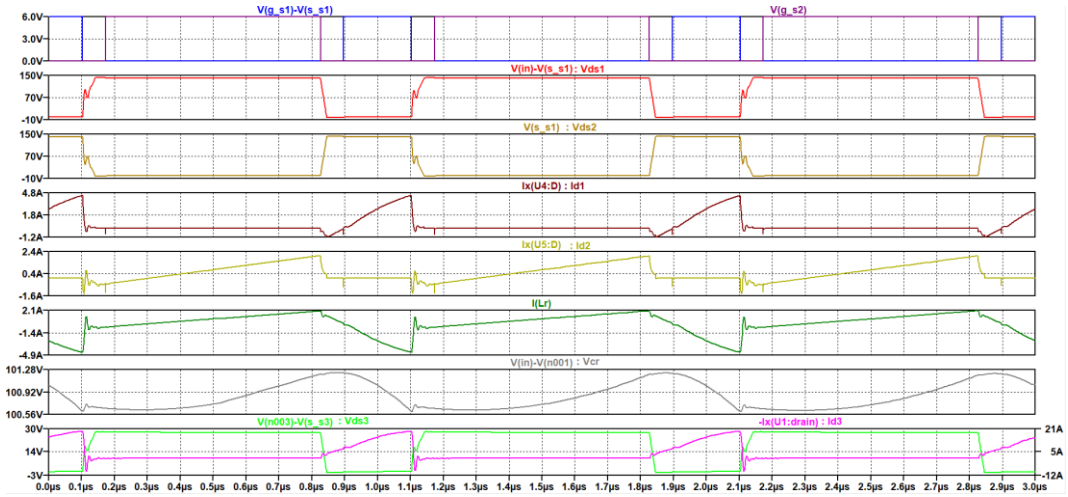


Figure 4.6: Circuit simulation results with real component models of the AHBF converter with both current dip effect and secondary side resonance scheme, with IPA105N15N3-G secondary side transistor and $V_{in,rms}$ = 90 V.

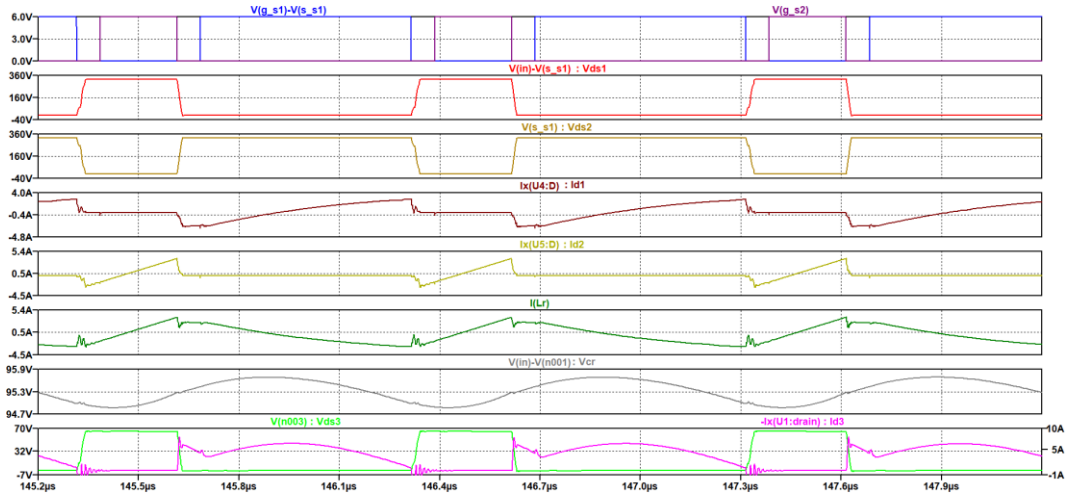


Figure 4.7: Circuit simulation results with real component models of the AHBF converter with both current dip effect and secondary side resonance scheme, with IPA105N15N3-G secondary side transistor and $V_{in,rms}$ = 230 V.

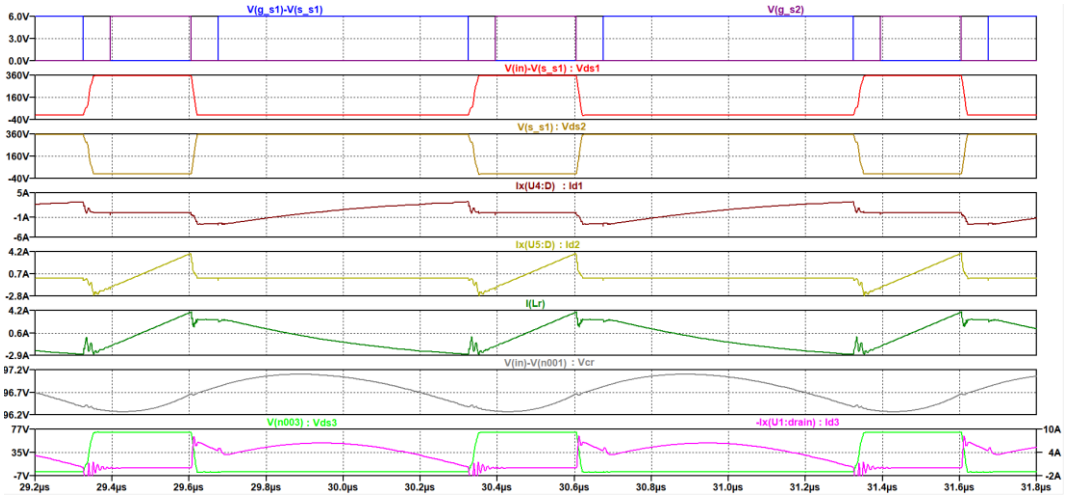


Figure 4.8: Circuit simulation results with real component models of the AHBF converter with both current dip effect and secondary side resonance scheme, with IPA105N15N3-G secondary side transistor and $V_{in,rms}$ = 250 V.

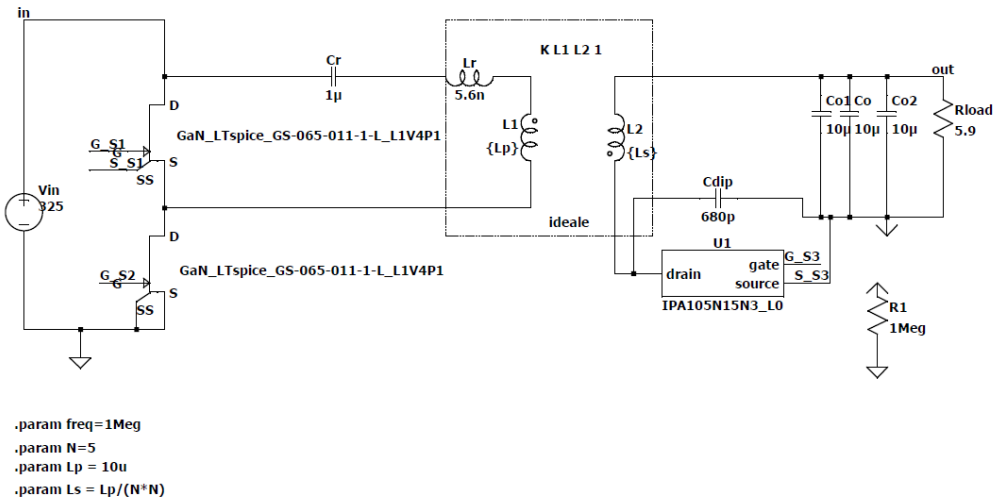


Figure 4.9: AHBF converter LTspice schematic with IPA105N15N3-G.

The power dissipated by the secondary side transistor has been significantly reduced from 1.5 W to 510 mW due to its lower on-resistance and the efficiency has increased up to 97.97%, as shown in Figure 4.10.

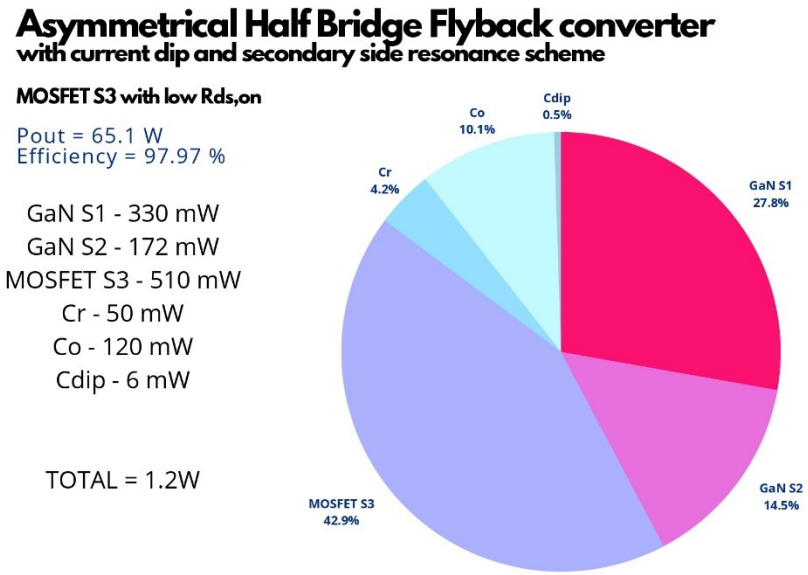


Figure 4.10: AHBF with current dip and secondary side resonance scheme power dissipation, with IPA105N15N3-G secondary side transistor.

4.4 Control method

The control signals for the switching operations of the primary and secondary side transistors are generated by the UCC28780 controller from Texas Instruments. This component is a transition-mode (TM) active clamp flyback controller which consists of advanced control schemes able to reduce the size of the passive components for high power-density and high efficiency applications [21]. The control method is optimized both for Si and GaN transistors in half-bridge configuration, it can operate at high switching frequency up to 1 MHz and allows to achieve ZVS over a wide operating range [21].

In this thesis work, the UCC2870 controller was adapted to the Asymmetrical Half Bridge Flyback converter topology for its ability to operate at a higher switching frequency such as 1 MHz and because the dead-time values reported in the datasheet specifications are compatible with those computed during the AHBF converter design and obtained from the simulations. For this purpose, the control law of the controller has been studied from its datasheet and the components involved in its operation have been appropriately designed for the AHBF topology.

The simplified schematic of the UCC28780 controller used for the ACF converter is shown in Figure 4.11.

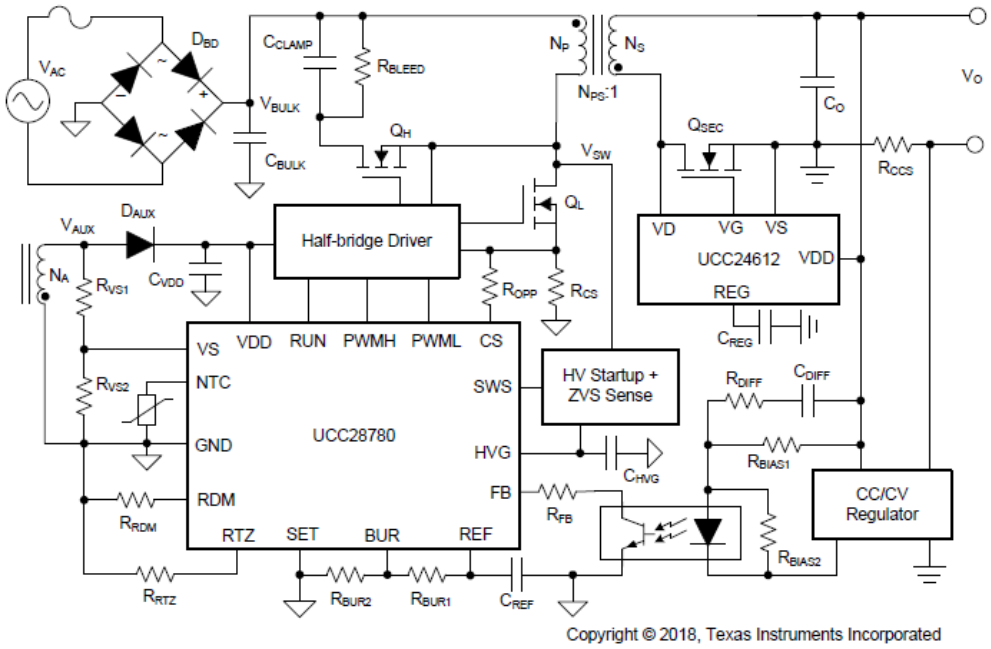


Figure 4.11: UCC28780 high frequency controller simplified schematic[21].

4.4.1 Operating modes

The adaptive ZVS control mode is able to auto-tune the on-time of the high side switch through the ZVS sensing network connected between the switching node and the SWS pin of the controller. The controller adaptively achieves ZVS for the low side switch over wide input voltage range and load conditions. The auto-tuning guarantees the ZVS even in the presence of component tolerances, input and output voltage variations, and temperature changes [21].

The high voltage sensing network (HV network) yields the copy of the switching node voltage V_{SW} to the ZVS discriminator block. The latter identifies the ZVS condition and corrects the on-time of the high side switch t_{DM}, cycle by cycle, by detecting if the V_{SW} reaches a fixed threshold value within the dead time t_z. t_z is the dead time between PWMH falling edge and PWML rising edge. If V_{SW} has not reached the threshold value within the defined time interval, the ZVS discriminator sends a signal to the t_{DM} optimizer block to increase t_{DM} for the next cycle. In this way, the magnetizing current decreases and V_{SW} reaches zero within t_z. This operation lasts a few cycles afterwards the t_{DM} optimizer sets the on-time of the high side switch and the ZVS for the low side switch is achieved [21].

Figure 4.12 shows the block diagram and the waveforms of the PWML and PWMH signals, and of the magnetizing current of the adaptive ZVS control mode.

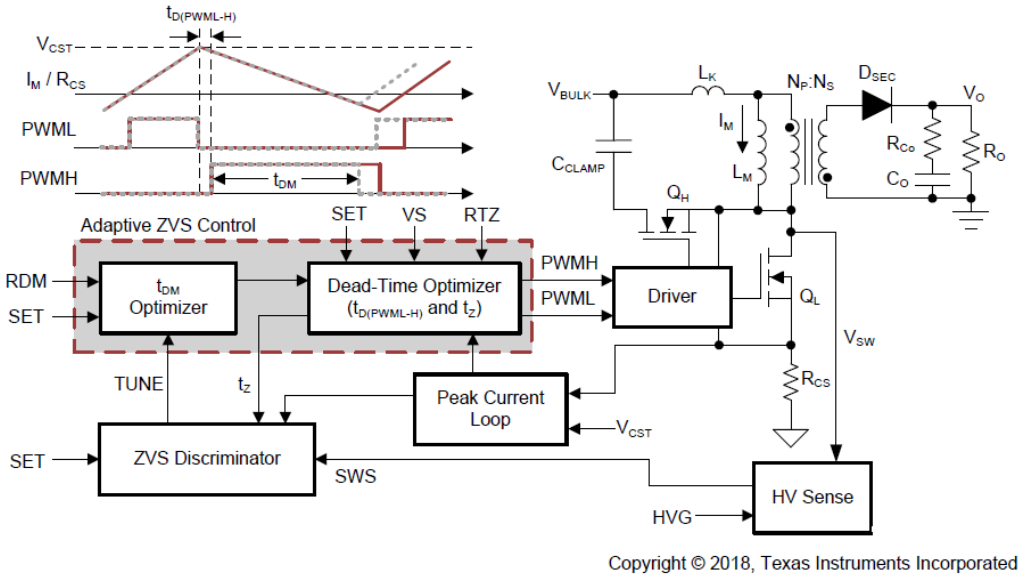


Figure 4.12: Block diagram and waveforms of the adaptive ZVS control mode [21].

The dead times are controlled by the dead-time optimizer block shown in Figure 4.12. There are two dead times:

- $t_{D(PWML-H)}$, the dead time between the PWML falling edge and the PWMH rising edge;
- t_Z, the dead time between the PWMH falling edge and the PWML rising edge.

The dead time t_Z is modulated by the adaptive control law which uses the line feed-forward signal to increase t_z as V_{BULK} decreases[21]. V_{BULK} is the rectified input voltage, and it is sensed by the VS pin through the voltage V_{AUX} across the auxiliary primary winding when the low side transistor is turned on. Then, the voltage V_{AUX} is converted in the line sensing current I_{VSL} that flows out of the VS pin through the upper resistor of a voltage divider [21]. Figure 4.13 shows how the minimum dead time is obtained with maximum input voltage and the maximum dead time with minimum input voltage.

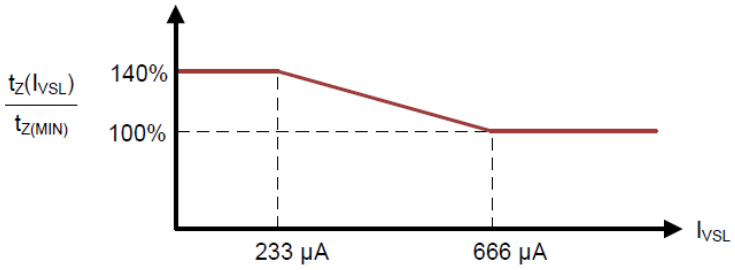


Figure 4.13: t_z dead time optimization [21].

The dead time $t_{D(PWML-H)}$ can be programmed through the SET pin voltage. There are two cases:

- V_{SET} = 0 V, the dead time is optimized for GaN devices;
- V_{SET} = 5 V, the dead time is optimized for Silicon devices.

In this work, the SET pin voltage must be equal to zero and a dead time around 40 ns is fixed. This time interval is suitable both for heavy load and light load as shown in Figure 4.14.
Furthermore, the minimum dead time computed in the design section of the AHBF converter is equal to 32 ns and therefore it is compatible with that set by the controller.

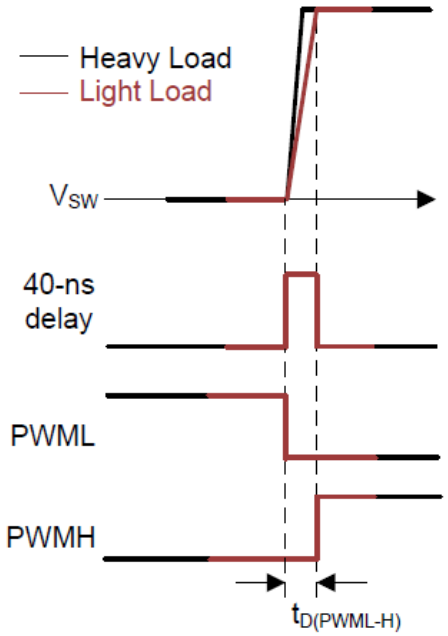


Figure 4.14: $t_{D(PWML-H)}$ dead time optimized for GaN devices [21].

The UCC28780 controller employs four different operating modes to maximize the efficiency over wide load conditions [21]:

- Adaptive Amplitude Modulation (AAM): it regulates the peak primary current at high load.
- Adaptive Bust Mode (ABM): it modulates the number of pulses of each burst packet at medium load.
- Low Power Mode (LPM): it decreases the peak primary current of each two-pulse burst packet at light load.
- Standby Power (SBP) mode: it reduces the losses during no load.

During AAM operating mode the ZVS tuning is enabled, while during LPM and SBP operating modes the ZVS tuning, and the high side transistor are disabled.
Figure 4.15 shows the control law over wide load conditions, where:

- V_{CST} is the peak current threshold that is compared with the current sense voltage from the CS pin;
- f_{SW} is the switching frequency;
- f_{BUR} is the burst frequency;
- N_{SW} is the number of pulses of each burst packet.

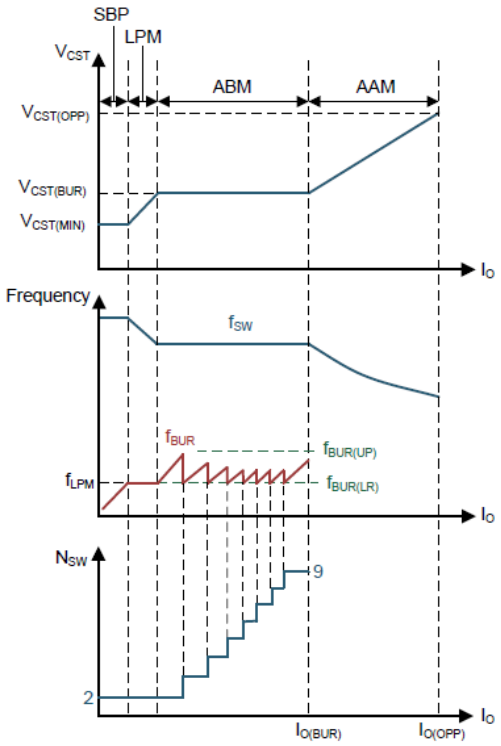


Figure 4.15: Control law over wide load conditions [21].

The **AAM** alternates the PWML and the PWMH in a complementary way with a dead time in between. When the load current decreases, the negative magnetizing current does not change while the positive magnetizing current is reduced by the internal peak current loop in order to keep the output voltage regulated [21]. The RUN signal remains high during this operating mode, therefore the driver of the half bridge is active. The switching pattern is shown in Figure 4.16.

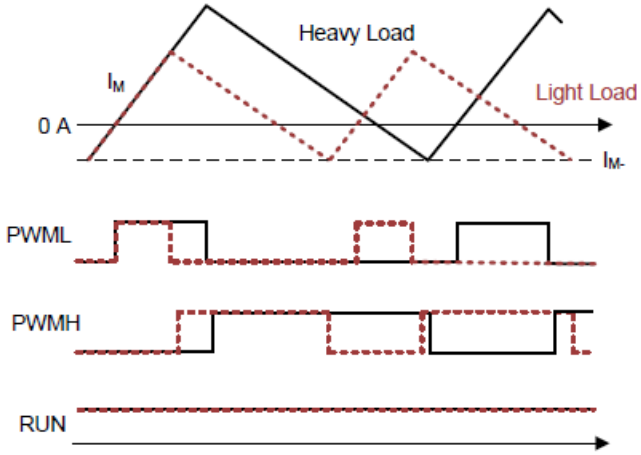


Figure 4.16: Switching pattern in AAM [21].

When the load current decrease and V_{CST} reaches the burst mode threshold voltage $V_{CST(BUR)}$, as shown in Figure 4.15, the UCC28780 controller enters in **ABM**. In this operating mode, the peak magnetizing current and the switching frequency are kept constant for each switching cycle and for a given input voltage [21]. As shown in Figure 4.17, when the RUN signal is activated, a time delay between the rising edge of the RUN signal and the one of the PWML signal is needed in order to allow the gate driver and the controller to reactivate after a wait state [21].

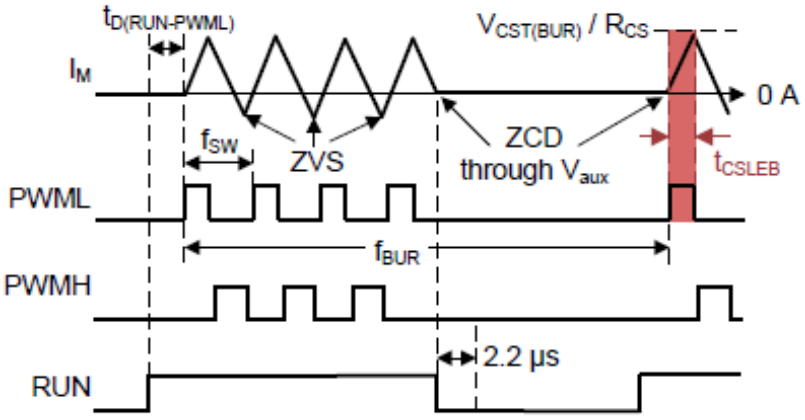


Figure 4.17: Switching pattern in ABM [21].

The first PWML pulse turns on the low side switch by detecting the condition of zero crossing detection (ZCD) on V_{AUX}. Then, in the following switching cycles the ZVS condition is achieved since the PWMH signal is enabled. When the number of PWML pulses N_{SW} in the burst packet is equal to a reference value, the RUN signal is disabled

after the ZCD of the last switching cycle through V_{AUX}. This situation puts the half bridge driver and the controller in a wait state to allow the reduction of their quiescent current [21].
When the number of pulses in the burst packet drops to the minimum value, i.e. two, and the burst frequency is lower than the minimum target value, the controller enters **LPM** mode and the PWMH signal is deactivated.
The aim of the LPM is to obtain a soft peak current transition between $V_{CST(BUR)}$ and $V_{CST(MIN)}$. In this operating mode, N_{SW} is fixed equal to two and the burst frequency is equal to the minimum value. When ZCD is detected at the end of the second pulse, the RUN signal is deactivated and the controller enters in low-power wait state [21].
Figure 4.18 shows the switching pattern in LPM operating mode.

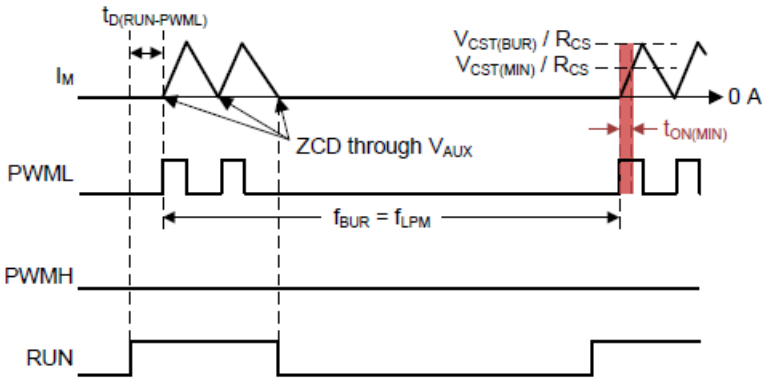


Figure 4.18: Switching pattern in LPM [21].

The last operating mode is the **SBP** mode. When V_{CST} reaches $V_{CST(MIN)}$, the controller enters SBP mode and the PWMH is still disabled.
The aim of the SBP is to reduce the burst frequency to minimize the standby power. In this operating mode, N_{SW} is still fixed equal to two and V_{CST} to $V_{CST(MIN)}$, while the burst off-time is modulated to keep the output voltage regulated. Furthermore, the burst frequency reduction puts the gate driver and the controller in a wait state to decrease the static power loss [21].
Figure 4.19 shows the switching pattern in SBP operating mode.

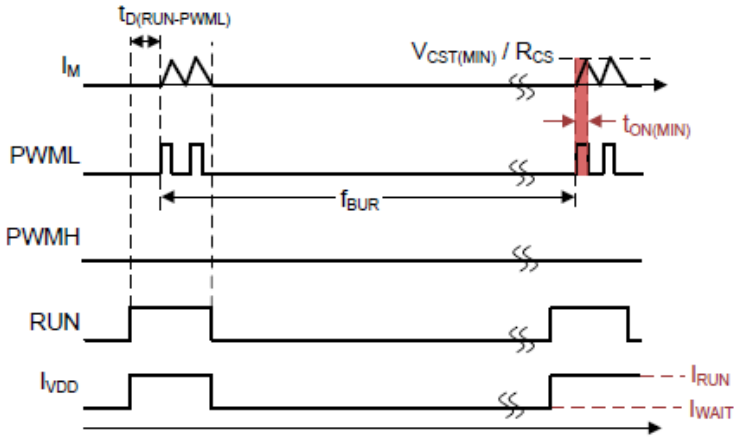


Figure 4.19: Switching pattern in SBP [21].

4.4.2 Additional component sizing

All the components required by the UCC28780 controller have been sized by referring to the design procedure illustrated in its datasheet[2]. These values have been computed based on the controller and power converter specifications. The component values of the controller circuit shown in Figure 4.20 are reported below.

- R_{BUR1} = 196 kΩ
- R_{BUR2} = 63.4 kΩ
- C_{BUR} = 180 pF
- C_{REF} = 0.1 µF
- C_{VDD} = 44 µF
- D_{AUX} → Super-Fast rectifier 600 V, 1 A
- R_{HVG} = 1 MΩ
- C_{HVG} = 2.2 nF
- D_{HVG} → Zener diode 22 V, 5 mA
- R_{SWS} = 121 Ω
- C_{SWS} = 22 pF
- Q_S → Depletion mode MOSFET 600 V, 21 mA
- D_{SWS} → Diode TVS 18 V
- R_{RTZ} = 91 kΩ
- R_{RDM} = 10 kΩ
- R_{VS1} = 36.5 kΩ
- R_{VS2} = 11 kΩ
- R_{OPP} = 820 Ω

[2] https://www.ti.com/lit/gpn/ucc28780

- C_{CS} = 24 pF
- C_{BULK} = 0.3 µF
- R_{BLEED} = 300 kΩ

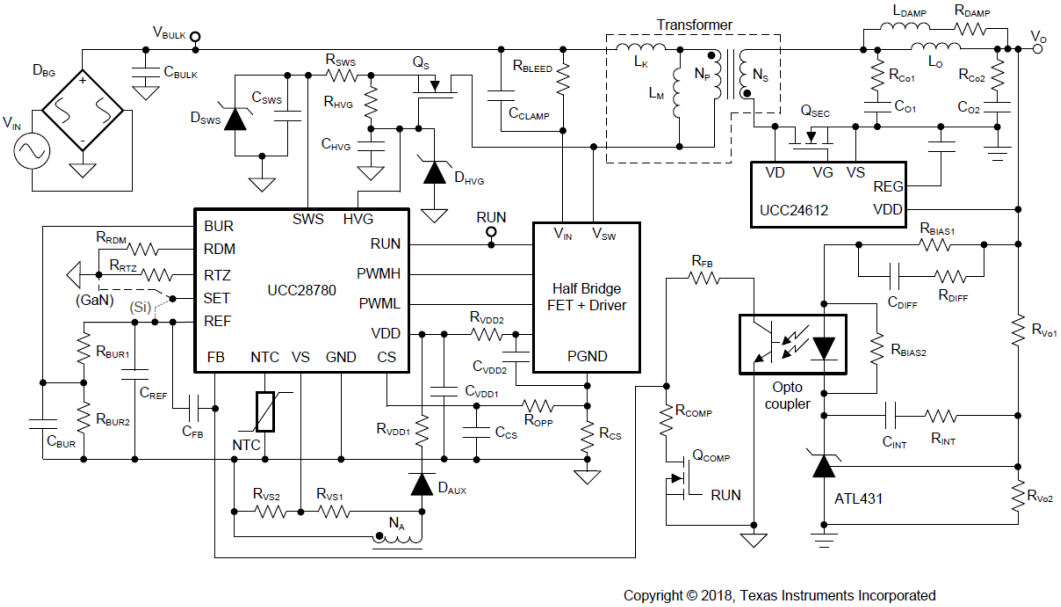


Figure 4.20: UCC28780 controller circuit [21].

More precisely, R_{RTZ} is the resistor connected to the RTZ pin that programs the delay between the PWMH falling edge and PWML rising edge [21]. R_{RDM} is the resistor connected to the RDM pin that programs the on-time of the high side switch to achieve ZVS on the low side switch [21].
Then, the value of the current sense resistor R_{CS} can be computed by:

$$R_{CS} = \frac{V_{CST(MAX)}}{I_{QL(MAX)}} = \frac{0.8\ V}{4.2\ A} = 190\ m\Omega. \tag{4.16}$$

The chosen normalized value of the current sense resistor according to the E12 series is R_{CS} = 180 mΩ.

4.4.3 Compensation network

The compensation network, shown in Figure 4.21 and Figure 4.22, consists of the Active Ripple Compensation (ARC) network, the Passive Ripple Compensation (PRC) network and the Regulator.

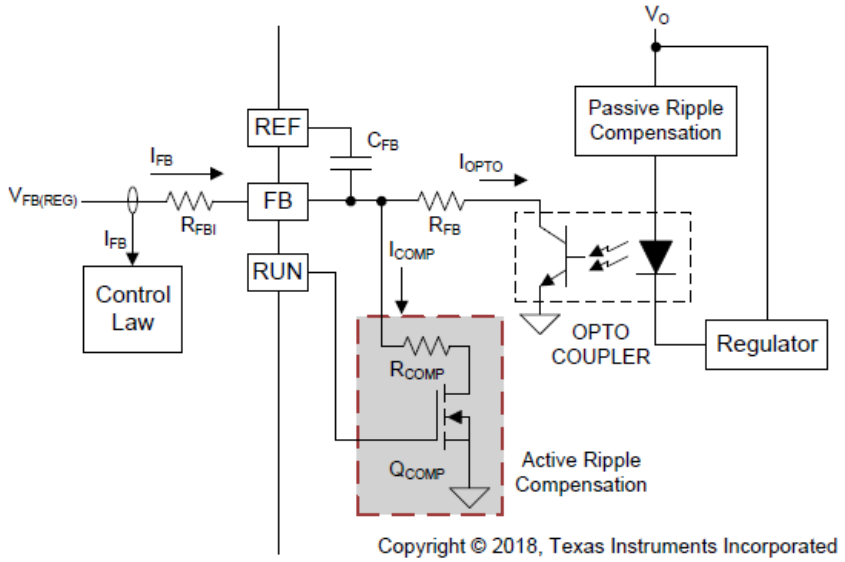


Figure 4.21: Compensation network with the ARC implementation[21].

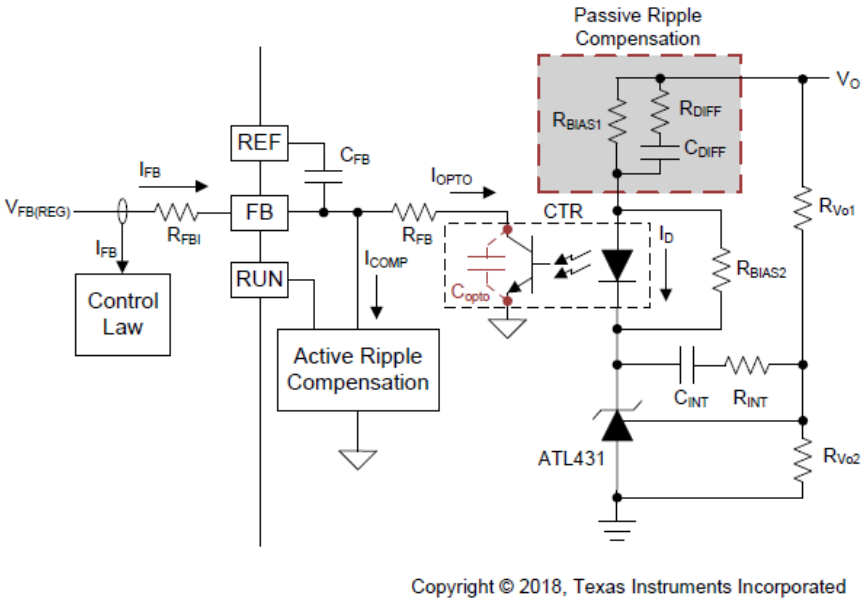


Figure 4.22: Compensation network with the PRC and Regulator implementation[21].

As previously mentioned, the advantage of the AHFB converter using an output capacitance with a low-ESR is to minimize the output voltage ripple. However, the burst ripple content is also reduced and hence this ripple interferes with the feedback current I_{FB} bringing it very close to the threshold value $I_{TH(FB)}$, which activates the next burst pulse at a wrong time [21].

This problem can be solved by implementing the Active Ripple Compensation, it generates burst ripple to stabilize the ABM operating mode of the AHFB converter which uses a low-ESR output capacitance. The ARC network consists of a high impedance resistor R_{COMP} in series with a small signal enhancement MOSFET Q_{COMP}, the gate of Q_{COMP} is controlled by the RUN pin of the controller. The resistor R_{COMP} is connected to the FB pin and it creates a compensation current. Then, when the RUN pin turns off Q_{COMP}, the resistor R_{COMP} and the output capacitance of Q_{COMP} slowly decrease the compensation current. Finally, the current coming from the optocoupler added to the compensation current becomes the feedback current which is compared with the threshold value [21]. This concept can be observed in Figure 4.23.

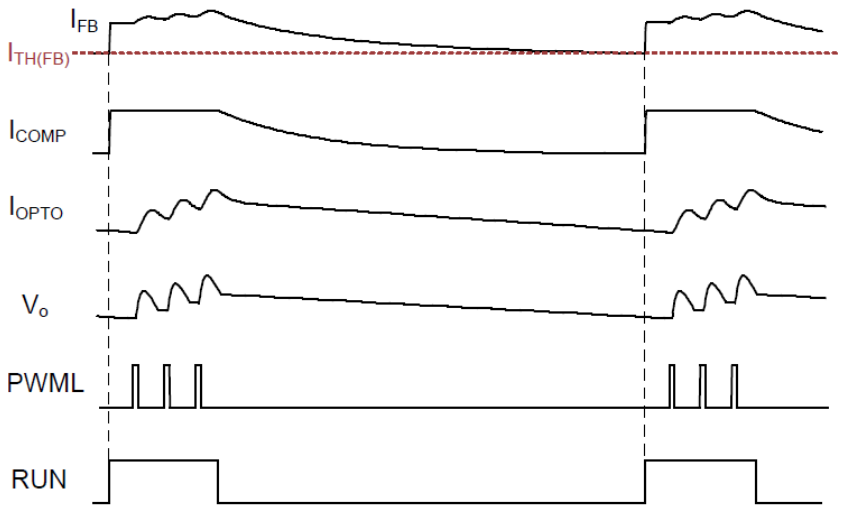


Figure 4.23: Active Ripple Compensation waveforms [21].

The typical behaviour of a stable ABM operation is shown in Figure 4.24, while that of an unstable ABM operation is shown in Figure 4.25. In the latter case, two burst packets are close to each other and the pulse count of the two packets is different.

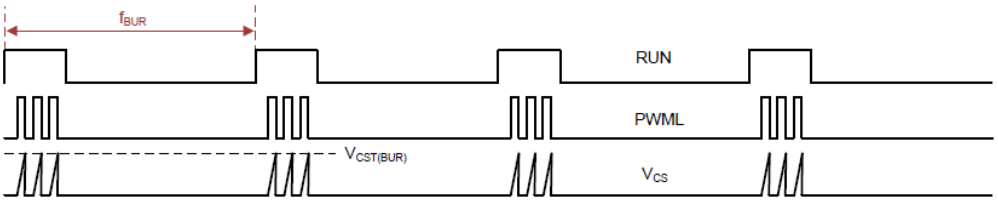


Figure 4.24: Typical behaviour of a stable ABM operation [21].

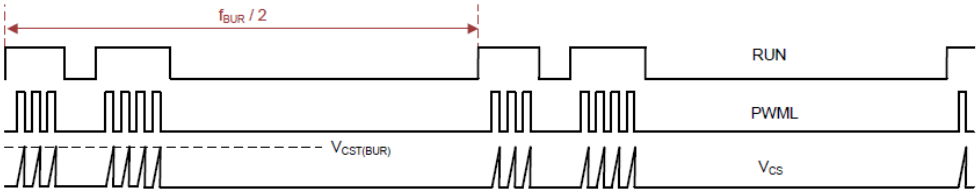


Figure 4.25: Typical behaviour of an unstable ABM operation [21].

From the datasheet of the UCC28780 controller, R_{COMP} = 1 MΩ and C_{FB} = 100 pF are recommended. The maximum value of feedback resistor R_{FB} is computed as follows:

$$R_{FB(MAX)} = \frac{V_{FB(REG)} - V_{CE(opto)}}{I_{FB(SBP)}} - R_{FBI} = 28\ k\Omega \qquad (4.17)$$

where $V_{FB(REG)}$, $I_{FB(REG)}$ and R_{FBI} can be found in the datasheet of the controller, while $V_{CE\ (opto)}$ in the datasheet of the optocoupler. Therefore, R_{FB} = 22.1 kΩ has been chosen. The ABM operating mode is a ripple-based control method, therefore the linear control theory cannot be applied.

A strong phase-delay can be present between the feedback current and the output voltage which generates a slope distortion around the intersection point between I_{FB} and $I_{TH(FB)}$. The purpose of this control is to ensure that the burst ripple content of feedback current I_{FB} is in-phase with the burst ripple output voltage [21]. To minimize the phase delay, a Passive Ripple Compensation network is implemented based on the transfer function from the feedback current I_{FB} to the output voltage V_o:

$$\frac{I_{FB}(s)}{V_o(s)} = \frac{CTR}{R_{BIAS1}} \cdot \frac{1 + \left({}^{s}/_{\omega_{z0}}\right)}{\left({}^{s}/_{\omega_{z0}}\right)} \cdot \frac{1}{1 + \left({}^{s}/_{\omega_{p1}}\right)} \cdot \frac{1 + \left({}^{s}/_{\omega_{z1}}\right)}{1 + \left({}^{s}/_{\omega_{OPTO}}\right)} \cdot \frac{1}{1 + \left({}^{s}/_{\omega_{FB}}\right)} \cdot \qquad (4.18)$$

The PRC network consists of an RC network composed by R_{DIFF} and C_{DIFF} in a parallel combination with the resistor R_{BIAS1}, this is needed to compensate the phase delay introduced by the optocoupler.

The poles and the zeros of the transfer function in the Equation (4.18) are the following:

$$\omega_{z0} = \frac{1}{(R_{vo1} + R_{INT})C_{INT}} \qquad (4.19)$$

$$\omega_{z1} = \frac{1}{(R_{DIFF} + R_{BIAS1})C_{DIFF}} \qquad (4.20)$$

$$\omega_{p1} = \frac{1}{R_{DIFF} C_{DIFF}} \tag{4.21}$$

$$\omega_{OPTO} = \frac{1}{(R_{FB} + R_{FBI}) C_{OPTO}} \tag{4.22}$$

$$\omega_{FB} = \frac{1}{(R_{FB} \,//\, R_{FBI}) C_{FB}} \tag{4.23}$$

The resistance R_{BIAS1} can be computed considering the current transfer ratio (CTR) of the optocoupler, the output voltage ripple ΔV_o and feedback current ripple ΔI_{FB}. The CTR is equal to 120% and it is given by the optocoupler datasheet, while $\Delta I_{FB} = 10$ µA can be found in the controller datasheet. Therefore, R_{BIAS1} is given by:

$$R_{BIAS1} = \frac{CTR}{\Delta I_{FB}} \Delta V_o = \frac{120\%}{10\,\mu}\, 0.1V = 12\ k\Omega\,. \tag{4.24}$$

The capacitance C_{DIFF} is computed considering ω_{z1} almost equal to ω_{OPTO} and placing ω_{p1} at least to $4\pi f_{BUR(UP)}$ as follows:

$$\begin{aligned} C_{DIFF} &= \frac{1}{R_{BIAS1}} \frac{\omega_{p1} - \omega_{z1}}{\omega_{p1} \times \omega_{z1}} = \\ &= \frac{1}{R_{BIAS1}} \frac{4\pi f_{BUR(UP)} - \omega_{OPTO}}{4\pi f_{BUR(UP)} \times \omega_{OPTO}} = 4.7\ nF \end{aligned} \tag{4.25}$$

where $f_{BUR(UP)}$ is derived from the controller datasheet and it is equal to 34 kHz, while ω_{OPTO} = 17x10^3 rad/s is computed following Equation (4.22) with C_{opto} = 2.2 nF. Finally, C_{DIFF} = 4.7 nF has been chosen.
The resistance R_{DIFF} is computed starting from the Equation (4.21) and considering ω_{p1} equal to $4\pi f_{BUR(UP)}$ as follows:

$$R_{DIFF} = \frac{1}{\omega_{p1} C_{DIFF}} = \frac{1}{4\pi f_{BUR(UP)} C_{DIFF}} = 498\ \Omega. \tag{4.26}$$

Then, R_{vo1} and R_{vo2} are used to provide the reference voltage V_{ref} = 2.5 V of the shunt regulator ATL431.
Since the output voltage V_o must be equal to 19.5 V, R_{vo1} and R_{vo2} have been chosen equal to 150 kΩ and 22.1 kΩ respectively to provide a reference voltage of 2.5V as shown below:

$$V_{ref} = V_o \frac{R_{vo2}}{R_{vo2} + R_{vo1}} = 19.5V \frac{22.1\ k\Omega}{22.1\ k\Omega + 150\ k\Omega} = 2.5\ V. \quad (4.27)$$

The resistor R_{BIAS2} provides the bias current for the shunt regulator ATL431. From its datasheet, a bias current equal to 35 μA is recommended.
The typical forward voltage of the diode of the FODM8801AV optocoupler is V_F = 1.35 V, so R_{BIAS2} is given by:

$$R_{BIAS2} = \frac{V_F}{I_{bias(ATL431)}} = \frac{1.35\ V}{35\ \mu A} = 38\ k\Omega. \quad (4.28)$$

The chosen value of the resistor R_{BIAS2} is 34 kΩ.
The previously mentioned FODM8801AV optocoupler and ATL431 shunt regulator are those recommended from the UCC28780 controller datasheet and from the users 'guide of the evaluation board[3] UCC28780EVM-002 provided by the Texas Instruments.
The values of the other components of the regulator, R_{INT} and C_{INT}, have been computed following a reverse engineering procedure starting from the evaluation board circuit. These two components, as explained in the UCC28780 datasheet, are needed to solve the problem of the slow large-signal response of the ATL431 shunt regulator [21].
First, the crossover frequency f_{c_ev} related to the circuit of the evaluation board has been obtained. Its simulations results show a switching frequency of 300 kHz, so the crossover frequency f_{c_ev} is obtained as follows:

$$f_{c\_ev} = \frac{300\ kHz}{8} = 37.5\ kHz \rightarrow\ \omega_{c\_ev} \cong 236\ \times 10^3\ {}^{rad}/_{s}. \quad (4.29)$$

The frequency of the ω_{zo} zero reported in the Equation (4.19) is computed considering the R_{INT} and C_{INT} values of the evaluation board to identify its position. Also, it must be much lower than the crossover frequency. Finally, ω_{zo} = 475 rad/s has been obtained, that is lower than the crossover frequency.
In this thesis work, instead, the switching frequency is equal to 1 MHz and the crossover frequency f_c is given by:

$$f_c = \frac{1\ MHz}{8} = 125\ kHz \rightarrow\ \omega_c \cong 785\ \times 10^3\ {}^{rad}/_{s}. \quad (4.30)$$

Also in this case, the frequency of the ω_{zo} zero is much lower than the crossover frequency. Therefore, R_{INT} = 60.4 kΩ and C_{INT} = 10 nF have been chosen as in the evaluation board.

[3] https://www.ti.com/lit/pdf/sluubo8

Furthermore, the ω_{z1} zero must be close to the ω_{OPTO} pole and the ω_{p1} pole must be higher than the crossover frequency. To meet these requirements, the resistance R_{DIFF} has been reduced from 498 Ω to 220 Ω.
Finally, the frequencies of the transfer function poles and zero are the following:

- ω_{zo} = 475 rad/s,
- ω_{opto} = 17 x 10^3 rad/s,
- ω_{z1} = 17.4 x 10^3 rad/s,
- ω_{p1} = 964 x 10^3 rad/s,
- ω_{fb} = 1.7 x 10^6 rad/s.

Chapter 5

PCB design

A practical implementation of the complete circuit consisting of the input stage, the AHBF converter, the gate drivers and the control circuit shown in Figure 5.1 is presented in this chapter.

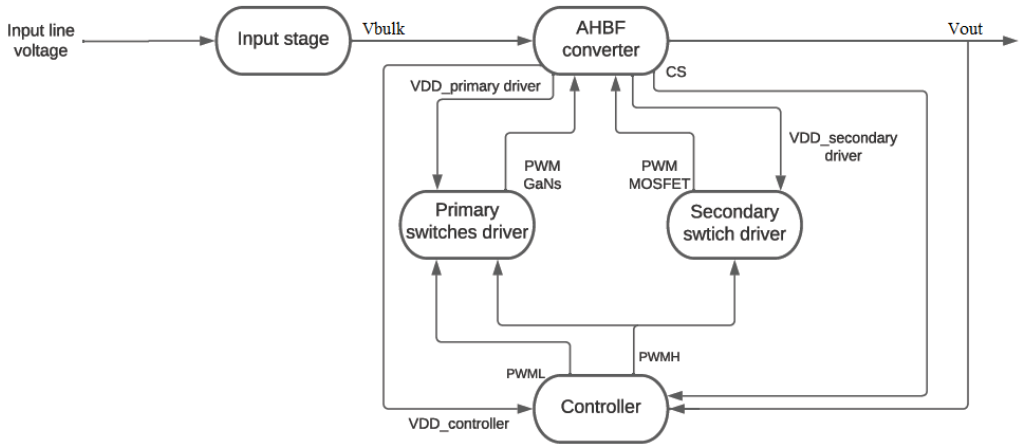


Figure 5.1: Block diagram of the AHBF converter.

More precisely, the AHBF converter block and the controller block have been described in detail in Chapter 3 and Chapter 4 respectively. Therefore, this chapter focuses on the input stage block and on the gate driver blocks.
The gate driver for the primary side switches and the one for the secondary side switch have been selected and properly connected.
Subsequently, after completing the description of the blocks constituting the circuit, the PCB has been designed by using the Altium Designer software, starting from the implementation of the schematic up to the realization of the layout.

5.1 Input stage

The input stage of the circuit has been implemented with reference to the evaluation board[4] UCC28780EVM-002. A simplified schematic of the input stage is shown in Figure 5.2.

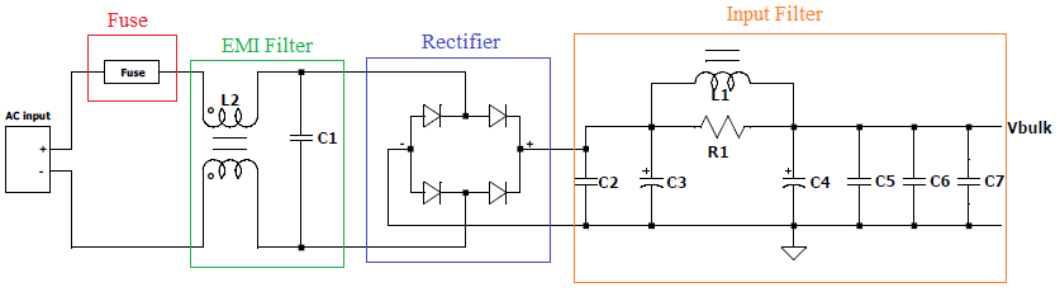


Figure 5.2: Simplified schematic of the input stage of the AHBF converter.

A fuse connected to the input connector is required to protect the power supply stage of the device from over currents. It consists of a fuse element, such as an electric wire properly dimensioned to melt when the current flowing through it exceeds a certain value thus interrupting the power supply. The 39213150000 TE5 Fuse from Littlefuse has been chosen, it is characterized by a voltage rating equal to 250 V and a current rating equal to 3.15 A.

The fuse is followed by an EMI filter. The latter is needed to reduce the electromagnetic noise by suppressing the unwanted high frequencies. Being positioned close to the power supply network, it prevents disturbances from affecting the device and creating malfunctions. Furthermore, the EMI filter prevents the noise generated by the operation of the device from disturbing the power supply network and interfering with other devices [22]. The 744821201 common mode filter line and the 890324022017CS capacitor with a value equal to 68 nF from Wurth Elektronik have been chosen.

Then, a full wave rectifier realized with four diodes in the Graetz bridge configuration has been added to produce a DC output from an AC input. The Z4DGP410L-HF bridge rectifier from Comchip Technology has been chosen, it is characterized by a peak reverse voltage equal to 1 kV and an average forward current equal to 4 A.

Finally, a filter at the input of the AHBF converter stage has been implemented with the following components:

[4] https://www.ti.com/lit/pdf/sluubo8

- C2 = 0.1 μF;
- C3 = C4 = 39 μF;
- C5 = C6 = C7 = 0.1 μF;
- R1 = 1 kΩ;
- L1 = 22 μH (7447462220 power inductor from Wurth Elektronik).

5.2 Selection of the gate drivers

Two different gate drivers are needed to drive the GaN HEMT devices in the half-bridge configuration in the primary side of the converter and the low side MOSFET device in the secondary side of the converter.
Gate drivers are chosen based on the current I_{DR} they must supply to the gate of the transistors to switch them from the off state to the on state and vice versa. The I_{DR} current is computed considering the total gate charge Q_g of the transistor and the desired switching turn-on/turn-off time t.
Focusing on the GaN HEMTs, the total gate charge Q_g is equal to 2.2 nC and, considering t equal to 10 ns, the required I_{DR_G} current is given by:

$$I_{DR\_G} = \frac{Q_g}{t} = \frac{2.2\ nC}{10\ ns} = 220\ mA\,. \tag{5.1}$$

To meet this constraint, the high-speed half-bridge driver for GaN power switches NCP51820 from Texas Instruments has been chosen. This device is characterized by a peak source current equal to 2 A and a peak sink current equal to 1 A, values compatible with the I_{DR_G} current computed in the Equation (5.1). Moreover, the NCP51820 gate driver is optimized for GaN devices with a V_{DS} voltage up to 650 V and to drive GaN power transistors in soft switching full-bridge and half-bridge configurations, LLC power converters, Active Clamp Flyback and Forward converters and synchronous rectifier topologies [23].
Now, focusing on the secondary side MOSFET, the total gate charge Q_g is equal to 40 nC and, considering t equal to 10 ns, the required I_{DR_M} current is given by:

$$I_{DR\_M} = \frac{Q_g}{t} = \frac{40\ nC}{10\ ns} = 4\ A\,. \tag{5.2}$$

Therefore, the single channel low-side gate driver UCC27614 from Texas Instruments has been chosen. This device is characterized by a peak source current equal to 10 A and a peak sink current equal to 10 A which respect the value of the I_{DR_M} current computed in the Equation (5.2).

5.2.1 GaN HEMTs gate driver configuration

A DC voltage is applied to the VDD pin of the NCP51820 gate driver to supply it, so a bypass capacitor C_{VDD} between the VDD pin and the GND pin is required. The bypass capacitor is needed to provide the gate charge for the high side and low side switches and it absorbs the reverse recovery charge of the bootstrap diode.
The NCP51820 datasheet recommends a bypass capacitance value greater than 100 nF, so $C_{VDD} = 1$ µF has been chosen.
Then, a bootstrap capacitor C_{BST} is needed to provide the gate charge for the high side switch and the reverse recovery charge of the bootstrap diode. The value of C_{BST} is computed as follows [24]:

$$C_{BST} > \frac{Q_{BS}}{V_{BS.drop}} \tag{5.3}$$

where $V_{BS,drop}$ is the maximum allowable voltage drop across the bootstrap capacitor given by:

$$V_{BS,drop} = V_{cc} - V_F - V_X - V_{BSUV+,MAX} = 1.9\,V \tag{5.4}$$

where:

- $V_{cc} = 12.7$ V is the supply voltage of the gate driver;
- $V_F = 1.7$ V is the bootstrap diode forward voltage drop;
- V_X is the transistor source voltage, it is computed as $V_X = R_{DSon,MAX} \cdot I_{DS,MAX} = 190\ m\Omega \cdot 11\ A = 2.09$ V;
- $V_{BSUV+,\,MAX} = 7$ V is the maximum UVLO positive voltage level of the gate driver.

Q_{BS} is the total amount of the charge supplied by the capacitor and it is computed as follows:

$$Q_{BS} = Q_g + Q_{rr} + Q_{LS} + \left(I_{LK,GS} + I_{LK,D} + I_{LK,LS} + I_{Q,LS}\right)t_{ON} \tag{5.5}$$

where:

- $Q_g = 2.2$ nC is the total gate charge;
- Q_{rr} is the reverse recovery charge of the bootstrap diode and it is negligible since the diode is an ultrafast type;
- Q_{LS} is the additional gate charge required by the internal level shifter, it is not provided by the datasheet hence 3 nC is a conservative value;
- $I_{LK,\,GS} = 57$ µA is the gate-to-source leakage current;
- $I_{LK,\,D} = 5$ µA is the diode leakage current;
- $I_{LK,\,LS} = 10$ µA is the level shifter leakage current;

- $I_{Q,\,LS}$ = 100 μA is the level shifter quiescent current;
- t_{ON} = 750 ns is the maximum on time of the high side transistor.

By using these values, Q_{BS} = 5.33 nC has been computed and the bootstrap capacitance C_{BST} must be higher than 2.8 nF. Therefore, C_{BST} = 0.1 μF has been chosen.
The NCP51820 gate driver requires a bootstrap diode with a series resistor lower than 10 Ω between VDD pin and VBST pin. The bootstrap diode D_{BST} must have a voltage rating higher than the input voltage V_{in}, low current, very low junction capacitance and it must be high speed [23]. To satisfy these requirements, the Ultrafast diode ES1J has been chosen as bootstrap diode and R_{BST} = 5.6 Ω.
The NCP51820 also includes linear regulators to provide a regulated signal to the high side and low side switches. To this purpose, two additional capacitors, C_{VDDH} and C_{VDDL}, are needed and they are computed as follows[23]:

$$C_{VDDH} < \frac{C_{BST}}{10} \rightarrow C_{VDDH} < 10\ nF \tag{5.6}$$

$$C_{VDDL} < \frac{C_{VDD}}{10} \rightarrow C_{VDDL} < 100\ nF. \tag{5.7}$$

Therefore, C_{VDDH} = 1 nF and C_{VDDL} = 10 nF have been chosen.
The other components, C_{en} = 10 nF, R_{en} = 1 kΩ and C_{DT} =100 nF are suggested by the NCP51820 datasheet[5].
The typical application schematic is shown in Figure 5.3.
The R_{DT} resistor which is in the circuit shown in Figure 5.3 is used to program the dead-time. However, in this case, the dead time is only programmed by the controller and therefore the R_{DT} resistor equal to 0 Ω has been chosen.
Then, gate resistors for both the high side and low side transistors can be used to modulate the switching times of the transistors and a value of 2.2 Ω has been chosen. Finally, a resistance equal to 10 kΩ is connected between the gate and the source of both transistors.

[5] https://www.onsemi.com/pdf/datasheet/ncp51820-d.pdf

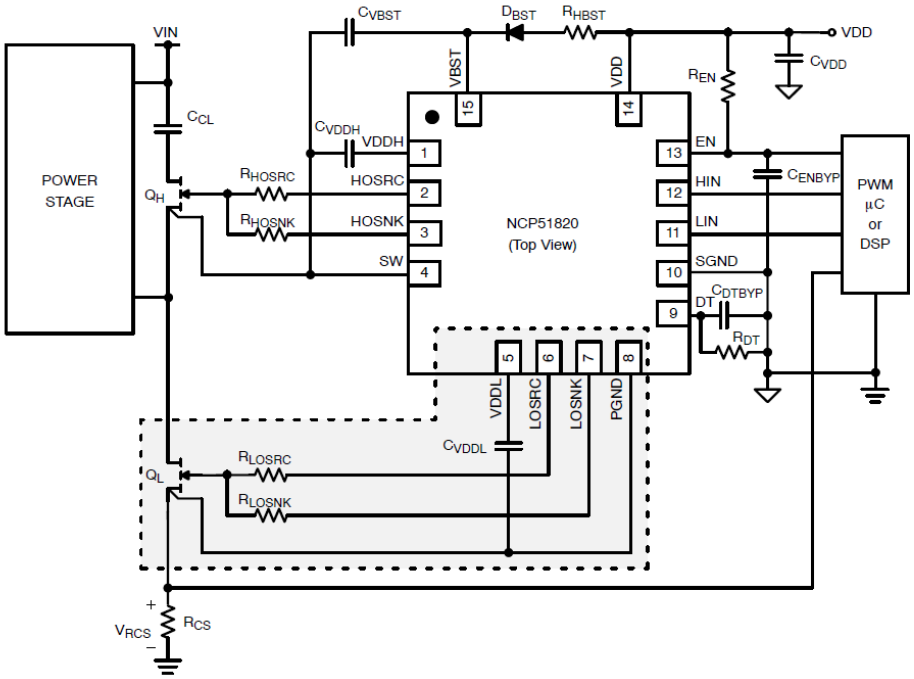


Figure 5.3: NCP51820 typical application [23].

5.2.2 MOSFET gate driver configuration

A typical application schematic of the UCC27614 gate driver is shown in Figure 5.4. The driver bias supply VDD is connected to a fast-switching diode 1N4148W-7-F and a series resistance of 10 Ω which is in turn connected to a voltage source, as done in the evaluation board UCC28780EVM-002.

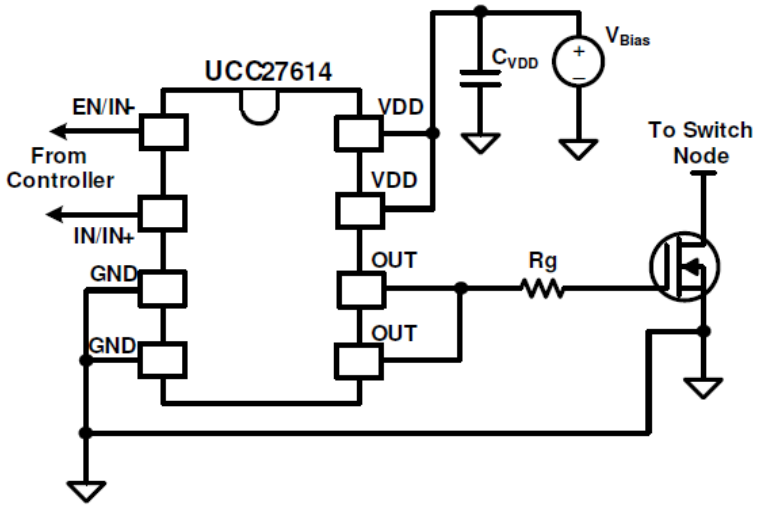


Figure 5.4: UCC27614 typical application [25].

The UCC27614 datasheet[6] recommends bypassing the VDD pin with two C_{VDD} ceramic capacitors greater than or equal to 0.1 µF and 1 µF, which are connected between the VDD pin and the GND pin of the device. Therefore, C_{VDD1} = 0.1 µF and C_{VDD2} = 10 µF have been chosen.
Finally, the gate resistor R_G = 2.2 Ω is added to modulate the switching times of the transistor.

5.3 Controller and Gate Drivers power supply

The controller and the gate drivers are opportunely powered by exploiting the voltages provided by the transformer. For this purpose, two auxiliary windings are added to the transformer, one on the primary side and one on the secondary side as shown in Figure 5.5. The two auxiliary winding are necessary to obtain lower voltages across them with respect to the voltages across the main windings, which are suitable for powering the devices.
In this Chapter, the characteristic values of the transformer manufactured by Italtras will be considered.

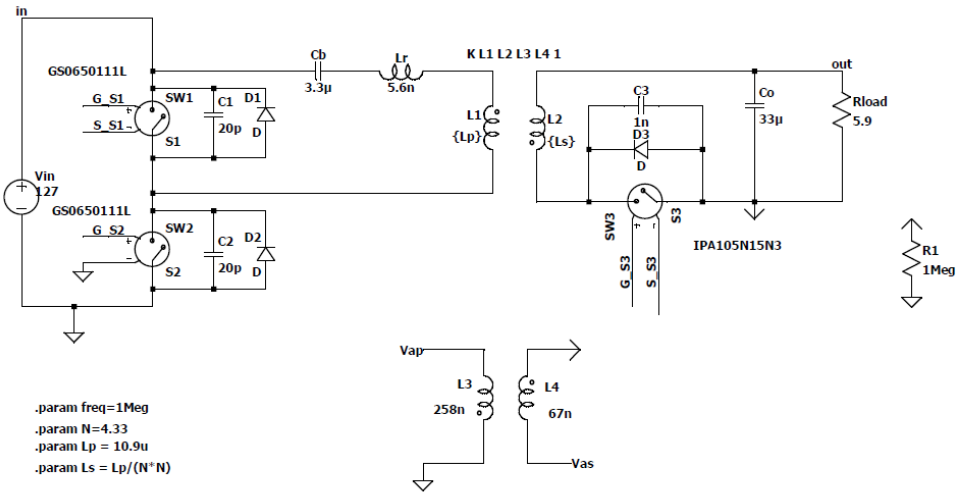


Figure 5.5: AHBF converter with the auxiliary windings of the transformer.

The voltage across the primary winding *L1*, when the *S1* switch is on, is equal to $-nV_o$ = -84 V, where *n* is the primary to secondary turns ratio equal to 4.33 and V_o is the

[6] https://www.ti.com/lit/gpn/ucc27614

output voltage equal to 19.5 V. Instead, the voltage across the *L2*, when the *S3* switch is on, is equal to $-V_o = -19.5$ V. With a primary to primary-auxiliary turns ratio n_{p_ap} equal to 6.5 and a secondary to secondary-auxiliary turns ratio n_{s_as} equal to 3, the voltage V_{ap} across the primary auxiliary winding *L3* is equal to 13 V and the voltage V_{as} across the secondary auxiliary winding *L4* is equal to 6.5 V.
Moreover, the values of the winding inductances are computed as follows:

$$L_s = \frac{L_p}{n^2} = \frac{10.9\ \mu H}{(4.33)^2} = 0.6\ \mu H \tag{5.8}$$

$$L_{ap} = \frac{L_p}{n_{p\_ap}^2} = \frac{10.9\ \mu H}{(6.5)^2} = 258\ nH \tag{5.9}$$

$$L_{as} = \frac{L_s}{n_{p\_ap}^2} = \frac{0.6\ \mu H}{(3)^2} = 67\ nH \tag{5.10}$$

where $L_p = L_m = 10.9$ µH is the magnetizing inductance.
Table 5.1 and Table 5.2 summarize the voltage values across the transformer windings for both the minimum input voltage and the maximum input voltage respectively.

	$V_{in} = 127$ V			
	V_p	V_{ap}	V_s	V_{as}
S2 ON *S1, S3 OFF*	$V_{in} - nV_o =$ 42.6 V	$-V_p/n_{p\_ap} =$ - 6.5 V	$V_{in}/n - V_o =$ 9.8 V	$-V_s/n_{s\_as} =$ - 3.3 V
S2 OFF *S1, S3 ON*	$- nV_o = -$ 84 V	$-V_p/n_{p\_ap} =$ 13 V	$-V_o = -$ 19.5 V	$-V_s/n_{s\_as} =$ 6.5 V

Table 5.1: Voltage values across the transformer windings for $V_{in} = 127$V.

	$V_{in} = 354$ V			
	V_p	V_{ap}	V_s	V_{as}
S2 ON *S1, S3 OFF*	$V_{in} - nV_o =$ 269 V	$-V_p/n_{p\_ap} =$ - 41 V	$V_{in}/n - V_o =$ 62 V	$-V_s/n_{s\_as} =$ - 20.7 V
S2 OFF *S1, S3 ON*	$- nV_o =$ - 84 V	$-V_p/n_{p\_ap} =$ 13 V	$-V_o =$ - 19.5 V	$-V_s/n_{s\_as} =$ 6.5 V

Table 5.2: Voltage values across the transformer windings for $V_{in} = 354$ V.

To verify this theoretical analysis, LTspice simulations have been performed. The results, shown in Figure 5.6 and Figure 5.7, confirm the values computed in the previous tables.

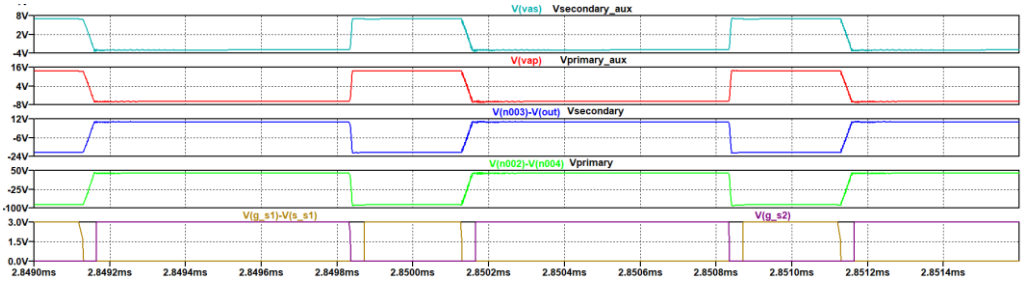


Figure 5.6: Transformer voltages with V_{in} = 127 V.

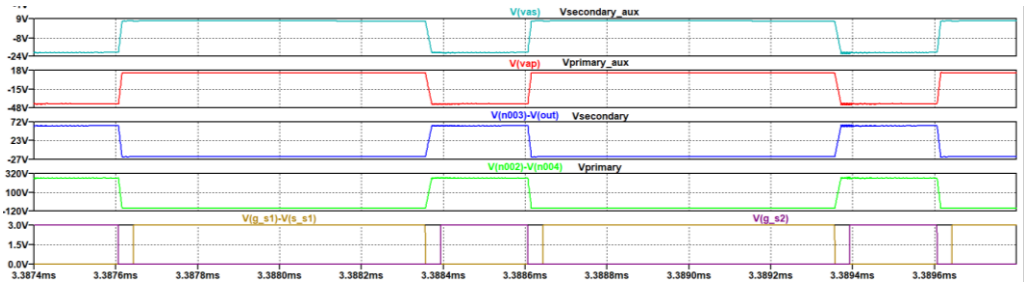


Figure 5.7: Transformer voltages with V_{in} = 354 V.

The UCC28780 controller requires a power supply voltage between 12 V and 34 V, therefore the voltage across the primary auxiliary winding may be the right one to power it. However, the controller must be always powered and hence the V_{ap} voltage must be rectified. The same rectified voltage is also used to power the GaN HEMTs gate driver NCP51820 which requires a power supply voltage between 9 V and 17 V. The V_{ap} voltage is rectified following the circuit of the evaluation board UCC28780EVM-002, by using the super-fast rectifier CSFMT108-HF in series with a resistance equal to 2.49 Ω. The rectified primary auxiliary voltage V_{pri_bias} is equal to 12.7 V, which is suitable for supplying the controller and gate driver of the GaN switches.

The controller provides the control signals for the GaN switches gate driver and for the MOSFET gate driver and, since it is located on the primary side of the converter, an isolator is needed to send the control signal to the secondary side of the converter. The ISO7710 isolator has been chosen and its schematic is shown in Figure 5.8. The latter requires two power supply voltages and it is referred to two different grounds. For what concerns the grounds, GND1 is connected to the primary side ground while

GND2 is connected to the secondary side ground. Considering the power supply voltages, the ISO7710 isolator requires voltage values between 2.25 V and 5.5 V.

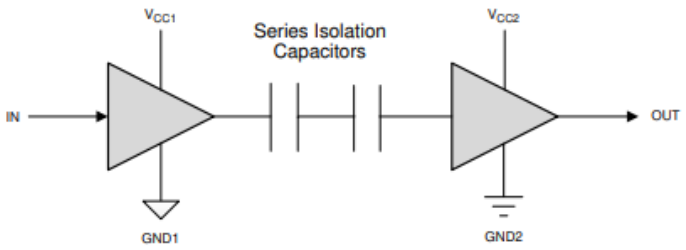


Figure 5.8: ISO7710 isolator schematic [26].

Focusing on the primary side of the isolator, a voltage divider is implemented to get a suitable power supply voltage value. The V_{CCp} voltage is obtained as follows:

$$V_{ccp} = V_{pri\_bias}\frac{R_6}{R_6 + R_5} = 12.7\ V\ \frac{1\ k\Omega}{1\ k\Omega + 1.5\ k\Omega} = 5\ V. \tag{5.11}$$

The same reasoning is followed to obtain the V_{CCs} voltage for the secondary side of the isolator:

$$V_{ccs} = V_{sec\_bias}\frac{R_4}{R_4 + R_3} = 6.15\ V\ \frac{1\ k\Omega}{1\ k\Omega + 1\ k\Omega} = 3\ V. \tag{5.12}$$

where V_{sec_bias} is the rectified secondary auxiliary voltage.
The V_{CCp} and the V_{CCs} voltages are connected to the VCC1 pin and VCC2 pin of the isolator respectively. The OUT pin of the isolator is then connected to the input pin of the UCC27614 gate driver.
As done for the primary auxiliary voltage, the secondary auxiliary voltage V_{as} is also rectified by using a fast-switching diode 1N4148W-7-F and a series resistance of 10 Ω as already explained in Section 5.1.2. The rectified secondary auxiliary voltage V_{sec_bias} is equal to 6.15 V and it is used to power the UCC27614 gate driver which requires a power supply voltage between 4.5 V and 26 V.
A complete schematic of the circuit described in this section is shown in Figure 5.9.
The bypass capacitors C_6 and C_7 with a value equal to 0.1 μF connected to the supply pins are recommended by the ISO7710 datasheet [7].

[7] https://www.ti.com/lit/gpn/iso7710

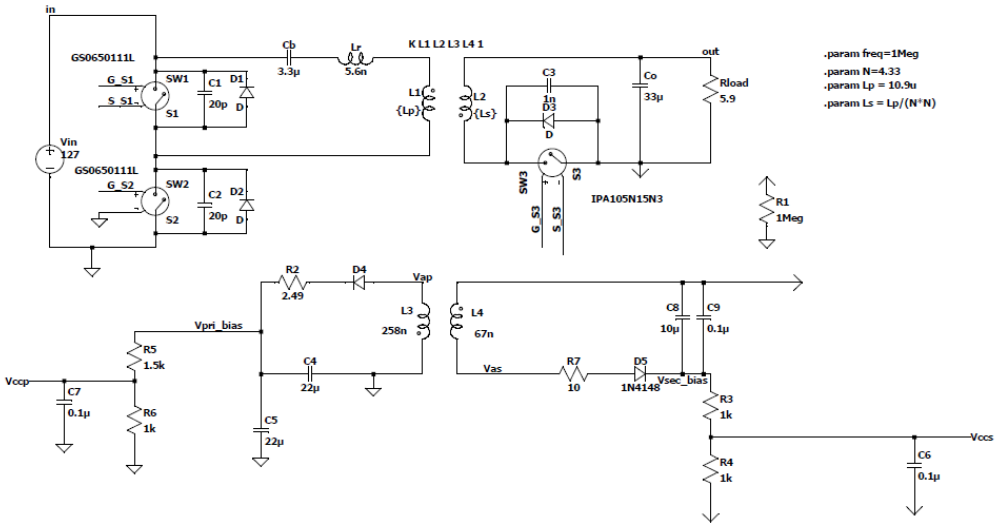


Figure 5.9: AHBF converter with power supply voltages.

Summarizing, the power supply voltage levels required by the devices are reported in Table 5.3 and the voltage values obtained to power the devices are reported in Table 5.4.

		Absolute maximum ratings	*Recommended operating conditions*
Controller	UCC28780	V_{DDmin} = 0 V V_{DDmax} = 38 V	V_{DDmin} = 12 V V_{DDmax} = 34 V
GaN HEMTs gate driver	NCP51820	V_{DDmin} = - 0.3 V V_{DDmax} = 20 V	V_{DDmin} = 9 V V_{DDmax} = 17 V
MOSFET gate driver	UCC27614	V_{DDmin} = - 0.3 V V_{DDmax} = 30 V	V_{DDmin} = 4.5 V V_{DDmax} = 26 V
Isolator	ISO7710	$V_{cc,min}$ = - 0.5 V $V_{cc,max}$ = 6 V	$V_{cc,min}$ = 2.25 V $V_{cc,max}$ = 5.5 V

Table 5.3: Device power supply voltage levels.

Voltage	*Value*	*Powered device*
$V_{pri\ bias}$	12.7 V	Controller and GaN HEMTs gate driver
$V_{sec\ bias}$	6.15 V	MOSFET gate driver
V_{ccp}	5 V	Isolator primary side
V_{ccs}	3 V	Isolator secondary side

Table 5.4: Powered devices.

Finally, to verify the behavior of the circuit shown in Figure 5.9 and the computed voltage values, LTspice simulations have been performed.
Figure 5.10 and ùFigure 5.12 show the rectified primary and secondary auxiliary voltages and the power supply voltages for the isolator with V_{in} = 127 V and V_{in} = 354 V respectively. The respective zooms are shown in Figure 5.11 and Figure 5.13. From these latter results, it is possible to notice how these voltages do not depend on the input voltage V_{in}.

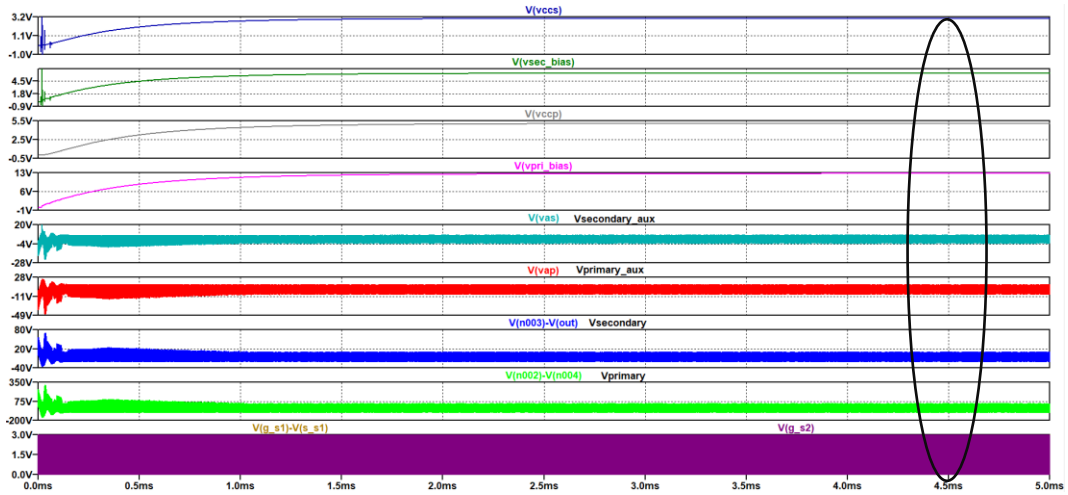


Figure 5.10: Transformer and rectified voltages with V_{in} = 127 V.

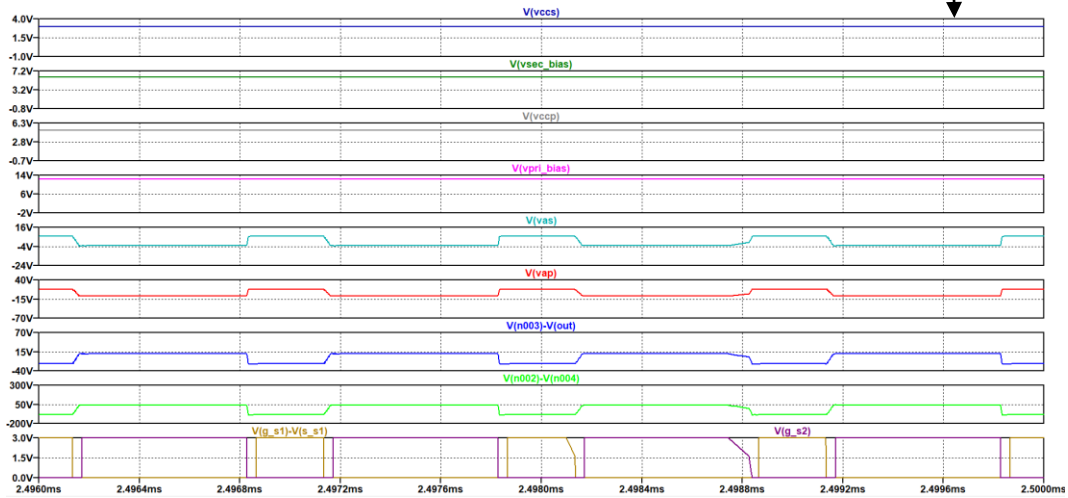
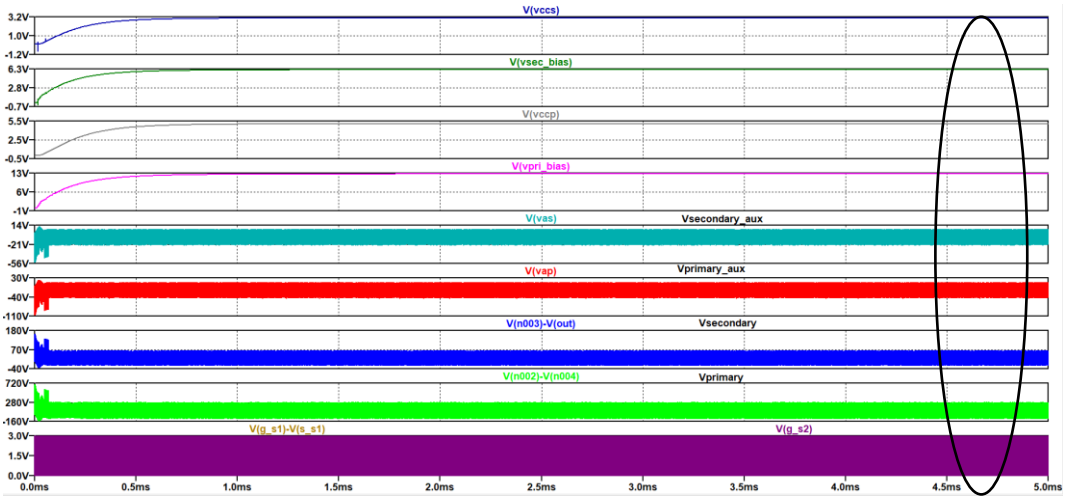


Figure 5.11: Zoom of the rectified voltages with V_{in} = 127 V.



ùFigure 5.12: Transformer and rectified voltages with V_{in} = 354 V.

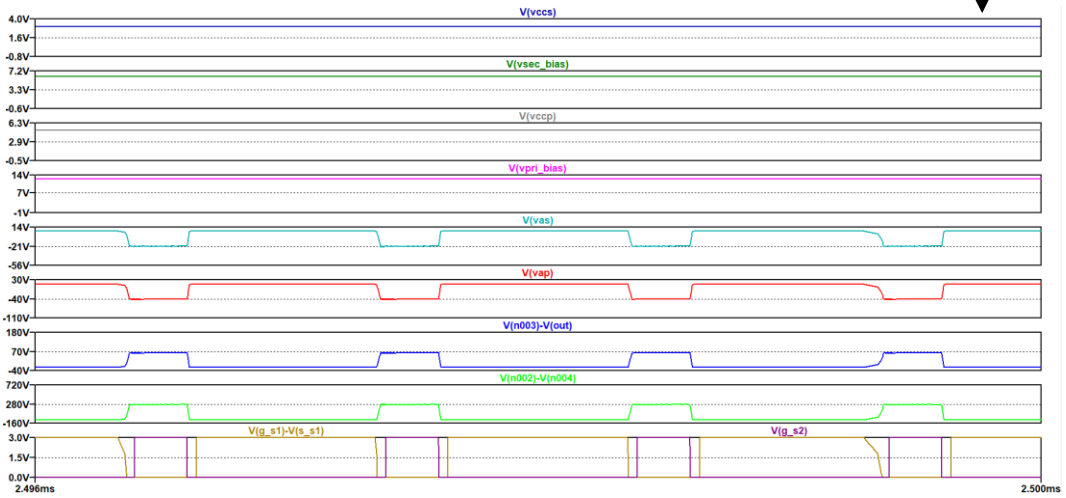


Figure 5.13: Zoom of the rectified voltages with V_{in} = 354 V.

5.4 PCB schematic and layout

The schematic and the layout of the PCB prototype has been designed by using Altium Designer software.
Table 5.5 shows the main components of the Bill of Material (BOM) provided by Altium, i.e., those of the AHBF converter stage, the gate drivers and the controller.

Component	*Manufacturer number*	*Manufacturer*
Half-bridge GaN HEMTs	GS-065-011-1-L	GaN Systems
Synchronous rectifier MOSFET	IPA105N15N3-G	Infineon
Resonant capacitor C_r	C1825C105K2RACTU	KEMET
Output capacitor C_o (x3)	C2012X5R1E106K125AB	TDK
Dip capacitor C_d	12062A681KAT2A	Kyocera AVX
Half-bridge gate driver	NCP51820AMNTWG	ON Semiconductor
MOSFET gate driver	UCC27614DSGR	Texas Instruments
Controller	UCC28780RTER	Texas Instruments

Table 5.5: AHBF converter, gate drivers and controller components of the BOM.

5.4.1 Schematics

The schematic of the PCB is divided into three sheets:

- the first sheet, shown in Figure 5.14, represents the input stage, the AHBF converter stage and the control circuit stage;
- the second sheet, shown in Figure 5.15, represents the half-bridge GaN HEMTs and the half-bridge gate driver configuration;
- the third sheet, shown in Figure 5.16, represents both the MOSFET gate driver and the isolator configurations.

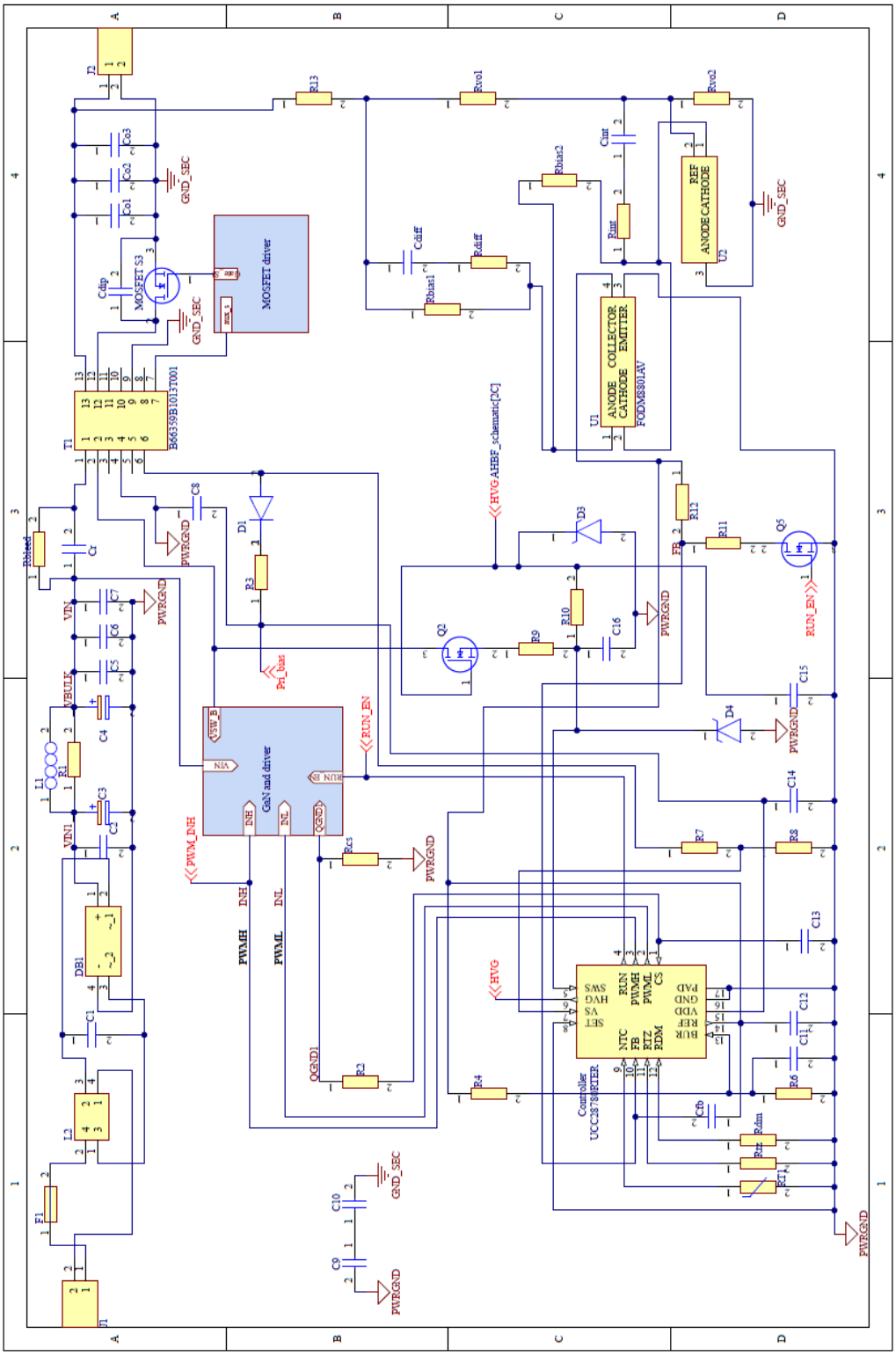


Figure 5.14: Sheet 1 of the PCB schematic.

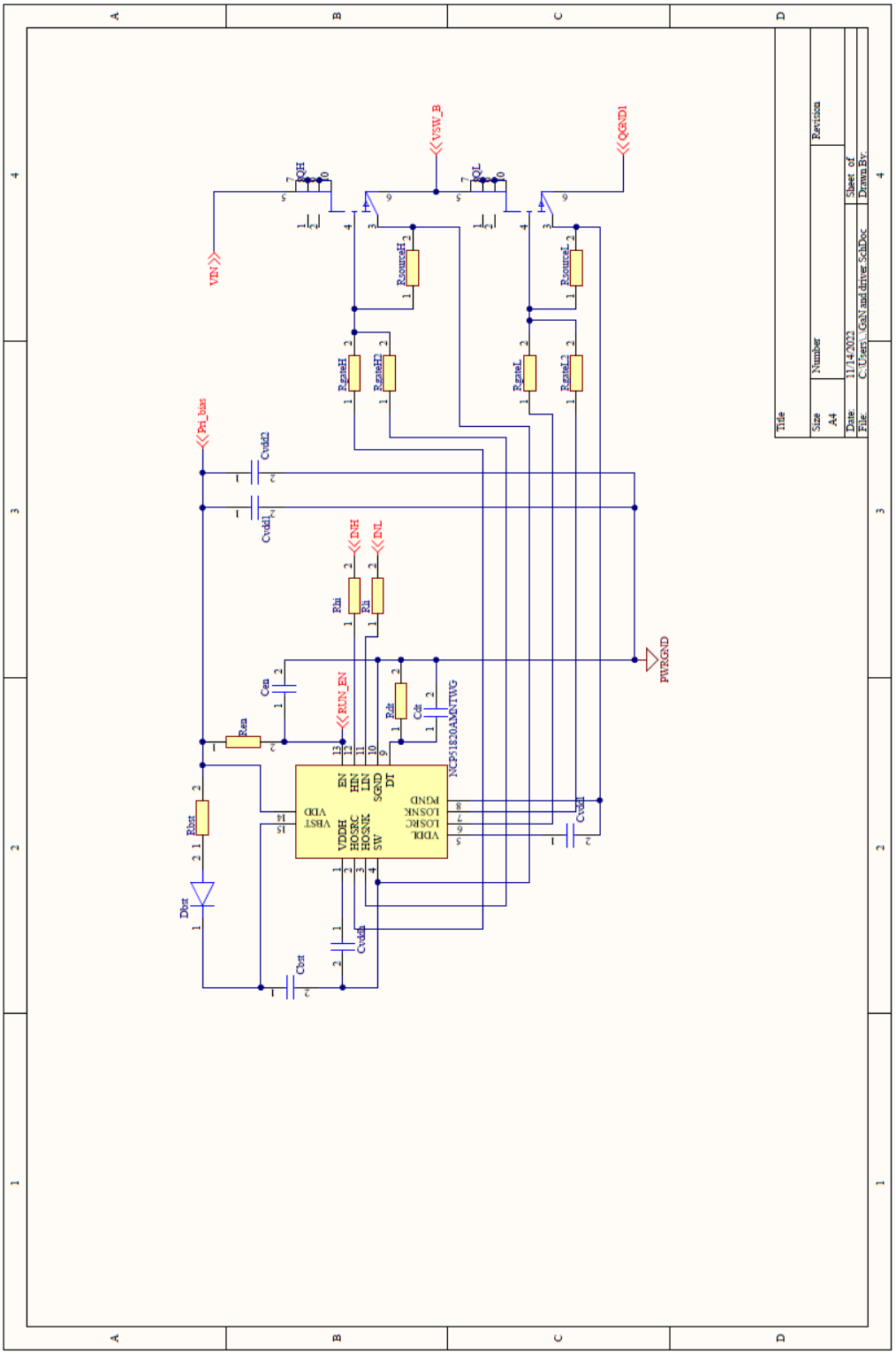


Figure 5.15: Sheet 2 of the PCB schematic.

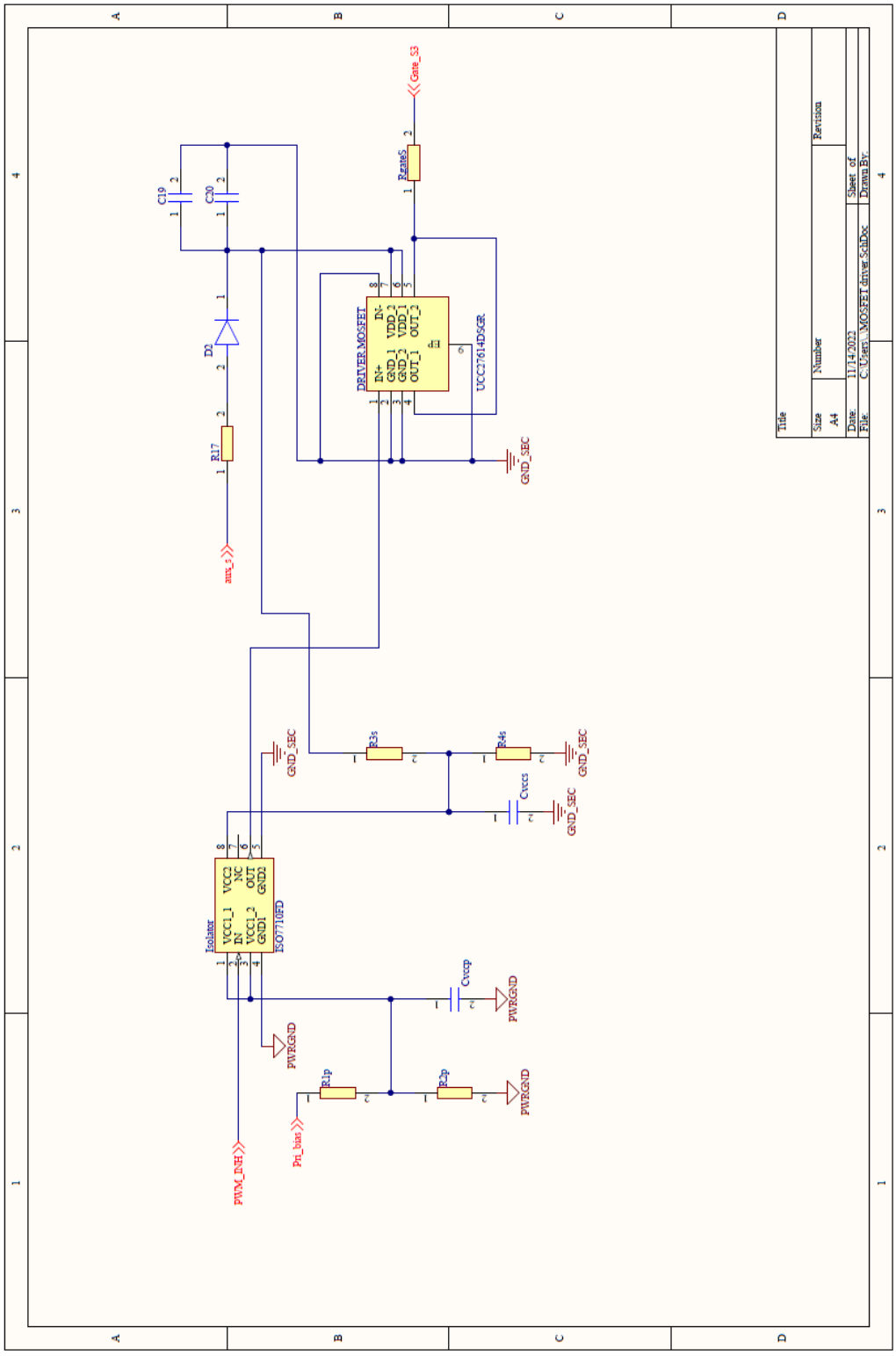


Figure 5.16: Sheet 3 of the PCB schematic.

5.4.2 Layout

The PCB layout has been carried out following the recommendations reported in the application note[8] of the NCP51820 half-bridge GaN HEMTs gate driver and in the UCC28780 controller datasheet[9]. These papers highlight the most important PCB layout considerations that must be taken into account to achieve good performance.
Particularly, GaN HEMTs switch faster than Silicon MOSFET and specific care in the layout design must be adopted to minimize parasitic inductances. The GaN HEMT devices can be overstressed by the parasitic inductances as these cause high overshoot voltage, ringing, and EMC issues [27].
First of all, a design rules file[10] provided by Eurocircuits has been imported in the Altium project. The *Class 6C – 4 layer – 1.55 mm* design rules file has been chosen to meet the GaN driver layout recommendations.
The dimensions of the PCB prototype needed to achieve a good component placement, ground planes arrangement and trace routing are (98 x 45.5) mm. The width of the traces is set equal to 0.2 mm for analog and digital signals and 1 mm for power signals. The layer stackup is shown in Figure 5.17 and it is organized as follows:

- Top Layer includes the through-hole components, the Graetz bridge and the power traces;
- Layer 1 includes signal traces;
- Layer 2 includes ground and return planes;
- Bottom Layer includes the surface-mount components and signal and power traces.

#	Name	Material	Type	Thickness	Weight	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask	0.01016mm		3.5
1	Top Layer	CF-004	Signal	0.0175mm	1/2oz	
	Dielectric 2	FR-4	Prepreg	0.36mm		4.8
2	Layer 1	CF-004	Signal	0.035mm	1oz	
	Dielectric 1	FR-4	Dielectric	0.71mm		4.8
3	Layer 2	CF-004	Signal	0.035mm	1oz	
	Dielectric 3	FR-4	Prepreg	0.36mm		4.8
4	Bottom Layer	CF-004	Signal	0.0175mm	1/2oz	
	Bottom Solder	Solder Resist	Solder Mask	0.01016mm		3.5
	Bottom Overlay		Overlay			

Figure 5.17: Altium Layer Stackup.

The best layout strategy described in the application note of the NCP51820 GaN driver and adopted in this thesis work is summarized in Figure 5.18.

[8] https://www.onsemi.com/pub/Collateral/AND9932-D.PDF
[9] https://www.ti.com/lit/gpn/ucc28780
[10] http://www.eurocircuits.com/altium-designer-templates-with-eurocircuits-design-rules/

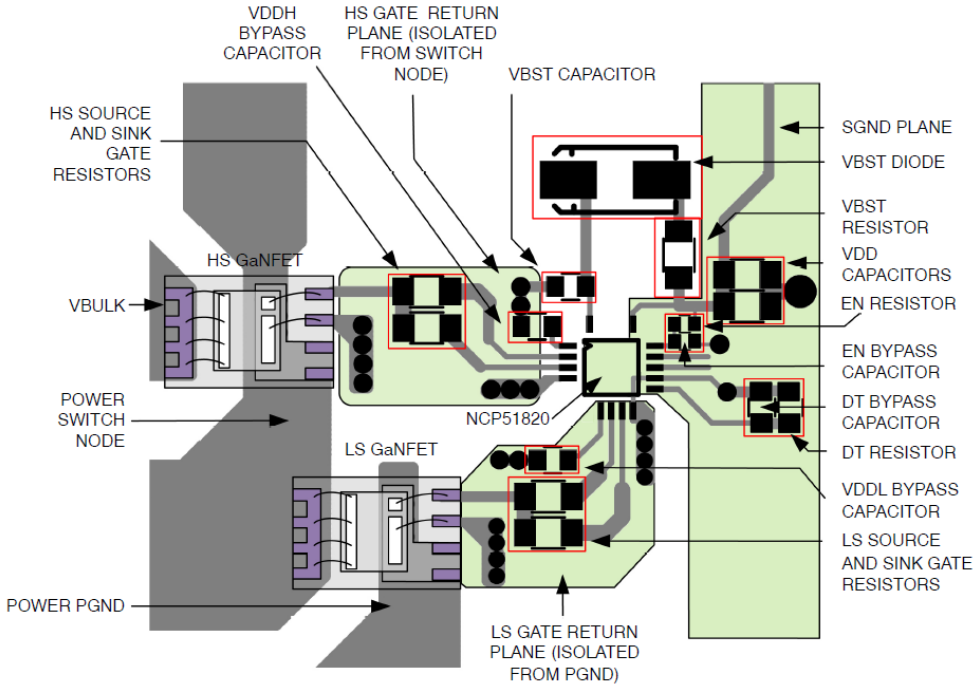


Figure 5.18: Half-bridge GaN HEMTs gate driver layout strategy [28].

The followed procedure is listed below:

- Multi-layer PCB design approach and proper ground and return planes placements are recommended due to high frequency, high voltage, high dV/dt and high di/dt [28].
- The VDD bypass capacitor must be placed as close as possible to the VDD pin. More precisely, two ceramic capacitors are used, a lower value bypass capacitor equal to 0.1 µF placed in parallel with the bypass capacitor of 1 µF computed in Section 5.2.1. An SGND return plane is required to keep all signals at the same potential. This return plane is placed on Layer 2 close to the signal-side pins of the gate driver and to the signal-side components, however, it does not extend close to the HO and LO gate driver pins to avoid noise coupling.

  The NCP51820 typical application schematic is reported in Figure 5.19 to easily understand this procedure.

  The VDD capacitors and the VDD pin are directly connected through a trace while the VDD capacitors return is connected to the SGND plane using vias [28].
- The BST bootstrap capacitor must be placed as close as possible to the VBST pin of the gate driver. The bootstrap capacitor return is connected to the VDDH capacitor return and to the SW pin of the gate driver using multiple vias linked to a dedicated return plane. This return plane is defined as the High Side (HS)

return plane and it is placed on Layer 2 close to the HO gate driver pins and to the high-side GaN HEMT.

It is important that there is no direct connection between the power stage switch node and the SW pin of the gate driver. The latter must be connected to the Source Kelvin pin of the high side GaN HEMT device. Similarly, there must be no connection between the source of the low-side switch and the PGND pin of the gate driver. The latter pin must be connected to the Source Kelvin pin of the low side GaN HEMT device. This prevents switching noise and power ground noise from being injected into the high side and low side gate driver paths.

Furthermore, the SGND plane must not be placed below the bootstrap diode and the bootstrap capacitor to prevent that the high dV/dt of the diode cathode from injecting noise into the SGND plane [28].

- The VDDL and the VDDH capacitors must be placed as close as possible to the VDDL and VDDH pins respectively. They are connected to their return planes through multiple vias.

  Moreover, the SW pin and the PGND pin of the gate driver are connected to the HS return plane and LS return plane respectively through multiple vias. Multiple vias are needed to reduce the parasitic inductance and due to the presence of high gate driver currents [28].
- The DT resistor and capacitor must be placed between the DT pin and the SGND pin [28].
- The HO and LO source and sink gate driver resistors must be placed as close as possible to the GaN HEMTs [28].
- To achieve nearly equal gate driver impedance for the high side and low side GaN devices, the HS and LS gate driver traces should be the same length [28].
- The NCP51820 high side and low side gate drivers are internally isolated, as shown in Figure 5.20, therefore they require dedicated return planes that are the HS return plane and the LS return plane [28].
- The SGND represents the ground for the internal control logic and digital inputs, while PGND is the low side gate driver return reference. They are internally isolated as shown in Figure 5.20 [28].
- In applications without a current-sense (CS) resistor, the PGND and the SGND pins are connected. However, in this project, the CS resistor is present and hence the PGND and the SGND pins must not be connected otherwise the CS resistor is short-circuited [28].
- The NCP51820 SGND return plane and the power ground of the PCB (PWRGND) must be connected through a thin trace [28].

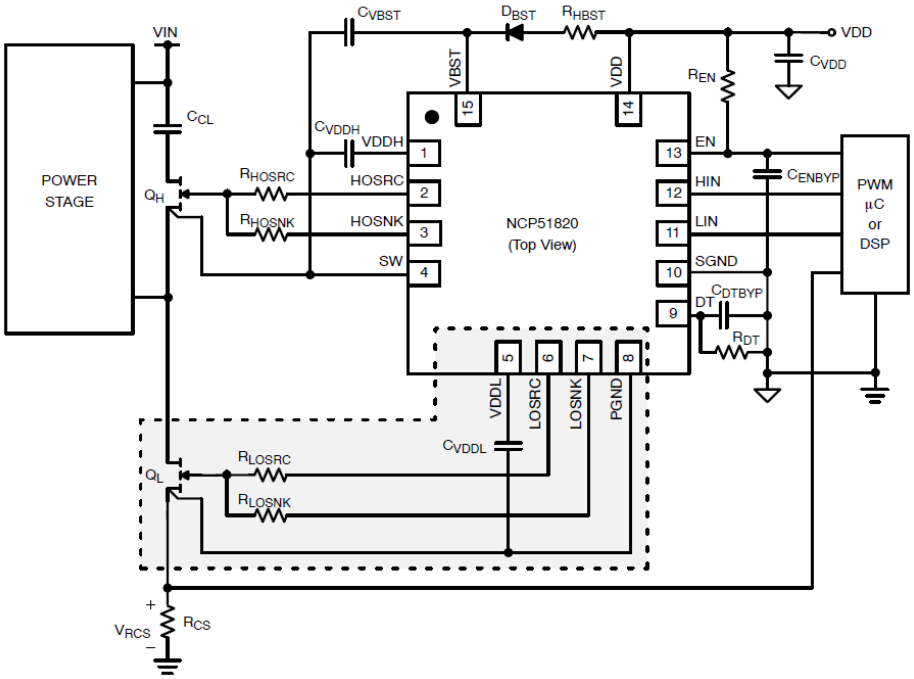


Figure 5.19: NCP51820 typical application schematic [23].

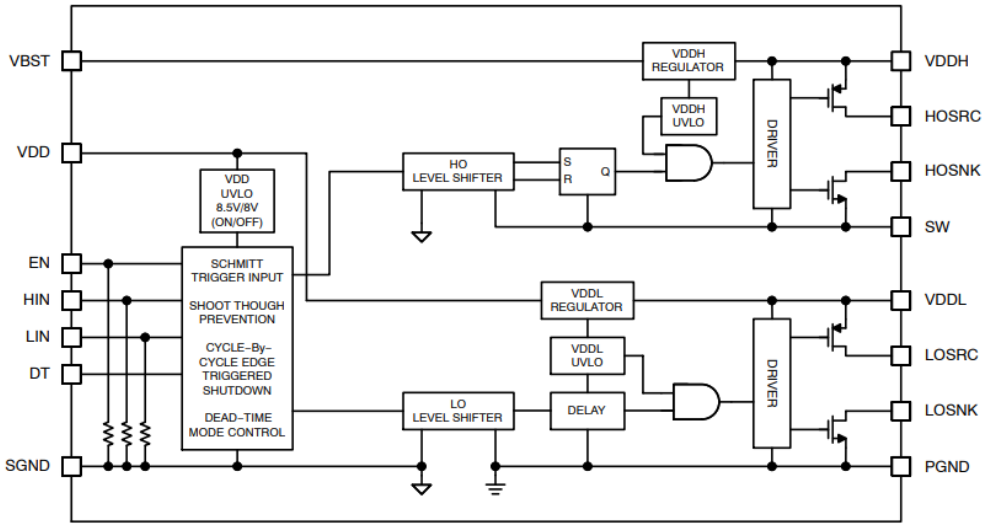


Figure 5.20: NCP51820 internal block diagram [23].

For what concerns the rest of the circuit, the guidelines reported in the controller datasheet have been adopted and they are reported in Figure 5.21. More precisely, the UCC28780 datasheet recommends removing the ground plane under the RDM, RTZ,

NTC, VS, SWS, HVG and VDD pins. Moreover, signal and power ground planes must be kept separated and they can be connected at the return of the R_{CS} current-sense resistor [21].

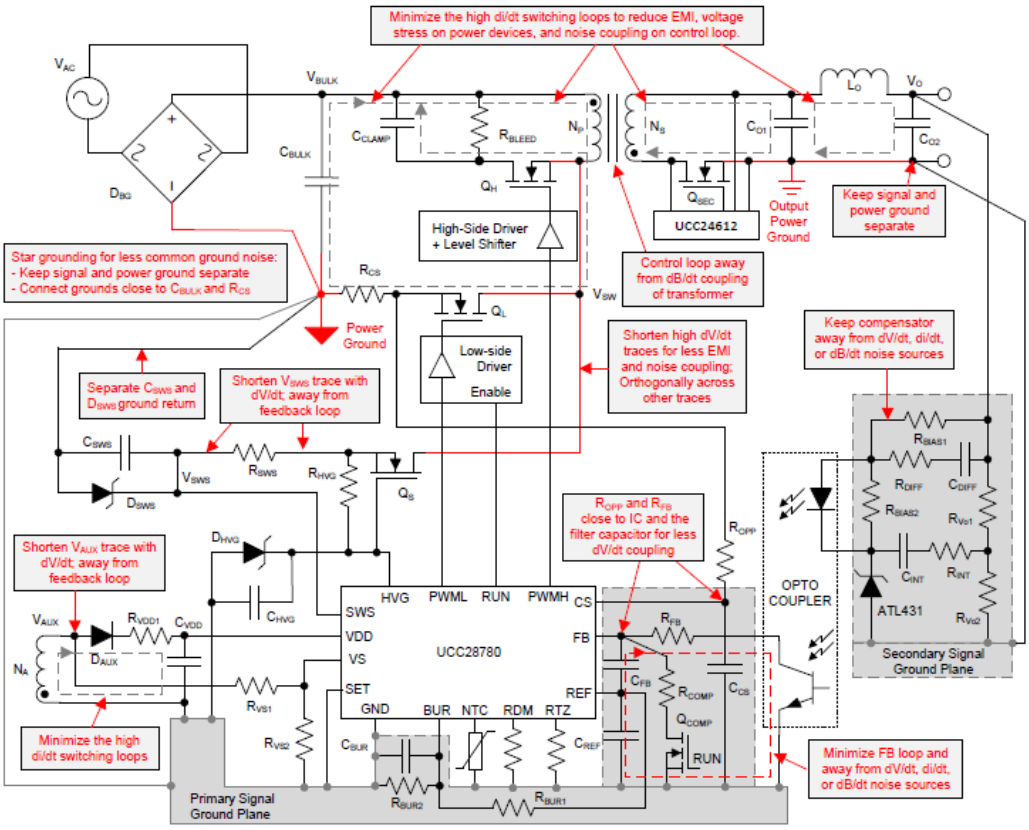


Figure 5.21: UCC28780 schematic with layout considerations [21].

Figure 5.22 and Figure 5.23 report the 2D views of the PCB Top Layer and Layer 1 respectively. Figure 5.24 reports the 2D view of the PCB Layer 2 highlighting the ground and return planes regions. Figure 5.25 reports the 2D view of the PCB Bottom Layer.

Finally, Figure 5.26 and Figure 5.27 shows the 3D Top view and Bottom view of the PCB prototype.

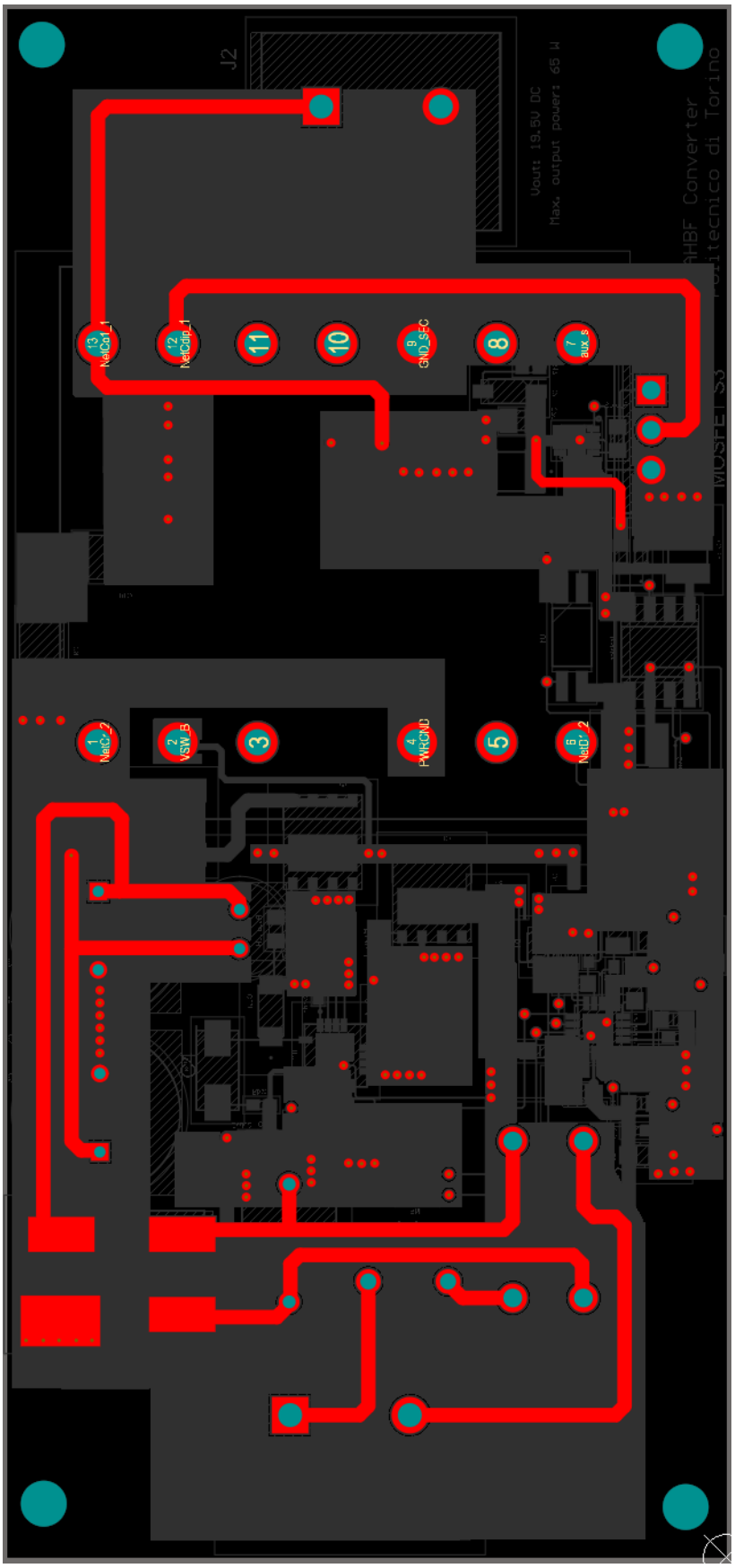


Figure 5.22: 2D PCB Top Layer.

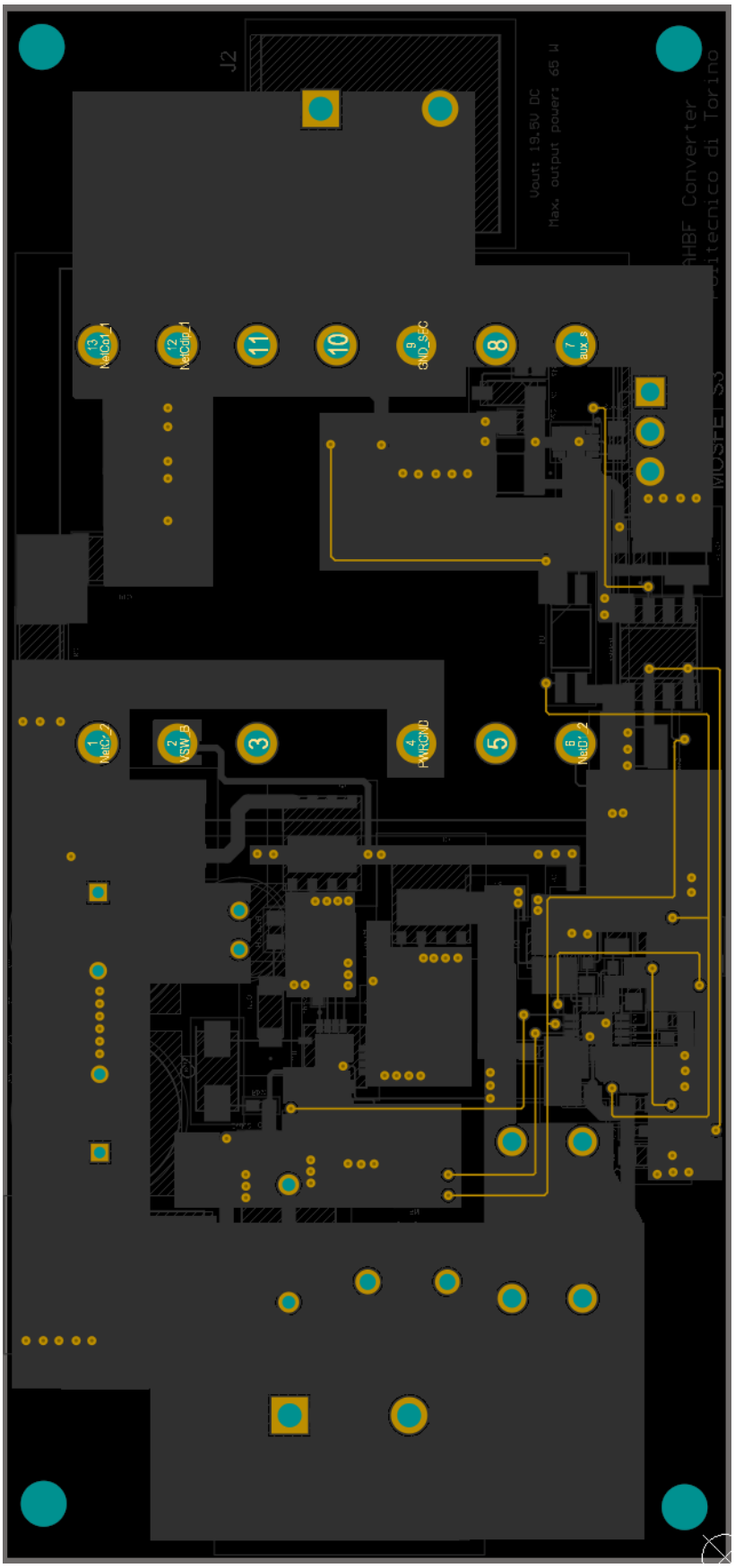


Figure 5.23: 2D PCB Layer 1.

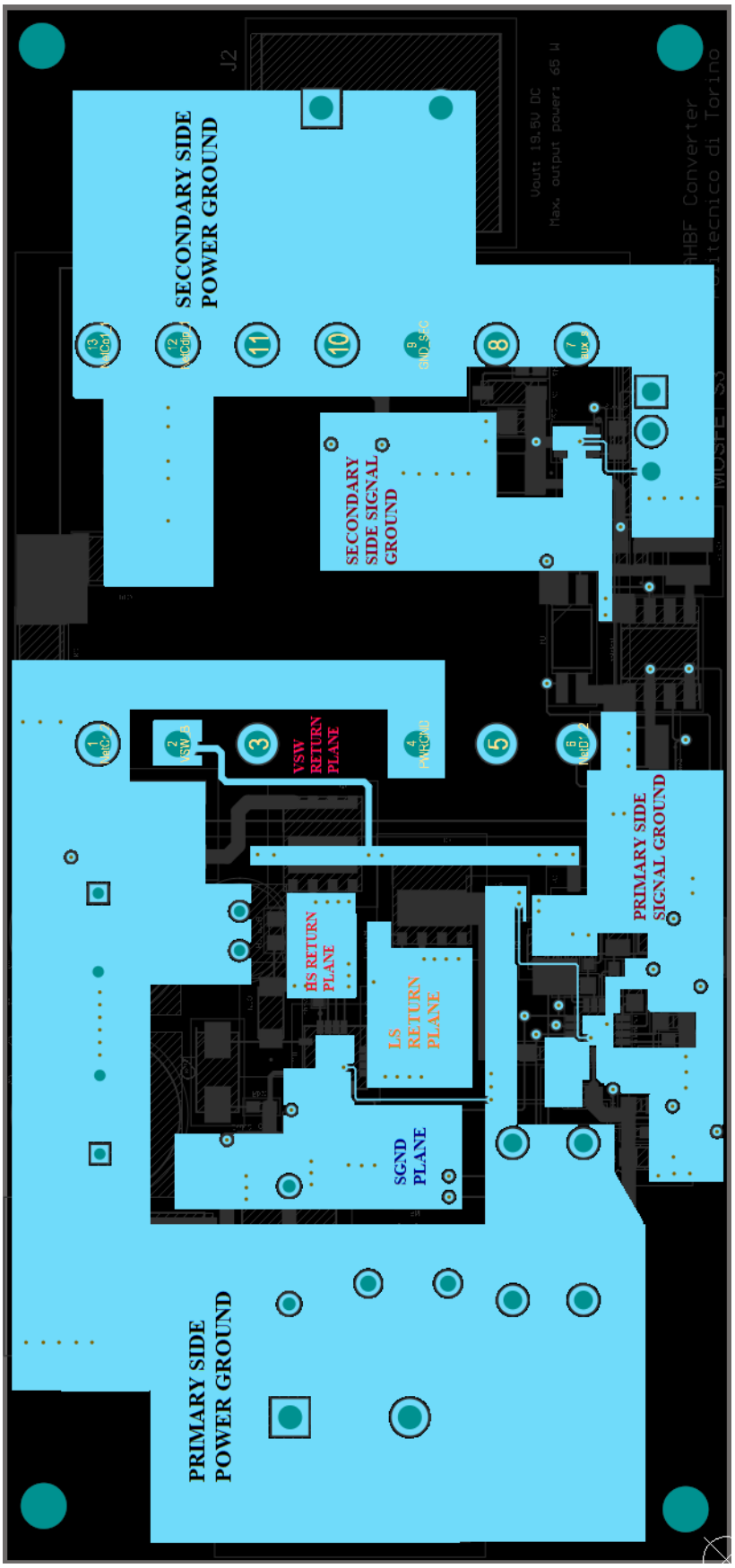


Figure 5.24: 2D PCB Layer 2.

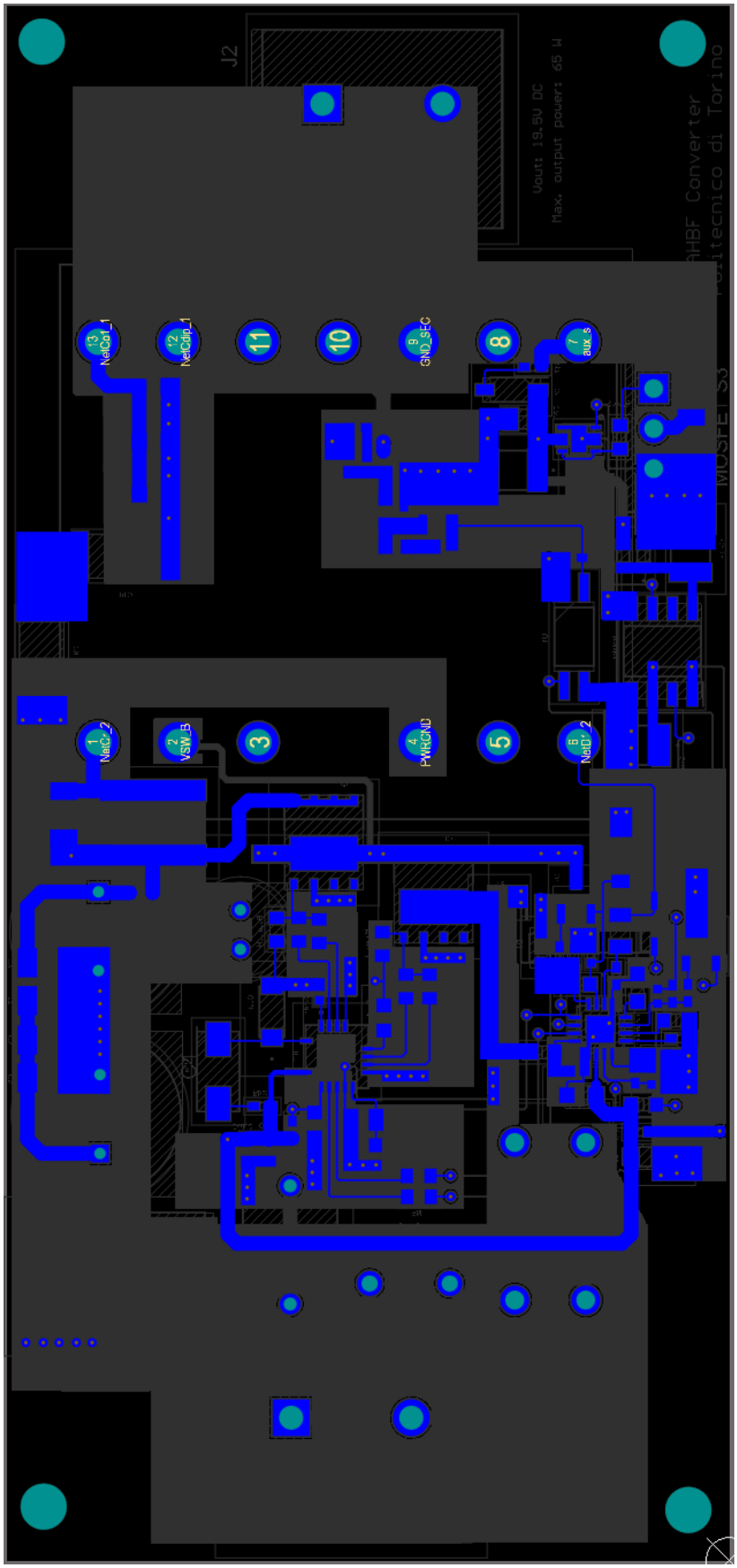


Figure 5.25: 2D PCB Bottom Layer.

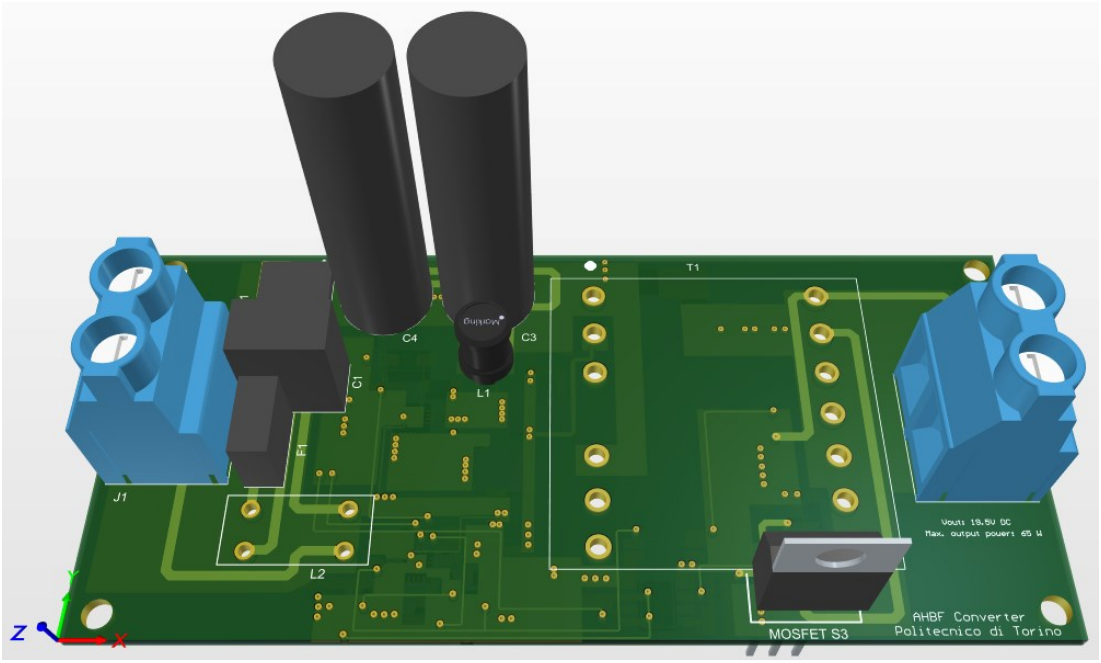


Figure 5.26: 3D PCB Top View.

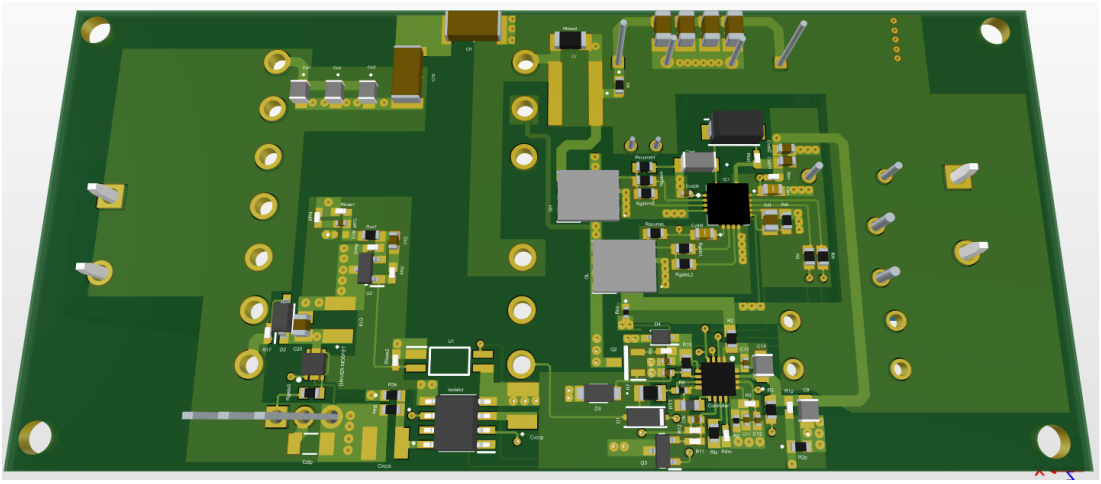


Figure 5.27: 3D PCB Bottom View.

Chapter 6

Conclusions

The activities described in this thesis focus on the design of the power converters employed in chargers/adapters for mobile electronic devices. The reduction in the adapter dimensions and in its losses oriented the design toward a high efficiency, high frequency (i.e., 1 MHz) and high-power density solution.

A preliminary study of the literature on power converter topologies used for adapter applications and their state of the art was performed. This literature analysis aimed to identify the best power converter topology in terms of efficiency, component stress and size reduction. The most common power converter topologies used for this kind of applications are based on the flyback converter and LLC resonant converter architectures. Indeed, they includes a resonant inverter and a synchronous rectifier. The resonant inverter consists of a half bridge switches configuration and a resonant LC tank which is composed of a resonant capacitor and a transformer, while the synchronous rectifier is the one employed in the flyback converter architecture. The studied papers highlighted three main power converter topologies: Active Clamp Flyback converter, Asymmetrical Half Bridge Flyback converter and LLC resonant power converter. A circuit analysis was performed for each of these mentioned topologies to understand the behaviour of the current and voltage waveforms and the energy transfer between the primary and the secondary side of the converter. The following step was to perform the converters designs to identify the topology with the minimum component stress and circuital simulations were performed to verify the theoretical analysis and to compute the converter efficiency. In terms of component stress, the AHBF converter and the LLC resonant converter were found to be the best with a noticeable reduction in the voltage stress of the primary and secondary switches compared to ACF converter. The voltage stress was reduced from $V_{in} + nV_o$ to V_{in} for the primary switches and from $V_{in}/n + V_o$ to V_{in}/n for the secondary switch, being V_{in} the input voltage, V_o the output voltage and n the transformer turns ratio. This feature allowed to have a greater safety margin for the choice of the transistors and also the reduction of the amount of power dissipated during their operation with a consequent increase in the efficiency. Nevertheless, the AHBF converter can operate correctly for a wide input voltage range achieving higher efficiency with respect to the LLC

resonant converter. For what concerns the efficiency, the AHBF converter reached higher values with respect to the ACF and LLC converters. Therefore, the AHBF converter was chosen in this thesis work as the most suitable topology to meet the starting requirements.

Further designs for the ACF and AHBF converter topologies were carried out implementing additional methods to the general design such as the primary resonant current dip effect, the secondary side resonance scheme, and the combination of these two methods. The studied papers showed how the latter method implemented in the ACF converter obtained good results in the efficiency, therefore it was also tested in the AHBF topology to further improve its efficiency. The AHFB converter with both the primary resonant current dip effect and the secondary side resonance scheme reached good results compared with the other designs increasing the efficiency of the converter from 97.2% to 98.9% in the simulation results with the ideal component models and from 96.5% to 97.6% in the simulation results with the real component models. Then, the evaluation of the power dissipated by the components was performed and the secondary side transistor was found to be the component that dissipates the most amount of power. Since the transistor conduction losses are related to its on-resistance, a transistor with a lower on-resistance was chosen and as expected, this achieved good results in the whole efficiency of the converter.

As next step, a programmable digital controller was selected to generate the control signals for the switching operation of the primary and secondary side transistors. It is an ACF controller consisting of a control method able to reduce the size of the passive components for high power-density and high efficiency applications. In this thesis work, it was properly adapted to the AHBF topology for its ability to operate up to 1 MHz and due to the compatible dead-time values with those obtained from the AHBF converter design and simulations. Furthermore, only one controller was adopted for both the primary side and the secondary side transistors. The latter was controlled simultaneously with the primary high side transistor thus saving an additional controller with its attached circuitry.

The last section of this work consisted in the practical implementation of the PCB prototype. The gate driver for the primary side switches and the one for the secondary side switch were selected and properly connected. Finally, the PCB was designed by using the Altium Designer software and a proper layout strategy was described in detail which should be able to achieve good performance in the presence of GaN devices.

During the development of this work, some difficulties related to the fabrication of the coupled inductors were encountered. These difficulties were particularly related in achieving a low leakage inductance value. The required low value of the leakage inductance can be obtained by interleaving the primary and the secondary windings. However, the coupled inductors realized with this method may not comply with the conditions imposed by the IEC 62368-1 electrical safety norm.

6.1 Future works

The future developments of this thesis are suggested in this section.

- This thesis work has to be completed with the assembly of the PCB prototype and its experimental measurements to validate the complete circuit of control circuit and gate drivers with the aim of confirming the results obtained from the simulations.

- To fully exploit the benefits of the AHBF converter described in Chapter 3, the 650 V GaN HEMT devices adopted for the half-bridge configuration should be replaced with GaN devices featuring a lower voltage rating than the current 650 V, again considering the low output capacitance required. For example, 450 V could be a good value since the maximum computed voltage rating is equal to 354 V. Obviously, this replacement can be possible when GaN HEMT devices with these voltage ratings will be available on the market and, at that time, the topology studied in this thesis will be better utilized.

- Another future development could concern the design of the coupled inductors. Their design could start from the identification of the value of leakage inductance that is best suited for complying with the requirements imposed by the IEC 62368-1 electrical safety norm. Then, the other components of the converter should be resized to implement the methods proposed in this thesis.

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