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Digital-Based Amplifier on Flexible Substrate: Analysis and Design



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Abstract

This thesis addresses design of a digital based operational transconductance amplifier (DB-OTA) in flexible integrated technology. The thesis begins with a review on flexible technologies, along with the specific IGZO TFT technology used, their applications and advantages, making an overview of its lithographic cross section. The work proceeds with a review of operational amplifiers performance parameters and some of its topologies.

Next, a flexible operational transconductance amplifier designed by using a traditional analog topology is provided. Design of the DB-OTA is on the basis of previous digital based OTA implemented in CMOS technology. Required revisions are done to adapt the design to the flexible technology.

For the purpose of a comparison between the performance of the two amplifiers, layout of both designs along with typical post layout and Monte Carlo Cadence simulations are done. Comparison of the proposed amplifiers and other flexible amplifiers in recent literature shows a better performance for DB-OTA in terms of area, power consumption and figure of merit.

Acknowledgments

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Chapter 1

Introduction

In this chapter an overview on flexible technology, fabrication, applications and state of the art is presented along with its advantages comparing to conventional silicon technology that makes it possible to be used for everyday smart objects.

Flexible electronics have significantly advanced over the last few years [4], as devices and circuits from nanoscale structures to printed thin films have started to appear. Simultaneously, the demand for high-performance electronics has also increased.

Many existing applications such as implantable systems that require bendability to conform to the curved surface of tissues are driving the progress in the field, which in turn is the enabler for numerous futuristic applications such as mobile healthcare (mHealth) wearable systems, smart cities and wearable internet-of-Things(IoT) products.

A commonly known application of flexible technology is organic light emitting diodes (OLEDs), which is more and more employed in consumer electronics. It is challenging to obtain flexible and compact integrated circuits as the silicon based CMOS electronics, which is currently the industry standard for high-performance, is planar and the brittle nature of silicon makes bendability difficult. Flexibility has been achieved by thinning the wafers down to 50 μ m. Conventional silicon technology faces key challenges to make everyday objects smarter [4], such as bottles (milk, juice, alcohol or perfume), food packages, garments, wearable patches, bandages, and so on. Cost is the most important factor preventing conventional silicon technology from being viable in these everyday objects. Although economics of scale in silicon fabrication have helped to reduce unit costs dramatically, the unit cost of a microprocessor is still prohibitively high. In addition, silicon chips are not naturally thin, flexible and conformable, all of which are highly desirable characteristics for embedded electronics these days.

1.1 Flexible Technology

Natively flexible electronics, are built on substrate such as paper, plastic or metal foil and use active thin-film semiconductor materials such as organics or metal

oxides or amorphous silicon [4]. The choice of substrate is critical and depends on the inherent material properties and the intended application.

The materials which have been used as flexible substrate can be broadly divided into two categories: metallic and polymeric. One advantage of metallic substrate is that it is a good electric and heat conductor, serving as heat sink or where electromagnetic shielding is required. While polymeric substrates are inherently elastic and flexible with ability to regain their normal shape.

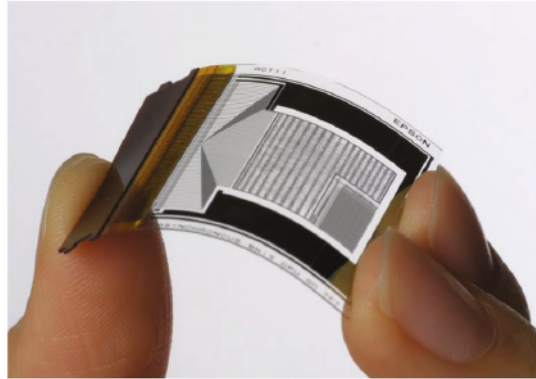


Figure 1.1: A flexible 8-bit asynchronous microprocessor based on low-temperature polysilicon TFT technology. Source [1])

Thin-film-transistors

The aim of the TFT technology is not to replace silicon. As both technologies continue to evolve, it is likely that silicon will maintain advantages in terms of performance, density and power efficiency. However, TFTs enable electronic products with novel form factors and at cost points unachievable with silicon, thereby vastly expanding the range of potential applications. Because of these properties a flexible TFT-based microprocessor can be possibly integrated imperceptibly into any object.

The thin-film transistor (TFT) became commercially available slightly more than 30 years ago in the form of a switch for the Liquid Crystal Display. It all started with an amorphous silicon (a-Si) TFT. Compared to the traditional crystalline silicon CMOS transistor, the a-Si TFT can be produced on large substrates and at low processing temperatures, below 300 °C, enabling integration on glass substrates and even flexible substrates.

A-Si TFTs are mainly implemented as simple pixel switches due to their low charge carrier mobility ($0.5\text{--}1\text{ cm}^2/\text{Vs}$). An alternative semiconductor on glass substrates is low-temperature polycrystalline silicon (LTPS), outperforming a-Si TFTs by a 100x larger mobility ($50\text{--}100\text{ cm}^2/\text{Vs}$) and often used for high-end displays and imagers. Despite the advantages, fabrication of an LTPS TFT takes more process steps, is limited in substrate size, and requires a larger process temperature. Oxide-based semiconductors as indium-gallium-zinc-oxide (IGZO) fill

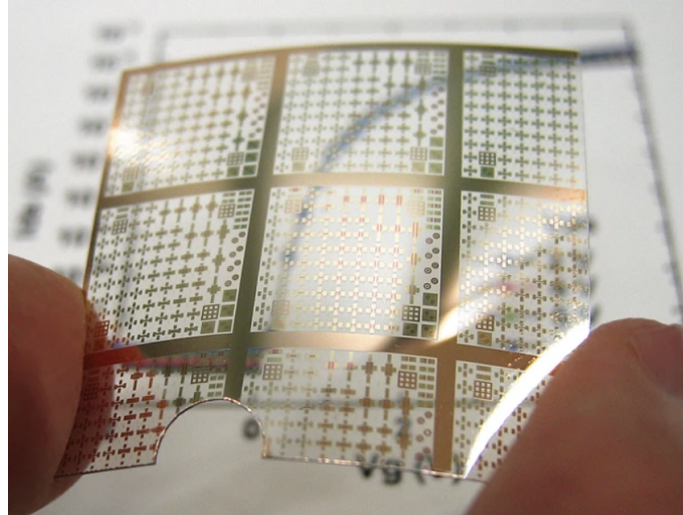


Figure 1.2: Amorphous indium gallium zinc oxide thin-film transistors fabricated on a plastic substrate. Source [2]

this gap between a-Si and LTPS nicely, exhibiting low processing temperatures and a decent charge carrier mobility of 10 up to 40 cm^2/Vs [9].

With such characteristics, the IGZO TFTs can be used to fabricate relatively complex circuits on flexible substrates. Consequently, IGZO TFTs are evolving beyond displays and entering the fields of wearable devices and the Internet of Things (IoT).

Some highlights include an ultra-flexible circuit for recording electrocardiograms [10], radiofrequency identification (RFID) tags and near-field communication (NFC) tags [9]. Even the memory field has noticed IGZO and its extremely low OFF current and recently demonstrated a capacitor-less IGZO-based DRAM cell with a retention time longer than 400 seconds [11].

We can expect the first IGZO products beyond display applications to emerge in the near future.

Overall for drawbacks of flexible technology we can mention: not complementary, poor power efficiency, low speed, high area, Indium and Gallium are rare earth metals.

In the fig. 1.3 the cross section of the fabricated IGZO TFT can be observed. A deposited silicon nitride (SiN_x) layer serves as adhesion layer to the substrate consisting of a kapton polyimide film,, the gate contact consists of an e-beam evaporated Cr layer, for drain and source contacts, titanium and gold are electronic-beam evaporated and structured using liftoff. Finally, the whole devices are passivated with a Al_2O_3 layer.

Applications

The applications of flexible technology are mostly related to the ones where the flexibility property is actually useful. The term "flexible" itself, can take different definitions varying from application to application. From bending and rolling for easier handling of large area photovoltaics, to conforming onto irregular shapes,

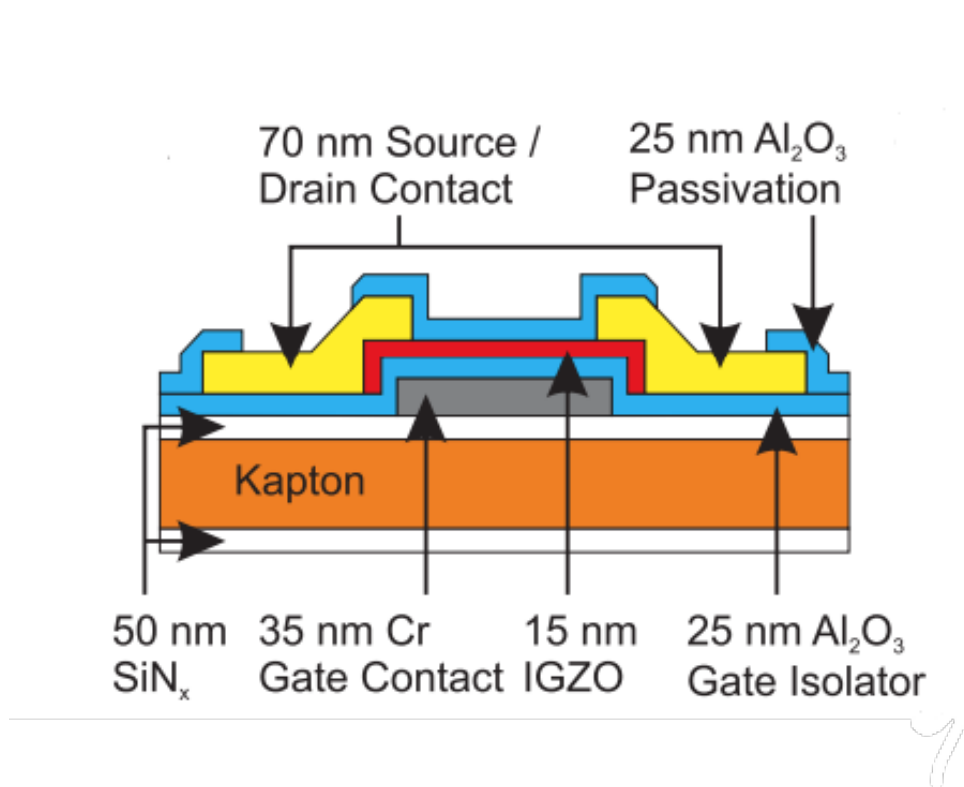


Figure 1.3: Cross section of fabricated IGZO TFT. Source [3]

folding, twisting, stretching, and deforming required for devices in electronic skin, all while maintaining device performance and reliability. Brief review of applications are as follows:

- Bioelectronics which takes advantage of wearable electronics. Some healthcare-related applications such as limb prosthesis can take advantage of flexible technology, since detecting various signals with extremely high sensitivity is required while withstanding high-levels of deformation [12].
- Energy storage: Research in flexible zinc-based rechargeable batteries is overcoming the limitations of rigidity and weight that characterize current portable batteries [13] and the difficulty in fabricating high-performance flexible lithium-ion batteries with thickness less than 1 mm [14].
- Communication: miniaturized, flexible and stretchable antennas are required to fulfil the needs of some sensors and have gained a lot of interest in order to overcome some challenges, for instance rigidity, deformation and hard integration with clothing [15].
- Energy harvesters: power sources, able to supply energy autonomous devices, like sensor nodes or wearable electronics, is among the applications which drive the development of flexible technologies. Still some challenges regarding the overall efficiency of these devices persist [16].

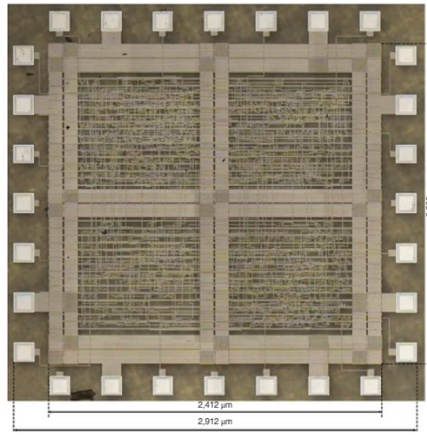


Figure 1.4: Micrograph of the natively flexible processing engine (NFPE) implementing the UB-FVC microarchitecture, Source [4].

State of the art

The field of flexible and stretchable electronics has evolved very rapidly over the past ten years, from electrochemical to optical societies. One application of flexible technology reported in [17], uses n-type metal-oxide TFT devices based on indium-gallium-zinc oxide (IGZO) and fabricates the flexible integrated circuit (flexIC) design on a 200mm diameter wafer by running several sequences of material deposition, patterning and etching as in traditional silicon technologies. Another demonstrative application of flexible technology has been reported in [1], a 8-bit flexible 6502 microprocessor in $0.8 \mu\text{m}$ metal-oxide thin-film transistor technology implemented with a complete digital design flow and capable of running real-time complex assembly code. Manufactured on a flexible polyimide substrate with total thickness less than $30 \mu\text{m}$.

Here a comparison table of 6502 then(1975) and now(2022) is presented.

	MOS 6502	Flexible 6502
Year	1975	2022
Device count	4528	16392
Area	21 mm^2	24.9 mm^2
Power consumption	250mW	134.9mW
Operation speed	1MHz	71.4kHz
Semiconductor	silicon	IGZO
Logic family	depletion-load	Pseudo-PMOS
Technology	$8 \mu\text{m}$	$0.8 \mu\text{m}$

Table 1.1: Comparison of characteristics of MOS and Flexible 6502 microprocessors

Worth to mention recent trends and achievements by PragmatIC:

- Fabrication of plastic chips on 300mm glass wafers, which have taken advantage of no supply chain issues as it has happened to silicon-based

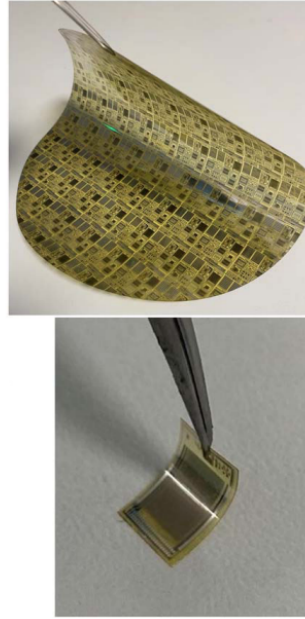


Figure 1.5: Test circuit of flexible 8b microprocessor. Source [5]

technologies during the Covid-19 pandemic [18] since no silicon is employed as the substrate, while also benefiting of faster process [19].

- Environmental and economical benefits by reusable containers given digital identities. The key challenges in transition to reusable containers is making it viable for any packaging to be smart and connected using Near Field Communication (NFC) technology [1].

This work

In this thesis the design of a digital based operational amplifier in flexible technology is discussed. The base idea is related to the Digital Operational Transconductance Amplifier (DIGOTA) presented in the article [8] which design has been revised for flexible technology.

Thesis organization

In the introduction chapter, an overview to the flexible technology and its development in the recent years is provided. Second chapter provides a review on op-amps, their performance parameters and some of their basic topologies. In the third chapter design of a traditional analog amplifier in flexible technology is discussed, providing small signal analysis and gain. Then the layout of the circuit is reported along with typical post-layout simulation results and Monte Carlo post-layout simulations.

Next in chapter four, the design of the digital-based Operational Transconductance Amplifier (DB-OTA) is addressed, presenting the schematic and discussing its behaviour. Following the design and waveforms of DB-OTA in voltage follower configuration from [8] are presented, considering the mathematical model of the

circuit and clarifying the performance of different stages with particular focus on the common-mode extractor.

Focusing on the differences in flexible technology with respect to CMOS, Nor and Inverter logic gates are designed and the complete circuit of the DB-OTA in flexible technology is discussed. Layout of the the two logic gates and the DB-OTA is presented along with post-layout and Monte Carlo Cadence simulations.

In chapter five Analog OTA and DB-OTA performance are compared with reference to the current state of the art.

Chapter 2

An overview on operational amplifiers

In this chapter an overview of performance parameters of operational amplifiers (op-amps) and its basic topologies are presented. These parameters are later used in the evaluation of the OTAs presented in this work.

Operational amplifiers Operational amplifiers (op-amps) are an integral part of many analog and mixed-signal systems. Op-amps with vastly different levels of complexity are used to realize functions ranging from DC bias generation to high-speed amplification or filtering. The design of op-amps continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technology. In figure below there is the simplified model

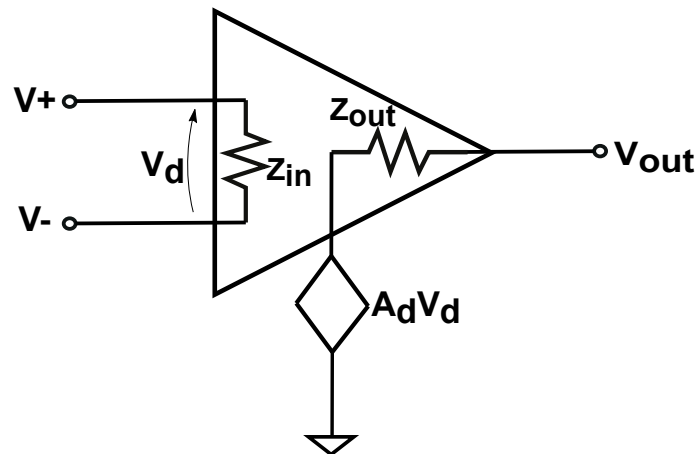


Figure 2.1: Op amp model for its analysis.

of op-amp including its parameters. The inputs are expressed as v_+ , v_- and the output as v_{out} .

$v_d = (v_+ - v_-)$ is the differential input voltage

A_d is the differential gain.

Z_{in} is the input impedance.

Z_{out} is the output impedance.

The ideal op-amp has infinite input impedance, zero output impedance and infinite differential gain. This way input/output loading is avoided.

2.1 Op-amp performance parameters

Small signal performance

Open-loop Gain The open-loop voltage gain, is defined as the ratio of changes in output voltage to the changes in the voltage across input terminals. It is the gain of amplifier without the feedback loop being applied. In Fig. 2.3 the bode plot of the open loop transfer function of an op-amp with one dominant pole is shown.

$$A_d(f) = \frac{v_{\text{out}}(f)}{v_d(f)}$$

Closed-loop gain To provide the op-amp with a fixed gain which is independent at first order from the open loop gain variations, negative feedback is applied to op-amps, in that case the overall gain of the op-amp is called closed-loop gain. Figure 2.2(b) shows the general structure of a negative feedback system consisting of feedback factor b and open-loop gain of op-amp A_d .

$$\frac{v_{\text{out}}}{v_{\text{in}}} = \frac{1}{b} \frac{A_d b}{1 + A_d b} \quad (2.1)$$

The ideal value of closed-loop gain occurs for an for a loop gain approaching infinite $A_d b \rightarrow \infty$, meaning that $\frac{v_{\text{out}}}{v_{\text{in}}}|_{\text{ideal}} = \frac{1}{b}$. Depending on whether the input signal is applied to the inverting input terminal or non-inverting input terminal, closed-loop gain can have negative or positive sign. Figure 2.2(a) shows a non-inverting op-amp. Considering op-amp's open-loop gain to be ideal, voltage gain is equal to:

$$\frac{v_{\text{out}}}{v_{\text{in}}} = 1 + \frac{R_1}{R_2}.$$

Gain bandwidth product Product of the open-loop voltage gain and the frequency at which it is measured is always the same value at different frequencies, this value is called gain bandwidth product (GBW).

Op-amp's transfer function (figure 2.3) is flat from DC to what is referred to as the dominant pole corner, from there the gain falls off at 20dB/decade while its DC value determines the precision of the feedback system. The frequency of the dominant pole of the open loop gain is also called the Open-loop-3dB-frequency f_b which is exactly -3dB below maximum voltage gain (A_0). The **open-loop bandwidth** is defined in the period of zero to f_b frequency. Unity-gain frequency or transition frequency (f_t) is where the open-loop gain passes 0dB or 1V/V.

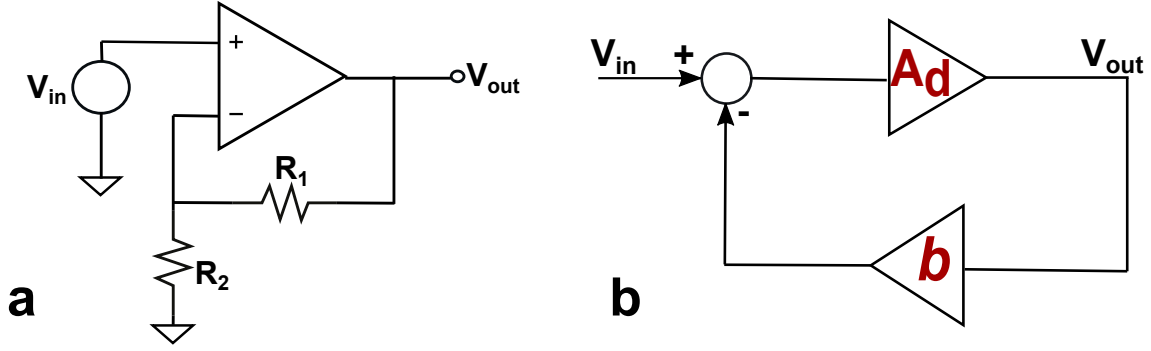


Figure 2.2: Op-amp with resistive feedback (a) general structure of negative feedback (b)

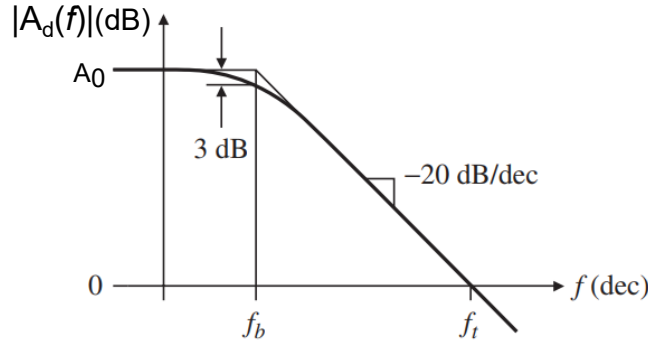


Figure 2.3: Transfer function of the op-amp indicating dominant pole and transition frequency.

Large signal parameters

Common mode rejection ratio In the absence of input offset, an op-amp should respond only to the voltage difference between its inputs, or $v_{out} = A_d(v_+ - v_-)$. A practical op amp is somewhat sensitive also to the common-mode input voltage $v_{CM} = (v_+ + v_-)/2$. Its transfer characteristic is thus $v_{out} = A_d(v_+ - v_-) + A_{cm}v_{cm}$, where A_d is the differential-mode gain, and A_{cm} is the common-mode gain. Rewriting as $v_{out} = A_d[v_+ - v_- + (A_{cm}/A_d)v_{CM}]$, and recalling that the ratio A_d/A_{cm} is defined as the common-mode rejection ratio CMRR.

Total harmonic distortion One of the most common ways to define dynamic range of an op-amp is to specify total harmonic distortion (THD). It is the ratio of root-sum-square value of all the harmonics to the first harmonic level in order to quantify the effect of unwanted harmonics. Generally speaking, only the first five or six harmonics are significant in the THD measurement.

$$\text{THD} = \frac{\sqrt{v_2^2 + v_3^2 + v_4^2 + \dots v_n^2}}{v_1} \quad (2.2)$$

where $v_{2,3,\dots}$ represents different harmonics of the signal.

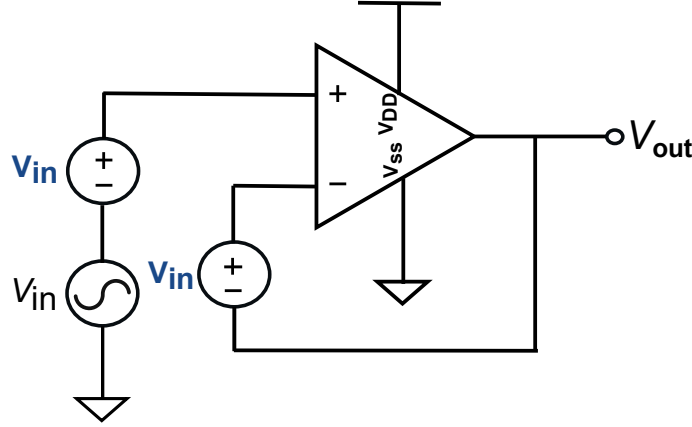


Figure 2.4: Test bench for CMRR calculation of DB-OTA.

Figure of merit The Figure of Merit (FOM) is an expression introduced to compare the overall performance of different implementations of the same circuit. Even though different FOMs can be defined depending on needs, one of the most common used to compare op-amps is the following, [20]:

$$\text{FOM} = \frac{\text{GBW} \cdot C_L}{\text{Power}} \quad (2.3)$$

where C_L is the load capacitance.

Power consumption Power consumption in an op-amp consists of various factors: quiescent power, op-amp output power and load power. The quiescent power is the power required to keep the amplifier functioning and is related to the op-amp's I_Q . The output power is power dissipated in output stage to drive the load. Finally, load power is the power dissipated in the load itself.

$$\text{Power} = V_{DD} \times I_Q \quad (2.4)$$

Slew rate From [6], the rate at which v_{out} changes with time is highest at the beginning of the exponential transition. In practice it is observed that above a certain step amplitude the output slope saturates at a constant value called the slew rate. Slew-rate limiting is a nonlinear effect.

Output swing From [7], most systems employing op-amps require large voltage swings to accommodate a wide range of signal amplitudes. The need for large output swings has made fully differential op-amps quite popular. Nonetheless, the maximum voltage swing is traded off with device size and bias currents and hence speed. Achieving large swings is principal challenge in today's op-amp design.

Offset voltage From [6], voltage offset is due to inherent mismatches between the two input-stage halves, processing v_+ and v_- . The effect of the offset voltage

can be modeled by adding a small voltage source in series with one of the op-amp inputs. and ideal op-amp will be modeled having a tiny source in series with one of its inputs. There will be an output error caused by this input offset voltage and expressed as follows:

$$E_o = \left(1 + \frac{R_2}{R_1}\right) \cdot V_{OS} \quad (2.5)$$

Input noise power spectral density $S_x(f)$ denotes power of noise waveform "X" in 1 Hz bandwidth around f . So the total noise power over a given bandwidth is calculated by computing the integral of S_x in that frequency band. The noise power spectral density from f_1 to f_2 can be expressed in V^2/Hz .

Power supply rejection ratio From [21] we assume for an ideal op-amp that the power-supply voltages are constant and the op-amp output voltage depends only on the differential input voltage. In practice, however, the power-supply voltage variations contribute to the op-amp output (see Fig. 2.5). Calling A_{ps} the small signal gain from the power supply to the output and recalling that A_d is the differential gain, the power source rejection ratio (PSRR) is defined as:

$$\text{PSRR} = \frac{A_d}{A_{ps}} \quad (2.6)$$

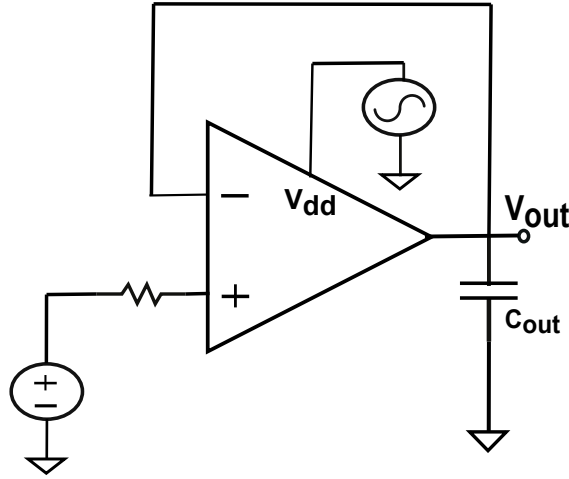


Figure 2.5: Circuit configuration for PSRR calculation of opamp.

2.2 OPAMP topologies

Single stage op-Amps

Figure 2.6 shows a single-ended op-amp topology which is made of a differential pair and a current source as bias [7]. General equation for voltage gain is as follows $A_d = \frac{v_{out}}{v_d} = g_m \cdot (r_N || r_P)$ where the subscripts N and P denote nMOS(M2) and

pMOS(M4) respectively. This value hardly exceeds a value of 20 in submicron devices with typical current levels. The bandwidth is usually dominated by the output pole, related to the load capacitance C_L .

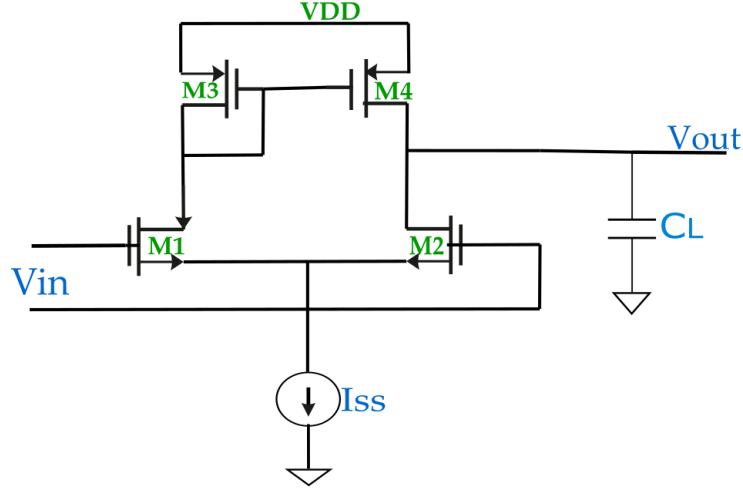


Figure 2.6: Simple op-amp topology

The proposed single stage op-amp suffers from noise contributions of transistors M1-M4. Generally speaking, in all op-amp topologies, at least four devices contribute to the input noise: two input transistors and two "load" transistors.

Small signal equivalent To obtain the small-signal model of the proposed op-amp, low-frequency gain and the dominant pole, the following equations are written based on the model shown below.

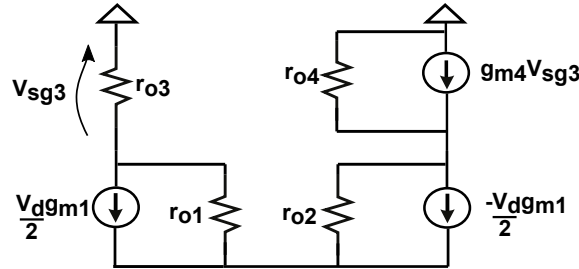


Figure 2.7: small signal equivalent of the op-amp topology in figure 2.6

$$v_{out} = \frac{v_d}{2} (g_{m1} \cdot 1/g_{m3}) \cdot g_{m4} \cdot (r_{o2} || r_{o4}) + \frac{v_d}{2} \cdot g_{m2} \cdot (r_{o2} || r_{o4}) \quad (2.7)$$

$$\text{if } g_{m1} = g_{m2} = g_m \text{ and } g_{m3} = g_{m4} \quad (2.8)$$

$$v_{out} = g_m \cdot (r_{o2} || r_{o4}) \quad (2.9)$$

$$p_1 = 1/R_{eq} \cdot C_L = 1/(r_{o2} || r_{o4}) \times C_L \quad (2.10)$$

Cascode op-Amp

Telescopic cascode The cascade of a common-source amplifier and a common-gate amplifier is called a "cascode" topology. Using this technique [6], we

can raise its effective output resistance r_o to make up for its poor g_m . Adding stacked transistors reduces the output swing at least by each one overdrive voltage. So the improvement of gain is at the cost of output swing reduction while facing additional poles. A cascode amplifier with a cascode load (current source) is called a "telescopic caDCode", having a larger gain with respect to the cascode topology. For the circuit presented below, total voltage gain is calculated as:

$$A_d = \frac{v_{out}}{v_d} = g_{m1}[(g_{m3}r_{o3} + 1)r_{o1} + r_{o3}]||[(g_{m7}r_{o7} + 1)r_{o5} + r_{o7}]$$

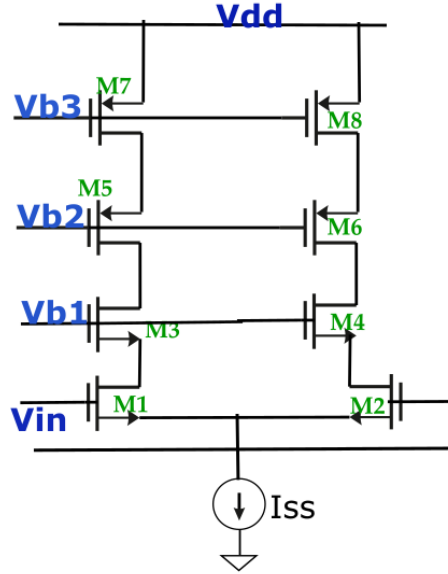


Figure 2.8: Cascode op-amp

Folded Cascode In order to alleviate the drawbacks of telescopic cascode op-amp, "folded cascode" op-amp can be employed [6]. The circuit in Fig.2.9 is a single-stage amplifier. The output MOS transistors are used for the purpose of raising the intrinsic gain of the basic stage by cascoding technique. In particular M_8 raises r_{o4} and M_6 raises r_{o2} to ensure a high overall output resistance R_{out} and thus maximize the gain ($g_{m1}R_{out}$). Input differential pair senses and converts any imbalance between its gate voltages to its drain currents. The drain current imbalance is then rerouted upwards towards $M_5 - M_6$ pair. The overall voltage swing of a folded-cascode op amp is only slightly higher than that of a telescopic configuration. This advantage comes at the cost of higher power dissipation, lower voltage gain, lower pole frequency and higher noise.

Two stage op-amp

One-stage op-amps allows the small signal produced by input pair to flow directly through the output impedance, as a result the gain of these topologies is defined as the product of the input pair transconductance and the output impedance [7]. In

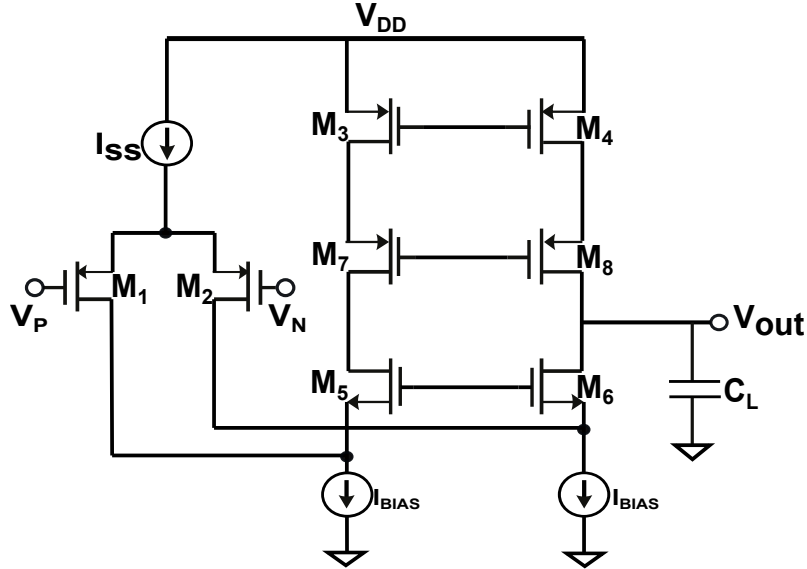


Figure 2.9: Folded cascode op amp topology. Source [6]

some applications, the gain and/or the output swings provided by cascode op-amps are not adequate.

In these cases we resort "two-stage" op-amps so that, the first stage provides a higher gain and the second stage, larger swing so in contrast to cascode configuration it isolates the gain and swing requirements.

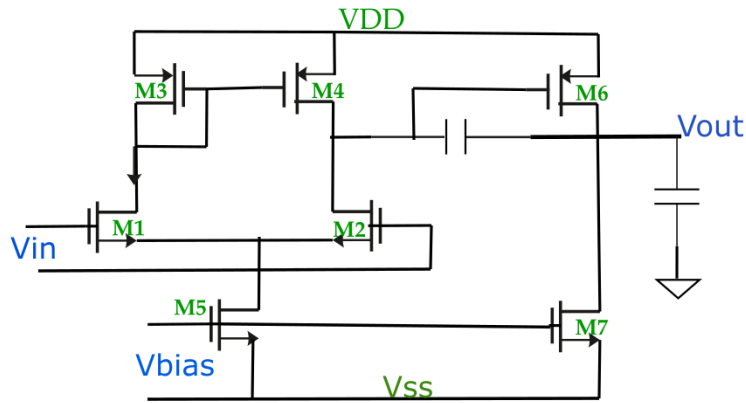


Figure 2.10: Two stage op-amp topology. Source: [7]

We can exploit virtually infinite gate resistance of MOSFETs to implement the second stage with a single transistor M_6 , while M_7 forms a current mirror together with M_5 for the purpose of biasing the differential pair and M_6 .

For the two stage circuit below, total voltage gain is calculated as the product of voltage gain of the two stages: $A_{v1} \times A_{v2} = g_{m2} \cdot (r_{o2} || r_{o4}) \times -g_{m6} \cdot (r_{o6} || r_{o7})$.

The second stage is typically configured as a simple common-source stage in pMOS, to allow maximum output swings.

Op-amps having more than two stages are rare, because each stage introduces a

pole in the frequency response and it would be more difficult to guarantee stability in a feedback system using such op-amps.

Chapter 3

Analog OTA in flexible technology working principle

This chapter presents the analysis and description of analog OTA design, small signal analysis and gain calculation. Followed by post layout simulation results and Monte Carlo analysis simulations.

A-OTA circuit design and description

The analog operational transconductance amplifier(A-OTA) consists of a differential stage, a source follower and a source-degenerated common-source output stage as depicted in Fig. 3.1.

The bias current for all stages is set to $10\text{ }\mu\text{A}$ as a compromise between gain, power consumption and noise. Accordingly, aspect ratio of transistors and the resistors have been set. The output stage resistor R_{out} has been set to provide a higher voltage gain, which results in a bias current of order of nano ampere in this stage. The source follower stage is employed as a level shifter to adapt the output voltage level of differential pair to the input voltage level of common-source output stage. Transistors M_0, M_3, M_5 are current mirrors for the purpose of duplicating the bias current. For the driving devices in the differential pair the largest aspect ratio is considered $150/1.6$, while the smallest is equal to $35/1.6$. In the final version of circuits schematic, intended to be used for matching comparison to circuits layout, a pair of dummy transistors are added to mitigate the effect of mismatch in the differential stage.

By applying a ramp voltage as the input signal, the exact range in which the output signal follows the input is discovered and based on the result in Fig.3.2, DC operating point for the input is set in middle of the range. In this way It's possible to have the maximum input swing.

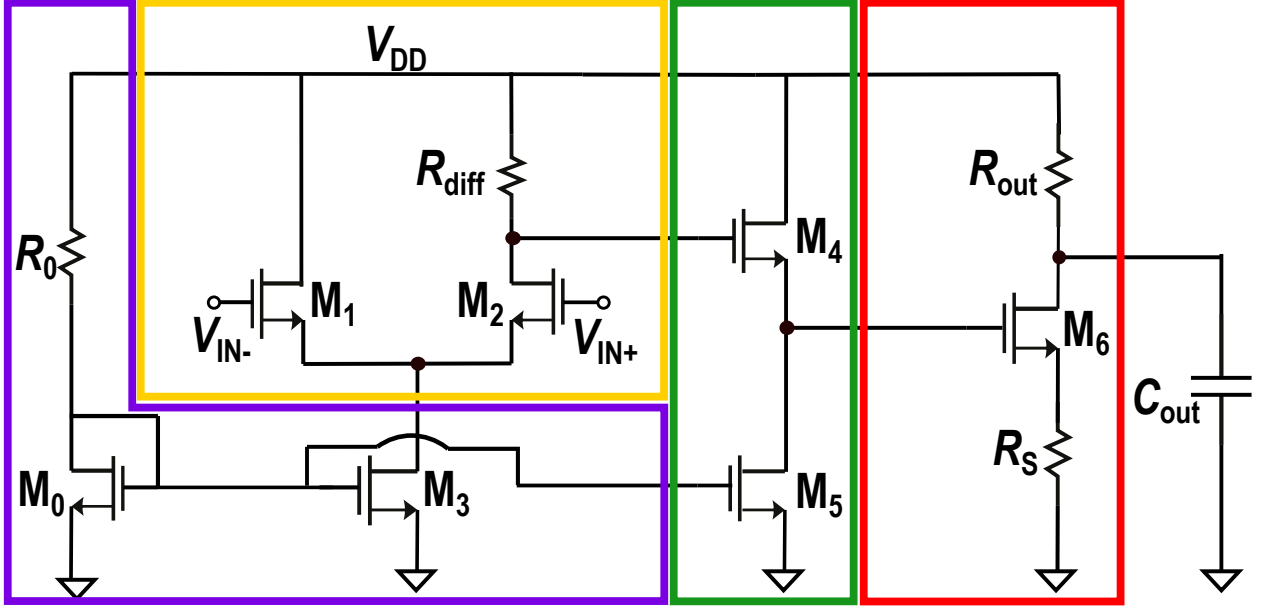


Figure 3.1: two stage differential analog OTA

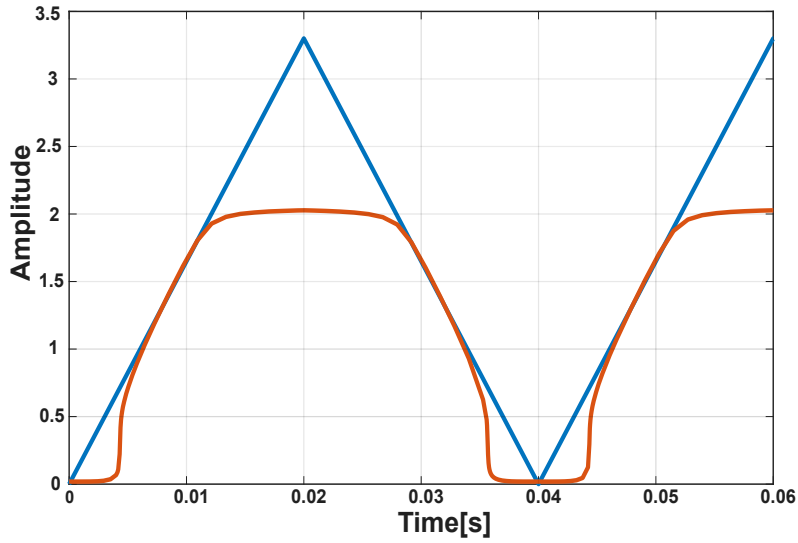


Figure 3.2: performance range of the analog OTA

Small signal analysis

Ensuring all transistors are in the saturation and design of the circuit is complete, considering the threshold voltage $V_{th} = 437 \text{ mV}$ and $\gamma = 221 \text{ m}$ from the Progmatic design Kit, small signal model of A-OTA is presented below.

Constant values of the circuit include:

$$R_{diff} = 477 \text{ K}\Omega, R_s = 14 \text{ k}\Omega, R_{out} = 5 \text{ M}\Omega, C_{out} = 50 \text{ pF}$$

Parameters for each transistor have been evaluated from DC simulation.

These parameters are reported in the table below:

Taking into account the load capacitance and the equivalent resistor seen from the

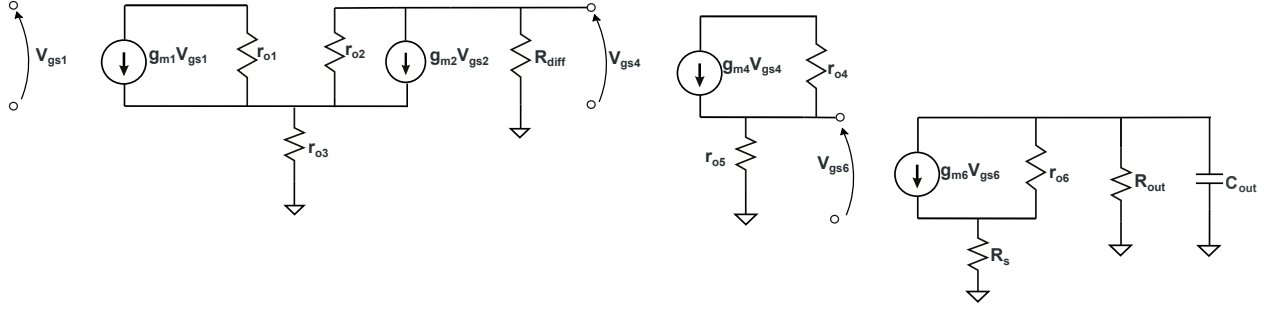


Figure 3.3: Equivalent small signal of the mentioned circuit

Transistor	r_o	g_m
M2	563k	24.34μ
M4	1.28M	25.4μ
M5	137k	17μ
M6	25M	3.86μ

load, calculation of the open-loop gain and the dominant pole is as follows:

$$\begin{aligned}
 A_d &= V_{out}/V_d = R_{out} \times (r_{o4} || r_{o5}) \times (g_{m6}/(1 + g_{m6} * R_s)) \times .. \\
 &\quad (g_{m4}/(1 + g_{m4} * r_{o5})) \times (R_{diff} || r_{o2}) * g_{m2} = 92.2 = 37.8dB. \\
 R_{eq} &= R_{out} || (R_s + r_{o6}(1 + g_{m6} R_s)) = 4.16M\Omega \\
 p_1 &= -1/R_{eq} \times C_{out} = -w_{p1} = 4.8kHz \\
 GBW &= A_d \times f_{p1} = A_d \times (w_{p1}/2 * \pi) = 59kHz \quad (3.1)
 \end{aligned}$$

Layout

The layout of A-OTA designed in flexible technology is seen in Fig. 3.4 with a total area of $42624\mu m^2$. As it is indicated in the layout, every stage is outlined in a color. It's worth mentioning that the largest area which is occupied by differential pair, also includes the dummy transistors.

The Calibre DRC and LVS tests have been done on the layout to check the design rules verification and the equality of the schematic and the layout of A-OTA circuit respectively.

Afterwards, to get ready for the post-layout simulations, the Calibre PEX test has been done to make a more realistic model of the circuit based on physical-structural properties, by adding parasitic components.

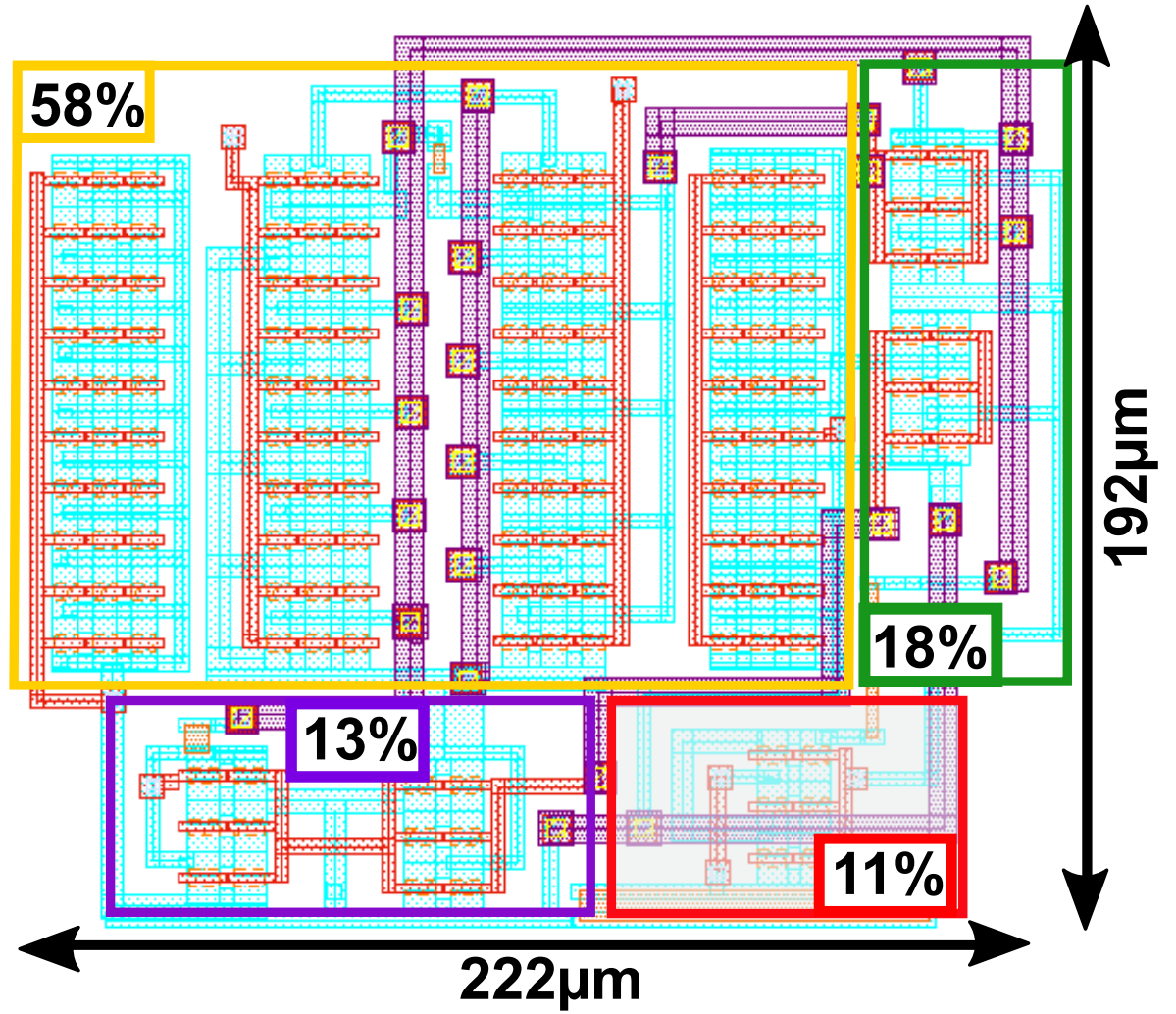


Figure 3.4: Layout of the A-OTA in flexible technology.

Post layout simulation results

The results have been obtained by performing cadence simulations on the Progmatic [19] nominal model libraries for 800nm IGZO TFT technology.

1. Time domain input and output.

Time domain input and output waveforms of the A-OTA in voltage-follower configuration with $V_{DD} = 3.3V$, with a 10Hz, 400mV sine wave input (corresponding to 80% of the amplifier input swing), 1.45V DC voltage (operating point in middle of the input voltage range) and $C_{out} = 50pF$ capacitive load. As expected from the configuration, output and input signals are quite identical or in other words the output has followed the input.

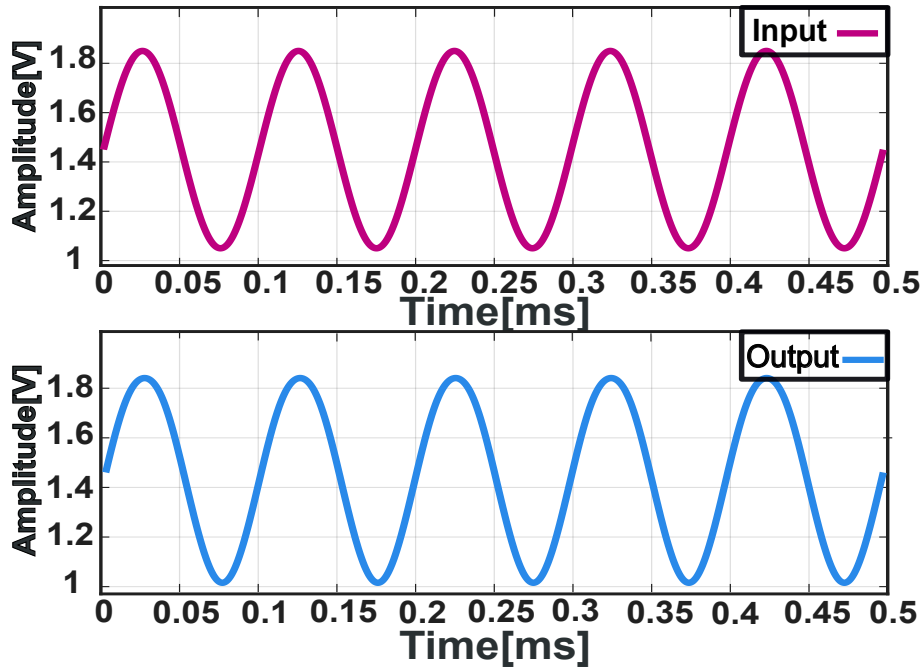


Figure 3.5: Simulated input and output voltages in voltage-follower configuration of A-OTA.

2. Phase and magnitude of the open-loop gain.

The frequency response of A-OTA has been evaluated in AC analysis and the ratio of $A_d(f) = \frac{V_{out}(f)}{V_{d(f)}}$ has been plotted in magnitude and phase, Fig.3.6.

Maximum open-loop gain is calculated from the simulation results 34.4 dB, it is almost coherent with the small signal gain calculation 37dB.

Limiting factors to mention are absence of pMOS transistor in pull-up circuit of all stages which reduces the gain value. Phase margin is equal to 88° which is adequate for a stable system.

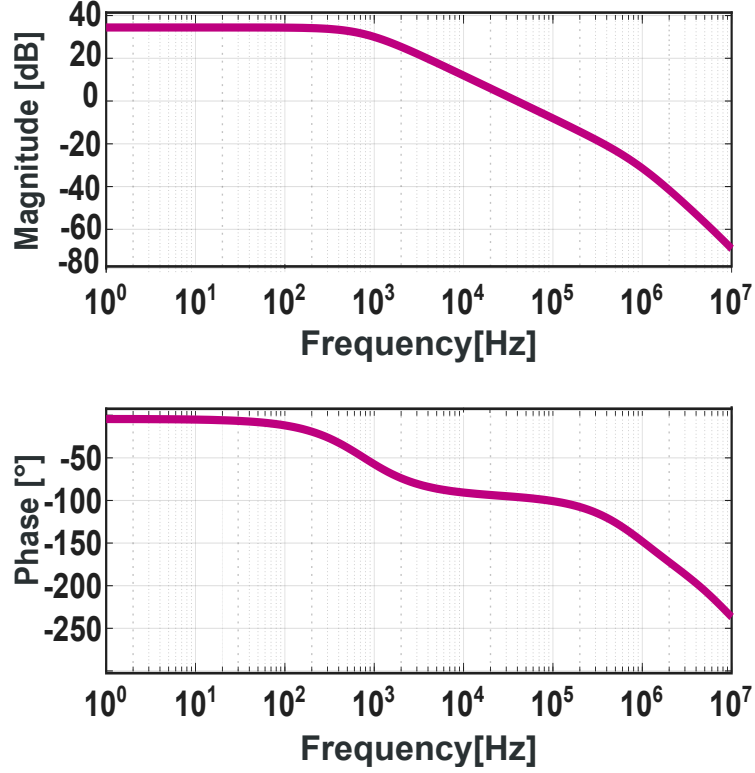


Figure 3.6: Simulated amplitude and phase of A-OTA Open-loop.

3. Phase and magnitude of the closed-loop gain.

The ratio of $A_v(f) = \frac{V_{out}(f)}{V_{in}(f)}$ is calculated with AC analysis for A-OTA. The frequency at which magnitude of closed-loop gain (Fig.3.7) reaches to -3 dB or GBW is approximately 39 kHz, this value is smaller with respect to the small signal GBW calculation 59 kHz, due to the fact that simulation is done after parasitic extraction so with a higher equivalent resistor and as a result a smaller dominant pole.

4. THD vs amplitude sweep.

The THD is simulated under a 10 Hz frequency sine wave and a 1.5 V DC input. It can be observed in Fig.3.8 that the THD increases monotonically with the amplitude. It's value at 100 mV is approximately 0.94 % which is as expected below one percent.

5. Slew-rate.

Time-domain input and output waveforms of A-OTA in voltage-follower configuration, with a $900 \mu\text{s}$ period square wave input have been plotted. Two values of positive and negative slew-rate have been measured by the derivative of simulated output signal (Fig.3.9) at rise and fall slope, the average of these two values is reported as the slew-rate of DB-OTA.

The negative slew-rate calculated for the A-OTA is -211.7 V/ms and the positive equals 13 V/ms which is consistent with the approximation $2\pi fV$, 12.56 V/ms . To avoid output signal limitation by the slew rate, amplitude of

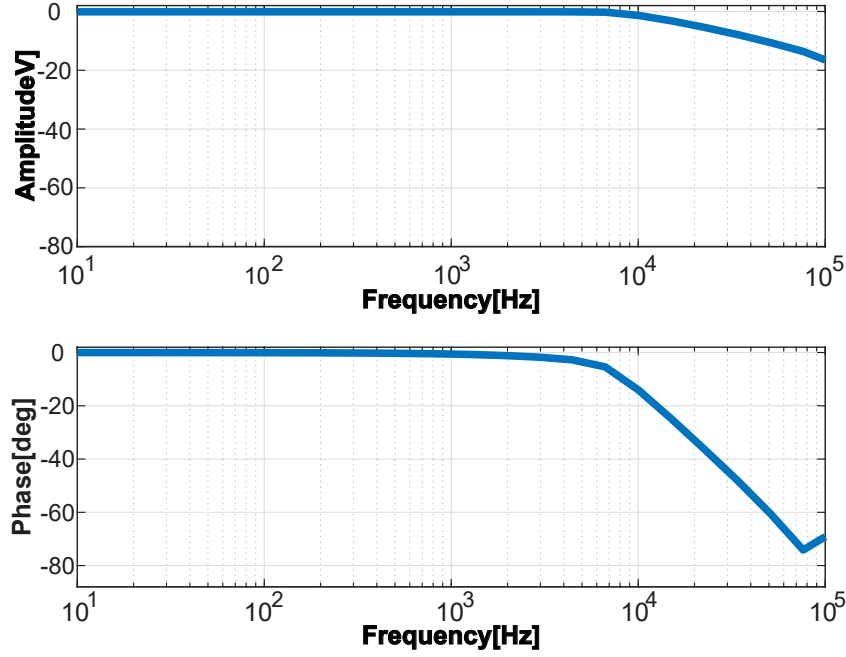


Figure 3.7: Simulated amplitude and phase of A-OTA closed-loop.

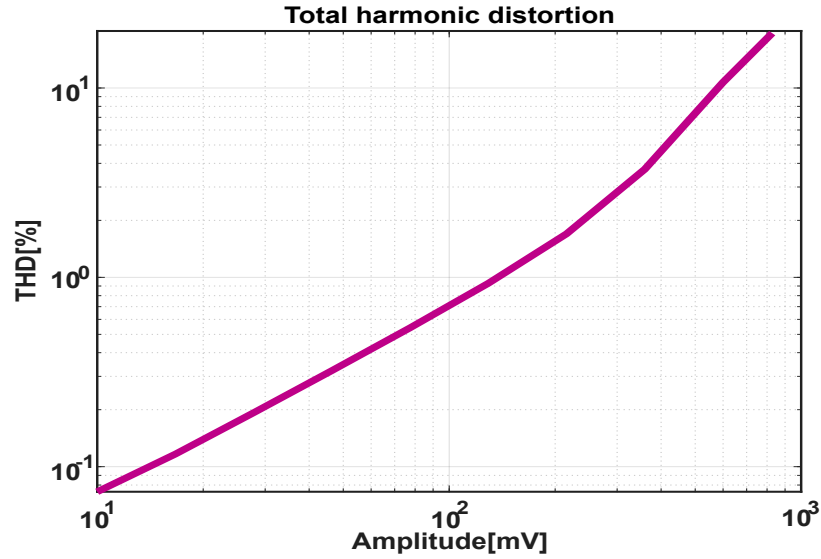


Figure 3.8: THD vs amplitude of A-OTA.

input signal is controlled. Higher value of slew-rate, means higher capability of the circuit against slew-rate limitation.

6. Input noise spectral density

It is obtained by AC noise analysis, applying a DC voltage as input signal of the circuit, in a process including fast Fourier transform of the output noise, noise power spectral density is obtained which is the noise power per unit of bandwidth. The RMS noise is $8.8 \mu\text{V}_{\text{RMS}}$, It can be observed that the thermal

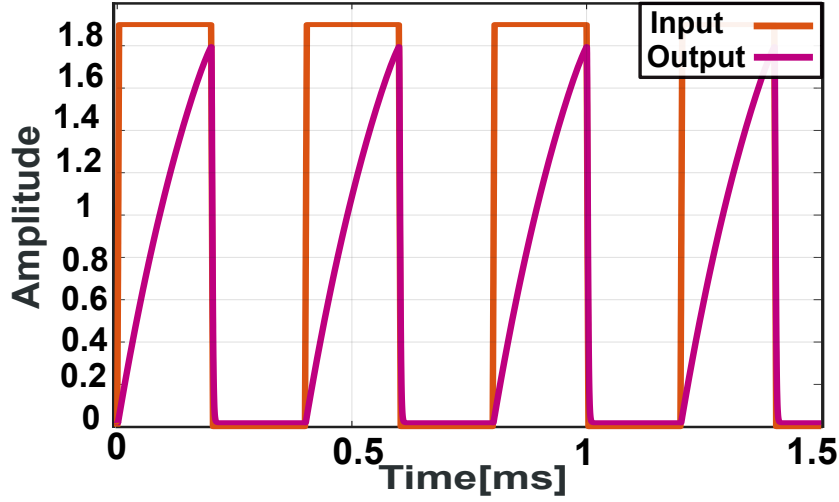


Figure 3.9: Simulated output and input of A-OTA for a square wave input.

noise (white noise) is shaped by the transfer function of the amplifier.

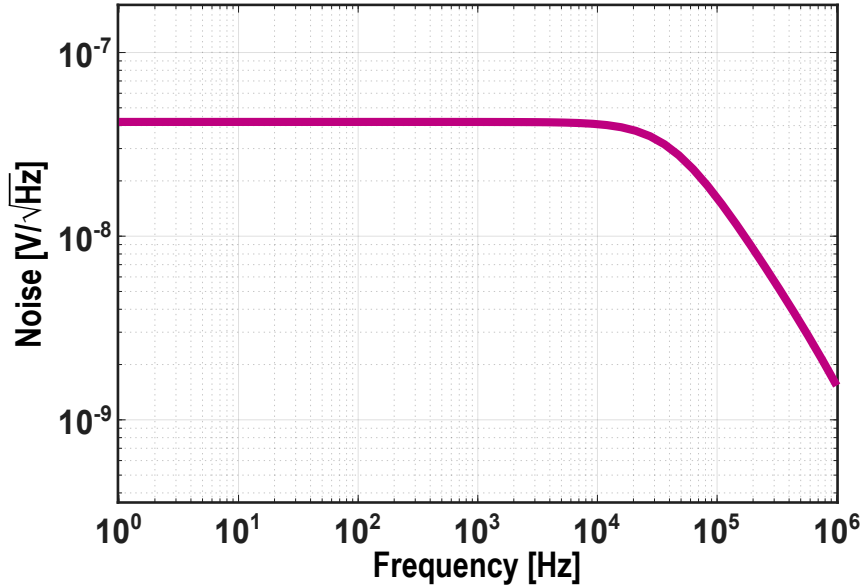


Figure 3.10: Noise spectral density of A-OTA.

7. **CMRR and PSRR** In order to calculate CMRR for A-OTA, instead of the voltage-follower configuration, v_+ and v_- are simply connected together to the input signal. A-OTA CMRR is evaluated as the ratio of differential voltage gain 34.4dB and the common-mode voltage gain -25dB, equal to 59dB.

To measure PSRR, the voltage signal is applied to V_{DD} and only a DC voltage is employed to the input for biasing, the ratio of power supply alteration to output is calculated 29dB by AC analysis.

Monte Carlo simulation results

To evaluate the effect of mismatch variations, Monte Carlo analysis has been applied on 100 samples in nominal temperature. Following parameters have been evaluated:

1. DC gain distribution.

The histogram of Monte Carlo analysis for DC gain Fig.3.11 has a mean value of 35.2 dB and a standard deviation equal to 4.1 dB. Pointing out that considering different possible values for DC gain, with their likelihood of occurrence, the mean of them is very close to 34.4 dB value obtained from post-layout simulation.

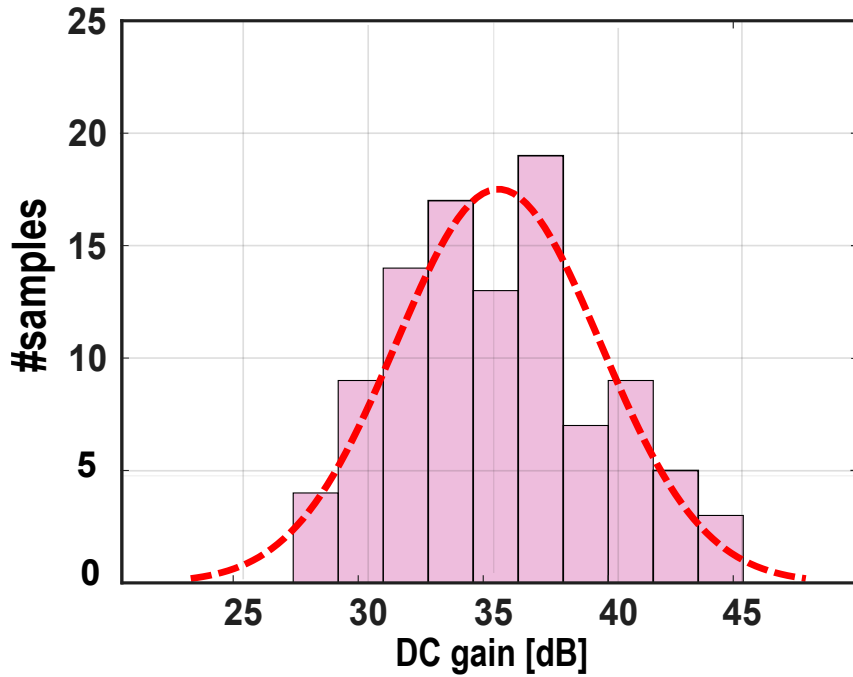


Figure 3.11: Monte Carlo of DC gain distribution for A-OTA

2. Voltage offset distribution.

The distribution of Monte Carlo analysis for voltage offset has a mean value of -0.07 mV and a standard deviation equal to 22.3 mV. Shown in Fig.3.12, although range of the offset reaches up to 50 mV, since the highest probability of happening are for values around zero, the mean value is adequate.

3. Power consumption distribution.

Since A-OTA since is an AC circuit, power consumption is evaluated by DC simulation. As it is shown in Fig.3.13, the histogram of MC analysis for power consumption has a mean value of $90 \mu\text{W}$ and a standard deviation equal to $14.77 \mu\text{W}$. The result is consistent with the value obtained by post layout simulation $91.1 \mu\text{W}$.

4. GBW distribution.

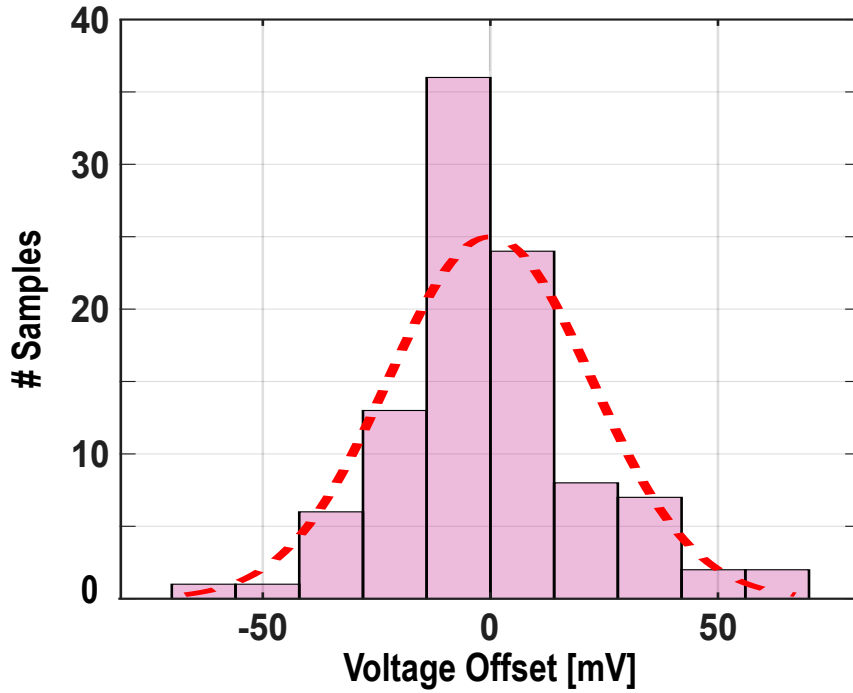


Figure 3.12: Monte Carlo of Voltage Offset distribution for A-OTA

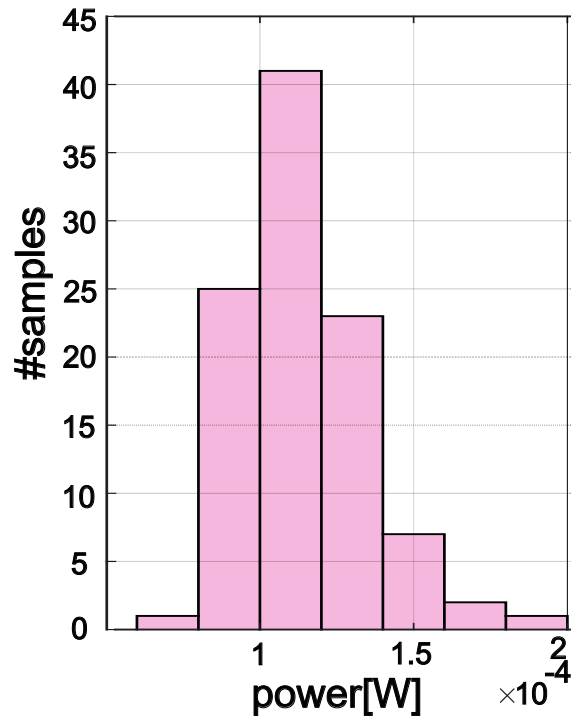


Figure 3.13: Monte Carlo of power consumption distribution for A-OTA

The mean value for this distribution is 57.8 kHz which is consistent to the small signal calculation of the GBW 59 kHz and the standard deviation equals to 31.9 kHz. As it is displayed in the Figure below, maximum probability of occurrence for GBW is almost equal to 38 kHz which is equal

to the value evaluated by post-layout simulation 39kHz.

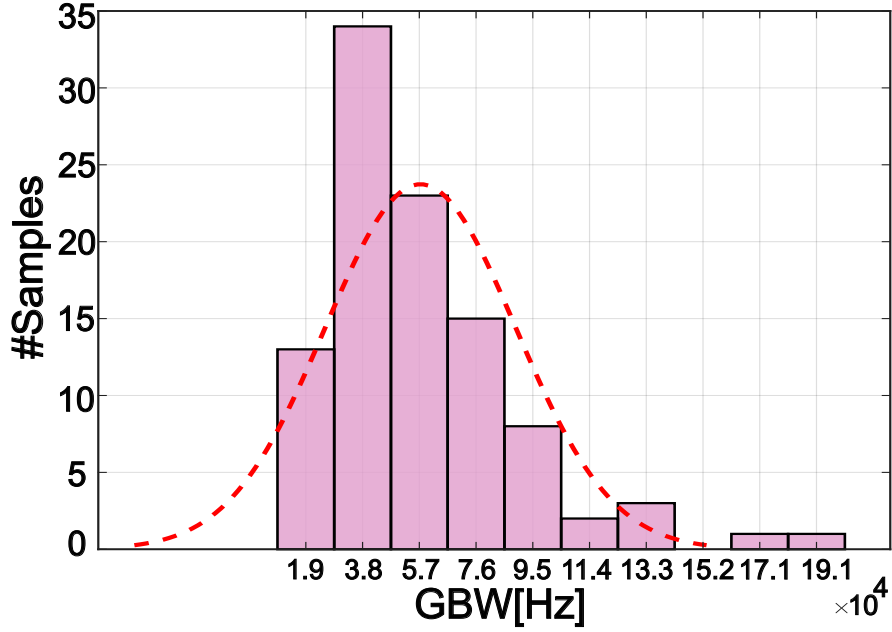


Figure 3.14: Monte Carlo of GBW distribution for A-OTA

5. Slew-rate distribution

Since positive slew-rate is negligible with respect to negative, only the negative one is calculated in MC analysis. The mean value of this distribution is -252.4 V/ms and the standard deviation equals to 11.8 V/ms. This distribution and its mean value are approximately consistent with the negative slew-rate obtained in the typical post-layout simulation -211.7 V/ms.

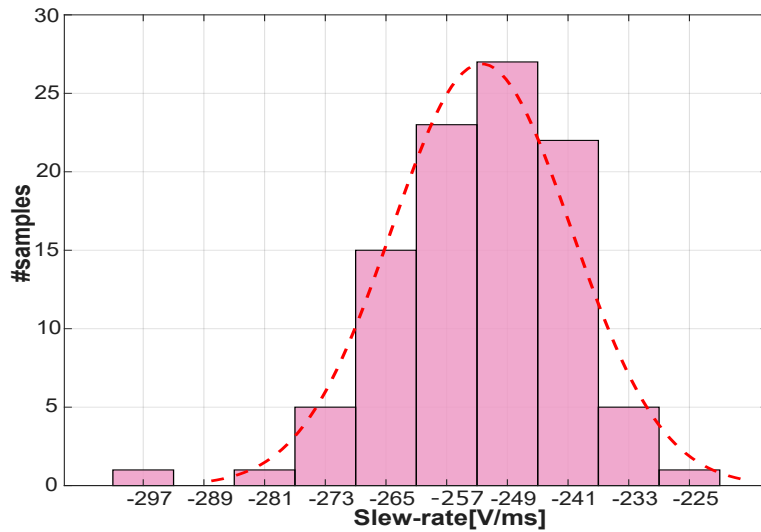


Figure 3.15: Monte-Carlo negative slew-rate distribution of A-OTA

Chapter 4

Digital-based OTA in flexible technology design, simulation and post layout verification

In this chapter analysis of a digital based differential circuit is reviewed and based on that, design of a digital based OTA (DIGOTA) is discussed. Followed by design of the same circuit in flexible technology, its analysis and required modifications due to the differences between the two technologies. Afterwards, layout of complete digital based OTA in flexible technology is provided. Eventually, post-layout and Monte Carlo simulation results are presented.

Differential circuit

From [8], an analog differential circuit has an output related to the difference of the two inputs or to the differential mode (DM) input $v_D = v_{IN+} - v_{IN-}$, and it is not influenced by the absolute value of input voltages with respect to the reference voltage (0V), in other words, it is insensitive to the common-mode (CM) voltage v_{CM} .

In Fig.4.1, Common mode input voltage (v_{CM}) is rejected by the biasing current sink and the differential voltage is provided by the input pair, if this voltage is greater than zero, output voltage will increase and if its smaller, it will decrease. For an analog differential pair, inputs in relation to the differential-mode (DM) and CM are defined as : $v_{IN-} = v_{CM} - v_D/2$ and $v_{IN+} = v_{CM} + v_D/2$. The DM and CM inputs can be defined in relation to the two inputs as: $v_{CM} = (v_{IN+} + v_{IN-})/2$ and $v_D = (v_{IN+} - v_{IN-})/2$. CM voltage gain, the ratio between output voltage and the CM input voltage, is defined as $A_c(f) = \frac{V_{out}(f)}{V_{cm}(f)}$.

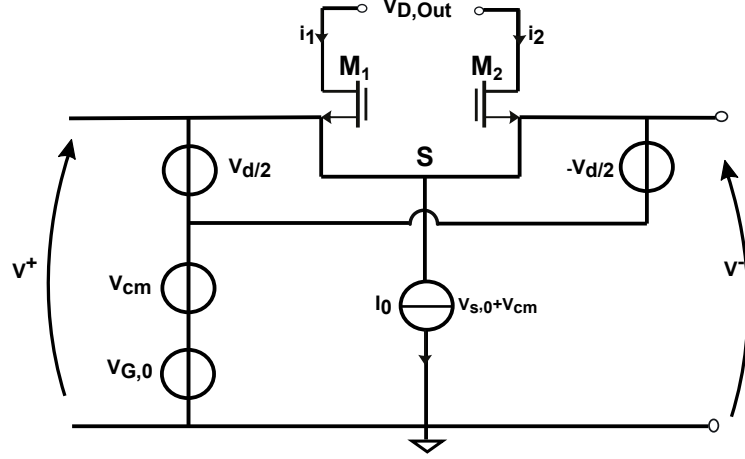


Figure 4.1: Classical analog differential pair

Two digital buffers as a differential circuit

From [8], applying the analog inputs to a pair of ideal digital buffers, a differential pair is build. Ideal in the sense that a high digital output $OUT = "1"$ ($V_{OUT} = V_{OH} > V_T$) is provided by the buffer if $v_{IN} > V_T$ and vice versa as shown in Fig. 4.3. Depending on the input signals v_{IN+} and v_{IN-} , it can be observed that the outputs of the circuit ($OUT+$, $OUT-$) are related to the DM input voltage as a differential circuit, from [22].

$$(OUT+, OUT-) = \begin{cases} (1, 0), & \text{if } v_{IN+} > V_T \wedge v_{IN-} < V_T \rightarrow v_D > 0 \\ (0, 1), & \text{if } v_{IN+} < V_T \wedge v_{IN-} > V_T \rightarrow v_D < 0 \end{cases} \quad (4.1)$$

Also configurations $(v_{IN+} < V_T \wedge v_{IN-} < V_T)$ and $(v_{IN+} > V_T \wedge v_{IN-} > V_T)$ are possible with outputs equal to $(OUT+, OUT-) = (0, 0)$ and $(OUT+, OUT-) = (1, 1)$ respectively. These two latter cases provide some information on the CM input voltage.

$$v_{CM} \begin{cases} > V_T, & \text{if } v_{IN+} > V_T \wedge v_{IN-} > V_T \rightarrow v_{IN+} + v_{IN-} > 2V_T \\ < V_T, & \text{if } v_{IN+} < V_T \wedge v_{IN-} < V_T \rightarrow v_{IN+} + v_{IN-} < 2V_T \end{cases} \quad (4.2)$$

This analysis is provided in conclusion in the table of Fig. 4.3.

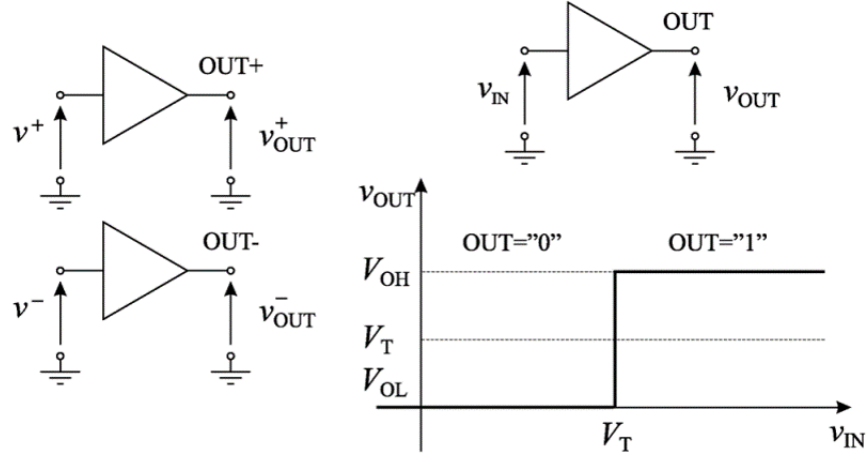


Figure 4.2: A pair of single-ended digital buffers as a digital differential stage (left) and input/output characteristic of each digital buffer(right), source [8]

DM AMPLIFIER OUTPUT							
OUT+	OUT-	OUT+	OUT-	OUT+	OUT-	OUT+	OUT-
1	1	0	0	1	0	0	1
V_{IN+}	V_{IN-}			V_{IN+}			V_{IN-}
		V_{IN-}	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN+}	V_{IN-}
$V_{CM} > V_T$		$V_{CM} < V_T$		$v_D > 0$		$v_D < 0$	

Figure 4.3: Summary of a two-buffer differential circuit performance, source [8]

4.1 Digital based OTA

To carry out the analysis of digital-based OTA (DB-OTA) shown in fig.4.4 a review of the differential pair operation was done earlier. For the digital-based differential amplifier, the idea of common-mode voltage compensation is designed by negative feedback employment. The DB-OTA in voltage follower in Fig.4.4 from [8], is made of four stages: differential mode amplifier, summing network, common mode extractor including a three-state inverter loaded by a capacitor C_{CMP} and output stage.

It can be seen in Fig.4.4 that the CM compensation signal v_{CMP} is added to the external input voltages through the summing network to keep the CM input voltage close to V_T , [23]. Actual (internal) inputs of the digital buffers are expressed as:

$v'_{IN+} = \frac{v_{IN+} + v_{CMP}}{2}$ and $v'_{IN-} = \frac{v_{IN-} + v_{CMP}}{2}$ and the internal DM and CM are related to external components as: $v'_{CM} = \frac{v_{CM} + v_{CMP}}{2}$ and $v'_D = v_{CMP}/2$.

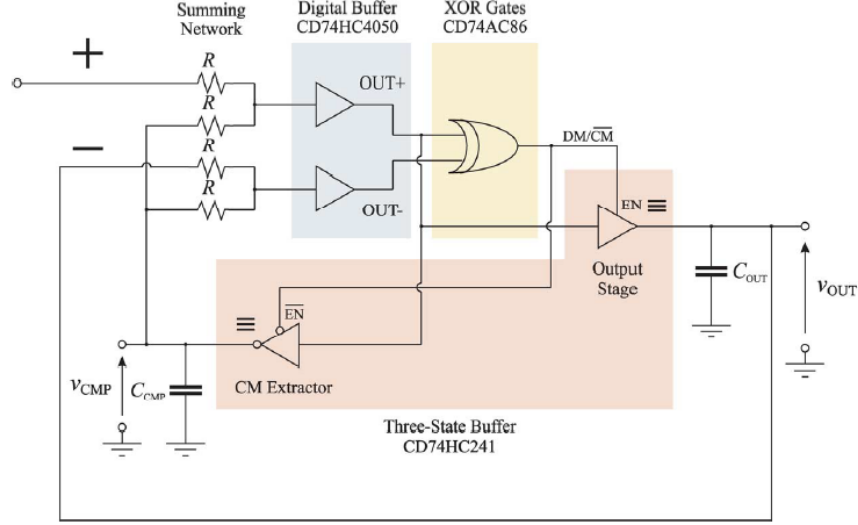


Figure 4.4: Digital-based differential circuit in voltage-follower configuration, source [8]

In case of $(OUT+, OUT-) = (1, 0)$, as the outputs of digital buffer pair, XOR gate will have a logic "1" as output and out voltage v_{out} will increase by its pull-up transistor turning on. In opposite, when $(OUT+, OUT-) = (0, 1)$ output voltage will reduce, since the pull-down transistor of the output stage turns on. In two other cases of $(OUT+, OUT-) = (0, 0)$ and $(1, 1)$ instead, the output is constant while the common mode extractor will increase or decrease the common mode compensation voltage, source [24].

The operational transconductance amplifier connected in negative feedback is employed directly as a voltage follower or a non-inverting voltage amplifier [25], for this purpose the output is connected to the inverting input terminal by a voltage divider so $v_{IN-} = [R_1/(R_1 + R_2)]v_{out} = \beta v_{out}$ and an external input voltage v_{IN} is applied to non-inverting input of the op-amp. In this case the internal inputs can be expressed as: $v'_{IN+}(t) = \frac{v_{IN}(t) + v_{CMP}(t)}{2}$ and $v'_{IN-}(t) = \frac{\beta v_{out}(t) + v_{CMP}(t)}{2}$, for the unity feedback system or voltage-follower, β is equal to one.

To better understand the performance of the circuit in Fig.4.4 and analyse its simulated waveform in Fig.4.9a, first, the mathematical model of the digital-based differential circuit is considered (source[8]):

The state variables v_{OUT} and v_{CMP} can be expressed in terms of external inputs by the following equation:

$$\begin{cases} \frac{\partial v_{OUT}}{\partial x_i} = \frac{i_{OUT}}{C_{OUT}} \\ \frac{\partial v_{CMP}}{\partial t} = \frac{i_{CMP}}{C_{CMP}} \end{cases} \quad (4.3)$$

where

$$i_{OUT}(t) = \begin{cases} i_{P,OUT} & \text{if } v'_{IN+}(t') > V_T \wedge v'_{IN-}(t') < V_T \\ i_{N,OUT} & \text{if } v'_{IN+}(t') < V_T \wedge v'_{IN-}(t') > V_T \\ 0 & \text{otherwise} \end{cases} \quad (4.4)$$

$$i_{\text{CMP}}(t) = \begin{cases} i_{\text{P,CMP}} & \text{if } v'_{\text{IN}+}(t'') < V_T \wedge v'_{\text{IN}-}(t'') < V_T \\ i_{\text{N,CMP}} & \text{if } v'_{\text{IN}+}(t'') > V_T \wedge v'_{\text{IN}-}(t'') > V_T \\ 0 & \text{otherwise} \end{cases} \quad (4.5)$$

where

$$t' = t_{\text{D,CMP}}, \quad t'' = t - t_{\text{D,out}} \quad (4.6)$$

That indicate 50% propagation delay from the input of digital buffers to the gate voltages of transistors in the output or the CM extractor.

The reason behind the triangular shape of v'_{CM} is the time delay of digital gates in CM extractor stage that causes the v_{CMP} to increase or decrease with some delay. For a varying external input, when the external input signal v_{IN} starts increasing, $v'_{\text{IN}-}$ crosses the threshold a time t'_{D} after $v'_{\text{IN}+}$, so that $v'_{\text{IN}+} > 0$ and $v'_{\text{IN}-} < 0$. After a time t_{D} from $v'_{\text{IN}-}$ zero crossing, output voltage will increase for a t'_{D} time interval. The net increment of v_{out} after t'_{D} corresponds to an overall reduction of $v_{\text{D}} = v_{\text{IN}} - \beta v_{\text{out}}$.

Figure 4.4 only exhibits the case of varying external input signal. According to these waveforms, output signal is constant most of the time and only increases in short pulses, in other words, the CM extractor stage is active much more than the output stage.

4.2 Logic gates design

Main challenge in making high gain-bandwidth amplifiers is designing the high-side subcircuit. Several solutions have been proposed for unipolar analog design; such as resistive load, diode-connected nMOS load, positive feedback based circuit and pseudo-CMOS which is a variant of positive feedback.

The resistive load is chosen for the design of DB-OTA in flexible technology because of its straightforward application beside the fact that other solutions did not have any particular advantage with respect to it.

First step to design DB-OTA in flexible technology is to transfer necessary logic gates commonly known in CMOS in this technology. Nor and inverter are chosen since they require few number of transistors and resistors to be built comparing to other gates, Fig.4.5.

After substitution of the p-type transistor with a resistor, it must be taken into account that this way the pull-up resistor is always functioning.

When output stage is not active in (OUT+, OUT-) = (0,0) and (1,1) cases, it's expected that v_{out} stays constant but due to the pull-up resistor, a RC network is created and output voltage will exponentially rise to V_{DD} . This fact causes a triangular waveform to be superimposed to the output voltage of the amplifier. In figure 4.9a the output voltage appears as a stair case since in the original circuit a pMOS transistor is applied as the pull-up network that can be off and keep v_{out} constant.

Minimum possible width and length for the flexible technology are respectively $10\ \mu\text{m}$ and 800nm , same values are employed in the design of Nor and Inverter gates.

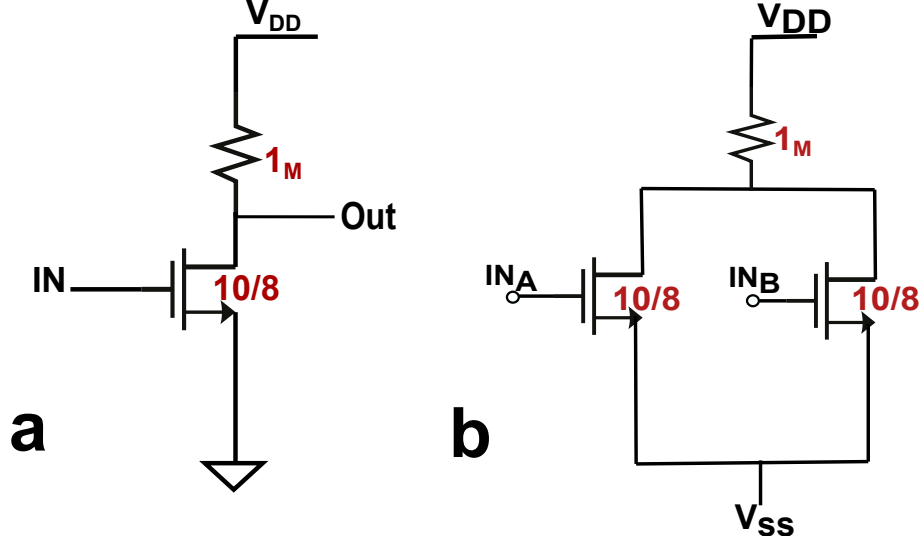


Figure 4.5: Schematic of Inverter (a) and Nor gate (b) designed in flexible technology

4.3 Architecture of final design

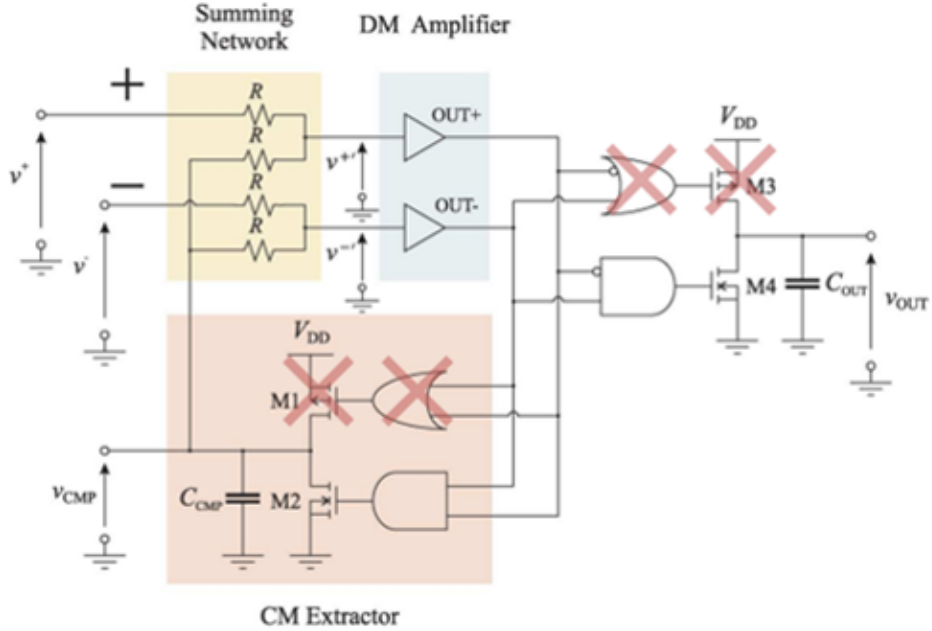


Figure 4.6: complete DIGOTA circuit from [8] paper

The schematic of digital-based OTA in flexible technology can be seen in figure 4.7. The reference circuit of digital OTA shown in figure 4.6 has been revised for

design in flexible technology. Since the pull-up is done by a resistor in this design, the logic gates which were used to drive the pull-up transistors are omitted. As mentioned earlier, logic gates used in the DB-OTA circuit have been redesigned only with n-type transistors.

To make the circuit easier to understand, Nor and inverter gates are drawn in their symbols. Operation of the circuit relies on the logical output of chain of cascaded inverters with trip point V_T . At least six inverters are required to have a reasonably high voltage gain. In order to reduce voltage offset, delay of the last inverter in the chain is avoided by connecting output of the inverter before the last one as the input of the nor gate in output stage.

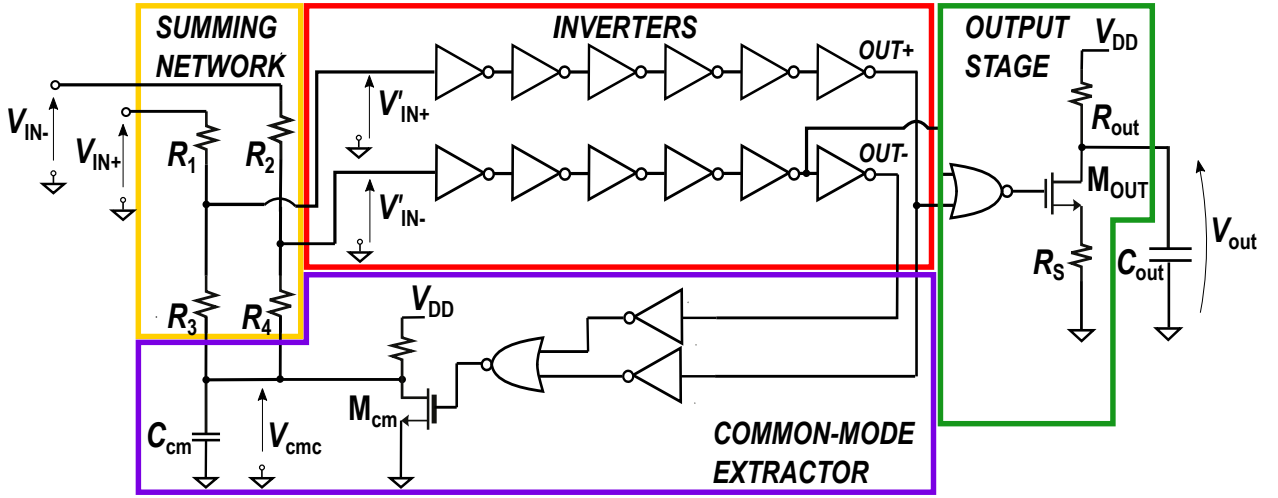


Figure 4.7: Schematic of Digital based OTA designed in flexible technology

It's essential to have resistors of input summing network of order of $M\Omega$ to reduce the loading effect both on voltage source and the feedback network, they have been designed so that $R_1 = R_2 > R_3 = R_4$ to accommodate for the lower trip point of nMOS logic with respect to the CMOS logic. The value of C_{cm} (R_{pu}) is chosen large (small) to keep the impedance of CM extractor network sufficiently low while introducing a limited area overhead, C_{cm} is 5 times smaller with respect to C_{out} . The transistor in common-mode extractor stage has a $7.8\mu m$ length which is so much larger with respect to the output stage $800nm$, while they both share a $10\mu m$ width, this results in a larger r_o for CM transistor which is meant for charge of the capacitance to be slowly discharged. Since $R_{pu} = 1 M\Omega$ and $C_{cm} = 10 pF$, together they create a time constant much smaller than the one of output stage, charge and discharge of the CM capacitor is much faster.

The source degeneration resistance in the output stage $R_s = 50k\Omega$ has been applied to reduce harmonic distortion of the circuit. Largest resistor is used in the output stage of value of $8M\Omega$ which helps with the gain while resistors in the summing network are all equal to $3M\Omega$ to have symmetric common mode input range with respect to the inverter trip point.

To consider the performance of the digital-based OTA connected in voltage-follower configuration in CMOS and flexible technology design, the waveforms in Fig.4.9a and 4.9b are compared. Including the inputs and outputs of

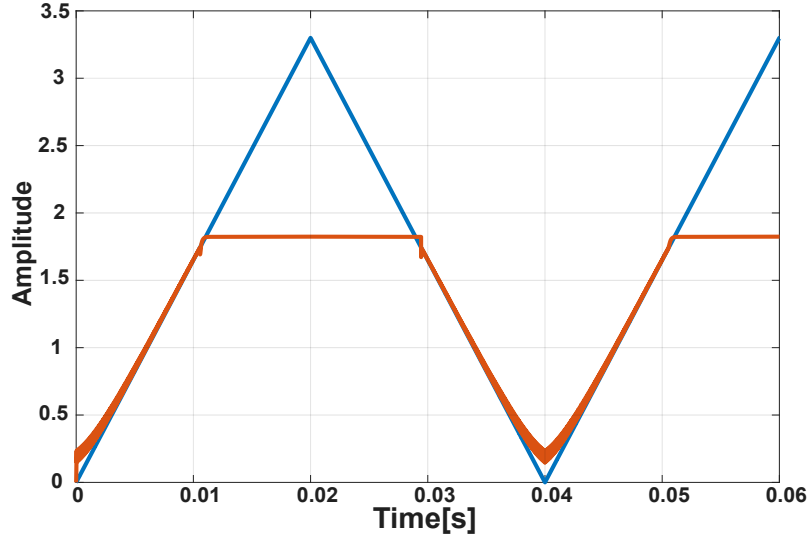


Figure 4.8: Input operating range of the circuit at Fig.4.7

buffers, common-mode voltage and output voltage of the DB-OTA circuit. First noticeable difference between the DIGOTA [8] and the flexible DB-OTA is the characteristic of the output ripple which is a staircase for DIGOTA (see Fig.4.9a) while it is triangular for DB-OTA. This is due to absence of pMOS transistor with respect to DIGOTA circuit. Outputs of inverter chains (OUT+, OUT-) are superimposed similar to DIGOTA waveforms however, they are narrower causing the (11) case to be shorter, this is due to faster discharge of the C_{cm} in summing network resistors with respect to DIGOTA.

Layout

In figure 4.10(a) layout of the inverter gate in flexible technology can be seen with a total width of $20\mu m$ and length of $20.3\mu m$. As well as the nor gate layout in flexible technology with $46.5\mu m$ width and $26.3\mu m$ length ,Fig.4.10 (b).

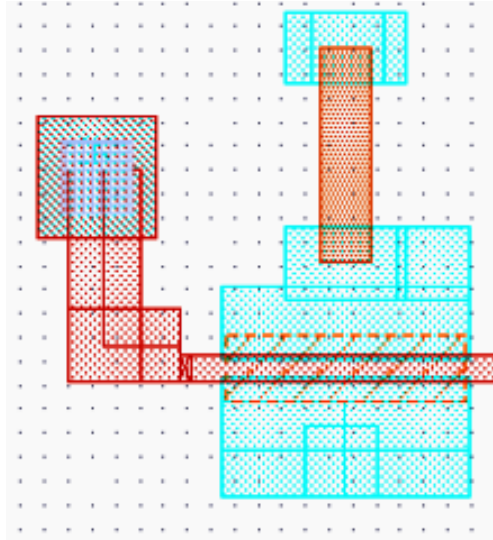
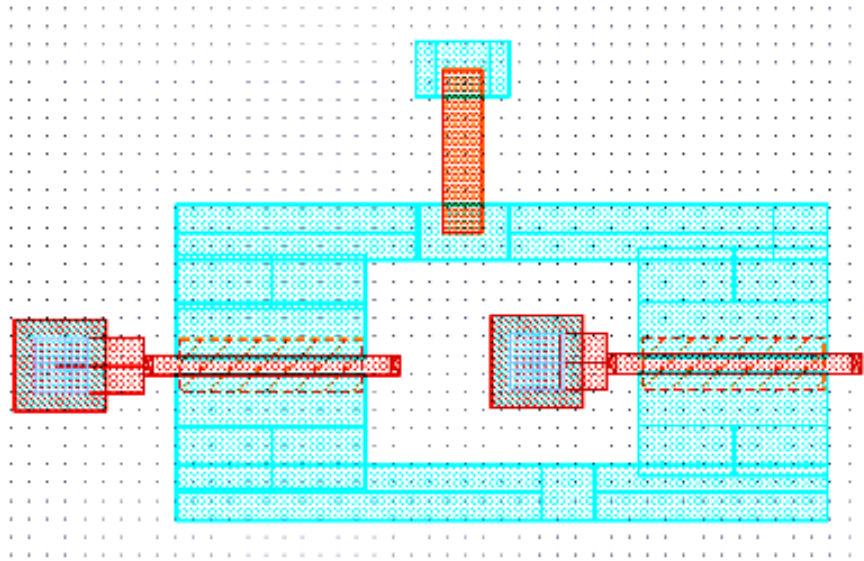
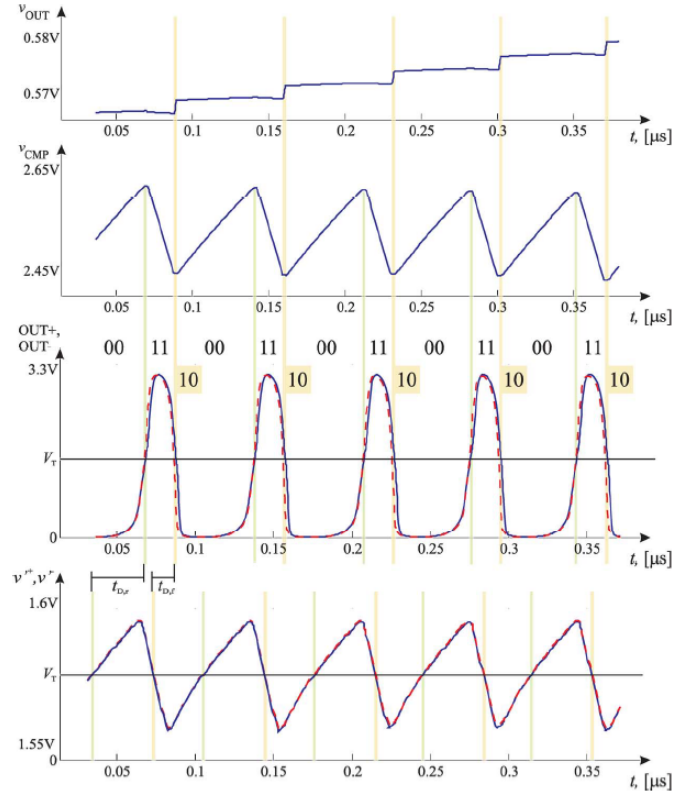
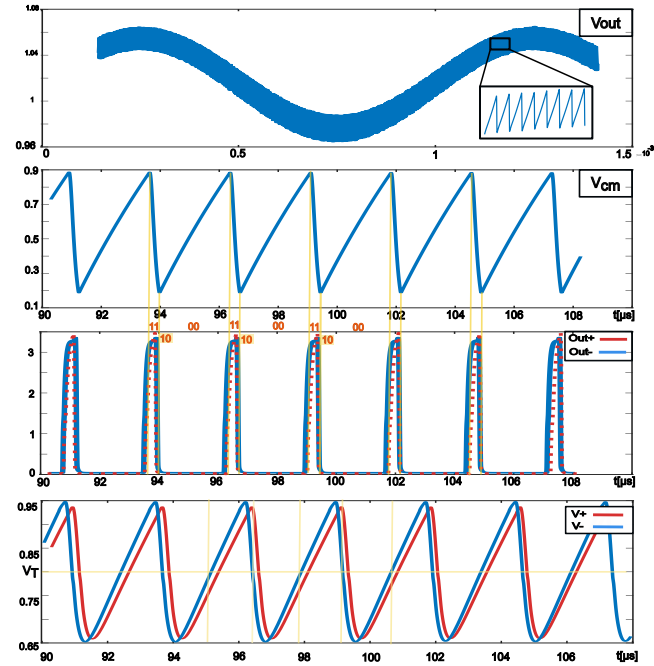
a**b**

Figure 4.10: Inverter(a) and Nor(b) gates designed in flexible technology



(a) Simulated waveform for digital-based opamp connected in voltage-follower [8]



(b) Simulated waveform for DB-OTA designed in flexible technology.

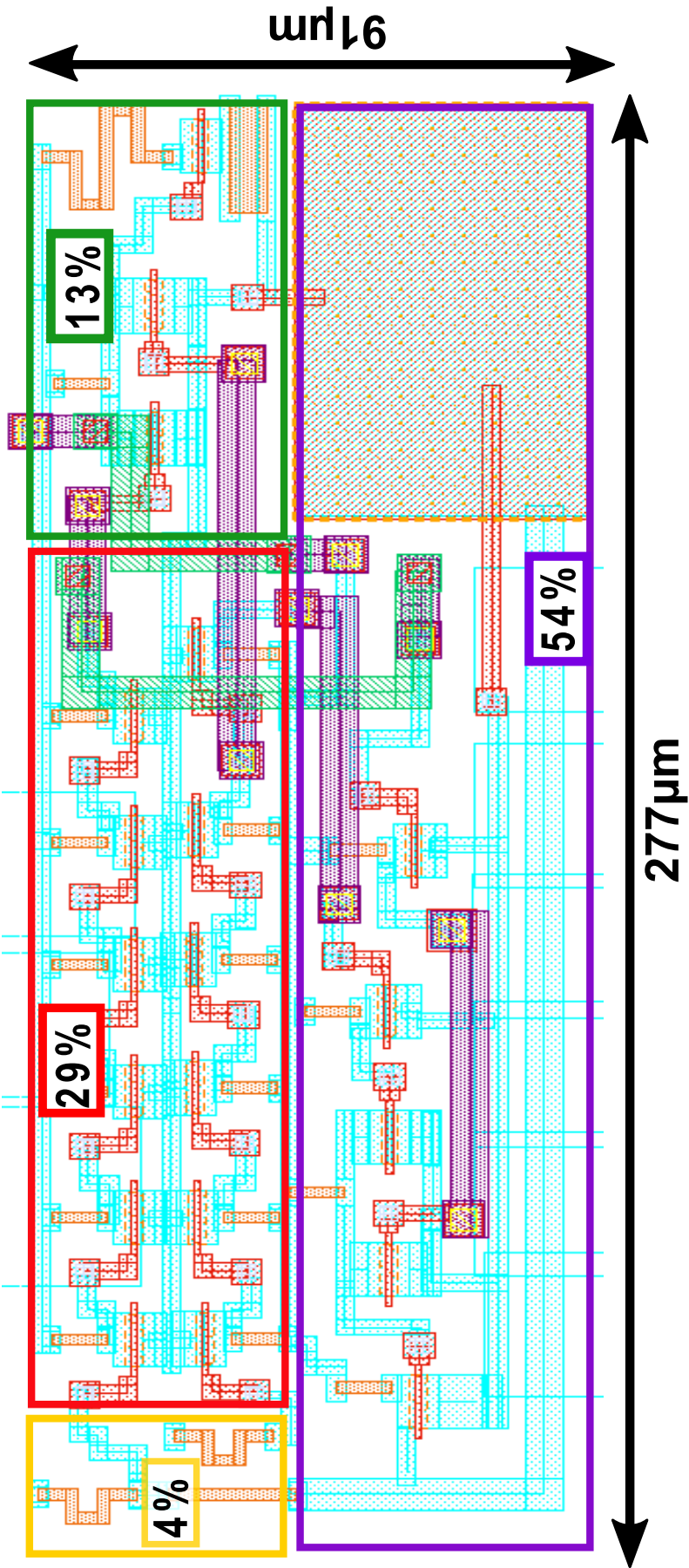


Figure 4.11: Complete layout of digital-based OTA.

The layout of full DB-OTA circuit designed in flexible technology can be seen above, with overall width of $277\ \mu\text{m}$ and the overall length of $91\ \mu\text{m}$. It is made of layers: semi, gate, res, metal1 and metal2. As it is indicated in Fig.4.11 the summing network occupies 4% of overall area, buffers together 29% , the output stage 13% and the common-mode extractor occupies 54% most of which is occupied by the CM capacitor in CM extractor stage, [26].

Post-layout results

The post-layout simulation results have been obtained using the PragmatIC [19] model libraries for 800nm IGZO TFT process [5], [27], [17] at room temperature.

1. Time domain input/output.

Time domain input and output waveforms of the DB-OTA in voltage-follower configuration with $V_{DD} = 3.3\text{V}$, a 10Hz, 400mV sine wave input (corresponding to 80% of the amplifier input swing), 1V DC voltage (operating point in middle of the input voltage range) and capacitive load $C_{out} = 50\text{pF}$ are exhibited at Fig.4.12. It can be noticed that the output waveform (in blue) shows an out-of-band ripple component (500kHz freq) resulting from its inherently digital components.

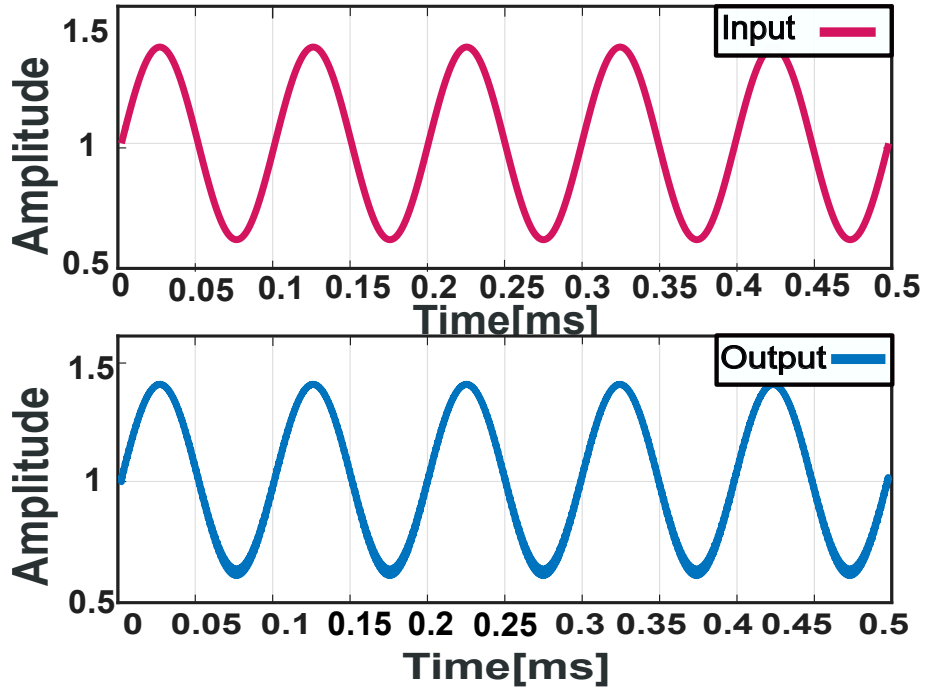


Figure 4.12: Simulated input and output voltages in voltage-follower configuration.

2. Phase and magnitude of the open-loop gain.

The frequency response of DB-OTA has been evaluated in transient analysis and then ratio of the fast Fourier transform (FFT) at the fundamental frequency of output voltage to the differential voltage $A_d(f) = \frac{V_{out}(f)}{V_d(f)}$ is calculated in magnitude and phase (Fig.4.13). The maximum value for the

DC gain is calculated **37.08dB** and phase margin is equal to **87°**. Limiting factors to consider are: absence of pMOS transistor in inverter gate circuit which would increase its gain, number of cascaded inverter gates, more gates helps with the open-loop gain, but on the other hand, bandwidth and the common-mode oscillation frequency will reduce.

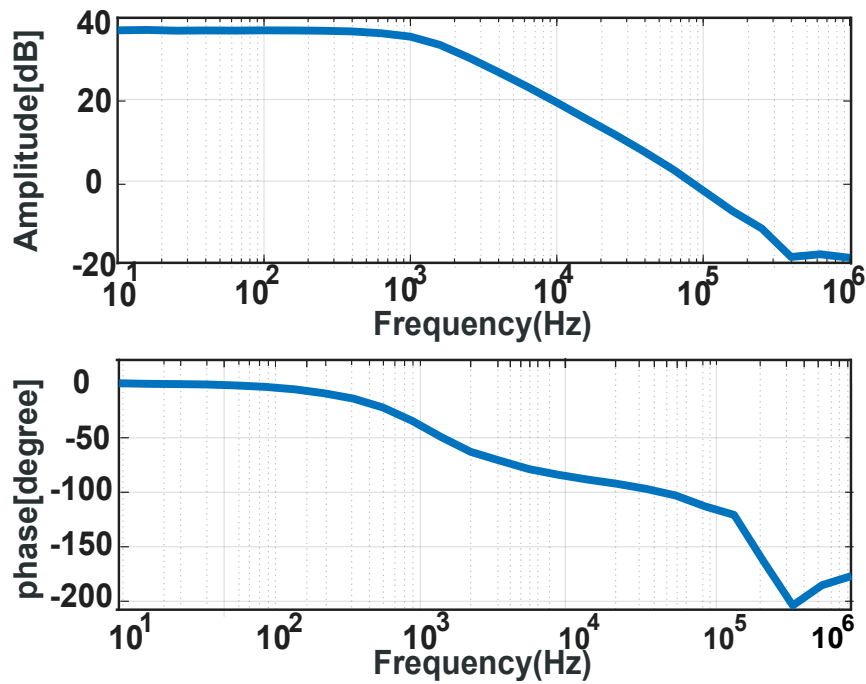


Figure 4.13: Simulated amplitude and phase of A-OTA open-loop.

3. Phase and magnitude of the closed-loop gain.

The closed loop gain or the ratio of ($A_v(f) = \frac{V_{out}(f)}{V_{in}(f)}$) is calculated by transient analysis and application of FFT, result is shown in the picture below. Typical GBW for DB-OTA equals to 76 kHz.

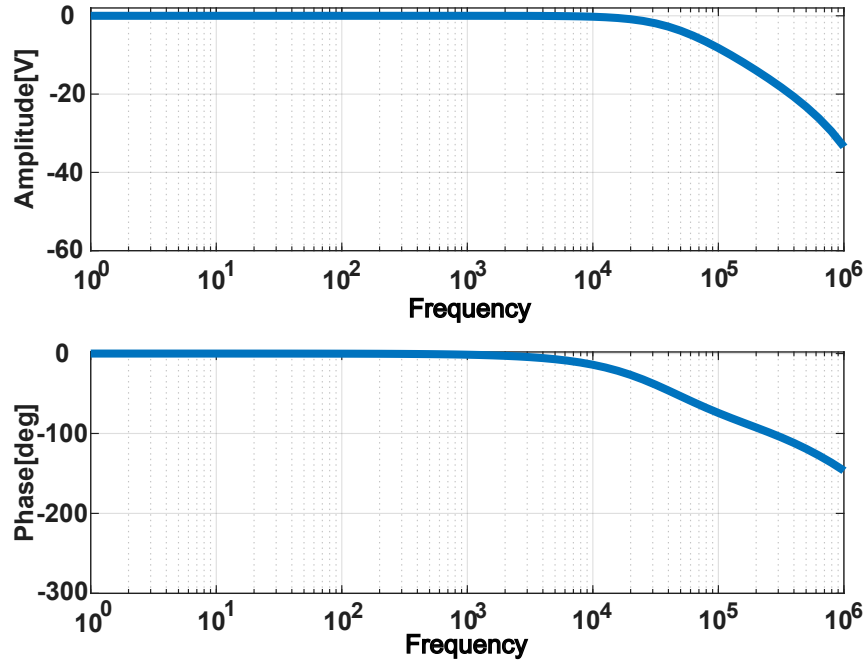


Figure 4.14: Simulated amplitude and phase of A-OTA closed-loop.

4. THD vs amplitude sweep.

The simulated total harmonic distortion of DB-OTA by transient analysis under 10Hz sinewave input excitation is plotted versus amplitude swing from [10-1000] mV. In Fig.4.15, despite the expectation, a higher THD is observed at lower input amplitude due to the "dead zone" effect highlighted in [24]. Total harmonic distortion for the DB-OTA is equal to 0.31% which is a significant result since below one percent is considered adequate.

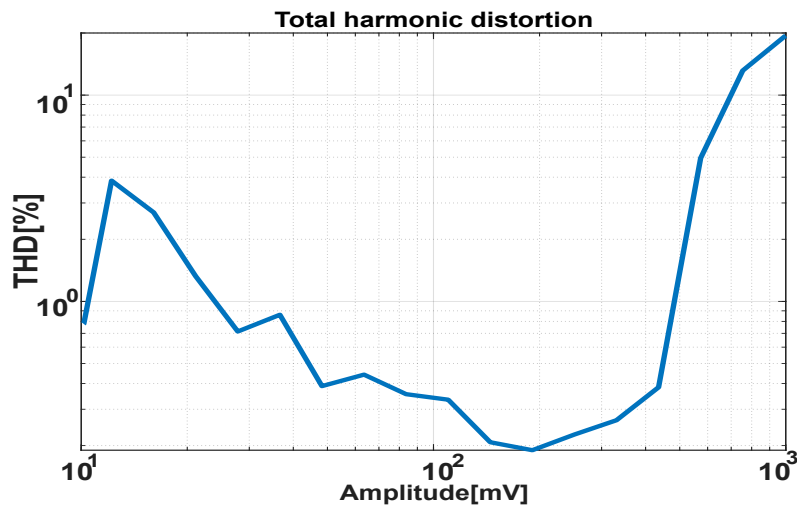


Figure 4.15: Total harmonic distortion versus amplitude for DB-OTA

5. Slew-rate.

Using the voltage-follower configuration, by applying a square wave as input voltage with a $900\mu s$ period. Two values of positive and negative slew-rate have been measured by the derivative of output voltage at rise and fall of the wave, afterwards the average is reported as the value of slew-rate. The positive slew-rate calculated for DB-OTA equals 12 V/ms and the negative is 362V/ms . An approximate calculation for positive slew rate is: $V_{DD}/(R_{out} \times C_{out})$ and for negative slew-rate equals $V_{DD}/((R_{out}||R_s + r_o) \times C_{out})$.

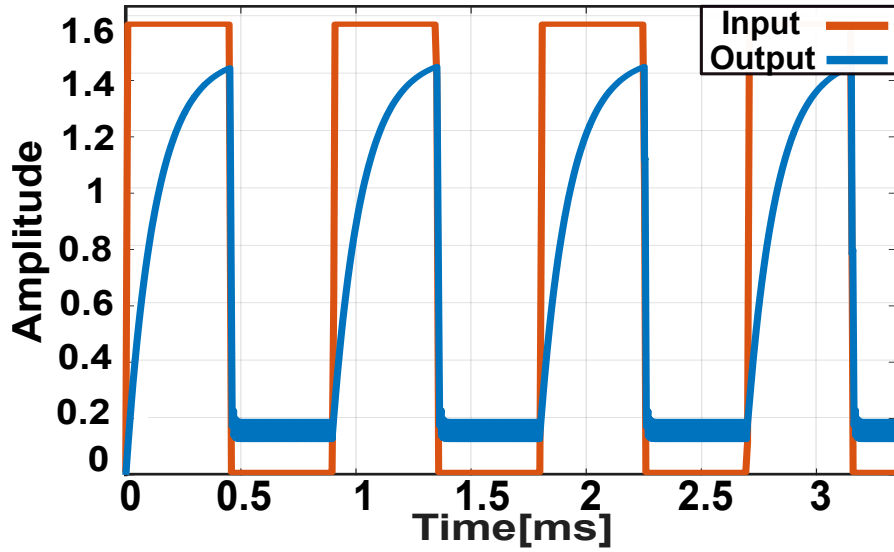


Figure 4.16: Simulated input and output voltages under square wave of DB-OTA

6. Input noise spectral density.

By applying a transient noise, and just a DC volt as input we can analyze output voltage for the noise power spectral density, Fig.4.17. The in-band noise equals to $87\mu V_{RMS}$ for DB-OTA. It is expected to have a larger input noise for DB-OTA with respect to A-OTA $8\mu V_{RMS}$ since DB-OTA have a larger bandwidth (76kHz to 40kHz) and also smaller transistor width $10\mu m$ compared to $150\mu m$. Although input signal is attenuated by the voltage division in the summing network but noise is the same at the input of inverters.

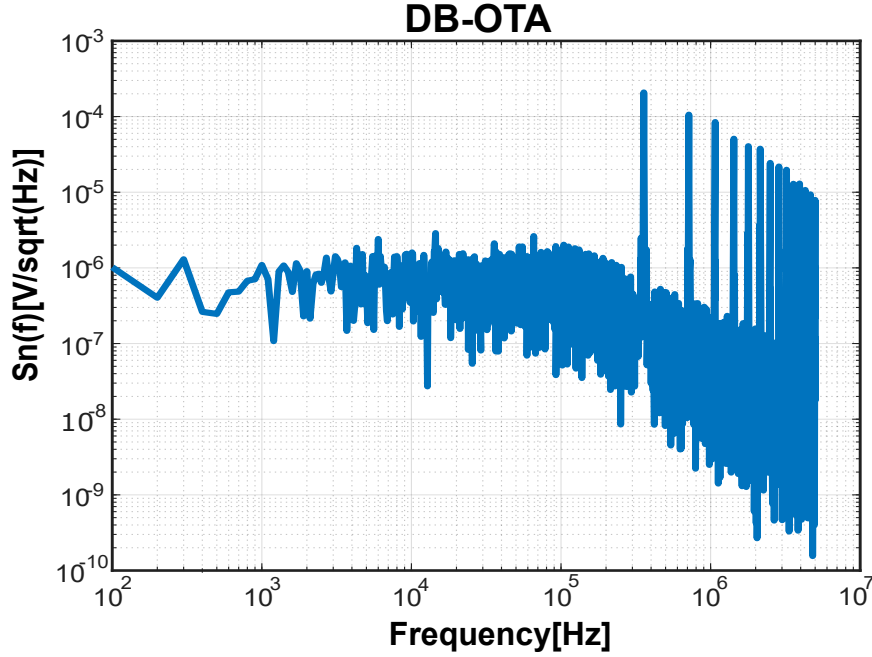


Figure 4.17: Noise spectral density of DB-OTA

7. **CMRR and PSRR** Since the CMRR is done in transient analysis there must be a DC volt along with the signal applied to the positive terminal of op-amp for biasing, while the same signal is applied to the negative terminal as well, CMRR is calculated 45.23dB. The test bench for PSRR calculation of DB-OTA is identical to the one of A-OTA, it is computed 39.25dB.

Monte Carlo simulation results

To evaluate the effect of mismatch variations, Monte Carlo analysis has been applied on 100 samples in nominal temperature, after parasitic extraction of DB-OTA layout.

1. DC gain distribution.

Histogram of Monte Carlo analysis for DC gain is shown in Fig.4.18, the mean value of this distribution is 36.3dB and standard deviation equals to 0.6 dB, this value is consistent with the 37dB calculated by typical model.

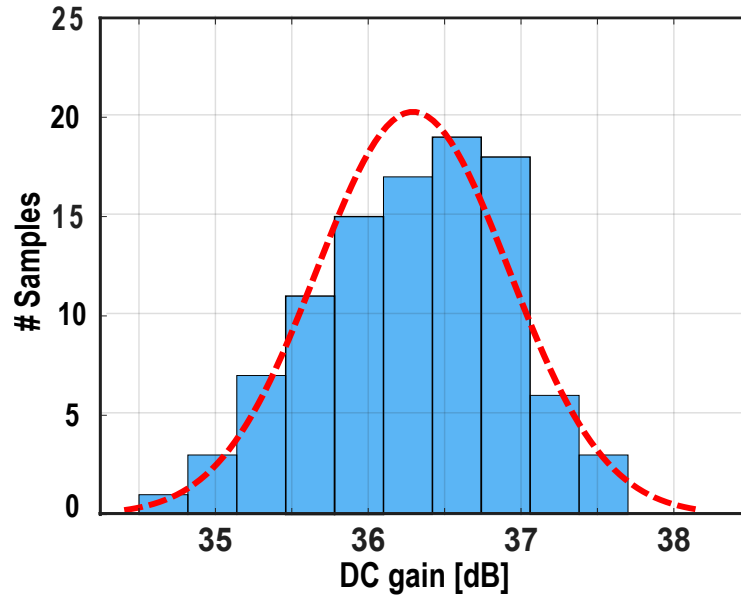


Figure 4.18: Monte Carlo DC gain distribution of DB-OTA

2. Voltage offset distribution.

The mean value of this distribution is -1 mV and the standard deviation equals to 7.2 mV. Voltage offset between input and output signals is due to effect of industrial tolerance and difference between temperatures of transistors.

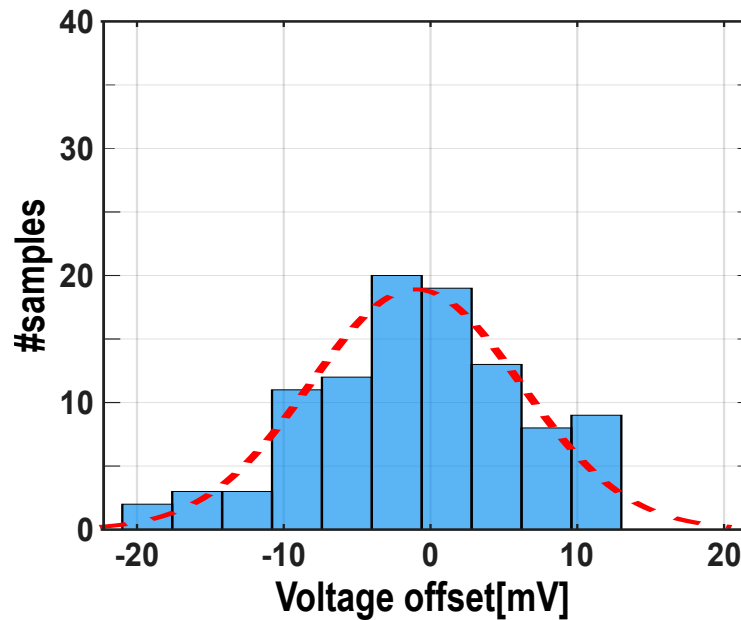


Figure 4.19: Monte-Carlo voltage offset of DB-OTA

3. Power consumption distribution.

Average of instantaneous power is reported as power consumption, evaluated with transient simulation due to digital aspects of the circuit. The mean

value of this distribution is $113 \mu W$ and the standard deviation equals to $20.4 \mu W$. This results are consistent with post layout simulation result $110.9 \mu W$.

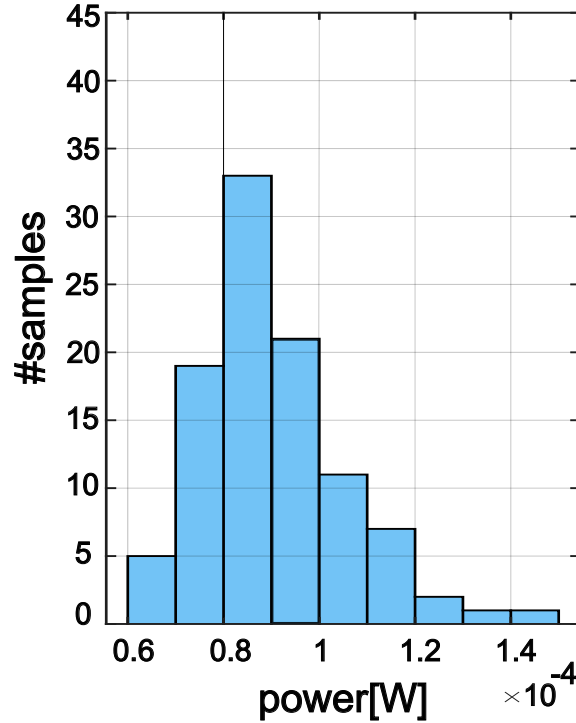


Figure 4.20: Monte-Carlo power consumption distribution of DB-OTA.

4. GBW distribution.

Since the DB-OTA circuit can't be linearized and as a result it's not possible to do AC analysis for this circuit; the GBW distribution has been calculated by obtaining amplitude of 100 samples of Monte Carlo DC gain at a fixed frequency (50kHz in this case) and then multiplication of these amplitudes to the mentioned frequency. The mean value of this distribution is 85.9 kHz which is higher with respect to the typical value estimated 76kHz, and the standard deviation is equal to 15.4 kHz. The histogram can be seen in Fig.4.21.

5. Slew-rate distribution.

The mean value of this distribution is $-356.2 V/ms$ and the standard deviation is equal to $52.8 V/ms$. Figure 4.22 shows the negative slew-rate distribution of DB-OTA.

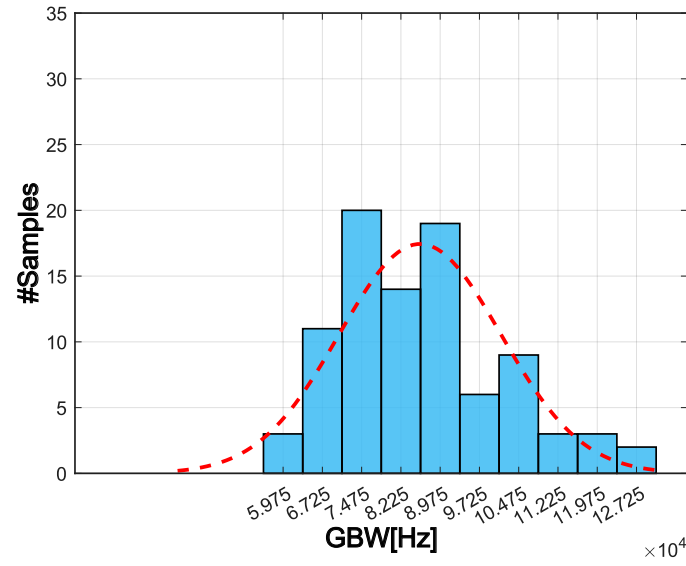


Figure 4.21: Monte-Carlo GBW distribution of DB-OTA

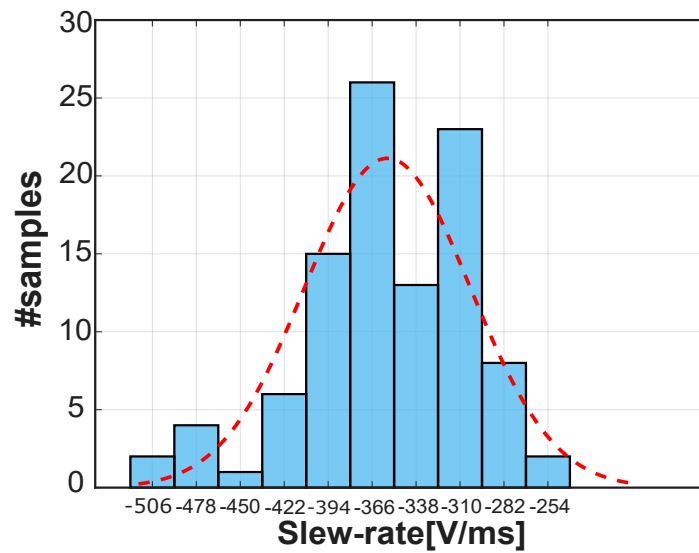


Figure 4.22: Monte-Carlo negative slew-rate distribution of DB-OTA

Chapter 5

Comparison of the Two Designs

In this chapter a comparison between Monte Carlo simulation results of the two proposed amplifiers in flexible technology is presented. Followed by a more general comparison between the two discussed amplifiers and flexible amplifiers in recent literature.

Table 5.1 shows a summary of Monte Carlo simulation results for A-OTA and DB-OTA. Performance parameters are indicated one by one in the following figures.

Table 5.1: MC Analysis for the flexible A-OTA and DB-OTA

Performance	A-OTA			DB-OTA		
	Mean (μ)	Std. Dev. (σ)	$\frac{\sigma}{\mu}$ [%]	μ	σ	$\frac{\sigma}{\mu}$ [%]
DC Gain [dB]	35.2	4.1	11.6	36.3	0.6	1.7
GBW [kHz]	58	31.9	55	86	15.5	18
Power [μW]	90	14.77	16.3	113	20.4	18
Voltage Offset [mV]	-0.07	22.3	-	-1	7.2	-
SR_{ave} [$\frac{V}{mS}$]	112	4.9	4.3	187	16.9	9
FOM [MHz \cdot pF/mW]	32.2	16	49.7	38.05	11.4	30

Monte Carlo simulations on 100 samples.

Comparing the two distributions of DC gain, one finds them almost similar. A-OTA has a larger standard deviation as the DC gain varies in a wider range wrt DB-OTA while DB-OTA has a larger mean value.

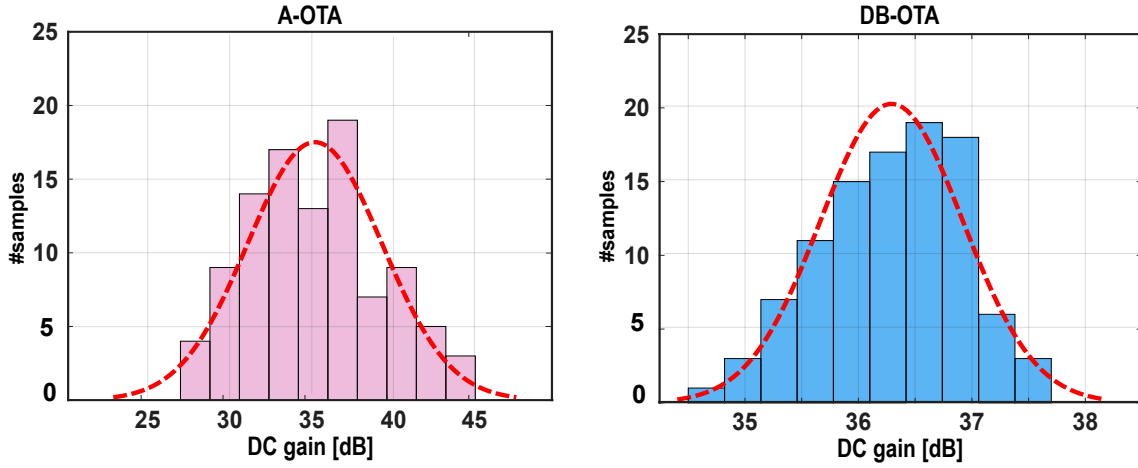


Figure 5.1: Monte-Carlo DC gain distribution of A-OTA (left) and DB-OTA (right)

Regarding the gain bandwidth of the two amplifiers, as it can be seen in the figure below, for DB-OTA, deviation of distribution is smaller and the mean value is higher, since there is a higher likelihood of occurrence for higher values of GBW.

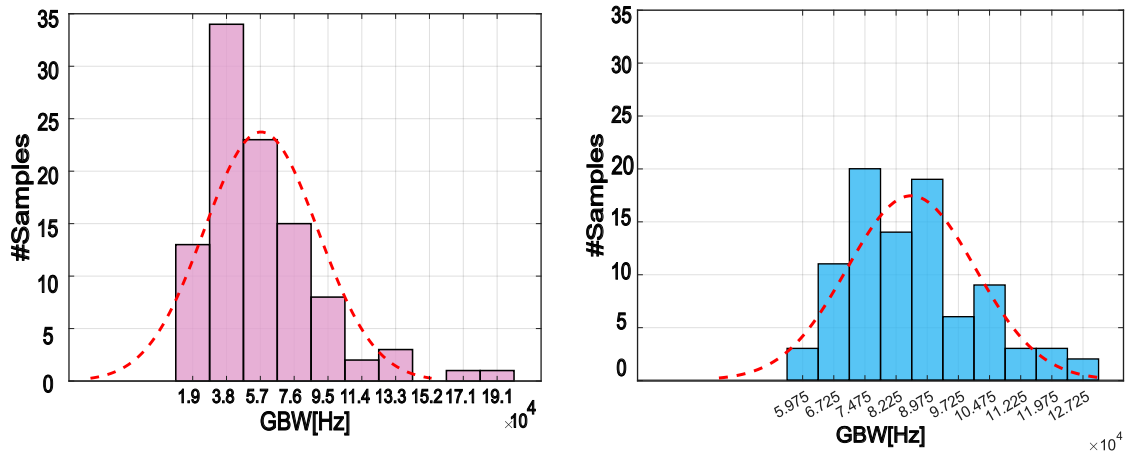


Figure 5.2: Monte-Carlo GBW distribution of A-OTA (left) and DB-OTA (right)

It can be observed in Fig. 5.3 the MC power distribution of the two amplifiers. Although the highest probability of occurrence is for A-OTA and its power consumption increases up to $200\mu W$, but, since DB-OTA has a more uniform distribution, it also has higher mean and standard deviation values.

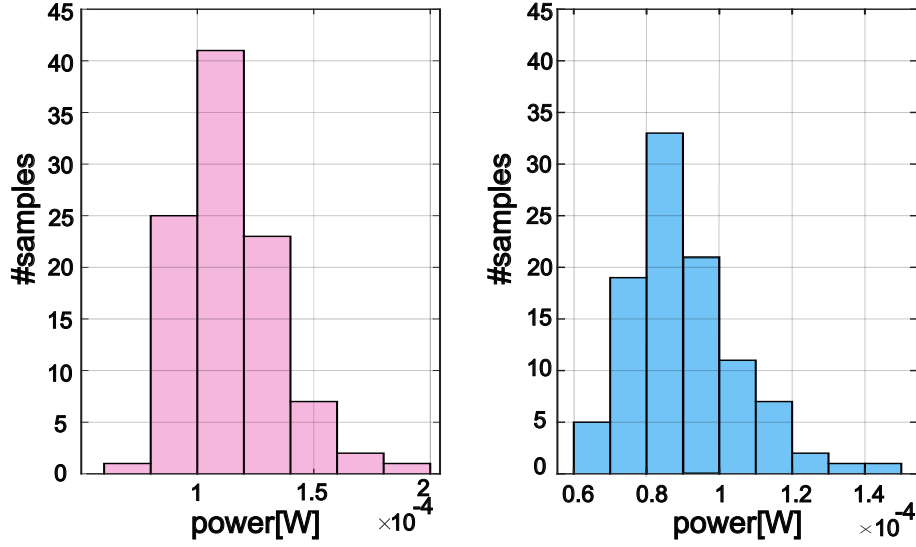


Figure 5.3: Monte-Carlo power consumption distribution of A-OTA (left) and DB-OTA (right)

Regarding the MC voltage offset distribution of the two amplifiers, the mean value for A-OTA is very close to zero and as it is observed, the distribution has high probability of occurrence around zero. On the other hand for DB-OTA, although it has a higher mean value with respect to A-OTA but, since its standard deviation is 3 times smaller, it is more robust against process variations.

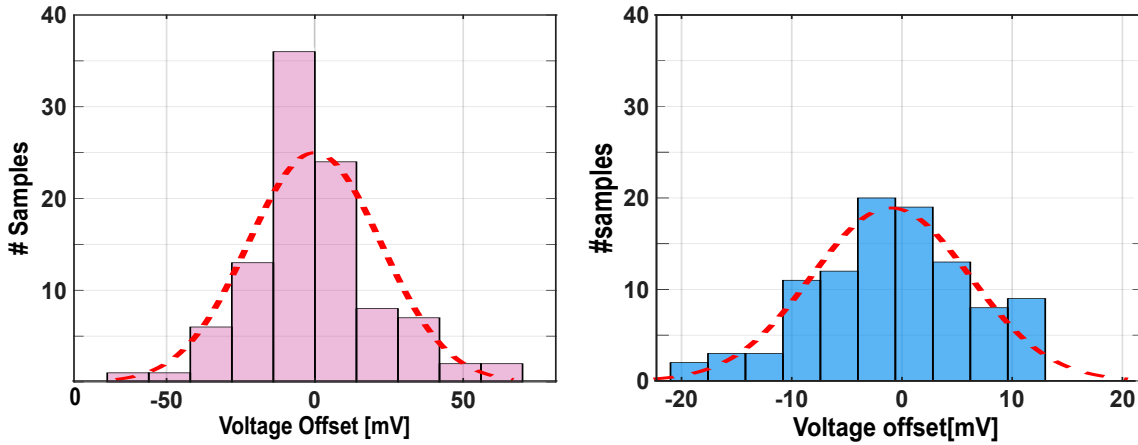


Figure 5.4: Monte-Carlo voltage offset distribution of A-OTA (left) and DB-OTA (right)

The negative slew-rate of the two amplifiers are compared. Distributions suggest a higher mean and standard deviation values for DB-OTA. This was expected since the output stage of A-OTA has a larger length with respect to DB-OTA which means it has a larger r_{on} , resulting in a smaller negative slew-rate value.

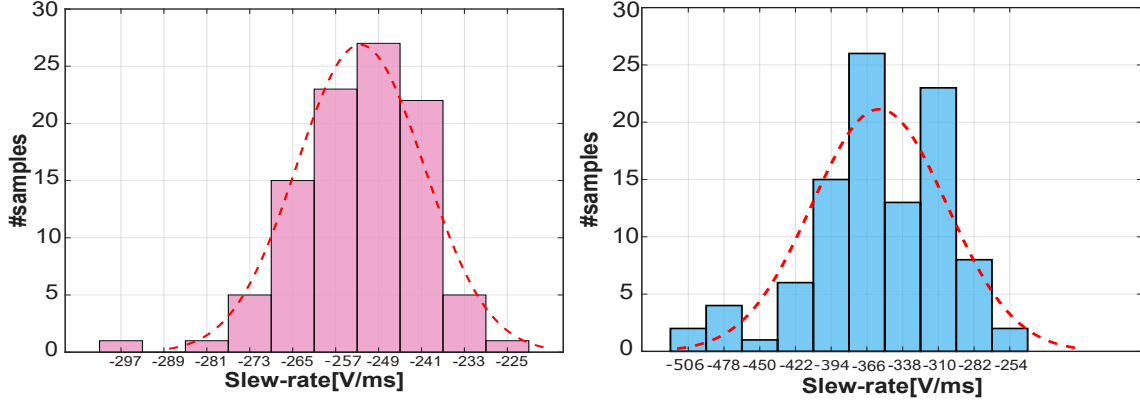


Figure 5.5: Monte-Carlo negative slew-rate distribution of A-OTA (left) and DB-OTA (right)

It can be observed in Fig.5.6 the MC figure of merit distribution of the two discussed amplifiers. As the histogram suggests DB-OTA has a higher mean value due to the fact that its FOM increases up to 200 [MHz.pF/mW] while for A-OTA this value is 80 [MHz.pF/mW]. This was expected since while they have equal load capacitance and A-OTA has slightly lower power consumption, but the GBW of DB-OTA is much more greater than A-OTAs.

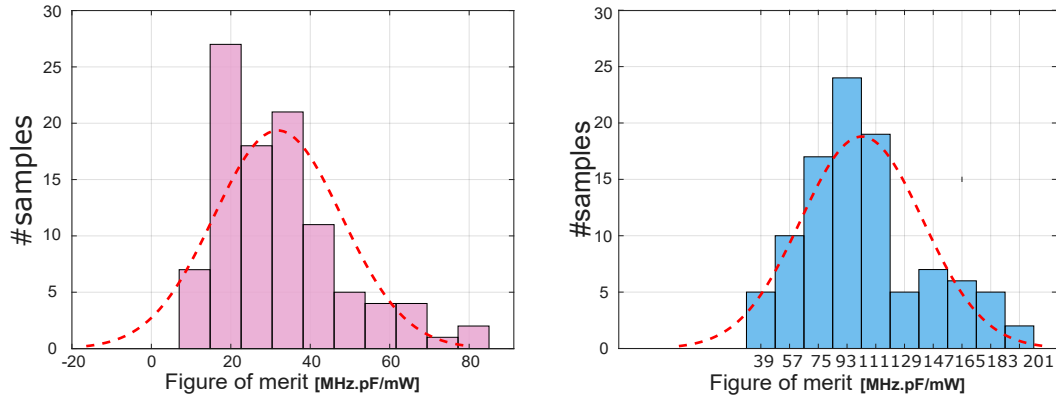


Figure 5.6: Monte-Carlo FOM distribution of A-OTA (left) and DB-OTA (right)

5.1 Comparison with the state of the art

Based on the simulation results of the two amplifiers in 800nm IGZO TFT and flexible amplifiers in recent literature, a comparison of the performance parameters is done. Table 5.2 indicates a better performance regarding the power consumption for A-OTA and DB-OTA, 5 and 4 times lower respectively compared to the minimum among other references.

Second aspect to notice is the highly reduced area consumption, as the A-OTA requires about 10 times smaller area compared to the other amplifiers, DB-OTA is even more area efficient with an area about half of A-OTAs. The large capacitive load (50pF) along with the reasonably low power consumption and comparable

Table 5.2: Comparison With State-of-the-Art among Flexible Operational Transconductance Amplifiers

	[28] ⁺	[29] ⁺	[30] ⁺	[31] ⁺	A-OTA*	DB-OTA*
Technology	a-IGZO	a-Si	Dual-gate, self-aligned a-IGZO	Dual-gate, self-aligned a-IGZO	Flexible IGZO	Flexible IGZO
Min. Feature Size [μm]	5	8	3	3	0.8	0.8
Amplifier Type	OpAmp	OpAmp	Fully Diff. OpAmp	OpAmp	OpAmp	OpAmp
#Stages/Topology	1 gain stage + 1 output stage	1 gain stage + 1 output stage	Single	2 stages internally compensated	2 stages	Single
Stage Load Type	positive-feedback	positive-feedback	Pseudo-PMOS	Pseudo-PMOS	Resistive	Resistive
DC Gain [dB]	19	42.5	40	57	35.2	36.3
GBW [kHz]	330	30	61	311	58	86
Load	15pF	20pF // 1 MΩ	30pF on PCB	-	50pF // 8 MΩ	50pF // 8 MΩ
Ph. Margin [deg.]	70	-	98	75	88	87
Supply Voltage [V]	6	25	10	10	3.3	3.3
Power[mW]	6.78	3.55	0.45	2.43	0.090	0.113
Area mm ²	25.2	5.1	0.425	3.69	0.0426	0.0252
PSRR [dB]	-	-	-	-	29	39
CMRR [dB]	-	-	-	-	59	45
In-band noise [μ V _{RMS}]	-	-	-	-	8.8	87
Slew Rate [V/mS]	-	5.2	210	-	112	187
FOM** [MHz·pF/mW]	0.73	0.147	4.06	-	32.2	38.05

1. ⁺experimental; *simulation, MC mean value; **FOM = $\frac{\text{GBW} \cdot C_{\text{out}}}{\text{Power}}$; **best performance in bold**;

GBW, outcomes the best figure of merits for DB-OTA(38MHz.pF/mW) and A-OTA(32.2 MHz.pF/mW) among flexible amplifiers in recent literature.

The supply voltage of 3.3V and the minimum feature size of 0.8 μm are the lowest among proposed amplifiers. Slew-rate of the two amplifiers are rather high, DC gains and phase margins are comparable.

Conclusions

This work presented the design of a digital-based operational transconductance amplifier along with the analog operational transconductance amplifier in flexible technology for the purpose of comparison. The discussion begun with an introduction to the recently developed flexible technology, its applications, advantages and structure.

Performance parameters and some topologies of operational amplifiers have been presented and verified by analytical expressions.

A two stage traditional analog amplifier has been designed in CMOS technology and then modified to fit the constraints of the flexible technology. Small signal model has been provided and analysis has been done to calculate DC gain and bandwidth.

Typical post-layout simulations have been done on PragmatIC model libraries for 800nm IGZO TFT at room temperature, results have been compared to the small signal analysis. After introducing effects of passive components parasitics, Monte Carlo analysis has been applied on 100 samples in nominal temperature to evaluate the effect of mismatch variations.

To meet the IoT requirements and to be compatible with the digital-based analog circuit trend, differential pair and following OTA has been designed with digital circuitry. The resulting amplifier (DIGOTA) is the basis of the presented DB-OTA. Required modifications for transferring the DB-OTA to the flexible technology has been applied and then the design has been improved.

Performance parameters have been evaluated and calculated based on the typical and Monte Carlo post-layout simulation results, taking into account the nonlinearity of the circuit.

An overall comparison between the obtained results of the two discussed amplifiers and recent literature flexible amplifiers proves advantages in case of power consumption and area nevertheless comparable DC gain, gain bandwidth product, slew-rate and phase margin.

Figure of Merit depending on the GBW, output capacitance and power consumption indicates the best performance result for the DB-OTA due to the larger bandwidth and comparable power consumption with respect to the A-OTA.

@articleRethink, author = Toledo, P. and Rubino, Roberto and Musolino, Francesco and Crovetto, Paolo, year = 2021, month = 01, pages = , title = Re-Thinking Analog Integrated Circuits in Digital Terms: A New Design Concept for the IoT Era, journal = Circuits and Systems II: Express Briefs, IEEE Transactions on, doi = 10.1109/TCSII.2021.3049680

Abbreviations

Symbols and Abbreviations

A-OTA Analog Operational Transconductance Amplifier

A-Si Amorphous Silicon

CMRR Common Mode Rejection Ratio

DB-OTA Digital-based Operational Transconductance Amplifier

DRC Design Rule Checking

E-beam Electron Beam

FlexIC Flexible Integrated Circuit

FOM Figure of Merit

GBW Gain Bandwidth Product

IGZO Indium-Gallium-Zinc-Oxide

IoT Internet of Things

LTPS Low-temperature Polycrystalline Silicon

LVS Layout Versus Schematic

m-Health Mobile Healthcare

NFC Near Field Communication

OLED Organic Light Emitting Diodes

Op-amp Operational Amplifier

PEX Parasitic Extraction

PSRR Power Supply Rejection Ratio

RFID Radio Frequency Identification

SiNx Silicon Nitride

TFT Thin Film Transistor

THD Total Harmonic Distortion

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