POLITECNICO DI TORINO

Master Degree course in Mechatronics Engineering

Master Degree Thesis

Development and testing of a three-phase SiC inverter-based eDrive

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Abstract

Permanent magnet synchronous motors are synchronous motors in which the field magnetomotive force is provided by permanent magnets. The use of rare earth magnet materials increases the flux density in the air gap and accordingly also in the motor power density and torque-to-inertia ratio: this makes these motors perfectly suited for applications like robotics and aerospace actuators, where it is preferable to have the weight as low as possible for a given output power.

The thesis work deals with developing, testing and implementing the hardware and software needed for the motor to operate properly.

The system consists of a DC-AC Inverter module with input filtering capacitors, the gate driver, voltage and current sensing boards and the PWM transmitting and receiving cards.

The process involves the design of the bus capacitors; the testing of the gate driver; the double-pulse test of the inverter; the design, soldering and testing of current and voltage sensing printed circuit boards; the design, soldering and testing of the electric-to-optical PWM transmitting board and the optical-to-electric PWM receiving board.

Before connecting the system to the motor, the behavior of the system is also simulated and tested without any load and with a resistive-inductive load.

Subsequently, the system is connected to the permanent magnet motor and started firstly with V/f scalar control technique and then with I/f closed-loop technique, showing how the second is safer and offers the possibility to run the motor at higher speeds without the angular position feedback.

Lastly, the closed-loop Field Oriented Control is designed and simulated for the system, ready to be implemented.

Contents

Chapter 1

Introduction

1.1 Electrical machines

Electrical motors are extensively used nowadays in lots of different fields, from household appliance to industrial applications. Since a wide range of electrical motors exist, the main decision criteria are the application usage and the budget available. Electrical motors are divided in two big families: the DC motors and the AC motors. An overview of the main available solutions is shown in Fig. 1.1. [13]

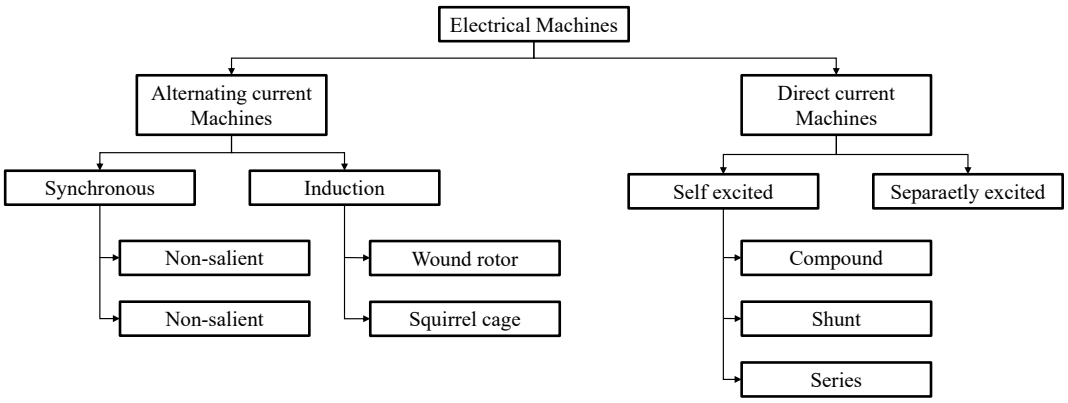


Figure 1.1: Scheme with main available electrical machines [6]

DC motors offer as their main advantages the simplicity of the control mechanism, relatively low manufacturing cost and technological maturity, which has made them very popolar in automotive industry for long time. Nevertheless, these benefits come with bulky construction, low efficiency, less reliable operation and need for frequent maintenance. In addition to this, sparking at brushes makes this motor type unsafe in specific environments. [8]

The significant progress made in the control algorithm of AC motors (combined with the advantage of a lower inertia, higher robustness and power efficiency) is now making the use of AC motors much more popular.

As shown in Fig. 1.1, AC motors can be sub-divided in:

- Asynchronous motors (also called Induction Motors, IM): a stator alternated current induces another current in the rotor winding, generating an interaction between the 2 magnetic fields produced. The two magnetic fields run at slightly different frequency generating torque;

- Synchronous motors: the rotor magnetic field generated by either a permanent magnet or an excitation coil, has constant direction in a reference frame fixed to the rotor. The rotor at steady state condition moves with a frequency synchronized with the one of the stator magnetic field.

Induction motors have gained significant popularity for industrial as well as automotive application because of their low cost, ruggedness and low maintenance requirement. Among the two types available, squirrel cage rotor motor is preferred over wound rotor motor. On top of that, they present a large constant power region which makes them more favorable for automotive application.

Due to the absence of permanent magnets, the induction motor has lower cost, zero cogging torque, is less sensitive to higher operating temperatures. In fact, it can sustain a higher peak stator current of several times the rated current without the danger of demagnetizing the magnets. Both the induction motors and the PMSM suffer from limited field weakening speed range.

It is important to point out that control of Induction machines is quite complex because rotor and stator windings are not fixed orthogonal with respect to each other: the rotor field is induced by the stator field, resulting in harder torque control. However Field Oriented Control gives satisfactory results. Nonetheless high losses, poor power factor, high weight, large volume and the limitations regarding overload have made the synchronous (especially permanent magnet) drives more suitable during the past few years.

1.2 Permanent magnet motors

The permanent magnet synchronous motor (PMSM) is a synchronous motor with sinusoidal magneto-motive-force(MMF), voltage and current waveforms where the field MMF is provided by permanent magnets.

The use of rare earth magnet materials increases the flux density in the air gap and accordingly also the motor power density and torque-to-inertia ratio: this makes PM motors perfectly suited for applications like robotics and aerospace actuators, where it is preferable to have the weight as low as possible for a given output power.

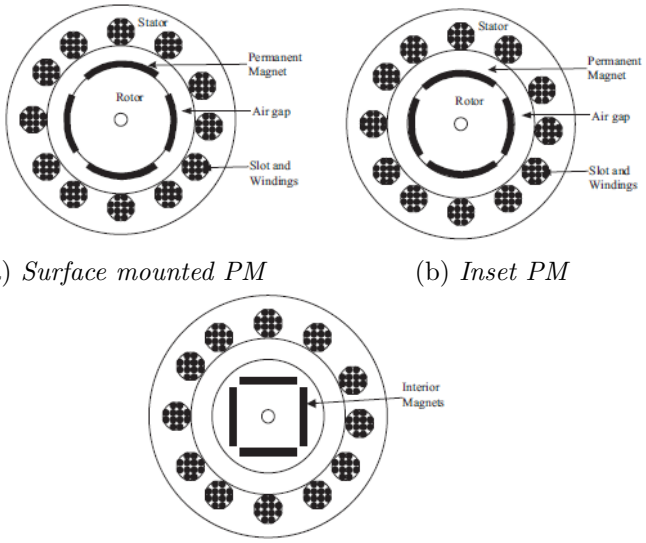
The PMSM is more efficient and easier to cool due to the absence of rotor copper loss compared to the induction machines.

The lower inertia of PMSM helps the electrical response time (although the induction motor electrical response characteristics will be faster because of the smaller time constant). The electrical time constant of magnetic circuits is determined by the L/R

ratio. The load current transient in induction machines is limited only by the small leakage inductance, where the time constant inductance in PM machines is the much higher self-inductance. When it comes to operating at higher speeds, both the induction motors and the PMSM suffer from limited field weakening speed range.

Even though PMSM present rugged motor structures, the risk of breaking magnet chips represents a major concern. The main drawbacks of having Permanent Magnets are that in addition to being expensive, they are also sensitive to temperature and load conditions. As a consequence, PMSMs are mostly found in small to medium power applications, although there are some high power applications for which PMSMs are being used.

Depending on the shape and the position of the permanent magnets, the behaviour of PMSMs change. The three common arrangements of the rotors are surface mounted, inset and interior (or buried) are shown in Fig. 1.2.



(a) *Surface mounted PM* (b) *Inset PM*

(c) *Buried PM*

Figure 1.2: Different Permanent Magnet motor structures

The difference between surface mounted and inset magnets is that the magnets in the latter are inside the rotor surface, but still exposed to the air gap: this makes the magnet more secured. In the surface-mounted PMSM (SMPMSM), the magnets can either be epoxy-glued or wedge-fixed to the cylindrical rotor. Another solution involves non-magnetic stainless steel or carbon fiber sleeves to contain the magnets. Manufacturing-wise this kind of rotor is relatively simple, although the mechanical strength of the rotor is limited by the epoxy glue.

The third type of PMSM is the interior PMSM (IPMSM): this solution consists in embedding the magnets inside the rotor. The manufacturing process increases in complexity since the magnets have to be inserted after the lamination stacking of the rotor and then magnetized. Nonetheless, the IPMSM has become the go-to solution for electric and hybrid vehicle applications due to their high power density and high efficiency.

Additionally, The rotor structure results to be more robust since the magnets are buried inside, eliminating the risk of chipping off which is present in SMPMSMs. However, it is important to mention that for electric and hybrid vehicle applications, the motor size is relatively large compared to the other smaller power applications of PM motors, which enhances the cost problem due to the high cost of rare-earth magnet materials used in traction IPMSMs.

Being the application in examination in the small to medium power range, SMPMSM represent a valid choice. The following discussion will focus on them. [6]

1.3 Inverter

A typical electric drive system consists of an electric motor and a power converter which serves as interface between motor and its DC supply. Converter comprises of DC-link and three-phase inverter.

The six-switch three-phase voltage source inverter (VSI) is used in electric and hybrid vehicle applications where the source typically consists of a DC voltage. Through the inverter the available on-board DC power is converted to a high-fidelity AC current and voltages required to meet the driver demands for vehicle propulsion.

Fig. 1.3 shows the typical 2-level 3-phase VSI.

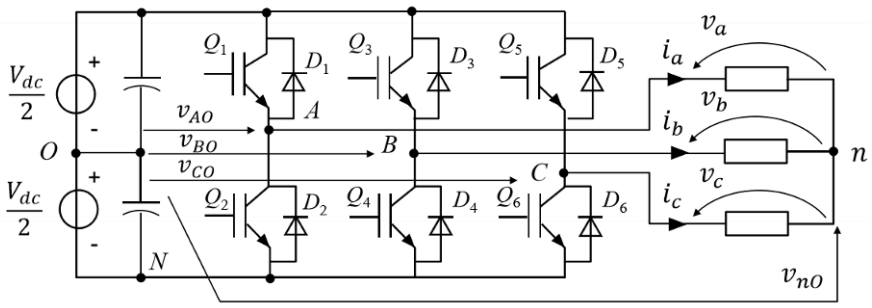


Figure 1.3: 2-level 3-phase VSI [3]

Regarding the switches employed, Si-IGBT are still the most popular due to cost. However, SiC and GaN power devices have made impressive progress and are gaining increasing popularity over Si-IGBTs for traction applications. Several EVs have already adopted the SiC technology: in fact, SiC MOSFETs are more mature and near term compared to GaN, although current studies show that GaNs have the potential to be the eventual choice in the future.

SiC MOSFETs can operate at higher frequency generating lower device losses: increasing the switching frequency enables better current regulation and reduced dead time to contribute towards less voltage and current distortion. Another significant advantage of SiC technology compared to Si-IGBT is the elimination of the anti-parallel diodes, essential in the case of Si-IGBT.

Chapter 2

Theoretical Models

2.1 Space vector representation

PM motors are usually manifactured with distributed windings at the stator to produce a magnetic field at the airgap that is as sinusoidal as possible.

A three-phase stator supplied by balanced three-phase currents produces a magnetic field rotating at the synchronous speed ω_s. The peculiarity of synchronous machines is that, at steady state, the rotor spins at the synchronous speed ω_m, which is directly related to the AC frequency delivered by the inverter, being $\omega_m = \omega_s/p = 2\pi f_s/p$.

Space vectors offer a convenient mean to describe the spatial location of quantities such as windings in a machine.

Fig. 2.1 shows a representation of the three-phase windings.

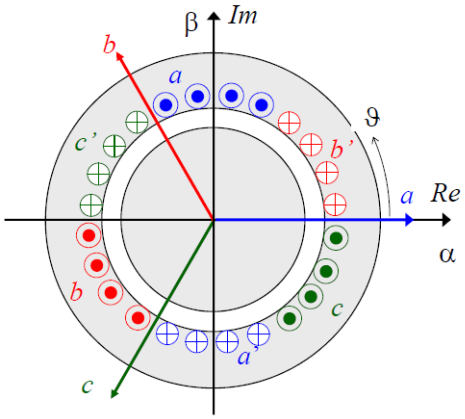


Figure 2.1: Three-phase windings of an electrical machine representation [3]

The spatial location of three-phase windings separated by 120 electrical degrees is easily described starting from the three unit vectors in Eq. 2.1

$$\begin{aligned} \vec{a} &= e^{j0} = 1 + j0 \\ \vec{b} &= e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{2}}{3} \\ \vec{c} &= e^{-j\frac{2\pi}{3}} = -\frac{1}{2} - j\frac{\sqrt{2}}{3} \end{aligned} \tag{2.1}$$

Naming "x" a generic three-phase electrical quantity, it is possible to express it as a space vector according to Eq. 2.2.

$$\vec{x_s} = \frac{2}{3}(x_a\vec{a} + x_b\vec{b} + x_c\vec{c}) \tag{2.2}$$

Such space vector can also be represented in the complex plane according to Eq. 2.3.

$$\vec{x_s} = x_{s\alpha} + jx_{s\beta} \tag{2.3}$$

Fig. 2.2 provides a visual description of the operations described.

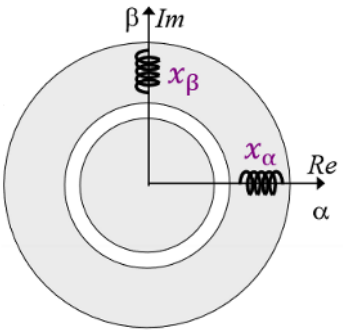


Figure 2.2: Visualization of Space Vector representation [3]

The homopolar component of a generic space vector is defined according to Eq. 2.4. This can be seen as the common mode component, but in reality it is defined with the purpose of deriving a square matrix (invertible) as it is not involved in the electromechanical energy conversion.

$$x_o = \frac{1}{3}(x_a + x_b + x_c) \tag{2.4}$$

It is now possible to introduce Clarke transformation: this consists of power non invariant coordinate transformation to express abc quantities in their $\alpha\beta o$ components.

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_o \end{bmatrix} = T \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \qquad T = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.5}$$

Recalling that at steady state operating condition the space vectors of the main electrical quantities (i.e. current, voltage and flux) rotate at the electrical synchronous speed ω_s, representing such quantities in a rotating reference frame is convenient in terms of

machine modeling for control purposes as they become constant. The rotating frame is called the dq frame.

The dq modeling provides a methodology to analyze three-phase electric machines by transforming three-phase variables into two-phase variables with the help of a set of two fictitious windings, known as dq windings. These are in quadrature with each other. In the dq coordinate system, the d-axis is the direct axis aligned with the permanent magnet magnetic field, while the q-axis is in quadrature to the direct axis.

Being the dq frame obtained by rotating the $\alpha\beta$ frame of an angle θ (which varies at rate ω_s), the relation between the two frames are retrieved and shown in Eq. 2.6. [3]

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \begin{bmatrix} A(\theta) \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \qquad \begin{bmatrix} A(\theta) \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \tag{2.6}$$

Fig. 2.3 shows the three possible ways to represent the machine electrical quantities.

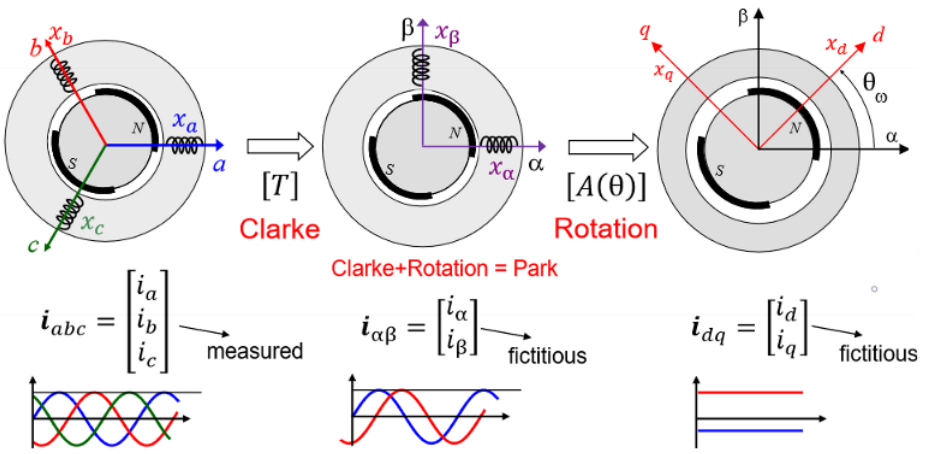


Figure 2.3: Representation of possible ways to model machine's electrical quantities [3]

2.2 Surface Mounted Permanent Magnet Synchronous Motor model

The voltage in each phase of Surface Mounted Permanent Magnet Synchronous Motor (SMPMSM) is given by two contributions: the voltage drop on the stator resistance (responsible for the Joule losses in the motor) and the flux linkage variation (induced back electro-motive force) resulting from the rotor spinning in a magnetic field. The matricial form of this expression is presented in Eq. 2.7.

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = R_s \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \lambda_a \\ \lambda_b \\ \lambda_c \end{bmatrix} \tag{2.7}$$

Exploiting Clarke transformation retrieved in the previous section, it is possible to represent the same quantities in the $\alpha\beta$ reference frame (the homopolar component is neglected as it is not of any interest from the electro-mechanical energy conversion point of view). The results are shown in Eq. 2.8 in two forms.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = R_s \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \lambda_\alpha \\ \lambda_\beta \end{bmatrix} \quad \text{or} \quad \vec{v}_{\alpha\beta} = R_s \vec{i}_{\alpha\beta} + \frac{d}{dt} \vec{\lambda}_{\alpha\beta} \tag{2.8}$$

Taking a further step, it is possible to apply the Park transformation to the equation just derived:

$$v_{\alpha\beta} = v_{dq} \cdot e^{j\theta} = R_s i_{dq} \cdot e^{j\theta} + \frac{d}{dt}(\lambda_{dq} \cdot e^{j\theta}) \tag{2.9}$$

Where the second term can be expressed as:

$$\frac{d}{dt}(\lambda_{dq} \cdot e^{j\theta}) = \frac{d}{dt}\lambda_{dq} e^{j\theta} + j\frac{d\theta}{dt}\lambda_{dq} e^{j\theta} \tag{2.10}$$

Expressing $d\theta/dt = \omega$, it is possible to derive the expression of the voltage in the dq frame according to Eq. 2.11.

$$\begin{gathered} \vec{v}_{dq} = R_s \vec{i}_{dq} + \frac{d}{dt}\vec{\lambda}_{dq} + j\omega\vec{\lambda}_{dq} \\ \begin{bmatrix} v_d \\ v_q \end{bmatrix} = R_s \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \lambda_d \\ \lambda_q \end{bmatrix} + \omega \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \lambda_d \\ \lambda_q \end{bmatrix} \end{gathered} \tag{2.11}$$

Eq. 2.11 provides a good way to understand how the voltage provided by the inverter is employed at the stator: the first term accounts for the drop on the stator resistance, the second term for the flux variation subsequent to load variations (this term is null at steady state) and the third is the motional (speed dependent) term. In practice, the back electro-motive force term present in Eq. 2.7 is equivalent to a three-phase voltage generator imposing a speed-dependent voltage.

The next step in the analysis of the SMPMSM motor is deriving a magnetic model. This model expresses the relation between current and flux, hence, it is related to the rotor. The flux at the air gap is result of two contributions: one from the permanent magnet mounted on the surface of the rotor, the other from the currents at the stator. Observing the representation in the abc frame, the flux at each phase, it includes a contribution from its phase current, a contribution from the self and mutual inductances and a contribution from the instantaneous projection of the permanent magnet flux on the phase.

$$\begin{bmatrix} \lambda_a \\ \lambda_b \\ \lambda_c \end{bmatrix} = L_{ls} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} M_{aa} & M_{ab} & M_{ac} \\ M_{ba} & M_{bb} & M_{bc} \\ M_{ca} & M_{cb} & M_{cc} \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \lambda_m \begin{bmatrix} \cos(\theta) \\ \cos(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) \end{bmatrix} \tag{2.12}$$

Where L_{ls} models the leakage phase inductance, M_{ij} the magnetizing self and mutual inductances. The value of the inductance is not constant along the air gap, but it depends sinusoidally on the angular position of the rotor.

For this reason, the expressions of the flux linkage is hard to be applied in practical contexts in *abc* and $\alpha\beta$ frames. However, applying both Clarke and Park transformations, it is possible to retrieve a much simpler expression in the *dq* frame for PM motors:

$$\begin{bmatrix}\lambda_d\\ \lambda_q\end{bmatrix} = \begin{bmatrix}L_d & 0\\ 0 & L_q\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix} + \lambda_m \begin{bmatrix}1\\ 0\end{bmatrix} \tag{2.13}$$

Where:

$$L_d = L_{ls} + \frac{3}{2}M_{avg} + \frac{3}{2}M_\Delta$$
$$L_d = L_{ls} + \frac{3}{2}M_{avg} - \frac{3}{2}M_\Delta$$
$$M_{avg} = \frac{M_d + M_q}{2} \quad \text{Average inductance}$$
$$M_\Delta = \frac{M_d - M_q}{2} \quad \text{Differential inductance due to rotor anisotropy}$$

In the case of SMPMSM, the reluctance values of the ferromagnetic material and of the air can be assumed equal, resulting in $M_\Delta = 0$ and hence $L_d = L_q = L_s$. As a result the previously derived relation can be updated in Eq. 2.14.

$$\begin{bmatrix}\lambda_d\\ \lambda_q\end{bmatrix} = \begin{bmatrix}L_s & 0\\ 0 & L_s\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix} + \lambda_m \begin{bmatrix}1\\ 0\end{bmatrix} \tag{2.14}$$

In general, the torque of an electric motor is:

$$T = \frac{3}{2}p\vec{\lambda} \wedge \vec{i} \tag{2.15}$$

Expressing it in the *dq* frame, it becomes:

$$T = \frac{3}{2}p(\lambda_d i_q - \lambda_q i_d) \tag{2.16}$$

Combining Eq. 2.16 and Eq. 2.13, Eq. 2.17 is obtained.

$$T = \frac{3}{2}p[\lambda_m i_q + (L_d - L_q) i_d i_q] \tag{2.17}$$

This equation shows that the contributions for torque production are two: one from the permanent magnet and one from the saliency (anisotropy) of the motor. In the case of a SMPMSM, being it isotropic, the second term gives no contribution. Hence, all the torque comes from the permanent magnet. Eq. 2.18 shows the equation of the torque in a SMPMSM in *dq* frame.

$$T = \frac{3}{2}p(\lambda_m i_q) \tag{2.18}$$

Observing Eq. 2.18 and Eq. 2.11, it is possible to deduce that at increasing motor speed (ω_m), also the contribution of the back EMF voltage increases: this means that

to generate the same torque at higher speeds, an increase in the voltage is necessary to maintain a constant i_q.

Lastly, the equation for motion in the mechanical domain is presented:

$$T_e - T_{load} - B\omega_m = J\frac{d\omega_m}{dt} \tag{2.19}$$

Where T_{load} is the mechanical load torque seen by the motor, B is the viscous friction of the motor and J is the mechanical inertia of the motor. [3]

2.3 Inverter operation

As presented in the previous section, synchronous electric motors require three-phase sinusoidal voltage to correctly operate. Such voltage is provided by the inverter. Referring to Fig. 1.3, we can define v_{no} as the common-mode voltage. Point O identifies the virtual DC reference point. The istantaneous line-to-line voltages (V_{kO}, k = A, B, C) switch at frequency f_{sw} between $\pm V_{DC}/2$ depending on the legs switching functions q_k.

The switching functions are obtained comparing the desired duty cycles to a triangular waveform. Further details for modulation techniques are provided in Sec. 2.4 and 2.5.

The phase voltages V_k can be retrieved using Kirchoff voltage law:

$$\begin{cases} v_a(t) = v_{AO}(t) - v_{nO}(t) \\ v_b(t) = v_{BO}(t) - v_{nO}(t) \\ v_c(t) = v_{CO}(t) - v_{nO}(t) \end{cases} \tag{2.20}$$

Assuming we can model a SMPMSM as a balanced load, with a phase impedance equal to $Z_k = Z$ (with k = a, b, c), it is possible to derive an expression for the common-mode voltage:

$$\begin{cases} v_{AO}(t) = Z \cdot i_a + v_{nO} \\ v_{BO}(t) = Z \cdot i_b + v_{nO} \\ v_{CO}(t) = Z \cdot i_c + v_{nO} \end{cases} \tag{2.21}$$

$$v_{AO} + v_{BO} + v_{CO} = Z(i_a + i_b + i_c) + 3 \cdot v_{nO}$$

Under the assumption of a balanced load, $i_a + i_b + i_c = 0$, hence:

$$v_{nO} = \frac{1}{3}(v_{AO} + v_{BO} + v_{CO}) \tag{2.22}$$

Another important relation can be found studying the average value of the common-mode voltage. The main objective of the inverter is to obtain an average line-to-line voltage equal to the desired one. Considering:

$$\begin{cases} \bar{v_{AO}} = \hat{V}^* \cdot \sin(\omega t) \\ \bar{v_{BO}} = \hat{V}^* \cdot \sin(\omega t - \frac{2\pi}{3}) \\ \bar{v_{CO}} = \hat{V}^* \cdot \sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{2.23}$$

Combining Eq. 2.22 and 2.23:

$$\bar{v_{nO}} = 0 \tag{2.24}$$

Substituting this in Eq. 2.20, it is possible to obtain:

$$\begin{cases} \bar{v_a} = \bar{v_{AO}} \\ \bar{v_b} = \bar{v_{BO}} \\ \bar{v_c} = \bar{v_{CO}} \end{cases} \tag{2.25}$$

The equations that have just been presented can now be compared with the results of a simulation of the inverter on PLECS. Simulation parameters are:

- $V_{DC} = 400$ V, $\hat{V}^* = 100$ V. Consequently $m_a = 0.5$;
- $f_s = 2$kHz, $f_o = 50$ Hz. Consequently $m_f = 40$;
- R $= 2\,\Omega$, L $= 500\mu$H;

The resulting phase, line-to-line, common-mode voltages are shown in Fig. 2.4.

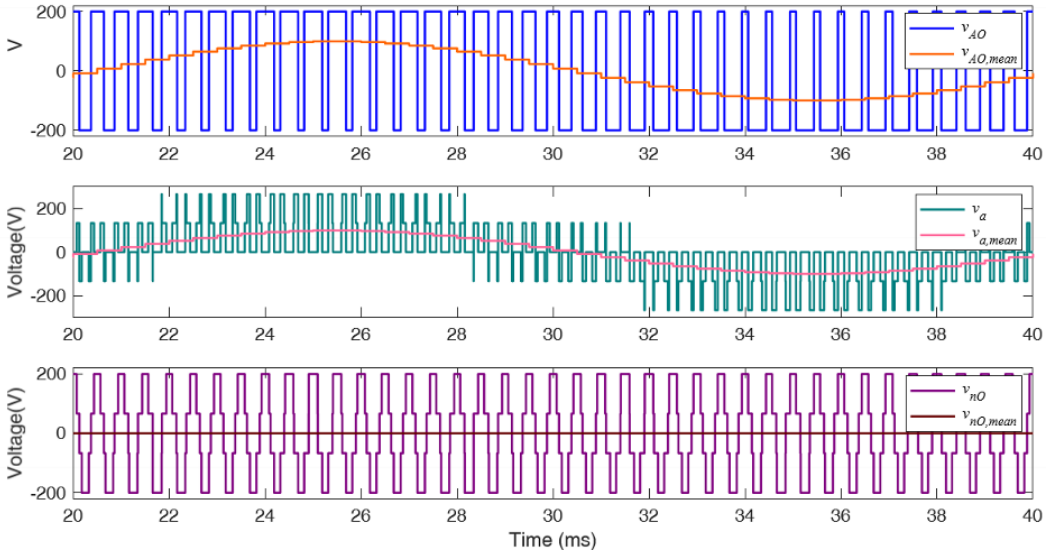


Figure 2.4: Line-to-line, phase-to-phase, common-mode voltages from inverter simulation [3]

The waveforms shown in Fig. 2.4 match the equations. In fact, considering that v_{kO} is equal to $\pm V_{DC}/2$, the set of all possible values for v_{nO} becomes:

$$\begin{cases} v_{nO,1} = \frac{1}{3}(3 \cdot \frac{V_{DC}}{2}) = \frac{1}{2}V_{DC} \\ v_{nO,2} = \frac{1}{3}(3 \cdot -\frac{V_{DC}}{2}) = -\frac{1}{2}V_{DC} \\ v_{nO,3} = \frac{1}{3}(V_{DC} - \frac{V_{DC}}{2}) = \frac{1}{6}V_{DC} \\ v_{nO,4} = \frac{1}{3}(-V_{DC} + \frac{V_{DC}}{2}) = -\frac{1}{6}V_{DC} \end{cases} \tag{2.26}$$

Eq. 2.26 can be substituted inside Eq. 2.20, obtaining the set of possible phase voltages:

$$\begin{cases} v_{k,1} = \pm\frac{V_{DC}}{2} \mp \frac{V_{DC}}{2} = 0 \\ v_{k,2} = \frac{V_{DC}}{2} + \frac{V_{DC}}{6} = \frac{2}{3}V_{DC} \\ v_{k,3} = \frac{V_{DC}}{2} - \frac{V_{DC}}{6} = \frac{1}{3}V_{DC} \\ v_{k,4} = -\frac{V_{DC}}{2} - \frac{V_{DC}}{6} = -\frac{2}{3}V_{DC} \\ v_{k,5} = -\frac{V_{DC}}{2} + \frac{V_{DC}}{6} = -\frac{1}{3}V_{DC} \end{cases} \tag{2.27}$$

Analyzing the Fourier spectrum of the pahse voltage (shown in Fig. 2.5), it is possible to observe it is composed of two main contributions: a fundamental component which is the desired one for the power conversion and the harmonics due to switching that create the voltage distortion.

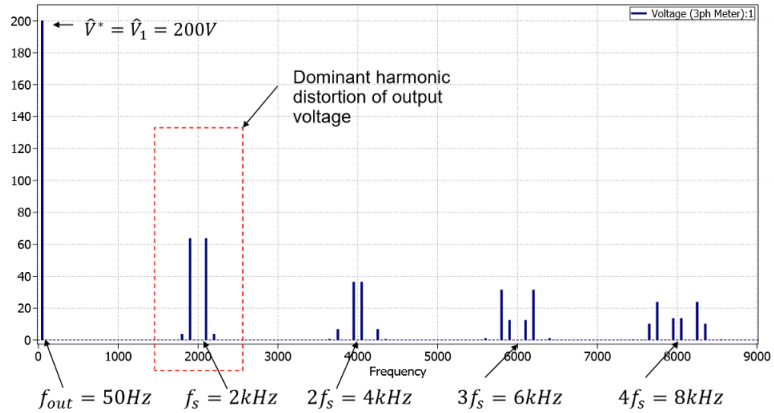


Figure 2.5: Fourier spectrum of the phase voltage [3]

This distortion is reflected in each phase current, as shown in Fig. 2.6.

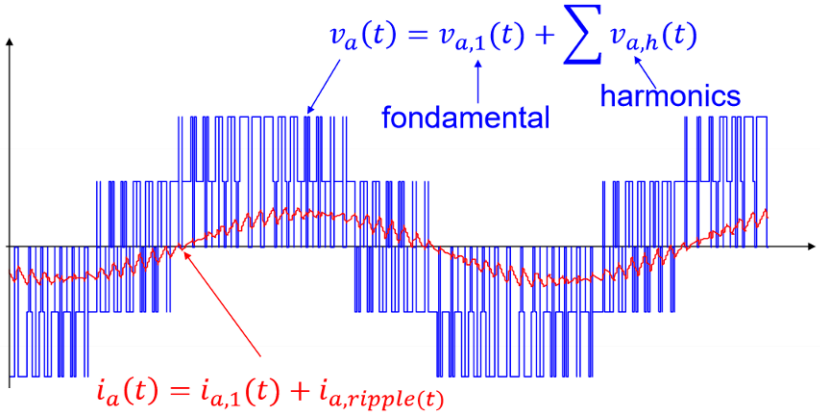


Figure 2.6: Ripple on the phase current due to switching operations [3]

The ripple in the current is always present, but it is desirable to have it as low as possible as the distortion in the current generates a distortion in the torque. A non-smooth torque can result in an unpleasant experience for the user. [3]

2.4 Sinusoidal Pulse Width Modulation (SPWM)

The control of an electrical drive consists in generating the correct switching function for the MOSFETs in order to obtain the desired inverter output.

The pulses to turn on each MOSFET are generated comparing the modulating signal($v_c(t)$) with a carrier waveform($v_{tr}(t)$), which can be sawtooth, triangular and bipolar triangular. For this application, a triangular carrier with unitary maximum amplitude is chosen. Naming q(t) the switching function, it is set to 1 when $v_c \geq v_{tr}$ and to 0 when $v_c < v_{tr}$.

The duty cycle of each MOSFET is:

$$d(t) = \frac{v_c(t)}{\hat{V_{tr}}} \tag{2.28}$$

Considering unitary carrier, $\hat{V_{tr}} = 1$, hence:

$$d(t) = v_c(t) \tag{2.29}$$

At this stage an expression for v_c is needed. For this purpose, it is important to decide how the switches belonging to the same leg have to operate. They can either switch synchronously or not: in the latter case, a short circuit at the leg might occur, destroying the converter. Hence, the first solution is chosen. This is called bipolar PWM modulation, and its functioning is presented in Fig. 2.7.

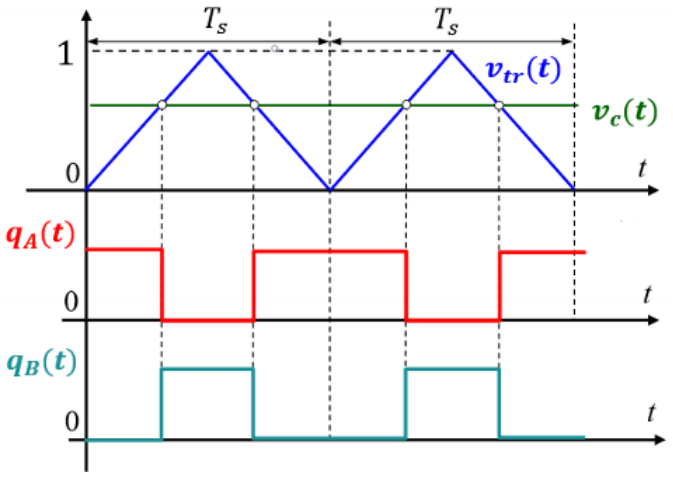


Figure 2.7: Operation with bipolar PWM modulation [3]

Consequently, the line-to-line voltage can be expressed as:

$$v_{kO}(t) = [2 \cdot q_k(t) - 1]\frac{V_{DC}}{2} \tag{2.30}$$

Averaging this expression over a sampling period T_{sw}, it becomes:

$$\begin{aligned} \bar{v_{kO}}(t) &= [2 \cdot d_k(t) - 1]\frac{V_{DC}}{2} \qquad d_k(t) = v_{c,k}(t) \\ \bar{v_{kO}}(t) &= [2 \cdot v_{c,k}(t) - 1]\frac{V_{DC}}{2} \\ v_{c,k} &= \frac{\bar{v_{kO}}(t)}{V_{DC}} + 0.5 \end{aligned} \tag{2.31}$$

The desired mean line-to-line voltages have been presented in Eq. 2.23. Combining the two expressions, Eq. 2.32 are obtained.

$$\begin{cases} v_{cA} = \frac{\hat{V}^* \sin(2\pi f_{sw})}{V_{DC}} + 0.5 \\ v_{cB} = \frac{\hat{V}^* \sin(2\pi f_{sw} - 2\pi/3)}{V_{DC}} + 0.5 \\ v_{cC} = \frac{\hat{V}^* \sin(2\pi f_{sw} + 2\pi/3)}{V_{DC}} + 0.5 \end{cases} \tag{2.32}$$

It is now crucial to discuss under which conditions the desired output is actually obtained. For this, two important quantities are introduced: the amplitude and frequency modulation indices.

$$\begin{aligned} m_a &= \frac{\hat{V}^*}{0.5 V_{DC}} \quad \text{Amplitude modulation index} \\ m_f &= \frac{f_{sw}}{f_o} \quad \text{Frequency modulation index} \end{aligned} \tag{2.33}$$

Here f_o is the frequency of the reference voltage (in this case it is the desired synchronous frequency f_s).

For the output mean voltage frequency to match the reference voltage frequency, it is suggested to have $m_f \geq 20$. The next question is what is the maximum mean output voltage amplitude obtainable given V_{DC}.

Being the duty cycle $d = T_{on}/T_s$, it cannot exceed 1. This is obtained for $\hat{V}^* = V_{DC}/2$, resulting in $m_a = 1$.

In this case, the modulation is linear and the inverter behaves as described in the previous section: the peak of the fundamental voltage equals the peak of the reference voltage, the common-mode voltage is null and the harmonics are grouped in sidebands around the switching frequency and its multiples.

In case the amplitude modulation index is increased above 1, the inverter operates in overmodulation: the duty cycle saturates at 0 and 1, becoming a trapezoidal waveform. This results in the loss of linearity, the introduction of low frequency harmonics which are responsible for a distorted output current.

The situation becomes even worse in the extreme case the duty cycle becomes a square wave, with the switches switching only once in the switching period. The inverter is said

to operate in square wave mode, and the amplitude of the fundamental component of the output is maximum, corresponding to $\hat{V}^*_{o,1,max} = 4/\pi \cdot V_{DC}/2$. This operating mode also generates the most distorted current.

Fig. 2.8 shows how the peak value of the fundamental voltage component varies in function of amplitude modulation index. [3]

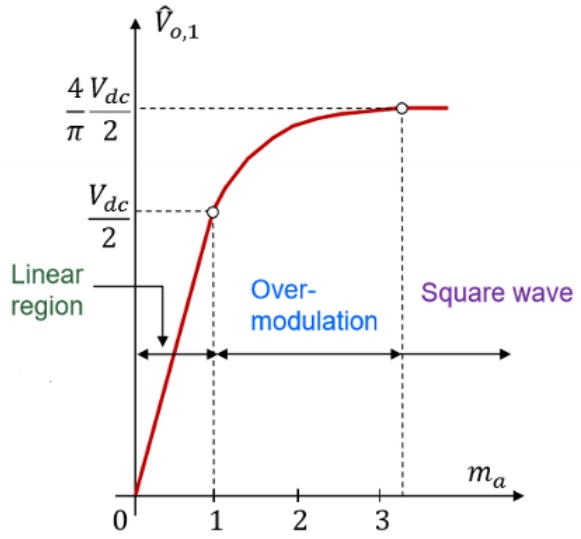


Figure 2.8: Fundamental voltage component as a function of modulation index in SPWM

The following discussion will only focus on the linear region operation of the inverter.

2.5 Space Vector Pulse Width Modulation (SVPWM)

SVPWM is one of the most recent trends for pulse generation. It is considered better approach as it provides flexibility to utilize pre-defined switching states for calculated time to minimize switching losses and low current ripple and increases the linear region. The peculiarity of this technique is that at a given instant only one leg will switch its state.

To analyze how the modulation technique works, it is first necessary to analyze what are the voltage space vectors in the $\alpha\beta$ frame corresponding to all the possible switching states of the inverter. As already stated, for each leg only one switch can be ON at a given instant: this leads to eight possible switching configurations, which are shown in Fig. 2.9.

Switches are considered ON when closed. A 3 bits binary number is assigned to each configuration, one for each inverter leg switch configuration from left to right. Each bit is 1 if the upper switch in the corresponding leg is close (hence, lower one is open) and 0 when the upper switch is open (lower one close).

Combining Eq. 2.20, 2.2 and Fig. 2.9, it is possible to retrieve Tab. 2.1.

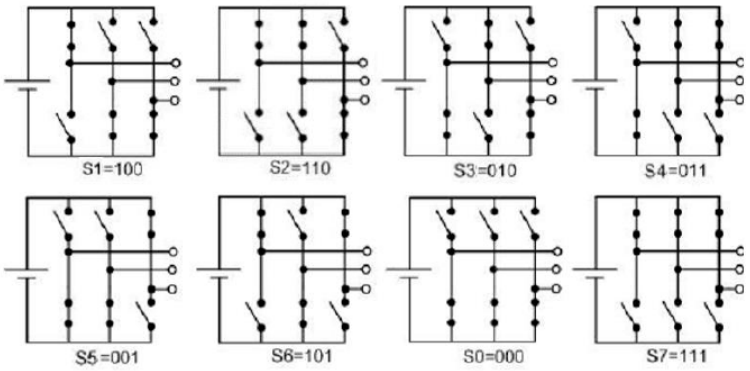


Figure 2.9: Switching configurations of a three-phase inverter

State	Switch ON	Binary sequence	v_a	v_b	v_c	$\vec{v_s}$
0	2,4,6	000	0	0	0	0
1	1,4,6	100	$\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$
2	1,3,6	110	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	$\frac{2}{3}V_{DC}e^{j\frac{\pi}{3}}$
3	2,3,6	010	$-\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}e^{j\frac{2\pi}{3}}$
4	2,3,5	011	$-\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}e^{j\pi}$
5	2,4,5	001	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$	$\frac{2}{3}V_{DC}e^{j\frac{4\pi}{3}}$
6	1,4,5	101	$\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}e^{j\frac{5\pi}{3}}$
7	1,3,5	111	0	0	0	0

Table 2.1: Phase voltages and space vectors on the basis on switching configuration

Fig. 2.10 shows all the achievable voltage space vectors can be represented on an hexagon.

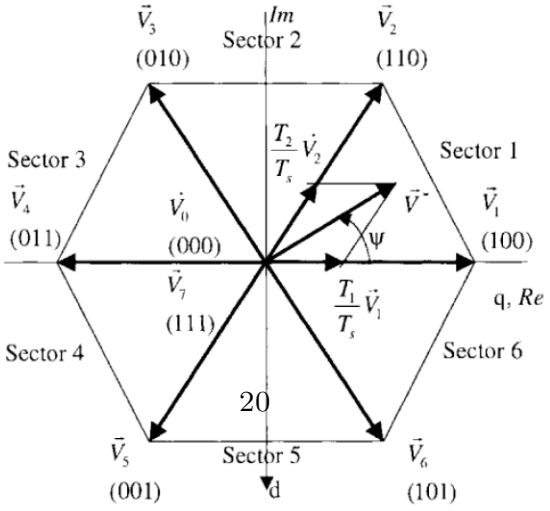


Figure 2.10: Space vector representation of the switch states

Also the reference voltage vector can be expressed in the $\alpha\beta$ frame. In particular, its amplitude and angular position are sampled every T_s. Each sampled reference vector will

and $\vec{V_2}$ the vectors at the edge of the sector, it is possible to write the following relation:

$$\vec{V^*}T_s = \vec{V_1}T_1 + \vec{V_2}T_2 \tag{2.34}$$

Bearing in mind that $|V_1| = |V_2| = V = 2/3V_{DC}$ and that the angle between V_1 and V_2 is $\pi/3$, the equation can be projected along the real axis, obtaining:

$$V^*T_s \cdot \cos(\theta) = VT_1 + VT_2 \cdot \cos(\frac{\pi}{3}) \tag{2.35}$$

Which, after trigonometrical rules are applied, leads to:

$$T_1 = \frac{V^*}{V}\frac{\sin(\frac{\pi}{3} - \theta)}{\sin(\frac{\pi}{3})}T_s \tag{2.36}$$

Similarly, projecting Eq. 2.34 along the imaginary axis:

$$V^*T_s \cdot \cos(\frac{pi}{2} - \theta) = VT_2 \cdot \cos(\frac{\pi}{2} - \frac{\pi}{3}) \tag{2.37}$$

Which analogously to the real axis case, leads to:

$$T_2 = \frac{V^*}{V}\frac{\sin(\theta)}{\sin(\frac{\pi}{3})}T_s \tag{2.38}$$

The values of T_1 and T_2 ensure the angular position of the obtained space vector output voltage matches the one of the reference voltage. The null vectors V_0 and V_7 are applied to modulate the amplitude of the output space vector.

$$T_{null} = T_0 + T_7 = T_s - (T_1 + T_2) \tag{2.39}$$

The following step is to sequence the time intervals computed. The general rule to limit the switching losses consists in admitting only one switching between 1 and 0 at each leg within a sampling period.

Fig. 2.11 shows one of the most popular solutions.

All the reasoning applied to the first sector can be extended to all the other sectors to retrieve the time slices. Tab 2.2 summarizes the results. [7]

Sector I	**Sector II**	**Sector III**
$(0 \leq \omega t \leq \frac{\pi}{3})$	$(\frac{\pi}{3} \leq \omega t \leq \frac{2\pi}{3})$	$(\frac{2\pi}{3} \leq \omega t \leq \pi)$
$T_1 = \frac{\sqrt{3}}{2}mT_s \cdot \cos(\omega t + \frac{\pi}{6})$ $T_2 = \frac{\sqrt{3}}{2}mT_s \cdot \cos(\omega t + \frac{3\pi}{2})$ $T_0 + T_7 = T_s - T_1 - T_2$	$T_2 = \frac{\sqrt{3}}{2}mT_s \cdot \cos(\omega t + \frac{11\pi}{6})$ $T_3 = \frac{\sqrt{3}}{2}mT_s \cdot \cos(\omega t + \frac{7\pi}{6})$ $T_0 + T_7 = T_s - T_2 - T_3$	$T_3 = \frac{\sqrt{3}}{2}mT_s \cdot \cos(\omega t + \frac{3\pi}{2})$ $T_4 = \frac{\sqrt{3}}{2}mT_s \cdot \cos(\omega t + \frac{5\pi}{6})$ $T_0 + T_7 = T_s - T_3 - T_4$
Sector IV	**Sector V**	**Sector VI**
$(\pi \leq \omega t \leq \frac{4\pi}{3})$	$(\frac{4\pi}{3} \leq \omega t \leq \frac{5\pi}{3})$	$(\frac{5\pi}{3} \leq \omega t \leq 2\pi)$

$T_4 = \frac{\sqrt{3}}{2} m T_s \cdot \cos(\omega t + \frac{7\pi}{6})$	$T_5 = \frac{\sqrt{3}}{2} m T_s \cdot \cos(\omega t + \frac{5\pi}{6})$	$T_6 = \frac{\sqrt{3}}{2} m T_s \cdot \cos(\omega t + \frac{\pi}{2})$
$T_5 = \frac{\sqrt{3}}{2} m T_s \cdot \cos(\omega t + \frac{\pi}{2})$	$T_6 = \frac{\sqrt{3}}{2} m T_s \cdot \cos(\omega t + \frac{\pi}{6})$	$T_1 = \frac{\sqrt{3}}{2} m T_s \cdot \cos(\omega t + \frac{11\pi}{6})$
$T_0 + T_7 = T_s - T_4 - T_5$	$T_0 + T_7 = T_s - T_5 - T_6$	$T_0 + T_7 = T_s - T_1 - T_6$

Table 2.2: Time slices computation at each sector

One interesting consideration can be carried out regarding the maximum amplitude of the reference phase vector. To retrieve this value in the linear modulation range, it is sufficient to impose $T_{null} = 0$. Choosing $T_1 = T_2 = T_s/2$ leads to $\theta = \pi/6$. Substituting in Eq. 2.38:

$$\begin{aligned} \frac{T_s}{2} &= \frac{V^*}{\frac{2}{3}V_{DC}} \frac{\frac{1}{2}}{\frac{\sqrt{3}}{2}} T_s \\ 1 &= \frac{V^*}{V_{DC}} \sqrt{3} \\ V^* &= \frac{V_{DC}}{\sqrt{3}} \end{aligned} \tag{2.40}$$

Considering the same simulations conditions presented in 2.3, except that $\vec{V^*} = \frac{V_{DC}}{\sqrt{3}} = 230V$ and the modulation technique changed to SVPWM, it is possible to visualize the waveform of the modulating signal in Fig. 2.12.

The maximum amplitude modulation index without saturating the duty cycle becomes:

$$m_a = \frac{\frac{V_{DC}}{\sqrt{3}}}{\frac{V_{DC}}{2}} = 1.154 \tag{2.41}$$

Hence, it is possible to conclude the inverter linear region is extended by 15.4% if SVPWM technique is employed. [3]

In general, the inverter operates:

- In linear modulation region if the reference voltage is within a circle of radius $V_{DC}/\sqrt{3}$;
- In overmodulation region if the referene voltage is in the region between the circle and the hexagon;
- In six step operation if the reference voltage matches the six non-null voltages.

This technique is used in the experimental implementation.

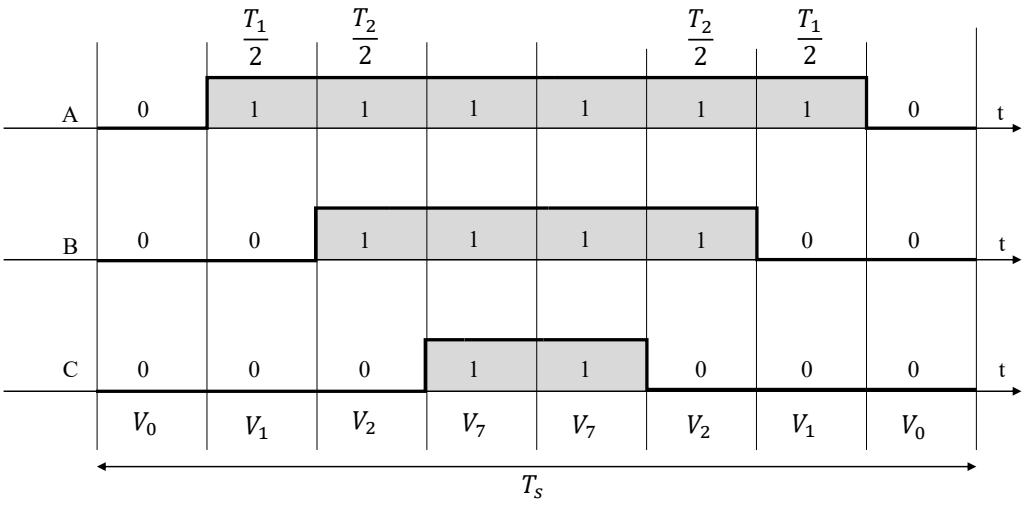


Figure 2.11: Time slices sequence

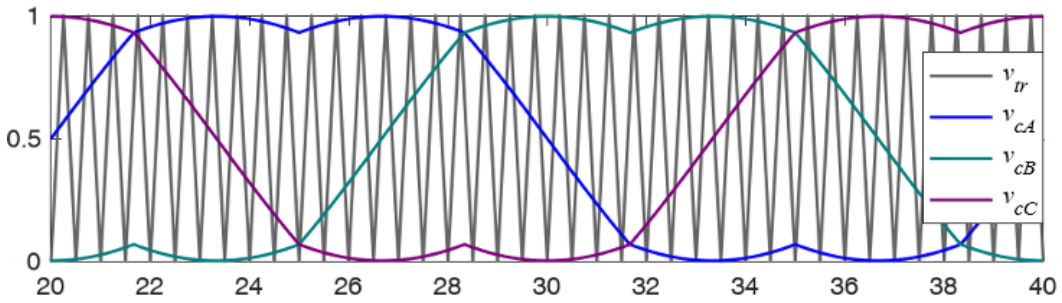


Figure 2.12: Comparison between carrier and referece voltage in SVPWM [3]

2.6 Controlled start-up of PMSM motors

PMSM motors offer all the advantages presented in Section 1.2. Since PMSM motors are synchronous machines, effective motion of the rotor is achieved only if the magnetic field of the latter is synchronized with the magnetic field of the stator. Therefore, the fundamental requirement in control design of PMSMs is the assurance of precise synchronization of machine's excitation with the rotor frequency, even if the requirement is as simple as getting the motor to spin at low speed with no load. The direct approach to achieve this requirement is the continuous measurement of the absolute rotor angular position. For this reason, it is usually used in the high precision case because of the cost of the position sensors. [2] [11].

V/f control is an effective way for general applications, and is particularly popular in the case of induction motors, as it offers the possibility to operate at high speeds without the need of any position sensor [9].

However, V/f control approach to the PMSMs without having rotor cage windings requires rotor frequency (rotor speed) information in order to achieve the synchronization

between AC excitation frequency and rotor frequency. This makes the design of V/f control for PMSMs somewhat difficult. In order to make this controller stable without any feedback different techniques have been studied: the most popular involve controlling the voltage vector to remain in phase with the current vector [1], [12].

This makes the V/f control unsuited if the aim is just to start the motor and have it spin at low speed.

A simpler technique presented in this section is the I/f, which gives the opportunity to spin the motor with no load applied and validate a closed loop control on the three phase currents through the help of the current sensors.

2.7 V/f control

V/f Scalar Control is the term used to describe a very basic form of motor control that is using a non-vector approach scheme.

V/f control is an effective way for general applications, and is particularly popular in the case of induction motors, as it offers the possibility to operate at high speeds without the need of any position sensor [9].

To explain this technique, it is necessary to recall Eq. 2.11.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = R_s \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \lambda_d \\ \lambda_q \end{bmatrix} + \omega \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \lambda_d \\ \lambda_q \end{bmatrix}$$

In steady state regime, the flux linkage variation is zero, and for further simplification the stator winding resistance is assumed negligible. Taking into consideration these simplifications and recalling flux linkage equations 2.13, it is possible to retrieve:

$$\begin{cases} V_d = -\omega L_q i_q \\ V_q = \omega L_d i_d + \omega \lambda_m \end{cases} \tag{2.42}$$

The context in which this control technique is considered is with no load attached to the motor, leading to no necessity of torque production and, hence, $i_q = 0$. In order to minimize the losses, also $i_d = 0$.

Under these assumptions it is possible to rewrite equation 2.13 as:

$$\begin{cases} V_d = 0 \\ V_q = \omega \lambda_m \end{cases} \tag{2.43}$$

Transforming the electrical speed in frequency according to $\omega = 2\pi f$:

$$\left\{ \frac{V_q}{f} = 2\pi \lambda_m \right. \tag{2.44}$$

In this case, the applied voltage must only compensate the EMF in the q axis. [10]

In V/f scalar control method the frequency of the stator magnetic flux is set according with the desired synchronous rotor speed while the magnitude of the stator voltage is adjusted to keep the ratio between them constant. No control over voltage or current vectors angles is utilized, hence the name scalar control. The drive does not require any

feedback and is used in low performance applications where precise speed control is not required. [5]

The V/f ratio is calculated from the nominal values of the PMSM voltage and frequency parameters. However, in practice a typical V/f profile is not constant over the entire range of motor speed: in fact, , when the frequency and hence also the voltage are low, the voltage drop across the stator resistance cannot be neglected and must be compensated. At frequencies higher than the rated value, the constant V/f principle also have to be violated because, to avoid insulation break down, the stator voltage must not exceed its rated value. [14]

As a result, the V/f profile can be divided in three regions:

- Compensation: a higher than normal voltage is required to compensate the voltage drop across the stator resistance that was neglected for simplified mathematical model;
- Linear: Constant V/f relation;
- Field weakening: constant V/f ratio cannot be satisfied due to the stator voltages limitation at the rated value in order to avoid insulation breakdown.

Fig. 2.13 shows the profile.

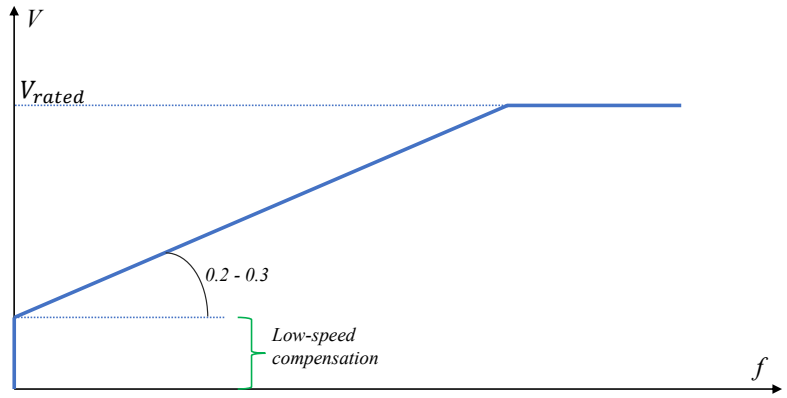


Figure 2.13: V/f profile

The schematic of the control is shown in Fig. 2.14.

By using V/f scalar control there is no need for high capability CPU, but the disadvantages of this simplicity include:

- Instability of the system after exceeding a certain applied frequency;
- Systems low dynamic performance, which limits the use of this control method;
- Poor fault protection against stall detection and over-currents.

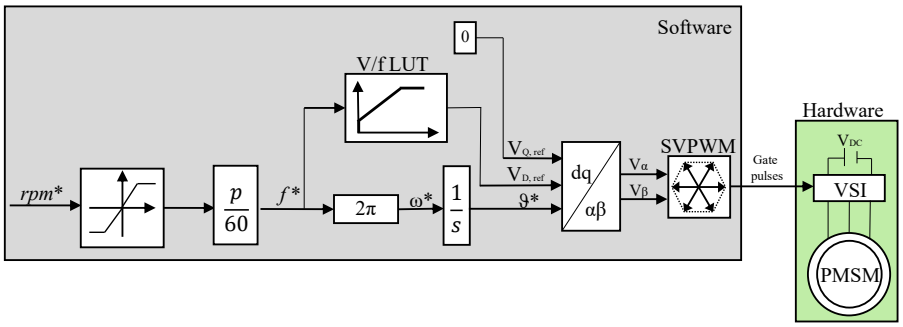


Figure 2.14: Schematic of V/f control

2.8 I/f control

The I/f technique implemented is based on current vector representation. As already presented in Section 2.1, in the case of a PMSM, the d-axis corresponds with the direction of the magnetic field of the rotor (produced by the permanent magnets). By design, the rotor magnetic field will tend to align with the rotating magnetic field generated by the stator currents. The direction of vector I_s corresponds with the direction of the north pole of the stator rotating field: imposing $I_q = 0$ and $I_d > 0$, it is possible to directly impose the direction of the stator magnetic field to always be in d-axis so that the rotor can follow it. Fig. 2.15 shows the control schematic.

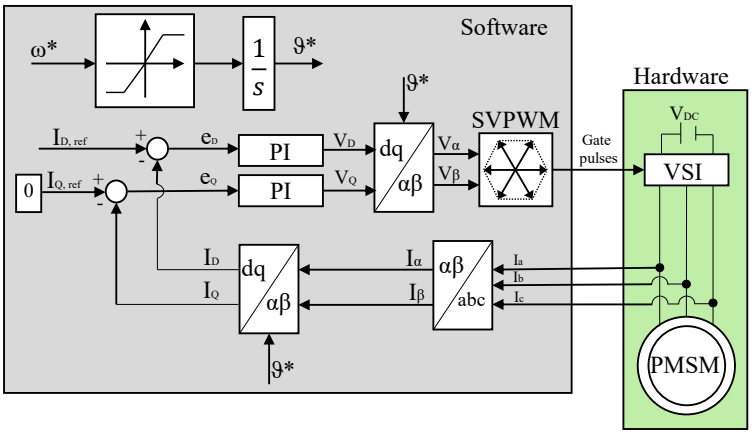
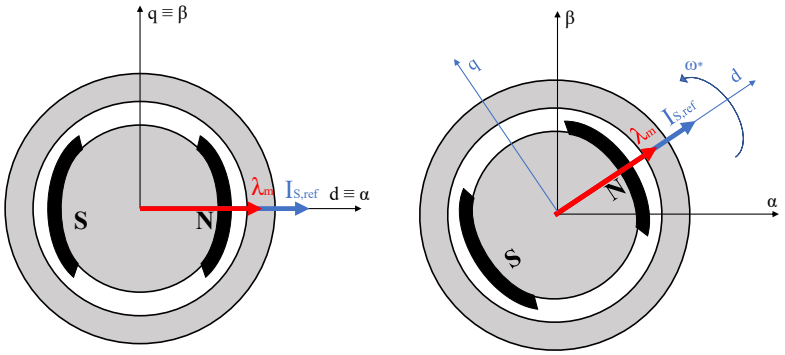


Figure 2.15: Schematic of I/f control

In practice, the control technique consists in first imposing $I_d = I_{rated}/2, I_q = 0$ and output frequency to 0, so that the rotor will align in position $\theta = 0$. After this, the output frequency will linearly increase maintaining $I_q = 0$, starting the rotation of vector I_d. The rotor will follow the rotation of the vector, hence it will start spinning.

As I_q is set to be at 0 for all frequency values, no torque will be produced: it is



(a) *Before frequency ramp start* (b) *During frequency linear increase*

Figure 2.16: Vector representation of I/f technique

fundamental no load is connected to the motor shaft, otherwise accordingly to Eq. 2.19, an acceleration will be produced on the shaft such that the synchronism is lost.

Furthermore, it is good practice not to impose high currents while the frequency (and hence, according to Eq. 2.11, the voltage provided) is increasing: the output power is 0, and all the power provided to the motor will be dissipated as heat.

2.9 Design of the current loop

The block diagram of the current loop is shown in Fig. 2.17.

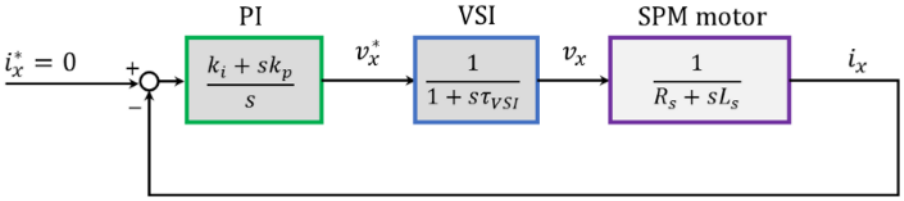


Figure 2.17: Block diagram employed for the design of PI compensators [3]

Where the PMSM transfer function is retrieved from Eq. 2.11, neglecting the speed term. The result is:

$$i_x = \frac{v_x}{R_s + sL_s} \qquad x = \{d, q\} \tag{2.45}$$

The VSI block models the inverter behaviour in the frequency domain. Ideally, the transfer function of converters is unitary, but in reality they always introduce some delay of the order of the switching frequency at which they are operated. Such behaviour can be approximated by a first order low-pass filter:

$$H_{VSI} = \frac{1}{1 + s\tau_{VSI}} \qquad \tau_{VSI} = 1.5 \cdot T_s \tag{2.46}$$

Lastly, the transfer function of a PI block is:

$$H_{PI} = \frac{k_i + sk_p}{s} \tag{2.47}$$

The resulting open-loop transfer function is:

$$\left.\frac{i_x}{i_x^*}\right|_{OL} = \frac{k_i + sk_p}{s} \cdot \frac{1}{1 + s\tau_{VSI}} \cdot \frac{1}{R_s + sL_s} \tag{2.48}$$

The resulting bode plots of both the open and closed loop are shown in Fig. 2.18.

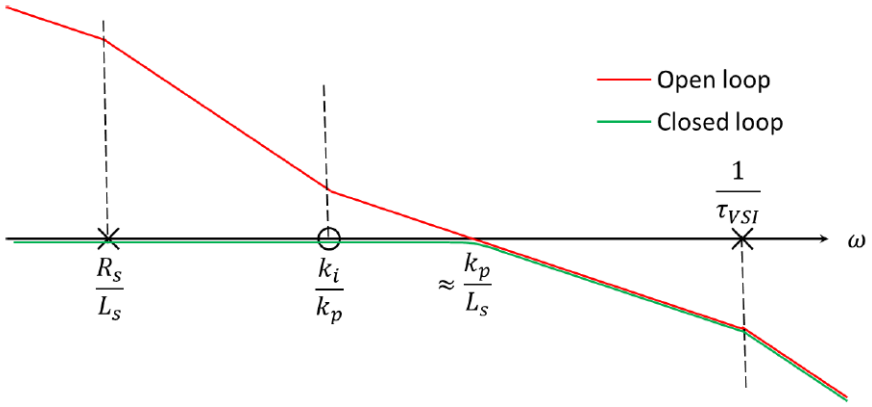


Figure 2.18: Open-loop and Closed-loop bode plots of the current loop [3]

The bandwidth of the system is approximately

$$w_b = \frac{k_p}{L_s} \tag{2.49}$$

It is important it meets the requirement for correct operation:

$$w_b = 2\pi f_b \ll 2\pi f_{sw} \tag{2.50}$$

Combining the two equations:

$$k_p = L_s w_b \tag{2.51}$$

The relation through which k_i is chosen is:

$$k_i \ll k_p w_b \tag{2.52}$$

Another aspect of paramount importance is ensuring the reference current does not exceed the maximum allowed current.

$$|i_{dq}| \leq I_{max} \qquad i_d^2 + i_q^2 \leq I_{max}^2 \tag{2.53}$$

Where the value of I_{max} can be chosen either from the maximum current capability of the inverter or from the maximum rated current of the motor of from the maximum peak current of the motor, depending on the application.

Based on this equation, the reference currents become;

$$i_d^* = \begin{cases} i_d^* & \text{if} \quad |i_d^*| \leq I_{max} \\ I_{max} & \text{if} \quad |i_d^*| > I_{max} \end{cases} \qquad i_q^* = \begin{cases} i_q^* & \text{if} \quad |i_q^*| \leq \sqrt{I_{max}^2 - i_d^{*2}} \\ \sqrt{I_{max}^2 - i_d^{*2}} & \text{if} \quad |i_q^*| > \sqrt{I_{max}^2 - i_d^{*2}} \end{cases} \tag{2.54}$$

Similarly, also the inverter voltage-production capabilities in linear operation must not exceeded by the value of v_{dq}^* computed by the PI compensators.

$$\begin{gathered} |v_{dq}| \leq V_{max} \qquad V_{max} = \frac{V_{DC}}{\sqrt{3}} \\ v_d^2 + v_q^2 \leq V_{max}^2 \end{gathered} \tag{2.55}$$

Based on this equation, the output of the PI compensators become:

$$v_d^* = \begin{cases} v_d^* & \text{if} \quad |v_d^*| \leq V_{max} \\ V_{max} & \text{if} \quad |v_d^*| > V_{max} \end{cases} \qquad v_q^* = \begin{cases} v_q^* & \text{if} \quad |v_q^*| \leq \sqrt{V_{max}^2 - v_d^{*2}} \\ \sqrt{V_{max}^2 - v_d^{*2}} & \text{if} \quad |v_q^*| > \sqrt{V_{max}^2 - v_d^{*2}} \end{cases} \tag{2.56}$$

2.10 Field oriented control

Field oriented control (FOC) is a control technique is a widely used in the last thirty years with SMPM motors as it operates smoothly and provides maximum torque, full speed range and instantaneous acceleration and deceleration.

The inverter acts as a current regulated voltage source. In fact, the reference voltages are generated to impose the reference stator current vector i_{dq}^* needed to obtain the desired reference torque T^*.

In the case of a SMPM motor, the relation between torque and current is shown in Eq. 2.18.

Given the relation, it is possible to retrieve the reference currents as:

$$\begin{cases} i_d^* = 0 \\ i_q^* = \frac{T^*}{\frac{3}{2} p \lambda_m} \end{cases} \tag{2.57}$$

Where the term $\frac{3}{2} p \lambda_m$ is usually assumed constant (even though it varies with temperature) and collected in the term K_t.

The torque is entirely controlled via the i_q component, it is crucial to set the q-direction component to zero as otherwise it would only increase the joule losses in the machine without adding any contribution to the mechanical torque production.

The schematic of the control technique is shown in in Fig. 2.19.

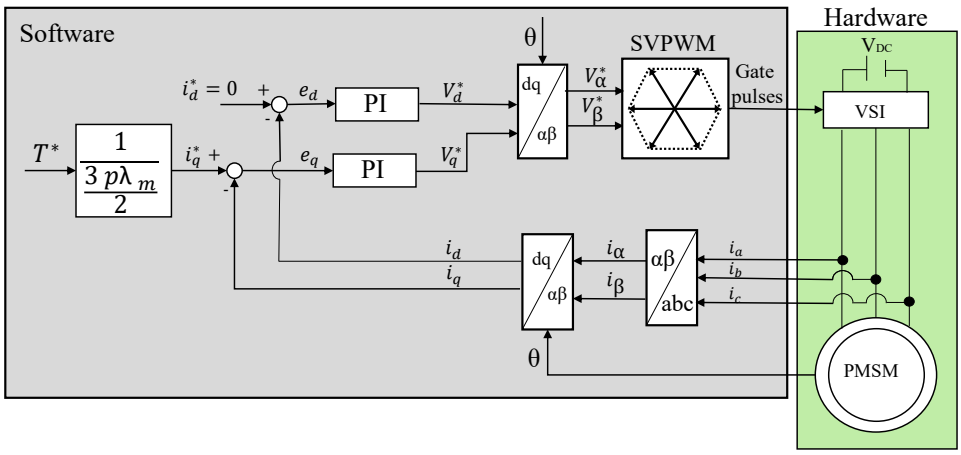


Figure 2.19: FOC schematic

As shown in the schematic, for the FOC to correctly work, it is required to have current and position feedback.

The position feedback is needed to ensure the synchronization between the stator and rotor magnetic fields to operate at high speed.

Moreover, λ_m and L_s must be known: as they are not constant in the usual operating ranges, they can either be thoroughly retrieved through tests on the motor or estimations (provided in the datasheet) can be employed. In this application, the latter option is chosen.

The design of the PI current compensators is the same presented in Sec. 2.9.

The complete motor model (with the mechanical model) are shown in Fig. 2.20.

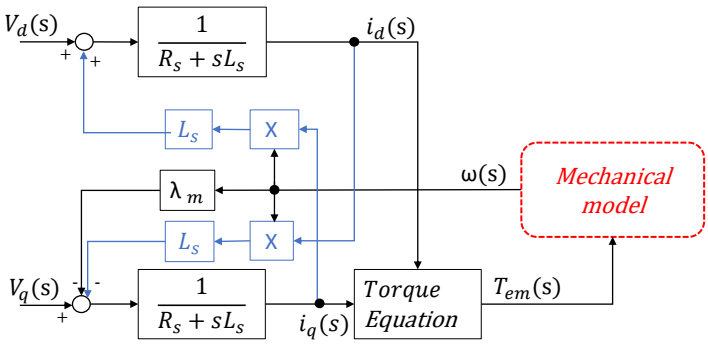


Figure 2.20: Motor model and mechanical model of SMPM motor [3]

As the transfer function for the current loop neglects the motional term, for performance enhancement it is good practice to include this contribution. In fact, at steady state for medium-high speed the voltage is mainly given by this contribution.

$$\begin{cases} v_d \approx -\omega\lambda_q \\ v_q \approx \omega\lambda_d \end{cases} \tag{2.58}$$

This term can be feed-forwarded at the output of the PI regulators, resulting in faster dynamic and compensation of cross coupling. The control schematic, updated including this term, is shown in Fig. 2.21.

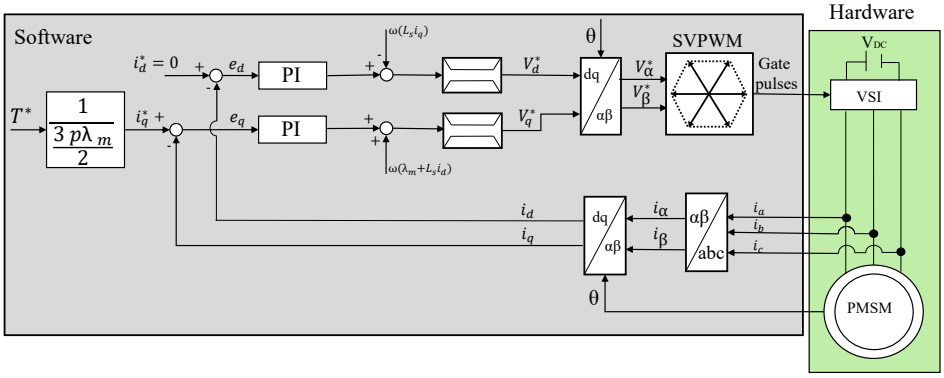


Figure 2.21: FOC schematic with feed-forward and saturation terms

For the correct computation of the feed-forward term, a flux observer must be implemented.

What has been presented so far works under the assumption that the speed at which the motor is spinning is below the so called "base speed", which is the speed that can be reached with the rated flux amplitude without exceeding the voltage limit imposed by V_{DC}.

The motor can actually be rotated faster than the base speed, decreasing the flux amplitude (and hence the maximum achievable torque). This range of operation (in which i_d is no longer 0) is called "flux weakening". Operating above the base speed is out of the scope of this thesis work.

Chapter 3

Test bench setup

3.1 Design of the bus capacitor

3.1.1 Reasons for introducing a Bus Capacitor

As motor drive systems are usually battery powered, it is important to ensure safe operating conditions, preventing high frequency current harmonics from flowing inside the battery itself. Furthermore, it is also necessary to ensure constant voltage at the input of the inverter regardless of any fluctuations in the battery.

3.1.2 Bus Capacitor design

To preserve the battery and ensure stable voltage at the inverter input, placing one (or more) capacitors in parallel with the battery, between *DC pos* and *DC neg* inverter buses is good practice. DC bus capacitors in motor drives need to deal with the following problems:

- Ripple current due to inverter switching;
- Voltage fluctuations due to the source lead inductance;
- Voltage transient due to leakage inductance and fast device switching;
- Over voltage due to regeneration.

The capacitance needed to deal with the first three problems may not be high, but the current handling capability and frequency response of the capacitor are significant concerns.

To properly choose the capacitor, the operating conditions of the inverter must be specified.

$$500V \leq V_{DC} \leq 800V \quad I_{MOS_{pk}} < 15A \quad f_{sw} > 10kHz$$

The range of voltage is determined by the rated voltage of the motor in use: in this case 500V is sufficient, but the same setup is also intended to be used with a motor with a higher rated voltage. The peak value limit for the SiC MOSFET current is chosen to

be 15 A_{pk}: looking at its datasheet, it can withstand a current of $20A_{rms}$, but both for safety reasons and because no more than that is needed for our application it has been decided to limit it.

The worst operating conditions in terms of components stress are:

$$V_{DC} = 500V \quad I_{MOS_{pk}} = 15A \quad f_s = 10kHz$$

Given these parameters, it is possible to set the requirements for the input capacitor.

- $V_{C_{ripple,p2p}} = 1\%\ V_{DC}$
- Reduce as much as possible the current ripple on the battery.

From the first requirement, the ripple RMS voltage value is retrieved in Eq. 3.1.

$$V_{C_{ripple,RMS}} = \frac{V_{DC}}{100 \cdot \sqrt{12}} = 1.4V_{rms} \tag{3.1}$$

Moving to the current requirement, the worst condition in terms of current ripple for the battery is of course when maximum current is flowing through the MOSFET.

With all this information, what remains is finding an appropriate value for the capacitance. It can be shown that the RMS value of the current flowing in the capacitor is 0.613 the RMS value of the current flowing through each load phase.

$$I_{C,RMS} = 0.613 \cdot \frac{I_{O,pk}}{\sqrt{2}} = 6.5A_{rms} \tag{3.2}$$

Combining Eq. 3.1 and Eq. 3.2, the needed capacitor impedance is shown in Eq. 3.3.

$$Z_C = \frac{V_{C_{ripple,RMS}}}{I_{C,RMS}} = 0.22\Omega \tag{3.3}$$

Knowing the impedance, the frequency to filter must be chosen. As shown in Fig. 3.5, the main harmonics are at f_{sw}. Eq. 3.4 shows the theoretical needed capacitance value.

$$C = \frac{1}{2\pi f_{sw} \cdot Z_C} = 71.67\mu F \tag{3.4}$$

Looking at what is already available in the laboratory, the final choice fell on placing two film capacitors in parallel:

$$\boxed{C_1 = 52\mu F \quad C_2 = 22\mu F}$$

Both capacitors can withstand more than $1200V_{DC}$ and $50A_{rms}$. It is preferred to employ film capacitors for their compactness, longer life span, and lower on resistance. Their datasheet can be found at C_1 datasheet and C_2 datasheet.

3.1.3 Design validation

To validate the design, the system is simulated on PLECS, as shown in Fig. 3.1.

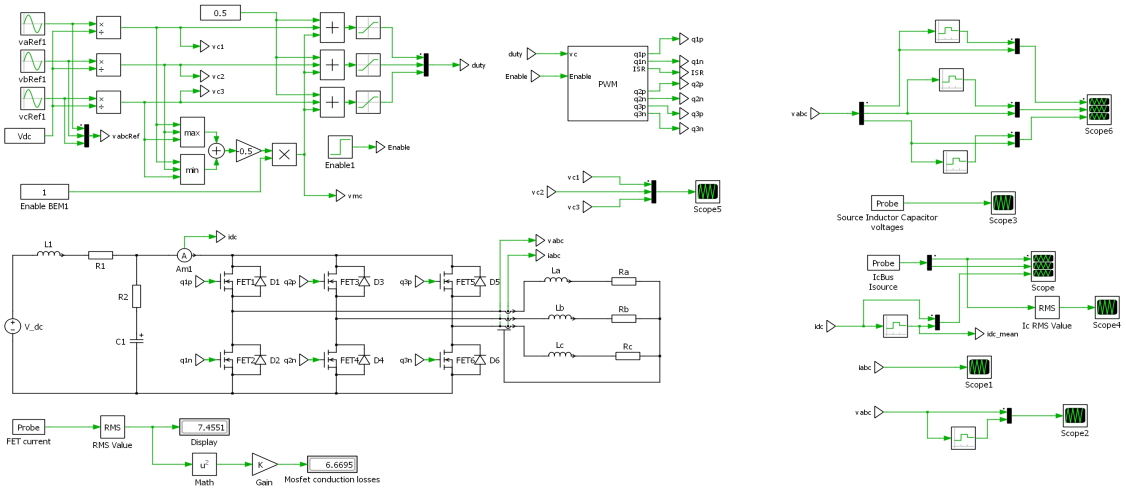


Figure 3.1: Schematic of the circuit to validate capacitance choice

In pursuance of ensuring the test condition current flows through the MOSFETs and hence the load, the RL load must be designed with adequate voltage reference.

The reference is a three-phase balanced sinusoidal reference with amplitude $V_{ref} = \frac{V_{DC}}{\sqrt{3}}$ (which is the maximum obtainable with the designed V_{DC} in linear region considering SVPWM modulation technique) and 50 Hz frequency. Assuming a load power factor of 0.97, it is possible to retrieve the needed values as follows:

$$\begin{cases} \phi = \arccos(PF) \\ V_{O,real} = V_{ref}\cos(\phi) \\ V_{O,img} = V_{ref}\sin(\phi) \\ X_L = \frac{V_{O,img}}{I_{O,pk}} \\ L_{phase} = \frac{X_L}{2\pi \cdot f_s} \\ R_{phase} = \frac{V_{O,real}}{I_{O,peak}} \end{cases}$$

The input inductance and resistor shown in Fig. 3.1 model the parasitics of the cable connecting battery to the inverter, the resistor in series with the capacitance model the sum of their parasitic resistances.

First of all, from Fig. 3.2 the phase current and voltage measurements match the values we imposed, confirming the test is performed under the right conditions.

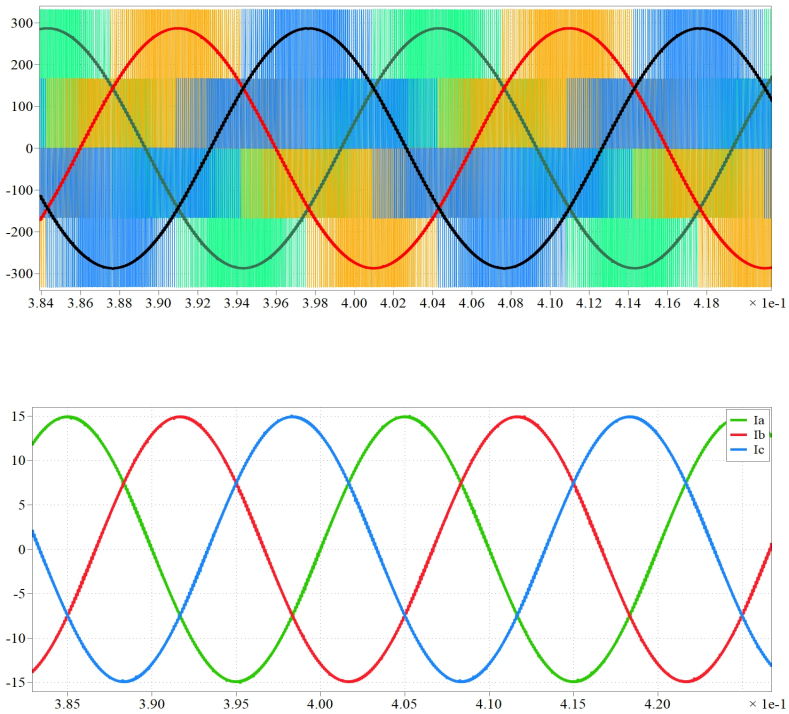


Figure 3.2: Three-phase voltages and currents

Moving to the requirements side, Fig. 3.3 shows that at steady state the voltage ripple requirement is more than fulfilled, having asked for 1% and obtaining 0.2%.

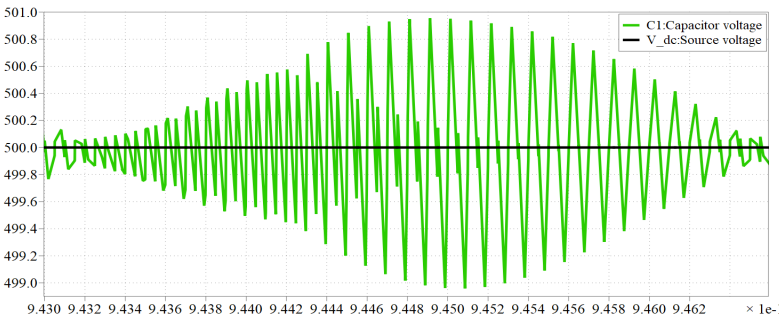


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Figure 3.3: Voltage across the battery and input capacitor

For what concerns the currents, the impressive contribution of introducing the input capacitor is shown in Fig. 3.4.

In fact, without the capacitor, the battery would be subject to the current flowing in the positive bus (shown in the bottom plot in blue), which could damage it in the long run. Instead, adding the capacitor, the ripple is reduced to 0.32%, with a calculated THD of 0.46. Fig. 3.5 shows the FFT (with fundamental frequency at f_s) of the currents shown in Fig. 3.4.

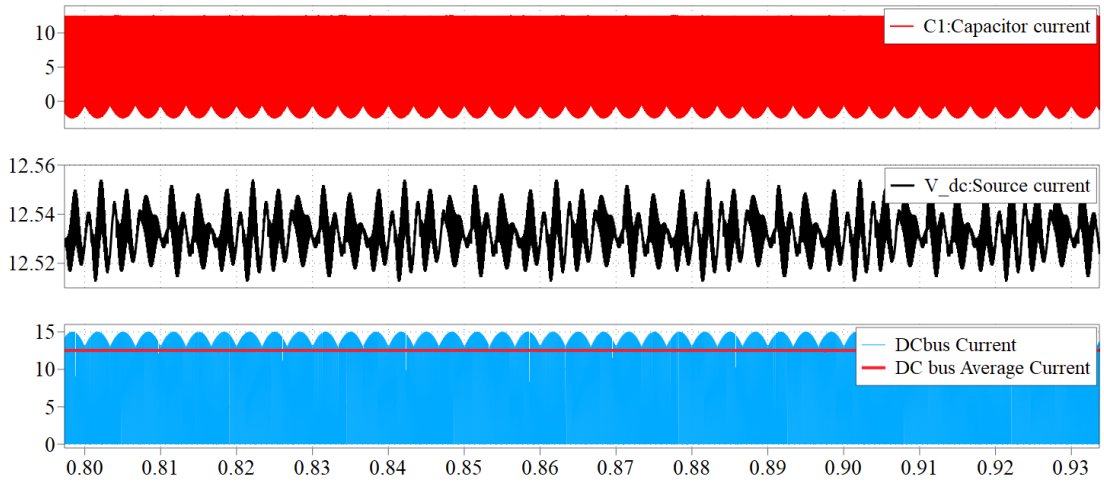


Figure 3.4: Currents flowing in the capacitor, battery and positive bus

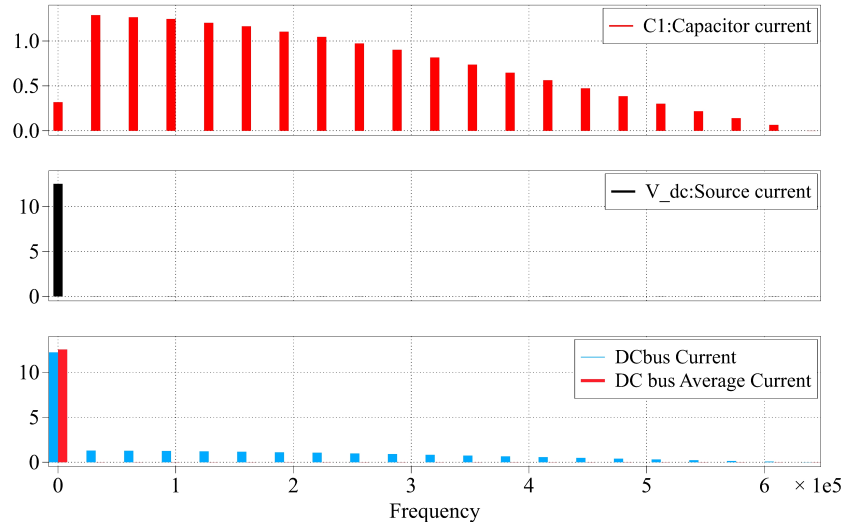


Figure 3.5: FFT of currents flowing in capacitor, battery and positive bus

Looking again at the bottom plot, it can be seen that the dominant distorting harmonic is at f_{sw}, confirming the reasoning behind Eq. 3.4.

Fig. 3.5 also proves that it is the capacitor that absorbs all the harmonics, leaving an almost perfect battery current.

3.2 Test of the gate driver

Before soldering the gate driver to the inverter module, it is crucial to ensure it is properly working. In particular, the test is performed on CGD15FB45P1 Six Channel 1200V SiC

MOSFET Driver. Its datasheet can be found at CGD15FB45P1 datasheet.

Fig. 3.6 shows the gate driver.

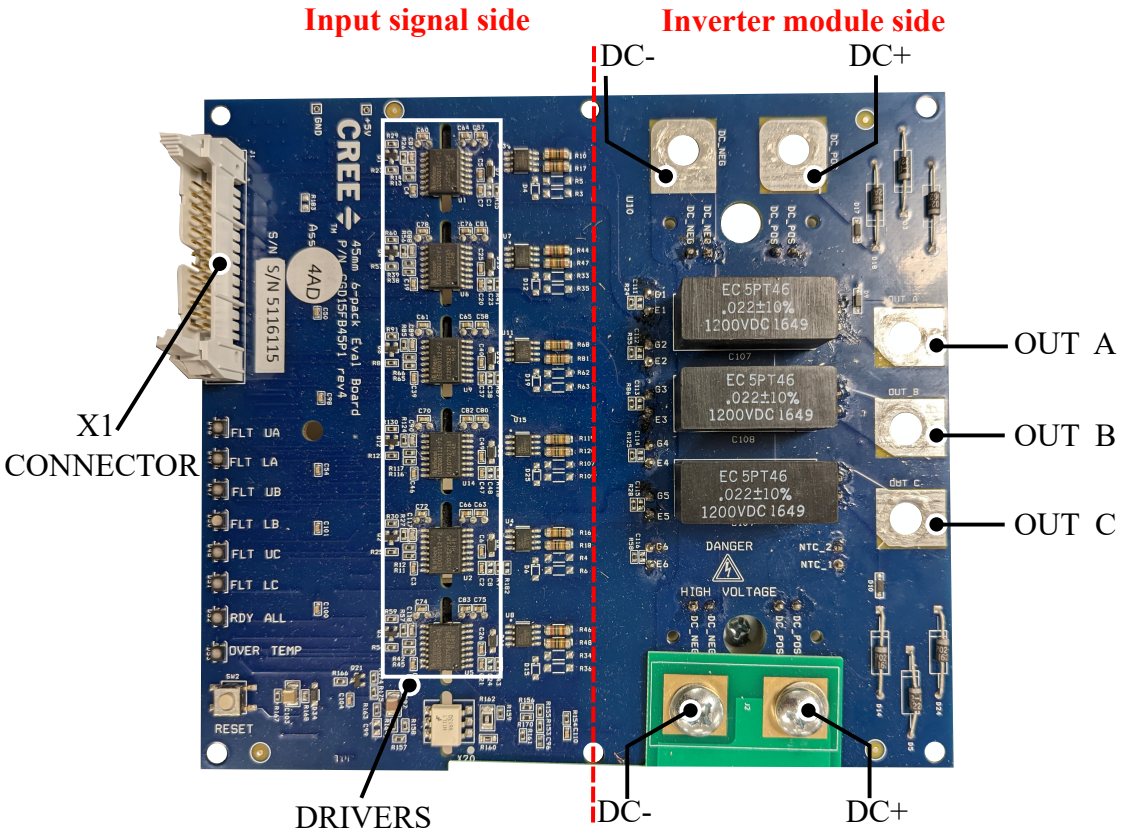


Figure 3.6: Overview of the Gate Driver

The inverter should be placed in the *inverter module side* in correspondence with the dedicated holes. It is important to notice the *Input signal* (bottom side) and the *Module Interface*(upper side) are electrically isolated: this is important to grant the safety of one side in case of failure of the other. Such isolation should never be broken. This gate driver comes with overtemperature and desaturation fault protections.

The fundamental points to be tested include:

- Correct voltage levels for the supplies at Signal Interface side and Module interface side;
- Correct transmission of PWM waveforms at both Signal and Module interfaces;
- Correct voltage levels for the fault detection pins.

First of all, the datasheet specifies all the signals the board needs at the *X1* connector. They are shown in Fig. 3.1.

1	PWM Upper A (5V Logic)	**2**	COMMON
3	PWM Lower A (5V Logic)	**4**	COMMON
5	PWM Upper B (5V Logic)	**6**	COMMON
7	PWM Lower B (5V Logic)	**8**	COMMON
9	PWM Upper C (5V Logic)	**10**	COMMON
11	PWM Lower C (5V Logic)	**12**	COMMON
13	RST (normally hi)	**14**	COMMON
15	RDY (normally hi)	**16**	COMMON
17	DESAT FAULT (normally low)	**18**	COMMON
19	OVER TEMP FAULT	**20**	COMMON
21	PWR In (V_s)	**22**	COMMON
23	PWR In (V_s)	**24**	COMMON
25	PWR In (V_s)	**26**	COMMON

Table 3.1: Pin map for X1 connector

Still looking at the datasheet, this Gate Driver requires an external supply of 15V. Pins 13-15-17-19 should be left floating, as their value will be changed by internal circuits in case of detected faults. All even pins should be grounded.

It becomes now essential to locate the points at which we should take our measurements. The most crucial element is Infineon 1ED020I12-F2 driver. We can find six of them (one per MOSFET): this component is the core of the gate driver and is the bridge between the input and inverter module sides, as it is in charge of conveying the signal from the DSP to the MOSFETs adjusting the voltage levels. Its datasheet can be found at 1ED020I12-F2 datasheet.

The function of its pins and its application circuit is shown in Fig. 3.7.

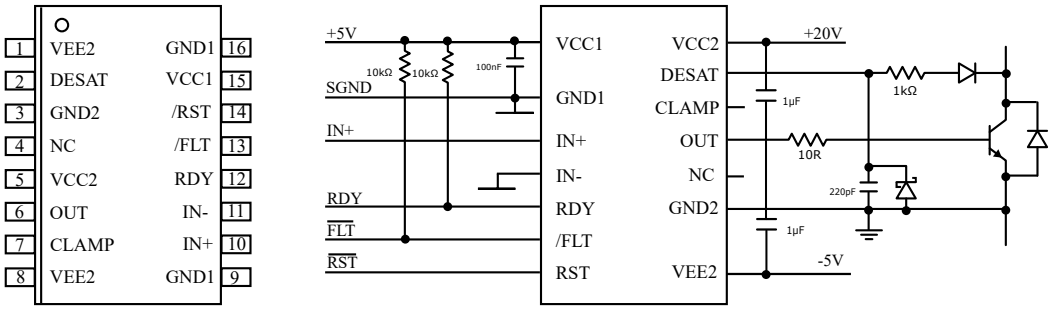


Figure 3.7: Infineon 1ED020I12-F2 pins scheme and bipolar voltage application circuit

The component in charge of adapting the 15V of the supply to the 5V needed to supply the Signal interface side is MC7805CD2TR4G linear voltage regulator. Instead, what adapts voltage levels between the Signal interface side and Module interface side is QA01C DC-DC converter: the +5V/0V levels of the DSP are converted into +20V/-5V needed by MOSFETs.

Hence, referring to Fig. 3.7 and 3.1, the voltage levels for each pin reported in Tab. 3.2 are retrieved. Both GND1 and GND2 do not have specified voltage levels as they are used as references (being the two sides isolated, they are not at the same value) for each side (pins 1 to 8 are for the module interface side, 9 to 16 for signal interface side).

Pin	**Voltage level**	**Pin**	**Voltage level**
1	-5V	16	GND1
2	-5V (No fault)	15	5V
3	GND2	14	5V (No fault)
4	Not connected	13	0V (No fault)
5	20V	12	5V (if supply is correct)
6	15V(High) -5V(Low)	11	0V (High) 5V (Low)
7	-5V	10	5V(High) 0V(Low)
8	-5V	9	GND1

Table 3.2: Infineon 1ED020I12-F2 voltage levels at each pin

Referencing Tab. 3.2, it becomes possible to check the correctness of the supply levels at the two sides through the use of an oscilloscope.

Once the supply levels are checked, all PWM pins of the X1 connector are fed with 1kHz square waves with D = 0.5 generated by a signal generator. The procedure to verify the signals are correctly propagated to the Inverter module involves checking pin 10 and pin 6 of each Infineon 1ED020I12-F2 driver and all $V_{G_iE_i}$ on the module interface.

Unfortunately, as soon as the output of the signal generator is connected to the X1 connector, a saturation fault occurs. Having a glance at the datasheet of the driver, further information about this fault is provided.

Monitoring of the IGBT saturation voltage (V_{CE}) to detect desaturation caused by short circuits. If OUT is high, V_{CE} is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

In practice, this fault arises because the inverter is not connected to the gate driver, leaving the drain source (called in the datasheet collector-emitter as the same driver can be used for IGBTs) floating: when the PWM signal turns high, the voltage between drain and source would still not go to zero as there is no physical switch soldered yet, activating the desaturation. To continue the test, it is necessary to manually short circuit source pins with DC+ for the upper switches and source pins with DC- for the bottom switches. By doing so, the fault does not appear anymore and the test can be completed.

Besides avoiding any future trouble related to malfunctionings in the board, this test also represents a good way to better familiarize and understand how gate drivers work and how they handle faults.

After having ensured the gate driver is working properly, the inverter is soldered in the specific pins. Furthermore, an heatsink with a fan for active cooling is placed below

the inverter with the use of thermal paste to avoid overheating while operating. Fig. 3.8 shows a view of the whole.

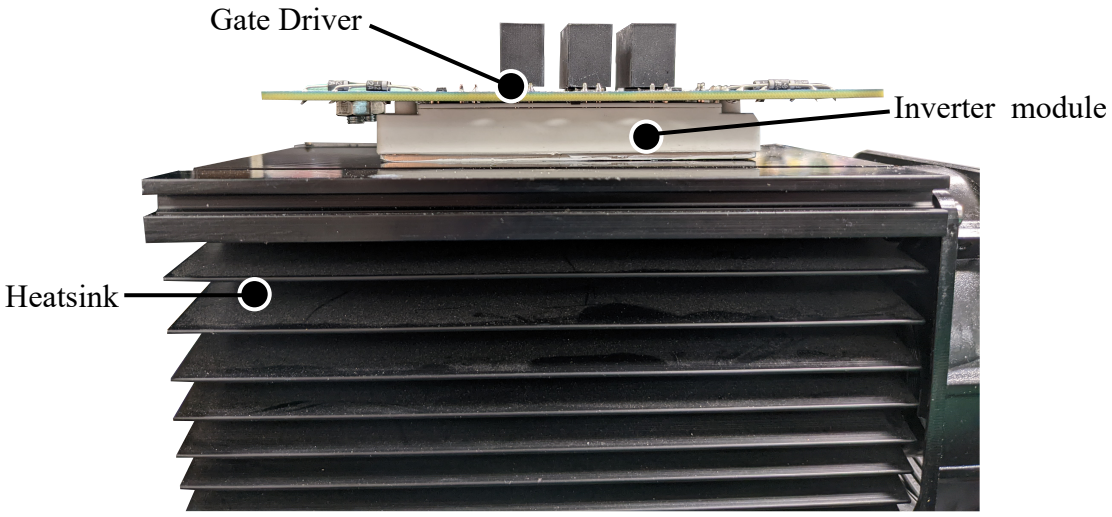


Figure 3.8: Inverter mounted underneath the gate driver with heatsink

3.3 Double pulse test

3.3.1 Reasons for double-pulse test

The double-pulse test is the preferred test method to measure the switching parameters and evaluate the dynamic behaviors of power devices. Looking at turn-on, turn-off, and reverse-recovery parameters, engineers can thoroughly evaluate the dynamic behaviors of power devices under a range of conditions, whether to optimize devices or confirm the actual value or deviation of power devices and modules.

3.3.2 How to perform a double-pulse test

The equivalent circuit schematic is shown in Fig. 3.9.

The test is performed on the bottom MOSFET and the upper body diode: it can be performed on all three legs or just on a subset, depending on the needs. A long pulse, followed by a shorter one (separated by a short amount of time) are delivered to the Gate of the bottom MOSFET. The Gate-Source of the upper MOSFET are short-circuited to ensure the upper MOSFET is never ON and we can evaluate its body diode. An inductor is connected between the drain and the source of the upper diode. The test consists of 3 phases:

1. Long Pulse: this sets the bottom MOSFET ON. During this time period, the inductor is subject to V_{DD} and hence its current linearly increases. The same current also flows through the bottom MOSFET.

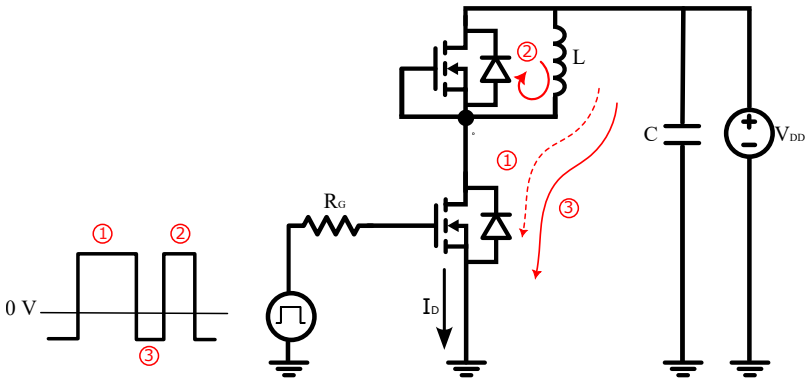


Figure 3.9: Schematic for the performance of a double-pulse test

The intention here is to measure the MOSFET turn-off time and the turn-off energy loss.

2. OFF time: this sets the upper MOSFET OFF. As the inductor wants to keep its current, the only path it can follow is through the body diode. In stage 2, the Drain - Source voltage of the bottom switch is V_{DD}.

3. Short Pulse: the bottom MOSFET is once again turned ON. This also means conduction in the body diode ceases. The current in the inductor (yet another time subject to V_{DD}) will rise again. The intention here is to measure the MOSFET turn-on time, the body diode reverse recovery current and the turn-on energy loss.

The expected waveforms are shown in Fig. 3.10.

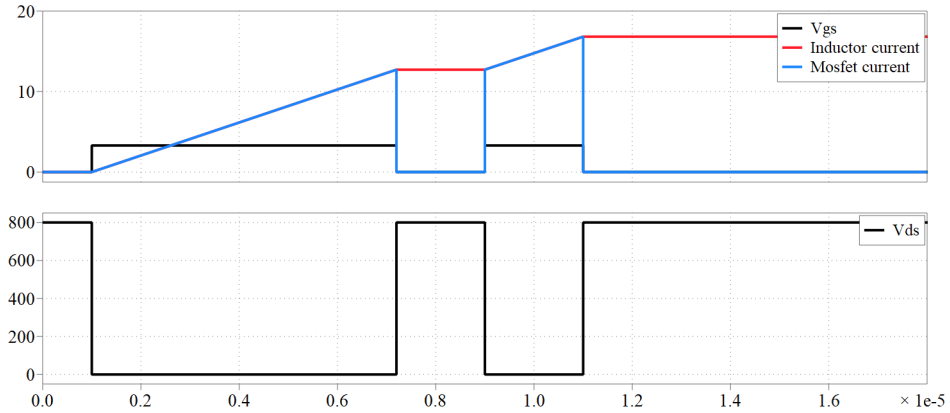


Figure 3.10: Simulated waveforms for double-pulse test

3.3.3 Setting up the double-pulse test

The inverter needs to be tested for its foreseen limit operating conditions:

$$V_{DD} = 800V \qquad I_{DS_{p2p}} = 15A$$

Given these values, the inductor can be chosen: it is important that it does not saturate for the current value it needs to be tested at. Moreover, it should reach the intended current value at around 10 µs. The final inductor choice is $L = 390\mu H$.

With all these parameters, it is possible to design the length of the long pulse with some trivial calculations starting from the equation of the current flowing through the inductor.

$$I_L = \frac{V_{DD}}{L} t_1 \tag{3.5}$$

Where I_L must be set equal to the desired current value flowing through the MOSFET, t_1 is the width of the long pulse.

$$t_1 = \frac{L}{V_{DD}} I^*_{DS} = 7.2\mu s \tag{3.6}$$

The OFF time should be very small, to ensure the inductor behaves as a current generator: it is decided to set it to $t_{OFF} = 1.8\mu s$.

The length of the second pulse should also be very small, not to increase the current significantly: the final choice is $t_2 = 2\mu s$.

The next problem to solve is how to generate these pulses: it is very important they are not periodic, as the test is intended for just two pulses and delivering more could lead to damage to the inverter. With the double pulse generator not available in the laboratory, it is necessary to generate it with a DSP. The one available is the TMS320F28379D by Texas Instruments.

The code is based on the generation of a PWM signal with period $T_{PWM} = t_1 + t_{OFF} = 9\mu s$ and alternating duty cycle ($D_1 = \frac{t_1}{T_{PWM}}$ and $D_2 = \frac{t_2}{T_{PWM}}$). The PWM is modified to stop the periodic signal just after the second pulse was sent. Considering the clock of the DSP is 100MHz and that the chosen carrier is a sawtooth wave, it becomes possible to retrieve the period of the carrier and the compare values, according to Eq. 3.7.

$$TB\_PRD = \frac{T_{PWM}}{T_{Clock}} - 1 = \frac{9\mu s}{0.01\mu s} - 1 = 899 \tag{3.7}$$

Eq. 3.8 shows how the two compare register values are retrieved.

$$\begin{aligned} CMP\_A1 &= \frac{t_1}{T_{PWM}} \cdot B\_PRD = 720 \\ CMP\_A2 &= \frac{t_2}{T_{PWM}} \cdot TB\_PRD = 200 \end{aligned} \tag{3.8}$$

The last problem in generating the pulses is their repeatability: in fact, the test is performed at various V_{DD} levels, for each of which sending a double pulse is required. As it is very bad practice to flash a code on the DSP in charge of generating PWM signals while it is connected to physical switches (risk of short-circuiting), the code needs to be continuously run in debug mode and a variable (named "*test*") is set up to activate the two pulses generation when its value is manually changed to 1 (returning to 0 once the two pulses are given). The resulting pulses are shown in Fig. 3.11.

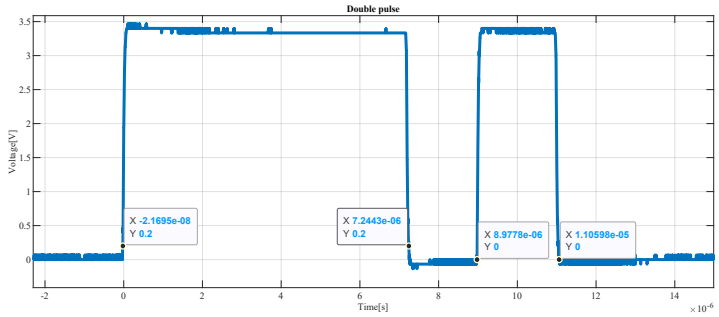


Figure 3.11: Double pulses generated via TMS320F28379D

The DSP is then connected to the Gate driver which converts the OFF value from 0 V to -4 V and the ON value from 3.3V to 20V.

Being the gate driver and the inverter module soldered together, there is no problem occurring regarding the connection of the driver signals. What is left to do is set up the measuring instruments and the supplies.

3.3.4 Setting up measurement instruments for double-pulse test

It is important to state that the main purpose of this test is not to evaluate the losses and the spikes of the current due to the reverse recovery of the body diode, as this information is already provided by the manufacturer for our operating conditions: instead, the main goal is to make sure the inverter correctly operates, outputting the desired waveforms at the desired levels. In addition to this, it is also intended to evaluate turn-on and turn-off times to correctly set the dead-band in the modulation block.

The test is performed on the bottom switch of inverter leg 1, as this is regarded sufficient. This note is important because the current flowing through the bottom MOSFET is not measured, as there is no direct access to the gate driver/inverter system: this makes it impossible directly evaluate the switching losses but not ensure the current values achieved match the desired ones. The instrumentation comprehends:

1. Global Specialities 1405 Power Supply. Set to output 15V with current limited to 250mA: employed to supply the gate driver.

2. EJ Series 600W Regulated High Voltage DC Power Supply. This high voltage power supply is employed to generate V_{DD} in a range from 10V to 800V.

3. LeCroy HVFO108 - High Voltage Fiber Optic Probe, 150 MHz Bandwidth: a very sensitive probe to measure gate-source voltage.

4. Differential oscilloscope probe: measures drain-source voltage.

5. PEM CWT Mini50HF AC Rogowski Current Probe: measures current flowing through the inductor.

6. Teledyne LeCroy wavesurfer 3024z oscilloscope. 4 channel, 4Gsa/s to display all the measured waveforms.
    - Channel 1: displays gate-source voltage.
    - Channel 2: displays drain-source voltage.
    - Channel 3: displays inductor current.
    - Trigger set in Normal mode on Channel 1.

Using differential probes is crucial, as the output side of the gate driver is isolated from the input side (connected to the DSP): using standard probes would have introduced the risk of breaking the isolation, resulting in the risk of damaging what is connected to the input side of the gate driver in case of malfunctioning on the output side. Referring to Fig. 3.6, the inductor is connected between DC+ and Phase A, V_{DS} is measured across Phase A and DC- and V_{GS} is measured across G2 and E2 pins. Fig. 3.12 shows the definitive connections.

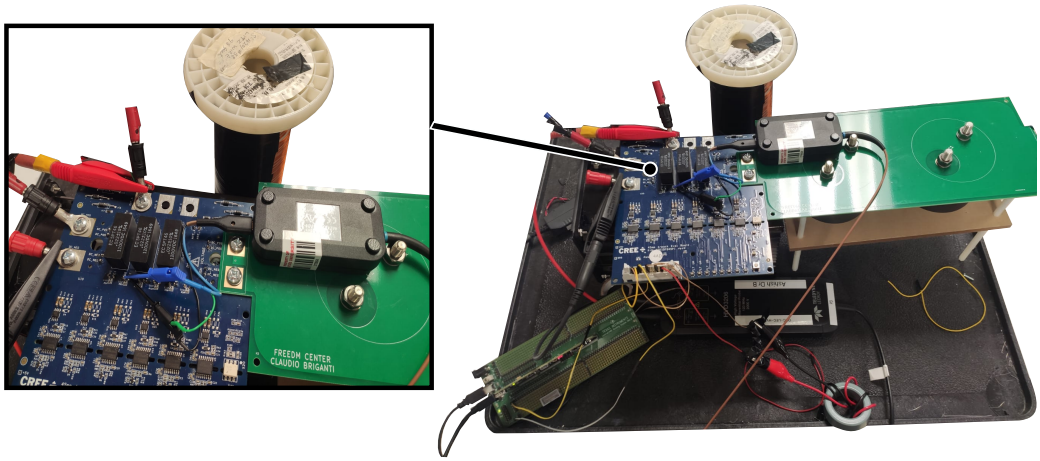


Figure 3.12: Gate driver-Inverter system with probes and supplies connected

3.3.5 Safety during and after the test

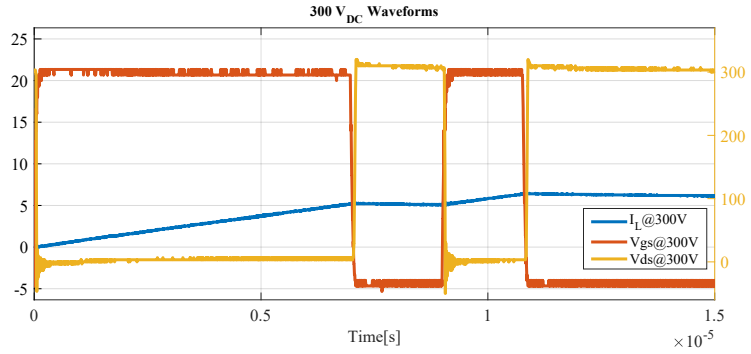
The test involved reaching 800V and 15A: these values are harmful to the human body and also can also permanently damage components (with the risk of dangerously blowing some). For these reasons, the testing bench is covered with a plexiglass box to avoid direct contact or risk of flying debris in case of component damage. It is also important to discharge the input capacitors with the help of resistors after the test is performed.

3.3.6 Results and conclusions

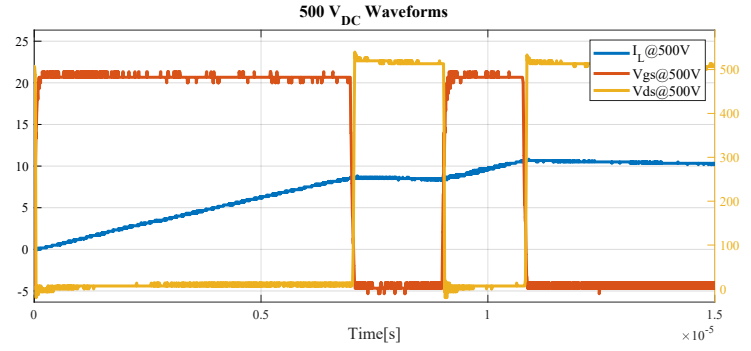
The testing points are V_{DD} = 10V,50V,100V,300V,500V,800V. Results have been captured only for the last three V_{DD} values, as the first three are not of particular interest for

our application but have been chosen to observe whether any unwanted behavior could show up at lower voltages.

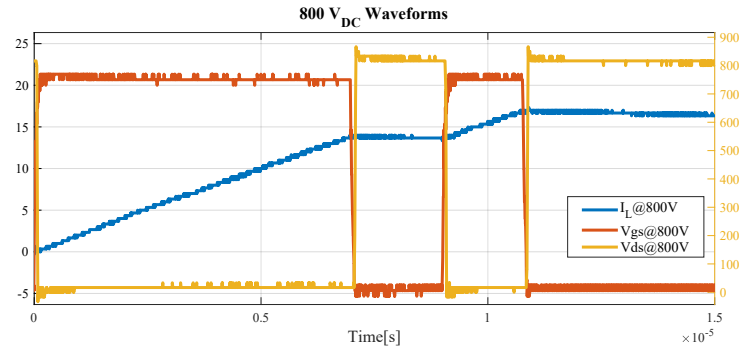
Fig. 3.13 shows all the captured waveforms.



(a)



(b)



(c)

Figure 3.13: Waveforms captured for (a) $V_{DD} = 300$V, (b) $V_{DD} = 500$V and (c) $V_{DD} = 800$V

The most interesting one is Fig. 3.13 (c). All the values of voltage and current match the expectations, which means there are no malfunctions in the inverter-gate driver ensemble. Consequently, it is possible to safely proceed with successive tests.

As already pointed out, the other goal of the test consists in evaluating the turn-on and turn-off times of the MOSFET at $V_{DD} = 800$V. Fig. 3.14 shows how turn-on and turn-off delays are measured.

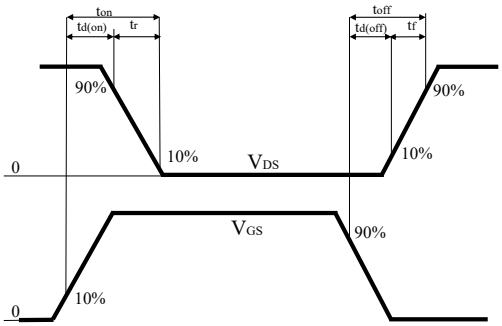
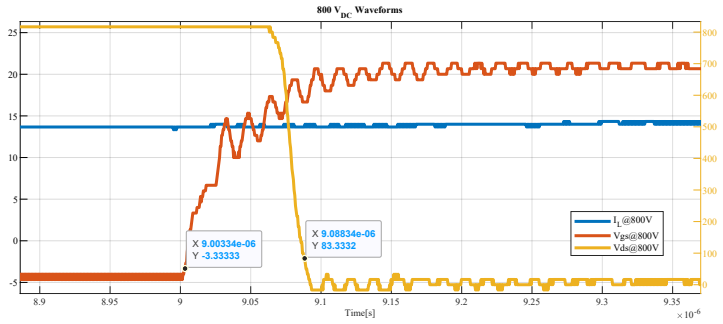
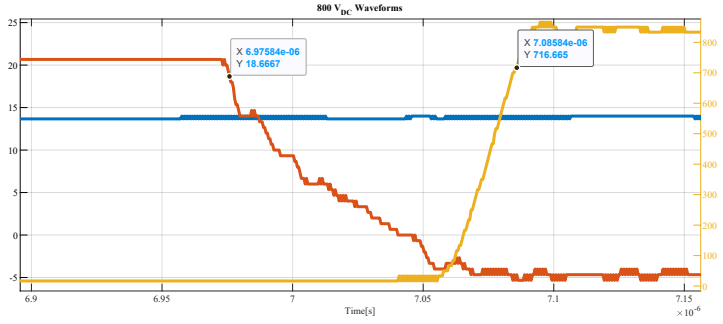


Figure 3.14: How turn-on and turn-off time delays are measured

The measurements are shown in Fig. 3.15.



(a)



(b)

Figure 3.15: (a) Turn on time delay and (b) Turn off time delay of MOSFET

From the highlighted points, it is possible to compute the two delays:

$$\boxed{t_{dON} = 85ns} \qquad \boxed{t_{dOFF} = 110ns}$$

The delay times are roughly tripled for safety reasons to choose the dead-bands, resulting in 500ns.

3.4 System setup

With the double pulse test, the correct capabilities of the inverter and gate driver have been successfully tested.

Before moving to perform tests on the motor, it is preferred to test the inverter in an open loop with a simpler resistive and inductive (RL) load: RL loads are very often chosen for simplified motor models and offer a good opportunity of testing inverter performances when connected to a load without the risk of damaging the motor itself. For this test and the subsequent, it is decided to introduce some of the features that will be part of the definitive motor control system: this time, to interconnect the DSP (generating the switching signals for the MOSFETs) and the gate driver, simple jumpers will no longer be employed as the two boards will be further apart and the need for shielding becomes more prominent. Instead, the signal will be conveyed optically: for this purpose, a board that converts the output of the DSP into the optical signals (close to the DSP) and one that converts them back to electrical (close to the gate driver) need to be inserted. Furthermore, at this stage, it is also decided to start introducing some of the features that will play a fundamental role in the closed-loop control: the sensors for the feedback path. They are not strictly required for an RL load test (as it will be conducted in open-loop fashion), but validating their calibration is helpful for future tests. The sensors introduced to the system at this stage are the three-phase current sensor, three-phase voltage sensor and V_{DC} voltage sensor. All these boards (except for the PWM receiver) will be placed on a larger board in charge of delivering the power supply and connecting them to the DSP.

3.4.1 Interface board

The interface board, shown in Fig.3.16 is a PCB of dimension 41cm x 41cm. It plays two roles:

- Powers the sensor cards presented in 3.4.4, the PWM transmitter presented in 3.4.6 and the DSP card
- Allows the communication between all the powered boards

The two power supplies at the top of Fig. 3.16 are two ECL30UT03-E (ECL30UT03-E datasheet) AC-DC converters with three outputs. They convert the AC input from the main line (120V - 60Hz in the US) and adjust it to +15V, -15V and +5V. At each of the outputs, a common mode choke is inserted to filter out high-frequency noise. These two supplies power the sensor cards: the $\pm 15V$ are used to supply the voltage and current transducers, the +5V instead powers the operational amplifiers.

The DSP and the PWM transmitter are instead powered up by the external +5V provided to the connector at the right bottom of Fig. 3.16: this power line includes a common mode choke to filter out high-frequency noise and capacitors for stabilization.

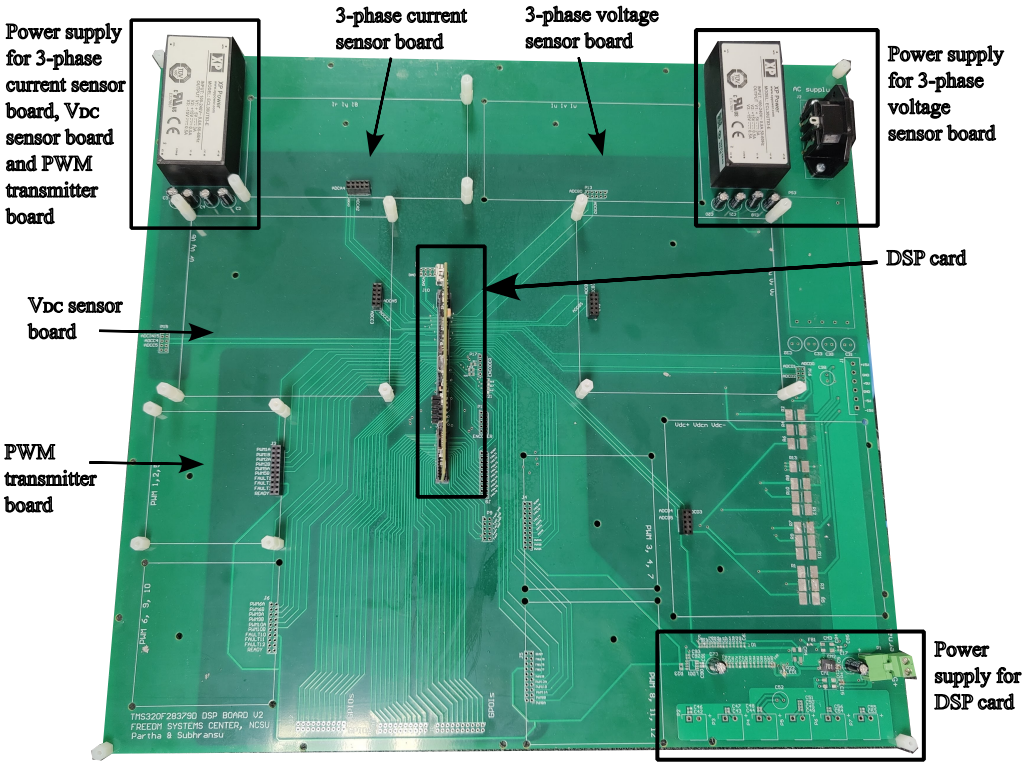


Figure 3.16: Interface board with highlighted purposes

The reason for having a different power supply for these two boards is to ensure galvanic isolation with the power supply of the transducers.

According to the pin-out scheme shown in Fig. 3.17, all the boards are connected to the DSP. Tab. 3.3 specifies the pin corresponding to the employed modules.

DSP Pin	Module	Function
49	PWM1 - channel A	PWM signal for top mosfet of leg 1
51	PWM1 - channel B	PWM signal for bottom mosfet of leg 1
53	PWM2 - channel A	PWM signal for top mosfet of leg 2
55	PWM2 - channel B	PWM signal for bottom mosfet of leg 2
57	PWM5 - channel A	PWM signal for top mosfet of leg 3
59	PWM5 - channel B	PWM signal for bottom mosfet of leg 3
15	ADC A - channel 2	Sensing current phase C
17	ADC A - channel 3	Sensing current phase B
21	ADC A - channel 4	Sensing current phase A
20	ADC B - channel 3	Sensing voltage phase A
24	ADC B - channel 4	Sensing voltage phase B
26	ADC B - channel 5	Sensing voltage phase C
31	ADC C - channel 2	Sensing positive voltage bus

33	ADC C - channel 3	Sensing negative voltage bus

Table 3.3: Pins through which the DSP interfaces with sensor boards and PWM receiver

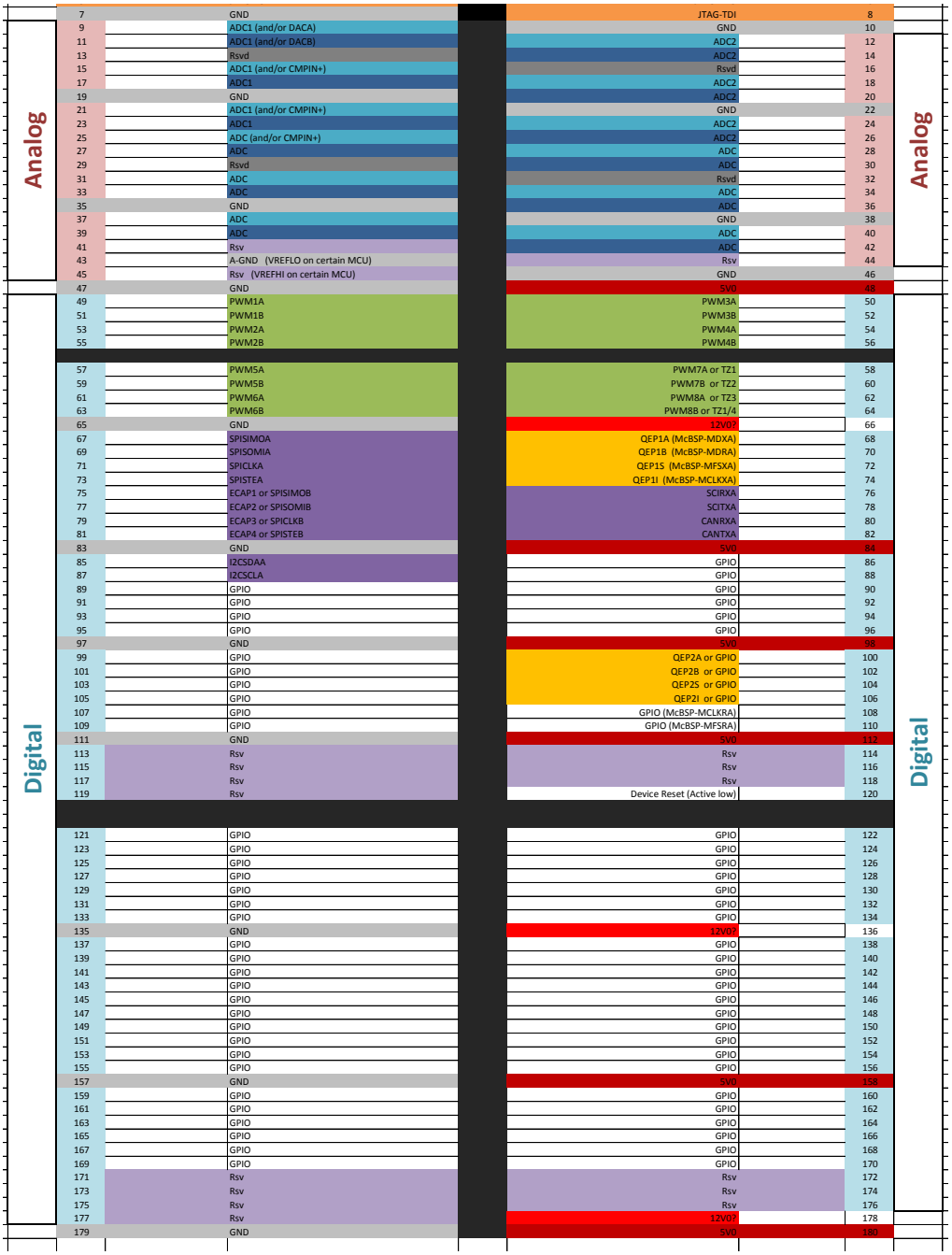


Figure 3.17: Output pin scheme of the DSP card

However, as visible in Fig. 3.16, the interface board can host more boards: the reason why these areas are not populated lies in the fact that the board can also be used to control six-phase motors, introducing the need for more three-phase current and voltage sensor board and another PWM transmitter board. In total, there is the possibility to have six PWM transmitter cards: these are not needed, and the purpose of having them is to allow the user to choose which PWM modules to use (the DSP offers 8 PWM modules, each with 2 channels).

3.4.2 DSP PWM generation

As already stated in 3.4.1, the DSP in use includes 8 PWM modules, each of which comes with two outputs. In our application, ePWM module 1,2,5 are employed.

The initialization of pins 49, 51, 53, 57, 59 as ePWM outputs is performed in "*Board_init()*" function. Such a function comes with the C2000 Ware library. Successively, the carrier waveform is defined. Fig. 3.18 shows all the waveforms it is possible to choose from.

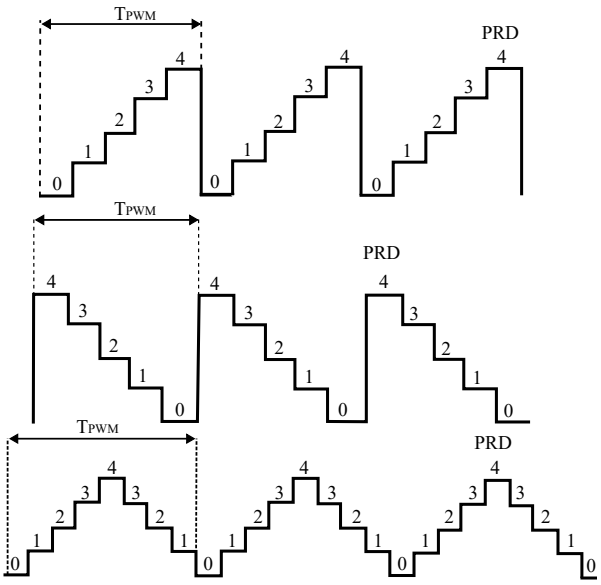


Figure 3.18: Carrier waveforms available in TMS320F28379D Digital signal processor board

The clock frequency is chosen to be 100 MHz (corresponding to $T_{PRD} = 0.01\mu s$). Tab. 3.4 reports how the period of the carrier can be computed for each type of carrier waveform.

To obtain a symmetrical PWM, which is crucial in space vector PWM modulation, the triangular is chosen. Given that the wanted switching frequency is 32 kHz (corresponding to 31.25µs), we need to compute the corresponding T_{PRD}: Eq. 3.9 shows how it is calculated.

Carrier waveform	Period [s]
Up counting sawtooth waveform	$(T_{PRD}+1)\cdot T_{CLK}$
Down counting sawtooth waveform	$(T_{PRD}+1)\cdot T_{CLK}$
Triangular waveform	$2\cdot T_{PRD}\cdot T_{BCLK}$

Table 3.4: Frequency equations for different types of carrier waveform

$$T_{PRD} = \frac{T_{PWM}}{2\cdot T_{Clock}} = \frac{31.25\mu s}{2\cdot 0.01\mu s} = 1562 \tag{3.9}$$

The state of the PWM output is retrieved by comparing the carrier waveform with the modulating reference signal: the output is set to high when the modulating signal is larger than the carrier signal and low in the other case. Fig. 3.19 shows how this can be translated into action commands in the code: the output is set to high when the carrier is up-counting and its counter value matches the value in the counter compare register (which is updated according to the modulating signal) and to low when the carrier is down-counting and its counter value matches the value in the compare register.

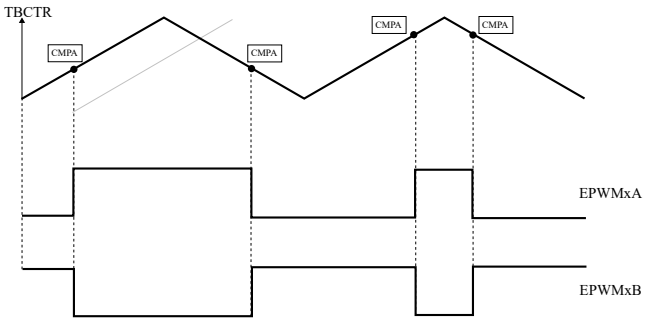


Figure 3.19: PWM output update based on the comparison between carrier and modulation signals

To obtain the complementary PWM waveform in channel B, the actions are reversed.

To update the compare registers, an interrupt is generated every time the value of the carrier counter is equal to 0.

An aspect that cannot be overseen is that the DSP outputs are not infinitely precise, hence it can happen that the two outputs of a module are not exactly complementary: this would mean that both switches in the same leg are simultaneously on, leading to a short circuit in the inverter leg with current values that could break the switches. For this reason, it is mandatory to add a delay between the moment one of the two MOSFETs is turned off and the other turned on: this delay is called dead band.

The dead band usually implemented in these applications is the active high complementary, which waveforms are shown in Fig. 3.20.

As already mentioned in sec. 3.3, analyzing the switching performances of the SiC MOSFETs in the inverter module in use, the dead band is chosen to be 500 ns for both

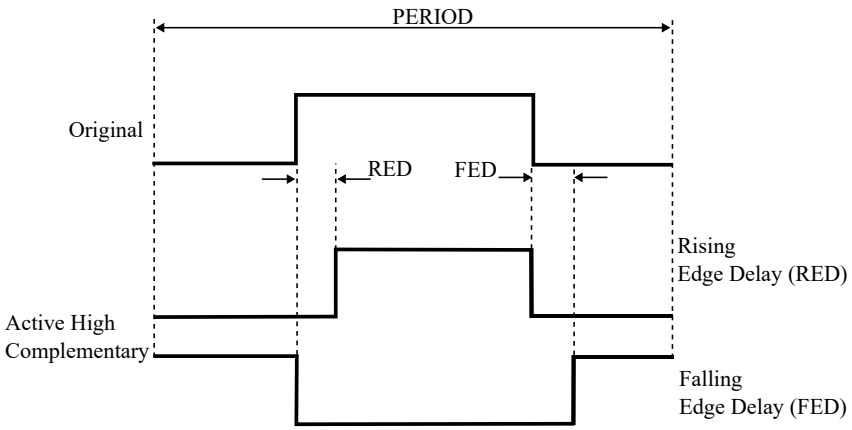


Figure 3.20: Active high complementary dead-band waveforms

rising edge delay (RED) and falling edge delay (FED): the corresponding counting steps are computed in Eq.3.10.

$$DB_{STEPS} = \frac{T_{DB}}{T_{PWM}} \cdot 2T_{PRD} = \frac{500ns}{31.25\mu s} \cdot 3124 = 50 \tag{3.10}$$

What is left to do is to update the compare registers of the three PWM modules with the modulator waveform values. Given some frequency and amplitude for the sinusoidal reference (either as the output of a controller or manually decided by the user), it is possible to compute its value as shown in List. 3.1.

Listing 3.1: Three-phase voltage reference in C

```
// Compute angular delta for sinusoidal since last update
delta_theta = ((0xFFFF)*Freq*2*EPWM_TIMER_TBPRD*0.00000001);
theta_bin = theta_bin + delta_theta;

// Compute new value of sinusoidal reference
ref[0] = Vm*sin((double)theta_bin*0.000095875);
ref[1] = Vm*sin((double)theta_bin*0.000095875 - 2.094395);
ref[2] = Vm*sin((double)theta_bin*0.000095875 + 2.094395);
```

First, the angular position difference since the last update is computed by multiplying the frequency and the PWM period. This value is then mapped into 16 bits (where 0 corresponds to 0° and 2^{16} corresponds to 360°) and added to the previous known angular position. Successively, inside the *sin* function, the angular position is converted into radians multiplying by $2\pi/65535 = 0.000095875$; reference B and C (ref[1] and ref[2] in List. 3.1) are shifted by $\pm 2\pi/3 = \pm 2.094395$ to obtain a three-phase reference. Successively, the operations for the Space Vector PWM already presented in are translated into C code.

3.4.3 ADC conversion on DSP

TMS320F28379D Digital signal processor board comes with four Analog-to-Digital Converters (ADCs) modules (A, B, C, D). Each ADC module comprehends 6 channels (numbered from 0 to 5) and is a successive approximation (SAR) style ADC with a selectable resolution of either 16 bits (for differential inputs) or 12 bits (for single-ended inputs). 16 bits resolution allows having up to 12 external channels, whereas 12-bit resolution allows up to 24 external channels. The ADC is composed of a core and a wrapper. The core is composed of the analog circuits which include the channel select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The wrapper is composed of the digital circuits that configure and control the ADC. These circuits include the logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules [4].

Tab. 3.3 shows which channels of which modules are chosen to convert the eight sensor acquisitions. Before enabling the converters, the modules are configured as follows:

- ADC clock: set to be SYSCLK/6, which means $200MHz/6 = 33.33MHz$;
- Single-ended mode conversion with 12-bit resolution;
- Interrupt generated when End of Conversion (EOC) signal is received.

The ADC triggering and conversion sequencing is accomplished through configurable start-of-conversions (SOCs). For our controller to work properly, the acquisitions must occur simultaneously. For this reason, only one trigger for the SOCs of all the 8 ADCs will be defined. The board in use offers different trigger solutions:

- S/W - software immediate start;
- All ePWMs - ADCSOC A or B;
- GPIO XINT2;
- CPU Timers 0/1/2;
- ADCINT1/2.

The choice fell on ePWM module 4, which has been configured as follows:

- Clock prescaler equal to 1: means the ePWM clock is SYSCLK/2(100MHz);
- Triangular waveform;
- Counter $T_{PRD} = 1000$;
- Generate the trigger for an SOC every time the counter value is 0.

This way a trigger is generated at 50kHz frequency. Once the trigger has been defined, it is necessary to configure each SOC. To do so, we need to specify:

- The ADC module;
- The number of SOC;
- The trigger for the SOC;
- Channel of the ADC module;
- The acquisition (sample) window duration.

While the trigger for different SOCs can be the same, it is better to avoid using the same SOC for channels inside the same module (it is instead alright to have the same SOC for different modules). Tab. 3.5 summarizes which SOC corresponds to which ADC channel.

SOC 0	ADC A4, ADC B3, ADC C3
SOC 1	ADC A3, ADC B4, ADC C2
SOC 2	ADC A2, ADC B5

Table 3.5: SOC for each ADC channel

The sampling window is set to 15 SYSCLCKs: this corresponds to $15 \cdot T_{ADC} = 15 \cdot 5\text{ns} = 75\text{ns}$.

Lastly, creating a SOC, also its corresponding EOC will be activated: an interrupt is assigned to each EOC and enabled. Inside this interrupt, all the acquisitions will be saved into variables.

The converted values will be in the 0-4095 range. Tab.3.6 summarizes how the analog input is remapped.

ADC_IN $\leq$ VREF_LO	ADC_OUT = 0
VREF_LO $\leq$ ADC_IN $\leq$ VREF_HI	ADC_OUT = $4096 \cdot \frac{ADC\_IN - VREF\_LO}{VREF\_HI - VREF\_LO}$
ADC_IN $\geq$ VREF_HI	ADC_OUT = 4095

Table 3.6: Analog input mapping into digital

For TMS320F28379D board, VREF_HI = 3 V and VREF_LO = 0 V.

3.4.4 Sensors

Three-phase current sensor

For current control loops to correctly operate, the reference current in dq axes must be compared to the actual current flowing through the motor. The three-phase current sensor PCB is shown in Fig.3.21.

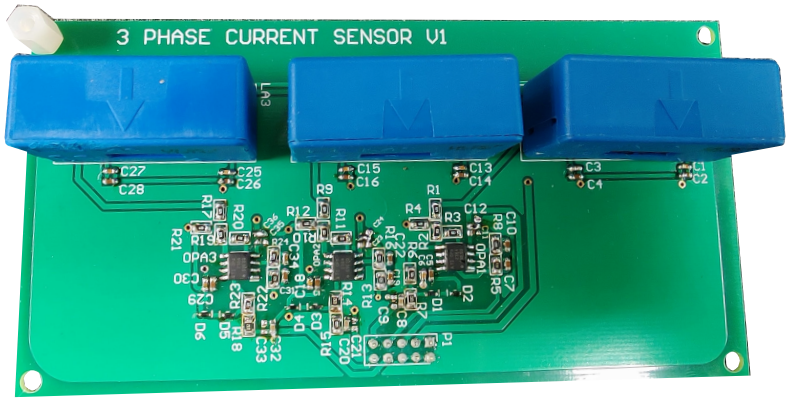


Figure 3.21: Three-phase current sensor board

Unfortunately, the schematic of the board is private, but the working principle of the sensor has been simulated on PLECS for one of the three phases (the same applies to the other two) and is shown in Fig.3.22.

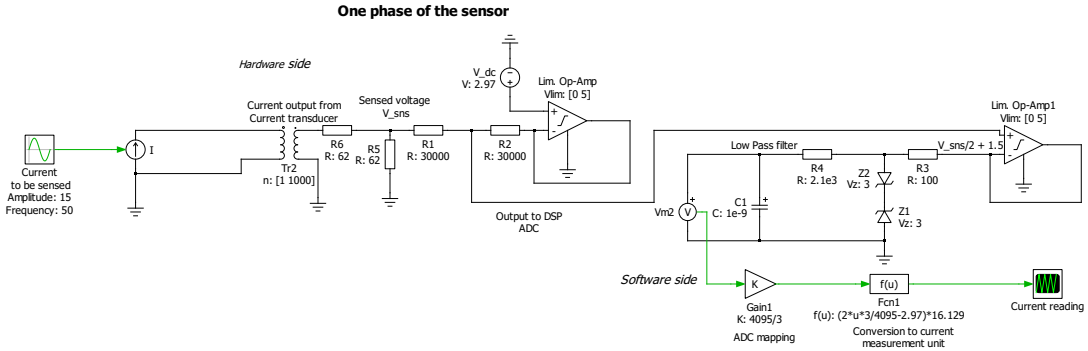


Figure 3.22: PLECS simulation of one phase of the three-phase AC current sensor

The central component of the board is Current Transducer LA 55-P, whose datasheet can be found at Current Transducer LA 55-P datasheet. It is a current transducer that exploits the Hall effect and can be used to sense both AC and DC currents ensuring galvanic separation between the primary circuit and the secondary circuit. The primary nominal RMS current (sensed current) is 50A, which is way above the maximum for our application.

The wire with the current to be sensed is inserted in the hole of the transducer in such a way that the direction of the flowing current is concordant with the arrow on the component (visible in Fig. 3.21). According to the datasheet, a current 1000 smaller will be generated at the secondary side. The DSP, in charge of reading the current measurement, can only perform analog to digital conversions on voltage measurements: the rest of the circuit is an analog interface needed to convert the current measurement into a voltage measurement and adapt its range to the one of the DSP reading capabilities.

Referring to Fig. 3.22, the sensed current in fact flows through R_5 and R_6, building

up V_{sns} across R_5. The first operational amplifier is in charge of remapping the sensed voltage to the DSP input voltage range: V_{sns} is divided into two by R_1 and R_2, then an offset corresponding to $V_{dc}/2$ is added (V_{dc} at the non inverting input pin is also partitioned in two by R_1 and R_2). The second operational amplifier is a voltage follower: at its inverting pin we find two Zener diodes to limit the voltage input to DSP to 3V (not to damage it) and an RC low pass filter with a cut-off frequency of $\frac{1}{RC} = 476kHz$ to filter out high frequency harmonics. The equations corresponding to all these operations are shown in Eq. 3.11.

$$\begin{aligned} I_s &= \frac{I_p}{1000} \\ V_{sns} &= 62 \cdot I_s \\ V_{ADC} &= \frac{V_{sns}}{2} + \frac{2.97}{2} \end{aligned} \tag{3.11}$$

As shown in 3.4.3, the range of voltage the DSP can take as input is 0-3V. In our application the maximum possible current is $\pm 14.56A$: combining Eq. 3.11, we can retrieve the range of V_{ADC}:

$$\boxed{1.05V \leq V_{ADC} \leq 1.95V}$$

The situation becomes even worse considering the nominal current for our motor operating at $400V_{rms}$ line to line voltage, equal to $2.87A_{rms}$ (corresponding to $\pm 4.05A$). In this case:

$$\boxed{1.375V \leq V_{ADC} \leq 1.625V}$$

The reason for not exploiting the full voltage range of the DSP analog to digital converter is that the sensor was not designed for this application but for one with a higher current range: the result is the sensitivity of the ADC will be very limited.

Three-phase AC voltage sensor

Sensing the motor three-phase voltage is not strictly required in the presented controlling technique. Nonetheless, it is chosen to have it in case in the future the controlling technique is changed. It can also be useful in this application to monitor the phase voltages directly from the laptop in debug mode. Fig. 3.23 shows the three-phase AC voltage sensor.

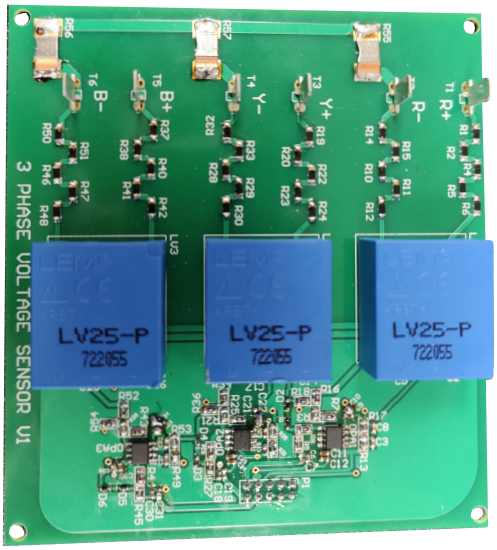


Figure 3.23: Three-phase AC voltage sensor PCB

The schematic of the board is private, but its functioning has been simulated in PLECS as shown in Fig. 3.24.

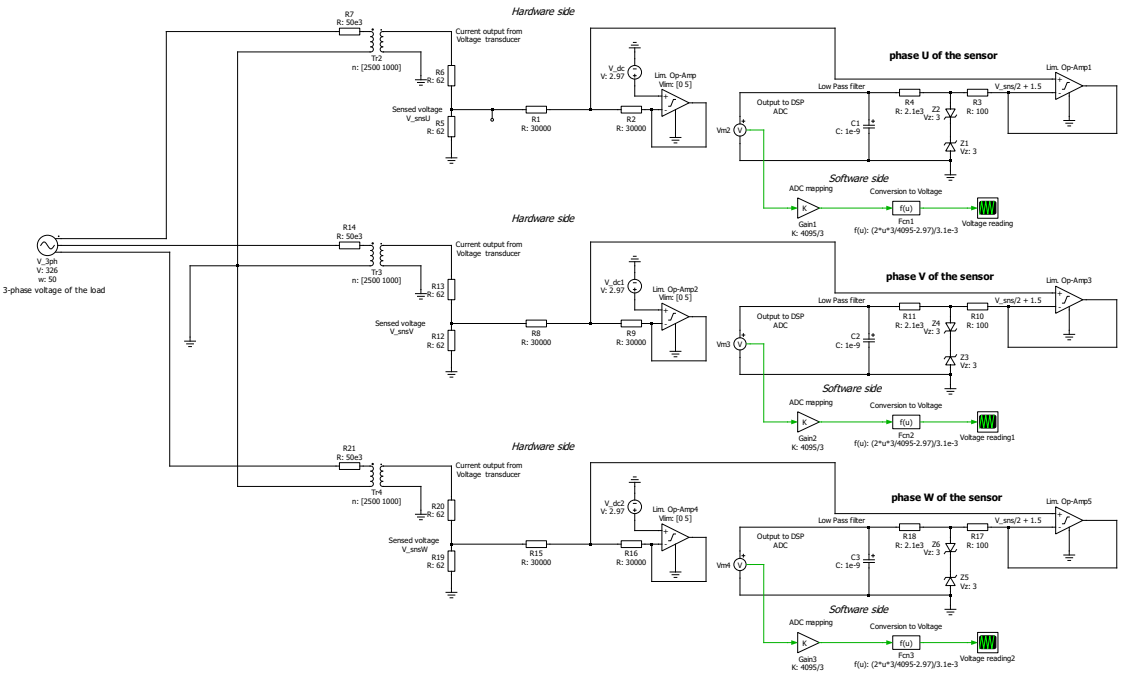


Figure 3.24: PLECS simulation of one phase of the three-phase AC voltage sensor

The voltage measured at each of the inverter output is connected to R+, Y+ and B+ through faston connectors. As can be seen in Fig. 3.23, R-, Y- and B- are connected through 0.02 Ω 1% accuracy shunt resistors to create a neutral point and hence allow

measuring the line to neutral voltage of each phase. Each sensor phase presents ten 50 kΩ resistors in series: hence, in each phase a current equal to $\frac{V_{ph}}{50\,\text{k}\Omega}$ will build up. Such currents also flow through the true sensing element, LV 25-P Voltage Transducer(LV 25-P Voltage Transducer datasheet). This sensor is based on the Hall effect and also ensures galvanic isolation with the analog interface that will directly connect to the DSP. As shown in Fig. 3.24, this component can be modeled as a transformer with a 2.5:1 turning ratio. The rest of the circuit is the same employed in the three-phase current sensor and is already presented in section 3.4.4. The equations describing the behavior of the circuit are shown in Eq. 3.12.

$$\begin{aligned} I_s &= \frac{V_{ph} \cdot 2.5}{50000} \\ V_{sns} &= 62 \cdot I_s \\ V_{ADC} &= \frac{V_{sns}}{2} + \frac{2.97}{2} \end{aligned} \tag{3.12}$$

In our application, the voltage limit is chosen to be the motor rated voltage. This corresponds to a peak value of 326V: combining Eq. 3.12, we can retrieve the range of V_{ADC}:

$$\boxed{1V \leq V_{ADC} \leq 2V}$$

Also in this case, the full range of the DSP ADC input is not entirely exploited, resulting in less sensitivity than the possible available.

DC voltage sensor

As shown in section 2.5 V_{DC} measurement is needed for the SVPWM algorithm, hence it is necessary to add a sensor for this too. Fig. 3.25 shows the DC voltage sensor PCB.

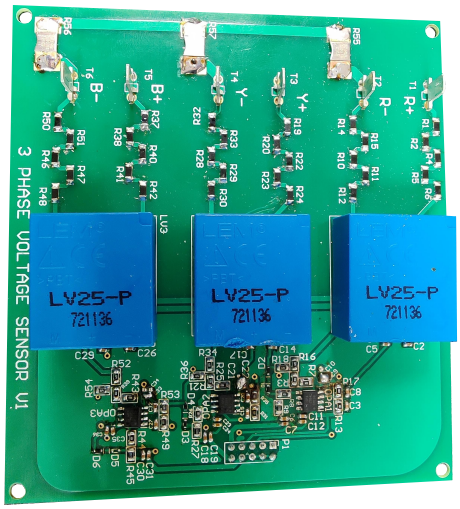


Figure 3.25: DC voltage sensor board

Fig. 3.25 clearly shows that the sensing components are three, in fact this board is the same employed for the three-phase voltage sensing with a different low pass filter cut-off frequency.

The way the sensing is performed is shown in Fig. 3.26.

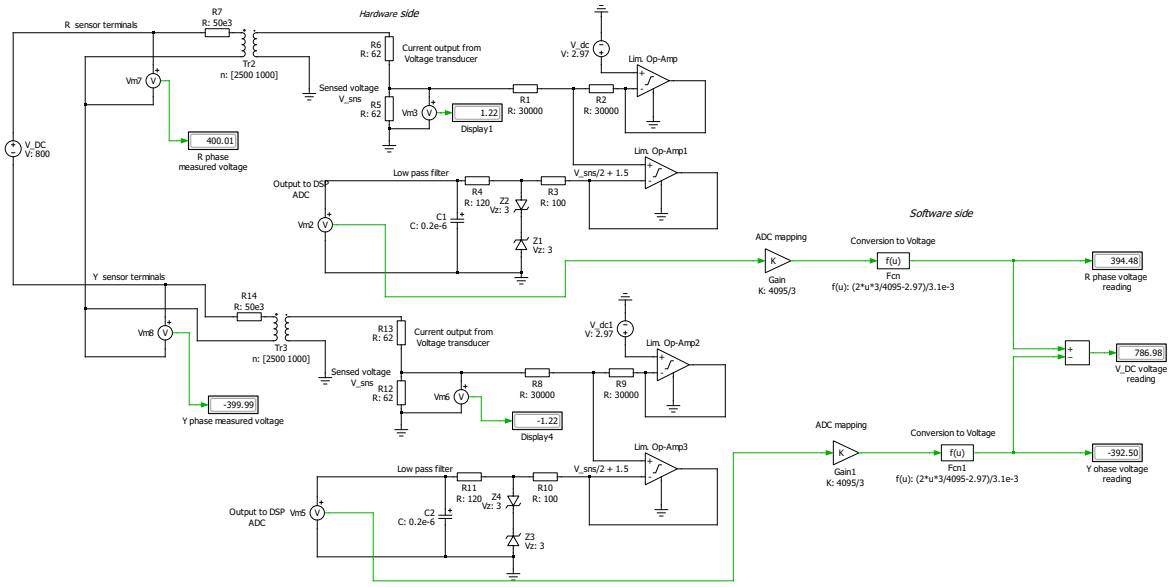


Figure 3.26: PLECS simulation of the DC voltage sensor board

Each phase works as already described in sec. 3.4.4 , but this time the cut-off frequency of the output low pass filter is smaller ($\frac{1}{R_4 C_1} = 41.6kHz$) as the measurement is on a DC value.

Measuring only one of the three phases would have not been possible for this application: V_{DC} is 800V, and applying it to only one of the three phases would have generated $I_P = \frac{V_{DC}}{50000} = 0.016A$, resulting in a power loss of $P_R = RI_P^2 = 1.28W$ on each resistor. As shown in 5 kΩ resistor datasheet, they can withstand up to 0.78W. The solution found to avoid the risk to damage them was to split the voltage measurement in two: connecting the positive voltage bus to one phase and the negative voltage bus to the other, this leads to having one phase measuring a positive constant voltage equal to $V_{DC}/2$ and the other phase measuring a negative constant voltage equal to $-V_{DC}/2$: the two measured values are then subtracted after the ADC conversion in the DSP code to retrieve the true V_{DC} value. By doing so, we can recompute the power dissipated on each resistor which results in $P_R = 0.32W$, ensuring good safety margins.

3.4.5 Sensors calibration

In 3.4.3, it is shown that the result of the analog-to-digital conversion is a 12-bit number: this needs to be converted through an inverse function to the quantity effectively measured either in amperes or volts. Summarizing what has been presented in 3.4.4 and 3.4.3, Eq. 3.13 show thes relationship between the ADC output for the current sensing board and

the voltage sensing board respectively.

$$\begin{aligned} \text{Current}_{ADC} &= 4096 \cdot \frac{\frac{\frac{62 \cdot I^*}{1000}}{2} + \frac{2.97}{2}}{3} \\ \text{Voltage}_{ADC} &= 4096 \cdot \frac{\frac{\frac{62 \cdot V^* \cdot 2.5}{50000}}{2} + \frac{2.97}{2}}{3} \end{aligned} \tag{3.13}$$

Inverting both, we can retrieve the inverse functions needed for the conversion. These are shown in Eq. 3.14.

$$\begin{aligned} I^* &= \frac{2 \cdot 1000}{62}\left(\frac{3 \cdot \text{Voltage}_{ADC}}{4096} - \frac{2.97}{2}\right) \\ V^* &= \frac{2 \cdot 50000}{62 \cdot 2.5}\left(\frac{3 \cdot \text{Voltage}_{ADC}}{4096} - \frac{2.97}{2}\right) \end{aligned} \tag{3.14}$$

To verify if these equations are reliable, the boards are tested with known voltage and current values. The voltage is generated from EJ Series 600W Regulated High Voltage DC Power Supply, while for the current the cables connected to Global Specialities 1405 Power Supply are shorted setting the current limit to the desired values. The comparison between input values and measurement readings are shown in Tab. 3.7 for one phase of each sensor.

Sensor	**Applied quantity**	**Conversion output**
I_{phaseA}	0 A	-0.6 A
	1 A	0.53 A
	1.5 A	0.98
	2 A	1.47 A
	2.5 A	1.94 A
	3 A	2.53 A
V_{phaseA}	0 V	-83.88 V
	100 V	6.84 V
	150 V	49.37 V
	200 V	91.89 V
	250 V	135.84 V
	300 V	178.37 V
V_{DC+}	0 V	-90.97 V
	50 V	-38 V
	75 V	-13V
	100 V	12.51 V
	125 V	37.55 V
	150 V	58.82 V

Table 3.7: Comparison between current and voltage applied to sensors and analog-to-digital output

It is clear these results are not satisfying: tolerances on the components and noises can result in the alteration of the sensed values (which are particularly high due to the

problems already described with the ranges of the sensors employed). To counterbalance these unwanted errors, slope compensation factors and offsets are added for each sensor. The new equations are shown in Eq. 3.15.

$$\begin{aligned} I^* &= \frac{2 \cdot 1000}{62}(\alpha \cdot \frac{3 \cdot \text{Voltage}_{ADC}}{4096} - \frac{2.97}{2}) + k \\ V^* &= \frac{2 \cdot 50000}{62 \cdot 2.5}(\alpha \cdot \frac{3 \cdot \text{Voltage}_{ADC}}{4096} - \frac{2.97}{2}) + k \end{aligned} \tag{3.15}$$

Tab. 3.8 shows the value of k and α chosen for each sensor.

Sensor	α	$\boldsymbol{k}$
I_{phaseA}	1	0.6 A
I_{phaseB}	1	0.73 A
I_{phaseC}	1	0.53 A
V_{phaseA}	1.12	-22V
V_{phaseB}	1	20.35 V
V_{phaseC}	1	20.35 V
V_{DC+}	1	87.8 V
V_{DC-}	1	84.8 V

Table 3.8: Offset and linear coefficient corrections

Subsequently to these corrections, Tab. 3.6 is updated in Tab. 3.9.

Sensor	**Applied quantity**	**Conversion output**
I_{phaseA}	0 A	0 A
	1 A	1.14 A
	1.5 A	1.59
	2 A	2.08 A
	2.5 A	2.56 A
	3 A	3.15 A
V_{phaseA}	0 V	-0.7 V
	100 V	100.89 V
	150 V	148.53 V
	200 V	196.18 V
	250 V	245.41 V
	300 V	293.05 V
V_{DC+}	0 V	-2.95 V
	50 V	49.97 V
	75 V	75.02 V
	100 V	100.54 V
	125 V	125.59 V
	150 V	146.86 V

Table 3.9: Comparison between current and voltage applied to sensors and analog-to-digital output after corrections

3.4.6 Transmitting PWM signals from DSP to gate driver

Depending on the application, the digital signal processor generating the PWM signal intended for the converter might be far from the gate driver. Power electronics systems work with high voltages/currents and high frequency, generating noticeable electromagnetic noises and disturbances, added to the presence of parasitics in the transmission cables themselves and possible impedance mismatches.

Hence, it becomes necessary to shield the PWM signal, as having it exposed to all the noise sources from the system itself and the surrounding environment would lead to distortions and possibly unwanted switching performances in the MOSFETs or even worse to the damage of some components.

A popular solution is to transmit these signals employing optical fiber cables, given their intrinsic EMI/ RFI immunity. Additional benefits of optical fiber include its easy field connector termination, via the OFS Crimp and Cleave Termination system, easy testing with visible light, damage-resistant cable, and electrical isolation. Events such as a ground fault or very high currents cause a difference in electrical potential from one location to another. This change in potential can damage equipment and injure people. Optical fiber provides the necessary electrical isolation to drastically reduce the risks to people and equipment.

Furthermore, PWM signals in one inverter leg need to include dead bands to avoid simultaneous switching of the two MOSFETs, as this would lead to a short circuit with catastrophic results for the health of the components. Such dead band can be implemented directly on the DSP (as described in 3.4.2). Unfortunately, this is a small percentage of the switching period (which is in the order of magnitude of microseconds): uncertainties in the output of the DSP itself, or noise in the path to the gate driver may alter the calculated delay between the two switchings. For this reason, it is common practice to generate the dead band as close as possible to the gate driver itself (often such devices have the capability of generating it themselves).

Gathering together all these requirements, it became clear that there is a necessity to implement a board able to convert the electrical PWM coming from the DSP board into optical signals(already designed and only to be assembled) and a second one to convert the PWM optical signals into electrical signals to be fed to a circuit that generated the dead band and then convey it to the gate driver board(to be designed).

PWM transmitter board

The PWM transmitter board had already been designed and was only to be soldered.

The board consists of:

- Capacitors to stabilize the supply voltages;
- Four SN75451BD buffers. these are connected to the +5V supply and their goal is to modify the 0-3.3V PWM coming out of the DSP to 0-5V compatible with the gate driver. Moreover, thanks to this buffer the current the opto-transmitter need to execute their duties will not be drawn from the DSP (which has very low current output capabilities) but from the supply itself;

- Six HFBR-1528Z opto-transmitter: these are the components that convert the signal from electrical to optical.

Fig. 3.27 shows the board ready to use.

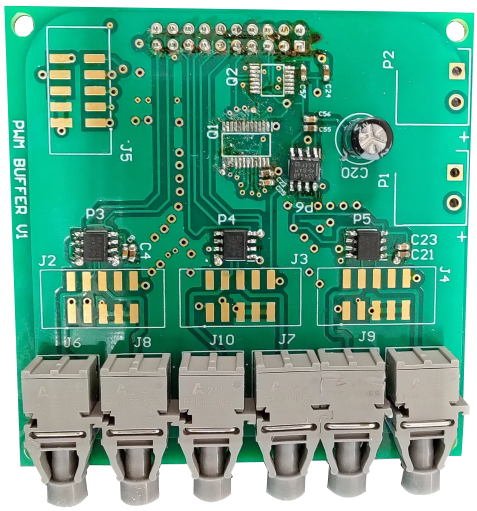


Figure 3.27: PWM transmitter board

As easily visible, most of the board is not populated: in fact, it included more logic components employed for faults handling in both DSP and inverter which are not regarded necessary to implement at this stage.

PWM receiver board

The schematic of the receiver board comprehends three modules (one per inverter leg): each module includes two optical fiber receiver circuits (retrieved directly from the datasheet of the fiber optic connector, which can be found at AFBR-2528CZ datasheet), and a circuit that takes the PWM signal for the upper switch and generates two signals from this: a copy of itself with the dead band included and its complementary with the dead band (for the bottom switch of the leg) according to the active high complimentary configuration shown in Fig. 3.20. These signals are then connected to two jumpers that allow choosing which signal to feed to the gate driver: for each switching signal it is possible to choose between the signal coming from the DSP (with digitally implemented PWM) and the one coming from the dead band generation circuit. The output of the jumper is then connected to an X1 connector that works as the interface with the gate driver.

The dead band generation circuit has been simulated in PLECS as shown in Fig. 3.28.

All the logical part is implemented in 74VHC132MX digital electronic component, which is nothing but a quad two input NAND Schmitt Trigger. Taking as an example the PWM signal for the upper switch of leg A of the inverter, it first gets inverted, becoming signal $AP1$. This signal is then used to charge an RC circuit on its rising edge while remaining unchanged during its falling edge (output is $AP3$) and discharge another RC circuit on its falling edge while remaining unchanged during its rising edge (output is

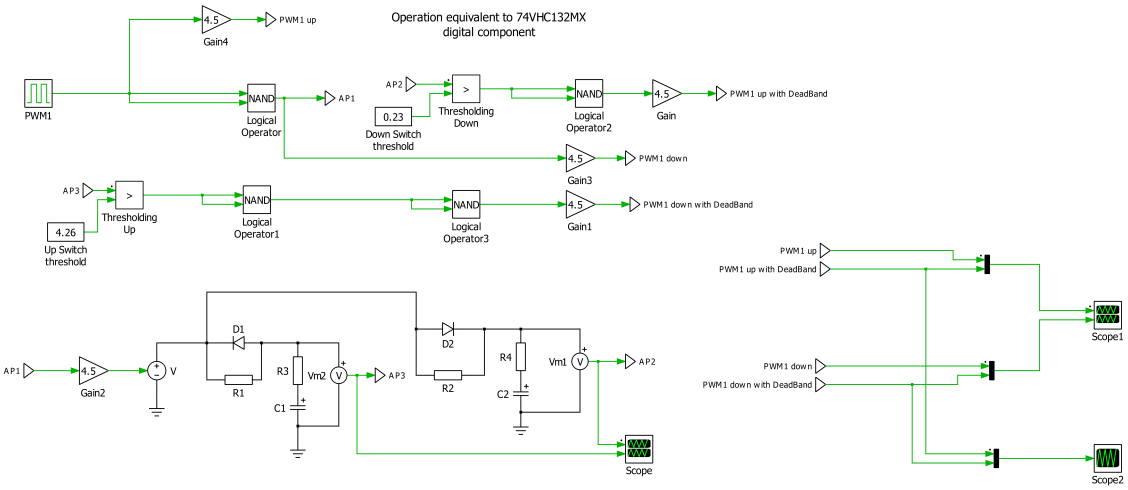


Figure 3.28: Simulation of the Dead Band circuit

$AP2$). $AP2$ and $AP3$ will now have a steep edge (respectively the rising and the falling) and the other edge following the exponential curve of an RC charging/discharging circuit. The two signals are shown in Fig. 3.29.

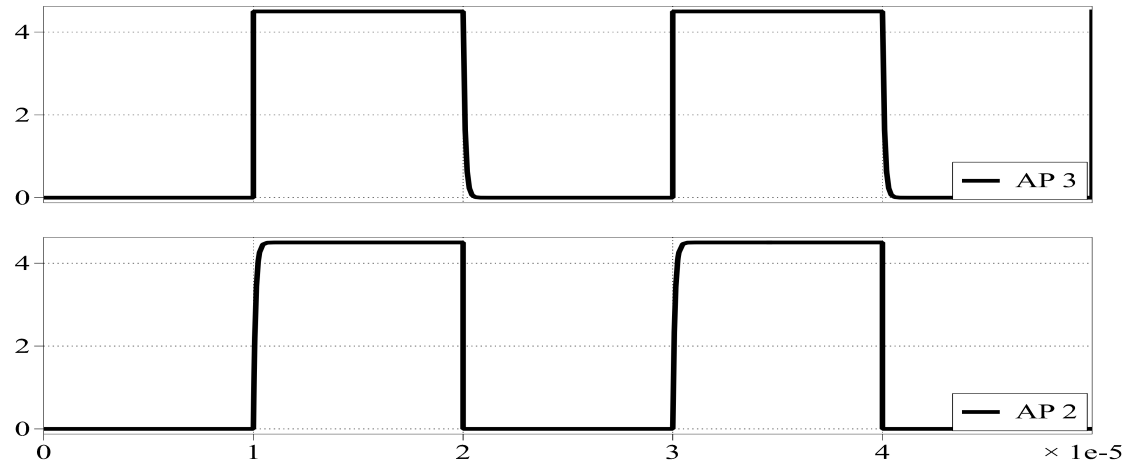


Figure 3.29: AP 2 and AP 3 waveforms

$AP2$ falling edge (having the shape of a decreasing exponential) is now compared with a threshold value to be converted again into a square wave: only when it goes below that value it will turn low. The signal is then inverted again and hence version of the initial PWM signal with dead band on its rising edge is obtained. The resulting square wave compared to the initial one is shown in Fig. 3.30.

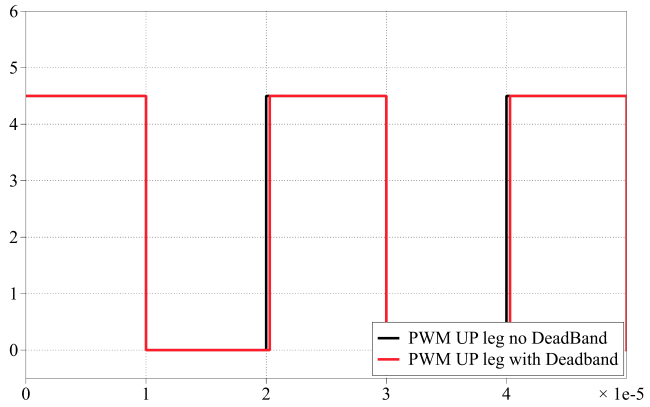


Figure 3.30: Comparison of initial PWM signal for the upper switch and one with deadband

Also $AP3$ rising edge (having the shape of an increasing exponential) is now compared with a threshold value to be converted into a square wave: when this value is overcome, the rising edge occurs. The signal is then inverted twice generating the PWM signal for the bottom switch with dead band on its rising edge. The resulting square wave compared to the complementary of the initial one is shown in Fig. 3.31.

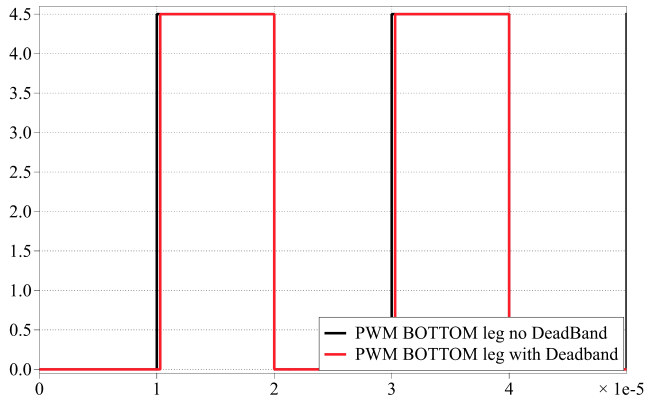


Figure 3.31: Comparison of initial PWM signal for the bottom switch and one with deadband

The PWM obtained by combining the two outputs of the dead band circuit is shown in Fig. 3.32.

The switching delay obtained for the circuit is around 300 ns (and can be adjusted by modifying the RC components), which is roughly 1 % of the switching period. These values can be adjusted by modifying the resistor, capacitor and threshold values.

The resulting PCB board, designed on Altium designer is shown in Fig. 3.33.

The PCB also includes a 15 V power supply connector (to supply the gate driver), and a linear voltage regulator (from 15 V to 5 V and 2 A maximum current) for supplying

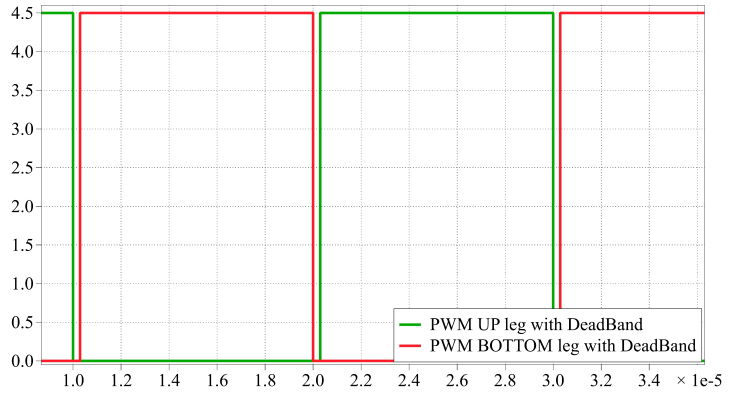


Figure 3.32: Both outputs of the DeadBand circuit

the fiber optic adapters.

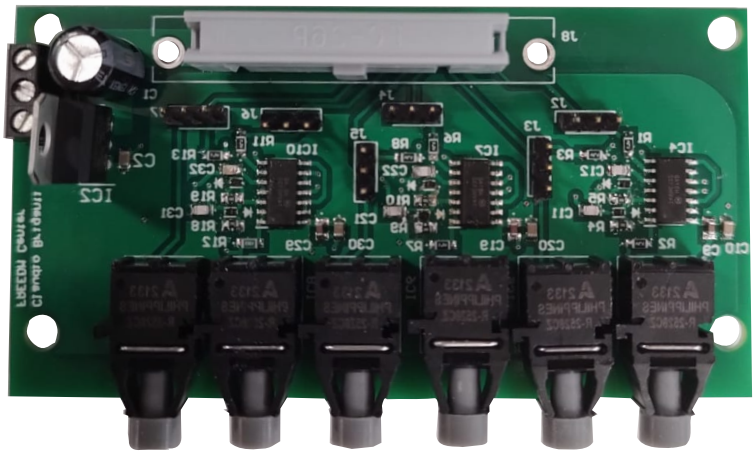


Figure 3.33: Fiber optic adapter plus dead band generator PCB board

3.5 Considerations about the interface and transmission system

Fig. 3.34 shows the Interface board with the DSP, all the sensor boards and the PWM transmitter board mounted.

It is important to highlight that having the boards connected by such long paths without any resistance inserted can introduce noise in the signals transmitted, which is reflected in very oscillatory sensor measurements (increased by the limited range of the sensors, which tends to make them more susceptible to noise) and also in the PWM signals. Moreover, the dead-band generation in the PWM receiver board has been designed for 300ns (as the same schematic is used for GaN MOSFETs), which might be risky for

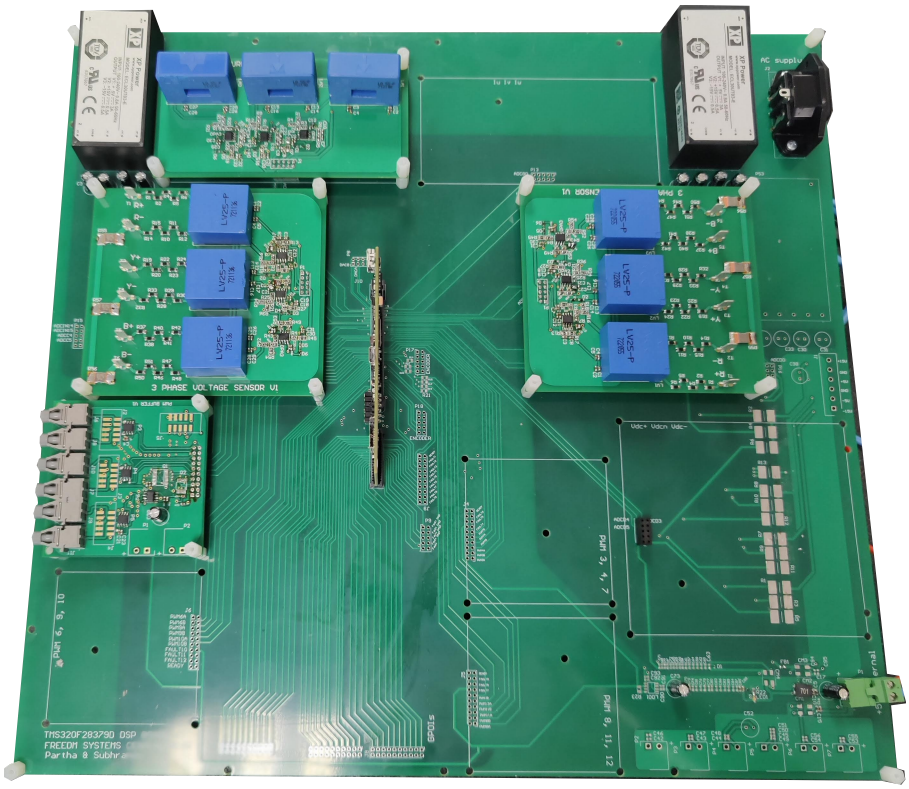


Figure 3.34: Interface board with the DSP, all the sensor boards and the PWM transmitter board mounted

SiC MOSFETs: hence, after having verified the dead-band generated by the DSP in reliable, it is preferred to proceed using directly the PWM signals coming from the DSP. Another solution involves re-calculating the values of RC presented in 3.4.6.

3.6 Inverter test with no load

3.6.1 Reasons for testing with no load

Before connecting a load to the inverter, it is good practice to verify its voltage outputs when the load is disconnected.

3.6.2 Setting up the inverter test with no load

Fig. 3.35 shows how the setup for the test. In this case the sensors do not play any role. The PWM transmitter and receiver instead play a fundamental role: the test offers an occasion to verify whether the code written to generate the PWM effectively works and in particular to validate the chosen dead time.

The line-to-line voltage between phase A and phase B, is measured simply by connecting the positive side of the probe to inverter output A and the negative side to inverter

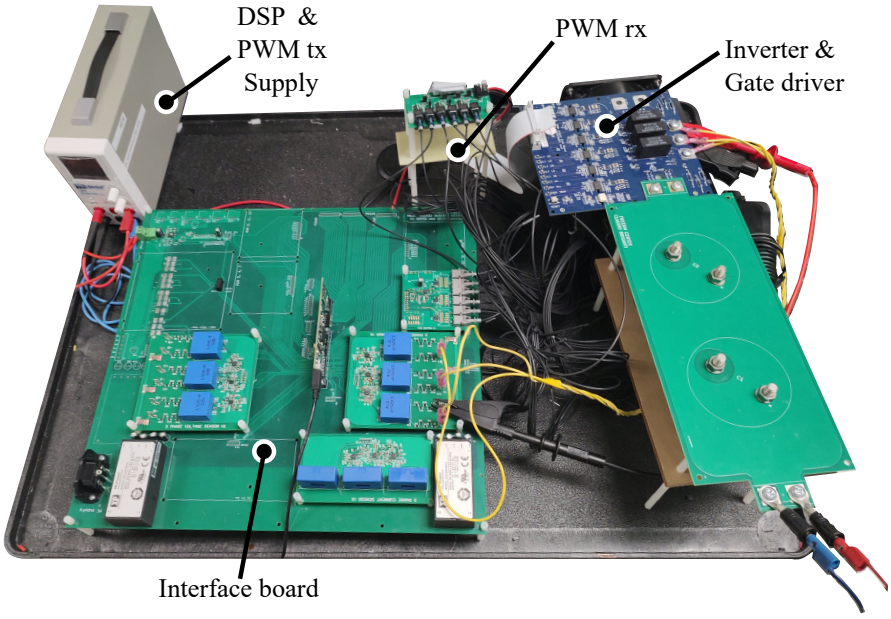


Figure 3.35: Setup for inverter test with no load

output B; whereas the one between phase B and C is measured connecting the positive side of the probe to inverter output B and the negative side to inverter output C. It is important to state that not to damage the oscilloscope it is mandatory to use differential probes.

The rest of the equipment employed includes:

- Global Specialities 1405 Power Supply: channel 3 supplies +5V to the DSP and the PWM transmitter card; channel 1 supplies +15V to the gate driver via the PWM receiver card.
- Chroma DC Power Supply (Model 62024P-600-8): provides V_{DC}.
- Teledyne LeCroy Wavesurfer 3024z oscilloscope. 4 channel, 4Gsa/s to display all the measured waveforms.

Unfortunately, the power supply in use is limited to 500V. Thus, the maximum obtainable phase voltage amplitude (with space vector modulation) is $V_{DC}/\sqrt{3} = 288.7V$, which is lower than the rated phase voltage of the motor.

The PWM signals to the gate driver are provided by the DSP on which the SVPWM code presented in 3.4.2 run in debug mode, so that any modification to the variables (as V_{DC}, f_o and output reference peak amplitude) can be performed without having to re-flash the code.

3.6.3 Simulation of inverter test with no load

Before proceeding, the system is simulated on PLECS to observe the expected output. The simulation schematic is shown in Fig. 3.36.

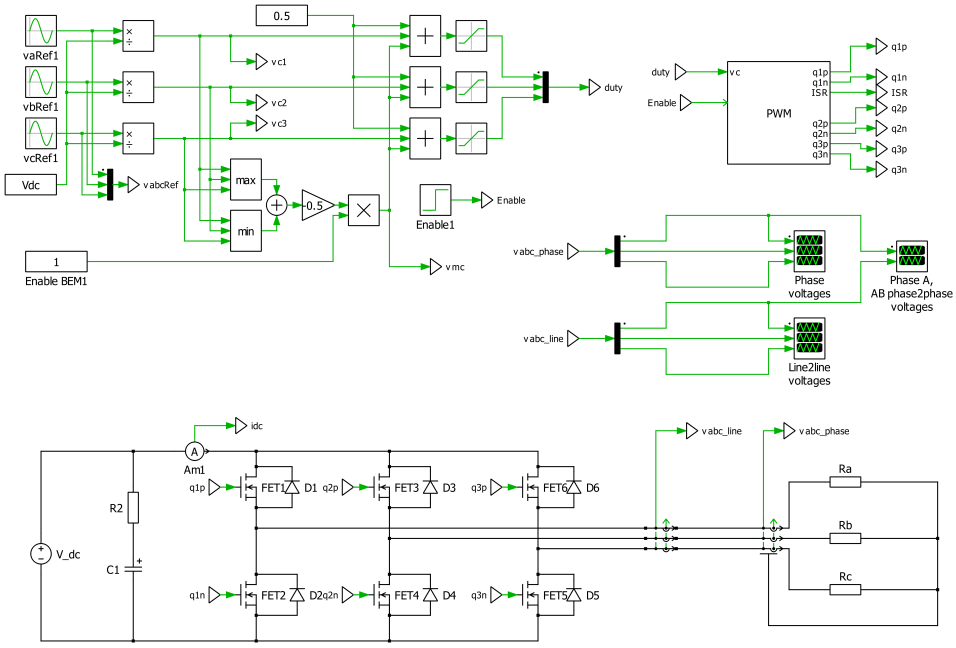


Figure 3.36: No load test simulation on PLECS

Simulation parameters are:

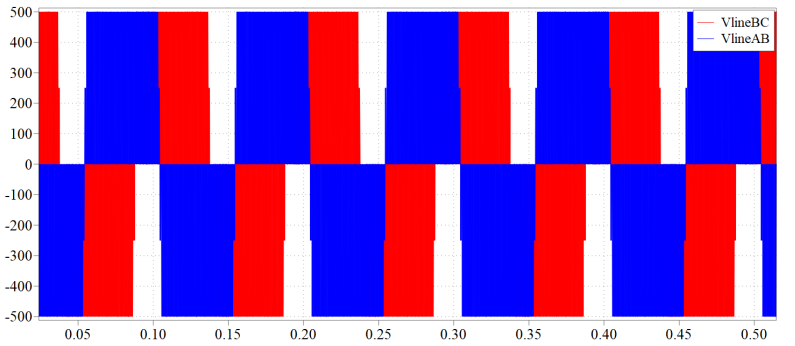
- $V_{DC} = 500\text{V}$;
- $f_{sw} = 32\text{kHz}$;
- $R_a, R_b, R_c = 50\,\text{k}\Omega$ (according to the schematic of the sensor board);
- $V_{ref,AMP} = 250\text{V}$;
- $f_{output} = 10\text{Hz}$, 1kHz.

The expected voltage waveforms are shown in Fig. 3.37 (a) and (b).

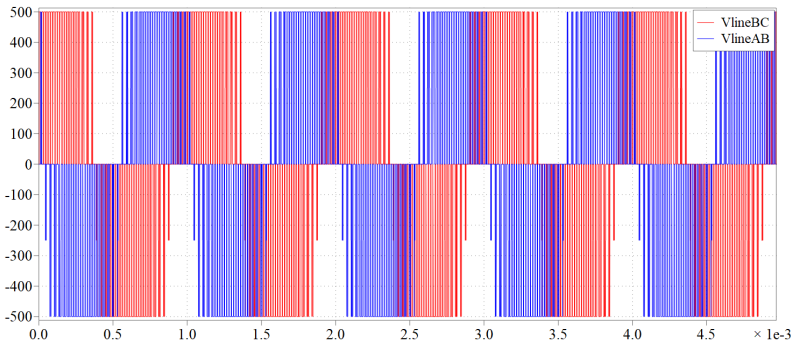
3.6.4 Results and conclusions

Moving to the actual test, before setting V_{DC} to 500V, only 3V is applied: This is done to validate the dead time without risking damaging the MOSFETs. The ON resistance of the MOSFETs is $90\,\text{m}\Omega$ and the maximum current is 20A, in the case of a short circuit of a leg with 3V applied, the current flowing would be 16.7 A.

After verifying no short circuit is happening, a first test is performed with $V_{DC} = 500V$ and setting the amplitude of reference sinusoidal voltage to 250V and output frequency to 10Hz. The line-to-line voltage measurements are shown in Fig. 3.38.



(a)



(b)

Figure 3.37: PLECS simulation waveforms at $V_{DC} = 500\text{V}$, $V_{ref,ampp} = 250\text{V}$ and $f_o = 10\text{Hz}$ in (a), 1kHz in (b)

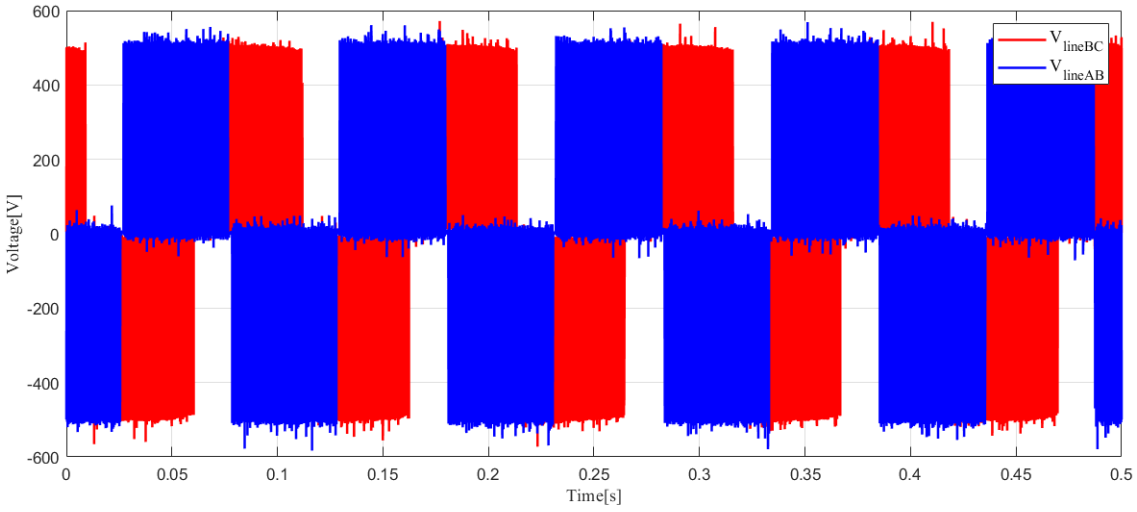


Figure 3.38: Three phase voltages with $V_{DC} = 500V$, $V_{ref,amp} = 250V$, $f_o = 10Hz$

Looking at Fig. 3.38 line to line voltage, It is already possible to see the output is

not exactly switching between $\pm 500V$ as can be observed in Fig. 3.39, the MOSFETs are switching between $\pm 500V$, but each switching action occurs with a significant 14% overshoot.

It is also possible to observe in both figures the output frequency is correctly matched.

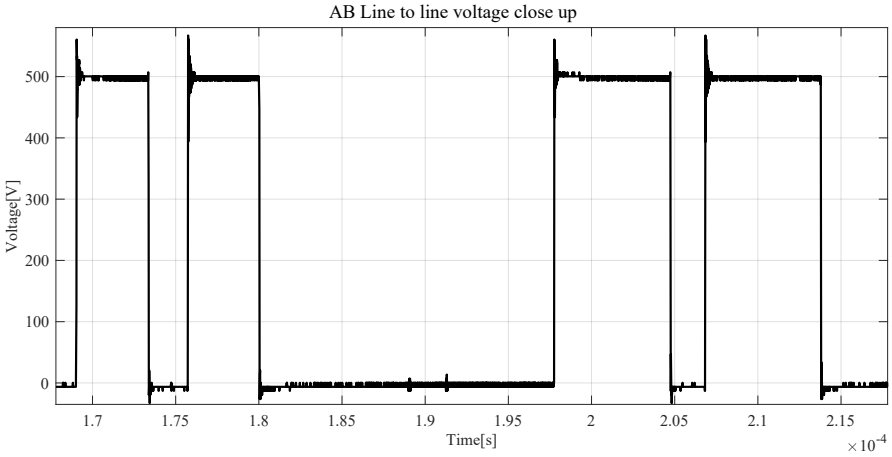


Figure 3.39: Zoom of the AB line to line voltage

The next test point is $V_{DC} = 500V$, amplitude of the sinusoidal reference of 250V and output frequency of 1kHz. The line-to-line voltage measurements are shown in Fig. 3.40.

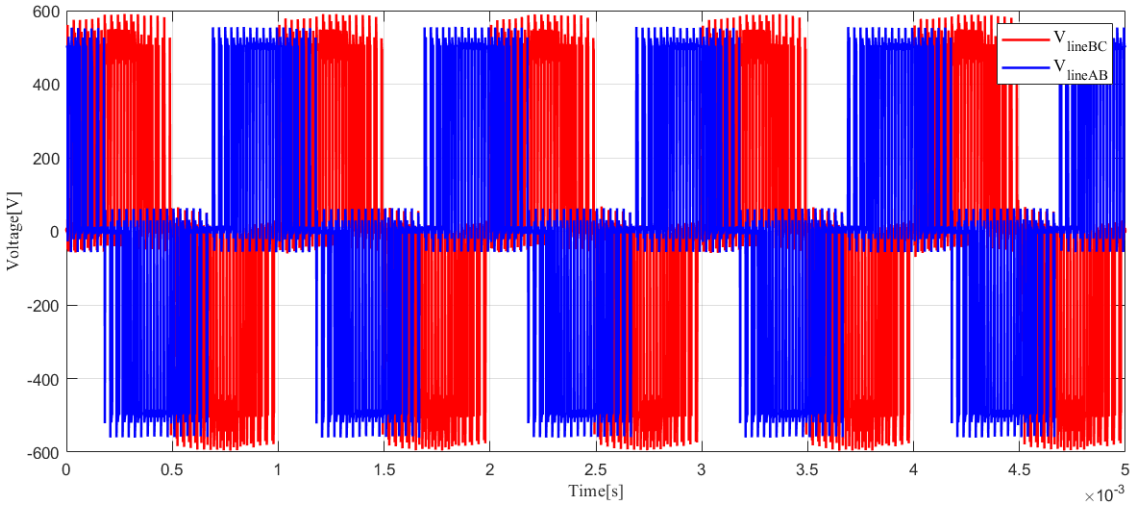


Figure 3.40: Three phase voltages with $V_{DC} = 500V$, $V_{ref,amp} = 250V$, $f_o = 1kHz$

The same reasoning applied in Fig. 3.38 can be applied to these results. It is possible to observe the output frequency is once again matched.

Spikes in inverter operations are not unusual, as they are generated by the parasitic capacitances and inductances present in the MOSFETs and by their resonant phenomena. Besides these, in this test the parasitic inductance is also increased by the cables that

connect the outputs of the inverter to the sensor board to create the reference point, which are almost 1m long and are not very well twisted. Moreover, not having any current makes the switches operate in hard switching conditions, which is particularly stressful.

Overall, the test is not completely satisfying as it was not possible to verify the outputs at the desired voltage levels. Nonetheless, the test introduces the problem of switching ripple and hard switching: these are the reasons why MOSFETs in inverter applications are designed to withstand up to double the V_{DC} coming from the supply.

3.7 Inverter Open-Loop test with RL load

3.7.1 Reasons for testing inverter with RL load

After having tested the inverter with no load, it is verified that it is capable of working in the voltage range intended for the motor use without high losses and highly distorted outputs. At this stage, it becomes necessary to verify its performances when a reactive load is attached to it.

This type of load is chosen because neglecting the back-emf (which plays a fundamental role at high speed), it is possible to model a motor as a resistive-inductive load. Hence, it is possible to retrieve a rough idea of how the inverter will perform when connected to the motor without having to care about any synchronism problem and without risking of damaging the motor in case of any malfunction.

3.7.2 Test setup

Fig. 3.41 shows the setup for the test.

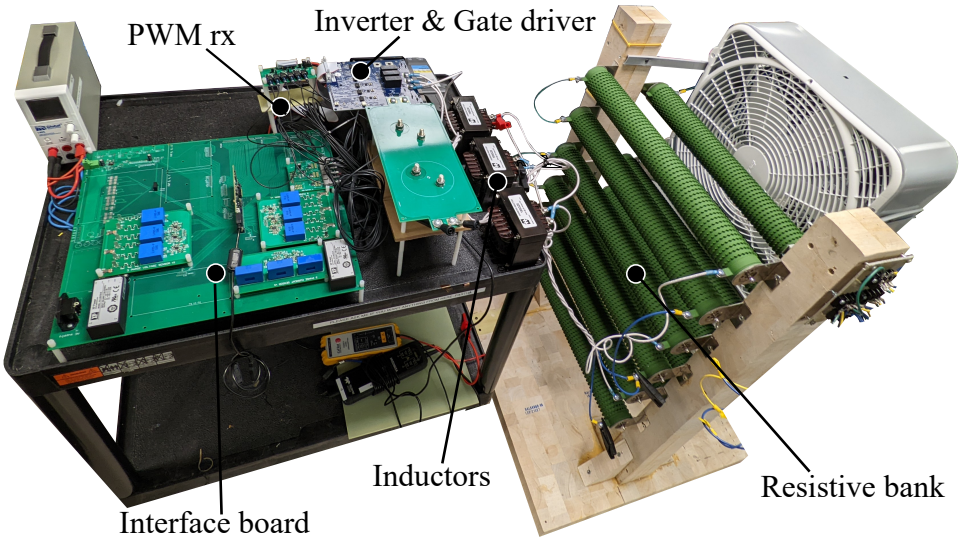


Figure 3.41: Setup for inverter Open-Loop test with RL load

The resistive bank consists of two sides, each with six 10 Ω, 2.5kW high power resistors

(High Power Wire Wound Resistor datasheet): only one of the two sides is employed, connecting the resistors in series two by two, in order to obtain a 20 Ω resistance per phase.

The inductors employed are 195G20 Hammond reactor (195G20 Hammond reactor datasheet): these are single coil DC Filter chokes intended for high current applications, not suggested for operations above 60Hz for long time. For this reason, it has been chosen not to go beyond 70Hz in this test. The inductance in the range 10-200Hz has been measured with E4980AL precision LCR meter, resulting in 3.68 mH.

The quantities measured during the test are the AB and BC line-to-line voltages and the A and B phase currents.

The rest of the equipment employed includes:

- Global Specialities 1405 Power Supply: channel 3 supplies +5V to the DSP and the PWM transmitter card; channel 1 supplies +15V to the gate driver via the PWM receiver card.
- Chroma DC Power Supply (Model 62024P-600-8): provides V_{DC}.
- Teledyne LeCroy Wavesurfer 3024z oscilloscope. 4 channel, 4Gsa/s to display all the measured waveforms.

Once again, being the Chroma DC Power Supply limited to 500V, it is not possible to go beyond 288.7V peak amplitude of sinusoidal output reference.

The test is conducted in an open-loop fashion, hence also this time the voltage and current sensors do not play any role. The code employed to generate the gate pulses is the same already employed for the test with no load.

3.7.3 Simulation

Before performing the test, the system is simulated on PLECS according to the schematic shown in Fig. 3.42.

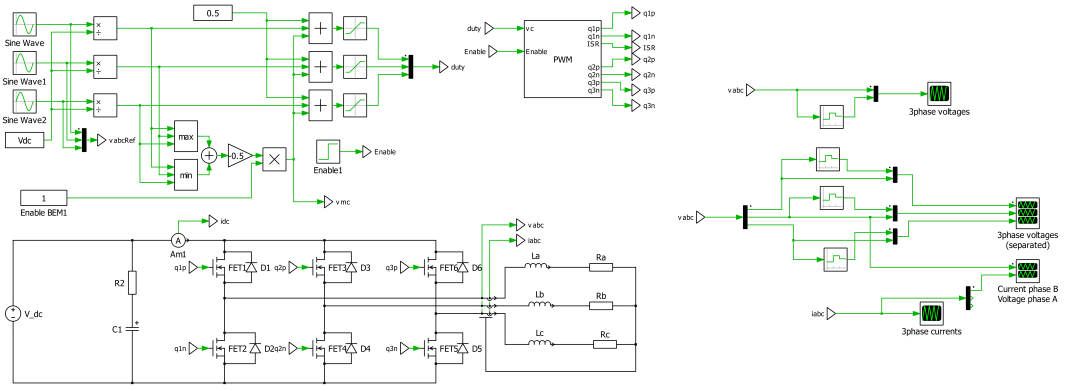


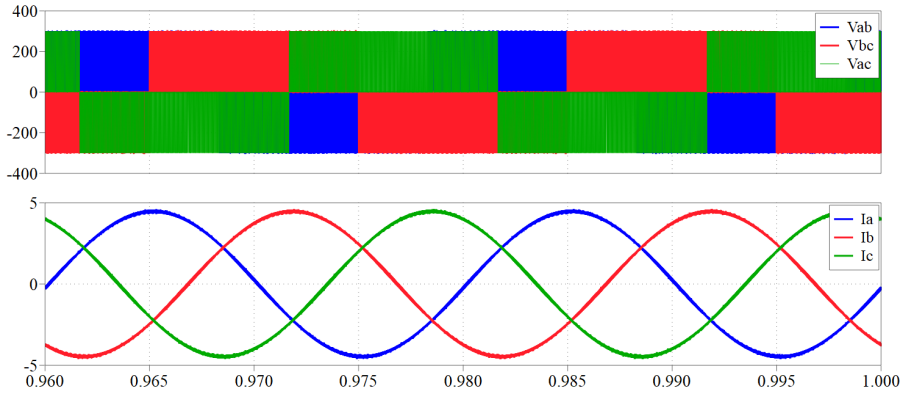
Figure 3.42: Schematic of inverter test with RL load in Open-Loop

The following test-points are simulated:

- $V_{DC} = 300V, F_o = 50Hz, V_{ref,pk} = 90V$

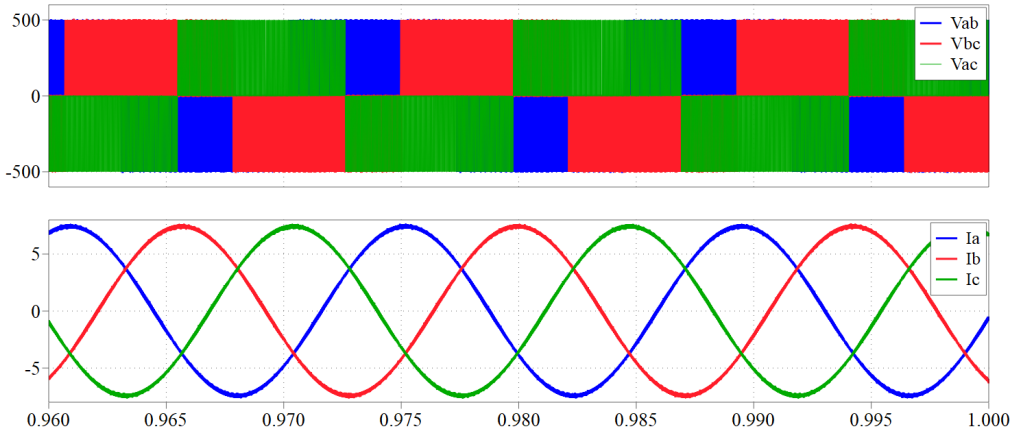
- $V_{DC} = 500V, F_o = 70Hz, V_{ref,pk} = 150V$

Results are shown in Fig. 3.43.



(a) $V_{DC} = 300V, F_o = 50Hz, V_{ref,pk} = 90V$

Figure 3.43: PLECS simulations of Inverter Open-Loop test with RL load



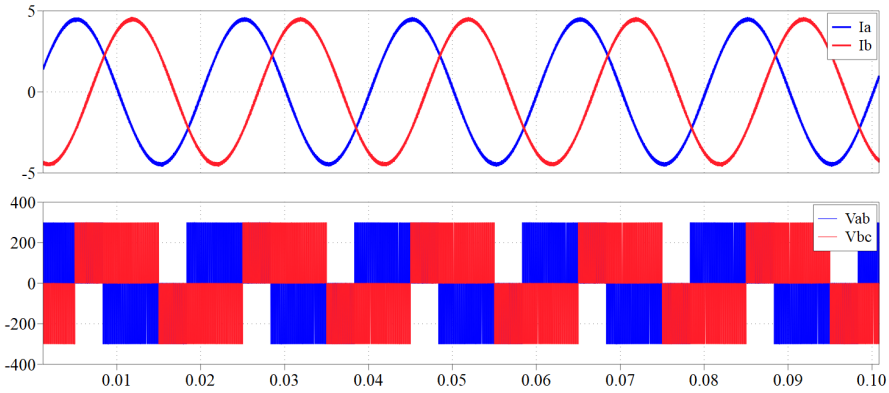
(b) $V_{DC} = 500V, F_o = 70Hz, V_{ref,pk} = 150V$

Figure 3.43: PLECS simulations of Inverter Open-Loop test with RL load

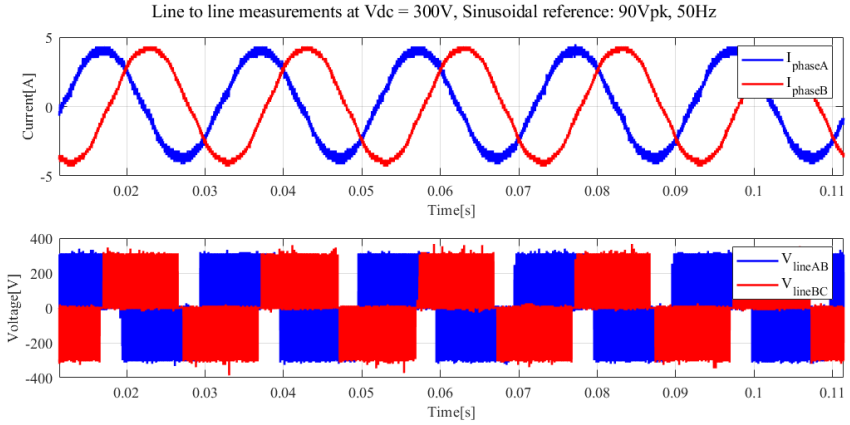
The peak amplitude of the phase currents in Fig. 3.43a is 4.6A and in Fig. 3.43b is 7.6A.

3.7.4 Test results and conclusion

For the sake of better understanding the results, the currents and voltages measured are shown together with the simulated ones, extracted from Fig. 3.43.

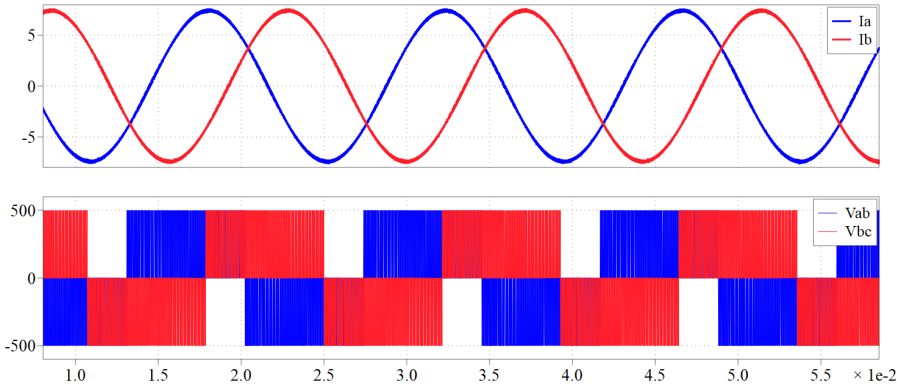


(a) Simulation results for current of phases A and B and AB, BC line-to-line voltage

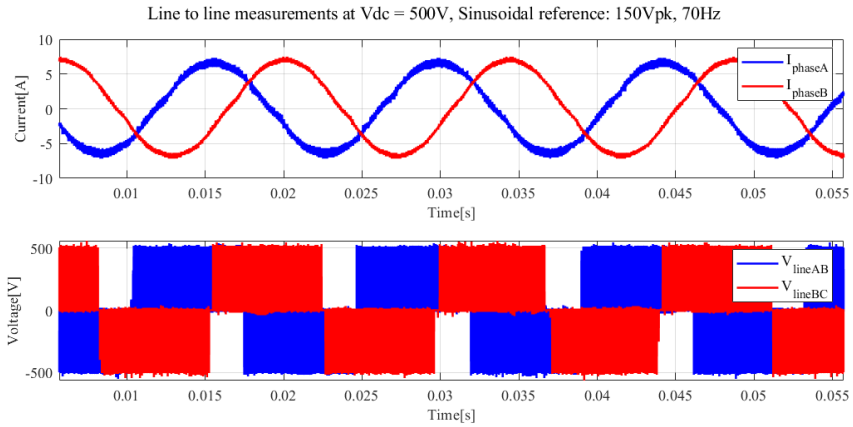


(b) Test results for current of phases A and B and AB, BC line-to-line voltage

Figure 3.44: Simulation and test at $V_{DC} = 300V, F_o = 50Hz, V_{ref,pk} = 90V$



(a) Simulation results for current of phases A and B and AB, BC line-to-line voltage



(b) Test results forcurrent of phases A and B and AB, BC line-to-line voltage

Figure 3.45: Simulation and test at $V_{DC} = 500V, F_o = 70Hz, V_{ref,pk} = 150V$

In both cases it is possible to state the system behaves according to the simulations. Hence, the test can be considered successful.

An interesting aspect to notice is the presence of a slight distortion in the phase currents when their value is 0: the cause lies in the dead-time, which introduces harmonics in the current that result in this distortion.

Chapter 4

Tests and simulations on the motor drive

4.1 Motor employed for the test

The motor on which the tests are conducted is a NV420EAI brushless servomotor by Parker. The most important parameters are shown in Tab. 4.1

Pole pairs	p		5
Peak torque	M_p	Nm	3.8
Current for peak torque	I_p	A_{rms}	10.3
Back-emf constant (100rpm, 24°)	K_e	V_{rms}	22.1
Torque sensitivity	K_t	Nm/A_{rms}	0.362
Winding resistance (25°, phase to phase)	R_b	Ω	1.94
Winding inductance(phase to phase)	L	mH	11.3
Motor mass	M	kg	3.8
Rotor inertia	J	$kgm^2 \cdot 10^{-5}$	29
Rated speed	N_n	14000	
Rated torque	M_n	Nm	0.95
Rated current	I_n	A_{rms}	2.87
Rated power	P_n	W	1390

Table 4.1: NV420EAI motor parameters

Given the table, the crucial parameters for the design and the simulation of the controller can be retrieved:

$$\begin{cases} R_s = 1.5 \cdot R_b = 1.455\,\Omega \\ L_s = 1.5 \cdot L = 8.5\text{mH} \\ K_t = \frac{K_{t(rms)}}{\sqrt{2}} = 0.256 \\ \lambda_m = \frac{2}{3}\frac{K_t}{p} = 0.0341 \end{cases} \tag{4.1}$$

4.2 V/f control

4.2.1 Implementation on DSP

The control shown in 2.7 is translated into C code to be implemented on the DSP and subsequently tested. The logic of the algorithm is shown in Fig. 4.1.

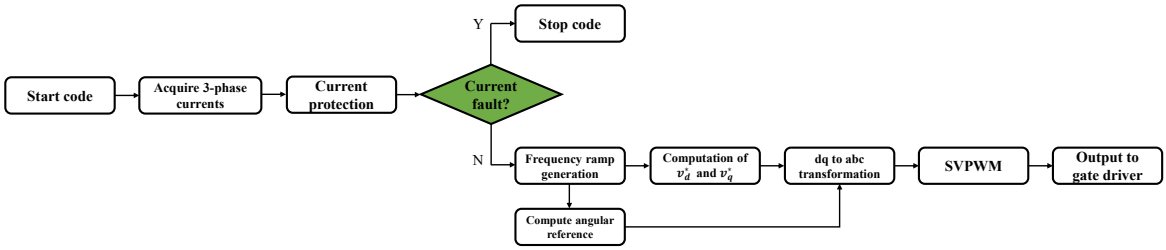


Figure 4.1: Function calls made during operation of the V/f control on the DSP

The first action consists in acquiring the three-phase currents flowing through the motor with the use of the ADC functions presented in 3.4.3. These are not strictly needed for control purposes, but are used as a safety measure to avoid any risk of damage to the system components.

At this point the current protection function is called. For each of the three phases the following actions are performed:

- While the phase current is above the motor rated current, a timer counts for a desired time: after that, all the switches are turned off;
- If the current exceeds the motor current for peak torque, all the switches are immediately turned off.

In case all the switches are turned off, a fault flag is set to 1 and the code enters a stand-by mode.

In case no fault is detected, the frequency ramp generator function is called to linearly increase the value of the frequency with an increase rate of 1.5. The function also computes the reference angular position used in the direct and inverse Park transformations: the frequency is first converted from Hz to rad/s and then integrated. The angular reference is then saturated at $\pm\pi$.

With the updated value of the frequency, it is possible to compute the reference value v_q^* according to the following relation:

$$v_q^* = 0.6 + 0.22 \cdot f \tag{4.2}$$

Where the bias of 0.6 V is retrieved from the motor back-emf constant K_e at 1000rpm:

$$v_q^*(0) = \frac{60 \cdot \sqrt{2}}{\pi} \frac{K_e(1000rpm)_{rms}}{1000} \tag{4.3}$$

It is needed to compensate the neglected terms which play a role at low speeds.

The slope equal to 0.22 is retrieved from the permanent magnet value:

$$\frac{V_q}{f} = 2\pi\lambda_m = 2\pi \cdot 0.0341 \approx 0.22 \tag{4.4}$$

The reference voltages are then converted into *abc* measures by means of two functions implementing the Park and Clarke transformations. The new *abc* references are the input of the SVPWM function where the output signals for the gate driver are generated.

4.2.2 Test setup

The setup to carry out the test is shown in Fig. 4.2.

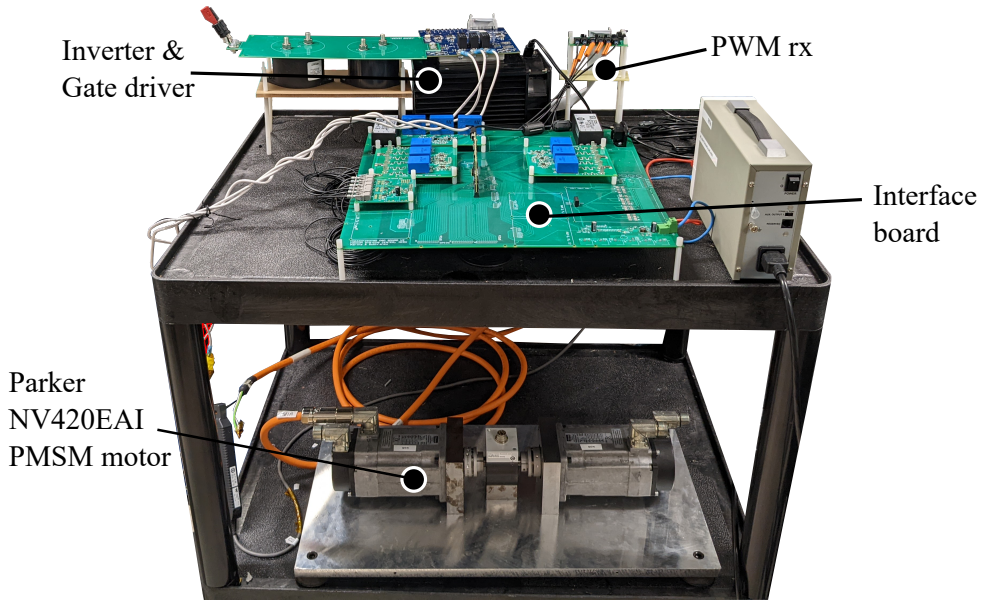


Figure 4.2: Setup for full electric drive test

The equipment employed to power the eDrive system and perform the measurements is the same employed in the inverter open-loop test with RL load.

Due to a lack of probes during the time the test is carried out, the only measured quantities are AB and BC line-to-line voltages and phase A current.

The main goal of this test is to understand how fast can the V/f open-loop control run the motor before it starts stalling and to ensure that using this technique no overcurrent phenomenon occurs.

4.2.3 Simulation on PM motor

Before performing the test, the system is simulated on PLECS according to the schematic shown in Fig. 4.3

The parameters for the simulation listed below, are the same employed for the actual test:

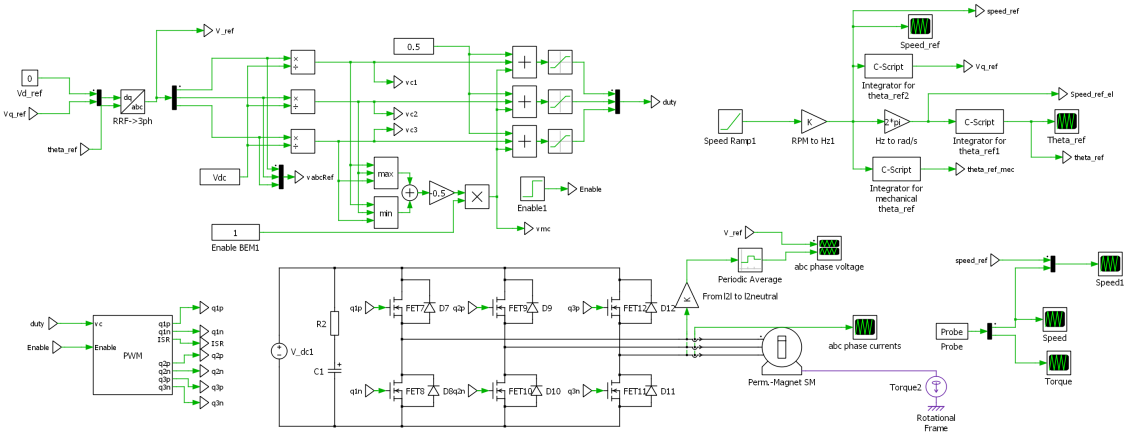


Figure 4.3: Schematic of eDrive with V/f control simulation

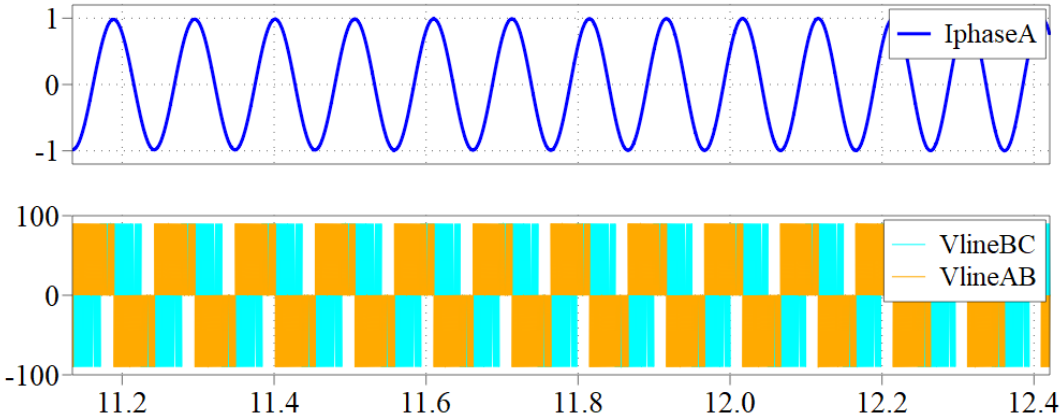
- $V_{DC} = 90$ V;
- $f_{sw} = 20$ kHz;
- Frequency increase rate of 1.5;

The results are compared with the test results in the following section.

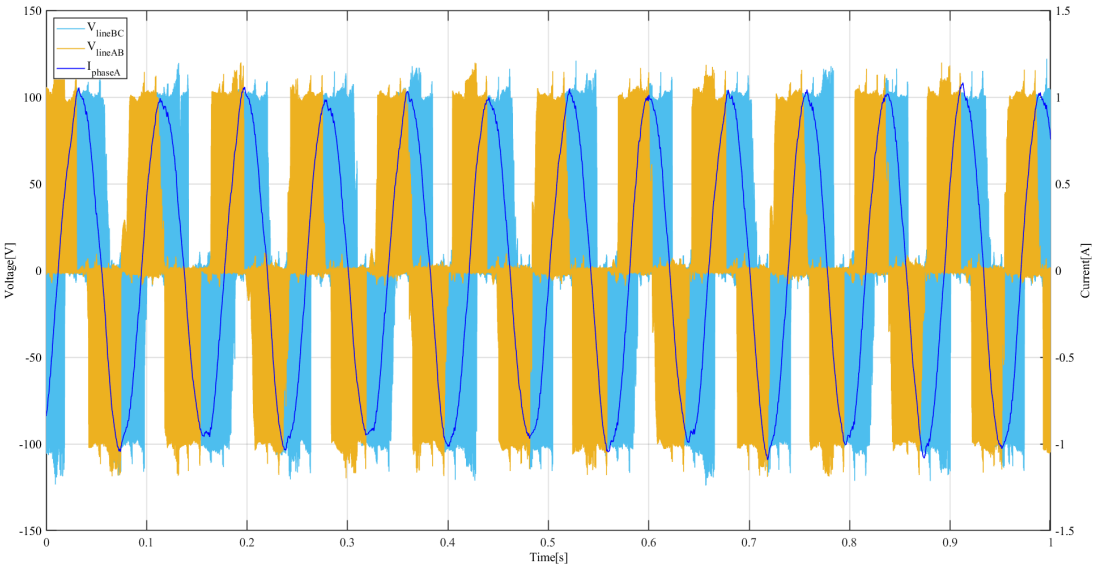
4.2.4 Test results and comparison with simulation

After launching the test, the motor starts running smoothly.

The first measurements capture is performed when the output current is at 12 Hz, corresponding to a mechanical speed of 144 rpm. Fig. 4.4 shows a comparison between the simulation and the test results.



(a) Simulation results for current of phase A and AB, BC line-to-line voltages

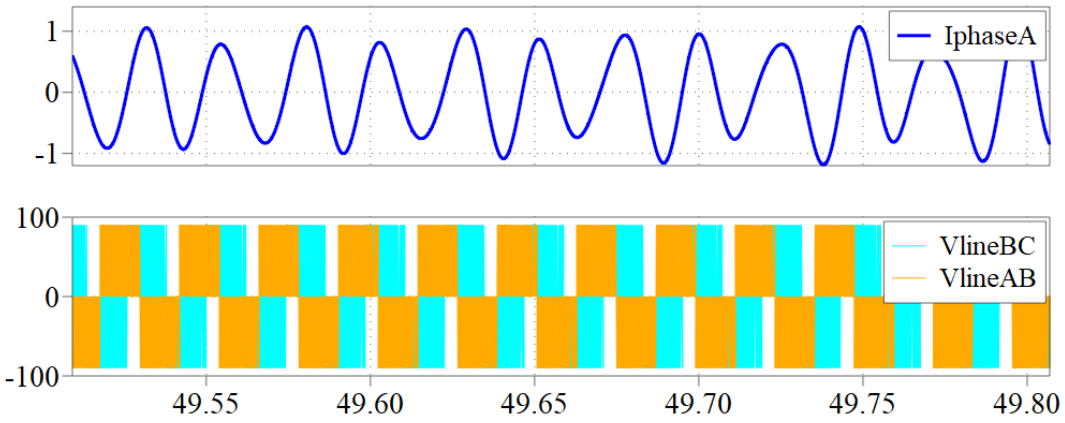


(b) Test results for current of phase A and AB, BC line-to-line voltages

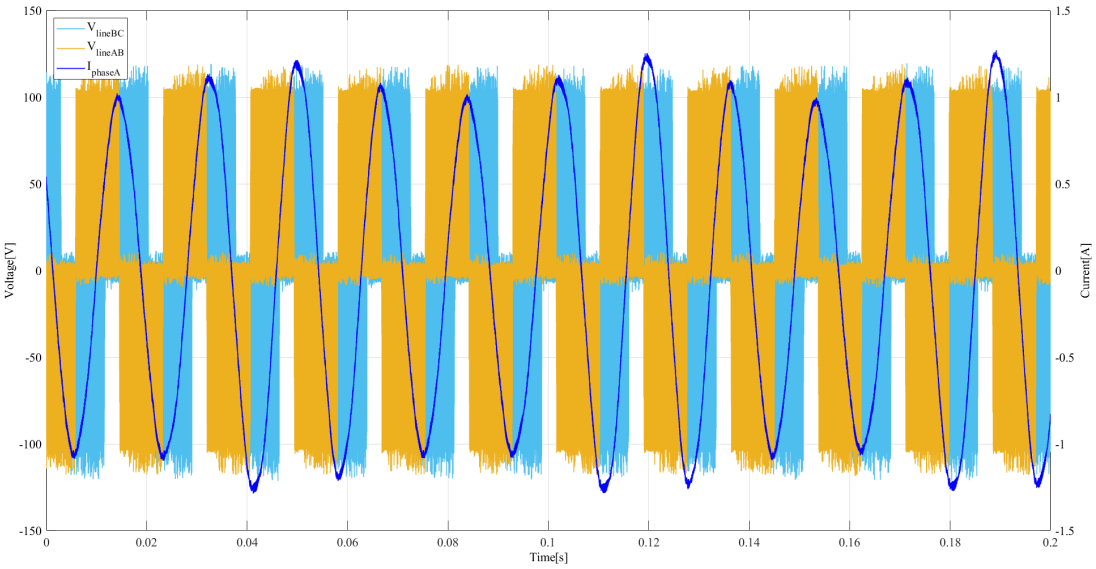
Figure 4.4: Starting stages of V/f control on eDrive

The shape of the waveforms matches except for some noise, especially visible in the line-to-line voltages which shows the turn-on spikes already described in previous tests.

Keeping the motor running, no issue occurs until an electrical frequency of 51 Hz (correspnding to a mechanical speed of 636 rpm) is reached. The waveforms at this operating point are shown in Fig. 4.5.



(a) Simulation results for current of phase A and AB, BC line-to-line voltages



(b) Test results for current of phase A and AB, BC line-to-line voltages

Figure 4.5: Starting stage of V/f control on eDrive

It is possible to observe in both the simulation and the oscilloscope output that the current slightly oscillates in both amplitude and frequency. This is the first symptom of loss of synchronism.

Keeping the motor spinning for a few more seconds, the oscillations become even more noticeable as shown in Fig. 4.6.

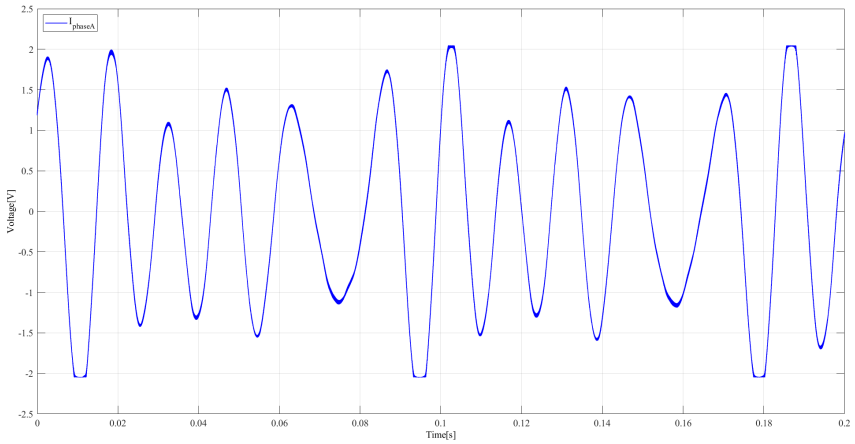


Figure 4.6: Oscillatory behaviour of phase A current during V/f test

At this point the motor stops spinning and shortly after the current protection implemented completely shuts down the system as the current was dangerously increasing.

Fig. 4.7 shows the comparison between the reference and measured electrical speed in the simulation performed on PLECS.

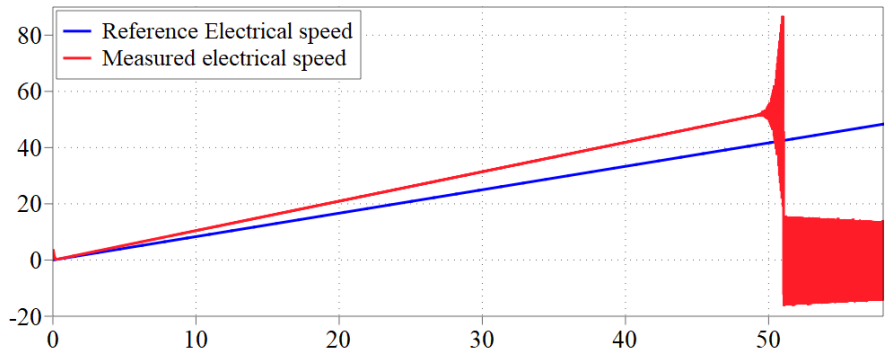


Figure 4.7: Reference electrical speed vs Measured electrical speed in V/f PLECS simulation

From this figure we can conclude that actual speed of the motor is always above the reference one, with their difference constantly increasing: at a certain moment, the difference becomes too large, leading to the loss of synchronism.

The test can be deemed concluded, matching with the simulation expectation of being able to run the motor until a speed of roughly 630 rpm.

4.3 I/f control

4.3.1 Implementation on DSP

The control shown in 2.15 is translated into C code to be implemented on the DSP and subsequently tested. The logic of the algorithm is shown in Fig. 4.8.

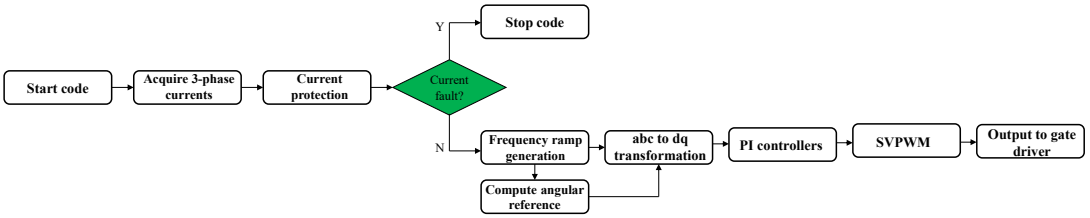


Figure 4.8: Function calls made during operation of the I/f control on the DSP

Similarly to the V/f algorithm, the first action consists in acquiring the three-phase currents and verify the peak values do not exceed the limits. Afterwards, the frequency ramp generator function is called: for the first 1000000 times the function is called (which corresponds roughly to 5 seconds) the frequency is kept at 0. This is done to give time to the rotor to align at 0°position. Subsequently, the ramp starts with an increase rate equal to 3.

Also in this case, the function computes the reference angular position used in the

direct and inverse Park transformations. Next operation consists in converting the measured three phase current first into $\alpha\beta$ reference frame and successively into dq reference frame according to Eq. 2.5, 2.6 presented in Section 2.1.

Once the feedback measurements are converted into the dq reference frame, the PI controller function is called. In this block, current compensation for both d and q axes is performed. To store the data of the two PI controllers, a struct is defined as shown in Tab. 4.2.

Variable	**Description**	**Data type**
Kp	Proportional term gain	float
Ki	Integral term gain	float
Out_max	Upper limit for output	float
Out_min	Lower limit for output	float
Ref	Reference value	float
Prop	Proportional term	float
Int	Integral term	float
prevError	Error computed at previous iteration	float
Sat_flag	1 if PI output saturates, 0 if not	uint8_t
Out	Sum of integral and proportional term	float
Sat_out	Saturated PI output	float

Table 4.2: Structure of PI object

First, the error in this iteration is computed subtracting the measured d and q current to the reference d and q values. Proportional terms are obtained multiplying the errors by k_p. The discrete integral term includes also anti-windup feature and is computed through the trapezoidal rule as shown in Eq. 4.5.

$$\text{Int} \mathrel{+}= \frac{T_s}{2}(e(n) + e(n-1)) * \text{Sat\_flag} \tag{4.5}$$

For each PI controller, the output is computed summing the proportional and integral term. The output of each axis is then compared with the maximum allowed value (in this application $V_{max} = 150V$, decided observing in simulations that the voltage amplitude during the test never exceed 100V) and eventually saturated, according to Eq. 2.56.

In the event of output saturation, the saturation flag (normally set at 1), changes its value to 0. This flag multiplies the integral term, as shown in Eq. 4.5: setting it to 0 neglects the integral term contribution in case of controller saturation, accounting for the anti-windup

The updated output of the PI controllers, is then transformed from the *dq* frame to the *abc* frame and sent as input to the SVPWM block which will subsequently generate the signals to send to the gate driver.

4.3.2 Tuning the PI controllers

The design of k_p and k_i is performed according to the relations presented in Section 2.9. First of all, the desired bandwidth must be chosen. For this application $f_b = 200Hz$ is

deemed sufficient.

Consequently:

$$\begin{cases} k_p = L_s w_b = 10.65 \\ k_i = \frac{1}{10} k_p w_b = 1338 \end{cases} \tag{4.6}$$

The resulting bode plots of the open loop and closed loop reference-to-output transfer functions are shown in Fig. 4.9,

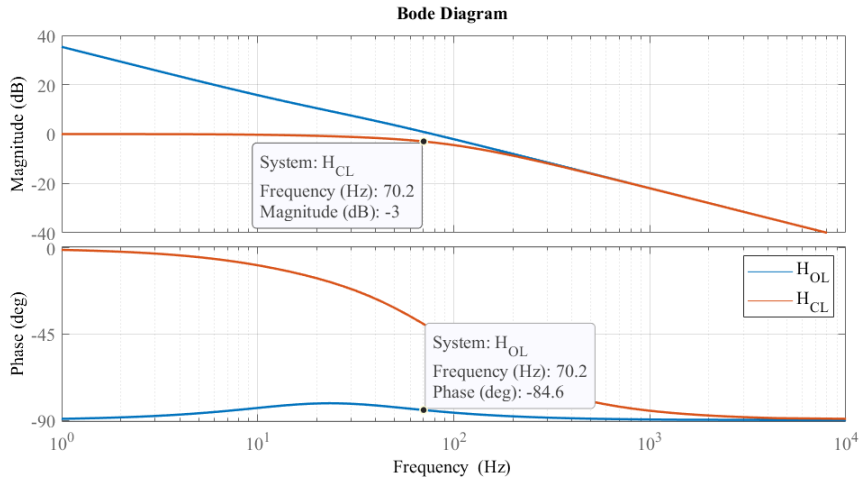


Figure 4.9: Bode plots of the open and closed loop current loop transfer functions

From the figure it is possible to observe the behaviour matches the ideal one and the stability criteria are respected. In fact, the phase margin can be computed:

$$\Phi_{PM} = |\Phi_{OL}|_{f=f_c} + 180° = 95.4° \tag{4.7}$$

4.3.3 Test setup on RL load

Accordingly to what stated in Sec. 3.7.1, the I/f control is firstly simulated and tested on the same RL load on which the open loop test has been performed. Also the employed equipment is the same already presented.

The value of the proportional and integral gains have to be recomputed based on the new values of resistance and inductance. The procedure is the same presented in the previous section.

The resulting k_p and k_i are:

$$k_p = 5 \qquad k_i = 28270$$

The quantities measured for this test are phase A voltage and phase A,B currents.

The main objective of this test is to ensure the correct tracking of the reference current, without creating any overcurrent or overvoltage and to evaluate the response to

a step variation in the reference current. As this is a static load, there is no concern about synchronism, but just the evaluation of the code written for the compensators.

It is also necessary to point out that, similarly to the open loop test, the maximum frequency at which the test is performed is 75Hz due to the type of available inductors.

4.3.4 Simulation on RL load

Before carrying out the test, the system is simulated on PLECS according to the schematic shown in Fig. 4.10.

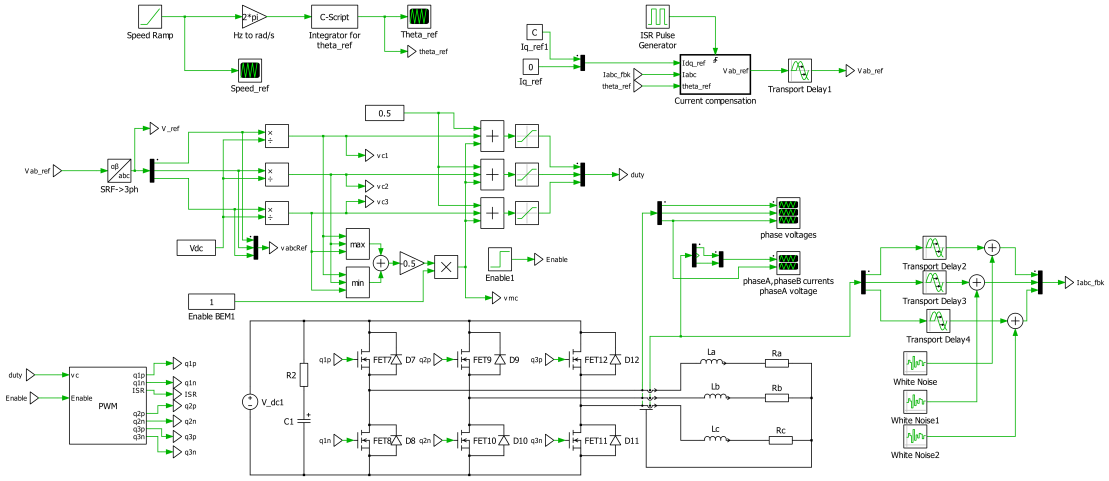


Figure 4.10: Schematic of I/f simulation on RL load

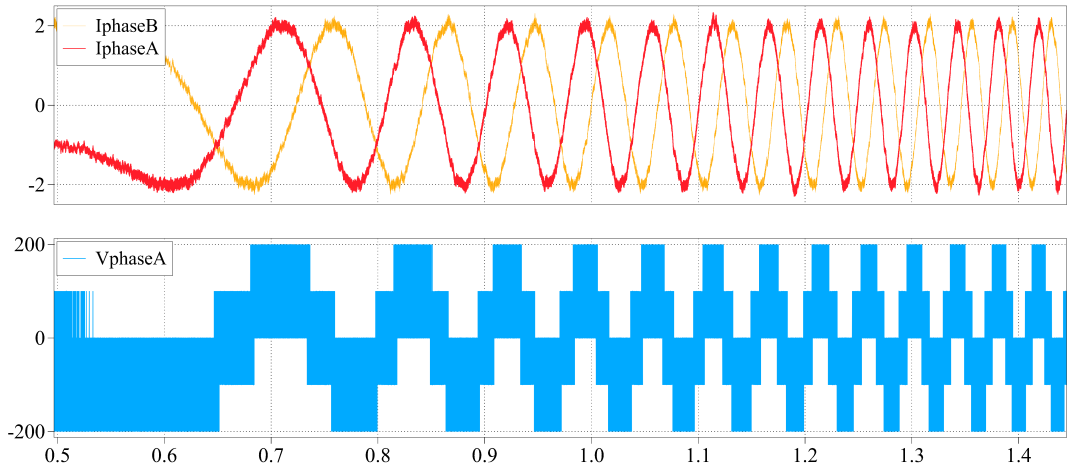
The parameters for this simulation, which are the same employed in the actual test are:

- $V_{DC} = 300$ V
- $f_{sw} = 20$ kHz
- Dead time of 500ns
- Frequency increase rate of 3
- Initial reference current amplitude of half motor rated current (2 A)
- Step variation in the reference current amplitude to 4A

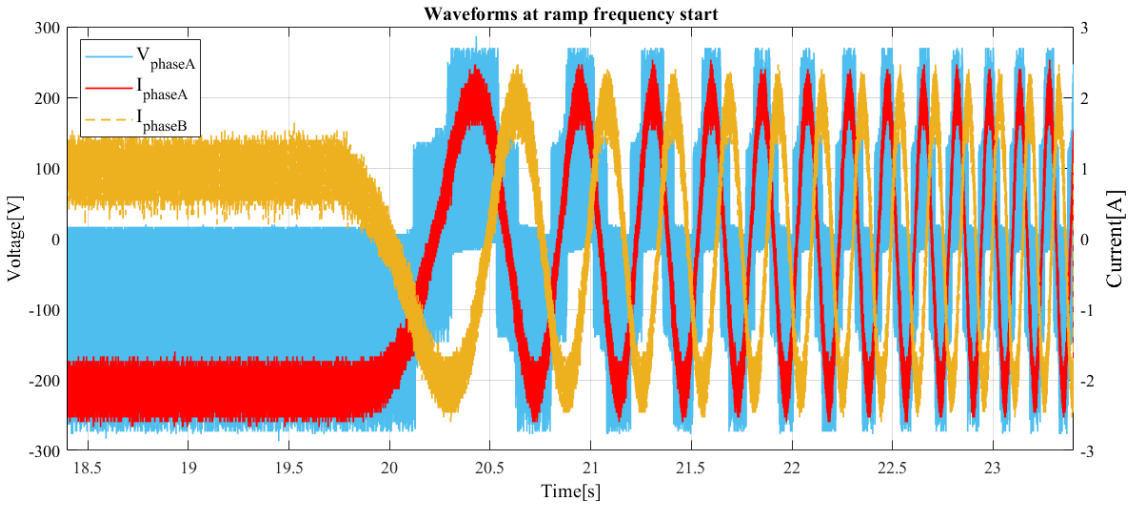
The results of the simulations are compared with the test results in the following section.

4.3.5 Test results on RL load and comparison with simulation

The first moment worth capturing is directly at the launch of the test, when the current vector starts rotating, moving from the d-axis where it has been held for a few seconds



(a) Simulation results for current of phases A and B and A phase voltage



(b) Test results for current of phases A and B and A phase voltage

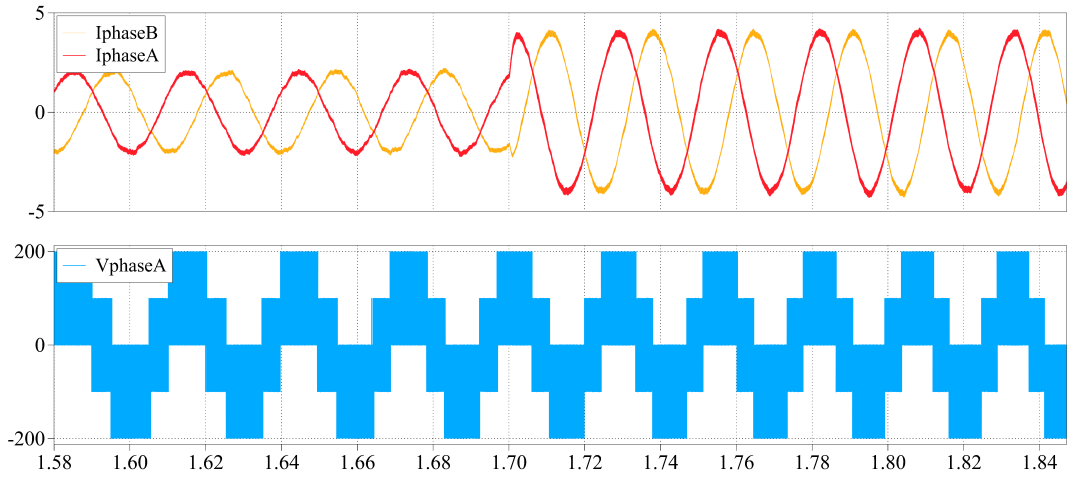
Figure 4.11: Ramp start of I/f control on RL load

to align the rotor and stator magnetic axes. Fig. 4.11 shows the comparison between the simulation and the actual test.

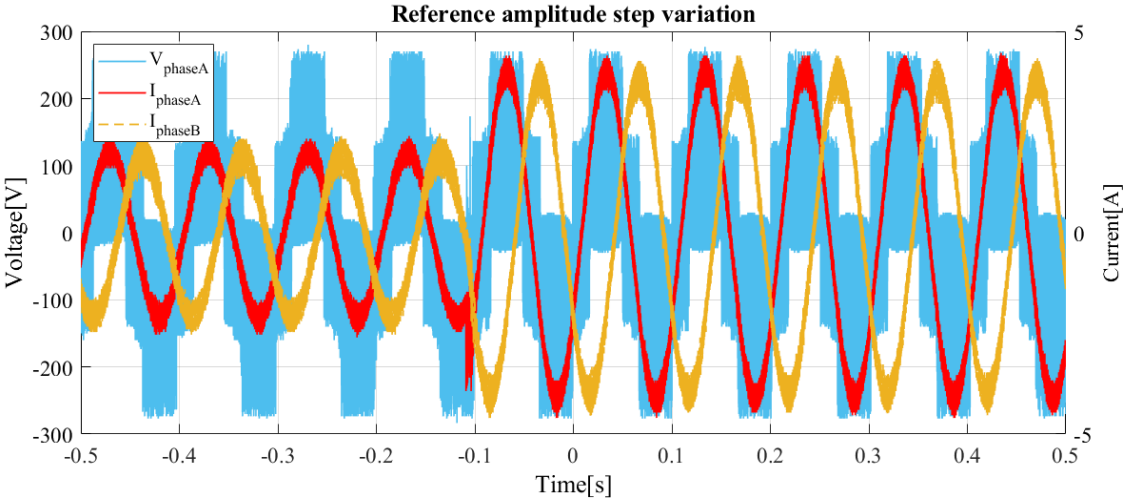
The tracking performance at the start can be deemed satisfying as the transition from constant current to sinusoidal current is smooth and without distortions. The phase voltage once again shows peak values higher than the ones retrieved in simulation, but this is once again due to the turn-on spikes generated by the parasitics.

The next important aspect to evaluate is whether the technique behaves well in the case of a step variation of the reference current. Fig. 4.12 shows the comparison between the simulation and the actual test.

The dynamic response is adequate, happening in less than a period. The spike visible (although not very high) in the test result and not in the simulations is due to the



(a) Simulation results for current of phases A and B and A phase voltage



(b) Test results for current of phases A and B and A phase voltage

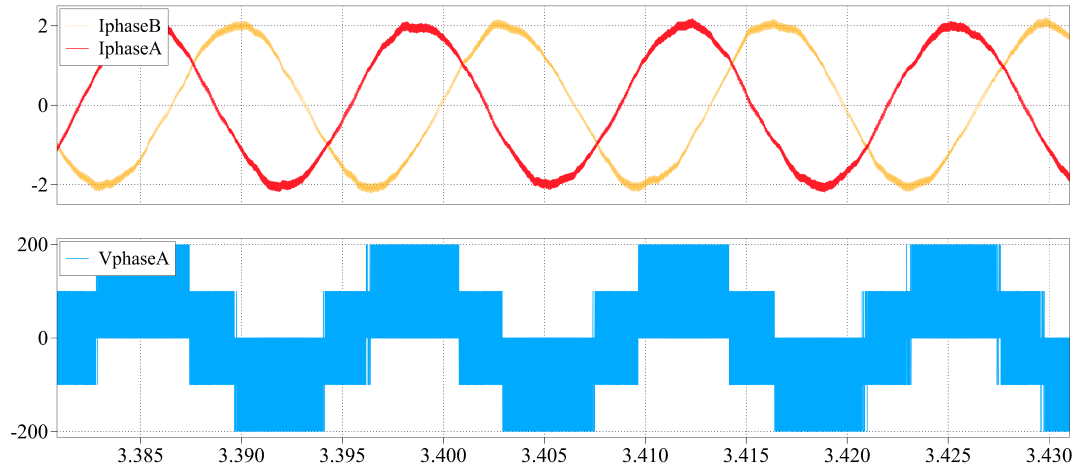
Figure 4.12: Reference current step change in I/f control on RL load

parasitics in the physical components, but it does not represent a concern.

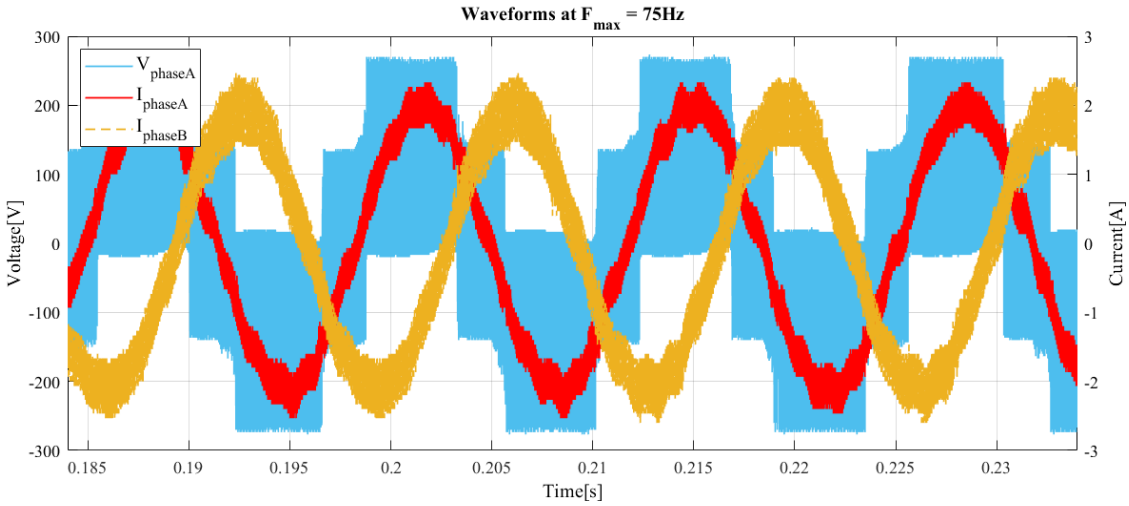
Lastly, it might be interesting to notice that at the maximum test speed, the system still behaves good and there are no distortions in the phase currents and voltage. This is shown in Fig. 4.13.

The test waveforms might not seem very clean: this is due to the large number of samples at which the capturing has been performed, necessary to show the transient phases and the phase voltage too. A large number of samples enhances the noise capture, making the waves less good looking.

The test can overall be deemed satisfactory, showing that the current response on a passive load is good and that the reasoning behind compensators tuning correctly works.



(a) Simulation results for current of phases A and B and A phase voltage



(b) Test results for current of phases A and B and A phase voltage

Figure 4.13: Maximum test speed in I/f control on RL load

4.3.6 Test setup on PM motor

Successively to the current compensators validation on RL load, the I/f control technique can be tested on the motor. The setup is the same employed for the V/f test on the motor shown in Fig. 4.2.

The objective of the test is to evaluate how fast it is possible to spin the motor without any position feedback with this technique before it stalls. Moreover, the dynamic response to a step variation in the reference current amplitude is evaluated.

The employed equipment, DC supply, PWM switching frequency, dead time and reference current peak values are the same tested with the RL load. However, in this

case instead of measuring phase voltages, it has been preferred to measure the line-to-line voltages. Moreover, the two digital-to-analog converters (DAC) channels available on the DSP to monitor controller internal variables like modulation indices and i_d and i_q currents.

4.3.7 Simulation on PM motor

As usual, before carrying out the test, the system is simulated on PLECS with the schematic shown in Fig. 4.14

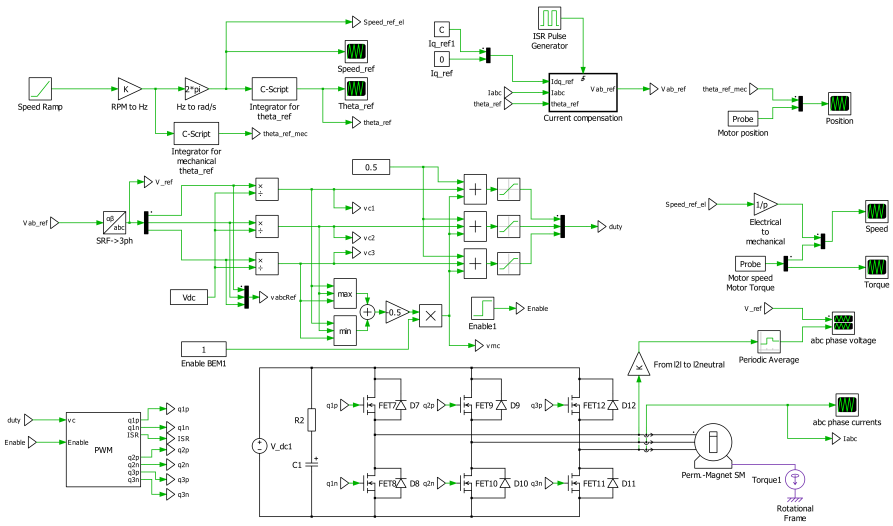


Figure 4.14: Schematic of I/f simulation on complete eDrive

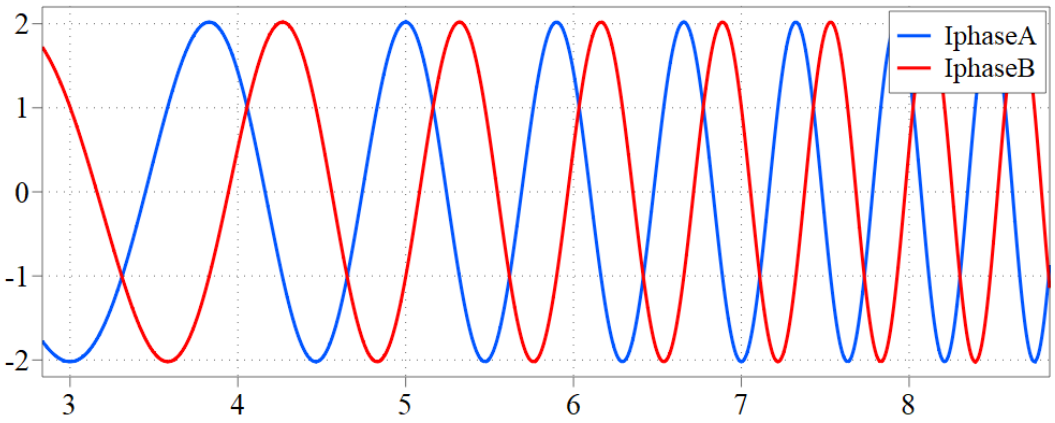
The parameters for the simulation are the same employed for the RL test and simulation and are also used in the actual test.

The results of the simulations are compared with the test results in the following section.

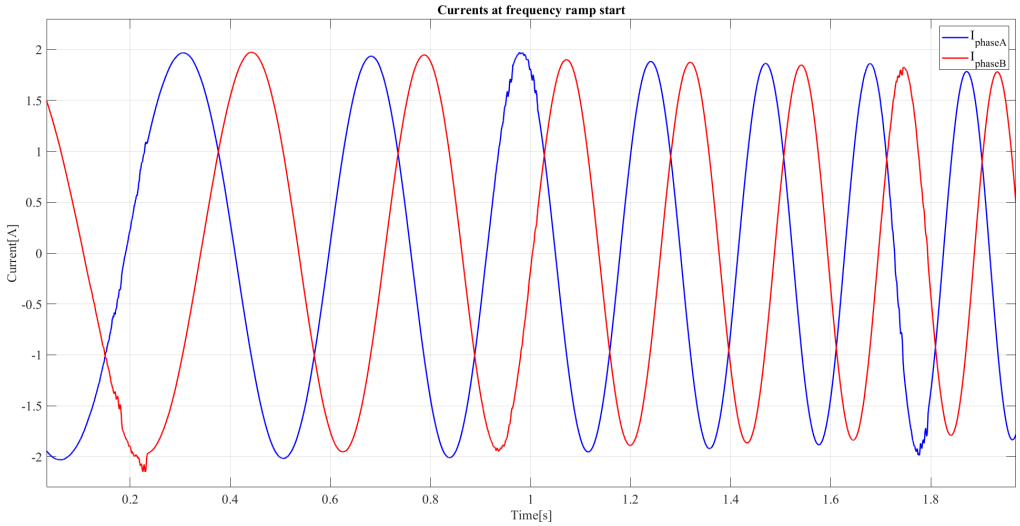
4.3.8 Test results on eDrive and comparison with simulation

When the test is launched, it is immediately possible to hear the instantaneous noise of the rotor aligning with the direction of the stator magnetic field. After having waited a few seconds in the same position, the motor starts spinning smoothly. As already done in the RL test, the measured quantities are captured the start of the ramp, when the electrical frequency is below 10Hz (120 rpm). Fig. 4.15 shows the comparison between the results from the simulation and the actual test.

Afterwards, the motor is kept spinning for a few more seconds, until the frequency of the output current reaches 60Hz (720 rpm). At that moment, step change in the current peak reference is performed. This measurement has been performed on all three phase currents to also verify that they are 120°shifted. Fig. 4.16 shows the comparison between the results from the simulation and the actual test.



(a) Simulation results for current of phases A and B



(b) Test results for current of phases A and B

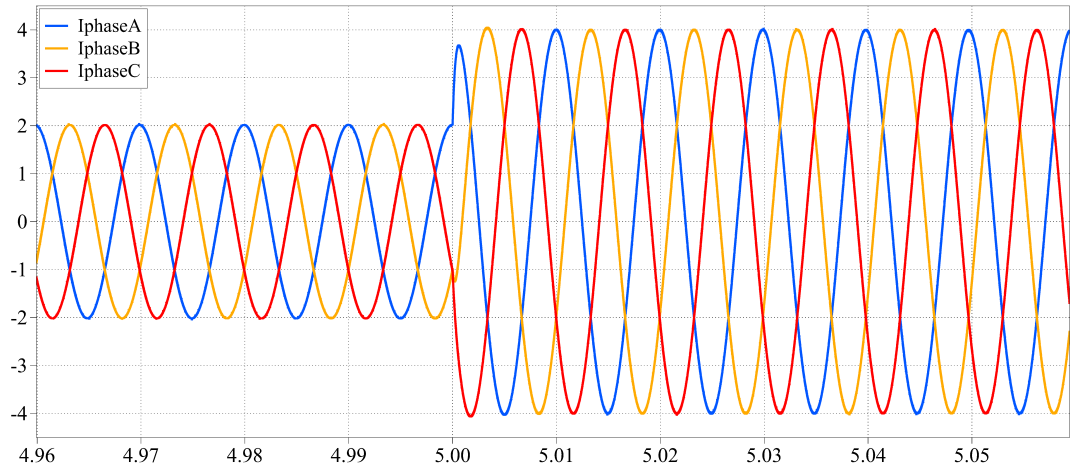
Figure 4.15: Starting stages of I/f control on motor

To further analyze the speed of response in the presence of the reference step variation, the DAC is set to show the behaviour of i_d and i_q. The voltage range of the DAC pins is 0-3V for the DSP employed, the range of the current under analysis is 0-4A. This means that in order to plot the results in the exact range, a remapping must be performed:

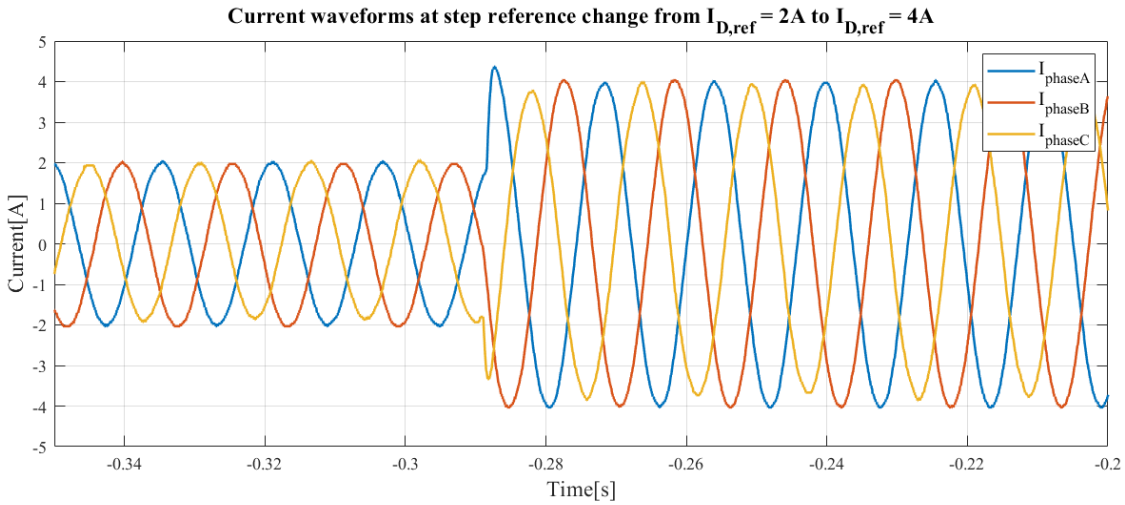
$$I_{DAC} = 4 \cdot \frac{V_{DAC}}{3} \tag{4.8}$$

Fig. 4.17 shows the i_d and i_q currents after remapping.

From this figure it is possible to state that the rising time is 0.04s. Considering that the frequency of the output current waves is 10Hz when the reference step change is performed (corresponding to a period of 0.1s), the response takes less than half a period,



(a) Simulation results for current of phases A,B and C



(b) Test results for current of phases A, B and C

Figure 4.16: Reference step variation in I/f control on RL load

which is more than acceptable.

The DAC is also exploited to capture the modulation indices generated by the control with reference current amplitude of 4A. In this case the range of the modulation indices is 0-1, hence the necessary remapping is

$$M_{idx} = \frac{V_{DAC}}{3} \tag{4.9}$$

The remapped modulation indices for phase A and phase B in Fig. 4.18.

From the figure it is clearly visible that the shape of the modulation indices matches the theoretical ones for the SVPWM technique shown in Fig. 2.12, with some inaccuracies due to the errors in the current sensors. Moreover, we can also state that the region of

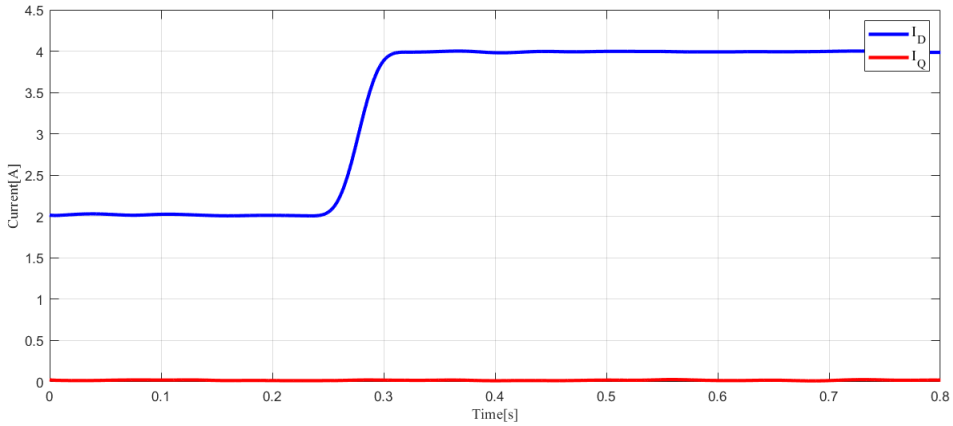


Figure 4.17: i_d and i_q currents response to reference step variation from DAC after remapping

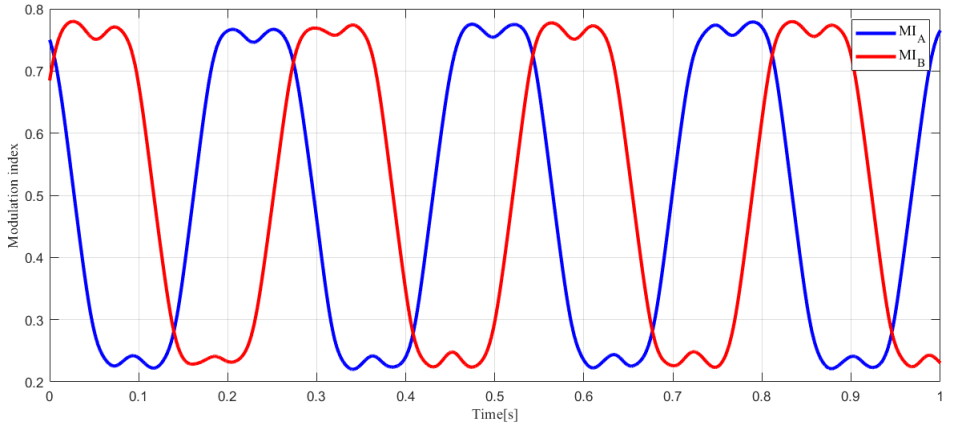


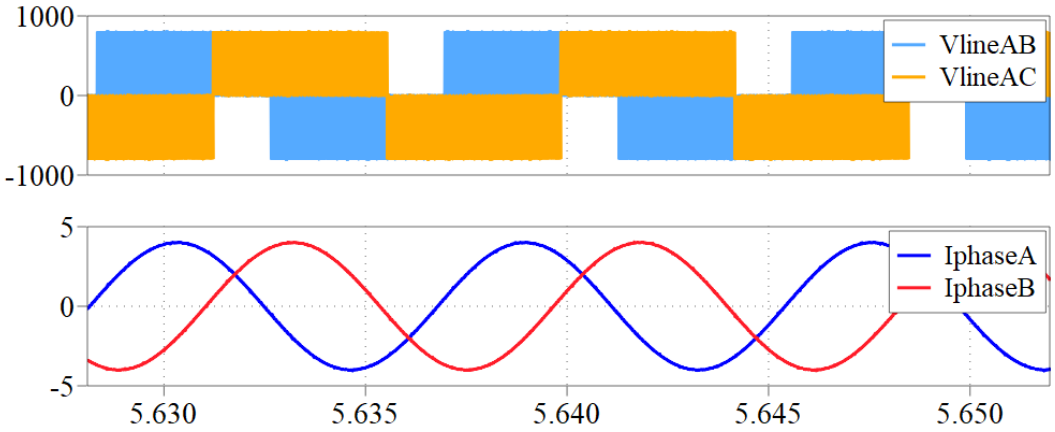
Figure 4.18: Modulation indices for phase A and phase B from DAC with reference current amplitude of 4A

operations is the linear one, as expected. These considerations suggest a good behaviour of the compensators.

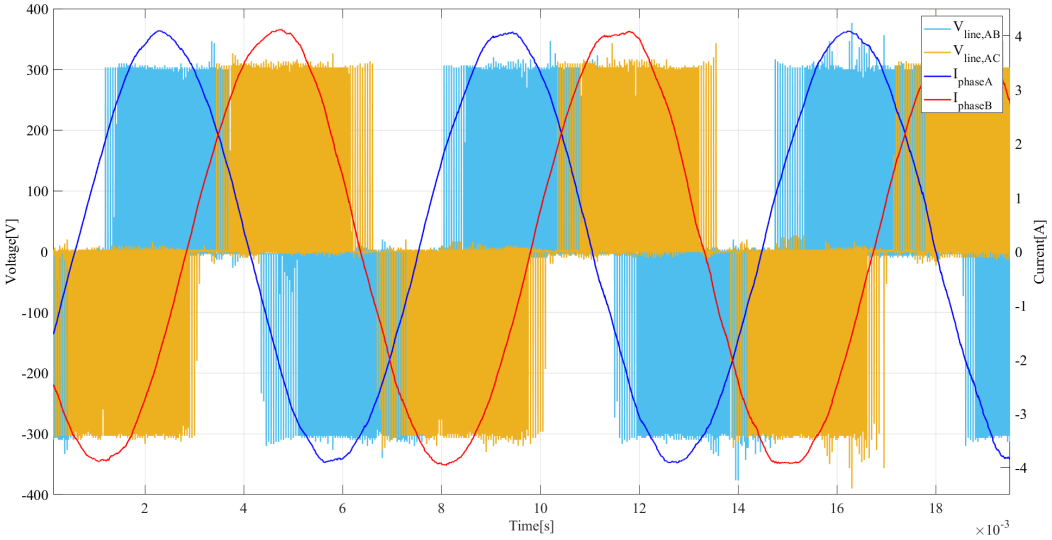
After the step variation, the motor is kept spinning until the electrical frequency reaches 145Hz, corresponding to 1740rpm, which is the maximum speed achieved before the motor stalls.

Fig. 4.19 shows the corresponding waveforms.

The test is then carried out other times to validate this value and also to be sure that keeping the electrical speed constant (below 145Hz) the motor keeps spinning at that speed without any issues. Moreover, when the motor stalls, the electrical quantities do not oscillate and increase in amplitude as in V/f, but remain the same as the current is directly controlled.



(a) Simulation results for current of phases A and B and AB,AC line-to-line voltages



(b) Test results for current of phases A and B and AB,AC line-to-line voltages

Figure 4.19: Maximum speed reached testing I/f technique on eDrive

4.4 Comparison of V/f and I/f control on PM motor

Comparing the results of the two techniques to start up the motor, the evident winner is the I/f technique for this type of motor: the maximum speed achieved without the need of mechanical position feedback is roughly three times higher with I/f. Also, when the motor stalls, I/f does a better job limiting damage risks to the motor.

The reason I/f performs better lies in the fact that it directly exploits the magnetic properties of the electric motor, providing a more stable synchronization of the rotor-stator electro-magnetial quantities, whereas V/f operates completely open loop and, as observable from the simulation, the speed reference is never truly met (both for approximation of parameters and for control schematic).

Looking at the I/f simulation results, it results that the motor could potentially spin faster than 1740rpm: this shows the test results could be further enhanced, tuning more finely the ADC conversion times and the speed of execution of the compensation blocks.

One may object that V/f allows to at least run the motor without the use of any sensors at all: this is only partly true as, besides being cheap and of small volume, they are very often employed for current monitoring and safety reasons.

Moreover, employing the I/f technique it is considerably easier to transition to the FOC control technique at higher speeds and hence also perform torque control as the current compensators involved are the same.

4.5 Simulation of FOC control on electric Drive

After the validation of the current compensation loop in the previous section and the theoretical discussion of the FOC control theory in sec. 2.10, it is possible to simulate its performances on the electric drive tested so far.

The schematic of the full system is shown in Fig. 4.20.

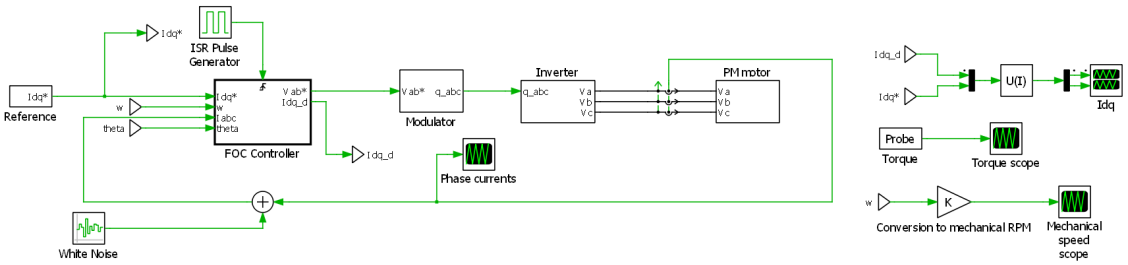


Figure 4.20: Schematic of the simulation of FOC control on electric drive

For better understanding, the schematic can be subdivided into three main blocks:

- Hardware block: containing PM motor model and inverter model;
- Modulator block: includes the SVPWM block;
- Control block: includes the reference generation and control loop.

Starting from the hardware side, this block takes the signals to the gate driver as input. There is not much to add regarding the inverter block as it contains the same inverter shown in all the simulations performed so far. The only thing worth noticing is that in this case, the inaccuracies of the current sensors are taken into account, estimating they are in the range $\pm 0.3A$

Some more discussion can be made analyzing the PM motor sub-block, shown in Fig. 4.21.

Inside it, the "permanent magnet synchronous motor" component takes care for all the electrical-to-mechanical model of the motor. FOC control is a torque control, so the speed is imposed by the mechanical system. Therefore, the mechanical speed is an input to the model: this is taken into account by the ramp-speed reference, which saturates at the base speed (equal to 14000rpm).

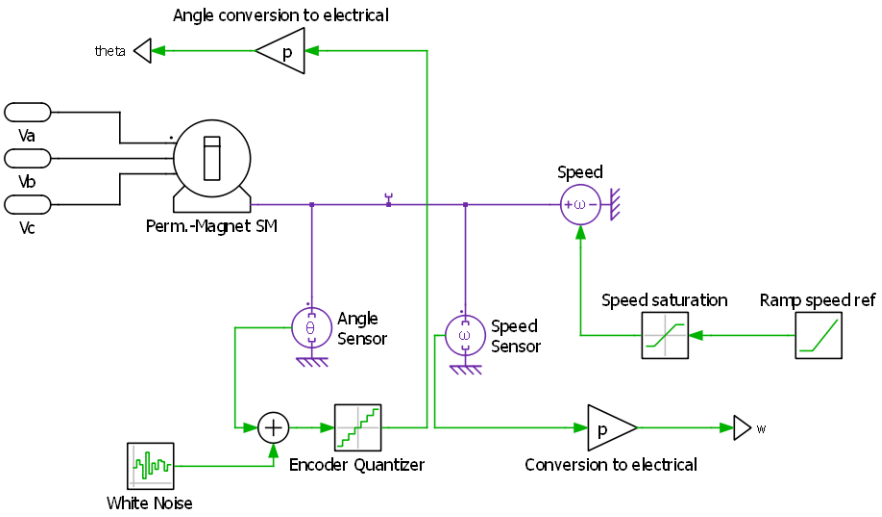


Figure 4.21: PM motor block in FOC control simulation on electric drive

In real applications, transducers measure the mechanical angular position with a limited digital resolution and introducing an offset which depends on the alignment between the transducer and the rotor: to take this into account, the quantization error is introduced with a quantization interval of $2\pi/65536$ assuming a 16bit encoder with an offset of 10 degrees (corresponding to 0.17 rad). The mechanical speed is usually estimated from the mechanical angular position: this is not taken into account in the simulation, assuming the availability of the information.

Moving forward, the modulator block is shown in Fig. 4.22.

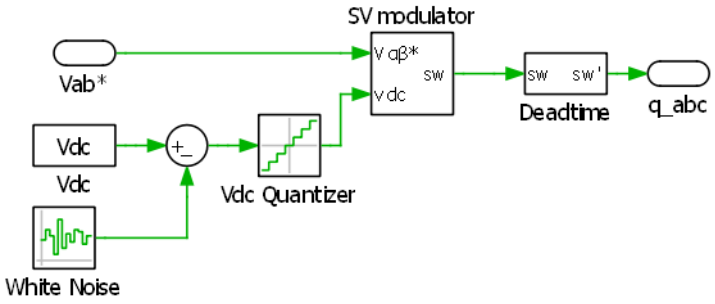


Figure 4.22: Modulator block in FOC control simulation on electric drive

This block takes into account the SVPWM technique already introduced in sec. 2.5 and extensively used in all tests and simulations, including a dead time of 500ns. It receives the reference voltage from the control block and outputs the command signals for the inverter MOSFETs. For the SVPWM to correctly work the measurement of V_{DC} is needed: this value is also affected by measurement noises, which in the case of the DC voltage sensor card presented in sec. 3.4.4 is modelled to be 10V.

Lastly, the control block is subdivided in two blocks: the first one is the reference

generator block, shown in Fig. 4.23.

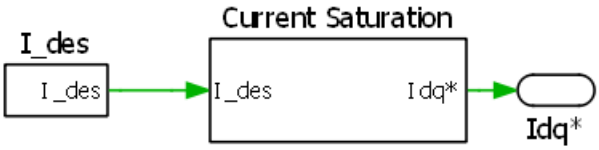


Figure 4.23: Reference block in FOC control simulation on electric drive

In the desired current sub-block, the value of i_q is derived from the desired torque, while i_d is kept at 0. For this simulation, the desired torque goes from zero to 0.97Nm (rated torque) and then a step variation to -0.97Nm is performed.

The saturation current sub-block takes into account the physical limitations of the system, implementing what discussed in sec. 2.9.

Coming to the FOC controller sub-block, the torque control is implemented by a real time microprocessor into a interrupt service routine (ISR) executed at every PWM period. To simulate the discrete time nature of the control, we implement it into a triggered subsystem executed at f_{sw}. The sub-block receives as input the reference currents from the reference sub-block, the currents measured at the inverter output, the electrical angular position from the encoder and the electrical speed derived from the encoder.

The schematic of this sub-block is shown in Fig. 4.24.

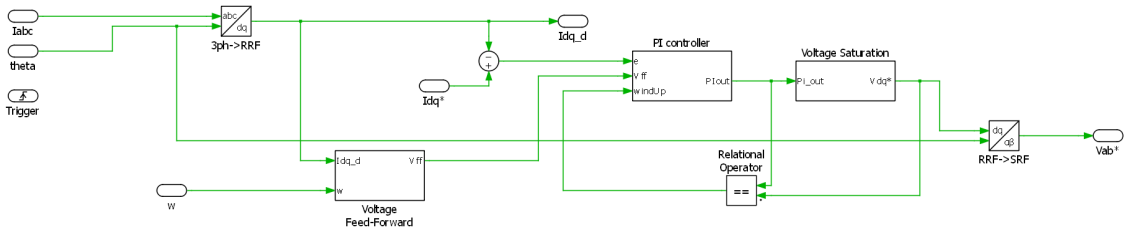


Figure 4.24: FOC controller sub-block in FOC control simulation on electric drive

First of all the current measurements in the abc frame from the sensors are converted to dq frame via Park-Clarke trasformation to be then compared with the reference values. The resulting dq axes errors are the input to the PI controller blocks, which are the exact same of the I/f control. The feed-forward terms are added to the output of the PI controller. The feed-forward sub-block is shown in Fig. 4.25.

The motional term is estimated with one of the simplest technique, which exploits Eq. 2.11 and Eq. 2.14.

The saturation block takes into account the operating limits of the inverter as presented in sec. 2.9. The anti wind-up technique is once again the simplest possible, setting to zero the integral term in case the voltage reference saturates.

The dq voltage output is converted back in the ab frame that will be input to the modulator block.

Other parameters of the simulation are:

- $V_{DC} = 600$V;

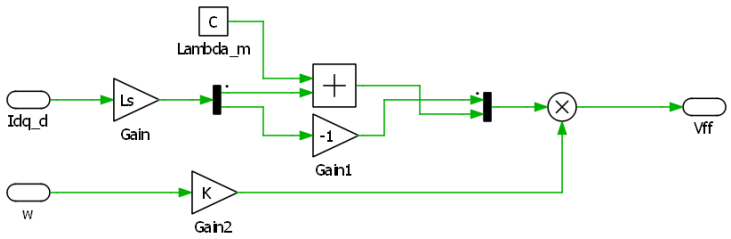


Figure 4.25: Feed-forward sub-block in FOC control simulation on electric Drive

- $f_{sw} = 20$ kHz.

Coming to the results of this simulation, the comparison between reference currents and output currents is shown in Fig. 4.26.

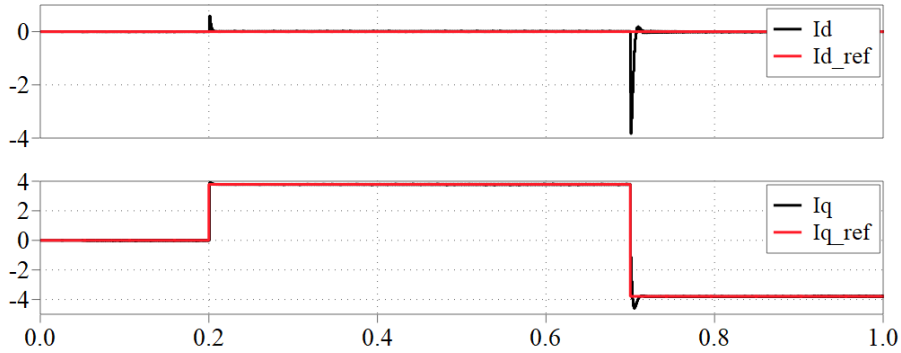


Figure 4.26: Comparison between dq current reference and output in FOC simulation on electric drive

Both the steady state tracking error and the dynamic performance can be deemed extremely satisfying.

Consequently, also the output torque matches the references, once again showing good performances. It is shwon in Fig. 4.27.

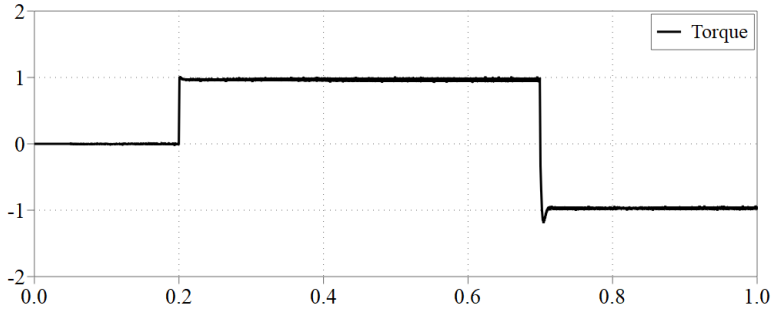
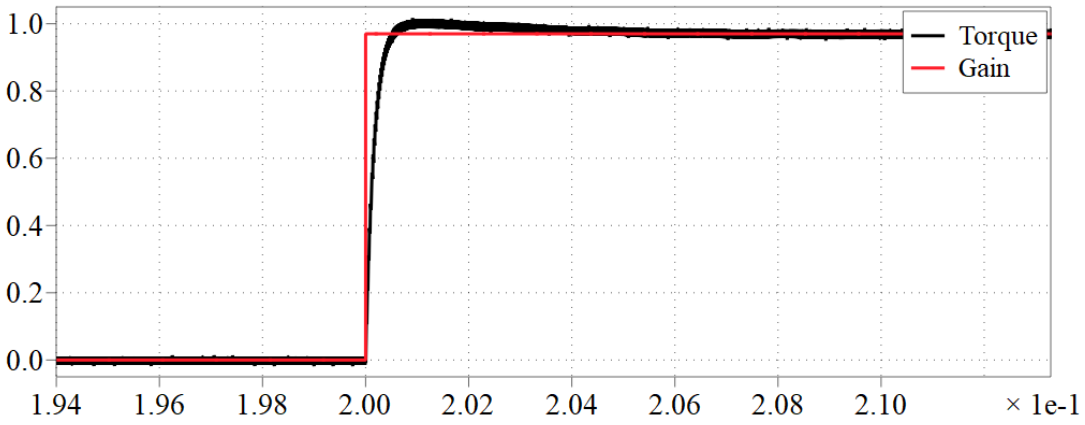


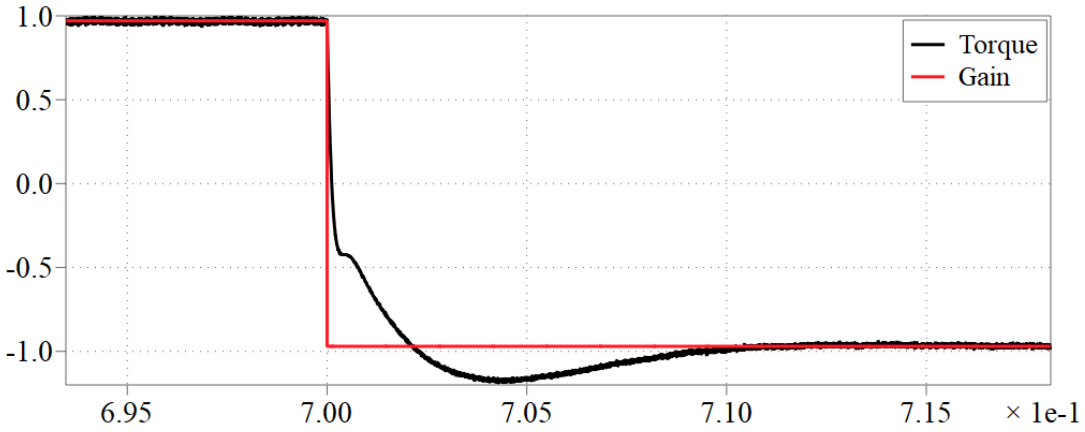
Figure 4.27: Measured torque in FOC control simulation on electric drive

A close up of the two step changes in the torque reference are shown in Fig. 4.28.

The positive increase in the torque reference is tracked in the order of milliseconds, which is definitely satisfying. The response to the negative torque step variation takes 100ms, which is worse but still acceptable. This is due to the significant reference variation, which turns the electrical machine from motor mode to generator mode, requiring a 180°variation in the output currents, which cannot happen instantaneously.



(a) Response to step increase



(b) Response to step decrease

Figure 4.28: Close up of torque step responses in FOC simulation on electric drive

Chapter 5

Conclusion

During this thesis work it has been decided to focus the attention on the development and testing of a complete electric drive based on SiC MOSFETs to control a Permanent Magnet Synchronous Motor.

Firstly, in chapter 1 and chapter 2, a theoretical background which includes the modelling of both the inverter and the motor in different reference frames is presented to better understand upon which basis the system is built.

Chapter 3 tackles the hardware testing and validation: the sub-components of the entire system are first individually tested and then assembled together. This stage is necessary to ensure the system properly works and can be used to control the motor.

Chapter 4 contains the actual start-up of the motor and the comparison between V/f and I/f techniques, showing how the latter better performs in terms of maximum speed achieved without position feedback and current regulation. This chapter also provides a simulation of a FOC control which can be added to the I/f after a certain minimum mechanical speed is reached.

The immediate next step could consist in adding the mechanical position (and hence speed) feedback to implement the full FOC control and test it with a mechanical load to verify its performances, with the opportunity to further extend it to operate in flux weakening conditions.

Moreover, as the I/f technique provides better performances and reliability, it is decided to use it in another electric drive based on GaN inverters with the same permanent magnet motor employed in this thesis work and also on the same SiC inverter based electric drive but with a custom-made permanent magnet synchronous motor with a base speed of 50000rpm.

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