POLITECNICO DI TORINO

Master degree in Electronic Engineering

Master's Thesis

3D Junctionless-FET technology: A comparative TCAD simulation study with FinFET and NSGAAFET

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Summary

The progress of semiconductor electronics devices has been marked by rapid improvement in terms of performance since the first MOSFET was invented in 1960 (1). In the last decades the down-scaling of the transistor has led to increasing performance in electronic systems while following the Moore's Law (2). However, this trend reached its limit, when the performance degradation of junction based metal-oxide-semiconductor field-effect-transistor (MOSFET) increased due to channel scaling (3). The limitations of the device related to the rising short channel effects (SCEs) are the threshold voltage (V_{TH}) roll-off, subthreshold current and drain-induced-barrier-lowering (DIBL). Moreover, process challenges concerning the fabrication of ultra steep p-n junctions restricts its functionality in the fabrication of the transistor itself.(3; 4)
The increasing demand for high integration density, high performance and low power consumption can be achieved with 3D multigate structures such as FinFET and NanoSheet GAAFET (NSGAAFET), thanks to a better control of the channel transport via fully surrounding gate (5).
Further challenges emerge during fabrication processes in the next technology nodes when decreasing the size of transistors. The junctions (p-type and n-type) will get closer, which means that the requirement of extremely high gradients in doping concentration to create the heavily doped source/drain regions becomes unfeasible (6; 7).
One of the solution to address the physical limitations of junction based MOSFET, while achieving better performance, has been proposed by designing a FET without junctions known as junctionless field-effect-transistor (JLFET) (4).
Combining the JLFET with the electrostatic gate control of multigate structures like GAA, it is possible to obtain a device with improved SCEs immunity and tunable V_{TH}, obtained by varying the channel width (4).
In this work, the electrical performance of junctionless FinFET (JL-FinFET) and NS-GAAFET (JL-NSGAAFET) are compared with the conventional FinFET and NSGAAFET.
A fabrication process simulation of the devices with highlights of different steps that could replace the current manufacturing of conventional transistors is provided.
The analysis carried out using Synopsys Sentaurus (8; 9) are developed to report electrical characteristics of each devices under exam.
Thereafter, the results have been compared to have an idea of how certain parameters affect the performance of each transistor.
Finally, there are presented some thoughts about the possible evolution of technologies and future works that may help investigating the application of junctionless devices.

Acknowledgements

I would like to express my gratitude to my parents for their unfailing support and continuous encouragement throughout my years of study. I cannot express how much I love them and how grateful I am.
Many thanks to my sister who inspired me to pursue my studies and gave me moral support.
Finally I would like to thank my supervisors, who helped throughout the master thesis.

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List of acronyms

ALD	Atomic Layer Deposition.
BOX	Buried Oxide.
CMOS	Complementary Metal-Oxide-Semiconductor.
CMP	Chemical Mechanical Polishing.
DIBL	Drain-Induced Barrier Lowering.
DRIE	Deep Reactive-Ion Etching.
EOT	Equivalent Oxide Thickness.
ESL	Etch Stop Layer.
FET	Field-Effect Transistor.
finFET	Fin Field-Effect Transistor.
GAA	Gate-All-Around.
GAAFET	Gate-All-Around Field-Effect Transistor.
JL-finFET	Junctionless Fin Field-Effect Transistor.
JL-NSGAAFET	Junctionless NSGAAFET.
JLT	Junctionless Transistor.
LKMC	Lattice Kinetic Monte Carlo.
LSTP	Low Standby Technology Power.
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor.
NS	Nanosheet.
NSGAAFET	Nanosheet Gate-All-Around Field-Effect Transistor.
NW	Nanowire.
PSG	Phosphosilicate Glass.
RIE	Reactive Ion Etching.
RMG	Replacement Metal Gate.
RTA	Rapid Thermal Annealing.
S/D	Source/Drain.
SAC	Self-Aligned Contact.
SCE	Short Channel Effect.
SIT	Sidewall Image Transfer.
SS	Subthreshold Slope.
STI	Shallow Trench Isolation.
TCAD	Technology Computer-Aided Design.
TFT	Thin Film Transistor.

Chapter 1

Introduction

Nowadays, semiconductor devices play a huge role in digital and telecommunications technology. The shrinking of transistors becomes more difficult, since more heat and power consumption indirectly enhances while trying to achieve better performance for an integrated system (13). Moreover, the scaling-down of MOSFETs boosts short channel effects (SCEs). To reduce them, 3D multigate structures such as finFETs and NSGAAFETs are developed to increase the electrostatic control of the channel.
Difficulties arise in transistors when developing ultra-sharp source and drain junctions at nanoscale due to the requirement of extremely high gradients in doping concentration (7; 13).
Junctionless transistor is a promising technology for the replacement of conventional MOSFETs. If we combined the junctionless technology with the 3D multigate, we can obtain high performance in terms of I_{ON}/I_{OFF}, while reducing SCEs.
The concept of junctionless transistor (JLT) was introduced by J.E. Lilienfeld in 1925. The characteristic of this device is the absence of any p-n junctions (14).The device is basically a resistor in which the current can be modulated by the gate (15). This technology has attracted the attention of many researchers and as a result many architectures were proposed. Combining the junction-free structure with the multi-gate structures allowed to build transistors with greater performance with respect to the conventional one, in terms of SCEs and less degradation of carrier mobility when the gate voltage is increased (10).
Trying to find a way to reduce parasitics in NSGAAFET was what motivated me in choosing this thesis subject. Therefore, since at nanoscale the major knobs of parasitics are related to random dopants, interface trap charges and line edge roughness, I decided to exploit the junctionless technology to investigate this issue (5).
Moreover, in Chapter 2 an overview of different technology regarding the MOSFET and their evolution is presented. In Chapter 3 the steps to fabricate JL-finFET and JL-NSGAAFET are proposed, while highlighting the differences and similarities with conventional transistors. In Chapter 4, the data of the simulations carried out by means of Synopsys Sentaurus TCAD (8) are reported. Finally, in Chapter 5 and in the appendix, a summary of the devices performances and the scripts employed in TCAD are provided.

Chapter 2

Junctionless Transistor

2.1 Junctionless working principle

The concept of junctionless transistor (JLT) was introduced by J.E. Lilinfield and patented in 1925 (16). However, the device was not fabricated at that time due to lack of equipment required to build this technology.
All existing transistors commercially available are based on the semiconductor junctions formed by implanting dopant atoms into the semiconductor material. Because of the laws of diffusion and the statistical nature of the distribution of the doping atoms, such junctions represent an increasingly difficult fabrication challenge for integrated circuits (ICs) industry.
In order to lower the fabrication costs while solving the problem related to the heavily and abrupt doped junctions, junctionless transistors were introduced.
The JLT works differently compared to inversion mode devices, and it is essentially a gate controlled resistor since there is no junction in the semiconductor material. The channel is fully depleted in off-state due to work function difference between gate and substrate material. To control the flow of current inside the Lilinfield device, a gate voltage is required to modulate the carriers inside the semiconductor film, thus modulating its conductivity (10). In Figure 2.1.1 is presented a schematic view of a junctionless nanowire gated resistor.

The choice of the metal work function is very important for the behaviour we want to design. Indeed, there are two possible working principles that can be used for the junctionless device:

- the first one consists in the conduction of the transistor at $V_G = 0V$ (depletion-mode), so that it can be turned-off if a gate voltage is applied, thus depleting the channel. Fig.2.1.2b shows the trans-characteristics of JLT working with this type of operating principle (17; 18; 19; 20). The thin film transistor (TFT) is similar to MOSFET built on SOI wafer with the exception that the active film is a deposited thin film, as it is shown in Fig.2.1.2a. Because the semiconductor layer is formed by deposition, the amorphous material has more defects and imperfections than in

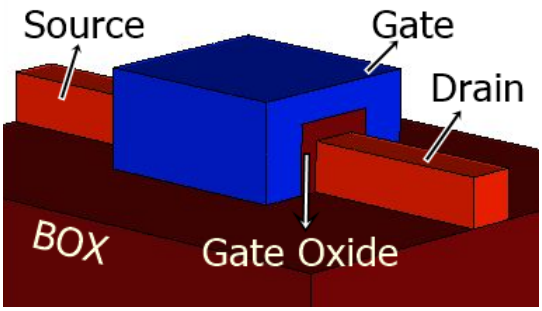
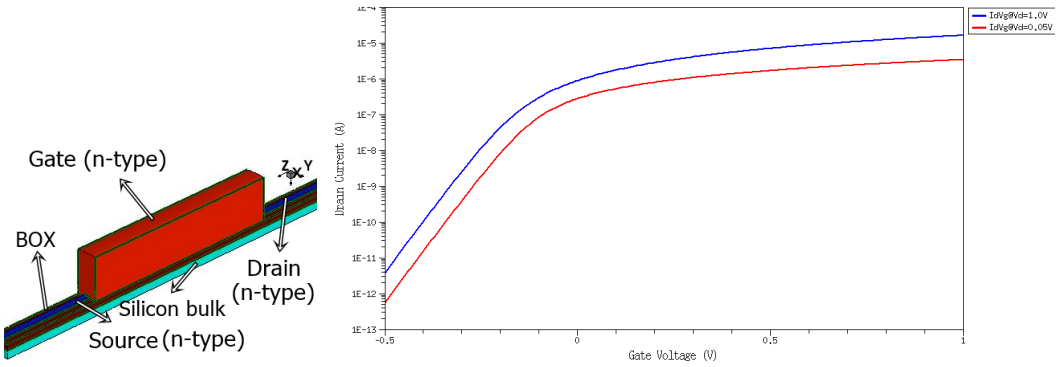


Figure 2.1.1: Schematic of an n-channel nanowire transistor. The nanowire is uniformly doped n-type and the gate material is p-type polysilicon. Opposite dopant polarities are used for p-channel devices (10).

single-crystalline semiconductors, resulting in more complicated transport mechanism for the TFT (21).

- the second operating principle of junctionless transistor consists in using work function engineering to bend the energy band diagram so that the channel region will result depleted of carriers at $V_G = 0V$ (enhancement-mode), thus obtaining the conventional behavior of CMOS devices(22; 21).
  At this point, if the semiconductor is sufficiently thin and the work function difference is large enough, then full depletion of carriers can be easily achieved, as reported in Fig.2.1.3.



(a) (b)

Figure 2.1.2: (a) Bird's eye view of n-type TFT, (b) I_D vs V_G of n-type TFT

Since the electrical behaviour in this thesis is obtained with enhancement-mode of the JLT, the focus will be on such structure. Even though the electrical behaviour of the junctionless transistors is similar to those of regular MOS transistors as it will be seen in chapter 4, there is a fundamental difference between the two devices, related to the drain

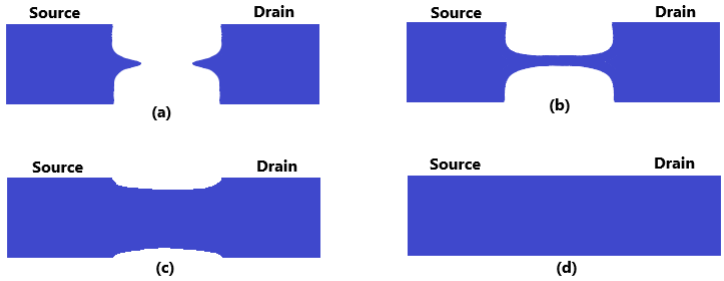


Figure 2.1.3: Electron concentration contour in an n-type junctionless nanowire for different gate-source voltage (V_{GS}). **(a)** $V_{GS} < V_{TH}$ the channel is depleted; **(b)** $V_{GS} = V_{TH}$ the channel is shaped and current starts to flow if a certain V_{DS} is applied; **(c)** $V_{GS} > V_{TH}$ the channel expands in width and thickness; **(d)** $V_{GS} = V_{FB}$ the channel has become a simple resistor (10).

current.
For what concern the conventional transistors, the drain current (I_D) in saturation region is given by:

$$I_{D,SAT} = \frac{1}{2}\mu C_{ox}\frac{W_{si}}{L_g}(V_{DD} - V_{TH})^2 \tag{2.1}$$

where μ is the carrier mobility, W_{si} is the effective width of the device, L_g the gate length, V_{DD} the supply voltage and C_{ox} the gate capacitance.
On the other hand, the junctionless transistor behaves like a resistor when flat band condition is met, hence the drain current for n-type JLT is given by:

$$I_D \approx q\mu N_D \frac{T_{si}W_{si}}{L_g}V_{DD} \tag{2.2}$$

where T_{si} is the thickness of the silicon and N_D the donor concentration (10). For the p-type, the donor concentration is swapped with the acceptor concentration N_A.
Considering the equation 2.2, the amount of current flowing depends on the doping concentration (10). Figure 2.1.4 shows the drain current as a function of gate voltage in two types of SOI MOSFETs: inversion-mode "N^+PN^+" and junctionless "$N^+N^+N^+$" transistor.

When the JLT is turned off, the distance between the non-depleted source and drain regions can be larger than the physical gate length across the entire section of the device as it shows Fig.2.1.5b (6). This feature can be controlled by the designer when choosing the parameters of the device, like the width of the spacers (L_{SP}).

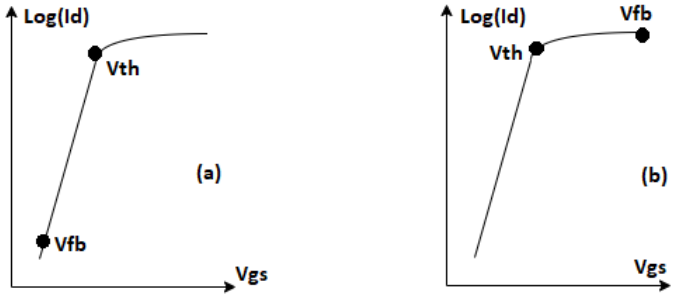


Figure 2.1.4: Drain current (log scale) as a function of gate voltage in **(a)** an inversion-mode MOSFET; **(b)** an accumulation-mode MOSFET and **c** a heavily-doped junctionless transistor (6).

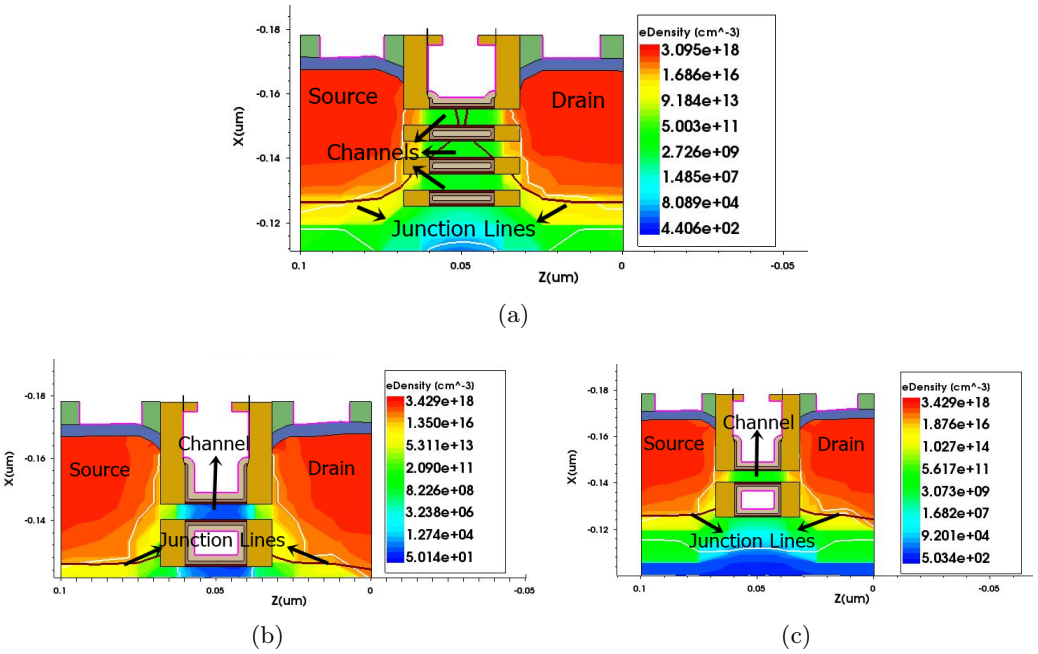


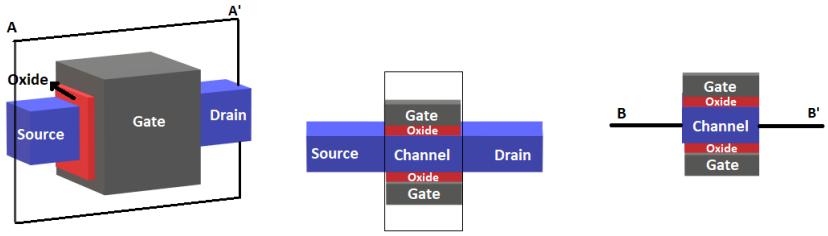
Figure 2.1.5: Electron concentration along the channel of n-type three vertical stacked NSGAAFET and JL NSGAAFET; (a) depletion of n-type NSGAAFET, (b) full depletion of n-type JL-NSGAAFET, (c) depletion of n-type JL-NSGAAFET

As it can be seen from Fig.2.1.5 when the device is switched-off, the electron concentration in junctionless devices is so low, that the short channel effects such as drain-induced barrier lowering (DIBL), subthreshold slope (SS) will be reduced. I_{OFF} is also improved, hence the overall performance I_{ON}/I_{OFF} as well (15; 10; 23; 24).
As the gate voltage is increased, the carrier concentration in the channel reaches the doping concentration N_D, in the n-type transistor. It is possible to further increase the gate voltage ($V_{GS} > V_{FB}$) to create accumulation channels, but it would be unnecessary since

the device relies on the body current(25).
Even though the bulk mobility is lower than the surface one (26; 27; 6), the carriers are subjected to a reduced electric field in the direction perpendicular to their flow and they are much less influenced by surface roughness scattering compared to inversion-mode transistors (23; 10; 25).
The JLT requires high doping concentrations for the source-channel-drain structure of the order of 10^{19} atoms cm^{-3}. Such high doping is usually reserved to only source-drain in conventional inversion-mode transistors but in junctionless devices it is needed to ensure a high current drive and good contact resistance. Moreover, due to the high level doping, the geometry must be small enough to allow for the full depletion of the channel region, which is necessary to turn-off the device (10).

2.2 Energy band diagram

The operating principle of the device can be understood from its energy band diagram. These diagrams help to explain the operation of many kinds of semiconductor devices and to visualize how bands change with position (band bending).
Using multigate structures like gate-all-around, the electrostatic gate control is improved. However, to better study the energy band bending behaviour, we consider the cross section of the device, then focus the attention on the channel region.



(a) (b) (c)

Figure 2.2.1: (a) Bird's eye view of gate-all-around (GAA) FET, (b) Cross section along plane AA' of the GAAFET, (c) Channel region cut.

The band diagram of a junctionless device is reported in Fig.2.2.3, and it is obtained by rotating of 90° the structure in Fig.2.2.1c along the BB' axis.
It can be observed that the band diagram of JLT is the same of the conventional MOSFET. What it changes between the two technologies is the doping of the source and drain contacts.
Conventional MOSFETs rely on the inversion of charges in the channel region to create the path where current flows, while the junctionless transistors exploit charges in the channel to provide current.
The JLT metal workfunction is 4.1 eV and 5.0 eV for p-type and n-type respectively.
The quantities reported in the following band diagrams are: E_F (Fermi energy), E_{Fm} (Fermi energy of the metal), $q\phi_M$ (metal workfunction), E_0 (vacuum level), χ_{Si} (electron affinity of silicon), χ_{SiO_2} (electron affinity of silicon dioxide), E_G (band-gap energy), E_{FI} (intrinsic Fermi energy), E_{Fn} (Fermi energy of n-type silicon), E_{Fp} (Fermi energy of p-type silicon), E_V (valence energy) and E_C (conduction energy).
First, to have a general understanding of what is going to happen, the energy band diagram of the isolated material is represented at thermal equilibrium.

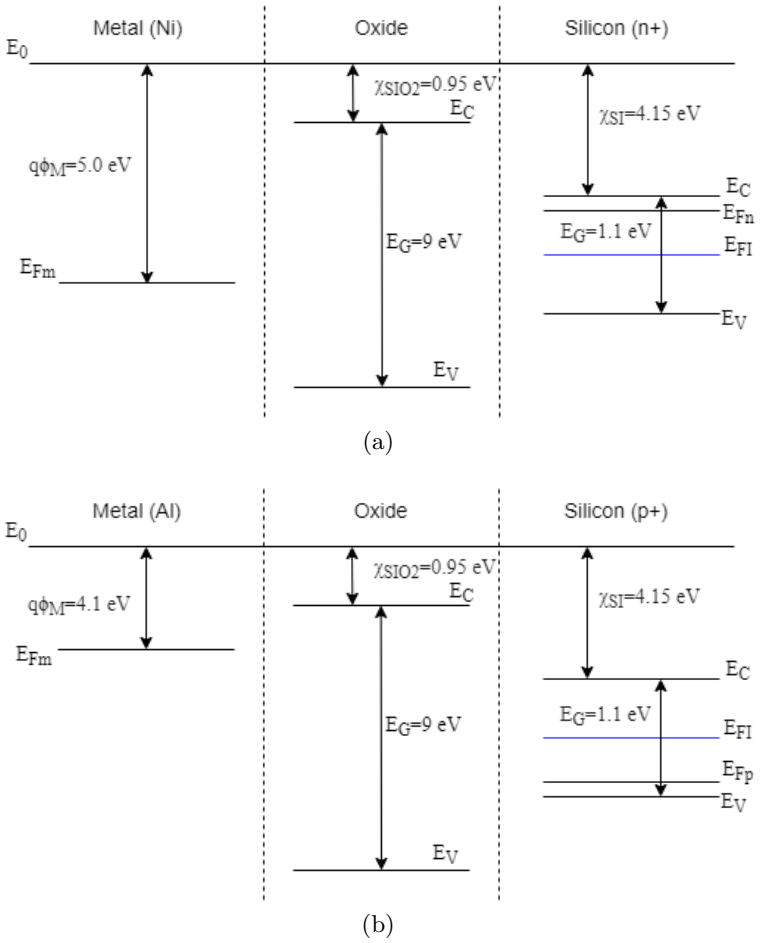


Figure 2.2.2: Energy band diagrams of isolated materials (a) n-type JLT, (b) p-type JLT.

At equilibrium, when contact is formed, a depletion region is formed in the channel region, due to the thin channel and the workfunction difference between the gate and the channel. The region may be fully depleted or partially depleted, depending on the device parameters.
As positive voltage is applied at the gate electrode, the band bending declines and depletion width tends to decrease. Therefore, current starts to flow through the bulk of the channel. If the voltage is further increased, the flat band condition is reached, and a completely neutral channel is created. Flat band is the condition where the energy band (E_C and E_V) of the substrate is flat at the Si-SiO_2 interface (28). When applied voltage crosses flat band voltage V_{FB}, charges accumulate in the surface of the channel, then current is governed by accumulation charges at the outer region of the channel (10; 29). As a result, the channel conduction for JLT goes from depletion to accumulation, which is different from the conventional MOSFETs, where the conduction progress from depletion to inversion.

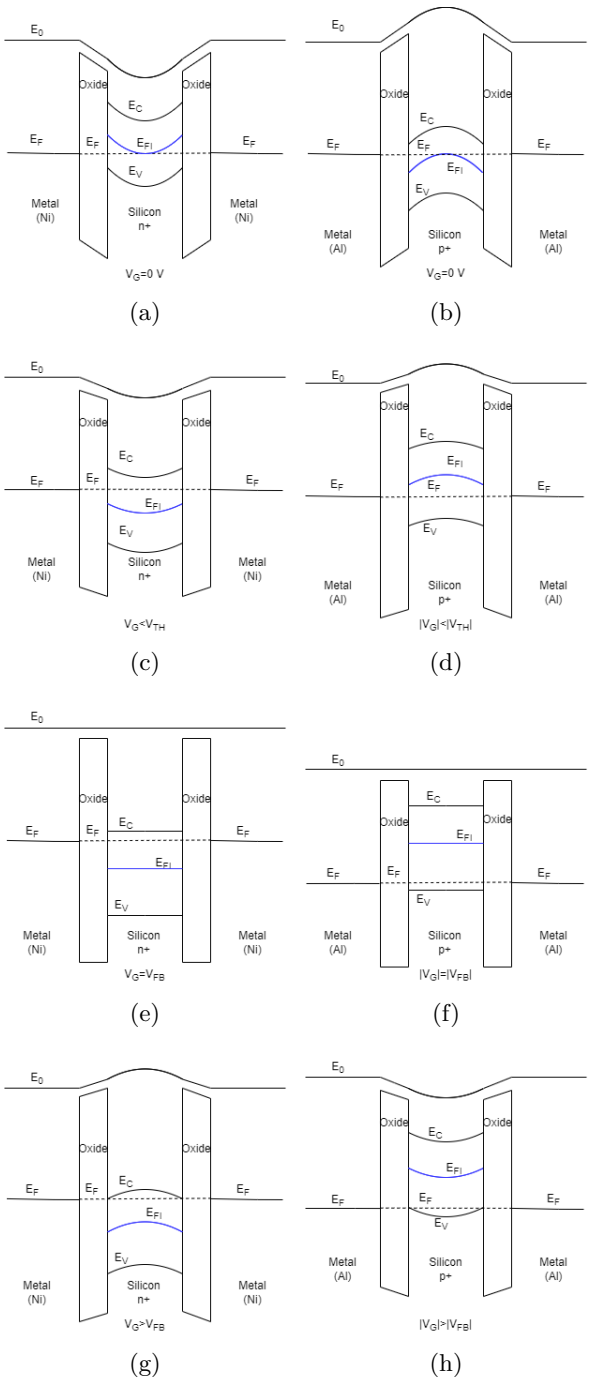


Figure 2.2.3: Energy band diagrams for n-type (left side) and p-type (right side) JLT under different bias, for the conditions of: a-b) full-depletion (OFF state), c-d) partial depletion, e-f) flat-band (ON state) and g-h) accumulation.

The energy band diagram along drain-channel-source of the junctionless devices are identical to those of a regular MOSFET. Figure 2.2.4 shows the band diagram of both type JLT, extracted by Sentaurus, for three ranges of voltage sweeps: V_{GS}=0 V and V_{DS}=0 V, V_{GS}=0 V and V_{DS}=V_{DD}, V_{GS}=V_{DD} and V_{DS}=V_{DD}. The supply voltage (V_{DD}) for the n-type and p-type transistors are 0.75 V and -0.75 V respectively (30).

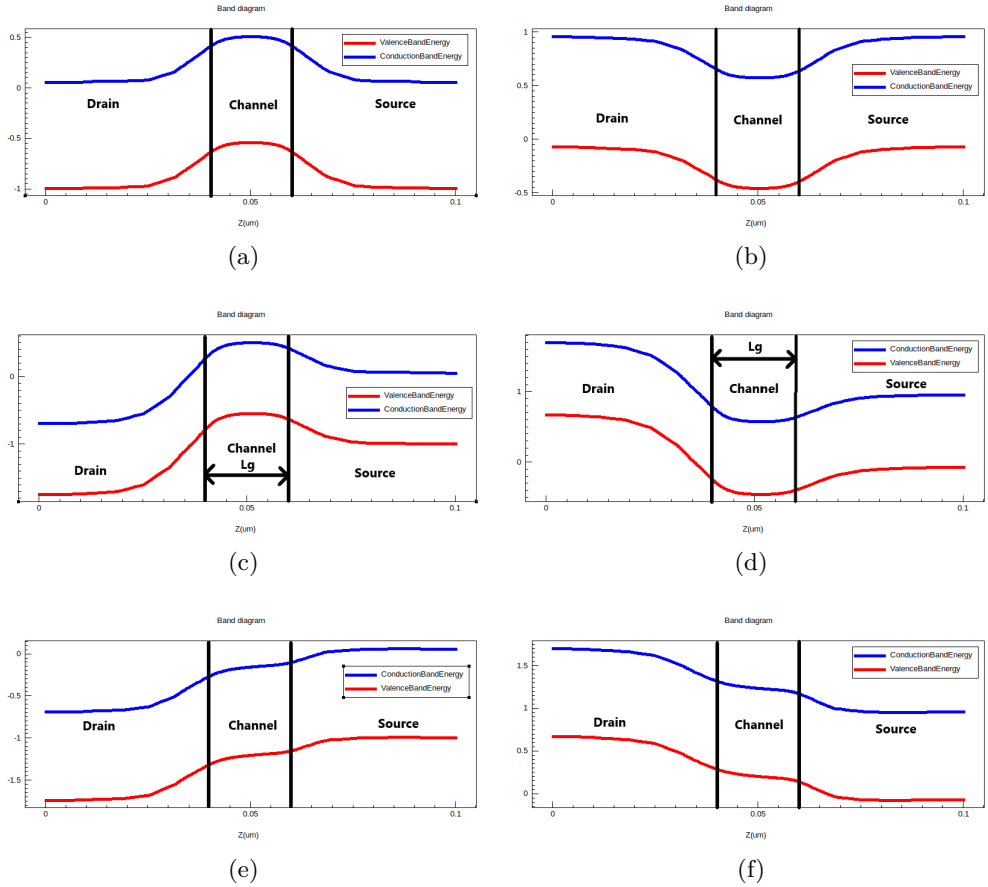


Figure 2.2.4: Energy band diagrams from drain to source when V_{GS}=0 V and V_{DS}=0 V of (a) n-type JLT and (b) p-type JLT. Energy band diagrams from drain to source when V_{GS}=0 V and V_{DS}=V_{DD} of (c) n-type JLT and (d) p-type JLT. Energy band diagrams from drain to source when V_{GS}=V_{DD} and V_{DS}=V_{DD} of (e) n-type JLT and (f) p-type JLT.

2.3 Junctionless: State-Of-The-Art

JLTs can be classified based on the geometrical shape, material composition of the channel and gate structure. When a single gate is exploited to control the current that flows through the channel, the device is called Single Gate or Planar junctionless transistor (31; 32; 11). If the channel is thin (≤10 nm) and made with polysilicon material, this is known as Thin Film transistor (17; 33; 18; 19).
As device dimension shrinks towards the nanoscale, the gate is less effective in controlling the carriers in the channel. The multi-gate field-effect transistor (MuGFET) improve the electrostatic control of the channel while suppressing the SCEs.
If the channel is sandwiched between two controlled gate structures, the structure built is the Double Gate junctionless transistor (18; 4). More advanced junctionless transistors can be built by merging the well-known multigate technologies such as FinFET, Nanosheet GAAFET and Nanowire GAAFET (10; 33; 19; 34; 20; 35; 36; 37; 38; 39). The analysis presented in the papers (34; 35; 36; 38; 39) compares different techniques like using stress-silicon and gate work function engineering while focusing on the main figures of merit (DIBL, SS, I_{ON}/I_{OFF}) to evaluate the performance of the respective JLT. Shallow trench isolation (STI) (23) and silicon-on-insulator (SOI) technology are also deployed to further reduce parasitic effects (6; 24).

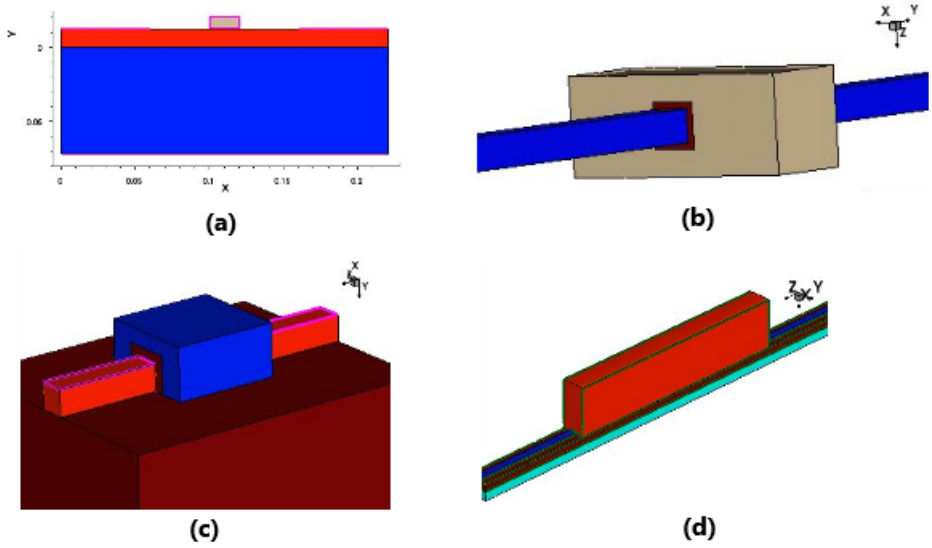


Figure 2.3.1: Bird's eye view of various type of junctionless devices: (a) Bulk planar junctionless transistor (11), (b) Gate-all-around nanowire (12), (c) nanowire transistor on SOI (10), (d) Thin Film transistor

Chapter 3

Fabrication process simulations

The junctionless transistor was initially demonstrated on a silicon-on-insulator (SOI) substrate because the thickness of the channel can be easily scaled down. Moreover, the fin formation process sequence using SOI makes the fabrication trivial and allows to get a rectangular fin profile (40). Nevertheless, the fabrication cost increases (41), and the implementation leads to non-compatibility with standard CMOS technology, which is typically built on a bulk substrate (42). Therefore, in this thesis the junctionless finFET is built on a substrate with the shallow trench isolation (STI) to isolate various devices fabricated on the wafer (43). The additional design parameter, i.e., substrate doping concentration, could be used to tune the device performance and since the channel-substrate junction produces an additional depletion region, the effective channel thickness is reduced, thus improving the electrostatic control of the gate (44).
The bulk finFET fabrication process discussed in this thesis follows the steps for conventional finFET manufacturing technology (43), while highlighting the differences between junction based finFETs and junctionless finFETs. To emulate what happens during the fabrication of the transistor, Sentaurus TCAD is employed (8).
In section 3.1, the manufacturing process steps are presented for the n-type and p-type junction based finFET, while it is suggested a new way to fabricate junctionless finFETs in 3.2 to adapt it to the current fabrication technology. This way to fabricate the junctionless finFETs and integrate it in the standard manufacturing technology is new, since in the current papers these finFET structures are SOI-based (45). Moreover, because this type of transistors is still relatively new, most papers related to fabrication build the junctionless transistors with polysilicon using solid-phase recrystallized (SPC) (46) process on amorphous-Si. The electrical performance of polysilicon made through SPC is strongly influenced by the lattice of the structure. The defects in the grain boundaries reduce the carrier mobility, which cause the decrease of I_{ON} due to scattering sites in the channel.
In literature (47), to test the behaviour of the junctionless technology, the channel has been fabricated through electron-beam (e-beam) lithography. In e-beam lithography an electron beam is guided in a scanning mode to the substrate and at the same time the

beam is rapidly switched on and off. As consequence, electron beam writing is a slow process but with high accuracy, which is not suited for the high volume productions in microelectronics, where the throughput is a key factor (48).
In another paper (42), it is reported how to build a junctionless vertically stacked silicon nanowire gate-all-around using the deep reactive ion etching (also called Bosch process). The trigate device structure simulated in this section has the following specifications:

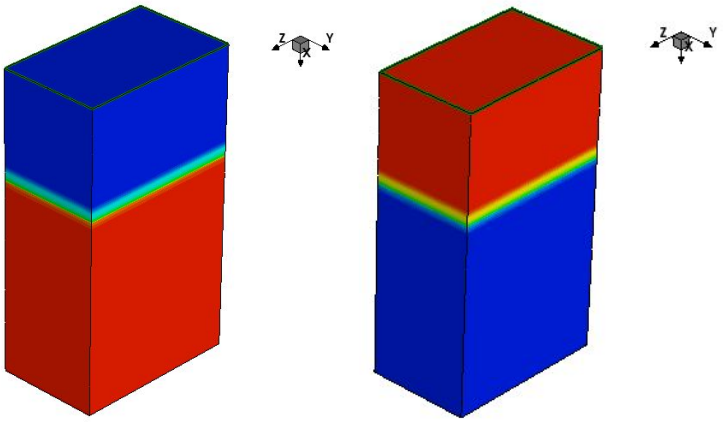
Parameters	Parameter Value	unit
Fin Height, H_{FIN}	40	nm
Fin width, W_{FIN}	18	nm
STI thickness	22	nm
Spacer length, L_{SP}	8	nm
Gate length	20	nm
S/D Doping, N_{SD}	$6 - 8 \times 10^{18}$	cm^{-3}
Channel Doping, N_{CH}	$9 \times 10^{16} - 1 \times 10^{17}$	cm^{-3}
Gate oxide (SiO_2)	0.7	nm
High-k dielectric (HfO_2)	1	nm
Metal Gate Stack (p-type finFET)		
TiN	1.5	nm
TaN	2.0	nm
TiN	5.0	nm
TiAl	5.0	nm
Metal Gate Stack (n-type finFET)		
TiN	1.5	nm
TaN	2.0	nm
TiAl	5.0	nm

Table 3.0.1: FinFET device parameters used in the simulation.

Notice that the concentration of source/drain and channel may be subjected to variation, since the simulation will emulate the implantation and diffusion of dopants when activated by rapid thermal annealing (RTA). Therefore, obtaining a constant concentration within source/drain/channel is unfeasible. Moreover, the increase in diffusivity arises from the large excess of point defects that result from the ion implantation process, hence RTA limit the transient-enhanced diffusion (49).

3.1 Bulk finFET

The starting material for the fabrication of finFET is a silicon substrate lightly doped with Boron and Phosphorus concentration of 10^{15} cm^{-3} for n-type and p-type finFET respectively. To have a better knowledge and accuracy of dopant concentration, a silicon epitaxial layer is grown on the wafer, with thickness determined by the target H_{fin} of finFET device technology.
A boron (phosphorus) implantation is performed to create the p-well (n-well) region for the n-type (p-type) transistor. Afterwards the wafer is annealed using the rapid thermal annealing (RTA) process to activate the implanted dopants (Fig.3.1.1).



(a) (b)

Figure 3.1.1: Bird's eye view of silicon epitaxial growth; a) n-type finFET, b) p-type finFET.

After the well formation, the thin silicon fin is formed using sidewall image transfer process (50). It is to be noted that the dimensions of such ultrathin vertical structures are beyond the resolution of available photolithography. Moreover, it is challenging to pattern such high aspect ratio (H_{fin}/W_{fin}) in high volume production.
The major processing step in patterning multiple fins is using self-aligned double patterning (SADP), which employ layers of different materials. The stack is composed by an oxide layer, a thick layer of silicon nitride and amorphous silicon (mandrel layer), using chemical vapor deposition (CVD). After the deposition, the photoresist is patterned on the wafer and by using a mask combined with the anisotropic etching, the location where the fins will be created is defined. Next the mandrel patterning, a thin layer of SiO_2 is deposited on the wafer, then a highly anisotropic etch process that is selective to oxide is used to form thin oxide spacer on the sidewalls of the amorphous silicon layer. After the oxide spacers formation, the mandrel strips are etched; then using the oxide spacers as mask, the underlying Si_3N_4 layer is removed by a highly anisotropic etching process using the SiO_2 as etch stop layer. The oxide spacers and nitride mask are used as patterns in

an anisotropic etch that goes through the silicon into the well region forming silicon fin (Fig.3.1.2).

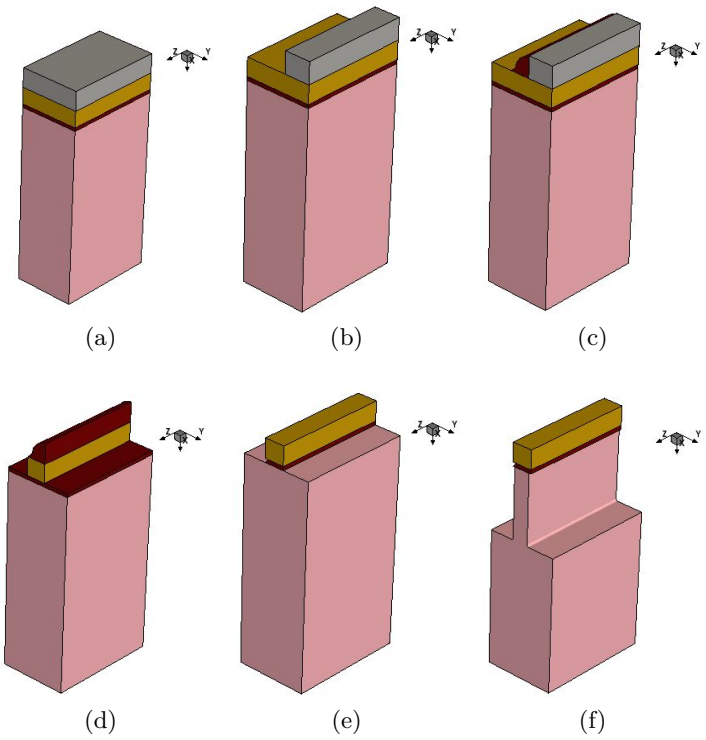


Figure 3.1.2: Bird's eye view of SIT process steps.

A thick layer of tetraethyl orthosilicate (TEOS) oxide is deposited using the CVD process. Then, the wafer is polished using chemical-mechanical planarization (CMP) process using Si_3N_4 layer as the CMP stopper. After the planarization of the surface, the residual Si_3N_4 layer is removed exposing the fin capped with oxide. The TEOS oxide is then etched back using selective etching to remove all the oxide surrounding the fins and expose it. This is a critical process since the electrical parameters of finFET depends on the aspect ratio of the fin (Fig.3.1.3). The fin is rounded to have structure more similar to what it is obtained in the reality during fabrication.

To limit punch through leakage in the off-state current of finFETs, a punch through stop layer (PTSL) is formed; a layer beneath the channel with relatively high impurity concentration obtained by ion implantation. In conventional process flow, the PTSL is made after fin formation (51).
For the gate definition, the fin is coated with oxide, then a dummy gate made of polysilicon is transferred through photolithography. The patterned gate will define the channel length of the transistor (Fig.3.1.4).

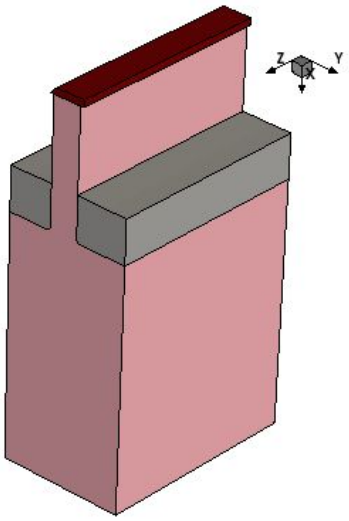


Figure 3.1.3: TEOS formation and fin aspect ratio definition.

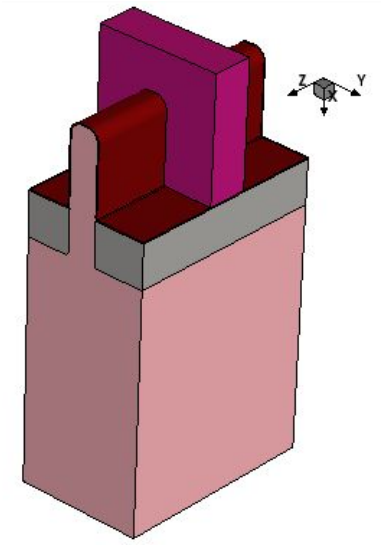


Figure 3.1.4: Dummy gate.

Afterwards, a photoresist is patterned to cover the gate and a dual Phosphorus (Boron) implantation is performed with a tilt angle of +10 degrees and -10 degrees for the n-type (p-type) transistor. The tilt is to ensure adequate coverage of tall fins. Nevertheless, a higher degree of tilt would be needed to obtain a higher electrical conformal doping (52; 53), but this would lead to shadow the nearby finFETs. The role of source/drain

extension is to reduce the maximum electric field near the drain, so that the hot carrier injection phenomenon can be mitigated. An RTA is performed to activate dopants, however the lateral diffusion taking place under the polysilicon will eventually affect the effective channel length of the transistor, thus changing some electrical parameters from the desired ones. A thin oxide layer is grown to cover the walls of the dummy gate. To form the spacers, a thick layer of Si3N4 is deposited on the wafer. Then a highly anisotropic etching process leaves the nitride residue on the sidewalls of the gate electrode and fins, which will prevent further implantation to penetrate the fin (Fig.3.1.5).

After the Si_3N_4 spacer-etch process, a layer of SiCN hard mask is deposited to protect

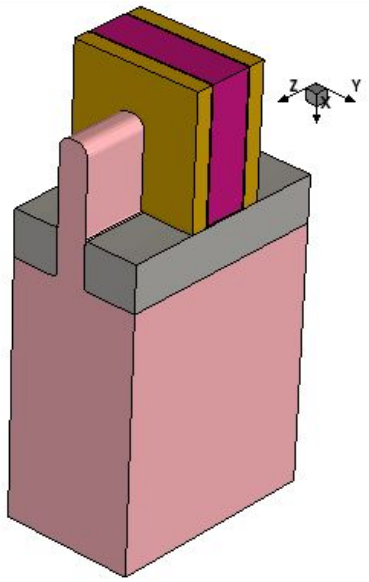
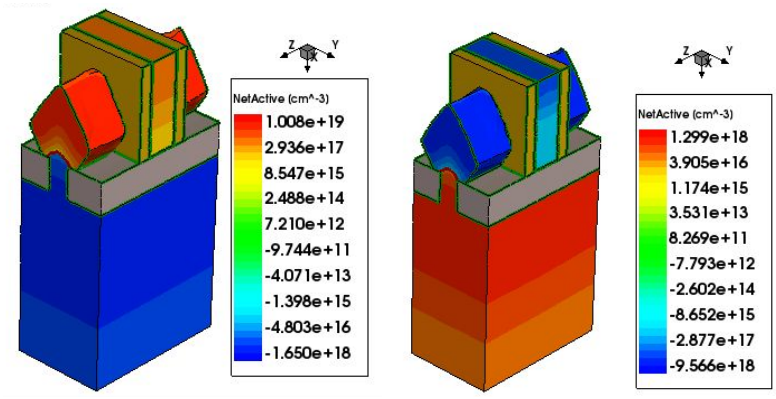


Figure 3.1.5: Spacer formation.

the dummy gate. The fin left uncovered by the mask are etched to promote the SiC (SiGe) epitaxial growth on the exposed silicon surface of the n-type (p-type) finFET. This procedure is developed to improve the mobility of carriers by exploiting strained silicon technology. The carbon (germanium) atom added with silicon modifies the lattice spacing inside the semiconductor, which translates into a tensile (compressive) stress on the channel, therefore, mobility increases (Fig.3.1.6).

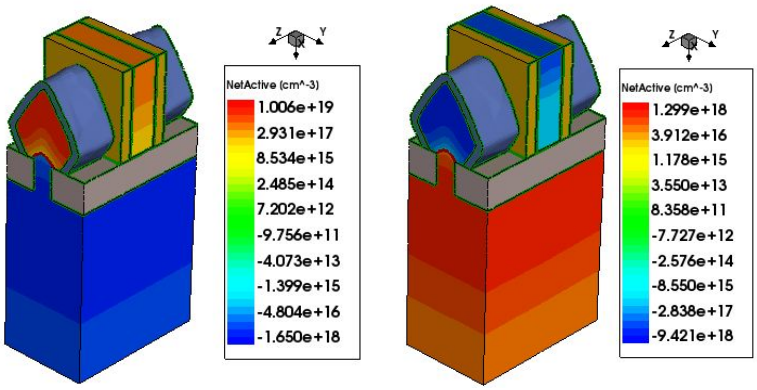
To further increase performance of the transistor, a silicidation with titanium is performed. This implant reduces the source-drain contact resistance. Next, the wafer is rapidly heated to form titanium silicide, then unreacted Ti located on the surface is etched away (Fig.3.1.7).

A thick layer of phosphorus doped glass, known as phosphosilicate glass (PSG) is deposited over the wafer then its surface is smoothed by CMP using the polysilicon gate as etch stop layer (Fig.3.1.8). After CMP, the top of the gate electrode is exposed, and the dummy gate is removed by selective etching.



(a) (b)

Figure 3.1.6: Source/Drain epitaxial growth with strained technology; a) n-type finFET with SiC for tensile stress, b) p-type finFET with SiGe for compressive stress.



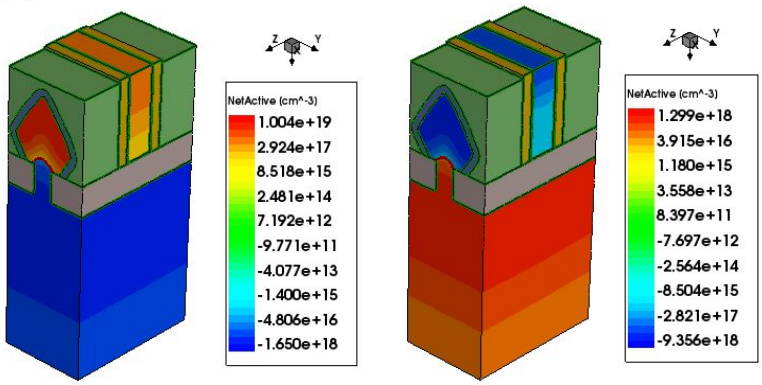
(a) (b)

Figure 3.1.7: Silicidation; a) n-type finFET, b) p-type finFET.

The gate dielectric consists of an ultrathin SiO_2 interfacial layer thermally grown and hafnium dioxide (HfO_2) high-k dielectric deposited using atomic layer deposition (ALD) (54). The equivalent oxide thickness (EOT) obtained is a length, given in nanometers, which indicates how thick a silicon oxide film would need to be to produce the same capacitance as the high-k material (HfO_2) being used (55).

$$EOT = t_{SiO_2} + t_{HfO_2}\frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}} = EOT_{SiO_2} + EOT_{HfO_2} \tag{3.1}$$

The dielectric stack is needed to increase the overall oxide capacitance while reducing the transparency coefficient, which is responsible for the gate tunnelling current.
Until now the fabrication process steps for n-type and p-type transistors were the same, despite having opposite doping. Since a metal gate is required to reduce the contact



(a) (b)

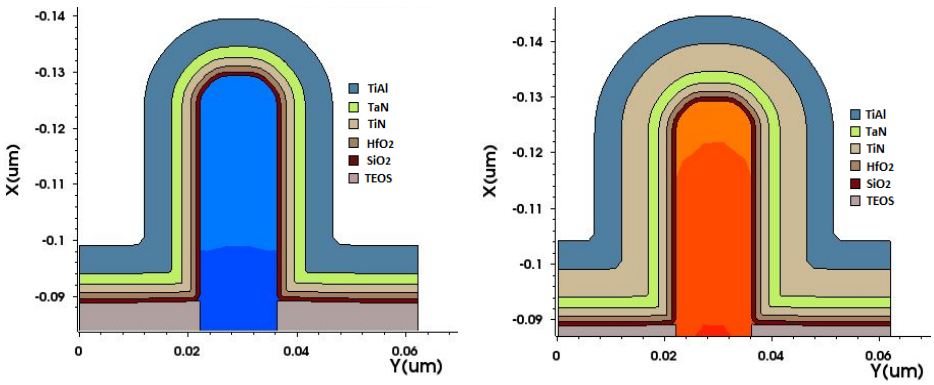
Figure 3.1.8: PSG; a) n-type finFET, b) p-type finFET.

resistance and poly-depletion effect, p-finFETs and n-finFETs need different metal work function to set the desired threshold voltage, thus improving the electrostatic control over the channel. Therefore, during the metal gate stack performed with ALD, there will be some differences between the two structures. However, to emulate what really happens during the fabrication, the steps employed in the 3D construction of the finFET will take into account this matter.

The first layer to be deposited on the whole wafer is TiN (15 Å), subsequently a thin layer of TaN (20 Å) is formed. Next, a thick layer of TiN (50 Å) covering both transistors is patterned. Photoresist is patterned to cover only the p-finFET region, so that the exposed TiN on the n-finFET region is etched away using TaN as an etch stop layer. Afterwards, the photoresist is stripped and a TiAl (50 Å) deposition is done. An annealing step is required to cause the Al in the TiAl to diffuse through the TaN barrier and creating the TiAlN (titanium aluminum nitride) for the n-finFET workfunction metal, on top of the high-k dielectric (56; 57; 55) . However, the thick layer of TiN (50 Å) over the p-type transistor region blocks the diffusion of aluminum into TiN, so that the p-finFET work-function metal is unaltered (TiN).

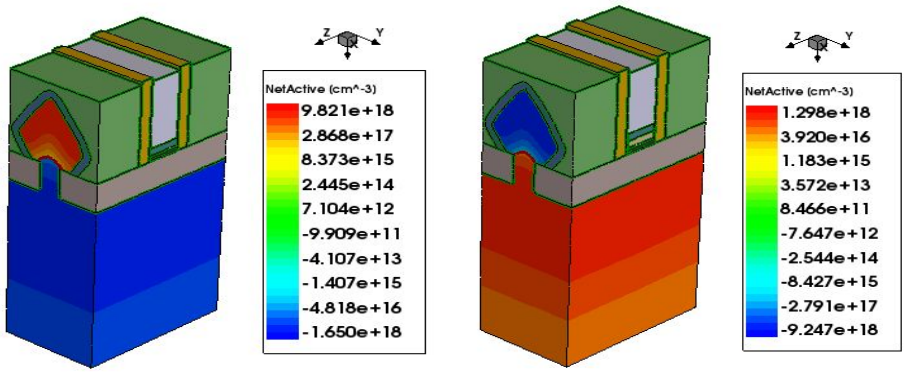
To fill cavities, a thick layer of tungsten (W) is deposited using CVD process and a CMP is done to polish the surface, thus make it coplanar with the top of the gate electrode (Fig.3.1.10).

After W deposition and planarization, self-aligned contacts (SAC) are formed for inter-connection purposes of the transistor to prevent short-circuits between gate and source/drain. This procedure consists in isolating the top gate electrode with Si_3N_4, so that if any mis-alignment occurs during the contact formation made with tungsten, no problems arise.



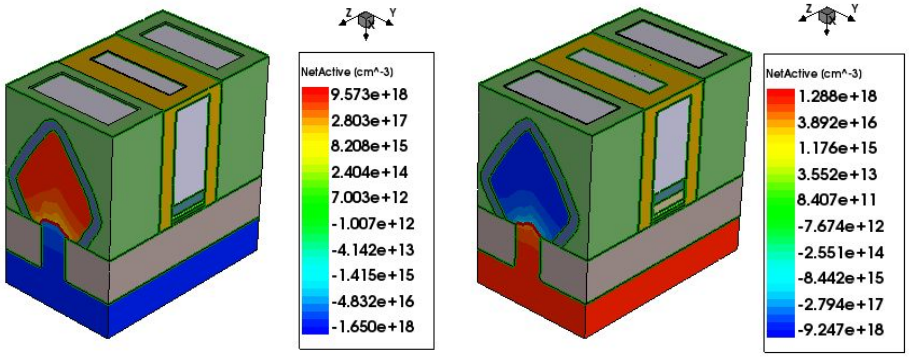
(a) (b)

Figure 3.1.9: Gate stack; a) n-type finFET, b) p-type finFET.



(a) (b)

Figure 3.1.10: Tungsten filling; a) n-type finFET, b) p-type finFET.



(a) (b)

Figure 3.1.11: Self-aligned contacts; a) n-type finFET, b) p-type finFET.

3.2 Bulk JL-finFET

The fabrication steps employed for JL-finFETs are based on existing process flows of conventional finFET (43), so the following pictures show the suggested sequence to build the JL-finFET.
To remind the geometries employed during the fabrication process steps of conventional finFET and report the doping used for the junctionless structure, the data are reported in the following table.

Parameters	Parameter Value	unit
Fin Height, H_{FIN}	40	nm
Fin width, W_{FIN}	18	nm
STI thickness	22	nm
Spacer length, L_{SP}	8	nm
Gate length	20	nm
Source/Channel/Drain Doping, N_{SD}	$6 - 8 \times 10^{18}$	cm^{-3}
Gate oxide (SiO_2)	0.7	nm
High-k dielectric (HfO_2)	1	nm
Metal Gate Stack (n-type finFET)		
TiN	1.5	nm
TaN	2.0	nm
TiN	5.0	nm
TiAl	5.0	nm
Metal Gate Stack (p-type finFET)		
TiN	1.5	nm
TaN	2.0	nm
TiAl	5.0	nm

Table 3.2.1: JL-finFET device parameters used in the simulation.

First, the well-implantation is done in the bulk silicon to block the unwanted leakage current that can flow along the silicon substrate. Fin formation is done using sidewall image transfer including trench etching into the bulk, and then oxide gap fill to create the shallow trench isolation (STI). The exposed fin is doped with phosphorus (boron) to build a n-type (p-type) transistor. The dummy gate is patterned to build the spacers but it is not related to the formation of the source/drain extension employed in conventional CMOS technology (Fig.3.2.1).

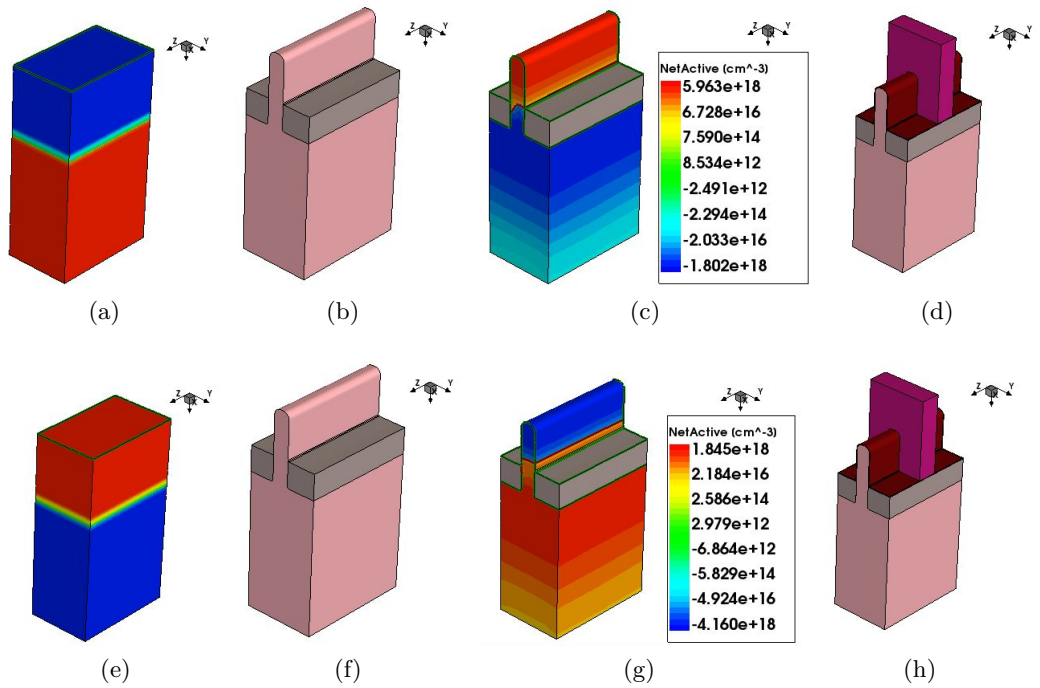


Figure 3.2.1: Bird's eye view of a) well implantation, b) SIT, c) channel doping, and d) dummy gate process flow of n-type JL-finFET. e) well, f) SIT, g) channel doping and h) dummy gate process flow of p-type JL-finFET

In JL-finFET, the spacers prevent short circuits between gate and S/D regions. Moreover, the electric field that fringes through the spacer to the device layer on both sides of the gate results in an effective increase in electrical gate length in the off-state (Fig.3.2.2). Therefore, the I_{OFF}, and SS are improved, because the channel layer gets depleted beyond the nominal channel length, when the transistor is switched off (58; 59; 60; 61; 62). Furthermore, the spacers mitigate the gate-induced drain leakage (GIDL), which is identified by the increase of drain current when a negative (positive) gate voltage is applied to the gate of an n-channel (p-channel) device (63). The GIDL is caused by band-to-band tunnelling (BTBT) in the gate and drain overlap region (GIDL is larger in inversion mode MOS because of the junction abruptness (64)).

In order to enhance carrier mobility, strained channel technology is introduced into JL-finFET (Fig.3.2.3). The application of strain engineering has improved the I_{ON}, I_{ON}/I_{OFF} and transconductance (65).

To enhance the drive current of the JL-finFET (Fig.3.2.4), titanium silicide is employed to lower the sheet resistance of source/drain contact (66).

The PSG is deposited to isolate the source/drain contacts then CMP is used to planarize the wafer surface.

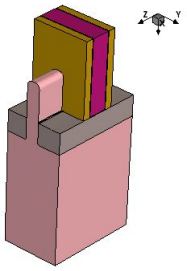
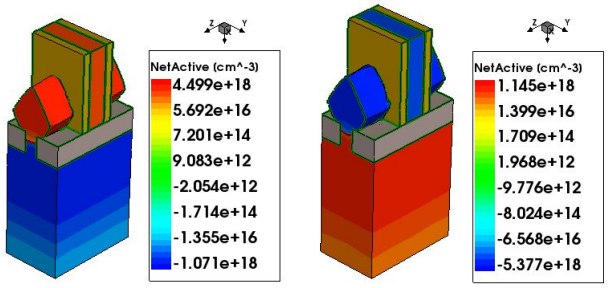
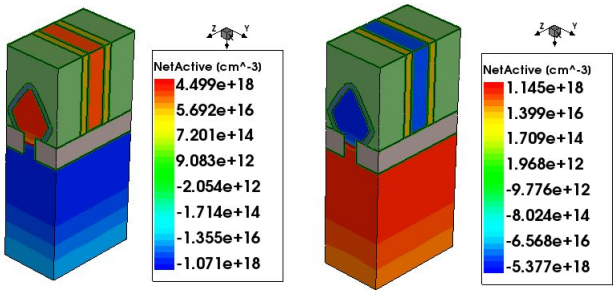


Figure 3.2.2: Spacer formation.



(a) (b)

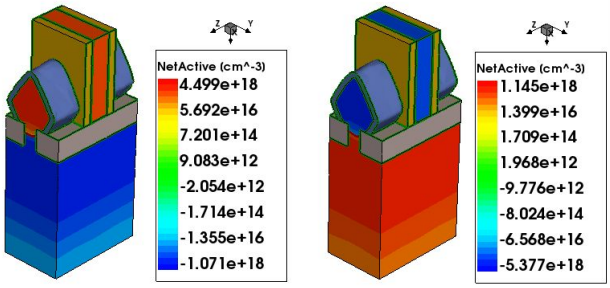
Figure 3.2.3: Source/Drain epitaxial growth with strained technology; a) n-type JL-finFET with SiC for tensile stress, b) p-type JL-finFET with SiGe for compressive stress.



(a) (b)

Figure 3.2.5: PSG; a) n-type JL-finFET, b) p-type JL-finFET.

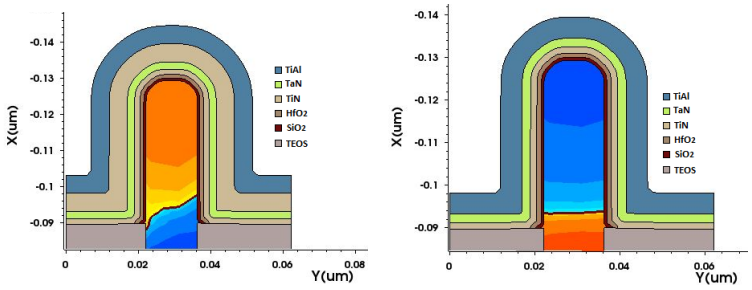
The dummy gate previously deposited to build the spacers is etched to create the gate stack. The gate dielectric consists in SiO_2 (low-k dielectric) and HfO_2 (high-k dielectric). The silicon dioxide employed as standalone dielectric in ultra-scaled transistors has become too leaky. Therefore, the introduction of HfO_2 is required to reduce the tunnel leakage current. However, the direct contact of hafnium dioxide with silicon decreases



(a) (b)

Figure 3.2.4: Silicidation; a) n-type JL-finFET, b) p-type JL-finFET.

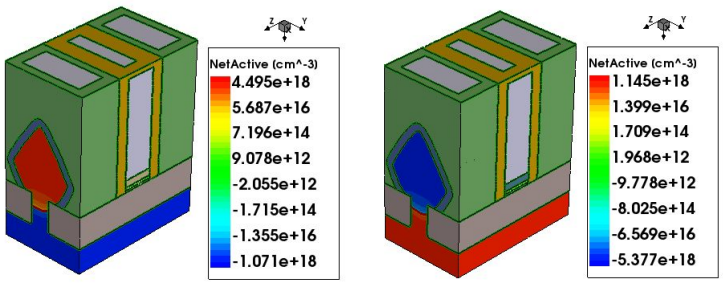
carrier mobility and creates defects, affecting the electrical characteristics of the transistors, including reliability (67). Hence, the HfO_2 is used to increase the gate capacitance which raises the gate control and SiO_2 is exploited over silicon body as interface material (68; 58; 69).
Junctionless devices exploit the work function difference between the gate electrode and the channel to deplete the carriers from the channel, so the choice of the gate material plays an important role in defining the threshold voltage. Moreover, the gate stack material employed for conventional n-type and p-type finFETs will be swapped for JL-finFETs. This procedure is done to merge the fabrication of junctionless transistors with the current manufacturing technology. Therefore, the optimal work function, which would be needed to improve the performance of the JLT won't be involved (39; 70).



(a) (b)

Figure 3.2.6: Gate stack; a) n-type JL-finFET, b) p-type JL-finFET.

To finish the process flow, a thick layer of tungsten is deposited and planarized with CMP, then self-aligned contacts is performed to prevent possible short-circuits between gate and source/drain contact due to misalignment.



(a) (b)

Figure 3.2.7: Self-aligned contacts; a) n-type JL-finFET, b) p-type JL-finFET.

The high compatibility with conventional finFET process makes this fabrication method a good choice to replace the current manufacturing steps.
The following scheme summarize the differences between the finFET and the JL-finFET.

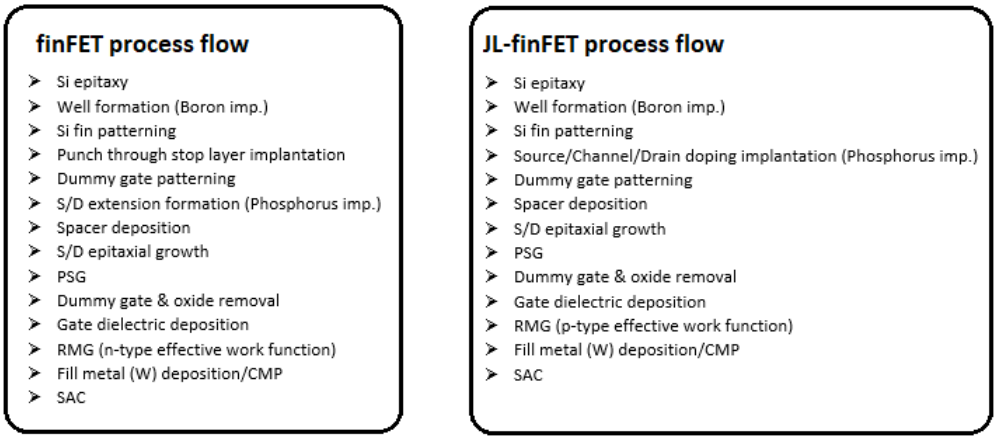


Figure 3.2.8: FinFET and JL-finFET fabrication process flow. In brackets are reported the dopants and gate workfunction for the n-type transistor.

3.3 Bulk NSGAAFET

FinFET technology was introduced to overcome limitations of planar technology relating to scaling and increasing fabrication complexity. Moreover, the continuously performance improvement demand for finFET has been achieved mainly by increasing fin height, since the effective width is twice the height plus the width. However, the resulting performance is less than what expected because of parasitic capacitance. In addition, once a technology node is chosen, the only parameter employed by designers to control the amount of current is the number of fins, which can limit flexibility (71).
Therefore, a vertically stacked nanosheet (NS) and Gate-All-Around (GAA) structure has been proposed as a promising candidate for replacing finFETs in future nodes, which allow getting better short channel control due to the GAA structure and design flexibility thanks to the variable NS widths. Larger widths will increase performance in terms of I_{ON} while increasing leakages such as DIBL. The opposite behaviour is expected if the width of the channel is reduced.
The bulk NSGAAFET structure has been built with the following specifications, by means of Sentaurus TCAD. Nevertheless, there are differences between the structure built with Sentaurus Process and the actual fabrication steps, due to the epitaxial deposition models employed in the simulations.

Parameters	Parameter Value	unit
Nanosheet height, H_{NS}	5	nm
Nanosheet channel gap, gap	5	nm
Nanosheet width, W_{NS}	18	nm
STI thickness	22	nm
Spacer length, L_{SP}	8	nm
Gate length	20	nm
S/D Doping, N_{SD}	$6 - 8 \times 10^{18}$	cm^{-3}
Channel Doping, N_{CH}	$9 \times 10^{16} - 1 \times 10^{17}$	cm^{-3}
Gate Stack		
Gate oxide (SiO_2)	0.7	nm
High-k dielectric (HfO_2)	1	nm
TiN	5.0	nm

Table 3.3.1: NSGAAFET device parameters used in the simulation.

The NSGAAFET is built on a substrate with the shallow trench isolation (STI), instead of using SOI wafer, to keep the cost low.
The process begins with the epitaxial growth of SiGe/Si multilayers. Then, fin is patterned using SIT technique, which allows to define the nanosheet width on the basis of the etching process.

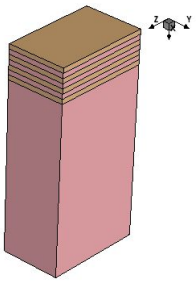
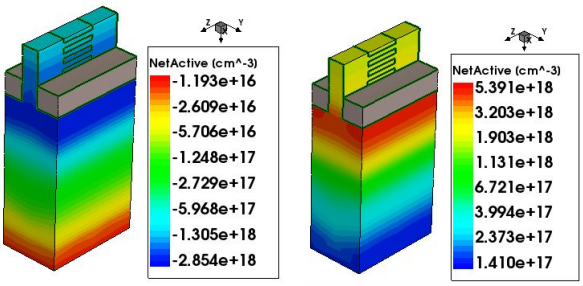


Figure 3.3.1: SiGe/Si epitaxy.

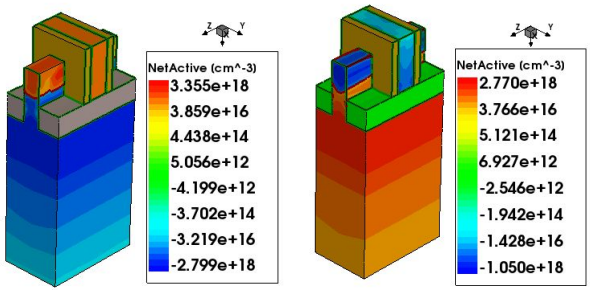
Differently from finFET process steps, the well implantation is performed after fin formation, instead of doing at the beginning of the fabrication process. This method exploit the H_{fin} to have an accurate estimation of well implant energy (43), as the diffusion of dopants in Si and SiGe is different.
However, the implementation of the NSGAAFET structure must be changed due to some issues related to the epitaxial growth used to create the raised source-drain pockets. The method employed in Sentaurus is based on the lattice kinetic Monte Carlo (LKMC) model, and it simulates the epitaxy of silicon and germanium in the atomistic scale. Hence, it describes for instance, how silane molecules interact with surface silicon atoms and then disintegrate, leaving new silicon atoms adsorbed to the surface. The hybrid mode is exploited to get the wanted shape of the grown region, so that the epitaxial growth is modelled atomistically during the diffusion step, and dopant diffusion in continuum mode. Since the alternating doped deposition and inert annealing are used, which take into account the material-dependent growth rates of silicon and silicon-germanium, the regrown crystalline is not completely free of irregularities, hence several defects can form. Furthermore, to obtain the desired shape of the raised source-drain pockets and control the dopants redistribution during annealing, some adjustments are needed for the 3D epitaxy (8; 72).
The solution adopted to solve these issues is to replace the SiGe material in the stacked layers, where the raised source-drain contacts will be built.



(a) (b)

Figure 3.3.2: Well implantation; (a) n-type NSGAAFET and (b) p-type NSGAAFET.

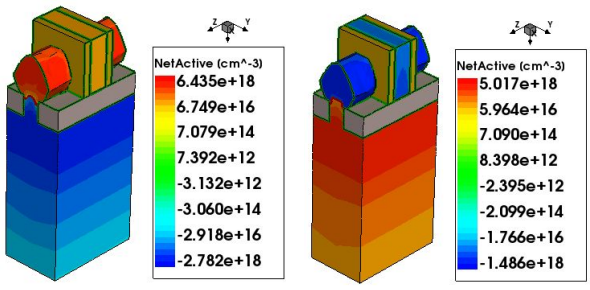
This is followed by the deposition and planarization of polysilicon, by means of CMP. A selective etching of polysilicon, performed through reactive ion etching (RIE), is now essential to define the dummy gate. Then, source and drain extension are formed. Successively, spacers made of SiN are patterned along the vertical walls of the gate with an anisotropic etching process.
Till now, the steps employed to fabricate three vertical-stacked NSGAAFET are similar to what illustrated during finFET process (3.1). However, to obtain the gate-all-around structure, it is required to build inner spacers, which will avoid short-circuits between the metal gate and the source/drain contacts. To this purpose, an anisotropic etching of SiGe/Si layers is carried out. At this point, the SiGe layers inside the spacers are partially etched back, leaving some cavities that will be later filled with SiN, to isolate the channels.



(a) (b)

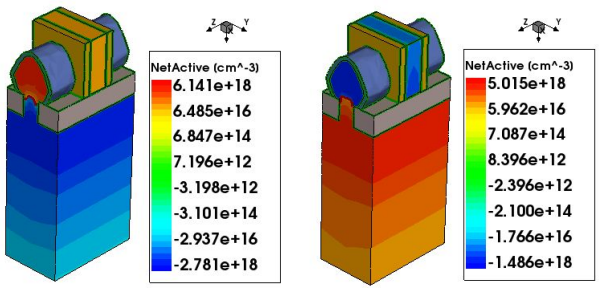
Figure 3.3.3: Spacer formation; (a) n-type NSGAAFET and (b) p-type NSGAAFET.

Source and drain regions are now epitaxially grown to exploit strain technology, thus enhancing the carrier mobility. Then, silicidation is performed to reduce contact resistivity.
The PSG is deposited on the structure as insulating layer, followed by a CMP process that planarized the structure using the dummy gate as etch stop layer (ESL).



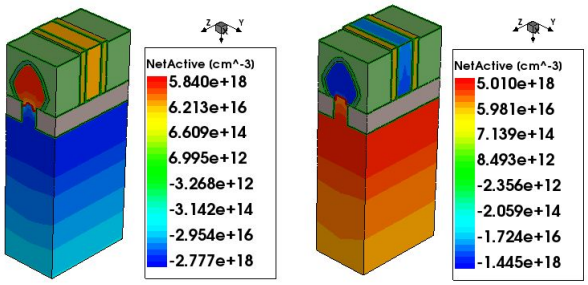
(a) (b)

Figure 3.3.4: S/D fabrication; (a) n-type NSGAAFET and (b) p-type NSGAAFET.



(a) (b)

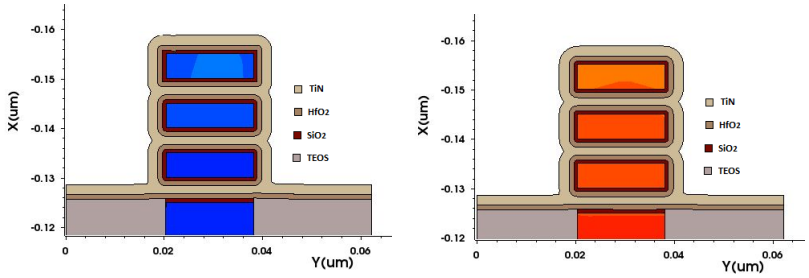
Figure 3.3.5: Silicidation; (a) n-type NSGAAFET and (b) p-type NSGAAFET.



(a) (b)

Figure 3.3.6: PSG; (a) n-type NSGAAFET and (b) p-type NSGAAFET.

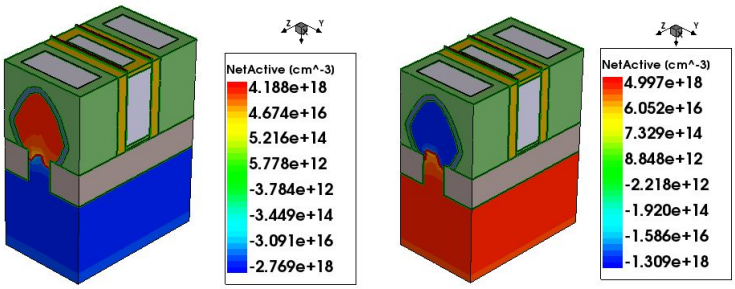
The dummy gate is removed and the silicon channels are released by etching the SiGe sacrificial layers. The gate stack is built by depositing through atomic layer deposition (ALD) the interfacial layer (SiO_2), the high-k dielectric (HfO_2) and metal gate (TiN).



(a) (b)

Figure 3.3.7: RMG; (a) n-type NSGAAFET and (b) p-type NSGAAFET.

Lastly, tungsten is deposited and planarized with CMP, then SAC is performed to prevent possible short-circuits between gate and source/drain contact due to misalignment (71; 73; 74; 75).



(a) (b)

Figure 3.3.8: SAC; (a) n-type NSGAAFET and (b) p-type NSGAAFET.

The fabrication process mentioned have great similarities with the finFET one, except for five steps: SiGe/Si epitaxial growth, SiGe/Si fin patterning, punch through stop layer, inner spacer definition and sacrificial SiGe layers removal.
The high compatibility with finFET process makes this approach the most used for NSGAFFET fabrication.

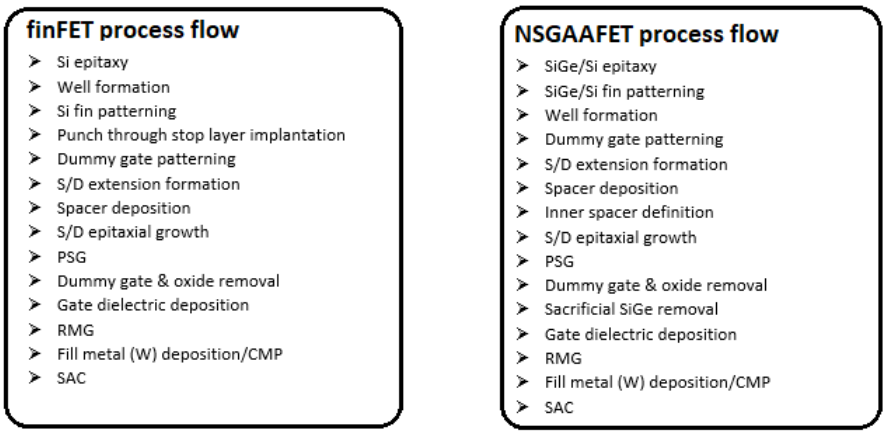


Figure 3.3.9: FinFET and NSGAAFET fabrication process flow.

3.4 Bulk JL-NSGAAFET

Gate-all-Around (GAA) nanowire (NW) or nanosheet (NS) field-effect transistors (FETs) are the promising candidate to continue scaling down the transistor. The improvement of electrostatic gate control over the channel can be achieved compared to other structures, such as finFETs.
However, finFET structure can offer higher drive current, since changing the finFET into GAA-NW while keeping same footprint, it reduces the active channel area. Therefore, the typical structure employed with the GAA technology is the nanosheet, which offers not only the possibility to significantly enhance the effective width (W_{eff}), but also the flexibility to the designers to adapt this parameter to the amount of current they want to achieve (76; 74; 73).
Moreover, it is also possible to stack several nanosheets vertically to improve the drain current when the transistor is turned on. Nevertheless, the parasitic components, such DIBL and I_{OFF}, might increase.
On the other perspective, the junctionless transistor (JLT) has been studied to improve short channel effects (SCE) and further scale down the technology. The JLT can be fabricated simpler than the existing inversion mode FET because of the absence of the p-n junctions. In addition, junctionless devices are subjected to lower electric field in the channels, lower leakage current, nearly ideal subthreshold slope (SS) and better scalability, over a conventional MOSFET (76).
Some studies involving the fabrication of junctionless GAA structures, exploit the electron beam lithography, which is not suitable for a large-scale production (77; 78). In other papers, they have reported building multi-channel gate-all-around devices, using deep reactive-ion etching (also called Bosch process) (79) and SOI wafers (80). However, the transistor reported in (79) works in depletion-mode and using SOI wafers would increase too much the manufacturing cost.
Therefore, in this thesis it is explored a fabrication process for JL-NSGAAFET, which takes the steps employed in the manufacturing of conventional NSGAAFET, and it is adjusted to satisfy the requirements of junctionless technology.
The current of JLT is dominated by body current instead of surface current between gate oxide and inversion channel layer, and it is proportional to the doping concentration as seen in equation 2.2. Hence, if N_{CH} is increased, the drive current is improved when the transistor is turned on. However, it is difficult to fully deplete the channel, if high doping concentration is exploited. Therefore, V_{TH} decreased (81; 82) . Moreover, if we want to keep the depletion effective as the doping concentration is increased, the channel cross section must be reduced.
The dimensions exploited for the fabrication of the JL-NSGAAFET in this chapter are the same of the NSGAAFET, so that the two technologies can be compared.
The parameters are reported in the Tab.3.4.1.

The major difference between the two structures, apart from the absence of the p-n junctions as it will be seen in the final structure, is that the JL-NSGAAFET has one suspended nanosheet, instead of three.

Parameters	Parameter Value	unit
Nanosheet height, H_{NS}	5	nm
Nanosheet channel gap, gap	5	nm
Nanosheet width, W_{NS}	18	nm
STI thickness	22	nm
Spacer length, L_{SP}	8	nm
Gate length	20	nm
Source/Channel/Drain Doping, N_{SD}	6×10^{18}	cm^{-3}
Gate Stack		
Gate oxide (SiO_2)	0.7	nm
High-k dielectric (HfO_2)	1	nm
TiN	5.0	nm

Table 3.4.1: JL-NSGAAFET device parameters used in the simulation.

The JL-NSGAAFET fabrication process begins with the epitaxial growth of SiGe/Si multilayers. This stack is performed to obtain one suspended channel when the silicon-germanium is going to be etched away.

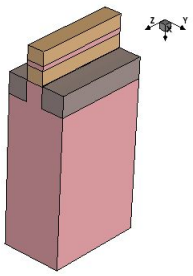
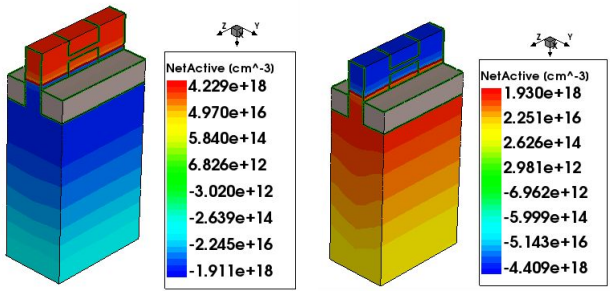


Figure 3.4.1: Deposition of SiGe/Si layers.

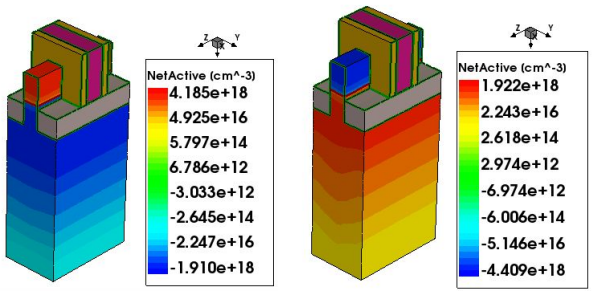
Fin is patterned using SIT technique, which allows to define the nanosheet width on the basis of the etching process parameters. Then, the shallow trench isolation is performed to reduce parasitics.
The well implantation is done after fin formation, like it has been seen for the conventional NSGAAFET. Then, the exposed fin is doped with phosphorus (boron) to build a n-type (p-type) transistor.



(a) (b)

Figure 3.4.2: Well and channel doping; (a) n-type JL-NSGAAFET and (b) p-type JL-NSGAAFET.

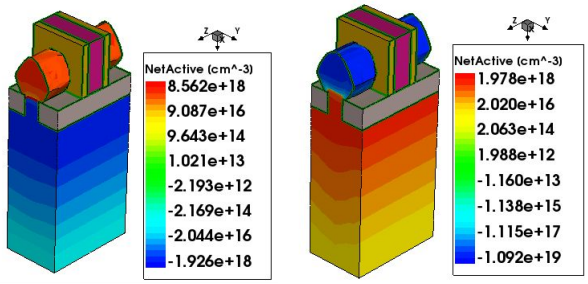
This is followed by the deposition and planarization of polysilicon, by means of CMP. A selective etching of polysilicon, performed through reactive ion etching (RIE), is now essential to define the dummy gate. Then, source and drain extension are formed. Successively, spacers made of SiN are patterned along the vertical walls of the gate with an anisotropic etching process.
To build the GAAFET, it is required to build inner spacers, which will avoid short-circuits between the metal gate and the source/drain contacts. To this purpose, an anisotropic etching of SiGe/Si layers is carried out. At this point, the SiGe layers inside the spacers are partially etched back, leaving some cavities that will be later filled with SiN, to isolate the channels.



(a) (b)

Figure 3.4.3: Spacer formation; (a) n-type JL-NSGAAFET and (b) p-type JL- NSGAAFET.

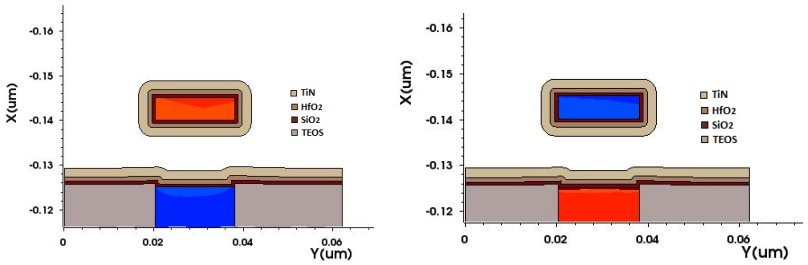
Source and drain regions are now epitaxially grown to exploit strain technology, thus enhancing the carrier mobility. Then, silicidation is performed to reduce contact resistivity. The PSG is deposited on the structure as insulating layer, followed by a CMP process that planarized the structure using the dummy gate as etch stop layer (ESL).



(a) (b)

Figure 3.4.4: S/D fabrication; (a) n-type JL-NSGAAFET and (b) p-type JL-NSGAAFET.

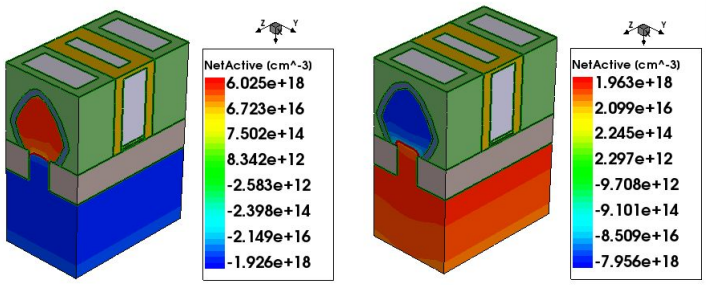
The dummy gate is removed and the silicon channel is released by etching the SiGe sacrificial layers. The gate stack is built by depositing through atomic layer deposition (ALD) the interfacial layer (SiO_2), the high-k dielectric (HfO_2) and metal gate (TiN).



(a) (b)

Figure 3.4.5: RMG; (a) n-type JL-NSGAAFET and (b) p-type JL-NSGAAFET.

Lastly, tungsten is deposited and planarized with CMP, then SAC is performed to prevent possible short-circuits between gate and source/drain contact due to misalignment (71; 73; 74; 75).



(a) (b)

Figure 3.4.6: SAC; (a) n-type JL-NSGAAFET and (b) p-type JL-NSGAAFET.

The fabrication process mentioned have great similarities with the NSGAAFET one, so it should be feasible to adopt this technology in the current industry. Moreover, the issue related to the dopant redistribution in the fabrication of p-n junctions of conventional MOSFET at nanoscale is solved.

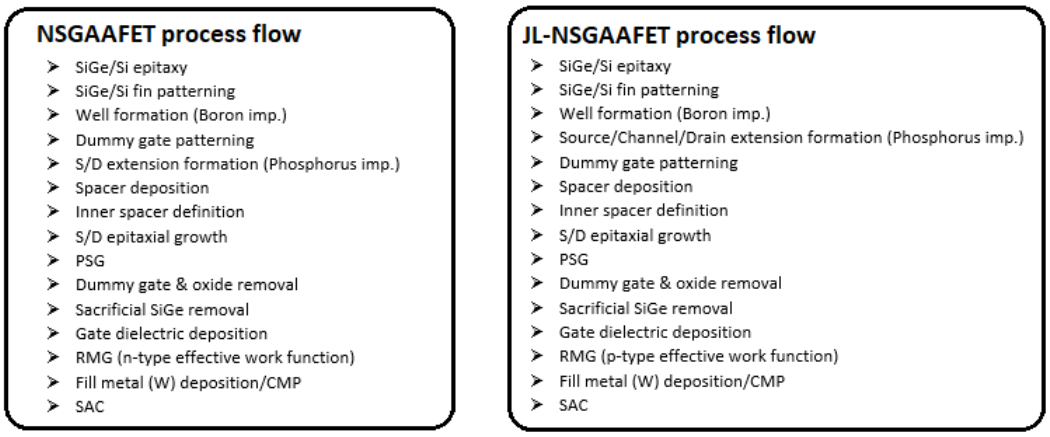


Figure 3.4.7: NSGAAFET and JL-NSGAAFET fabrication process flow.

Chapter 4

Electrical simulations

The electrical device simulations of junctionless and conventional transistors are made by means of Synopsys Sentaurus Device (8), then the results are visualized, analysed, and compared with Sentaurus Inspect.

4.1 Simulation models

The simulation performed on the 3D devices comprehends the silicon bandgap narrowing model that determines the intrinsic carrier concentration, and the density gradient model. The mobility model specifications take into account the carrier mobility degradation due to carrier scattering on ionized impurities, the carrier velocity saturation in high electric field, and the mobility degradation due to surface roughness scattering. The bandgap narrowing model is activated due to the presence of doping according to the Slotboom model. Shockley-Read-Hall recombination with doping-dependent lifetime and band-to-band tunnelling are also included in the simulation.
The analytical study is performed on the n-type and p-type 3D multigate structures previously made with Sentaurus Process. The trans-characteristic I_D-V_{GS} is obtained by computing a set of equations: the Poisson equation and continuity equations (electrons and holes), while taking into account quantum corrections for the specified carriers related to the type of the transistor.
The Poisson equation is:

$$\nabla \cdot (\varepsilon \nabla \phi) = -q\,(p - n + N_D - N_A) \tag{4.1}$$

While the continuity equations for carrier transport are:

$$\nabla \cdot \overrightarrow{J}_n = qR_{net,n} + q\frac{\partial n}{\partial t} \qquad -\nabla \cdot \overrightarrow{J}_p = qR_{net,p} + q\frac{\partial p}{\partial t} \tag{4.2}$$

where:

- ε is the electrical permittivity.

- q is the elementary electronic charge.
- N_D is the concentration of ionized donors.
- N_A is the concentration of ionized acceptors.
- $R_{net,n}$ and $R_{net,p}$ are the electron and hole net recombination rate, respectively.
- $\overrightarrow{J}_n$ is the electron current density.
- $\overrightarrow{J}_p$ is the hole current density.
- n and p are the electron and hole density, respectively.

These equations in their differential form describes the local microscopic behaviour of the material under analysis. The Poisson equation expresses the local change of the electric field due to the volumetric charge density in a point (x, y, z), in the material. The continuity equations express the conservation of electrons and holes in the same point. The flow of electrons and holes are either driven by an electric field (when a voltage is applied) in case of drift current or by a concentration gradient in case of diffusion current.
Moreover, the potential distribution and the electron/hole distribution are obtained by solving these equations with the proper boundary conditions (initial operating electrode potentials). In this way, the electron current and hole current can be estimated at any proper section. Thanks to the device simulator developed by Synopsys, the results give an accurate knowledge of the semiconductor parameters, which allow to estimate the electrical characteristics of the transistor.
The method employed to describe carrier confinement in arbitrary potential wells is called density gradient model, which is a first-order quantum-correction model. The model exploits the gradients of the carrier densities to describe carrier confinement by locally modifying the electrostatic potential through a correction potential. This correction potential has to be calculated separately for each carrier type and added to the electrostatic potential for and only for the respective charge carrier transport equation (83).
In the density gradient approximation, the quantum potential is a function of the carrier densities and their gradients, which requires the self-consistent quantum potential and the carrier transport equations solution (8). The analysis is focused on collecting the figures of merit, such as V_{TH}, SS and DIBL.
The threshold voltage is extracted from the I_D-V_{GS} curve in linear regime using the maximum transconductance method. Therefore, the V_{TH} is defined as the intersection of the tangent at the maximum transconductance ($g_m = dI_D/dV_{GS}$) point with the gate voltage (84).
The subthreshold slope (SS) indicates how easily a transistor can be turned off, in particular it is the V_{GS} reduction needed to reduce of one order of magnitude I_{OFF}.
This parameter has been calculated according to the following equation, which is defined as the inverse of logarithmic slope in sub-threshold slope drain current.

$$SS = \left(\frac{d \log_{10} I_D}{dV_{GS}} \right)^{-1} \tag{4.3}$$

The subthreshold slope is obtained by setting the voltage where the slope of the transcharacteristic (in linear regime) is read. Since the slope may be noisy at the beginning of the curve or at very low current levels, the data are obtained at I_D=182 pA.
Since the transistor under analysis is a short-channel device, the threshold voltage decreases as the voltage applied to the drain increases. Moreover, as drain voltage is increased, the depletion region of the p-n junction between the drain and body increase in size and extends under the gate, so that the gate can control less effectively the charge in the channel, due to the reduction of the energy barrier near the drain electrode (85). This is what it is called drain-induced barrier lowering (DIBL). DIBL has been calculated according to the following equation as reported in (69):

$$DIBL\left(\frac{mV}{V}\right) = -\frac{V_{TH(V_{D2})} - V_{TH(V_{D1})}}{V_{D2} - V_{D1}} \tag{4.4}$$

where $V_{TH(V_{D1})}$ is the threshold voltage estimated at low drain voltage (V_{D1}); $V_{TH(V_{D2})}$ is the threshold voltage when the drain voltage is equal to the supply voltage (V_{D2}=V_{DD}).
Another relevant figure of merit for a device working as a switch is the I_{ON}/I_{OFF}, which is used to have a better understanding of the performance of the device. Having an high ratio means that the transistor can drive high current when it is turned on while having low leakage current when the device is switched off.
The I_{ON} and I_{OFF} are evaluated in saturation regime, which means that the V_{DS} is set to V_{DD} and V_{GS} goes from 0 V to V_{DD}. In particular I_{OFF} is acquired at V_{DS}= V_{DD}, V_{GS}= 0 V, while I_{ON} is extracted at V_{DS}= V_{DD} and V_{GS}= V_{DD}.

4.2 Bulk finFET

4.2.1 p-type finFET

Firstly, the p-type transistor was simulated in linear and saturation region for a V_{DS}=-0.05 V and V_{DS}=-0.75 V respectively. The gate was varied in the range [0 V, -0.75 V] for both transients then the resulting curves were plotted with Sentaurus Inspect. The simulation range is chosen considering the performance and power scaling in nanostructures (30).

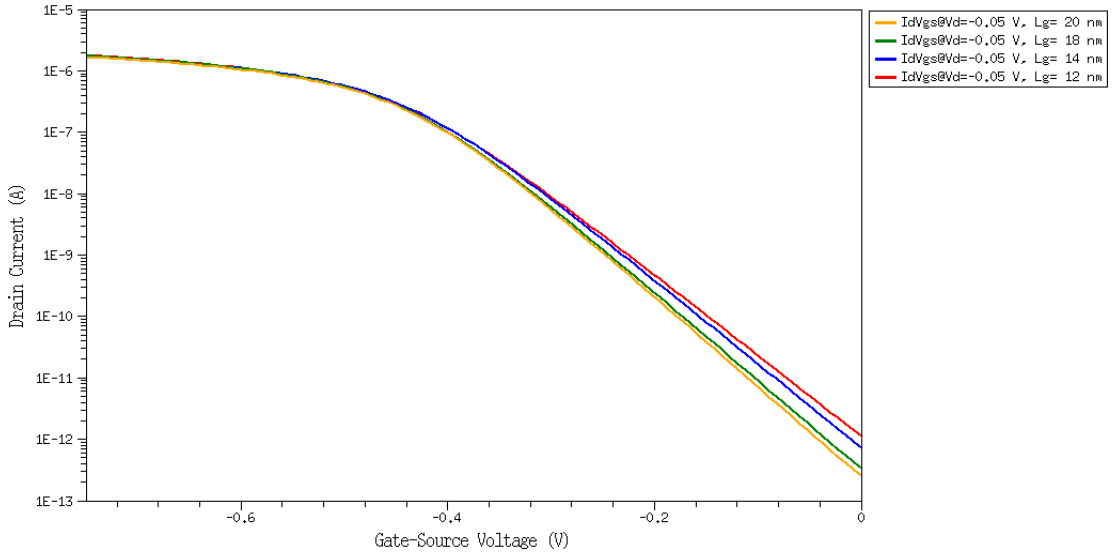


Figure 4.2.1: $I_D - V_{GS}$ characteristic of p-type finFET with different channel lengths, in linear regime.

All the figures of merit related to the p-type transistor with L_g= [12,14,18,20] nm are reported in the following table:

finFET (p-type) V_{DD}= -0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	-0.40	-0.40	-0.41	-0.41
I_{ON} (µA)	-5.34	-5.25	-5.14	-4.94
I_{OFF} (pA)	-8.09	-3.88	-1.15	-0.72
I_{ON}/I_{OFF}	6.61×10^5	1.35×10^6	4.48×10^6	6.90×10^6
SS (mV/dec)	80.01	79.63	79.43	78.92
DIBL (mV/V)	64.39	51.95	45.33	40.34

Table 4.2.1: V_{TH}, I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS, DIBL of p-type bulk finFET with different channel lengths.

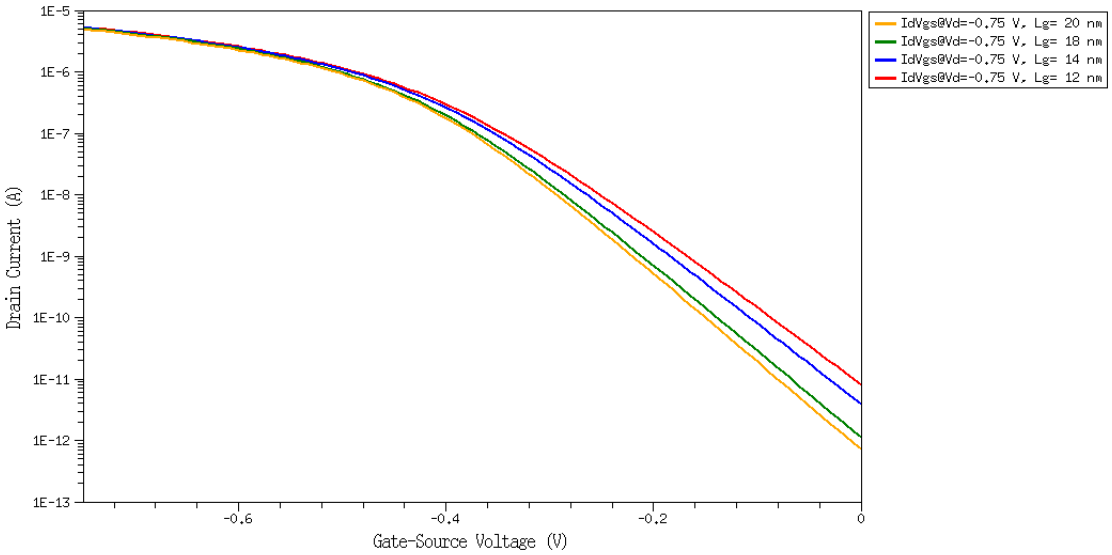


Figure 4.2.2: $I_D - V_{GS}$ characteristic of p-type finFET with different channel lengths, in saturation regime.

Despite the fact that the IRDS (30) suggests a supply voltage of -0.75 V for these channel lengths, the V_{DD} has been raised to increase the current I_{ON} (Tab.4.2.2).

finFET (p-type) V_{DD}= -1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	-11.11	-10.92	-10.81	-10.44
I_{OFF} (pA)	-14.06	-6.23	-1.65	-1.10
I_{ON}/I_{OFF}	7.90×10^5	1.75×10^6	6.55×10^6	9.49×10^6

Table 4.2.2: I_{ON}, I_{OFF}, I_{ON}/I_{OFF} of different channel lengths p-type bulk finFET.

As it can be seen from the data extracted from Sentaurus TCAD, the threshold voltage is slightly reduced when the channel shrinks. Moreover, it's clear that as the device is scaled down, the parameters such as I_{OFF}, SS, DIBL and I_{ON}/I_{OFF} are worsened.
Nevertheless, the drain current increases, which is expected, considering that in equation 2.1, when the oxide capacitance and the channel length are reduced, the current is improved if all the other parameters are constant. However, the current is not as high as expected and this is due to the doping concentration of the raised source/drain contacts. Comparing the current obtained in (74) with its high dopant concentration (10^{20} cm^{-3}), the transistor I made, takes into account the various steps required to build the structure during fabrication. Therefore, the process steps adopted to obtain the electrical characteristics in Tab. 4.2.1 emulate different scenario, such as implantation with tilt of 10° and annealing processes.

Most papers in literature in which are built transistors to test their behaviours, it is not taken into account the lateral diffusion that occurs during fabrication, since when making the source and drain epitaxially grow, the dopant concentration is initialized within the silicon structure.
The software employed for the simulations does not consider the diffusion of metals in the semiconductor which occurs in conventional transistors, thus affecting the resistance of the source/drain contacts.
Moreover, the program written for different channel lengths exploits the same dose implanted in the device, which is not correct according to the scaling policy. This is done to analyse how the transistors behave when changing one parameter at a time.
Therefore, the dose is chosen considering the worst case scenario in terms of lateral diffusion, which occurs when the gate length is the shortest one (12 nm), as it is shown in Fig.4.2.3.

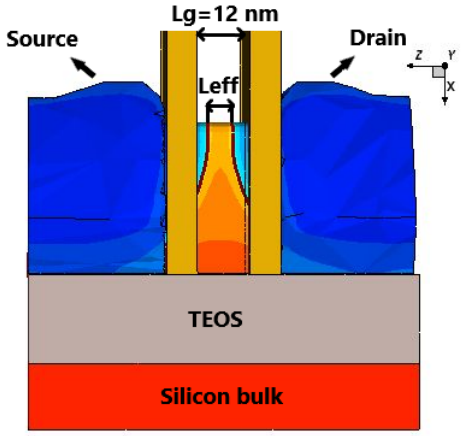


Figure 4.2.3: p-type finFET with physical gate length L_g= 12 nm, and shorter channel length (L_{eff}), due to dopant redistribution.

The actual channel length is shorter than the nominal one, due to the lateral diffusion of dopants from source/drain contacts into the channel (23). This dopant fluctuations are a relevant problem in nanoscale devices, since it affects the threshold voltage of the transistor, thus compromising its reliability.
Hence, it is becoming difficult to fabricate a conventional MOSFET with abrupt doped junctions, while keeping high doped source/drain contacts to further reduce the electrical resistance, and therefore increasing the current.
This is why junctionless technology has become more relevant nowadays, since the wanted current can be simply increased by doping concentration and no junctions is present.
The structure has been simulated with different channel lengths while keeping constant the dose implanted in the transistor. The reason why the gate length is explored within 10 nm variation for the simulations, is to attenuate the error due to the constant dose implanted in the device under analysis.

Thereafter, it is important to study what happens when the dose implanted in the source and drain pockets is increased for the L_g=20 nm transistor.
This study is carried out to prove that bigger transistor can provide more current with respect to shorter one, due to scaling policy.
The results are reported in Tab.4.2.3. It can be noticed that the drive current is improved by 156% for the p-type transistor (L_g=20 nm).

p-type finFET (L_g=20 nm) V_{DD}= -0.75 V				
Parameters	Parameter Values			
Dose (cm^{-2})	7.0 E12	1.0 E13	2.0 E13	5.0 E13
V_{TH} (V)	-0.40	-0.40	-0.40	-0.39
I_{ON} (µA)	-6.26	-8.08	-12.19	-16.16
I_{OFF} (pA)	-0.91	-1.33	-3.20	-10.41
I_{ON}/I_{OFF}	6.91×10^6	6.10×10^6	3.81×10^6	1.55×10^6
SS (mV/dec)	78.95	79.69	80.79	83.60
DIBL (mV/V)	40.42	41.74	42.12	43.43

Table 4.2.3: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of p-type bulk finFET with various doses implanted.

4.2.2 n-type finFET

Considering the equations 4.1 and 4.2, the n-type finFET trans-characteristic is estimated by means of Sentaurus TCAD.
During the fabrication of finFETs, the aim was to obtain a symmetric voltage for p-type and n-type, so that they could be employed in a CMOS technology. Therefore, even though they use different dopants according to their conduction mechanism, the process steps are calibrated to get the wanted behaviours. The same concept is applied when analysing the electrical parameters.
Moreover, the range where the device is tested is the same for the p-type but with opposite polarity. The linear regime (V_{GS}=[0, 0.75] V, V_{DS}=[0, 0.05] V) and saturation regime (V_{GS}=[0, 0.75] V, V_{DS}= [0, 0.75] V) are shown in Fig.4.2.4 and Fig.4.2.5. The figures of

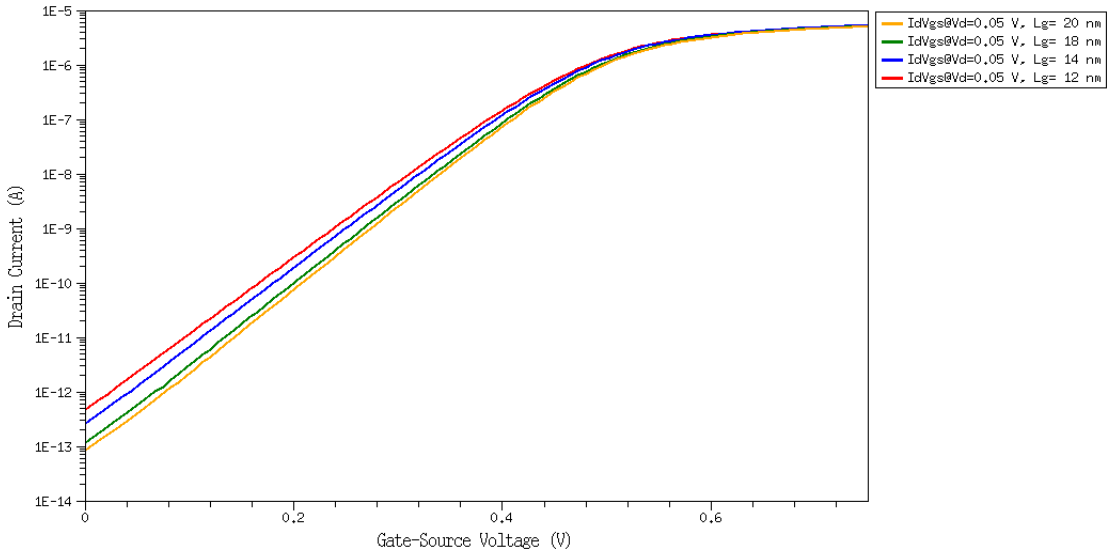


Figure 4.2.4: $I_D - V_{GS}$ characteristic of n-type finFET with different channel lengths, in linear regime.

merit of the n-type finFET are extracted from the data of the I_D-V_{GS} curves for different channel lengths and reported in Tab.4.2.4. The V_{DD} has been raised to increase the current I_{ON}, for the n-type finFET structure (Tab.4.2.5). Since the L_g=20 nm transistor is able to preserve better its channel length with respect to the shorter one (L_g= 12 nm), due to lateral redistribution of dopants, the dose implanted in the source and drain pockets can be increased to enhance the I_{ON}. Indeed, the drive current is improved by 85% for the n-type transistor, as reported in Tab.4.2.6.
It can be noticed from the results obtained, that the n-type finFET has an overall better performance with respect to the p-type finFET. This behaviour is expected since the electron mobility is higher than the hole mobility. Electrons travel in the conduction band whereas holes travel in the valence band. Since holes are created by electron excitation, they are subjected to stronger atomic force by the nucleus than the electrons, hence holes has lower mobility.

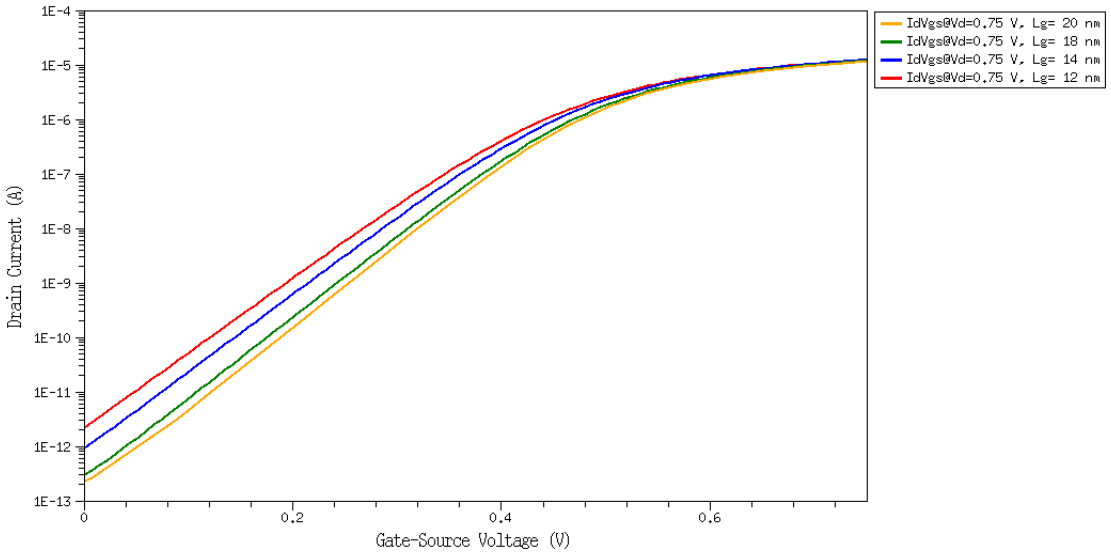


Figure 4.2.5: $I_D - V_{GS}$ characteristic of n-type finFET with different channel lengths, in saturation regime.

finFET (n-type) V_{DD}= 0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	0.44	0.45	0.45	0.46
I_{ON} (µA)	12.38	12.36	11.86	11.81
I_{OFF} (pA)	2.20	0.92	0.30	0.23
I_{ON}/I_{OFF}	5.64×10^6	1.35×10^7	3.96×10^7	5.20×10^7
SS (mV/dec)	78.93	78.24	77.56	75.93
DIBL (mV/V)	57.12	47.14	44.47	39.20

Table 4.2.4: V_{TH}, I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS, DIBL of n-type bulk finFET with different channel lengths.

n-type finFET (L_g=20 nm) V_{DD}= 0.75 V				
Parameters	Parameter Values			
Dose (cm^{-2})	7.0 E12	1.0 E13	2.0 E13	5.0 E13
V_{TH} (V)	0.46	0.46	0.46	0.45
I_{ON} (µA)	13.64	15.60	19.64	25.27
I_{OFF} (pA)	0.24	0.29	0.44	1.25
I_{ON}/I_{OFF}	5.65×10^7	5.48×10^7	4.48×10^7	2.02×10^7
SS (mV/dec)	75.80	76.11	77.98	79.60
DIBL (mV/V)	39.65	40.13	40.70	41.63

Table 4.2.6: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of n-type bulk finFET with various doses implanted.

finFET (n-type) V_{DD}= 1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	21.92	21.90	21.35	21.32
I_{OFF} (pA)	3.65	1.35	0.43	0.27
I_{ON}/I_{OFF}	5.99×10^{6}	1.63×10^{7}	4.97×10^{7}	7.90×10^{7}

Table 4.2.5: I_{ON}, I_{OFF}, I_{ON}/I_{OFF} of different channel lengths n-type bulk finFET.

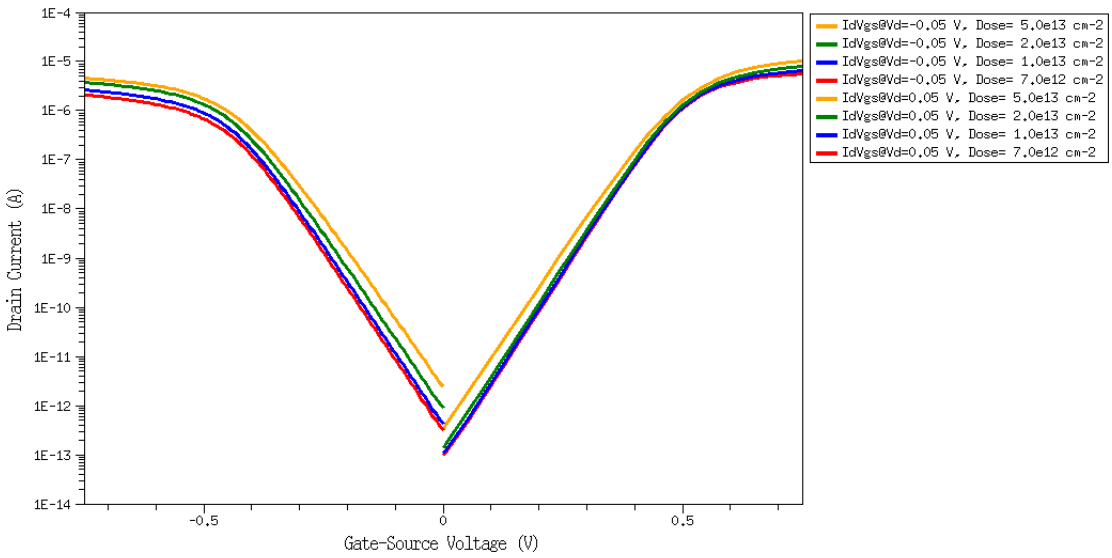


Figure 4.2.6: $I_D - V_{GS}$ characteristic of p-type finFET (left) and n-type finFET (right) (L_g= 20 nm), in linear regime.

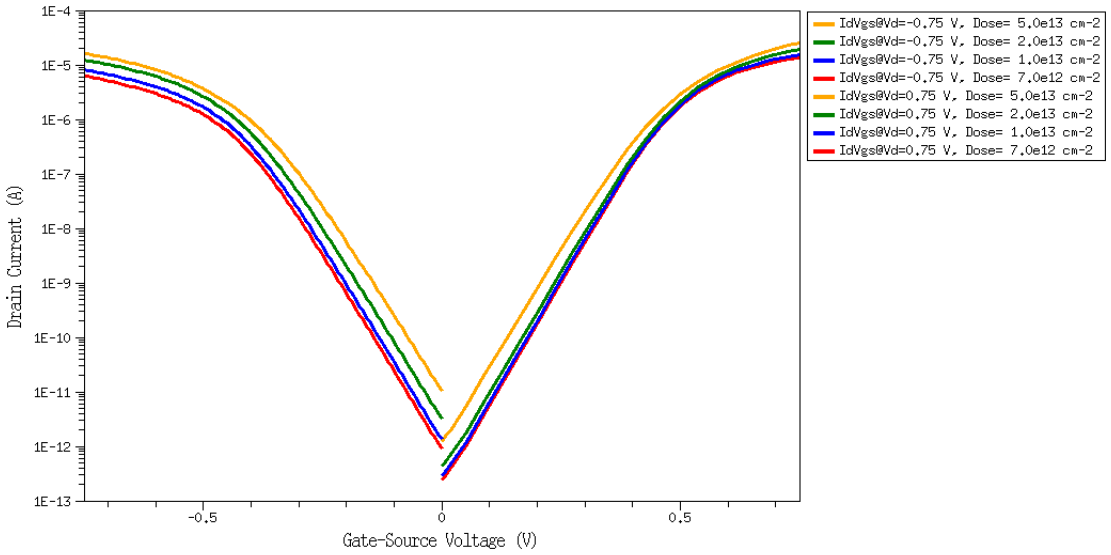


Figure 4.2.7: $I_D - V_{GS}$ characteristic of p-type finFET and n-type finFET (right) (L_g= 20 nm), in saturation regime.

4.3 Bulk JL-finFET

4.3.1 p-type JL-finFET

Considering equations 4.1 and 4.2, the simulations are carried out for junctionless devices as well. In particular, the analysis is focused on the comparison of conventional MOSFETs and the junctionless finFETs, therefore the SDevice settings employed must be the same to have faithful data.
The current-voltage characteristics of the JL-finFET are very similar to those of a conventional MOSFET.
The p-type JL-finFET is analysed in linear and saturation region for a V_{DS}=-0.05 V and V_{DS}=-0.75 V respectively. The gate was varied in the range [0 V, -0.75 V] for both transients for different channel lengths to observe how it works when the device is shrunk.

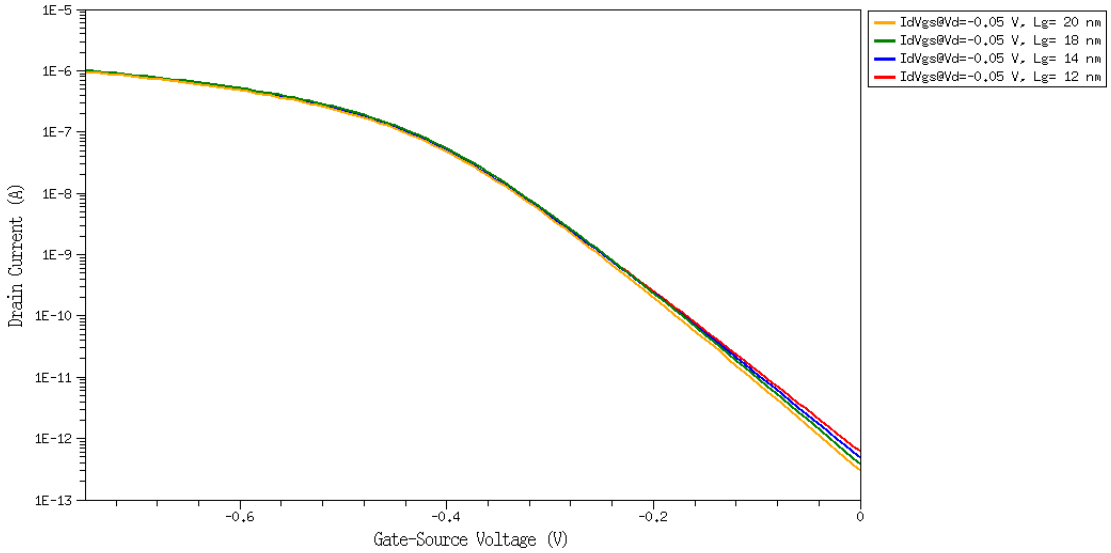


Figure 4.3.1: $I_D - V_{GS}$ characteristic of p-type JL-finFET with different channel lengths, in linear regime.

The figures of merit extracted from the plots are reported in Tab.4.3.1. As it can be seen from the data extracted from Sentaurus TCAD, the threshold voltage is slightly reduced when the channel shrinks. Moreover, it's clear that as the device is scaled down, the parameters such as I_{OFF}, SS, DIBL and I_{ON}/I_{OFF} are worsened. Moreover, it can be noticed, that the I_{ON}/I_{OFF} provided by the p-type junctionless device is worse than the conventional finFET.
However, since the device behaves like a resistor (2.2), when the length is reduced, the I_{ON} is slightly improved.

The V_{DD} has been raised to increase the current I_{ON}, for the p-type finFET structure (Tab.4.3.2).

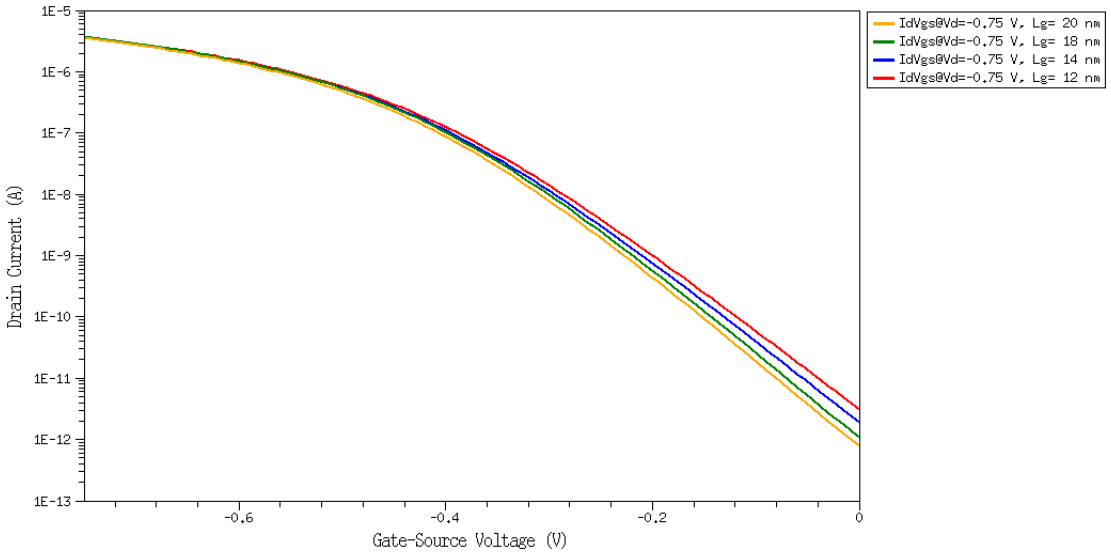


Figure 4.3.2: $I_D - V_{GS}$ characteristic of p-type JL-finFET with different channel lengths, in saturation regime.

Junctionless finFET (p-type) V_{DD}= -0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	-0.45	-0.45	-0.45	-0.46
I_{ON} (µA)	-3.71	-3.65	-3.60	-3.54
I_{OFF} (pA)	-3.11	-1.93	-1.10	-0.78
I_{ON}/I_{OFF}	1.19×10^6	1.89×10^6	3.38×10^6	4.51×10^6
SS (mV/dec)	75.55	73.48	70.54	69.70
DIBL (mV/V)	49.43	39.61	28.91	25.60

Table 4.3.1: V_{TH}, I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS, DIBL of p-type bulk JL-finFET with different channel lengths.

Now, the same analysis done for the dose in conventional finFET is performed for the junctionless device. The current I_{ON} is increased by 84% for the p-type transistor, as the implanted dose gets higher (Tab.4.3.3).

Junctionless finFET (p-type) V_{DD}= -1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	-8.78	-8.66	-8.61	-8.55
I_{OFF} (pA)	-4.70	-2.73	-1.46	-1.04
I_{ON}/I_{OFF}	1.87×10^{6}	3.17×10^{6}	5.88×10^{6}	8.21×10^{6}

Table 4.3.2: I_{ON}, I_{OFF}, I_{ON}/I_{OFF} of different channel lengths p-type bulk JL-finFET.

p-type JL-finFET (L_g=20 nm) V_{DD}= -0.75 V			
Parameters	Parameter Values		
Dose (cm^{-2})	7.0 E13	1.0 E14	3.0 E14
V_{TH} (V)	-0.50	-0.48	-0.45
I_{ON} (µA)	-7.76	-9.66	-14.28
I_{OFF} (pA)	-0.46	-0.70	-5.25
I_{ON}/I_{OFF}	1.69×10^{7}	1.39×10^{7}	2.72×10^{6}
SS (mV/dec)	69.80	70.25	74.59
DIBL (mV/V)	26.26	27.83	33.83

Table 4.3.3: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of p-type bulk JL-finFET with various doses implanted.

4.3.2 n-type JL-finFET

For different channel lengths, the I_D-V_{GS} characteristics in linear and saturation regime for the n-type JL-finFET is reported in Fig.4.3.3 and Fig.4.3.4 respectively. As expected, when shrinking the channel lengths, the performances of the transistor such as V_{TH}, DIBL, SS, I_{OFF} and I_{ON}/I_{OFF} get worse. However, since the device behaves like a resistor (2.2), when the length is reduced, the I_{ON} is slightly improved.
All the figures of merit related to the n-type JL-finFET with various gate lengths are reported in the following table:

Junctionless finFET (n-type) V_{DD}= 0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	0.53	0.55	0.59	0.60
I_{ON} (µA)	9.46	8.39	6.75	6.18
I_{OFF} (pA)	1.62	0.30	2.66 E-2	1.29 E-2
I_{ON}/I_{OFF}	5.85×10^{6}	2.82×10^{7}	2.54×10^{8}	4.78×10^{8}
SS (mV/dec)	77.17	73.52	68.80	66.15
DIBL (mV/V)	65.97	53.95	37.78	30.49

Table 4.3.4: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of different channel lengths n-type bulk JL-finFET.

The data trends follow what expected from different papers regarding junctionless multigate transistors (20; 23; 86).

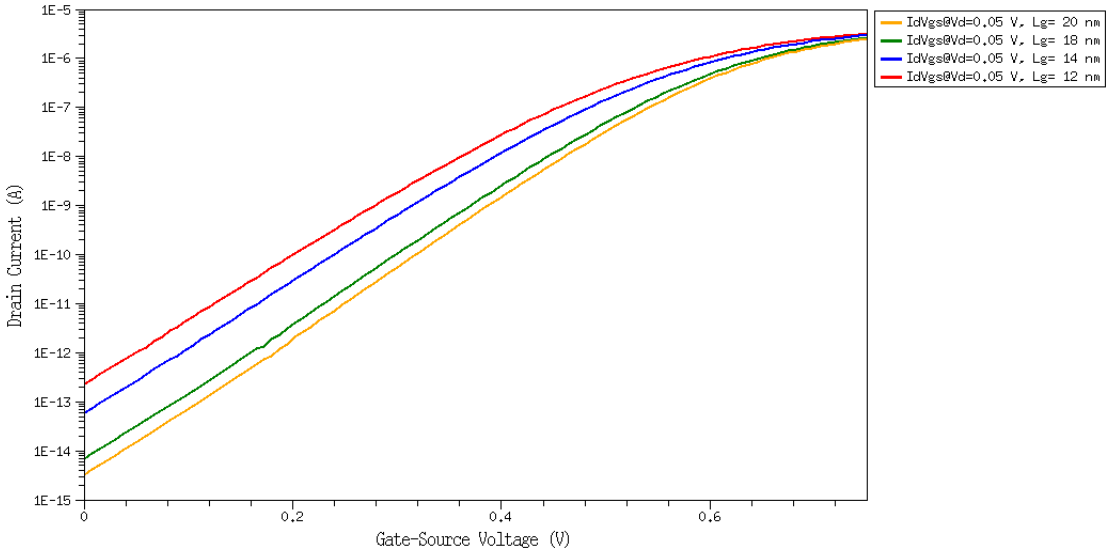


Figure 4.3.3: $I_D - V_{GS}$ characteristic of different channel lengths n-type JL-finFET, in linear regime.

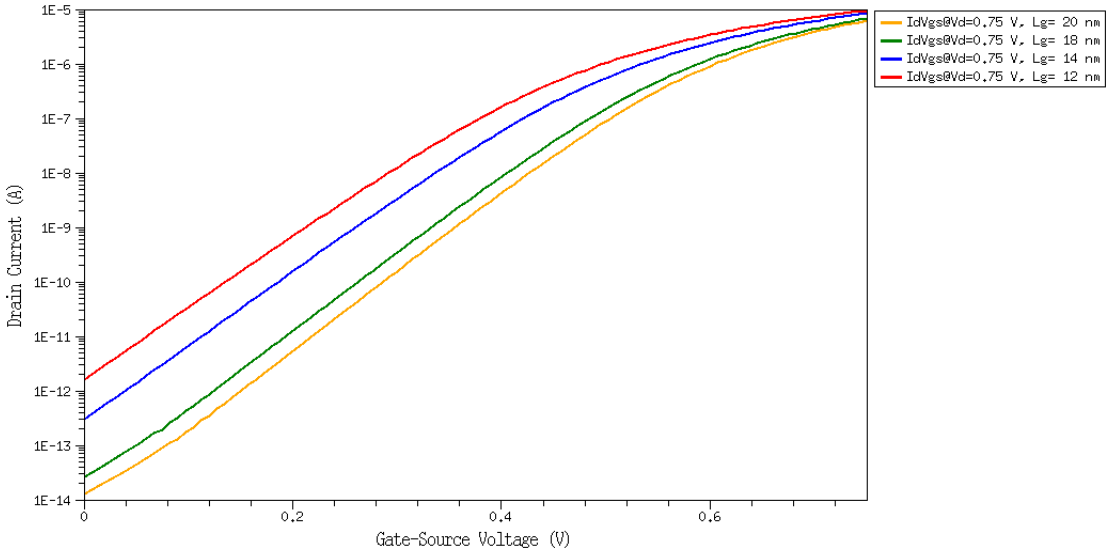


Figure 4.3.4: $I_D - V_{GS}$ characteristic of different channel lengths n-type JL-finFET, in saturation regime.

Considering the figures of merit reported in Tab.4.3.4 for n-type JL-finFET and Tab.4.3.1 for p-type JL-finFET, it can be noticed that as channel length increases, the I_{OFF} is greatly

reduced in the n-type transistor with respect to the p-type one.
The V_{TH} is reduced from 0.60 V to 0.53 V as the channel length gets shorter, while the DIBL doubles the value.
Nevertheless, it has been demonstrated the feasibility and device functionality of the junctionless technology, which was the first important point of this thesis.
The evolution of the current finFET dimensions due to scaling is optimized in such a way that the effective channel width is increased by making the fin height as tall as possible while reducing the fin width (high aspect ratio). This method is exploited because the channel in inversion-mode transistors is created at the interface of the gate dielectric and the silicon layer, so by increasing the aspect ratio of the finFET, it is possible to have a better electrostatic control of the channel and increase the effective channel width, while reducing the fin pitch.
For what concern the JL-finFET, the high aspect ratio is a demerit, because the conduction path is located near the center of the fin, since it operates under bulk conduction rather than channel conduction.
Therefore, the junctionless transistors is subjected to large variation in terms of electrical parameters when changing channel length during fabrication, which is in agreement with the data obtained from the simulations.
Even though the geometry adopted for the JL-finFET is not suitable for its application, the leakage current of junctionless devices is less than the conventional finFET, for each channel length simulated.
However, the drive current of inversion mode finFET is greater than the JL-finFET one, which is consistent with the results of other papers (10; 20).
Nevertheless, the junctionless devices can achieve I_{ON}/I_{OFF} significantly higher, thus establishing the fact that turning off the device by electrostatically depleting the channel of carriers works better than using a revere-biased junction (10).

Despite the fact that the IRDS (30) suggests a supply voltage of 0.75 V for these channel lengths, the V_{DD} has been raised to increase the current I_{ON}, for the JL-finFET structure (Tab.4.3.5). The structure has been simulated with different channel lengths

Junctionless finFET (n-type) V_{DD}= 1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	19.98	19.20	18.33	18.00
I_{OFF} (pA)	3.21	0.64	0.17	0.16
I_{ON}/I_{OFF}	6.22×10^6	2.99×10^7	1.05×10^8	1.15×10^8

Table 4.3.5: I_{ON}, I_{OFF}, I_{ON}/I_{OFF} of different channel lengths n-type bulk JL-finFET.

while keeping constant the dose implanted in the transistor. The reason why the gate length is explored within 10 nm variation for the simulations, is to attenuate the error due to the constant dose implanted in the device under analysis.
Thereafter, it is important to study what happens when the dose implanted in the source and drain pockets is increased for the L_g=20 nm transistor.

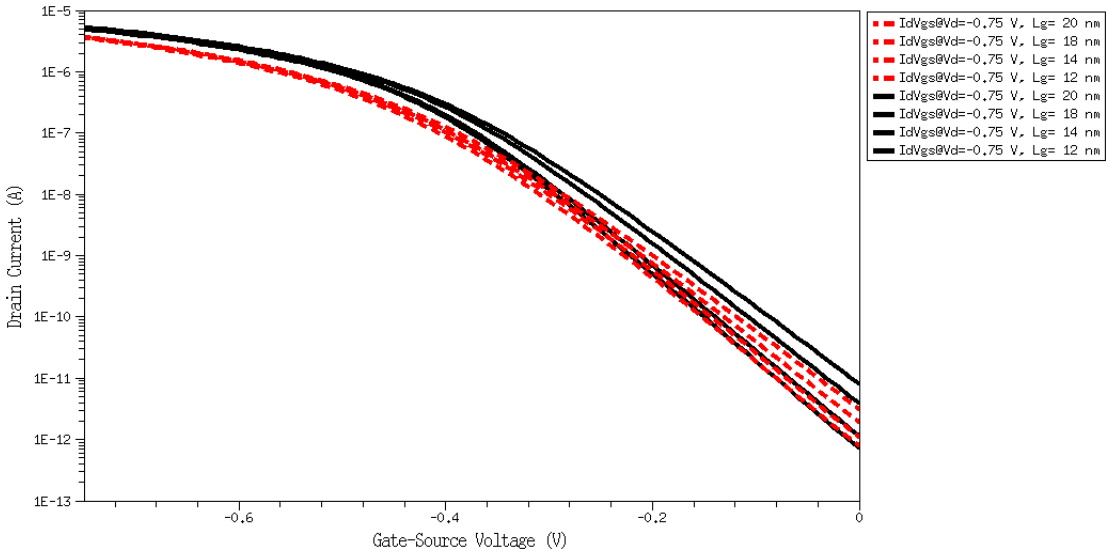


Figure 4.3.5: $I_D - V_{GS}$ characteristic of different channel lengths p-type finFET (black), $I_D - V_{GS}$ characteristic of different channel lengths p-type JL-finFET (red).

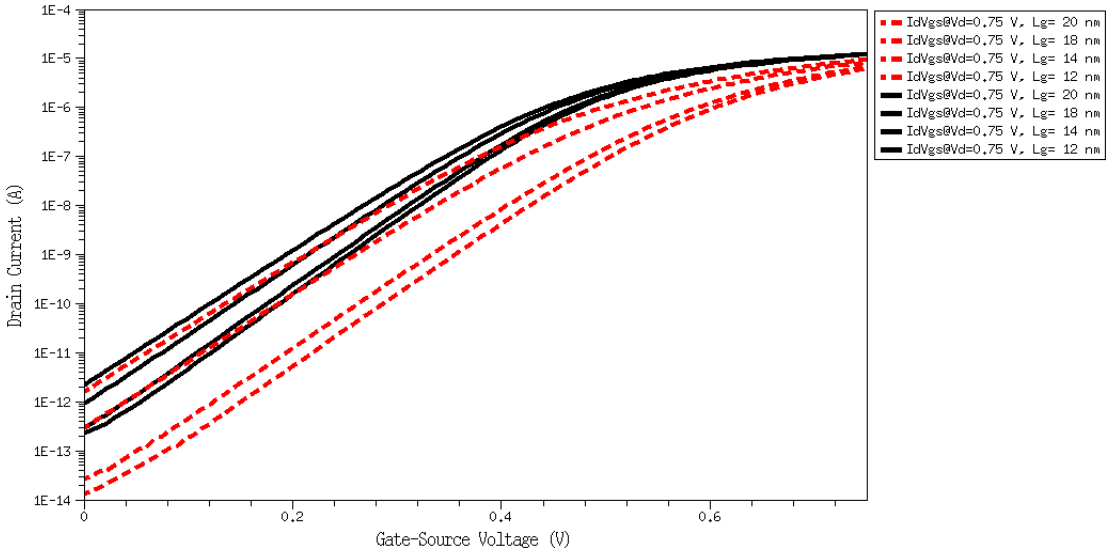


Figure 4.3.6: $I_D - V_{GS}$ characteristic of different channel lengths n-type finFET (black), $I_D - V_{GS}$ characteristic of different channel lengths n-type JL-finFET (red).

This study is carried out to prove that bigger transistor can provide more current with respect to shorter one, due to scaling policy. Therefore, the electrical parameters extracted by the plots obtained by Sentaurus TCAD are reported in Tab.4.3.6 for the n-type JL-finFET. The I_{ON} is improved by 69% as the dose implanted is increased.

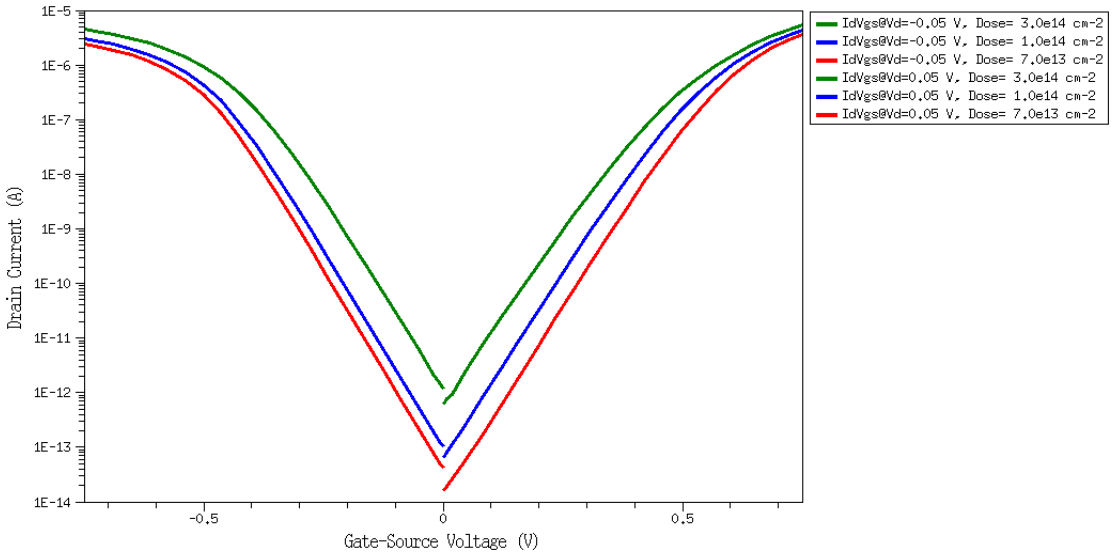


Figure 4.3.7: $I_D - V_{GS}$ characteristic of p-type JL-finFET (left) and n-type JL-finFET (right) (L_g= 20 nm), in linear regime.

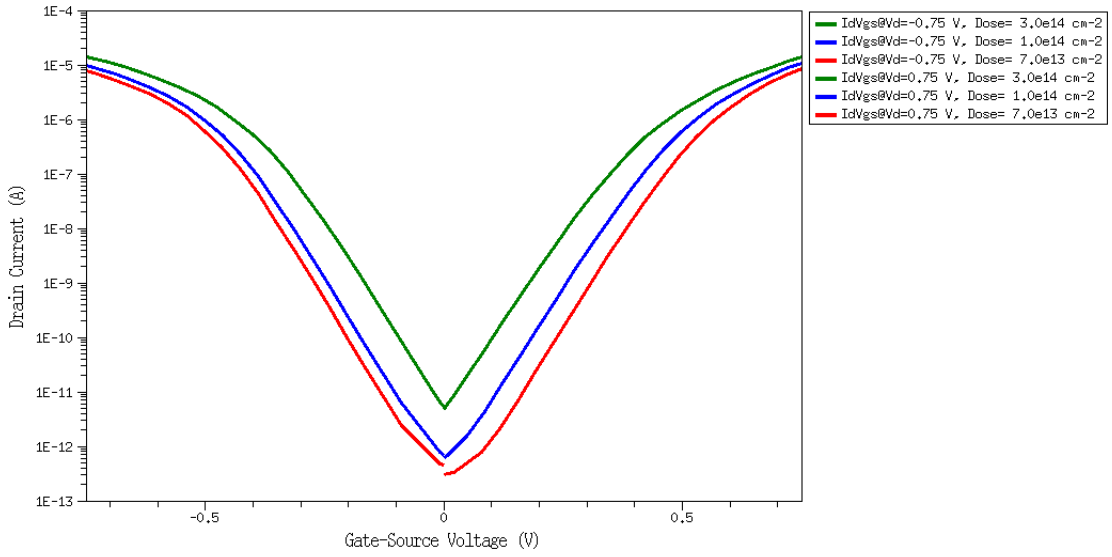


Figure 4.3.8: $I_D - V_{GS}$ characteristic of p-type JL-finFET (left) and n-type JL-finFET (right) (L_g= 20 nm), in saturation regime.

As expected, when the dose implanted in the raised pockets or V_{DD} is increased, the transistor provides higher I_{ON}. However the increase of SCEs affect the overall performance, which lead to worsening the leakage current (I_{OFF}), SS and DIBL.

n-type JL-finFET (L_g=20 nm) V_{DD}= 0.75 V			
Parameters	Parameter Values		
Dose (cm^{-2})	7.0 E13	1.0 E14	3.0 E14
V_{TH} (V)	0.63	0.62	0.59
I_{ON} (µA)	8.64	10.08	14.56
I_{OFF} (pA)	0.31	0.62	4.85
I_{ON}/I_{OFF}	2.81×10^7	1.73×10^7	3.00×10^6
SS (mV/dec)	69.32	74.04	77.40
DIBL (mV/V)	34.32	37.38	40.41

Table 4.3.6: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of n-type bulk JL-finFET with various doses implanted.

4.4 Bulk NSGAAFET

4.4.1 p-type NSGAAFET

The development of nanosheet gate-all-around field effect transistors (NSGAAFET) has been promoted to overcome some limitations of finFET related to scaling. The NSGAAFET provides higher electrostatic channel control and better immunity to short channel effects (SCEs), compared to the fin technology.
The simulation settings for the NSGAAFET are the same of the one employed for the finFETs. This is done to compare the performances between the two technologies while the gate length is shrunk.
The current-voltage characteristics of the p-type NSGAAFET are simulated in linear regime (V_{GS}=[0, -0.75] V, V_{DS}=[0, -0.05] V) and saturation regime (V_{GS}=[0, -0.75] V, V_{DS}= [0, -0.75] V).

The figures of merit related to the p-type NSGAAFET with various gate lengths are reported in the following table:

NSGAAFET (p-type) V_{DD}= -0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	-0.38	-0.38	-0.39	-0.39
I_{ON} (µA)	-3.90	-3.39	-3.19	-3.18
I_{OFF} (pA)	-0.69	-0.42	-0.39	-0.17
I_{ON}/I_{OFF}	5.68×10^6	8.01×10^6	8.12×10^6	1.88×10^7
SS (mV/dec)	77.09	76.18	75.59	69.04
DIBL (mV/V)	47.16	46.97	39.26	35.40

Table 4.4.1: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of different channel lengths p-type NSGAAFET.

As it can be seen from the data extracted from Sentaurus TCAD, the threshold voltage is slightly reduced when the channel shrinks, thus obtaining a higher leakage current.

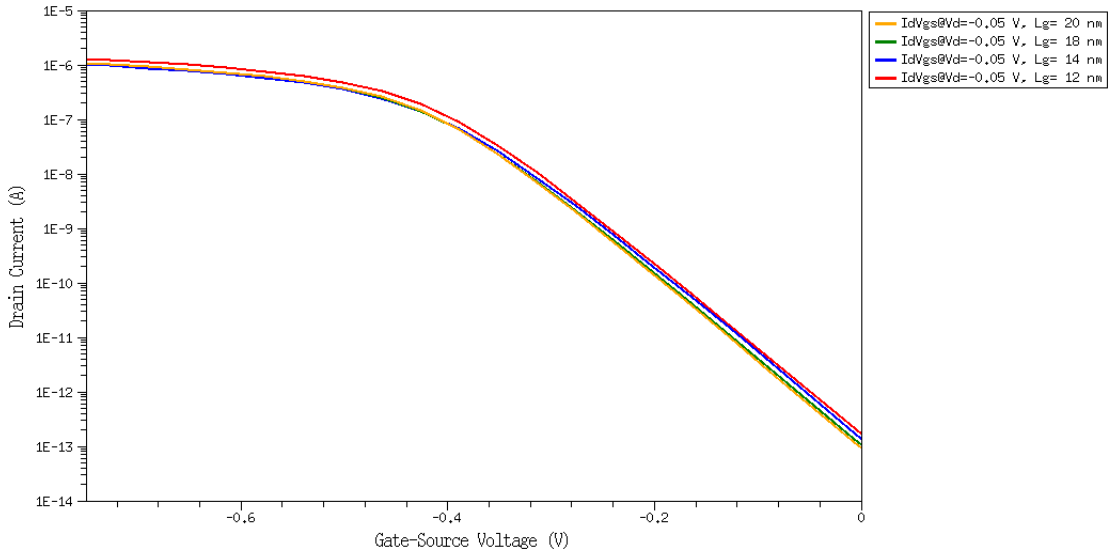


Figure 4.4.1: $I_D - V_{GS}$ characteristic of p-type NSGAAFET with different channel lengths, in linear regime.

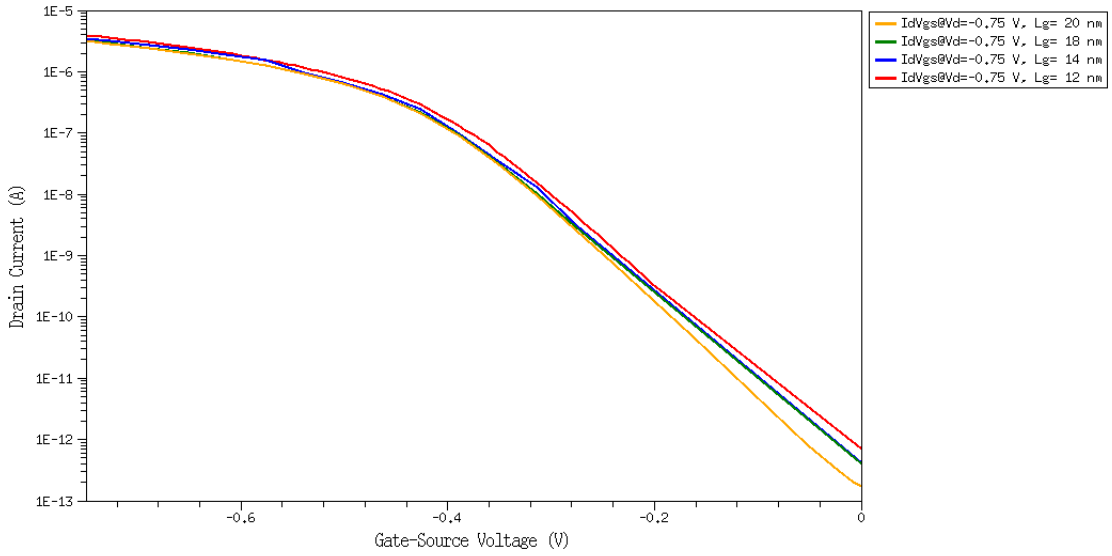


Figure 4.4.2: $I_D - V_{GS}$ characteristic of p-type NSGAAFET with different channel lengths, in saturation regime.

Moreover, it's clear that as the device is scaled down, the parameters such as I_{OFF}, SS, DIBL and I_{ON}/I_{OFF} are worsened.
However, the drive current for long transistors (L_g=20 nm) is not high as expected, when the transistor is turned on. This is because the script written to simulate the 3D structure for different channel lengths exploits the same dose implanted in the device, which is not

correct according to the scaling policy. Therefore, the dose is chosen considering the worst case scenario in terms of lateral diffusion, which occurs when the gate length is the shortest one (L_g=12 nm).
Although the IRDS (30) suggests a supply voltage of -0.75 V for these channel lengths, the V_{DD} has been set up to -1.00 V to increase the current I_{ON}.

NSGAAFET (p-type) V_{DD}= -1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	-7.61	-7.61	-7.22	-6.96
I_{OFF} (pA)	-0.77	-0.47	-0.40	-0.26
I_{ON}/I_{OFF}	9.92×10^{6}	1.62×10^{7}	1.79×10^{7}	2.65×10^{7}

Table 4.4.2: I_{ON}, I_{OFF}, I_{ON}/I_{OFF} of different channel lengths p-type bulk NSGAAFET.

The dose chosen for the NSGAAFET when analysing the behaviour of various channel length devices has been kept constant. This was done to prevent further lateral diffusion for the shortest transistor (L_g=12 nm).
Therefore, if we take the NSGAAFET with L_g=20 nm, the dose implanted in S/D contacts can be increased to further increase the I_{ON} (Tab.4.4.3).

p-type NSGAAFET (L_g=20 nm) V_{DD}= -0.75 V				
Parameters	Parameter Values			
Dose (cm^{-2})	1.0 E13	3.0 E13	7.0 E13	1.0 E14
V_{TH} (V)	-0.40	-0.40	-0.39	-0.39
I_{ON} (µA)	-6.16	-8.85	-10.54	-11.10
I_{OFF} (pA)	-0.18	-0.20	-0.21	-0.22
I_{ON}/I_{OFF}	3.52×10^{7}	4.48×10^{7}	4.99×10^{7}	5.10×10^{7}
SS (mV/dec)	69.04	69.59	69.99	70.18
DIBL (mV/V)	35.42	35.74	36.12	36.43

Table 4.4.3: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of p-type bulk NSGAAFET with various doses implanted.

The drive current is improved by 80% for the p-type transistor. Moreover, when the dose implanted in the raised pockets is increased, the transistor is subjected to lateral dopant redistribution during annealing, which affect the overall performance and the leakage current (I_{OFF}) is worsened.

4.4.2 n-type NSGAAFET

The procedure to simulate the n-type NSGAAFET is the same exploited for the p-type one, apart from the doping used during ion implantation.
The I_D-V_{GS} characteristics in linear and saturation regime are reported in Fig.4.4.3 and Fig.4.3.4 respectively, for different channel lengths. As expected, when shrinking the channel lengths, the performances of the transistor such as V_{TH}, DIBL, SS, I_{OFF} and I_{ON}/I_{OFF} get worse.

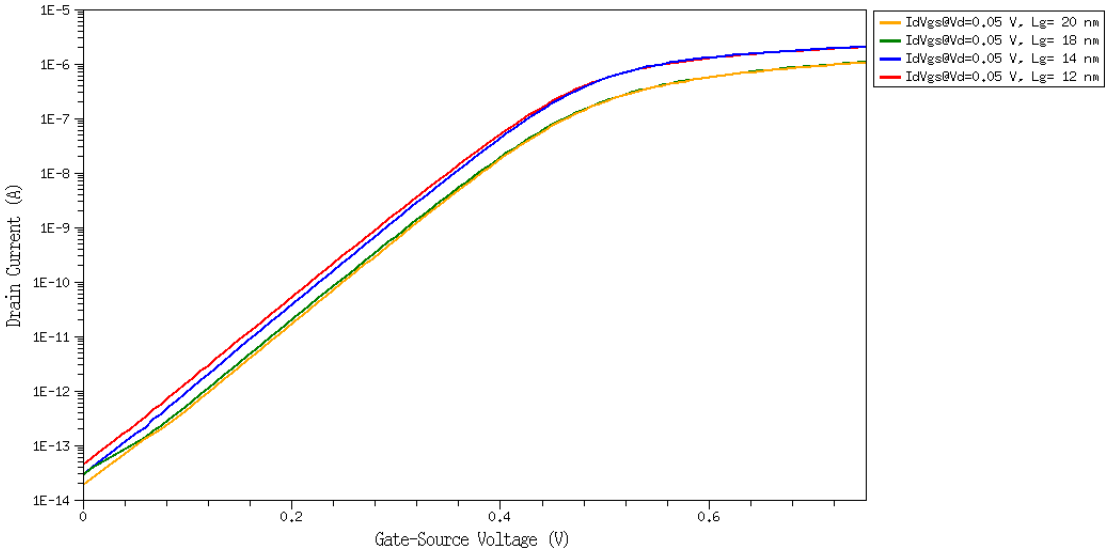


Figure 4.4.3: $I_D - V_{GS}$ characteristic of n-type NSGAAFET with different channel lengths, in linear regime.

The figures of merit of the n-type NSGAAFET are extracted from the data of the I_D-V_{GS} curves for different channel lengths and reported in Tab.4.4.4.

NSGAAFET (n-type) V_{DD}= 0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	0.43	0.44	0.45	0.45
I_{ON} (µA)	5.19	5.11	4.15	3.05
I_{OFF} (pA)	0.11	0.10	7.98 E-2	5.80 E-2
I_{ON}/I_{OFF}	4.86×10^7	5.06×10^7	5.20×10^7	5.26×10^7
SS (mV/dec)	74.60	74.45	73.90	73.38
DIBL (mV/V)	41.02	35.16	34.30	30.27

Table 4.4.4: V_{TH}, I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, SS, DIBL of n-type NSGAAFET with different channel lengths.

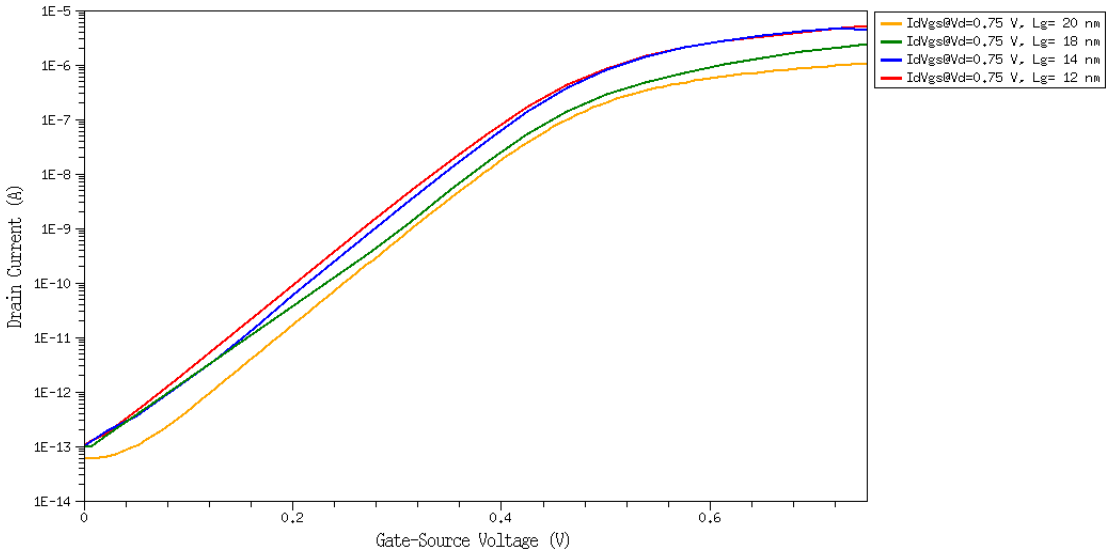


Figure 4.4.4: $I_D - V_{GS}$ characteristic of n-type NSGAAFET with different channel lengths, in saturation regime.

The V_{DD} has been raised to increase the current I_{ON}, for the n-type NSGAAFET structure (Tab.4.4.5).

NSGAAFET (n-type) V_{DD}= 1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	11.65	11.21	11.12	10.88
I_{OFF} (pA)	0.18	0.16	0.15	0.14
I_{ON}/I_{OFF}	6.31×10^7	6.91×10^7	7.55×10^7	7.93×10^7

Table 4.4.5: I_{ON}, I_{OFF}, I_{ON}/I_{OFF} of different channel lengths n-type bulk NSGAAFET.

The same analysis carried out for the dose in p-type NSGAAFET is performed for the n-type device. The current I_{ON} is increased by 149% for the p-type transistor, as the implanted dose gets higher (Tab.4.4.6).Moreover, when the dose implanted in the raised pockets is increased, the transistor is subjected to lateral dopant redistribution during annealing, which affect the overall performance and the leakage current (I_{OFF}) is worsened.

n-type NSGAAFET (L_g=20 nm) V_{DD}= 0.75 V				
Parameters	Parameter Values			
Dose (cm^{-2})	1.0 E13	3.0 E13	7.0 E13	1.0 E14
V_{TH} (V)	0.47	0.47	0.46	0.46
I_{ON} (µA)	8.19	12.98	18.09	20.45
I_{OFF} (pA)	8.23 E-2	0.16	0.28	0.33
I_{ON}/I_{OFF}	9.95×10^7	8.21×10^7	6.50×10^7	6.23×10^7
SS (mV/dec)	73.39	73.42	73.45	73.63
DIBL (mV/V)	30.27	31.35	32.71	33.30

Table 4.4.6: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of n-type bulk NSGAAFET with various doses implanted.

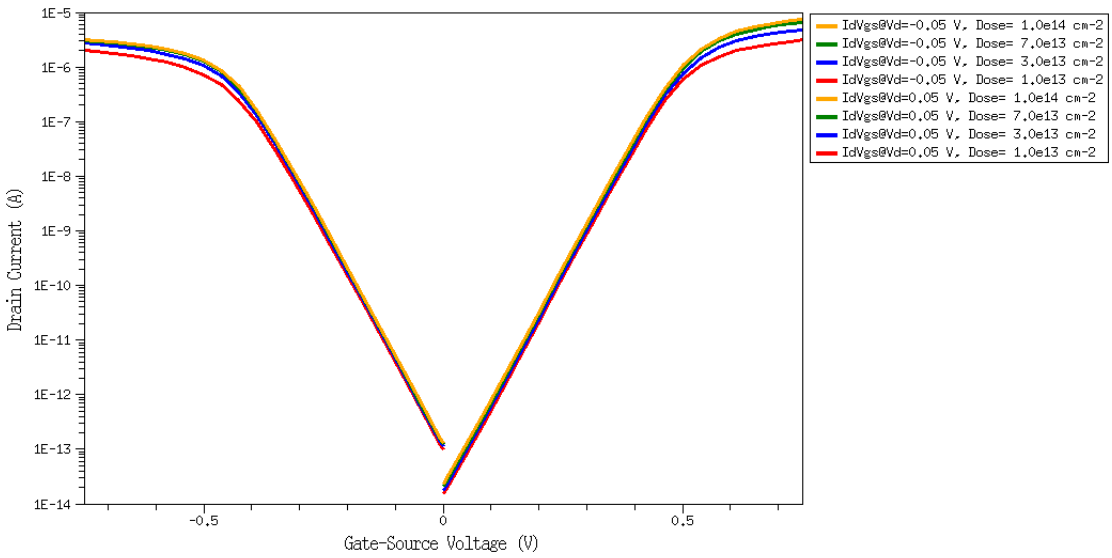


Figure 4.4.5: $I_D - V_{GS}$ characteristic of p-type NSGAAFET (left) and n-type NSGAAFET (right) (L_g= 20 nm), in linear regime.

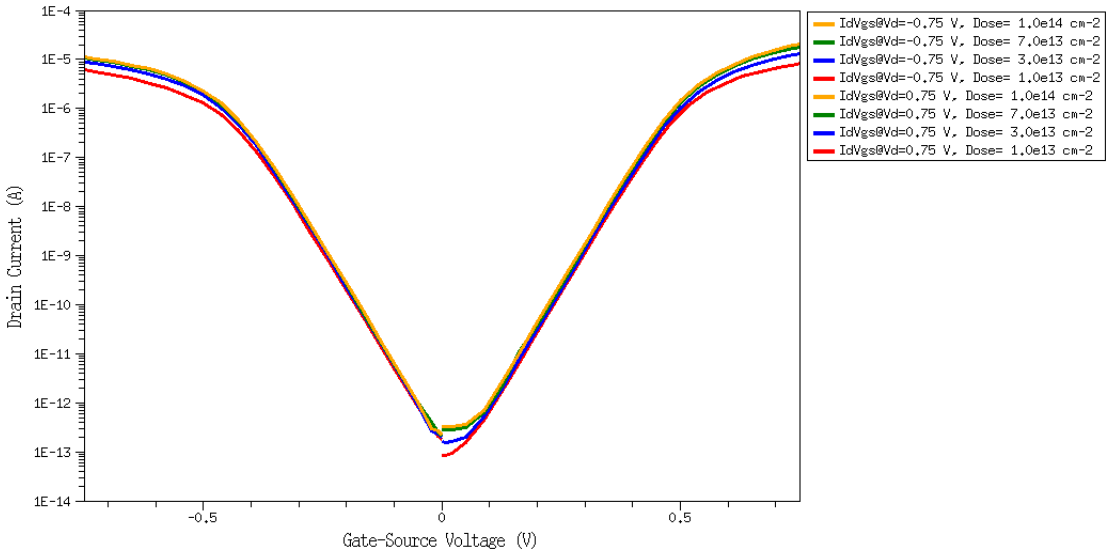


Figure 4.4.6: $I_D - V_{GS}$ characteristic of p-type NSGAAFET and n-type NSGAAFET (right) (L_g= 20 nm), in saturation regime.

It can be noticed from the results obtained, that the n-type NSGAAFET has an overall better performance with respect to the p-type NSGAAFET. This behaviour is expected since the electron mobility is higher than the hole mobility.
Moreover, it can be noticed that the gate-all-around structure provides a better immunity to SCEs. Nevertheless, the I_{ON} in saturation regime is not high compared to what it was obtained in finFET, which is to be expected if the width of the nanosheet is not increased (71).

4.5 Bulk JL-NSGAAFET

4.5.1 p-type JL-NSGAAFET

The junctionless transistor (JLT) has been studied for improving short channel effects for very short channel transistors. The fabrication of junctionless devices is simpler than the existing inversion mode FET, because it is not necessary to employ fast annealing to build the p-n junction S/D profiles (76).
Since the junctionless technology relies on the silicon channel thickness (T_{CH}) and doping concentration to allow its switching capability, the GAA can alleviate the strict requirement of reducing T_{CH}, which is needed to deplete the carriers in the channel.
The script used to simulate the JL-NSGAAFET is the same as the NSGAAFET one, to faithfully compare the behaviour of both devices.
The ranges where the JL-NSGAAFET is tested are: V_{GS}=-0.75 V and V_{DS}=-0.75 V, V_{GS}=-0.75 V and V_{DS}=-0.05 V, for saturation and linear regime respectively.
The data extracted from the plots (Fig. 4.5.1-4.5.2) are reported in the Tab.4.5.1.

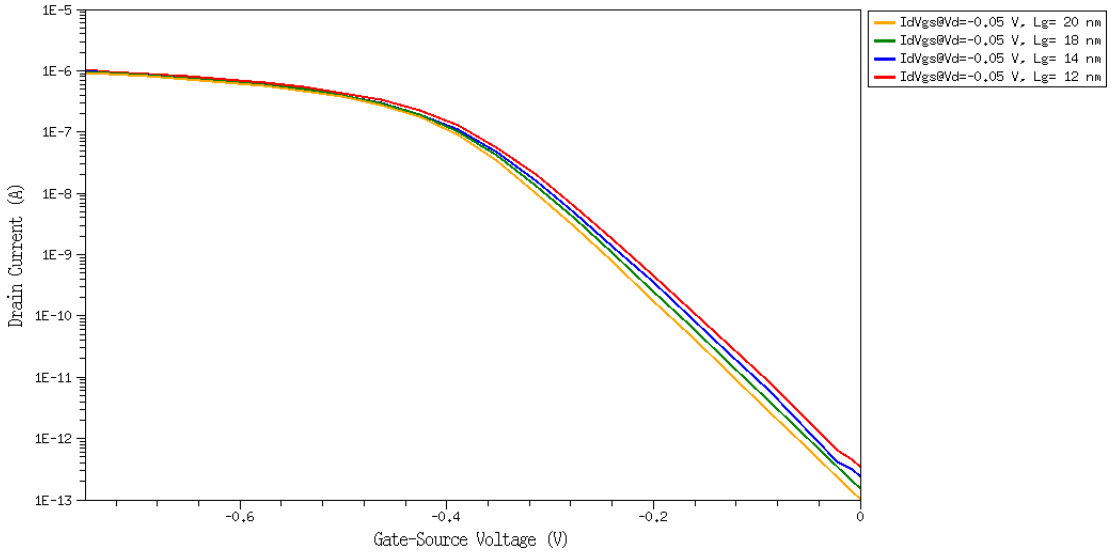


Figure 4.5.1: $I_D - V_{GS}$ characteristic of p-type JL-NSGAAFET with different channel lengths, in linear regime.

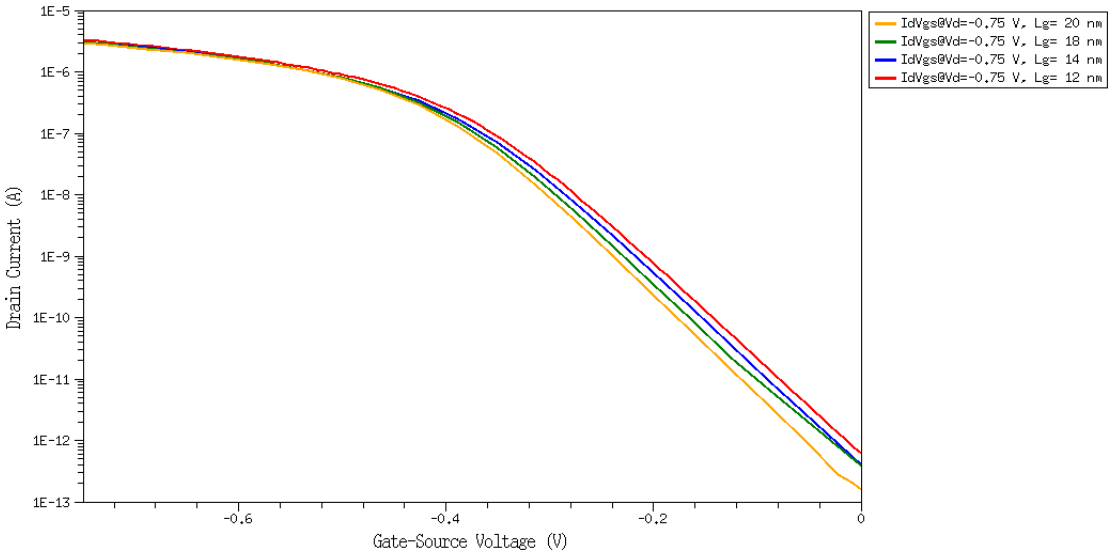


Figure 4.5.2: $I_D - V_{GS}$ characteristic of p-type JL-NSGAAFET with different channel lengths, in saturation regime.

Junctionless NSGAAFET (p-type) V_{DD}= -0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	-0.35	-0.35	-0.36	-0.36
I_{ON} (µA)	-3.30	-3.10	-3.06	-2.94
I_{OFF} (pA)	-0.61	-0.40	-0.38	-0.16
I_{ON}/I_{OFF}	5.38×10^6	7.77×10^6	8.14×10^6	1.86×10^7
SS (mV/dec)	66.50	65.63	63.90	62.91
DIBL (mV/V)	31.70	29.41	28.85	20.60

Table 4.5.1: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of different channel lengths p-type JL-NSGAAFET.

The V_{TH} does not change much, as the channel shrinks, which is a good behaviour at nanoscale. The current I_{ON} and I_{OFF} are similar to what obtained for the p-type NSGAAFET.
Despite the fact that the IRDS (30) suggests a supply voltage of -0.75 V for these channel lengths, the V_{DD} has been raised to increase the current I_{ON} (Tab.4.5.2).

To improve the drive current without affecting the channel doping, an additional S/D implantation is performed to limit the resistance of the contacts.
The simulation settings implemented in Sentaurus Device to analyse the benefits of this process are the same as what is used in the script for the various channel length devices explored before. The electrical parameters extracted from the plot of p-type JL-NSGAAFET are reported in Tab.4.5.3. It can be noticed that the drive current of p-type is increased by 69%, when the doping concentration is increased.

Junctionless NSGAAFET (p-type) V_{DD}= -1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	-6.36	-6.00	-5.88	-5.56
I_{OFF} (pA)	-0.61	-0.41	-0.34	-0.22
I_{ON}/I_{OFF}	1.05×10^7	1.45×10^7	1.71×10^7	2.55×10^7

Table 4.5.2: I_{ON}, I_{OFF}, I_{ON}/I_{OFF} of different channel lengths p-type bulk JL-NSGAAFET.

p-type Junctionless NSGAAFET (L_g=20 nm) V_{DD}= -0.75 V				
Parameters	Parameter Values			
Dose (cm^{-2})	1.0 E13	3.0 E13	7.0 E13	1.0 E14
V_{TH} (V)	-0.37	-0.37	-0.36	-0.36
I_{ON} (µA)	-3.00	-3.79	-4.79	-5.07
I_{OFF} (pA)	-0.18	-0.20	-0.22	-0.23
I_{ON}/I_{OFF}	1.63×10^7	1.88×10^7	2.17×10^7	2.25×10^7
SS (mV/dec)	62.46	62.78	63.04	63.44
DIBL (mV/V)	21.21	21.65	22.15	22.22

Table 4.5.3: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of p-type bulk JL-NSGAAFET with various doses implanted.

4.5.2 n-type JL-NSGAAFET

The I_D-V_{GS} characteristics in linear and saturation regime is reported in Fig.4.5.3 and Fig.4.5.4 respectively, for different channel lengths. All the other critical dimensions and processing conditions are kept constant, so that the only difference lies in L_g for fair comparison.
As expected, when shrinking the channel lengths, the performances of the transistor such as V_{TH}, DIBL, SS, I_{OFF} and I_{ON}/I_{OFF} get worse.

All the figures of merit related to the n-type JL-NSGAAFET with various gate lengths are reported in table 4.5.4. Although the IRDS (30) suggests a supply voltage of 0.75 V for these channel lengths, the V_{DD} has been raised to increase the current I_{ON}. The new setting has been applied to the JL-NSGAAFET structure, which have different channel lengths. To emulate the process fabrication performed in the industry, the gate material chosen for p-type and n-type JL-NSGAAFET is TiN (5) . Since the gate workfunction is set to 4.66 eV, the doping concentration for junctionless technology must be lower than 10^{19} to ensure a proper switching of the transistor. The consequence of this is that the drain current is reduced. However, it allows to employ a feasible metal gate workfunction and it counteracts the increase of sensitivity to parameters, such as V_{TH}, SS and DIBL, which is related to the high dopant concentration (87).

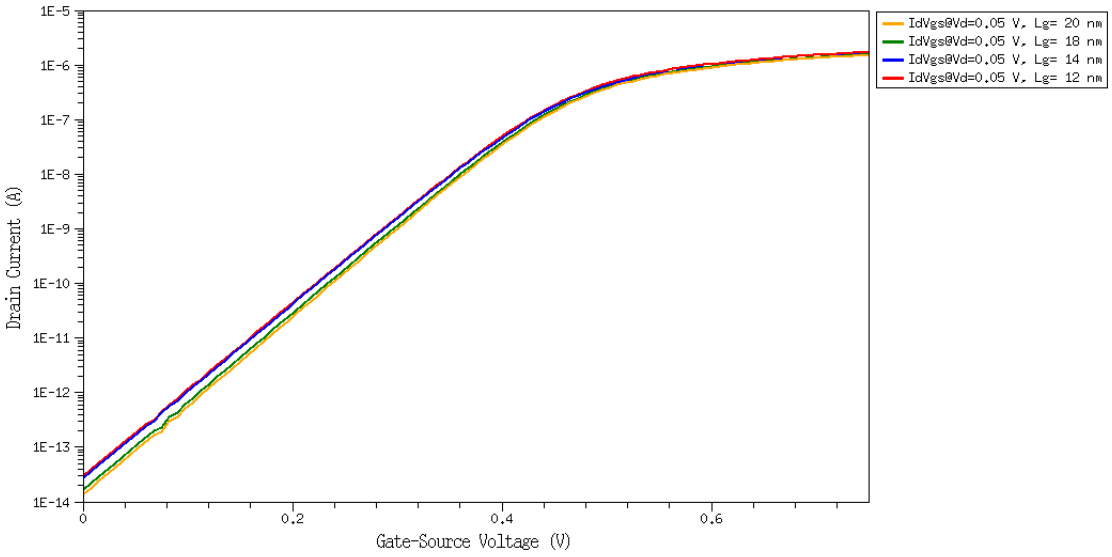


Figure 4.5.3: $I_D - V_{GS}$ characteristic of different channel lengths n-type JL-NSGAAFET, in linear regime.

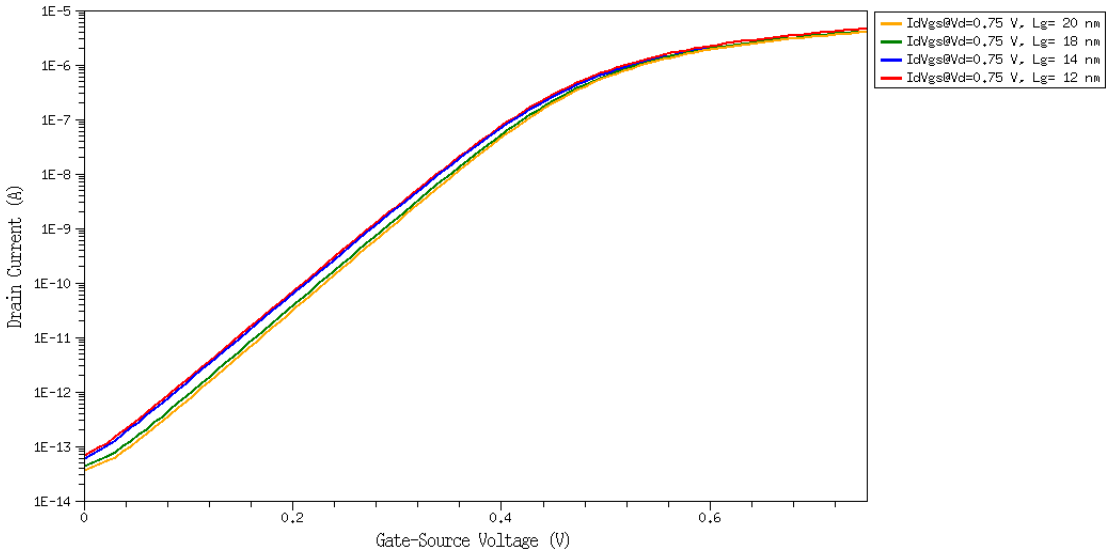


Figure 4.5.4: $I_D - V_{GS}$ characteristic of different channel lengths n-type JL-NSGAAFET, in saturation regime.

A higher doping concentration could improve the I_{ON}, thanks to the large number of mobile carriers devoted to the total saturation current. However, when the channel concentration (N_{CH}) exceed a critical point where full depletion of the channel does not occur, the feasibility of JLT is compromised (88).

Junctionless NSGAAFET (n-type) V_{DD}= 0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	0.42	0.43	0.43	0.43
I_{ON} (µA)	4.62	4.16	4.15	4.00
I_{OFF} (pA)	6.83 E-2	5.88 E-2	4.37 E-2	3.69 E-2
I_{ON}/I_{OFF}	6.75×10^{7}	7.00×10^{7}	9.50×10^{7}	1.08×10^{8}
SS (mV/dec)	63.28	63.07	61.90	61.52
DIBL (mV/V)	22.01	21.35	17.71	16.62

Table 4.5.4: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of different channel lengths n-type bulk JL-NSGAAFET.

Junctionless NSGAAFET (n-type) V_{DD}= 1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	9.00	8.53	7.98	7.63
I_{OFF} (pA)	0.12	0.11	9.79 E-2	9.23 E-2
I_{ON}/I_{OFF}	7.31×10^{7}	7.46×10^{7}	8.15×10^{7}	8.26×10^{7}

Table 4.5.5: I_{ON}, I_{OFF}, I_{ON}/I_{OFF} of different channel lengths n-type bulk JL-NSGAAFET.

To improve the drive current without affecting the channel doping, an additional S/D implantation is performed to limit the resistance of the contacts.
The simulation settings implemented in Sentaurus Device to analyse the benefits of this process are the same as what is used in the script for the various channel length devices explored before.
Thereafter, the curves obtained with various dose implanted in the junctionless transistors are plotted for linear and saturation regime. The electrical parameters extracted from the plots of n-type JL-NSGAAFET are reported in Tab.4.5.6. It can be noticed that the drive current of n-type JL-NSGAAFET is increased by 59%, when the doping concentration is increased. Nevertheless, it becomes more difficult to deplete the channel, hence V_{TH} decreases (81; 82).
Although the subthreshold slope is slightly degraded as the channel length gets shorter, it is still kept under 65 mV/dec (near thermionic limit) at L_g=12 nm. Moreover, the deviation is not prominent owing to the strong gate controllability of the gate-all-around structure and effectively suppressed I_{OFF} (89).
Apart from the result at L_g=[18,20] nm, the I_{ON} in the junctionless devices is smaller, if compared to the conventional NSGAAFET, and it is a well-known characteristic resulting from the large impurity scattering which comes from the high doping concentrations throughout the channel.
The plots in Fig.4.5.7-4.5.8 are reported to show the differences between the junctionless (in red) and inversion mode NSGAAFET (in black).

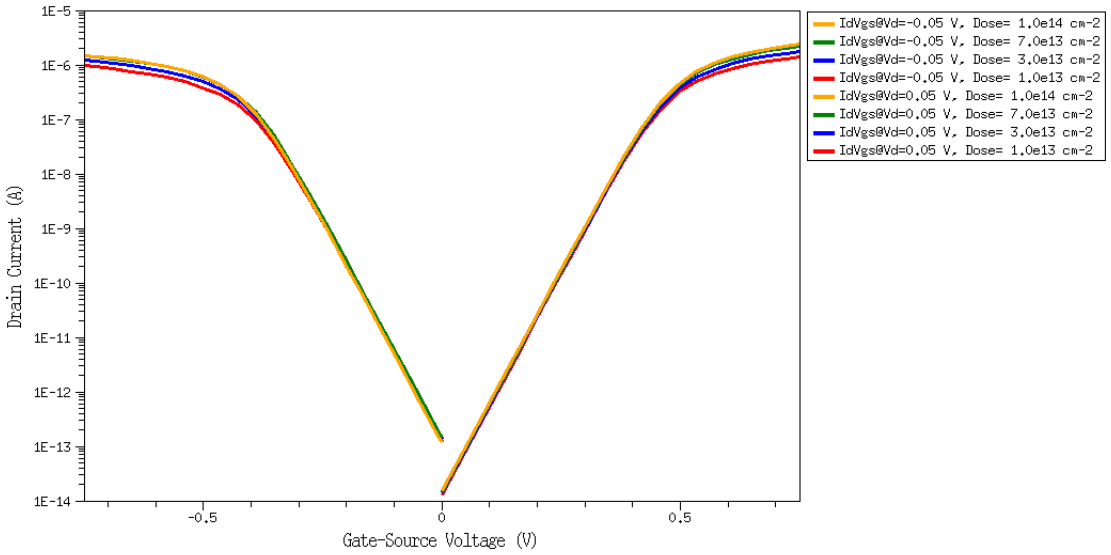


Figure 4.5.5: $I_D - V_{GS}$ characteristic of p-type JL-NSGAAFET (left) and n-type JL-NSGAAFET (right) (L_g= 20 nm), in linear regime.

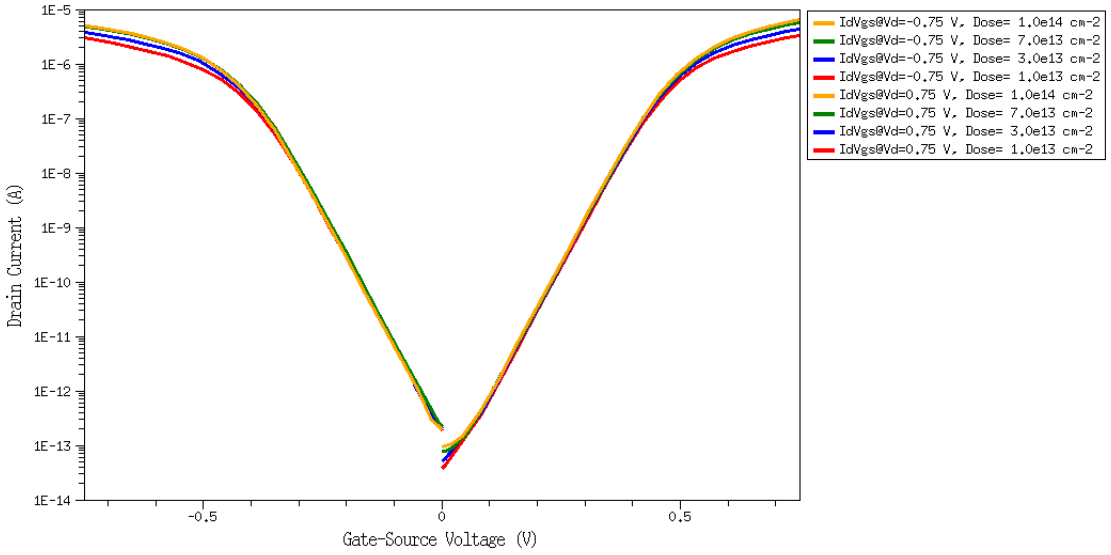


Figure 4.5.6: $I_D - V_{GS}$ characteristic of p-type JL-NSGAAFET and n-type JL-NSGAAFET (right) (L_g= 20 nm), in saturation regime.

The inversion mode and junctionless NSGAAFET have similar characteristics both for p-type and n-type. On the other hand, while the JL-NSGAAFET shows lower I_{OFF} at V_{GS}=0 V, the NSGAAFET has higher drain saturation current at V_{GS}=V_{DD} than the others.

n-type Junctionless NSGAAFET (L_g=20 nm) V_{DD}= 0.75 V				
Parameters	Parameter Values			
Dose (cm^{-2})	1.0 E13	3.0 E13	7.0 E13	1.0 E14
V_{TH} (V)	0.45	0.44	0.44	0.43
I_{ON} (µA)	4.02	4.29	5.69	6.40
I_{OFF} (pA)	3.87 E-2	5.20 E-2	7.70 E-2	9.36 E-2
I_{ON}/I_{OFF}	1.04×10^{8}	8.25×10^{7}	7.40×10^{7}	6.84×10^{7}
SS (mV/dec)	61.74	61.74	61.75	61.77
DIBL (mV/V)	16.71	17.10	17.81	17.92

Table 4.5.6: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of n-type bulk JL-NSGAAFET with various doses implanted.

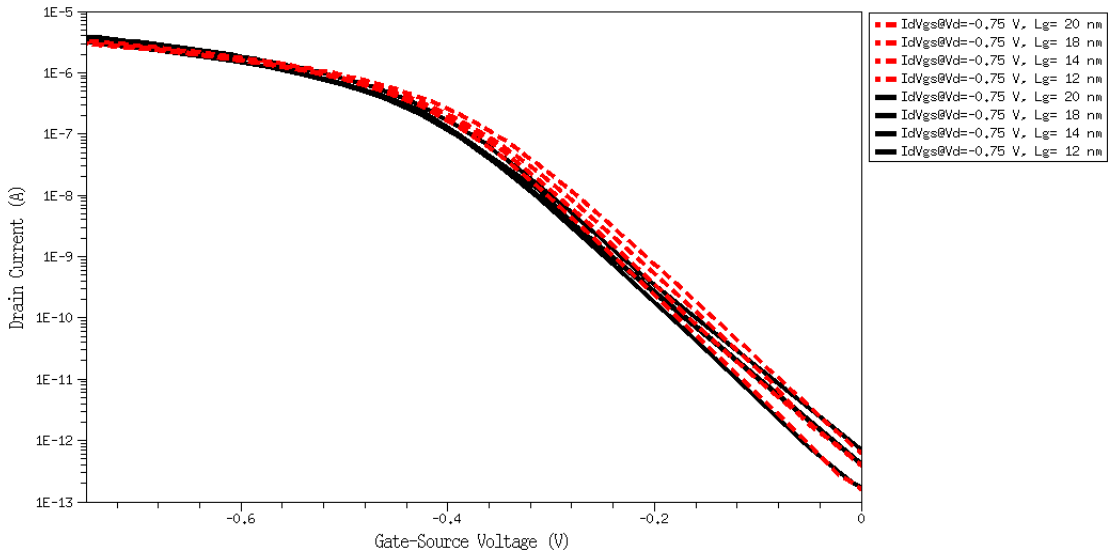


Figure 4.5.7: $I_D - V_{GS}$ characteristic of different channel lengths p-type NSGAAFET (black), $I_D - V_{GS}$ characteristic of different channel lengths p-type JL-NSGAAFET (red).

However, the junctionless devices have a near-ideal subthreshold slope, close to 60 mV/dec at 300 K (known as thermionic limit) and extremely low leakage currents (10). The junctionless NSGAAFET simulated in this section has only one suspended channel, to compare the results with others published in the literature.
Since the JL-NSGAAFET has only one suspended channel instead of three vertical stacked channels like the NSGAAFET structure, the drive current of the JLT is expected to be lowered than the inversion mode transistor.

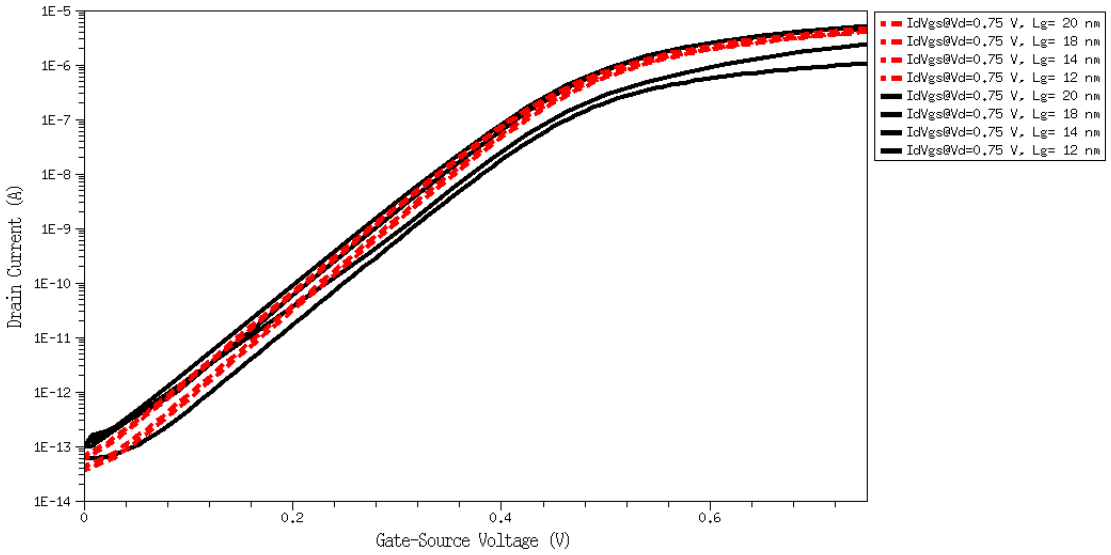


Figure 4.5.8: $I_D - V_{GS}$ characteristic of different channel lengths n-type NSGAAFET (black), $I_D - V_{GS}$ characteristic of different channel lengths n-type JL-NSGAAFET (red).

Gate-all-around junctionless transistor papers have been reported in the literature, which have treated multi-channel junctionless devices (76; 79). However, the first one (76) has simulated the 3D device without considering any fabrication aspect, while the latter (79) has exploited Bosch process to build the structures. Nevertheless, the shape of the suspended channels made by deep reactive-ion etching (DRIE) are not regular and uniform between each others. Moreover, this transistor is simulated in depletion-mode, which means that the device is normally on at zero gate-source voltage.

4.5.3 Vertically stacked JL-NSGAAFET

Until now, the JL-NSGAAFET has been simulated considering only one suspended channel, due to its dependency on doping concentration. In literature, the data available for this type of technology has been obtained by testing one channel, so to compare the results reported in this thesis, the design choice has taken this characteristic into account.
The feasibility of three vertical stacked nanosheet in junctionless mode (76) has been analysed, while considering a uniform and constant doping concentration along each channels, which in reality it's not achievable.
Therefore, the same fabrication steps employed for the NSGAAFET to make the three suspended channels has been adopted to the junctionless one, to simulate if the requirement of constant and uniform doping concentration is strictly required to implement a working device.
According to the IRDS (30), the voltage ranges for these channel lengths in saturation and linear regime are V_{GS}=0.75 V, V_{DS}=0.75 V and V_{GS}=0.75 V, V_{DS}=0.05 V, respectively. For duality, the p-type transistors have opposite polarity for what concern the voltages applied to the device.

Junctionless NSGAAFET (n-type) V_{DD}= 0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	0.41	0.41	0.42	0.42
I_{ON} (µA)	10.99	10.74	10.81	10.87
I_{OFF} (pA)	0.29	0.20	0.12	0.10
I_{ON}/I_{OFF}	3.77×10^7	5.50×10^7	8.83×10^7	1.05×10^8
SS (mV/dec)	64.66	63.58	62.24	61.84
DIBL (mV/V)	26.78	25.43	23.74	22.41

Table 4.5.7: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of n-type bulk three-stacked channels JL-NSGAAFET.

There is an improvement for the I_{ON}, which is expected since three channels are now vertically stacked. Indeed, the plots obtained by simulating the 3D structure show the drive current improvement of about 175%.
The supply voltage has been raised of 0.25 V to increase the current provided by the device. The I_{ON} current at V_{GS}=1 V in saturation regime is around 20 µA, while the I_{OFF} tends to slightly increase (Tab.4.5.8).

The same analysis has been performed for the p-type JL-NSGAAFET to test its behaviour.
There is an improvement for the I_{ON}, which is expected since three channels are now vertically stacked. Indeed, the plots obtained by simulating the 3D structure show the drive current improvement of about 240%.
The p-type transistor is providing the same amount of current of the n-type one, even though the electron mobility is higher than the hole mobility. The reason for this lies

Junctionless NSGAAFET (n-type) V_{DD}= 1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	20.36	19.81	20.14	19.46
I_{OFF} (pA)	0.40	0.30	0.23	0.21
I_{ON}/I_{OFF}	5.07×10^7	6.61×10^7	8.64×10^7	9.31×10^7

Table 4.5.8: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of n-type bulk three-stacked channels JL-NSGAAFET.

in the the gate workfunction ($q\phi_{TiN}$= 4.66 eV) employed for the transistor. It allows a greater current as showed in (39; 70), however the depletion of carriers is worsened due to the $q\phi_{TiN}$ compared to the n-type transistor. Indeed, the V_{TH} is lower than the n-type counterpart, therefore I_{OFF} extracted from the plots for the p-type device is higher of one order of magnitude, as reported in Tab.4.5.9.

The supply voltage for p-type JL-NSGAAFET has been changed to -1.00 V (Tab.4.5.10),

Junctionless NSGAAFET (p-type) V_{DD}= -0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	-0.32	-0.33	-0.33	-0.34
I_{ON} (µA)	-11.21	-10.94	-10.25	-9.99
I_{OFF} (pA)	-6.25	-4.38	-1.45	-1.00
I_{ON}/I_{OFF}	1.79×10^6	2.50×10^6	7.05×10^6	9.96×10^6
SS (mV/dec)	68.80	68.09	64.42	63.97
DIBL (mV/V)	33.53	32.51	31.58	30.69

Table 4.5.9: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of p-type bulk three-stacked channels JL-NSGAAFET.

to increase the drive current provided by the device. The leakage current is slightly increased however, the improvement of I_{ON} and the ratio I_{ON}/I_{OFF} makes the effort worth it. The junctionless devices aren't subjected to reliability problem if lateral diffusion occurs, since they have uniform doping for their entire structure. However, since it has been adopted a bulk fabrication with STI, the high dose implanted during the fabrication of bulk structure with STI would cause a high leakage current flowing through the substrate.

Therefore, setting the concentration within the transistors to control better the dopant redistribution, the current provided by the p-type and n-type JL-NSGAAFET greatly improve. The channel concentration has been set up to 5.0e18 cm^{-3} to allow a full depletion of the channel, when the transistor is switched-off. The source and drain contacts have been initialized with 1.0e21 cm^{-3} to limit the resistance and provide an higher current. To avoid the spreading of dopants during diffusion, the bulk has to be implanted with a dose which leads to a concentration of 2.0e18 cm^{-3}, thus controlling the leakage current under

Junctionless NSGAAFET (p-type) V_{DD}= -1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	-18.77	-18.50	-17.54	-17.28
I_{OFF} (pA)	-7.34	-5.17	-1.64	-1.17
I_{ON}/I_{OFF}	2.56×10^6	3.58×10^6	1.07×10^7	1.47×10^7

Table 4.5.10: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of p-type bulk three-stacked channels JL-NSGAAFET.

a certain threshold.
The I_{ON} current extracted from the plots (Fig.4.5.9-4.5.10) has reached almost 100 µA for the transistors, as reported in Tab.4.5.13-4.5.14. The supply voltage has been raised

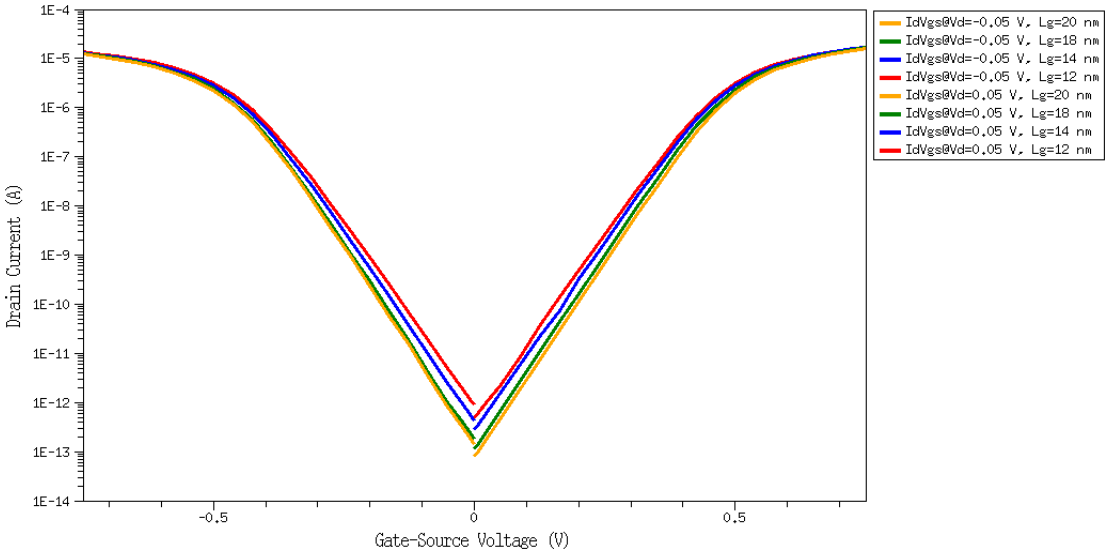


Figure 4.5.9: $I_D - V_{GS}$ characteristic of p-type JL-NSGAAFET (left) and n-type JL-NSGAAFET (right) with varying channel lengths, in linear regime.

to increase the I_{ON} provided by the devices. From the data extracted, the current has improved of 113% and 107% for the n-type and p-type transistor, respectively.

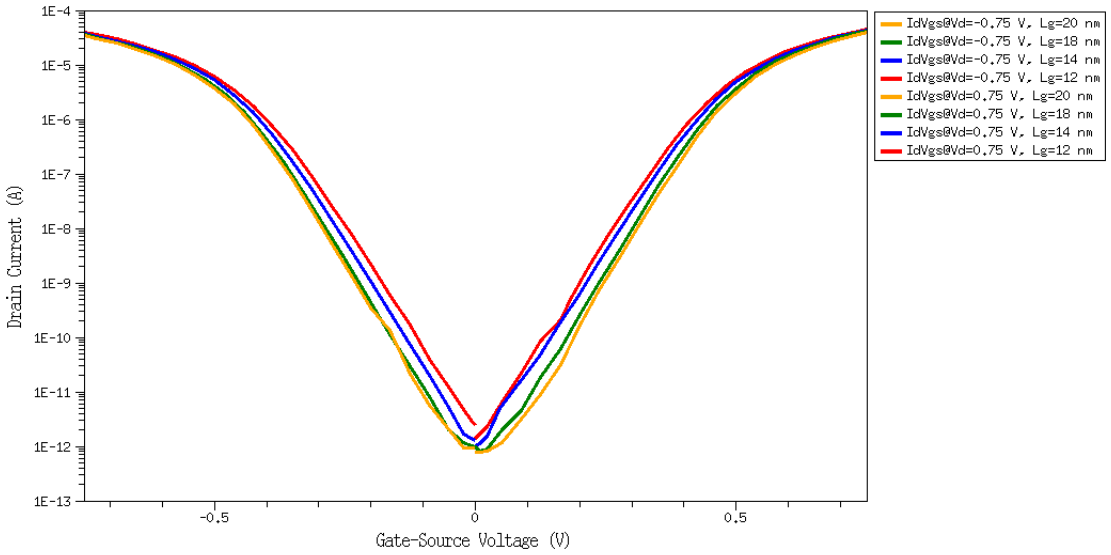


Figure 4.5.10: $I_D - V_{GS}$ characteristic of p-type JL-NSGAAFET and n-type JL-NSGAAFET (right) with varying channel lengths, in saturation regime.

Junctionless NSGAAFET (n-type) V_{DD}= 0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	0.45	0.46	0.47	0.48
I_{ON} (µA)	45.14	43.73	42.26	40.23
I_{OFF} (pA)	1.38	1.03	0.99	0.77
I_{ON}/I_{OFF}	3.28×10^7	4.23×10^7	4.27×10^7	5.23×10^7
SS (mV/dec)	67.29	63.37	62.94	62.69
DIBL (mV/V)	22.64	21.77	20.28	20.48

Table 4.5.11: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of n-type bulk three-stacked channels JL-NSGAAFET, with concentration configured.

Junctionless NSGAAFET (p-type) V_{DD}= -0.75 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
V_{TH} (V)	-0.43	-0.44	-0.45	-0.45
I_{ON} (µA)	-39.27	-37.26	-35.51	-34.57
I_{OFF} (pA)	-2.37	-1.26	-0.98	-0.93
I_{ON}/I_{OFF}	1.66×10^7	2.99×10^7	3.62×10^7	3.70×10^7
SS (mV/dec)	68.10	65.59	63.22	62.66
DIBL (mV/V)	32.93	31.79	28.37	27.65

Table 4.5.12: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of p-type bulk three-stacked channels JL-NSGAAFET, with concentration configured.

Junctionless NSGAAFET (n-type) V_{DD}= 1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	96.13	95.92	98.96	96.67
I_{OFF} (pA)	1.75	1.36	0.93	0.89
I_{ON}/I_{OFF}	5.51×10^7	7.06×10^7	1.07×10^8	1.08×10^8

Table 4.5.13: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of n-type bulk three-stacked channels JL-NSGAAFET, with concentration configured.

Junctionless NSGAAFET (p-type) V_{DD}= -1.00 V				
Parameters	Parameter Values			
L_g (nm)	12	14	18	20
I_{ON} (µA)	-81.07	-78.62	-80.84	-81.10
I_{OFF} (pA)	-2.90	-1.34	-1.19	-0.95
I_{ON}/I_{OFF}	2.79×10^7	5.87×10^7	6.77×10^7	8.54×10^7

Table 4.5.14: V_{TH}, SS, DIBL, I_{ON}/I_{OFF} of p-type bulk three-stacked channels JL-NSGAAFET, with concentration configured.

Chapter 5

Conclusions and Future works

This thesis aimed to cover different aspects related to the current technology, from the fabrication to the electrical performance point of view, when the channel length of transistors is shrunk.
The starting point (Chapter 2) was to provide an overview of the transistor and its limit. The junctionless technology was introduced as an alternative solution to the present inversion mode transistors, to overcome SCEs.
In Chapter 3, fabrication processes for JL-finFET and JL-NSGAAFET are proposed and simulated with Sentaurus TCAD (sprocess), while highlighting the differences and similarities with conventional 3D transistors. The absence of junctions between channel and S/D, has simplified the process steps required to fabricate transistors, at the nanoscale.
The electrical performances of junctionless and inversion mode 3D FETs are compared, and it is shown the functionality of the junctionless devices while varying gate length and dose implanted in S/D (Chapter 4). The data extracted from the electrical characteristics obtained by means of TCAD simulations (8) have proved that the junctionless transistors have a near-ideal subthreshold slope, low DIBL and extremely low leakage currents, if compared to the corresponding inversion mode based technologies. In this thesis, the moderate dopant concentration ($\sim 10^{18}$ cm^{-3}) employed for the JLT channel is proved to enhance the I_{ON}/I_{OFF} and reduce the sensitivity to variation in parameters as demonstrated in (87), and allow to deplete the channel using common gate materials (TiN).
Nevertheless, the drain current provided by this type of technology is lower than conventional MOSFETs. To improve the I_{ON} of junctionless multigate structures, the use of additional source and drain doping is employed (86), so that the parasitic contact resistances are furtherly reduced.
From the results obtained throughout the thesis, it can be concluded that the JLT, in the currently analysed structure on the basis of literature supporting works, is suitable for low standby technology power (LSTP), because of the really low leakage current (I_{OFF}). The JL-NSGAAFET threshold voltage has varied at most within 30 mV, in the overall range of channel lengths devices analysed.
Instead, the simulated inversion mode transistors has provided higher current so it can be exploited for low power applications.
For future works, the actual fabrication of the junctionless transistors in the industry

using the proposed process steps might provide a better comprehension of how the device works in reality. The investigation of new gate materials could improve the junctionless devices and allow to deplete more efficiently carriers from the channel. Replacing the silicon semiconductor material with alternative material like GaN may contribute to enhance the electrical performances of devices.
The junctionless devices built on SOI wafers are expected to provide better electrical performance because of limited parasitics and lowered I_{OFF}, so it could be interested to study the behaviour of such structures.
A possible application of JLTs in the near future, might be the use of this technology for the manufacturing of memories, since the reduced fabrication complexity due to the absence of junctions and low leakage currents, are crucial requirements for these types of devices.

Appendix A

Synopsys Sentaurus TCAD Codes

A.1 n-type JL-finFET sprocess file

```
math coord.ucs

math numThreads=4
AdvancedCalibration 2017.09

pdbSet Mechanics StressRelaxFactor 1

# Solver Enhancement
pdbSet Math diffuse 3D ILS.hpc.mode 4
# turn off stress relaxation after depo/etch
pdbSet Mechanics EtchDepoRelax 0

# meshing parameters
mgoals resolution= 1.0/3.0 accuracy= 1e-4
pdbSet Grid SnMesh max.box.angle.3d 175
grid set.min.normal.size= 0.005/1.0 \
 set.normal.growth.ratio.3d= 2.0 \
 set.min.edge= 1e-7 set.max.points= 1000000 \
 set.max.neighbor.ratio= 1e6

#------------------------------------------------------
# Structure parameters, [um]
set H        0.06                ;# Fin exposure
set STI      0.02              ;# STI
set Hfin     [expr ($H - $STI)]    ;# Fin height

set HalfLg   [expr (@Lg@*0.5)]     ;# Half gate length
set Tox      0.002                 ;# Total thickness of gate insulator
set LSpacer  0.008               ;# Length Spacer

#thickness of gate insulator
```

```
set Tiox      0.0007                ;#Gate interlayer oxide thickness
set Tihfo2    0.001                 ;#Gate high-k

#RMG (metal stack)
set TiN1      0.0015              ;# First layer TiN
set TaN2      0.0020              ;# Second layer TaN
set TiN3      0.0050              ;# Third layer TiN
set TiAl4     0.0050              ;# Fourth layer TiAl

# Doping parameters
set Nsub      1.0e15                ;#Substrate doping [/cm3]
set Nepi      7.0e18

set Nsd       1.9e13                ;#SD doping [/cm2]
set Nch       1.4e13              ;#channel doping [/cm2]


line x location= -70.0<nm> spacing=10.0<nm> tag= SiTop
line x location= 20.0<nm> spacing= 10.0<nm>
line x location= 50.0<nm> spacing= 20.0<nm> tag= SiBottom

line y location= 0.0 spacing= 50.0<nm> tag= Left
line y location= 0.062<um> spacing= 50.0<nm> tag= Right

line z location= 0.0 spacing= 50.0<nm> tag= Back
line z location= 0.1<um> spacing= 50.0<nm> tag= Front

#substrate
region Silicon xlo= SiTop xhi= SiBottom ylo= Left yhi= Right zlo= Back
    zhi= Front substrate

init concentration=$Nsub<cm-3> field=Boron wafer.orient= {0 0 1} flat.
    orient= {1 1 0} !DelayFullD

struct tdr= n@node@_pGAA1

refinebox name= nw min= {-0.12 0 0.0} max= {-0.05 0.11 0.1} xrefine= 5<
    nm> yrefine= 10<nm> zrefine= 50<nm>
grid remesh

#--Epi layer with known doping concentration (well)

temp_ramp name= epi temperature= 750<C> time= 4.5<min> Epi \
  epi.doping= { Boron= $Nepi<cm-3> } epi.doping.final= { Boron= $Nepi<cm
    -3> } epi.model= 1 epi.thickness= $H

diffuse temp_ramp= epi

#----Sidewall Image Transfer (SIT)
diffuse temperature= 900<C> time= 4.0<min> O2
deposit material= {Nitride} type= isotropic time= 1<min> rate= {0.0165}
deposit material= {AmorphousSilicon} type= isotropic time= 1<min> rate=
    {0.0195}
```

```
80
81 mask name= fin left= 0<nm> right= 38<nm> back= -1 front= 0.17<um>
       negative
82
83 etch material= {AmorphousSilicon} type= anisotropic time= 1<min> rate=
       {0.04} mask= fin
84
85 struct tdr= n@node@_pGAA4
86
87 deposit material= {Oxide} type= isotropic time= 1 rate= {0.015}
88 etch material= {Oxide} type= anisotropic time= 1 rate= {0.015} isotropic
       .overetch= 0.1
89 etch material= {AmorphousSilicon} type= anisotropic time=1<min> rate=
       {0.3}
90 etch material= {Nitride} type=anisotropic time= 1<min> rate= {0.02}
91 etch material= {Oxide} type= anisotropic time=1 rate= {0.02}
92 etch material= {Silicon} type=anisotropic time=1<min> rate= {$H}
       isotropic.overetch= 0.03
93
94 struct tdr= n@node@_pGAA8 ;# fin exposure
95
96 mater add name=TEOS new.like=oxide
97 deposit material= {TEOS} type= isotropic time= 1<min> rate= {($H+0.0165)
       }
98
99 etch material= {TEOS} type=cmp etchstop= {Nitride} etchstop.overetch
       =0.01
100
101 struct tdr= n@node@_pGAA10 ;# TEOS CMP
102 #---------------------
103 etch material= {TEOS} type=isotropic time=1 rate= {(0.0165+0.003+$Hfin)}
104 etch material= {Nitride} type=anisotropic time=1 rate= {0.02}
105
106 #Fin rounding
107
108 etch material= {Oxide} type= anisotropic time=1<min> rate= {0.01}
109
110 etch material= {Silicon} type= isotropic rate= {0.004} time= 1.0
111 deposit material= {Silicon} type= isotropic rate= {0.004} time= 1.0
       selective.materials= {Silicon}
112
113 struct tdr= n@node@_pGAA12 ;# Fin rounding
114
115
116 #-----------------------------------------------------------#
117
118 # Channel doping
119
120 implant Phosphorus dose= $Nch<cm-2> energy=3<keV> tilt=10 rotation=90
121
122 implant Phosphorus dose= $Nch<cm-2> energy=3<keV> tilt=10 rotation=270
123
124 diffuse temperature=1000<C> time=60<s>
```

```
125
126 SetPlxList {PTotal BTotal}
127 WritePlx n@node@_NMOS_sddiff.plx y=0.03 z=0.0 Silicon
128
129 struct tdr= n@node@_pGAA12c ;# channel doping
130
131 #Dummy gate
132 deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox}
133 struct tdr= n@node@_pGAA13b
134
135 deposit material= {Polysilicon} type= fill coord= -0.17
136
137 mask name= gate back= (0.05-$HalfLg)<um> front= (0.05+$HalfLg)<um>
138 etch material= {Polysilicon} type= anisotropic time=1 rate= {0.17} mask=
      gate
139
140 struct tdr= n@node@_pGAA13 ;# Dummy Gate
141
142
143 etch material= {Oxide} type=anisotropic time=1 rate=1.0
144
145 deposit material= {Oxide} type= isotropic time=1<min> rate= {$Tiox}
    selective.materials= {PolySilicon}
146
147 etch material= {Oxide} type=cmp etchstop= {PolySilicon} etchstop.
    overetch=0.001
148
149
150 deposit material= {Nitride} type= isotropic time=1<min> rate= {$LSpacer}
      selective.materials= {Oxide}
151
152 etch material= {Nitride} type=cmp etchstop= {PolySilicon} etchstop.
    overetch=0.001
153
154 struct tdr= n@node@_pGAA17 ;# Spacer
155
156 mask name= gate_neg back= (0.05-$HalfLg)<um> front= (0.05+$HalfLg)<um>
    negative
157
158 # S/D fabrication
159
160 mater add name=SiCN new.like= Nitride
161 deposit material= {SiCN} type=anisotropic time=1 rate= {0.08} mask=
    gate_neg
162
163 etch material= {Silicon} type= anisotropic rate= {0.003} time= 1.0
164
165 struct tdr= n@node@_pGAA18b ;# S/D epitaxy
166
167 etch material= {Silicon} type= isotropic rate= {0.001} time= 1.0
168
169 struct tdr= n@node@_pGAA18c ;# S/D epitaxy
170
```

```
171 #-- To activate stress in Si:C pocket for nFinFET---#
172 pdbSetDoubleArray Silicon Carbon Conc.Strain {0 0 1 -0.432}
173
174 # Diamond shaped Si/SiC Pocket using Lattice KMC (LKMC)
175 pdbSet Grid KMC UseLines 1
176 pdbSet KMC  Epitaxy true
177 pdbSetBoolean LKMC PeriodicBC false
178 pdbSet LKMC Epitaxy.Model Coordinations.Planes
179
180 set EpiDoping_init  "Carbon= 1.5e21"
181 set EpiDoping_final "Carbon= 1.5e21"
182
183 temp_ramp name= epi temperature= 450<C> t.final= 740<C> time= 7.0<min>
    Epi epi.doping= $EpiDoping_init epi.doping.final= $EpiDoping_final
    epi.model= 1 epi.layers= 10 epi.thickness= 0.02
184
185 diffuse temp_ramp= epi lkmc
186
187 pdbSet KMC Epitaxy false
188
189 struct tdr= n@node@_pGAA18 ;# S/D epitaxy
190
191 #-------------------------------------------------------------#
192
193 # S/D Implantation
194
195 implant Phosphorus dose= $Nsd<cm-2> energy=6<keV> tilt=10 rotation=90
196
197 implant Phosphorus dose= $Nsd<cm-2> energy=6<keV> tilt=10 rotation=270
198
199 SetPlxList {BTotal Phosphorus_Implant}
200 WritePlx n@node@_NMOS_sdimp.plx y=0.03 z=0.0 Silicon
201
202 etch material= {SiCN} type=isotropic rate=1.0 time=1
203
204 diffuse temperature=1000<C> time=60<s>
205
206 SetPlxList {PTotal BTotal}
207 WritePlx n@node@_NMOS_sddiff.plx y=0.03 z=0.0 Silicon
208
209 struct tdr= n@node@_pGAA19 ;# SD implantation
210
211 #-------------------------------------------------------------#
212
213 # Silicidation
214
215 deposit material= {TiSilicide} type= isotropic rate= 0.12*$Hfin time=
    1.0 temperature= 450 selective.materials= {Silicon}
216
217 struct tdr= n@node@_pGAA20 ;# Silicidation
218
219 #-------------------------------------------------------------#
220
```

```
221 # Planarization PSG
222
223 mater add name= PSG
224 ambient name=Silane react add
225 reaction name= PSGreaction mat.l= Phosphorus mat.r= Oxide mat.new= PSG
        new.like= Oxide ambient.name= {Silane} diffusing.species= {Silane}
226
227 deposit material= {PSG} type= isotropic time=1 rate= {0.2}
228
229 etch material= {PSG} type=cmp etchstop= {Nitride} etchstop.overetch=0.01
230
231 struct tdr= n@node@_pGAA21 ;# PSG
232
233 #-------------------------------------------------------------#
234
235 # Dummy gate etching
236
237 strip Polysilicon
238
239 etch material= {Oxide} type=anisotropic time=1 rate= {0.1} mask=gate_neg
         isotropic.overetch=0.01
240
241 struct tdr= n@node@_pGAA23 ;# SiO2 removal
242
243 # Gate stack fabrication
244
245 deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox} selective
        .materials= {Silicon}
246
247 struct tdr= n@node@_pGAA24 ;# SiO2
248
249 deposit material= {HfO2} type= isotropic time=1 rate= {$Tihfo2}
        selective.materials= {Oxide}
250
251 struct tdr= n@node@_pGAA25 ;# HfO2
252
253 # MIG
254
255 mater add name= TiAl new.like= Aluminum
256
257 # TaN metal
258 mater add name=TaN new.like=Aluminum
259 pdbSet TaN Mechanics BulkModulus    1.96e12
260 pdbSet TaN Mechanics ShearModulus   0.69e12
261 pdbSet TaN Mechanics ThExpCoeff     6.5e-6
262
263 deposit material= {TiN} type= isotropic time=1 rate= {$TiN1} mask=
        gate_neg
264
265 deposit material= {TaN} type= isotropic time=1 rate= {$TaN2} selective.
        materials= {TiN}
266
```

```
267 deposit material= {TiN} type= isotropic time=1 rate= {$TiN3} selective.
    materials= {TaN}
268
269 deposit material= {TiAl} type= isotropic time=1 rate= {$TiAl4} selective
    .materials= {TiN}
270
271 struct tdr= n@node@_pGAA29 ;# TiAl4 deposition
272
273 diffuse temp=500<C> time=1.0e-6<s> stress.relax
274
275 deposit material= {Tungsten} type=fill coord= -0.2
276
277 struct tdr= n@node@_pGAA31 ;# W fill
278
279 etch material= {Tungsten} type=cmp etchstop= {PSG} etchstop.overetch
    =0.01
280
281 struct tdr= n@node@_pGAA32 ;# metal gate cmp
282
283 etch material= {Tungsten} type=isotropic time=1 rate= {0.003}
284
285 deposit material= {Nitride} type=fill coord=-0.2
286
287 etch material= {Nitride} type=cmp etchstop= {PSG} etchstop.overetch=0.01
288
289 struct tdr= n@node@_pGAA35
290
291 mask name=s left=8<nm> right=54<nm> back=(0.05+$HalfLg+$LSpacer+0.006)<
    um> front=94<nm> negative
292
293 mask name=d left=8<nm> right=54<nm> back=6<nm> front=(0.05-$HalfLg-
    $LSpacer-0.006)<um> negative
294
295 mask name=g left=8<nm> right=54<nm> back=45<nm> front=56<nm> negative
296
297 etch material= {PSG} type=anisotropic  time=1 rate= {0.1} mask=s
298
299 struct tdr= n@node@_pGAA36
300
301 etch material= {PSG} type=anisotropic  time=1 rate= {0.1} mask=d
302
303 struct tdr= n@node@_pGAA37
304
305 etch material= {Nitride} type=anisotropic  time=1 rate= {0.1} mask=g
306
307 struct tdr= n@node@_pGAA38
308
309 deposit material= {Tungsten} type=fill coord=-0.2
310
311 etch material= {Tungsten} type=cmp etchstop= {Nitride} etchstop.overetch
    =0.01
312
313 struct tdr= n@node@_pGAA40
```

```
314
315 #-----------------------------------------------------------#
316 transform cut location= -0.05 down
317
318 # clear the process simulation mesh
319 refinebox clear
320 refinebox !keep.lines
321 line clear
322
323 # reset default settings for adaptive meshing
324 pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
325 pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
326 pdbSet Grid AdaptiveField Refine.Target.Length 100.0
327
328 # Set high quality Delaunay meshes
329 pdbSet Grid sMesh 1
330 pdbSet Grid Adaptive 1
331 pdbSet Grid SnMesh DelaunayType boxmethod
332 pdbSet Grid SnMesh CoplanarityAngle 179
333 pdbSet Grid SnMesh MaxPoints 2000000
334 pdbSet Grid SnMesh max.box.angle.3d 179
335
336 refinebox name= gate min= {-0.088 0.0 0.038} max= {-0.2 0.062 0.061}
    xrefine= 5<nm> yrefine= 10<nm> zrefine= 5<nm> materials= {Silicon}
    adaptive
337
338 refinebox name= source min= {-0.088 0.0 0.061} max= {-0.2 0.062 0.1}
    xrefine= 5<nm> yrefine= 5<nm> zrefine= 5<nm> materials= {Silicon}
    adaptive
339
340 refinebox name= drain min= {-0.088 0.0 0.0} max= {-0.2 0.062 0.03}
    xrefine= 5<nm> yrefine= 5<nm> zrefine= 5<nm> materials= {Silicon}
    adaptive
341
342 refinebox name= sub min= {-0.088 0.0 0.0} max= {-0.05 0.062 0.1} xrefine
    = 5<nm> yrefine= 5<nm> zrefine= 5<nm> materials= {Silicon} adaptive
343
344 refinebox name= channel min= {-0.080 0.0 0.05-$HalfLg-$LSpacer} max=
    {-0.2 0.062 0.05+$HalfLg+$LSpacer} xrefine= 1<nm> yrefine= 1<nm>
    zrefine= 1<nm>
345
346 refinebox name= source_Ti min= {-0.088 0.0 0.061} max= {-0.2 0.062 0.1}
    xrefine= 15<nm> yrefine= 10<nm> zrefine= 15<nm> materials= {
    TiSilicide}
347
348 refinebox name= drain_Ti min= {-0.088 0.0 0.0} max= {-0.2 0.062 0.03}
    xrefine= 15<nm> yrefine= 10<nm> zrefine= 15<nm> materials= {
    TiSilicide}
349
350 refinebox name=SiGOX min.normal.size=0.1<nm> normal.growth.ratio=1.4 \
351 max.lateral.size=5.0<nm> min= {-0.089 0.0 0.05-$HalfLg-$LSpacer} max=
    {-0.2 0.062 0.05+$HalfLg+$LSpacer} interface.materials= {Silicon}
352
```

```
grid remesh

struct tdr= n@node@_pGAA41 ;# remeshing

#-------------------------------------------------#

contact bottom name= bulk Silicon

contact name= gate x= -0.140 y= 0.014 z= 0.050 Tungsten

contact name= source x= -0.14 y= 0.0166 z= 0.08 Tungsten

contact name= drain x= -0.14 y= 0.0166 z= 0.01 Tungsten

struct tdr= n@node@_presimulation !Gas

exit
```

A.2 n-type JL-NSGAAFET sprocess file

```
math coord.ucs

math numThreads=4
AdvancedCalibration 2017.09


pdbSet Mechanics StressRelaxFactor 1

pdbSet Math diffuse 3D ILS.hpc.mode 4
pdbSet Mechanics EtchDepoRelax 0

mgoals resolution= 1.0/3.0 accuracy= 1e-6
pdbSet Grid SnMesh max.box.angle.3d 175
grid set.min.normal.size= 0.005/1.0 \
 set.normal.growth.ratio.3d= 2.0 \
 set.min.edge= 1e-7 set.max.points= 1000000 \
 set.max.neighbor.ratio= 1e6

#-------------------------------------------------
# Structure parameters, [um]
set STI      0.02                ;# STI
set Tns      0.005                 ;# Thickness nanosheet
set Spacing  0.015                 ;# Space between nanosheet (SiGe)
set H        [expr 2*$Spacing + $Tns + $STI]  ;# Fin exposure
set Hfin     [expr ($H - $STI)]             ;# Fin height

set Lg       @Lg@                        ;# Gate length
set HalfLg   [expr $Lg*0.5]             ;# Half gate length
set Tox      0.002                      ;# Thickness of gate insulator
set LSpacer  0.008                   ;# Length Spacer

#thickness of gate insulator
```

```
set Tiox      0.0007                          ;#Gate interlayer oxide
    thickness
set Tihfo2    0.001                           ;#Gate high-k

#RMG (metal stack)
set TiN1      0.0020                  ;# layer TiN

# Doping parameters
set Nsub      1.0e15                          ;#Substrate doping [/cm3]

set Nsd       7.0e12                          ;#SD doping [/cm2]
set Nch       1.0e13                  ;#S/D/channel  doping [/cm2]
set Nstop     1.0e13                          ;#well doping [/cm2]


line x location= -70.0<nm> spacing=10.0<nm> tag= SiTop
line x location= 20.0<nm> spacing= 10.0<nm>
line x location= 50.0<nm> spacing= 20.0<nm> tag= SiBottom

line y location= 0.0 spacing= 50.0<nm> tag= Left
line y location= 0.062<um> spacing= 50.0<nm> tag= Right

line z location= 0.0 spacing= 50.0<nm> tag= Back
line z location= 0.1<um> spacing= 50.0<nm> tag= Front

#substrate
region Silicon xlo= SiTop xhi= SiBottom ylo= Left yhi= Right zlo= Back
    zhi= Front substrate

init concentration=$Nsub<cm-3> field=Boron wafer.orient= {0 0 1} flat.
    orient= {1 1 0} !DelayFullD

refinebox name= nw min= {-0.12 0 0.0} max= {-0.05 0.11 0.1} xrefine= 5<
    nm> yrefine= 10<nm> zrefine= 50<nm>
grid remesh

#--Epi layer with known doping concentration (well)

deposit material= {Silicon} type=isotropic time=1 rate= {$H}

deposit material= {SiliconGermanium} type=isotropic time=1 rate= {
    $Spacing}

deposit material= {Silicon} type=isotropic time=1 rate= {$Tns}

deposit material= {SiliconGermanium} type=isotropic time=1 rate= {
    $Spacing}

#----Sidewall Image Transfer (SIT)
diffuse temperature= 900<C> time= 4.0<min> O2
deposit material= {Nitride} type= isotropic time= 1<min> rate= {0.0165}
deposit material= {AmorphousSilicon} type= isotropic time= 1<min> rate=
    {0.0195}
```

```
79
80 struct tdr= n@node@_pGAA3 ;#deposit SiO2, hardmask, mandrel
81
82 mask name= fin left= 0<nm> right= 38<nm> back= -1 front= 0.17<um>
       negative
83
84 etch material= {AmorphousSilicon} type= anisotropic time= 1<min> rate=
       {0.04} mask= fin
85
86 deposit material= {Oxide} type= isotropic time= 1 rate= {0.015}
87 etch material= {Oxide} type= anisotropic time= 1 rate= {0.015} isotropic
       .overetch= 0.1
88
89 etch material= {AmorphousSilicon} type= anisotropic time=1<min> rate=
       {0.3}
90 etch material= {Nitride} type=anisotropic time= 1<min> rate= {0.02}
91 etch material= {Oxide} type= anisotropic time=1 rate= {0.02}
92 etch material= {Silicon SiliconGermanium} type=anisotropic time=1<min>
       rate= {$H}
93
94 mater add name=TEOS new.like=oxide
95 deposit material= {TEOS} type= isotropic time= 1<min> rate= {($H+0.0165)
       }
96
97 etch material= {TEOS} type=cmp etchstop= {Nitride} etchstop.overetch
       =0.0001
98 etch material= {TEOS} type=isotropic time=1 rate= {(0.0165+0.002+$Hfin)}
99 etch material= {Nitride} type=anisotropic time=1 rate= {0.02}
100 etch material= {Oxide} type= anisotropic time=1<min> rate= {0.01}
101
102 mask name= inner back= (0.05-$HalfLg-$LSpacer)<um> front= (0.05+$HalfLg+
       $LSpacer)<um>
103
104 etch material= {Silicon SiliconGermanium} type= anisotropic time=1 rate=
        {$Hfin} mask= inner
105
106 mask name= fin_dummy left=20.3<nm> right=38<nm> back=-1<um> front= 0.17<
       um>
107
108 deposit material= {Silicon} type= fill coord= -0.16
109
110 etch material= {Silicon} type=cmp etchstop= {SiliconGermanium} etchstop.
       overetch=0.001
111
112 etch material= {Silicon} type= anisotropic time=1 rate= {$Hfin} mask=
       fin_dummy
113
114 #well implant
115
116 refinebox name= etchstop min= {-0.13 0 0.0} max= {-0.04 0.062 0.1}
       xrefine= 2<nm> yrefine= 10<nm> zrefine= 50<nm>
117 grid remesh
118
```

```
implant Boron dose= $Nstop<cm-2> energy=2<keV> tilt=0 rotation=0

SetPlxList {BTotal}
WritePlx n@node@_NMOS_etchstoplayer.plx y=0.03 z=0.0 Silicon

implant Boron dose= $Nstop<cm-2> energy=4<keV> tilt=0 rotation=0

SetPlxList {BTotal}
WritePlx n@node@_NMOS_etchstoplayer1.plx y=0.03 z=0.0 Silicon

implant Boron dose= $Nstop<cm-2> energy=6<keV> tilt=0 rotation=0

SetPlxList {BTotal}
WritePlx n@node@_NMOS_etchstoplayer2.plx y=0.03 z=0.0 Silicon

diffuse temperature=1050<C> time=20.0<s>

SetPlxList {BTotal}
WritePlx n@node@_NMOS_etchstoplayer3.plx y=0.03 z=0.0 Silicon

struct tdr= n@node@_pGAA12b

#S/D/channel doping

refinebox name= sd min= {-0.13 0 0.0} max= {-0.04 0.062 0.1} xrefine= 2<
    nm> yrefine= 5<nm> zrefine= 2<nm>
grid remesh

mask name= gate_neg back= (0.05-$HalfLg)<um> front= (0.05+$HalfLg)<um>
    negative

implant Phosphorus dose= $Nch<cm-2> energy=3<keV> tilt=10<degree>
    rotation=90<degree>

implant Phosphorus dose= $Nch<cm-2> energy=3<keV> tilt=10<degree>
    rotation=270<degree>

SetPlxList {BTotal Phosphorus_Implant}
WritePlx n@node@_NMOS_sdext.plx y=0.03 z=0.0 Silicon

diffuse temperature=1050<C> time=10<s>

SetPlxList {PTotal BTotal}
WritePlx n@node@_PMOS_sdext2X.plx y=0.03 z=0.0 Silicon

SetPlxList {PTotal BTotal}
WritePlx n@node@_PMOS_sdext2Y.plx x=-0.12 z=0.0 Silicon

struct tdr= n@node@_pGAA15 ;# Phosphorus implantation

#Dummy gate
deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox}
struct tdr= n@node@_pGAA13b
```

```
168
169 deposit material= {Polysilicon} type= fill coord= -0.18
170
171 struct tdr= n@node@_pGAA13c
172
173 mask name= gate back= (0.05-$HalfLg)<um> front= (0.05+$HalfLg)<um>
174 etch material= {Polysilicon} type= anisotropic time=1 rate= {0.18} mask=
        gate
175
176 struct tdr= n@node@_pGAA13d
177
178 mask name= inner_neg back= (0.05-$HalfLg-$LSpacer)<um> front= (0.05+
    $HalfLg+$LSpacer)<um> negative
179
180 etch material= {Oxide} type=anisotropic time=1 rate=1.0
181
182 struct tdr= n@node@_pGAA13e
183
184 etch material= {SiliconGermanium} type= anisotropic time=1 rate= {0.18}
    mask= gate
185
186 struct tdr= n@node@_pGAA13f
187
188 deposit material= {Oxide} type= isotropic time=1<min> rate= {$Tiox}
    selective.materials= {PolySilicon}
189
190 struct tdr= n@node@_pGAA13g
191
192 etch material= {Oxide} type=cmp etchstop= {PolySilicon} etchstop.
    overetch=0.001
193
194 struct tdr= n@node@_pGAA13h
195
196 mask name= spacer_neg back= (0.05-$HalfLg-$LSpacer)<um> front= (0.05+
    $HalfLg+$LSpacer)<um> negative
197
198 deposit material= {Nitride} type= anisotropic time=1<min> rate= {0.1}
    mask=spacer_neg
199
200 etch material= {Nitride} type=cmp etchstop= {PolySilicon} etchstop.
    overetch=0.001
201 struct tdr= n@node@_pGAA17 ;# Spacer
202
203 # S/D fabrication
204 mask name= spacer_neg back= (0.05-$HalfLg-$LSpacer)<um> front= (0.05+
    $HalfLg+$LSpacer)<um> negative
205
206 mater add name=SiCN new.like= Nitride
207 deposit material= {SiCN} type=anisotropic time=1 rate= {0.08} mask=
    spacer_neg
208
209 #-- To activate stress in Si:C pocket for nFinFET---#
210 pdbSetDoubleArray Silicon Carbon Conc.Strain {0 0 1 -0.432}
```

```
pdbSetDouble Silicon Mechanics TopRelaxedNodeCoord 0.05e-4

# Diamond shaped Si/SiC Pocket using Lattice KMC (LKMC)
pdbSet Grid KMC UseLines 1
pdbSet KMC  Epitaxy true
pdbSetBoolean LKMC PeriodicBC false
pdbSet LKMC Epitaxy.Model Coordinations.Planes

struct tdr= n@node@_pGAA18c ;# S/D epitaxy

set EpiDoping_init  "Carbon= 1.5e21"
set EpiDoping_final "Carbon= 1.5e21"

temp_ramp name= epi temperature= 450<C> t.final= 740<C> time= 7.0<min>
    Epi epi.doping= $EpiDoping_init epi.doping.final= $EpiDoping_final
    epi.model= 1 epi.thickness= 0.02

diffuse temp_ramp= epi lkmc

pdbSet KMC Epitaxy false

struct tdr= n@node@_pGAA18 ;# S/D epitaxy

# S/D Implantation

implant Phosphorus dose= $Nsd<cm-2> energy=5<keV> tilt=10 rotation=90

implant Phosphorus dose= $Nsd<cm-2> energy=5<keV> tilt=10 rotation=270

SetPlxList {BTotal Phosphorus_Implant}
WritePlx n@node@_NMOS_sdimp.plx y=0.03 z=0.0 Silicon

etch material= {SiCN} type=isotropic rate=1.0 time=1

diffuse temperature=1000<C> time=1<s>

SetPlxList {PTotal BTotal}
WritePlx n@node@_NMOS_sddiff_ch.plx y=0.03 x=-0.142 Silicon

SetPlxList {PTotal BTotal}
WritePlx n@node@_NMOS_sddiff.plx y=0.03 z=0.0 Silicon

struct tdr= n@node@_pGAA19 ;# SD implantation

deposit material= {TiSilicide} type= isotropic rate= 0.12*$Hfin time=
    1.0 temperature= 450 selective.materials= {Silicon}

# Planarization PSG

mater add name= PSG
ambient name=Silane react add
reaction name= PSGreaction mat.l= Phosphorus mat.r= Oxide mat.new= PSG
    new.like= Oxide ambient.name= {Silane} diffusing.species= {Silane}
```

```
260
261 deposit material= {PSG} type= isotropic time=1 rate= {0.2}
262 etch material= {PSG} type=cmp etchstop= {Nitride} etchstop.overetch=0.01
263
264 # Dummy gate etching
265
266 strip Polysilicon
267
268 strip Oxide
269
270 etch material= {SiliconGermanium} type=isotropic time=1 rate= {0.1}
271
272 # Gate stack fabrication
273
274 deposit material= {Oxide} type= isotropic time=1 rate= {$Tiox} mask=
    gate_neg
275
276 etch material= {Oxide} type=cmp etchstop= {Nitride} etchstop.overetch
    =0.01
277
278 struct tdr= n@node@_pGAA24 ;# SiO2
279
280 deposit material= {HfO2} type= isotropic time=1 rate= {$Tihfo2}
    selective.materials= {Oxide}
281
282 struct tdr= n@node@_pGAA25 ;# HfO2
283
284 deposit material= {TiN} type= isotropic time=1 rate= {$TiN1} selective.
    materials= {HfO2}
285
286 diffuse temp=500<C> time=1.0e-6<s> stress.relax
287
288 deposit material= {Tungsten} type=fill coord= -0.2
289
290 etch material= {Tungsten} type=cmp etchstop= {PSG} etchstop.overetch
    =0.01
291
292 etch material= {Tungsten} type=isotropic time=1 rate= {0.003}
293
294 deposit material= {Nitride} type=fill coord=-0.2
295
296 etch material= {Nitride} type=cmp etchstop= {PSG} etchstop.overetch=0.01
297
298 mask name=s left=8<nm> right=54<nm> back=74<nm> front=94<nm> negative
299
300 mask name=d left=8<nm> right=54<nm> back=7<nm> front=25<nm> negative
301
302 mask name=g left=8<nm> right=54<nm> back=45<nm> front=56<nm> negative
303
304 etch material= {PSG} type=anisotropic  time=1 rate= {0.1} mask=s
305
306 etch material= {PSG} type=anisotropic  time=1 rate= {0.1} mask=d
307
```

```
etch material= {Nitride} type=anisotropic  time=1 rate= {0.1} mask=g

deposit material= {Tungsten} type=fill coord=-0.2

etch material= {Tungsten} type=cmp etchstop= {Nitride} etchstop.overetch
    =0.01

struct tdr= n@node@_pGAA40

transform cut location= -0.05 down

# clear the process simulation mesh
refinebox clear
refinebox !keep.lines
line clear

# reset default settings for adaptive meshing
pdbSet Grid AdaptiveField Refine.Abs.Error 1e37
pdbSet Grid AdaptiveField Refine.Rel.Error 1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0

# Set high quality Delaunay meshes
pdbSet Grid sMesh 1
pdbSet Grid Adaptive 1
pdbSet Grid SnMesh DelaunayType boxmethod
pdbSet Grid SnMesh DelaunayTolerance 5.0e-2
pdbSet Grid SnMesh CoplanarityAngle 179
pdbSet Grid SnMesh MaxPoints 2000000
pdbSet Grid SnMesh max.box.angle.3d 179

refinebox name= gate min= {-0.088 0.0 0.038} max= {-0.2 0.062 0.061}
    xrefine= 5<nm> yrefine= 10<nm> zrefine= 5<nm> materials= {Silicon}

refinebox name= source min= {-0.088 0.0 0.061} max= {-0.2 0.062 0.1}
    xrefine= 5<nm> yrefine= 10<nm> zrefine= 5<nm> materials= {Silicon}

refinebox name= drain min= {-0.088 0.0 0.0} max= {-0.2 0.062 0.03}
    xrefine= 5<nm> yrefine= 10<nm> zrefine= 5<nm> materials= {Silicon}

refinebox name= channel min= {-0.089 0.0 0.05-$HalfLg} max= {-0.2 0.062
    0.05+$HalfLg} xrefine= 2<nm> yrefine= 1<nm> zrefine= 1<nm> materials
    = {Silicon}

refinebox name= source min= {-0.088 0.0 0.061} max= {-0.2 0.062 0.1}
    xrefine= 15<nm> yrefine= 10<nm> zrefine= 15<nm> materials= {
    TiSilicide}

refinebox name= drain min= {-0.088 0.0 0.0} max= {-0.2 0.062 0.03}
    xrefine= 15<nm> yrefine= 10<nm> zrefine= 15<nm> materials= {
    TiSilicide}

refinebox name=SiGOX min.normal.size=0.1<nm> normal.growth.ratio=1.4 \
```

```
max.lateral.size=5.0<nm> min= {-0.089 0.0 0.05-$HalfLg-$LSpacer} max=
    {-0.2 0.062 0.05+$HalfLg+$LSpacer} interface.materials= {Silicon}

grid remesh

struct tdr= n@node@_pGAA41 ;# remeshing

contact bottom name= bulk Silicon

contact name= gate x= -0.170 y= 0.014 z= 0.050 Tungsten

contact name= source x= -0.17 y= 0.0166 z= 0.08 Tungsten

contact name= drain x= -0.17 y= 0.0166 z= 0.01 Tungsten

struct tdr= n@node@_presimulation !Gas


exit
```

A.3 n-type JL-NSGAAFET and JL-finFET sdevice file

```
File {
*Input Files
  Grid      = "n@previous@_presimulation_fps.tdr"
  Parameter = "sdevice.par"


*Output Files
  Plot      = "n@node@_tdrdat"
  Current   = "n@node@_nJL-NSGAAFET_I"
  Output    = "n@node@_log"

}

Electrode
{
* defines which contacts have to be treated as electrodes; initial bias
* & boundary conditions
{ name="source" Voltage=0.0 }
{ name="drain" Voltage=0.0 }
{ name="gate" Voltage=0.0 }
{ name="bulk" Voltage=0.0 }
}

Physics
{
  Mobility( DopingDep Enormal(RPS) HighFieldSaturation )
    EffectiveIntrinsicDensity( BandGapNarrowing( OldSlotBoom ) NoFermi )
    Recombination ( SRH(DopingDep) Auger Band2Band ( Model = Hurkx ) )
}
```

```
Physics (Material="Silicon")
{
  Aniso(eQuantumPotential(Direction(SimulationSystem)=(0,0,1)))
}

Plot{
*--Density and Currents, etc
   eDensity hDensity
   ConductionCurrentDensity
   TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
   eMobility/Element hMobility/Element
   eVelocity hVelocity
   eQuasiFermi hQuasiFermi
   ElectrostaticPotential

*--Fields and charges
   ElectricField/Vector Potential SpaceCharge

*--Doping Profiles
   Doping DonorConcentration AcceptorConcentration

*--Generation/Recombination
   SRH Band2Band Auger
   AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

*--Driving forces
   eGradQuasiFermi/Vector hGradQuasiFermi/Vector
   eEparallel hEparallel eENormal hENormal

*--Band structure/Composition
   BandGap
   MetalWorkFunction
   BandGapNarrowing EffectiveBandGap
   Affinity ElectronAffinity
   ConductionBandEnergy ValenceBandEnergy
   eQuantumPotential hQuantumPotential
}

Math
{
coordinateSystem { UCS }
-CheckUndefinedModels
GeometricDistances
* use previous two solutions (if any) to extrapolate next
Extrapolate
* use full derivatives in Newton method
Derivatives
* control on relative and absolute errors
-RelErrControl
* relative error= 10^(-Digits)
Digits=5
* absolute error
Error(electron)=1e8
```

```
Error(hole)=1e8
* numerical parameter for space-charge regions
eDrForceRefDens=1e10
hDrForceRefDens=1e10
* maximum number of iteration at each step
Iterations=100
* solver of the linear system
Method=ILS
* display simulation time in 'human' units
Wallclock
* display max.error information
CNormPrint
* to avoid convergence problem when simulating defect-assisted tunneling
NoSRHperPotential
StressMobilityDependence=TensorFactor
CheckRhsAfterUpdate
RHSmin=1e-12
Number_of_Threads = 4
}

Solve {
   *- Build-up of initial solution:
   Coupled { Poisson }
   Coupled (Iterations=100 LineSearchDamping=1e-4) { Poisson
    eQuantumPotential }
   Coupled { Poisson Electron eQuantumPotential }
   Coupled { Poisson Electron Hole eQuantumPotential }
    Save ( FilePrefix= "n@node@_init" )

    NewCurrentPrefix = "n@node@_IdVd1"
#-- Ramp drain to VdSat
  Quasistationary(
    InitialStep= 0.001 MinStep= 1e-7 MaxStep= 0.025
    Goal { Name= "drain" Voltage= 0.75 } )
    { Coupled { Poisson Electron Hole eQuantumPotential }
*I-V calculated at regular intervals
       CurrentPlot(Time=(Range=(0 1) Intervals=100))
    }

NewCurrentPrefix = "n@node@_IdVg1"
#-- Vg sweep for Vd=VdSat
  Quasistationary(
    InitialStep= 0.001 MinStep= 1e-7 MaxStep= 0.025
    Goal { Name= "gate" Voltage= 0.75 } )
    { Coupled { Poisson Electron Hole eQuantumPotential }
*I-V calculated at regular intervals
       CurrentPlot(Time=(Range=(0 1) Intervals=100))
    }

}
```

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