

POLITECNICO DI TORINO

Master's Degree in Biomedical Engineering



**Politecnico
di Torino**

Master's Degree Thesis

Development and characterization of integrated microelectrodes for miniaturized neurostimulators

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*“Alla mia meravigliosa famiglia,
pilastro della mia vita
e a te che brilli
più luminosa di tutte.”*

Abstract

Brain stimulation is an effective technique to restore impairing neural functions, such as deafness and blindness. Despite the progresses in leaps and bounds in these technologies, several limitations are still present, such as wiring connection to implants, bulky batteries and invasiveness of surgical procedure. For these reasons, neuroengineering research is moving towards the development of miniaturized and wireless implantable devices for selective and specific neurostimulation. This, inevitably, brings up new issues to face, such as mechanical and electrochemical stability of microelectrodes after integration. This aspect is the core of my master's thesis, conducted at EPFL (*École Polytechnique Fédérale de Lausanne*) at the *Integrated Circuits LABORatory (ICLAB)* in Neuchâtel and at the *Center of Micronanotechnology (CMi)* in Lausanne. The goal of the project is developing and characterizing a system for the integration of penetrating microelectrodes for intracortical neurostimulation in ultra-miniaturized CMOS implants, exploiting three fabrication methods.

First, I analyze the feasibility of manual 3D Pt/Ir microelectrodes integration in ultra-miniaturized CMOS chip. Microelectrodes are cut to obtain 1.5 mm-long needles with an exposed truncated cone-shaped 20 μm -long tip and a base diameter of 55 μm . For our purpose, two microelectrodes on two 60x60 μm^2 pads with a pitch of 30 μm must be integrated. Conductive glue is dispensed on the pads and two cut microelectrodes are perpendicularly manually placed on the two pads. A curing session follows to make glue harden.

Secondly, maintaining the same described setup, a new Focused Ion Beam (FIB) aided integration method is developed. Microelectrodes are cut using the ion beam. The integration is then performed using the high precision micromanipulator and by depositing Pt through the FIB nozzle to weld the electrode base on the pads.

Results show that 3D integration of microelectrodes with ultra-miniaturized CMOS unit is extremely challenging, due to limited hand precision in manual integration and weakness of micromanipulator-microelectrode welding in FIB aided integration.

Therefore, I develop a system in which the microelectrodes are microfabricated at CMOS level, in post-processing. The latter are developed in cleanroom, following several dry steps of evaporation, photolithography and etching. 1575 μm -long Aluminum microelectrodes are fabricated and insulated with SiO_2 , obtaining an exposed triangular tip with a base of 45 μm and a height of 70 μm . Microelectrodes are finally and successfully perpendicularly bent and morphologically characterized at SEM.

Electrochemical characterization is performed by means of cyclic voltammetry. A miniaturized three-electrodes electrochemical cell is developed by an O-ring fixed on a PCB and filled by a drop of PBS. The manually integrated Pt/Ir microelectrode is used as *working electrode*, a commercial Ag/AgCl as *reference electrode* and a Pt-wire as *counter electrode*. Cyclic voltammetry is performed on the microelectrode before and after integration, showing comparable values of charge storage capacity and, thus, validating the electrochemical stability after 3D integration.

Considering the overall work, CMOS-compatible microfabrication is convenient to merge chip fabrication together with the microelectrodes. On the other hand, developing an automatized integration of commercial microelectrodes would represent a starting point for a novel industrial process in 3D integration.

Keywords: Implantable Medical Devices, Neural implants, Cortical Visual Prosthesis, Miniaturization, Integration, Microtips, Microelectrodes, CMOS, Microfabrication, Focused Ion Beam, Clean Room, Characterization, Electrochemistry, Cyclic Voltammetry.

Sommario

La stimolazione neurale è una tecnica efficace che permette il recupero di funzioni neurali compromesse, come la sordità e la cecità. Nonostante i passi da gigante fatti su queste tecnologie, sono ancora presenti diverse limitazioni, come le connessioni cablate agli impianti, batterie ingombranti e invasività della procedura chirurgica di inserzione. Per queste ragioni, la ricerca neuroingegneristica si sta muovendo verso lo sviluppo di dispositivi impiantabili miniaturizzati e wireless per la stimolazione selettiva e specifica. Questo aspetto, inevitabilmente, fa nascere nuovi problemi da affrontare, come la stabilità meccanica ed elettrochimica dei microelettrodi dopo l'integrazione. Quest'ultimo è l'argomento centrale su cui si sviluppa la mia tesi di Laurea Magistrale, che è stata sviluppata all'EPFL (*École Polytechnique Fédérale de Lausanne*), presso il *Laboratorio di Circuiti Integrati (ICLAB)*, a Neuchâtel e al *Centro di Micronanotecnologia (CMi)* a Losanna. L'obiettivo del progetto riguarda lo sviluppo e la caratterizzazione di un sistema di integrazione di elettrodi penetranti per neurostimolazione intracorticale in impianti CMOS ultra miniaturizzati, sfruttando tre metodi di fabbricazione.

Per prima cosa, ho analizzato la realizzabilità della integrazione manuale di elettrodi 3D in Pt/Ir in chip CMOS ultraminiaturizzati. I microelettrodi sono tagliati per ottenere degli aghi da 1.5 mm di lunghezza, con una punta esposta a forma di tronco di cono lunga 20 μm e con una base di 55 μm di diametro. Per il nostro obiettivo, due microelettrodi devono essere integrati su due pad da 60x60 μm^2 , separati da 30 μm . La colla conduttiva viene depositata sui pad e i due microelettrodi sono inseriti manualmente, verticalmente sui due pad. Infine, una sessione di polimerizzazione è richiesta, per fare indurire la colla.

In secondo luogo, mantenendo lo stesso setup appena descritto, è stato sviluppato un nuovo metodo di integrazione con aiuto di uno strumento a Fascio Ionico Focalizzato (FIB). I microelettrodi sono tagliati sfruttando il fascio ionico. L'integrazione viene, poi, effettuata utilizzando un micromanipolatore ad alta precisione e del Platino viene depositato per mezzo dell'ugello del FIB, per saldare la base dell'elettrodo ai pad.

I risultati mostrano che l'integrazione 3D dei microelettrodi su di una unità CMOS ultra miniaturizzata è estremamente impegnativa, a causa della limitata precisione della mano nella tecnica di integrazione manuale e della debole saldatura tra micromanipolatore e microelettrodo nella integrazione con FIB. Per questo motivo, ho sviluppato un sistema in cui i microelettrodi vengono fabbricati a livello CMOS, terminata la fabbricazione del chip. I microelettrodi sono sviluppati in cleanroom, seguendo diversi step di evaporazione, fotolitografia ed etching. Sono stati fabbricati microelettrodi in Alluminio lunghi $1575 \mu m$ e isolati con SiO_2 , in modo da ottenere una punta triangolare esposta, con una base di $45 \mu m$ e una altezza di $70 \mu m$. I microelettrodi sono, infine e con successo, piegati perpendicolarmente e caratterizzati morfologicamente al Microscopio a Scansione Elettronica (SEM).

La caratterizzazione elettrochimica è stata effettuata con voltammetria ciclica. È stata sviluppata una cella elettrochimica a tre elettrodi miniaturizzata, incollando un O-ring su una PCB e riempiendolo con una goccia di PBS. L'elettrodo manualmente integrato in Pt/Ir è usato come *elettrodo di lavoro*, un elettrodo commerciale in Ag/AgCl come *elettrodo di riferimento* e un filo in Platino come *elettrodo ausiliario*. La voltammetria ciclica è stata effettuata sul microelettrodo prima e dopo l'integrazione, mostrando valori confrontabili di capacità di immagazzinamento di carica (CSC) e, di conseguenza, potendo validare la stabilità elettrochimica dopo l'integrazione tridimensionale.

Considerando tutto il lavoro svolto, la microfabbricazione CMOS compatibile permette di unire la fabbricazione di un chip con quella dei microelettrodi. Al contrario, lo sviluppo di una tecnica di integrazione automatizzata di elettrodi commerciali rappresenterebbe un punto di partenza per un nuovo processo industriale nella integrazione 3D.

Keywords: Dispositivi Medici Impiantabili, Impianti neurali, Protesi Visive Corticali, Miniaturizzazione, Integrazione, Micropunte, Microelettrodi, CMOS, Microfabbricazione, Fascio di ioni focalizzato, Camera Bianca, Caratterizzazione, Elettrochimica, Voltammetria Ciclica.

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Table of Contents

List of Tables	XV
List of Figures	XVI
Acronyms	XXI
1 Introduction	1
1.1 Visual Prostheses - State of the Art	3
1.1.1 Retinal Implants	6
1.1.2 Optic nerve implants	7
1.1.3 Cortical implants	8
1.2 Microelectrodes basic requirements for neural implants	10
1.3 Microelectrodes materials	11
1.3.1 Faradaic charge injection materials	11
1.3.2 Capacitive charge injection materials	13
1.3.3 Polymeric materials	13
1.4 Types of microelectrodes	13
1.4.1 Microwire probes (MWP)	14
1.4.2 Micromachined probes (MMP)	18
1.4.3 Polymer-based probes	22
1.5 Towards miniaturized implantable devices	23
1.5.1 Challenges of present integration techniques	24
1.6 Smart Micro Neural Dust Project	24
1.6.1 Master's thesis outline	26
2 Integration of commercial microelectrodes	27
2.1 Substrate preparation	27
2.1.1 Manual integration	30
2.1.2 FIB aided integration	30
2.2 Manual integration results	32
2.3 FIB integration results	34

3	Microfabricated electrodes	37
3.1	Involved materials	37
3.2	Microfabrication steps	39
3.2.1	Aluminum deposition on front side	42
3.2.2	Photolithography for aluminum pattern	44
3.2.3	Aluminum dry etching and photo resist strip	51
3.2.4	Silicon dioxide (SiO ₂) deposition on front side	53
3.2.5	Photolithography for Silicon dioxide (SiO ₂) pattern	55
3.2.6	Silicon dioxide (SiO ₂) dry etching and photo resist strip	57
3.2.7	Iridium oxide (IrOx) deposition on front side	58
3.2.8	Photolithography for Iridium Oxide (IrOx) pattern	59
3.2.9	Iridium Oxide (IrOx) dry etching and photo resist strip	59
3.2.10	Front side parylene-C coating	60
3.2.11	Back side photolithography	61
3.2.12	Back side dry etching	62
3.2.13	Silicon dioxide (SiO ₂) deposition on back side	64
3.2.14	Structures release	65
3.3	Design results	66
3.3.1	Chip sizing	66
3.3.2	Probes length	67
3.3.3	Probes body shape	67
3.3.4	Probes tip shape	70
3.3.5	Probes orientation	71
3.4	Microfabrication results	71
3.4.1	aluminum layer	72
3.4.2	Silicon dioxide layer	73
3.4.3	Back side etch	75
3.4.4	Free standing structures	77
3.4.5	Bent structures	77
4	Electrochemical characterization	79
4.1	Electrochemistry introduction	79
4.2	Electrochemical characterization techniques	81
4.2.1	Cyclic Voltammetry (CV)	82
4.2.2	Electrochemical Impedance Spectroscopy (EIS)	86
4.2.3	Voltage Transient (VT)	86
4.3	Cyclic voltammetry (CV) in miniaturized electrochemical cell	88
4.3.1	Cyclic voltammetry measurements comparison among pre-integration and post-integration	92

5	Conclusions and future developments	97
5.1	Future developments	98
A	Microfabrication Process Flow	100
B	Matlab code	108
	Bibliography	112

List of Tables

3.1	Available wafers at <i>CMi</i>	40
3.2	RCA cleaning procedure summary [91]	41
3.3	<i>Pfeiffer Spider 600</i> recipe parameters for Ti/Al deposition	43
3.4	Spin speed and softbake time for different photo resist thicknesses. [93]	47
3.5	aluminum etching recipe (<i>STS Multiplex ICP</i>)	52
3.6	Photo resist strip recipes (<i>TePla GiGAbatch</i>)	53
3.7	<i>Pfeiffer Spider 600</i> recipe parameters for SiO ₂ deposition	54
3.8	SiO ₂ etching recipe (<i>STS Multiplex ICP</i>)	57
3.9	Back side silicon etching recipe (<i>SPTS Rapier DSE</i>)	64
4.1	Total CSC values [$mCcm^{-2}$] @ scan rates [mVs^{-1}]	93

List of Figures

1.1	Number of neuroengineering articles per year, since 2005. From <i>PubMed®</i>	2
1.2	Anatomical reconstruction of an eye. From [7]	3
1.3	Overview of visual implants. a) Retinal implants; b) Optic nerve implants; c) Cortical implants [9]	5
1.4	Setup of <i>Argus II Retinal Prosthesis System</i> . From [16]	6
1.5	Spiral cuff multicontact electrode for nerve stimulation. From [21]	8
1.6	Overview of a Utah Electrode Array. From [25]	9
1.7	Cortical implant. From [26]	9
1.8	Charge injection mechanisms. Faradaic charge injection mechanism (top). Capacitive charge injection mechanism (bottom). From [43]	12
1.9	Example of a) microwire probes (MWP); b) micromachined probes (MMP); c) polymer based probes. Adapted from [32],[58],[59]	14
1.10	a)-c) MWA implants. Courtesy of <i>Microprobes for Life Science</i>	15
1.11	a) ZIF-CLIP® based array; b) Omnetics based array. Courtesy of <i>Tucker-Davis Technologies</i>	16
1.12	Examples of integration methods from literature. a) From [65]; b) From [67]; c) From [69]; d) From [61]	18
1.13	Michigan probe®. From [71]	19
1.14	Multielectrode planar probes from literature. a) From [72]; b) From [73]; c) From [74]	20
1.15	Examples of three-dimensional microelectrode arrays. a) Traditional UEA, from [80]; b) Convuluted UEA, from [77]; c) Novel USEA. Courtesy of Oregon State Univesity; d) Novel UMEA, from [80].	22
1.16	Examples of polymer probes. a) Flexible fish-bone-shaped neural probe, from [59]; b) Three-dimensional macroporous nanoelectronic network, from [82].	23
1.17	Schema of SMND cortical visual prosthesis.	25
2.1	Microfabricated CMOS chip for microelectrodes integration	27

2.2	Front side and back side of the PCB used for chip support and testing purposes. Distances in mm. [84]	28
2.3	Commercial microelectrodes characteristics. [87]	29
2.4	Available tips for monopolar microelectrode. [87]	29
2.5	Autocad (<i>by Autodesk Inc.</i>) model of SEM aperture used as microelectrode support	31
2.6	SEM acquisition demonstrating the dirtiness of manual blade cut on PtIr microelectrode	33
2.7	SEM acquisition of FIB aided cut of PtIr microelectrode at 1.5 mm. a) Overview of the cut microelectrode; b) Detail of the cut.	33
2.8	Results of manual integration of two PtIr microelectrodes on CMOS chip. a) Lateral view showing vertical orientation of microelectrodes; b) Overview of CMOS chip on PCB with integrated microelectrodes.	34
2.9	a) FIB/SEM chamber overview. (1) GIS nozzle, (2) Micromanipulator, (3) Microelectrode, (4) Substrate with SEM aperture; b) Detail of the vertical microelectrode.	35
3.1	Autocad (Autodesk Inc.) three-dimensional design of microfabricated free-floating implants. a) Final structure after fabrication process flow; b) Ready-to-implant structure after probes bending.	38
3.2	Silicon wafer after RCA process and SiO_2 deposition	42
3.3	Aluminum deposition	43
3.4	Wafers surface treatments for enhanced photo resist adhesion.[93]	45
3.5	Photo resist coating of the wafer, over the aluminum layer, after dehydration procedure.	46
3.6	Film thickness vs. rotation speed of the chuck. [93]	47
3.7	Example of cross-shaped alignment mark	48
3.8	Exposure doses for different thicknesses and exposure tools	49
3.9	Photo resist exposure following aluminum pattern layout for probes framework and alignment marks.	50
3.10	Photo resist development.	51
3.11	a) Aluminum etching; b) Remaining photo resist strip.	53
3.12	Silicon dioxide deposition on the front side of the wafer.	54
3.13	<i>EVG150</i> . Thickness-dependant contact time for photo resist automatic development. [93]	56
3.14	Silicon dioxide deposition on the front side of the wafer.	57
3.15	a) Exceeding silicon dioxide etching; b) Photo resist strip.	58
3.16	IrOx deposition on the front side.	59
3.17	IrOx deposition on the front side.	60
3.18	a) Exceeding IrOx etching; b) Photo resist strip	61
3.19	parlylene-C coating of the front side.	62

3.20	Back side photolithography. a) Photo resist coating; b) Exposure; c) Photo resist development.	63
3.21	Bosch Process illustration. [98]	63
3.22	Back side dry etching.	64
3.23	Back side SiO ₂	65
3.24	Back side dry etching.	65
3.25	Wafer design overview (Autocad, Atodesk Inc.). a) Front side; b) Back side	66
3.26	Support CMOS chip dimensions (Autocad, Atodesk Inc.)	67
3.27	First design (Autocad, Atodesk Inc.) - geometrical dimensions . . .	68
3.28	Second design (Autocad, Atodesk Inc.) - geometrical dimensions . .	69
3.29	Third design (Autocad, Atodesk Inc.) - geometrical dimensions . . .	69
3.30	Fourth design (Autocad, Atodesk Inc.) - geometrical dimensions . .	70
3.31	Details of a microelectrode tip	70
3.32	Overview of designs distribution on silicon wafer.	71
3.33	Aluminum layer deposition results. a) Detail of the tip (optical microscope); b) Detail of the tip (SEM acquisition); c) Detail of the pads (optical microscope); d) Overview of a probe (optical microscope)	72
3.34	Aluminum and SiO ₂ layers. a) Overview of a probe (optical microscopy); b) Overview of two probes (SEM acquisition); c) Exposed Al tip (SEM acquisition); d) Exposed Al pad (SEM acquisition). . .	74
3.35	Profilometer analysis conducted on fabricated probes. 3D reconstruction of the probe and 2D frontal and lateral cross-section profiles.	75
3.36	Back side alignment assessment through optical microscopy on transparent wafer holder and infra-red (IR) light from the bottom. . . .	76
3.37	Back side etching results. a) Back side view; b) Front side view; c) Back side detail of two etched structures; d) Front side detail of two etched structures.	76
3.38	Free-standing implants. a) Overview of collected structures after parylene-C removal; b) SEM acquisition of a single structure, showing total compliance with design constraints; c) Detail of the exposed tip of a structure.	77
3.39	Free standing bent structures. a),b) Single structure acquired through optical microscopy; c) SEM acquisition of a single structure	78
4.1	Example of a three electrodes electrochemical cell for electrodes characterization.[102]	80
4.2	Different Helmholtz layers in a polarized water solution. [103]	82

4.3	Typical excitation signal for cyclic voltammetry - a triangular potential waveform with switching potential at 0.8 and -0.2 V versus SCE.[106]	83
4.4	Voltammogram of the reversible reduction of a 1mM Fc^+ solution to Fc , at scan rate of 100mVs^{-1} . [107]	83
4.5	Diffusion layer shapes for a) macroelectrodes and b) microelectrodes. [109]	85
4.6	Example of a typical microelectrode voltammogram. [108]	85
4.7	EIS plot on Gold discoidal microelectrodes with diameter of $200\ \mu\text{m}$ [112]	87
4.8	A voltage transient of an AIROF (Activated Iridium Oxide Film) microelectrode in response to a biphasic, symmetric ($i_c = i_a$) current pulse. [42]	87
4.9	Electrochemical cells: a) becker setup for macroelectrodes. b) miniaturized setup - working electrode before integration. c) miniaturized setup - integrated working electrode	89
4.10	Examples of miniaturized electrochemical setups.	89
4.11	Electrochemical cell - becker setup	91
4.12	Miniaturized electrochemical cell - electrodes pierce the PBS bubble from above	91
4.13	a) CMOS chip with integrated microelectrodes; b) Miniaturized electrochemical setup for integrated microelectrodes characterization.	92
4.14	Cyclic voltammetry plot of integrated microelectrode @ S.R.=50 mV/s	94
4.15	Cyclic voltammetry plot of integrated microelectrode @ S.R.=200 mV/s	94
4.16	Cyclic voltammetry plot of integrated microelectrode @ S.R.=500 mV/s	95
4.17	Cyclic voltammetry plot of integrated microelectrode @ S.R.=1000 mV/s	95
4.18	Cyclic voltammetry plot of integrated microelectrode @ S.R.=5000 mV/s	96

Acronyms

AIROF

Activated Iridium Oxide Film

AMD

Age related Macular Disease

CIL

Charge Injection Limit

CMI

Center of Micronanotechnology

CMOS

Complementary Metal-oxide-Semiconductor

CNT

Carbon Nanotubes

CSC

Charge Storage Capacity

CV

Cyclic Voltammetry

CVD

Chemical Vapor Deposition

DI

De Ionized (water)

DRIE

Deep Reactive Ion Etching

EIS

Electrochemical Impedance Spectroscopy

EPD

End Point Detection

ESA

Electrochemical Surface Area

FIB

Focused Ion Beam

GIS

Gas Injection System

GSA

Geometrical Surface Area

HMDS

Hexamethyldisilazane

IBE

Ion Beam Etching

ICMS

IntraCortical MicroStimulation

ICP

Inductively Coupled Plasma

IMI

Intelligent Medical Implant

IRIS

Intelligent Retinal Implant System

ITO

Iridium Thin Oxide

MEA

MicroElectrode Array

MMP

Micromachined Probe

MWA

Microwire Array

MWCNT

Multi-Walled Carbon Nanotubes

MWP

Microwire Probe

NHE

Normal Hydrogen Electrode

NP

Neural prosthesis

PBS

Phosphate-Buffered Saline

PCB

Printed Circuit Board

PDMS

Polydimethylsiloxane

PECVD

Plasma Enhanced Chemical Vapor Deposition

PEDOT

Poly(3-4-ethylenedioxythiophene)

PMMA

Polymethyl methacrylate

PR

Photo Resist

RCA

Radio Corporation of America

RF

Radio Frequency

RP

Retinitis Pigmentosa

SAR

Specific Absorption Rate

SCE

Saturated Calomel Electrode

SEM

Scanning Electron Microscopy

SHE

Standard Hydrogen Electrode

SIROF

Sputtered Iridium Oxide Film

SMND

Smart Micro Neural Dust

SOI

Silicon On Insulator

UEA

Utah Electrode Array

UMEA(1)

Utah Multisite Electrode Array

UMEA(2)

Ultra MicroElectrode Array

USEA

Utah Slanted Electrode Array

UV

Ultraviolet

VCS

Visual Cortex Stimulation

VPU

Video Processing Unit

VT

Voltage Transient

WFMEA

Wireless Floating Microelectrode Array

Chapter 1

Introduction

The nervous system can be defined as the “engine” of our body. It is the centralized node through which information is processed and dispatched to peripheral districts. The scientific community has been concentrating its effort on the development of novel devices for mitigating Parkinson’s Disease, epilepsy symptoms and for restoring highly impairing disabilities, such as blindness or deafness. The new frontiers of bio-sciences are moving more and more towards innovative solutions whose aim is to provide an improvement in people’s health and wellness. Engineering has a crucial role in the realization of these solutions, as it brings multidisciplinary knowledge, especially from the medical, electronics, software, mechanics, and material fields. Interest in neuroscience dizzyingly increased in the last twenty years, as stated by *PubMed*®, one of the biggest American free resources, property of the *NIH (National Institutes of Health)*, which collects all the literature works from life sciences world. It clearly shows that in 2005 the number of articles on the topic “neuroengineering” was 21, while at the end of 2021 was 224 1.1. With regard to implantable neural devices, some of them are also known as *neural prostheses* (NPs). A neural prosthesis can be defined as a "*device that uses electrodes to interface with the nervous system and aims to restore a function that has been lost*" [1]. There exist different types of NPs with different purposes. Their development has been made possible, thanks to the accumulated scientific knowledge, driven by an ever-increasing effort to define more and more complex biophysical models for body subsystems [2]. One must consider the concept of the neuroprostheses in their broader sense, being aware that the term includes all those devices which have a direct effect on either CNS (Central Nervous System) or the PNS (Peripheral Nervous System). For this reason, they must follow some strict rules and fulfill several criteria, in order to be implanted. Specifically, they must be biocompatible, thus they do not have to cause adverse reactions on the implant site. Moreover, they must be durable, electrically and mechanically safe and cost-effective [3]. The first developed neural prostheses are related to the PNS (Peripheral Nervous

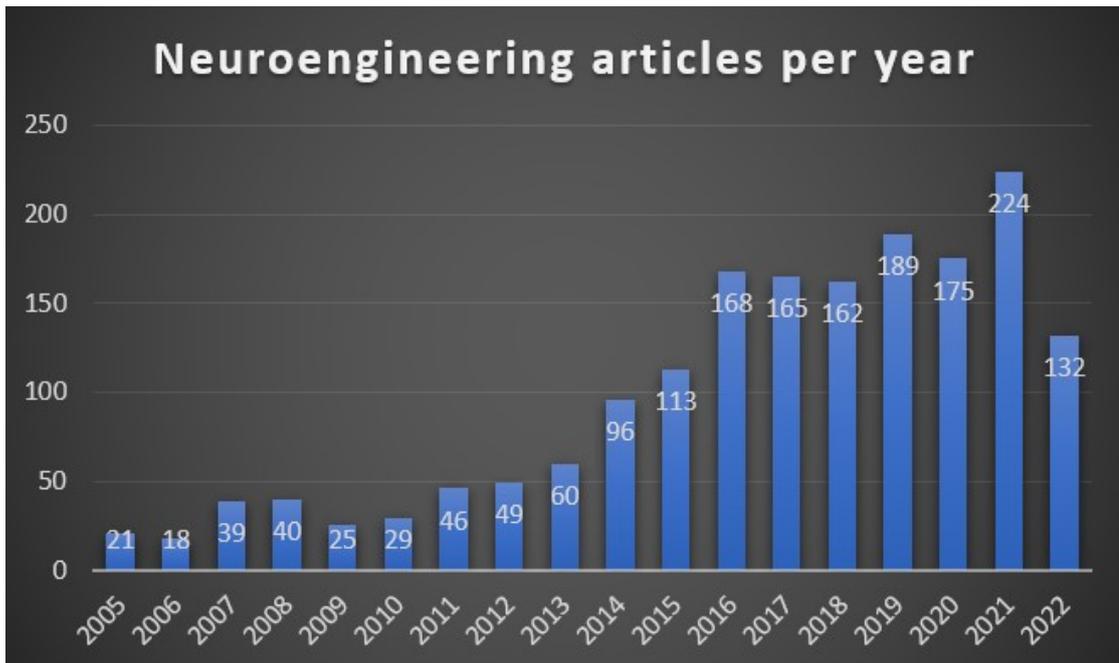


Figure 1.1: Number of neuroengineering articles per year, since 2005. From *PubMed*®

System). In particular, *spinal cord microstimulation* is one of the most valuable achieved results. In fact, several physiological functions can be controlled, modified, and recovered through spinal cord stimulation, such as voluntary muscles, bladder, and bowel impairments [4]. With innovations and progress in leaps and bounds in neuroengineering, research expanded its knowledge also to the recovery of "central" functions, thus involving the direct stimulation of brain areas. In this scenario, it is worth mentioning brain stimulators to recover from two of the most widespread and common impairments: deafness and blindness. With regard to deafness, according to the official data from the WHO (*World Health Organization*), more than 1.5 billions people worldwide (nearly 20% of the total population) live with hearing loss, with the number expected to dramatically increase until 2.5 billion by 2050 [5]. Consequently, cochlear implants are, up to now, the most advanced and used neural prostheses, directly implanted under the skin and in contact with the cochlea, through dedicated electrodes. Another dramatic impairment concerns sight, with around 2.2 billion people worldwide with eyesight problems, from lighter ones to totally disabling ones [6]. Based on the level of impairment of the structures responsible for the eyesight, several prosthetic alternatives with different degrees of invasiveness exist.

1.1 Visual Prostheses - State of the Art

The large number of people affected by sight impairment pushed the neuroengineering research to find new solutions to enable at least a partial recovery, where possible. However, it is dutiful to make some distinctions among blindness conditions. First of all, visual impairments are characterized by different degrees of intensity, from a few minor flaws to a complete impairment, which strongly affects the patient's life. To better understand how the mechanism of sight works, it is appropriate to make a concise description of it. In brief, (figure 1.2) light, first, hits the cornea; then part of it passes through the pupil and part through the iris, which controls the amount of light allowed to pass into the pupil. After that it is conveyed to the lens, which represents the innermost part of the eye and, together with the cornea, it contributes to correctly focusing the light to the retina. Finally focused light hits the retina, which is made of photoreceptors, responsible for converting light itself into an electrical signal. The latter is, then, conveyed to the optical nerve, thus to the brain, where it is modulated, generating the image [7].

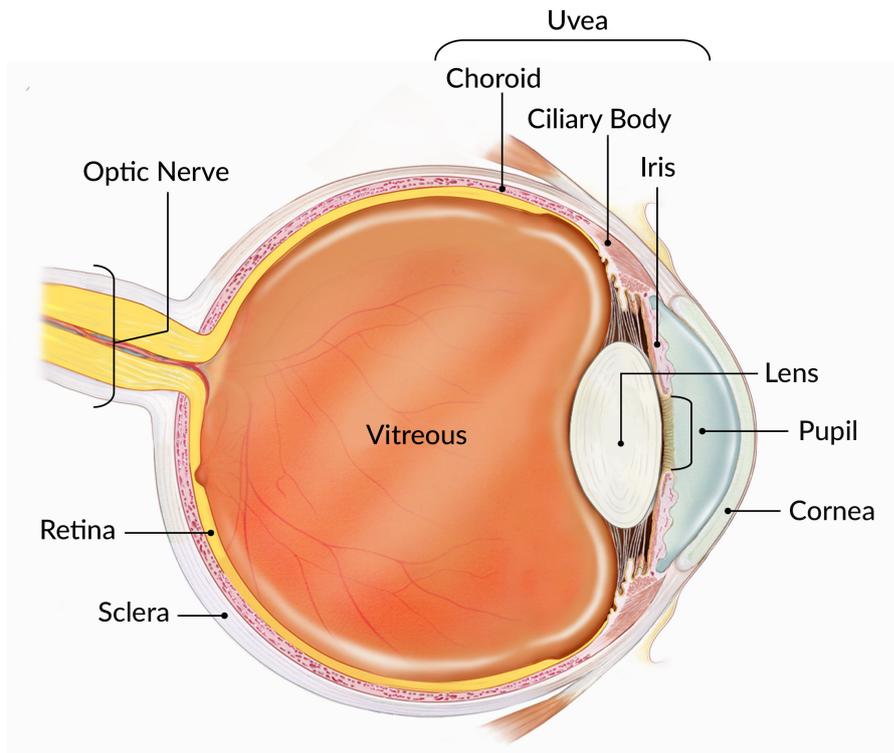


Figure 1.2: Anatomical reconstruction of an eye. From [7]

Leaving aside the most common sight problems such as farsightedness, nearsightedness, astigmatism, and presbyopia, which can be treated more easily, as they only affect the first structures of the eye, the core of the analysis is focused on all those diseases that can lead to total blindness. The most common diseases which start affecting the retina and continue affecting the optic nerve with time are *age related macular degeneration (AMD)*, *retinitis pigmentosa (RP)* [8] and *glaucoma*. Whenever the problem is related to the retina, several approaches have been investigated, and numerous solutions have been developed. Merabet et al. in [9] give a synthetic overview of the possibilities of implants, based on the level of the damage. They propose three main approaches:

- *Retinal approach*. This approach has been designed to replace the lost photoreceptors in the retina, when all the other structures, such as the optic nerve, are intact. Moreover, there are multiple configurations for retinal implants, based on the level of damage and on the stability of the layers (figure 1.3a).

- *Optic nerve approach*. It is preferred when the majority of proximal visual structures are maintained. The retina is bypassed, thus optical nerve is directly stimulated, and the electrical signal can be conveyed to the visual cortex in the brain (figure 1.3b).

- *Cortical approach*. This last approach is used in all those cases where no intact structures are present, so both the retina and nerve must be bypassed. Stimulation, thus, happens directly in the brain's visual cortex. In fact, it has been demonstrated that proper cortical stimulation generates the so-called *phosphenes*, which are defined by [10] as "*sensation of a spot of light in the visual field*" (figure 1.3c).

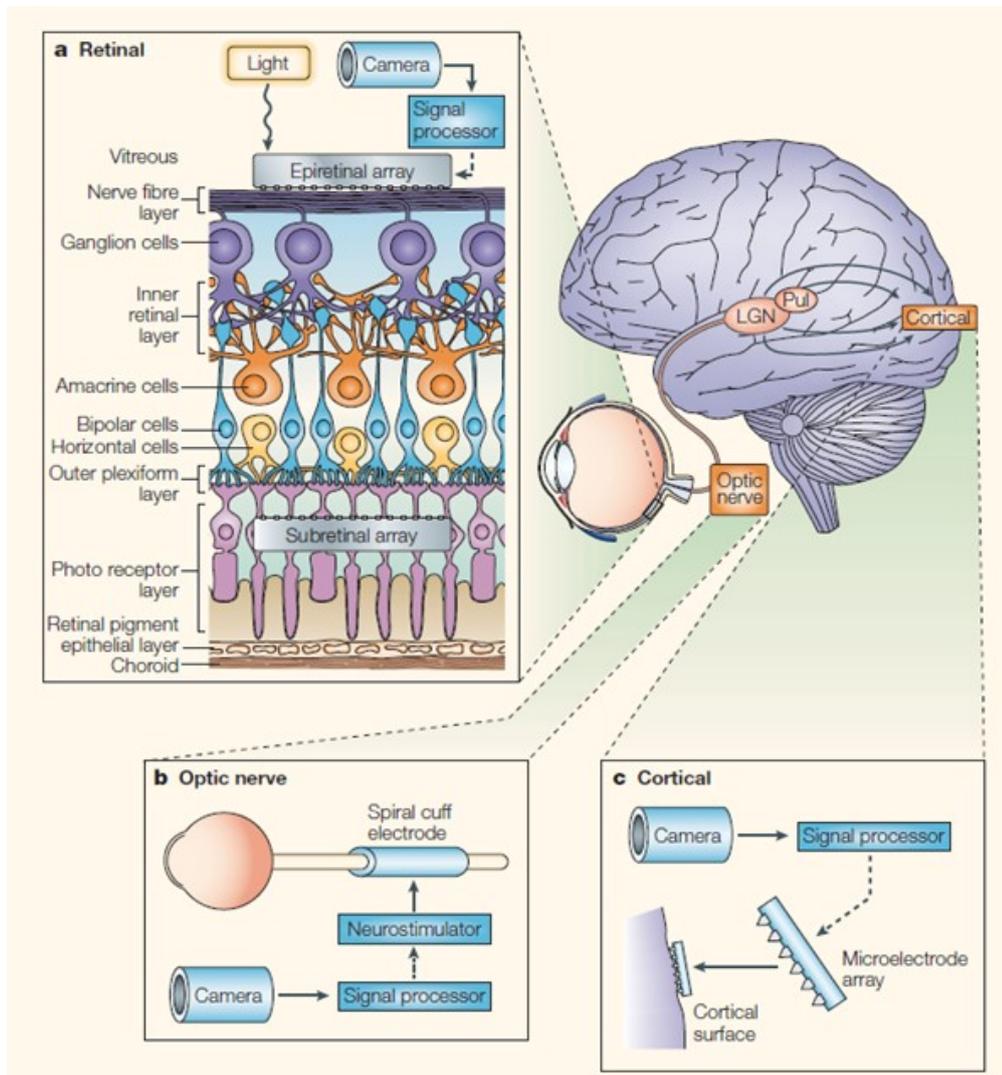


Figure 1.3: Overview of visual implants. a) Retinal implants; b) Optic nerve implants; c) Cortical implants [9]

The general concept of a visual prosthesis involves the presence of a video camera for image capturing; images information is, then, processed and translated into an electrical signal through a processing unit; signal is, in the end, modulated and sent to the implanted MEA (Microelectrode Array), deputed to the stimulation of the district where the implant is inserted [11].

1.1.1 Retinal Implants

Retinal implants are the most developed and widely implanted visual prostheses since they are less invasive and the related implant surgery is almost routine for eye surgeons. Retinal prosthesis can be further divided into subgroups, based on the location of the implants: *epiretinal*, *subretinal* and *suprachoroidal* prostheses.

Epiretinal Prosthesis

An *epiretinal implant* is, generally, implanted near the surface of the neurosensory retina adjacent to the nerve fiber and ganglion cell layers [12]. The most worldwide developed and famous epiretinal implant is the *Argus II Retinal Prosthesis System*, which works collecting an image of the external environment through a camera; the image is processed by a VPU (Video Processing Unit) and the related information is wirelessly transferred to the implanted structure and subsequently to the epiretinal MEA (Microelectrode Array) [13]. Figure 1.4 shows a typical setup of the *Argus II Retinal Prosthesis System*. A similar approach was also developed by the company *Intelligent Implants GmbH*, with the *Intelligent Medical Implants (IMI)*. The working principles are almost the same, since an external image is first generated, then processed and, finally, an electrical signal is sent to the retina through an epiretinal MEA [14]. Several other examples of epiretinal implants exist, such as *Intelligent Retinal Implant System II (IRIS II)*, proposed by the company *Pixium Vision S.A.* [12] or again the *EPI-RET3 Retinal Implant System*, developed by Koch et al. [15].

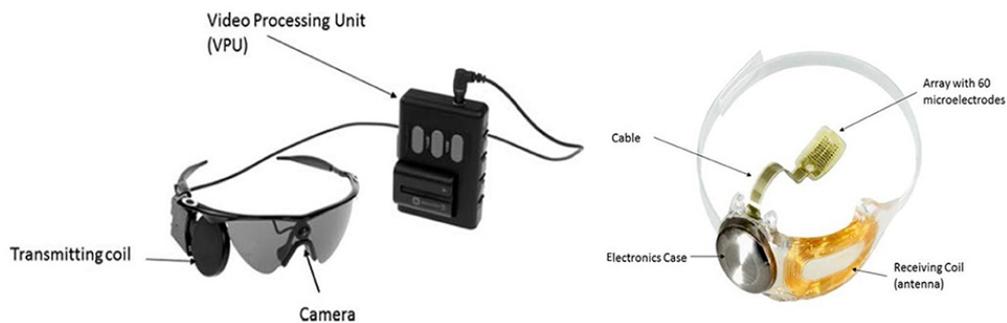


Figure 1.4: Setup of *Argus II Retinal Prosthesis System*. From [16]

Subretinal Implants

According to [12], subretinal implants can exploit some advantages, with respect to the epiretinal ones, such as the reduced stimulation intensity, since the device is implanted closer to the retina. Moreover, positioning the device nearby the damaged Photo Receptors allows us to take advantage of the intrinsic signal processing

capacity of retinal neurons, thus less demand for image processing is required. Moreover, the surgical procedure is more challenging, since it does not belong to the routine retinal surgery [12]. The design of the overall system is very similar to the epiretinal implants. The most developed implants are the *Boston Retinal Implant* developed by *Boston Retinal Implant Project (Boston, Massachusetts, United States)* [17], the *Artificial silicon retina*, developed by *Optobionics (Glen Ellyn, IL, USA)*, which is the first attempt in the realization of a passive prosthesis, activated by ambient light [18]. Finally, *Alpha IMS*, with its iteration *Alpha AMS*, developed by *Retina Implant AG (Reutlingen, Germany)* and *Photovoltaic Retinal Implant (PRIMA) bionic vision system*, developed by *Pixium Vision S.A.* are noteworthy.

Suprachoroidal implants

Suprachoroidal implants represent the third alternative for visual prosthesis implant location. As we can notice from figure 1.3, the choroid is the external layer, thus the first advantage is that the surgical procedure does not involve any vitrectomy or retinal incision, with the subsequent risk of damaging the retina itself. On the other hand, the major drawback concerns the distance to the ganglion cells, thus the higher demand in stimulation power, than in epiretinal and subretinal implants [19]. As for the aforementioned described implants, the current system preserves the same pattern in terms of involved parts and working principles. The location of the MEA is the real difference and, accordingly, the stimulation parameters. *Bionic Vision Australia* team developed a series of suprachoroidal implants prototypes [12] in 2019. Moreover, *Japan's Artificial Vision Project*, in conjunction with NIDEK, is currently developing the *suprachoroidal-transretinal stimulation (STS) system*, a very promising solution.

1.1.2 Optic nerve implants

The optic nerve approach is a valid alternative in patients where the proximal structures of the eyes are completely damaged, such as the retina. If the optic nerve is intact, it can be directly stimulated, and the signal can be conveyed to the visual cortex, where it is processed. The working principle of these prostheses is the same as described for the retinal implants, thus stimulating a specific site where the signal is directly generated from the external image acquired with a camera. As mentioned in [20] by Veraart et al., Retinal Ganglion Cells (RGCs) are not stimulated straight on the retina, at cell body level, but through their axonal fibers along the optic nerve. For this purpose, a spiral cuff multi-contact electrode is wrapped around the nerve, so all the fibers can sense the stimulation and the signal can reach the specific cortical area of the brain. Figure 1.5 shows an example

of a standard spiral nerve cuff electrode, normally used for nerve stimulation.

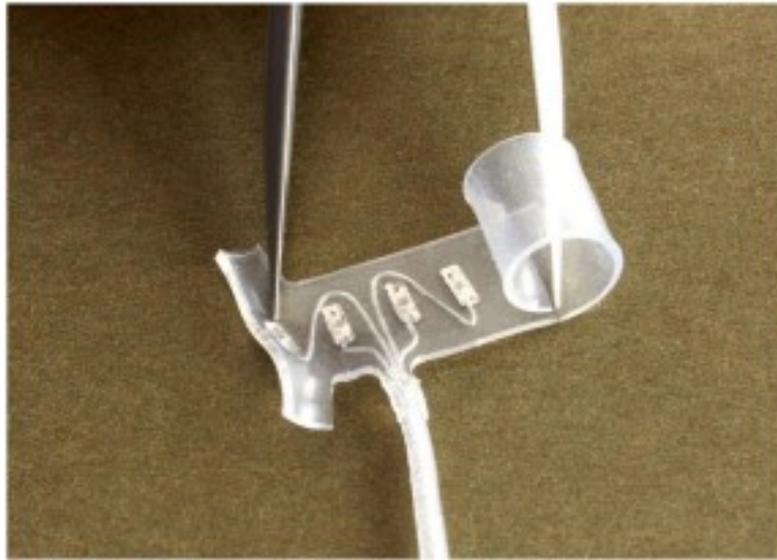


Figure 1.5: Spiral cuff multicontact electrode for nerve stimulation. From [21]

1.1.3 Cortical implants

Cortical implants represent the ultimate solution in those cases characterized by complete damage of all the proximal and distal structures involved in the sight. In this application, the retina and optic nerve must be bypassed, so the stimulation happens directly on the brain's visual cortex. In this scenario, the concept of penetrating electrodes for intracortical microstimulation (ICMS) acquires great importance. Visual Cortex Stimulation (VCS) refers to a precise stimulation area, which is located in the primary visual cortex, in layer 4-C of V1 [22]. Since the working principles are the same as described for retinal and optic nerve approaches, the only remarkable difference is represented by microelectrodes, which, normally, refer to the famous *Utah Electrode Array (UEA)* [23], which takes its name from the University where it was developed. It consists of a silicon-micromachined structure, which allows the implantation of a great number of microelectrodes in small regions of the cerebral cortex, allowing for an increase in the selectivity of the stimulation. In terms of geometry and design, it is made of 100 microelectrodes, highly densely packed on a 16 mm^2 support. The UEA is derived from a $4.2 \times 4.2 \times 0.2 \text{ mm}^3$ square-based silicon substrate; the one-hundred 1.2 mm long needles are organized in a 10×10 grid. The interaction between the microelectrodes and the surrounding tissues is ensured by a multi-layer coating structure represented by Platinum-Titanium-Tungsten-Platinum. The single needles are coated with Polyimide, leaving only 50

μm of tip free to deliver charge [24].

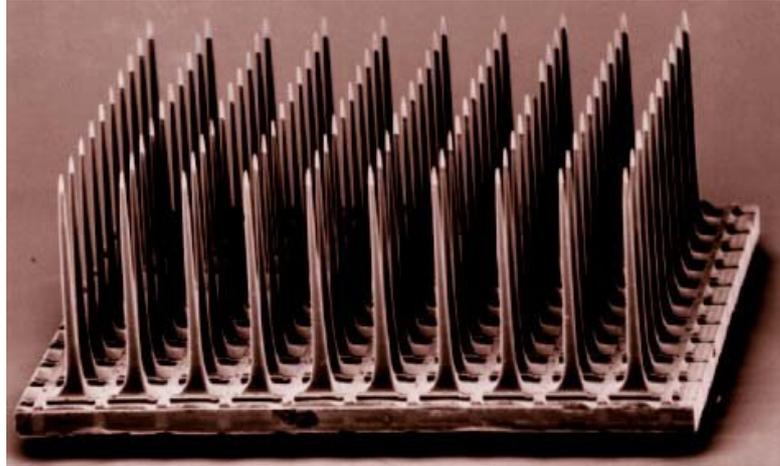


Figure 1.6: Overview of a Utah Electrode Array. From [25]

In general, cortical implants are the newest, temporarily speaking. Moreover, they are deeply attractive from new frontiers in brain stimulation point of view, since they must meet several strict requirements, such as biocompatibility, biostability, mechanical integrity, and functional stability. In this scenario, the portion of covered visual cortex by the implant, as well as the density of microelectrodes are two crucial aspects to take into consideration, since they are responsible for the number of generated phosphenes. The variation of two mentioned aspects can lead to a more or less detailed perception of an object. By increasing the covered visual cortex region and the number of microelectrodes, the spatial selectivity increases and, consequently, the quality of the generated image. Figure 1.7 illustrates the typical implant location of a visual prosthesis.

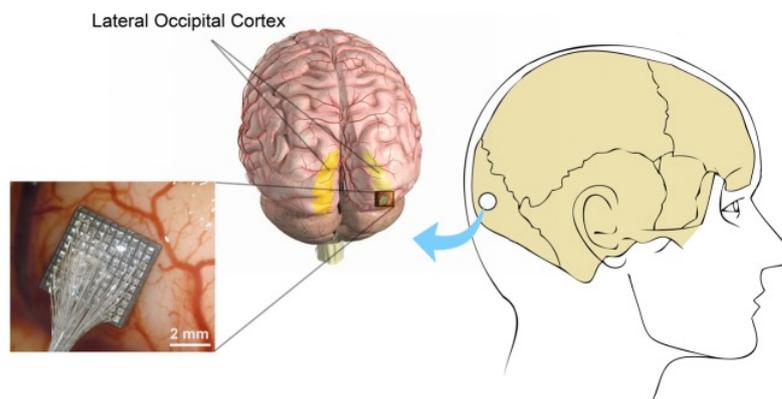


Figure 1.7: Cortical implant. From [26]

The literature proposes some reviews [26] on the most important and noteworthy devices for intracortical visual neurostimulation. Dobbelle et al. are one of the first research groups to focus on cortical implants to revert blindness in 1968 [27]. In 2000, the *Illinois University of Technology* created a new project for neural prostheses, called *Intracortical Visual Prosthesis Project (ICVP)*, which maintained the classical cortical stimulation method, but with the novelty of wireless communication between the external system and the implant, defined as a *Wireless Floating Microelectrode Array (WFMEA)* [28]. Moreover, also the Commission of the European Communities contributed to the development of a visual cortical prosthesis, *CORTIVIS* [29], which takes advantage of the benefits of UEA. In addition, *Monash Vision Group*, together with the *Australian Research Council*, developed the *Gennaris* bionic vision system, which is very similar to the mentioned ICVP. In the end, *Orion*, developed by *Second Sight Medical Products*, worths a mention, since it involves a subdural electrode grid, unlike the previously described devices which involve the implant being fixed on the surface of the cortex.

1.2 Microelectrodes basic requirements for neural implants

As mentioned, microelectrodes are a crucial and fundamental part of the overall stimulating system, since they are responsible for delivering the stimulation pulse properly to the surrounding tissues. Accordingly, since implants are thought to remain in place for long periods of time, long-term stability and viability must be optimized [30]. One of the first properties to assess and to be ensured is biocompatibility. In fact, it must be guaranteed from the early stages of the implant, during insertion, as well as during the whole working period. Biocompatibility involves three crucial sub-concepts: *Biosafety*, *Biofunctionality* and *Biostability* [31]. Therefore, the implant must not harm the surrounding tissues and the body where it is hosted; it must perform the function it has been designed for, and it must not be susceptible to biological attack from the host body. A possible helping solution to improve biocompatibility would be to minimize the amount of materials in contact with tissues, thus miniaturizing the implants and taking advantage of wireless communications. In fact, Lehew et al. in [32] demonstrated that neurodegeneration is significantly reduced for free-floating implants, instead of tethered implants. Moreover, also some mechanical and electrical properties must be met, and they strongly depend on the design constraints and selected materials. In particular, Harris et al. in [33] suggest the use of materials that are initially stiff enough to be able to penetrate the cortex, but then they should become more mechanically compliant to match the stiffness of the brain tissues. Moreover, the usage of soft material with an elastic module similar to the cerebral

tissue one may help to reduce tissue damage due to brain micromotion [34][35][36]. Lee et al. in [37] demonstrated that the usage of specific coatings might promote better electrode integration in the host tissue. Finally, the shape has not to be forgotten, since for cortical implants penetrating electrodes must be used. As for electrical properties, these are very dependent on the interaction between the used materials and surrounding tissue, on time elapsed from implantation, and on the shape of the conductive framework of a microelectrode. Therefore, one of the most important parameters to define is the maximum value of complex impedance at the stimulation signal frequency. According to [38], Sankar et al. demonstrated that for tungsten microwires the best stimulation yield is achieved when the overall impedance at 1 kHz is 40-150 $k\Omega$. Normally, due to the biological response of the tissues, the overall impedance value tends to grow over time, but for good working conditions it should always be lower than 1 $M\Omega$ [39]. Impedance is also directly connected with heat generation, and SAR (Specific Absorption Rate) is a crucial related parameter. It is regulated by the *Federal Communications Commission* and defined by the latter as the "*measure of the rate of RF (radiofrequency) energy absorption by the body from the source being measured*". SAR values are limited by the IEEE standards to 0.08 W/kg for whole body exposure, and 2 W/kg for localized exposure [40]. The suggested SAR value is 1.6 W/kg for RF radiation from 3 kHz to 300 GHz [41]. Since the stimulation is in the RF range, impedance plays a critical role in dissipating energy, thus increasing local tissue temperature. If SAR limits are met, the increase in local temperature does not affect the surrounding tissue.

1.3 Microelectrodes materials

Materials are a crucial aspect to consider for microelectrodes since they are responsible for mechanical, electrochemical, and stimulation properties. In fact, it is appropriate to differentiate electrode materials in two groups, based on *charge injection mechanism*, thus on the way charge is exchanged at the electrode-tissue interface. Two ways microelectrodes can exchange charge with the surrounding tissue are described: *capacitive* and *faradaic* charge injection mechanisms [42] (figure 1.8).

1.3.1 Faradaic charge injection materials

Materials belonging to this category mediate the transition from electron flow in the electrode to the ion flow in the tissue through *faradaic reactions*. It means that chemical species at the electrode-tissue interface are continuously oxidized and reduced. Therefore new species are created, and some others are consumed by the mentioned reactions. Generally, faradaic materials can provide a higher level of

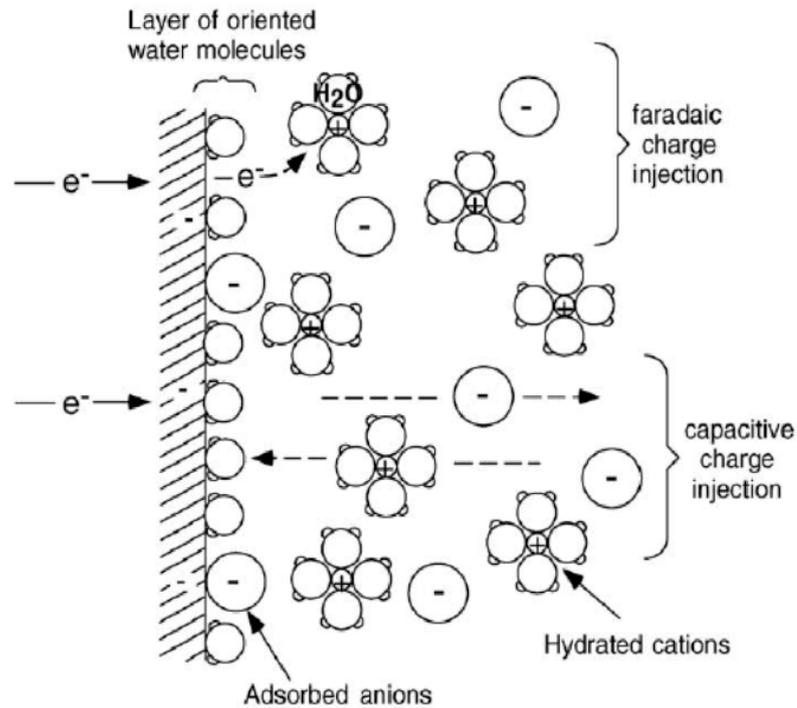


Figure 1.8: Charge injection mechanisms. Faradaic charge injection mechanism (**top**). Capacitive charge injection mechanism (**bottom**). From [43]

charge available for stimulation [42]. One of the most important categories of materials that exploit a faradaic behavior is noble metals. They can inject charge taking advantage of both the mechanisms, even if the faradaic is predominant. Among the others, Pt and PtIr are the most noteworthy, since they have attractive electrical properties for stimulation, such as the high *charge injection limit (CIL)*, which is synthetically defined by [44] as "*the maximum charge density ($mC\ cm^{-2}$) that an electrode can inject before reaching the water electrolysis potential*". The latter is the potential at which water dissociates into hydrogen and oxygen. Several studies were carried out to electrochemically test such materials in vitro [45] [46][47][48] and in vivo [49][46][50]. Iridium oxide is one of the most used materials for coatings since it can provide exponential growth in CIL in noble metal microelectrodes. In detail, based on how the IrOx film is deposited, it can become *AIROF (Activated IRidium Oxide Film)* or *SIROF (Sputtered IRidium Oxide Film)*. AIROF is obtained by growing of a thin layer of oxide on the Ir film through a cyclic session of reductions and oxidations. On the other hand, SIROF is obtained through Ir sputtering in a high-energy oxidizing plasma. Advantages of the use of IrOx are described by Slavcheva et al. in [51], by Cogan et al. in [52] and Wessling et al. in [53].

1.3.2 Capacitive charge injection materials

The capacitive charge injection mechanism involves the continuous charge and discharge of the species at the electrode-tissue double-layer interface. This mechanism is slightly more desirable than the previously mentioned one since it does not involve the creation or consumption of species. Titanium nitride is the first investigated material for microelectrodes which exchanges charges with surrounding tissues capacitively. In particular, TiN achieves optimal values of injected charge when the surface is rough. It means that the GSA (Geometrical Surface Area), which is the real extension of a microelectrode, is smaller than the ESA (Electrochemical Surface Area), which is the actual surface that contributes to the exchanges of charge. Porous TiN has been studied by Guyton and Hambrecht in [54] and by Rose et al. in [55]. Cogan et al. [42] also suggest that TiN coating is characterized by intrinsic mechanical and chemical stability. Another important material to mention is Tantalum/Tantalum oxide. In fact, the use of a dielectric can increase the charge injection capabilities. As for TiN, a high ESA/GSA ratio is required, as mentioned in [56].

1.3.3 Polymeric materials

Until now, only metallic materials have been discussed. Therefore, it is advisable not to forget about new emerging *Polymeric conductive materials*, such as Poly(3,4-ethylenedioxythiophene) (PEDOT) which is characterized by great chemical stability and is fully compatible with in vivo stimulation purposes, as demonstrated by Vazquez et al. in [57]. Variants of doped PEDOT exist, such as the PEDOT/PSS (Poly(4-styrenesulfonic) acid) or PEDOT/MWCNT (Multi-Walled Carbon Nanotubes). Having mentioned CNT, carbon materials are dramatically acquiring importance, since they are characterized by intriguing electrical, chemical, and mechanical properties, which label them as potential candidates for novel stimulation implants.

1.4 Types of microelectrodes

The most important materials for microelectrodes have, now, been mentioned. Therefore it is appropriate to make a distinction among the most used types of penetrating microelectrodes for neural stimulation. They are mainly divided into three groups, as shown in figure :

- Microwire probes (MWP) (fig. 1.9a)
- Micromachined probes (MMP) (fig. 1.9b)

- Polymer based probes (fig. 1.9c)

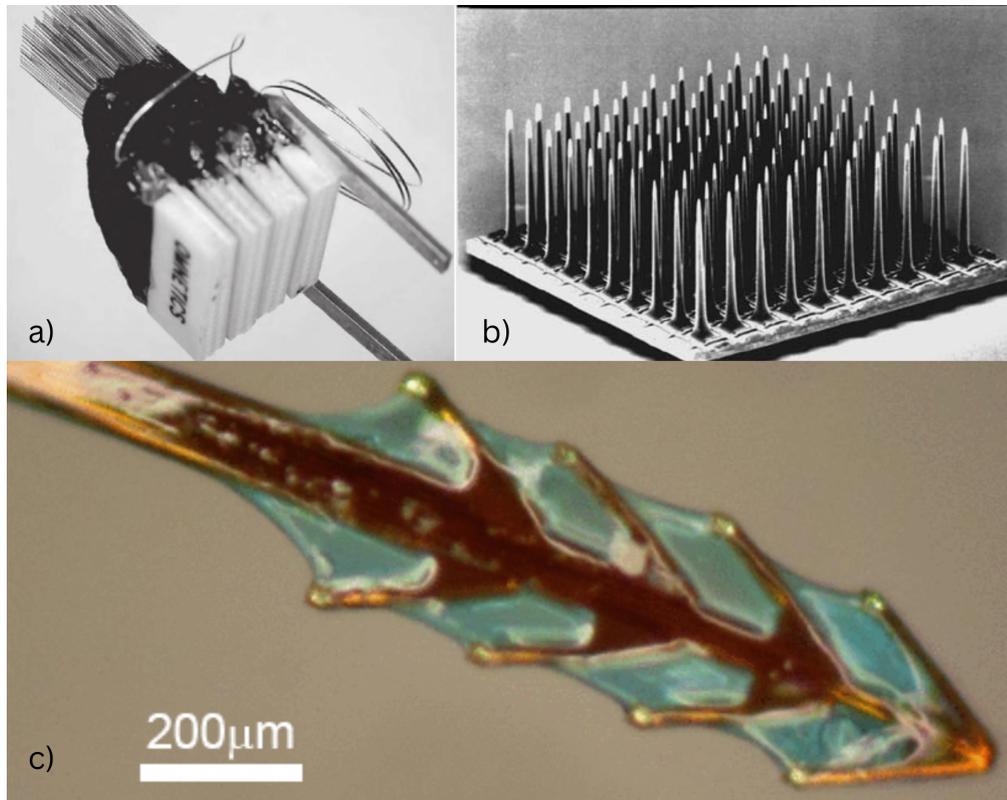


Figure 1.9: Example of a) microwire probes (MWP); b) micromachined probes (MMP); c) polymer based probes. Adapted from [32],[58],[59]

1.4.1 Microwire probes (MWPs)

Microwire probes are the first ever developed probes for stimulation purposes. In fact, the very first example of MWP dates back to the twentieth century, when both recording and stimulation studies were approached with silver-based probes [60]. The latter are suitable for implants in rodents, birds, and larger animals. The common approach of neurostimulation involves the development of arrays of microwires, to increase selectivity, as well as to cover a higher area to stimulate. Therefore, most of the times, implants require microwire arrays (MWAs), which consist of a repetition of the same single MWP. Nowadays, several neural implants have been developed using MWP and MWA technology [61][62][63]. The latter are obtained by integrating two components together: wires and connectors. Normally, wires and connectors can be bought from official vendors, based on the requirements of the implant and they are, then, integrated. Commercial applications are available,

like MWAs proposed by *Microprobes for Life Science* (18247 Flower Hill Way D, Gaithersburg, MD 20879, United States) (figure 1.10), or like the *ZIF-CLIP*[®] based electrodes (figure 1.11a) and *Omnetics* based electrodes by *Tucker-Davis Technologies Inc.* (11930 Research CIR, Alachua, FL 32615, United States) (figure 1.11b). It

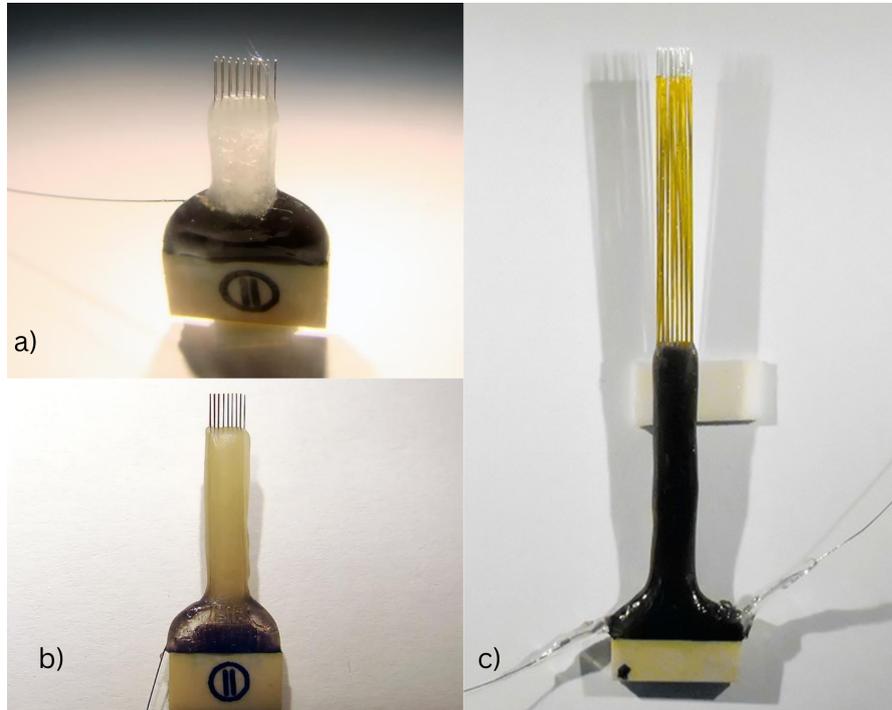


Figure 1.10: a)-c) MWA implants. Courtesy of *Microprobes for Life Science*

is essential to clarify that when we refer to microwires, microelectrodes with a base diameter ranging from $10\ \mu\text{m}$ to $200\ \mu\text{m}$ are intended. The development of these implants from scratch requires a specific sequence of processes, resumed in [64]:

- Wire cutting
- Wire straightening
- Tip sharpening
- Wire insulation deposition
- Tip deinsulation
- Array assembly

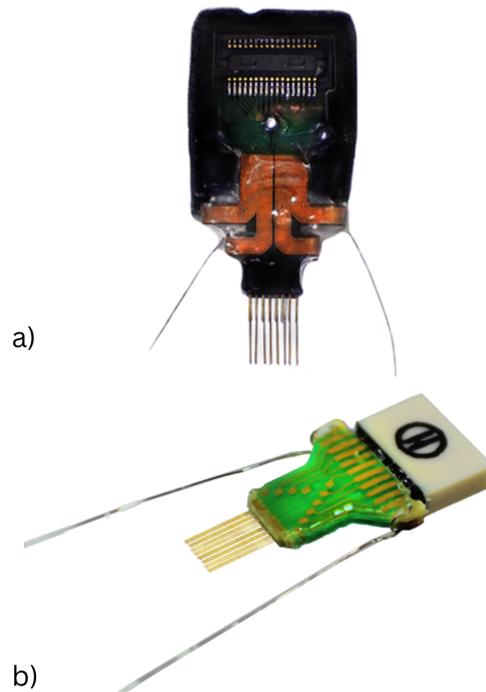


Figure 1.11: a) ZIF-CLIP[®] based array; b) Omnetics based array. Courtesy of *Tucker-Davis Technologies*

Array assembly

Among the aforementioned processes, the array assembly is the most crucial and challenging step, in order to obtain the final implantable device. Literature provides several approaches that have been tried to assemble microwires with connectors. As already mentioned, the first official integration trial example is brought by [60] in the early '20s. Rheinberger et al. obtained fine silver electrodes from a $500\ \mu\text{m}$ diameter wire, making one end of the microelectrodes rounded, by heating. The whole array has, then, been insulated, leaving one extremity free. Once the silver microwires were implanted, they were, then, connected to Litz wires and bound together to a harness and a leash to make them simultaneously implantable on the cortex of a cat. This configuration allowed the cat to fully and rapidly recover from the surgery. In [65], Schmidt et al. propose a study on 50 blind implanted individuals. For visual selective intracortical microstimulation (ICMS) they created a dual hat-pin microelectrode. It was made by two 3 mm-long Iridium wire, with a diameter of $37.5\ \mu\text{m}$, and the tip covered in AIROF. They were, then, connected to a $25\ \mu\text{m}$ gold wire with tens of millimeters of free length. Gold wires were wrapped with stainless steel teflon-coated wires. The connection between the

Iridium wires and the gold was achieved by welding, while the whole structure was connected to a miniaturized printed circuit through silicone tubes (figure 1.12)a. In 1999, Williams et al. [66] developed a protocol for chronic multi-site recording and stimulation on awake animals, for more than three months. The protocol also involved the fabrication of a microelectrode array. In detail, it consisted of 33 microwires arranged in three rows. They were made of 35 μm diameter tungsten with 7 μm polyimide insulation. The assembling procedure was achieved using an electrode jig, which could help to maintain a constant spacing for the wires. Each of them was cut into an 8 cm-long unit and placed on the mentioned dedicated jig; it was then used to place the wires into the connector, while polymethyl methacrylate (PMMA) is dispensed among the electrodes to maintain the current spacing among each other and to provide enhanced rigidity to the structure. This operation is repeated for the three rows and, finally, a thin layer of epoxy is dispensed on the whole assembled array to consolidate the connection. In 2001, Ulbert et al. [67], developed a thumbtack linear multielectrode array (figure 1.12)b. PtIr (90/10%) rounded microelectrodes are located on a polyimide shaft and separated by 25 μm . The shaft is perpendicularly attached to a silicone sheet to stabilize and control the shaft insertion. Two years later, Nicolelis et al. [68] worked on the development of a multi-site, multi-electrode recording in macaque monkeys. In detail, they used chronically implanted microwire arrays. The whole system involves Teflon-coated tungsten microwires, a printed circuit board (PCB) and a high-density miniaturized connector. The PCB-microwires connection is achieved through an adhesive epoxy. It is also worth mentioning the work by Merlo et al. [69], where in 2012 they developed a novel hybrid non-lithographic microfabrication method to assemble a multi-electrode epoxy insulated shank to a PCB (figure 1.12)c. In 2020, Obaid et al. [61] developed a novel mechanical integration technique for microwires. To summarize the whole procedure, they take insulated microwires of different materials, such as Au, PtIr, and W; the latter are covered in a sacrificial layer of Parylene-C to provide inter-electrode spacing; tips are, then, prepared with a sharp shape and wires are bundled together with the help of a biomedical epoxy, leaving the distal part free. The proximal part of the wires is polished, to make them ready to be connected to a CMOS substrate. Bonding is mechanical; in fact, the whole structure is pressed against the CMOS substrate, making the proximal extremities of the wires bend and firmly fix on the dedicated pads (figure 1.12d). A very similar approach is repeated by Kollo et al. [70].

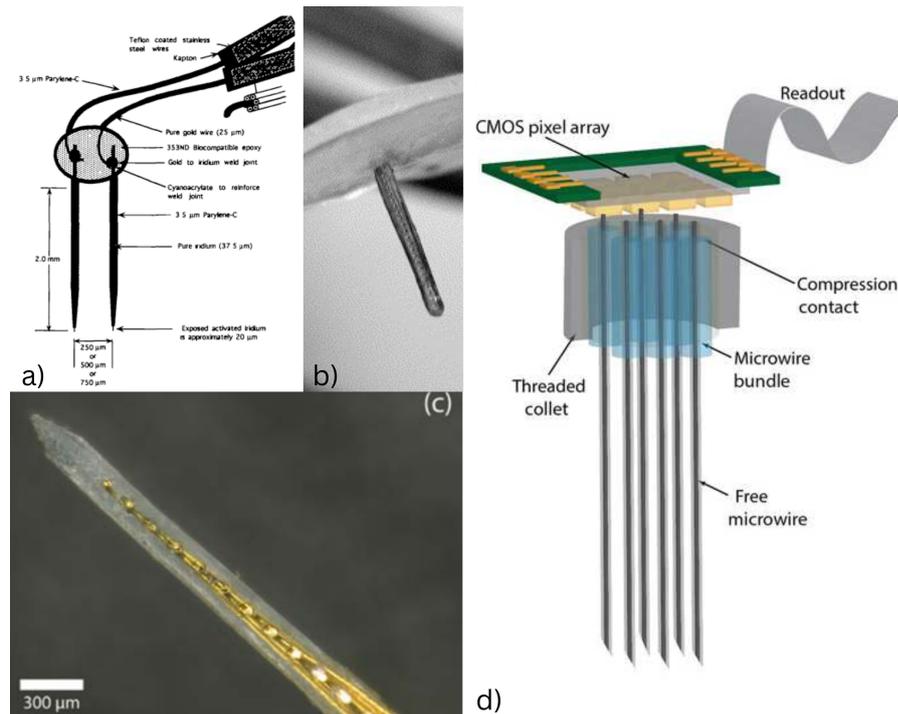


Figure 1.12: Examples of integration methods from literature. a) From [65]; b) From [67]; c) From [69]; d) From [61]

1.4.2 Micromachined probes (MMP)

The second investigated example of microelectrodes is the micromachined probes. In fact, as its name suggests, their production is strictly related to silicon-based microfabrication processes, which, among others, include material deposition, photolithography, and etching. MMPs have been widely developed as an alternative to MWP and MWA and they have been thought to be used for human implant purposes. The first reason is deputed to the dramatic reduction in the size of the probes. Therefore, it means that implants can be miniaturized, resulting in less invasive systems. The second convenient aspect is represented by the simultaneous microelectrode arrays (MEAs) fabrication and CMOS embedded electronics one. This allows skipping the integration steps mentioned for microwires. In summary, the innovation is the possibility of working with wireless free-floating miniaturized neural implants. In general, MMPs can be divided into two main categories, based on the geometry and shape, following two cornerstones in microelectrodes:

- 2D Michigan-style probes
- 3D Utah-style MEAs

2D planar microelectrodes

A typical example of a planar MMP is presented in figure 1.13 (Michigan probe[®], University of Michigan, United States).

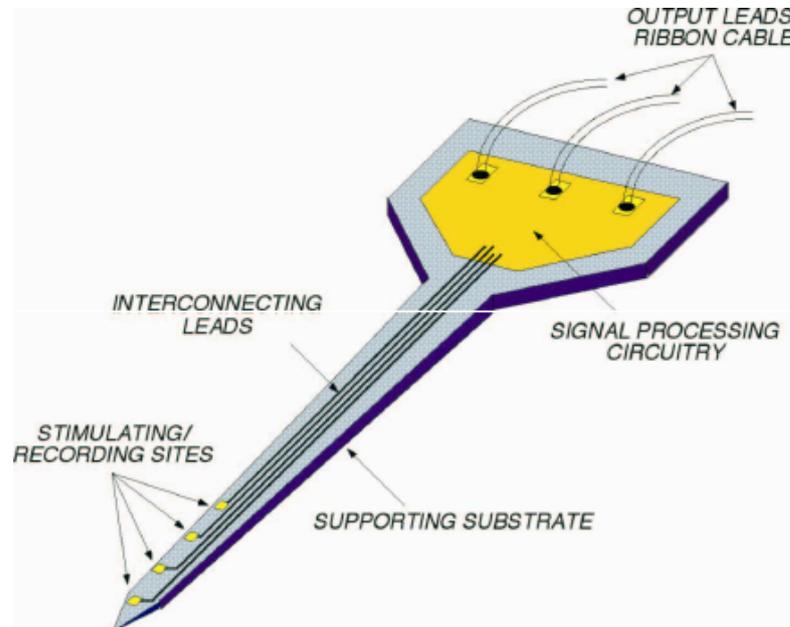


Figure 1.13: Michigan probe[®]. From [71]

Probes like the presented one can be used individually or in a multi-shank probe to extend the stimulated volume of tissue. Stimulating spots are located along the probe body, which is also covered by the interconnecting leads coming from the embedded circuitry. The very first example of a planar probe dates back to 1970 when Wise et al. [72] developed a Gold based microelectrode, where the conductive part is the extremity of the probe (1.14a). The main advantage of this type of probe is related to a higher dimensional control. More recently, Aarts et al. [73] developed a compressible multifunctional interconnect for out-of-plane MEMS structures, using the film transfer process, an innovative technique (1.14b). Finally, another example to mention about microfabricated planar probes is related to the recent work developed by Kiliyas et al. [74]. They developed a novel planar multi-electrode array to exploit the advantages of both soft and stiff materials, such as polyimide wings with platinum electrodes and silicon backbone to ensure the correct insertion procedure. Differently from a standard Michigan-style probe[®], which contains microelectrodes directly along the longitudinal extension of the probe, in this study, the latter presents the electrodes shifted laterally with respect to the polyimide probe body (1.14c).

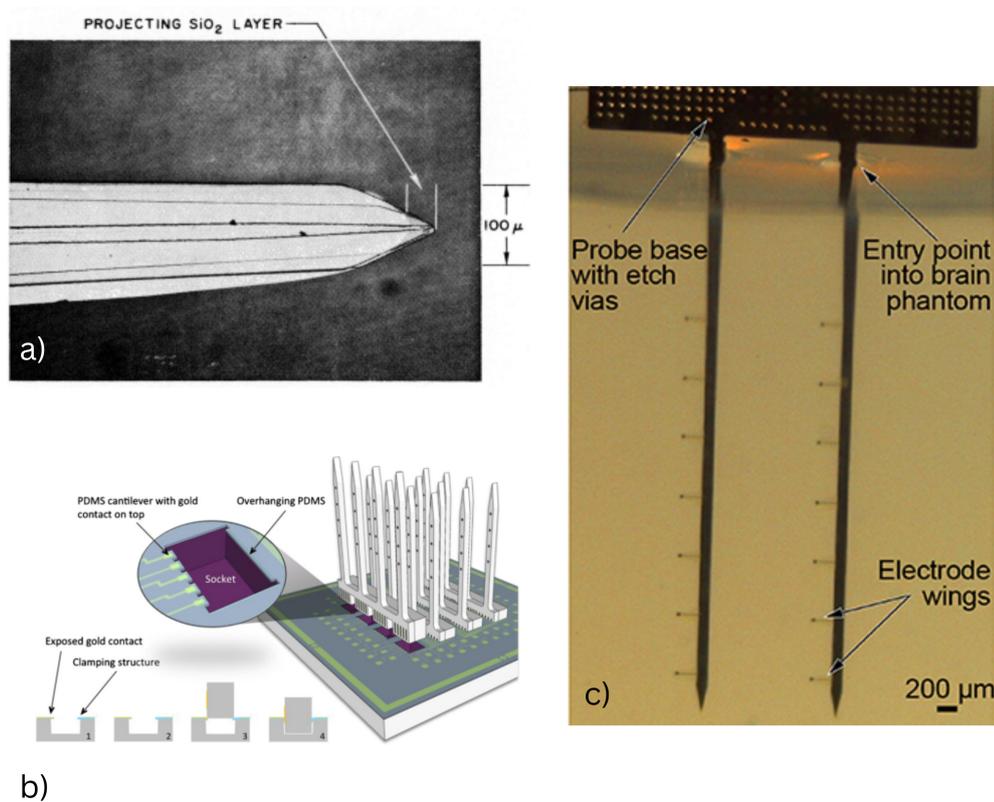


Figure 1.14: Multielectrode planar probes from literature. a) From [72]; b) From [73]; c) From [74]

3D microelectrode arrays

Three-dimensional MEAs represent reality, as well as the gold standard in brain stimulation and, in particular, intra-cortical microstimulation (ICMS). As already mentioned in section 1.1.3, the cornerstone in this scenario is represented by the Utah Electrode Array (UEA) (figure 1.15a), which is, basically, a microelectrode array made of several penetrating needles. Some technical details are explained in the mentioned section and in [24]. One of the first studies devoted to the fabrication of MEAs dates back to 1991 when Campbell et al. [23] developed a three-dimensional electrode array for chronic intracortical neurostimulation. The array is $4.2 \times 4.2 \times 0.12 \text{ mm}^2$ thick monocrystalline silicon substrate. The project involves the fabrication of 100 conductive penetrating electrodes with 0.09 mm base diameter and 1.5 mm long. Needles are, then, coated in Pt, to enhance electrical properties. The geometrical uniformity of the majority of the electrodes is assessed. Similar work is carried out in 1992 by Jones, Campbell, and Normann [75], who developed a glass/silicon MEA, with 100 microelectrodes of 80 μm diameter and

1.5 mm long. They demonstrated that the use of glass dielectric instead of p-n-p junction [23] can represent an advantage in microelectrodes mutual insulation ($\sim 10^{13}\Omega$). Further improvements have been achieved in terms of conductive coating, with iridium oxide that can provide extended longevity to silicon needles [76]. Bhandari et al. [77] proposed a combination of microfabrication techniques, such as dicing and etching to fabricate a novel convoluted shape UEA (figure 1.15b), which is more suitable to conform to the cylindrical morphology of peripheral nerve fascicles or the spherical structure of the retina. The implant consists of a 10x10 electrode matrix of variable-height rectangular columns. The latter undergoes an anisotropic etching procedure to obtain sharp microelectrodes. In the end, the whole structure is covered in parylene-c, and the tip is deinsulated to deliver charge to surrounding tissues. The mentioned design can be placed in the USEA (Utah Slanted Electrode Array) category of MEAs (figure 1.15c). In fact, it is thought for PNS (Peripheral Nervous System) recording and stimulation purposes, and it can provide less redundancy in terms of nerve fibers contacting if compared to traditional UEA [78]. The last aspect is explained by Branner and Normann in 2000 [79], who demonstrated the usefulness of the novel implant in solving the problem of a selective interface to many nerve fibers. Recently, in 2020, Shandhi and Negi [80] developed a novel microelectrode array, the UMEA (Utah Multisite Electrode Array) (figure 1.15d), to solve the disadvantage of having a single contact per electrode, as it happens in the traditional UEA. In this application, it has been demonstrated that the UMEA can highly improve the channels density, with respect to traditional UEA, therefore more neurons can be stimulated; the consequence is that stimulation can be performed at different layers of the human cortex without the risk of neuronal damage.

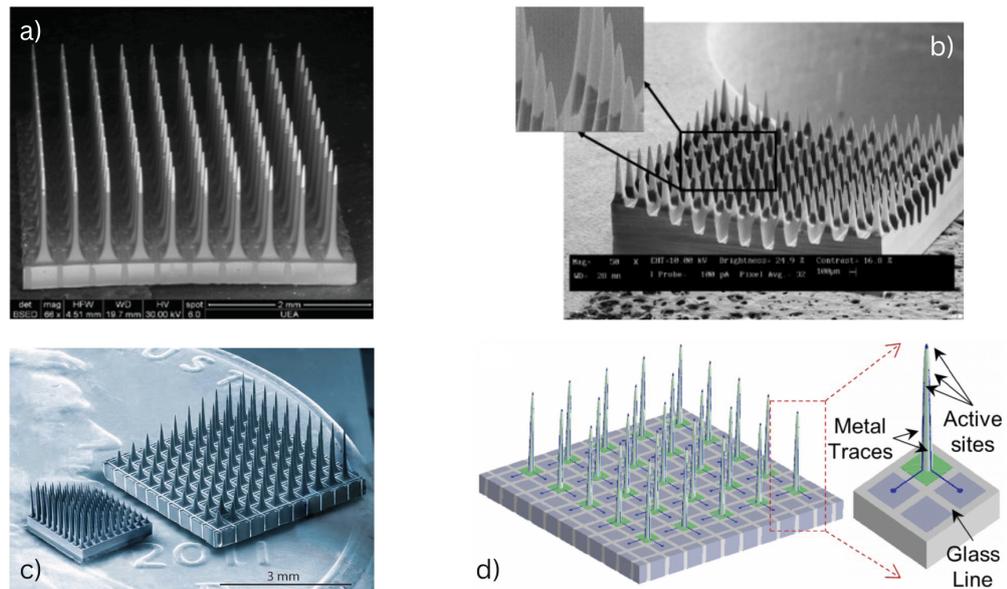


Figure 1.15: Examples of three-dimensional microelectrode arrays. a) Traditional UEA, from [80]; b) Convolved UEA, from [77]; c) Novel USEA. Courtesy of Oregon State University; d) Novel UMEA, from [80].

1.4.3 Polymer-based probes

Polymers are becoming widely used materials for neural implants since, as stated by [34],[35],[36], flexibility, minimized mismatch between mechanical properties with cerebral tissue's ones, and extensibility may help to minimize the likelihood of triggering major inflammatory response. Therefore, the literature provides several insights into polymer-based neural probes. Essentially, since it is necessary to deal with penetrating probes, they must have shape and geometrical properties similar to the ones mentioned for planar microelectrodes and three-dimensional MEAs. Wu et al. [59] proposed a possible alternative to metallic probes represented by a flexible fish-bone-shaped neural probe coated with silk to improve biocompatibility and strength (figure 1.16a). This application exploits a flexible substrate, small dimensions, and a large separation distance between electrodes and probe shank to minimize tissue reaction. The probe backbone is made of polyimide since it has comparable mechanical properties to cerebral tissue ones, while the electrodes are located at the extremities of the fish-bones. The overall structure is covered in silk, a biodegradable coating, which, other than making the probe biocompatible, increases the stiffness required for penetration into the cortex. A novel design is introduced by Sohal et al. [81] with the sinusoidal probe. In fact, the sinusoidal shape is used to minimize the micromotions of the electrode tip once implanted. Flexible materials

are used, such as parylene-c, and the sinusoidal shank is demonstrated to minimize tethering forces. Xie et al. [82] in 2015 tried to overcome the mechanical limitations of metallic probes with a novel three-dimensional macroporous nanoelectronic network based on SU-8 polymer (figure 1.16b).

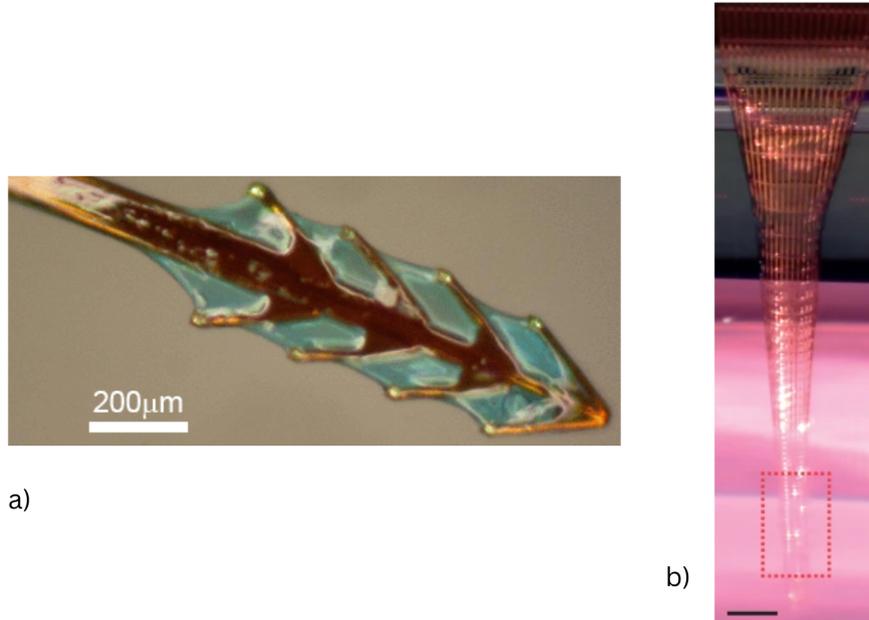


Figure 1.16: Examples of polymer probes. a) Flexible fish-bone-shaped neural probe, from [59]; b) Three-dimensional macroporous nanoelectronic network, from [82].

1.5 Towards miniaturized implantable devices

In the previous introductory sections, a state-of-the-art revision has been proposed, both on neural implants and microelectrodes. The first aspect to consider is the substantial difference between the first traditional stimulation implants and the most recent ones. In fact, the first developed implants are, normally, made of the following modules:

- External data processing unit
- Implanted transceiver
- Wired implants connected to the transceiver

Traditionally, the external processing unit sends the informative signal for stimulation to the transceiver, which is, usually, located underneath the skin. The latter

must, then, modulate and transfer the required stimulation pulse to the wired electrode-based implant. Therefore, from a quick analysis of the whole system, it is evident that the internal transceiver needs to be battery supplied since it is an active electronic component. Another drawback is represented by the wires and transceiver encumbrance, which can strongly limit the choice of implant location and can determine a more serious inflammatory response to the surrounding tissues as a consequence of the internal motion of the structures. Thereby, as already stated, the scientific community has started moving towards the miniaturization of stimulating implants that allow the transceiver removal, thus a direct wireless communication with the implanted structures, which can easily exploit the CMOS microelectronics. In conclusion, miniaturized neural prostheses can boast less bulky implants, no presence of wires, and, especially, the absence of a battery for power supply since both data and power are transferred to the implant wirelessly.

1.5.1 Challenges of present integration techniques

The crucial role of microelectrodes has been assessed in this first introductory discussion, with several integration approaches proposed in the literature to merge them with electronic drivers. Despite this, there are several limitations and challenges to face as far as electrode-electronics connection is concerned. In fact, when it comes to microwires, all the investigated applications proposed bulky solutions, with a cumbersome electronic driver, which prevents implant miniaturization. Moreover, the use of welding or epoxy for fixing can result in a general instability of the implant. In this last scenario, it is crucial to assess both mechanical and electrochemical stability before and after integration. As for MEAs and planar probes, the issue of miniaturization can be improved and partially solved. On the other hand, the main concern is represented by the monolithic array structure that must be connected to the related electronics. Lack of compatibility between electrode arrays and CMOS electronics, demonstrated in [83], can represent a hard issue to overcome.

1.6 Smart Micro Neural Dust Project

In this scenario, a mention must necessarily be made about the ongoing project named *Smart Micro Neural Dust (SMND)*, on which I based my experimental work. This project is related to the development of a novel cortical neural prosthesis to revert blindness in people with total impairment of all the anatomical sight structures. Therefore the idea is to stimulate the visual cortex with electrical pulses to generate localized phosphenes through the system presented in figure 1.17.

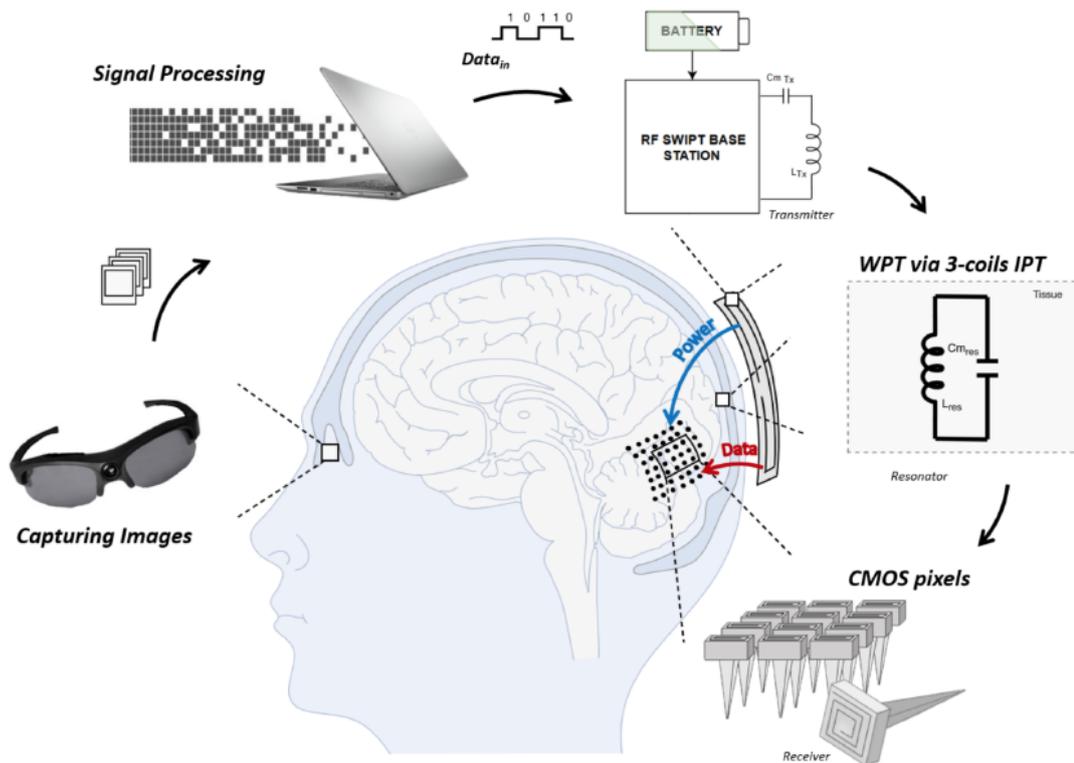


Figure 1.17: Schema of SMND cortical visual prosthesis.

The prosthesis involves an external camera to capture images of the external world; it can be mounted on a pair of glasses. The acquired B/W image is, then, sent to an external VPU (Video Processing Unit), which converts the gray-scale floating-point pixel values into zeros and ones, thus binary format. The information related to the image, is then, wirelessly transferred from an external transmitter to an array of free-floating penetrating implants, through an inductive coil, together with the needed amount of power to supply the implants themselves. The novelty of this prosthesis is focused on the implant, which is neither made of microwire arrays with bulky electronic drivers nor of monolithic MEA. In fact, it is thought to be made of single free-floating miniaturized units, one for each pixel of the image, and each one equipped with its own embedded CMOS circuitry. In detail, the circuitry is made of a demodulator and a clock-recovery system. The latter process the analogic signal coming from the external transmitter and convert it into a digital one. Finally, a biphasic stimulation pulse is generated, and it is delivered to the surrounding cortical tissue, through biocompatible penetrating microelectrodes.

1.6.1 Master's thesis outline

The aim of my master's thesis is to focus on the crucial and critical aspects related to the interface between a cortical prosthesis and the surrounding cerebral tissue. Therefore, since there are still challenges regarding electrodes and their integration into dedicated electronic supports, I concentrated my efforts on the development of integration methods to study and evaluate the mechanical stability of the implant, as well as on the development of a novel miniaturized electrochemical setup, to assess either electrochemical stability of a microelectrode after integration. In brief, the overall work is distributed as follows:

- Chapter 2 - Investigation of traditional integration methods for microelectrodes on a separately fabricated chip. It involves the study of a manual integration technique with conductive glue and tweezers and an automatized FIB-aided integration technique.
- Chapter 3 - Development of a novel CMOS-compatible microfabrication procedure of electrodes directly on CMOS chip in post-process. This chapter represents a possible solution to the major drawbacks encountered with traditional integration techniques.
- Chapter 4 - Development of a miniaturized electrochemical setup, and assessment of preservation of original electrochemical characteristics of microelectrodes.

All the requirements presented in the chapters are referred to the SMND project, to which my work is oriented.

Chapter 2

Integration of commercial microelectrodes

2.1 Substrate preparation

As mentioned in the introductory part, microelectrodes integration is a critical aspect, when it comes to miniaturized implantable devices. In particular, regarding the *SMND (Smart Micro Neural Dust)* project, two microwires should be integrated on two $60 \times 60 \mu\text{m}^2$ pads with a pitch of $30 \mu\text{m}$ on a CMOS fabricated chip of $200 \times 200 \mu\text{m}^2$. Trials are performed on a test $1500 \times 1500 \mu\text{m}^2$ CMOS chip (*180nm technology-TSMC, Taiwan*) shown in figure 2.1.

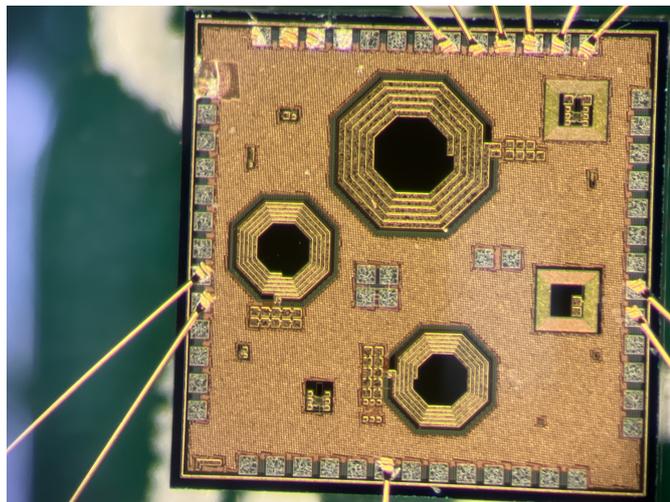


Figure 2.1: Microfabricated CMOS chip for microelectrodes integration

First, the chip must be placed and fixed on a PCB so that it can be used for testing purposes. Multiple adapter for QFP44 & QFN44, RE934-02E (*Roth Elektronik GmbH, Hamburg, Germany*) is used as a PCB and is shown in figure 2.2.

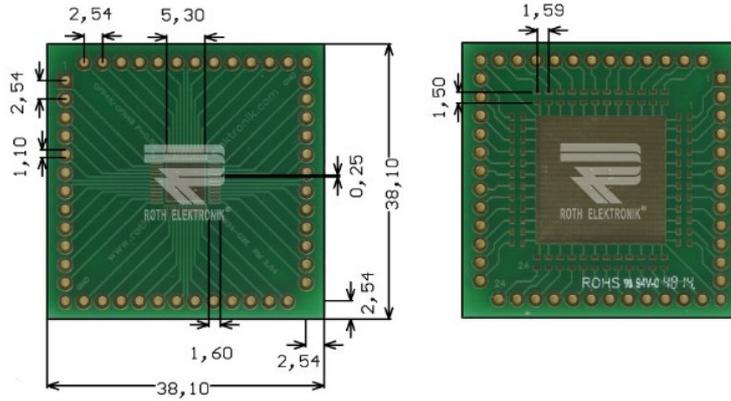


Figure 2.2: Front side and back side of the PCB used for chip support and testing purposes. Distances in mm. [84]

The fixing procedure requires conductive glue, and *EPO-TEK H20E* (*Epoxy Technology, Billerica, MA, United States*) is used for this purpose. From datasheet information [85], it is made of two parts to be mixed in equal parts by weight. Once the compound is ready, an Acetone and IPA pre-cleaning procedure is strongly recommended for the PCB area where the chip has to be placed, to avoid contamination and leak of adhesion. At this point, a small amount of conductive epoxy is deposited on the big conductive square in the middle of the PCB, with the aid of a fine tool. The chip can, now, be softly placed on the glued area without any pressure. Conductive epoxy technical datasheet [85] also gives information on the procedure for glue curing in the oven, to make it harden and consolidate the bonding between the chip and the PCB. The recommended cure procedure is 140°C for 10 minutes. Once the chip is firmly fixed to the PCB, wire bonding is performed between the small pads of the chip and the bigger ones on the PCB, to allow external electrical contact during chip testing. The used wire bonder tool for this procedure is the *TPT HB10* (*TPT Wire Bonder, Germany*) located at *CMi* (*Center of Micronanotechnology*). Gold wire of $20\ \mu\text{m}$ diameter is chosen for *wedge-wedge bonding*, a type of bonding where the wire extremity is deformed into a flat elongated shape of a wedge that bonds to pads through pressure and ultrasonic energy. The shape of the wedge highly limits the orientation of the wiring, which must always be performed from the bottom up of the structure to bond. *TPT HB10* datasheet [86] recommends working with wiring distances

ranging from $500\ \mu\text{m}$ to 2 mm only on gold pads, to have good adhesion of the bond. Some parameters regarding force, power, and ultrasonic energy must be set for the first and second bond, based on the type of used wire. Once the chip has been wire bonded with pads on the PCB, it is ready to be integrated with microelectrodes. Chosen microelectrodes are commercial Pt/Ir monopolar electrodes (Item PI20030.5A3, *MicroProbes for Life Science, 18247 Flower Hill Way D, Gaithersburg, MD 20879, United States*). Figure 2.3 shows some general characteristics of these microelectrodes.

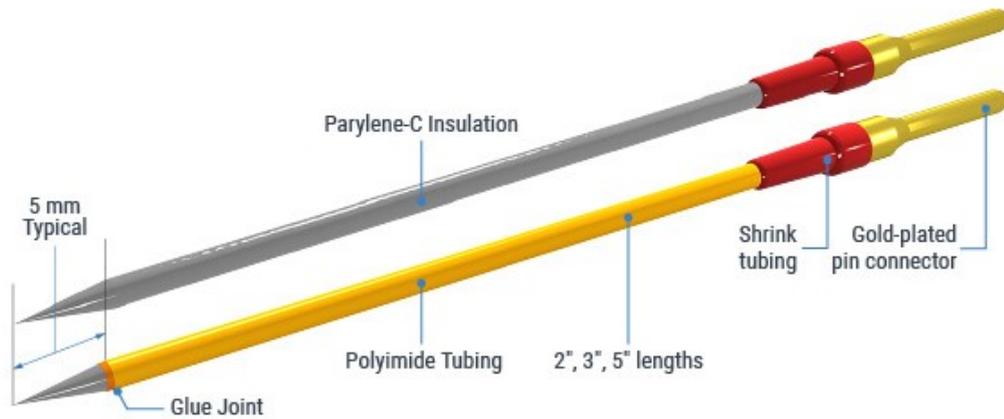


Figure 2.3: Commercial microelectrodes characteristics. [87]

For our purpose, Parylene-C coated microelectrodes are chosen. Moreover, the latter are available in three models, based on the tip shape, as shown in figure 2.4. The choice fell on the *standard tip* microelectrodes, which offer versatile performance, as well as an effective balance between penetration and durability.



Figure 2.4: Available tips for monopolar microelectrode. [87]

Microelectrodes are sold in boxes of ten units, each 5 cm long. They are used to inspect the feasibility of two types of integration techniques:

- Manual integration
- FIB aided integration

2.1.1 Manual integration

Manual integration is the first investigated technique, which requires basic minimal equipment to be performed: tweezers and conductive epoxy. Since microelectrodes are 5 cm long, cutting them to the right length is the first step to perform. The required length is 1.5 mm, and it can be achieved either by manual cutting with a blade or with the aid of FIB beam or laser, to obtain a more precise cutting line. Once the microelectrode is cut, a little drop of conductive epoxy is dispensed on the pad. The glue is the same used to fix the chip on the PCB, before wire bonding, the *EPO-TEK H20E (Epoxy Technology, Billerica, MA, United States)*. At this point, the electrode is handled with metallic precision biology tweezers, *7SG.CX.0.ITU model (Ideal-Tek SA, Balerna, Switzerland)* and it is fixed in the glue drop on the proper pad. The final step after integration is represented by chip insulation with electrically insulating glue *EPO-TEK H70E (Epoxy Technology, Billerica, MA, United States)* and related curing session, 120°C for 15 minutes.

2.1.2 FIB aided integration

With regard to FIB-aided integration, the overall procedure is synthesized as follows:

1. Microelectrode FIB cutting
2. Microelectrode vertical placement in the FIB/SEM chamber
3. Microelectrode-micromanipulator welding
4. Microelectrode integration

FIB cutting

The ionic beam is exploited for cutting the electrode to 1.5 mm, as requested by project specifications. The used SEM/FIB tool is the *Zeiss NVision 40 CrossBeam (Carl Zeiss, Sports, Optics)* which merges together FIB and SEM columns. The microelectrode is placed horizontally on conductive Carbon tape which is itself fixed on a SEM specimen holder. The cutting is performed using the FIB beam with the voltage set at 30 kV and the current varied from 65 nA to 100 nA . The average time required for the cut is around 1 hour, but it is strongly dependent on the electrical parameters chosen for the beam.

Microelectrode vertical placement in the FIB/SEM chamber

Once the microelectrode is cut, from an analysis of geometrical constraints inside the FIB/SEM chamber to correctly transfer the microelectrode on the chip, it results that the microelectrode must be placed vertically. Because of this, the latter must be taken out from the chamber and manually placed in a dedicated holder. In our case, an old SEM aperture is used. It is a 3 mm diameter discoidal metallic structure with a small hole in the center of 200 μm in diameter, serving as support for microelectrode. Figure 2.5 shows the CAD realization of the used support to keep the microelectrode vertical. It must also be pointed out that, considering the base diameter of the microelectrode of 55 μm , the diameter of the hole should not be much higher than the used one; in this situation there would be the risk that the microelectrode leans horizontally on the structure, thus invalidating the procedure. At this point, both the SEM aperture with a vertically placed microelectrode and PCB with a fixed CMOS chip must be inserted in the SEM/FIB chamber together on the same specimen holder.

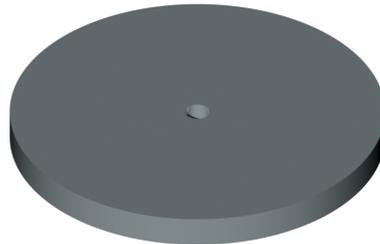


Figure 2.5: Autocad (*by Autodesk Inc.*) model of SEM aperture used as microelectrode support

Microelectrode-micromanipulator welding

As the specimen holder is inserted into the SEM/FIB chamber, the following step to be performed is the welding between the microelectrode and the high-precision micromanipulator. The latter needs to be approached towards the body of the microelectrode and carbon needs to be deposited through the Focused Ion Beam

nozzle, while GIS (Gas Injection System) nozzle provides a constant Argon flow to reduce the charging effect of the beams and to enhance the deposition yield and precision. The voltage required for Carbon deposition is 30 kV , while the area of the deposited material depends on the current. In particular, $1\ \mu\text{m}^2$ of material is deposited with 3 pA of current. In our application, we need few μm^2 of deposition area.

Microelectrode integration

Once the microelectrode is firmly fixed to the micromanipulator, it should, then, be driven toward the dedicated pad on the CMOS chip and the microneedle's base should come in contact with the pad. Finally, the FIB can be used to solder the microelectrode to the pad, through Pt deposition. The very last step, as already performed at the end of manual integration, is the chip insulation with *EPO-TEK H70E* (*Epoxy Technology, Billerica, MA, United States*). The latter requires a curing session at 120°C for *15 minutes*.

2.2 Manual integration results

As mentioned in the methods section, manual integration is the easiest technique to perform in terms of equipment constraints, since the only required tools are tweezers for microelectrodes handling and conductive glue, for microelectrodes fixing on the chip. The first problem that we can encounter is the need to cut the microelectrode since the commercial one is 5 cm long. The cut to 1.5 mm can be achieved manually, with a dramatic decrease in precision of the length and the cutting cleanliness. Figure 2.6 shows the result of the "dirty" manual blade cut, which might have some implication on the stability of the implant.

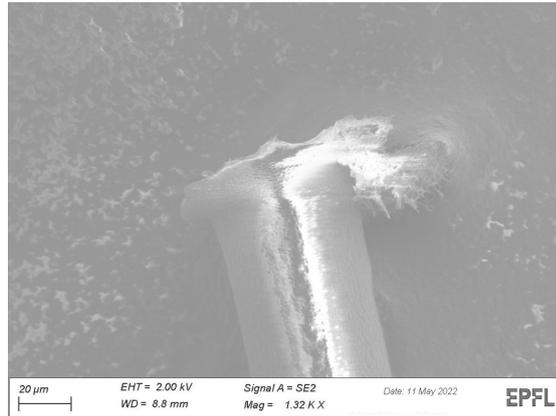


Figure 2.6: SEM acquisition demonstrating the dirtiness of manual blade cut on PtIr microelectrode

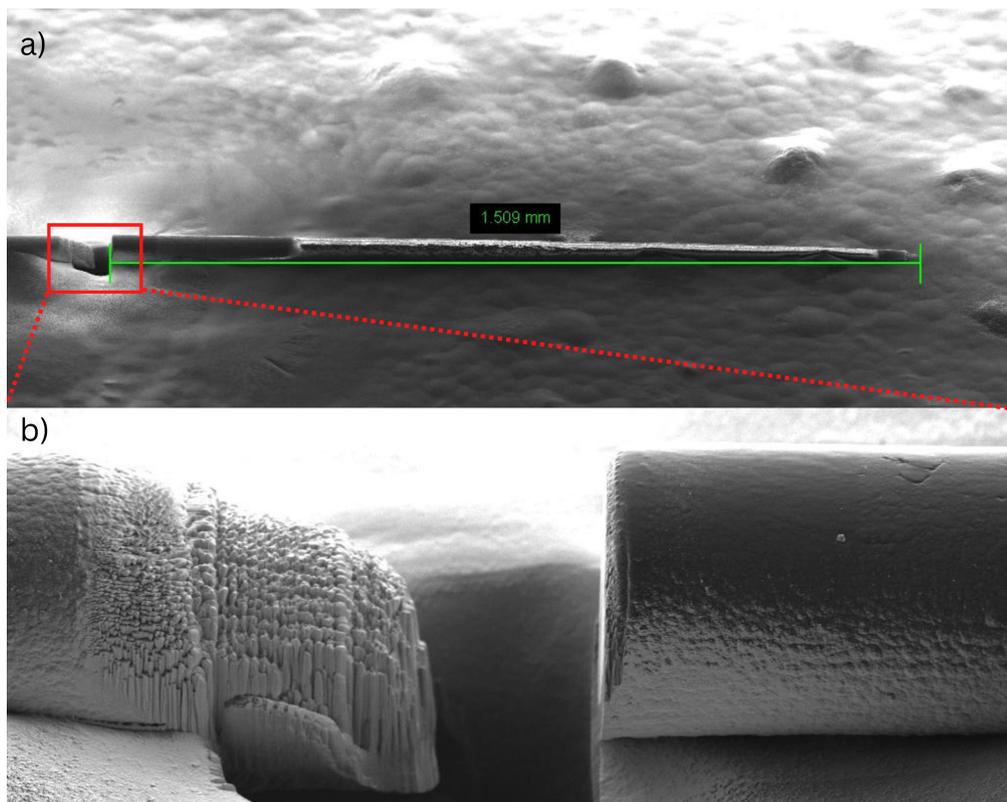


Figure 2.7: SEM acquisition of FIB aided cut of PtIr microelectrode at 1.5 mm. a) Overview of the cut microelectrode; b) Detail of the cut.

Therefore, there are some other preferred methods to achieve the requested precision for the cut and the desired length, such as laser and FIB-aided cuts. The latter is chosen for our application since it provides the best results in terms of cut precision and cleanliness (figure 2.7a,b.). The most complicated part of the manual technique is the integration with tweezers. First of all, the dispensing of a drop of conductive glue on a $60 \times 60 \mu\text{m}^2$ is limited by the hand precision and by the tool used to dispense it. Therefore, the main challenge is to prevent the two drops of glue from coming in contact with each other. Otherwise, the two microelectrodes are short-circuited together, invalidating the purposes of the stimulating implant. The overall result after integration, curing and protection of the chip with transparent non-conductive glue is shown in figure 2.8a,b.

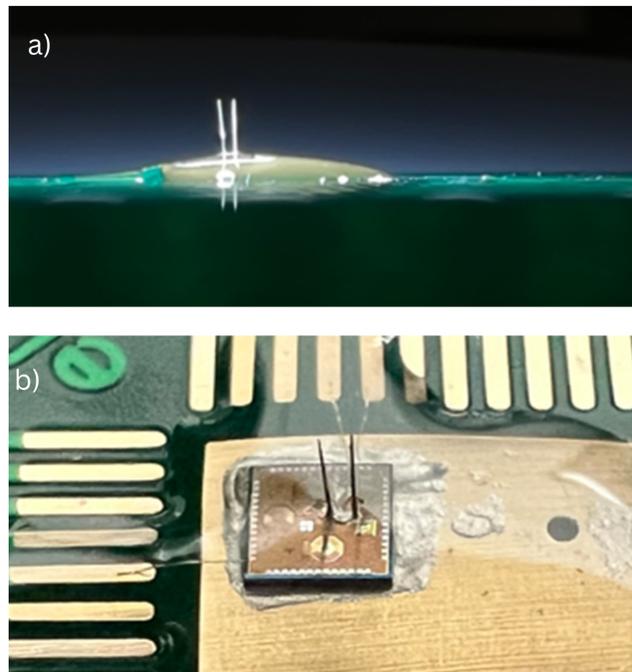


Figure 2.8: Results of manual integration of two PtIr microelectrodes on CMOS chip. a) Lateral view showing vertical orientation of microelectrodes; b) Overview of CMOS chip on PCB with integrated microelectrodes.

2.3 FIB integration results

The second investigated technique has been developed through the FIB tool. It represents an advanced and more automatic technique, which is thought to replace the traditional manual integration, overcoming its main limitations, such as hand

precision during fixing epoxy dispensing and microelectrode placement on the chip. With regard to this technique, FIB cut of the microelectrode is performed, since it produces the best results in term of length precision and cleanliness of the cut (figure 2.7). The main criticality of this technique is represented by the fact that the microelectrode must be inserted vertically in the FIB/SEM chamber, thus the placement is externally done with tweezers. This aspect should be automatized, for instance, using a microtweezer as micromanipulator inside the FIB/SEM chamber. This would help to avoid taking the sample out of the chamber and spending time inserting the microelectrode in the aforementioned aperture, with a $200\ \mu\text{m}$ diameter hole. Figure 2.9 shows the overall setup inside the FIB/SEM chamber ready for integration. The microelectrode is placed vertically inside the aperture hole; the micromanipulator is placed near the microelectrode, ready to be welded to the latter. The GIS nozzle is extended near the welding site, to provide Argon for a precise carbon deposition. Despite the fact that a carbon layer of $4\ \mu\text{m}$ has been deposited to solder the micromanipulator to the microelectrode, the connection proved to be unstable when the micromanipulator was moved and lifted. The main reason can be blamed on friction between the microelectrode and the walls of the hole when it is moved.

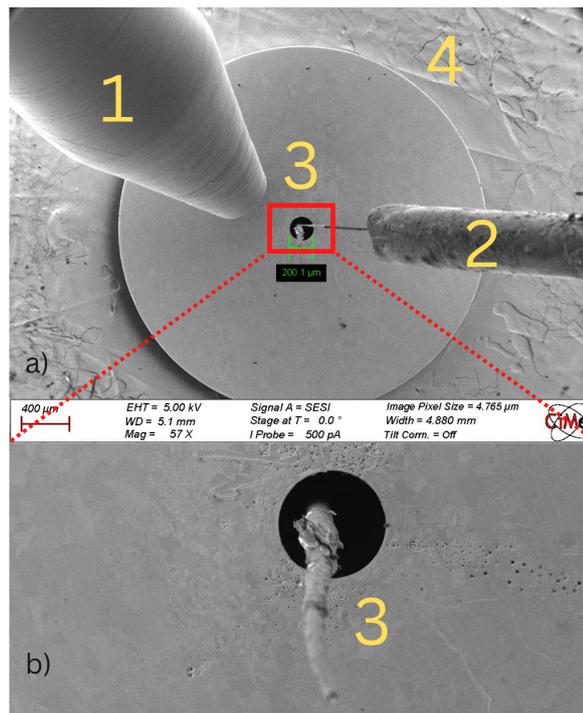


Figure 2.9: a) FIB/SEM chamber overview. (1) GIS nozzle, (2) Micromanipulator, (3) Microelectrode, (4) Substrate with SEM aperture; b) Detail of the vertical microelectrode.

Therefore the proposed technique has not been terminated. A possible solution that can fix the mentioned issues is the use of precision tweezers as micromanipulator for the FIB. In this way, the electrode can be cut and directly handled towards the integration continuously inside the FIB/SEM chamber, avoiding the welding procedure.

Chapter 3

Microfabricated electrodes

The alternative to the integration of commercial microelectrodes is to find a solution that can simplify the fabrication of miniaturized implantable devices. For this reason, another option to test is represented the CMOS-compatible microfabrication of electrodes, which was carried out at the *CMi (Center Of Micronanotechnology)* based at *EPFL campus (Lausanne, Switzerland)* in Clean Room environment (ISO 5/6/7). In general, the overall microfabrication work is focused on the development of a free-floating miniaturized implant containing embedded CMOS electronics and microelectrodes. The following sections describe the detailed procedure to fabricate CMOS-compatible microelectrodes in post-processing. Since the developed structures should be implanted, it is crucial to develop penetrating planar probes. Figure 3.1 shows the expected structure at the end of the whole process flow with the two 90° oriented wings open (a) and the structure ready for the implant, where the wings have been bent against the silicon pillar walls (b). The first mandatory step to face is to define and design a complete process flow, specifying all the technologies and machines used for every step. The process flow for CMOS microelectrodes fabrication can be found in Appendix A. Once it is submitted to the *CMi* staff, it is revised meticulously, and the feasibility of the overall process is verified, as well as interactions and eventual incompatibilities among single steps.

3.1 Involved materials

With respect to the strict requirements that neural implants must follow in terms of structure and used materials, it is fundamental to remember the most important property, biocompatibility. Thereby, only materials that do not overreact with the highly corrosive environment of the brain tissue must be used, also to avoid complications for the patient and annihilation of the device's purpose. For this reason, the material chosen as the framework for the microprobes is *aluminum*,

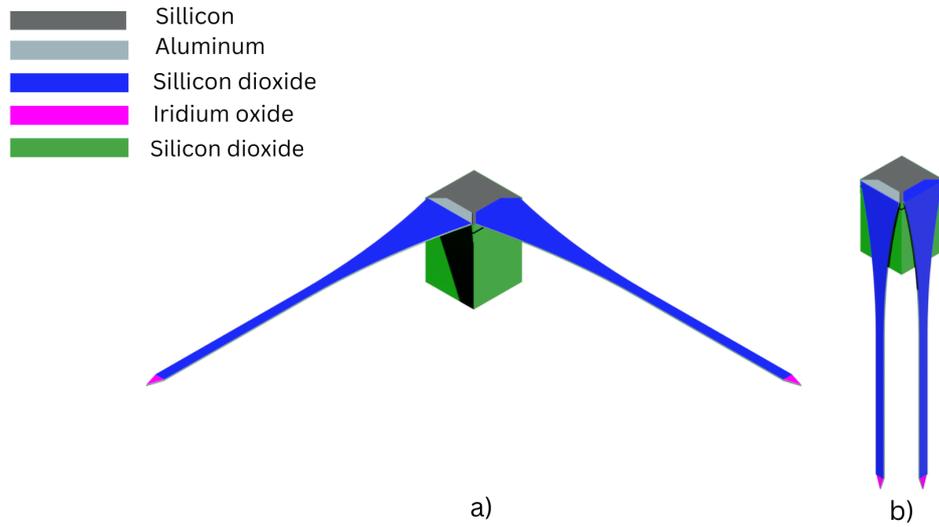


Figure 3.1: Autocad (Autodesk Inc.) three-dimensional design of microfabricated free-floating implants. a) Final structure after fabrication process flow; b) Ready-to-implant structure after probes bending.

because of the listed advantages:

- High availability
- Low-cost material
- Good conductivity
- Corrosion resistant
- Lightweight
- Good mechanical strength
- CMOS compatible

In addition to the excellent mechanical, electrical, and biocompatibility characteristics, aluminum is chosen mainly because it is one of the most common materials used as top metal layer by the majority of foundries. This aspect allows full compliance with a complete CMOS fabrication procedure. To ensure insulation, *Silicon dioxide* is chosen. It is an inert material, very frequently used in MEMS and CMOS fabrication and especially biocompatible and non-toxic [88]. In order to enhance

the electrical characteristics of the microelectrodes tips, a deposition of a layer of $IrOx$ is chosen. In fact, among the others, *charge injection limit (CIL)* is a crucial parameter for an electrode. It is defined as the "*maximum charge density ($mC\ cm^{-2}$) that an electrode can inject before reaching the water electrolysis potential* [44]. Also according to [44], $IrOx$ is one of the most promising materials because it is characterized by a high value of CIL. Based on the deposition method of $IrOx$, two types of films can be created: AIROF (Activated IRidium Oxide Film) and SIROF (Sputtered IRidium Oxide Film). AIROF is obtained by repeated oxidation and reduction of Ir, which forms the oxide layer. On the other hand, SIROF is formed by reactive sputtering of Ir metal in an oxidizing plasma. Zheng et al. in [44] collected CIL data from different works, demonstrating the improvements with respect to other metallic materials. With regard to the protective and second insulation layer for the overall final structure, *parylene-C (poly(monochloro-p-xylylene))* is selected. This is one of the most used polymers in CMOS fabrication mainly because of its excellent properties, which can be maintained for a long time after implantation with very low levels of deterioration. Among all the properties, biocompatibility, biostability, resistance against hydrolytic degradation and low cytotoxicity are the most noteworthy. Moreover, parylene-C coating is perfectly conformal, resistant to HF, KOH, and solvents [89]. In fact, it can be used for three main purposes:

- Protective or support layer for sensitive devices
- Sacrificial layer with Al or Si device
- Device layer with photo resist, SiO_2 or Si as a sacrificial layer

3.2 Microfabrication steps

The starting point of the microelectrodes fabrication process is represented by a wafer, as a substrate, which is supplied by the *CMi*, directly from the foundry. The department provides different types of wafers:

- Silicon wafers
- SOI (*Silicon On Insulator*) wafers
- Glass wafers

As our process is thought to be CMOS oriented, the choice moves inevitably toward silicon wafers. Table 3.1 summarizes the available wafers at *Cmi*.

Table 3.1: Available wafers at *CMi*

Name	Diameter [mm]	Thickness [μm]	Orientation	Conductivity, Dopant	Resistivity [Ωcm]
Silicon prime wafers 100/P/DS/1-10	100 \pm 0.2	380 \pm 10	<100>	P Boron	1-10
Silicon prime wafers 100/P/SS/01-05	100 \pm 0.2	525 \pm 20	<100>	P Boron	0.1-0.5
Silicon prime wafers 100/P/DS/01-05	100 \pm 0.2	380 \pm 10	<100>	P Boron	0.1-0.5
Silicon prime wafers 100/P/SS/15-25	100 \pm 0.2	525 \pm 20	<100>	P Boron	15-25
Silicon prime wafers 150/P/SS/15-25	150 \pm 0.2	675 \pm 20	<100>	P Boron	15-25

Since the application requires a wafer with no native layer on it, *100/P/DS/01-05* is the one that meets the needs. Since silicon is a semiconductor material, it has both conductive and insulating properties, and for this reason, if our structures were built directly on the bare substrate, they would be all short-circuited together, thus resulting in a useless application. Accordingly, the preliminary step involves the deposition of a stronger insulator, and it has been agreed that silicon dioxide (SiO_2) has excellent insulating properties with a general conductivity of $\sim 10^{-12} Scm^{-1}$ [90]. The deposition of the SiO_2 is performed everywhere on the wafer front side, through a service provided by the *CMi* staff, which can also include an RCA cleaning procedure [91]. The RCA clean is a crucial procedure, particularly in microelectronics, because every single particle of contaminant can seriously damage the correct process flow, especially in CMOS complex fabrications. The RCA cleaning procedure takes its name from the laboratory in which W.Kern et al. [92] developed the cleaning sequence in 1970. For our application, since the substrate is pure silicon with no layers to protect, the whole procedure is performed. Here is the cleaning procedure in details, also summarized in table 3.4 [91]:

- RCA-1 for the elimination of the organic elements. The processing temperature is $75^\circ C$ for *15 minutes*
- Rinse for *1 minute*
- HF treatment for the removal of the Silicon dioxide generated during the RCA-1 step. The removed thickness is 70 Å for *15 seconds* on thermal oxide.

This step can be optional, depending on the presence/absence of insulator layers on the wafer to process.

- Rinse for *1 minute*
- RCA-2 for the elimination of metallic elements. The processing temperature is *75°C* for *15 minutes*
- Full rinse for *15 minutes* with the *Fast Fill Rinse* bath (FFR) and the *Trickle Tank* (TT) bath.
- Drying of the wafers with the *Spin Rinse & Dry* (SRD) system

Table 3.2: RCA cleaning procedure summary [91]

Step	Solution	Temperature	Duration
RCA-1	H ₂ O:NH ₄ OH:H ₂ O ₂ 5:1:1	75°C	5 to 15 min
HF	HF:H ₂ O 1:10	20°C	15 s
RCA-2	H ₂ O:HCl:H ₂ O ₂ 6:1:1	75°C	5 to 15 min

Once the RCA procedure is completed, silicon dioxide can be deposited on the wafer surface, and it is done in *Centrotherm Furnaces* (*Centrotherm equipment, Germany*), which are made by four stacks for a total of 15 tubes. Every tube is dedicated to a particular process, based on the application. Wet Oxide is deposited on the front side for a total thickness of *200 nm*, sufficient to guarantee insulation among the conductive structures (figure 3.2). The temperature for this process ranges from *800°C* for small thickness values up to *1250°C* for bigger thickness values.



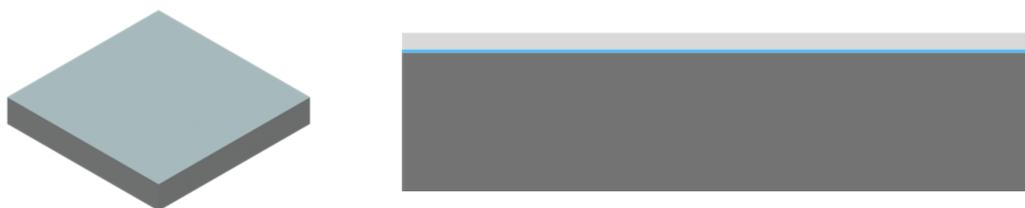
Figure 3.2: Silicon wafer after RCA process and SiO_2 deposition

3.2.1 Aluminum deposition on front side

The very first step involves aluminum deposition (figure 3.3), which is needed to create the framework of our structures. For our purpose, a $4 \mu m$ layer is deposited on the front side, with $10 nm$ of Titanium as the adhesion layer, which is strongly recommended since the adhesion between aluminum and silicon/silicon dioxide is poor. Two deposition methods are tried:

- Sputtering
- Thermal evaporation

Sputtering is performed with the *Pfeiffer Spider 600* (*Pfeiffer-Vacuum, Germany*), a machine developed especially for the deposition of metallic and dielectric layers. *Sputtering* is an innovative technique that involves high energy plasma particles, which are used to bombard a target made of the material to deposit on the substrate; the latter detaches from the target, due to the high energy collisions and deposits on the substrate. The *Pfeiffer Spider 600* allows recipes with more than one deposited material per batch since it is configured with four *Process Modules*. Recipes contain all the information needed for the software to handle the wafer among the modules, automatically. In this case, both Titanium and aluminum depositions are performed at *room temperature*, with the parameters resumed in table 3.3. Deposition time is the only modifiable parameter, while all the other

**Figure 3.3:** Aluminum deposition**Table 3.3:** Pfeiffer Spider 600 recipe parameters for Ti/Al deposition

Material	Target	Film	Recipe	Source	Power [W]	Gas [sccm]	V [nm/mn]	Ramp [s]
Ti	Ti _r	Ti	Ti(1)-#	RF	1000	Ar(15)	90.0	4
Al	Al	Al	Al-#	DC	1000	Ar(15)	215.0	5

process parameters are fixed. It is fundamental, especially for thin layers, like in our case 10 nm Titanium layer, to consider the ramp parameter, which is the time required for the power to reach its maximum value. It must be considered because the deposition starts even before the power reaches its maximum value. It is commonly agreed to use the deposition rate for half the time of the ramp during this time frame to compute the already deposited amount of material; the product between the deposition rate and half the ramp time results in a good estimate of the deposited layer. Ramp time parameter becomes negligible with high-thickness layers, like $4\ \mu\text{m}$ of aluminum. In details, the required time to deposit 10 nm of Titanium is 9 seconds , while the one required to deposit $4\ \mu\text{m}$ of aluminum is $18\text{ minutes and }37\text{ seconds}$. Considering Titanium layer, half ramp time is 2 seconds , and the deposition rate is 90.0nm/mn or 1.5nm/s . Following the rule, the already

deposited amount of Titanium during the ramp time frame is:

$$d = 1.5nm/s * 2s = 3nm \quad (3.1)$$

The remaining amount to be deposited is:

$$r = 10nm - 3nm = 7nm \quad (3.2)$$

Now, we can consider the standard deposition rate to deposit $7nm$, and calculate the remaining time:

$$time_r = \frac{7nm}{1.5nm/s} \sim 5s \quad (3.3)$$

In conclusion, the total amount of time required for deposition is:

$$time_t = ramp + time_r = 4s + 5s = 9s \quad (3.4)$$

As previously mentioned, the same calculation can be performed for aluminum, even if for thick layers ramp time becomes negligible if compared to the total deposition time.

The second technique which is tried for aluminum deposition is *thermal evaporation*, performed at *IPHYS Clean Room* with *Alliance Concept EVA 451* (*Alliance-Concept, Annecy, France*). The mechanism is slightly different from sputtering; first of all, the process is high temperature, and the target is not hit with plasma particles, but it is heated until it evaporates. The thickness of the evaporated material is controlled with quartz crystal balance, remotely interfaced with a PLC sequences controller. The time required for this deposition is slightly higher than sputtering, with the whole process duration of about *30 minutes*. The power of the RF source for target heating is controlled and always calibrated, based on users' reports. One big constraint is that the maximum deposition per run is limited to $1 \mu m$, so with our requirements, the requested time to obtain the desired thickness is extended to about *2 hours*, for four runs.

3.2.2 Photolithography for aluminum pattern

The following step after aluminum deposition is the creation of the pattern of microelectrodes on the front side of the wafer. This is achieved through a photolithographic procedure, which is repeated multiple times in the process flow, following the same framework. Photolithography is, in fact, a procedure that allows

to transfer any 2D pattern on a wafer surface; this is the crucial part where all the geometrical features are created, following the layouts which are made with *Autocad (version 2023, Autodesk Inc., Mill Valley, California, United States)*. Photolithography process can be divided into four sub-steps:

- Surface preparation
- photo resist coating
- Wafer exposure to UV light
- Development

Surface preparation

The chosen photoresist for all the photolithographic steps is *AZ10XT-60*, from *AZ10XT series (Merck KGaA, Germany)*. With noteworthy sidewall profiles, aspect ratio and photo speed, it represents the optimal choice to obtain precise and defined structures. One crucial requirement is surface preparation and cleaning before photo resist dispensing. *CMi* suggests different types of surface preparations, based on the material in contact with the photo resist. This is required since many organic materials offer a dramatically poor adhesion of the resist, which can easily detach from the surface during development. Figure 3.4 summarizes all the available and recommended surface treatments, based on the layer material.

Surface material (larger area)	Vapor HMDS	Plasma O ₂	Thermal dehydration
Si	√√	√	√
SiO ₂ , fused silica, SiN, Si ₃ N ₄	√√	√	√
Float glass, pyrex	√	√√	√
Metals: Al, Au, Pt, Ti	...	√	√√
Metals: Ag, Cu, Cr, Fe	...	X	√√
III/V semiconductors (GaN, GaAs)	...	X	√√

Legend: √√ Strongly recommended / √ Alternative process / ... Not effective / X May affect or destroy underlying material

Figure 3.4: Wafers surface treatments for enhanced photo resist adhesion.[93]

In our specific case, photo resist should cover the aluminum layer, so the most recommended procedure for surface preparation is the *dehydration*, which

prevents the formation and subsequent encapsulation of small water droplets due to environmental humidity. *Dehydration* step is performed automatically in the coating recipe, fully handled by *EVG150 Automatic Coater and Developer (EV Group)*. It consists on pre-coating bake at 150°C for *4 minutes and 30 seconds*.

Photo resist coating

Once the wafer surface is treated, it is ready to be coated with the previously mentioned positive photo resist *AZ10XT-60* (figure 3.5).



Figure 3.5: Photo resist coating of the wafer, over the aluminum layer, after dehydration procedure.

Different thicknesses can be chosen, based on the following steps to perform and for our purposes $8\ \mu\text{m}$ is sufficient. photo resist is dispensed automatically with the aforementioned *EVG150 Automatic Coater and Developer* through spin coating. The correct thickness is achieved by modulating the rotation speed of the chuck where the wafer is vacuum-fixed; the higher the rpm and time values are, the thinner the photo resist layer becomes, as shown in figure 3.6. The specific coating recipe includes a spinning session of *100 seconds* at *2800 rpm*, followed by *60 seconds* at *0 rpm* to allow stress relaxation in the dispensed layer. A post-coating soft bake for *5 minutes* at 112°C follows to let all the remaining solvent particles flow away and to allow a better drying. Soft bake parameters are shown in table 3.4, based on the resist thickness.

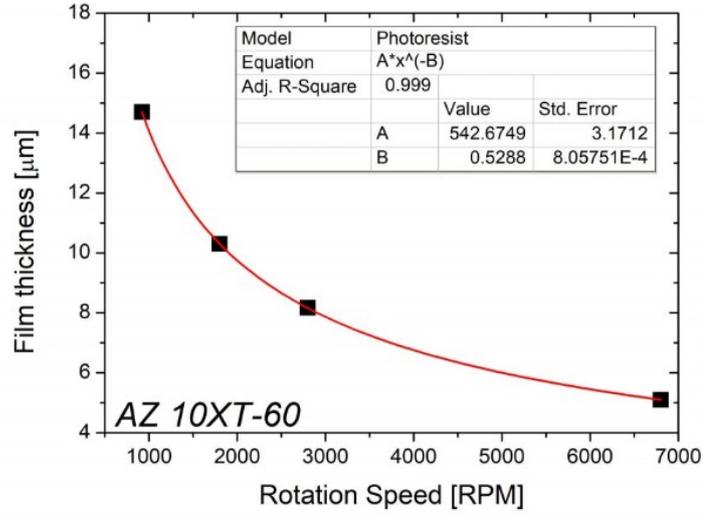


Figure 3.6: Film thickness vs. rotation speed of the chuck. [93]

Table 3.4: Spin speed and softbake time for different photo resist thicknesses. [93]

Recipe name	Spin speed [rpm]	Softbake time [mm:ss]	PR thickness [μm]
C4_D_10XT_5u_EC	6800	04:00	5
C4_D_10XT_8u_EC	2800	05:00	8
C4_D_10XT_10u_EC	1800	06:00	10
C4_D_10XT_15u_EC	920	07:00	15
C4_D_10XT_20u_EC	720	08:00	20

Wafer exposure

After coating, the photo resist must be selectively exposed to UV light. Since it has a positive tone, the exposed part becomes soluble and can be washed away during the subsequent development procedure. Exposure is conducted with *MLA150 Mask-Less Aligner* (Heidelberg-Instruments Mikrotechnik GmbH, Germany). The pattern

to be exposed is identified through an Autocad (by Autodesk Inc.) *.gds* design which must be uploaded and converted in machine language through dedicated software. The metal layer is identified in the *.gds* mask file by layer *163/0*. Once a pattern is converted, the software distinguishes the different layers on a *closed figure* basis. For this reason, it is crucial to make it sure during the Autocad design session, through the layer properties panel. This definition allows the software to perform logical operations on the design, thus allowing a distinction among layers and background. Since the goal is to expose photo resist everywhere, except the area of the probes, care must be taken to set the machine to expose only outside this area. Moreover, since further exposures will follow, it is essential to print cross-shaped alignment marks, as they will be useful for correct alignments of new layouts to the already printed ones. An example of an alignment mark is shown in figure 3.7 and they are printed using layer *58/0* of the *.gds* mask file.

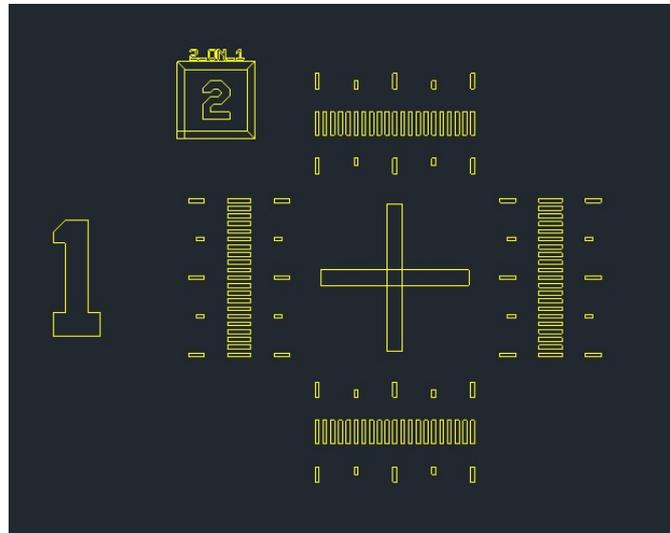


Figure 3.7: Example of cross-shaped alignment mark

The overall exposure with the *MLA150 Mask-Less Aligner* allows overcoming the standard process of photolithography, which involves the fabrication of a specific Chromium mask for every layer to expose. Actually, it performs a *direct writing* of the layout on the wafer, taking advantage of the focused UV laser beam, which can reach sub- μm exposure precision. Since the *critical dimension* of probes layout is around 2-3 μm localized on the tip, the machine is perfectly suitable for the job. *Critical dimension* is defined by [94] as "the line of width of the photo resist (PR) line printed on a wafer" which "reflects whether the exposure and development are proper to produce geometries of the correct size".

The *MLA150 Mask-Less Aligner* uses two exposure wavelengths, based on the

photo resist:

- 405 nm
- 375 nm

The recommended wavelength for *AZ 10XT-60* is *405 nm*. Furthermore, two other parameters must be set:

- Dose [mJ/cm^2]: the amount of energy the radiation should transfer on surface unit.
- Defocus (-10...+10): definition of the height of the focus of the laser radiation. When defocus is set at 0, it means that the radiation is focused on top of the resist, while a positive value means that the radiation is focused downwards inside the resist, with 10 equivalent to a shift of $6 \mu\text{m}$. The defocus parameters allow to change the concentration of energy at different resist thicknesses.

Figure 3.8 summarizes the optimal Dose values, based on the used exposure tool and photo resist thickness.

<i>Illumination:</i>	Broadband*	i-line (355-365 nm)	h-line (405 nm)
<i>Equipment:</i>	MABA6, MA6 Gen3 (no filter)	VPG 200, MA6 Gen3 (filter), MJB4	MLA 150
PR thickness [μm]	Dose [mJ/cm^2] ⁺	Dose [mJ/cm^2] ⁺⁺	Dose [mJ/cm^2] ⁺⁺⁺
5	360	330	240
8	460	420	340
10	555	470	390
15	660	580	490
20	800	690	580

Figure 3.8: Exposure doses for different thicknesses and exposure tools

In our specific case, 340 mJ cm^{-2} should be the right dose value, but under suggestion of the *CMi* staff it was decided to use 400 mJ cm^{-2} with a Defocus of +3. It must be pointed out that, before exposure, the *MLA150 Mask-Less Aligner*

always performs a edges and shape detection of the wafer, in order to correctly center the design on the substrate. Another important aspect to mention is that, once the edges are detected, the software also estimates the rotation of the wafer on the chuck of the exposure chamber, to be applied to the exposed layout. The overall exposure time of a standard 100 mm Silicon wafer strongly depends on the complexity of the design and on an the needed quality of exposure:

- Fast exposure \sim 12 minutes
- High quality exposure \sim 25 minutes

Figure 3.9 shows a schematic view of the process.

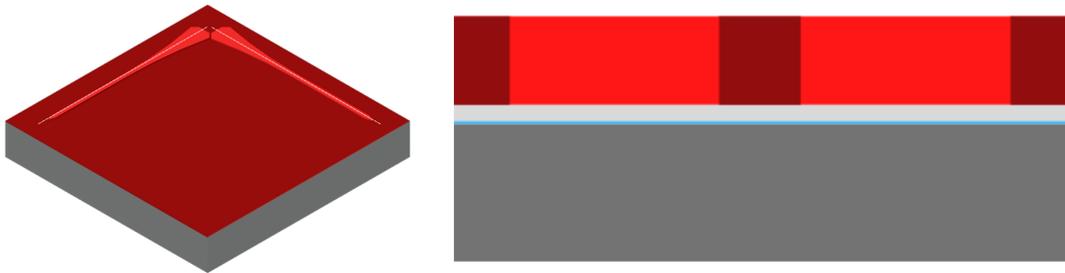


Figure 3.9: Photo resist exposure following aluminum pattern layout for probes framework and alignment marks.

Photo resist Development

Once the layout is exposed, only specific parts of the resist are soluble. For this reason, the final step includes the removal of these parts and it can be done through the *development* procedure. As the *CMi* suggests, at this point of the process flow it is highly recommended to develop the resist manually because the automatic development solution would affect the aluminum layer, which is too reactive, thus it would detach. For this reason, the *AZ400K development solution* is specific to *AZ 10XT-60* photo resist and the following steps must be followed:

- 1 to 3.5 DI water dilution of *AZ400K developer* (*Clariant Industries, Germany*)
- Wafer transfer in the solution bath for *6 minutes* (45"/min)
- DI water rinse for 1 minute
- Wafer drying

After development, photo resist can be found only on the probes area, as shown in figure 3.10.



Figure 3.10: Photo resist development.

3.2.3 Aluminum dry etching and photo resist strip

aluminum etching is the following step to perform, with the photo resist acting as a protection layer. Etching is executed with the *STS Multiplex ICP* (*Surface Technology Systems, GB*), which is a machine dedicated to the etching of a broad variety of materials, like insulators (SiO_2 , Si_3N_4 , and SiC), silicon, metals (Al alloys, Pt, Ti) and some polymers. According to the material to etch, different gases can be used:

- Chlorine chemistry for metals
- Fluorine/carbonate chemistry for dielectrics
- Oxygen chemistry for polyimide

The appropriate recipe for aluminum etching is presented in table 3.5

Table 3.5: aluminum etching recipe (*STS Multiplex ICP*)

Material to etch	Process name	Mask	Selectivity/Mask	Etch Rate [$\mu\text{m}/\text{min}$]	Chemistry
Al	Al_etch	PR	>1:1	0.2 to 0.5 Si: 0.215 SiO ₂ : 0.08	Cl ₂ /BCl ₃

It must be noted that, apart from the etching rate of the aluminum, there is also the one related to silicon and silicon dioxide. In fact, chlorine is a very aggressive and corrosive gas, which also affects these materials, even though the effect on them is almost negligible, with respect to the one related to aluminum. The machine is also equipped with an *End Point Detection (EPD)* system, which allows the user to abort every single step of the recipe, for instance when it is finished before the set time. Time exposure to gases is the only real parameter that can be changed, based on the etching rate of the material of interest. Moreover, to help the user understand if the process is terminated before the time, an aid system based on the reflectivity of the surface is used. Typically, the light signal is sent to the surface at the center of the wafer, since the etching starts at the edges of the wafer and ends in the center; aluminum has a certain rate of reflectivity, estimated as the percentage of light intensity that comes back to the source. When aluminum is fully etched, the light intensity signal drops down and this explicit the end of the etching procedure, as the exposed surface is now made of SiO₂. At the end of the process, it may happen that some chlorine gas particles remained trapped in the photo resist, with the risk of degradation, which has to be avoided. For this reason, before proceeding with the following steps, it is necessary to provide to the wafer a specific DI water bath, called *cascade*, which is simply a fine rinsing bath. Figure 3.11a shows a schematic view of the mentioned etching procedure. Once the aluminum is etched and the wafer rinsed, the remaining photo resist can be definitely removed (figure 3.11b), and this is performed with *Tepla GiGAbatch (PVA TePla, Germany)*, which uses high-frequency oxygen plasma for:

- photo resist (PR) strip
- Wafer surface cleaning before subsequent processes
- Descuming before wet etching

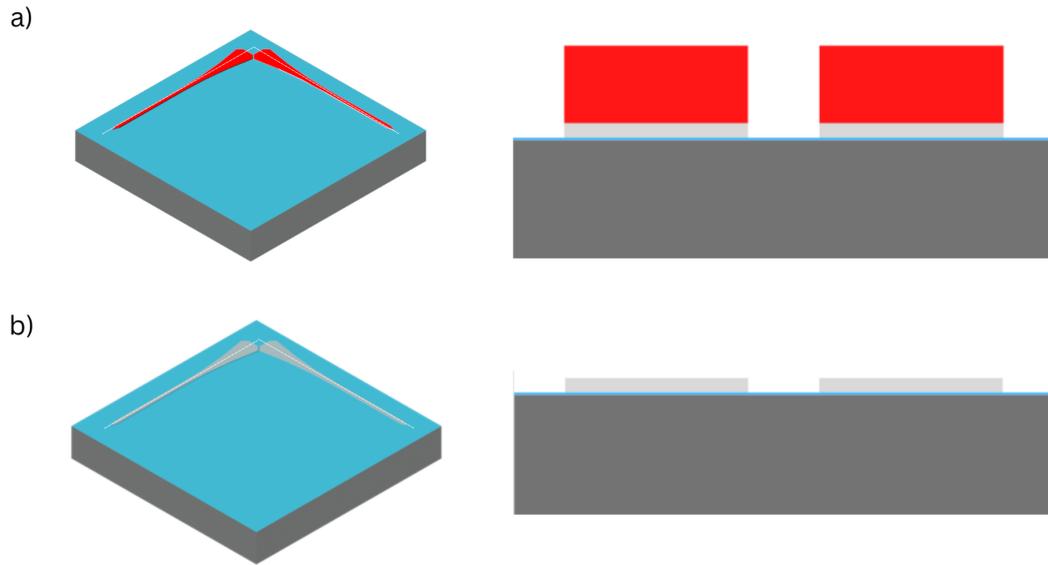


Figure 3.11: a) Aluminum etching; b) Remaining photo resist strip.

In detail, there are two families of recipes for resist strip: *Resist Strip High Power/Flow* and *Resist Strip Low Power/Flow*. Table 3.6 shows the parameters used for the two recipes.

Table 3.6: Photo resist strip recipes (*TePla GiGAbatch*)

Programs	Power [W]	O ₂ flow [sccm]	Pressure [mbar]	Time	Uniformity
PR_Strip_High_xx	600	400	0.8	1min-30min	20%-30%
PR_Strip_Low_xx	200	200	0.5	10sec-15min	20%-30%

For our purpose, since the photo resist layer is 8 μm thick, it is recommended to use *PR_Strip_High_15*, which means that the recipe is run for 15 minutes. The wafer must be placed vertically on a quartz cassette with the front side facing the door, where the oxygen flow comes from.

3.2.4 Silicon dioxide (SiO₂) deposition on front side

When photo resist is stripped, the wafer contains metal structures on the front side, which should be insulated leaving only the tip exposed. The best candidate

for insulation is SiO_2 , which is one of the most used materials for this purpose in CMOS processes. According to the process flow, $1 \mu\text{m}$ of insulation layer is required (figure 3.12), and for this purpose, two methods are tried:

- Sputtering
- PECVD (Plasma Enhanced Chemical Vapor Deposition)



Figure 3.12: Silicon dioxide deposition on the front side of the wafer.

With regard to sputtering, it is performed by the *Pfeiffer Spider 600* tool, previously mentioned for Ti/Al deposition. SiO_2 deposition is performed at room temperature, with RF reactive sputtering. Table 3.7 shows the parameters related to the specific used recipe.

Table 3.7: *Pfeiffer Spider 600* recipe parameters for SiO_2 deposition

Material	Target	Film	Recipe	Source	Power [W]	Gas [sccm]	V [nm/mm]	Ramp [s]
SiO_2	SiO_2	SiO_2	$\text{SiO}_2\text{-\#}$	RF	1000	Ar(15)	58.0	30

Following the same considerations done in section 3.2.1, it is possible to determine the deposition time for SiO₂, in order to reach a homogeneous layer of 1 μm , which is *17 minutes and 30 seconds*.

The second tried procedure for deposition is PECVD, which mainly differs from sputtering in two features:

- Sputtering is a *physical* vapor deposition while the current procedure is a *chemical* vapor deposition (CVD)
- Sputtering is performed at room temperature, while the current procedure is performed at a high temperature (300°C)

PECVD is performed at *IPHYS Clean Room* with the *Oxford Instrument Plasmalab System 100 – PECVD (Oxford Instruments, UK)*, a very powerful tool capable of depositing silicon oxide, silicon nitride and amorphous silicon. Like most of the machines, the only modifiable parameter is the deposition time, known the deposition rate, which is, for SiO₂, *60 nm/min*. Doing a rapid calculation, the required time to deposit 1 μm of the insulator is:

$$t = \frac{1000\text{nm}}{60\text{nm}/\text{min}} = 16.67\text{min} \sim 16'40'' \quad (3.5)$$

3.2.5 Photolithography for Silicon dioxide (SiO₂) pattern

The very same procedure and machines (*EVG150 Automatic Coater and Developer* and *MLA150 Mask-Less Aligner*) described in section 2.2.2 are used, with three substantial differences:

- *HMDS* as surface preparation
- Alignment is required through alignment marks
- Automatic development

As already mentioned in section 3.2.2, the adhesion of the photo resist on an inorganic layer is very poor; for this reason, it is appropriate to define a suitable surface preparation procedure; while for aluminum, dehydration is the optimal choice, when it comes to silicon/silicon dioxide, the optimal procedure is an *HMDS* treatment. *HMDS* stands for "*Hexamethyldisilazane*" and it consists of a surface modification to promote the adhesion of photo resist through a *silanization* process, as explained in details by [95]. With regard to alignment, it has to be mandatorily performed, as the SiO₂ layer must perfectly cover the body of the probes. The aforementioned alignment marks, now, assume crucial importance, and one more alignment step is required in the *MLA150* before exposure. The user should, first,

provide the planar Cartesian coordinates of at least two alignment crosses, and, secondly, acknowledge their positions directly on the wafer, with the help of a camera. When this procedure is terminated, the exposure can be started and conducted as described in section 3.2.2. The used layer in the *.gds* mask file is *165/0*.

The last difference concerns the photo resist development, after exposure. In fact, it can always be done manually, with *AZ400K developer*, but since there is no exposed aluminum, it can also be performed automatically, with the *EVG150 Automatic Coater and Developer*. The wafer is loaded into the machine, and it is handled automatically, after the selection of a photo resist thickness-dependant recipe. According to the manual of the machine, the development consists of short spray dispense strokes, followed by puddle (no rotation)/rinse development cycles. The parameter that drives the development of different thicknesses is the time of contact (figure 3.13), which is the total time the development solution remains in contact with the photo resist. The last step after development is represented by wafer rinse and drying.

Recipe name	PR thickness [μm]	Total contact time [s]
D4_N_10XT_5u_PUD	4...6	140
D4_N_10XT_8u_PUD	7...9	210
D4_N_10XT_10u_PUD	9...12	250
D4_N_10XT_15u_PUD	12...17	370
D4_N_10XT_20u_PUD	17...22	490

Figure 3.13: *EVG150*. Thickness-dependant contact time for photo resist automatic development. [93]

Figure 3.14 shows the complete photolithography procedure for silicon dioxide, from photoresist coating (a), to exposure (b) and final development (c)

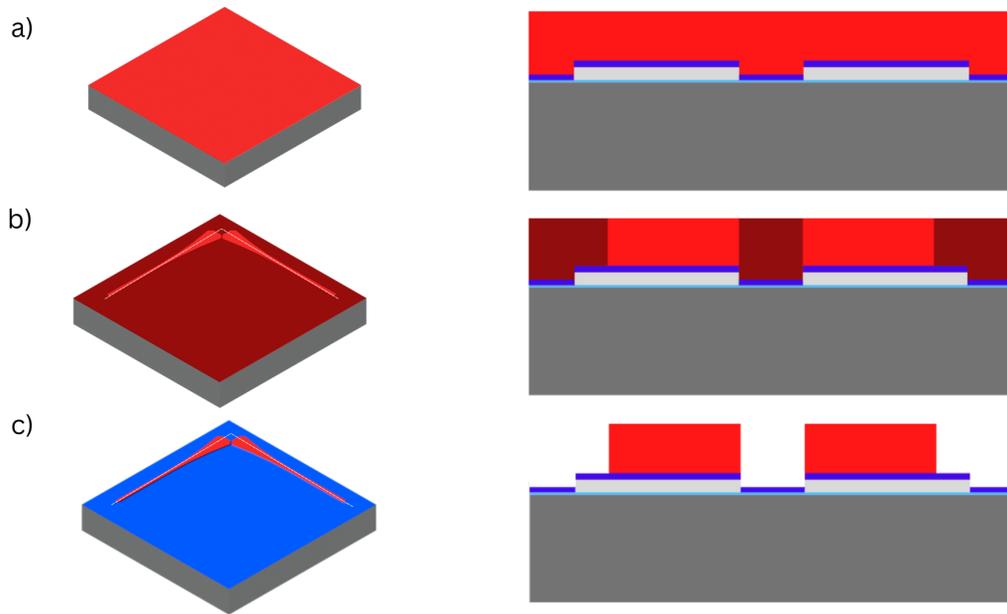


Figure 3.14: Silicon dioxide deposition on the front side of the wafer.

3.2.6 Silicon dioxide (SiO_2) dry etching and photo resist strip

Wafer after development exhibits photo resist only on the probe bodies, with a $1 \mu\text{m}$ layer of SiO_2 all over it. For this reason, it is necessary to etch the exceeding oxide. This is achieved through dry etching, with the *STS Multiplex ICP*, already mentioned for aluminum etching in section 3.2.3. Fluorine/carbonate chemistry is used to etch dielectrics, such as SiO_2 . Table 3.8 reports the main characteristics of the related recipe.

Table 3.8: SiO_2 etching recipe (*STS Multiplex ICP*)

Material to etch	Process name	Mask	Selectivity/Mask	Etch Rate [$\mu\text{m}/\text{min}$]	Chemistry
SiO_2	Oxide	PR	1:1	0.25	CF_4

Since the only modifiable parameter is the exposure time to CF_4 , etch rate value must be considered. Moreover, besides the $1 \mu\text{m}$ layer, also the 200 nm thermally grown layer, preliminary deposited during RCA cleaning procedure, must be etched, to make the following back side etching possible. The total amount of time required

for etching is ~ 5 minutes. It is always recommended to set a higher exposure time and then to take advantage of the *End Point Detection* system, which allows the user to abort the exposure at any moment since the etch rate value could be slightly lower than the nominal one. Unlike the aluminum dry etching procedure, the DI water *cascade* rinse is not required, as non-corrosive gases are used. Once the SiO_2 is completely etched, the remaining protective layer of photo resist should be removed and, same as mentioned in section 3.2.3, *Tepla GiGAbatch* is used for this purpose, taking advantage of high power oxygen plasma exposure for 15 minutes. Probes are, now, fabricated and insulated, with exposed tips. Figure 3.15 provides a schematic view of both the etching (a) and photo resist strip procedure (b).

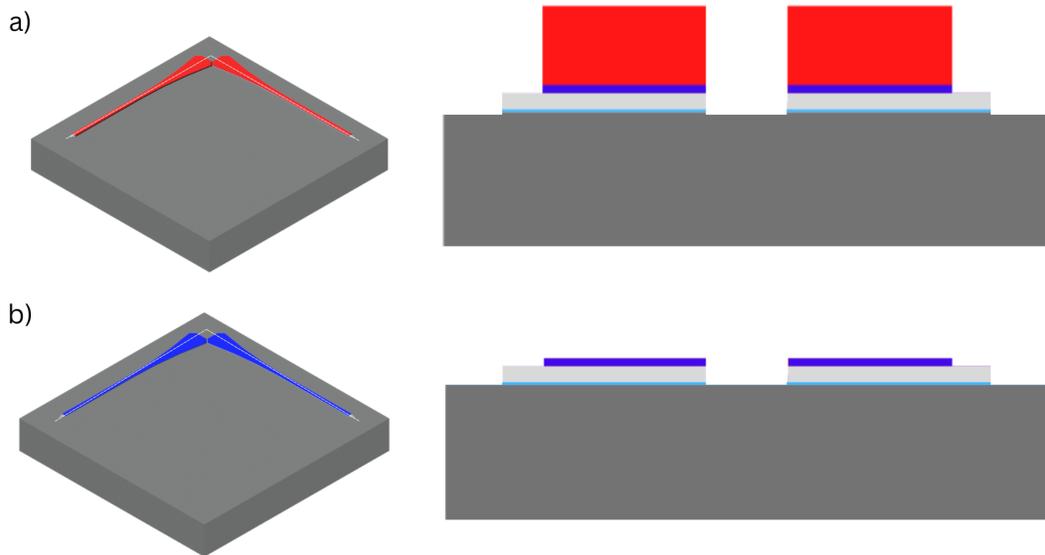


Figure 3.15: a) Exceeding silicon dioxide etching; b) Photo resist strip.

3.2.7 Iridium oxide (IrOx) deposition on front side

IrOx has huge advantages as a coating material for microelectrodes tips. For this reason, a thin film is deposited through the *Alliance-Concept DP650* (*Alliance Concept SARL, Annecy, France*) sputtering machine for a total thickness of 200 nm (figure 3.16), thus the film can be classified as SIROF. According to the manual of the tool, the *room temperature uniform deposition* is chosen for our application. Moreover, since the deposition rate is about 0.65 nm/s, 308 seconds are required to deposit 200 nm.



Figure 3.16: IrOx deposition on the front side.

3.2.8 Photolithography for Iridium Oxide (IrOx) pattern

Third front side photolithography is dedicated to creating the pattern to leave the IrOx only on the tip of our microelectrodes. The procedure is the very same as described for the SiO₂ photolithography in section 3.2.5, with the very same parameters to set. The used layer of the *.gds* mask file is *164/0*. Figure 3.17a shows the preliminary photo resist coating, figure 3.17b shows the exposure, while figure 3.17c the photo resist development.

3.2.9 Iridium Oxide (IrOx) dry etching and photo resist strip

The wafer is ready for exceeding IrOx etching. For this purpose, Ion Beam Etching (IBE) is chosen as the most suitable technique. It is performed with the *Veeco Nexus IBE350* (*Veeco, New York, United States*) (figure 3.18a). It consists of a broad-beam ion etcher. In particular, it uses Argon ions which are extracted by an ICP (Inductively Coupled Plasma) source, accelerated and conveyed to form a mono-energetic beam, which is used to etch any materials by means of pure physical sputtering. Before IrOx etching, a preliminary session of photo resist reflow is required. This procedure involves the increase of temperature of the photo resist for *2 minutes* at *125 °C*, slightly over its *glass transition temperature* (T_g) through the *Despatch LCD1-16NV-3, biocompatible oven* (*Despatch Thermal*

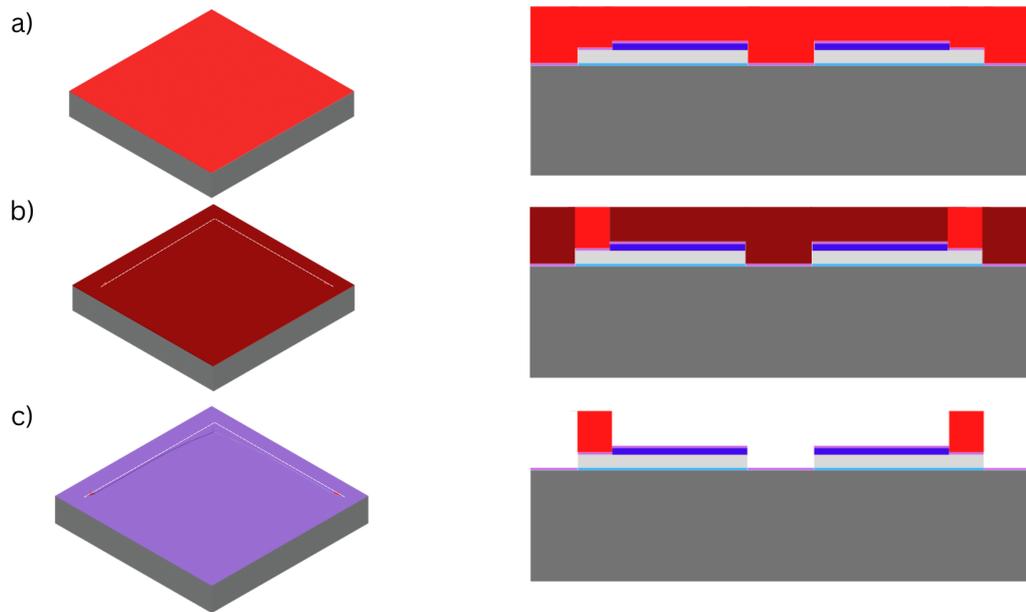


Figure 3.17: IrOx deposition on the front side.

Processing Technology, Minneapolis, MN 55044, United States). This process is strongly recommended before ion beam etching, since physical sputtering is characterized by unwanted re-deposition of etched materials in regions not directly exposed to the ion beam. The vertical photo resist sidewalls are highly affected by this phenomenon. Therefore, a reflow session is required to tilt the sidewalls, to have them directly exposed to the ions [96]. Like most of the machines at *CMi*, also in this case, the only modifiable parameter is the exposure time, after consulting the information about the etching rate of the different materials. Once the IrOx etching procedure is completed, the remaining photo resist must be stripped off the wafer (figure 3.18b). For this purpose, the already mentioned *Tepla GiGAbatch* is used, providing a high-power oxygen plasma for *15 minutes*. This represents the last process of the front side.

3.2.10 Front side parylene-C coating

According to the submitted process flow, the front side must be protected, in order to proceed with the back side processes. Front side protection is achieved with a $5\ \mu\text{m}$ parylene-C layer deposition. As already mentioned, parylene-C is one of the most used polymers in CMOS fabrication, with good mechanical, electrical, and biocompatibility properties, among others. In its raw form, it appears as a dimer. Under vacuum conditions, the dimer is heated at 150°C and changes to

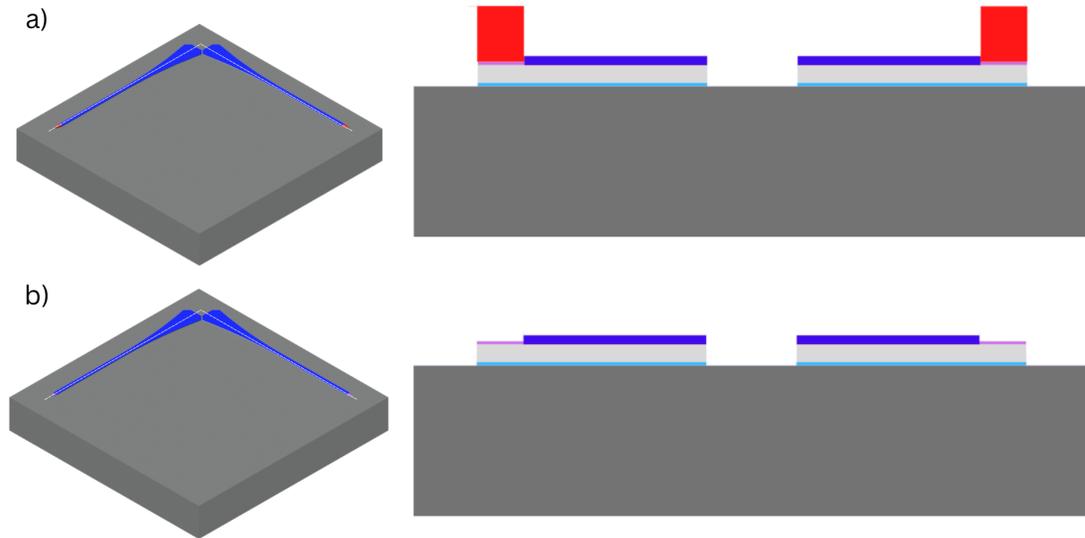


Figure 3.18: a) Exceeding IrOx etching; b) Photo resist strip

vapor phase. It diffuses to pyrolysis chamber at 670°C, where it dissociates into single monomers, which diffuse to the room temperature or slightly heated (80°C) process chamber and condensate to fabricate the parylene-C layer. Specifically, the layer thickness depends on the amount of material inserted into the vaporization boat. The layer uniformity is very high, with $< 1\%$. parylene-C deposition is a service provided by the *CMi* and performed with the *Comelec C-30-S* (*Comelec SA, Switzerland*), as sketched in figure 3.19

3.2.11 Back side photolithography

The wafer back side must, now, be prepared for silicon selective etching, in order to release free-standing structures. Moreover, etching must occur only around the fabricated probes, leaving them fixed two by two on a Silicon pillar. For this reason, photolithography must be set to open only areas around the probes, after photo resist development, in order not to etch most of the wafer, which can maintain enough strength and rigidity to be handled by etching machine (figure 3.20a,b,c). Equally to the previous photolithography steps, *EVG150* is used for 8 μm coating with photo resist and *MLA150* for design exposure (layer 167/0). Also in this case, as mentioned for SiO₂, alignment is crucial to open the areas corresponding to the probes area. *MLA150* allows the back side alignment, which is performed in the very same way like front side one explained in section 3.2.5. The only difference is

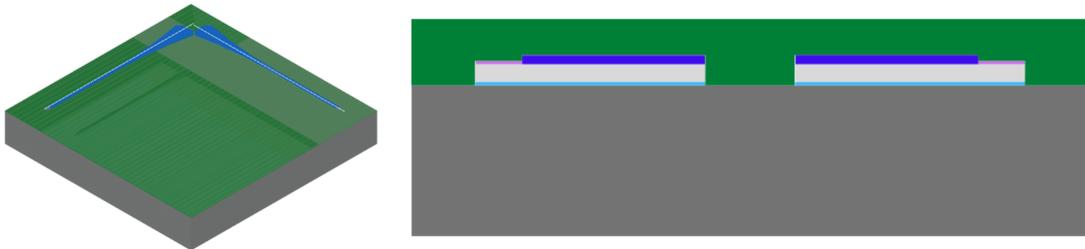


Figure 3.19: parylene-C coating of the front side.

represented by the upside-down placement of the wafer on the chuck, to expose the back side to the laser head. Another crucial aspect involves the *mirroring* of the design before exposure, as well as the alignment crosses coordinates.

3.2.12 Back side dry etching

Once the back side is correctly processed, it is ready to be etched, with photo resist acting as a protection layer. The dry etching of Silicon is performed with the *SPTS Rapier DSE* (*SPTS Technology, UK*), which is an optimized machine for *DRIE* (*Deep Reactive Ion Etching*) for Silicon (Si) and Silicon On Insulator (SOI). Before going into details of the procedure, a brief description of *DRIE* follows. *DRIE* can be defined as an anisotropic CMOS process used to create structures in silicon when deep and precise trenches are needed. There exist two types of reactive ion etching: *Cryogenic* and *Bosch Process*. The second is the one of interest for this application, and if compared to wet chemical etching such as *Potassium Hydroxide* (*KOH*) and *Tetra Methyl Ammonium Hydroxide* (*TMAH*), Bosch Process has a higher aspect ratio. The process is a cyclic succession of two steps: CF_4 and SF_6 exposure. SF_6 is a gas used as an etchant for silicon, while CF_4 is a gas used to passivate the already etched walls to achieve the requested anisotropy level. The succession of the two gases is called *loop* and the sequence of loops determines the so-called *scallopings*, which can resemble “waves” on the etched surface. These can

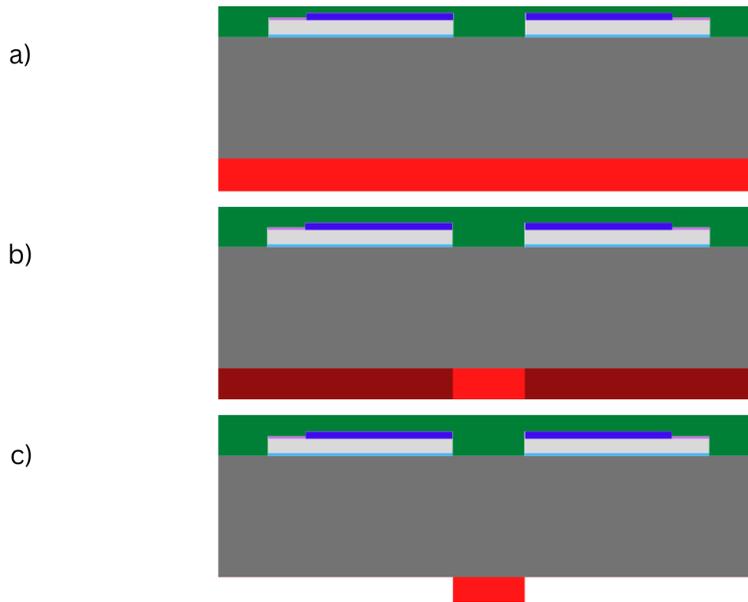


Figure 3.20: Back side photolithography. a) Photo resist coating; b) Exposure; c) Photo resist development.

be reduced by adjusting exposure parameters for the gases, such as exposure time for every loop [97]. Figure 3.21 illustrates how *Bosch Process* works. According to

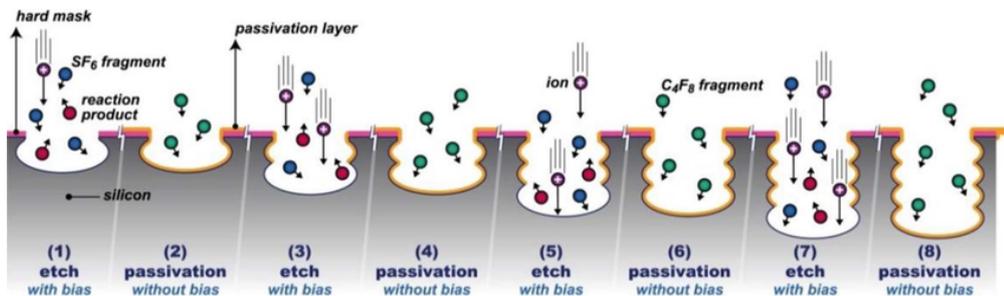


Figure 3.21: Bosch Process illustration. [98]

the manual of the tool, table 3.9 shows the recipe parameters. The process clearly also affects the photo resist and SiO_2 , apart from silicon. Since the thickness of silicon to etch amounts to $380 \mu m$, it is appropriate to consider an etching rate between 600 nm/loop and 800 nm/loop . Considering that the only modifiable parameter is the number of loops, it is strongly recommended to set an initial number of loops lower than expected to inspect the real etched amount under a

Table 3.9: Back side silicon etching recipe (*SPTS Rapier DSE*)

Process	Si etch rate	PR etch rate	SiO ₂ etch rate
DRIE	Trench 2 μm : 300 nm/loop Trench > 200 μm : 800 nm/loop	6 nm/loop	2.5 nm/loop

microscope and to estimate the etch rate through simple calculations involving the etched thickness and the number of loops. Therefore, the remaining loops should be estimated, considering an overestimation equal to 5%-10% of the overall amount, to be sure to etch the global thickness. By practical evidence, the required number of loops is around *630-650*, including loops overestimation, with an average etching rate of *600 nm/loop*. When the silicon is completely etched, the etching stops automatically, as parylene-C and aluminum are two natural stopping agents. With regard to the photo resist, it is etched with its specific etching rate, for a total amount of $\sim 3.78 \mu\text{m}$; still $\sim 4.22 \mu\text{m}$ of it is present. For this reason, before releasing the structures, it is necessary to strip the photo resist from the wafer. The optimal and suggested solution would be a exposure to oxygen plasma, but the parylene-C would be affected. Accordingly the best solution, even if not optimal, is to perform an *Acetone* bath for at least *2 minutes* followed by an immediate *IPA (IsoPropyl Alcohol)* rinse to avoid *Acetone* to contaminate the structures, since it is characterized by a very high vapor pressure. The wafer can, then, be rinsed in DI water and dried. The result of dry etching is shown in figure 3.22.

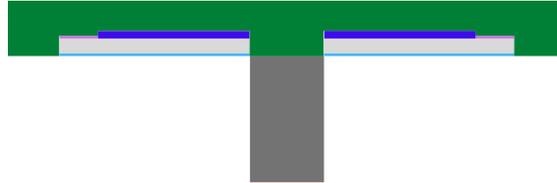


Figure 3.22: Back side dry etching.

3.2.13 Silicon dioxide (SiO₂) deposition on back side

A protective and insulator layer is required for all the structures on their back side (figure 3.23) before they are released. For this purpose, SiO₂ is chosen. It is deposited with *PECVD (Plasma Enhanced Chemical Vapor Deposition)* at *IPHYS Clean Room* with the *Oxford Instrument Plasmalab System 100 – PECVD*, already mentioned in section 3.2.4. The overall result is a full coverage of *500 nm* of SiO₂,

for a total deposition time of *8 minutes* and *30 seconds* at *60 nm/min* of deposition rate.

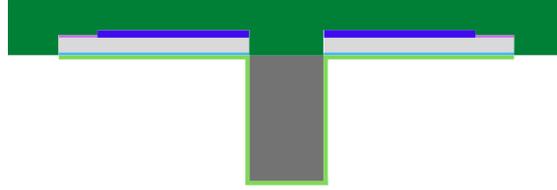


Figure 3.23: Back side SiO₂

3.2.14 Structures release

The final microfabrication step towards the realization of CMOS-compatible micro-electrodes is the release of the structures, which, until now, are fixed together to the wafer because of the $5\ \mu\text{m}$ parylene-C adhesive layer. To release the structures, the parylene-C must be stripped. The optimal recommended stripping method is *high-power oxygen plasma* to be performed for at least *10 minutes*. The deputed machine to perform this treatment is the *TePla GiGAbatch*, already used for photo resist strip. The wafer must be placed on a horizontal quartz holder, so it is easier to collect the free-floating structures (figure 3.24).

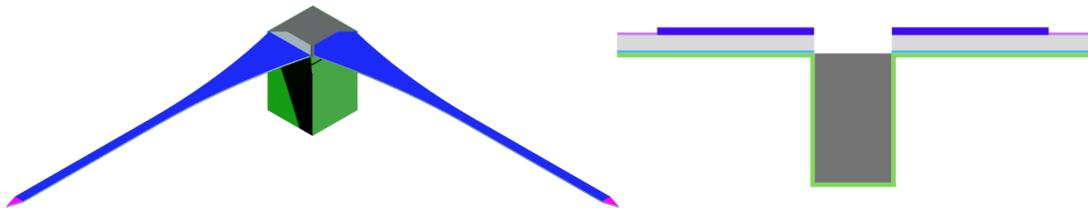


Figure 3.24: Back side dry etching.

3.3 Design results

As mentioned at the beginning of the current chapter, the whole structure has been completely designed on Autocad (version 2023, Autodesk Inc.). The starting point of the design is represented by a *.gds* layout provided by the *CMi* [99]. It contains all the most important information, such as wafer edges, alignment marks, camera openings for photolithography tools. It is a very useful template that can help with the dimensions of the layout to design. Figure 3.25 shows the overall design on front side and back side, defined with the help of the aforementioned *CMi* template.

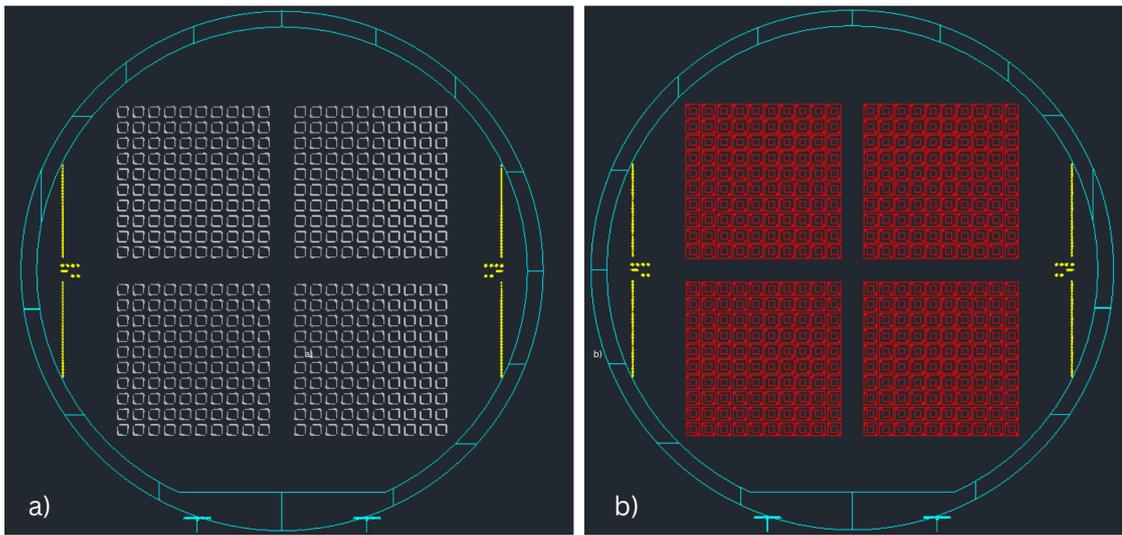


Figure 3.25: Wafer design overview (Autocad, Autodesk Inc.). a) Front side; b) Back side

3.3.1 Chip sizing

The overall dimension of the CMOS chip is the very first parameter to define. In fact, it acts as support for the probes. Since the microelectrodes fabrication is oriented to be part of the *Smart Micro Neural Dust* project, it must follow some strict constraint. CMOS chip will be a $200 \times 200 \times 75 \mu\text{m}^2$ parallelepiped. Therefore, since the layout is needed especially for photolithography, it is fundamental to define the surface dimensions. Since the back side etching of silicon is anisotropic, but not perfectly perpendicular to the wafer, it is appropriate to overdimension the

chip size. For this reason, a $250 \times 250 \mu\text{m}^2$ chip is designed. This aspect also helps avoiding that the probes pads are fabricated perfectly on the edge of silicon chip. This last issue would be critical during silicon etching, since some silicon would be over-etched even under the aluminum probes, thus compromising the stability of the structure. Figure 3.26 shows the Autocad (Autodesk Inc.) detail of the silicon pad dimensions.

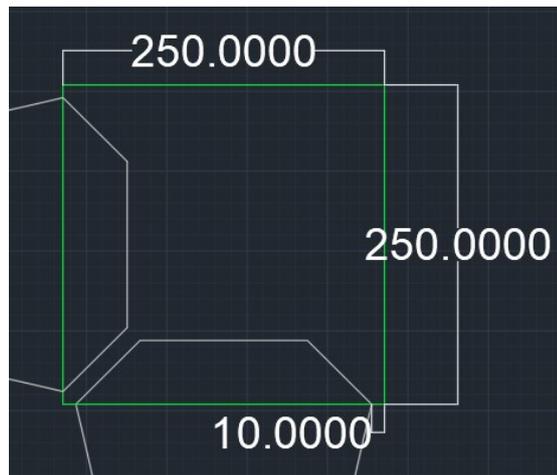


Figure 3.26: Support CMOS chip dimensions (Autocad, Autodesk Inc.)

3.3.2 Probes length

A critical aspect of stimulation is the length of the probes. In fact they must be long enough to be able to penetrate the cortical layer of the brain and reach the neurons so that they can be correctly stimulated. For this reason, the minimum free length to provide to the probes to allow correct implantation is set to 1.5 mm. According to the expected chip thickness of $75 \mu\text{m}$, the total length of the probes should be at least $1575 \mu\text{m}$.

3.3.3 Probes body shape

The design has been structured to contain four different layouts, useful for assessing the mechanical strength during the insertion procedure. The layouts are distributed in the wafer in four different quadrants, as shown in figure 3.25. In particular, two main layouts are investigated. Both of them are characterized by a straight terminal part near the tip, while the main differences can be found on the proximal part, near the pads. The proximal part can be straight or curved. Below, details of the designs are explained.

Design 1

The proximal part of the probe (50% of the total length) is curved, while the distal part is straight. In this design, the mask of Silicon dioxide is set to cover all the probe body, since the pad will be contacted by the embedded CMOS chip. Figure 3.27 shows a detail of the design.

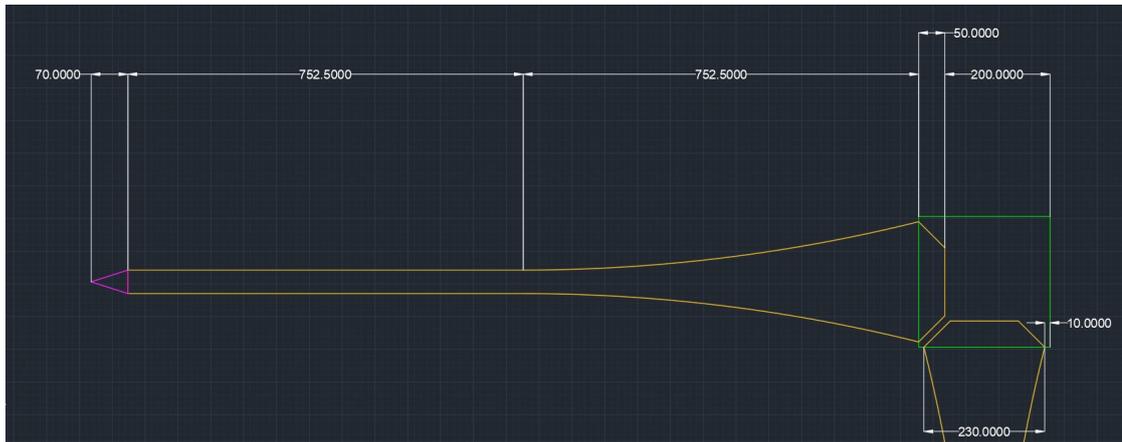


Figure 3.27: First design (Autocad, Atodesk Inc.) - geometrical dimensions

Desing 2

One difference between the current design and "design 1" is that now the distal straight part represents the 60% of the probe, while the curved one 40%. Another difference concerns the insulator, which is, in this case, limited to the probes body, excluding pads and leaving $30 \mu m$ free after pads themselves. This is performed in order to avoid the increase of rigidity of the probe at the bending point brought by the Silicon dioxide. Figure 3.28 shows details of the current design.

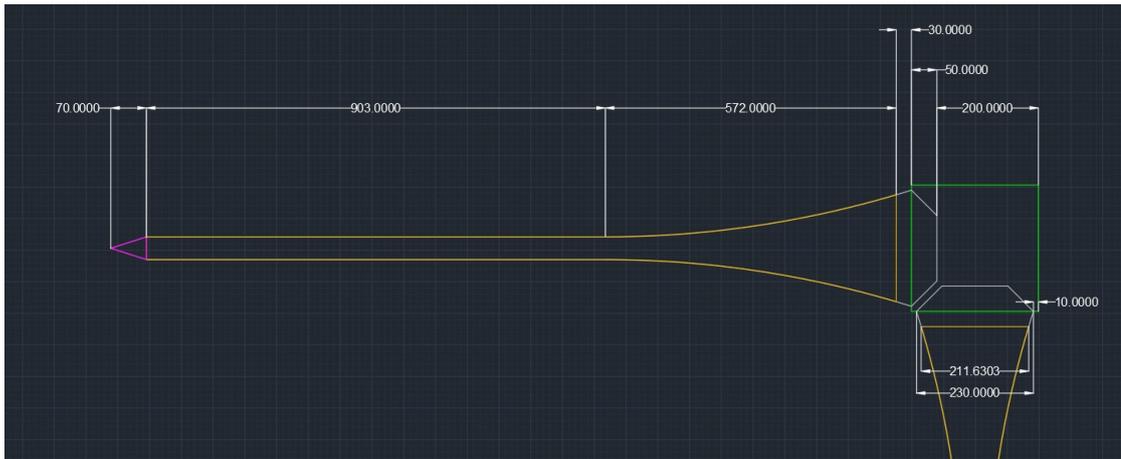


Figure 3.28: Second design (Autocad, Atodesk Inc.) - geometrical dimensions

Design 3

The current design is the same as "design 1" in terms of dimensions and geometry, but it is similar to "design 2" concerning the Silicon dioxide deposition. In fact, also in this case, insulator is deposited all over the probes body leaving the pads free. Figure 3.29 shows some related characteristics.

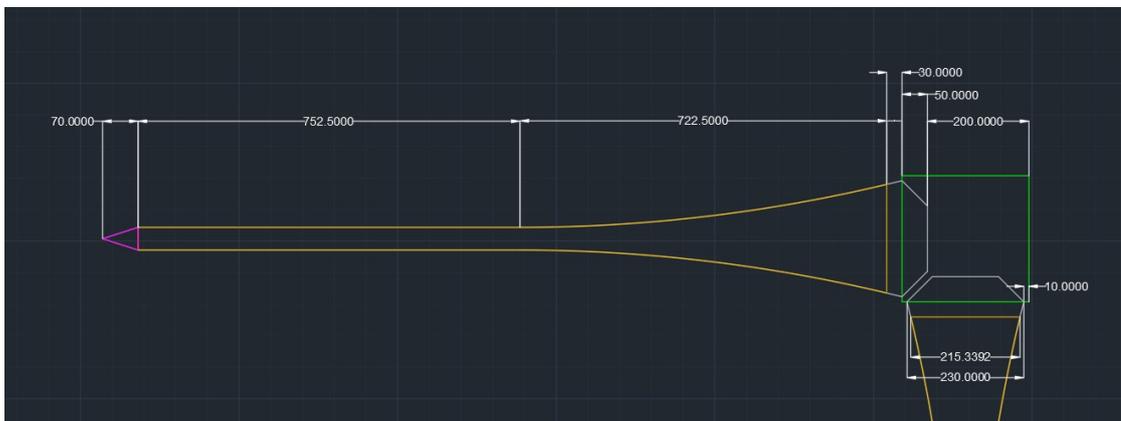


Figure 3.29: Third design (Autocad, Atodesk Inc.) - geometrical dimensions

Design 4

Fourth design has some substantial differences in terms of geometry. In fact the curved proximal part is replaced by a straight trapezoidal part, as shown in figure 3.30 and it is similar to the design presented in the famous *Michigan Probe* [83]). Moreover the distal straight part represent 65% of the total probe length, while the

trapezoidal part 35%. In the end, Silicon dioxide insulates all the probe, including pads.

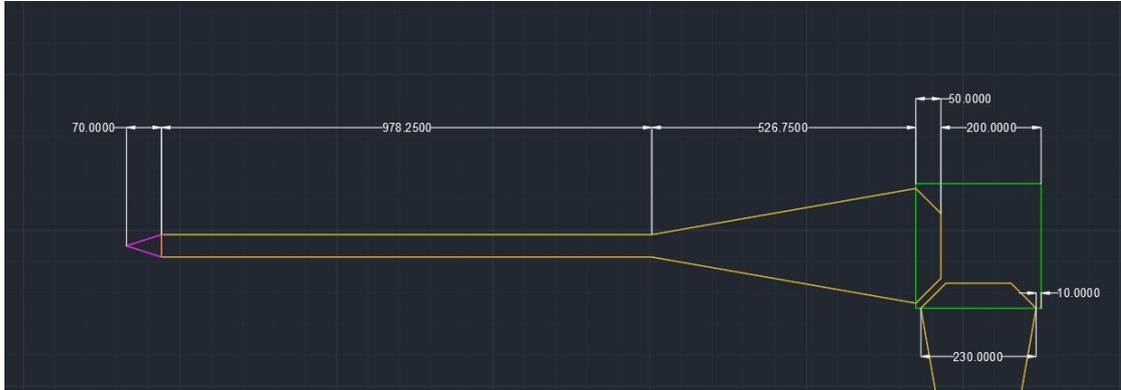


Figure 3.30: Fourth design (Autocad, Atodesk Inc.) - geometrical dimensions

3.3.4 Probes tip shape

The tip is the fundamental unit of a microelectrode, as it is the only exposed conductive part that has to deliver charge to the tissue, during a stimulation pulse. Since every material is characterized by its own CIL, it is appropriate to design the electrode with a defined exposed surface. As the project requirements include a surface of $\sim 1600 \mu m^2$, the tip is designed with a triangular shape, with $45 \mu m$ for the base and $70 \mu m$ for the height. Therefore the total exposed surface is $\sim 1575 \mu m^2$. Figure 3.31 shows some details related to the tip.

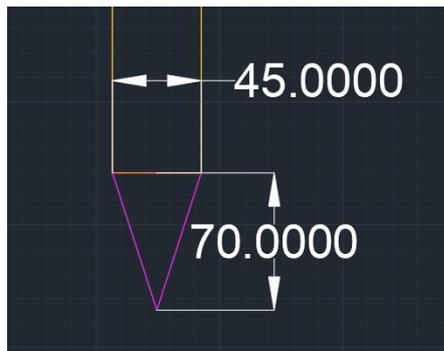


Figure 3.31: Details of a microelectrode tip

3.3.5 Probes orientation

Since the chip is square-based, the two required probes can be fabricated 180° or 90° oriented on a horizontal plane. It has been decided to fabricate them on two adjacent edges, thus 90° oriented, as it is possible to notice from design illustrations. Pads have been designed to guarantee at least $14\ \mu\text{m}$ gap between each other, which can, therefore, ensure the insulation of the probes. The main reason for the chosen orientation is that, when they are bent, they are more next to each other, thus, the generated electric and magnetic fields during the stimulation pulse are more focused in a limited volume, exploiting an increased selectivity in stimulation.

3.4 Microfabrication results

Microelectrodes fabrication has been demonstrated to be an effective technique to be used for microelectrodes integration. The main reason is related to the convenience of merging the CMOS chip fabrication with the probes fabrication in post-process, all completely achieved in the cleanroom. Photolithography steps are the most crucial ones since they are responsible for the shape of the probes. Image 3.32 shows the silicon wafer used to obtain the free-floating miniaturized implants.

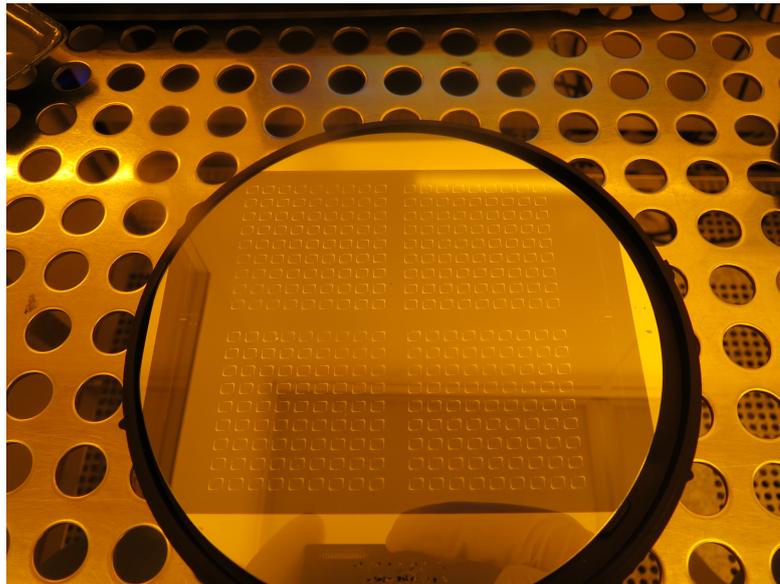


Figure 3.32: Overview of designs distribution on silicon wafer.

3.4.1 aluminum layer

Aluminum layer represents the framework of our structures. For this reason, the layout must be carefully transferred on the wafer, together with the cross-shaped *alignment marks* shown in figure 3.7. Figure 3.33 shows the result of aluminum deposition, through optical microscopy (a,c,d) and SEM (b) (*Zeiss LEO 1550, Carl Zeiss Sports Optics, Wetzlar, Germany*) inspection. SEM image shows a homogeneous granular pattern, due to the room temperature sputtering. It has been demonstrated by [100] that an increase in deposition temperature causes the growth of agglomerates, thus, a decrease in homogeneity.

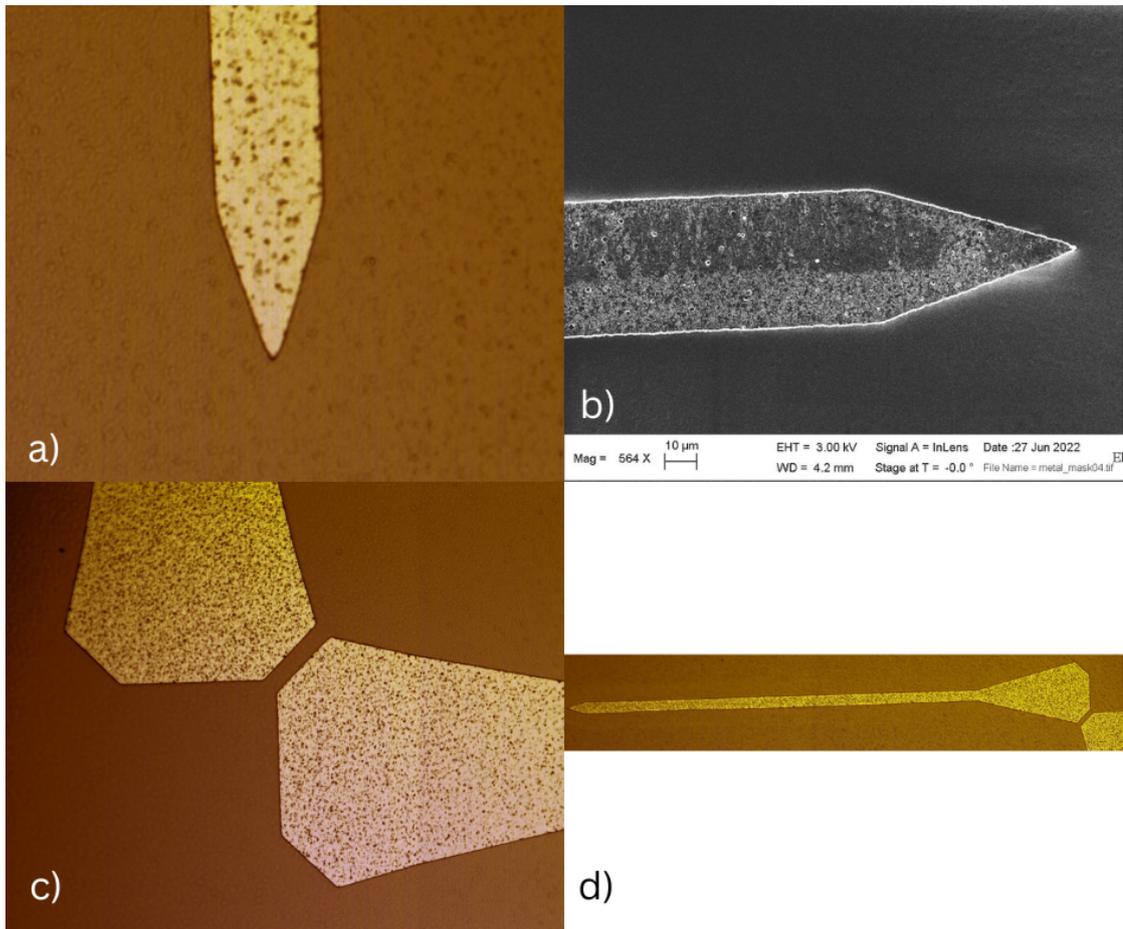


Figure 3.33: Aluminum layer deposition results. a) Detail of the tip (optical microscope); b) Detail of the tip (SEM acquisition); c) Detail of the pads (optical microscope); d) Overview of a probe (optical microscope)

3.4.2 Silicon dioxide layer

Silicon dioxide is crucial to guarantee the insulation of the probes. This layer must be perfectly overlaid with the aluminum one. Therefore the alignment is fundamental before the UV exposure in photolithography, and it has not represented an issue since the alignment marks were correctly printed on the wafer. Like the aluminum framework, also the silicon dioxide layer has been exposed in high quality to increase the precision of the overlay 3.34. From figure 3.34c it is possible to notice that the exposed tip correctly meets the design constraints. In fact, the base is $\sim 45 \mu m$, while the height is $\sim 70 \mu m$. Furthermore, an analysis of the thicknesses of the layers has been conducted with the *Bruker Dektat XT Profilometer* (*Bruker, Billerica, Massachusetts, United States*). It consists of a small diamond-tipped stylus that is put in contact with the surface whose thickness has to be measured. The measure of the thickness is achieved electromechanically, thanks to the connection to an LVDT (Linear Variable Differential Transformer), which senses the electrical signal coming from the diamond tip. Figure 3.35 shows the 3D overview of part of the probe body and the tip. The thickness is identified through a color scale. Moreover, the 2D plots of both the frontal and lateral cross-section profiles of the probe are displayed. It is clearly visible that the tip has an overall thickness of $\sim 4 \mu m$, while the probe body $\sim 5 \mu m$.

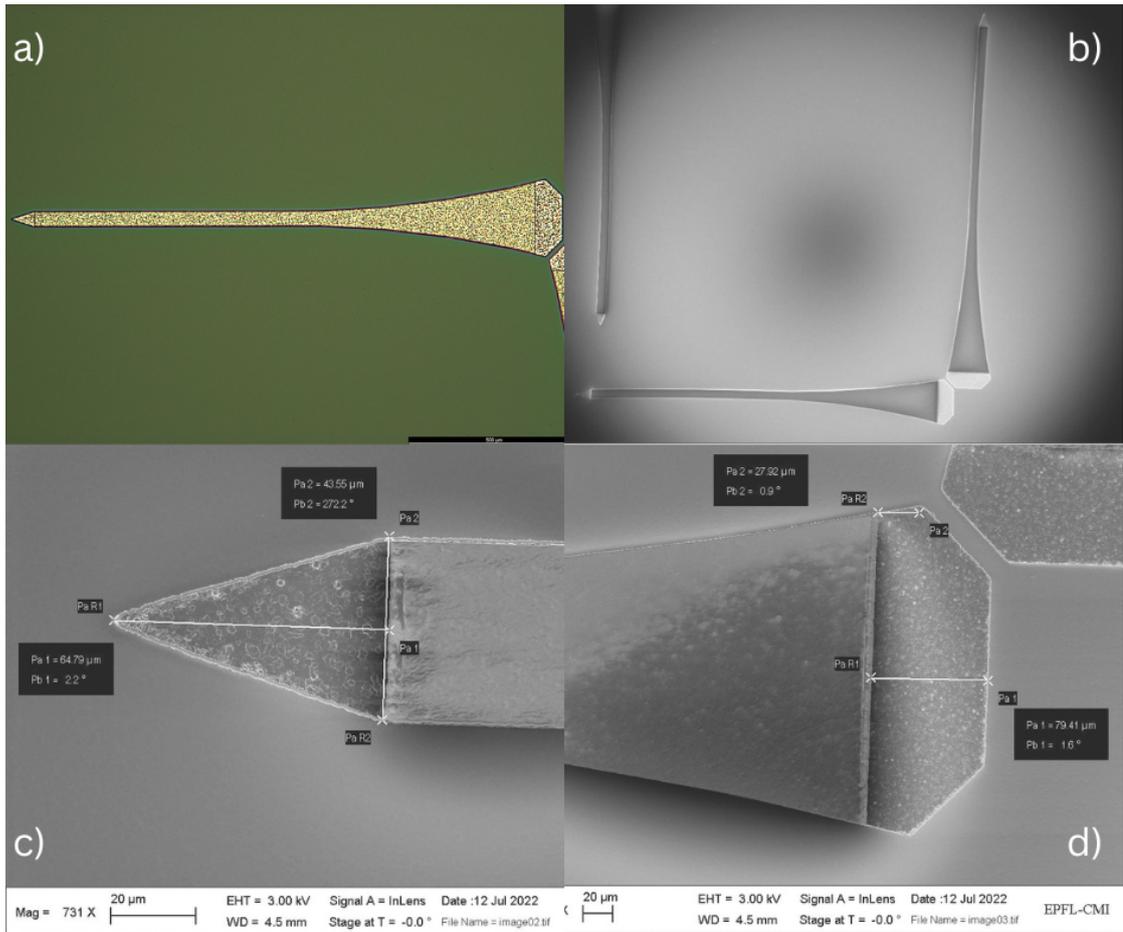


Figure 3.34: Aluminum and SiO₂ layers. a) Overview of a probe (optical microscopy); b) Overview of two probes (SEM acquisition); c) Exposed Al tip (SEM acquisition); d) Exposed Al pad (SEM acquisition).

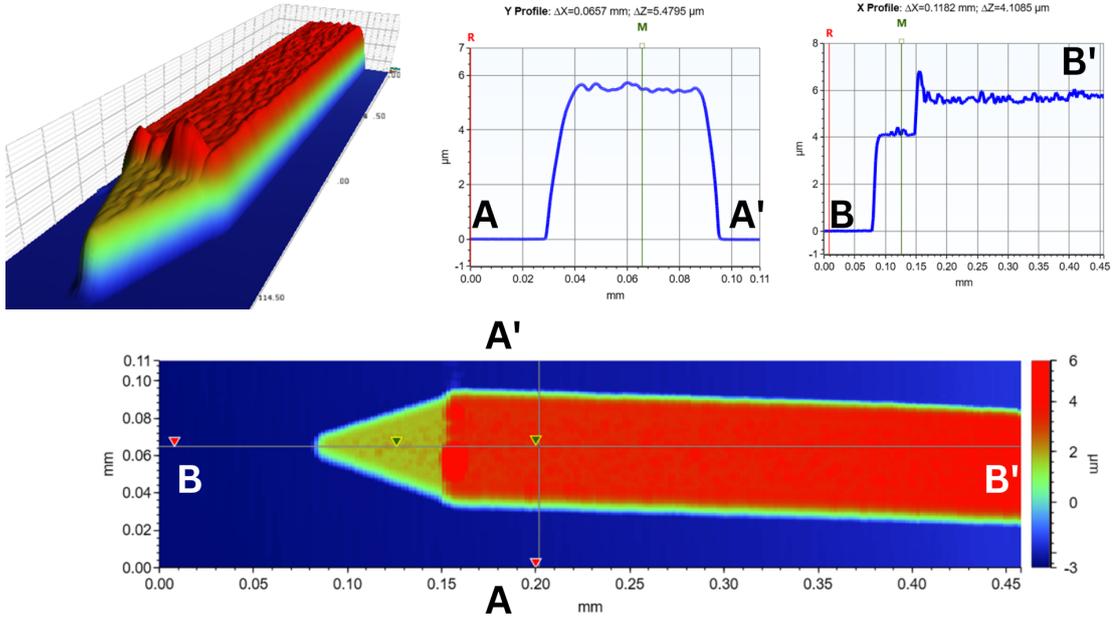


Figure 3.35: Profilometer analysis conducted on fabricated probes. 3D reconstruction of the probe and 2D frontal and lateral cross-section profiles.

3.4.3 Back side etch

Once the front side of the wafer is completed with the definition of both the aluminum and silicon dioxide layer, a back side etch is needed to make the structures free-standing and to leave the probes linked two by two at 90° of orientation among each other. Only the bare minimum of silicon must be etched to maintain the wafer intact at the edges, thus allowing the correct handling of the latter in the tools. For this reason, back side photolithography is needed, and we must be sure about the correct alignment of the layout with the one on the front side. The result of the correct alignment, achieved through the aforementioned alignment marks, is demonstrated by figure 3.36, which is obtained with a traditional optical microscope with infrared light from the bottom. The wafer is placed upside-down, with the front side on the transparent microscope holder. The darker square on the back side represents the left photo resist as a protective layer to avoid the etching of silicon since it will be preserved to create the silicon pillar containing the CMOS chip. On the other hand, probes shadows can be noticed on the front side, thanks to infrared light. This is made possible by the transparency of silicon to IR light frequency band. As it is possible to assess from figure 3.37, photolithography has been correctly performed since we can clearly check that there are silicon pillars on the back of the wafer (figures 3.37a,c), while the front side design of the probes is still attached to the parylene-C layer (figures 3.37b,d).

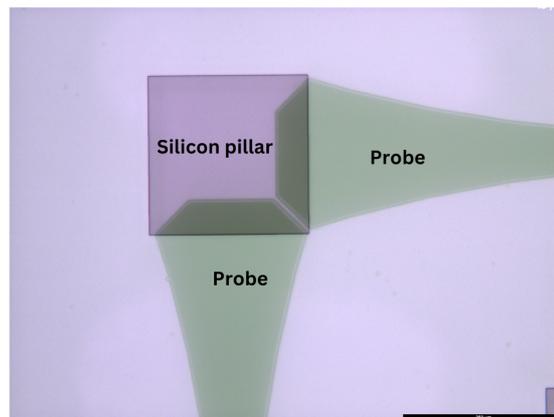


Figure 3.36: Back side alignment assessment through optical microscopy on transparent wafer holder and infra-red (IR) light from the bottom.

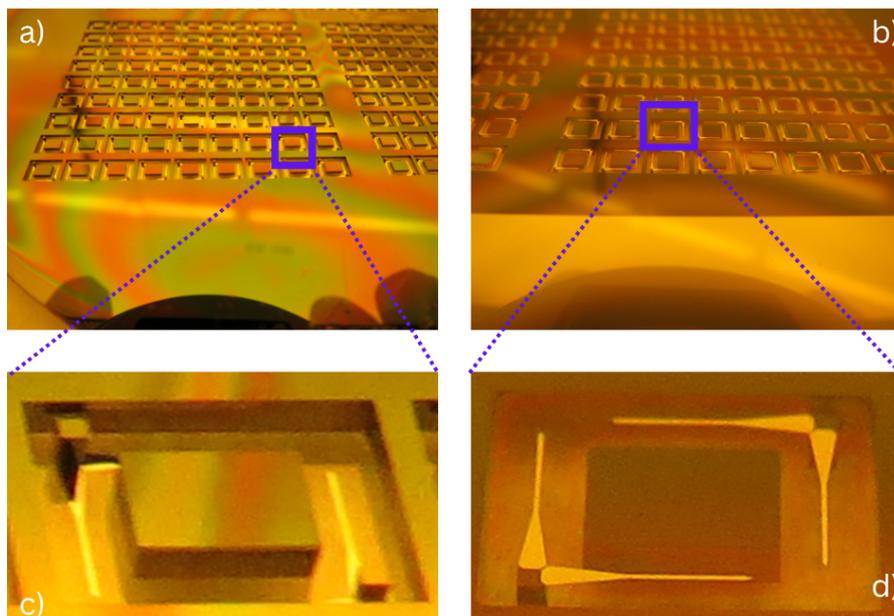


Figure 3.37: Back side etching results. a) Back side view; b) Front side view; c) Back side detail of two etched structures; d) Front side detail of two etched structures.

3.4.4 Free standing structures

As mentioned in the procedure, the last step involves the detachment of the structures, and it is done by breaking the parylene-C layer. Once the structures are released from the wafer, they look like the ones shown in figure 3.38.

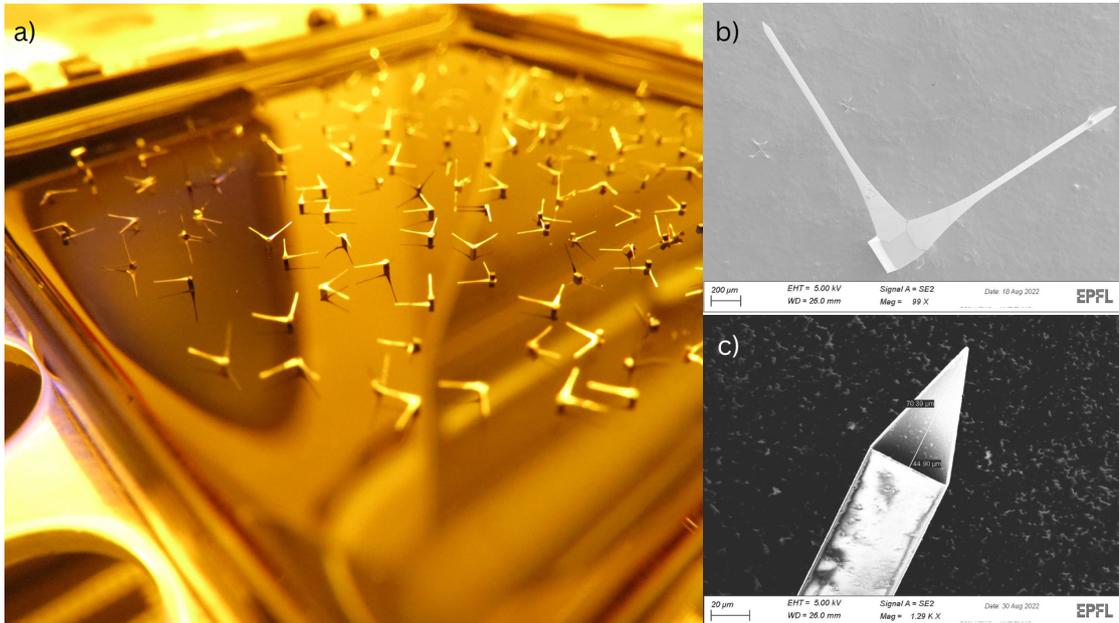


Figure 3.38: Free-standing implants. a) Overview of collected structures after parylene-C removal; b) SEM acquisition of a single structure, showing total compliance with design constraints; c) Detail of the exposed tip of a structure.

3.4.5 Bent structures

Once the structures are released, to make them suitable for the implant, they must be bent. The bending procedure is performed manually, but it can be optimized, also with a view of an industrial application. Released structures are handled with precision tweezers and pushed against a rigid wall, in this case, a slide of a microscope, fixed on a holder. The result is, therefore, the structure that can be seen in figures 3.39a,b taken with an optical microscope immediately after the bending. On the other hand, the same bent structures are characterized at SEM, as shown in figure 3.39c.

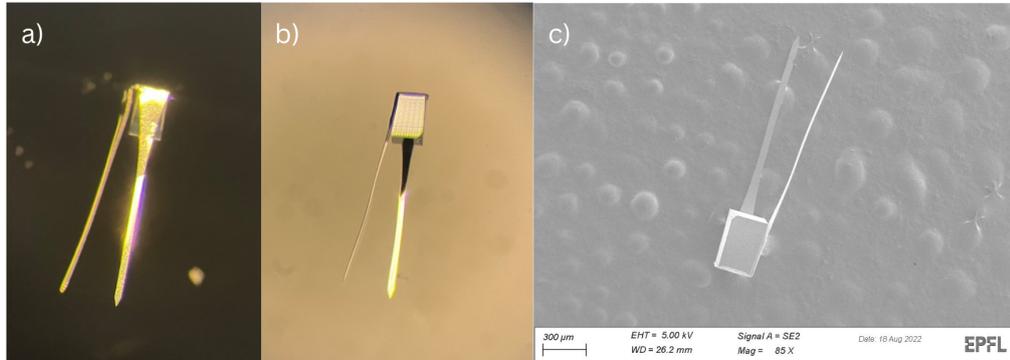


Figure 3.39: Free standing bent structures. a),b) Single structure acquired through optical microscopy; c) SEM acquisition of a single structure

Chapter 4

Electrochemical characterization

It has already been discussed that one of the crucial aspects of integrated microelectrodes is represented by electrochemical stability. In fact, processes such as microelectrode cut and integration on the dedicated pad on a chip could affect the electrochemical properties of the microelectrode. This assessment covers the last part of my work. Before proceeding with the description of the procedure and the setups, it is appropriate to describe some details about electrochemistry in general, and applied electrochemistry to microelectrodes.

4.1 Electrochemistry introduction

Electrochemistry is the branch of chemistry, which is responsible for interrelating electrical and chemical effects.[101] Since microelectrodes have a crucial role in delivering charge to the surrounding human tissues, once they are implanted, it is appropriate to analyze their electrochemical behavior. Electrical current and voltage changes are taken into consideration to gain information on the types of chemical reactions occurring at the microelectrode-electrolyte solution interface. The basic setup needed for characterization is a *three electrodes electrochemical cell*, as shown in figure 4.1 The first bottom-line requirement is the presence of a conductive mean, through which current can flow among the different electrodes. It is, thus, imperative that the solution contains electrolytes, simulating the brain tissue environment. For this purpose, a *buffer solution* is required, which only contains water and dissolved salts. Salts in water dissociate, causing the formation of ionic species, hence providing a suitable environment for charge motion. As we can notice from figure 4.1, the characterization is focused on the *working electrode*, while the two remaining auxiliary electrodes play a key role in the setup.

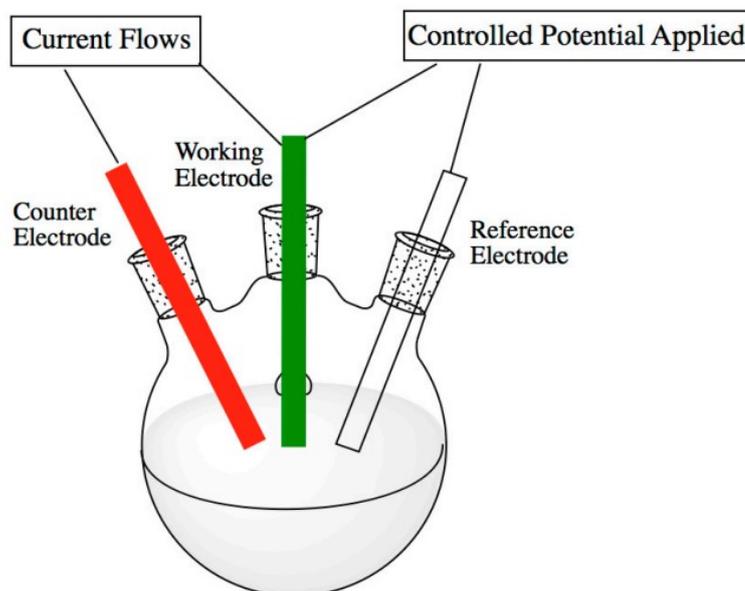


Figure 4.1: Example of a three electrodes electrochemical cell for electrodes characterization.[102]

In particular *reference electrode* is crucial to provide a reference voltage for the working electrode, thus controlling the current flow. Finally, *counter electrode* acts like a sink for the current flow between itself and the *working electrode*. In brief, the voltage value of the *working electrode* is set using *reference electrode* as zero voltage reference, while the current due to a forced potential value different from zero of the *working electrode* flows between the latter and the *counter electrode*, resulting in a decoupled circuit, whose reasons are meticulously explained in [103]. Current can flow only if there is a difference in voltage between the *working electrode* and the *counter electrode*. Therefore, the voltage is applied through a *Potentiostat*, a very powerful electronic device that is needed in the aforementioned characterization setup, for two main reasons [104]:

- It induces a specified potential drop between the *working electrode* and the liquid solution.
- It amplifies the resulting current from the electrochemical reaction at the *working electrode*, due to redox chemical reactions.

As mentioned, the *working electrode* is the electrode whose characteristics have to be assessed, thus depending on the application under analysis. With regard to the reference electrode, the most common and frequently used ones are *Ag/AgCl*

electrode, saturated calomel electrode (SCE), but also *Standard Hydrogen Electrode (SHE)* and *Normal Hydrogen Electrode (NHE)*. On the other hand, the *counter electrode* should be made of good conductive material, and the best choice is platinum.

4.2 Electrochemical characterization techniques

Electrochemical characterization is performed with the so-called *Voltammetric methods*, defined as techniques that involve the application of a potential (E) to an electrode and the subsequent monitoring of the resulting current (i) flowing through the electrochemical cell [105], specifically between *working electrode* and *counter electrode*. In particular voltammetric methods are also considered *active* techniques, since the potentiostat actively forces a potential, thus it induces redox reactions at the electrodes-electrolyte interface. In this scenario, the most used characterization techniques for electrodes and microelectrodes are the following:

- Cyclic Voltammetry
- Electrochemical Impedance spectroscopy
- Voltage transient

To better understand how the reactions take place, it is appropriate to describe how the solutions ions distribute themselves in the cell. As precisely described in [103], when the interface between the electrode and the solution is polarized using a DC potential, the charged electrodes can attract solution ions by means of electrostatic forces. On the other hand, this is a dynamic condition, where also counterions of the same solution are present, as shown in figure 4.2.

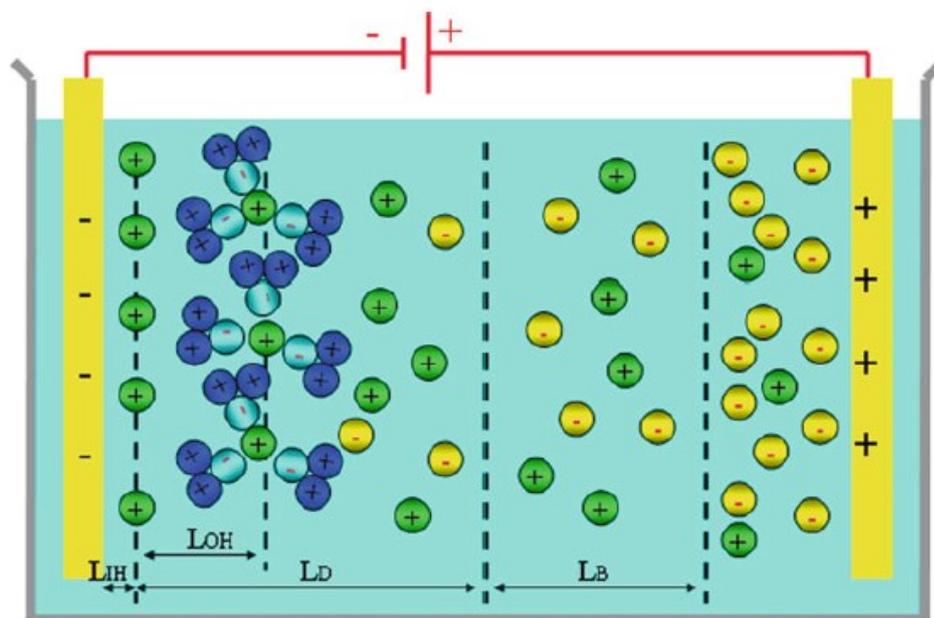


Figure 4.2: Different Helmholtz layers in a polarized water solution. [103]

Considering the cathode, the immediately adjacent layer, predominantly made of solution ions, is called *inner Helmholtz layer*, while the locus of the center of all the charges belonging to this layer is called *inner Helmholtz plane* ($L_I H$). The second adjacent layer, called *outer Helmholtz layer*, with the related *outer Helmholtz plane* ($L_O H$), contains all the solution ions that are surrounded by water molecules, thus not able to reach the interface. The homogeneity of the ion distribution increases as the distance from the polarized electrode increments until a homogeneous bulk solution is reached. This allows the distinction of two other layers: *diffusion layer* (L_D), which also includes the *outer Helmholtz plane* and the *bulk layer* (L_B), where the solution is homogeneous.

4.2.1 Cyclic Voltammetry (CV)

Cyclic voltammetry is one of the most powerful electrode characterization techniques, primarily used to assess the reduction and oxidation of molecular species. This technique, basically, consists on the application of a triangular potential waveform to the *working electrode*. This procedure is, normally, repeated multiple times, resulting in multiple cycles of oxidation and reduction reactions. Potential is, thereby, linearly varied from a starting value to an end value, as shown in figure 4.3.

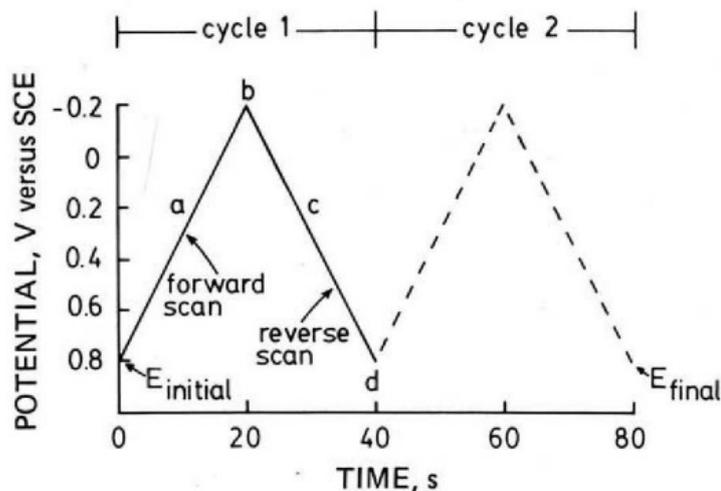


Figure 4.3: Typical excitation signal for cyclic voltammetry - a triangular potential waveform with switching potential at 0.8 and -0.2 V versus SCE.[106]

Since current flow between *working electrode* and *counter electrode* is measured, the resulting plot is represented by the current itself i versus the applied potential to the *working electrode*, E . The traces are known as *voltammograms* or *cyclic voltammograms* [107] and figure 4.4 shows an example of a typical "duck-shape" voltammogram of a reversible reaction.

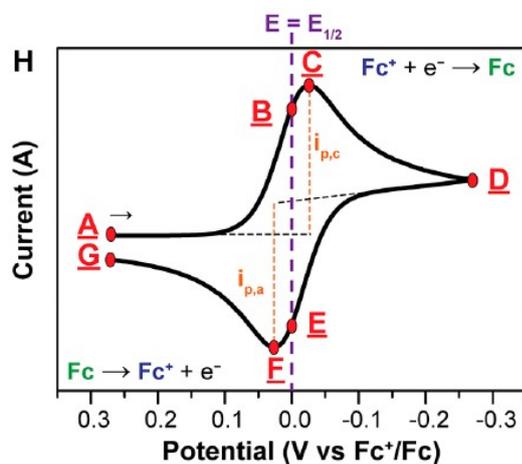


Figure 4.4: Voltammogram of the reversible reduction of a 1mM Fc^+ solution to Fc , at scan rate of 100mVs^{-1} . [107]

A crucial parameter is represented by the *scan rate*, which in figure example

4.4 is set at 100 mVs^{-1} . This value refers to how fast the voltage is changed into a defined scan window, thus representing the derivative function of plot in figure 4.3. As mentioned, the voltammogram shown in figure 4.4 represents a typical pattern of a reversible redox chemical reactions happening at the electrode-electrolyte solution interface. The reversibility can be noticed from the two current peaks, which appear almost symmetric. Normally, to better understand the connection between the plot trend and the chemical reactions happening at the *working electrode*-solution interface, it is advisable to refer to the equilibrium between ferrocenium (Fc^+) and ferrocene (Fc), which is reversible. The involved redox reactions are synthesized as follows:



The equilibrium of the species is described by the Nernst equation, which relates the equilibrium of an electrochemical cell (E) to the standard potential of species (E^0) and the relative activities of oxidized (Ox) and reduced (Red) analyte in the system at equilibrium [107].

$$E = E^0 + \frac{RT}{nF} \ln \frac{(\text{Ox})}{(\text{Red})} = E^0 + 2.3026 \frac{RT}{nF} \log_{10} \frac{(\text{Ox})}{(\text{Red})} \quad (4.3)$$

In the case of ferrocene and ferrocenium, the Nernst equation becomes:

$$E = E^{0'} + \frac{RT}{nF} \ln \frac{[\text{Fc}^+]}{[\text{Fc}]} = E^{0'} + 2.3026 \frac{RT}{nF} \log_{10} \frac{[\text{Fc}^+]}{[\text{Fc}]} \quad (4.4)$$

The equation can predict the changes in concentration of the two species, as the potential varies. Following the path of the voltammogram, from point A to point D, at point A, the $[\text{Fc}^+]$ is located near the electrode. When the potential is decreased, we can notice a cathodic current peak ($i_{p,c}$), due to the continuous diffusion of additional $[\text{Fc}^+]$ from the bulk layer, seen as a charged mass transport, thus current. When potential is further decreased, the volume of Fc solution increases, decelerating the rate of mass transport of $[\text{Fc}^+]$ to the electrode layer, thereby decreasing the current value. At switching potential point (D), the potential is scanned positively, and if the reactions are reversible, a new symmetric pattern can be noticed, with an anodic current peak ($i_{p,a}$). The $[\text{Fc}]$ present at the electrode starts to be oxidized back to $[\text{Fc}^+]$, following the reverse aforementioned processes. In case the redox reactions are not reversible, then the plot is not symmetric anymore. Reversibility depends on the materials involved in the electrochemical cell.

This is the traditional behavior of macroelectrodes. In fact, when it comes to the electrochemical characterization of microelectrodes, the plot does not follow the "duck-shape" pattern with current peaks anymore. The first reason for this is

geometrical. In fact figure 4.1 shows the formation of *planes* of charge, so even the *diffusion layer* is planar. Since the available surface for charge swaps is much smaller if compared with macroelectrodes (tens of μm^2), the *diffusion layer* in microelectrodes is not comparable to a plane anymore. For instance, for a disk-shaped microelectrode, the diffusion layer can be represented by a hemispherical surface. This difference also has an impact on the current, which is at least three orders of magnitude smaller, compared with the one recorded in macroelectrodes. The Cottrell equation is responsible for mathematically describing the current profile at the electrode interface. In [108] it is precisely described how current becomes steady state in case of hemispherical diffusion layer, thus not showing any oxidation/reduction peaks. Figure 4.5 shows the difference in shape of the diffusion layers of macroelectrodes and microelectrodes, while figure 4.6 shows a typical trend of a microelectrode-related voltammogram.

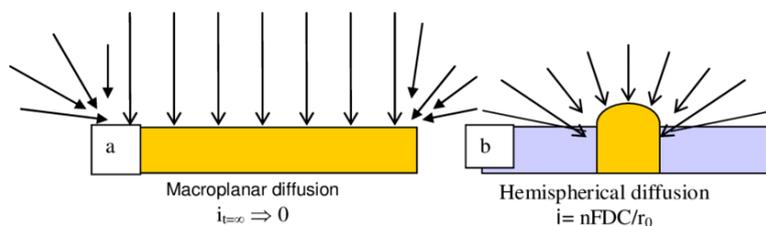


Figure 4.5: Diffusion layer shapes for a) macroelectrodes and b) microelectrodes. [109]

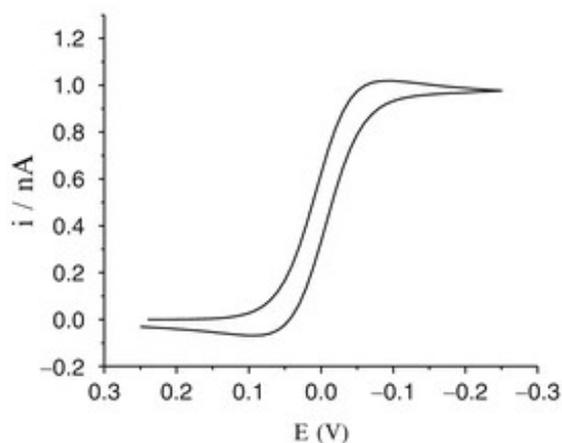


Figure 4.6: Example of a typical microelectrode voltammogram. [108]

With regard to microelectrodes, much information can be deduced from a

voltammogram, such as *Charge Storage Capacity* (CSC). According to [42], cathodal CSC has become a frequently used characterization technique for microelectrode, and it can be defined as "*time integral of the cathodic current in a slow-sweep-rate cyclic voltammogram over a potential range that is just within the water electrolysis window*". Typically, the water electrolysis window for Pt and IrOx electrodes is taken from -0.6 V to 0.8 V versus Ag/AgCl [42]. CSC_c represents a measure of the total amount of charge available for the stimulation pulse, thus representing a crucial aspect to take into consideration and analyze. Normally, only a small percentage (5% to 20%) of the charge stored in the electrode is effectively injected into the tissue during a stimulation pulse. For this reason, CSC_c cannot be considered a good predictor of injected charge during stimulation [42]. Given a voltammogram, the CSC can be calculated as the sum of CSC_c and CSC_a , as follows:

$$CSC_{tot} = \frac{1}{SR * S} * \int_{E_c}^{E_a} |i| dE = \frac{1}{SR * S} \left(\int_{E_c}^0 |i| dE + \int_0^{E_a} |i| dE \right) = CSC_c + CSC_a \quad (4.5)$$

In conclusion, it is fundamental to stress one more aspect of CSC; its value has been demonstrated by [76] to increase with decreasing geometric size of the electrode.

4.2.2 Electrochemical Impedance Spectroscopy (EIS)

Electrochemical Impedance Spectroscopy is the second described characterization technique belonging to the class of voltammetry techniques. It is performed in an electrochemical cell. In detail, it consists of applying a sinusoidal voltage/current to the *working electrode*, varying the frequency of the excitation itself, in order to evaluate the impedance of the microelectrode on a broad range of frequencies, normally from <1 Hz to 10^5 Hz. EIS is a potent tool to foresee tissue and microelectrodes properties, once the latter is implanted. Normally, the applied voltage can go from 10mV [110] to 50mV [111]. A typical example of an EIS plot is shown in figure 4.7.

4.2.3 Voltage Transient (VT)

Voltage transient is the last presented electrochemical characterization technique for microelectrodes. It is defined by [42] as a technique used to "*estimate the maximum charge that can be injected in a current-controlled stimulation pulse*". This technique is performed in a three electrode electrochemical cell too. According to [44], Voltage Transient is performed by "*recording the voltage response to a specific stimulation current pulse and is used to determine the charge injection limit (CIL) of a stimulation electrode*". Again, [44] defines the CIL as "*the maximum charge that can be safely injected to electrodes without reaching the water window*". [42] provides a detailed overview of voltage and current pulse plots for VT (figure 4.8).

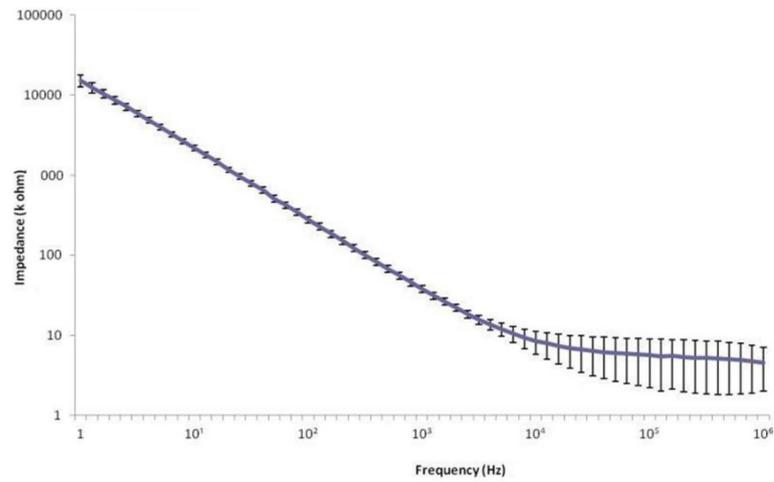


Figure 4.7: EIS plot on Gold discoidal microelectrodes with diameter of $200 \mu m$ [112]

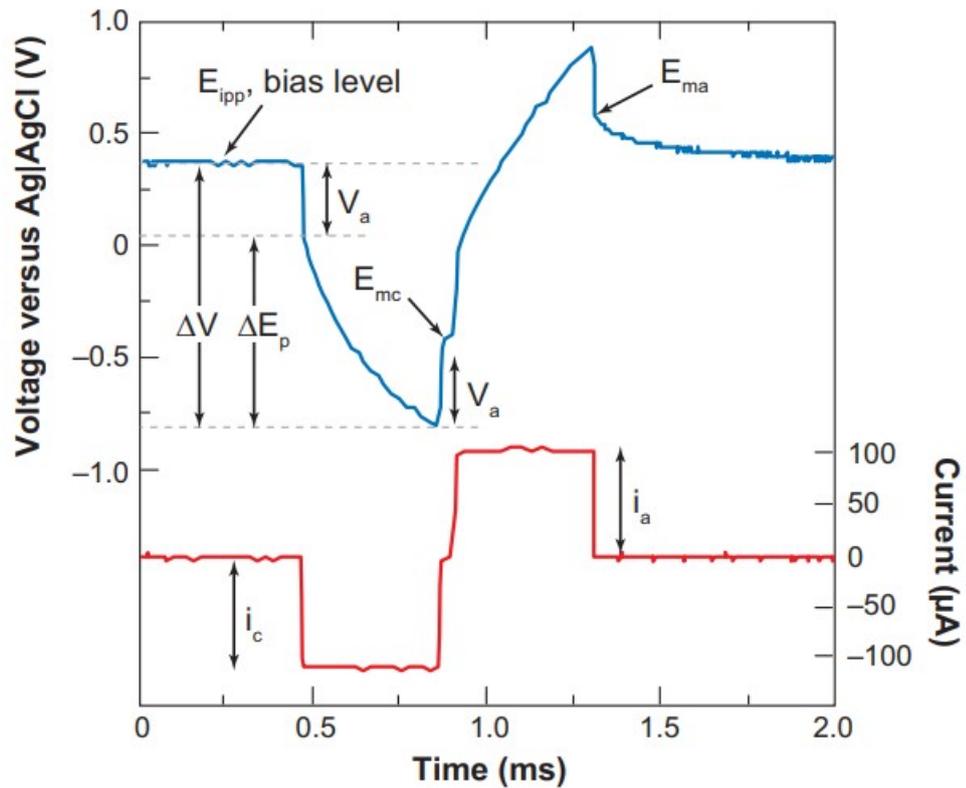


Figure 4.8: A voltage transient of an AIROF (Activated Iridium Oxide Film) microelectrode in response to a biphasic, symmetric ($i_c = i_a$) current pulse. [42]

As we can notice, the current pulse used for excitation is biphasic, which is one of the most used types of stimulation. In fact, it provides charge and subsequent discharge of the surrounding tissues, with an overall charge balance equal to zero. The voltage transient can be synthesized as follows [42]:

$$\Delta V = i_c R_i + \eta_c + \eta_a + \Delta E_0 \quad (4.6)$$

Where:

- $i_c R_i$ is the *Ohmic voltage drop* due to the electrolyte resistance.
- η_c is the *concentration overpotential*, due to the voltage drop determined by the concentration gradient of ions and counterions between the electrode surface and the bulk layer.
- η_a is the *activation overpotential*, which is the voltage drop needed to be maintained on the electrode surface to guarantee a net current flow, which is provided by redox reactions.
- ΔE_0 represents the *shift in the equilibrium potential of the electrode*.

V_a is defined as "the near-instantaneous voltage change at either the onset of the current pulse or immediately after the current pulse is terminated" [42].

4.3 Cyclic voltammetry (CV) in miniaturized electrochemical cell

In the introduction of the current chapter electrochemical cell is mentioned as an inescapable configuration for electrochemical characterization. Therefore, because the overall work is oriented to the fabrication of microelectrodes, the focus is to develop a novel miniaturized electrochemical cell, suitable for integrated microelectrodes. The concept is to maintain the typical framework of a traditional three electrodes electrochemical cell, thus miniaturizing the majority of the components, as shown in the designs in figure 4.9

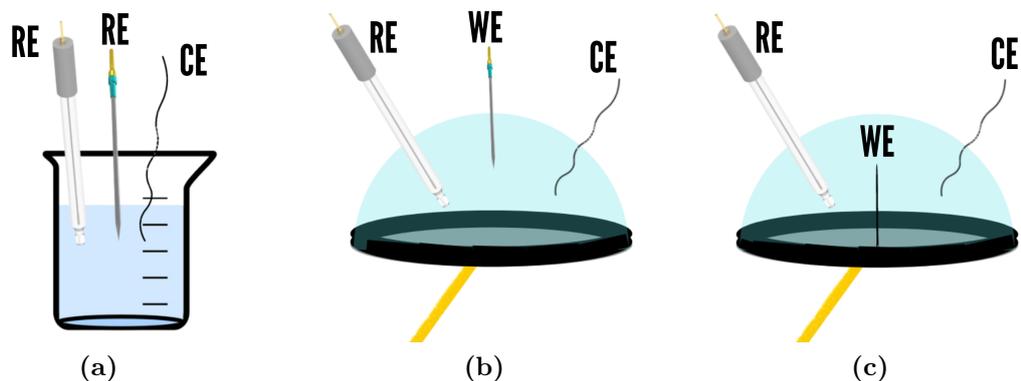


Figure 4.9: Electrochemical cells: a) becker setup for macroelectrodes. b) miniaturized setup - working electrode before integration. c) miniaturized setup - integrated working electrode

Literature proposes several setups for miniaturized electrochemical characterization. For instance, [113] developed a miniaturized characterization setup, suitable for ITO (*Iridium thin oxide*) UMEA (Ultra MicroElectrodes Array) (figure 4.10a). Moreover the same group developed [114] a novel and revised microfluidic platform, mainly based of PDMS (*Polydimethylsiloxane*) for on-chip cell analysis (figure 4.10b). Finally, also [115] fabricated a polymer-based miniaturized electrochemical measurement setup (figure 4.10c).

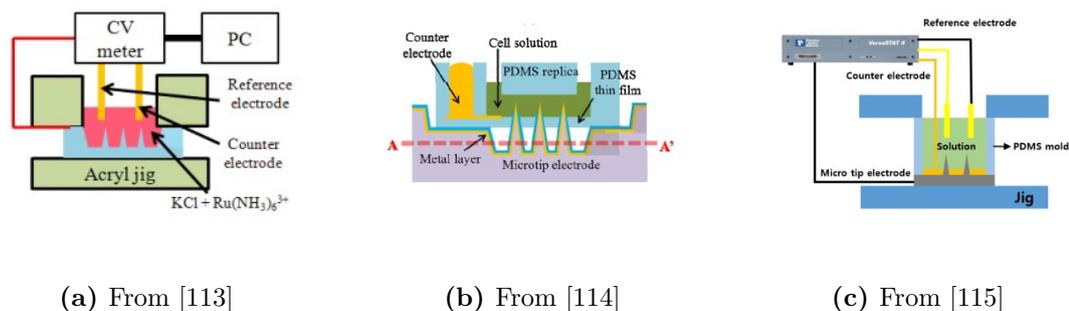


Figure 4.10: Examples of miniaturized electrochemical setups.

Currently, electrochemical characterization is performed only on the commercial Pt/Ir microelectrodes, mentioned in section 2.1 (Item PI20030.5A3, *MicroProbes for Life Science, 18247 Flower Hill Way D, Gaithersburg, MD 20879, United States*). To summarize the setup, the electrochemical cell is implemented with PBS

(*Phosphate-Buffered Saline*), a buffer solution made of four different salts, diluted in 800 ml distilled water [103]:

- 8 g sodium chloride (NaCl)
- 0.2 g potassium chloride (KCl)
- 1.44 g disodium hydrogen orthophosphate (Na_2HPO_4)
- 0.24 g potassium dihydrogen phosphate (KH_2PO_4).

As far as electrodes materials are concerned, the aforementioned Pt/Ir microelectrode is our *working electrode*, a commercial Ag/AgCl is the *reference electrode*, while a Pt-wire is the *counter electrode*. A support stand with clamps is used to keep all the electrodes in the buffer solution, while they are connected to the Potentiostat (*Autolab PGSTAT12, Metrohm Autolab BV, Utrecht, Netherlands*) through electrical clamp connectors. The set parameters for CV measurement are the following:

- Max voltage: +0.8 V
- Min voltage: -0.6 V
- Scan rate: 50-200-500-1000-5000 mV/s
- Number of points per scan: 224
- Number of scans per scan rate value: 5

The approach is to perform five scans to trash for every used scan rate, to let the Potentiostat stabilize. First, CV measurements are conducted on the becker setup (figure 4.11), the traditional electrochemical cell, to assess that the microelectrode works properly. The following measurements are executed on the novel miniaturized electrochemical cell. It is assembled using an O-ring, fixed on a PCB, which is, then, filled with a drop of PBS, that forms a bubble. The first measurements implemented with this cell are done with the entire 5 cm-long microelectrode. All the electrodes pierce the bubble from above, thus it is fundamental to make sure that the conductive parts are located inside the bubble (figure 4.12). Lastly, also the integrated microelectrode is characterized, in order to assess the electrochemical stability even after integration. The miniaturized electrochemical setup is the same as the just introduced one. The only constraint is that the whole system must be compulsorily created on a PCB (figure 4.13), so the integrated microelectrode on the chip can be electrically connected to an external pad, through metallic traces on the PCB.

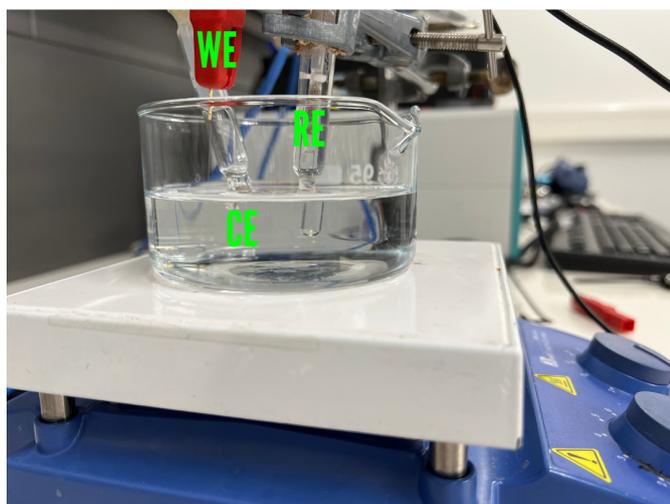


Figure 4.11: Electrochemical cell - becker setup

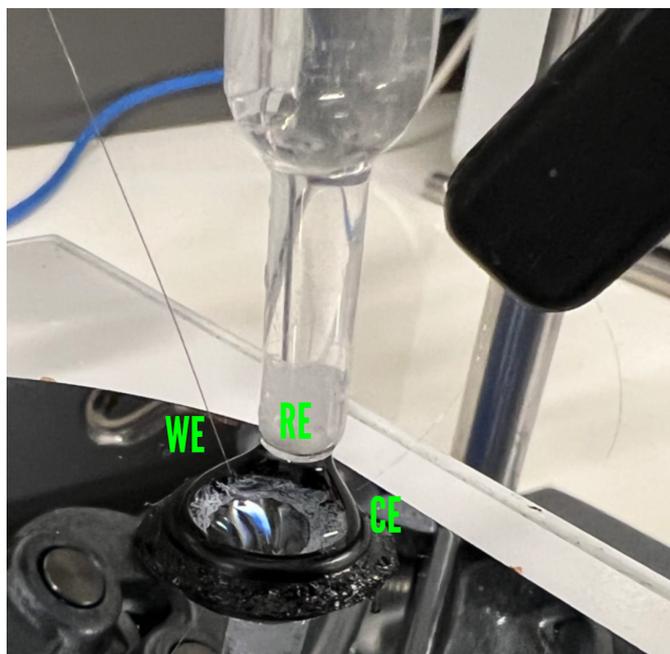


Figure 4.12: Miniaturized electrochemical cell - electrodes pierce the PBS bubble from above

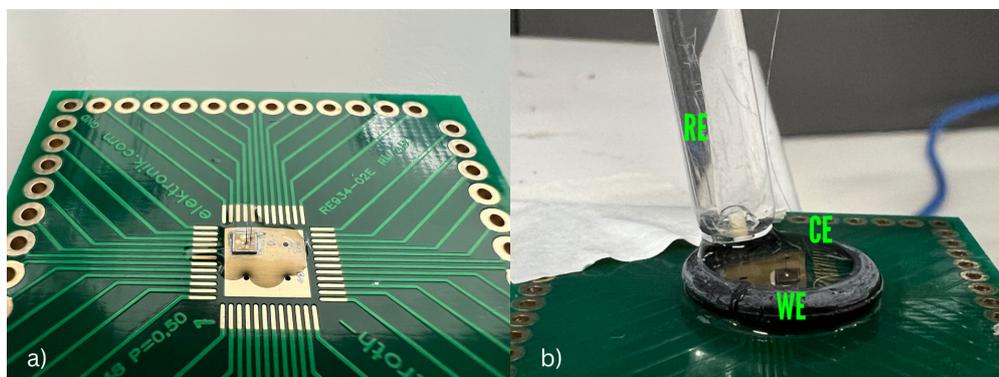


Figure 4.13: a) CMOS chip with integrated microelectrodes; b) Miniaturized electrochemical setup for integrated microelectrodes characterization.

4.3.1 Cyclic voltammetry measurements comparison among pre-integration and post-integration

As aforementioned, cyclic voltammetry measurements are conducted on both the pre-integration and post-integration microelectrode, in order to assess if the electrochemical stability is granted even after integration. Cyclic Voltammetry data are recorded using the mentioned Autolab PGSTAT12 potentiostat and the software *NOVA 2.0* (Metrohm Autolab). In detail, 5 complete scans were recorded for each scan rate value, and a further data processing session is performed using *Matlab* (MathWorks Inc., Natick, Massachusetts, United States). In particular, an averaging procedure is performed on the 5 scans, in order to limit small variability given by the low range current values to detect, few nA. Moreover, to further reduce this variability, a smoothing session, based on interpolation of the data, is performed. Details and related code of signal processing are available in *Appendix B*, while the result of data processing can be seen on the Matlab plots, where, for each scan rate, curves from the different setups are superimposed (figures 4.14,4.15,4.16,4.17,4.18). The first characteristic that is possible to notice is that the plots do not have any peak current due to redox reactions, as expected for microelectrodes [116]. We can also notice that the electrochemical stability is fully preserved, since the two curves are almost coincident. In addition we can clearly confirm that the current range increases with the scan rate increase, since its value is proportional to the square root of the scan rate itself. In fact, for a reversible

reaction, with faster scan rates the diffusion layer reduces its size, and the current increases its value [101] [117]. Moreover, for every scan rate value and for every measurement setup an average CSC value is computed, following equation 4.5. Results of the calculation are summarized in table 4.1.

Table 4.1: Total CSC values [$mCcm^{-2}$] @ scan rates [mVs^{-1}]

Config.	50	200	500	1000	5000
Integrated	2.8189	2.3579	1.8070	1.6536	1.1012
Non-integrated	2.5759	1.2008	0.9836	0.8276	0.6189
Becker	2.3379	1.2349	1.1093	1.0449	1.1129

As we can notice, the CSC values decrease when the scan rate increases. In fact, CSC is related to the capacitance characteristic of the material in question, PtIr in this case. Low scan rate values, thus slower voltage variations, allow the electrolyte to make greater contact with the questioned material surface, consequently, more charge is stored in the electrode, as demonstrated in [118]. In conclusion, the literature can confirm the correctness of the computed values of CSC for metallic Pt or PtIr electrodes. Cogan et al. in [47] found a value for CSC equal to $5.6 mCcm^{-2}$ at 50 mV/s scan rate. Vitale et al. [119] found the CSC of PtIr microelectrode to be $1.2 \pm 0.08 mCcm^{-2}$ at 100 mV/s, while Kane et al. [120] obtained a value for PtIr of $3.375 mCcm^{-2}$ at 50 mV/s.

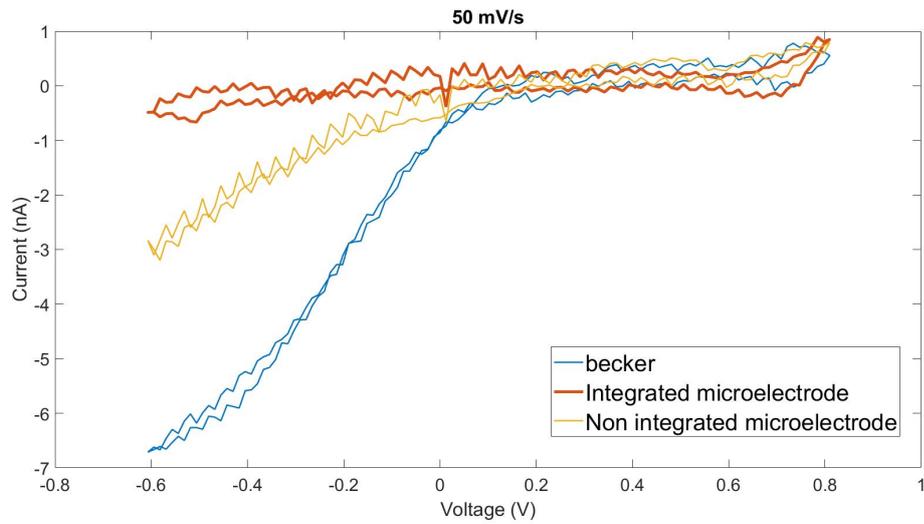


Figure 4.14: Cyclic voltammetry plot of integrated microelectrode @ S.R.=50 mV/s

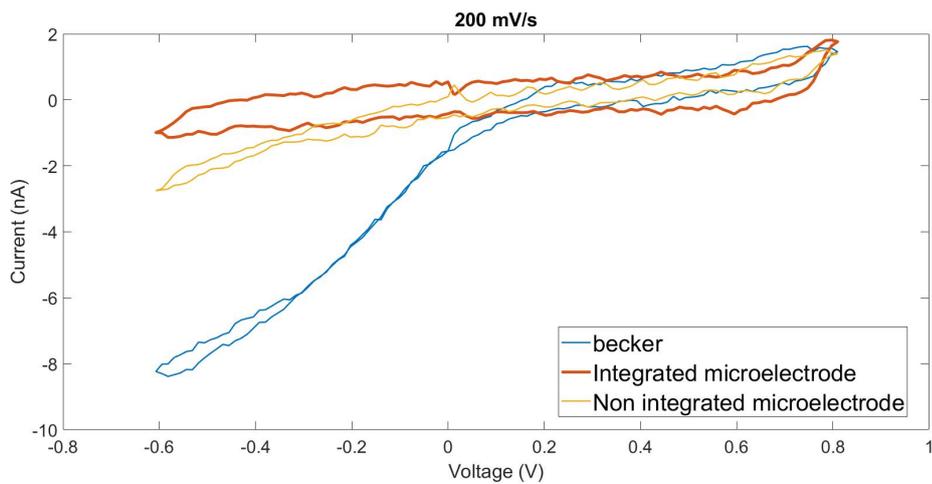


Figure 4.15: Cyclic voltammetry plot of integrated microelectrode @ S.R.=200 mV/s

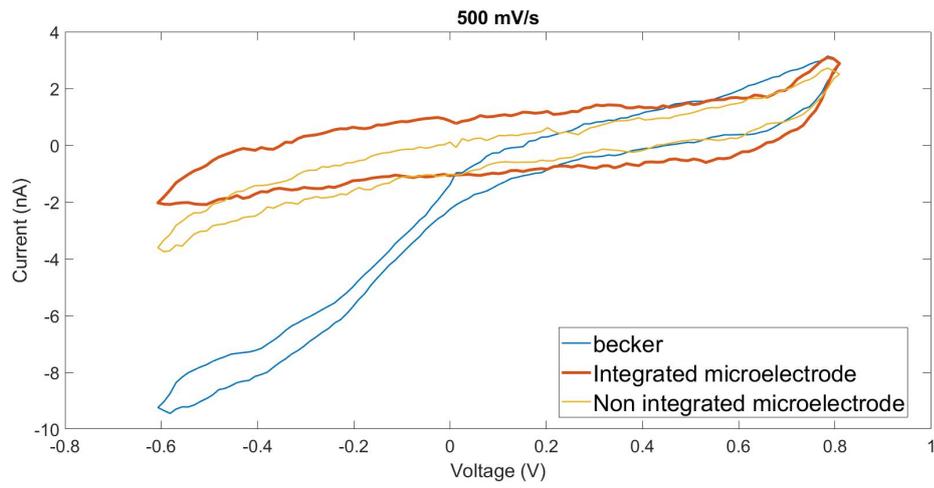


Figure 4.16: Cyclic voltammetry plot of integrated microelectrode @ S.R.=500 mV/s

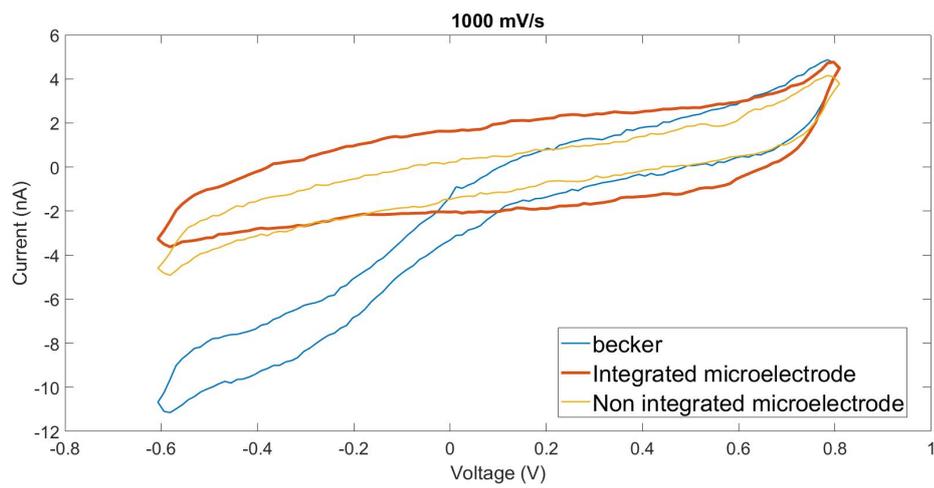


Figure 4.17: Cyclic voltammetry plot of integrated microelectrode @ S.R.=1000 mV/s

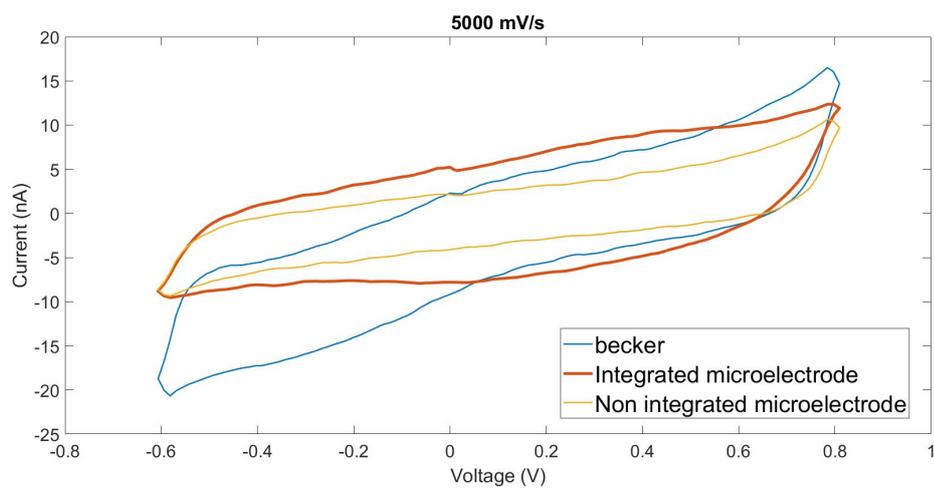


Figure 4.18: Cyclic voltammetry plot of integrated microelectrode @ S.R.=5000 mV/s

Chapter 5

Conclusions and future developments

Brain stimulation is an effective and proven solution used as state-of-the-art to mitigate impairing disease symptoms, such as Parkinson's disease, with excellent results. Moreover, brain stimulation has recently started to become the object of investigation to recover from impairments mostly related to deafness and blindness. Although there have been several advances in this field, limitations associated with mechanical and electrochemical stability of implants are still present after microelectrodes integration into their electronic drivers. Therefore, I first tried to investigate two categories of integration techniques, traditional integration of microwires and CMOS electrodes microfabrication.

With regard to the first group, manual integration has presented discrete results, considering the simplicity of the used tools, such as tweezers and glue. The FIB-aided cut of the microelectrode has been demonstrated to be effective and suitable for such applications. The bigger criticality is represented by the reduced hand precision for glue dispensing and on-site electrode placement. Therefore a more automatized integration technique is developed, where FIB is not only used for precise electrode cut, but it is also used to handle it and fix it on the dedicated pad taking advantage of the high-energy Pt deposition. The presented technique has great potential as well as promising expected results, but it was not possible to complete it because of the weakness of the microelectrode-micromanipulator welding that prevented the electrode from being able to be placed in the desired position and fixed.

Given the aforementioned limitations, I developed a novel CMOS-based technique to link the fabrication of the electrodes to the chip one in order to make the whole procedure cleanroom-compatible. The fabrication process flow has been validated, and the implementation of the miniaturized devices has been demonstrated to be

effective and feasible in a clean room environment, laying the foundation for further related works. Fabricated implants showed good mechanical strength and stability once handled.

Finally, the last step of my work is related to the assessment of the electrochemical stability of both traditionally integrated microelectrodes and microfabricated ones. Therefore, I developed a prototype of a novel miniaturized electrochemical cell setup, suitable for the reduced size of the implants. Tests have been carried out only on traditionally integrated electrodes, showing very promising results since electrochemical stability has been assessed before and after integration with cyclic voltammetry (CV) and demonstrated by identical CV plots in the two cases.

5.1 Future developments

The overall work is intended as a starting point for the investigation of both mechanical and electrochemical stability of integrated microelectrodes. Therefore, there is still plenty of space for improvement.

First of all, since the manual integration technique of microelectrodes is limited by the aforementioned aspects, the FIB-aided integration technique can be improved. In fact, it has been established that the use of a tweezer manipulator, instead of a tip one, may help to handle the microelectrode, avoiding the need to place it vertically by hand outside the chamber and to weld it to the manipulator itself.

When it comes to microfabrication, the whole fabrication can be furtherly improved and optimized in terms of process parameters. First of all, the developed probes deliver charge only with aluminum; therefore, iridium oxide has yet to be deposited so that an electrical properties comparison can be made. Moreover, the final required thickness of the chip should be reduced from $380\ \mu\text{m}$ to $75\ \mu\text{m}$. This last process should be performed as one of the last steps of microfabrication since it is almost impossible for cleanroom tools to handle $75\ \mu\text{m}$ thick wafers. Another improvement aspect is to enlarge the area of the CMOS chip in photolithography designs, since DRIE is not fully anisotropic, thus it does not create perfectly vertical silicon walls, during backside etching. Finally, shrewdness can be added to the design, regarding the variable length of the probes. In fact, varying the length of one probe may help to direct and focus both magnetic and electric field in the desired way.

As for electrochemical measurements, the developed miniaturized setup represents a prototype of a cell for microelectrodes characterization. Therefore, it can be optimized, for instance taking advantage of precise fabrication methods. Moreover, the analysis has been conducted only on the traditionally integrated microelectrodes and only through cyclic voltammetry. Future characterization of the CMOS microfabricated electrodes can be performed, both with bare aluminum

tip and with IrOx covered tip, to assess differences. Moreover, multiple electrochemical characterization techniques can be used for microelectrodes, such as EIS (Electrochemical Impedance Spectroscopy) to determine the overall impedance at different frequency values, and VT (Voltage Transient) to assess the electrical properties related to the stimulation.

Appendix A

Microfabrication Process Flow

Semestral Project Master Project Thesis Other

Project Name

Description of the fabrication project

Microelectrodes for neural stimulation must be fabricated. The general idea is to create flat Aluminum probes to be fixed on small square-based Silicon substrate two-by-two. Aluminum is insulated all over the probes body with SiO₂, except the tip which is covered in Iridium Oxide. Patterns of different materials are determined with photolithography steps. Structures must, then, be released and this is achieved by a backside etch procedure. Once the two probes structures are released, probes are bent, to be ready for insertion. Layout file for photolithography patterns is *mangionoTemplateMask.gds*. Layers are specified in the document.

Technologies used <i>!! remove non-used !!</i>			
Sputtering, positive resist, Dry etching, Wet etching, SEM, Photolithography			
Ebeam litho data - Photolitho masks - Laser direct write data			
Mask #	Critical Dimension	Critical Alignment	Remarks
1	1.0 μm	First mask	Metal deposition
2	1.0 μm	-	SiO ₂ deposition
3	1.0 μm	-	IrOx deposition
4	1.0 μm	-	Si etching
Substrate Type			
Silicon <100>, Ø100mm, 200 nm SiO ₂ , 380 μm thick, Double Side polished, Prime, p type, 01-05 Ohm.cm			

Interconnections and packaging of final device

Thinning/grinding/polishing of the samples is required at some stage of the process.

No Yes => confirm involved materials with CMi staff

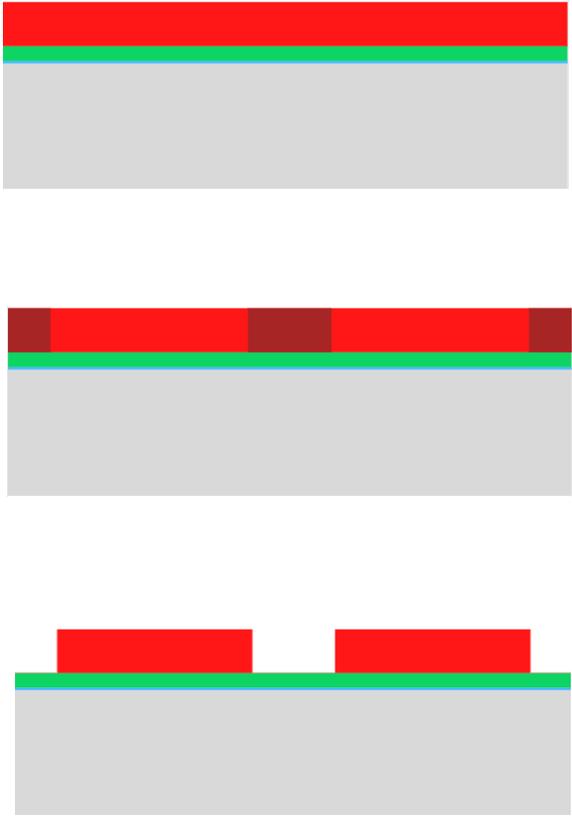
Dicing of the samples is required at some stage of the process.

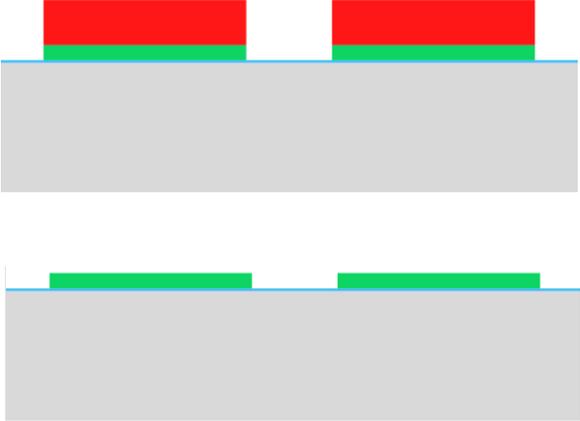
No Yes => confirm dicing layout with CMi staff

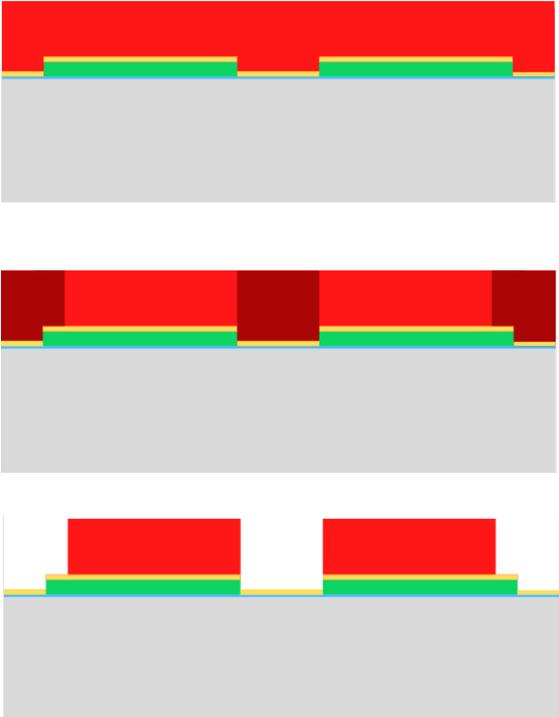
Wire-bonding of dies, with glob-top protection, is required at the end of the process.

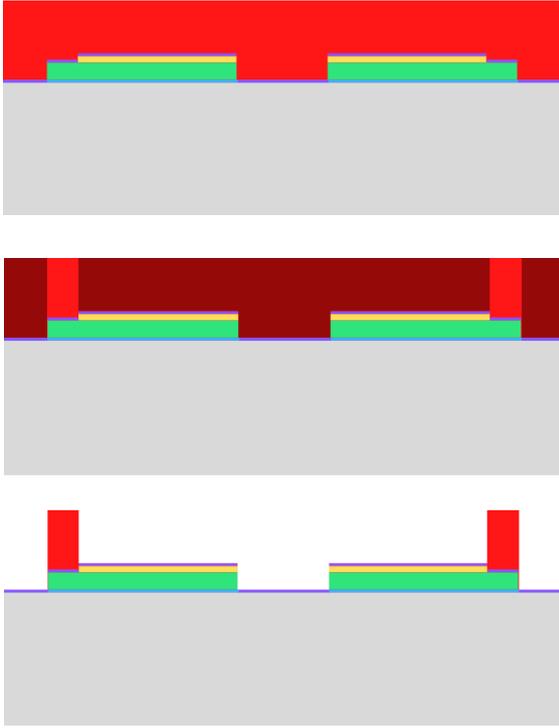
No Yes => confirm pads design (size, pitch) and involved materials with CMi staff

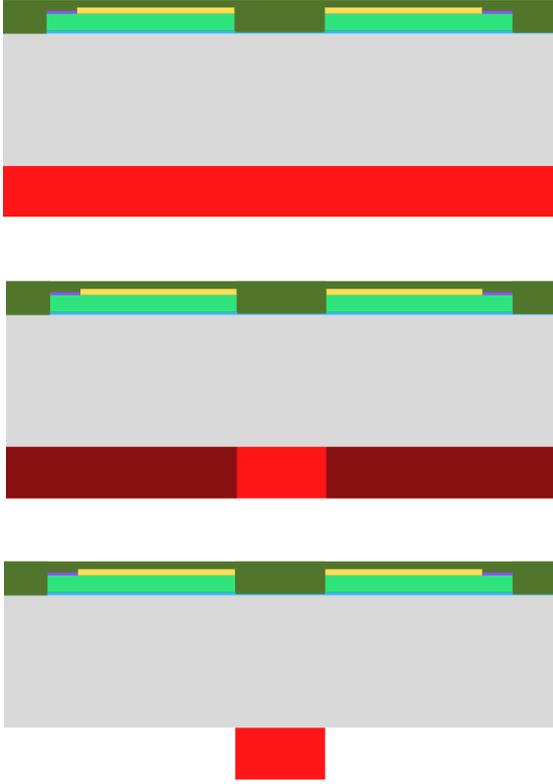
Step-by-step process outline

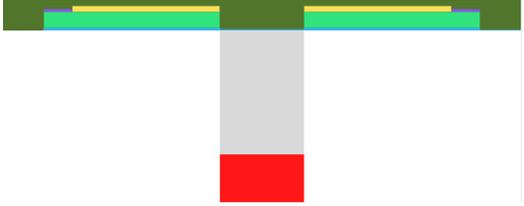
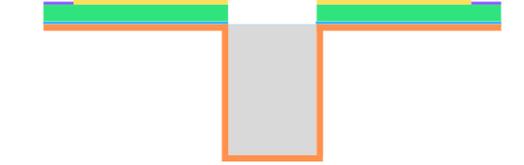
Step	Process description	Cross-section after process
01	<p>Substrate: Si wafer RCA + Wet Oxide (Service) Material: SiO₂ Thickness: 200 nm</p>	
02	<p>Metal deposition Material : Ti/Al Thickness : 10 nm / 4 μm Machine : Pfeiffer Spider 600 (Z02)</p>	
03	<p>Photolitho Mask-less aligner</p> <ul style="list-style-type: none"> <p>PR coating Resist : AZ10XT-60 (Positive) Thickness : 8 μm Machine : EVG150 (Z06)</p> <p>Design exposure Machine : MLA150 (Z16) Laser : 405 nm Dose : 400 mJ/cm² Defocus : +3 Mask : Layers 163/0, 58/0</p> <p>PR development Resist : AZ10XT-60 Thickness : 8 μm Manual : ‘AZ 400K developer’ solution (Z13)</p> 	

<p>04</p>	<ul style="list-style-type: none"> • Dry etching Material : Al Thickness : 4 μm Machine : STS Multiplex ICP (Z02) • PR strip Machine : TePla GiGAbatch (Z02) 	 <p>The diagrams for step 04 show two stages of a process. The top diagram shows a grey substrate with a thin blue layer, a green layer, and a red layer. Two red rectangular blocks are positioned on top of the green layer. The bottom diagram shows the same substrate after the red and green layers have been removed, leaving only the blue layer on the surface.</p>
<p>05</p>	<p><i>Insulator deposition</i></p> <ul style="list-style-type: none"> • Insulator deposition Material : SiO_2 Thickness : 1 μm Machine : Pfeiffer Spider 600 (Z04)/Oxford Plasmalab (IPHYS) 	 <p>The diagram for step 05 shows a grey substrate with a thin blue layer. A yellow layer is deposited on top of the blue layer. Two green rectangular blocks are positioned on top of the yellow layer.</p>

<p>06</p>	<p><i>Photolitho Mask-less aligner</i></p> <ul style="list-style-type: none"> PR coating Resist : AZ10XT-60 (Positive) Thickness : 8 μm Machine : EVG150 (Z06) Design exposure Machine : MLA150 (Z16) Laser : 405 nm Dose : 400 mJ/cm^2 Defocus : +3 Mask : Layer 165/0 PR development Resist : AZ10XT-60 Thickness : 8 μm Machine : EVG150 (Z06) 	
<p>07</p>	<ul style="list-style-type: none"> Dry etching Material : SiO_2 Thickness : 1 μm Machine : SPTS APS/STS Multiplex ICP (Z02) PR strip Machine : Tepla GiGAbatch + UFT remover (Z02) 	

<p>08</p>	<p><i>Oxide deposition</i> Material : IrOx Thickness : 200 nm Thickness : Evaporator DP650 (Z11)</p>	 <p>A cross-sectional diagram showing a grey substrate with two rectangular regions of IrOx deposition. Each region consists of a thin blue layer on top of a thicker green layer.</p>
<p>09</p>	<p><i>Photolitho Mask-less aligner</i></p> <ul style="list-style-type: none"> • PR coating Resist : AZ10XT-60 (Positive) Thickness : 8 μm Machine : EVG150 (Z06) • Design exposure Machine : MLA150 (Z16) Laser : 405 nm Dose : 400 mJ/cm² Defocus : +3 Mask : Layer 164/0 • PR development Resist : AZ10XT-60 Thickness : 8 μm Machine : EVG150 (Z06) 	 <p>Three cross-sectional diagrams illustrating the photolithography process. The top diagram shows a red photoresist layer coating the substrate. The middle diagram shows the photoresist after exposure and development, with red resist remaining on the substrate and over the patterned regions. The bottom diagram shows the photoresist after reflow, where the red resist has melted and formed a smooth, rounded top surface.</p>
<p>10</p>	<p><i>IrOx etching</i></p> <ul style="list-style-type: none"> • PR reflow Material : AZ10XT-60 Time : 2 min Temperature : 125° C Machine : Despatch LCD1 – 16NV – 3 (Z11) 	 <p>A cross-sectional diagram showing the IrOx etching step. The red photoresist from the previous step is now being used as an etch mask. The IrOx layer (green) is being etched away from the substrate (grey) in the areas not covered by the photoresist.</p>

	<ul style="list-style-type: none"> • Ion Beam etching Material : IrOx Thickness : 200 nm Machine : Veeco Nexus IBE350 (Z11) • PR strip Machine : Tepla GiGAbatch (Z02) + UFT removal (Z02) 	
<p>11</p>	<p><i>Parylene coating</i> Thickness : 5 μm Backside covered with UV tape to avoid deposition (CMi service)</p>	
<p>12</p>	<p><i>Photolitho Mask-Less Aligner on the back side</i></p> <p>a) PR coating Resist : AZ10XT-60 (Positive) Thickness : 8 μm Machine : EVG150 (Z06)</p> <p>b) Design exposure Machine : MLA150 (Z16) Mask : (3rd DXF) Laser : 405 nm Dose : 400 mJ/cm² Defocus : +3 Mask : Layer 167/0</p> <p>c) PR development Resist : AZ10XT-60 Thickness : 8 μm Machine : EVG150 (Z06)</p>	

<p>13</p>	<p><i>Resist stabilization</i> Machine : EUS (Z14) 85°C oven Over night</p>	
<p>15</p>	<p><i>Dry Etch – Back Side</i> Material : Si Machine : SPTS Rapier DSE (Z02) Depth : 380 µm</p>	
<p>16</p>	<p><i>Coating with SiO₂</i> Thickness : 2 µm (PR strip with Acetone and IPA) Mchine: Pfeiffer Spider 600 (Z04)/Oxford Plasmalab (IPHYS)</p>	
<p>17</p>	<p><i>Parylene – C strip</i> Machine : Tepla 300 (Z11)/Tepla GiGABatch (Z02)</p>	

Appendix B

Matlab code

The following code is related to cyclic voltammetry data processing, at different scan rates of the three configurations: becker, non integrated electrode and integrated electrode in a miniaturized electrochemical setup.

```
1 clear all
2 close all
3 clc
4
5 %Scan rate choice
6 sr = input("Choose the desired scan rate: 50, 200, 500, 1000, ...
7           5000 mV/s:\n");
8 sr_str = num2str(sr);
9 init_path = "C:\Users\Home\Desktop\EPFL\...
10           Electrodes_characterization\Matteo_CV\...
11           Comparison_among_setups";
12 final_path = strcat(init_path, '\', sr_str, 'mVs');
13
14 list = dir(final_path);
15 list(1:2) = [];
16 dim_list = size(list,1);
17
18 N = 5; %Number of scans
19
20 conf = convertCharsToStrings(input("Choose the plots that you ...
21 want to show:\n[a]ll for all the plots\n[n]ew for only the ...
22 new plots\n", "s"));
23 if strcmp(conf, 'n')
24     list(3) = [];
25     list(3) = [];
26 end
```

```

22 for i=1:size(list,1)
23
24     matr = double(readmatrix(final_path + '\' + list(i).name));
25     matr = [zeros(1,3);matr];
26
27     %Separation of the single scans
28     zeroes = find(~matr);
29     start(1) = 2;
30
31     m = 2;
32     for k=2:length(zeroes)
33         pos = zeroes(k);
34         if matr(pos-1)<0
35             stop(m-1) = pos;
36             start(m) = pos+1;
37             m = m+1;
38         end
39     end
40     start(end) = [];
41
42     fields = ["Applied_V";"WE_V";"WE_A"];
43     for j=1:N
44         data(i).(fields(1))(:,j) = matr(start(j):stop(j),1);
45         data(i).(fields(2))(:,j) = matr(start(j):stop(j),2);
46         data(i).(fields(3))(:,j) = matr(start(j):stop(j),3);
47     end
48
49     av_data(i).(fields(1)) = mean(data(i).(fields(1))');
50     av_data(i).(fields(2)) = mean(data(i).(fields(2))');
51     av_data(i).(fields(3)) = mean(data(i).(fields(3))');
52
53     data1 = [av_data(i).(fields(1)), av_data(i).(fields(1))(1)...
54 ];
55     data2 = [av_data(i).(fields(2)), av_data(i).(fields(2))(1)...
56 ];
57     data3 = [av_data(i).(fields(3)), av_data(i).(fields(3))(1)...
58 ];
59
60     av_data(i).(fields(1)) = data1;
61     av_data(i).(fields(2)) = data2;
62     av_data(i).(fields(3)) = data3;
63
64     av_data(i).(fields(3)) = smooth(av_data(i).(fields(3))*1e9)...
65 ;
66
67     %plot of the curves
68     if i~=2 | i~=3
69         if strcmp(list(i).name, 'becker.txt')

```

```

67         legend_name = 'becker';
68         field = 'becker';
69         plot(av_data(i).(fields(2)),av_data(i).(fields(3)),...
'LineWidth',1.5,'DisplayName',legend_name)
70         elseif strcmp(list(i).name,'ring_top.txt')
71             legend_name = 'ring - from top';
72             field = 'ring_top';
73             plot(av_data(i).(fields(2)),av_data(i).(fields(3)),...
'LineWidth',1.5,'DisplayName','Non integrated microelectrode...
')
74             elseif strcmp(list(i).name,'ring_int.txt')
75                 legend_name = 'new ring - integrated';
76                 field = 'ring_int';
77                 plot(av_data(i).(fields(2)),av_data(i).(fields(3)),...
'LineWidth',3,'DisplayName','Integrated microelectrode')
78                 elseif strcmp(list(i).name,'ring_int_old_dirty.txt')
79                     legend_name = 'old ring - integrated (dirty)';
80                     field = 'old_ring_int_dirty';
81                     plot(av_data(i).(fields(2)),av_data(i).(fields(3)),...
'LineWidth',1.5,'DisplayName',legend_name)
82                     elseif strcmp(list(i).name,'ring_int_old_clean.txt')
83                         legend_name = 'old ring - integrated (clean)';
84                         field = 'old_ring_int_clean';
85                         plot(av_data(i).(fields(2)),av_data(i).(fields(3)),...
'LineWidth',1.5,'DisplayName',legend_name)
86                 end
87             hold on
88             title(strcat(sr_str,' mV/s'))
89             xlabel(" Voltage (V) ")
90             ylabel(" Current (nA) ")
91             lgd = legend;
92             lgd.FontSize = 16;
93         end
94
95     % Calculation of some statistical values
96     % stdev(i).(fields(1)) = std(data(i).(fields(1))');
97     % stdev(i).(fields(2)) = std(data(i).(fields(2))');
98     % stdev(i).(fields(3)) = std(data(i).(fields(3))');
99     %
100    % mean_stdev(i).(fields(1)) = mean(stdev(i).(fields(1)));
101    % mean_stdev(i).(fields(2)) = mean(stdev(i).(fields(2)));
102    % mean_stdev(i).(fields(3)) = mean(stdev(i).(fields(3)));
103    % disp("Mean Standard Deviation:")
104    % disp("    Applied Voltage: " + mean_stdev(i).(fields(1)) +...
" V")
105    % disp("    Recorded Voltage: " + mean_stdev(i).(fields(2)) ...
+ " V")
106    % disp("    Recorded Current: " + mean_stdev(i).(fields(3))...
*1e9 + " nA")

```

```
107
108     %Lateral surface of the tip
109     r = 3.5e-4;
110     h = 25e-4;
111     lat_surf = pi*r*sqrt((r^2)+(h^2));
112     scanrate = sr;
113     scanrate = scanrate * 1e-3;
114     [CSC.(field), CSCc.(field), CSCa.(field), CSCtot.(field)] =...
115     CSC_function(av_data(i), scanrate, lat_surf);
115 end
```

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