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Phase-Change Memory and OTS Selector

a challenge for the future of computing

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Aknowledgemets

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Chapter 1

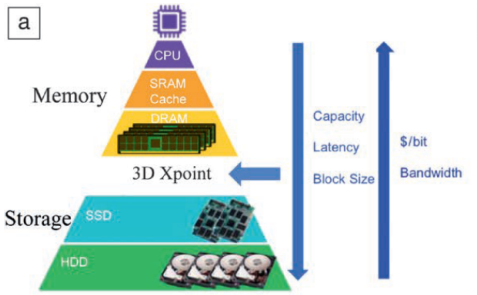
Introduction

Memory has a central role in computing and is a current subject of research and considerable investments; in the last few decades, new technologies and architectures have been proposed to overcome the significant limits of the currently available memories based on charge storage.

Intel already launched on the market the first generation of Phase Change Memory based on an innovative storage mechanism (figure 1.1a) that meets the requirements of the *Storage Class Memory* niche [1] (figure 1.1b); other companies like ST Microelectronics are already developing PCM memories for Automotive and Embedded Market [2].

Alongside PCM, new types of selectors willing to replace CMOS that exploit different physical principles are making their way into the scene offering new and innovative solutions [3]. Ovonic Threshold switching materials based on chalcogenide alloy analogs to the ones that make PCM exploit a highly nonlinear characteristic to block or let current flow depending on the applied bias. This type of device, similar in behavior to breakdown diodes, can be exploited as selectors for all the emerging memory technology with different requirements than either Flash or DRAM.

(a) Intel Optane 3DXpoint™Phase Change Memory technology is used to boost the performance of your computing system by allowing less and buffered data transfer from the Main Memory (HDD, SSD) and the DRAM: misses are reduced and access speed increases.



(b) Memory hierarchy in modern computer based on Harvard architecture: Each memory level transfers data from the underlying one in the pyramid. Closer to the CPU, access time is faster but the size is limited; Storage Class Memory offers larger densities and non-volatility, aiming to fill the gap between Main and Mass Memory.

Figure 1.1: Intel's memory solution proposed in 2015 [4], pictures from [3].

This work aims to introduce Phase-Change memory technology by depicting the state of art and describing its physics. Ovonic Threshold Switching selector is introduced, and its major physical models are described. With the theoretical and bibliography summary, experimental results obtained during a six-months work are reported and discussed.

1.1 Internship Overview

The internship was granted by CEA-Leti[1] in Grenoble; the company, offspring of the *Centre à l'énergie atomique* (CEA), is a technology research institute whose aim is to develop innovative and competitive solutions for information technology.
The work was performed under the DCOS[2] department in the LDMC[3] laboratory.

[1] https://www.leti-cea.com/cea-tech/leti/english
[2] Dispositif Composant Silicium
[3] Laboratoire des Dispositif Memoire Calcul

The internship comprises two complementary parts: a bibliographic study on the subject and electrical characterization and verification on real devices. It was possible in a first step to fully understand the topic, the opportunities, and the challenges offered by this technology that then were verified by testing and studying cutting-edge devices representative of their category.
In figure 1.2 a Gantt chart that summarizes the six months of the internship is reported; theoretical study and practical activity were performed concurrently to maximize the understanding. The last period focused on summarizing the results to produce this report and a final oral defense.

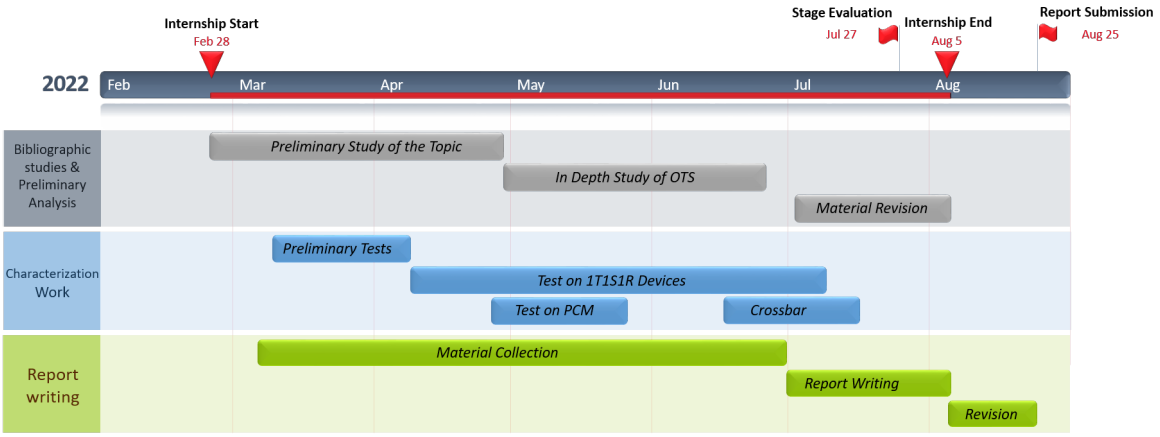


Figure 1.2: Gantt diagram of the internship period, split into three segments: Bibliographic studies, Characterization, and Report Writing.

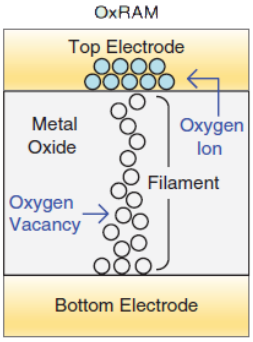
Chapter 2

Theoretical background

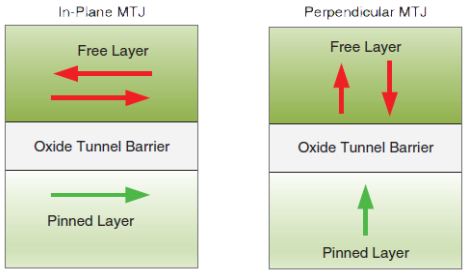
Memory is a crucial technology in microelectronics that, combined with CMOS digital logic, has made computation as we know it today possible.
Memory performance has been improving slower than CPUs; year after year, the lag in speed and power consumption makes it often the bottleneck for many applications [5]: the *Memory Wall* was already a matter of fact in 1994.
In the last couple of decades, new and emerging memory technologies emerged to overcome widespread MOS-based Flash memory limitations. Many new technologies offer benefits like endurance (Flash is limited to $10^5 - 10^6$ writing cycles), power consumption, fabrication complexity, or total/partial resilience to temperature and radiation-induced errors.

2.1 The Memory Problem

To enable computing for IoT, Cloud, In-Memory Computing, and many more applications, an increase in performance and reduction of power consumption are of utmost importance.
Emerging memory technologies and architectures show promising results in meeting the market's requirements. Notable ones are OxRAM (RRAM), MRAM, and PCRAM; those are based on the resistance to store



(a) RRAM based on Oxygen vacancies, when programmed a conductive filament is formed while once RESET the filament is destroyed and the resistance of the cell increases.



(b) STT-MRAM scheme for either In-Plane or Perpendicular MTJ; depending on their spin, electrons face different resistance through the junction.

Figure 2.1: Example of two emerging memory technologies from [6], each working mechanism may present some advantages over the others like the low programming currents of STT-MRAM or the scalability of the OxRAM.

information, low or high resistance state are used to represent binary data 2.1.

OxRAM is a memory in which each cell is made of an Oxygen-rich material that shows enhanced atomic migration under high voltage, the material usually is highly resistive. When a writing voltage is applied, Oxygen vacancies form inside the memory layer, thus creating a conductive path between the Top and Bottom Electrode 2.1a. Upon reaching a threshold voltage, the filament fully shorts the electrodes with low-to-none Resistivity. When a suitable reverse polarity pulse is applied, the Oxygen ions migrate back, filling the vacancies and breaking the conductive filament.

In magnetic memories like FeRAM and MRAM, the information is stored as a magnetization field inside ferroelectric layers. The final device may exploit different configurations or physical phenomena to program it (like Giant Magnetoresistance in STT-MRAM 2.1b); its resistance is read to detect the programmed state.

Phase-Change Memory is a resistive memory that aims to both stand-alone and embedded market, offering performances that are a trade-off between volatile Working Memory (DRAM) and Solid State Mass Memory (Flash). Products like Intel Optane were developed and produced [4], and others will be out on the market soon [2].
The advantages granted by this technology are numerous. To cite some:

- It is a Non-Volatile Memory (NVM);
- Has high endurance (more than $10^8/10^9$ writing cycles are easily achievable, and even more were demonstrated [7]);
- When used in Read-Mostly schemes, it saves a massive amount of energy since the reading step requires very low voltages, and the data is maintained even after shutdown;

And many more [8].

A key point in this work is the choice of a selector device required to address and access the memory cell when integrated into an array or matrix configuration.
Standard MOS-based transistors are no longer suitable for such memories mainly due to the low current density that they can provide, not compatible with the increasing memory density and scaling requirements.

Closely related to PCM, there are the *Ovonic Threshold Switching* (OTS) selectors.
OTS shows a highly non-linear characteristic that allows one to select the desired memory cell and consistently write or read it. Further discussion on the selector and final architecture will be carried out in the following.

2.2 Phase Change Memory (PCM)

Phase-Change Memories (PCM) are based on chalcogenide elements from the 16th group of the periodic table. Phase-Change alloys exhibit a significant bulk resistance (and refractive index) variation when rearranging from their stable crystalline phase to a disordered amorphous phase; one of the most studied and known chalcogenide materials is $Ge_2Se_2Te_5$ referred to as GST-225.
Chalcogenide materials have been used in rewritable optical discs (CD-RW, DVD-RW, DVD-RAM, Blu-ray Disk RE) and, more recently, in solid-state integrated memories [9]. The Working principle involves two main phases: an amorphous metastable (glassy) highly resistive phase and a stable low-resistance crystalline phase (figure 2.2).

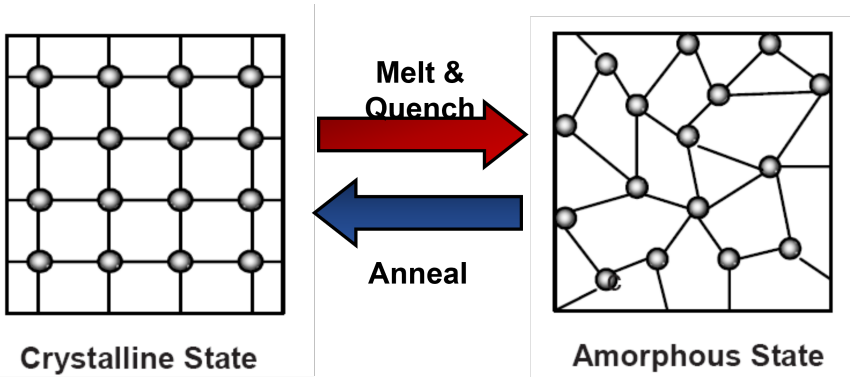


Figure 2.2: Pictorial representation of the stable ordered crystalline phase (on the left) and the metastable disordered amorphous phase (on the right). When the material is melted and quenched, it amorphizes; on the contrary, it will crystallize after an annealing step.

2.2.1 Working Principle

In its stable form, the material is ordered in a crystalline configuration that can be either cubic or trigonal, as in the case of GST-225. The crystalline phase presents a low resistance due to the periodic band gap that allows electrons in the conduction band to move freely. The behavior is ohmic with relatively low resistance. In optical media, a large refractive

is associated to the crystalline phase, in GST-225 $n > 7$ is measured for photons with energies between $1 - 1.5eV$ [9] (figure 2.3).

When the crystalline material is heated to its melting temperature and then quenched (i.e., steep cooling rate), the liquid phase does not have time to rearrange the crystalline structure by establishing all the stable bonds. The melt portion of the material will instead *freeze* in place in a disordered, defect-rich matrix. The amorphous (or glassy) phase is a disordered arrangement of atoms with entirely different properties than the crystalline one. In the case of optical media, the melt-quench operation could be performed by a strong focused laser that heats a region of the chalcogenide substrate and then switched off in a fraction of a ns. For electronic devices, since the layer resistance is low but nonzero, when a large current flows across it, the device heats up due to Joule heating. As the temperature increases, a region in the material will eventually melt. If the thermal capacity of the material's region of interest is sufficiently small and the switching time fast enough, it will allow for quenching of the melted portion. For example, figure 2.4 shows a bridge configuration, where a stripe of chalcogenide material connects two electrodes; its resistance is pictorially superimposed on the material.

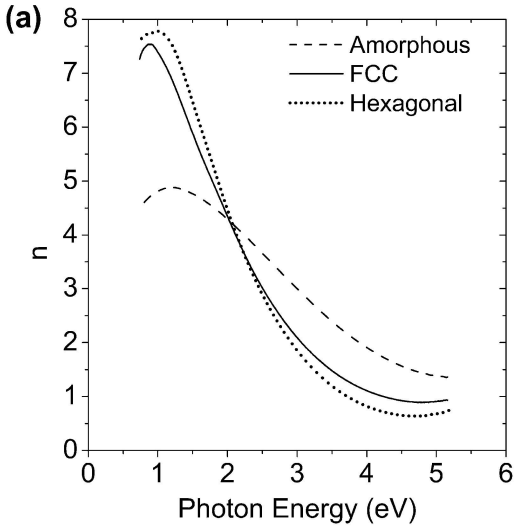
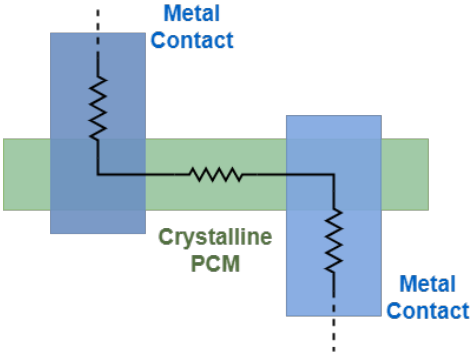
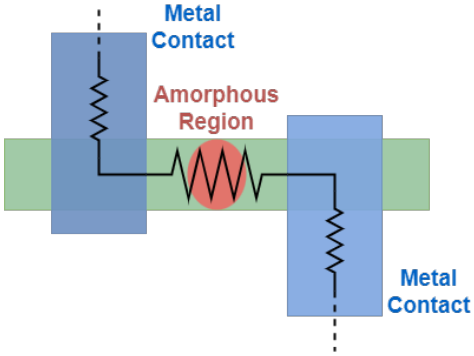


Figure 2.3: GST-225 refractive index variation as a function of the photon energy, the long dash line is the amorphous phase while the solid line is the stable crystalline FCC phase; the short dash line is the metastable hexagonal crystalline phase.



(a) PCM in the crystalline state has low resistivity (here pictorially shown as a small resistor).



(b) PCM in RESET stat presents an amorphized region that accounts for most of the device resistance (depicted as a big resistor).

Figure 2.4: Simplified scheme for a PCM for the SET (a) and RESET (b) state in a bridge cell, the different resistivity of each phase allows the reading of the programmed state.

The low refractive index and highly resistive amorphous phase does not have a liquid-like composition but, in fact, a defects-rich structure

that shows no Long Range Order (LRO), unlike the crystal lattice. In this configuration, Medium Range Order (MRO) and Low Range Order (LRO) are still present; they affect conduction in the chalcogenide layer. Stable bonds with lower energy are still favored over homopolar and dangling ones [10]. The number of defects may provide a piece of information on the *degree of amorphization*.

When the material is in the amorphous configuration, it can recrystallize by heating it to its crystallization temperature. At the crystallization temperature T_X, below the melting temperature T_m, atomic mobility is high enough to allow the redistribution of elements to form more stable bonds. Crystallization could be reached either through a solid-to-solid transition or by melting the material again but cooling it slowly so that the melted region spends enough time at temperatures close to T_X. This last process is preferred in microelectronics since it is easier to perform, for example, by the peripheral circuitry of a memory array; unless otherwise stated, this will be the crystallization technique implied. The writing or programming step is performed by biasing the cell; the heat produced by the current rise the temperature to the target value.

When dealing with memory, it is said to be SET when it is in the crystalline low-resistance state (LRS); on the contrary, it is RESET when it features a high resistance state (amorphous). To avoid unwanted changes to the programmed state the reading operation is performed at a low reading voltage V_{read}. SET and RESET states may be associated respectively to '1' and '0', although this choice is arbitrary.

2.2.2 Device Architecture

To program a cell, that is, to melt a portion of it, one has to reach a high temperature. The heating step thus requires a significant current; hence care must be taken in the optimization of the topology of the cell to maximize the heat transfer to the chalcogenide layer. One can lower the

current required to achieve crystallization/amorphization with careful design [11]. The most used and known architecture is the Wall-Heater (figure 2.5); this configuration consists of a PCM layer sandwiched between a metal electrode (Top contact) and a narrow metal heater (Bottom contact).

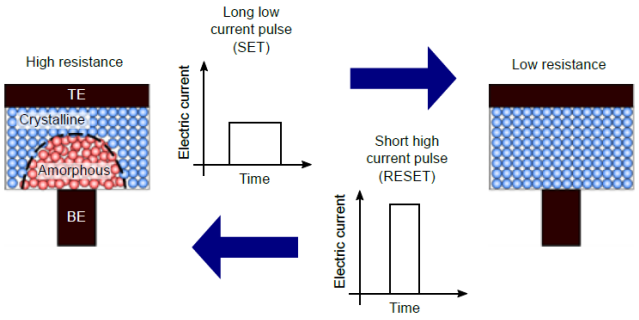


Figure 2.5: SET and RESET pulse of a PCM vary in amplitude and duration to reach either crystallization or melt-quenching. High-intensity pulse melts a portion of the material while a long but lower pulse may achieve crystallization of the layer. From [12]

The high current density reached in the small heater area produces a temperature increase with the hot spot between the chalcogenide layer and the heater. With this configuration, a circular sector around the heater interface can amorphize for a short pulse or crystallize if the pulse decay is longer; the shape of the amorphous region gives this architecture the name *mushroom cell*.

Many other architectures are possible, each one with its advantages and drawbacks. The Bridge structure, already shown in figure 2.4 and reported again in figure 2.6, consists of a simple line of chalcogenide material that connects two electrodes. In this configuration, there is no heater, and the hot spot is located in the bridge's middle point, where the pitch is usually narrower. While this is probably the simplest solution to fabricate, it is not suitable for dense arrays due to the minimum width required to make the cell reliable.

The Pore structure (fig. 2.7) is another heaterless solution where patterning in the substrate allows the opening of tiny pores filled by the

chalcogenide layer; current crowding in the small pore surface achieves the desired heating. This solution has a small footprint and reduces the requirements for chalcogenide deposition since the patterning is performed on the dielectric.

In the μTrench architecture, an opening in the substrate is performed in one direction to deposit the heater; in the other, the dielectric is etched to deposit the chalcogenide material. The heater deposition thickness determines the interface's cross-section, which can be extremely narrow (fig. 2.8); this architecture may be self-aligned, thus loosening even more the requirements for precision.

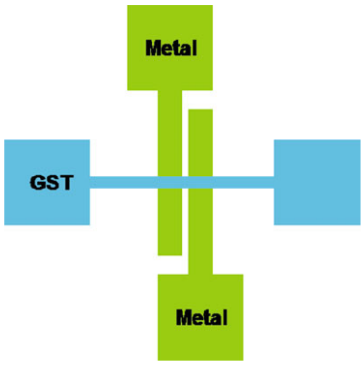


Figure 2.6: Bridge structure is made by a layer of chalcogenide material deposited on top of two parallel metal electrodes. Since the structure is symmetric the hot spot is located close to the center of the bridge [11].

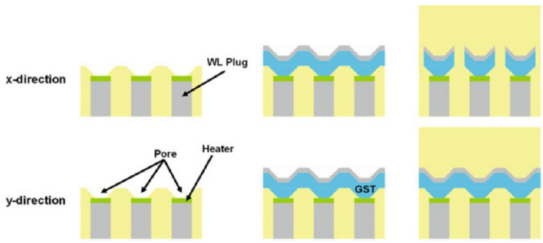


Figure 2.7: Pore Structure: due to the narrow pore filled with chalcogenide material, the high current density will heat the region in a similar fashion to the Wall-Heater structure [11].

2.3 Ovonic Threshold Switching

The *Ovonic Threshold Switching* (OTS) is the enabling phenomenon of PCM memories: once amorphized, the device is in a high resistance state, and to reach the current needed to heat it up to crystallization (or melting) temperature would require a too high voltage [14], not compatible with the power supply used in embedded systems (that is

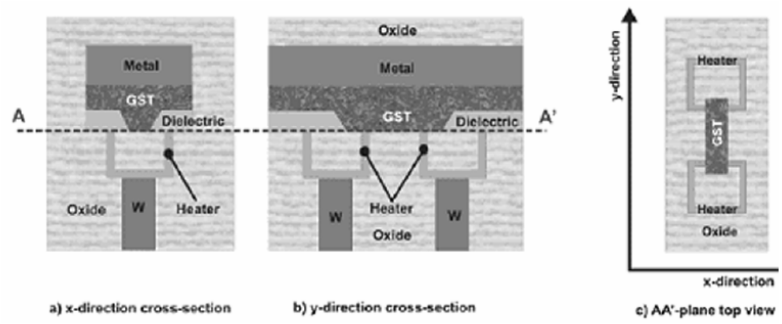


Figure 2.8: $\mu Trench$ Cell shares a similar working principle to the Wall-Heater structure but uses a thin trench filled with metal to form the heater and allows for multiple close cells integration [13].

$3.3V$ or at most $5V$). When a voltage ramp is applied to the amorphous chalcogenide, the device becomes highly conductive with a sudden reduction of the voltage drop across it (fig. 2.9). The voltage at which the device shows this reduction in resistance is called Threshold Voltage V_{th} and depends on the material composition, the layer's thickness, and other device parameters. The highly nonlinear characteristic of the device, with the presence of a Negative Differential Resistance (NDR) snap-back at the switching voltage, requires a positive feedback mechanism.

By increasing the voltage, the current in the device increases, leading to recrystallization of the memory layer producing a phase change (blue curve in figure 2.9). The amorphous cell is defined as *OFF* when read below its threshold; above V_{th}, it is called *ON*. Due to the high current that flows in the device above the threshold, it will move from the RESET to the SET state if no current control is present. Reading is usually performed at low voltages such that it is possible to appreciate the resistance of the PCM before switching: the distance between the crystalline and amorphous characteristics determines the reading window.

Since the original work from Ovshinsky in 1968 [15], OTS materials have been developed to cycle between ON and OFF states without crystallizing: Material Engineering allows the fabrication of devices that show a good

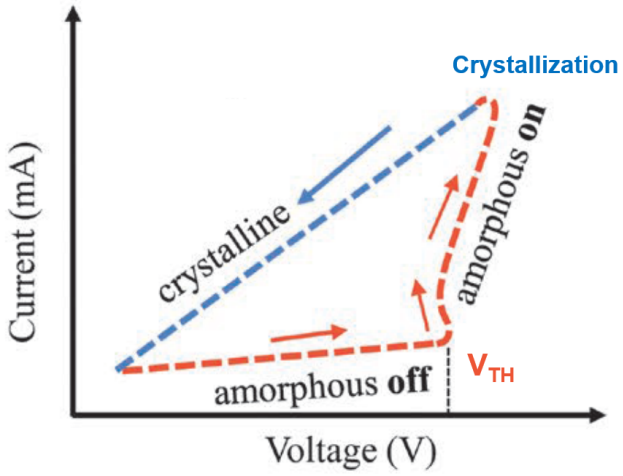


Figure 2.9: OTS switching characteristic [9]. When the amorphous layer switches (red curve), a high current passes, if this current is properly controlled then is possible to exploit Joule heating to crystallize the cell (blue curve).

and reliable OTS phenomenon. OTS materials are used only for switching devices and not for their Phase-Change properties. Due to the nonlinear, switching nature of the device, it is employed as an access device or selector.

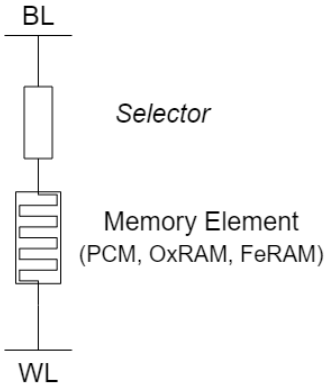
2.3.1 OTS as Selector Device

Using the OTS as a selector device is a relatively simple concept. Every memory element in an array or matrix configuration requires individual addressing to be read/written while deselecting unwanted devices, avoiding altering the reading result due to current sneak paths in neighboring cells.

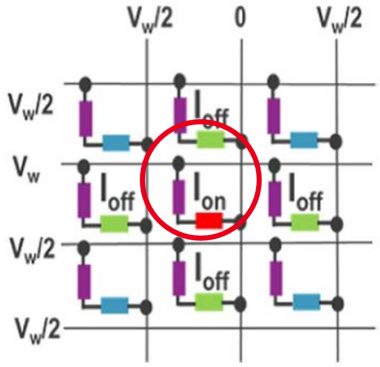
The selector[1] is placed in series with the memory element (figure 2.10a) that could be either a PCM or any RRAM. The OTS starts conducting when the voltage across the Bit Line and the Word Line exceeds its threshold: the peripheral circuitry reads or programs the underlying memory. In an array, each cell consists of a memory element and its corresponding ots selector

[1] equivalently *access device*

(figure 2.10b).



(a) Circuit scheme of a selector and memory stack, bias is applied across Bit-Line (BL) and Word-Line (WL)



(b) Array configuration with a possible voltage scheme, the selected device is correctly biased between V_w and ground (in red) where a current I_{ON} flows.
In the picture, a $V_w/2$ bias scheme is shown.

Figure 2.10: OTS Selector combined with a generic memory element.

OTS Selector has already been explored as a viable alternative to the well-established MOS selector; a qualitative comparison is reported in figure 2.11. Its primary advantage is the high ON current density J_{ON} it can withstand, in the order of a few tens of MA/cm^2; such high current density is required to RESET a PCM or to form a filament in an OxRAM.

3D integration of such a selector is more accessible due to the need for only two contacts; fabrication is straightforward, resulting in a minimal footprint of $4F^2$. In addition, chalcogenide materials, in general, are deposited in Back-End-of-Line (BEOL), making this technology independent from the front end, portable, and stackable.

Another critical parameter when dealing with arrays or matrices is the OFF leakage current I_{OFF} that determines the maximum array size achievable and must be kept under control. OTS have large OFF resistance, in the order of $1 - 10M\Omega$ for a typical $300nm$ device.

The OTS characteristic is slightly different from the PCM one shown in

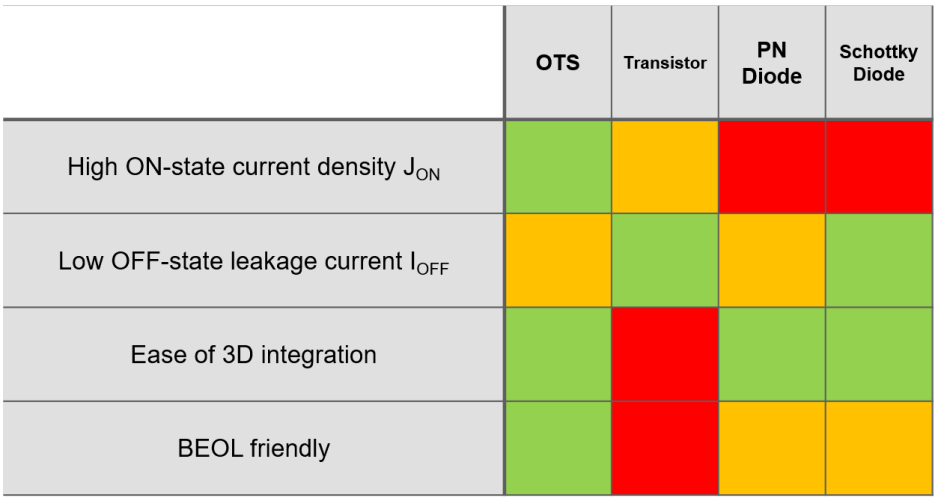


Figure 2.11: Qualitative comparison between OTS and other major well-established selector technologies. Green indicates Good performance, Yellow average, and Red bad performance. Data adapted from [16].

figure 2.9; the selector does not exper The OTS characteristic resembles the one of the PCM with the critical difference that it does not feature crystallization phenomena: it means that the OFF/ON transition is volatile (figure 2.12).

Following the red curve in figure 2.12 at low voltages, the device is in the OFF state, and the current I_{OFF} is very low. Upon reaching the threshold voltage V_{TH}, the device starts conducting with a sudden drop in voltage and increased current (snap-back). The device is now conductive, and a large current may flow without crystallization. When the bias is reduced (yellow curve in fig. 2.12), the device remains ON down to the holding voltage V_{hold} when it switches back to its OFF state, recovering its high resistivity. The electrical parameters that characterize the OTS are strongly dependent on the chosen OTS material (i.e. V_{th}, V_{hold}, I_{OFF}).

2.3.2 Physical Model

The first models to explain the switching phenomenon were based on a temperature-activated carrier injection, but such models disagree with experimental results and measured switching time. Electronic models

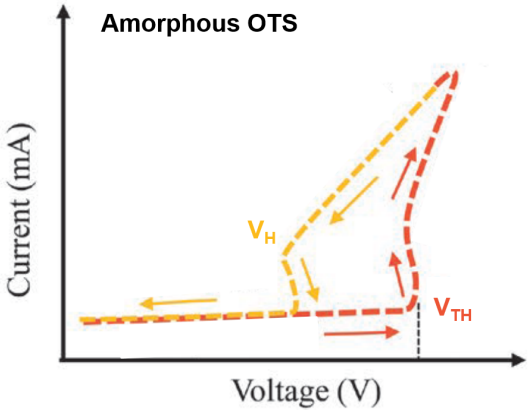


Figure 2.12: General switching characteristic of an OTS material, at V_{TH} it starts conducting with a voltage snap-back; the device remains in the ON state until the voltage is lowered below V_{hold}.

had more success in predicting the OTS behavior; the first model that showed good agreement with the experimental results was proposed by Adler [17]. The model was later revised by Ielmini et al. [14], and Jacoboni et al. [18] that achieved a better agreement with experimental results. While the phenomenon of Ovonic Threshold Switching has been known since 1968 [15], the predominant physical mechanism is still debated. Nowadays, there is an agreement toward a combination of electronic and structural phenomena, as filamentary conduction proposed by Karpov et al. [19], later revised by Nardone et al. [20], up to the latest structural model (from Guo et al.) that tries to describe conduction and switching altogether [21].

Subthreshold Conduction A modified Poole-Frenkel mechanism explains conduction in the amorphous chalcogenide (figure 2.13). The amorphous chalcogenide material is characterized by defects, voids, and dangling bonds. These features are schematized as potential wells in which the bound electron has energy E_T corresponding to the trap energy level. An electron must acquire sufficient energy to overcome the potential barrier and jump to a neighboring trapped state; it may happen either due to Thermal Emission (TE), where the thermal energy of the electron is exactly the height of the barrier $E_C - E_T$, or by tunneling

through the barrier. When a bias is applied, the electric field induces a barrier lowering that reduces the energy needed by the electron to be accelerated [14], [18], [22].

TE transport is described by the Poole-Frenkel model for conduction that predicts a current [14]:

$$I = I_{PF} e^{\beta_{PF} V_A^{1/2}} \tag{2.1}$$

Where V_A is the applied bias, I_{PF} and β_{PF} are constant parameters of the model.

Experimental results show different behavior when the average distance between close traps δz reduces. The slope of the barrier lowering energy appears proportional to the electric field rather than the square root of it, so that equation 2.1 is modified:

$$I = I'_{PF} e^{\beta'_{PF} V_A} \tag{2.2}$$

Where now V_A has unitary exponent; I'_{PF} and β'_{PF} are constants.

The full expression for the current in the subthreshold regime, from [14], is:

$$I = 2qAN_{T,tot} \frac{\Delta z}{\tau_0} e^{-\frac{E_C - E_F}{kT}} \sinh \frac{qV_A}{kT} \frac{\Delta z}{2u_a} \tag{2.3}$$

Here the current depends clearly on the area of the contact A and on the Maxwell-Boltzmann approximation of the Fermi distribution of populated state (the exponential term) times the trap distribution in the energy gap above the Fermi Energy, N_T, tot.
$\frac{\Delta z}{\tau_0}$ is the electron velocity, that is the distance between two neighboring traps Δz divided by the characteristic attempt-to-escape time τ_0 that the electron spends in average in a single trap before being able to tunnel.
The hyperbolic sine provides the field-induced transport term that depends on the inter-trap distance Δz and on the amorphous layer thickness u_a.

The hyperbolic sine is approximated by its argument when the latter is small and by an exponential function when it is large. Referring to figure 2.14, the shapes represent measurements while the solid lines are the calculated $I - V$ curves. For low voltages, the current is directly proportional to V_A while increasing the bias, the relation becomes exponential (mind the log scale of the figure).

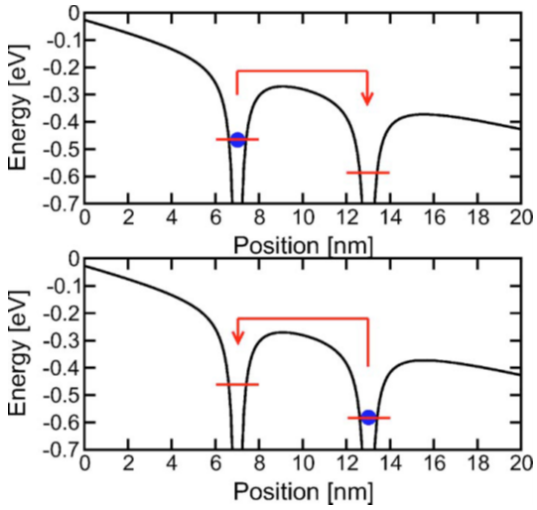


Figure 2.13: Poole-Frenkel model for conduction, the electrons are trapped in potential wells due to the defective nature of the amorphous phase. Electrons may tunnel and move from one trapped state to the other due to thermal emission, when an Electric field is applied, current in one direction is favored [14].

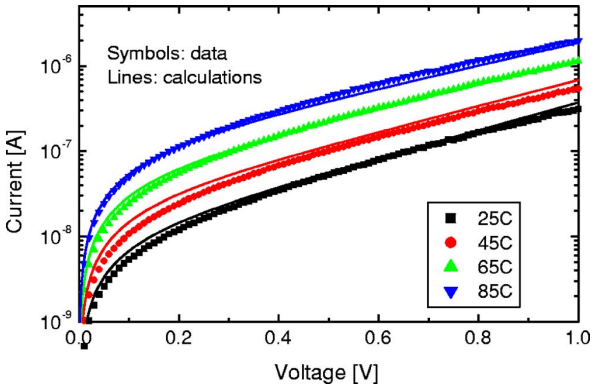


Figure 2.14: Measured and calculated I-V curve for increasing temperature; is possible to appreciate the linear regime for voltages lower than $0.2V$ followed by the exponential regime up to $1V$. Adapted from [14].

Threshold Switching While the agreement on the subthreshold conduction mechanism is shared, The switching process is still under investigation. The electronic model considers a non-equilibrium carrier distribution due to the applied electric field.

Electrons accelerated by the field may reach higher energy traps due to TE or tunneling 2.15. Injection requires a finite distance from the electrode to take place; for example, ballistic tunneling happens at a

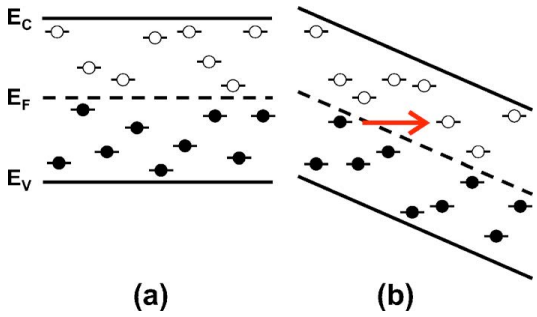


Figure 2.15: Low-field (a) and High-field (b) electrons energy distribution scheme. With Low or No field applied all the electrons fill trap states below the fermi energy; when the applied field increases, TE and tunneling are favored and electrons fill higher energy traps [14].

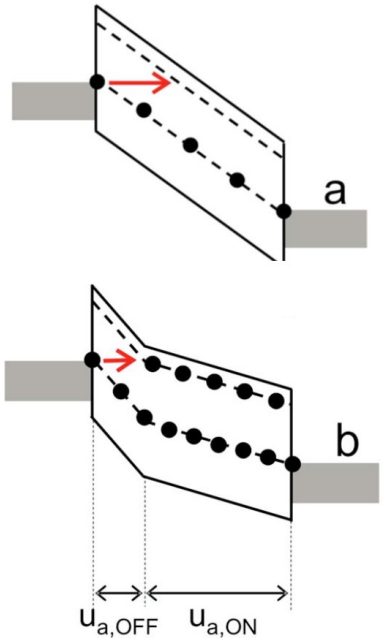


Figure 2.16: Close to the threshold voltage, the electric field is high but the current in the device is still low (a). Upon switching, electrons are accelerated and after a distance $u_{a,OFF}$, they reach the conduction band. The mobility in the conduction band is much greater and the voltage drop on $u_{a,ON}$ is much lower [14].

distance $\frac{\Delta E}{qF}$ where ΔE is the energy difference between the starting and destination trap energy, and F is the electric field. After a minimum distance $u_{a,OFF}$, the electrons will eventually reach the conduction band. Once electrons have energy in the conduction band, they move freely with much higher mobility; therefore, the voltage drop in the region $u_{a,ON}$ where they are excited is lower (figure 2.16), the conductivity of the sample is orders of magnitude higher. The voltage snap-back is justified since most of the voltage drop happens in the OFF region and the overall drop across the device is lower than the starting one. The analytical result associated with this model provides a good fitting close to the switching point while still not matching the experimental characteristic at V_{TH}

(figure 2.17).

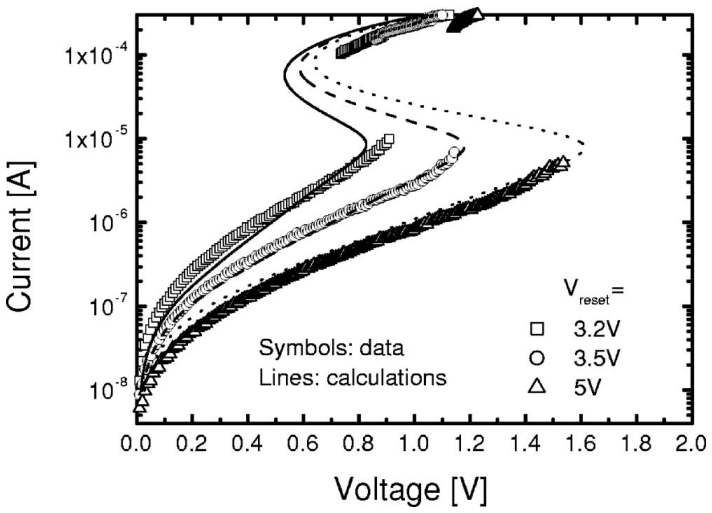


Figure 2.17: Experimental (shapes) and calculated (lines) data for three different PCM programming pulses (V_{reset}), each one corresponding to an increased volume of the amorphous phase. The sub and above threshold have good agreement while in the threshold region the model does not fit the experimental data [14].

More recently, a model from Nardone et al. [20] unifies a previous model [19], describing the switching phenomenon as field-induced nucleation. In the case of a conductive nucleus present in the material, the system's free energy is reduced due to the electrostatic energy close to the conducting particle, which depends on the volume Ω of the particle and a depolarizing distortion factor n. When a conductive path or *filament* starts to form (figure 2.18), the field-induced nucleation term becomes more significant because of the reduction in free energy. It eventually reaches a length such that the overall free energy of the system is negative, and the conductive filament fully shorts the two electrodes. Upon filament formation, the electric field may be lowered to the holding value E_{hold} before the system's energy leads to filament destruction and the device turns back OFF.

Latest models tend to unify structural and electronic phenomena [21]; purely electronic models fail to represent materials like $GeSe$. Another work from Chai et al. [23] demonstrated filamentary switching in

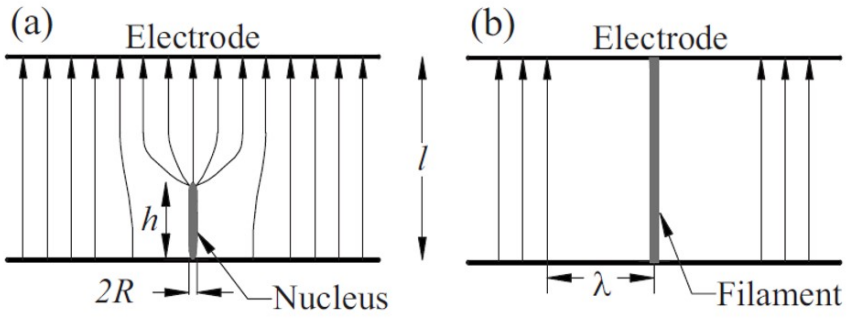


Figure 2.18: Field Screening effect that happens for (a) a conductive nucleus (supposedly cylindrical) of height h and radius R. The electric field concentrates at the tip and is weakened around it; the filament grows until it shorts the electrodes (b).

chalcogenide materials, implying that the switching process involves some structural relaxation phenomena. Molecular dynamics simulations on $GeSe$ showed that upon switching, the density of homo-elemental $Ge - Ge$ bonds increases 2.19, distorting the delocalized conduction states close to the conduction band edge 2.20. The distorted local coordination of the material thus accounts for the higher conductivity in the ON state; once the bias is removed, the material is subject to relaxation due to energy minimization.

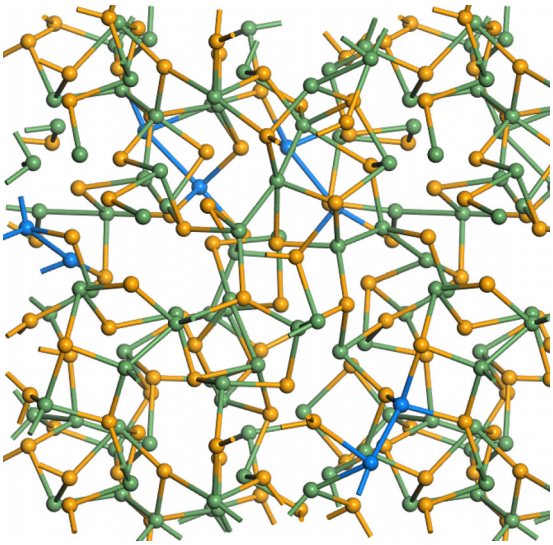


Figure 2.19: Simulation of 72 atoms random network. In blue are highlighted the new Ge-Ge bonds formed with switching [21].

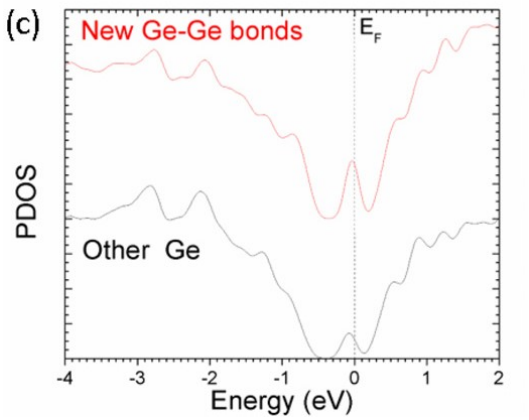


Figure 2.20: Partial Density of States of the newly formed Ge-Ge bonds close to E_F, compared to neighboring Ge sites in the excited state [21].

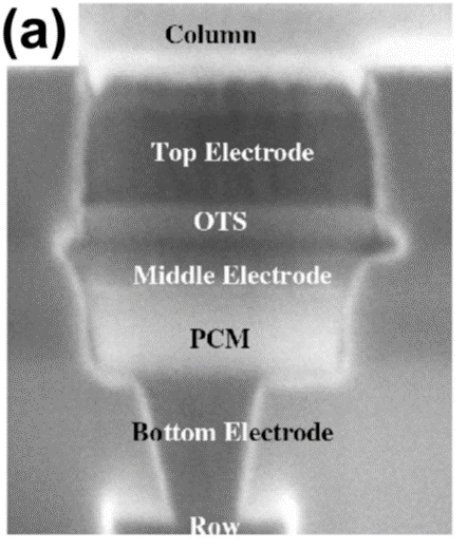
2.4 Crossbar Array

Since OTS selectors enable integration with a minimal footprint, they are well suited to be stacked with PCM cells organized in an array or matrix configuration. Even if the idea was already proposed in the past [24], it did not have the desired success due to fabrication limits until recently, when it appeared a practical choice for increasing the memory array density.

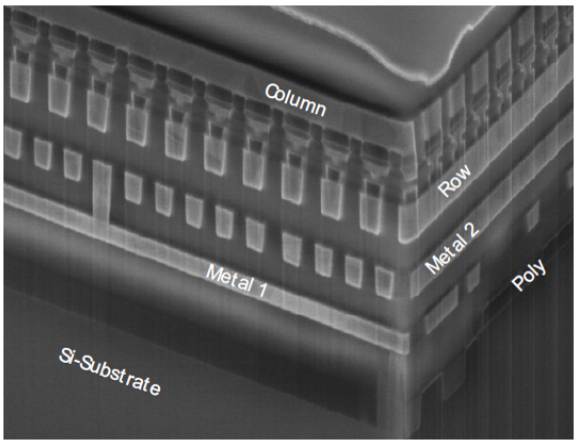
In figure 2.21a is reported the stack of OTS and PCM proposed by Intel in 2009, It has been arranged in what is called a Crossbar configuration (figure 2.21b). The Crossbar[2] structure consists of an array of Word Line (WL) metallic buses perpendicular to a series of Bit Line (BL) that are joined together at each intersection by a selector and memory element (figure 2.22).

The Crossbar architecture is stackable since, on top of a WL, another BL can be fabricated to achieve high-size arrays, limited only by the leakage

[2]Intel refers to it as 3DXPoint™or Crosspoint architecture [4].



(a) Memory device from [24], the heater corresponds to the Bottom Electrode.



(b) An overview of the complete device that shows a layer of the array.

Figure 2.21: SEM pictures of the memory devices by Kau et al. [24].

current of the selectors that determines the maximum number of devices in the chip to be correctly read. This architecture achieves the minimum footprint with a $2F$ lateral size [3] and makes the integration process more straightforward, thus offering a dense and portable Non-Volatile-Memory design.

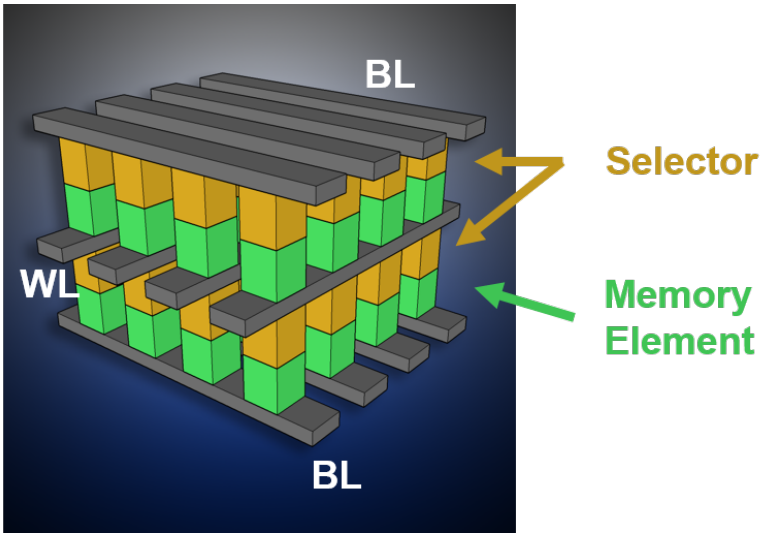


Figure 2.22: Crossbar architecture scheme, here reported for two layers. WL is in the middle perpendicular to the BL above and below, selectors are depicted in mustard while the memory element is in green.

Chapter 3

Electrical Characterization

During the frame of the Internship, the devices tested were the following:

- single device PCM cell
- single device PCM memory with OTS selector in series
- Array of 1T1S1R devices

The tested devices were given a series transistor to select and isolate a single cell during test operations. While it provides no advantages in a finite device, it is of utmost importance during the first characterization.

The electrical tests were primarily performed on a Cascade Summit 12000 bench operated by a Keysight B1500 parametric analyzer; the loading/unloading of the wafer is manual.
The bench can handle $200mm$ and $300mm$ wafers; it is equipped with a custom probe card that grants contact with the pads of each die. The instrument can perform electrical tests by applying voltage pulses of the desired duration and measuring the current with different calibers. The accuracy of the measuring equipment was not relevant for the first qualitative description of the device.

The device under test (DUT hereafter) was put in contact with the probes: the chip exposed contacts are the word line and bit line, as well

as the source line of each transistor and the bulk that are often connected and grounded.
To test a single device a suitable gate bias for the selector transistor is applied on the Word Line, and the reading or programming voltage on the Bit Line, depending on the desired operation.
In the case of crossbar and matrix arrays, the addressing was performed by the periphery circuitry controlled by a scripted protocol.

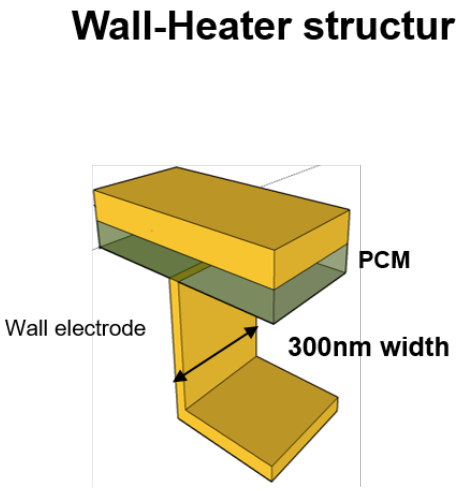
3.1 Single device PCM (1R)

The ***1R*** device has only the resistive memory element and the series transistor. Limiting the current in the PCM is crucial to avoid permanent damage if the current is too high for a long time.
The tested architecture is a Wall-Heater as described in section 2.2.2; the DUT structure is reported in figure 3.1a. The metal heater is patterned through a hole in the dielectric to achieve the desired width with a thin thickness. After polishing, the Calchogenide layer is deposited, followed by the top electrode; a circuit schematic of the stack is shown in figure 3.1b.

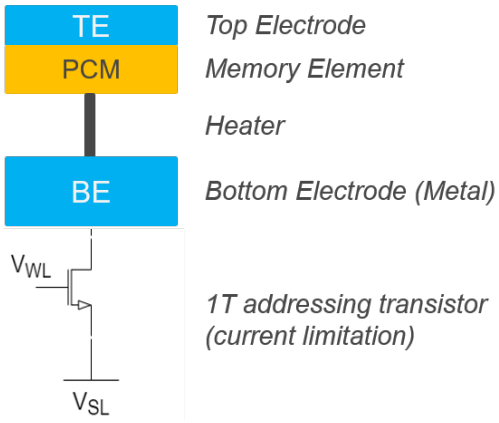
The DUT has a feature size (wall width) of $300nm$ and, while relatively large compared to the current state of the art, it provides excellent insight into the behavior and characteristic of a PCM memory element. Other sizes were available to test, and some results are discussed in the following. The material of choice is the well-established $Ge_2Sb_2Te_5$ or GST-225; the chalcogenide layer thickness is $50nm$.

3.1.1 Programming the cell

Two programming schemes were employed to RESET (amorphize) and SET (crystallize) the device. The principle is the same, the device is heated to its melting temperature and then is quenched to RESET or slowly cooled to SET the cell. As hinted in section 3.1, the solid-to-solid transition is not



(a) 3D model of the tested PCM, the wall electrode shaped like an "L" is placed at the bottom of the memory layer.



(b) Pictorial Circuit representation of device (a), the series current limiting transistor is shown with its circuital symbol.

Figure 3.1: PCM device architecture (a) and pictorial circuit scheme (b).

practical to quickly SET the cell; a solid-liquid-solid step is preferred to loose the current and temperature control requirements.

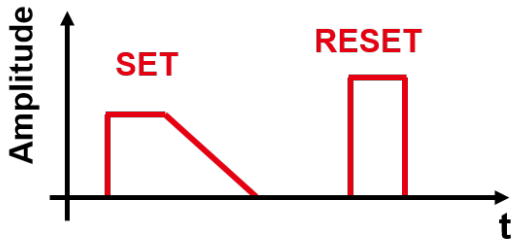


Figure 3.2: SET and RESET pulse scheme, here *Amplitude* is the current during the pulse, the SET pulse has a long fall time while the RESET pulse has a short fall time to ensure the amorphization of the melted region.

For the RESET operation, the transistor was biased to allow around $I_D \approx 2mA$ to ensure the correct amorphization of the PCM device; the corresponding gate voltage is $V_{WL} = 3V$ [1].
The pulse used has a square shape (i.e. short rise and fall times in the

[1]The transistor used with this devices has a width of $5900nm$ and a channel length of $500nm$

order of $20ns$) with duration (pulse width) of $300ns$ (figure 3.2). It is important to note that the pulse shape and timing will hugely impact the programmed state; for simplicity, only pulse amplitude has been analyzed.

To SET the cell the approach was to bring it to melt as for the RESET pulse, but having a long fall time of the pulse to achieve recrystallization of the amorphized area (i.e. slow quenching of the PCM material). The current needed during the SET operation is much lower, so it was programmed by limiting the current at around $I_D \approx 700\mu A$ corresponding to a gate voltage of $V_{WL} = 1.5V$. In this case, the pulse has a width of $300ns$ and a fall time of $5\mu s$; in both cases, the voltage applied on the BL was the same and equal to $V_{BL} = 5V$. The programming scheme is reported in figure 3.2.

The cell in the SET state has low resistance and behaves like a resistor while in the RESET state it shows high resistance up to the threshold.
Depending on the programming scheme and conditions, we can move from the SET to the RESET state and achieve a different degree of amorphization of the cell: the threshold voltage amplitude depends on the portion of amorphous material in the device. By increasing the current that flows during the programming pulse, it is possible to amorphize a bigger volume, thus obtaining a gradual increase of the resistance up to the point where the amorphous region reaches the top electrodes and the threshold voltage tends to saturate to its maximum value.

The mentioned characteristic is reported in figure 3.3, with the resistance as a function of the programming current. The blue curve starts from the high resistance RESET state: when there is almost no flow of current the reset state is unperturbed.
By increasing the current of the pulse slightly, partial recrystallization occurs (blue valley in the plot), associated with a drop of resistance. The two curves will eventually overlap (within experimental precision) when the pulse current is high enough to produce amorphization of the layer.
The saturated resistance seems to decrease for currents larger than

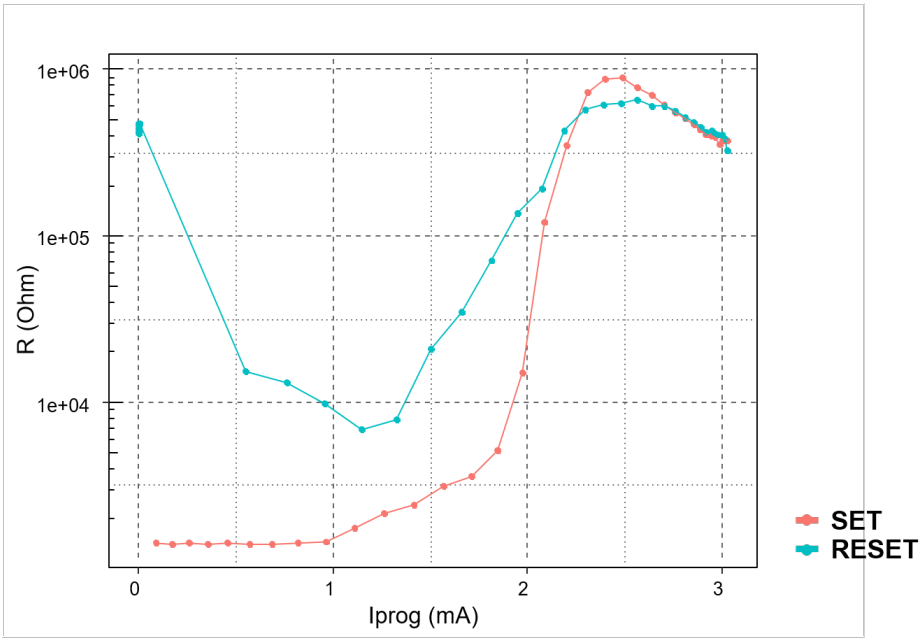


Figure 3.3: Resistance of the PCM after an applied programming pulse of intensity I_{prog}.
If the PCM starts from a SET state (red curve) it has low resistance until the pulse is sufficient to start amorphizing the chalcogenide layer. If the PCM starts in the amorphous phase then it will be unaffected for very low currents but for intermediate values, it features partial recrystallization before overlapping to the SET curve.

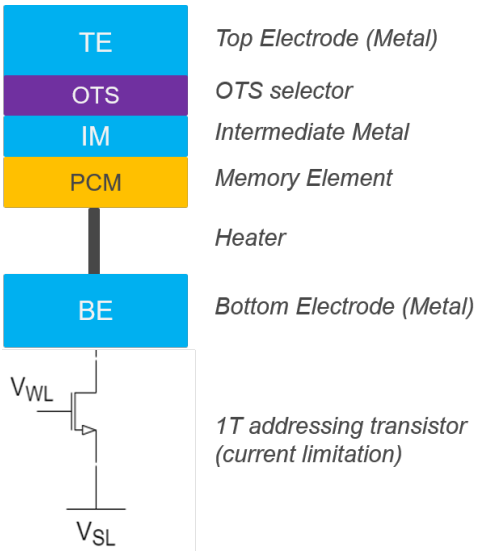
$2.5mA$. This behavior may seem contradictory to the idea of a larger amorphous region; the idea is that there is an optimum value of current to perform the RESET operation. When the current exceeds this optimum, the hot spot in the metal heater will move towards the bottom electrode; the amorphization is affected since the temperature gradient origin is no longer located at the interface with the chalcogenide layer. Overall the pulse is less effective and amorphize a smaller material region with lower resulting resistance.

The reading operation must be performed at voltages sufficiently low not to alter the programmed state; from figure 3.3, one might want to measure in the leftmost part of the I-V region. The reading voltage V_{read} of choice for this case is $0.4V$.

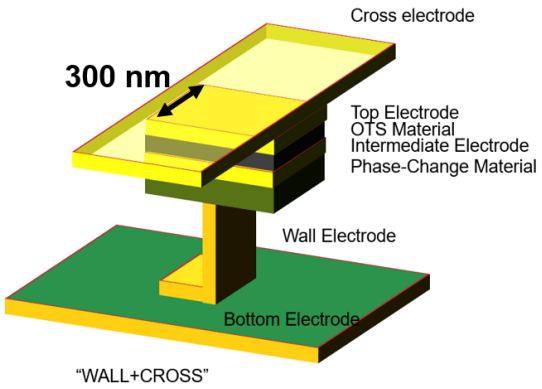
3.2 OTS Selector and Memory (1S1R)

The DUT is made by a stacked OTS selector and a PCM cell with a Wall-Heater configuration (figure 3.4).
To enable single device test and current control, each device is stacked on top of a front-end N-MOS transistor. The presence of the transistor is important to enable the proper current control necessary to avoid damage to the 1S1R device during programming and reading operations.
In a final Crossbar architecture, the OTS itself would be the only selector, and current-limiter transistors will be present only at the periphery.

The device was fabricated in various sizes, ranging from the largest $300nm$ proof-of-concept down to state-of-the-art technology feature size. Unless otherwise specified the size is assumed to be the largest ($300nm$). The OTS material employed is $GeSbSeN$ referred to as GSSN.



(a) Circuit scheme of the selector and memory stack, OTS is sandwiched between the Top Electrode (BL) and an intermediate electrode.



(b) 3D representation of the fabricated device, wall width of $300nm$ is highlighted.

Figure 3.4: OTS Selector with PCM memory layer.

The typical characteristic of the Device is reported in figure 3.5, here the subthreshold and threshold regions are highlighted. To acquire such

characteristics an increasing voltage is applied to the Bit Line while keeping the source at the ground. The Word Line acts on the gate of the transistor and limits the current (in figure 3.5 the current is limited at around $1mA$).

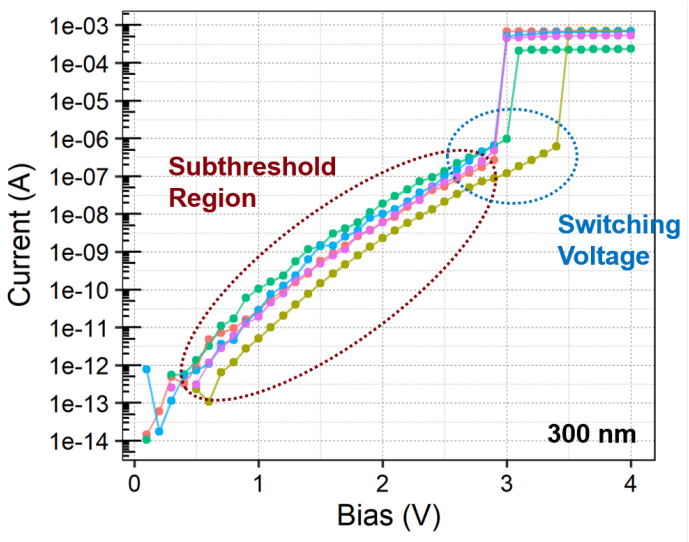


Figure 3.5: I/V Characteristic of five devices, subthreshold and threshold region are circled.
The threshold voltage is slightly different across the five devices and hints at the inter-device variability issue that will be discussed afterward. The current after switching appears flat (reported in logarithmic scale) due limitation provided by the transistor.

3.2.1 Subthreshold region

Subthreshold conduction depends on the material and may be dominated by one or more phenomena, as described in section 2.3.2. To investigate it, subthreshold characteristics of multiple devices have been taken into account and their linear regression approximations have been extracted (figure 3.6). Slope and Intercept parameters from the fitting are collected and may be related to the physical model.

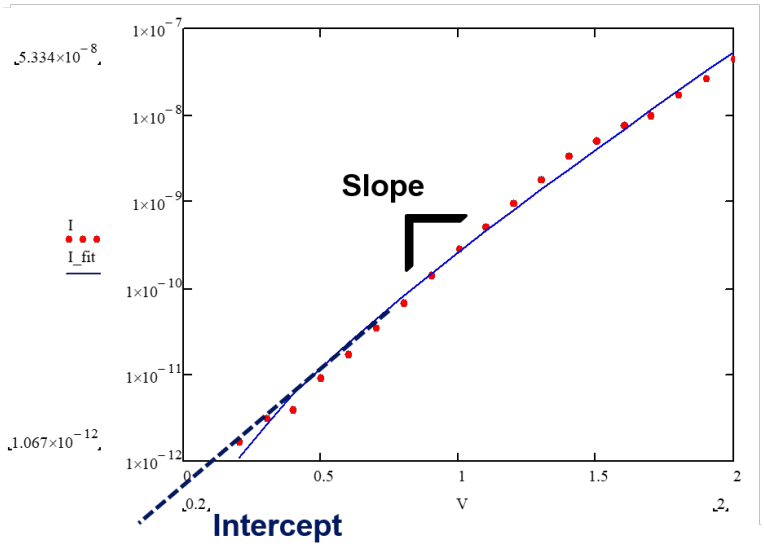


Figure 3.6: Experimental points (red) and fitted line (blue) of the subthreshold I/V characteristic for a single device. This model extrapolation has been performed multiple times for over 40 devices to acquire sufficient data on the slope and intercept of the lines.

Referring to the conduction model proposed by Ielmini [14] and already described in section 2.3.2, the current in subthreshold is expressed as a function of physical parameters and applied bias.

$$I = 2qAN_{T,tot}\frac{\Delta z}{\tau_0}e^{-\frac{E_C-E_F}{kT}}\sinh\frac{qV_A}{kT}\frac{\Delta z}{2u_a} \tag{3.1}$$

To quickly recall the symbols in the equation: A is the contact area, the amorphous layer thickness u_a, $N_{T,tot}$ is the total trap density above E_F. $\frac{\Delta z}{\tau_0}$ is the electron velocity; Δz is the inter-trap distance over the characteristic attempt-to-escape time τ_0.

This relation may be approximated in the Exponential subthreshold region (just before the switching voltage) since for large voltages the sinh function will approach an exponential function, and the current may be approximate with only the forward current (neglecting the thermal activated backward current) $I \approx I_{\rightarrow}$.
Since we are interested mostly in the Subthreshold Slope (STS) of the

curve, we can perform the logarithm of the current to obtain a linear relation with the voltage.

$$I \approx 2qAN_{T,tot}\frac{\Delta z}{\tau_0}e^{-\frac{E_C-E_F}{kT}}e^{\frac{qV_A}{kT}\frac{\Delta z}{2u_a}} \tag{3.2}$$

$$\Longrightarrow \log I = \log K + \frac{q}{kT}\frac{\Delta z}{2u_a}V_a \tag{3.3}$$

Where K is the intercept in the log plot and it includes all the multiplicative terms before the exponential; it will not be accounted for in this preliminary analysis.
The STS is therefore $STS = \gamma/kT$ where γ is simply $\gamma = q\Delta z/2u_a$ and is related to the material properties like the average inter-trap distance and the amorphous region thickness.
The STS may provide interesting results to compare different materials and architecture, but due to the lack of sufficient experimental data and comparison elements, its discussion will be omitted.

The proportionality between voltage and log of current seems to be linear, but this may not be the case depending on the underlying physical model. In particular, the proportionality $\log I \propto V$ implies a Poole model of conduction, while in the literature it is often reported the proportionality with the square root of the voltage $\log I \propto \sqrt{V}$ that corresponds to a Poole-Frenkel model of conduction.

To verify which phenomenon is more predominant in our case, the linear regression has been performed to minimize the error between the experimental data and V^n where the exponent n is the parameter to act to achieve minimization.
Results were collected for a population of more than forty devices and are reported in figure 3.7, the normal distribution seems to be centered at around 0.6, hinting that the underlying mechanism (withing experimental uncertainty) may be a Poole-Frenkel one with $\log I \propto \sqrt{V}$.

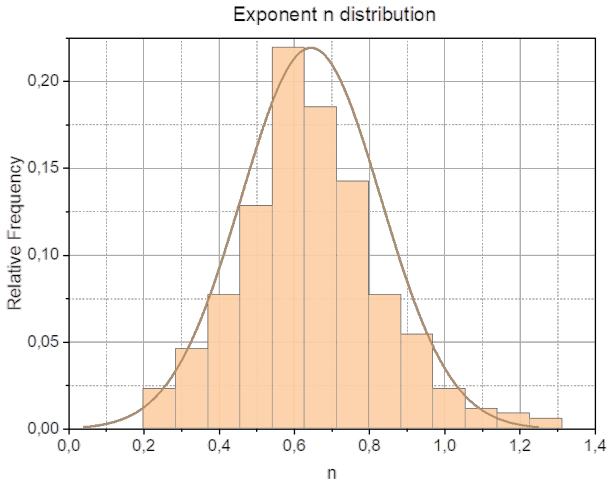


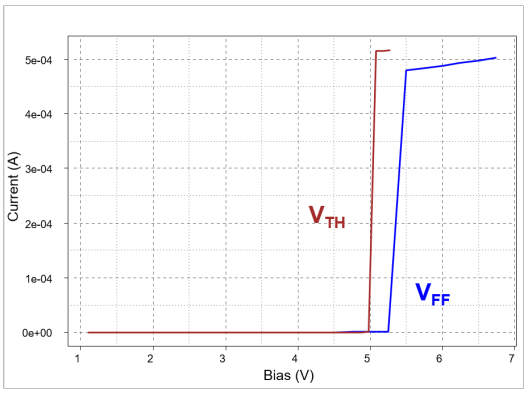
Figure 3.7: Exponent n distribution, the current is proportional to the exponent of the voltage at the nth power. Within experimental error, the coefficient appears close to 0.5 implying the dominant contribution of Poole-Frenkel conduction type.

3.2.2 First Fire

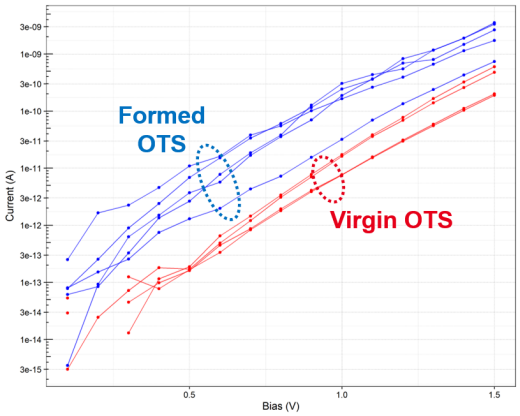
OTS materials require de facto a First-Fire (FF) step in order to start showing the expected Threshold Switching.
Before FF step the as-deposited OTS is in a high-resistive state. The state of the PCM is unknown and depends on the fabrication process, and on the thermal budget of the BEOL process: once the device is fired, a large current will pass that must be kept under control to avoid damages to the stack.
If the current is too high for too long the OTS may irreversibly crystallize; electro and thermal migration may form voids in the layer.

First Fire voltage is usually higher than the highest RESET threshold voltage (figure 3.8a) so care must be taken when designing commercial devices since such high voltage must be achieved at the beginning of each device's life.
After Firing a conductive filament is formed in the device hence making structural changes to the device (figure 3.8b) that may be appreciated as an increase of conductivity and dispersion from the pristine to the

formed state.



(a) I/V characteristic that shows the threshold voltage during First Fire step and the highest threshold voltage during RESET for the same device.



(b) Subthreshold characteristic comparison. In Red are the curves for five virgin (as deposited) devices, and in blue are reported the same devices after the FF step.

Figure 3.8: Effect of First Fire (Forming) step on the device characteristic.

3.2.3 Threshold voltage measurements

Referring to picture 3.5 the most interesting behavior is the one around the switching voltage. The device is characterized by means of an I/V curve: the voltage is increased and the current is measured at the same time. At the switching event, the transistor in series with the 1S1R device limits the current by proper control of the gate voltage.
The threshold voltage of the device is determined by the state of the PCM, and it shifts to higher voltages when the PCM amorphize.

The protocol consists of first programming the device in a known state (either SET or RESET) with reasonable pulses for this step; once programmed, a current pulse is applied whose intensity starts as low as possible and increases after each iteration of the protocol. The last step is the staircase for the threshold detection.
Such protocol (reported in figure 3.10) allows us to appreciate what happens to the memory device when it is subject to different current pulse intensities.

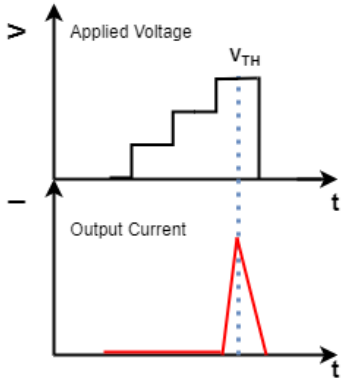


Figure 3.9: Reading staircase step: a voltage staircase is applied to the device and the current is read, when a spike of current is detected it means that the device has switched. After switching the voltage value is stored and the sequence is stopped to avoid damaging the cell with high currents for a long time.

(a) SET-Prog-Staircase protocol (b) RESET-Prog-Staircase protocol

Figure 3.10: SET and RESET protocols. After programming the PCM in the desired state, an increasing pulse is applied and then the threshold is recorded with a staircase ramp. The increasing programming pulse will change the state of the PCM causing a shift in the threshold voltage

The results are reported in figure 3.11 with a programming pulse current going from almost zero up to $3mA$. When the device is programmed in the SET state (red curve) it has a low threshold voltage. As the current increases, the PCM starts to amorphize leading to an increase in the threshold voltage. The threshold voltage saturates for currents that approach $2.5mA$ since the amorphous region has reached the maximum size possible: applying higher currents does not produce any increase in the threshold and on the contrary, it could be detrimental to the device functionality.

The blue curve in figure 3.11 shows the same protocol that starts with a

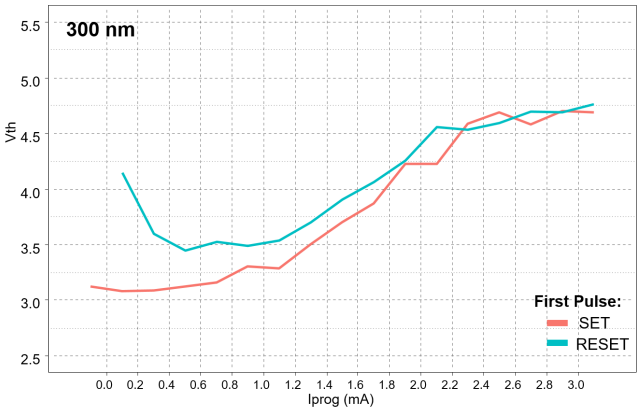


Figure 3.11: Protocol results for the DUT, the curve of the SET protocol in red while the RESET one in blue. The curve is obtained by averaging the characteristic of about 40 devices.

RESET pulse. For increasing current, the PCM will experience partial recrystallization before following the same trend as the SET curve.

In figure 3.12 the regions to optimize both SET and RESET pulses are highlighted. The figure reports also the reading windows between a full SET and RESET that is, for the $300nm$ device around $\Delta V_{TH} \approx 1.5V$.

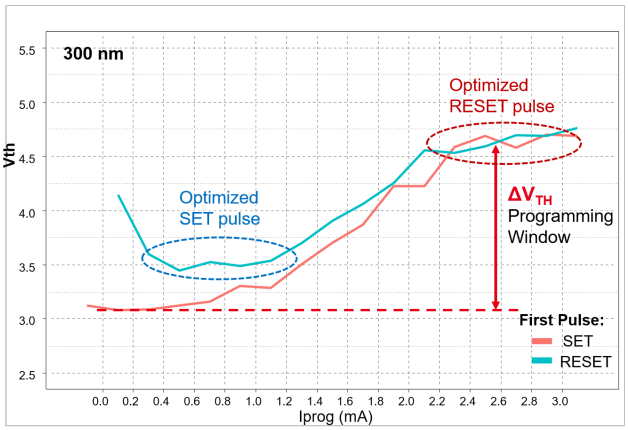


Figure 3.12: Same graph as in figure 3.11, here the optimized current values for SET and RESET pulses are highlighted; the threshold voltage window ΔV_{TH} is the difference between full SET and RESET V_{TH}.

Size comparison

During the Internship, it was possible to test smaller devices as well ($60nm$). Threshold voltage comparison of the characteristic to the largest proof-of-concept $300nm$ stack is reported in figure 3.13.
It is clear that the voltage range between the two sizes is compatible: both have V_{TH} bounded between 3 and 4 Volts. What changes between the two is of course the current, lower in the smaller size, in agreement with expectations.
Such scaled devices were not further analyzed during the internship.

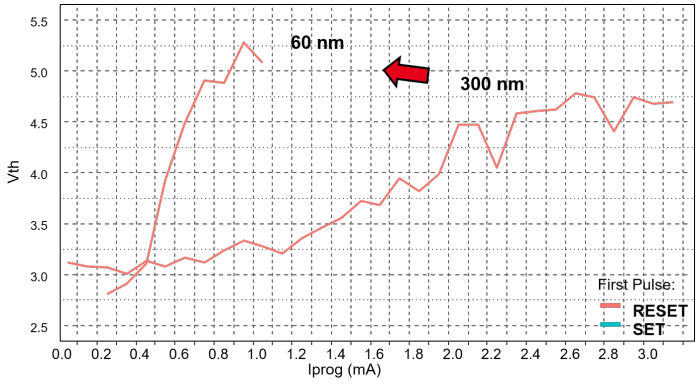


Figure 3.13: Effect of size on the threshold voltage. The adopted protocol is the same, the data for $300nm$ devices is reported alongside the curve for a $60nm$ wall width device.

Threshold Voltage Distribution

From all the data collected to perform the aforementioned tests, is possible to represent a distribution of the two programmed states. In figure 3.14 cumulative data for 40 devices are reported.
In agreement with what has been shown before, the $V_{TH,SET}$ is centered at around $3.2V$ and $V_{TH,RES}$ at $4.5V$ with a voltage reading window of about $1.5V$.
This representation highlights a different aspect of the inter-device variability: the overlapping tails between the two normal distributions are the devices that were not able to consistently SET or RESET leading to intermediate V_{TH} values. Such cells would not work in a final product and

will therefore increase the overall Bit Error Rate (BER) of the array device. Keeping these tails as low as possible, and achieving distributions with low variability (and narrow σ) is the final goal.

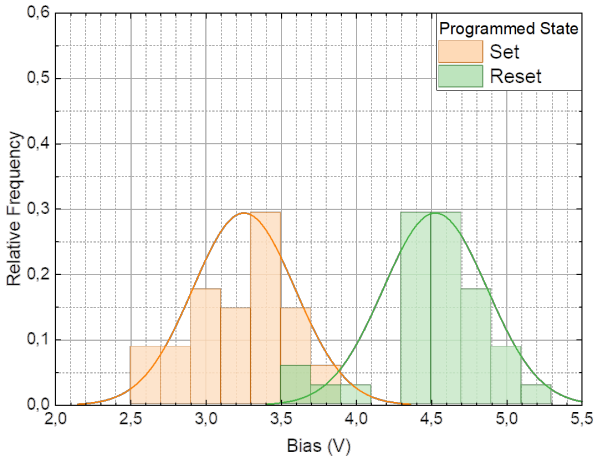


Figure 3.14: Threshold voltage distribution for the two possible states. Distribution appears quite broad indicating a large variability in the process. The overlapping tails correspond to an increase of the BER in the memory.

3.2.4 Cycling Endurance

Along cycling, both OTS and PCM could face partial or total degradation compromising the device functionality. Therefore is important to quantify and characterize the cycling endurance of the device.

The filament formation in the OTS usually limits its lifetime to lower switching cycles than a PCM device because of unwanted and permanent crystallization of the selector [25]. Nonetheless, the PCM is affected by switching, large current density, and electric field that may cause electromigration of species and formation of voids [26]. Such phenomena should be limited by proper engineering of the materials, the device structure, and of the array design and programming/reading strategies.

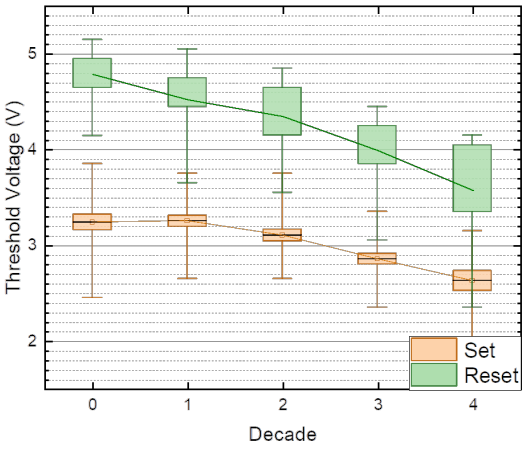


Figure 3.15: Vth for SET and RESET state reported as a function of the cycling decade. The solid box represents the standard error while the whiskers show the outlier elements.

Devices have been tested by repeating SET and RESET pulses over 10^4 times to obtain preliminary insight on the threshold window evolution.
As shown in figure 3.15 the window reduces from the stated $1.5V$ to about $0.6V$ in just 10.000 iterations. Is worth mentioning that the RESET state seems to suffer more from this increase of dispersion than the SET state, this could be related to a degradation of the PCM rather than the OTS. The SET state, while moving towards slightly lower V_{TH} seems to be unaffected by the cycling: the OTS can switch correctly when the PCM is crystalline. On the contrary, the threshold voltage associated with the amorphous PCM seems to increase in variability.
In the picture also the extremes V_{TH} values are reported (as whiskers) that show how distribution tails overlap right after few cycles.

3.3 Crossbar Array (1T1S1R)

The crossbar architecture as described in section 2.4 is not the one that has been implemented in the tested wafer; in fact, the architecture is an array of 1T1S1R devices with a transistor in series (figure 3.16), the size of the

array is $32 \times 32 = 1024$ cells. The wall width is $60nm$ as in the test in 3.2.3. Due to time constraints, 1S1R Crossbar test vehicles were not tested.

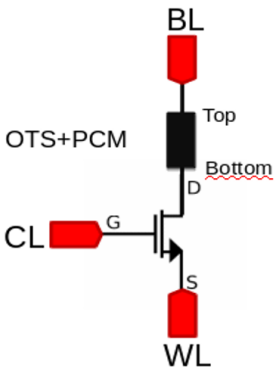


Figure 3.16: Circuit scheme of a single device in the array structure, that is identical to the ones described in section 3.2

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The presence of the transistor makes this architecture substantially different from a *real* crossbar, in this case, single device addressing is achieved by setting the gate voltage of the limiting transistor.
For test purposes, the presence of the transistor allows controlling the current that flows into the stack and isolating broken or malfunctioning devices from the analysis. Final validation should be performed in a real Crossbar architecture made of 1S1R devices only.

First Fire in the array is more difficult than for a single device: the requirement is to be compliant with the periphery that in this case is biased with a $5V$ supply. From single device test (figure 3.8a) we know that the forming voltage may be higher than the supply; in this case, the procedure involves applying the forming pulse repeatedly for a longer cumulative time so that, due to the stochastic process of switching, the device can undergo the fire operation.
This is what has been done in figure 3.17 where the number of devices not yet formed (over the total) is reported versus the cumulative time of applied $5V$ pulses. After about $1ms$ more than 90% of devices seem to be correctly formed.

Given the results of this preliminary test, the correctly formed devices

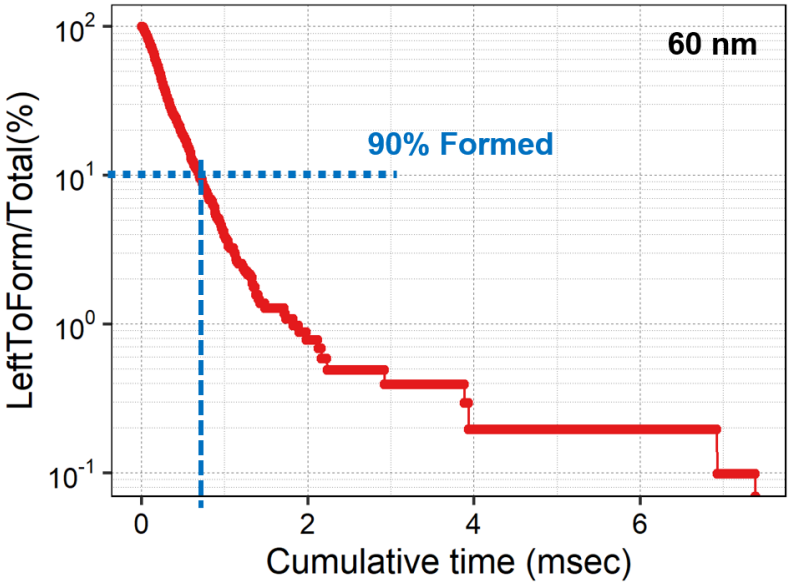

Figure 3.17: Percentage of devices that are yet to be formed over the cumulative time of the forming pulse. After many repeated pulses, each device may stochastically fire: after about $1ms$ more than 90% of the array has successfully fired.

have been SET and RESET (over about 100 times) to verify the programming window for the family of DUTs analyzed. The results shown in figure 3.18 demonstrate a good separation between the two threshold voltages while most of the devices seem to be correctly programmed with only a few that have intermediate tail V_{TH} values.

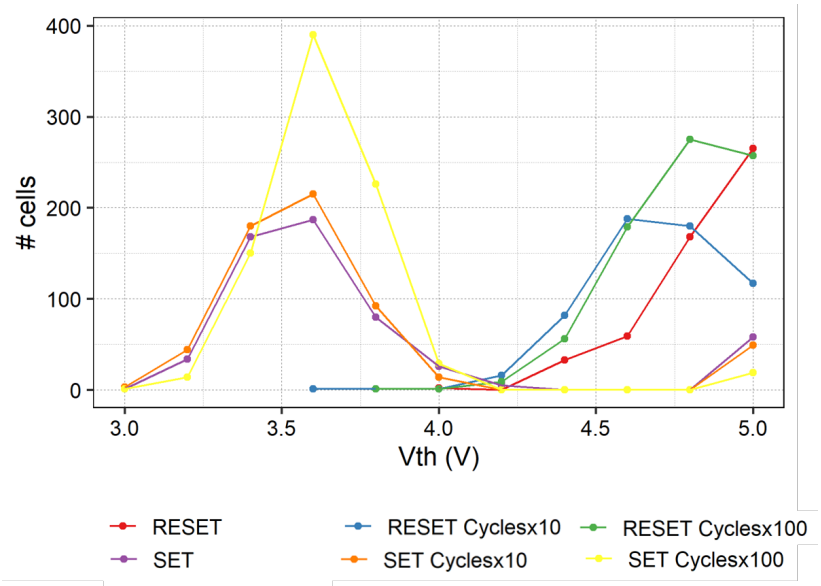

Figure 3.18: Threshold voltage distribution for a 1kbit array of devices, the two distributions show SET and RESET state V_{th} for a few cycles.

Chapter 4

Outlook

In the frame of the Internship PCM memory, OTS selectors, and Crossbar Array architecture have been studied starting from the bibliography and supporting the theory with experimental evidence on real devices available thanks to the capability of the CEA-Leti laboratory. The internship was structured to gradually improve knowledge starting from the basics of Phase-Change memory (figure 4.1) moving to the combined adoption of PCM memory with OTS selector, and ending with an overview of the Crossbar Array architecture.

Figure 4.1: Internship outlook scheme, starting from the study of PCM up to the future perspectives on emerging memories.

This work introduces the topics of PCM memory, OTS selectors, and Crossbar Array architecture. A brief theoretical description of the device and physics is followed by experimental electrical characterization as performed during the internship, thanks to the capability of the CEA-Leti laboratory. The internship was structured to improve knowledge gradually, starting from the basics of Phase-Change memory (figure 4.1), advancing to the combined adoption of PCM memory with OTS selector,

and concluding with an overview of the Crossbar Array architecture.

PCM memory has been studied from the available bibliography (sec. 2.2); preliminary test to validate the devices were carried out (sec. 3.1). Devices work as expected and within ranges compatible with those available in the literature.

The analysis pivoted on OTS selectors used in combination with the memory element. Devices have been first studied from the physics standpoint (sec. 2.3.2), then verified with experimental results; the working principle and main figures of merit were reported (sec. 3.2). The results show that such a device behaves as expected and may be exploited to enable new opportunities either as is or in combination with other memory technologies [16]. There are still challenges regarding V_{TH} variability and device fabrication.

The Crossbar architecture promise to further improve and push forward the performance of this technology by achieving a dense, stackable and portable solution that is independent on the front end. It may find many applications in the market as both stand-alone or embedded [3], [4], [27].
I could perform only a preliminary test with a simplified and safer structure closer to an array than a real cross-point; further test to verify leakage and addressing is required.

4.1 Future Perspectives

Following the scheme of figure 4.1, future study (with a Ph.D.) may involve a real Crossbar array with OTS selectors to fully address all the opportunities enabled by this technology. Different materials, new and emerging paths, can be investigated to improve current performance.
Recent papers [28] propose innovative ways to approach the matter, like the voltage polarity-dependent memory effect of some OTS materials.

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