



Politecnico
di Torino

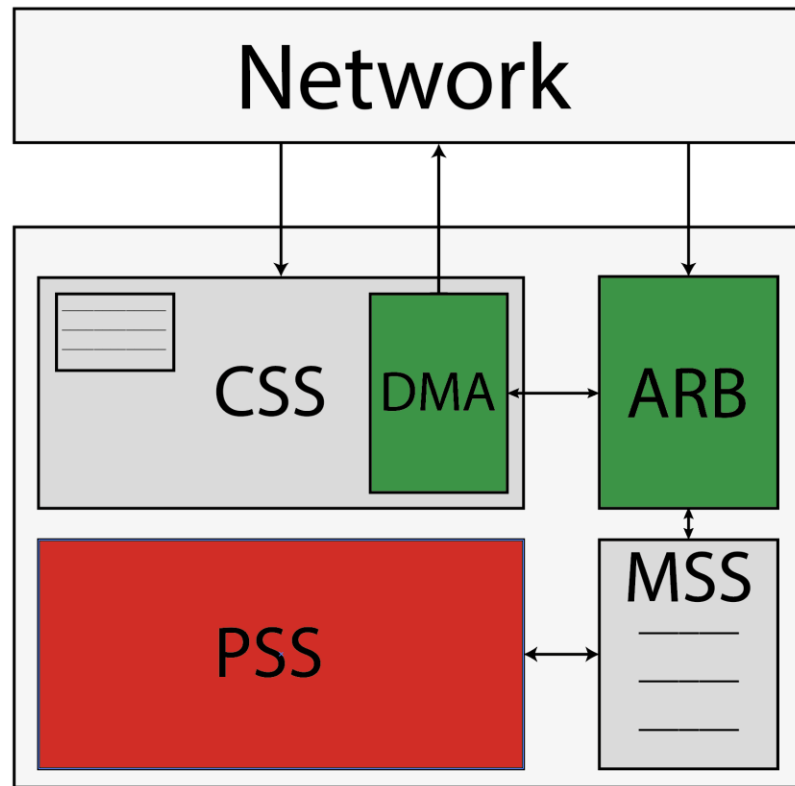


LDPC 5G decoder implementation for EMBB project

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Overview of the library to be implemented

The **grey** blocks will not be implemented in this Project.

The two **green** blocks are used for handling the transfer of data inside and outside the library.

The **red** block is used for processing the decoding process.

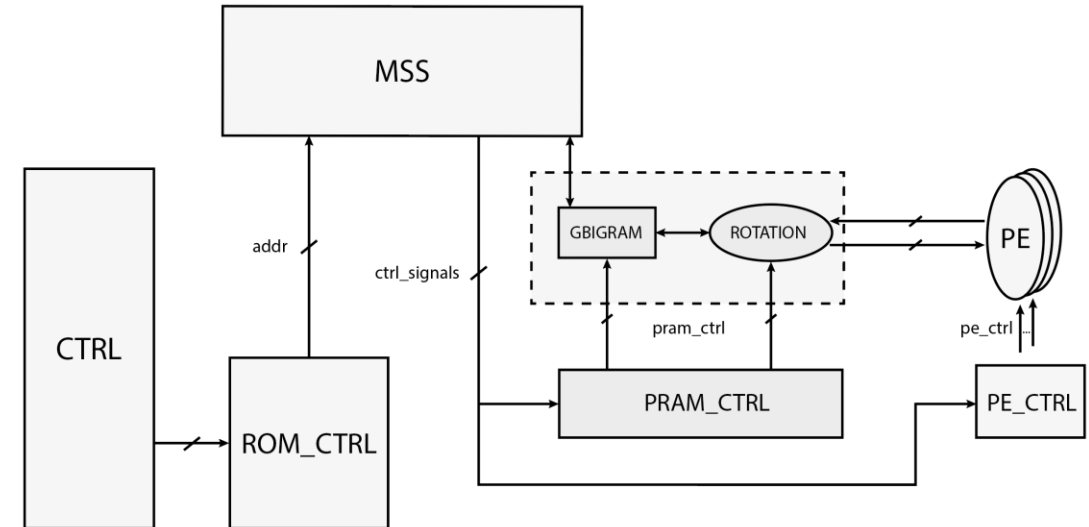
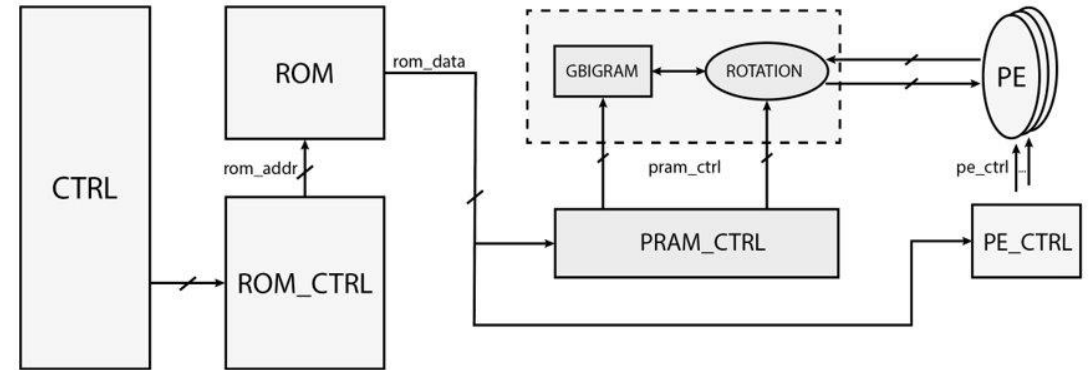
INTRODUCTION TO THE TOPICS COVERED

- ▶ The discussion of this block will be divided into the following parts:
 - **Overview** of general block structure
 - **Analysis** of the most important blocks
 - **Generation** of control signals
 - **Timing diagram** using the processing of the first two lines as an example.



Process Sub System (PSS)

- ▶ This block deals with decoding, and its structure is divided into three blocks:
 - **ROM:** where the PSS control signals are stored. The values stored in this block are actually stored in the MSS.
 - **PRAM:** where the samples to be decoded are stored.
 - **PE:** where the decoding algorithm is processed.



PROCESSING ELEMENT (PE)

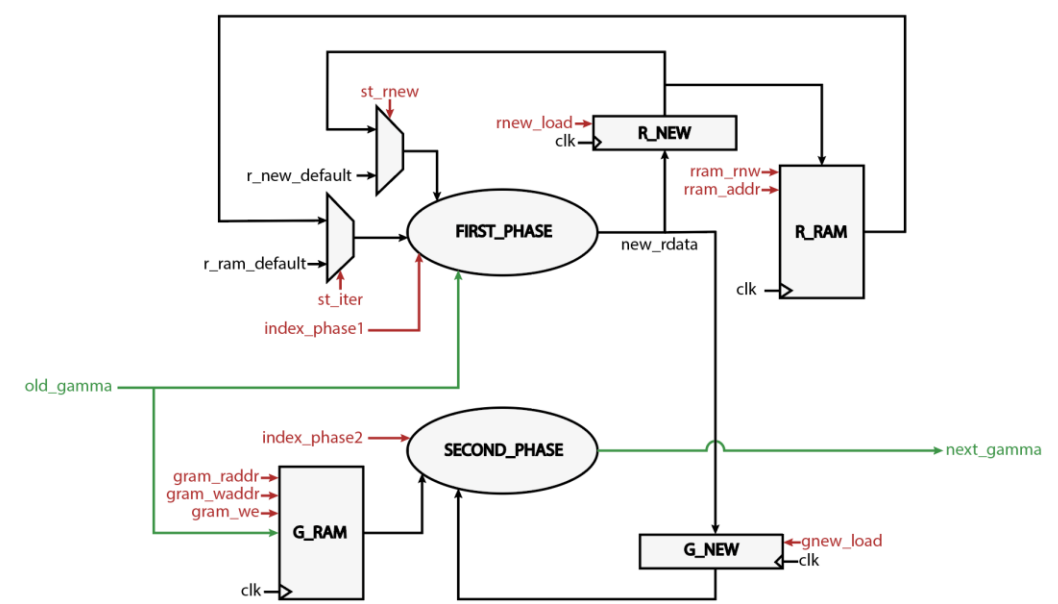
The structure of this block is intended to implement algorithm 5 shown in the figure.

The algorithm in question is the result of various optimizations; it divides the decoding work into two phases:

- The first phase runs from line 7 to line 25; it takes care of updating vectors' value, previously initialized in line 9.
- During the second phase, the new corrected values of the samples (*next_gamma*) will be generated. This correction is made using the array of values previously updated during the first phase.

As the LDPC algorithm is *iterative*, it is necessary to save the array values calculated in the first step to be reused for subsequent iterations.

The **R_RAM** memory is used to store the arrays of values calculated during the first phase, then read during subsequent iterations.



Algorithm 5 The memory-optimized SCMS algorithm with layered schedule

```

1: for  $n = 0$  to  $N - 1$  do ▷ For all columns
2:    $\tilde{\gamma}_n^{(0)} \leftarrow \ln(\Pr(x_n = 0 | \text{channel}) / \Pr(x_n = 1 | \text{channel}))$  ▷ LLRs
3: end for
4: for  $m = 0$  to  $M - 1$  do ▷ For all rows
5:    $r_m^{(0)} = \{0, 0, 0, +1, +1, \text{true}\}$ 
6: end for
7: for  $l = 1$  to  $l_{max}$  do
8:   for  $m = 0$  to  $M - 1$  do
9:      $r_m^{(l)} \leftarrow \{+\infty, +\infty, 0, +1, +1, \text{false}\}$ 
10:    for  $n \in \mathcal{H}(m)$  do
11:       $\alpha \leftarrow \tilde{\gamma}_n^{(l-1)} - \beta(r_m^{(l-1)}, n)$ 
12:      if  $\text{sgn}(\alpha) \neq r_m^{(l-1)}. \alpha_n^s$  and (not  $r_m^{(l-1)}. \alpha_n^e$ ) then
13:         $\alpha \leftarrow 0$ 
14:         $r_m^{(l)}. \alpha_n^e \leftarrow \text{true}$ 
15:      end if
16:       $r_m^{(l)}. \alpha_n^s \leftarrow \text{sgn}(\alpha)$ 
17:       $r_m^{(l)}. sp \leftarrow r_m^{(l)}. sp \times \text{sgn}(\alpha)$ 
18:      if  $|\alpha| < r_m^{(l)}. m_1$  then
19:         $r_m^{(l)}. m_2 \leftarrow r_m^{(l)}. m_1$ 
20:         $r_m^{(l)}. m_1 \leftarrow |\alpha|$ 
21:         $r_m^{(l)}. i \leftarrow n$ 
22:      else if  $|\alpha| < r_m^{(l)}. m_2$  then
23:         $r_m^{(l)}. m_2 \leftarrow |\alpha|$ 
24:      end if
25:    end for
26:    for  $n \in \mathcal{H}(m)$  do
27:       $\tilde{\gamma}_n^{(l)} \leftarrow \tilde{\gamma}_n^{(l-1)} + \beta(r_m^{(l)}, n)$ 
28:    end for
29:  end for
30: end for

```

Algorithm 4 Computing $\beta_{m,n}^{(l)}$ from $r_m^{(l)}$ compact data structure

```

1: if  $n = r_m^{(l)}. i$  then
2:    $\beta_{m,n}^{(l)} \leftarrow r_m^{(l)}. \alpha_n^s \times r_m^{(l)}. sp \times r_m^{(l)}. m_2$ 
3: else
4:    $\beta_{m,n}^{(l)} \leftarrow r_m^{(l)}. \alpha_n^s \times r_m^{(l)}. sp \times r_m^{(l)}. m_1$ 
5: end if

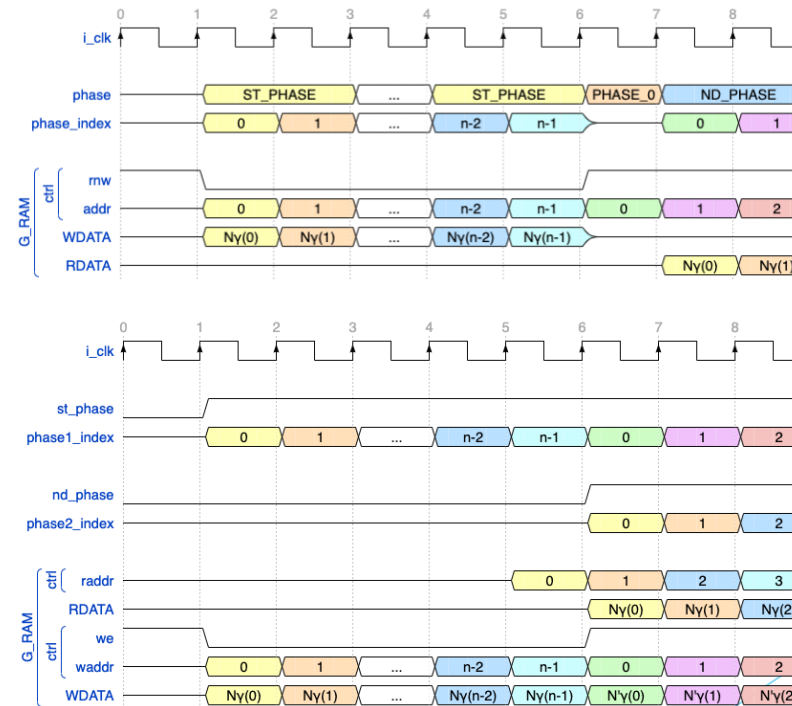
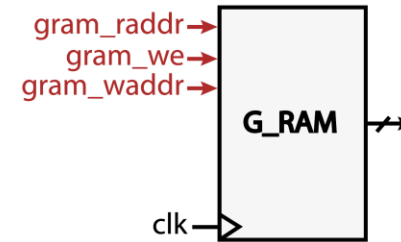
```

GRAM

This memory is used for **storing values**, as in the second one, the previously analyzed gamma values must also be used to generate the correct values.

For this reason, a single-access memory is used within the project. Its use, however, makes it necessary to have clock strokes in which no phase is processed, and the memory is accessed in reading mode for the second phase.

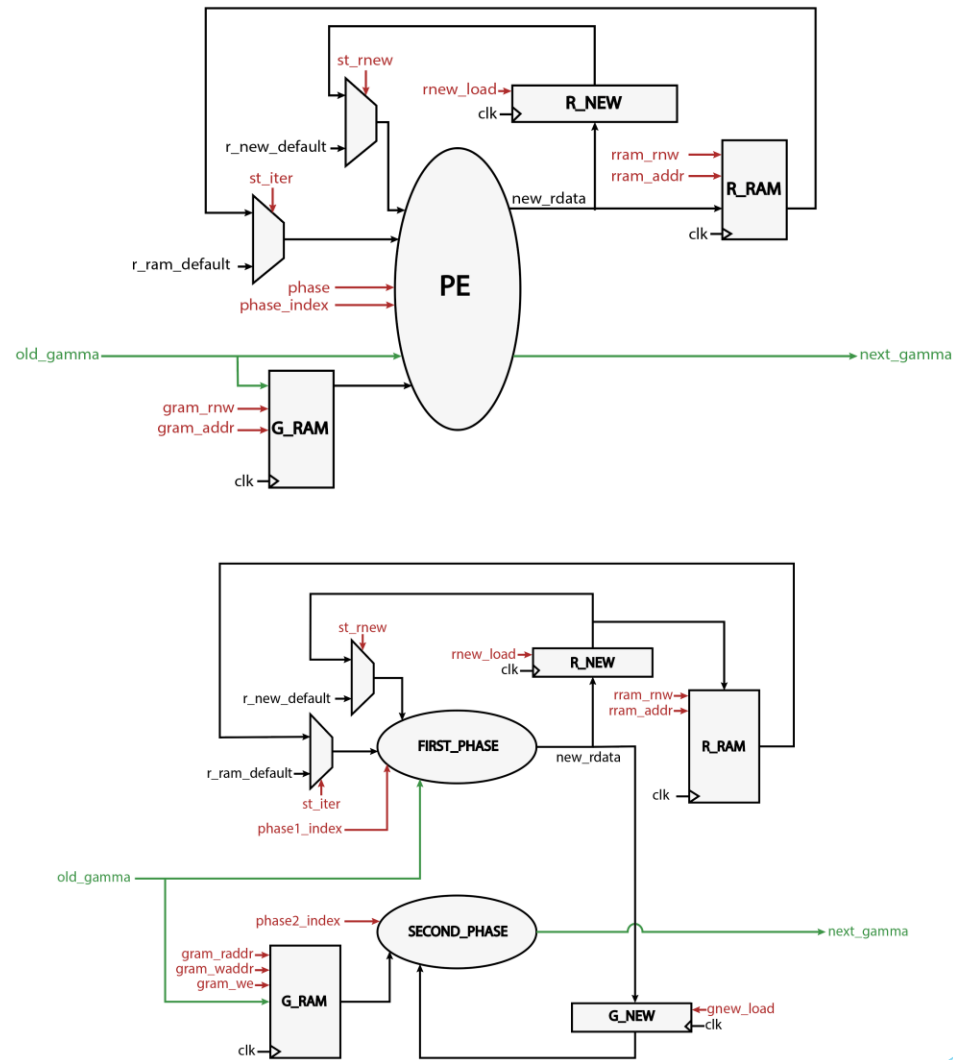
To eliminate this problem and guarantee independence between the first and second phase, this memory is replaced by a **dual-port memory**.



Parallelisation of the two phases

Finally, what is missing actually to *process the two phases in parallel* is to ensure that the array of values calculated during the first phase is stored, as needed during the second phase.

For this reason, the register **G_NEW** was introduced, which is identical to **R_NEW**, but unlike it, its value is only updated at the end of the first phase in order to store the new value array.

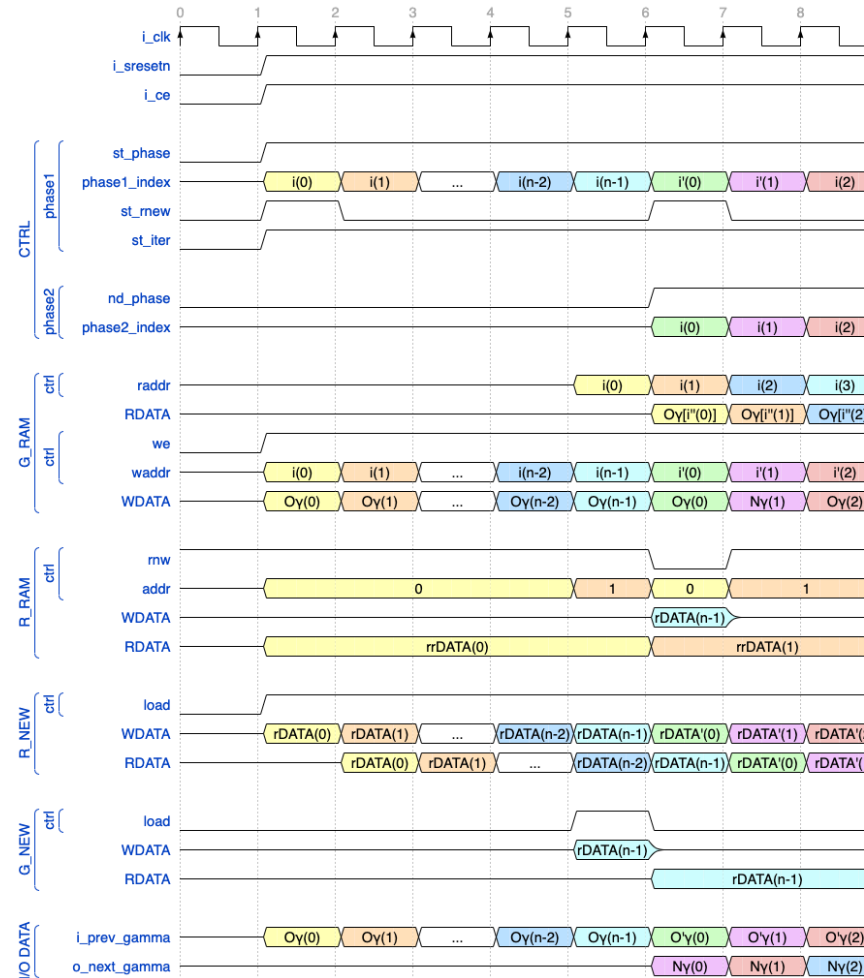


PE Timing diagram

The timing diagram opposite summarises all the features discussed above.

Following the workflow, it is interesting to note the following points:

- The constant use of both **GRAM** read and write operations.
- The alternation of **RRAM** read and write operations.
- The updating of the **G_NEW_REG** values at the end of the first phase.

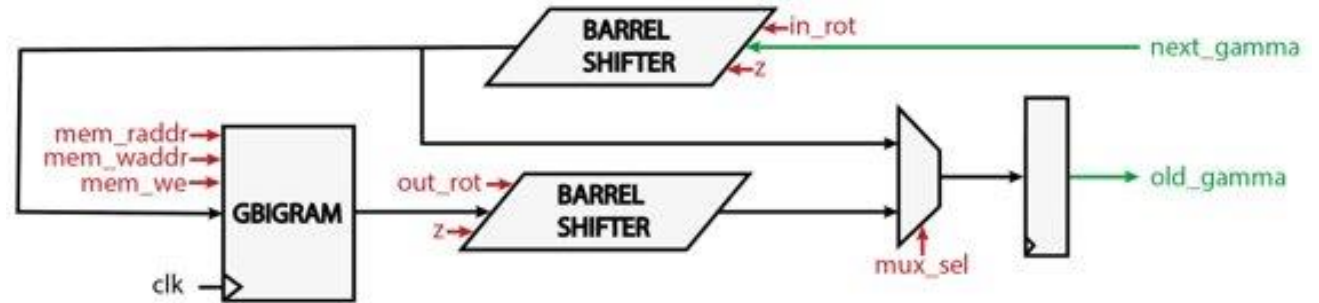
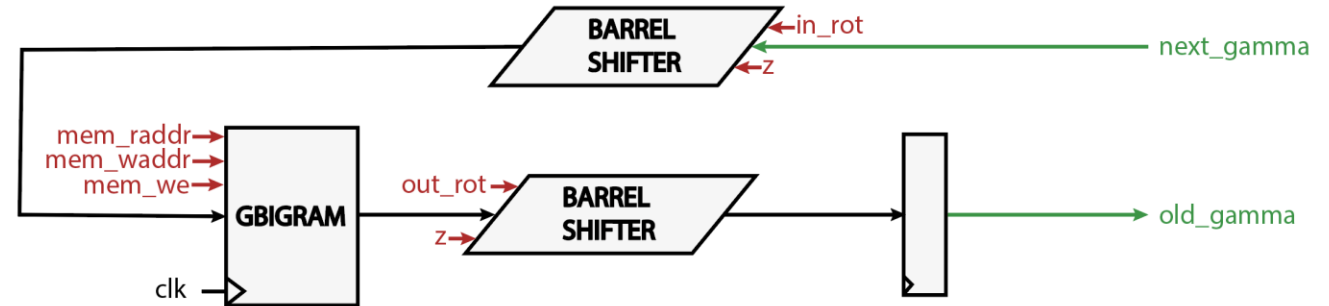


PRAM

This block handles the management of new and old gamma values sent and received, respectively from the PE.

Its initial structure, shown in the image above, is already equipped with two barrel shifters for the rotation of the values to be analyzed. This is because, to parallel the first and second phases, it will also be necessary to manage in parallel the data to be sent and those to be rewritten in GBIGRAM.

In this case, the only optimization is implementing a bypass process that allows the data coming from a previous PE processing to be analyzed directly without the need to rewrite them in memory.



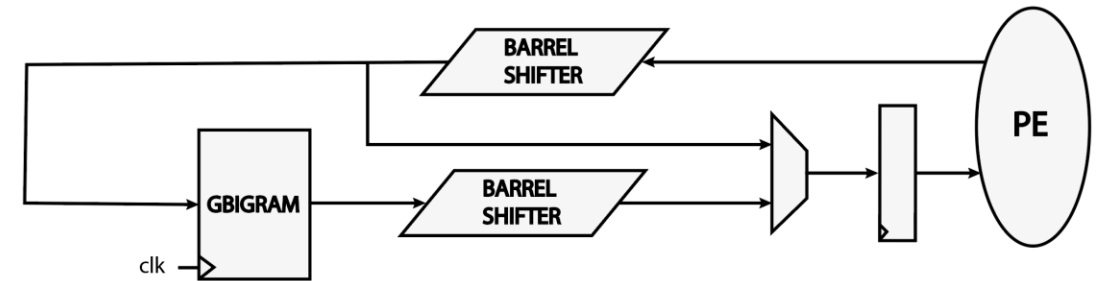
Control signals generator

The last of the three blocks is the **ROM** and what is interesting is not the hardware implementation but the software implementation that leads to the generation of the signals that will then be stored inside the **ROM**.

For this purpose, **Python code** was written to describe the behavior of the entire datapath and simulate data movement within it.

For this purpose, values can be set at program launch to set the memory elements within the circuit, leading to a delay in propagating the data.

In this case, the two memory elements register at the input of the **PE** and the **GBIGRAM**.



LDPC Base graph and its parity check matrices

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3	0	121	276	220	201	187	97	4	128
	1	89	87	208	18	145	94	6	23
	3	84	0	30	165	166	49	33	162
	4	20	275	197	5	108	279	113	220
	6	150	199	61	45	82	139	49	43
	7	131	153	175	142	132	166	21	186
	8	243	56	79	16	197	91	6	96
	10	136	132	281	34	41	106	151	1
	11	86	305	303	155	162	246	83	216
	12	246	231	253	213	57	345	154	22
	13	219	341	164	147	36	269	87	24
	14	211	212	53	69	115	185	5	167
	16	240	304	44	96	242	249	92	200
	17	76	300	28	74	165	215	173	32
	18	244	271	77	99	0	143	120	235
	20	144	39	319	30	113	121	2	172
	21	12	357	68	158	108	121	142	219
	22	1	1	1	1	1	1	0	1
	25	0	0	0	0	0	0	0	0
4	0	157	332	233	170	246	42	24	64
	1	102	181	205	10	235	256	204	211
	26	0	0	0	0	0	0	0	0

4	0	157	332	233	170	246	42	24	64
	1	102	181	205	10	235	256	204	211
	26	0	0	0	0	0	0	0	0
5	0	205	195	83	164	261	219	185	2
	1	236	14	292	59	181	130	100	171
	3	194	115	50	86	72	251	24	47
	12	231	166	318	80	283	322	65	143
	16	28	241	201	182	254	295	207	210
	21	123	51	267	130	79	258	161	180
	22	115	157	279	153	144	283	72	180
	27	0	0	0	0	0	0	0	0

It is important to note that analyzing the rows in the order described by the base graph leads to situations where, when moving from one row to another, there is a significant difference in the number of columns analyzed.

This means that it will be necessary to stop one of the two phases in many cases because it is **waiting for the other to finish**.

This problem is solved by **reordering the rows** at the beginning of the process.

0	0	250	307	73	223	211	294	0	135
	1	69	19	15	16	198	118	0	227
	2	226	50	103	94	188	167	0	126
	3	159	369	49	91	186	330	0	134
	5	100	181	240	74	219	207	0	84
	6	10	216	39	10	4	165	0	83
	9	59	317	15	0	29	243	0	53
	10	229	288	162	205	144	250	0	225
	11	110	109	215	216	116	1	0	205
	12	191	17	164	21	216	339	0	128
	13	9	357	133	215	115	201	0	75
	15	195	215	298	14	233	53	0	135
	16	23	106	110	70	144	347	0	217
	18	190	242	113	141	95	304	0	220
	19	35	180	16	198	216	167	0	90
	20	239	330	189	104	73	47	0	105
	21	31	346	32	81	261	188	0	137
	22	1	1	1	1	1	1	0	1
	23	0	0	0	0	0	0	0	0
1	0	2	76	303	141	179	77	22	96
	2	239	76	294	45	162	225	11	236
	3	117	73	27	151	223	96	124	136
	4	124	288	261	46	256	338	0	221
	5	71	144	161	119	160	268	10	128
	7	222	331	133	157	76	112	0	92
	8	104	331	4	133	202	302	0	172
	9	173	178	80	87	117	50	2	56
	11	220	295	129	206	109	167	16	11
	12	102	342	300	93	15	253	60	189
	14	109	217	76	79	72	334	0	95
	15	132	99	266	9	152	242	6	85
	16	142	354	72	118	158	257	30	153
	17	155	114	83	194	147	133	0	87
	19	255	331	260	31	156	9	168	163
	21	28	112	301	187	119	302	31	216
	22	0	0	0	0	0	0	105	0
	23	0	0	0	0	0	0	0	0
	24	0	0	0	0	0	0	0	0

RADDR	WADDR	WDATA	DATA(0)	DATA(1)	DATA(2)	RDATA
0	0	$O_\gamma(0)$	$O_\gamma(0)$	$O_\gamma(1)$	$O_\gamma(2)$	—
2	1	$O_\gamma(1)$	$O_\gamma(0)$	$O_\gamma(1)$	$O_\gamma(2)$	$O_\gamma(0)$
3	2	$O_\gamma(2)$	$O_\gamma(0)$	$O_\gamma(1)$	$O_\gamma(2)$	$O_\gamma(2)$

RADDR	WADDR	WDATA	DATA(0)	DATA(1)	DATA(2)	RDATA
0	0	$O_\gamma(0)$	$O_\gamma(0)$	$O_\gamma(1)$	$O_\gamma(2)$	—
2	2	$O_\gamma(1)$	$O_\gamma(0)$	$O_\gamma(1)$	$O_\gamma(2)$	$O_\gamma(0)$
3	3	$O_\gamma(2)$	$O_\gamma(0)$	$O_\gamma(1)$	$O_\gamma(1)$	$O_\gamma(2)$

In addition to reordering rows, it is also possible to **reorder columns**.

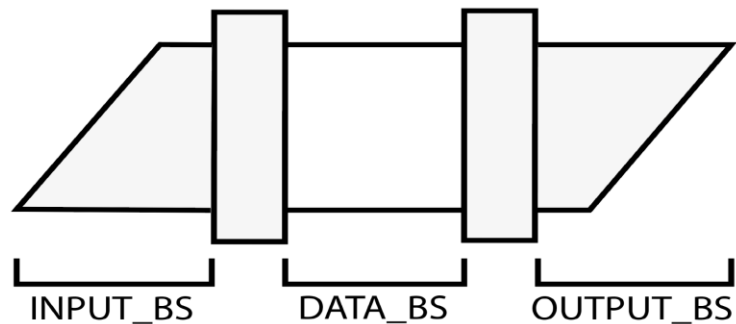
This optimization stems from the observation that two successive rows often have columns to process in common. For this reason, a **bypass** option has been added.

To take full advantage of this feature, it is necessary first to process the second phase within the PE, relating to the columns that are also present in the next row.

However, this **reordering of addresses inevitably affects the index's choice for the first phase**. It can no longer be chosen simply by increasing its value each time but must be congruent with that used for the second phase. In this way, the unread gamma values will not be overwritten.

BYPASS	INPUT_BS	DATA_BS	OUTPUT_BS
0	$O_{\gamma}(0)[\text{rot}(0)]$	—	—
0	$O_{\gamma}(1)[\text{rot}(1)]$	$O_{\gamma}(0)[\text{rot}(0)]$	—
0	$O_{\gamma}(2)[\text{rot}(2)]$	$O_{\gamma}(1)[\text{rot}(1)]$	$O_{\gamma}(0)[\text{rot}(0)]$
0	$O_{\gamma}(3)[\text{rot}(3)]$	$O_{\gamma}(2)[\text{rot}(2)]$	$O_{\gamma}(1)[\text{rot}(1)]$
1	$O_{\gamma}(4)[\text{rot}(4)]$	$O_{\gamma}(3)[\text{rot}(3)]$	$O_{\gamma}(2)[\text{rot}(2)]$
1	$O_{\gamma}(4)[\text{rot}(4)]$	$O_{\gamma}(4)[\text{rot}(4)]$	$O_{\gamma}(3)[\text{rot}(3)]$
1	$O_{\gamma}(4)[\text{rot}(4)]$	$O_{\gamma}(4)[\text{rot}(4)]$	$O_{\gamma}(4)[\text{rot}(4)]$

BYPASS	CE	INPUT_BS	DATA_BS	OUTPUT_BS
0	1	$O_{\gamma}(0)[\text{rot}(0)]$	—	—
0	1	$O_{\gamma}(1)[\text{rot}(1)]$	$O_{\gamma}(0)[\text{rot}(0)]$	—
0	1	$O_{\gamma}(2)[\text{rot}(2)]$	$O_{\gamma}(1)[\text{rot}(1)]$	$O_{\gamma}(0)[\text{rot}(0)]$
0	1	$O_{\gamma}(3)[\text{rot}(3)]$	$O_{\gamma}(2)[\text{rot}(2)]$	$O_{\gamma}(1)[\text{rot}(1)]$
1	0	$O_{\gamma}(4)[\text{rot}(4)]$	$O_{\gamma}(3)[\text{rot}(3)]$	$O_{\gamma}(2)[\text{rot}(2)]$
1	0	$O_{\gamma}(4)[\text{rot}(4)]$	$O_{\gamma}(3)[\text{rot}(3)]$	$O_{\gamma}(2)[\text{rot}(2)]$
1	0	$O_{\gamma}(4)[\text{rot}(4)]$	$O_{\gamma}(3)[\text{rot}(3)]$	$O_{\gamma}(2)[\text{rot}(2)]$



A final consideration should be made when it is necessary or optional to pipeline the barrel shifter.

In this case, it will be necessary to implement a **chip enable** to *block the data rotation process during the bypass period*.

Without a chip enable, all the data inside the barrel shifter would inevitably be lost during the bypass period, as can be seen in the table on the left.

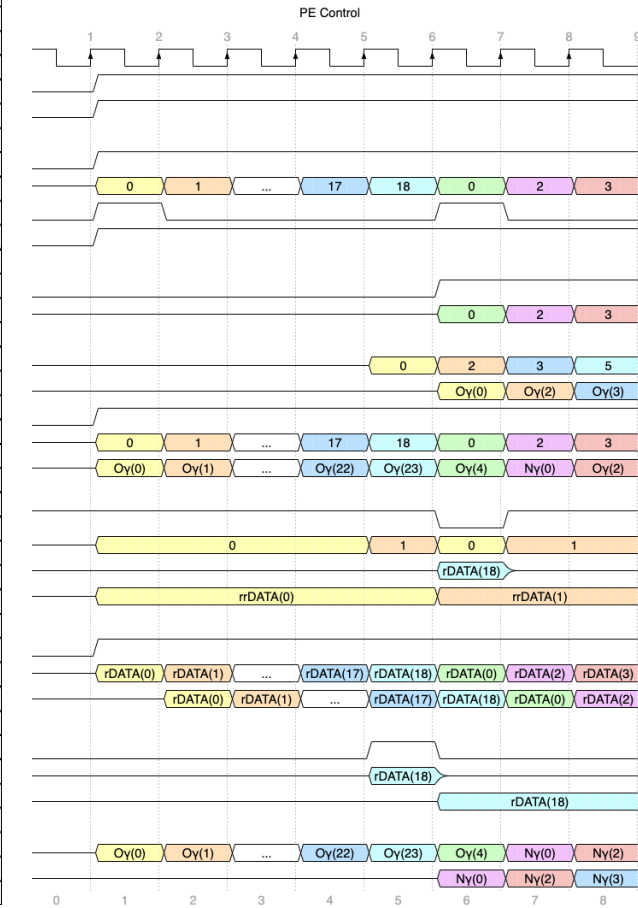
PE Timing Diagram

This timing diagram shows PE processing in the case of the two rows of the base graph.

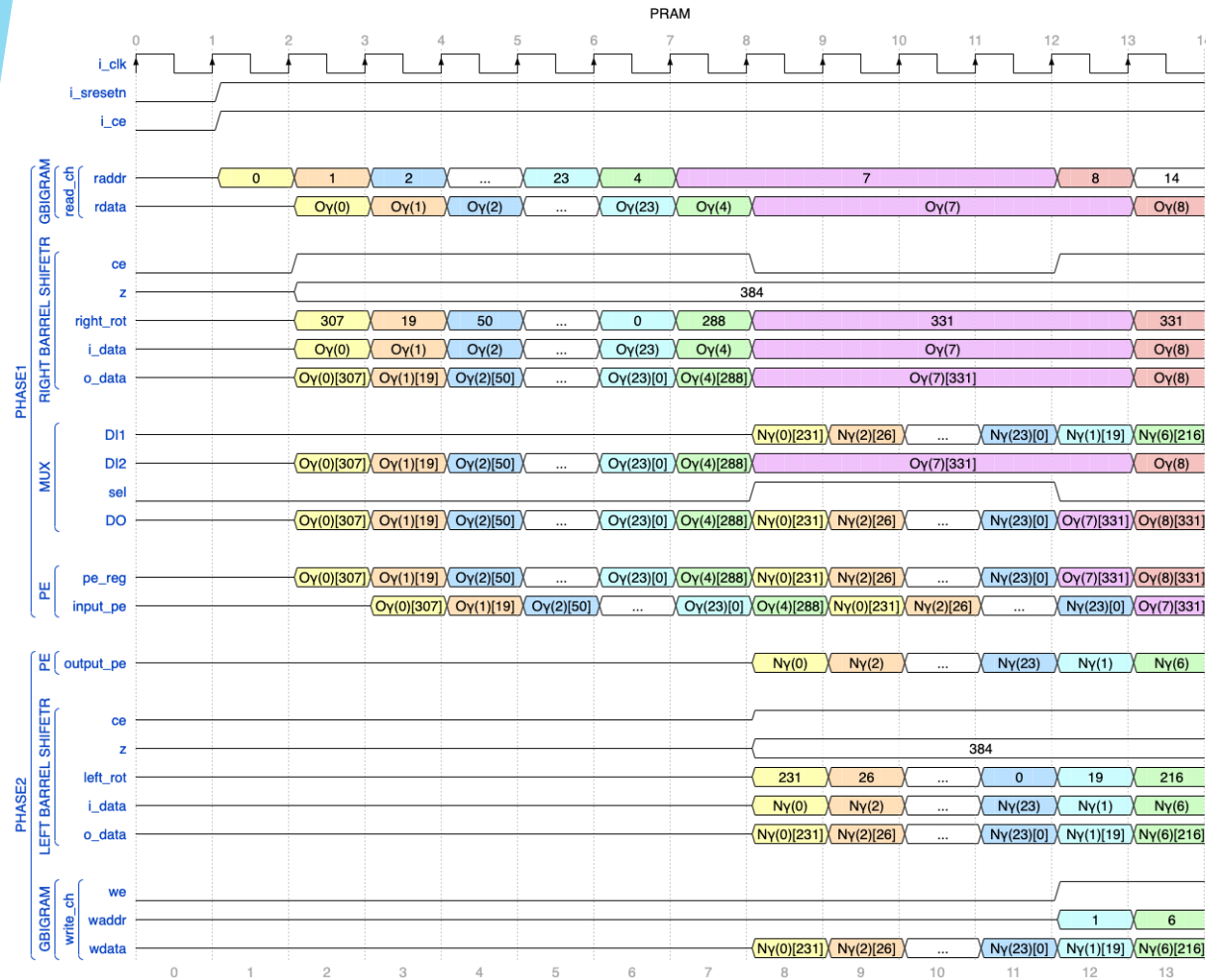
The values highlighted in yellow represent the columns present in both rows.

The values highlighted in orange represent the rotation value associated with each column.

0	0	250	307	73	223	211	294	0	135
	1	69	19	15	16	198	118	0	227
	2	226	50	103	94	188	167	0	126
	3	159	369	49	91	186	330	0	134
	5	100	181	240	74	219	207	0	84
	6	10	216	39	10	4	165	0	83
	9	59	317	15	0	29	243	0	53
	10	229	288	162	205	144	250	0	225
	11	110	109	215	216	116	1	0	205
	12	191	17	164	21	216	339	0	128
	13	9	357	133	215	115	201	0	75
	15	195	215	298	14	233	53	0	135
	16	23	106	110	70	144	347	0	217
	18	190	242	113	141	95	304	0	220
	19	35	180	16	198	216	167	0	90
	20	239	330	189	104	73	47	0	105
	21	31	346	32	81	261	188	0	137
	22	1	1	1	1	1	1	0	1
	23	0	0	0	0	0	0	0	0
1	0	2	76	303	141	179	77	22	96
	2	239	76	294	45	162	225	11	236
	3	117	73	27	151	223	96	124	136
	4	124	288	261	46	256	338	0	221
	5	71	144	161	119	160	268	10	128
	7	222	331	133	157	76	112	0	92
	8	104	331	4	133	202	302	0	172
	9	173	178	80	87	117	50	2	56
	11	220	295	129	206	109	167	16	11
	12	102	342	300	93	15	253	60	189
	14	109	217	76	79	72	334	0	95
	15	132	99	266	9	152	242	6	85
	16	142	354	72	118	158	257	30	153
	17	155	114	83	194	147	133	0	87
	19	255	331	260	31	156	9	168	163
	21	28	112	301	187	119	302	31	216
	22	0	0	0	0	0	0	105	0
	23	0	0	0	0	0	0	0	0
	24	0	0	0	0	0	0	0	0



PRAM Timing Diagram



0	0	250	307
	1	69	19
	2	226	50
	3	159	369
	5	100	181
	6	10	216
	9	59	317
	10	229	288
	11	110	109
	12	191	17
	13	9	357
	15	195	215
	16	23	106
	18	190	242
	19	35	180
	20	239	330
	21	31	346
	22	1	1
	23	0	0
1	0	2	76
	2	239	76
	3	117	73
	4	124	288
	5	71	144
	7	222	331
	8	104	331
	9	173	178
	11	220	295
	12	102	342
	14	109	217
	15	132	99
	16	142	354
	17	155	114
	19	255	331
	21	28	112
	22	0	0
	23	0	0
	24	0	0

QUESTIONS?





THANK YOU
FOR YOUR
ATTENTION