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Master's Degree in Electronic Engineering

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Analysis and design of a high efficiency PV-fed battery charger with soft-switching tracking and MPPT control

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Abstract

The flourishing development and the increasing interest in renewable energy sources need to investigate new approaches to convert and distribute power in a highly efficient way. In line with this objective, this work presents the analysis, design, and PCB implementation of a novel topology of resonant low-voltage battery charger fed by a 48-cell photovoltaic (PV) module. The work aims to go beyond the existing research about PV-fed low-voltage battery chargers, by proposing a new solution from both the topological and control points of view.

The power converter designed in this work consists in a single DC-DC stage, frequency-modulated battery charger that exploits both topological and control-based solutions to achieve Zero-Voltage Switching (ZVS) and Zero-Current Switching (ZCS) of the converter MOSFETs. An ad-hoc control algorithm is designed to real-time track the soft-switching condition in almost any irradiance and battery voltage operation. The control is based on the acquisition of a single voltage at every switching cycle to update the timing scheme of the MOSFETs gate drivers. In parallel, the implemented frequency modulation technique allows to track the absolute maximum power point (MPP) of the PV module under various uniform-irradiance conditions, thanks to a Perturb & Observe approach. The topology improves the conversion efficiency of an already existing constant-power battery charger, in addition including the novel soft switching-tracking control and MPPT, absent in the original converter. With the goal of comparing different solutions to achieve the highest efficiency, two topologies are considered, differing in the inductance value of the resonant inductor (exploited to assist the soft switching) and in the nature of the output filter (inductive and capacitive).

In a first phase, the two topologies were analysed in *Matlab* and *PLECS* environments to derive the ideal voltage/current waveforms within a switching cycle, and mathematical models were developed to describe the static characteristics at stationary operation.

In a second phase, the topologies were simulated in *LTSpice XVII* and *PSIM* with a preliminary components selection, to derive the overall conversion efficiency and the losses contributions from each component, with the aim to tune the definitive bill of materials. The circuits were tested in standardized conditions specified in IEC 62509: 2011 (efficiency tests for lead-acid batteries charge controllers) and EN 50530:2010 (standardized tests for conversion and MPPT efficiency for low-voltage grid microinverters, here applied to a battery charger). The simulations showed that the analysed topologies exhibit EURO efficiencies above 97%, and peak charging efficiencies around 98%.

Since the conduction losses become more impactful at large operating powers for the larger resonant inductance topology, the other battery charger was selected to realize a 100 W PCB prototype. This work proposes the design procedure for the components selection and illustrates the PCB layout design in *Altium* environment. The PCB prototype is intended to be tested in laboratory to validate the expected performances. The experimental results are meant to be put in relation to the simulations and with the performances of existing topologies analysed in the literature review.

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Chapter 1

Introduction

Among the 17 Goals of the 2030 Agenda for Sustainable Development, Goal 7 ("Ensure access to affordable, reliable, sustainable and modern energy for all") explicitly addresses the need to move towards more sustainable energy targets that should be affordable for anyone. The ultimate goal is the reduction of greenhouse gas emissions associated to the actual carbon-dependent human activities, with the aim of keeping the temperature increase well below the 2 °C with respect to pre-industrial levels, by 2030. SDG7 is in turns subdivided into targets, ranging from the universal access to affordable and modern energy services to the increase of share of renewable energies in the countries energy mix, from the improvement of energy efficiency to the promotion of investments in research and technologies related to clean energy[1]. Key point of this goal, but more in general of the recommendations for an incisive climate action, is the massive adoption of energy systems based on Renewable Energy Sources (RES) and the necessity to optimize the efficiency in their conversion and utilization.

The *Sustainable Development Goals Report 2022* of the United Nations reveals that, although the access to electricity has risen from 83% to 91% between 2010 and 2020, the share of RES in the electricity sector is still confined around 25%. A negligible progress in the share of RES in the heat generation and transport sectors is outlined from 2010 and 2019 [1].

In the electricity production sector, beside the spread of RES to compensate for traditional fossil fuels, it is important to provide an infrastructure to effectively convert and distribute energy. As known, one of the main differences with carbon-based sources is the intrinsic variability of the nature of the renewable source: irradiance scenario, wind speed, ocean tidal movements. This intrinsic feature requires power converters, responsible for the conversion of energy, to

[1] `https://sdgs.un.org/goals/goal7` (accessed on 8/10/22).

effectively adapt to the source in different operating conditions, while maintaining a high conversion efficiency. This is the case, for instance, of photovoltaic (PV) generators, requiring dedicated power converters to track in any irradiance scenario the maximum operating point of the source (the so called *Maximum Power Point Trackers*, or MPPT).

More in general, the targets of the Sustainable Development Goals require an overall improvement of the current energy systems in terms of conversion efficiency. The design and implementation of high efficiency systems enables a more responsible exploitation of the limited resources at our availability. Many contributions, from large-scale massive investments and policies, to small-scale actions, can be given to address this critical point. This work in intended to provide a research contribution in perspective of the spread of high efficiency power converters to be used as interface with PV sources.

1.1 Organization of the work and method

This work aims to explore the current state of the art of power electronic converters for photovoltaic applications, in order to outline the main challenges and performance indicators associated to this field. Specifically, the original target of this work was to explore and propose an innovative solution in the field of solar microinverters, DC-AC converters designed to convert energy from a single PV panel to the low voltage grid.

The cumulative installed capacity of PV plants have grown exponentially in the last years, increasing from 40 GW in 2010 to 770 GW in 2020[2]. In this trend, the so-called *micro-PV* is acquiring more and more commercial relevance thanks to the decreasing cost of PV panels. A spread diffusion of roof-top PV panels endowed with smart microinverters could contribute to enhance the feasibility of smart grids infrastructures. These are based on the automated balance of energy supply and demand through an integrated infrastructure of storage systems, demand feedback, distributed sensors and controllers [2]. The increasing interest in solar microinverters pushes the research towards the development of high efficiency, cost effective and high power-density power converters.

A literature review of the current state of the art is proposed at the beginning of this work, with the aim of outlining the main solutions (from both topological and control points of view) in this field. A set of performance parameters must be identified to allow a comparison between various solutions. Among these:

[2] `https://www.statista.com/statistics/280220/` (accessed on 10/09/22).

- the behaviour of the conversion efficiency under various power operations;
- the extension of the input voltage range, taken as a performance parameter to evaluate the effectiveness of the MPPT;
- the number of conversion stages and components, indicators of the power density of the proposed solutions.

The analysis of the state of the art solutions considered a top-level classification into resonant and non-resonant converters, and a lower-level categorization between single- and dual-stage converters (already present in other literature reviews, like in [3]). The goal of this classification was to outline design trends, and eventually identifying a dominant design in this field. A large attention is devoted to resonant solutions, based on the inclusion of inductor-capacitor energy tanks. Thanks to their possibility to shape the voltages or currents in the circuit to enable the soft switching of the power semiconductor devices, they are appointed as promising solutions to achieve high conversion efficiencies. A theoretical framework is provided in this work to enlighten perks and disadvantages of resonant converters. The literature highlighted that peak efficiencies of 98% are already achievable targets, thanks to a wise combination of technological, topological and control features.

The main technological revolution adopted in some works is the integration of Wide Band-Gap (WBG) devices such as SiC MOSFETs and GaN FETs, to reduce both the conduction and switching losses of the power switches. The still high cost of these devices is, in some cases, justified by the significant improvement of efficiency.

From the topological point of view, the main challenge is to provide a sufficiently high step-up ratio, to adjust the PV panel voltage to the DC-link voltage required by the DC-AC inverting stage. Several solutions have been developed to overcome the traditional Pulse-Width Modulated (PWM) boost topology, such as the inclusion of a transformer or of switched capacitor networks.

From the control point of view, finally, the main requirement is to adjust the voltage gain of the DC-DC stage according the MPPT scheme. The control variable must be selected according to the specific features of the converter topology, in order not to lose the benefits it is designed for: in dual-stage resonant converters, for instance, the resonant stage is usually operated at the resonance frequency, to realize a soft switching condition and operate the stage at the maximum efficiency.

In perspective of giving a more general view on high-efficiency solar-fed power converters, also battery chargers were included in the literature review. Also in this case, the goal was to classify multiple converter solutions on the basis of the number of stages, and on the presence or absence of resonant elements. New performance parameters needed to be identified to establish a comparison, such as:

- the charging efficiency, defined as the efficiency behaviour during the charging process;
- the filtering effort required at the output to ensure a smooth charging current;
- once again, the number of stages and components, indicator of the power density of the converter.

Especially in the application field of low-voltage (12 V) battery chargers, the literature review revealed multiple possible ways of innovation. Here, a dominant design class seems to emerge: single-stage, quasi-resonant converters. The low load voltage requirement and the relatively small voltage gap between input and output sides (few tens of volts) discourages the design of isolated or multiple-stage converters. Many of the solutions proposed in literature are buck-derived quasi-resonant topologies. These consist in improvements of the original topology obtained by including resonating/quasi-resonating elements to enable the soft switching of the main power switch. However, these solutions always refer to constant DC voltage sources.

A single topology was found to be explicitly addressed for PV sources. This converter, however, relies on a dual-stage topology in which the first DC-DC stage is a conventional boost, resulting in a limited peak efficiency around 92%.

The last battery charger considered in the literature review, originally meant to be fed from the grid, reveals interesting aspects, like the single-stage scheme, the presence of a small inductor to assist the Zero-Voltage switching of the main MOSFETs, and the intrinsic power limitation. This converter topology, achieving a relatively low peak efficiency (88%) is taken as starting point for the development of a novel high efficiency battery charger.

The work provides a detailed analysis of two modified topologies in which the galvanic isolation is removed, not necessary for this application, and the passive rectifier is substituted by an active one. The converters are intended, from the beginning, to be interfaced with a 48-cells PV panel, which exhibits a suited voltage-current characteristic compliant with the load and converter requirements.

All the components of the new topologies need to be re-designed, considering the new voltage and current ratings set by the source. This work goes beyond the original converter also proposing two innovating control features:

1. in the original converter, the Zero-Voltage Switching of the converter MOSFETs is enabled by the presence of a small inductance. In this work, instead, due to the need to operate at different powers according to the irradiance scenario, a combination of a topological element (the small inductance) and of a real-time control is designed to track the ZVS condition adapting to the working point.

The control acts on the half-bridge deadtime to ensure that the MOSFETs turn ON at zero voltage;

2. the possibility to track the maximum power point of the PV panel is also included in this work. After a review of the state of the art MPPT schemes presented in Chap.2.3.3, an adaptive Perturb & Observe control is designed and tested in *Simulink*[3] environment.

A detailed mathematical description is given for both the topologies. For each one, the behaviour of the meaningful converter voltages and currents is analysed, after splitting the switching period into operating modes. In each mode, the state equations are set and solved under proper general assumptions and by recurring to approximations to derive analytic solutions.

To complete the mathematical description, the static characteristic is analysed in both the topologies for an ideal DC voltage source. This work proposes equivalent circuit models to numerically or analytically derive the dependence of the output power to the switching frequency. Also, the models consider the presence of different operating regions, according to the switching frequency. The models are then validated in simulations.

Conceptually, the second analysed converter, endowed with a larger and single inductor, was developed to provide possible solutions to the limitations of the first one:

- the limited time window for the ZVS tracking controller;
- the presence of two inductors, possibly causing a significant power loss;
- the dependence of the monotonicity of the static characteristic to the irradiance scenario.

The comparison of the two converters is carried out in Chap.6. The converters are analysed on the basis of *LTSpice XVII*[4] and *PSIM*[5] simulations, adopting models of real components, to evaluate in a more accurate way the performances in presence of parasitic elements. The operating conditions are set according to standardized tests, to allow a more coherent comparison with existing topologies adopting common performance indicators. The simulations have the ultimate goals of validating the mathematical description, evaluating the conversion efficiency

[3] `https://it.mathworks.com/products.html?s_tid=gn_ps`.

[4] `https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html`.

[5] `https://powersimtech.com/products/psim/capabilities-applications/`.

under various operating conditions, and proving the effectiveness of the designed controls. Moreover, the evaluation of the share of losses for each component allows to tune the physical design and the definitive components selection. The first charger topology, promising a larger efficiency at higher powers, was then selected for a PCB prototype development.

The last part of this work concerns the physical design of a 100 W PCB prototype. The design criteria are specified for each of the main components of the circuit, and the description of the main PCB layout choices is provided. This work is meant to proceed in a PhD project at Politecnico di Torino, where the design will be validated through experimental tests. The testing phase will be necessary to validate the design, by measuring the expected performances in terms of conversion efficiency, effectiveness and reliability of the ZVS/ZCS tracking control and MPPT control. The experimental results will be put in relation with the performances of existing topologies analysed in the literature review.

For this work, the following pieces of software were adopted and exploited for different purposes:

- MathWorks *Matlab/Simulink* 2022a[6], an integrated programming and numeric computing environment, was exploited for the definition and solution of the mathematical description of the converters. Moreover, *Simulink* environment was used in combination with *PSIM* to host the control part of the converters, realized as state machines;

- Plexim *PLECS* 4.6.4[7] provides a graphical and intuitive modelling and simulation environment for power electronic systems. It was exploited in this work to prove the ideal behaviour of the converter topologies;

- Analog Devices *LTspice XVII*[8] was exploited as reference simulation tool to test the converters under static operating conditions. The possibility to include models of real components allows to evaluate the impact of non-idealities on the converter performances. However, this tool is not optimized to design and test complex control schemes, hence the need to move to another simulations environment;

[6] `https://it.mathworks.com/products.html?s_tid=gn_ps`.

[7] `https://www.plexim.com/products/plecs`.

[8] `https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html`.

- Powersim *PSIM* 2021b[9], thanks to the possibility to integrate SPICE models in the power circuit, and to be coupled to a *Simulink* control architecture, was identified as the most suitable environment where to simulate the converters behaviour under time-varying operating conditions, namely irradiance values. The integrated *PSIM/Simulink* environment provides a powerful tool to develop control and power designs in parallel, combining the characteristic functionalities of the two pieces of software;
- *Altium Designer*[10], finally, was exploited for the PCB schematic and layout design, in perspective of the physical implementation of a prototype. The unique environment allows an intuitive and immediate communication between schematic and layout views.

[9] `https://powersimtech.com/products/psim/capabilities-applications/`.

[10] `https://www.altium.com/it/altium-designer`.

Chapter 2

PV sources modelling and resonant power converters

2.1 PV panels models

In the present work, one of the leading features of the proposed power converter design is the possibility to be interfaced to a photovoltaic (PV) module, as power source of the charger. As it will be explained in the following sections, the PV panel interface is an innovative feature with respect to the originary power converter topology on which the current one is based.

The optimization of the converter design to interface PV modules needs to consider at least two fundamental limitations when compared to ideal, constant DC voltage sources:

- the current-voltage characteristic of a PV source (cell, module, or array) is strongly dependent on environmental conditions, mainly irradiance (expressed as the flux of solar radiant power per unit area) and temperature. The series connection of cells, moreover, makes the IV curve to depend on the possibly non-uniform distribution of irradiance on the module surface. Details on the influence of this phenomenon and the consequent limitations on the PV characteristic will be given in the following section;
- the power-voltage curve, analysed through the generator convention (positive power when the power flows from the PV source to the load) is strongly non-linear and exhibits, according to the irradiance condition and to the presence or absence of antiparallel bypass diodes, one or more local maxima. The global maximum is called *Maximum Power Point* and denoted by *MPP*.

The latter characteristic implies the simultaneous achievement of two conditions in order to work at the rated power reported on commercial PV modules datasheets. The rated power is indeed referred to an operation at the so-called Standard Temperature Conditions, consisting in 1,000 W/m^2 irradiance, 25 °C cell temperature and AM 1.5 air-mass solar spectral distribution [4]. To achieve the rated power, the irradiance condition should be uniform and nominal (1,000 W/m^2); moreover, the load must be matched, meaning that its load curve must intersect the IV curve of the PV panel in the Maximum Power Point (MPP) [5].

Fig.2.1 shows a typical output characteristic under uniform irradiance condition of a monocrystalline Silicon (mc-Si) PV cell. Independently from the technology and from the cell surface, the IV characteristic always exhibits key nodes used to characterize it:

- the short circuit current I_{SC}, identifying the current that the cell can provide when its terminals are short-circuited. This parameter is mainly dependent on the irradiance and, in a minor part, on the temperature;
- the open circuit voltage V_{OC}, the voltage that appears at the cell terminals in absence of external load. This voltage value is affected in a minor part by irradiance changes, and, more significantly, by temperature changes;
- the MPP, representing the working condition in which the maximum power can be extracted. The values of current and voltage associated to this working condition, usually denoted with I_{MPP} and V_{MPP}, are themselves dependent on technology, irradiance and temperature.

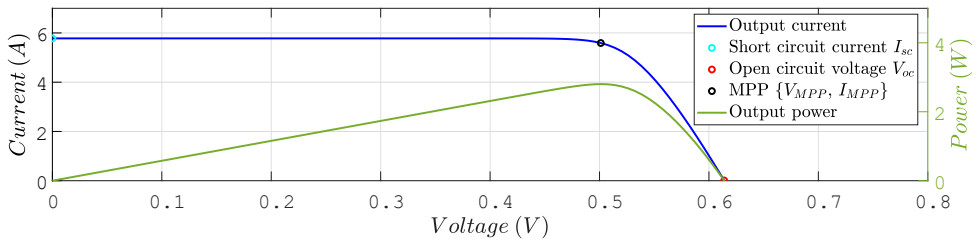


Figure 2.1: Typical I-V and P-V characteristic of a monocrystalline silicon cell.

It is important to observe that Fig.2.1 only reports the output characteristic in the first I-V/P-V plane quadrant, associated to a positive power flow from the photovoltaic generator. The second and fourth quadrants, in which the panel/cell works as a passive device, are obviously of no interest for this work. The third

quadrant does not include any working points.

To reproduce the characteristic shape of the PV cells/modules IV-curve and its dependence on environmental conditions, a proper parametrized electrical model must be adopted in the simulations. Due to the semiconductor p-n junction-based structure of a PV cell (even though more sophisticated technologies adopt hetero-junction structures), it is reasonable that the basic electrical model should be diode-based. The series connection of multiple cells, as explained later, represents a "scaled" version of the single cell in its output characteristic, and thus can be modelled by recurring to the same approach developed for the single cell.

The most common models adopted in the literature to fit to the experimental IV curves are composed of the following elements:

- an irradiance-dependent current source $I_{\mathrm{ph}}(G)$, modelling the drift current flow due to the photovoltaic effect;
- an antiparallel diode (in more sophisticated models, two or three are also considered, like in [5];
- a parallel resistance R_{sh};
- a series resistance R_s.

To improve the fitting, sometimes a non-linear conductance is considered [5] in parallel to the current generator and diodes. In the present work, a single diode model (SDM) is considered to fit the IV curve of a commercial 48-cells PV panel from Solar Innova[1]. As the following sections will highlight, 48-cells modules were considered because of the intrinsic input voltage limitations of the proposed battery charger, whose correct functioning is not compliant with the typical open circuit voltage of PV panels with 36 cells or less. Fig. 2.2 shows the single diode equivalent circuit adopted in this work.

[1] `https://www.solarinnova.net/` (accessed on 19/09/22).

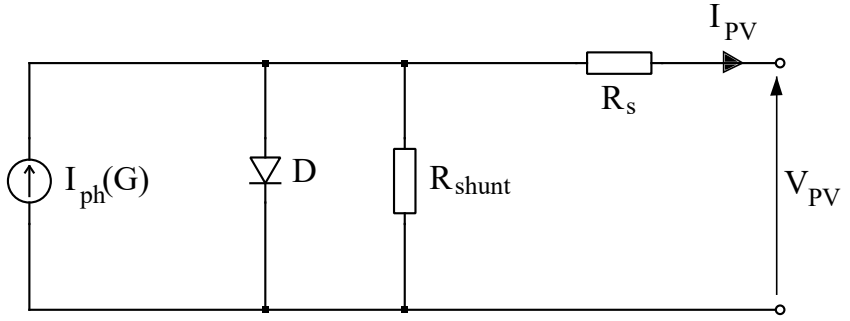


Figure 2.2: Single diode equivalent circuit for a PV panel.

The output characteristic, according to this equivalent model, can be described by the following implicit equation [6], corresponding to the Kirchhoff Current Law applied at one of the two components' common nodes:

$$I_{\mathrm{PV}} = I_{\mathrm{ph}} - I_0\left(e^{\frac{q(V_{\mathrm{PV}}+R_{\mathrm{s}}I_{\mathrm{PV}})}{N_{\mathrm{s}}\eta K_{\mathrm{B}}T}} - 1\right) - \frac{V_{\mathrm{PV}} + R_{\mathrm{s}}I_{\mathrm{PV}}}{R_{\mathrm{shunt}}}\,, \tag{2.1}$$

where N_{s} is the number of series-connected cells, K_{B} is the Boltzmann's constant and q is the elementary electron charge.

Apart from the variables of interest for the output characteristic plot (I_{PV} and V_{PV}), Eq.2.1 contains 5 unknowns: the photovoltaic current I_{ph}, the inverse saturation current of the diode I_0, the diode ideality factor η, and the previously mentioned series and parallel resistances R_s and R_{shunt}, which needs five equations to be determined. Since the equivalent model should fit as accurately as possible to the experimental behavior which is declared on a panel datasheet, the selection of the equations should establish a clear link between the mathematical model and the physical device. To do so, the experimental IV-curve available on the datasheet, is exploited to derive key nodes and to set the initial guesses for the solution of the non-linear system. The reference experimental data from which the model parameters usually refer to the STC.

Multiple possibilities have been developed in the literature to define the set of equations. In this work, the approach suggested in [6] has been adopted, where the non-linear system is defined through the following criteria:

1. the first equation is derived by interpolating the output characteristic at the experimental short-circuit working condition (at STC);

2. a second equation is obtained from the interpolation of the characteristic at the open-circuit node (always at STC);

3. a third equation is obtained from the interpolation at the absolute MPP (always at STC);

4. the fourth equation exploits the fact that, at the MPP, the power-voltage characteristic exhibits null derivative. Equivalently, this condition can also be rearranged and expressed in the following terms:

$$\left.\frac{dI_{\mathrm{PV}}}{dV_{\mathrm{PV}}}\right|_{\mathrm{MPP}} = -\frac{I_{\mathrm{MPP}}}{V_{\mathrm{MPP}}}\,; \tag{2.2}$$

5. the fifth constraint results by equating the area underlying the IV experimental characteristic (computed through a trapezoidal integral through N nodes) and the trapezoidal integral (through the same N nodes) of the curve described by the non-linear characteristic. Fig.2.3 shows an example of partition into equally wide sections of the mentioned area for the computation of the trapezoid integral.

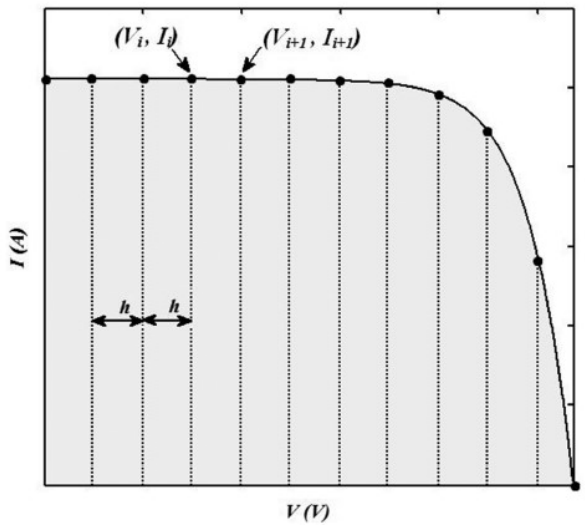


Figure 2.3: Partition into N equally h-wide sections of the area below the experimental IV curve (from [6]).

Summarizing, the non-linear system of equations becomes:

$$\begin{cases} I_{\mathrm{SC}} = I_{\mathrm{ph}} - I_0\left(e^{\frac{qI_{\mathrm{SC}}Rs}{N_{\mathrm{s}}\eta K_{\mathrm{B}}T}} - 1\right) - \dfrac{R_{\mathrm{s}}I_{\mathrm{SC}}}{R_{\mathrm{shunt}}} \\ 0 = I_{\mathrm{ph}} - I_0\left(e^{\frac{qV_{\mathrm{OC}}}{N_{\mathrm{s}}\eta K_{\mathrm{B}}T}} - 1\right) - \dfrac{V_{\mathrm{OC}}}{R_{\mathrm{shunt}}} \\ I_{\mathrm{MPP}} = I_{\mathrm{ph}} - I_0\left(e^{\frac{q(V_{\mathrm{MPP}}+I_{\mathrm{MPP}}R_{\mathrm{s}})}{N_{\mathrm{s}}\eta K_{\mathrm{B}}T}} - 1\right) - \dfrac{V_{\mathrm{MPP}}+R_{\mathrm{s}}I_{\mathrm{MPP}}}{R_{\mathrm{shunt}}} \\ I_{\mathrm{MPP}} = (V_{\mathrm{MPP}} - R_{\mathrm{s}}I_{\mathrm{MPP}})\left(\dfrac{qI_0}{N_{\mathrm{s}}\eta K_{\mathrm{B}}T}e^{\frac{q(V_{\mathrm{MPP}}+I_{\mathrm{MPP}}Rs)}{N_{\mathrm{s}}\eta K_{\mathrm{B}}T}} + \dfrac{1}{R_{\mathrm{shunt}}}\right) \\ h\sum_{i=0}^{N} I_i = h\sum_{i=0}^{N}\left(I_{\mathrm{ph}} - I_0\left(e^{\frac{q(V_i+RsI_i}{N_{\mathrm{s}}\eta K_{\mathrm{B}}T}} - 1\right) - \dfrac{V_i+R_{\mathrm{s}}I_i}{R_{\mathrm{shunt}}}\right) \end{cases} . \tag{2.3}$$

In the last equation, I_i and V_i represent the set of experimental currents and voltages derived from the datasheet of the module.

The non linear system can be solved numerically in *Matlab* by the *fsolve* function, which exploits the Newton-Raphson method to iteratively search for the solution starting from an initial guess. This is another crucial part of the approach, because a proper choice of initial values improves the convergence of the algorithm. In this work, the selection of the initial guesses follows the here described approach.

First of all, the series and shunt resistances of the equivalent circuit in Fig.2.2 can be estimated, in the first instance, by the inverse of the gradient of the IV-curve at the open-circuit and short-circuit point, respectively.

$$\begin{cases} \left(-\dfrac{dV_{\mathrm{PV}}}{dI_{\mathrm{PV}}}\right)_{\mathrm{OC}} = R_{\mathrm{OC}} \approx R_{\mathrm{s},0} \\ \left(-\dfrac{dV_{\mathrm{PV}}}{dI_{\mathrm{PV}}}\right)_{\mathrm{SC}} = R_{\mathrm{SC}} \approx R_{\mathrm{shunt},0} \end{cases} . \tag{2.4}$$

The first guess of ideality factor η, in this work, is approximated by imposing the equality between the ratio of the non-linear characteristic equation evaluated at the open circuit and MPP working conditions, in order to be able to express η as a function of the previously derived series and shunt resistances (first guesses). If, in this equation, I_{ph} is approximated by I_{SC} and the contribution of I_0 is neglected, the expression becomes independent from these not-yet-defined initial guesses.

$$\eta_0 = \frac{V_{\mathrm{OC}} - V_{\mathrm{MPP}} - R_{\mathrm{s},0}I_{\mathrm{MPP}}}{\frac{K_{\mathrm{B}}TN_{\mathrm{s}}}{q}\log\left(\frac{V_{\mathrm{OC}}-R_{\mathrm{shunt},0}I_{\mathrm{SC}}}{R_{\mathrm{shunt},0}(I_{\mathrm{MPP}}-I_{\mathrm{SC}})+V_{\mathrm{MPP}}+R_{\mathrm{s},0}I_{\mathrm{MPP}}}\right)} . \tag{2.5}$$

The last two initial guesses, $I_{0,0}$ and $I_{\mathrm{ph},0}$, can be derived by interpolating the output characteristic at the short circuit and open circuit working points, respectively [6]):

$$\begin{cases} I_{0,0} = \dfrac{I_{\mathrm{SC}} - \frac{V_{\mathrm{OC}}}{R_{\mathrm{shunt},0}} + \frac{R_{\mathrm{s},0}}{R_{\mathrm{shunt},0}} I_{\mathrm{SC}}}{e^{\frac{V_{\mathrm{OC}}}{\eta N_{\mathrm{s}} V_{\mathrm{th}}}} - e^{\frac{R_{\mathrm{s},0} I_{\mathrm{SC}}}{\eta N_{\mathrm{s}} V_{\mathrm{th}}}}} \\ I_{\mathrm{ph},0} = I_{0,0}\left(e^{\frac{V_{\mathrm{OC}}}{\eta N_{\mathrm{s}} V_{\mathrm{th}}}} - 1\right) + \dfrac{V_{\mathrm{OC}}}{R_{\mathrm{shunt},0}} \end{cases} , \tag{2.6}$$

where V_{th} represents the thermal voltage at the standard 25 °C cell temperature:

$$V_{\mathrm{th}} = \frac{K_{\mathrm{B}} T}{q} \approx 26\,\mathrm{mV}\,. \tag{2.7}$$

The *Matlab* function for the definition of the non-linear system describing the approach adopted to derive the single diode model parameters is reported in Appendix A (A.2).

Once the parameters of the equivalent circuit model were extracted, Eq.2.1 was numerically solved through the Newton-Raphson method, to derive the array of output currents starting from a pre-defined set of equally-spaced voltages (from 0 V to V_{OC}). Due to the non-linearity of the system and to the approximations in the algorithm, it was necessary to perform an *a-posteriori* tuning of at least one of the initial guesses, to improve the convergence of the Newton-Raphson method exploited by *Matlab*. The criterion adopted in this phase was to tune the initial guess or the series resistance, whose value is determinant in providing the quality of the fitting of the numerical curve to the larger voltage nodes of the experimental IV-curve. Since, as the following section will describe, the proposed power converter topology can work effectively only when the output voltage of the PV module is larger than V_{MPP}, the aim of the $R_{\mathrm{s},0}$ tuning was to minimize the Root-Mean-Square Error (RMSE) related to the fitting of the nodes with $V_{\mathrm{PV}} > V_{\mathrm{MPP}}$, where the RMSE is defined as:

$$RMSE = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(I_{\mathrm{num,i}} - I_{\mathrm{exp,i}})^2}\,. \tag{2.8}$$

A larger deviation of the numerical curve for $V_{\mathrm{PV}} < V_{\mathrm{MPP}}$ was considered acceptable for the purpose of this work. Tab.2.1 reports the comparison between the initial guesses of the single-diode model parameters and the solutions of the non-linear system in Eq.2.3.

With the obtained values, the computed RMSE in the mentioned interval is around 0.236. Fig.2.4 underlines a good agreement of the numerically-computed and experimental IV-curves.

Parameter	Initial guess	After optimization
R_s	$0.62\,\Omega$	$0.531\,\Omega$
R_{shunt}	$300\,\Omega$	$1.83\times10^{10}\,\Omega$
η	0.427	0.588
I_0	2.18×10^{-24} A	1.59×10^{-17} A
I_{ph}	5.792 A	5.779 A

Table 2.1: Five parameters of the single diode model before and after the numerical algorithm.

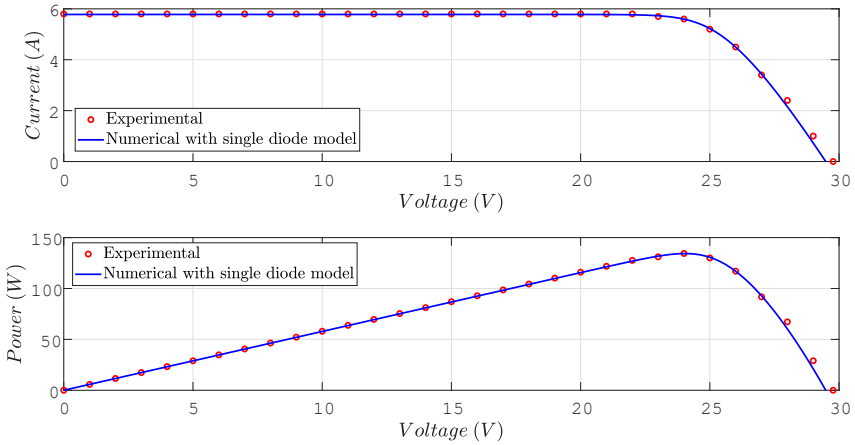


Figure 2.4: Comparison between experimental and numerically computed IV-curve with the proposed single diode model.

Tab.2.1 shows a considerable deviation of the parallel resistor (8 orders of magnitude) and of the diode inverse saturation current (7 orders of magnitude) with respect to the initial guesses. This phenomenon can be explained by observing that the experimental IV-curve is significantly flat around the short-circuit operating point: as a result, the single-diode model nearly collapses into an ideal current generator model (large parallel resistor, negligible contribution of the diode for low forward voltages). The adopted model can well reproduce the behavior of the experimental IV-curve around the global MPP: at V_{MPP}, the experimental and numerical values of I_{MPP} are, respectively, 5.52 A and 5.46 A (around 1% deviation). Lst.A.3 in Appendix A reports the complete *Matlab* code implementing the described algorithm.

2.2 MPPT and partial shading conditions

As mentioned, PV sources differ from ideal constant-voltage or constant-current sources for specific features, such as the strong dependence on environmental conditions, mainly temperature and irradiance. The analysis of the dependence of the electrical characteristic to those conditions is necessary in order to predict how the power capacity of the source varies will vary during a typical working day. In some application fields, like grid interface from PV panels/plants, the knowledge of the IV-characteristic dynamics is required since the design phase, because the power converter should be optimized to exhibit a large efficiency on a reasonable range of operating points.

Due to the significant dependence of the photovoltaic current from the irradiance, the literature, and the practical solutions, mostly focus on the decrease of performances when the irradiance is not the nominal one (at STC). To increase the power capability of a PV module from low-power solar cells, these are typically connected in series, to obtain increased output voltages which are compliant with a variety of load requirements. The main drawback of series-connection of solar cells, however, is that the total current of the module is determined by the lowest current. If the cells are assumed to be identical but subjected to different irradiance conditions (the so-called *partial shading condition*, or PSC), the global current will be limited by the lowest irradiance condition, which, of course, keeps from working in the optimal condition for the module. Moreover, since unshaded cells that conduct a low current would work near their maximum voltage V_{OC}, a negative overvoltage may occur across the shaded cells, possibly leading to the junction breakdown or the generation of hot-spots.

For these reasons, all PV panels exhibit two or more bypass diodes in anti-parallel connection with a group of series-connected cells. When part of the module is partially or totally shaded, instead of imposing its decreased current (related to the low level of irradiance), the bypass diodes may instead enter in conduction to sustain the nominal, high-irradiance current generated by the unshaded cells. In this way, overvoltages across the shaded cells are avoided until the diode keeps conducting [5, 7].

The presence of bypass diodes, however, modifies the electrical characteristic of the module, by leading to the generation of multiple local peaks of power in the P-V curve. A possible way to analyse this behavior is to apply a swept DC-voltage on a partially shaded PV module to construct, point by point, the modified electrical characteristic. Let's consider, as a simplified case, a 36-cells module endowed with two bypass diodes (each one in antiparallel connection with 18 cells). If half of the cells are fully lighted (nominal 1,000 $\mathrm{W/m^2}$ irradiance), and the other half only

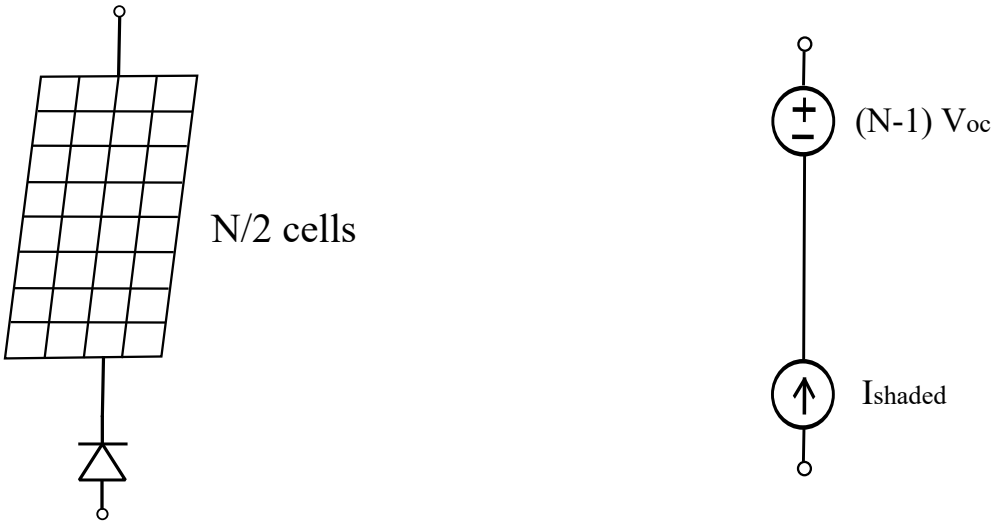
partially ($400\,\mathrm{W/m^2}$), the IV-characteristic exhibits two distinct operating regions as the panel voltage increases [5]:

- at low load voltages, the bypass diode of the shaded cells conducts and carries the nominal current imposed by the series of the nominally-lighted cells. As a result, the IV-characteristic of the unshaded cells is dominant in determining the global behaviour. Moreover, the characteristic in this region is independent from the partial shading scenario (percentage of shaded cells and irradiance value). The equivalent circuit describing this operation is shown in Fig.2.5a;

- after a certain load voltage value, which can be estimated by recurring to a model-based approach [7], the diode becomes reverse-biased. From this voltage on, the characteristic drastically diverges and becomes strictly dependent on the number and the irradiance of the shaded cells. The shaded cells can be modelled by irradiance-dependent current sources, whereas the unshaded cells, forced to conduct a lower current, can be approximately modelled by constant DC voltage sources in series. Fig.2.5b shows an example where a single cell is shaded and $N-1$ are subjected by the same, nominal irradiance. In this second operating region, the P-V characteristic exhibits a second local maximum, whose position and value depends on the partial shading scenario. In [5], a semi-analytical model based on two empirical coefficients is adopted to estimate the V_{MPP}.

The description can be generalized to modules with N bypass diodes: in this case, according to the partial shading scenario, the P-V characteristic will exhibit N local maxima. The position of the global maximum power point (GMPP) depends on the single values of irradiance and on the technology of the module. Fig.2.6 shows an example of I-V and P-V characteristic for a partially shaded Polycrystalline Silicon module endowed with 3 bypass diodes.

The presence of multiple peaks is critical for the algorithm of Maximum Power Point Tracking because may converge to a solution which is not globally the optimal one. Some of the MPPT algorithms, such as Hill-climbing (HC) or the derived Perturb & Observe (P&O) or Incremental Conductance (InC) are based on progressively incrementing the control variable of a circuit until a local maximum is reached [8]. These conventional techniques, despite the simple implementation, are not optimized to distinguish if the encountered maximum is also the global one. This is why more sophisticated techniques have been developed, based on Artificial Intelligence (AI) or the so-called Biologically-Inspired (such as Ant-Colony, Grey-Wolf, Particle-Sworm optimization schemes). In alternative, hybrid schemes can be designed by combining two techniques, to overcome the limitations of



(a) Equivalent circuit in the first operating region.

(b) Equivalent circuit in the second operating region.

Figure 2.5: Equivalent circuits of the partially shaded PV module in the two operating regions.

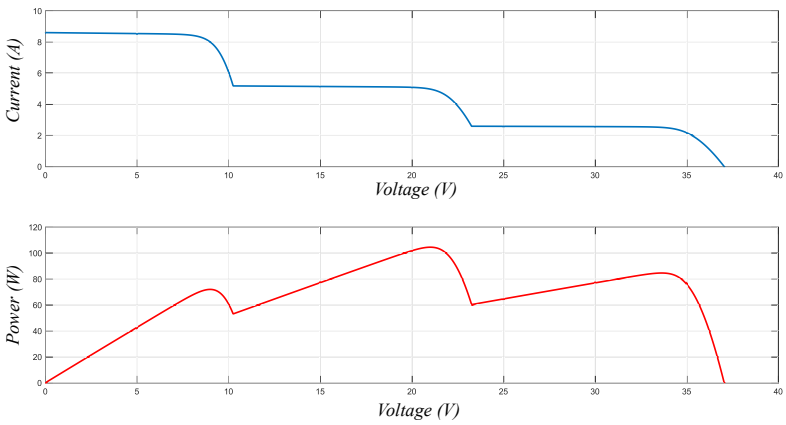


Figure 2.6: Example of I-V and P-V characteristics for a partially-shaded PV module with 3 bypass diodes.

the HC approach. The main goal is to exploit the auxiliary technique to primarily estimate the position of the global maximum, and then adopt the HC

algorithm to converge to the solution. In some cases, some solutions exploit, for the estimation of the GMPP, irradiance sensors distributed along the module surface [8].

The last remark is that the dynamics of the electrical characteristic with varying environmental conditions also depends on the technology of the cells. In [9], the experimental analysis of different modules (in Monocrystalline Silicon, Polycrystalline Silicon and Amorphous Silicon) is carried out to compare how the P-V curve varies in presence of partial shading scenarios. The main finding of the work is that the lower curvature of the I-V characteristic of Amorphous Silicon modules helps the MPPT algorithm to:

- increase the tracking efficiency (the probability for the MPPT algorithm to reach the GMPP) independently on the MPPT scheme;
- reduce the tracking time (time required to lock the maximum) independently on the MPPT scheme.

2.3 Resonant power converters

In the previous sections, the PV sources were described in their main features and issues. The presented discussion was necessary to outline the distinctive characteristics of a PV source, but, from this moment on, this work will focus on the power conversion stage meant to interface with it. The starting point of the following analysis is the need for high-efficiency power converters, which can deliver power to the desired load in a reliable and effective way. The combination of a PV source and of a high-efficiency converter, indeed, provides a sustainable solution from both the points of view of the generation and delivery of electrical power.

Regarding the power conversion stage, resonant power converters represent a promising alternative to conventional Pulse-Width Modulated converters, thanks to their possibility to decrease the switching losses of power semiconductor devices. In this section, after the description of the soft-switching mechanism in power switches, the theoretical background behind resonant power converters is presented, including a general classification, benefits and the main issues.

2.3.1 Soft switching in power semiconductor devices

The need for reliable and safe electronic systems is also connected to the way they are supplied. Power electronic converters are designed to regulate the power transfer according to the load requirements, and this task is to be solved in a high efficient way. The advantages to design high-efficiency power converters are multiple:

- for the same output power required by a load, working with low conversion efficiency means to absorb a larger input power from the energy source, since:

$$P_{\text{in}} = \frac{P_{\text{out}}}{\eta}\,. \tag{2.9}$$

  This is especially critical for energy sources that exhibit a limited capacity (this is the case of electrochemical cells): the overall effect is to reduce the autonomy of the system. More in general, however, in perspective of environmentally sustainable systems, reducing the amount of power dissipation in the energy conversion chain ensures to responsibly exploit the energy sources;

- The amount of dissipated power is primarily associated to Joule losses: the generated heat, if not properly dissipated, may increase the system temperature above critical values for which electronic components, especially semiconductor devices, are destroyed. The adoption of heat-sinks may become necessary to solve this task, especially in presence of high power-density circuits. High efficiency conversion means to adopt lighter, smaller and cheaper heat-sinks, with direct advantages to the miniaturization of the power converter. Thermal stresses are primary sources in the failure of semiconductor power components: this is why a highly efficient conversion is also directly associated to a larger reliability.

The exploitation of semiconductor power devices operated in switching-mode has enabled the possibility to achieve significantly higher efficiencies with respect to linear power converters (such as Low Dropout regulators, LDOs). In this last category, indeed, semiconductor devices are operated in their active region to exploit their linear characteristic, but this operating region causes a significant power dissipation at the output port, due to the overlap of a non-null voltage and the conduction current. The switching mode operation allows instead to drastically reduce the dissipated power, since the conduction current is null when the switch is turned OFF, and the output voltage is nearly zero when it's turned ON. This is the main reason why switching-mode power converters have completely replaced the other class in almost any medium and high power application.

Despite the adoption of a switching operation, the power semiconductor devices, in many cases, still represent the main contribution of losses in a power converter. For all the power semiconductor devices, the main mechanisms of dissipation can be grouped into two general categories: conduction and commutation losses.

The first phenomenon is related to the Joule dissipation occurring during the conduction (ON state) of the switch. Independently on the conduction mechanism

(drift/diffusion) and on the nature of charge carriers, the power semiconductor devices always exhibit non-idealities that can be modelled in form of a non-null output voltage (diodes, BJTs or IGBTs) or resistive behaviour during conduction. In some cases, a more accurate models needs to consider a combination of the two equivalent circuit elements (diodes, BJTs and IGBTs).

The second mechanism is more complex to model and to quantify, and includes the loss mechanisms occurring during a switch commutation (from conduction to interdiction and vice-versa). The reason why some power is dissipated during commutations is that the presence of parasitic reactive components (mainly, output capacitances and leakage inductances) keeps it from being instantaneous. As a result, there are transient intervals of time in which the output current and voltage overlap between the complete conduction and interdiction. Fig.2.7 shows the qualitative behaviour of the drain-source voltage and drain current of a MOSFET during the commutation from ON-state to OFF-state (extracted from a simulation in *LTSpice* environment): the plots show the temporary overlap of a non-zero voltage and a non-zero current during the commutation.

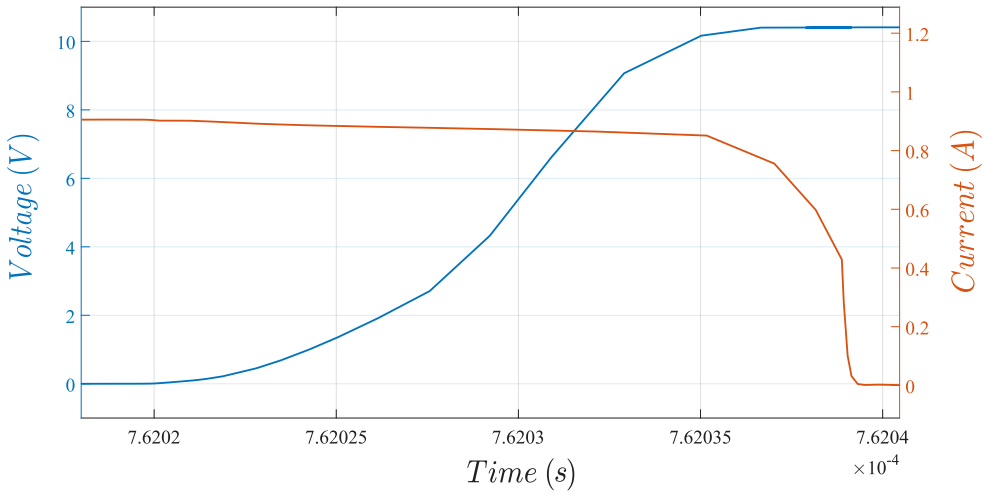


Figure 2.7: Typical voltage and current waveforms of a MOSFET during a commutation from ON-state to OFF-state.

Before proceeding, it is still necessary to clarify the distinction between the so-called hard-switching and soft-switching commutations. Conventional power converters based on pulse-width modulation (PWM) techniques are based on the modulation of the average desired output current or voltage through the instantaneous rectangular currents/voltages. To realize this operation mode, semiconductor switches are turned OFF when their conduction current is still non-null, and turned

ON when the voltage across the output port is non-null. Due to the finite non-null values of initial current/voltage and to the presence of reactive components, this commutation is typically slower and involves a temporary overlap of output current/voltage in its working points trajectory.

The soft-switching technique is, on the other hand, based on switching OFF the power semiconductor devices when its conduction current is null (Zero-Current switching) or turning it ON when its output voltage is null (Zero-Voltage switching). In this approach, the commutations result faster and the temporary overlap of current/voltage is minimised.

Fig.2.8 shows a qualitative comparison between the trajectory in the IV plane for a typical hard switching commutation compared to a soft-switching one, for a generic transistor. v_T and i_T represent, respectively, the output voltage and current. Since the dissipated power during the commutation is linked to integral of the product of instantaneous currents and voltages, it's clear that soft-switching can lead to a reduction of commutation losses.

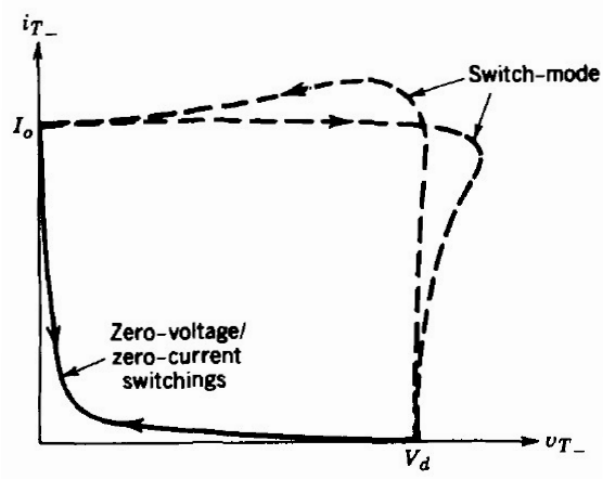


Figure 2.8: Qualitative behaviour of working points trajectories for a hard-switching and soft-switching commutation (image from [10]).

An accurate description of the switching loss mechanisms should consider the physical nature of the power semiconductor devices and is beyond the scope of this work. In this context, the following sources of commutation losses typical of hard-switching and referred to Silicon MOSFETs, are considered to explain the potential advantages in adopting resonant power converters [11]:

- the drain/source parasitic inductances induce significant voltage spikes during turn OFF, due to the steep current transient $\frac{di}{dt}$;
- the charged parasitic output capacitances, when subjected to a steep voltage transient $\frac{dv}{dt}$ during turn ON, generate current spikes;
- the reverse recovery mechanism of a MOSFET body diode, associated to the fast removal of charges from the drift layer, is another mechanism of commutation loss associated to a temporary current spike.

As a general and approximated rule, hard-switching operation leads to switching losses directly proportional to the switching frequency [12]: as a result, traditional PWM converters exhibit upper frequency limits linked to the maximum allowed losses. The need to work with lower frequencies, however, leads to increased dimensions of the filter components to reduce the switching ripple. As a consequence, reducing switching losses through soft commutation allows to increase the operating frequency, with advantages in terms of filtering effort and size.

Another important drawback of conventional PWM operation is the broadband emitted electromagnetic energy: fast and steep transitions of voltages and currents in the circuit are linked to a wideband harmonic content. Resonant converters, thanks to dedicated resonant structures, allow to decrease the voltage and current derivatives during transients, in turns resulting in lower electromagnetic interference (EMI) levels [11].

The basic idea of resonant converters is to exploit a resonating tank composed of one or more inductors and capacitors, exhibiting a large quality factor to shape some of the currents/voltages in the circuit into sinusoids or arcs of sinusoid. With a proper selection of the operating frequency, this topological structure provides the possibility to switch the power semiconductor devices in ZVS or ZCS. Since the operating frequency modifies the impedance of the LC tank, voltage or current regulation is typically achieved by adopting a frequency modulation technique.

2.3.2 Classification of resonant converters

According to the literature, there is no unique classification of resonant converters. In this work, the taxonomy provided in [10], including both DC-DC and DC-AC converters, is adopted.

1. **Load-resonant converters**: This class of DC-DC converters, in other works simply called "Resonant converters", include voltage-source and current-source converters in which a resonant tank is added in series or in parallel to the

load. Normally, these topologies include a first DC-AC stage, where the AC current/voltage is nearly sinusoidal due to the presence of the resonant tank, followed by an AC-DC rectifying stage. These converters are usually operated with a frequency modulation technique, around the resonance frequency (or resonance frequencies, in case of multiresonant tanks). The simplest topologies, including a single resonant inductor and a single resonant capacitor, are reported in Fig.2.9 and Fig.2.10.

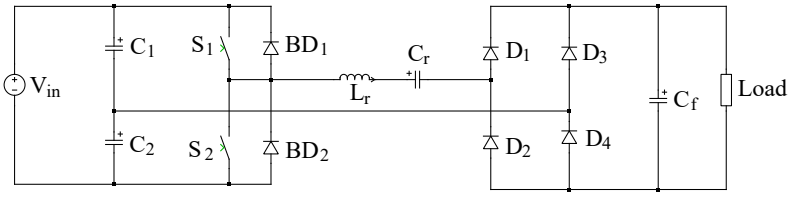


Figure 2.9: Series resonant converter (SRC).

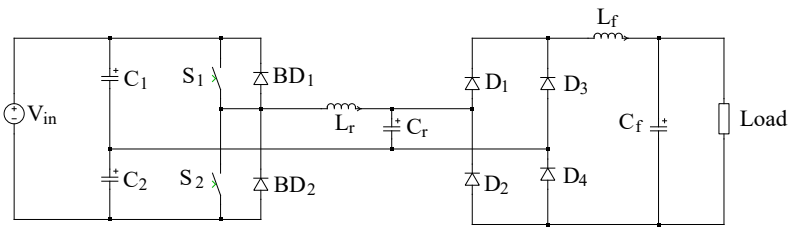


Figure 2.10: Parallel resonant converter (PRC).

More in details, Fig.2.9 reports a *voltage-source series-resonant converter* (VS-SRC), since the load current is obtained by full-wave rectifying and filtering the AC current flowing in the resonant tank (L_r and C_r). The input capacitors C_1 and C_2 are designed to be equal and large enough to maintain a nearly constant voltage $\frac{V_\mathrm{in}}{2}$, as in traditional PWM half-bridge converters. The unidirectional switches S_1 and S_2 are controlled with 50% duty cycle to provide symmetrical operation within a switching cycle. To provide bidirectional current capability, antiparallel body diodes are added. VS-SRC are widely described in [13], where the main operating regions, determined by the ratio of operating and resonant frequency, are presented. When the circuit is operated at a frequency lower than the resonance frequency of the LC tank, the tank behaves as a capacitive impedance and the resonant current leads the fundamental component of the input square-wave voltage generated by the switching action of the half-bridge structure. As a consequence, adopting unidirectional switches, they can be turned OFF in ZCS. This operation, however, cannot provide soft switching during OFF-ON commutations. If Silicon-controlled rectifiers (SCR) are exploited as power semiconductor switches, when the current would reverse,

these devices are instead naturally turned OFF (natural commutation). This soft-switching technique is optimised also for IGBTs, whose turn OFF is critical for the presence of a tail current (internal recombination current of minority carriers). A possible disadvantage of this technique is that the body diodes, which enter in conduction when the current reverses, should exhibit a fast recovery, to limit their turn OFF losses.

When the circuit is operated above resonance, instead, the resonance tank behaves as an inductive impedance, and the resonant current lags the fundamental component of the half-bridge output voltage. In this operating region (inductive region), when a switch of the half bridge is turned OFF (in hard-switching commutation), the tank current starts flowing in the opposite body diode. In this way, ZVS is achieved for the corresponding switch. Actually, the commutation is not instantaneous, due to the charging/discharging mechanism of the parasitic output capacitances of the transistors. The principle is that the energy stored in the parasitic capacitance during the interdiction state is exchanged with the resonant inductor instead of being dissipated in the transistor in the form of a current spike.

Fig.2.10 shows an example of *voltage-source parallel-resonant converter* (VS-PRC), which differs from the previous circuit for the position of the resonant capacitor, in parallel with the output stage. Its resonant voltage is full-wave rectified and filtered by a second-order output filter. Unlike SRCs, PRCs can step-up or step-down the input voltage (only step-down operation in SRCs) and can supply multiple outputs, thanks to the parallel connection of the tank capacitor. According to the operating frequency, multiple operating regions can be defined also in this case. Further information can be found in [10].

Hybrid topologies between SRCs and PRCs can also be defined, where the output rectifying stage is parallel-connected to only part of the overall resonating capacitance of the tank. These topologies, briefly described in [10], combine the inherent short-circuit protection offered by SRCs with the possibility of no-load operation of PRCs. In applications where a large voltage-gain range is required within a limited frequency range, such as in solar microinverters, the resonating tank can be composed by multiple reactive components (LLC, LCC, $LLCLC$): some examples are analysed further in this work in what follows.

In the class of load-resonant converters, it is possible to define current-sourced class E inverters, which exploits a sharply-tuned resonant tank to shape a sinusoidal output current. The basic topology of this converter class, based on a single switch, is depicted in Fig.2.11, where L_f is assumed to be sufficiently large to provide a nearly constant input current and C_1 is exploited to ensure ZVS turn ON of the switch.

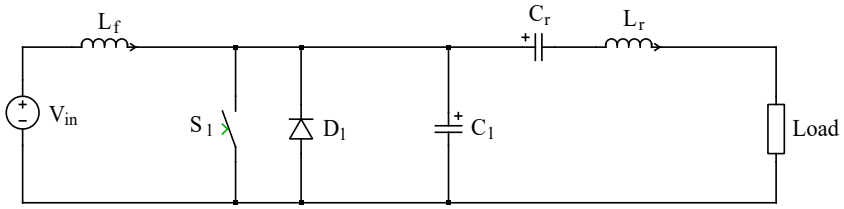


Figure 2.11: Class E resonant inverter.

In presence of sufficiently high quality factors and for operating frequencies next to the resonance frequency, a useful modelling tool is the first-harmonic approximation. This technique consists in approximating the tank inductor current and capacitor voltage as single-tone sinusoidal quantities. The high quality factor of the tank allows to neglect the contributions of higher order harmonics of square-wave voltages or currents to the transferred power. This approach greatly simplifies the analysis and allows to easily decouple cascaded stages of converters [11]. When at least one of the two above-mentioned hypotheses is not true, the first harmonic approximation is no more capable of correctly describe the behaviour of the circuit waveforms, and general tools like state-space representation become necessary.

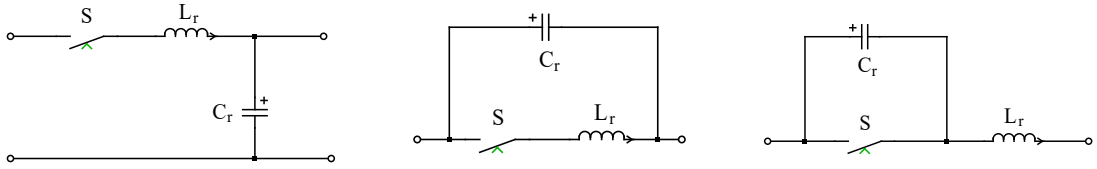
2. **ZCS/ZVS resonant converters**: The same principle of including a resonating tank in the topology is exploited for this second class of DC-DC resonant converters. The main difference with the previous class is that the LC network does not shape a full-wave sinusoidal current or voltage. Its goal is, in combination with a proper gating signal technique, to shape the switch current (or voltage) into arcs of sinusoids, to achieve zero-current or zero-voltage switching. The behaviour of the circuit within a switching cycle can be sub-divided in multiple modes, some of which are characterized by a resonance, and some are not. This is the reason why in some books, like in [11], this class is also referred to as *quasi-resonant converters*.

   Quasi-resonant converters can be derived by substituting the switches of conventional PWM DC-DC converters (Buck, Boost, Buck-boost, SEPIC, Čuk, buck-derived isolated topologies) with resonant (or quasi-resonant) switches. These are obtained by equipping the switch with a resonating LC tank such that:

   - ZCS can be achieved if the inductor is series-connected to the switch;
   - ZVS can be achieved if the capacitor is parallel-connected to the switch.

   Fig.2.12 shows three possibilities of resonant switches, obtained by different combinations of the LC tank: L-type ZCS network (inductor in series, capacitor

in parallel to the output stage), M-type ZCS network (capacitor in parallel to the series connection of switch and inductor), ZVS network (inductor in series with the parallel-connection of switch and capacitor).



(a) L-type ZCS resonant switch. **(b)** M-type ZCS resonant switch. **(c)** ZVS resonant switch.

Figure 2.12: Examples of resonant switches.

A detailed analysis of the properties and behavior of the different resonant switches is presented in [12]. Some of the distinctive features of these converters are the following:

- the quasi-resonant topology is easily derived from the original one by the addition of the resonant tank. As a consequence, differently from the previous class, single-stage DC-DC converters can be obtained without the need of an intermediate AC stage;
- the position of the resonant tank is such to "absorb" either the parasitic inductances or capacitance of the switch. However, due to the different orders of magnitude, the parasitics have negligible influence in determining the resonance frequency;
- the effect of the LC tank is to generate resonant current or voltage pulses that may require to re-consider the ratings of the switch. Resonant current pulses may increase the conduction losses, whereas voltage pulses may lead to the switch breakdown if it's not properly selected. To reduce the risk of failure, a sub-class of these converters (defined in [10]), exists to limit the switch voltage pulse to the value of the input voltage. These converters are called *resonant-transition* or *clamped-voltage* converters;
- voltage/current regulation is obtained through frequency modulation, with $f_{\text{sw}} < f_{\text{res}}$, to ensure that the resonant pulse is terminated within a switching cycle. The main drawback is that the size of the output filter should be tuned for the worst case (minimum frequency).
- a single resonant tank is responsible for allowing ZCS/ZVS of a single switch. When multiple resonant switches are present in the converter, it is said to be *multiresonant*. This class allows to reduce the overall commutation losses at the expense of a more complex architecture.

- to further reduce EMI levels, the commutation should occur in presence of null derivative of current (for ZCS turn OFF) or voltage (for ZVS turn ON). Another class of converters can be derived from this one by adding an auxiliary active or passive resonant network specifically designed for this goal. These converters are called *zero-voltage transition* (ZVT) and *zero-current transition* (ZCT) resonant converters [11, 14].

3. **Resonant DC-link converters**: The principle of this class of DC-DC and DC-AC converters is to exploit an input high-quality-factor LC tank to generate a sinusoidal DC-link voltage superimposed to the average DC input voltage. The switching frequency is controlled to be equal to the resonance frequency. If the topology of the converter is such that the resonating capacitor is in parallel to a switch of the converter, there is the possibility to turn ON the switch in zero-voltage condition.

4. **High frequency-link integral-half-cycle converters**: These AC-AC converters exploit the same principle as DC-link resonant ones, where switches are controlled to be turned ON at zero-voltage. The difference is that the input source is a high-frequency purely-AC voltage, and the average desired low-frequency output voltage is synthesized by an integer number of high-frequency cycles. More details on these converters can be found in [10].

2.3.3 Resonant converters issues

Despite the great advantage to provide ZVS or ZCS, reducing the switching losses and EMI, resonant converters, independently on the considered class, are characterized by common drawbacks [13]:

- the input-output transcharacteristic is usually a complex function depending on the input source, tank parasitics and load. Very often, to provide a compact description, the analytical transcharacteristic and circuit waveforms are parametrized by the *loaded quality factor* and the *characteristic impedance* of the tank. The definition of these quantities is not unique and depend on the topology. This dependence may make it difficult to achieve a high efficiency over a wide range of input voltages and load conditions;

- as mentioned, the presence of a resonating tank shapes some of the circuit currents/voltages to be larger than in conventional PWM converters. The generation of current pulses, specifically, can be source of larger conduction losses in the switches, which may deteriorate the overall efficiency at low loads operation;

- the tank itself is not ideal: the circulating current is source of conduction losses due to resistive parasitics.
- even with resonating structures, there is no guarantee to achieve soft-switching for all the load conditions. ZVS/ZCS, in some resonant topologies, can be achieved only for a certain range of loads [13] above or below a critical resistance value. The analysis of these boundaries is specific for each topology and cannot be generalized;
- the modelling of resonant converters for control purposes is not straightforward. In few cases and with strict hypotheses (mentioned earlier in this work), the first harmonic approximation offers a simplified tool. Research is focusing on how to derive generalized methods to deal with resonant converters modelling. In [11], the extended describing function method is mentioned, which is based on the decomposition of reactive state-variables of the tank (inductor current, capacitor voltage) into d-axis and q-axis components. This approach allows to derive a small signal model by perturbing the system around a stationary operating point. The approach is applied to a SRC and to a PRC in [15].

Chapter 3

State of the art of resonant power converters for PV applications

3.1 Solar microinverters

In this section, a literature review is presented to outline the current state of the art of solar microinverters. These power converters are optimised to interface an input PV module with a low-voltage grid. Thanks to the increasing diffusion of micro-PV systems, the demand for reliable and efficient power conversion units has grown consequently. In 2015, the largest majority of installed PV capacity (99%) was associated to grid-tied PV plants [16]. These can be broadly classified into four categories according to the architecture of the power conversion unit, and the dimension/power of the PV plant:

1. AC-module inverters (or **microinverters**) are connected to single modules for direct interface with a low-voltage grid. Given the DC voltage requirements necessary for a correct DC-AC conversion (400 V), and given the typical output voltages of single PV modules (few tens of volts, depending on the number of cells), it is necessary to step-up the PV voltage. Thus, this solution typically requires a multistage conversion unit, unless the DC-AC stage is already capable of boosting the input voltage up to the grid requirements. Due to the reduced dimensions and the low power involved (up to few hundreds of watts), this architecture is the most diffused for rooftop applications. The addition of eventual intermediate DC-DC step-up stages may lead to an overall conversion efficiency decrease: from this, the need to explore innovative high-efficiency solutions, like resonant ones. On the other hand, the interface with a single

PV module eases the MPPT process. Due to the increasing attention of the research towards microinverters and the multiple challenges to be addressed, this class of PV-sourced converters is the object of the following literature review, and the starting point for the research of an innovative solution;

2. **string inverters** are exploited as interface between an array/string of PV modules to the low-voltage grid. The series connection of multiple PV panels may avoid the need of an intermediate DC-DC stage, which however is necessary to decouple the MPPT control (first stage) from the control of active-reactive power injected to the grid (second stage). The larger power rating and the adoption of a unique converter for multiple PV modules allow to increase the efficiency and reduce the cost-per-Watt. Despite this, the MPPT efficiency is lower when compared to microinverters, especially in presence of partial shading scenarios;

3. **multistring** converters represent a more versatile solution with respect to string inverters. Here, the PV plant is divided into smaller strings of series-connected modules. Every string is connected to a high-voltage DC-link through a DC-DC converter endowed with MPPT control. Finally, a single grid inverter provides the required DC-AC conversion;

4. the largest scale solution (hundreds of kW) consists of a single high-power grid-tied inverter connected to an entire PV plant composed of several strings in parallel (**central inverter**). This solution is clearly the least flexible in terms of MPPT accuracy, but the most efficient. Due to the large power capacity, a three-phase inverter followed by a LV-MV transformer is typically adopted.

The selection of the architecture mainly depends on the power ratings and the desired flexibility. Compared to the other solutions, microinverters exhibit the need to step-up the voltage up to around 400 V, to make them compliant for the grid voltage requirements. The boost stage must not only provide gain to the PV module output voltage, but should be able to dynamically adjust the gain according to the environmental conditions, to track the absolute MPP [17]. Step-up stages, at the same time, should be optimised to achieve a high efficiency over the proposed gain range. Several high-efficiency solutions to extend the gain range for tracking effectively the MPP even in PSC have been explored. In this work, some of these solutions, resonant and non-resonant, single-stage and multistage, are compared to outline the state of the art of solar microinverters.

For each converter, the topology and control scheme are briefly described to outline what is the adopted innovative solution to increase the efficiency over the

proposed voltage gain range. When available, the efficiency graphs as function of the input voltage are compared. The main limitations for each converter are instead collected in a final summary table to provide a general overview of the state of the art in terms of possible issues still to be solved.

3.1.1 Resonant topologies

Dual DC-DC stage and inverter stage

The first class of microinverters analysed in this section consists in dual-stage resonant converters. The following circuits, actually, refer only to the DC-DC conversion stage for two main reasons:

- the DC-AC stage is normally implemented as a full-bridge inverter (in case of single-phase grid) or 2-level 3-phase inverter (in case of three-phase grid). All the following works adopt the same full-bridge inverter topology for this stage;
- the real bottleneck for the conversion efficiency is the DC-DC stage, which must ensure a high step-up ratio (from around 30 V to 400 V) without compromising the efficiency. Traditional PWM boost stages, indeed, due to hard-switching and to the dependence of semiconductor devices losses on the duty cycle, do not represent a viable solution for high-efficiency conversion.

For these reasons, in the following circuit schematics the DC-AC stage is represented as a generic DC load for the DC-DC stage.

Fig.3.1a shows the proposed converter in [18]. It consists of a hybrid resonant converter implemented as an isolated LLC converter with the addition of a bidirectional GaN switch. This consists of two series-connected GaN FETs with opposite polarity (S_{5a} and S_{5b}) and controlled by the same signal $M5$. The converter topology includes a full-bridge inverter operated at the resonant frequency ($f_{res} = \frac{1}{2\pi\sqrt{L_r \cdot (C_{r1}+C_{r2})}}$), a high-frequency transformer (represented, in the schematic, by an ideal transformer with the parasitic magnetizing inductance, L_{magn} and leakage inductance, $L_{leakage}$) and a voltage doubler rectifier (VDR). The bidirectional switch terminals are connected to the AC rail. The VDR is a common and efficient alternative to conventional bridge rectifiers thanks to its simultaneous tasks of doubling the input AC voltage amplitude and rectifying it.

As the following converters will show, the combination of a real transformer and a VDR allows to generate a LLC resonant tank exploiting inductive parasitics already present in the transformer (L_{magn} and $L_{leakage}$) and the capacitors of the rectifier (C_{r1} and C_{r2}). In this way, no additional resonant component must be added for the tank, with benefits to the power density. At the same time, the transformer turns ratio provides an intrinsic additional step-up capability.

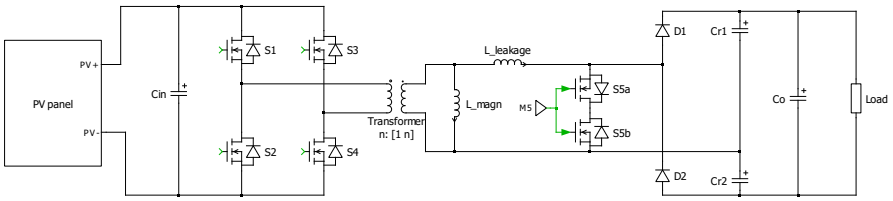
The key approach exploited in the work is a multi-mode (or multi-region) operation according to the desired gain to achieve. Since the output voltage is regulated at 315 V by the following DC-AC stage, varying the gain implies controlling the input voltage. The goal of the MPPT controller is to control the conversion gain to achieve $V_{\mathrm{PV}} = V_{\mathrm{GMPP}}$. According to the environmental condition (and, consequently, to the position of V_{GMPP}), the circuit can operate in three possible regions:

1. **Normal mode** ($V_{\mathrm{GMPP}} = 30\,\mathrm{V}$, selected as the nominal V_{GMPP}). In this mode, the full-bridge MOSFETs are controlled with 50% duty cycle and 180^o phase shift. Working at the resonant frequency and with symmetric operation ensures sinusoidal behaviour of the tank leakage inductance current and the capacitors voltages, in turns resulting in the MOSFETs ZVS turn ON and rectifier diodes ZCS turn ON. The bidirectional switch is always inactive in this mode. The highest efficiency is reached in this condition;

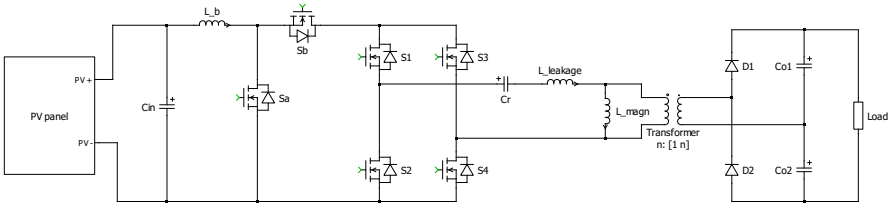
2. **Buck mode** ($V_{\mathrm{GMPP}} > 30\,\mathrm{V}$). In this mode, a phase-shift modulation (PSM) technique is exploited to control the full bridge MOSFETs, whereas the bidirectional switch is always kept open. The phase shift is the control variable by which the amplitude of the fundamental component of the primary voltage can be shaped. The magnetizing inductance is exploited to discharge the output capacitances of the MOSFETs to be turned ON: in this way, ZVS can be achieved. The circuit operates in discontinuous conduction mode (DCM), allowing the rectifier diodes to turn ON in ZCS;

3. **Boost mode** ($V_{\mathrm{GMPP}} < 30\,\mathrm{V}$). In this region, the full bridge MOSFETs are controlled as in the normal mode (50% duty cycle and 180^o phase shift). The gain can be modified by setting the duty cycle of the bidirectional switch ($S_{5\mathrm{a}}$ and $S_{5\mathrm{b}}$), which is controlled at twice the resonant frequency. The exploited principle is that the leakage inductance, during the conduction time of the GaN switch, is forced to charge linearly, behaving as a boost inductor, and releasing its stored energy during the resonant stage (when the switch turns OFF). Since the switch is always operated in hard-switching and at twice the operating frequency, a GaN FET with low parasitic capacitances (compared to Silicon MOSFETs) is exploited to reduce the switching losses.

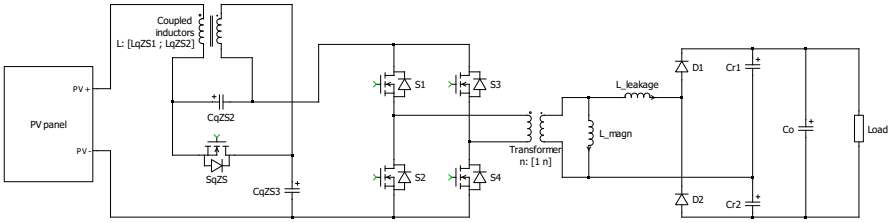
Another dual-stage resonant converter [19] is shown in Fig.3.1b. Differently from the previous case, here the two conversion stages are clearly separated: a traditional PWM boost stage is followed by a *LLC* series resonant stage. The last one is designed to operate always in the best operating condition from the point of view of efficiency (50% duty cycle, 180^o phase shift and $f_{\mathrm{sw}} = f_{\mathrm{res}}$ of the full-bridge



(a) Hybrid resonant converter with a bidirectional GaN switch [18].



(b) Isolated step-up dual stage DC-DC converter [19].



(c) Quasi-Z source Series Resonant DC-DC converter [20].

Figure 3.1: Resonant dual-stage DC-DC converters.

MOSFETs). As such, the resonant stage provides fixed gain, determined by the transformer turns ratio and the presence of a voltage doubler rectifier:

$$G_{\text{resonant stage}} = 2n\,. \tag{3.1}$$

The intermediate DC-link voltage is chosen to minimize the losses of the first PWM boost stage. The MOSFETs of this stage always operate in hard switching condition. To decrease the conduction losses, then, the DC-link voltage was chosen to minimise the duty cycle required for the stepping up the PV module voltage (50 V, to realize a 15 V − 45 V input voltage range with 10% − 70% duty cycle range). In the article, care is devoted to the selection of the boost inductor and high-frequency transformer cores. Since the full-bridge MOSFETs are turned ON with ZVS, thanks to the non-null magnetizing current, indeed, the core losses represent the main source of dissipation of the second stage. Since core losses are independent on the power level of the circuit, they become critical at part-load operation: this is why the half-cycle skipping technique is adopted to improve the part-load efficiency.

Fig.3.1c depicts the converter proposed in [20]. It consists of a first quasi-Z source (qZS) network, including two capacitors, two coupled inductors and a MOSFET, and a second *LLC* series-resonant converter. As in the previous cases, a full-bridge topology is exploited to generate the AC voltage at the transformer primary side, whereas a VDR is designed to rectify and doubling the output voltage. The qZS network here adopted has been analysed in its operating modes (*non-shoot through* and *shoot-through*) in [21].

As in [18], this converter can operate in three different conditions according to the desired voltage gain to be achieved:

1. **Normal mode** ($V_{\mathrm{GMPP}} = 34\,\mathrm{V}$). In this mode, the full-bridge MOSFETs work at the resonance frequency ($f_{\mathrm{res}} = \frac{1}{2\pi\sqrt{L_{\mathrm{r}} \cdot (C_{\mathrm{r1}} + C_{\mathrm{r2}})}}$), 50% duty cycle and 180^o phase shift. During this mode, the MOSFET of the qZS is always kept closed and the qZS network provides a unitary voltage gain. As in [18], the nominal voltage of this mode is selected as the most common V_{MPP} associated to the PV panel taken as reference.

2. **Buck mode** ($V_{\mathrm{GMPP}} > 34\,\mathrm{V}$). In this mode, the same phase-shift modulation (PSM) technique is exploited to control the full bridge MOSFETs, as in [18]. S_{sZS} is still kept closed. This region implies the same features previously described for the circuit in Fig.3.1a;

3. **Boost mode** ($V_{\mathrm{GMPP}} < 34\,\mathrm{V}$). In this region, the qZS operating mode is toggled between the *shoot-through* and the *non-shoot-through* according to the full bridge MOSFETs state. A shoot-through time T_{ST} is realized in which all the MOSFETs of the full bridge conduct: to avoid short-circuiting the qZS capacitors, S_{sZS} is turned OFF during this time. The equivalent shoot-through duty cycle $D_{\mathrm{ST}} = \frac{T_{\mathrm{ST}}}{T_{\mathrm{sw}}}$ becomes the control variable by which a step-up voltage gain can be achieved:

$$G_{\mathrm{BOOST}} = \frac{2n}{1 - 2D_{\mathrm{ST}}}\,. \tag{3.2}$$

The converter power density is increased thanks to the adoption of a magnetically-integrated qZS network (coupled inductors) and the exploitation of the HF transformer parasitics as inductive components of the resonant tank.

The multimode operation, moreover, allows to achieve a broad input voltage range from 10 V to 60 V, larger than the actual requirements of any commercial module.

Single DC-DC stage and inverter stage

In this section, three single-stage resonant DC-DC converters are presented. Compared to the previous solutions, where typically the resonant stage was operated at the resonance frequency to maximise the conversion efficiency, and the voltage gain was adjusted through an auxiliary control variable, here the switching frequency represents the control variable by which the tank impedance, and consequently the voltage gain, can be modified.

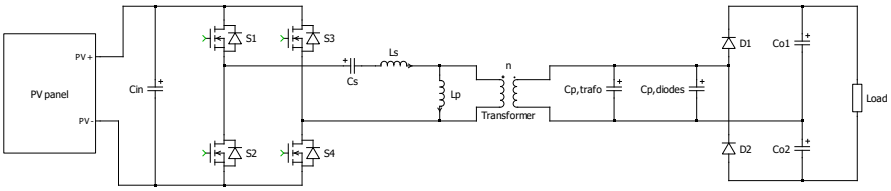
Fig.3.2a shows the converter proposed in [22]. It consists of a single-stage series-parallel resonant converter ($LLCC$) with an input full-bridge inverter and an output voltage doubler rectifier, as the previous analysed topologies. The difference lies in the exploitation of the capacitive parasitics at the secondary side of the transformer (referred to the transformer itself, $C_{\mathrm{p,trafo}}$, and to the diodes, $C_{\mathrm{p,diodes}}$) to generate a second resonance peak in the voltage transfer function, at:

$$f_{\mathrm{res},2} = \frac{1}{2\pi\sqrt{L_{\mathrm{p}}C_{\mathrm{p}}}}\,. \tag{3.3}$$

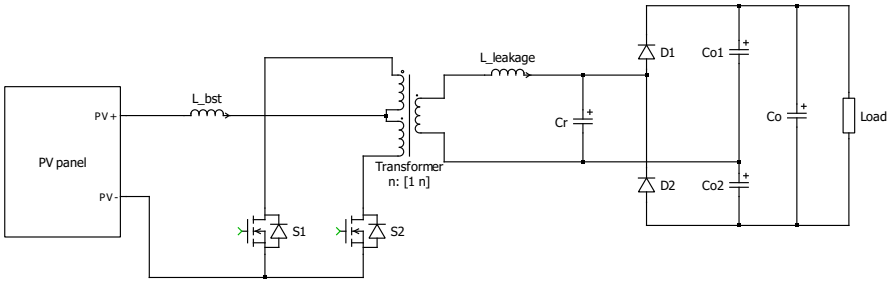
The presence of four tank elements complicates the voltage gain, which is studied in the paper through the first harmonic approximation (FHA) method. The converter is always operated in the inductive region to achieve ZVS of the bridge MOSFETs. The main advantage of $LLCC$-based converters is that a relatively small frequency range (unspecified in the paper) can provide a wide voltage gain range (from 1 V/V to 2 V/V). Since the transfer function depends on multiple parameters (resonance frequencies, inductance and capacitance values, and turns ratio), a design procedure is proposed to optimise the selection of parameters according to the minimization of the total losses (considering gate, turn OFF and core losses).

A current-fed push-pull resonant converter is proposed in [23] (Fig.3.2b). The converter improves the efficiency of the conventional PWM push-pull thanks to the resonant tank at the secondary side of the transformer, which helps achieving ZCS turn ON and ZVS turn OFF. Moreover, the presence of an input boost-inductor provides additional step-up capability together with the output voltage doubler rectifier, resulting in a lower required turns ratio of the transformer (lower copper losses).

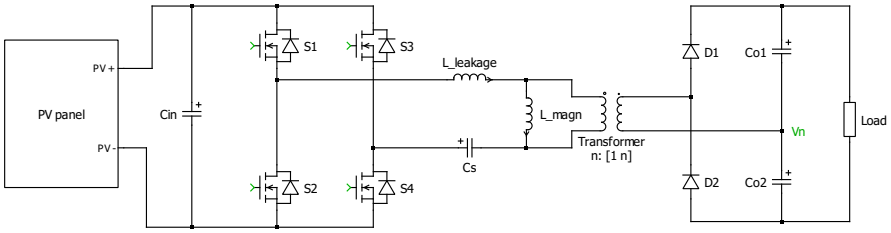
The conduction periods of the switches are slightly overlapped to provide the required boosting action of the input inductor. Moreover, the switches are operated at $f_{\mathrm{sw}} \ll f_{\mathrm{res}}$ in order to achieve soft commutations independently from load, as previously mentioned. The resonant behaviour of the tank is then obtained in a short interval of time compared to the switching period, and is exploited to achieve



(a) Single-stage series-parallel resonant converter [22].



(b) Current-fed resonant push-pull converter [23].



(c) *LLC* Resonant DC-DC converter [24].

Figure 3.2: Resonant single-stage DC-DC converters.

soft-switching operation. A frequency modulation technique is adopted to control the voltage gain.

Finally, another single-stage resonant converter is proposed in [24] and shown in Fig.3.2c. Differently from the previous topologies, this microinverter is designed to interface a larger power PV module with a three-phase low-voltage grid. The highlighted node V_{n} is connected to the neutral of the grid. Actually, the DC-DC stage of the microinverter consists in a conventional full-bridge *LLC* resonant converter connected to a voltage doubler rectifier, responsible to track the MPP through a frequency modulation technique. This first stage, beside the adoption of a center-point iteration algorithm for the MPPT (instead of a conventional P&O or InC), does not provide any significant improvement with respect to the previously described *LLC*-based topologies.

The paper, indeed, focuses on the second DC-3Φ AC stage, which instead

exploits the presence of the AC-filter inductors to realize ZVS condition for the three-phase inverter MOSFETs. The grid filter inductor currents are intentionally made oscillating between positive and negative values to allow the charge/discharge of the output capacitances of the inverter MOSFETs. Their average values are the desired low-frequency sinusoidal currents.

Single stage inverter

The last converter presented in this review of resonant microinverters is a single-stage buck-boost inverter, shown in Fig.3.3 [25]. The topology is based on the conventional full-bridge inverter, but includes an additional series resonant LC tank composed of L_{r1}, L_{r2} and C_r. According to the half-wave of the low-frequency voltage sinusoid, either the left leg or the right leg of the bridge operates: within a switching cycle, inductor L_{r1} or L_{r2} is forced to charge by closing simultaneously both the IGBTs of a leg, in this way acting as a boost inductor. When the low-side IGBT is turned OFF, the LC tank resonates with the previously stored energy, and this allows to realize a step-up action.

The adoption of unidirectional devices (IGBTs) and the selection of switching frequency are such that the inductor operates in discontinuous conduction mode (DCM). This operation allows to turn ON the IGBTs in ZCS. The circuit is operated at the constant frequency of 40 kHz, whereas the gain modulation to produce an average low-frequency voltage sinusoid is achieved by varying the duty cycle of the low side switches S_3 and S_4.

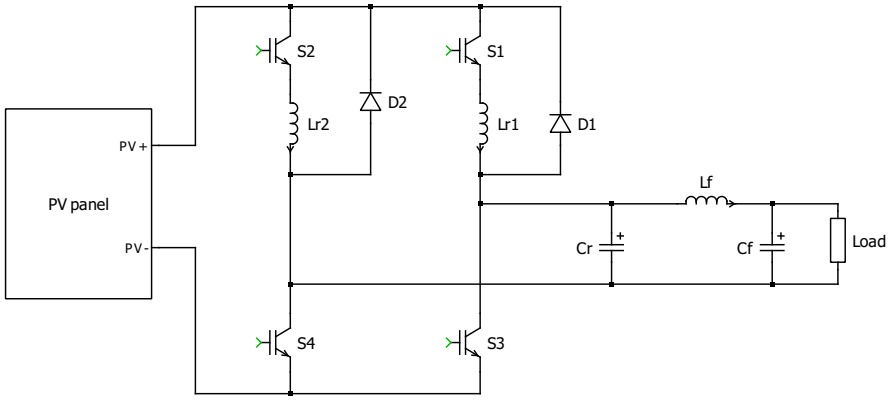


Figure 3.3: Resonant single-stage buck-boost inverter [25].

3.1.2 Non-resonant topologies

Single DC-DC stage and inverter stage

In this section, to provide a comparison with the previously presented resonant DC-DC stages for microinverters, some of the current state-of-the-art non-resonant converters are presented. These converters are always optimised to interface effectively a PV module with a 400 V DC-link, and thus they must be able to adjust dynamically the voltage gain according to the environmental conditions. In the following pictures, to keep the same approach adopted for the previous section, the load represents the input impedance of the DC-AC stage of the microinverter.

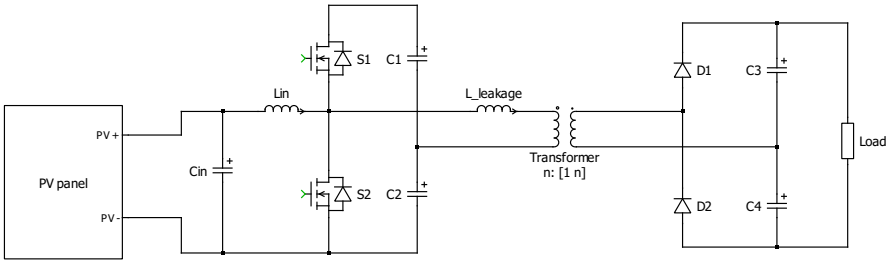
The first non-resonant topology is presented in [26] and shown in Fig.3.4a. It consists in a half-bridge single stage DC-DC converter which integrates an input boost inductor (L_{in}) to provide an adjustable step-up gain through the control of the duty cycle of switches S_1 and S_2. The turns ratio n of the transformer and the output voltage doubler rectifier provides, instead, a fixed gain $2n$. As in the previous cases, the following DC-AC stage is a conventional full-bridge PWM inverter which is not considered here.

The transformer is assumed to be ideal for the analysis of the circuit operation. As a result, soft-commutation of the switches linked to the circulation of a non-null magnetizing current of the transformer is not considered.

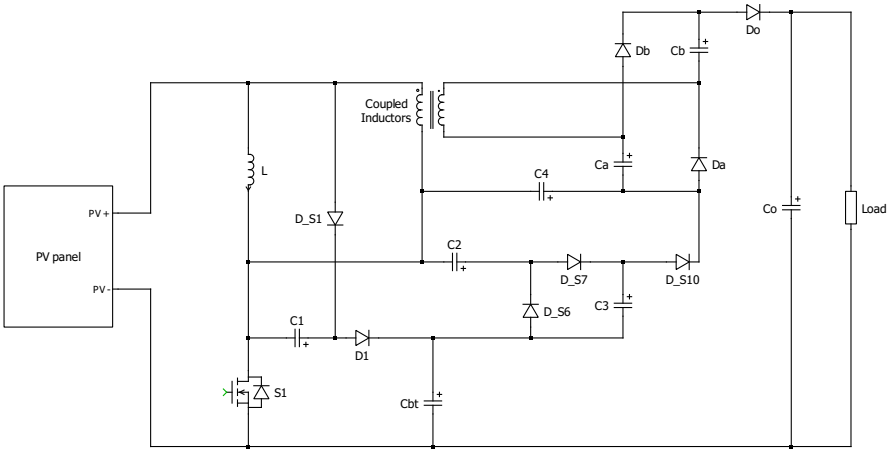
The grid current control scheme is based on the adoption of a repetitive controller to reject high-order harmonics from the current control loop. The authors of [26] specifically addresses the problems related to step changes of the control variable (in this case, the duty cycle), such as the possibility of inrush currents or temporary LC oscillations. This is the reason why a ramp-changing adjustment of the PV module voltage reference is realized in combination with an adaptive step P&O algorithm in the MPPT scheme.

Another possibility of single-stage non-resonant DC-DC converter is analysed in [27] (Fig.3.4b). Contrarily to the previous one, this is not based on a modification of the half-bridge isolated topology. The relatively complex topology aims to overcome the efficiency limitations of a conventional PWM boost (L, S_1, D_1 and C_{bt}) by combining several step-up techniques to increase the gain:

- two superlift switched-capacitor networks (C_1 and D_{S1}, and C_4 and D_{S10}), which are based on the arithmetic progression increase of the capacitor voltage, cycle by cycle;
- a voltage multiplier (C_{a}, D_{a}, C_{b} and D_{b}) combined with coupled inductors;
- a Dickson switched-capacitors network (C_3, D_{S6}, C_4 and D_{S7}).



(a) Boost half-bridge DC-DC converter [26].



(b) High step-up gain DC-DC converter [27].

Figure 3.4: Non-resonant single-stage DC-DC converters.

Despite the complexity and the number of capacitors and diodes required for the topology, the converter includes a single controlled switch, whose duty cycle is exploited for the MPPT cotrol. Every network contributes to the final gain, which results in a non-linear function od the switch duty cycle:

$$M = \frac{4 + n(2 - D) - D}{1 - D}, \tag{3.4}$$

where n and D represent the coupled inductors turns ratio and the duty cycle, respectively.

The topology allows to significantly increase the gain for the same duty cycle, with respect to the traditional boost converter, decreasing in this way the switch losses. Moreover, as analysed in the paper, the voltage stresses of semiconductor devices are reduced with respect to the standard boost: as a result, the devices voltage ratings can be reduced, with benefits to the conduction losses. The large number of diodes (8) accounts for the largest part of the converter losses. The paper does not focus on the MPPT control scheme.

Single stage inverters

In this final section, two examples of non-resonant single-stage inverters are considered. These converters must include a doubled symmetric structure to allow the generation of an AC voltage, but must be capable at the same time to provide a step-up/step-down gain according to the instantaneous value of the grid voltage.

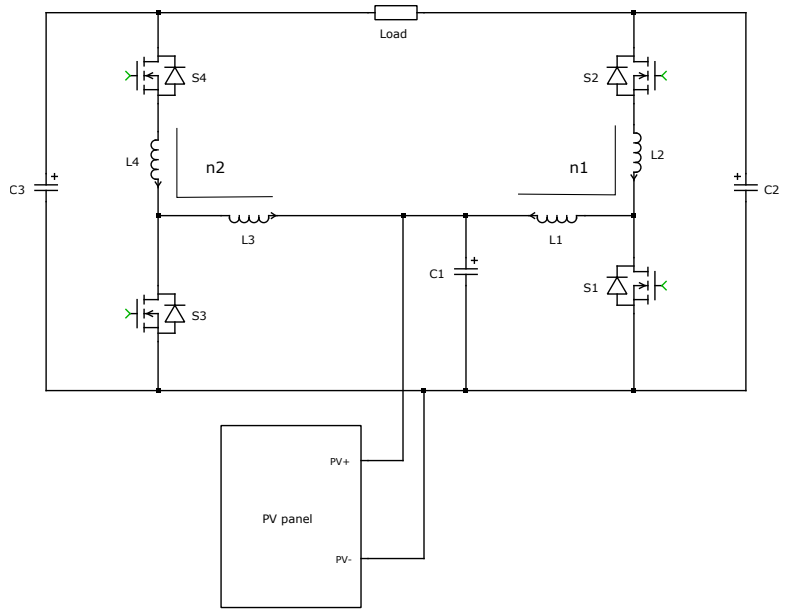
The first example is analysed in [28] and shown in Fig.3.5a. It consists in a boost-derived topology with doubled structure (to provide a differential output, as in full-bridge inverters) and with the presence of two pairs of coupled inductors, to increase the gain. Compared to the PWM double-boost converter topology presented in [29], this one exploits coupled inductors to provide additional step-up capability according to their turns ratio, while keeping the duty cycle in a low variation range around 50%.

The switches of the two legs are controlled in a complementary way (complementary duty cycles) in order to remove the DC-bias from the output voltage. As a result, S_1 and S_4 share the same driving signal, and the same happens for S_2 and S_3. The duty cycles are generated with a sinusoidal PWM approach. The MPPT is achieved through a conventional P&O algorithm.

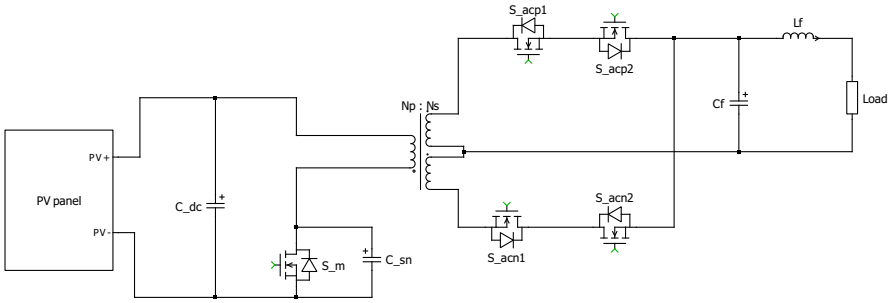
Finally, a flyback-derived single-stage microinverter is presented in [30]. The circuit, shown in Fig.3.5b, aims to improve the efficiency of a conventional PWM flyback, by modifying the topology to allow achieving ZVS turn ON of the primary side MOSFET (S_{m}) and the secondary side MOSFETs (S_{acp2} and S_{acn2}). To inject a bidirectional current into the grid, a center-tapped transformer is exploited.

During the positive/negative half grid voltage cycles, either S_{acp1} or S_{acn1} is always ON, respectively, whereas S_{acp2} (or S_{acn2}) are just turned ON for a short interval of time to allow a temporary current reverse at the secondary side. When S_{acp2} (or S_{acn2}) is turned OFF, this magnetizing current is forced to recirculate at the primary side, discharging the output capacitance of S_{m} and allowing its ZVS turn ON.

To increase the amount of transferred power, the boundary conduction mode (BCM) is exploited for the magnetizing current. A peak-current mode control technique is adopted to control the magnetizing current: a MPPT controller, according to the maximum allowed power that can be extracted, produces a rectified sinusoidal reference current to which the magnetizing current must be compared. As a consequence, the converter results to be frequency modulated with variable turn-ON time for the primary switch, and fixed turn OFF time.



(a) Double-boost microinverter with coupled inductors [28].



(b) Flyback-based single-stage microinverter [30].

Figure 3.5: Non-resonant single-stage inverters.

3.1.3 Performance comparison

In this section, the previously analysed converters of the state of the art of solar microinverters are compared on the basis of their efficiency (as a function of the operating power and, when available, of the input voltage) and input voltage range. Graphs illustrating the performance of the presented converters are not always reported in the corresponding publications, so the comparison will be performed only on the available data.

In order to present a coherent comparison, only the performances of DC-DC stages are considered, assuming that the DC-AC conversion stages, usually with

full-bridge inverters, exhibit comparable performances. As previously mentioned, due to the high step-up gain requirements, the DC-DC converter may represent the most critical part of the conversion chain. As a consequence, single-stage inverters are excluded from the comparison. Moreover, since the converter described in [24] is designed for a three-phase inverter working at 700 V and for larger power modules, it will be excluded as well. For the presented performance graphs, the main reasons for efficiency peaks or drops in a precise power or input voltage range are described, outlining what limitations the research could possibly go beyond.

Efficiency under various load conditions

Any solar microinverter analysed in the previous sections exhibits specific limitations or improvements in efficiency linked to the components selection or the adoption of a specific control technique. Fig.3.6 reports all the available efficiency curves as function of the operating power of the described DC-DC converters. Every curve is relative to a fixed input voltage operation (at the V_{MPP} measured at the STC conditions) and can be interpreted as the efficiency measured for different irradiance conditions, under the hypothesis that the GMPP voltage does not vary significantly. Solid lines refer to resonant dual-stage converters, dotted lines to resonant single-stage converters, and dashed lines to non-resonant single-stage DC-DC converters.

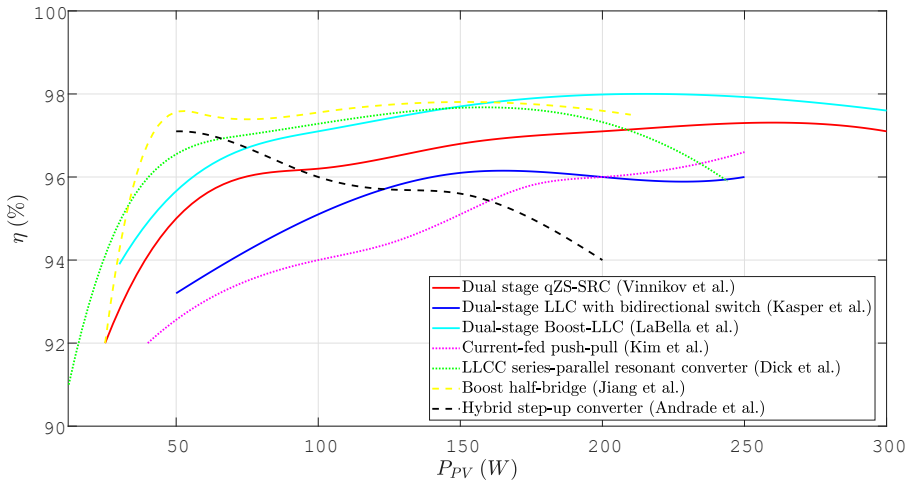


Figure 3.6: DC-DC converters efficiency as function of the operating power.

A global consideration is that all the resonant converters, dual or single-stage, exhibit e nearly monotonous increasing behaviour of the efficiency as the operating

power increases. This is mainly linked to the presence of nearly fixed dissipation sources such as gate losses and, most importantly, of transformer core losses, which are dependent on the operation frequency. As a consequence, these losses impact more at low operating power conditions. The same happens for the converter in [26] (light green curve) which itself includes a transformer, despite not exploited for LC resonance.

The efficiency performances of the converter in [27] are instead represented by a monotonically decreasing curve. This can be explained by reminding the large number of diodes of this topology, to realize the step-up networks: the 8 diodes conduction losses increase linearly with the transferred power, and moreover they are forced to hard-switching commutations. In the input inductor, instead, the conduction losses approximately increase quadratically with the transferred power.

What can be observed is that the adoption of a resonant network to achieve soft switching of power semiconductor devices not necessarily implies a significant increase in efficiency with respect to non-resonant converters. The presence of conduction losses linked to the magnetizing current and of larger current peaks of resonant networks can counterbalance the benefits to commutation losses.

Efficiency under various input voltage conditions

The efficiency of the three analysed dual-stage resonant converters (in [18, 19, 20]) are characterized in their respective papers as a function of the input voltage. The aim of the authors was to prove the efficiency of their proposed converters when they operate over a wide range of input voltage, when, for instance, the PV module is subjected to various partial shading scenarios and the MPPT controller forces the converter to operate outside the STC V_{MPP}.

Despite the really large input voltage range reported in [20], which is, according to the authors, beyond the real possible voltage range of a common 48-cell or 60-cell Silicon PV module, its non-monotonic behavior recalls the one of [18]. Both the converters can operate, according to the instantaneous input voltage, in three different operating modes.

The efficiency peaks refer exactly to the normal operating mode, when the converter operates as a LLC resonant converter working at the resonance frequency, achieving in this way soft switching for all the power semiconductor devices.

When operating in buck mode (above the nominal V_{MPP}), they exploit a phase-shift modulation of the full-bridge MOSFETs. During the simultaneous conduction of both high-side or both low side MOSFETs, the magnetizing current of the transformer is forced to recirculate in a free-wheeling loop, leading to an increase in the conduction losses. Moreover, far from the nominal V_{MPP}, the extracted power from a PV module decreases significantly, and the above-mentioned fixed losses

acquire more and more impact.

In the boost mode, different approaches are exploited. In [20], a shoot-through time is controlled during which all the MOSFETs of the full-bridge conduct (cross-conduction). In this operating mode, however, soft-switching of the MOSFETs is lost both during turn ON and OFF. In [18], instead, the bidirectional GaN switch exploited to charge the boost inductor causes additional conduction losses, and is always turned ON and OFF in hard-switching.

Finally, the dual-stage converter in [19] is composed of two distinct stages: a traditional PWM boost, responsible for the MPPT control, and a SRC, always operated in its optimal conditions (resonance frequency, 50% duty cycle and 180^o of the full-bridge MOSFETs). As a consequence, the efficiency profile recalls that of the PWM boost operating in CCM, where the inductor and switch losses increase as the duty cycle (gain) increases.

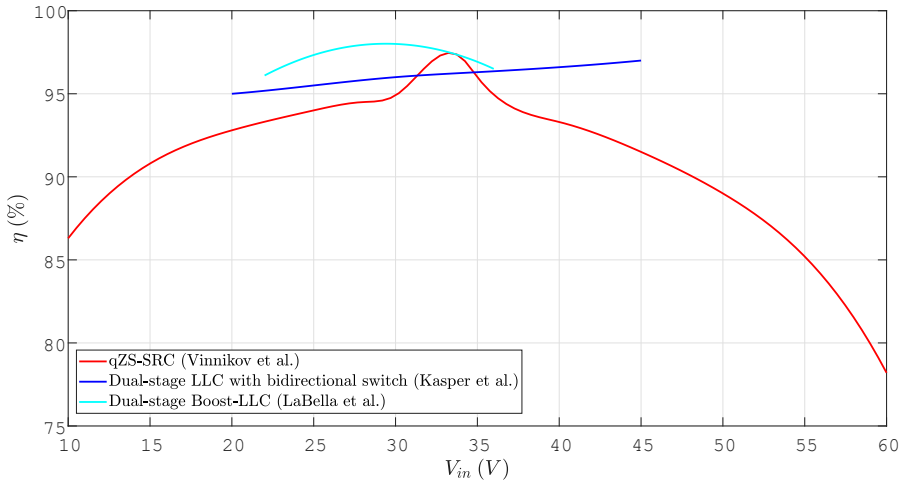


Figure 3.7: DC-DC converters efficiency as function of the input voltage.

Performance comparison

Tab.3.1 reports a comparison of the previously described converters for solar microinverters applications. For each topology, the control variable for the MPPT technique, the peak efficiency referred to a specific operating condition, the input voltage range and the adopted MPPT technique are reported.

This literature review of solar microinverters has outlined that many solutions, resonant and non, exist to allow tracking effectively the MPP under various partial

Microinverter topology	Control variable	Operating conditions	Peak efficiency	Input voltage range	MPPT technique
RESONANT DUAL STAGE DC-DC + INVERTER					
Hybrid resonant converter with bidirectional GaN switch [18]	Full bridge switches phase shift (Buck mode) Bidirectional switch duty cycle (Boost mode)	$V_{in} = 30\,V$; $V_{out} = 315\,V$; $P_{out} = 300\,W$	97.5%	15 V – 55 V	(not specified)
Isolated step-up dual stage DC-DC converter [19]	Boost switch duty cycle (fixed frequency)	$V_{in} = 45\,V$; $V_{out} = 400\,V$; $P_{out} = 250\,W$	97%	15 V – 45 V	(not specified)
Quasi-Z source Series Resonant DC-DC converter [20]	Full bridge switches phase shift (Buck mode) Shoot through time (Boost mode)	$V_{in} = 34\,V$; $V_{out} = 400\,V$; $P_{out} = 250\,W$	97.4%	10 V – 60 V	(not specified)
RESONANT SINGLE STAGE DC-DC + INVERTER					
Single-stage series-parallel resonant converter [22]	Switching frequency (around f_{res})	$V_{in} = 35\,V$; $V_{out} = 700\,V$; $P_{out} = 88\,W$	96%	20 V – 35 V	Variable frequency P&O
Current-fed resonant push-pull converter [23]	Switching frequency ($\ll f_{res}$)	$V_{in} = 30.9\,V$; $V_{out} = 400\,V$; $P_{out} = 250\,W$	96.6%	20 V – 40 V	Variable frequency P&O
LLC resonant DC-DC converter [24]	Switching frequency (around f_{res})	$V_{in} = 55\,V$; $V_{out} = 400\,V$; $P_{out} = 150\,W$	98.2%	35 V – 55 V	Center point iteration
RESONANT SINGLE STAGE INVERTER					
Resonant single-stage buck-boost inverter [25]	Full bridge switches duty cycles	$V_{in} = 75\,V$; $V_{out} = 120\,V_{RMS}$; $P_{out} = 200\,W$	93%	(not specified)	(not specified)
NON RESONANT SINGLE STAGE DC-DC + INVERTER					
Boost half-bridge DC-DC converter [26]	Half bridge switches duty cycle	$V_{in} = 40\,V$; $V_{out} = 370\,V$; $P_{out} = 160\,W$	97.8%	30 V – 50 V	Adaptive step P&O
High step-up gain DC-DC converter [27]	Single switch duty cycle	$V_{in} = 30\,V$; $V_{out} = 400\,V$; $P_{out} = 200\,W$	94%	24 V – 45 V	(not specified)
NON RESONANT SINGLE STAGE INVERTER					
Double-boost microinverter with coupled inductors [28]	Switches duty cycle (around 50%)	$V_{in} = 34.8\,V$; $V_{out} = 220\,V_{RMS}$; $P_{out} = 218\,W$	97.5%	(not specified)	Fixed frequency P&O
Flyback-based single-stage microinverter [30]	Switching frequency	$V_{in} = 45\,V$; $V_{out} = 220V_{RMS}$; $P_{out} = 205\,W$	94%	35 V – 75 V	(not specified)

Table 3.1: Comparison table of the previously described resonant and non resonant microinverters.

shading scenarios, thanks to the design of the input stage optimised for a wide input voltage range. The peak efficiency of these converters always overcome 90%, thanks to the optimization of the gating signal algorithm to achieve soft-switching of the semiconductor devices and, often to the adoption of wide bandgap semiconductors. Whenever possible, the wise exploitation of reactive parasitics intrinsically present in the circuits (transformer leakage and magnetizing inductance, diodes and MOSFETs output capacitances) allowed to realize the desired resonance tank without the need to include additional ad-hoc components. As a result, many of the presented circuits were optimised also from the power density point of view.

One of the possible flaws of the described circuits is the intrinsic limitation in efficiency when the PV module operates far from the nominal STC conditions. When partial shading occurs, indeed, as also outlined in Fig.3.7, the converter is forced to work in a region where losses are increased due to the variation of the control variable. To overcome this intrinsic limitations, the research has proposed creative solutions, like the one described in [31], which is based on the concept of topology-morphing. The resonant circuit described in the paper embeds a hybrid secondary-side rectifier (composed of two diodes and two MOSFETs) which, according to the instantaneous input voltage, can work as a conventional full-wave rectifier (unity gain), or as a voltage-doubler rectifier (doubled voltage). In this way, two optimal operating conditions (two efficiency peaks) can be achieved at different input voltages, with unity and doubled gain of the rectifier, respectively. In between the two peaks, the efficiency is almost flat (details can be found in the paper). Actually, this converter is designed for high input voltage ranges and for traction batteries charging; moreover, the desirable feature of almost flat gain comes at the expense of a more complex control scheme.

As a consequence, after careful considerations on the feasibility to provide an element of innovation in the field of solar microinverters, which already seems to exhibit optimised solutions from both the efficiency and input voltage range points of view, this work has moved to the outline of the state of the art in another field of application, always connected to solar energy conversion through resonant converters: low-voltage battery chargers. The reasons of this choice will be better clarified in the following section, and are connected to the relatively higher margin of improvement of the performances of current state of the art battery chargers.

3.2 Low-voltage resonant battery chargers

3.2.1 Single-stage resonant battery chargers

In this section, similarly to the previous one, the current state of the art of resonant power converters adopted for low-voltage battery charging applications is outlined. For each topology, the circuit is graphically reported and its operating principles analysed, to understand what solutions the authors explored to increase the performances in terms of efficiency and power density. In this application, the main figures of merit outlined in every publication are the following ones:

- charging efficiency, which, according to the EN 62509:2011 standard [32], is computed for steps of 10% from 10% to 100% of the maximum charging current. The standard defines, specifically for lead-acid low-voltage batteries, the experimental setup and the standard test conditions for *Battery Charge Controller* (BCC) systems supplied by PV modules. A high charging efficiency allows to minimize the temperature increase of the converter;
- the power density, which is in turns linked to the number of components of the converter;
- the charging current ripple, which should be maintained low for a safe charging operation, without temporary overcurrents.

The voltage requirements of a 12 V battery are significantly low compared to the DC-link voltage necessary for a DC-AC conversion stage of a solar microinverter. To enable a charging process in a 12 V battery, for instance, as also specified in [32], a typical voltage of 2.2 V/cell is needed (13.2 V for a 6 cell standard lead-acid battery). As a consequence, given the typical open circuit voltages of the commercial PV modules (few tens of volts), only step-down converters are required. This is why all the converters analysed in this section are single-stage: with such low requirements on the step-down gain, an additional stage would be unnecessary and would decrease the conversion efficiency. Actually, almost all the presented battery chargers are not explicitely addressed to photovoltaic applications, and consequently, do not provide any mention to MPPT techniques. The integration of a PV source is one of the possible paths of innovation in the field of low-voltage battery chargers.

Moreover, this kind of application allows to decrease the voltage ratings of semiconductor and passive devices, and, due to the charging current limitations for a safe charging process, involves lower power levels, up to 100 W typically. Isolated *LLC* resonant converters, which were largely exploited in the previous converters for their possibility to step-up the voltage with high efficiency, are here replaced,

in many cases, by quasi-resonant converters, where semiconductor switches are equipped with resonant elements to achieve their soft-switching. For simplicity, the batteries in the following schematics are modeled by constant voltage DC sources. After presenting the converters, an overall comparison is presented as before.

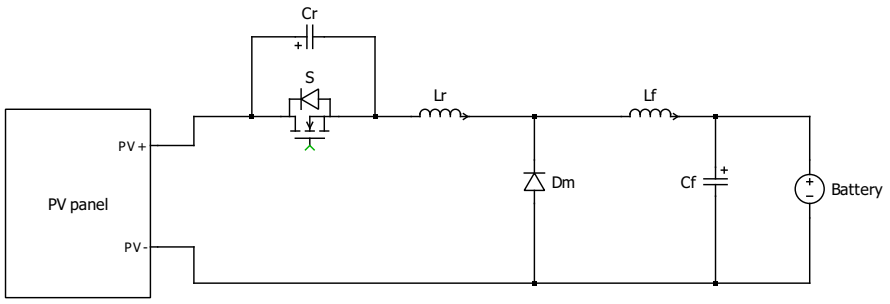
The first converter is proposed in [33] and shown in Fig.3.8a. The converter consists in a simple buck-converter where the main MOSFET S has been replaced by a ZVS quasi-resonant switch (capacitor C_{r} in parallel, inductor L_{r} in series with the parallel structure). The parallel capacitor is intended to limit the voltage derivative $\frac{dv}{dt}$ during the commutations of the power MOSFET and to resonate with the inductor L_{r} to generate a voltage pulse. The second order low-pass filter (L_{f} and C_{f}) filters out the switching ripple and allows to maintain a constant voltage across the battery. In the analysis, the filter is assumed to behave as a constant current sink throughout a cycle.

Within a switching cycle, as all the quasi-resonant converters, there is a sequence of non-resonant and resonant modes. The resonant mode is activated when the main switch is OFF and the diode D_{m} is ON: during this mode, the capacitor voltage exhibits a unipolar pulse which is concluded when the body diode of S is becomes forward-biased. Thanks to this operation, the switch S is turned ON at zero voltage. At the same time, when S is turned ON, the diode D_{m} is turned OFF at zero current, when the L_{r} current linearly increases up to the load current.

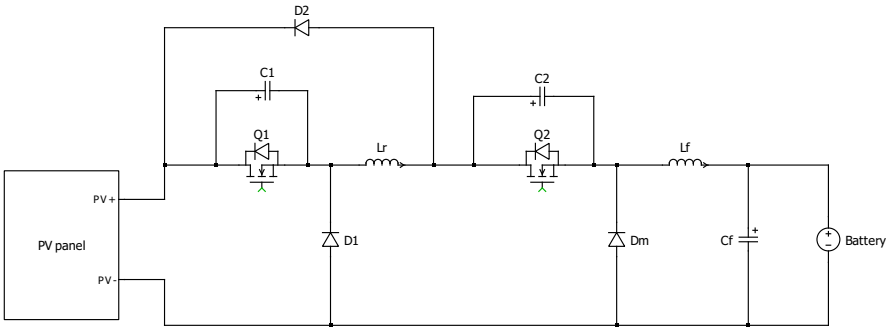
The duration of the ON time of the switch (equivalently, its conduction angle) determines the average output power delivered to the battery. Assuming to work with a fixed OFF time, the result is a frequency modulation technique, where the switching frequency must be sufficiently low to ensure the completion of the capacitor voltage pulse to achieve the desired ZVS of the switch.

The same authors proposed in [34] a zero-voltage-transition resonant converter (Fig-3.8b). As described in the paper, the ZVT concept tries to limit the voltage stresses of active devices that are typical of resonant and quasi-resonant converters (as in [33]). The buck-derived topology includes due additional clamp diodes (D_1 and D_2) and an auxiliary switch Q_2, whose conduction angle determines the voltage gain of the converter.

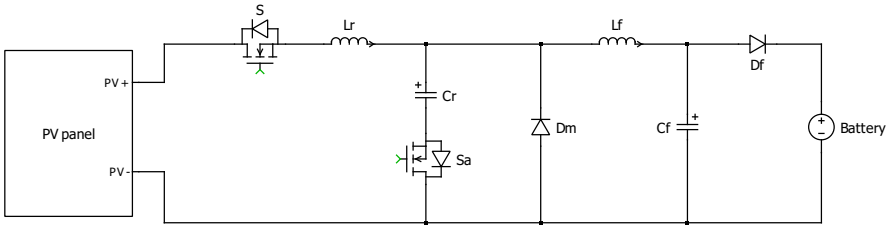
The presence of D_1 and D_2 allows to clamp the capacitor C_1 voltage to the input voltage, in turns limiting the voltage stresses across the main switch Q_1. At the same time, the multi-resonance among L_{r}, C_1 and C_2 allows to turn both the MOSFETs ON at zero voltage. The authors show in the paper that the ZVT buck converter, compared with a conventional PWM buck one, allows to decrease the temperature during the charging process by 20^o, for the same operating conditions and filter components.



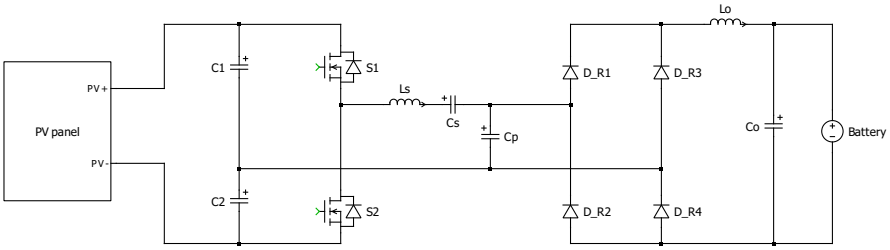
(a) Resonant ZVS buck converter [33].



(b) Resonant ZVT buck converter [34].



(c) Resonant ZCS buck converter [35].



(d) Resonant half-bridge series-parallel converter [36].

Figure 3.8: Resonant single-stage battery chargers.

A ZCS buck converter is proposed in [35] (Fig.3.8c). The basic principle is to adopt an auxiliary branch and a series resonant tank (L_r and C_r) to shape the

main MOSFET S current in order to offer a zero-current condition for turn OFF. The auxiliary switch S_{a} also turns ON with zero current.

Moreover, the presence of capacitor C_{r} in parallel to the freewheeling diode D_{m} and the conduction scheme of S_{a} allow to turn D_{m} ON with ZV and ZC simultaneously.

Contrarily to the previous frequency-modulated converters, which generate harmonics at frequencies that are dependent on the instantaneous power level, here the converter can operate at a fixed frequency: the power regulation is achieved through the control of the auxiliary switch S_{a} conduction angle, in turns resulting a better predictability of the harmonic content.

A class-D half-bridge series-parallel resonant converter is presented in [36] (Fig.3.8d). The choice of a series-parallel converter is based on the exploitation of the combined advantages of a series resonant converter (relatively high part-load efficiency) and of a parallel resonant converter (possibility of voltage regulation even at no-load or light loads). The operating principle of this converter differs from the previous quasi-resonant ones and recalls the LLC resonant architectures presented above in this work. The LCC resonant tank is indeed designed to generate a full-wave sinusoidal L_{s} current and C_{p} voltage, that is rectified at the output. Since the half bridge MOSFETs are operated at a switching frequency slightly higher than the tank resonance frequency:

- the circuit can be modelled by recurring to the first harmonic approximation (FHA);
- the circuit is operated in the inductive region: as a consequence, the lagging inductor current exhibits the correct polarity to discharge the output capacitances of the switch to be turned ON (ZVS turn ON).

The average charging current can be adjusted by modifying the tank impedance through a variation of the switching frequency. The presence of input capacitors across the half-bridge MOSFETs allows to limit their voltage ratings to the input voltage (reduced voltage stresses, differently from traditional quasi-resonant converters, in which the voltage stresses may be as high as twice the input voltage, as in [33]).

3.2.2 Dual-stage resonant battery chargers

A dual-stage resonant battery charger is proposed in [37] and shown in Fig.3.9. Contrarily to the previous topologies, this one specifically addresses the possibility to interface a PV source and, as a consequence, includes a first conversion stage (a traditional PWM boost converter, L_{k}, S_{o}, D_{m} and C_{o}) endowed with a MPPT control scheme. The two stages are decoupled by capacitor C_{o}.

The parallel-loaded resonant circuit can be operated in step-up or step-down mode: indeed, the quality factor of the resonant tank (which determines the voltage transcharacteristic) can be designed according to the number of cells of the battery to be charged.

As in the previous series-parallel resonant converter, the switching frequency is set to be larger than the resonance frequency of the tank (L_r and C_r) to work in the inductive region and, thus, to achieve ZVS of the half bridge switches.

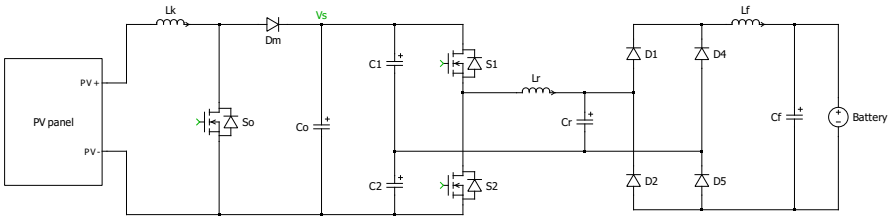


Figure 3.9: Resonant dual-stage battery charger [37].

3.2.3 Constant power charger

In this section, a constant power charger is described in more details. The reasons will be better clarified at the end of this chapter and are related to the high improvement potential of this converter. This topology will be considered as the starting point for the design of a novel battery charger to be interfaced with a PV module, feature which is not considered in the original converter.

The converter is proposed in [38] and shown in Fig.3.10. The topology is composed of:

- an input half-bridge based on Silicon MOSFETs M_1 and M_2. The switches are controlled with switching frequency f_s and 50% duty cycle, to ensure a symmetrical operation. The conduction intervals are separated by a small blanking time, to avoid cross-conduction;

- two equal capacitors C_1 and C_2, realizing a voltage partition at node B. Clamping diodes D_1 and D_2 are connected in parallel to each of them, to clamp their voltages between 0 V and V_i (neglecting the forward voltages of the diodes);

- a small inductor L_r whose goal, as will be explained, is to assist the ZVS half bridge MOSFETs turn ON, by buffering the energy stored in the parasitic output capacitances $C_{\mathrm{s}1}$ and $C_{\mathrm{s}2}$ (explicited in Fig.3.10);

- a step-down center-tapped transformer with turns ratio N_s/N_p;
- at the secondary side of the transformer, the primary voltage is stepped down and rectified by diodes D_3 and D_4;
- a large filter inductor L_o. Through the entire analysis, this inductor is assumed to keep the output current (the charging current) constant.

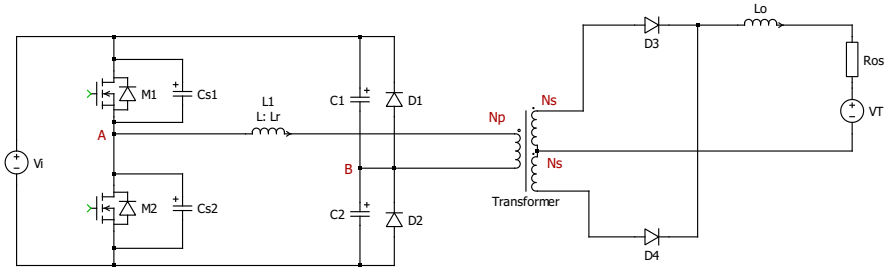


Figure 3.10: Constant power charger with soft-switching and power factor correction [38].

The converter is designed to charge a low-voltage battery (lead-acid, $12V$) from the grid: V_i represents the rectified sinusoidal output of a rectifying stage (not shown). The operation of the circuit can be described on a switching cycle level, to highlight how power is transferred at each cycle, and on a mains cycle level, to outline the averaged transferred power and the input impedance "seen" by the grid. The switching frequency is chosen to be much larger than the mains frequency: if this is true, the input voltage can be assumed to be constant within a switching cycle, and this allows to carry out the switching cycle-level analysis without considering the dynamics of the grid.

The converter realizes a constant-power charger (CP), which represents a third alternative to more common constant-voltage (CV) and constant-current (CC) charging techniques. These charging modes, indeed, exhibit specific drawbacks such as a large dissipation at the starting interval of constant-voltage mode, or risk of overcharging the battery in the last stages of the constant-current mode. This is the reason why these modes are typically combined into a CC-CV mode to provide a controlled charging current at the first stages (through constant-current charging) by avoiding an overcharge in the last stages (constant-voltage charging). The constant-power approach allows to intrinsically limit the charging power without the need to complicate the charging control.

Operation in a switching cycle

The operation of the converter is based on the transfer to the load of a discretized amount of energy which is, in the first half of the switching cycle, stored in capacitors C_1 or C_2, and then released in the second half. Since, in a switching cycle, the input voltage is assumed to be constant, the two capacitors store and release energy in a complementary way. The operation in a switching cycle can be divided into three modes for each half cycle [39]:

- *Power transfer state.* This mode begins when M_1 is turned ON. During its conduction period, the primary voltage of the transformer is positive, diode D_3 is forward biased and the primary current, whose value is obtained by re-scaling the load current by $N_\mathrm{s}/N_\mathrm{p}$, flows from node A to node B. During this half cycle, the voltage at node B increases linearly (assuming constant load current), C_1 discharges and C_2 charges. This mode ends when the node B voltage rises up until the clamping diode D_1 is turned ON. The duration of this mode can be computed assuming linear increase of node B voltage:

$$t_\mathrm{A} = \frac{(V_\mathrm{i} - V_{\mathrm{i},0})(C_1 + C_2)}{I_\mathrm{p}}\,, \tag{3.5}$$

  where I_p represents the primary side current and $V_{\mathrm{i},0}$ the initial voltage value, derived from the last mode of the previous half cycle;

- *Current circulating state.* When the clamping diode D_1 starts conducting, the primary current flows in a freewheeling loop, interrupting the charging/discharging process of capacitors C_1 and C_2. Assuming a negligible forward voltage of the diode, the primary side voltage of the transformer is approximately zero, and then there is no power transfer to the secondary side. The converter is frequency modulated, indeed the duration of this mode, for the same energy stored in capacitor C_2, determines the amount of average power transfer. The second mode ends when MOSFET M_1 is turned OFF;

- *Crossover resonant state.* This mode, whose duration is much shorter, occurs during the primary current reversal and can itself be subdivided into three submodes. During the first one, starting with M_1 turn OFF, the small inductor L_r resonates with the output capacitances $C_{\mathrm{s}1}$ and $C_{\mathrm{s}2}$ of the MOSFETs. The inductor exchanges energy with the capacitors, by pushing down the voltage at node A down to the point where the body diode of M_2 starts conducting. The inductor L_r, despite small, should satisfy the condition to store a sufficient amount of energy to assist the capacitors charge/discharge:

$$L_\mathrm{r} I_\mathrm{p}^2 > (C_{\mathrm{s}1} + C_{\mathrm{s}2}) V_\mathrm{i}^2\,. \tag{3.6}$$

At the same time, an upper boundary for L_r can also be defined from the condition that the energy stored in the inductor is anyway much lower than the amount of energy stored and released by capacitors C_1 and C_2. This condition results in:

$$L_r \ll \frac{1}{4(C_1 + C_2)} \left(\frac{V_T N_p}{V_i f_{sw} N_s} \right)^2 . \tag{3.7}$$

The duration of this resonant sub-mode t' is derived by imposing the voltage at node A to reach zero:

$$t' = \frac{1}{\omega_{res}} \sin^{-1} \left(\frac{V_i (C_{s1} + C_{s2})}{I_p} \right), \tag{3.8}$$

where $\omega_{res} = \frac{1}{\sqrt{L_r (C_{s1} + C_{s2})}}$.

In the second sub-mode, MOSFET M_2 is still OFF and its body diode conducts, until the primary side current is positive. During this interval of time, the voltage across the inductor is fixed to be around $-V_i$ (assuming negligible forward voltages of the diodes). As a result, the primary current linearly decreases towards zero. To achieve ZVS turn ON, M_2 should be programmed to be turned ON in this interval, before the current polarity reversal. Considering the initial value of the current from the previous mode, the time required for the current to drop to 0 is:

$$t'' = \frac{L_r I_p \cos(\omega_{res} t')}{V_i} . \tag{3.9}$$

If M_2 is controlled to be turned ON later, the primary current reverses and starts again to exchange energy with the output capacitances, increasing again the voltage at node A. During this sub-mode, both the secondary side diodes conduct the load current: specifically, D_4 current increases whereas D_3 current decreases. When M_2 is turned ON, the third sub-mode begins and lasts until the primary side current has reached the nominal value $-I_o \frac{N_s}{N_p}$. When the polarity reversal of the current occurs, the clamping diode D_1 does not conduct more, and L_r resonates with capacitors C_1 and C_2. The duration of this mode can be easily computed imposing the resonant current to be $-I_p$:

$$t''' = \frac{1}{\omega_{res,2}} \sin^{-1} \left(\frac{I_p L_r \omega_{res,2}}{V_i} \right), \tag{3.10}$$

where $\omega_{res,2} = \frac{1}{\sqrt{L_r (C_1 + C_2)}}$. The final voltage value of node B constitutes the starting condition for the *power transfer mode* of the negative half cycle ($V_{i,0}$).

Fig.3.11 shows two significant waveforms of the circuit: the node B voltage (voltage across C_2) and the primary side current. As clearly visible, the primary side current consists in a quasi-square wave, whose amplitude is a rescaled version of the load current (assumed constant within a cycle). As a consequence, the node B voltage, during the first modes of each half cycle, linearly increases/decreases, whereas is clamped during the *circulating current mode*. The third mode duration is definitely shorter than the other two modes. Voluntarily, the capacitance values are designed to be sufficiently low to allow a complete charge/discharge: as a result, the converter is said to be operated in *discontinuous voltage mode*. To achieve this condition, however, the switching frequency must be ensured to be sufficiently low to enable the second mode:

$$f_{\mathrm{sw}} < f_{\max} = \frac{1}{2(t_{\mathrm{A}} + t' + t'' + t''')} \,. \tag{3.11}$$

Since the duration of each mode depends on the input voltage, the switching frequency should be chosen to satisfy this condition for any operating voltage.

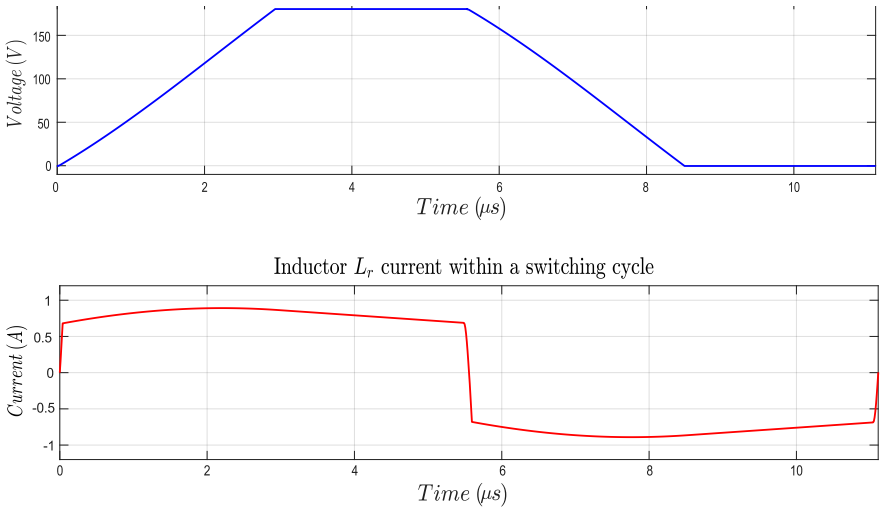


Figure 3.11: Node B voltage and inductor L_{r} current waveforms within a switching cycle.

The operation during the second half cycle is exactly complementary.

Operation in a mains cycle

As mentioned, this converter is designed to recharge a battery from the grid. As a result, the input voltage of the converter describes a rectified sinusoid and, consequently, the instantaneous power delivered to the load varies through a mains

cycle. However, due to the discontinuous voltage mode and frequency modulation, and assuming a negligible contribution of L_r on the overall transferred energy, what can be proved is that:

$$P_{out} \approx (C_1 + C_2) f_{sw} V_i^2 \,, \tag{3.12}$$

corresponding to applying an equivalent resistive input impedance $R_{in} = \frac{1}{f_{sw}(C_1+C_2)}$ to the rectified grid voltage. As a result, this converter intrinsically works with high power factors approaching the unity.

Actually, the above-described operation is achieved only when the input voltage satisfies the following constraint:

$$V_i(t) > 2\frac{N_p}{N_s} V_T \,. \tag{3.13}$$

This constraint comes from the output inductor L_o volts-seconds balance: the stationary operation of the converter can be sustained only if this condition is satisfied.

The mains-cycle operation can itself be divided into four stages, here briefly summarized:

- during the short first stage ($0 < t < \tau_0$), the input voltage is lower than a threshold voltage defined by the residual stored energy in capacitors C_1 and C_2. No input current flows in this mode;

- during the second stage ($\tau_0 < t < \tau_1$), although the input voltage overcomes the above mentioned threshold voltage, it is still too low to satisfy Eq.3.13. As a result, input capacitors are energized but there is still no power flow to the secondary side;

- during the short third stage ($\tau_1 < t < \tau_2$), power begins to flow through the transformer, but the voltage is still to low to work in discontinuous voltage mode: capacitors C_1 and C_2 cannot charge and discharge completely and the *circulating current mode* is absent;

- the longest fourth stage ($\tau_2 < t < \tau_3$) corresponds exactly to the nominal discontinuous voltage mode described until now, with the equivalent resistive input impedance;

- during the last stage ($\tau_3 < t < \tau_4$), the input voltage becomes again too low to sustain the discontinuous voltage mode, and the input current progressively drop to zero at τ_4.

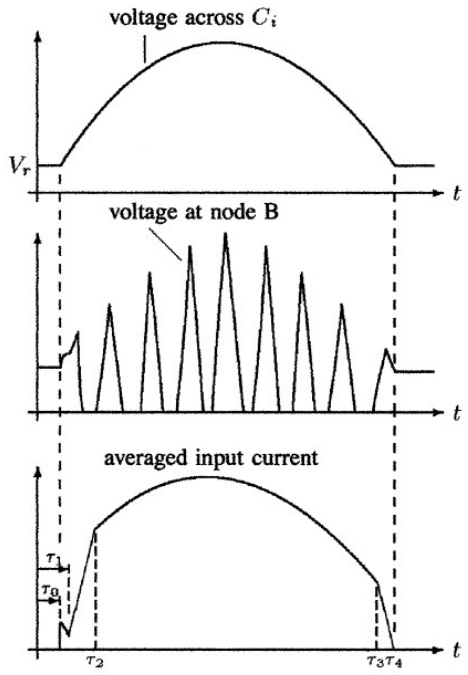


Figure 3.12: Main waveforms during a mains half cycle (from [38]).

Fig.3.12 shows simplified relevant waveforms (input voltage, input current and node B voltage) to summarize the converter behaviour throughout a mains half cycle.

Further details on the equivalent circuits in every stage and the expressions for each time interval can be found in [38]. Integrating the input power over a mains cycle gives the total input power extracted from the grid, which can be estimated by:

$$\mathrm{P_{in}} \approx \frac{(C_1+C_2) f_{\mathrm{sw}} \hat{V}^2}{2\pi} \Big(\cos(\omega_m \tau_2) \sin(\omega_m \tau_2) - \cos(\omega_m \tau_3) \sin(\omega_m \tau_3) + \omega_m \tau_3 - \omega_m \tau_2 \Big) . \tag{3.14}$$

Clearly, all the derivations carried out for a switching cycle should consider that the input voltage is time-variant. An interesting aspect is that, considering constant frequency operation, as the battery voltage increases, the interval of time in which the converter operates in discontinuous voltage mode decreases. As a consequence, the transferred power decreases gradually throughout the charging process, avoiding the risk of overcurrents in the final stages.

The design of switching frequency and dividing capacitors is based on the desired charging power, whereas inductor L_{r} must satisfy the constraints of Eq.3.6 and Eq.3.7. The turns ratio and the number of turns are selected, respectively, according

to the admitted input current and to avoid the transformer core saturation. The maximum efficiency will be reported in the summarizing table at the end of this chapter.

3.2.4 Performance comparison of battery chargers

In this last section of the literature review, concluding remarks are drawn from the overview of the presented topologies. Tab.3.2 reports a comparison in terms of the input voltage adopted for the experimental validation, the peak efficiency, and the control variables for the MPPT and output current control, respectively. Few considerations can be done from this table:

- beside the dual-stage converter presented in [37], all the converters are not designed for a PV module interface. As a consequence, the experimental validation considers a conventional DC voltage source. Actually, the adopted voltages could in principle refer to solar modules: 24 V and 36 V are, for instance, the typical MPP voltages of a 48-cell and 72-cell module, respectively. However, the control schemes, as presented in the articles, are not suited for MPPT. The last topology [38] is, instead, designed for a completely different source (the grid);
- the charging profile adopted in all the converters, beside the constant-power charger [38], is always a combination of constant-current and constant-voltage. Independently on the charging approach, by the way, the charging current decreases in the last charging stages, to avoid overcharging the battery;
- the typical efficiency curve of battery chargers reports the conversion efficiency as function of the charging time. Due to the previous consideration on the charging profile, efficiency is, in all the converters, higher in the last charging stage, thanks to the reduction of conduction losses in all the components. In the table, only the peak efficiency is reported.

A second interesting comparison could be made on the basis of the number of components, both active and passive (Tab.3.3). The ZCS and ZVT buck-derived converters include additional power devices and reactive components to realize resonance and, at the same time, avoiding larger current/voltage stresses on the main switches. The half bridge structures realized in [36], [37] and [38], instead, intrinsically allow to bound the voltage stresses to the input voltage. In these converters, the exploitation of a magnetizing inductance or an additional discrete inductance can offer the possibility to achieve ZVS of the input switches. One of the main drawbacks of half-bridge-based converters, however, is the need to rectify the primary AC voltage. Rectifiers increase the amount of semiconductor

Battery charger topology	Input voltage	Peak efficiency	Control variable (MPPT)	Control variable (output current)
ZVS Buck converter [33]	24 V	87%	(not provided)	Switching frequency ($< f_{res}$)
ZVT multiresonant buck converter [34]	36 V	90.1%	(not provided)	Q_2 conduction time (duty cycle)
ZCS resonant buck converter [35]	20 V	90.3%	(not provided)	S_a conduction time (duty cycle)
Half-bridge series-parallel resonant converter [36]	40 V	94%	(not provided)	Switching frequency ($> f_{res}$)
Dual-stage boost parallel resonant battery charger [37]	24 V	92%	Boost switch duty cycle	Half bridge switching frequency
Constant-power battery charger [38]	Rectified grid voltage	88%	(not provided)	Half bridge switching frequency

Table 3.2: Comparison of the presented low-voltage battery chargers.

devices needed and, especially when passive rectifiers are exploited, may lead to a significant increase of conduction and switching losses.

For all of these reasons, the reported efficiencies of these battery chargers are almost always upper bounded by 90%. This work starts from the topology presented in [38], which is interesting for multiple reasons (intrinsic power limitation, input switches ZVS), to develop a new converter for low-voltage battery charging applications from a PV module. At the same time, as will be explained, the novel topology will try to overcome the efficiency limitations of the original one, such as the adoption of a hard-switched passive rectifier. The following two chapters introduce a detailed analysis on the operating principles and switching-cycle operation of two possible improvements of this converter. The difference between the two, as will be pointed out, stands in the value of resonant inductor.

Battery charger topology	**Number of power semiconductor devices**	**Number of reactive components**
ZVS Buck converter [33]	1 switch, 1 diode	2 inductors, 2 capacitors
ZVT multiresonant buck converter [34]	2 switches, 3 diodes	2 inductors, 2 capacitors
ZCS resonant buck converter [35]	2 switches, 3 diodes	2 inductors, 2 capacitors
Half-bridge series-parallel resonant converter [36]	2 switches, 4 diodes	2 inductors, 5 capacitors
Dual-stage boost parallel resonant battery charger [37]	3 switches, 5 diodes	3 inductors, 4 capacitors
Constant-power battery charger [38]	2 switches, 4 diodes	1 transformer, 2 inductors, 2 capacitors

Table 3.3: Comparison of the presented low-voltage battery chargers on the basis of the components count.

Chapter 4

Proposed constant-power charger

4.1 General features

In this chapter, a novel low-voltage battery charger based on the working principles of the one in [38] is presented. The converter topology is shown in Fig.4.1. As it can be seen, it presents similar topological features but also relevant differences with the original converter.

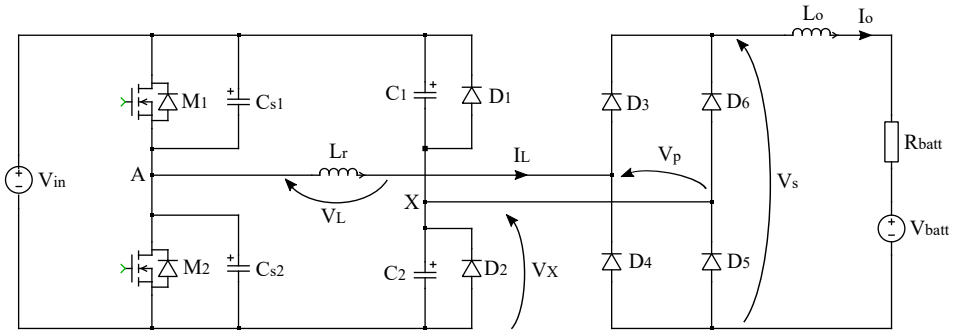


Figure 4.1: Schematic of the novel low voltage battery charger analysed in this work.

The first fundamental difference concerns the power source. The converter presented in [38] was intended to be supplied from the grid, through an input line-frequency rectifier stage. This converter, instead, is voluntarily designed to be interfaced with a PV module: as a result, to the purpose of analysing its behaviour through a switching cycle, a more appropriate equivalent circuit consists in a DC

voltage source V_{in}. The non-linearity of a PV module electrical characteristic will be taken into account later on in this work. In a physical implementation, a capacitive filter, not shown, would be designed to provide a stable voltage against input current fluctuations). The source negative terminal is taken as reference for the converter voltages.

Beside the source, the input DC-AC stage is substantially equal and is composed of:

- a half bridge structure with MOSFETs M_1 and M_2 controlled with 180^o phase shift and 50% duty cycle (slightly less, in order to avoid cross-conduction in presence of non-instantaneous commutations). The control algorithm produces a square wave voltage with $\frac{V_{\text{in}}}{2}$ average value. The output parasitic capacitances of the MOSFETs (C_{s1} and C_{s2}), which play a major role in the switching behaviour of the devices, are explicitly shown;
- two dividing capacitors C_1 and C_2, each one connected in parallel to a clamping diode (D_1 and D_2). The intermediate node voltage (the voltage across capacitor C_2) is denominated v_{x} in the following derivations;
- a small inductor L_{r}, whose inductance value is designed to provide ZVS of the half-bridge MOSFETs. For the following derivations, the adopted convention for the inductor current I_L is a left-to-right direction, and its voltage v_L points to node A.

The rectifying stage mainly differs from the converter in [38] for the absence of a transformer. Typical commercial PV modules exhibit, indeed, according to the number of their series-connected cells, voltages in the order of some tens of V. Such low voltages, comparable with the load voltage (around $12V$ for a typical lead-acid 6-cell battery) do not strictly require to galvanically isolate the input and output sides, or to provide consistent step-up or step-down gains. The rectifying stage of the converter, consequently, consists in a diode-based Graetz bridge (diodes D_3, D_4, D_5 and D_6) realizing a full-wave rectification of the AC primary voltage v_{p}. The rectified voltage v_{s} is filtered out by a large output inductor L_{o} and supplies the battery. As in [38], the battery is represented by a simple Thevenin equivalent circuit consisting in a slowly varying DC voltage generator V_{batt} and a small internal resistance R_{batt}. The dynamic model of the battery, taking into account the dependence on the state-of-charge, is not considered due to the large time constants compared to the switching behaviour of the converter. The large output filter inductor is, for the following derivations, assumed to be so large to keep the charging current constant at I_{o} within a switching cycle: its goal, then, is to decouple the switching dynamics from the averaged output characteristic of the converter.

Thanks to the symmetric structure and control of the converter, its operation can be divided into two equally long sub-intervals corresponding to the halves of the switching period T_{sw}. The power transfer principle is the same as in [38]. When M_1 is turned ON, a positive primary voltage at the input of the rectifier turns ON diodes D_3 and D_5, which conduct the nearly constant load current I_o. The same current, in its return path, causes a linear charge of C_1 and discharge of C_2, up to the point at which v_x is clamped by the diode D_1. The operation is analogue during the conduction time of M_2, but the load current flows through the other pair of rectifier diodes (D_4 and D_6), charges C_1 and discharges C_2. The detailed analysis of the relevant waveforms during the switching period is provided in the following section.

The overall principle is still based on the transfer of fixed amounts of energy (the energy alternatively stored and released in capacitors C_1 and C_2). The clamping diodes allows to achieve the discontinuous voltage mode already exploited in [38], and the averaged transferred power can be set by selecting the duration of the previously analysed *current circulating* mode. Consequently, this converter realizes a frequency-modulated battery charger. One of the main benefits of this approach is, once again, the intrinsic output power limitation, which is related to the limited amount of energy that can be alternatively stored and released by the dividing capacitors.

As already highlighted in [38], the proposed converter, under specific circumstances (namely, too low input voltage) could not be operated in the nominal and desired Discontinuous Voltage Mode (DVM), where the power transfer is predictably related to the amount of energy stored in the dividing capacitors. The entire design, starting from the transformer turns ratio and the frequency selection, is based on the maximisation of the mains cycle interval in which the DVM is obtained. However, the work does not provide an accurate description of the working operation when the conditions for DVM are not met. This works, instead, in order to fully characterise the converter, provides a detailed analysis of the working operation of the converter through its two main operating regions. As it will be described, above a certain frequency, whose value is function of input and battery voltages, and the design parametres, the converter can no more operate in DVM, meaning that the dividing capacitors store and release an amount of energy lower than $2CV_{in}^2$. The static characteristic $P_{out}(f_{sw})$ starts becoming non linear above this frequency. The characterization of the converter in this operating region enables a second possibility for a frequency modulation of the converter.

4.2 Working operation in the low frequency region

In this section, a detailed derivation of the governing equations and relevant waveforms of the converter operation are analysed. Due to the symmetric operation, only a single half-cycle is taken in analysis. In this derivation, the half-cycle in which M_1 is conducting is considered.

The following assumptions are considered to simplify the analysis:

- the voltage source is assumed to be constant within the switching period;
- the load current, due to the presence of a large filter inductor at the output side, is constant within the switching period;
- when the MOSFETs are conducting, their voltage is assumed to be null. In other terms, their $R_{\mathrm{DS,ON}}$ is considered to be negligible. The output capacitances are the only parasitics considered in the derivation. When the MOSFET is OFF but its body diode is conducting, it is modelled by a negative DC drain-source voltage source equal to $-V_{\mathrm{F,M}}$;
- all the diodes (from D_1 to D_6) are equal and are modelled by constant DC voltage sources $V_{\mathrm{F,D}}$ while they conduct. No reactive parasitic nor forward/reverse recovery is considered: as a consequence, their commutation is instantaneous;
- the reactive components C_1, C_2, L_{r} and L_{o} are lossless and ideal. Moreover, $C_1 = C_2 = C$.

These assumptions allows to reasonably simplify the governing equations and to derive explicit waveform behaviors. The relevant waveforms considered in the derivation are C_2 voltage v_{x}, inductor L_{r} voltage and current v_L/i_L, diode D_3 and D_4 currents (D_5 and D_6 currents are respectively identical), the input and output voltages of the rectifier v_{p} and v_{s}. The operation during a half switching cycle can be divided into 3 modes.

4.2.1 Power transfer mode

This mode starts when the AC current flowing through L_{r} has just reversed from the negative half-wave and reached the nominal value I_{o}. M_1 is ON and M_2 is OFF. The initial value of v_{x}, which will be derived by studying the end of the previous mode, is defined to be $V_{\mathrm{x,0}}$ and is slightly positive. During this mode, the voltage $v_{\mathrm{AX}}(t) = V_{\mathrm{in}} - v_{\mathrm{x}}(t)$ is always positive and turns ON diodes D_3 and D_5. Since the

L_r current is "latched" to the constant load current I_o, v_L is null and the primary voltage is exactly equal to v_AX. The rectified voltage v_s differs from v_p for two diodes voltage drops. Fig.4.2a shows in red the conducting devices, and highlights the direction of the current flows in the converter during this mode.

The Kirchhoff Current Law (KCL) at node X allows to describe the charging/discharging process of the dividing capacitors:

$$I_\mathrm{o} = C_2\frac{dv_\mathrm{x}}{dt} - C_1\frac{d}{dt}(V_\mathrm{in} - v_\mathrm{x}) = (C_1 + C_2)\frac{dv_\mathrm{x}}{dt} = 2C\frac{dv_\mathrm{x}}{dt}\,. \tag{4.1}$$

As a result, since I_o is constant, a simultaneous linear charge of C_2 and linear discharge of C_1 occurs:

$$\begin{cases} v_{\mathrm{C}_2}(t) = v_\mathrm{x}(t) = V_{\mathrm{x},0} + \dfrac{I_\mathrm{o}}{2C}(t - t_0) \\ v_{\mathrm{C}_1}(t) = V_\mathrm{in} - v_\mathrm{x}(t) = V_\mathrm{in} - V_{\mathrm{x},0} - \dfrac{I_\mathrm{o}}{2C}(t - t_0) \end{cases}, \tag{4.2}$$

where t_0 is the initial instant of the mode interval.

Eq.4.7 summarizes the relevant waveforms behaviour during this first mode:

$$\begin{cases} v_\mathrm{x}(t) = V_{\mathrm{x},0} + \dfrac{I_\mathrm{o}}{2C}(t - t_0) \\ v_L(t) = 0 \\ i_L = I_\mathrm{o} \\ v_\mathrm{p}(t) = V_\mathrm{in} - v_\mathrm{x}(t) = V_\mathrm{in} - V_{\mathrm{x},0} - \dfrac{I_\mathrm{o}}{2C}(t - t_0) \\ v_\mathrm{s}(t) = v_\mathrm{p}(t) - 2V_\mathrm{F,D} = V_\mathrm{in} - V_{\mathrm{x},0} - 2V_\mathrm{F,D} - \dfrac{I_\mathrm{o}}{2C}(t - t_0) \\ i_{\mathrm{D}_3} = I_\mathrm{o} \\ i_{\mathrm{D}_4} = 0 \end{cases}. \tag{4.3}$$

The power transfer mode, as in the converter of [38], is the unique mode where a positive power flows towards the battery side, since the instantaneous product $v_\mathrm{s}(t) \cdot I_\mathrm{o}$ is always positive. The mode ends when the voltage $v_\mathrm{x}(t)$ increases up to the point where the clamping diode D_1 is turned ON. The ending time instant t_1 can be computed by imposing $v_\mathrm{x}(t_1) = V_\mathrm{in} + V_\mathrm{F,D}$, which gives:

$$t_1 = 2C\frac{V_\mathrm{in} + V_\mathrm{F,D} - V_{\mathrm{x},0}}{I_\mathrm{o}}\,. \tag{4.4}$$

4.2.2 Current circulating mode

During the second mode, which is present also in the converter of [38], the load current does not charge/discharge more the dividing capacitors, but flows in a freewheeling loop through the clamping diode D_1. In order to understand which rectifier diodes conduct, it is necessary to make a hypothesis, and to verify it *a posteriori*. If only D_3 and D_4 were turned ON, then inductor L_r would keep conducting the constant load current, and $v_L(t) = 0$. As a consequence, the anode-cathod voltage of D_6 (or, equivalently, of D_4) would be $2V_{\mathrm{F,D}}$. This voltage would be enough to turn the diode ON, so the initial hypothesis results in a contradictory conclusion.

By supposing that, instead, all the four diodes of the rectifier are conducting, the following consequences occur:

- L_r does no more conduct the entire load current, which starts instead to be splitted between the two legs of the Graetz bridge;
- the primary voltage becomes null. As a result, $v_L(t) = -V_{\mathrm{F,D}}$. This slightly negative voltage across the inductor leads to a gradual and linear discharge of the inductor current:

$$i_L(t) = I_\mathrm{o} - \frac{V_{\mathrm{F,D}}}{L_\mathrm{r}}(t - t_1)\,; \tag{4.5}$$

- from the KCL applied at the X node and at the positive terminal of the rectifier output, the diodes currents can be easily derived as:

$$\begin{cases} i_{\mathrm{D}_3}(t) = \dfrac{I_\mathrm{o}}{2} + \dfrac{i_L(t)}{2} = I_\mathrm{o} - \dfrac{V_{\mathrm{F,D}}}{2L_\mathrm{r}}(t - t_1) \\ i_{\mathrm{D}_4}(t) = \dfrac{I_\mathrm{o}}{2} - \dfrac{i_L(t)}{2} = \dfrac{V_{\mathrm{F,D}}}{2L_\mathrm{r}}(t - t_1) \end{cases} . \tag{4.6}$$

As a result:

$$\begin{cases} v_\mathrm{x}(t) = V_\mathrm{in} + V_{\mathrm{F,D}} \\ v_L(t) = -V_{\mathrm{F,D}} \\ i_L(t) = I_\mathrm{o} - \dfrac{V_{\mathrm{F,D}}}{L_\mathrm{r}}(t - t_1) \\ v_\mathrm{p}(t) = 0 \\ v_\mathrm{s}(t) = -2V_{\mathrm{F,D}} \\ i_{\mathrm{D}_3}(t) = \dfrac{I_\mathrm{o}}{2} + \dfrac{i_L(t)}{2} = I_\mathrm{o} - \dfrac{V_{\mathrm{F,D}}}{2L_\mathrm{r}}(t - t_1) \\ i_{\mathrm{D}_4}(t) = \dfrac{I_\mathrm{o}}{2} - \dfrac{i_L(t)}{2} = \dfrac{V_{\mathrm{F,D}}}{2L_\mathrm{r}}(t - t_1) \end{cases} . \tag{4.7}$$

The current circulating mode is not associated to any power transfer: the energy previously stored in L_r is gradually dissipated inside diodes. The duration of this mode, $t_2 - t_1$, determines the amount of averaged transferred power to the battery side. The mode ends when MOSFET M_1 is turned OFF.

4.2.3 Crossover resonant mode

This operating mode, whose duration is shorter than the previous ones, also recalls the analogue third mode of the converter in [38], and is associated to the transition from the positive to the negative half wave of i_L. It can be itself divided in three sub-modes.

Mode 3.1

Once M_1 has been turned OFF, the instantaneous behaviour of the two half-bridge MOSFETs is dictated by their output capacitances. Assuming that the two MOSFETs are equal, $C_{\mathrm{s}1} = C_{\mathrm{s}2} = C_\mathrm{s}$. Due to the slow discharge of the inductor current through the *current circulating mode*, when M_1 is turned OFF, the initial value of i_L, $I_{\mathrm{L},2}$, is still positive, despite lower than I_o:

$$I_{\mathrm{L},2} = I_\mathrm{o} - \frac{V_{\mathrm{F,D}}}{L_\mathrm{r}}(t_2 - t_1)\,. \tag{4.8}$$

During this mode, the behaviour of the voltage at node A (drain-source voltage of the low-side MOSFET) and of the current i_L, both state variables, can be described by a system of two Ordinary Differential Equations (ODEs):

$$\begin{cases} i_L = -2C_\mathrm{s}\dfrac{dv_\mathrm{A}(t)}{dt} \\ L_\mathrm{r}\dfrac{di_L(t)}{dt} = -V_{\mathrm{F.D}} - V_\mathrm{in} + v_\mathrm{A}(t) \end{cases}\,. \tag{4.9}$$

The two equations can easily be decoupled into two second-order ODEs, and solved after defining the initial conditions. For voltage $v_\mathrm{A}(t)$, the following differential equation is derived (for simplification, the time origin is shifted):

$$\begin{cases} v_\mathrm{A}''(t) + \omega_\mathrm{res}^2 v_\mathrm{A}(t) = \omega_\mathrm{res}^2(V_\mathrm{in} + V_{\mathrm{F,D}}) \\ v_\mathrm{A}(0) = V_\mathrm{in} \\ v_\mathrm{A}'(0) = -\dfrac{i_L(0)}{2C_\mathrm{s}} = -\dfrac{I_{\mathrm{L},2}}{2C_\mathrm{s}} \end{cases}\,, \tag{4.10}$$

where $\omega_\mathrm{res} = \frac{1}{\sqrt{2C_\mathrm{s}L_\mathrm{r}}}$ is the resonant frequency of the L_r-C_s tank. The solution of the equation is the following:

$$v_{\mathrm{A}}(t) = V_{\mathrm{in}} + V_{\mathrm{F,D}} - \frac{I_{\mathrm{L,2}}}{2C_{\mathrm{s}}\omega_{\mathrm{res}}} \sin(\omega_{\mathrm{res}} t) - V_{\mathrm{F,D}} \cos(\omega_{\mathrm{res}} t)\,. \tag{4.11}$$

The resonant voltage pulse (and, consequently, the duration of this mode) is limited by the time instant at which v_{A} becomes negative, turning ON the body diode of M_2. Its forward voltage $V_{\mathrm{F,M}}$ clamps the resonant pulse.

An important consideration must be done on the necessary condition to induce a sufficiently large resonant voltage pulse to turn the body diode ON. Since, in this phase, energy is exchanged between the output capacitances and L_{r}, the inductor must store, before M_1 turns OFF, enough energy to charge its output capacitance completely. This results in the following lower bound for L_{r}:

$$L_{\mathrm{r}} > \frac{2C_{\mathrm{s}}V_{\mathrm{in}}^2}{I_{\mathrm{L,2}}^2}\,. \tag{4.12}$$

Since the output capacitances are small (for typical Silicon MOSFET rated $60V$, for instance, up to some hundreds of pF) the duration of this mode is the shortest one among the other modes. As such, to approximate the final expression and to easily determine the interval of time, the *cosine* term of v_{A} can be first-order approximated by $-V_{\mathrm{F,D}}$.

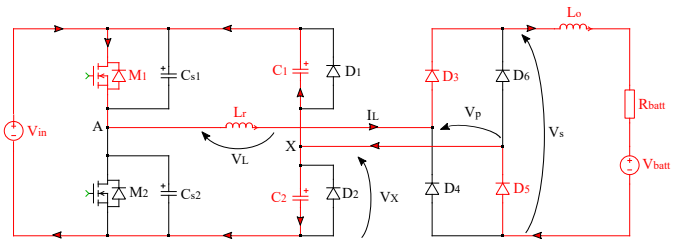
Denoting by t_3 the time instant at which $v_{\mathrm{A}}(t) = -V_{\mathrm{F,M}}$:

$$t_3 \approx \frac{1}{\omega_{\mathrm{res}}} \sin^{-1}\left(\frac{2C_{\mathrm{s}}\omega_{\mathrm{res}}(V_{\mathrm{in}} + V_{\mathrm{F,M}})}{I_{\mathrm{L,2}}}\right). \tag{4.13}$$

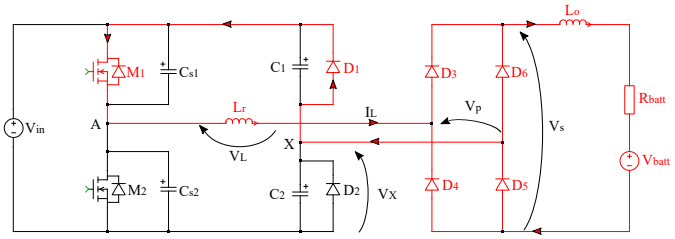
The rectifier diode currents expressions are the same as in the previous mode. The resulting relevant waveforms for this mode, shifted again to the previously adopted time origin, are described by the following expressions:

$$\begin{cases} v_{\mathrm{x}}(t) = V_{\mathrm{in}} + V_{\mathrm{F,D}} \\ v_L(t) \approx -L_{\mathrm{r}}\omega_{\mathrm{res}} I_{\mathrm{L,2}} \sin(\omega_{\mathrm{res}}(t - t_2)) \\ i_L(t) \approx I_{\mathrm{L,2}} \cos(\omega_{\mathrm{res}}(t - t_2)) \\ v_{\mathrm{p}}(t) = 0 \\ v_{\mathrm{s}}(t) = -2V_{\mathrm{F,D}} \\ i_{\mathrm{D_3}}(t) = \dfrac{I_{\mathrm{o}}}{2} + \dfrac{1}{2} I_{\mathrm{L,2}} \cos(\omega_{\mathrm{res}}(t - t_2)) \\ i_{\mathrm{D_4}}(t) = \dfrac{I_{\mathrm{o}}}{2} - \dfrac{1}{2} I_{\mathrm{L,2}} \cos(\omega_{\mathrm{res}}(t - t_2)) \end{cases}. \tag{4.14}$$

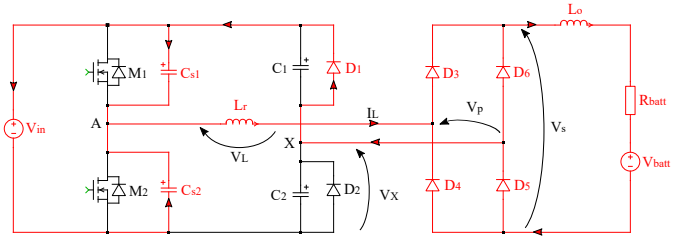
The final value value of the inductor current, helpful for the description of the behaviour at the beginning of the next mode, is denoted by $I_{\mathrm{L,3}} = i_L(t_3)$.



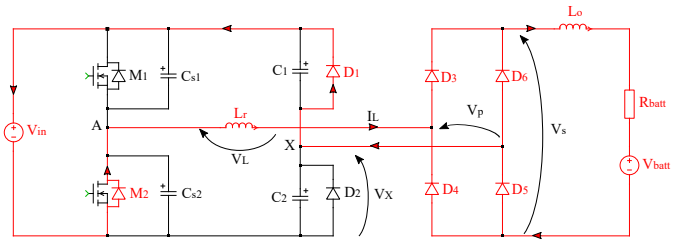
(a) Mode 1.



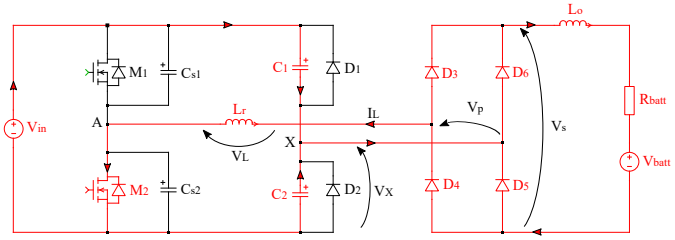
(b) Mode 2.



(c) Mode 3.1.



(d) Mode 3.2.



(e) Mode 3.3.

Figure 4.2: Operation of the novel battery charger during the different modes.

Mode 3.2

Once the body diode of M_2 has started conducting, the voltage across L_r is clamped and maintained at $-V_{\text{in}} - V_{\text{F,D}} - V_{\text{F,M}}$. As a result, the inductor current starts discharging fast and linearly. During this mode, the rectifier diodes currents keep gradually being switched among themselves. The body diode of M_2 can conduct until i_L remains positive. When the current reverses, indeed, it would start again to charge C_{s2} and discharge C_{s1}, forbidding the possibility to turn ON M_2 at zero voltage. For this reason, the control algorithm should turn ON M_2 during the interval of time associated to this mode. The maximum time $t_{\max}$ for which ZVS turn ON can be achieved can be easily derived by imposing to 0 the inductor current:

$$t_{\max} = \frac{L_{\text{r}} I_{\text{L,3}}}{(V_{\text{in}} + V_{\text{F,D}} + V_{\text{F,M}})} \,. \tag{4.15}$$

For simplicity, here it is assumed that M_2 is turned ON exactly at time $t_4 = t_{\max}$, ending this sub-mode at the zero-crossing of i_L. The relevant waveforms are here reported:

$$\begin{cases} v_{\text{x}}(t) = V_{\text{in}} + V_{\text{F,D}} \\ v_L(t) = -V_{\text{in}} - V_{\text{F,D}} - V_{\text{F,M}} \\ i_L(t) = I_{\text{L,3}} - \dfrac{V_{\text{in}} + V_{\text{F,D}} + V_{\text{F,M}}}{L_{\text{r}}}(t - t_3) \\ v_{\text{p}}(t) = 0 \\ v_{\text{s}}(t) = -2V_{\text{F,D}} \\ i_{\text{D}_3}(t) = \dfrac{I_{\text{o}}}{2} + \dfrac{V_{\text{in}} + V_{\text{F,D}} + V_{\text{F,M}}}{2L_{\text{r}}}(t - t_3) \\ i_{\text{D}_4}(t) = \dfrac{I_{\text{o}}}{2} - \dfrac{V_{\text{in}} + V_{\text{F,D}} + V_{\text{F,M}}}{2L_{\text{r}}}(t - t_3) \end{cases} . \tag{4.16}$$

Mode 3.3

In the last sub-mode of the *crossover resonant* state, the inductor current has reversed, but not yet reached the load current value. As a consequence, all the rectifier diodes still conduct. During this mode, as shown in Fig.4.2e, the return current does not flow through the freewheeling diode, but starts discharging C_2 and charging C_1. Another resonant behaviour is induced, but among L_{r} and the dividing capacitors. The following system of ODEs describes the behaviour of i_L

and v_{x} during this mode:

$$\begin{cases} i_L = 2C\dfrac{dv_{\mathrm{x}}(t)}{dt} \\ L_{\mathrm{r}}\dfrac{di_L(t)}{dt} = -v_{\mathrm{x}}(t) \end{cases}, \tag{4.17}$$

whose unknowns can be decoupled. The resulting second-order ODE for $v_{\mathrm{x}}(t)$, considering a shifted time origin, is given by:

$$\begin{cases} v_{\mathrm{x}}''(t) + \omega_{\mathrm{res},2}^2 v_{\mathrm{x}}(t) = 0 \\ v_{\mathrm{x}}(0) = V_{\mathrm{in}} + V_{\mathrm{F,D}} \\ v_{\mathrm{x}}'(0) = \dfrac{i_L(0)}{2C} = 0 \end{cases}, \tag{4.18}$$

where $\omega_{\mathrm{res},2} = \frac{1}{\sqrt{2CL_{\mathrm{r}}}}$ is the resonance frequency of the tank.

From the solution of this system, $v_{\mathrm{x}}(t)$ and, consequently, $i_L(t)$, can be derived. The resulting waveforms are here reported:

$$\begin{cases} v_{\mathrm{x}}(t) = (V_{\mathrm{in}} + V_{\mathrm{F,D}})\cos\left(\omega_{\mathrm{res},2}(t-t_4)\right) \\ v_L(t) = -(V_{\mathrm{in}} + V_{\mathrm{F,D}})\cos\left(\omega_{\mathrm{res},2}(t-t_4)\right) \\ i_L(t) = -2C\omega_{\mathrm{res},2}(V_{\mathrm{in}} + V_{\mathrm{F,D}})\sin\left(\omega_{\mathrm{res},2}(t-t_4)\right) \\ v_{\mathrm{p}}(t) = 0 \\ v_{\mathrm{s}}(t) = -2V_{\mathrm{F,D}} \\ i_{\mathrm{D_3}}(t) = \dfrac{I_{\mathrm{o}}}{2} - C\omega_{\mathrm{res},2}\sin\left(\omega_{\mathrm{res},2}(t-t_4)\right) \\ i_{\mathrm{D_4}}(t) = \dfrac{I_{\mathrm{o}}}{2} + C\omega_{\mathrm{res},2}\sin\left(\omega_{\mathrm{res},2}(t-t_4)\right) \end{cases}. \tag{4.19}$$

The end of this mode coincides with the instant at which i_L reaches $-I_o$:

$$t_5 = \frac{1}{\omega_{\mathrm{res},2}}\sin^{-1}\left(\frac{I_{\mathrm{o}}}{2C\omega_{\mathrm{res},2}(V_{\mathrm{in}} + V_{\mathrm{F,D}})}\right). \tag{4.20}$$

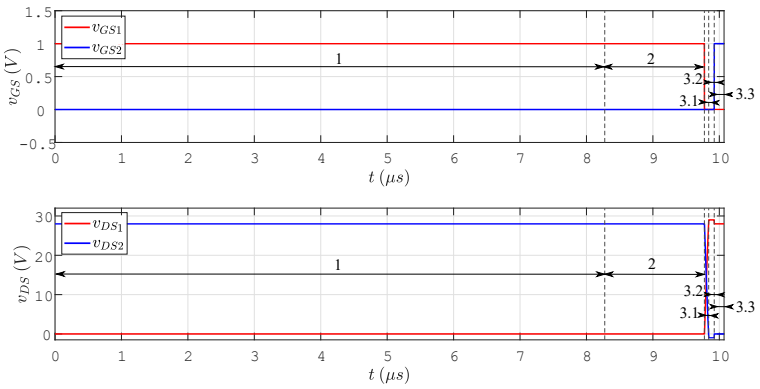
At t_5, the conceptually equal, but complementary, half cycle begins. The remaining quantity to evaluate is the initial value $V_{\mathrm{x},0}$ at the beginning of the *power transfer* mode. This can be derived by symmetry from the final value of v_{x} at t_5:

$$v_{\mathrm{x}}(t_5) = (V_{\mathrm{in}} + V_{\mathrm{F,D}})\sqrt{1 - \left(\frac{I_{\mathrm{o}}}{2C\omega_{\mathrm{res},2}(V_{\mathrm{in}} + V_{\mathrm{F,D}})}\right)^2}. \tag{4.21}$$

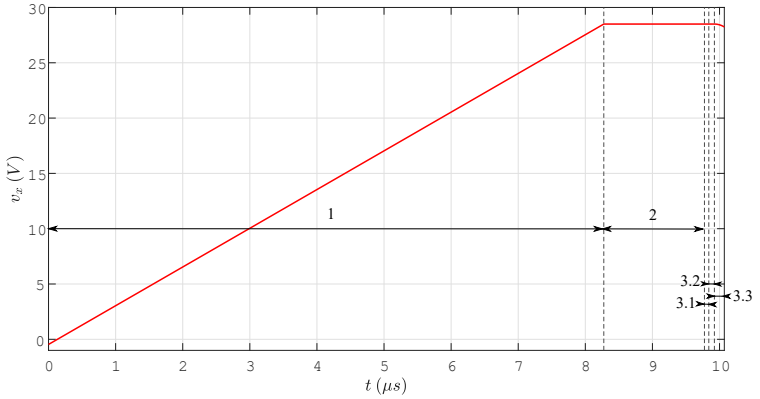
With the same approach followed with the positive half wave:

$$V_{\mathrm{x},0} = V_{\mathrm{in}} - (V_{\mathrm{in}} + V_{\mathrm{F,D}})\sqrt{1 - \left(\frac{I_{\mathrm{o}}}{2C\omega_{\mathrm{res},2}(V_{\mathrm{in}} + V_{\mathrm{F,D}})}\right)^2}. \tag{4.22}$$

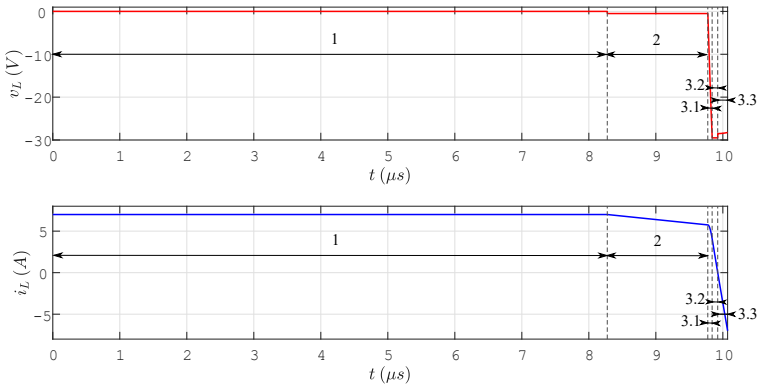
Finally, Fig.4.3 reports the qualitative behaviour of some of the relevant waveforms above-considered. Actually, the duration of the sub-modes of the *crossover resonant* state is exaggerated in the plots to better outline the specific behaviour of the waveforms. Mode 3.1, in particular, involving the charge or discharge of parasitic capacitances, has negligible duration compared to modes 1 or 2 (three or four orders of magnitude lower, typically).



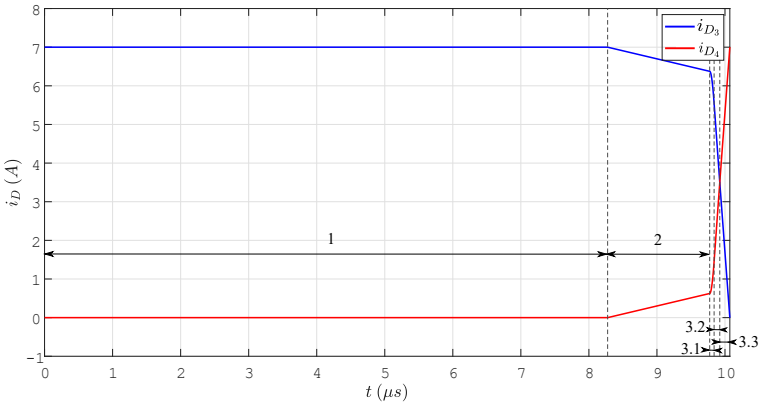
(a) MOSFETs driving signals and output voltages.



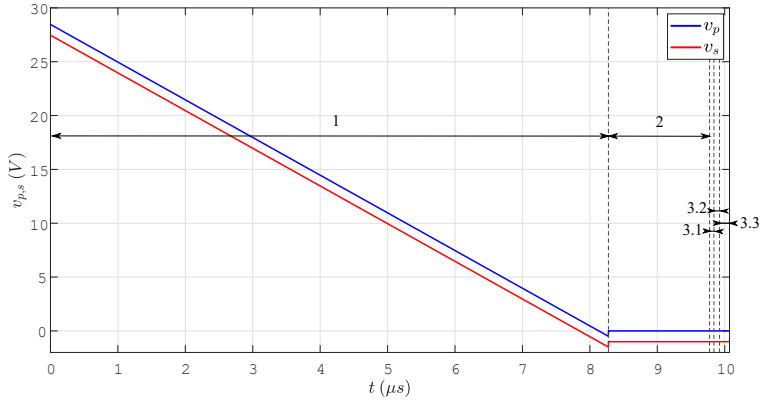
(b) Voltage at node X.



(c) Inductor L_r voltage and current.



(d) Diodes D_3 and D_4 currents.



(e) Input and output voltages of the Graetz bridge rectifier.

Figure 4.3: Some of the relevant waveforms of the analysed converter within a half cycle.

4.3 Working operation in the high frequency region

Until now, the dividing capacitors have been assumed to work always in discontinuous voltage mode, charging and discharging to approximately V_{in} and GND, respectively. As also Poon reports in [38], however, the input voltage, together with the switching frequency selection, may not always be sufficient to induce a complete charge/discharge of the capacitors. This may happen when the input voltage is too low (approximately twice the battery voltage). If the average charging voltage is too low, indeed, the average output current may not be sufficient to work in the discontinuous voltage mode. The same happens when the switching frequency is increased above a certain limit (this can be analytically derived, and will be done in the following section): at larger frequency, the contribution of the L_{r} reactance begins to influence the static characteristic. A qualitative explanation, which will be supported by analytical derivations, in the following one: as the switching period decreases, the time interval required to reverse completely the L_{r} current, during which there is no instantaneous power transfer, becomes more and more dominant. This results in a non-linear and decreasing behaviour of the output current as function of the switching frequency.

Before the derivation of the static characteristic, the analytic derivation of the relevant waveforms during the various modes of operation is presented. Since the C_1 and C_2 voltages do not reach V_{in} nor GND, the clamping diodes D_1 and D_2 never conduct. As a result, the *current circulating* mode is absent in this operating region. Due to the symmetric operation of the half bridge, the DC value of $v_{\mathrm{x}}(t)$ is still $\frac{V_{\mathrm{in}}}{2}$, but the instantaneous voltage varies between $\frac{V_{\mathrm{in}}}{2} - \Delta V$ and $\frac{V_{\mathrm{in}}}{2} + \Delta V$, where $\Delta V <= \frac{V_{\mathrm{in}}}{2} + V_{\mathrm{F,D}}$. As in the previous case, due to the same symmetry considerations, only half a switching period is considered. The same assumptions on the ideal features of active and passive components made previously are still considered here.

4.3.1 Power transfer mode

The first mode is identical, from the working operation point of view. During this mode, the load current, flowing from node A to node X, linearly charges C_2 and discharges C_1. For simplification purposes, in this derivation ΔV and I_{o} are assumed to be linked by the following approximated law:

$$2C\frac{2\Delta V}{\frac{T_{\mathrm{sw}}}{2}} = I_{\mathrm{o}}\,. \tag{4.23}$$

Actually, Eq.4.23 does not consider the duration of the other modes, which is frequency-dependent. The detailed expression for the two related parametres will be derived further in thi work.

Eq.4.24 summarizes the relevant waveforms behaviour during this first mode:

$$\begin{cases} v_{\mathrm{x}}(t) = V_{\mathrm{x},0} + \dfrac{I_{\mathrm{o}}}{2C}(t - t_0) \\ v_L(t) = 0 \\ i_L = I_{\mathrm{o}} \\ v_{\mathrm{p}}(t) = V_{\mathrm{in}} - v_{\mathrm{x}}(t) = V_{\mathrm{in}} - V_{\mathrm{x},0} - \dfrac{I_{\mathrm{o}}}{2C}(t - t_0) \\ v_{\mathrm{s}}(t) = v_{\mathrm{p}}(t) - 2V_{\mathrm{F,D}} = V_{\mathrm{in}} - V_{\mathrm{x},0} - 2V_{\mathrm{F,D}} - \dfrac{I_{\mathrm{o}}}{2C}(t - t_0) \\ i_{\mathrm{D_3}} = I_{\mathrm{o}} \\ i_{\mathrm{D_4}} = 0 \end{cases} , \tag{4.24}$$

where $V_{\mathrm{x},0}$ is the initial value of the state variable v_{x}, which can be derived from the final value of the last mode, as before. The first mode ends when M_1 is turned OFF, at t_1. Fig.4.4a shows the conducting devices and the polarity of the currents in the circuit during this mode.

4.3.2 Crossover resonant mode

As mentioned, Mode 2 is absent in this working region. As a result, when M_1 turns OFF, the voltage at node X is not sufficient to turn ON the clamping diode D_1.

Mode 3.1

The current through L_{r} is still positive and can charge/discharge the output capacitances C_{s} of the half bridge MOSFETs. Contrarily to the previously analysed working region (at lower frequencies), where the rectifier diodes enter into conduction since mode 2, here they can't be turned ON until the beginning of mode 3.1. The reason is that, when M_1 turns OFF, the primary voltage v_{p}, assuming that L_{r} is still conducting the load current ($v_L \approx 0\,\mathrm{V}$), would be $V_{\mathrm{in}} - \left(\frac{V_{\mathrm{in}}}{2} + \Delta V\right) = \frac{V_{\mathrm{in}}}{2} - \Delta V > 0$. In principle, while the voltage at node A decreases, at a certain point the rectifier diodes D_4 and D_6 should enter into conduction, enabling a resonant stage among L_{r}, the output capacitances C_{s} and, differently from the previous case, the dividing capacitances C_1 and C_2. Considering a constant input voltage, the parallel connection between C_{s1} and C_{s2} results in series with $2C = C_1 + C2$. The following assumptions are made to simplify the analysis:

- due to the much lower value of the output capacitances ($\approx 10^2 pF$) compared to C_1 and C_2 ($\approx 10^2 nF$), the resulting resonance frequency with L_r will be determined by $2C_\mathrm{s} = C_{\mathrm{s}1} + C_{\mathrm{s}2}$. Since, due to the small parasitic capacitances, this state is the shortest one, the state variable v_x can be assumed to be constant during this mode;

- as in the previous case, the inductor L_r is assumed to store enough energy to effectively be able to charge and discharge completely the output capacitances (Eq.4.12);

- the duration of this mode is very short compared to the other ones. As a result, a negligible error is obtained if one assumes that the rectifier diodes D_4 and D_6 turn ON immediately after the beginning of this mode.

After these considerations, the behaviour of the resonant variable v_A can be derived by solving the following ODE:

$$\begin{cases} v''_\mathrm{A}(t) + \omega^2_\mathrm{res} v_\mathrm{A}(t) = \omega^2_\mathrm{res}\left(\dfrac{V_\mathrm{in}}{2} + \Delta V\right) \\ v_\mathrm{A}(0) = V_\mathrm{in} \\ v'_\mathrm{A}(0) = -\dfrac{i_L(0)}{2C_\mathrm{s}} = -\dfrac{I_\mathrm{o}}{2C_\mathrm{s}} \end{cases} . \tag{4.25}$$

From v_A, i_L can be derived by simply considering the KCL at node A:

$$i_L(t) = -2C_\mathrm{s}\frac{dv_\mathrm{A}}{dt} . \tag{4.26}$$

The diodes currents begin to exchange among themselves, in order to obtain, at the end of the *crossover resonant* state a complete reversal of i_L. The ensemble of

relevant waveforms during this mode is here reported:

$$\begin{cases} v_{\mathrm{x}}(t) = \dfrac{V_{\mathrm{in}}}{2} + \Delta V \\ v_L(t) = \left(\dfrac{V_{\mathrm{in}}}{2} - \Delta V\right)\cos\left(\omega_{\mathrm{res}}(t-t_1)\right) - \dfrac{I_o}{2C_{\mathrm{s}}\omega_{\mathrm{res}}}\sin\left(\omega_{\mathrm{res}}(t-t_1)\right) \\ i_L(t) = 2C_{\mathrm{s}}\omega_{\mathrm{res}}\left(\dfrac{V_{\mathrm{in}}}{2} - \Delta V\right)\sin\left(\omega_{\mathrm{res}}(t-t_1)\right) + I_{\mathrm{o}}\cos\left(\omega_{\mathrm{res}}(t-t_1)\right) \\ v_{\mathrm{p}}(t) = 0 \\ v_{\mathrm{s}}(t) = -2V_{\mathrm{F,D}} \\ i_{\mathrm{D_3}}(t) = \dfrac{I_{\mathrm{o}}}{2} + \dfrac{i_L(t)}{2} \\ i_{\mathrm{D_4}}(t) = \dfrac{I_{\mathrm{o}}}{2} - \dfrac{i_L(t)}{2} \end{cases} . \quad (4.27)$$

This mode ends when the voltage at node A becomes negative and turns ON the body diode of M_2. Adopting the same first-order approximation of the *cosine* term of $v_{\mathrm{A}}(t)$ already considered before, the duration of this mode, t_2, can be computed as:

$$t_2 \approx \frac{1}{\omega_{\mathrm{res}}}\sin^{-1}\left(\frac{2C_{\mathrm{s}}\omega_{\mathrm{res}}(V_{\mathrm{in}} + V_{\mathrm{F,M}})}{I_{\mathrm{o}}}\right). \quad (4.28)$$

Let's denote by $I_{\mathrm{L},2}$ the value assumed by the inductor current at the end of the mode. Fig.4.4b shows in red the conducting devices and the polarity of the currents in the circuit.

Mode 3.2

Also the second sub-mode of the *crossover resonant* state differs in this working region. The reason is related, also in this case, to the absence of the clamping diode conduction, which does not fix the dividing capacitor voltages. As a result, a second resonant stage is enabled between L_{r} and the parallel capacitive network $2C = C_1 + C_2$, characterised by the following resonance frequency:

$$\omega_{\mathrm{res},2} = \frac{1}{\sqrt{2CL_{\mathrm{r}}}}. \quad (4.29)$$

Until the MOSFET M_2 is OFF and the inductor current is positive, the conducting body diode keeps the voltage at node A fixed at $-V_{\mathrm{F,M}}$.

The resonant behaviour of the state variable v_{x} is described by the following second-order ODE (assuming a shifted time origin):

$$\begin{cases} v_{\mathrm{x}}''(t) + \omega_{\mathrm{res},2}^2 v_{\mathrm{x}}(t) = -\omega_{\mathrm{res},2}^2 V_{\mathrm{F,M}} \\ v_{\mathrm{x}}(0) = \dfrac{V_{\mathrm{in}}}{2} + \Delta V \\ v_{\mathrm{x}}'(0) = \dfrac{I_{\mathrm{L},2}}{2C} \end{cases} . \tag{4.30}$$

By solving the equation for $v_{\mathrm{x}}(t)$, it is also possible to derive i_L from the KCL applied at node X:

$$i_L(t) = 2C\frac{dv_{\mathrm{x}}}{dt} . \tag{4.31}$$

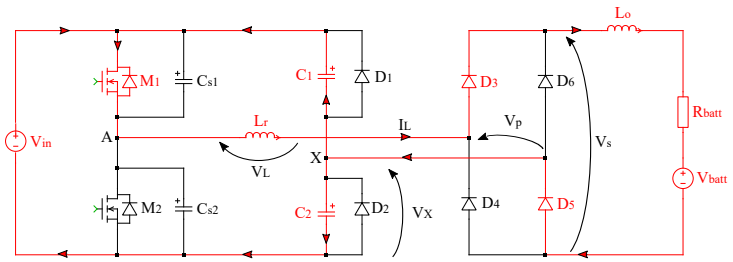
The resulting waveforms for this mode are here reported:

$$\begin{cases} v_{\mathrm{x}}(t) = -V_{\mathrm{F,M}} + \left(\dfrac{V_{\mathrm{in}}}{2} + \Delta V + V_{\mathrm{F,M}}\right)\cos\left(\omega_{\mathrm{res},2}(t-t_2)\right) + \dfrac{I_{\mathrm{L},2}}{2C\omega_{\mathrm{res},2}}\sin\left(\omega_{\mathrm{res},2}(t-t_2)\right) \\ v_L(t) = -\left(\dfrac{V_{\mathrm{in}}}{2} + \Delta V + V_{\mathrm{F,M}}\right)\cos\left(\omega_{\mathrm{res},2}(t-t_2)\right) - \dfrac{I_{\mathrm{L},2}}{2C\omega_{\mathrm{res},2}}\sin\left(\omega_{\mathrm{res},2}(t-t_2)\right) \\ i_L(t) = -2C\omega_{\mathrm{res},2}\left(\dfrac{V_{\mathrm{in}}}{2} + \Delta V + V_{\mathrm{F,M}}\right)\sin\left(\omega_{\mathrm{res},2}(t-t_2)\right) + I_{\mathrm{L},2}\cos\left(\omega_{\mathrm{res},2}(t-t_2)\right) \\ v_{\mathrm{p}}(t) = 0 \\ v_{\mathrm{s}}(t) = -2V_{\mathrm{F,D}} \\ i_{\mathrm{D_3}}(t) = \dfrac{I_{\mathrm{o}}}{2} + \dfrac{i_L(t)}{2} \\ i_{\mathrm{D_4}}(t) = \dfrac{I_{\mathrm{o}}}{2} - \dfrac{i_L(t)}{2} \end{cases} \tag{4.32}$$

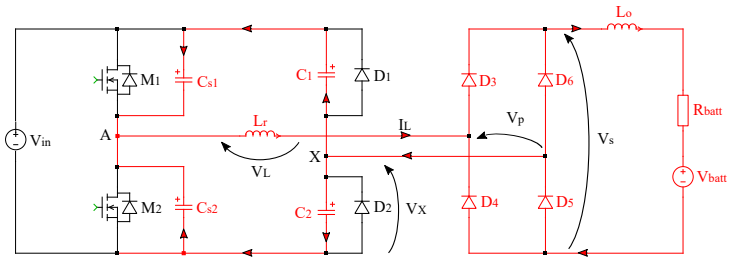
This mode ends when M_2 is turned ON. In order to achieve ZVS, it must be turned ON before i_L reverses. If this happens, indeed, as in the previous case, the negative current starts charging the output capacitance of M_2 again and soft switching is lost. The time required for i_L to reach 0, t_3, also delimiting the maximum allowed deadtime, can be easily computed from the current waveform:

$$t_3 = \frac{1}{\omega_{\mathrm{res},2}}\sin^{-1}\left(\frac{I_{\mathrm{L},2}}{2C\omega_{\mathrm{res},2}\left(\frac{V_{\mathrm{in}}}{2} + \Delta V + V_{\mathrm{F,M}}\right)}\right) . \tag{4.33}$$

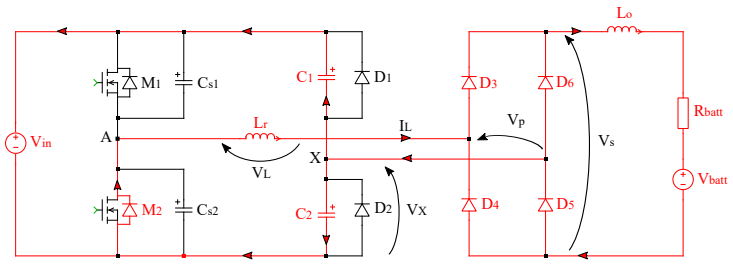
In this context, it is assumed that M_2 is exactly turned ON at the end of this mode. The final value of $v_{\mathrm{x}}(t)$ is denoted by $V_{\mathrm{x},3} = v_{\mathrm{x}}(t = t_3)$. The schematic representation of the currents directions and of the conducting devices during this mode is presented in Fig.4.4c.



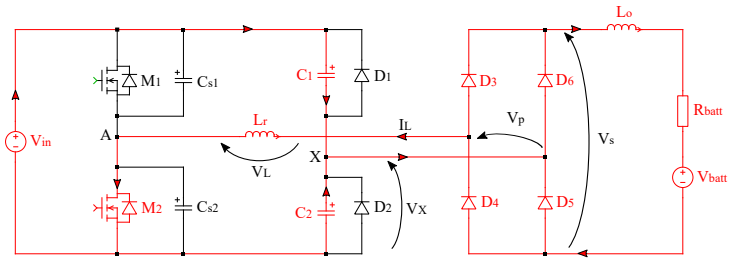
(a) Mode 1.



(b) Mode 3.1.



(c) Mode 3.2.



(d) Mode 3.3.

Figure 4.4: Operation of the novel battery charger during the different modes, in the high frequency region.

Mode 3.3

From the point of view of the working operation, this sub-mode is identical to the previous one. The primary voltage is still clamped at zero because all the rectifier

diodes conduct. As a consequence, the inductor resonates with capacitors C_1 and C_2 and keeps decreasing until the end of the mode (when it finally reaches $-I_\mathrm{o}$). The only difference in the describing equations is that, for the assumption adopted, the ON-state voltage of MOSFET M_2 is null, rather than the forward voltage of its body diode. The resulting second-order ODE describing $v_\mathrm{x}(t)$ during this mode is:

$$\begin{cases} v_\mathrm{x}''(t) + \omega_{\mathrm{res},2}^2 v_\mathrm{x}(t) = 0 \\ v_\mathrm{x}(0) = V_{\mathrm{x},3} \\ v_\mathrm{x}'(0) = 0 \end{cases} . \tag{4.34}$$

After solving the equation, it is also possible to derive $i_L(t)$ from the same KCL at node X. The resulting relevant expressions of voltage and current waveforms are here reported:

$$\begin{cases} v_\mathrm{x}(t) = V_{\mathrm{x},3} \cos\Big(\omega_{\mathrm{res},2}(t-t_3)\Big) \\ v_L(t) = -V_{\mathrm{x},3} \cos\Big(\omega_{\mathrm{res},2}(t-t_3)\Big) \\ i_L(t) = -2C\omega_{\mathrm{res},2} V_{\mathrm{x},3} \sin\Big(\omega_{\mathrm{res},2}(t-t_3)\Big) \\ v_\mathrm{p}(t) = 0 \\ v_\mathrm{s}(t) = -2V_{\mathrm{F,D}} \\ i_{\mathrm{D}_3}(t) = \dfrac{I_\mathrm{o}}{2} - C\omega_{\mathrm{res},2} V_{\mathrm{x},3} \sin\Big(\omega_{\mathrm{res},2}(t-t_3)\Big) \\ i_{\mathrm{D}_4}(t) = \dfrac{I_\mathrm{o}}{2} + C\omega_{\mathrm{res},2} V_{\mathrm{x},3} \sin\Big(\omega_{\mathrm{res},2}(t-t_3)\Big) \end{cases} . \tag{4.35}$$

The duration of this mode, t_4, can be computed by imposing that $i_L(t_4) = -I_\mathrm{o}$, which results in:

$$t_4 = \frac{1}{\omega_{\mathrm{res},2}} \sin^{-1}\left(\frac{I_\mathrm{o}}{2C\omega_{\mathrm{res},2} V_{\mathrm{x},3}}\right). \tag{4.36}$$

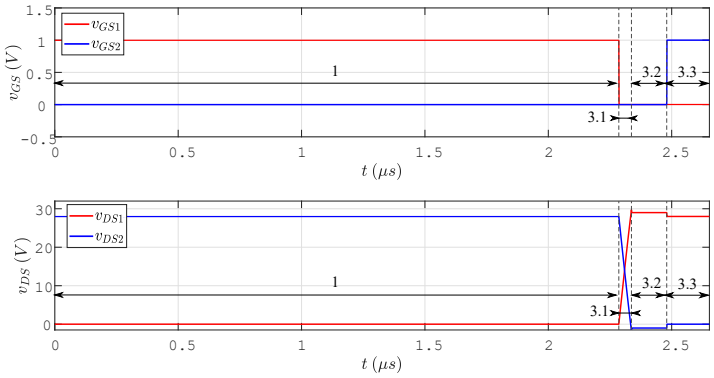
The final value of $v_\mathrm{x}(t)$ at the end of this last mode is an interesting parametre to evaluate, because gives information on the initial value $V_{\mathrm{x},0}$:

$$v_\mathrm{x}(t_4) = V_{\mathrm{x},3}\sqrt{1 - \left(\frac{I_\mathrm{o}}{2C\omega_{\mathrm{res},2} V_{\mathrm{x},3}}\right)^2}. \tag{4.37}$$

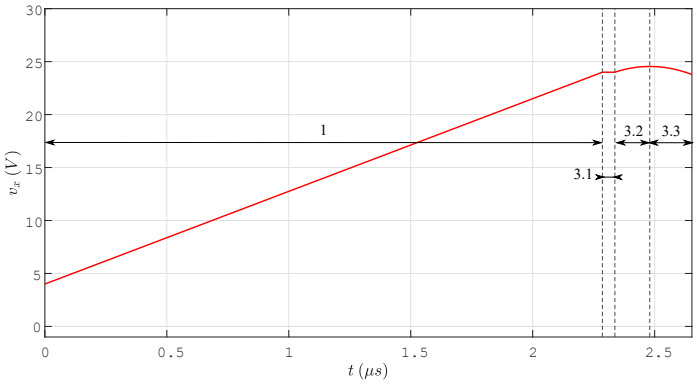
Thanks to the symmetric operation, $V_{\mathrm{x},0} = V_\mathrm{in} - v_\mathrm{x}(t_4)$. Fig.4.4d highlights the conducting devices and the direction of currents during this last mode.

Fig.4.5 reports the qualitative behaviour of some of the relevant waveforms previously described. Also in this case, to better outline the behaviour during

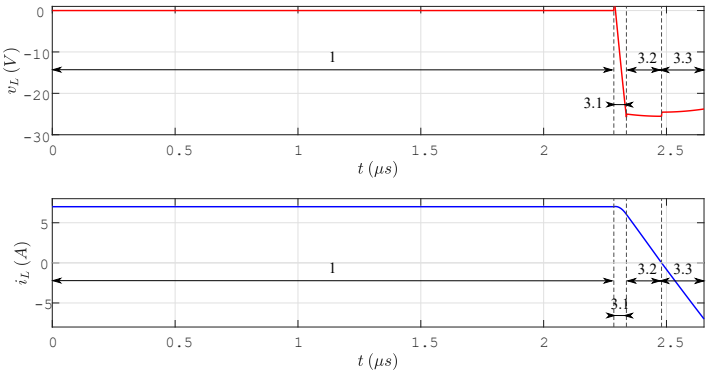
the relatively short *crossover resonant* state, the duration of the sub-modes is exaggerated in the plots.



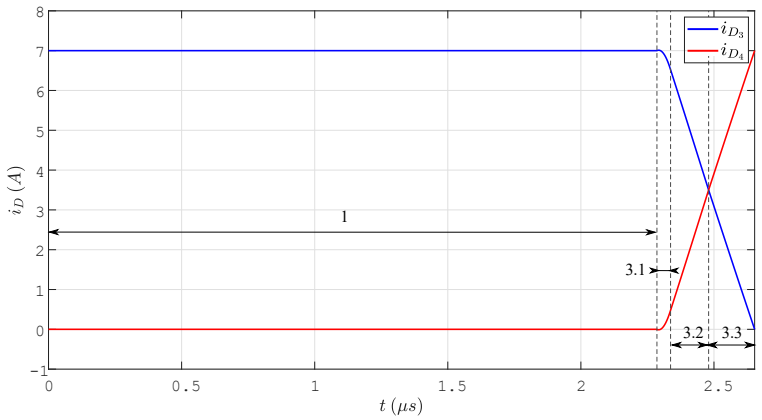
(a) MOSFETs driving signals and output voltages.



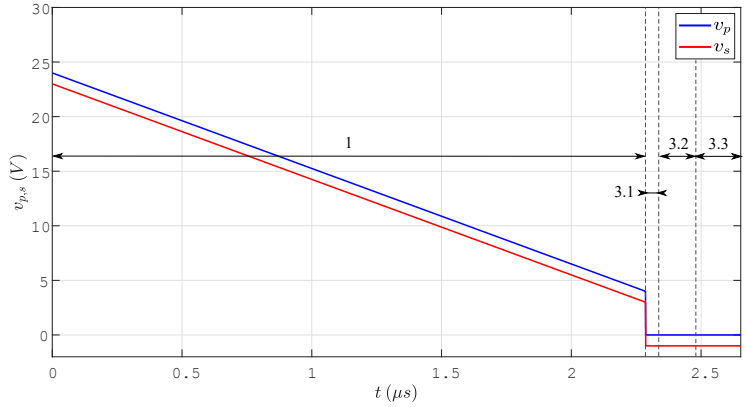
(b) Voltage at node X.



(c) Inductor L_r voltage and current.



(d) Diodes D_3 and D_4 currents.



(e) Input and output voltages of the Graetz bridge rectifier.

Figure 4.5: Relevant waveforms of the analysed converter within a half cycle in the high frequency region.

4.4 Static characteristic

4.4.1 Necessary conditions for power transfer

In this section, the derivation of the static characteristic $P_{\text{out}}(f_{\text{sw}})$ of the previously presented two operating regions is detailed. Before proceeding, it is however necessary to outline the necessary conditions for a non-null power transfer from the PV panel side to the battery side.

As described in [38] for the isolated constant-power charger, the output current must be maintained at a level such that the dividing capacitors are charged

and discharged completely (discontinuous voltage mode). This condition can be translated, also in the case of the converter here analysed, into two simultaneous constraints, on the input voltage and on the battery internal resistance:

$$\begin{cases} V_{\text{in}} \geq 2V_{\text{batt}} + 4V_{\text{F,D}} \\ R_{\text{batt}} \leq \dfrac{\frac{V_{\text{in}}}{2} - V_{\text{batt}}}{4Cf_{\text{sw}}V_{\text{in}}} \end{cases} . \tag{4.38}$$

The first equation differs from the one in [38] because it considers the contribution of the additional voltage drops of the rectifier diodes (assuming a passive rectifier). If diodes are replaced by a MOSFETs with reasonably small ON-state resistance (active rectifier), the voltage drops across the rectifier can be assumed to be negligible. The second equation, instead, can be interpreted in the following way: the ohmic voltage drop across the internal battery resistance must be low enough to ensure that the specified input voltage can charge the battery with the charging current required for the discontinuous voltage mode.

Equivalently, the first equation can be extracted from the analysis of the output filter inductor voltage waveform. The reason is that the *volts-seconds balance* for this inductor must be satisfied to sustain the stationary operation of the converter. From Fig.4.3e, representing the instantaneous voltage waveforms for the input and output sides of the rectifier, the output inductor voltage can be obtained by considering approximately a $-V_{\text{batt}}$ offset with respect to v_{s}. As a rough approximation, considering a sawtooth waveform varying from $V_{\text{in}} - 2V_{\text{F,D}} - V_{\text{batt}}$ to $V_{\text{in}} - 2V_{\text{F,D}}$ (mode 2 absent, and negligible duration of mode 3), the volts-seconds balance translates again in the condition $V_{\text{in}} > 2V_{\text{batt}} + 4V_{\text{F,D}}$.

The consequences of this constraint are significant when the input power source is not a DC-voltage voltage power supply. In this case, indeed, it would be simply sufficient to set the input voltage to satisfy this condition for all the operating battery voltages within a charging cycle. When the power source is a PV module, instead:

- a minimum number of series-connected cells is required to satisfy the condition at STC. Considering a tipical 0.6 V Si-PV cell, for instance, and a 12 V battery, at least 40 cells would be required to charge the battery when completely discharged;
- the constraint becomes stricter considering the progressive increase of the battery voltage during the charging process, and the PV voltage decrease for the effect of an instantaneous decrease of the irradiance level or an increase of temperature. Due to the variability of the PV panel electrical characteristic,

the instantaneous working point may not be compliant with the voltage constraint and the current requirement for the discontinuous voltage mode.

4.4.2 Low-frequency region static characteristic

The derivation of the static characteristic in this region is quite straightforward and recalls the same operating principles of the converter in [38]. The amount of transferred power is linked to the energy which is stored and released every cycle by the dividing capacitors:

$$\mathscr{E}_{\mathrm{C}} = \frac{1}{2} C V_{\mathrm{in}}^2 \,. \tag{4.39}$$

Denoting by P_{p} the power transferred to the primary side of the rectifier, and considering that only during the first mode there is an effective power transfer:

$$\begin{aligned} P_{\mathrm{p}} &= \frac{1}{T_{\mathrm{sw}}} \int_0^{T_{\mathrm{sw}}} v_{\mathrm{p}}(t) i_L(t) dt \\ &\approx \frac{1}{T_{\mathrm{sw}}} \left(\int_0^{t_1} \Big(V_{\mathrm{in}} - v_{\mathrm{x}}(t) \Big) I_{\mathrm{o}} dt + \int_{\frac{T_{\mathrm{sw}}}{2}}^{t_1 + \frac{T_{\mathrm{sw}}}{2}} \Big(- v_{\mathrm{x}}(t) \Big) (-I_{\mathrm{o}}) dt \right) \\ &= (C_1 + C_2) V_{\mathrm{in}} (V_{\mathrm{in}} + V_{\mathrm{F,D}}) f_{\mathrm{sw}} \,. \end{aligned} \tag{4.40}$$

Assuming a negligible power loss associated to the battery internal resistance and to the MOSFETs, the output power basically coincides with P_{p} and the average charging current becomes:

$$I_{\mathrm{o}} \approx \frac{2 C f_{\mathrm{sw}} V_{\mathrm{in}} (V_{\mathrm{in}} + V_{\mathrm{F,D}})}{V_{\mathrm{batt}}} \,. \tag{4.41}$$

From Eq.4.41, a simple equivalent circuit model for the battery side of the converter can be extracted (Fig.4.6). The converter output, with the approximations previously made, behaves as a constant current source whose average value depends on the input voltage, the battery voltage and the switching frequency. Since the model does not take into account the voltage drops of the rectifier, it better applies to active rectifiers whose MOSFETs are characterised by low ON-state resistances.

A last consideration regards the L_{r} energy. Since, as in [38], the stored energy in L_{r} is not transferred to the battery side, but recovered at the input, its energy contribution must be subtracted by P_{p}. If L_{r} is designed to be sufficiently small, its contribution of energy can be neglected without committing a significant mistake:

$$L_{\mathrm{r}} \ll \frac{1}{(C_1 + C_2) f_{\mathrm{sw}}^2} \left(\frac{V_{\mathrm{batt}}}{V_{\mathrm{in}}} \right)^2 \,. \tag{4.42}$$

This condition, together with Eq.4.12, specifies the high and low boundaries of the inductance value, respectively.

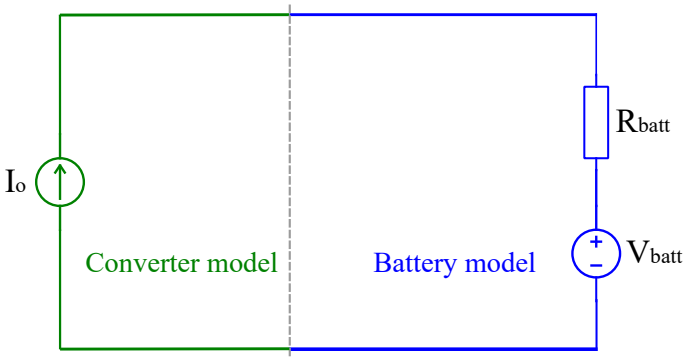


Figure 4.6: Output side simplified equivalent circuit model in the low-frequency region.

4.4.3 High-frequency region static characteristic

The linearity of the static characteristic in the low-frequency operating region is lost when the frequency is increased above a certain frequency limit. The reason is that the L_r reactance, whose contribution appears to be negligible at low frequencies, starts becoming important in determining the amount of transferred power. As it will be clarified in the present section, the result is a non-linear and decreasing behaviour of the output power as function of the switching frequency, whose analytic expression is derived in this work. The frequency threshold can also be determined explicitly, in order to immediately derive it once the source and battery voltages, and the values of reactive components, are known.

The derivation of the static characteristic $P_{out}(f_{sw})$ in the high-frequency operating region is based on the analysis of the rectifier output voltage waveform. This analysis, presented in this section, allows to derive an equivalent parametric circuit model for the output side of the rectifier which, in turns, allows to compute in an explicit way the output average current as function of the input and battery voltages, switching frequency and power devices non-idealities.

During half of the switching cycle, the qualitative behaviour of the output voltage of the rectifier, already displayed in Fig.4.5e, is characterized by two distinct sections:

- in the first interval ($t \in \{0, T_{sw}/2 - t^*\}$), $v_s(t)$ basically reproduces the linear charge/discharge of the dividing capacitors, beside the additional voltage drops of the rectifier and half-bridge MOSFETs;
- in the second, shorter interval, instead, during the L_r current reversal, the output voltage is clamped at a slightly negative value, linked to the rectifier

MOSFETs body diodes. In the following analysis, to simplify the computations, during this interval of time it is assumed that, for each rectifier leg, only one MOSFET is conducting, whereas the other one is kept OFF (in other words, its body diode conducts). As a result, $v_{\mathrm{s}}(t) = -V_{\mathrm{F,D}}$.

Fig.4.7 shows the output voltage waveform within a switching cycle.

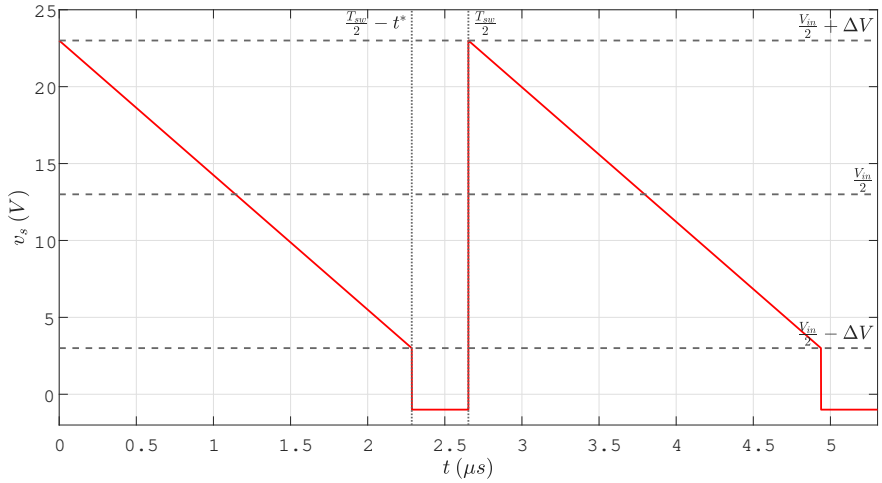


Figure 4.7: Instantaneous rectifier output voltage within a switching cycle.

From this consideration, the duration of the second interval of time t^* is the time required by the L_{r} current to reverse from $+I_{\mathrm{o}}$ to $-I_{\mathrm{o}}$ (or viceversa):

$$L_{\mathrm{r}} \frac{2I_{\mathrm{o}}}{t^*} \approx \frac{V_{\mathrm{in}}}{2} + V_{\mathrm{F,D}} + \Delta V \,. \tag{4.43}$$

In this derivation, the assumption of a linear discharge of the L_{r} current is adopted. This assumption is reasonable if the duration of the crossover resonant state sub-modes is short enough to approximate the sinusoidal behaviour of the L_{r} current into a linear decrease. This is equivalent to say that the $v_{\mathrm{x}}(t)$ remains basically constant during the *crossover resonant* state. Inverting the equation to express t^*:

$$t^* = \frac{2I_{\mathrm{o}}L_{\mathrm{r}}}{V_{\mathrm{in}}/2 + V_{\mathrm{F,D}} + \Delta V} = \frac{4I_{\mathrm{o}}L_{\mathrm{r}}}{V_{\mathrm{in}}(1+\alpha)} \,, \tag{4.44}$$

where $\alpha \triangleq \frac{V_{\mathrm{F,D}}+\Delta V}{\frac{V_{\mathrm{in}}}{2}}$ is defined for compactness purposes. It is worthwhile to notice that:

$$0 \approx \frac{2V_{\mathrm{F.D}}}{V_{\mathrm{in}}} < \alpha \leq 1 + \frac{2V_{\mathrm{F.D}}}{V_{\mathrm{in}}} \approx 1 \,. \tag{4.45}$$

More specifically, the lowest boundary is reached for really low output powers, when the output current can't charge/discharge effectively the dividing capacitors, whereas the highest limit at the boundary with the first operating region.

The average output secondary voltage, which is the effective charging voltage across the battery, is obtained by integrating $v_{\mathrm{s}}(t)$ through half a switching cycle:

$$\begin{aligned}\overline{V_{\mathrm{o}}} &= \frac{2}{T_{\mathrm{sw}}}\int_0^{\frac{T_{\mathrm{sw}}}{2}} v_{\mathrm{s}}(t)dt = \frac{2}{T_{\mathrm{sw}}}\left[\frac{V_{\mathrm{in}}}{2}\left(\frac{T_{\mathrm{sw}}}{2}-t^*\right)-V_{\mathrm{F,D}}t^*\right] \\ &= \frac{V_{\mathrm{in}}}{2}-\frac{4L_{\mathrm{r}}}{(1+\alpha)T_{\mathrm{sw}}}I_{\mathrm{o}}-\frac{8V_{\mathrm{F,D}}L_{\mathrm{r}}}{(1+\alpha)V_{\mathrm{in}}T_{\mathrm{sw}}}I_{\mathrm{o}}\,.\end{aligned} \tag{4.46}$$

It is possible to notice that the output average voltage includes one frequency-independent term $\frac{V_{\mathrm{in}}}{2}$ and two ohmic-like, frequency-dependent voltage drops. For the following derivations, the second and third terms are re-written in terms of two equivalent resistances:

$$\begin{cases} R_{\mathrm{eq,1}}(f_{\mathrm{sw}}) = \dfrac{4L_{\mathrm{r}}f_{\mathrm{sw}}}{1+\alpha(\Delta V)} \\ R_{\mathrm{eq,2}}(f_{\mathrm{sw}}) = \dfrac{8V_{\mathrm{F,D}}L_{\mathrm{r}}f_{\mathrm{sw}}}{V_{\mathrm{in}}\Big(1+\alpha(\Delta V)\Big)} \end{cases}. \tag{4.47}$$

$R_{\mathrm{eq,1}}$ and $R_{\mathrm{eq,2}}$, as it can be seen, are proportional to the L_{r} reactance: they do not represent ohmic losses in the circuit, but the contribution of the L_{r} in the switching dynamics of the converter. The non-null time required to charge/discharge the inductor current is reflected in an equivalent frequency-dependent voltage drop in the output average voltage.

The output loop equivalent circuit is represented in Fig.4.8, which explicitly includes the internal battery resistance R_{batt} and an additional resistor R_{ext} accounting for the ohmic losses of the other circuit components.

From this simple resistive circuit, a first equation relating the output current, the variable ΔV and the switching frequency f_{sw} can be determined:

$$I_{\mathrm{o}} = \frac{\frac{V_{\mathrm{in}}}{2}-V_{\mathrm{batt}}}{R_{\mathrm{eq,1}}(\Delta V, f_{\mathrm{sw}})+R_{\mathrm{eq,2}}(\Delta V, f_{\mathrm{sw}})+R_{\mathrm{ext}}+R_{\mathrm{batt}}} = \frac{\frac{V_{\mathrm{in}}}{2}-V_{\mathrm{batt}}}{\frac{X_{\mathrm{eff}}(f_{\mathrm{sw}})}{1+\alpha(\Delta V)}+R_{\mathrm{ohm}}}\,, \tag{4.48}$$

where, for compactness of notation, $X_{\mathrm{eff}}(f_{\mathrm{sw}}) \triangleq 4L_{\mathrm{r}}f_{\mathrm{sw}}\Big(1+\frac{2V_{\mathrm{F,D}}}{V_{\mathrm{in}}}\Big)$ and $R_{\mathrm{ohm}} \triangleq R_{\mathrm{ext}}+R_{\mathrm{batt}}$. A single equation, however, is not sufficient to explicit I_{o} as a function

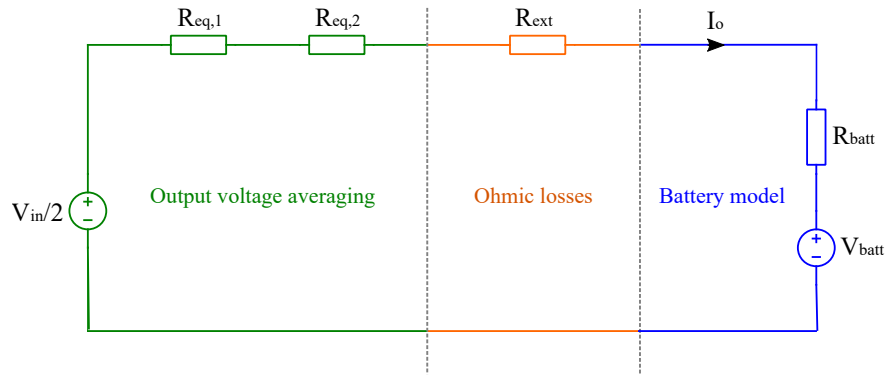


Figure 4.8: Equivalent circuit schematic of the output side of the converter in the high frequency region.

of the only variable f_{sw}. A second equation can be determined by recalling that, during mode 1, the dividing capacitors are subjected to a linear charge/discharge linked to the output current I_{o}:

$$2\Delta V = \left(\frac{T_{\mathrm{sw}}}{2} - t^*\right)\frac{I_{\mathrm{o}}(\Delta V, f_{\mathrm{sw}})}{2C}\,. \tag{4.49}$$

By inserting Eq.4.48 and Eq.4.44 into Eq.4.49, and after performing some computations and simplifications, a single third-order non-linear equation in the unknown ΔV is obtained:

$$P_3\Delta V^3 + P_2(f_{\mathrm{sw}})\Delta V^2 + P_1(f_{\mathrm{sw}})\Delta V + P_0 = 0\,, \tag{4.50}$$

where the expressions of the coefficients P_i are here reported:

$$\begin{cases} P_3 = \dfrac{4R_{\mathrm{ohm}}^2}{V_{\mathrm{in}}} \\ P_2(f_{\mathrm{sw}}) = 4R_{\mathrm{ohm}}\left(X_{\mathrm{eff}}(f_{\mathrm{sw}}) + R_{\mathrm{ohm}}\left(1+\dfrac{2V_{\mathrm{F,D}}}{V_{\mathrm{in}}}\right)\right) - \dfrac{R_{\mathrm{ohm}}\left(1-\frac{2V_{\mathrm{batt}}}{V_{\mathrm{in}}}\right)}{4Cf_{\mathrm{sw}}} \\ P_1(f_{\mathrm{sw}}) = V_{\mathrm{in}}\left(X_{\mathrm{eff}}(f_{\mathrm{sw}}) + R_{\mathrm{ohm}}\left(1+\dfrac{2V_{\mathrm{F,D}}}{V_{\mathrm{in}}}\right)\right)^2 - \dfrac{R_{\mathrm{ohm}}\left(\frac{V_{\mathrm{in}}}{2}-V_{\mathrm{batt}}\right)\left(1+\frac{2V_{\mathrm{F,D}}}{V_{\mathrm{in}}}\right)}{4Cf_{\mathrm{sw}}} - \dfrac{\left(X_{\mathrm{eff}}(f_{\mathrm{sw}}) + R_{\mathrm{ohm}}\left(1+\frac{2V_{\mathrm{F,D}}}{V_{\mathrm{in}}}\right)\right)\left(\frac{V_{\mathrm{in}}}{2}-V_{\mathrm{batt}}\right)}{4Cf_{\mathrm{sw}}} + 2\dfrac{L_{\mathrm{r}}}{2C}\dfrac{\left(\frac{V_{\mathrm{in}}}{2}-V_{\mathrm{batt}}\right)^2}{V_{\mathrm{in}}} \\ P_0(f_{\mathrm{sw}}) = -\dfrac{\frac{V_{\mathrm{in}}}{2}\left(X_{\mathrm{eff}}(f_{\mathrm{sw}}) + R_{\mathrm{ohm}}\left(1+\frac{2V_{\mathrm{F,D}}}{V_{\mathrm{in}}}\right)\right)\left(\frac{V_{\mathrm{in}}}{2}-V_{\mathrm{batt}}\right)\left(1+\frac{2V_{\mathrm{F,D}}}{V_{\mathrm{in}}}\right)}{4Cf_{\mathrm{sw}}} + \dfrac{L_{\mathrm{r}}}{2C}\left(\dfrac{V_{\mathrm{in}}}{2}-V_{\mathrm{batt}}\right)^2\left(1+\dfrac{2V_{\mathrm{F,D}}}{V_{\mathrm{in}}}\right) \end{cases} \tag{4.51}$$

Despite the existence of Cardano's method for the explicit solution of cubic equations, this approach, considering the complexity of the polynomial coefficients, would lead to an unbearably complex expression of $\Delta V(f_{\mathrm{sw}})$. In this work, an alternative and approximated approach is proposed to simplify the solution. This approach is based on the following consideration: if the ratio of the second and third order terms $\frac{P_2(f_{\mathrm{sw}})}{P_3}$ turns out to be always much larger than the maximum

value that ΔV can assume (i.e. $\frac{V_{\text{in}}}{2} + V_{\text{F,D}}$), then it would be possible to neglect the entire third-order monomial $P_3 \Delta V^3$.

Fig.4.9 shows the ratio of second and third order coefficients of the equation, as a function of the switching frequency, computed for the design parametres reported in Tab.4.1:

V_{in}	28 V
V_{batt}	13.2 V
R_{batt}	30 mΩ
R_{ext}	32 mΩ
$V_{\text{F,D}}$	0.85 V
L_{r}	330 nH
$C_{1,2}$	1 µF

Table 4.1: Parametres adopted for the plot of $\frac{P_2}{P_3}$ in Fig.4.9.

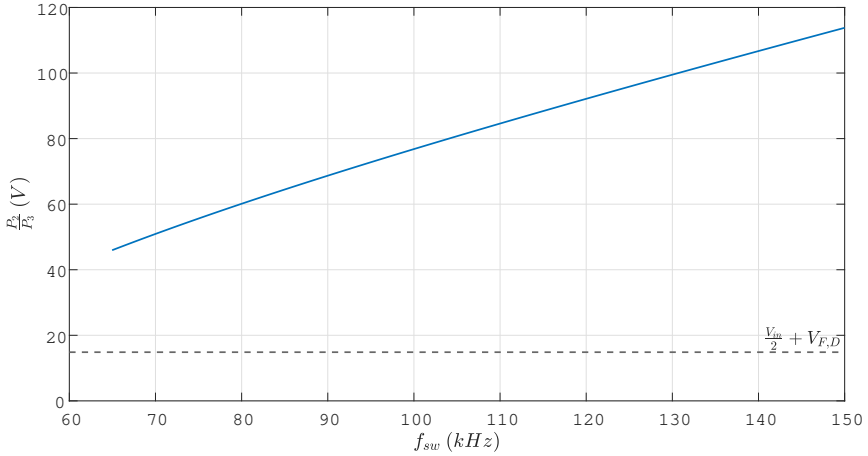


Figure 4.9: Frequency behavior of the ratio $\frac{P_2}{P_3}$.

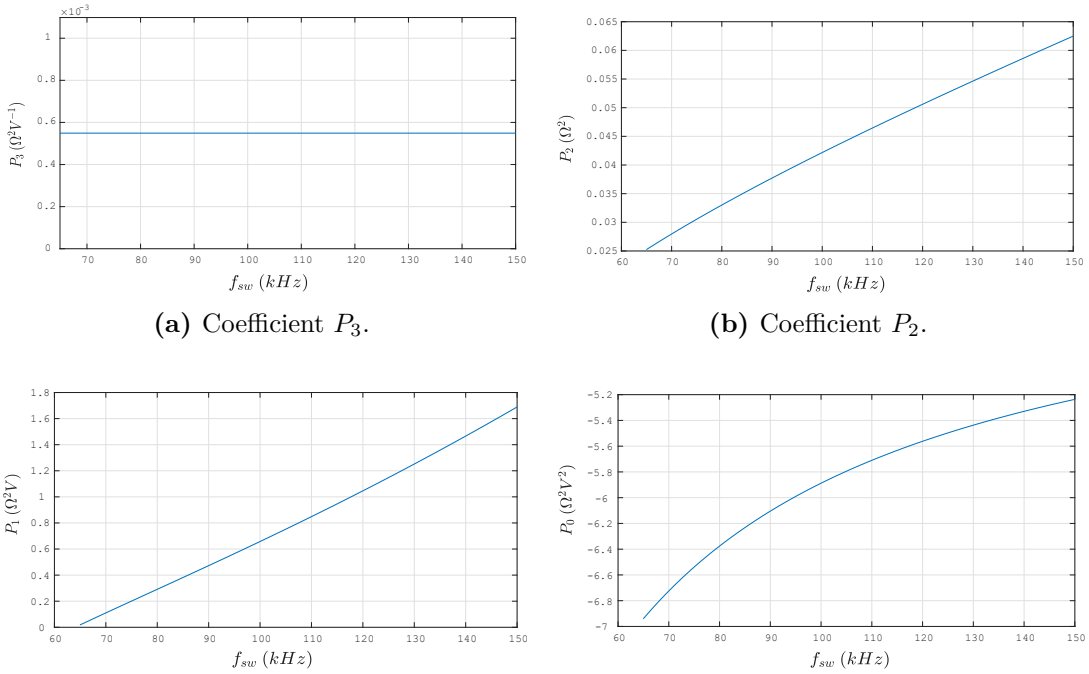
Since the third-order coefficient P_3 is independent from frequency, the overall behaviour is dictated by the monotonous increasing function P_2. The possibility to neglect the third order term in the equation to obtain a simpler and explicit solution is justified only if:

$$\frac{P_2(f_{\text{sw}})}{P_3} \gg \frac{V_{\text{in}}}{2} \;,\; \forall f_{\text{sw}} \geq f_{\text{limit}} \;, \tag{4.52}$$

where f_{limit} is the boundary frequency between the first and second operating regions (still to be derived). From the plot in Fig.4.9, at low frequencies the ratio

turns out to be around 45 V, only around three times the value $\frac{V_{\text{in}}}{2}$. As a consequence, the expected result will be a lower convergence of the model at the boundary with the first operating region, progressively increasing with the switching frequency.

Fig.4.10 reports the frequency behaviour of the equation coefficients.



(a) Coefficient P_3. **(b)** Coefficient P_2.

(c) Coefficient P_1. **(d)** Coefficient P_0.

Figure 4.10: Frequency behaviour of the cubic equation coefficients.

If the third order term is neglected, the cubic equation collapses into a quadratic one, and the solution ΔV can be explicitly computed as:

$$\Delta V(f_{\text{sw}}) \approx \frac{-P_1 + \sqrt{P_1^2 - 4P_0P_2}}{2P_2}\,. \tag{4.53}$$

The equation admits two real solutions, thanks to the positive determinant, but the negative one must be discarded. Fig.4.11 highlights the comparison between the numeric solution of Eq.4.50 (obtained through the *fsolve* macro of *Matlab*) and the approximated solution neglecting the third-order term. As expected, the two solutions tend to converge at higher frequencies: at the boundary with the first operating region, instead, the approximation leads to a 14% deviation. Although alternative techniques could be adopted to extract more precise analytical solutions, the rough approximation of neglecting the third-order term of Eq.4.50 is here

considered.

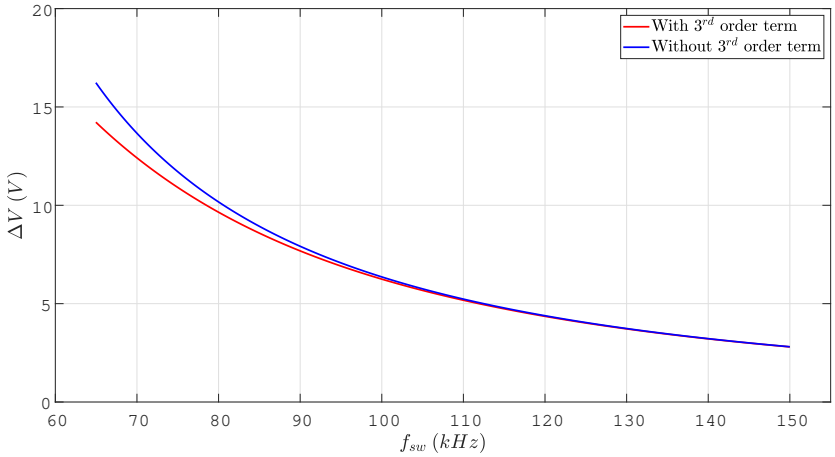


Figure 4.11: Comparison of the frequency behaviour of ΔV with and without third-order term approximation.

Once the variable ΔV is computed for a certain switching frequency, the load current I_{o} can be derived explicitly by using Eq.4.48. Eventually, the charging power can be simply derived by:

$$P_{\mathrm{out}}(f_{\mathrm{sw}}) = V_{\mathrm{batt}} I_{\mathrm{o}}(f_{\mathrm{sw}})\,. \tag{4.54}$$

.

With the parametres specified in Tab.4.1, the output current is plotted in Fig.4.12.

As the presented derivation has shown, the output power not only depends on the switching frequency, which is the control variable of the circuit. Since, for different physical reasons, both the PV module and battery electrical characteristics vary with time, for the same switching frequency the transferred power varies as well. In Chapter 6, the analytic static characteristics for a DC voltage source will be compared with simulated results extracted from *Simulink/PSIM*, to validate the models of the low frequency and high frequency operating regions.

Derivation of the limit frequency

As described, one of the main features of the high-frequency operating region is the impossibility for the load current to completely charge and discharge the dividing capacitors C_1 and C_2. In other words, the discontinuous voltage mode can't be

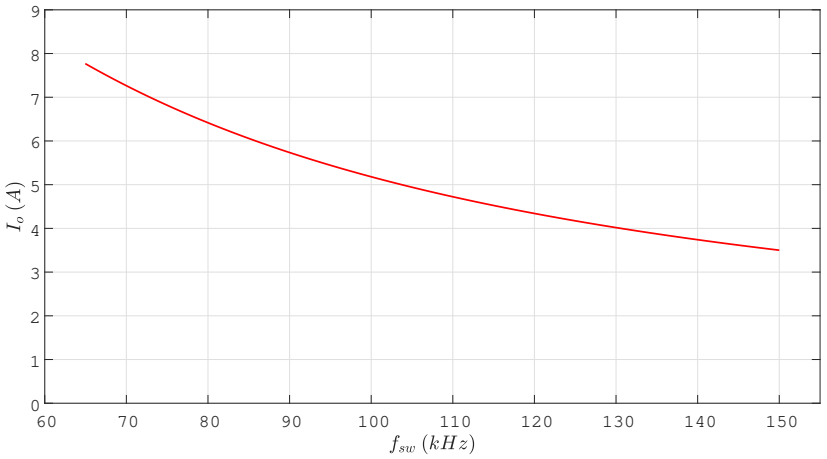


Figure 4.12: Frequency behaviour of the output current in the second operating region.

achieved in this working region, because ΔV is always lower than $\frac{V_{\text{in}}}{2} + V_{\text{F,D}}$. The boundary frequency f_{limit} between the two operating regions can be derived by imposing:

$$\Delta V(f_{\text{limit}}) \stackrel{!}{=} \frac{V_{\text{in}}}{2} + V_{\text{F,D}}\,. \tag{4.55}$$

Instead of deriving f_{limit} from Eq.4.50, which would lead to complex numerical computations, a simplified approach is followed, based on Eq.4.49. Assuming that the capacitors charging/discharging interval of time coincides with half a switching period, the simplified expression for ΔV becomes:

$$\Delta V \approx \frac{1}{8C f_{\text{sw}}} \frac{\frac{V_{\text{in}}}{2} - V_{\text{batt}}}{R_{\text{eq,1}}(\Delta V, f_{\text{sw}}) + R_{\text{eq,2}}(\Delta V, f_{\text{sw}}) + R_{\text{ext}} + R_{\text{batt}}}\,. \tag{4.56}$$

By combining Eqs.4.55 and 4.56, a second order equation for f_{limit} is obtained, whose explicit solution is:

$$f_{\text{limit}} = -\frac{R_{\text{batt}} + R_{\text{ext}}}{2(L_{\text{eff,1}} + L_{\text{eff,2}})} + \sqrt{\frac{1}{4}\left(\frac{R_{\text{batt}} + R_{\text{ext}}}{L_{\text{eff,1}} + L_{\text{eff,2}}}\right)^2 + \frac{\alpha_{\text{V}}}{8C(L_{\text{eff,1}} + L_{\text{eff,2}})}}\,, \tag{4.57}$$

where, for compactness of notation:

$$\begin{cases} L_{\text{eff},1} \triangleq \dfrac{4L_{\text{r}}}{2+\frac{4V_{\text{F,D}}}{V_{\text{in}}}} \\ L_{\text{eff},2} \triangleq \dfrac{4L_{\text{r}}}{2+\frac{V_{\text{in}}}{V_{\text{F,D}}}} \\ \alpha_{\text{V}} \triangleq \dfrac{\frac{V_{\text{in}}}{2}-V_{\text{batt}}}{\frac{V_{\text{in}}}{2}+V_{\text{F,D}}} \end{cases} . \tag{4.58}$$

4.5 Control

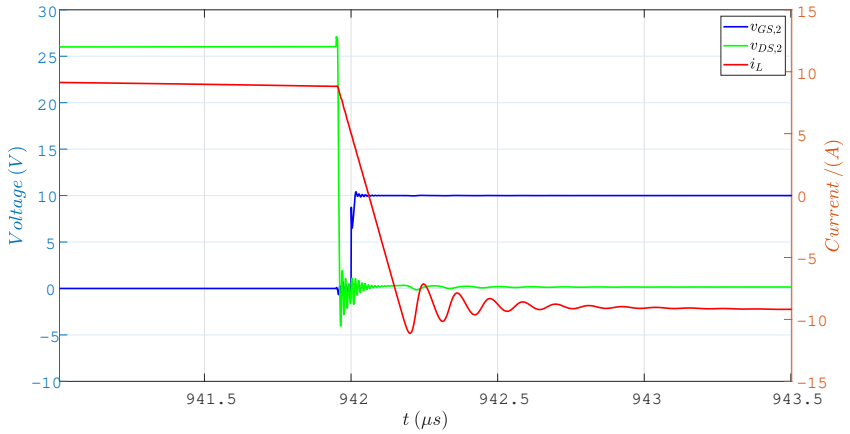
As mentioned, the converter adopts a frequency modulation to regulate the amount of average transferred power through a switching cycle. For any frequency condition, a symmetrical operation of the half bridge and the full bridge rectifier is needed to retrieve the described results. This section presents some considerations about how the gating signals algorithm influences the achievement of the ZVS condition for the half bridge, and proposes a novel dynamic control scheme. Moreover, in perspective of replacing a passive rectifier with an active one, its driving signals scheme is discussed.

4.5.1 Half-bridge MOSFETs control

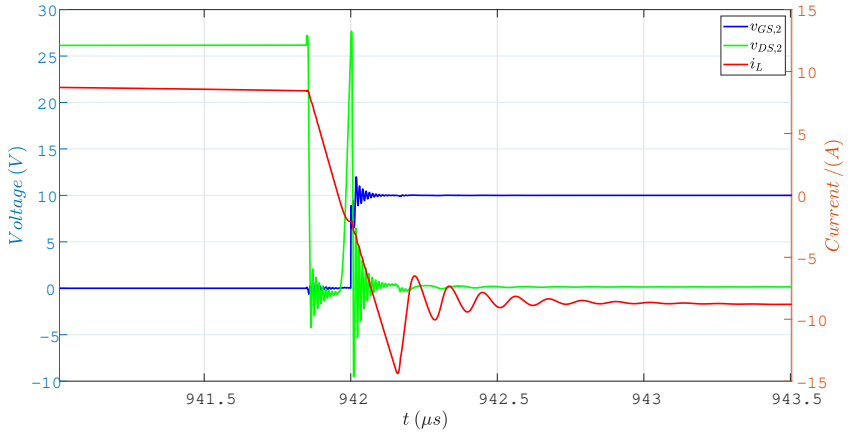
One of the main features already present in the constant-power charger proposed in [38] is the exploitation of inductance L_{r} to assist the soft switching of the half-bridge MOSFETs. The reason is that this inductance opposes to fast current changes, defining a time window in which MOSFETs M_1 (or M_2) can be turned ON at zero voltage. It is however of interest to evaluate when this condition can be obtained and how the time window is influenced by the working power and the value of L_{r}.

The available time window for which ZVS turn ON can be achieved is limited by t_3 (Eq.4.13) and $t_3 + t_4$ (where t_4 is expressed in Eq.4.15). Considering M_2 turn ON, for instance, the ZVS condition can be achieved if its output capacitance has already been discharged, its body diode is conducting and the current i_L has not reversed yet. Fig.4.13, obtained through a *LTSpice XVII*[1] simulation, compares two situations in which ZVS turn ON is achieved (on the left) and not (on the right). As expected, when the gate driver signal v_{GS} is sent after the current zero-crossing, the output voltage starts rising again and the ZVS condition is lost.

[1] `https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html`.



(a) Waveforms with 50 ns deadtime.



(b) Waveforms with 150 ns deadtime.

Figure 4.13: MOSFET M_2 voltages and L_r current during M_2 turn-ON, under two different deadtime conditions.

Fig.4.14 shows the minimum and maximum allowed values of deadtime as function of the choice of inductance L_r. Three curves are reported for three different values of output power. Due to the slightly different expressions of t_3 and t_4 for the two described operating regions, different curves should be obtained. However, it is possible to prove that very similar results are retrieved in the two cases. The graphs are plotted for constant input voltage (28 V) and battery voltage (12 V). As shown, the duration of Mode 3.1 looks negligible when compared to Mode 3.2. The upper boundary of allowed deadtime is nearly proportional to the output power (thus, to the output current) and, as expected, is also proportional to L_r.

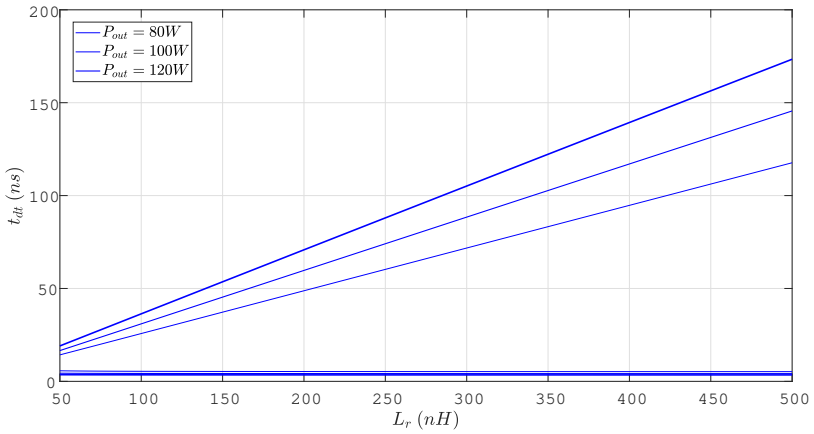


Figure 4.14: Influence of the inductance value L_r on the minimum and maximum allowed dead-time for achieving M_1/M_2 ZVS turn ON.

The selection of L_r should take into account several aspects:

- for very low values of inductance ($\approx 10^1 nH$), the allowed deadtimes for ZVS reduce to few tens of ns or below. Such time constraints may become incompatible with real devices (MOSFETs and gate drivers) characterized by switching and propagation delays. Moreover, L_r should be large enough to satisfy Eq.3.6;
- for higher values, the contribution of L_r reactance becomes more and more significant, eventually shifting to lower frequencies the boundary between first and second operating regions. Fig.4.15 shows the dependence of f_limit on the inductance value L_r. Since $P_\mathrm{out,max} \approx 2CV_\mathrm{in}^2 f_\mathrm{limit}$, for the same source and battery voltages, lower maximum powers can be achieved with higher inductance values. At the same time, the time window constraint is more relaxed.

As a consequence, the value of L_r should consider both timing constraints and power requirements. A unique value of deadtime for the half-bridge MOSFETs could be selected in principle, from average power considerations. However, due to the intrinsically time-varying electrical characteristic of a PV source, it may become necessary to dynamically modify the half-bridge deadtime according to environmental conditions. In this work, an innovative ZVS-tracking control scheme is designed: it is based on the acquisition of the M_2 output voltage immediately before its turn-ON:

1. a negative $v_\mathrm{DS,2}$ highlights that the body diode of M_2 is conducting, and that ZVS can be achieved if the MOSFET is turned ON immediately after. Notice

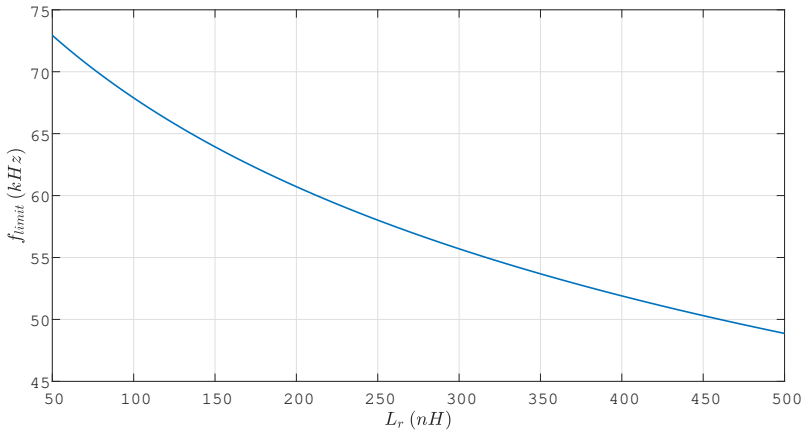


Figure 4.15: Influence of the inductance value L_r on the boundary frequency between the two operating regions.

that the average value of the negative voltage is disturbed by the voltage oscillations linked to inductive parasitics: the bandwidth of the acquisition system should be low enough to ensure a good filtering of these high-frequency oscillations;

2. assuming a negligible time for Mode 3.1, a positive $v_{\mathrm{DS},2}$ would be linked to a too large delay in turning ON the MOSFET, when the current i_L has already reversed. In this case, in the following switching cycles, the deadtime should be reduced to increase the possibility to obtain ZVS turn ON.

As it can be noticed, this algorithm is based only on the acquisition of the polarity of $v_{\mathrm{DS},2}$, and not on its actual value. As a consequence, from a physical implementation point of view, the adoption of a fast comparator could be enough, rather than relying on an ADC. The control scheme will be validated through simulations in Chap.6.

4.5.2 Full-wave rectifier MOSFETs control

Contrarily to the converter in [38], where the combination of a center-tapped transformer and a two-diode rectifier was sufficient to provide a full-wave rectification, the absence of a transformer here forces to adopt a traditional Graetz-bridge rectifier. A conventional passive rectifier, however, is source of significant conduction losses and of a double forward-voltage drop between primary and secondary side voltages. This limitation becomes significant if the constraints of Eq.4.38 are considered.

For these two reasons, with the aim of reducing conduction losses and relaxing the voltage constraints, a MOSFET-based active rectifier is here adopted. From the control point of view, these MOSFETs should replicate the conduction scheme of a passive rectifier: if this happens, the qualitative behaviour of the previously described waveforms is still valid, but with a reduced switch voltage drop (approximately $R_{\mathrm{DS,ON}} I_{\mathrm{D,S}}$ instead of $V_{\mathrm{F,D}}$). From now on, diodes $D_3 - D_6$ of Fig.4.1 will be replaced with MOSFETs $M_3 - M_6$, respectively (Fig.4.16).

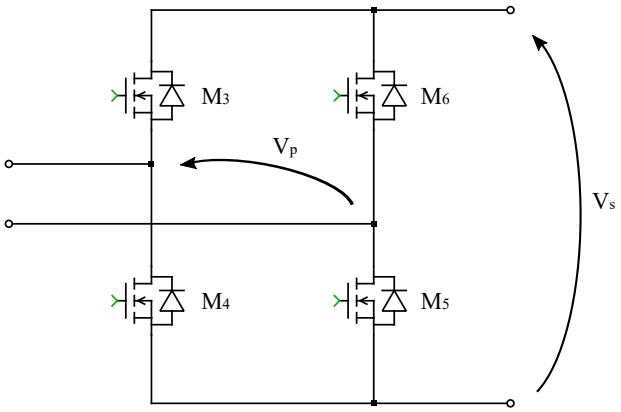
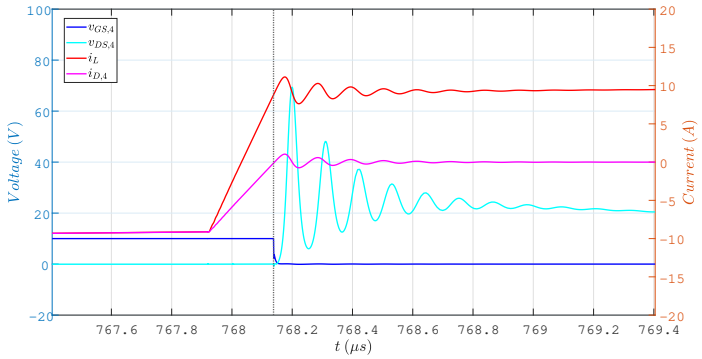


Figure 4.16: Schematic of the MOSFET-based active rectifier.

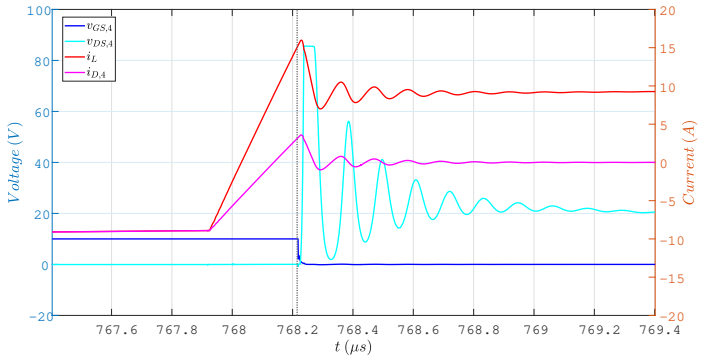
During the positive half-wave of i_L, M_3 and M_5 conduct the load current. During Mode 3.1, in absence of any change in the gating signals scheme, the body diodes of M_4 and M_6 would anyway start conducting to enable the L_{r} current discharge. Their turn ON driving signal can be sent in at any time of the *crossover resonant state*: however, to reduce the conduction losses, it is preferable to turn ON MOSFETs before the end of Mode 3. In the scheme adopted in this work, M_4 and M_6 are turned ON simultaneously with M_2, whereas M_3 and M_5 are turned ON with M_1. Since their body diodes are already conducting, all the rectifier MOSFETs are turned ON at zero voltage condition.

The turn OFF control of the MOSFETs, instead, represents the real difference with a passive rectifier, and the main challenge to avoid significant switching losses. Contrarily to diodes, which would be naturally turned OFF as soon as their current goes to zero (Zero-Current turn OFF), the current through the rectifier MOSFETs would keep flowing as long as the conducting channel is formed, even when the L_{r} has reached and overcome I_{o} (or $-I_{\mathrm{o}}$). The reason is that, during Mode 3.3, the inductor voltage v_L, as long as all the rectifier MOSFETs conduct, is clamped at $V_{\mathrm{in}} - v_{\mathrm{x}}(t)$ (or $-v_{\mathrm{x}}(t)$). As a result, the L_{r} current would keep increasing or decreasing. To prevent this phenomenon, which results in a significant switching

power dissipation, the rectifier MOSFETs should be turned OFF when their current is zero (ZCS). Fig.4.17 compares two different situations in which M_4 (left leg, low side) switches at zero current and not.



(a) Voltage and current waveforms at ZCS turn OFF condition.



(b) Voltage and current waveforms in absence of ZCS turn OFF condition.

Figure 4.17: MOSFET M_4 voltages and current, and L_r current during M_4 turn OFF, under two different timing schemes.

As shown, the non-zero current switching results in a large resonant voltage spike across the MOSFET during turn OFF: contrarily to the first case, the voltage spike is clamped at the breakdown voltage, nearly 80 V. This situation should be avoided as much as possible because the temporary switching losses associated to the breakdown region may destroy the device. Fig.4.18 compares the instantaneous power dissipation in case of ZCS and HS (hard switching). Clearly, the commutation losses averaged through a switching cycle are larger in the hard-switching case. In Chap.6, a more detailed report of switching losses as function of the gating signals timing is reported.

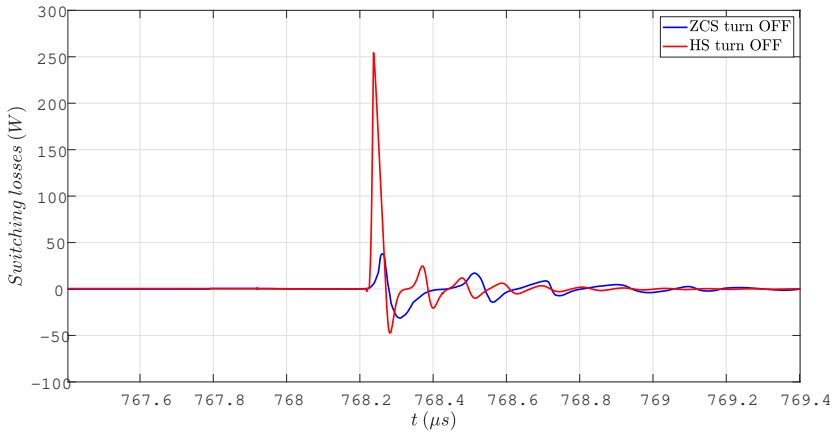


Figure 4.18: Comparison of instantaneous switching losses in case of ZCS and HS turn OFF of M_4.

The unitary switching functions representative for the gating signals of the half-bridge MOSFETs and rectifier MOSFETs are shown in Fig.4.19. The duration of the interval dt is set by the above mentioned control algorithm to track dynamically the ZVS turn ON condition for M_2 (thanks to the symmetry, also for M_1). The duration of interval dt_1 can also, in principle, be set according to a dynamic control scheme. Let's consider as reference situation, for instance, the interval of time between M_3/M_5 turn OFF and M_2/M_4 turn ON. A possible solution would be to acquire the M_2 output voltage immediately before its turn OFF: what is meaningful to acquire is not the actual value of this voltage, but just its polarity, as in the previously described control for the half-bridge MOSFETs. Since the desirable situation would be to turn OFF M_2 when its current crosses zero, and since $v_{\mathrm{DS},2} \approx R_{\mathrm{DS,ON}} i_{\mathrm{D},2}$, the polarity of $v_{\mathrm{DS},2}$ highlights if the turn OFF occurs too early (negative voltage, current flowing from source to drain) or too late (positive voltage, current flowing from drain to source). However, there is a fundamental distinction with the previous control scheme: the voltage to be acquired, considering ON-state resistances of few $m\Omega$, turns out to be in the mV-order of magnitude. This fact forces the comparator to exhibit extremely low offset voltage and current in order not to compromise the measurement. In any case, the signal-to-noise ratio (SNR) of the input signal would be too low to offer a reliable estimation of the ZCS condition. Any spurious voltage oscillation resulting from the just occurred commutation of M_1 would compromise the measurement.

For this reason, a "sensorless" approach is adopted for the rectifier MOSFETs driving. This is based on the following considerations or assumptions:

- the L_r current transition during Mode 3 is approximately linear;
- the control algorithm for the half bridge MOSFET M_2 is able to ensure its turn ON at the zero crossing of i_L, after a time dt from the M_1 turn OFF (and viceversa).

If these conditions are true, then the time required for i_L to move from I_o to $-I_o$ is $2dt$ (Fig.4.17). As a result, the overall dynamic control only adjusts dt, and imposes $dt_1 = dt$. As a consequence, in principle, achieving ZVS turn ON of the half-bridge MOSFETs should ensure at the same time ZCS turn OFF of the rectifier MOSFETs.

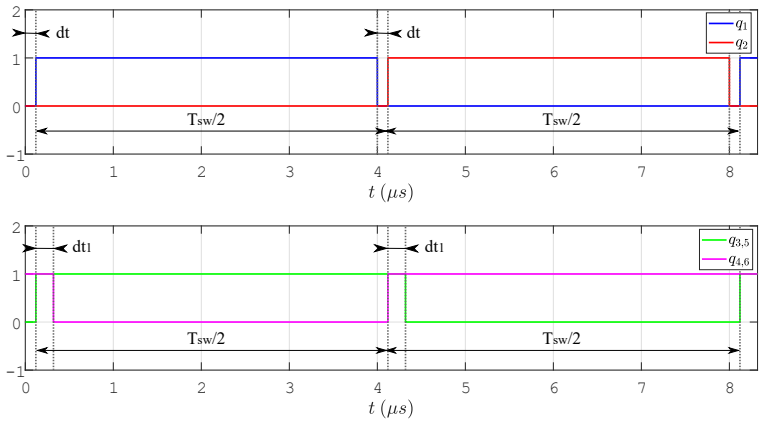


Figure 4.19: Unitary switching functions for the the half-bridge (above) and rectifier (below) MOSFETs.

Chapter 5

Modified topology with larger resonant inductance L_r

5.1 General features

In this chapter, an alternative version of frequency-modulated power converter is described and discussed. The starting point for an improvement of the previously presented converter is a combination of two factors:

- as already outlined in Fig.4.14, an increased inductance L_r value allows to soften the deadtime constraints to achieve ZVS turn ON of the half-bridge MOSFETs;

- the presence of two inductors, needed for the desired operation of the converter, is critical from the point of view of losses. Inductors are indeed characterized by conductor and core losses: the latter, especially, are difficult to predict. In perspective of a high-efficiency and high-power density converter, the reduction of the number of required inductors may bring benefits in terms of PCB surface and losses.

From these considerations, this work considers an alternative topology in which the inductor value is increased up to the μH region and the output inductive filter is replaced by a capacitive one, as shown in Fig.5.1. In the following derivations, the output capacitance C_o will be assumed to be sufficiently large to maintain a constant voltage V_o throughout a switching cycle.

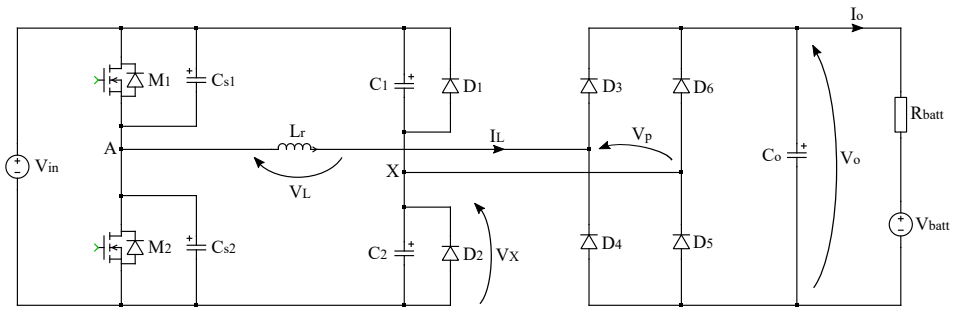


Figure 5.1: Schematic with the alternative topology with increased L_r value and output capacitive filter.

The first significant consequence of increasing the inductance value is to decrease the resonance frequency between the equivalent capacitance $2C$ and L_r, for the same C value. Assuming, for instance, to work with $C_1 = C_2 = 680\,\mathrm{nF}$ and $L_\mathrm{r} = 2.2\,\mu\mathrm{H}$, the resonant frequency results:

$$f_\mathrm{res} = \frac{1}{2\pi\sqrt{2CL_\mathrm{r}}} \approx 92\,\mathrm{kHz}\,, \tag{5.1}$$

which is a reasonable switching frequency for MOSFET-based low/medium power converters (around 100 W). Although the working principle for power transfer is still based on energy store and release of the dividing capacitors within a switching cycle, their charging current i_L is no more approximately constant within a half-cycle, but starts being influenced by the resonance tank, if the switching frequency is sufficiently near to f_res. Both v_x and i_L start assuming the sinusoid-like behaviours of a traditional series-resonant converter (SRC), which will be detailed in the following section.

In the previous topology, the clamping diodes D_1 and D_2 were needed to clamp the voltage at node X to V_in and GND, ensuring the desired relation $P_\mathrm{out} \approx 2Cf_\mathrm{sw}V_\mathrm{in}^2$ in the first operating region. The linearity with the switching frequency was then ensured up the limit frequency between the two described operating regions (Eq.4.57). Here, the resonance frequency $f_\mathrm{res,2} = \frac{1}{2\pi\sqrt{2CL_\mathrm{r}}}$, as will be proved in the following sections, becomes the boundary between two working regions: inductive ($f_\mathrm{sw} > f_\mathrm{res,2}$) and capacitive ($f_\mathrm{sw} < f_\mathrm{res,2}$). As described in [11], the capacitive region is characterized by a leading inductor current of the tank, whereas the current lags in the inductive region. Since the topology is conceived to preserve the ZVS turn ON feature already present in the previous one, it is desirable to operate the converter in the inductive region, in which the inductor current i_L still exhibits the correct polarity to charge/discharge the parasitic capacitances of the MOSFETs during the half-bridge deadtime. In the capacitive region, instead,

i_L reverses before M_1 (or M_2) is turned OFF, preventing ZVS turn ON of the other MOSFETs. The hard-switching condition causes considerable efficiency loss (shown further in this work), and thus the operation in capacitive region is not explored.

Since the resonance frequency becomes the switching frequency at which the maximum power transfer occurs, the clamping diodes lose their role to ensure a linear relationship $P_{\text{out}}(f_{\text{sw}})$ at low frequencies: thus, they can be avoided in the topology (Fig.5.2).

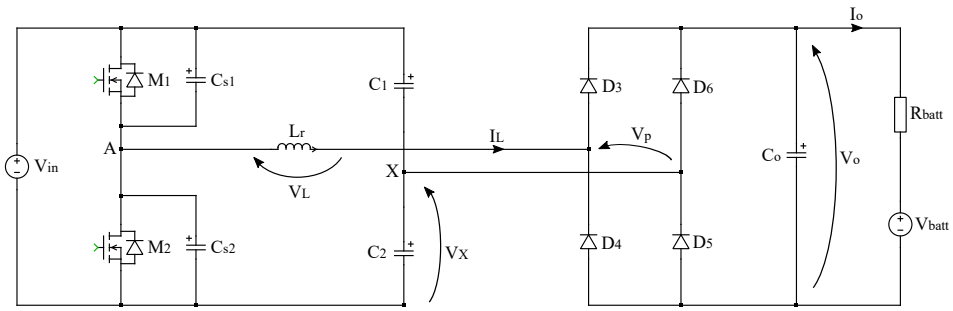


Figure 5.2: Schematic of the alternative topology without clamping diodes.

5.2 Working operation in the inductive region

As previously done for the other topology, this section presents the main mathematical equations for the time-domain description of the behaviour of the converter in the inductive region ($f_{\text{sw}} > f_{\text{res},2}$). The working operation during half cycle can be divided into two modes (in absence of clamping diodes): the symmetrical operation allows to easily derive the behaviour during the other half cycle. Actually, as before, the second mode can be in turns subdivided. The following assumptions are considered to simplify the analysis:

- the input voltage source is assumed to be constant within the switching period;
- the output capacitor is assumed to be sufficiently large to maintain a constant secondary voltage $v_{\text{sec}}(t) = V_{\text{o}}$ throughout the entire switching period;
- the MOSFETs ON-state voltage is assumed to be null. The output capacitances are the only parasitics considered in the derivation. When the MOSFET is OFF but its body diode is conducting, it is modelled by a negative DC drain-source voltage source equal to $-V_{\text{F,M}}$;
- all the diodes (from D_1 to D_6) are equal and are modelled by constant DC voltage sources $V_{\text{F,D}}$ while they conduct. No reactive parasitic nor forward/reverse

recovery is considered: as a consequence, their commutation is instantaneous;

- the reactive components C_1, C_2, L_r and L_o are lossless and ideal. Moreover, $C_1 = C_2 = C$.

A passive rectifier diode is considered for the analysis, although the control design will be based on an active rectifier, thanks to the possibility to achieve a higher efficiency. In the following derivation, the working modes refer to the half switching cycle in which the current i_L is positive (according to the polarity of Fig.5.2. Notice that the output capacitor prevents the rectifier diodes to conduct all simultaneously, as in the previous topology. As a consequence, a positive i_L is carried by D_3 and D_5, whereas D_4 and D_6 conduct i_L when it's negative.

5.2.1 Mode 1

Mode 1 begins when M_1 is turned ON. The following consideration is taken as assumption: the control ensures M_1 turn ON exactly when the negative current i_L crosses the zero, becoming positive. D_3 and D_5 start conducting i_L and, as a consequence, $v_\mathrm{p} = V_\mathrm{o} - 2V_\mathrm{F,D}$. The currents directions and the conducting devices are shown in Fig.5.3a. During this mode, the inductor L_r enters in resonance with the dividing capacitors. The resonant behaviour is described by the following system of ODEs:

$$\begin{cases} i_L = 2C\dfrac{dv_\mathrm{x}}{dt} \\ L_\mathrm{r}\dfrac{di_L}{dt} = V_\mathrm{in} - V_\mathrm{o} - 2V_\mathrm{F,D} - v_\mathrm{x} \end{cases} . \tag{5.2}$$

By combining the two equations, a single 2^{nd} order ODE can be obtained for v_x, whose solution allows to derive also i_L:

$$\begin{cases} v_\mathrm{x}'' + \omega_{\mathrm{res},2}^2 v_\mathrm{x} = \omega_{\mathrm{res},2}^2 (V_\mathrm{in} - V_\mathrm{o} - 2V_\mathrm{F,D}) \\ v_\mathrm{x}(0) = \dfrac{V_\mathrm{in}}{2} - V_1 \\ v_\mathrm{x}'(0) = \dfrac{i_\mathrm{L}(0)}{2C} = 0 \end{cases} . \tag{5.3}$$

V_1 is an unknown voltage variable representing the gap with the capacitors DC voltage, $\frac{V_\mathrm{in}}{2}$. It value cannot be established *a priori* and can be computed by solving a non-linear system of equation presented further in this section. The expressions of some of the relevant waveforms during this mode are reported in Eq.5.4.

$$\begin{cases} v_{\mathrm{x}}(t) = V_{\mathrm{in}} - V_{\mathrm{o}} - 2V_{\mathrm{F,D}} + \left(-\frac{V_{\mathrm{in}}}{2} - V_1 + V_{\mathrm{o}} + 2V_{\mathrm{F,D}} \right) \cos\left(\omega_{\mathrm{res},2}(t - t_0)\right) \\ v_L(t) = \left(-\frac{V_{\mathrm{in}}}{2} - V_1 + V_{\mathrm{o}} + 2V_{\mathrm{F,D}} \right) \cos\left(\omega_{\mathrm{res},2}(t - t_0)\right) \\ i_L(t) = -2C\omega_{\mathrm{res},2} \left(-\frac{V_{\mathrm{in}}}{2} - V_1 + V_{\mathrm{o}} + 2V_{\mathrm{F,D}} \right) \sin\left(\omega_{\mathrm{res},2}(t - t_0)\right) \\ v_{\mathrm{p}}(t) = V_{\mathrm{o}} - 2V_{\mathrm{F,D}} \\ v_{\mathrm{s}}(t) = V_{\mathrm{o}} \end{cases} . \tag{5.4}$$

Mode 1 ends when M_1 turns OFF, at t_1. In absence of clamping diodes, indeed, the described resonant behaviour cannot be interrupted by any other switching device. At the end of this mode, after a time $t_1 - t_0 < \frac{T_{\mathrm{sw}}}{2}$, the resonant variables assume the following values (to be determined):

$$\begin{cases} i_L(t_1) = I_{\mathrm{L},1} \\ v_{\mathrm{x}}(t_1) = \frac{V_{\mathrm{in}}}{2} + V_2 \end{cases} . \tag{5.5}$$

5.2.2 Mode 2

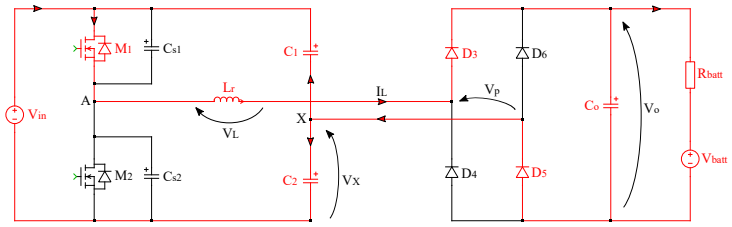
As in the previously described topology, the more complex working mode describing the behaviour of the converter during the half-bridge deadtime, can be further subdivided.

Mode 2.1

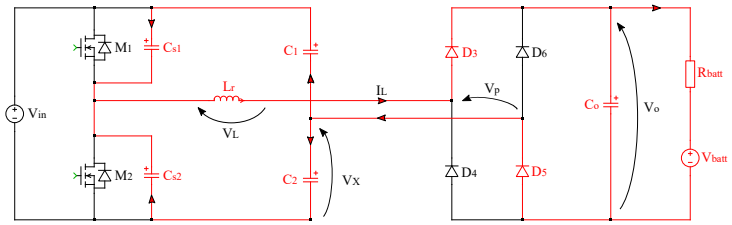
When M_1 is turned OFF, the still positive current i_L starts discharging $C_{\mathrm{s}2}$ and charging $C_{\mathrm{s}1}$ (Fig.5.3b). The fact that the current is still positive comes directly from the inductive operation of the converter: the equivalent square-wave voltage generator at node A sees a globally inductive load, resulting in a lagging resonant current i_L.

This very short mode lasts until the $v_{\mathrm{DS},2}$ voltage becomes negative, turning ON the body diode of M_2. During this mode, L_{r} starts resonating with the series equivalent capacitance composed of $2C_{\mathrm{s}}$ and $2C$. However, considering that C_{s} takes into account only parasitic capacitances ($C_{\mathrm{s}} \ll C$), it is reasonable to assume that the resonance frequency is not affected by $2C$:

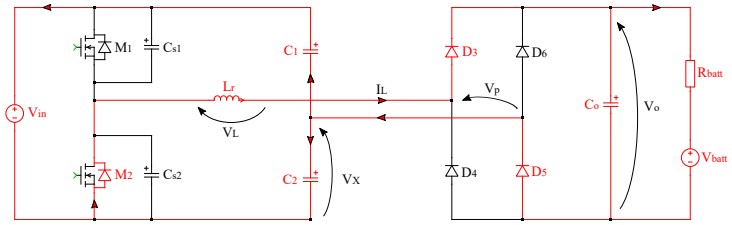
$$f_{\mathrm{res}} \approx \frac{1}{2\pi\sqrt{2C_{\mathrm{s}}L_{\mathrm{r}}}} . \tag{5.6}$$



(a) Mode 1.



(b) Mode 2.



(c) Mode 3.

Figure 5.3: Operation of the modified battery charger during the different modes.

From the KCL applied at nodes A and X, the following relation holds:

$$2C\frac{dv_{\mathrm{x}}}{dt} = -2C_{\mathrm{s}}\frac{dv_{\mathrm{DS},2}}{dt}\,, \tag{5.7}$$

from which it is possible to make another simplifying assumption:

$$\Delta v_{\mathrm{x}}(\text{mode 2.1}) = -\frac{C_{\mathrm{s}}}{C}\Delta v_{\mathrm{DS},2}(\text{mode 2.1}) \approx -\frac{C_{\mathrm{s}}}{C}V_{\mathrm{in}} \approx 0\,. \tag{5.8}$$

If v_{x} is assumed to be constant and equal to $\frac{V_{\mathrm{in}}}{2} + V_2$ during this mode, the resonant behaviour or i_{L} is described by the following ODE (considering to move the time origin at the beginning of this mode):

$$\begin{cases} i_L'' + \omega_{\mathrm{res}}^2 i_L \approx 0 \\ i_L(0) = I_{\mathrm{L},1} \\ i_L'(0) = -\dfrac{V_{\mathrm{o}} + 2V_{\mathrm{F,D}} + \frac{V_{\mathrm{in}}}{2} - V_2}{L_{\mathrm{r}}} \end{cases}\,. \tag{5.9}$$

From the solution of this 2^{nd} order ODE, all the other relevant quantities on the converter can be derived (Eq.5.10).

$$\begin{cases} v_{\mathrm{x}}(t) \approx \dfrac{V_{\mathrm{in}}}{2} + V_2 \\ v_L(t) = -L_{\mathrm{r}}\omega_{\mathrm{res}} I_{\mathrm{L},1} \sin\Big(\omega_{\mathrm{res}}(t-t_1)\Big) - \left(V_{\mathrm{o}} + 2V_{\mathrm{F,D}} + \dfrac{V_{\mathrm{in}}}{2} - V_2\right) \cos\Big(\omega_{\mathrm{res}}(t-t_1)\Big) \\ i_L(t) = I_{\mathrm{L},1} \cos\Big(\omega_{\mathrm{res}}(t-t_1)\Big) - \dfrac{1}{\omega_{\mathrm{res}} L_{\mathrm{r}}} \left(V_{\mathrm{o}} + 2V_{\mathrm{F,D}} + \dfrac{V_{\mathrm{in}}}{2} - V_2\right) \sin\Big(\omega_{\mathrm{res}}(t-t_1)\Big) \\ v_{\mathrm{p}}(t) = V_{\mathrm{o}} - 2V_{\mathrm{F,D}} \\ v_{\mathrm{s}}(t) = V_{\mathrm{o}} \end{cases} . \tag{5.10}$$

From the KCL applied at node A, and adopting a Taylor expansion at the first order to simplify the expression:

$$v_{\mathrm{DS},2}(t) \approx V_{\mathrm{in}} - L_{\mathrm{r}} I_{\mathrm{L},1} \omega_{\mathrm{res}}^2 (t - t_0) \,. \tag{5.11}$$

The above-mentioned approximation would only be valid if the duration of this mode is short enough, specifically $t_2 - t_1 \ll \frac{2\pi}{\omega_{\mathrm{res}}}$. This approximation must be validated *a posteriori*. Assuming it is valid:

$$t_2 - t_1 \approx \frac{V_{\mathrm{in}} + V_{\mathrm{F,M}}}{L_{\mathrm{r}} I_{\mathrm{L},1} \omega_{\mathrm{res}}^2} \,. \tag{5.12}$$

Let's denote by $I_{\mathrm{L},2}$ the value assumed by i_L at the end of this sub-mode ($I_{\mathrm{L},2} = i_L(t_2)$).

Mode 2.2

When the voltage $v_{\mathrm{DS},2}$ turns ON the body diode of M_2, it completely carries the current i_L (mode 2.2 begins, represented in Fig.5.3c). The same consideration for the maximum allowed deadtime made before is valid here: if MOSFET M_2 is turned ON during this sub-mode, the turn ON occurs at zero voltage; otherwise, the current would revers and the ZVS condition would be lost. During this sub-mode, L_{r} resonates again with the equivalent capacitance $2C$. As a consequence, the converter behaviour is described by the same equations, beside the voltage at node A ($-V_{\mathrm{F,M}}$ instead of V_{in}) and the initial conditions of the ODEs.

Globally:

$$\begin{cases} v_{\mathrm{x}}(t) = -V_{\mathrm{o}} - 2V_{\mathrm{F,D}} - V_{\mathrm{F,M}} + \left(\frac{V_{\mathrm{in}}}{2} + V_2 + V_{\mathrm{o}} + 2V_{\mathrm{F,D}} + V_{\mathrm{F,M}}\right)\cos\left(\omega_{\mathrm{res},2}(t-t_2)\right) + \frac{I_{\mathrm{L},2}}{2C}\sin\left(\omega_{\mathrm{res},2}(t-t_2)\right) \\ v_L(t) = -\left(\frac{V_{\mathrm{in}}}{2} + V_2 + V_{\mathrm{o}} + 2V_{\mathrm{F,D}} + V_{\mathrm{F,M}}\right)\cos\left(\omega_{\mathrm{res},2}(t-t_2)\right) - \frac{I_{\mathrm{L},2}}{2C}\sin\left(\omega_{\mathrm{res},2}(t-t_2)\right) \\ i_L(t) = -2C\omega_{\mathrm{res},2}\left(\frac{V_{\mathrm{in}}}{2} + V_2 + V_{\mathrm{o}} + 2V_{\mathrm{F,D}} + V_{\mathrm{F,M}}\right)\sin\left(\omega_{\mathrm{res},2}(t-t_2)\right) + I_{\mathrm{L},2}\cos\left(\omega_{\mathrm{res},2}(t-t_2)\right) \\ v_{\mathrm{p}}(t) = V_{\mathrm{o}} - 2V_{\mathrm{F,D}} \\ v_{\mathrm{s}}(t) = V_{\mathrm{o}} \end{cases} \tag{5.13}$$

This final sub-mode ends when the current becomes null. The duration of this mode, $t_3 - t_2$ can then be derived by imposing $i_L(t_3) = 0$, resulting in:

$$t_3 = \frac{T_{\mathrm{sw}}}{2} = \frac{1}{\omega_{\mathrm{res},2}}\tan^{-1}\left(\frac{I_{\mathrm{L},2}}{2C\omega_{\mathrm{res},2}\left(V_{\mathrm{o}} + 2V_{\mathrm{F,D}} + V_{\mathrm{F,M}} + \frac{V_{\mathrm{in}}}{2} + V_2\right)}\right) \tag{5.14}$$

All the previously presented describing equations are functions of multiple unknowns that must still be defined. Specifically, the duration of mode 1 (t_1), of mode 2 ($t_2 - t_1$), $I_{\mathrm{L},1}$, $I_{\mathrm{L},2}$, V_1 and V_3. A set of 6 continuity equations (2 for the voltage v_{x}, 3 for the current i_L and 1 for $v_{\mathrm{DS},2}$) is sufficient to derive the unknowns after fixing the working frequency:

$$\begin{cases} i_L(t_1) \overset{!}{=} I_{\mathrm{L},1} \\ v_{\mathrm{x}}(t_1) \overset{!}{=} \frac{V_{\mathrm{in}}}{2} + V_2 \\ i_L(t_2) \overset{!}{=} I_{\mathrm{L},2} \\ v_{\mathrm{DS},2}(t_2) \overset{!}{=} -V_{\mathrm{F,M}} \\ i_L\left(\frac{T_{\mathrm{sw}}}{2}\right) \overset{!}{=} 0 \\ v_{\mathrm{x}}\left(\frac{T_{\mathrm{sw}}}{2}\right) \overset{!}{=} \frac{V_{\mathrm{in}}}{2} + V_1 \end{cases} \tag{5.15}$$

Listing A.4 in Appendix provides the Matlab function defining the 6 equations of the non-linear system to be solved with the use of the *fsolve* macro.

Finally, Fig.5.4 reports the half-bridge MOSFETs driving and output voltages, the voltage at node X and the resonant inductor voltage and current. The output parasitic capacitances of the MOSFETs have been exaggerated ($\approx 2\,\mathrm{nF}$) to make mode 2.1 better visible. As mentioned, it is less relevant to report v_{p} and v_{s}, which are constant and equal to $V_{\mathrm{o}} - 2V_{\mathrm{F,D}}$ and V_{o}, respectively. During the entire half-cycle, moreover, the inductor current flows through D_3 and D_5, while D_4 and D_6

are always OFF. As a consequence, an instantaneous positive power is transferred during all the half cycle (differently from the previously presented topology, in which the rectifier behaves as a free-wheeling path during the *crossover resonant* mode). Moreover, it is interesting to observe that the inductor current becomes approximately linear during mode 2.2: when approaching the resonance frequency, this mode gradually disappears and i_L assumes a sinusoidal behaviour.

In the previous computations, the duration of mode 2.1 was assumed to be sufficiently short to approximate the sinusoidal behaviour into a linear one (only if $t_2 - t_1 \ll \frac{2\pi}{\omega_{\text{res}}}$). From the parametres adopted for the plots in Fig.5.4, for instance, the inequality holds, since:

$$t_2 - t_1 \approx 45\,\text{ns} \ll \frac{2\pi}{\omega_{\text{res}}} \approx 590\,\text{ns}\,. \tag{5.16}$$

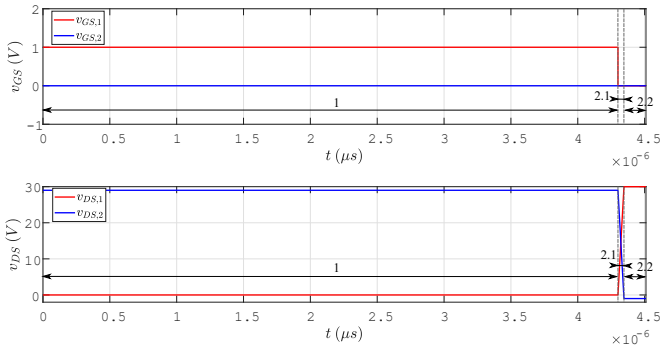
5.3 Static characteristic in the neighborhood of the resonance frequency

In this section, a simplified derivation of the static characteristic $P(f_{\text{sw}})$ based on the First Harmonic Approximation (FHA) is presented. This modelling technique, already described in detail in [11], is based on the assumption that only the first harmonic components of the resonant current or voltage contribute to the power transfer. Clearly, this approximation becomes more and more valid when approaching the resonance frequency, at which the resonant quantities are exactly sinusoidal. Far from the resonance frequency, the contributions of higher order harmonics cannot be neglected and improved modelling techniques must be adopted, such as the Extended FHA [40].

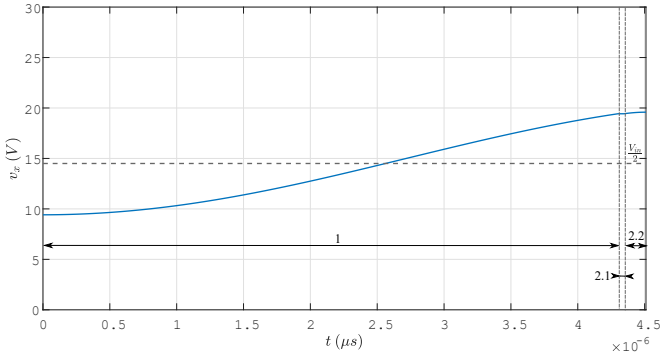
In this context, since the converter control is intended to be based on a MPPT technique, it is of interest to model the static characteristic especially around the resonance frequency, where the maximum power can be extracted. As a consequence, the simplified FHA is adopted here. When the converter operation is analysed only for the first harmonic, the equivalent circuit in Fig.5.5 is obtained, where:

- $V_{\text{A,1}}$ is the fundamental component of the square wave generated at the output node of the half-bridge (node A). Since the amplitude of the square wave, assumed to be ideal, is V_{in}, the corresponding fundamental component is:

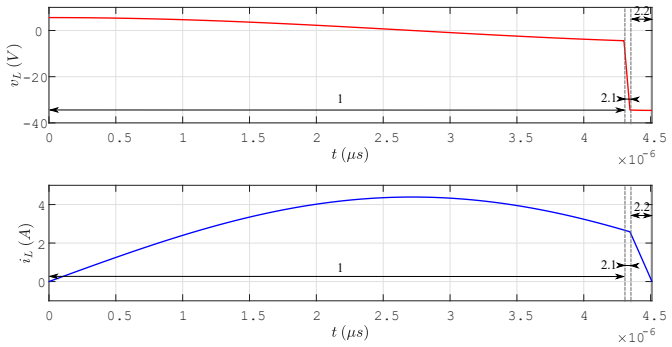
$$V_{\text{A,1}} = \frac{4}{\pi}\frac{V_{\text{in}}}{2}e^{j\alpha}\,, \tag{5.17}$$



(a) MOSFETs driving signals and output voltages.



(b) Voltage at node X.



(c) Inductor L_r voltage and current.

Figure 5.4: Relevant waveforms of the analysed converter within a half cycle.

where α is defined as the phase shift with the current phasor $I_{\mathrm{L},1}$;

- L_r and $2C$ are the lossless component of the resonant tank. Notice that, since V_in is assumed to be constant, the 2 dividing capacitors C_1 and C_2 appear in

parallel;

- r represents the equivalent series resistance modelling the inductor, MOSFET and capacitors conduction losses. This resistance significantly affects the quality factor of the resonance and must then be considered. The parametre r should be derived after the components selection as a sum of the various resistive parasitic contributions;

- R_{eq} represents the equivalent virtual resistive impedance seen at the input of the rectifier. The reason why this impedance is resistive is that the rectifier diodes (or MOSFETs) conduction is such that the square wave primary voltage v_{p} results in phase with the sinusoidal current i_L. Thus, R_{eq} can be expressed by the ratio of the fundamental components of v_{p} and i_L:

$$R_{\mathrm{eq}} = \frac{4V_{\mathrm{o}}}{\pi I_{\mathrm{L},1}}\,, \tag{5.18}$$

where V_{o} is the DC voltage across the output capacitor.

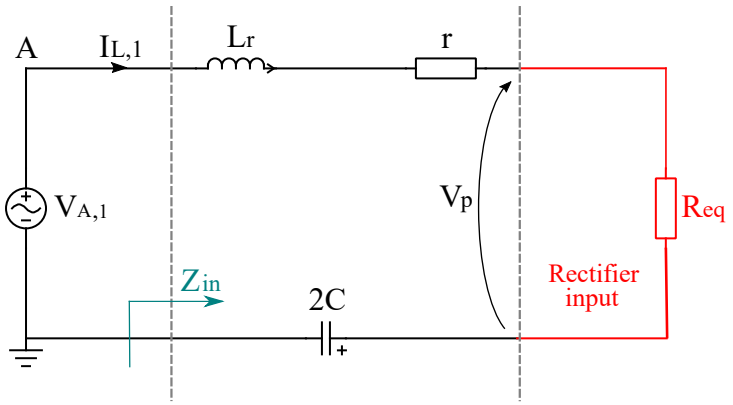


Figure 5.5: Equivalent converter circuit in the FHA.

In the following derivation, the voltage drops across the rectifier devices is neglected ($P_{\mathrm{Req}} \approx P_{\mathrm{out}}$). Moreover, to simplify the final equation, the internal resistance of the battery is neglected as well ($V_{\mathrm{o}} \approx V_{\mathrm{batt}}$).

The goal of the following computations is to derive an equation to relate P_{out} and the switching frequency, valid only in the surroundings of the resonance frequency. In the FHA equivalent circuit, it is clearly visible that the converter operation is based on a series resonance (SRC). First of all, the input impedance seen by the

sinusoidal voltage generator is:

$$Z_{\text{in}}(f_{\text{sw}}) = j2\pi f_{\text{sw}} L_{\text{r}} + \frac{1}{j4\pi f_{\text{sw}} C} + r + R_{\text{eq}} \quad = \left(r + \frac{4}{\pi}\frac{V_{\text{batt}}}{I_{\text{L,1}}}\right) - j\frac{1 - \left(\frac{2\pi f_{\text{sw}}}{\omega_{\text{res,2}}}\right)^2}{4\pi f_{\text{sw}} C}\,. \tag{5.19}$$

Eq.5.19 shows that the input impedance expression can be easily decoupled into a resistive and reactive part. When working in the inductive region ($2\pi f_{\text{sw}} > \omega_{\text{res,2}}$), the imaginary part of Z_{in} becomes positive, highlighting the inductive nature of the resonance tank. By construction, the previously defined phase shift α coincides with $\underline{/Z_{\text{in}}}$.

To derive an equation for expressing the output power as function of the switching frequency, the following system of two equations can be defined:

$$\begin{cases} I_{\text{L,1}} = \dfrac{\frac{4}{\pi}\frac{V_{\text{in}}}{2}}{|Z_{\text{in}}|} = \dfrac{\frac{4}{\pi}\frac{V_{\text{in}}}{2}}{\sqrt{\left(\frac{4}{\pi}\frac{V_{\text{batt}}}{I_{\text{L,1}}} + r\right)^2 + \frac{1}{16 f_{\text{sw}}^2 C^2}\left(1 - \left(\frac{2\pi f_{\text{sw}}}{\omega_{\text{res,2}}}\right)^2\right)^2}} \\ I_{\text{L,1}} = \dfrac{\pi}{2}\dfrac{P_{\text{out}}}{V_{\text{batt}}} \end{cases}\,. \tag{5.20}$$

The first equation of Eq.5.20 simply exploits the KVL applied at the converter main loop. The second equation, instead, follows from the consideration that only the fundamental component of the primary voltage v_{p} is involved in the power transfer:

$$P_{\text{out}} \approx P_{\text{R}_{\text{eq}}} = \frac{1}{2} I_{\text{L,1}} \cdot \frac{4}{\pi} V_{\text{batt}}\,. \tag{5.21}$$

Combining the two equations of the system, the following implicit equation in P_{out} can be derived:

$$\left(\frac{8}{\pi^2}\frac{V_{\text{batt}}^2}{P_{\text{out}}} + r\right)^2 + \frac{1}{16\pi^2 f_{\text{sw}}^2 C^2}\left(1 - \left(\frac{2\pi f_{\text{sw}}}{\omega_{\text{res,2}}}\right)^2\right)^2 - \left(\frac{4}{\pi^2}\frac{V_{\text{in}} V_{\text{batt}}}{P_{\text{out}}}\right)^2 = 0\,. \tag{5.22}$$

The numerical solution of Eq.5.22 provides the desired static characteristic $P(f_{\text{sw}})$. The derivation of an alternative, analytic and explicit expression of P_{out} is beyond the scope of this work and could be subject of further improvements. The exploitation of more accurate models to describe the converter characteristic far from the resonance frequency is not investigated as well. In Chap.6, the validity of this model will be proved through *LTSpice XVII* simulations. The numerical solution of Eq.5.22 can be extracted through the *fsolve* function in *Matlab*.

5.4 Control

In this section, similarly to the previous considered converter, the control scheme of the half-bridge and rectifier MOSFETs is analysed. Even in this case, an ad-hoc control scheme is adopted to dynamically track soft-switching conditions for the converter MOSFETs.

5.4.1 Half-bridge MOSFETs control

This modified topology is designed to preserve the ZVS feature of the half-bridge MOSFETs. As mentioned, this converter can operate in the inductive or capacitive region according to the switching frequency. In order to achieve the desired discharge of the output capacitance of the MOSFET to be turned ON, the switching frequency must be larger than the resonance frequency. If this is true, the resonant tank behaves as an inductive load for the half-bridge, and i_L lags the fundamental component of v_{A}. In the capacitive region, instead, the zero crossing of current i_L leads the instant at which the half-bride MOSFET is turned OFF: as a result, the inductor current cannot correctly resonate with the output capacitances of the half-bridge MOSFETs.

The same principle of dynamic ZVS condition tracking can be adopted here. Despite the different i_L waveform, indeed, M_2 must still be turned ON while its body diode is conducting, during mode 2.2 (the same is valid for M_1). The control is based on the dynamic update of the deadtime dt, between M_2 turn OFF and M_1 turn ON (or viceversa). The comparison between soft and hard commutations is well described by the waveforms of Fig.4.13.

The larger inductance in general helps increasing the allowed time window (up to some hundreds of ns): however, as explained, the duration of mode 2.2 decreases as the switching frequency approaches the resonance frequency. The following conflict occurs: at the resonance frequency, the maximum power can in principle be extracted. However, the time window for ZVS reduces to zero, preventing ZVS turn ON. Notice that in the previously considered topology, instead, the allowed time window for ZVS increased proportionally with the output current (power). As a result, a larger power operation increases the possibility to achieve soft switching. Since the dynamic control scheme is the same as in the previous converter, it is not described again. It is to be noticed that, in the inductive region operation, the turn OFF always occurs in hard switching conditions.

5.4.2 Full-wave rectifier MOSFETs control

As in the previousy presented converter, the role of a MOSFET-based active rectifier is to replicate the behaviour of a conventional Graetz bridge with the goal of reducing the conduction losses. Differently from the previous case, however, the output capacitance keeps almost fixed the output voltage, while the L_r current is rectified. As a result, a cross-conduction of the entire rectifier would short-circuit the output capacitance and must be avoided.

While the commutation of diodes is unregulated, a proper control scheme must be designed to ensure the desired conduction scheme of the rectifier MOSFETs. To decrease switching losses, the desired feature would be to turn OFF the conducting MOSFETs when their current (momentarily equal to i_L) becomes null. If this condition occurs, the MOSFET is turned OFF at zero current (ZCS) and the $i_\mathrm{D} - v_\mathrm{DS}$ overlap during the commutations is drastically reduced.

A sensored solution can be proposed to dynamically track this ZCS condition. Let's consider, for instance, the ZCS tracking for M_4. The solution is based on the acquisition of the $v_{\mathrm{DS},4}$ polarity immediately before M_4 turn OFF. If the voltage is negative, it means that i_L has not reversed yet (the turn OFF would occur too early). Otherwise, a positive $v_{\mathrm{DS},4}$ indicates that the inductor current has already reversed, and then the MOSFET is turned OFF too late. From the physical implementation point of view, this solution is critical because based on the acquisition of low voltages (few mV or lower): the SNR may become unbearably small.

An alternative solution which does not require additional components is based on the exploitation of the half-bridge MOSFETs control. The principle is the same as in the previous converter: if the control scheme of the half-bridge MOSFETs is able to dynamically track the their ZVS condition, then these MOSFETs are turned ON approximately when the inductor current crosses zero. As a result, if the rectfier MOSFETs turn OFF is simultaneous with the half-bridge MOSFETs turn ON, ZCS can be achieved.

An additional benefit occurs if this *sensorless* control works correctly. When M_4 and M_6 are turned OFF, the positive inductor current, during the deadtime, charges their output capacitances and discharges the ones of the M_3 and M_5: as a result, these MOSFETs turn ON at zero voltage, independently from the deadtime. Fig.5.6 shows a detail of i_L, and the driving and output voltages of M_3 and M_4 during a rectifier deadtime. When M_4 is turned OFF with zero current, i_L is crossing the zero and becoming positive. As a consequence, L_r resonates with the output capacitances, and $v_{\mathrm{DS},3}$ decreases to zero while $v_{\mathrm{DS},4}$ increases to V_o. The

body diode of M_3 starts conducting the inductor current. After the deadtime, M_3 is turned ON at zero voltage. The presence of the output capacitor prevents the generation of large voltage spikes typical of the commutations in the previously analysed converter.

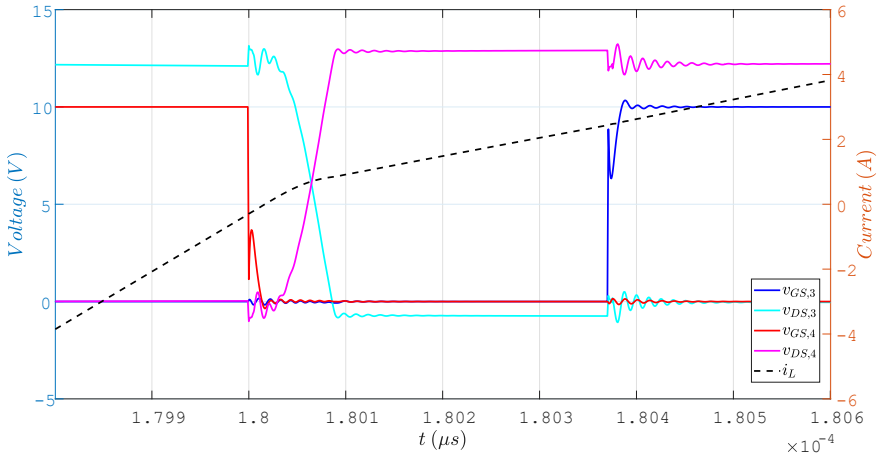


Figure 5.6: Detail of the ZCS turn OFF of M_4 and ZVS turn ON of M_3.

To simplify the design, for instance, the rectifier MOSFETs deadtime is assumed to be equal to dt. The resulting unitary switching functions for the six MOSFETs are reported in Fig.5.7.

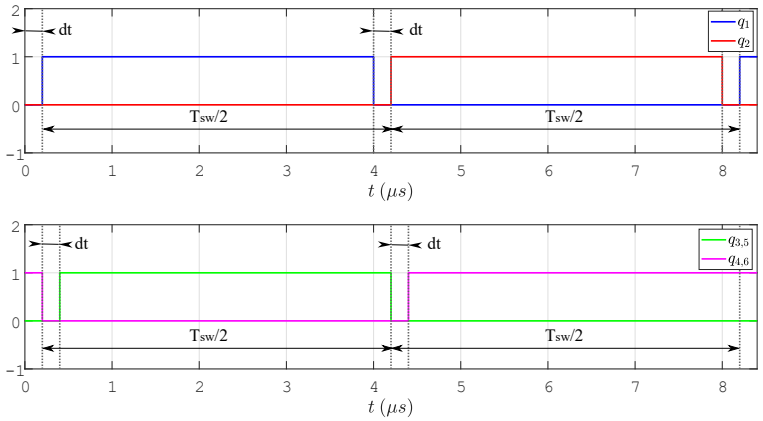


Figure 5.7: Unitary switching functions for the the half-bridge (above) and rectifier (below) MOSFETs.

Chapter 6

Simulation results

6.1 Validation of analytical models for static characteristics

6.1.1 Proposed topology

In this section, the analytical model derived in Chap.4 is validated through *Simulink-PSIM* simulation results. For clearness of notation, the converter described in Chap.4 will be denoted by *quasi-Resonant* converter (qR), to distinguish it from the one described in Chap.5. The converter, indeed, exhibits a partially resonant behaviour, limited to few of the operation modes, a typical feature of quasi-resonant converters.

The entire chapter presents simulation results referred to a preliminary, and not definitive, bill of materials, for multiple reasons:

- some of the simulations of conversion efficiency were carried out in *LTSpice XVII* environment[1]. As such, components whose SPICE models are already available on their manufacturers' websites were preferred;

- the current shortage of electronic components made it difficult, in some cases, to find the availability of simulated components in the main distributors' stocks, at the time of the definition of the final bill of materials. This is the case of MOSFETs and inductors, whose selection was particularly critical due to their stock shortage;

[1] `https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html`.

- apart from validating the mathematical models, an additional goal of simulations was to derive useful information to tune the final components selection, in the basis of their losses or switching response. The exploitation of preliminary components allowed to detail more precisely the specifications for the definitive components;
- this investigation is intended to proceed in a PhD path, where the missing aspects of the work will be completed.

For the purpose of simulations, the preliminary components selection involved the Silicon MOSFETs ($M_1 - M_6$), the resonant inductor L_r, the dividing capacitors $C_1 - C_2$, the output filter inductor L_o. An input capacitor is not needed if considering an ideal DC voltage source. The MOSFETs driving was performed by ideal, behavioral gate drivers. The complete design of each component of the converters will be presented further in this work, in a dedicated section. Tab.6.1 summarizes the selection of the components adopted for the simulations.

Half-bridge MOSFETs	$M_1 - M_2$	Infineon OptiMOS-T2 BSC076N04ND
Rectifier MOSFETs	$M_3 - M_6$	Infineon OptiMOS 5 BSZ070N08LS5
Resonant inductor (330 nH)	L_r	TDK Ferrite core, wire-wound HPL758040FR33MRD3P
Dividing capacitors	$C_1 - C_2$	KEMET MLCC C1825C105K5RAC
Output filter inductor	L_o	Coilcraft Ferrite core, wire-wound AGP4233-333ME

Table 6.1: Preliminary components selection adopted for the simulations.

The criteria for the preliminary design are here summarized. The specifications are derived considering a 100 W prototype, coherent with the 48 cells PV panel previously mentioned[2]:

- the half-bridge MOSFETs $M_1 - M_2$, when OFF, must withstand the open circuit voltage of the PV panel (around 30 V). The maximum conduction current is the load current when the battery voltage is minimum:

$$I_\mathrm{max} \approx \frac{100\,\mathrm{W}}{12\,\mathrm{V}} \approx 8.3\,\mathrm{A}\,.$$

  A 40 V, 20 A Silicon MOSFET was selected[3];

[2] `https://www.solarinnova.net/` (accessed on 09/09/22)

[3] `https://www.infineon.com/dgdl/Infineon-BSC076N04ND-DS-v02_00-EN.pdf?fileId=5546d462689a790c016905fc2e050ce9`.

- the secondary voltage waveform exhibits voltage spikes linked to the MOSFETs parasitics, which force to increase the voltage rating for the rectifier MOSFETs. Their current rating is the same as the half-bridge MOSFETs. A 80 V, 74 A Silicon MOSFET was chosen[4];
- for the dividing capacitors, the maximum voltage coincides with the input voltage, whereas the charging/discharging current is half the load current. A 50 V, 1 µF *X7R* MLCC was selected[5];
- the resonant inductor L_r was selected on the basis of its inductance value and its current ratings (the maximum current coincides with the load current). The inductance value was selected to be 330 nH, which ensures typical deadtimes around 100 ns for achieving ZVS. The selected ferrite inductor exhibits 25 A saturation current[6];
- finally, the load inductor was selected on the basis of its inductance value (further details in Chap.7) and maximum current. The chosen inductor exhibits 25.8 A saturation current for 30 % inductance drop [7].

In Chap.4, a full analytical procedure is presented to derive the explicit expression of the output power as function of the input voltage, battery voltage and switching frequency, in the case of a constant DC voltage source and ideal battery. The converter, however, would be designed as interface with a PV panel, whose voltage-current characteristic is strongly non-linear and drastically differs from an ideal voltage source. However, once the input power-voltage characteristic is known, a simple intersection with the source $P-V$ curve is needed to find the working point of the converter. This is the reason why the analysis of the static characteristic with constant DC voltage source is meaningful.

Output power as a function of switching frequency

As previously mentioned, the static characteristic of the proposed converter can be splitted into two operating regions, below the boundary frequency (in which

[4] `https://www.infineon.com/dgdl/Infineon-BSZ070N08LS5-DataSheet-v02_03-EN.pdf?fileId=5546d4625696ed760156e60d9bc9507d`.

[5] `https://www.mouser.it/datasheet/2/212/KEM_C1002_X7R_SMD-1102033.pdf`.

[6] `https://product.tdk.com/en/search/inductor/inductor/smd/info?part_no=HPL758040FR33MRD3P`.

[7] `https://www.coilcraft.com/en-us/products/power/shielded-inductors/high-current-flat-wire/agp-ver/agp4233/`.

the voltage at node X sweeps over the entire input voltage dynamic), and above (in which this does not happen). The $P_{\text{out}}(f_{\text{sw}})$ characteristic is linear in the low-frequency region (Eq.4.40), and is described by a relatively complex implicit-form expression in the second. The approximation performed on the third-order Eq.4.50 allows to derive an explicit expression for ΔV and, as a consequence, for I_{o} and P_{out}.

Fig.6.1 reports a comparison among the simulated static characteristic (red curve) and the results obtained with the complete 3^{rd} order mathematical model (blue dashed curve) and the approximated 2^{nd} order model (green dotted curve).

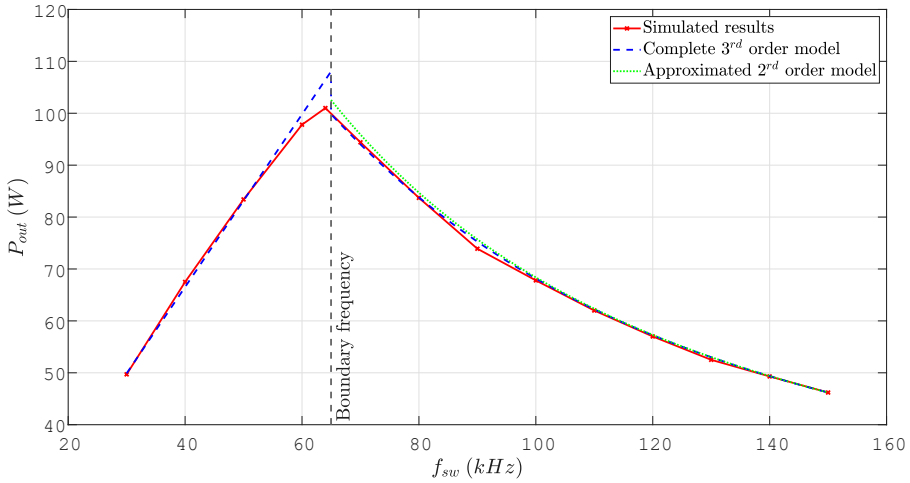


Figure 6.1: Comparison of simulated and analytical static characteristics in the proposed topology, with $L_{\text{r}} = 330\,\text{nH}$.

The simulations refer to a constant 28 V voltage source and a 13.2 V. The main parametres of the mathematical model are reported in Tab.4.1. What still remains to detail is the R_{ext} parametre. By performing an a-posteriori tuning of this parametre, what results is that the fitting is maximised for $R_{\text{ext}} = 32\,\text{m}\Omega$, approximately close to:

$$ESR_{\text{L}_\text{r}} + ESR_{\text{L}_\text{o}} + 0.5ESR_{\text{C}_{1,2}} + R_{\text{DS,ON}_{\text{M1}}} + 2R_{\text{DS,ON}_{\text{M3}}} \approx 39\,\text{m}\Omega\,. \tag{6.1}$$

From this consideration, it is possible to observe that R_{eq} takes into account, approximately, the sum of the equivalent resistances of the loop delimited by node A, node X and the battery side.

Fig.6.1 outlines that the complete mathematical model can well fit the static characteristic in the two regions. When the 2^{nd} order approximation is considered, the fitting is worsened for switching frequencies slightly above the boundary frequency,

as predicted in Chap.4. The model, moreover, cannot well-describe what happens in the neighborhood of the boundary frequency: this results in an abrupt discontinuity of the mathematical model that is not observed in the simulated characteristic.

It might be interesting to observe the parametric behaviour of the static characteristic by varying the input voltage. Fig.6.2 reports the behaviour of the static characteristic for 4 different input voltages, derived from the complete mathematical model. As visible, the increase of the input voltage allows to shift to higher frequencies the boundary between the two operating regions, and the maximum achievable power.

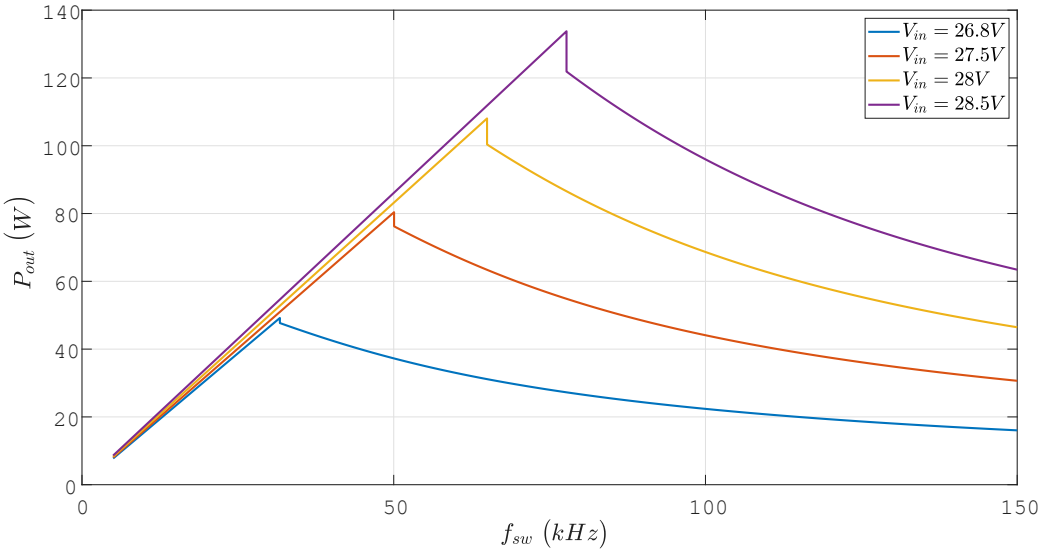


Figure 6.2: Representation of multiple static characteristics for different input DC voltages.

Output power as a function of input voltage

By fixing the switching frequency and battery voltage, one can extract the $P-V$ characteristic of the converter. As mentioned, this information is helpful when it is desirable to find the working point of the system when the power source is non-linear. According to the choice of switching frequency, the $P-V$ characteristic is defined in the first or second operating region. From Fig.6.2, it is clear that, for a certain f_{sw}, it is more likely that the converter will work in the second operating region for higher input voltages. Fig.6.3 shows the behaviour of the $P-V$ curve (simulated and analytical results) for the parametres specified in Tab.6.2. At

100 kHz and with the chosen design parametres, the converter always operates in the second operating region. The increasing behaviour can be expected from the equivalent resistive circuit reported in Fig.4.8, since the Thevenin-like open circuit voltage is $\frac{V_{\text{in}}}{2}$. From Eq.4.40, in the first operating region the $P_{\text{out}}(V_{\text{in}})$ behaviour is parabolic.

V_{batt}	13.2 V
f_{sw}	100 kHz

Table 6.2: Parametres adopted for the simulations of Fig.6.4

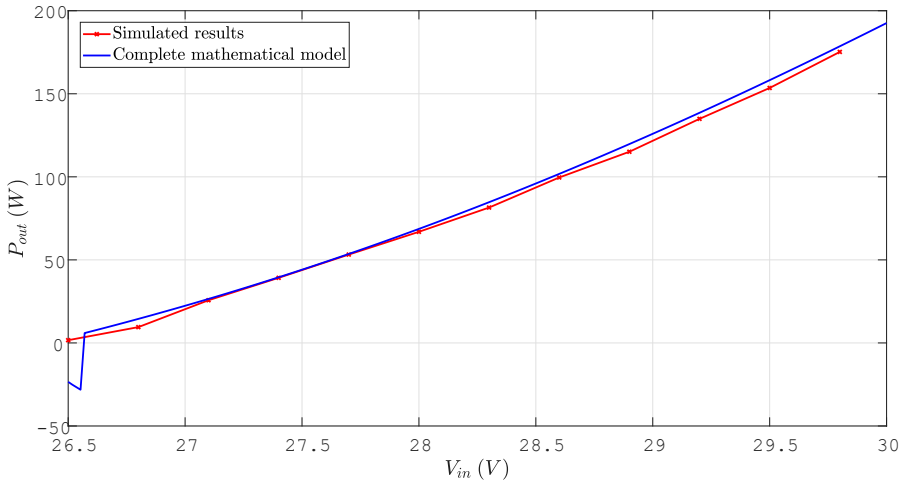


Figure 6.3: Comparison of simulated and analytical behaviour of $P_{\text{out}}(V_{\text{in}})$.

Output power as a function of the battery voltage

Since this converter is conceived to charge a 12 V battery, whose voltage varies according to the state of charge, it is meaningful to observe how the static characteristic changes during the charging process. In other terms, how the battery voltage increase influences the charging power. What is expected is to obtain, for a fixed input voltage and switching frequency, a behaviour dependent on the operating region:

- in the first operating region, the battery voltage does not appear in the output power expression;
- in the high-frequency operating region, instead, by looking at Fig.4.8, it is expected that the output power decreases as the battery voltage increases,

approximately with a hyperbolic behaviour. As a consequence, considering a realistic case in which the battery voltage increases with the state of charge during a charging process, the charging power automatically reduces by approaching the end of the charging, for the same switching frequency and input source. This phenomenon may help decreasing the risk of overcharging the output battery, with benefits on its life-cycle.

Fig.6.4 outlines the behaviour of $P_{\text{out}}(V_{\text{batt}})$ for the simulation parametres specified in Tab.6.3. With these parametres, the converter operates in the second region almost for the entire typical battery voltage sweep ($12.5\,\text{V} - 14\,\text{V}$). At very low battery voltages, at the beginning of the charging process (around $12.5\,\text{V}$), the two curves start diverging because the converter enters the first operating region: the mathematical model can no more well-describe the output power behaviour.

V_{in}	$28.5\,\text{V}$
f_{sw}	$100\,\text{kHz}$

Table 6.3: Parametres adopted for the simulation results of Fig.6.4.

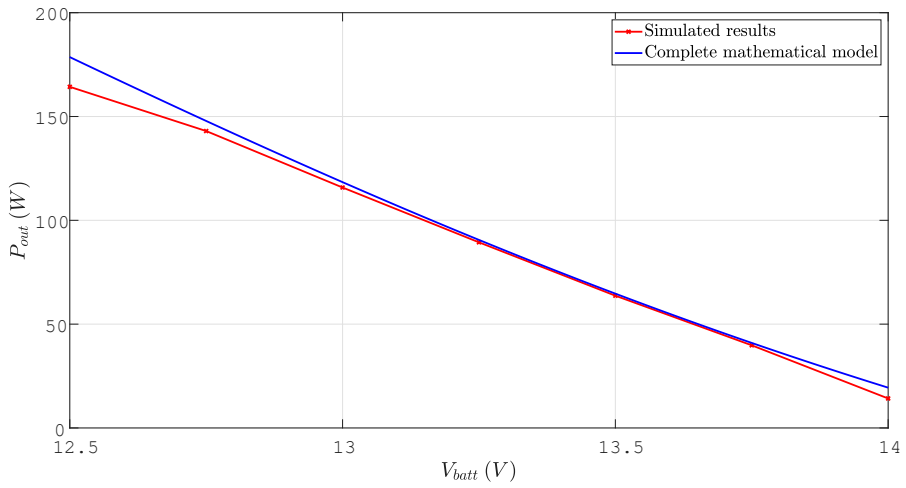


Figure 6.4: Comparison of simulated and analytical behaviour of $P_{\text{out}}(V_{\text{batt}})$.

The previous expectations are confirmed by Fig.6.5, showing multiple static characteristic graphs for 4 different battery voltages. The curves are derived from the complete mathematical model of the converter. When the converter operates in the first region, the static characteristic is linear and independent from the battery

voltage. An increasing output voltage causes the boundary frequency to decrease, at the same time lowering the $P_{\text{out}}(f_{\text{sw}})$ curve in the second operating region. After a certain battery voltage (slightly above $\frac{V_{\text{in}}}{2}$), the static characteristic becomes null because the input voltage cannot sustain the power transfer to the secondary side of the rectifier.

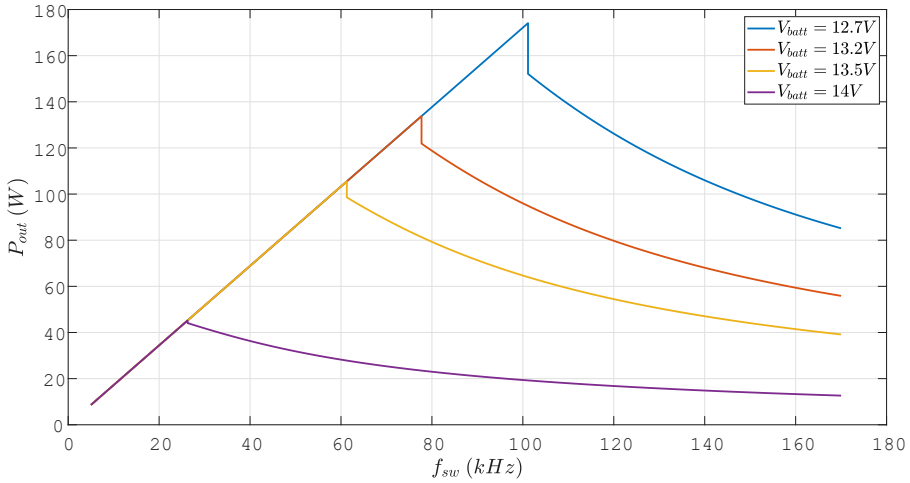


Figure 6.5: Representation of multiple static characteristics for different output battery voltages.

6.1.2 Larger L_{r} resonant topology

This section reports some simulation results of the static characteristic $P_{\text{out}}(f_{\text{sw}})$ for the second converter topology described in this work, endowed with larger L_{r} in the μH range and an output capacitive filter. For clearness of notation, this topology will from now on be referred to as *Series-Resonant* topology (*SR*), given the resonance nature of its working operation. The simulations of this section were carried out in *PSIM* environment[8] with an ideal, constant DC voltage source, and an ideal battery at the output. The objective is the comparison of simulation results with the predicted numerical results derived from the mathematical model presented in Chap.5.

As in the previous section, the *PSIM* simulations adopt models of preliminary components, summarized in Tab.6.20d. Actually, this converter was not physically implemented for this work. The simulations carried out with this preliminary BOM

[8] `https://powersimtech.com/products/psim/capabilities-applications/`.

represented the final point of analysis for this alternative topology. The components differ from the previous converter topology for the following reasons:

- the output capacitive filter prevents the generation of voltage spikes across the rectifier MOSFETs. As a consequence, the voltage rating of these MOSFETs can be chosen to be equal to the half-bridge ones. The same device is selected for both;
- the larger resonant inductor is chosen in the μH range and with 26 A saturation current for a 30% inductance drop, to consider the worst case scenario of maximum current [9]. This can be approximately derived considering a 100 W prototype charging a completely discharged battery ($V_{\text{batt}} \approx 12\,\text{V}$). The peak current corresponding to this condition can be derived as:

$$I_{\text{L}_{\text{peak}}}\Big|_{\text{max}} = \frac{\pi}{2}\frac{100\,\text{W}}{12\,\text{V}} \approx 13\,\text{A}\,; \tag{6.2}$$

- the dividing capacitors were selected with a lower value (680 nF instead of 1 µF) to shift the resonance frequency at around 100 kHz (92 kHz, more precisely). The goal of shifting ahead the resonance frequency is to decrease the filtering effort of the output capacitor. The dividing capacitors were selected to be low-ESR *X7R* MLCC with 50 V voltage rating[10];
- the output capacitive filter must filter out the switching noise from a rectified sine current waveform, in order to produce an almost-constant charging current. To sustanin the significant filtering effort required, this works considers the parallel of 3 identical 100 µF Tantalium electrolytic capacitor with low ESR (60 mΩ) [11]. The parallel connection allows to reduce the overall ESR and to split the current ripple on each individual capacitor, with the goal of reducing the temperature increase and the risks of failure.

Fig.6.6 reports the comparison of the simulated and modelled static characteristics for this converter topology, for given input and battery voltages specified in Tab.6.5. The static characteristic is analysed uniquely in the inductive region, for the control issues of working in the capacitive region mentioned in Chap.5.

[9] `https://www.coilcraft.com/en-us/products/power/shielded-inductors/ferrite-drum/mss-mos/mss1278t/mss1278t-222/`.

[10] `https://www.mouser.it/datasheet/2/212/KEM_C1012_X7R_OPENMODE_SMD-1103265.pdf`.

[11] `https://www.mouser.it/datasheet/2/212/1/KEM_T2076_T52X_530-1104134.pdf`.

Half-bridge MOSFETs	$M_1 - M_2$	Infineon OptiMOS-T2 BSC076N04ND
Rectifier MOSFETs	$M_3 - M_6$	Infineon OptiMOS-T2 BSC076N04ND
Resonant inductor (2.2 µH)	L_r	Coilcraft Ferrite-core, wire-wound MSS1278T-222
Dividing capacitors	$C_1 - C_2$	KEMET MLCC C1210F684K5RACTU
Output filter capacitor	C_o	Kemet Tantalium electrolytic capacitor T521X107M025ATE060

Table 6.4: Preliminary components selection adopted for the simulations of the SR topology.

V_{in}	28 V
V_{batt}	13.2 V

Table 6.5: Parametres adopted for the simulation results of Fig.6.6.

Some considerations must be done:

- as expected, the maximum power transfer is achieved at the resonance frequency. After this frequency, the simulated characteristic outlines a rapid power decrease (-50% at 105 kHz);
- it is important to remark that the simplified mathematical model is based on the FHA: as a consequence, it assumes that the power transfer is uniquely associated to the first harmonic of i_L. This approximation, as mentioned, is only valid in the neighborhood of the resonance frequency, where the inductor current is almost sinusoidal. Far from this tight region, the contributions of higher-order harmonics become more and more important to the output power. The mathematical model does not provide reliable results outside the neighborhood of the resonance frequency;
- the parametre r was included in the 1^{st} harmonic equivalent circuit of Fig.5.5 to take into account the resistive contributions otherwise neglected. By tuning r in the mathematical model, the fitting at the resonance frequency is maximised for $r = 77\,\text{m}\Omega$, which approximately corresponds to the sum of the resistive contributions in the loop defined by node A, node X and the battery side:

$$ESR_{L_r} + ESR_{\text{Battery}} + 0.5ESR_{C_{1,2}} + R_{DS,ON_{M1}} + 2R_{DS,ON_{M3}} \approx 72\,\text{m}\Omega\,. \quad (6.3)$$

Fig.6.7 reports multiple static characteristics for different input DC voltages (on the left) and fixed battery voltage (13.2 V), and for different battery voltages (on the right) with fixed input voltage (27.5 V). The curves are derived from the

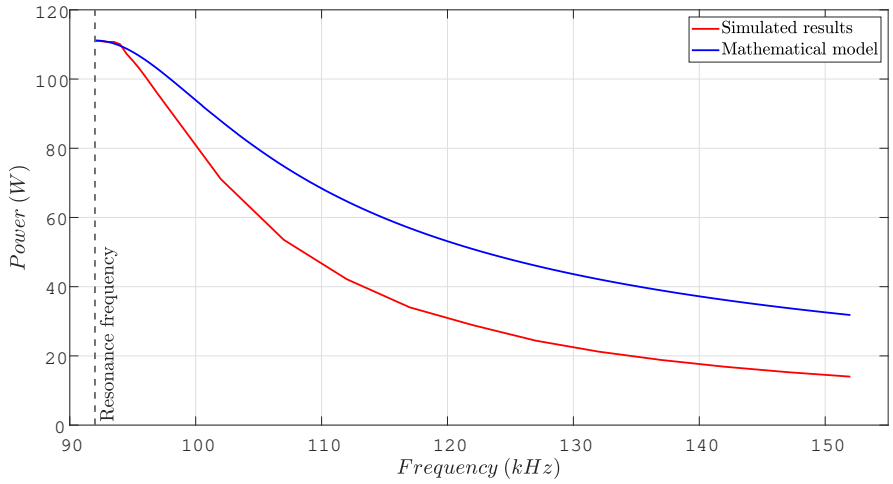


Figure 6.6: Comparison of simulated and analytical static characteristics in the SR topology.

FHA-based mathematical model of the converter, and then only consider a limited frequency range above the resonance frequency. As expected, an increase of the transferred power can be obtained by increasing the input voltage or decreasing the battery voltage. Also in this case, then, while the charging process goes on, the transferred power automatically reduces, decreasing the risk of overcharging the battery.

6.1.3 Static characteristics in presence of a PV source

In the previous parts, an analytical model to derive the static characteristic behaviour was developed for the two topologies, in case of an ideal DC voltage source. Due to the strong non-linearity of a PV panel characteristic, the derivation of static characteristics with PV sources would be complicated and not easily manageable with analytic expressions. In principle, the derivation of static characteristics could be performed numerically, by intersecting, for each operating frequency, the $P_{\text{in}} - V_{\text{in}}$ characteristic of the converters with the $P - V$ characteristic of the panel. Even this approach would lead to solve complex, non-linear equations.

This is the reason why, in this section, only simulated results are reported to display the non-linear behaviour of $P_{\text{out}}(f_{\text{sw}})$. The following results are derived in *PSIM/Simulink* environment, where the power converter is drawn in *PSIM*[12],

[12] `https://powersimtech.com/products/psim/capabilities-applications/`.

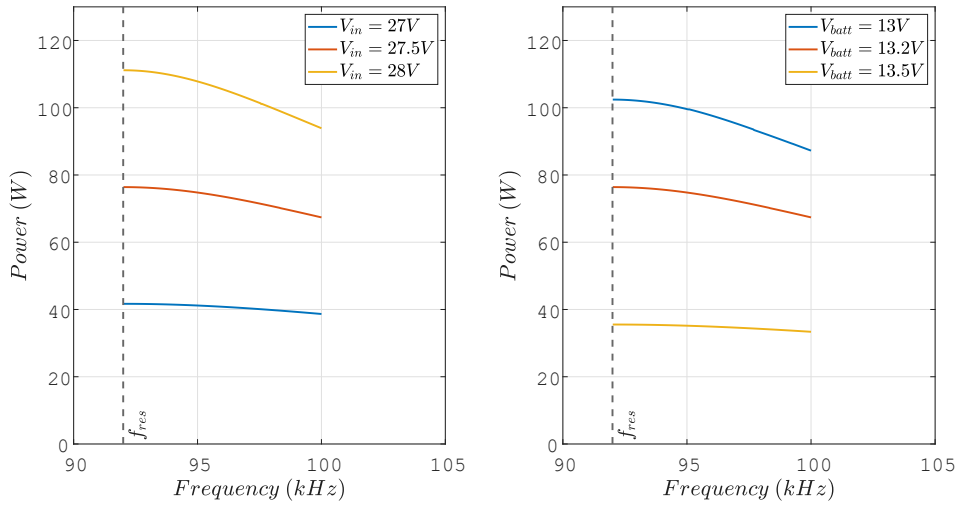
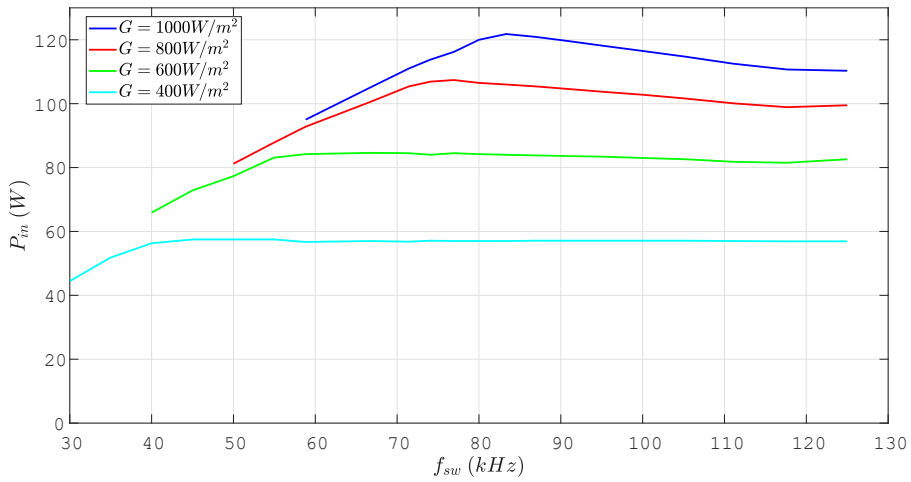


Figure 6.7: Static characteristic of the SR converter topology for multiple input voltages (on the left) and multiple battery voltages (on the right).

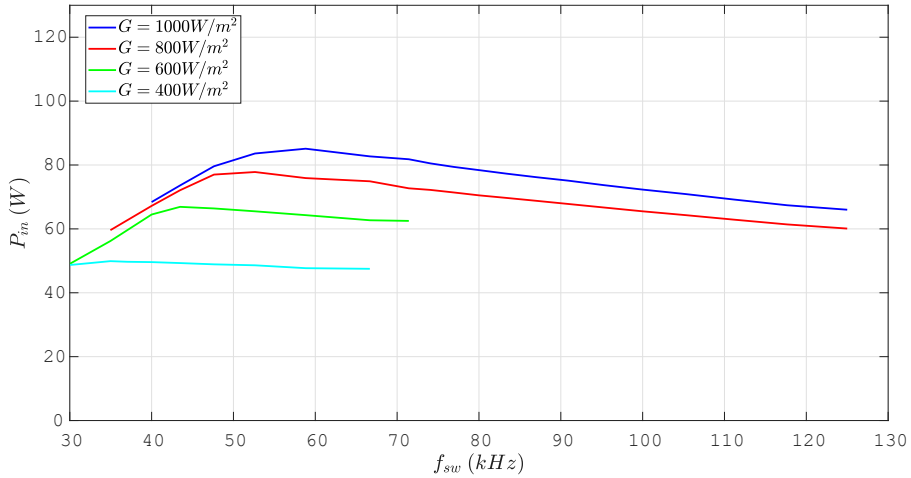
whereas the control algorithm is handled by *Simulink*[13]. The two environments can be coupled through the *SimCoupler* block, allowing bidirectional data transfer between the two domains of the converters. All the simulations are performed under the designed dynamic ZVS tracking control (more details on the implementation will be given later in this chapter). The PV model adopted for the simulations is a *Solar module (Physical model)* available on *PSIM*, where the model parametres are the ones derived in Chap.2.3.3.

Fig.6.8 shows the static characteristics of the qR topology at four different irradiance conditions, for two different battery voltages (12 V and 13.2 V, respectively). The results show that the static characteristics still behave differently according to the two working regions, as with DC sources. For each irradiance condition, the maximum power is achieved at the boundary frequency, which decreases as the irradiance decreases. This behaviour can be justified by recalling that the characteristic of a PV panel rigidly translates down as the irradiance decreases (at fixed temperature operation). As a result, for the same frequency, the PV panel would be forced to work at approximately the same voltage level, but with lower current. The working current in this new condition would not be enough to make the voltage at node X sweeping from 0 V to V_{in}.

[13] `https://it.mathworks.com/products/simulink.html`.



(a) $V_{\text{batt}} = 12\,\text{V}$.

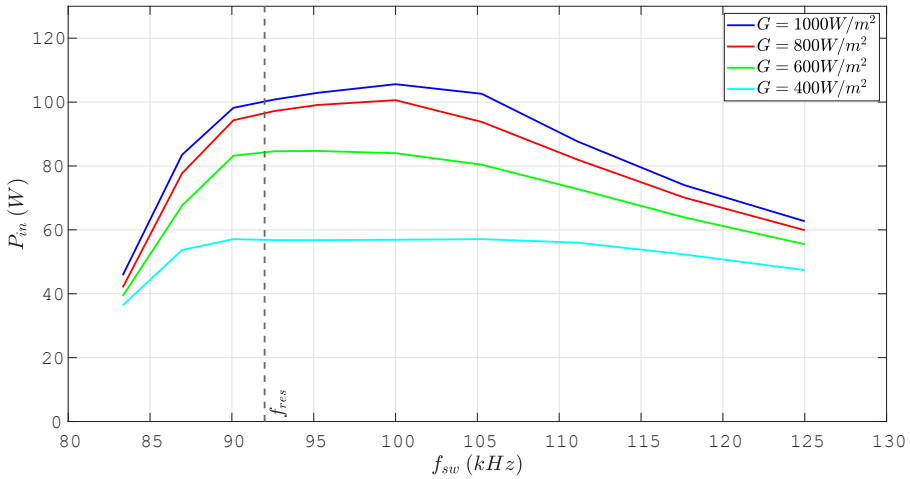


(b) $V_{\text{batt}} = 13.2\,\text{V}$.

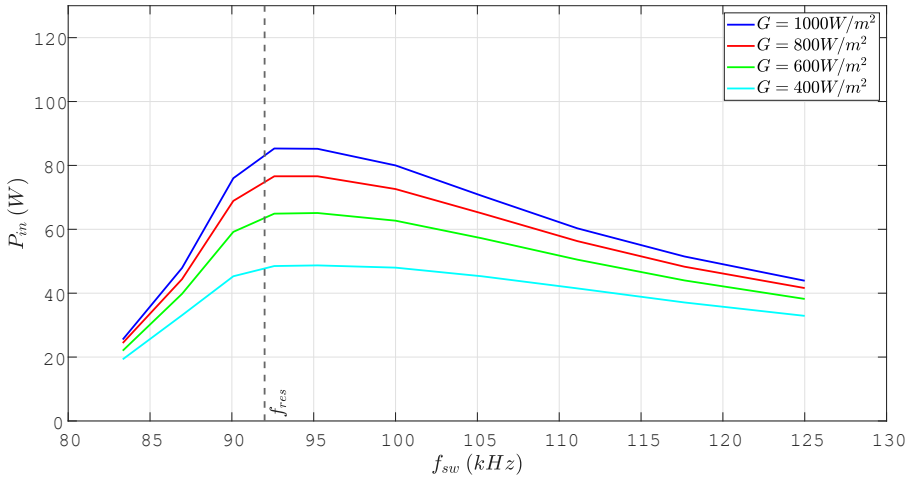
Figure 6.8: Simulated static characteristics for various irradiance conditions at two different battery voltages, qR topology.

Fig.6.9 reports the results of the same simulations, but for the SR topology analysed in this work. These results confirm the expectation that the resonance frequency, dividing the capacitive and inductive working regions, is the frequency at which the maximum power can be extracted. More precisely, this is not exactly true when considering large power operations (around 100 W). As the red and blue curves of Fig.6.9a outline, indeed, the maximum power is achieved at slightly larger frequencies (100 kHz). This phenomenon can be explained by recalling that the

ZVS tracking control works only if the L_r current is sufficiently large to effectively discharge the output capacitances of the half-bridge MOSFETs: at exactly the resonance frequency, this condition is no more satisfied and the MOSFETs turn ON in hard switching, resulting in larger switching losses and an overall transferred power decrease. What can also be highlighted is that, as expected, the power drastically decreases in the capacitive region, due to the unfit control.



(a) $V_{\text{batt}} = 12\,\text{V}$.



(b) $V_{\text{batt}} = 13.2\,\text{V}$.

Figure 6.9: Simulated static characteristics for various irradiance conditions at two different battery voltages, SR topology.

A general consideration valid for both the converters is that the curved shape of the $I-V$ characteristic of the PV panel results in an enlargement of the graphs. In other terms, the output power is in general less sensitive to frequency variations as it is in the constant DC source case. As a consequence, it might get difficult to the control algorithm to track the absolute maximum power point, especially for low irradiance conditions.

Another consideration is that the sign of the power gradient $\frac{\partial P_{\text{out}}}{\partial f_{\text{sw}}}$ in the SR topology is almost independent from the irradiance, beside the exceptions for high power operation. This is not true for the qR topology, where the boundary frequency depends on the irradiance. However, by adopting a simple $P\&O$ scheme, this behaviour is irrelevant for the effectiveness of the control to achieve the maximum power operation.

6.2 Simulation results in standardized efficiency tests

After deriving a proper mathematical model to predict the static characteristic of the two analysed converters, the efficiency under various operating conditions was tested in this work. The results are reported in this section for both the topologies, in order to compare their performances. All the simulations of this section were performed in *LTSpice XVII* environment under the following conditions:

- the main components of the power converter (MOSFETs, dividing and filter capacitors, resonant and filter inductors) are included as SPICE models downloaded from the manufacturers' websites. The adoption of models referred to real components, as explained, allowed to better tune the choice of the definitive BOM for the physical implementation;

- the driving approach, on the other hand, is purely behavioral. *LTSpice XVII* exhibits some limitations in terms of complex control scheme implementations. This is the reason why the implementation of a MPPT scheme and of a ZVS/ZCS tracking scheme was realized in *PSIM/Simulink* environment: *LTSpice XVII* was exploited to test the efficiency of the two converters under fixed switching frequency and timing parametres (deadtimes);

- the battery was always assumed to be an ideal DC voltage source with a small 30 mΩ series resistance. The influence of the battery state of charge (SOC) was considered through simulations at different, increasing battery voltages;

- for the power source, a single-diode model was considered for the PV panel mentioned in Chap.2.3.3 (SDM parametres in Tab.2.1).

- the efficiency measurement was performed by averaging the input and output powers (evaluated at the PV model terminals and battery terminals, respectively) over 10 switching cycles, at steady-state operation, after the extinction of the start-up transient. The *.meas* directive combined with the *AVG* macro was exploited. The dissipated power values presented at the end of this section were derived with the same averaging approach.

The reported results refer to standardized testing conditions defined in EN 50530:2010 ("Overall efficiency of grid connected photovoltaic inverters", [41]) and in IEC 62509:2011 ("Battery charge controllers for photovoltaic systems - Performance and functioning", [42]).

Specifically, the first standard provides definitions and a procedure for the experimental measurement of the efficiency of the MPPT of inverters. Actually, the standard refers to microinverters fed by PV panels connected to the low voltage grid. The MPPT capability is a necessary feature for grid-connected microinverters, to allow continuous operation of the PV panel at its rated power. This is the reason why the standard provides a mathematical procedure to extract the so-called static and dynamic MPPT efficiencies. Actually, in this work, only the conversion efficiency is tested under different irradiance conditions specified further in this section.

The second standard, instead, applies to low-voltage battery charge controllers and defines "functional and performance requirements". The standard details the experimental setup and procedure to test the performances of charge controllers: battery lifetime protection, energy performance, fail safety. The simulations only allow to test the performances in terms of charging efficiency.

6.2.1 Euro efficiency

The simulation results reported in this sections refer to standard irradiance conditions specified in [41]. Since a PV module, as described, exhibits a strong dependence of its electrical characteristic to the environmental condition, the so-called *EURO efficiency* and *CEC efficiency* are defined in the standard to provide a unique figure of merit of the converter performances at realistic operating conditions. The two quantities are defined as weighted averages of conversion efficiencies evaluated at different partial irradiance scenarios reproducing typical operating conditions characterizing a certain geographical area. The first one, specifically, tries to reproduce middle-Europe countries climate, whereas the second one was proposed by the California Energy Commission and applies to South-Western USA states. The two definitions differ in the weighting factors, modelling the probability of a PV panel to work in a specific irradiance condition within a day. In this work,

the *EURO efficiency* definition is adopted.

The *EURO efficiency* is defined as follows:

$$\eta_{\mathrm{EURO}} = a_1\eta_{\mathrm{MPP},1} + a_2\eta_{\mathrm{MPP},2} + a_3\eta_{\mathrm{MPP},3} + a_4\eta_{\mathrm{MPP},4} + a_5\eta_{\mathrm{MPP},5} + a_6\eta_{\mathrm{MPP},6}\,, \quad (6.4)$$

where the a_i and $\eta_{\mathrm{MPP,i}}$ parametres represent the weighting factors and the conversion efficiencies at different power levels, respectively, as defined in Tab.6.6.

Index i	Weighting factor a_i	Power level MPP, i
1	0.03	$5\%P_{\mathrm{rated}}$
2	0.06	$10\%P_{\mathrm{rated}}$
3	0.13	$20\%P_{\mathrm{rated}}$
4	0.1	$30\%P_{\mathrm{rated}}$
5	0.48	$50\%P_{\mathrm{rated}}$
6	0.2	$100\%P_{\mathrm{rated}}$

Table 6.6: Parametres of the *EURO efficiency* definition.

Given the 140 W rated power of the PV panel, the two converters were tested at the operating powers defined in Tab.6.6. In every simulation, the operating power was tuned from a proper selection of the irradiance (to select the IV curve of the PV panel corresponding to the desired MPP power) and of the switching frequency (to set the working point at the MPP of that curve). For instance, for the first conversion efficiency, an irradiance value was selected to provide a PV characteristic with $MPP = 5\%P_{\mathrm{rated}}$, and the switching frequency was tuned until the working point coincided with the MPP.

The battery voltage was fixed at 12 V for all the simulations. The deadtimes for the half-bridge and rectifier MOSFETs were manually tuned to provide always ZVS and ZCS, respectively, in the two converters. In this way, the operating conditions are analogous. Actually, due to the previously mentioned input voltage constraints, none of the two converters manage to work at the rated power, 140 W. The 100% rated power condition was then replaced by the maximum achievable transferred power condition of the converters (around 117 W and 101 W, respectively). For all the other operating power conditions, instead, a switching frequency exists for which the converters can transfer the desired power.

Clearly, the unique value of the *EURO efficiency* does not provide a complete and satisfactory indication of the efficiency of the converters: this is why the results at each working condition are here reported and commented. The obtained results for the two topologies are summarized in Tab.6.7 and plotted in Fig.6.10. As the

results show, the qR topology allows to reach larger maximum transferred power, thanks to the lower resonant inductance value. Both the converters start exhibiting steep decreases of efficiency below 20% of the rated power: the decreasing efficiency is probably due to losses contributions that do not scale down linearly with the output power, such as the switching losses of half-bridge MOSFETs when they are turned OFF. At such low powers, moreover, sometimes the ZVS of half-bridge MOSFETs cannot be achieved, since the current through the resonant inductor L_r may not be sufficient to charge/discharge their output capacitances. At larger powers, instead, the efficiency decrease, mainly due to increasing conduction losses, is more important in the SR topology, due to the larger peak and RMS currents in the circuit, for the same output power. At 50% of the maximum power, which represents the most significant contribution in the EURO efficiency definition, the qR converter exhibits a peak, contributing to the larger EURO efficiency value.

Power level MPP, i	$\eta_{\mathrm{MPP,i}}$, qR topology	$\eta_{\mathrm{MPP,i}}$, SR topology
$5\%P_{\mathrm{rated}}$	93.0%	95.4%
$10\%P_{\mathrm{rated}}$	96.2%	97.1%
$20\%P_{\mathrm{rated}}$	97.8%	98.8%
$30\%P_{\mathrm{rated}}$	98.0%	98.3%
$50\%P_{\mathrm{rated}}$	98.5%	97.6%
$100\%P_{\mathrm{rated}}$	97.4% (at 117 W)	95.4% (at 101 W)

Table 6.7: Tabular comparison of conversion efficiencies for the two converter topologies at partial operating powers.

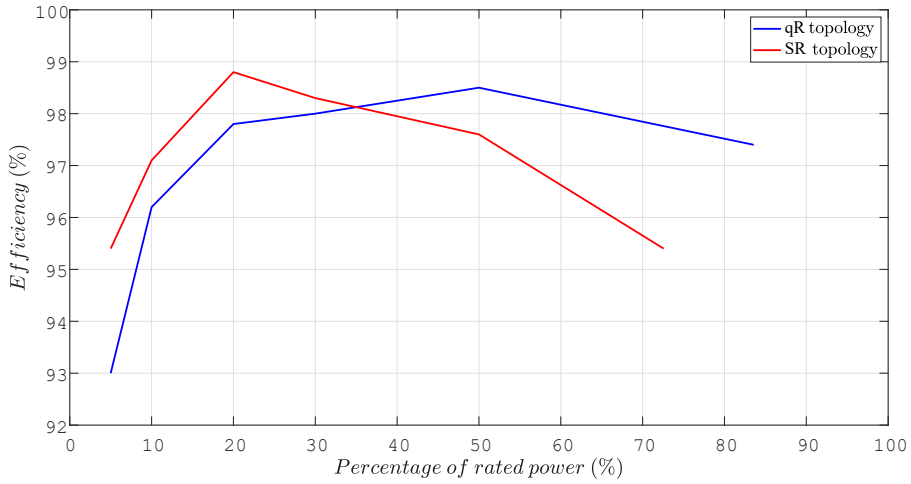


Figure 6.10: Comparison of conversion efficiencies for the two converter topologies at partial operating powers.

The computed *EURO efficiency* in the two cases results, respectively, in:

$$\eta_{\text{EURO}}|_{\text{qR}} \approx 97.84\%$$
$$\eta_{\text{EURO}}|_{\text{SR}} \approx 97.29\%$$

6.2.2 Charging efficiency

The second mentioned standard, IEC 62509:2011, concerns the definition of the setup and procedure to measure the performances of a battery charge controller. The standard specifically addresses 6-cell lead-acid batteries. Among the other recommendations, the charging efficiency measurement procedure is defined. The standard requires to measure the efficiency of the converter at various charging current conditions, at steps of 10% up to the maximum charging current. The measurement must be performed with fixed battery voltage at 13.2 V (2.2 V for each cell) and 25 °C ambient temperature.

The standard does not provide further information on the irradiance condition, so the STC was considered for the simulations. Once the maximum charging current at 1,000 W/m^2 irradiance was detected, the switching frequency was tuned to make the converter operate at the required working conditions. The results are shown in Fig.6.11. As it can be noted, the behaviour of the two curves is similar, with lower efficiencies at lower currents and almost the same maximum efficiency

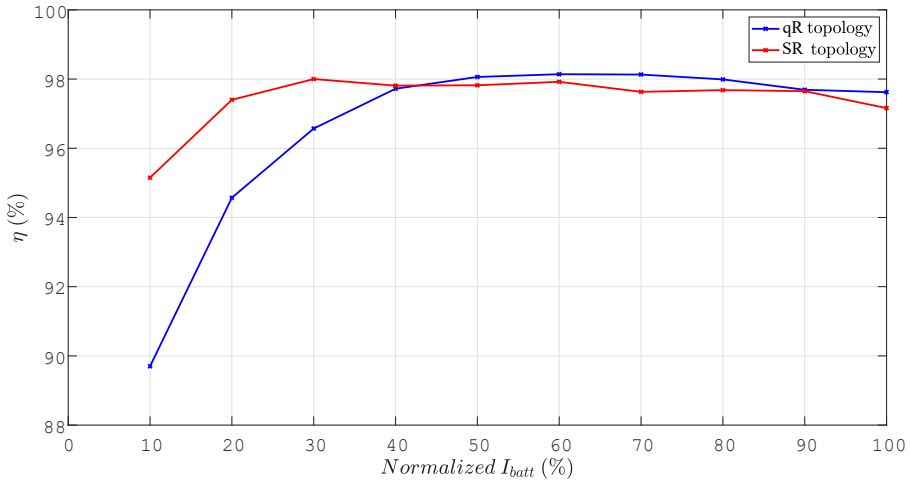


Figure 6.11: Conversion efficiency of the two analysed topologies at different charging currents.

(around 98%). The efficiency decrease at very low currents can be easily explained by two reasons:

1. in order to work at such low power levels, the switching frequency must be increased up to around 500 kHz. At these frequencies, the gate and inductor losses start becoming significant over the overall transferred power. Obviously, the same power level could be obtained by working at lower irradiance levels, and with a lower frequency;

2. at such low frequencies, there is no condition for the half bridge ZVS. Independently from the choice of deadtime, the inductor L_r current is always too low to discharge the output capacitances of the MOSFETs. For the same reason, the ZCS condition for the rectifier MOSFETs can't be achieved. In the qR topology case, the absence of ZCS generates voltage spikes that increase significantly the switching power losses: this is the reason why the efficiency decrease is larger when compared to the other topology.

6.2.3 Efficiency at various battery voltages

A third possible comparison in terms of efficiency can be made for different battery voltages. These simulations would intend to predict the efficiency behaviour during the charging process, when the battery SOC (and, consequently, its voltage) gradually increases. Fig.6.12 shows the comparison of the two converters efficiencies as function of the battery voltage, from 10.5 V to 14 V. Actually, voltages below

12 V are unrealistic for a battery subjected to a charging process, but these simulation results outline what would be the expected efficiency for large power. The simulations are performed at fixed STC conditions and at the switching frequency maximising the power transfer.

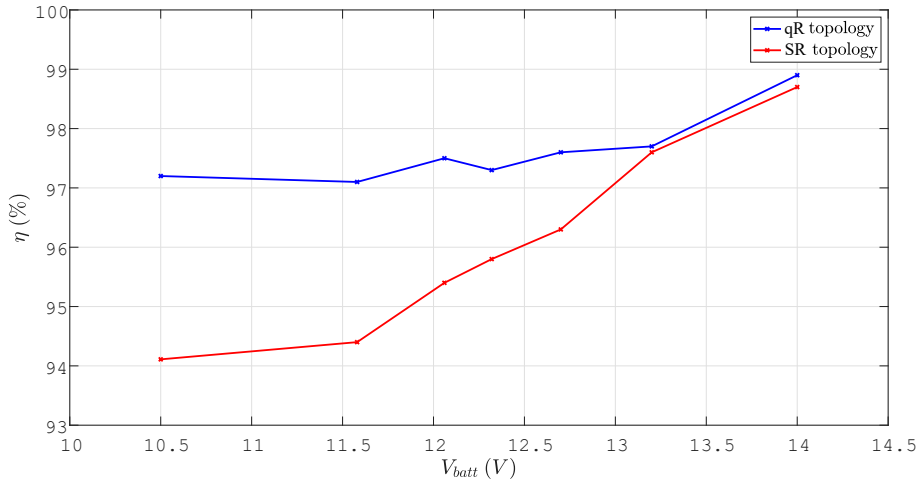


Figure 6.12: Conversion efficiency of the two analysed topologies for different battery voltages.

The plots show that at very low battery voltages (high operating powers, above 100 W), the efficiency curve for the SR topology start to decrease significantly compared to the qR one: this is linked to the fact that, for the same operating power, the RMS value of the L_r inductor current is larger. This consideration comes from the analysis of the i_L and i_o current waveforms and results in:

$$\frac{I_{\mathrm{L,RMS}}|_{1^{\mathrm{st}}}}{I_{\mathrm{L,RMS}}|_{2^{\mathrm{nd}}}} \approx \frac{\pi}{2\sqrt{2}} \approx 1.11\,. \tag{6.5}$$

That inductor, as will be explained in the last section of this chapter, represents one of the most critical components from the losses point of view. The larger inductor in the SR topology exhibits a larger ESR and this, combined with the larger RMS current, results in a larger power dissipation. Independently from the converter topology, the efficiency decreases for higher power, given the larger contribution of the conduction losses for larger operating powers.

6.3 Control implementation and validation

In this section, the control scheme adopted in the simulations, which represents the basis for the physical implementation on a FPGA, is illustrated in its principles and implementation in *Matlab/Simulink* environment. As mentioned, the MOSFETs gate driving is based on an innovative tracking control whose goal is to turn ON the half-bridge MOSFETs at zero voltage and turn OFF the rectifier MOSFETs at zero current. Given the different resonant current waveform in the two converters, the gating scheme for the rectifier transistors slightly differs between the two topologies.

The general controller block diagram including both the MPPT control for the maximization of the power transfer, and the driving scheme for the adaptive soft-switching tracking, is shown in Fig.6.13. The MPPT scheme, realized by a simple P&O controller, takes as input the voltage and current of the PV source, to reconstruct the transferred power at the time instant k. This controller acts on the switching frequency to adjust the extracted power according to the MPPT algorithm. The *ZVS/ZCS tracking* controller, on the basis of the $v_{\mathrm{DS},2}$ acquisition at the instant k, generates the control signals $q_{1,6}$ for the gates drivers. Actually, the cascaded controllers work on a different time basis: the inner one, adjusting the gating signals scheme, acts at every switching cycle. The MPPT controller, on the other hand, measures the input power and adjusts the switching frequency after a certain number of clock cycle, in order to measure the power update after the extinction of the transient caused by the previous frequency adjustment.

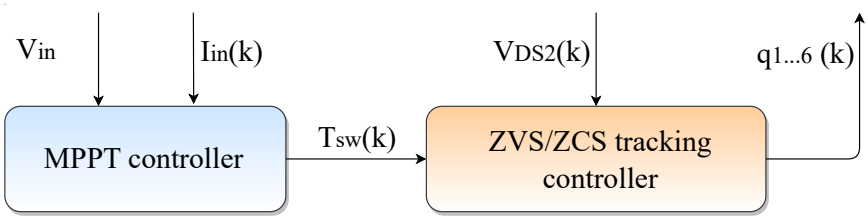


Figure 6.13: Simplified block diagram of the complete control.

6.3.1 Sensitivity of switching losses to deadtime variations

Before moving to the description of the ZVS/ZCS tracking control implementation, it may be interesting to justify its adoption by analysing how much the MOSFETs (both the half-bridge's and rectifier's) losses vary when the soft switching condition is not achieved. The analysis of the sensitivity of MOSFETs losses to deadtime variations can be helpful to establish the maximum delay specifications of the gate drivers. In the following plots, the sensitivity to MOSFETs losses is defined as

follows:

$$S = \frac{P_{\mathrm{diss,M}}(dt) - P_{\mathrm{diss,M}}(dt_{\mathrm{opt}})}{P_{\mathrm{diss,M}}(dt_{\mathrm{opt}})} \cdot 100\,, \tag{6.6}$$

where dt_{opt} is the optimum deadtime for which ZVS is achieved. Fig.6.14 reports the sensitivity analysed for three different working operations: $G = 1{,}000\,\mathrm{W/m^2}/V_{\mathrm{batt}} = 12\,\mathrm{V}$, $G = 1{,}000\,\mathrm{W/m^2}/V_{\mathrm{batt}} = 14\,\mathrm{V}$, $G = 50\,\mathrm{W/m^2}/V_{\mathrm{batt}} = 12\,\mathrm{V}$. For each operating condition, the switching frequency is selected to achieve the maximum power. After identifying the optimum dt, this parametre is increased by 10 ns each time and the average MOSFETs losses computed. In the specific case of the qR topology, due to the relation between the ZVS control (for half-bridge MOSFETs) and the ZCS control (for rectifier MOSFETs) highlighted in Chap.4.5.2, the sensitivity of rectifier MOSFETs losses is computed for 20 ns steps of dt.

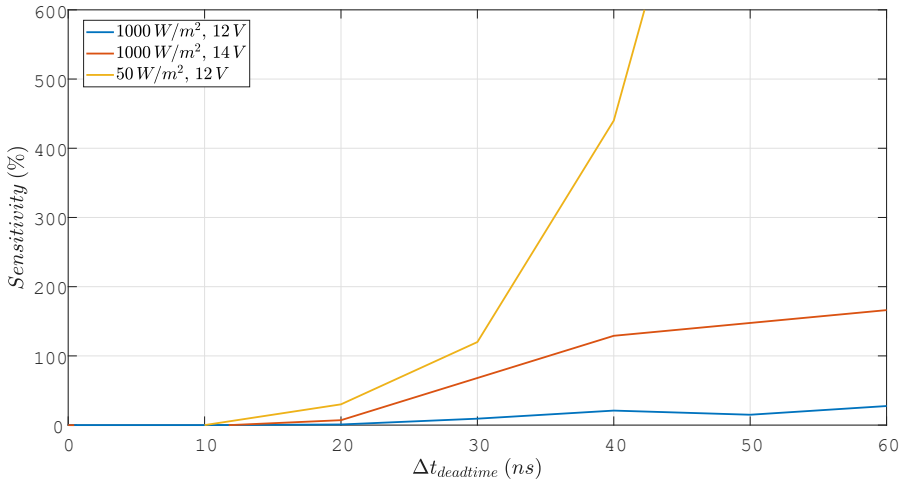
What immediately emerges from Fig.6.14 is that, for the same $\Delta(dt)$, the rectifier MOSFETs experience a larger losses increase.

In relative terms, the lower power operating conditions cause a larger sensitivity of MOSFETs losses to deadtime variations. In absolute values, on the other hand, the losses at the $G = 1{,}000\,\mathrm{W/m^2}$-$V_{\mathrm{batt}} = 12\,\mathrm{V}$ operation are ten times larger than in the $G = 1{,}000\,\mathrm{W/m^2}$-$V_{\mathrm{batt}} = 14\,\mathrm{V}$ one, and around 30 times than in $G = 50\,\mathrm{W/m^2}$-$V_{\mathrm{batt}} = 12\,\mathrm{V}$. By considering the maximum power operation as the reference condition, it is possible to extract that the losses for the rectifier MOSFETs nearly duplicate for $\Delta(dt) \approx 45$ ns. As a consequence, the sum of gate driver and switching delays should be kept below few tens of ns to achieve high efficiency performances.

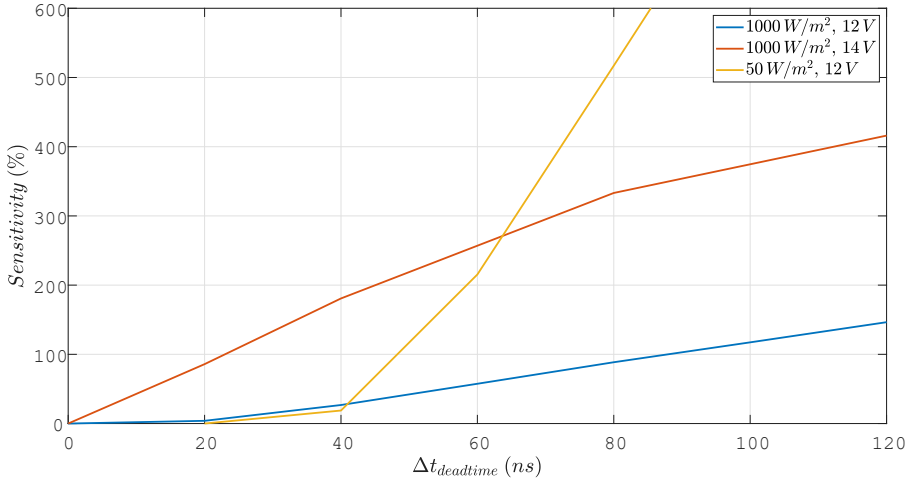
Fig.6.15 reports the sensitivity of the half-bridge MOSFETs in the SR topology.

Two differences can be immediately highlighted with the previous plots. First of all, the absence of the $G = 50\,\mathrm{W/m^2}$-$V_{\mathrm{batt}} = 12\,\mathrm{V}$ working condition, linked to the fact that, at such low power operation, there is no possibility to achieve ZVS for any switching frequency selection. As a consequence, it is impossible to identify an optimum operation.

Secondly, it is not trivial to compare the rectifier MOSFETs losses. Assuming to consider $\Delta(dt)$ as the deadtime gap to the ZCS condition, it was outlined in simulations that a change in dt causes sensible output power variations which make the comparison less meaningful. Specifically, a positive $\Delta(dt)$ causes an overall power increase, with consequent increase in the conduction losses, for which it is not trivial to decouple the influence of the hard switching. Figs.6.16a and 6.16b shows a switching period waveforms of the resonant current and output current for 5 different dt selections ranging from 0 ns (ZCS) to 200 ns. The simulations refer to a $G = 1{,}000\,\mathrm{W/m^2}/V_{\mathrm{batt}} = 13.2\,\mathrm{V}$ operation. What emerges is that the higher order harmonics become more and more important as the $\Delta(dt)$ increases,



(a) Half-bridge MOSFETs sensitivity.



(b) Rectifier MOSFETs sensitivity.

Figure 6.14: Sensitivity of half-bridge and rectifier MOSFETs losses towards deadtime variations (qR topology).

distorting the sinusoidal-like i_L. By moving from 0 ns to 200 ns cases, the output power increases from around 71.3 W to around 89.6 W ($\approx 25\%$ power increase). In the qR topology case, instead, the deadtime variations cause sensibly lower power variations.

The possibility to regulate the output power by exploiting deadtime variations is not explored in this work and could be subject of further analysis. However, the main drawbacks of this strategy is the intrinsic loss of the ZCS benefit, and the

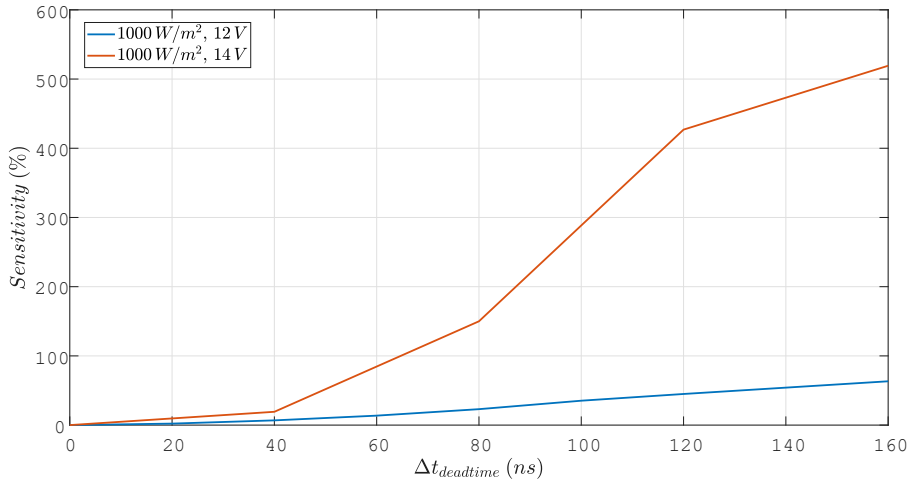


Figure 6.15: Sensitivity of half-bridge MOSFETs losses to *dt* variations.

larger harmonic content of the charging current, for the same filter capacitor.

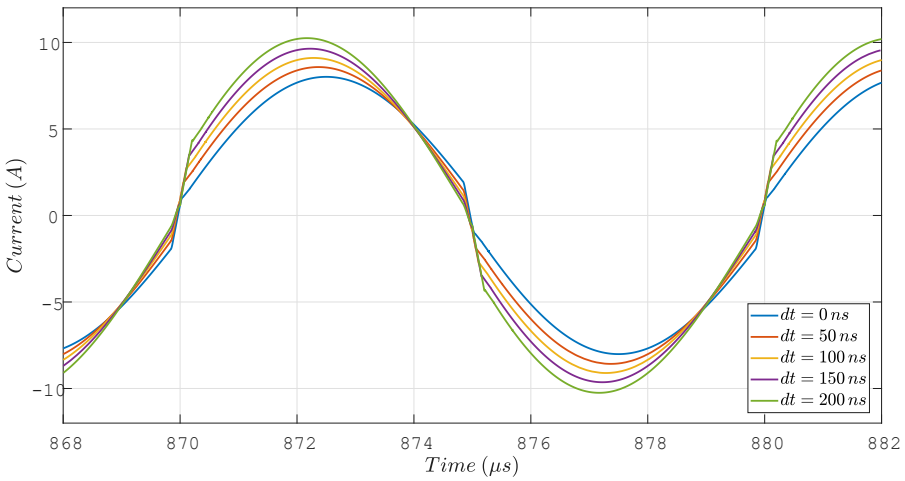
6.3.2 ZVS tracking control implementation

The *Stateflow* block on *Matlab/Simulink* provides an intuitive tool to design algorithmic state machines. The control section of the Power Processing Unit (PPU) was entirely designed in this environment, and linked to the power section in *PSIM* through the *SimCoupler* block. As illustrated in Fig.6.13, the inner controller takes the switching period as parameter and the measured drain-source voltage of M_2 as input, to determine whether the actual deadtime is enough to ensure ZVS of the half-bridge MOSFETs or not.

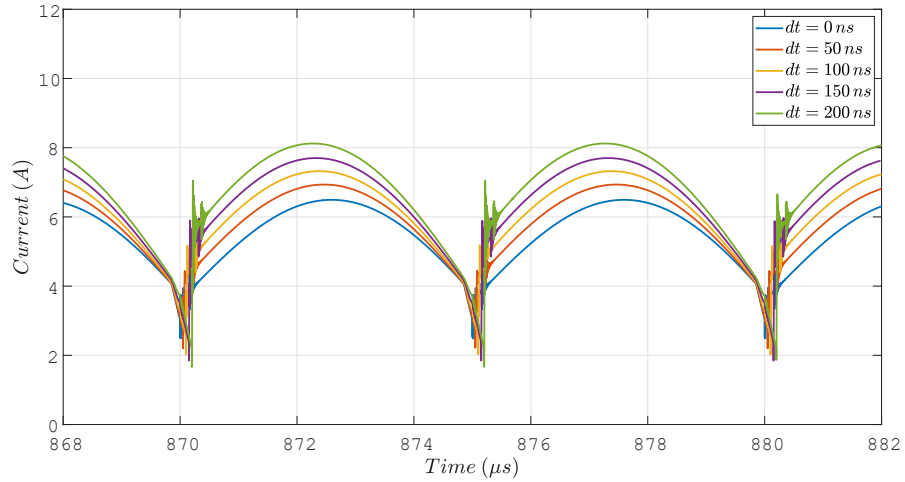
Actually, the role this controller has already been discussed in Chaps.4.5.2 and 5.4.2. The control schemes for the two converters can be easily converted into Moore state machines, where the state transition is not regulated by specific input variables, but is dictated by a timing scheme. The switching period calculated by the MPPT controller is used to detail the duration of the states. The other input variable, $v_{\mathrm{DS},2}(k)$, is exploited for the update of the half-bridge deadtime to achieve ZVS turn ON. The rectifier driving scheme, as previously described, relies on the half-bridge control to achieve ZCS turn OFF.

Fig.6.17 shows the state-chart representation of the gating signals schemes for the two analysed converter topologies: they coherently correspond to the graphical representation of Figs.4.19 and 5.7, respectively.

As it can be noted, the principle of the state charts is exactly the same, as well



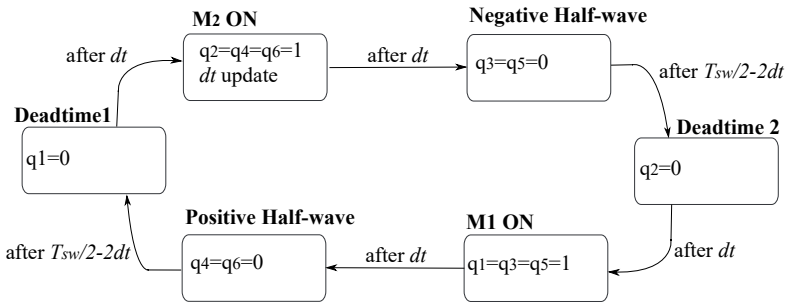
(a) Resonant current waveforms.



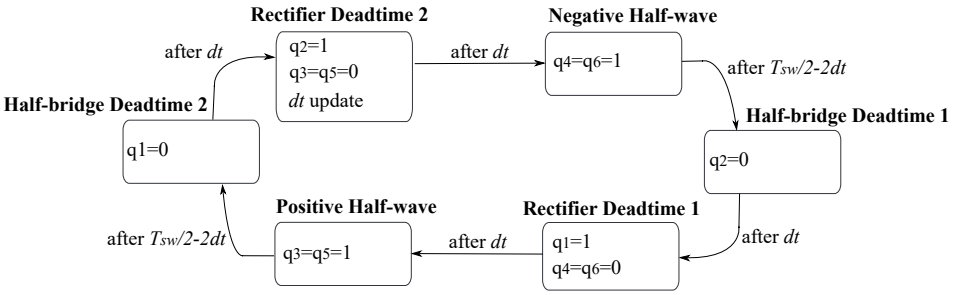
(b) Output current waveforms.

Figure 6.16: Resonant and output current waveforms for different deadtime selections (SR topology).

as the position of the "dt update" function. As described, the controller measures if the MOSFET M_2 drain to source voltage, immediately before turning it ON, is negative or positive, highlighting the polarity of the L_r current. The designed control relies on a support variable m, which represents a dimensionless rescaling of the half-bridge deadtime (the time interval to be adjusted). Specifically, the deadtime is defined in the control as $m \cdot T_\mathrm{min}$, where T_min is the minimum time interval that the FPGA can handle. Listing 6.1 reports the pseudo-code adopted to



(a) qR topology.



(b) SR topology.

Figure 6.17: Simplified state charts for the ZVS/ZCS tracking controllers of the two converter topologies.

update the deadtime a every cycle, also considering the saturation of m in case the required deadtime was too low to be physically realized (lower limit), or too high to be realistic (upper limit, when the control is probably making some mistakes).

```
if (vDS2(k)>0)
    m=m-1;
    if (m<m_min)
        m=m_min;
    end
else
    m=m+1;
    if (m>m_max)
        m=m_max;
    end
end
dt=m*T_min;
```

Listing 6.1: *Matlab* pseudo-code for the real-time update of the half-bridge deadtime in the two converters.

6.3.3 Implementation of the MPPT control

The MPPT control scheme designed for this application is a simple adaptive-step, P&O scheme. It is designed in *Matlab/Simulink* environment through a *Stateflow* block, like the ZVS/ZCS tracking controller. As described, the goal of this controller is to adjust the switching frequency (actually, the switching period) to track the absolute maximum of the PV panel $P-V$ characteristic. The switching is provided to the inner controller as a parametre for the state machine. The algorithm of the MPPT control is illustrated in Fig.6.18 in form of a parametric state chart.

In the initialization phase, the initial period T_{sw} and power $P_{\mathrm{k-1}}$ are set, as well as the initial period and power step (dT_{sw} and $dP_{\mathrm{threshold}}$, respectively). Also, the number of cycles N is defined as a constant. An initial *Transient macro-state* is continuously run until the power difference between two consecutive measurements is lower than the previously specified $dP_{\mathrm{threshold}}$. During this state, input voltage and current are measured and the input power computed, but the switching period is not updated. The meaning of this initial state is to wait until the startup transient is terminated, in order to avoid changing the switching frequency on the basis of transitory power oscillations.

When the *Transient macro-state* is left, the main loop of the state chart is taken. In this loop, the input voltage and current are measured for consecutive N cycles. The variables I_{in} and V_{in} collect the partial sum of the current and voltage samples. After N cycles, the inner loop is left and the power at step k is computed as follows:

$$P(k) = \left(\frac{1}{N}\sum_{i=0}^{N-1} V_{\mathrm{in,i}}\right) \cdot \left(\frac{1}{N}\sum_{i=0}^{N-1} I_{\mathrm{in,i}}\right). \tag{6.7}$$

In this approach, the average power is computed as product of the averages of voltage and currents through the N cycles, to minimize the number of products. An alternative approach could be to compute at every cycle the power $P_i = V_{\mathrm{in,i}} I_{\mathrm{in,i}}$ and executing an average at the end. But in this way, a multiplication needs to be performed at every cycle.

If the difference between two consecutive average powers is positive, the direction of the period step is correct; otherwise, it must be reversed (*Inverse direction* state). The strength of the P&O scheme is that it is independent from the actual power characteristic of the power converter. The monotonicity of the characteristic can be unknown from the point of view of the MPPT scheme.

This algorithm is adaptive-step, then the control adjusts the period step and power threshold according to how much the actual measured power is expected to be near to the MPP. The reason is that one of the main issues of algorithms based on *hill-climbing* approach, such as the P&O, is the unavoidable presence of oscillations around the MPP. Decreasing the switching period step when approaching the MPP helps reducing them.

To do so, the power difference is compared with $dP_{\text{threshold}}$ (if positive) or $-dP_{\text{threshold}}$ (if negative) to understand if the current power is *sufficiently near* to the MPP. If $-dP_{\text{threshold}} < dP(k) < dP_{\text{threshold}}$, and the period step can be reduced (manageable by the FPGA), both dT_{sw} and $dP_{\text{threshold}}$ are halved. dT_{sw} is the lower increment bound that the FPGA can handle.

On the other hand, when the irradiance scenario changes, it is necessary to quickly adjust to the new MPP. To make the controller more responsive, the period step and threshold power gap are increased when $dP(k) < -dP_{\text{threshold}}$ or $dP(k) > dP_{\text{threshold}}$. Also in this case, an upper bound for T_{sw} is defined to avoid too rapid power excursions. If dT_{sw} is already saturated at the lower or upper bound, there is no update. After all these checks, the switching period is updated, $P(k-1)$ assumes the value of $P(k)$ an the count is reset.

What still remains to define is how to choose the missing parametres defined in the control scheme. N can be chosen according to the desired responsiveness according to a pre-defined working condition (for instance, setting a specific time delay from startup to the MPP at a pre-defined irradiance condition). The initial $dP_{\text{threshold}}$ should be selected on the basis of the accuracy at which voltage and current are measured. An improved version of this algorithm could decouple the switching period update and the power threshold update, on the basis of the *smoothness* of the $P(f_{\text{sw}})$ characteristic around the MPP.

The combination of the two nested controllers allows to adjust the switching frequency to track the maximum power point of the PV panel for a certain environmental scenario, and to track the ZVS and ZCS condition at that specified working operation. Since the ZVS tracking controller is more reactive (it updates the deadtime at every switching period), the overall effect is that the ZVS should be achieved also during the transitions between two different irradiance scenarios. To understand in simulations whether the ZVS tracking controller has managed to achieve the desired condition, it is sufficient to observe if the parametre m (the dimensionless ratio between the actual deadtime and the minimum time interval T_{min}) oscillates between two values. If it happens at stationary operation, it means that the measured M_2 voltage $v_{\text{DS,2}}$ is alternatively positive and negative, thus at the border of the ZVS region. Fig.6.19 reports two plots of the evolution of m in the two converters, for piecewise contant irradiances. Actually, this is an unreal situation, since the irradiance cannot vary instantly, but exhibits a limited bandwidth. The purpose of these simulations was to prove the capability of the ZVS tracking controller to react to rapid working point variations. The plots show that, as soon as the irradiance changes, m starts changing until it reaches an oscillating operation. Contrarily to the ideal expectations, most of the times the oscillations involve three values: this deviation from ideality is linked to the unavoidable oscillations of $v_{\text{DS,2}}$ linked to the inductive parasitics of the MOSFETs.

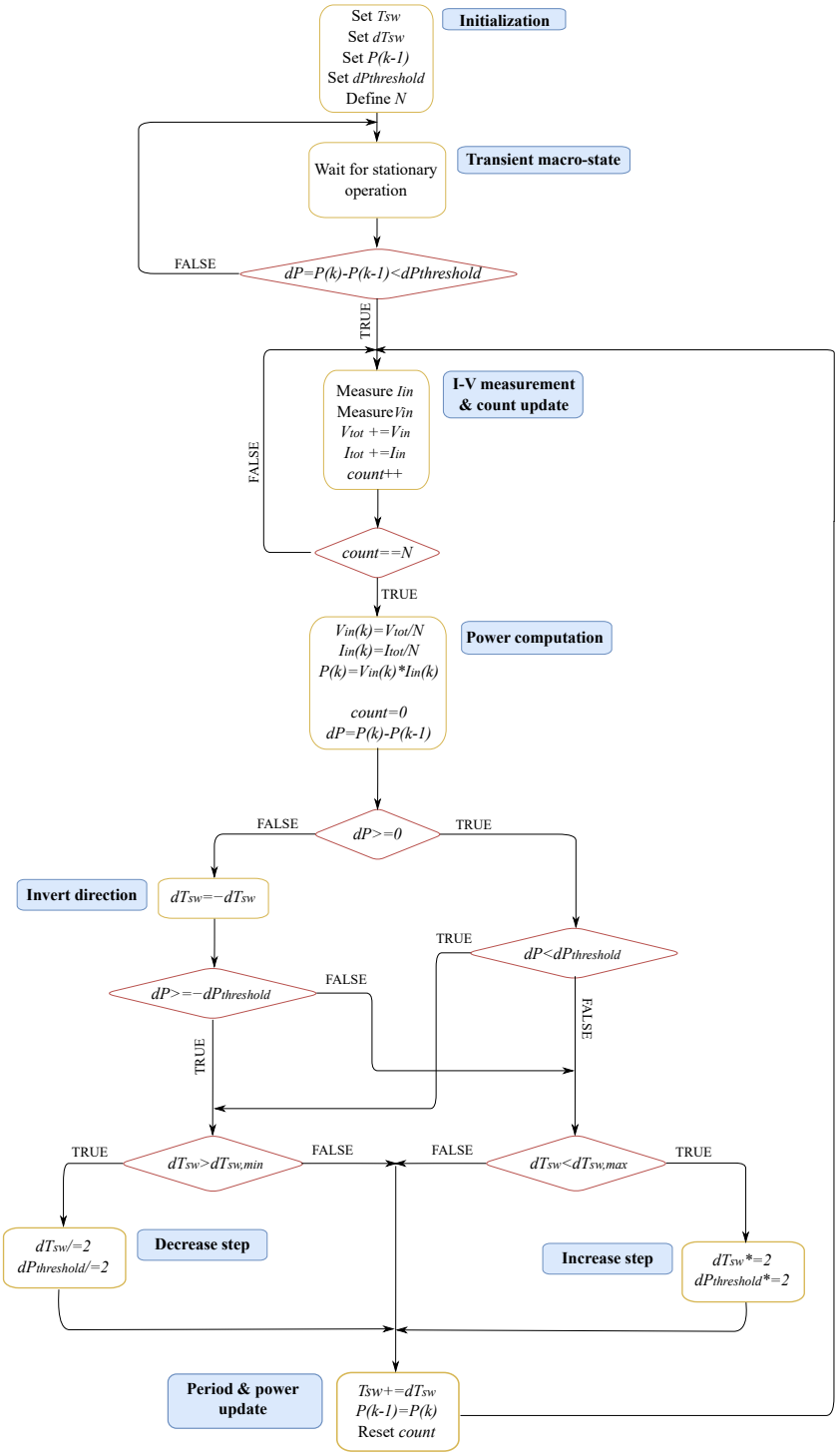


Figure 6.18: State chart of the implemented P&O MPPT scheme.

In Fig.6.19b, it is possible to observe a saturation of m to the minimum allowed value (set, in these simulations, to 60 ns), symptom that this value cannot ensure ZVS. Here, it is also interesting to observe that the SR converter topology, originally introduced in this work with the aim of increasing the allowed deadtime for ZVS, does not provide significant advantages for non-maximum power operations. There is, for this topology, an intrinsic conflict between power and ZVS operation: working next to the resonant frequency would ensure the maximum power transfer, but at the same time decreasing the possibility to achieve ZVS.

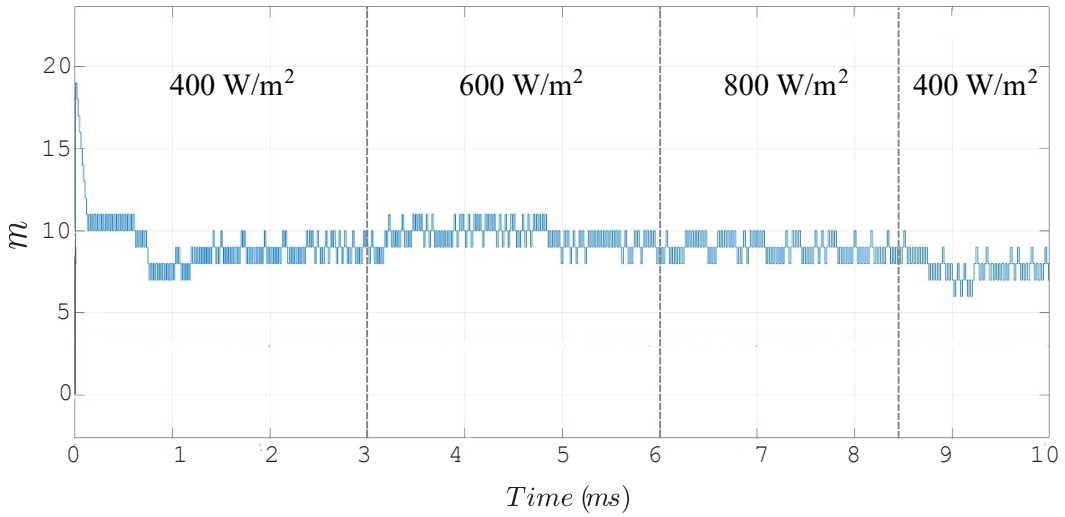
6.4 Evaluation of components losses

In this section, some of the simulation results are analysed from the point of view of the components losses. The objective is to evaluate the contribution of each main component of the power section of the converters, in order to tune the definitive selection for the BOM. The reference simulated conditions for the comparison of the two converters are here detailed:

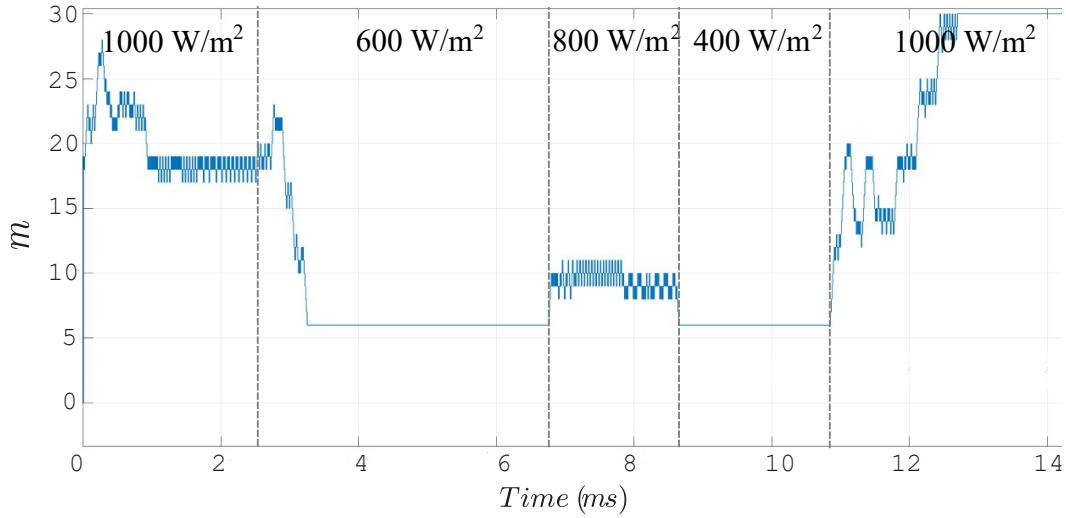
- the input source is the PV panel adopted for the previous simulation results, operating at STC ($T = 25\,°C$, $G = 1{,}000\,W/m^2$);
- the load is the usual ideal battery with 13.2 V voltage, the one specified in IEC 62509:2011 for the standardized charging efficiency measurement [42];
- the converters are operated at 100% and 50% of the maximum charging power obtained with the specified source and battery voltage. For each operating condition, the switching frequency is tuned to achieve the desired output power;
- the timing of the driving scheme was selected to achieve ZVS of the half-bridge MOSFETs and ZCS of the rectifier MOSFETs. Figs.6.14 and 6.15 already provided indications on how the MOSFETs losses vary by modifying the timing scheme.

The simulations were carried out in *LTSpice XVII*[14] environment, providing helpful macros for the waveforms post-processing. As in the previous simulations, the entire control is behavioral, so only the losses related to the power section components could be evaluated. The pie charts in Fig.6.20 show how losses within every simulation were shared among the main components (MOSFETs, resonant

[14] `https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html`.



(a) qR topology.



(b) SR topology.

Figure 6.19: Evolution of parameter m to irradiance variations, for the two topologies.

inductor, dividing capacitors, input/output filters components). The pie charts should be read together with Tab.6.8, reporting in absolute form the computed losses for each of the main components of the charts. General comments of the simulation results are the following:

- despite the same choice of MOSFETs for the two topologies, and the same output power operation, the qR topology exhibits lower total losses (higher efficiency);

- the half-bridge MOSFETs, especially, exhibit sensibly lower dissipation in the qR topology. A possible explanation stands in the conduction losses, which are increased in the SR topology due to the larger *RMS* current. Considering idealized MOSFETs currents (square wave in the qR case, half-sinusoid in the SR), it is possible to prove that the ratio of *RMS* currents is:

$$\frac{I_{\mathrm{M_1}}(\mathrm{RMS,\ SR})}{I_{\mathrm{M_1}}(\mathrm{RMS,\ qR})} \approx \frac{\sqrt{2}\pi}{4} \approx 1.11\,. \tag{6.8}$$

  Approximately, it would be expected to retrieve a 20% additional power dissipation in the SR topology;

- the same explanation (larger *RMS* current) can be given to the larger losses of the dividing capacitors;

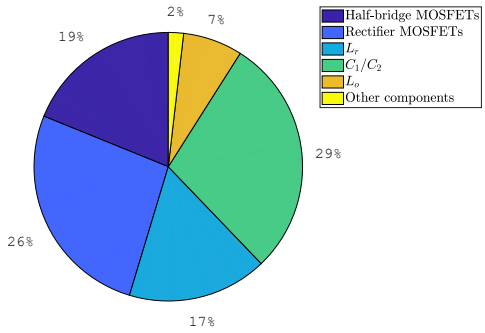
- the larger inductor in the SR topology is responsible for a significant part of the total losses. Both the increased inductance value (requiring a larger number of coil turns) and the adoption of high saturation cores (necessary to withstand the larger peak currents without causing saturation) lead to a sensible increase of the resonant inductor dissipation. The increased inductor power in the qR topology at 50% of the maximum current operation is linked to the higher switching frequency, which causes larger core losses;

- the input capacitance is way more influential on the total losses in the SR topology. Once again, the reason stands in the higher *RMS* current. which can be analysed by applying the KCL at the input node;

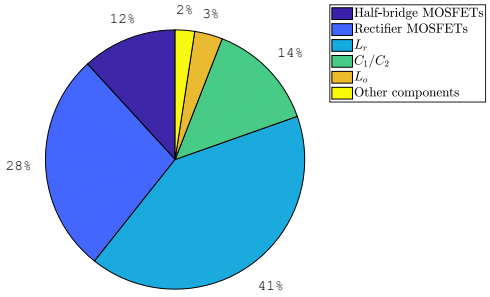
- the analysis of the output filter components losses shows, as expected, a larger dissipation in case of an inductive filter (qR topology) rather than a capacitive one (SR topology).

	$M_{1,2}$	$M_{3...6}$	$C_{1,2}$	L_r	C_in	L_o	C_o	Total losses
qR topology, 100% current	119 mW	83 mW	182 mW	212 mW	17 mW	90 mW	/	1.26 W
SR topology, 100% current	160 mW	137 mW	218 mW	715 mW	252 mW	/	46 mW	2.38 W
qR topology, 50% current	44 mW	51 mW	51 mW	304 mW	14 mW	26 mW	/	0.74 W
SR topology, 50% current	119 mW	47 mW	56 mW	454 mW	71 mW	/	8 mW	0.90 W

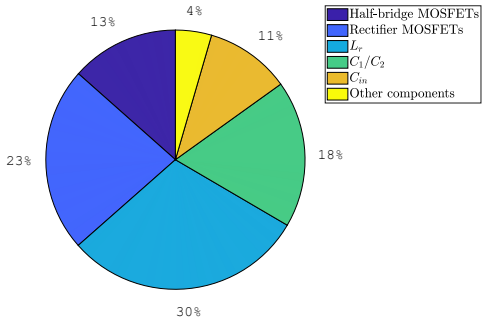
Table 6.8: Comparison of components losses and total losses for the two topologies.



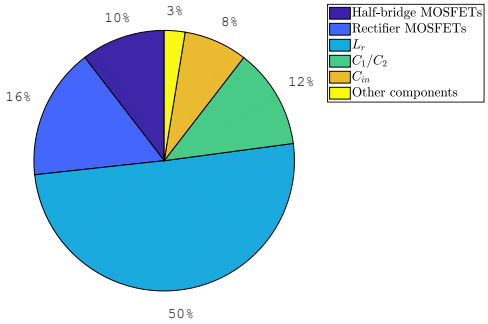
(a) qR topology, 100% maximum current operation.



(b) qR topology, 50% maximum current operation.



(c) SR topology, 100% maximum current operation.



(d) SR topology, 50% maximum current operation.

Figure 6.20: Share of losses in the two analysed converters for 100% and 50% maximum current operations.

Chapter 7

PCB prototype implementation

Until now, the description of both the converter topologies was carried along. The simulation results in Chap.6 allowed to compare the performances under reference working conditions. In the context of this work, however, only the qR topology (reported again in Fig.7.1) was considered for a physical PCB implementation.

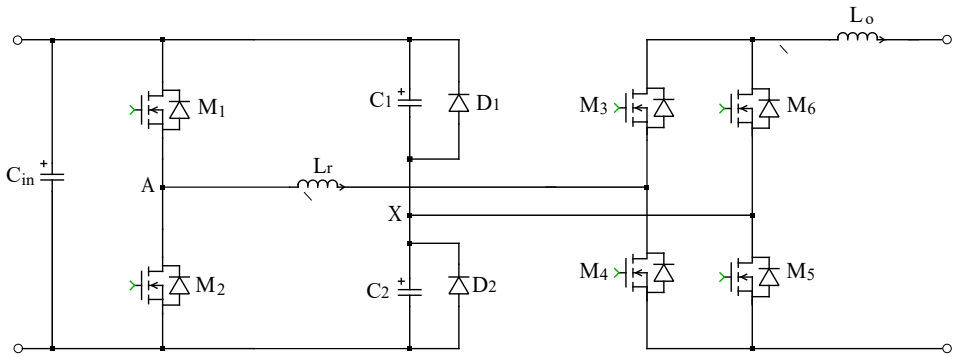


Figure 7.1: Schematic of the qR topology.

Multiple aspects were taken in account for this selection:

- this topology, according to the simulation results, exhibits higher efficiencies in the high-power region, and allows to transfer a higher maximum power;
- a full mathematical model was developed in this work to describe the behaviour of the static characteristic, detailed in both the low-frequency and high-frequency operating regions and validated by simulations. The mathematical model of the SR topology, instead, is only valid in a neighborhood of the resonance frequency and should be expanded in further work;

- the load of these converters is a battery to be recharged. General guidelines specify that the charging current ripple should be limited for an efficient and safe charging. The presence of an inductive filter in the qR topology allows to reduce effectively the current ripple: in the highest power operation, the current ripple was observed to be around 0.7 A with a 33 µH inductor. An effective filtering of the output current from a capacitor in the SR topology, instead, would require it to exhibit $ESR \ll R_{\text{batt}}$ (30 mΩ, in this case). Typical electrolytic capacitors could hardly have such low parasitic resistances;

- the resonant inductor L_{r} selection was another determinant factor in the choice: for the same output power, the qR topology allows to decrease the peak and *RMS* currents of this components. Due to the power-ZVS conflict mentioned before, the larger L_{r} value in the SR topology does not even ensure larger deadtime windows.

On the other hand, the qR topology exhibits critical aspects to be taken into account in the definitive components selection. The absence of an output capacitive filter causes significant voltage spikes across the rectifier MOSFETs, requiring an increased voltage rating of these MOSFEts. This topology exhibits two inductors rather than a single one. The output inductor selection should be taken with care, in order not to penalise the high efficiency measured in simulations.

This chapter is organized in two sections. The first one presents the design criteria for the selection of the definitive components of the BOM for the physical implementation of a prototype. The second section illustrates the PCB design performed in *Altium* environment[1].

7.1 Components selection

7.1.1 Power circuit components and gate drivers

Due to the temporary semiconductor devices shortage, it was not possible to adopt, for the physical implementation, the same MOSFETs adopted for the simulations. The simulation of a preliminary device, however, allowed to derive definitive design criteria:

- the voltage rating of the rectifier MOSFETs, due to the voltage spikes developed during their turn OFF, must be larger than the input MOSFETs one. Infineon $BSZ070N08LS5$, rated 80 V, was proved to temporary enter the breakdown

[1] `https://www.altium.com/it/altium-designer`.

region when turned OFF in hard-switching. For safety purposes, it is necessary to increase the voltage rating to 100 V. A good PCB layout design should minimize the parasitic inductance of the drain and source traces, to limit the amplitude of the voltage spike as much as possible. The presence of an input capacitor, instead, allows to reduce the voltage rating of the half-bridge MOSFETs, which depends on the maximum PV panel voltage (≈ 30 V for a 48-cell panel);

- the current ratings is established from the maximum conducted current, equal for all the MOSFETs to the maximum load current ($\approx$ 10 A for a 120 W operation with a completely discharged battery);
- the ad-hoc design of a control tuned to achieve ZVS/ZCS should significantly decrease the switching losses of the MOSFETs. As also observed in simulation, when the control manages to ensure soft swtiching, the conduction dissipation is the main contribution to the total losses. A low ON-state resistance (below 10 mΩ), then, is fundamental to ensure low conduction losses.

Due to the necessity to decrease the intrinsic $R_{\mathrm{DS,ON}}$ and the switching losses (that are associated to the energy stored in the parasitic capacitances), a GaN FET was also considered in the selection phase, EPC2214[2]. This GaN FET exhibits 15 mΩ resistance and 129 pF C_{oss}, against the 7 mΩ $R_{\mathrm{DS,ON}}$ and 490 pF C_{oss} of the MOSFET. A $G = 1{,}000\,\mathrm{W/m^2}$, $V_{\mathrm{batt}} = 12$ V simulation showed the meaningful results of Tab.7.1, reporting the losses for a single rectifier MOSFET/FET in case of ZCS ($dt = 60$ ns) and hard-switching ($dt = 140$ ns). What emerges at first glance is that the significantly lower output capacitance of the GaN FET (and consequently, the contribution of switching losses) is not sufficient to compensate for the larger $R_{\mathrm{DS,ON}}$. The apparently unexplained losses of the GaN FET at HS operation, lower than the ones at ZCS, are due to the slightly lower output current operation. For this specific case, the larger driving complexity and cost would not jystify the adoption of a GaN FET.

Of course, this result refers to a specific selection of semiconductor devices. In general, as long as the control is designed correctly, the priority design criterion is to minimize the conduction losses.

The final choice for both the half-bridge and rectifier switches is Silicon MOSFET Toshiba TPH4R10ANL[3], exhibiting low $R_{\mathrm{DS,ON}}$ (4.1 mΩ at $V_{\mathrm{GS}} = 4.5$ V), 100 V breakdown voltage, 70 A maximum DC current. Moreover, the MOSFETs exhibits

[2] `https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2214_datasheet.pdf`.

[3] `https://www.mouser.it/datasheet/2/408/TPH4R10ANL_datasheet_en_20191018-1114606.pdf`.

Device	Dissipated power in ZCS operation	Dissipated power in HS operation
Si MOSFET (Infineon)	264 mW	400 mW
GaN FET (EPC)	571 mW	516 mW

Table 7.1: Comparison of Silicon MOSFET and GaN FET losses in presence and absence of ZCS condition.

low typical turn-ON and turn-OFF times (few tens of ns), making it suited for accurate turn-ON/OFF control.

Together with the MOSFETs, the selection of the gate drivers took into account the following criteria:

- galvanic insulation, necessary to isolate the digital domain (FPGA) and the power section domain;
- many gate drivers for half-bridge configurations provides the possibility to control two MOSFETs with a single control signal, thanks to the internal generation of the deadtime. For this application, however, the need to adjust real-time the deadtime requires two independent inputs;
- a low propagation delay (no more than few tens of ns) is required to ensure a fast response of the power system to the digital signals generated by the FPGA.

The adopted MOSFETs can be completely turned ON with $V_{GS} = 5\,V$. The selection of the three gate drivers (for the input and the rectifier legs) is the following one: Analog Devices ADuM3223 [4]. The input side of the driver is compliant with the typical digital supply voltages (3.3 V or 5 V) and the output exhibits an allowed voltage range from 4.5 V to 18 V. The floating supply for the high-side MOSFETs can be obtained with an external bootstrap circuit, for which the datasheet recommends the specifications. The IC exhibits a typical propagation delay of 47 ns, and two independent channels.

The inductor L_r value, 330 nH, was selected at the beginning of the simulation phase as a good trade-off between allowed ZVS time window and achievable output power, according to Figs.4.14 and 4.15, respectively. The saturation and thermal currents should be larger than the maximum output current. Differently from the output filter inductor, this component is troublesome from the point of view of AC losses, which, however, are not easy to be estimated.

[4] `https://www.mouser.it/datasheet/2/609/ADuM3223_4223-1503589.pdf`.

For the implementation, the 330 nH ferrite-core inductor from the Vishay IHLP-5050CE-01 series[5] was selected, exhibiting low DC resistance (1.3 mΩ), 36.5 A rated current for 40 °C temperature increase, and 62 A saturation current for a 20% inductance decrease.

Vishay's website provides a tool for the estimation of the DC, AC and core losses of its high-current inductors, when operating in elementary DC-DC converter topologies (buck, boost, buck-boost), *IHLP Inductor Loss Calculator Tool*[6]. To derive at least a generic indication of the order of magnitude of AC and core losses, a fictitious equivalent buck configuration was simulated in the tool, trying to tune the simulation parametres to obtain the desired *RMS* AC current. The *RMS* value of a triangular wave is indeed equal to its peak-to-peak value divided by $\sqrt{3}$. A $7\,\mathrm{A_{RMS}}$ AC current at 60 kHz, for instance, produced the following results:

$$\begin{cases} P_{\mathrm{core}} = 83\,\mathrm{mW} \\ P_{\mathrm{AC}} = 205\,\mathrm{mW} \\ \Delta T_{\mathrm{rise}} = 8.2\,^{\circ}\mathrm{C} \end{cases},$$

where ΔT_{rise} is the temperature rise during operation. In a 84 W operation (with 12 V battery voltage), these losses would represent the 0.3% of the output power.

The dividing capacitors are as well subjected to a high current stress: $I_{\mathrm{C_{1,2},RMS}} = \frac{I_{\mathrm{o}}}{2}$. As a consequence, they should exhibit a low ESR to avoid overheating. Their voltage rating is selected according to the maximum input voltage. Since, when working in the low-frequency region, their voltage can reach slightly negative values (clamped by the antiparallel diodes), these capacitors cannot be polarized. The capacitance value, 1 µF, was tuned in the preliminary simulations according to the maximum transferred power: increasing the capacitance value, indeed, determines a larger power transfer in the low frequency region, but shifts to lower frequencies the boundary with the second region. As a result, it is possible to determine an optimal trade-off value.

The final choice is MLCC stacked capacitor KEMET C1812C944J5JLC7805[7]. Its dielectric, U2J, ensures large stability of the capacitance value with respect to DC voltage changes, and a linear and predictable variation of capacitance to temperature changes. Its new packaging technology, KONNEKT, ensures really low ESL and ESR. The capacitor exhibits $50\,\mathrm{V_{DC}}$ rated voltage, $12\,\mathrm{A_{RMS}}$ rated current at 100 kHz and 940 nF. The slightly lower capacitance value is expected to shift at slightly larger values the boundary between the two operating regions.

[5] `https://www.mouser.it/datasheet/2/427/ihlp_5050ce_01-1762386.pdf`.

[6] `https://www.vishay.com/en/inductors/calculator/calculator/`.

[7] `https://www.mouser.it/datasheet/2/212/1/KEM_C1097_KONNEKT_U2J-1627561.pdf`.

7.1.2 Input and output filters

The input electrolytic capacitor, which is responsible for stabilizing the working point of the PV panel by providing a low-impedance path for high frequency currents, was selected according to the allowed input current ripple. This limit can be studied from the deterioration of the output power of a PV panel when it is forced to provide a current with high ripple content.

Lin et al., in [43], investigated the effects of a triangular current ripple on the output power provided by a PV panel. The device-under-test was connected to a boost converter, absorbing an average current equal to I_{MPP} and variable ripple. The authors observed that the dynamic $P-V$ characteristic of the panel exhibit an hysteresis, more important with low-frequency ripples, with an overall decrease in the average power compared to the MPP. For the same triangular current (with peak-to-peak ripple equal to 60% of the average value), the PV panel experienced 5% power decrease at 10 kHz and 0.4% at 100 kHz. At 90% ripple current at 10 kHz, the panel power decreased by 20% compared to the MPP.

Elkhateb et al., in [44], proposed a model-based derivation of the power decrease of a PV panel when providing a rippled current. By adopting a single-diode model for the PV panel, the authors derive the following approximated formula:

$$\frac{P_{\mathrm{ripple}}}{P_{\mathrm{MPP}}} \approx 10.67\left(\frac{\Delta I_{\mathrm{RMS}}}{I_{\mathrm{MPP}}}\right)^2, \tag{7.1}$$

where ΔI_{RMS} is the *RSM* value of the ripple current. From this equation, the authors report a 2.7% power decrease with 5% current ripple, and 6.83% power decrease with 8% current ripple. Despite the absence of quantitative constraints, it is recommended in the article to maintain the ripple current of a PV panel below 50% of the short-circuit current I_{SC}.

This constraint was taken a reference for the selection of the input capacitor. The following analytical approach was followed for the determination of the necessary ESR of the input capacitor. At few tens of kHz, the typical frequency region of this converter, an electrolytic capacitor impedance is expected to be dominated by its ESR. It is necessary to impose that the ESR is much lower than the PV panel small-signal resistance.

Following an analytical approach based on the SDM of a PV panel, the minimum small signal resistance, evaluated as $\frac{dV_{\mathrm{PV}}}{dI_{\mathrm{PV}}}$, is found at the open-circuit working point:

$$r_{\mathrm{ss,min}} \approx R_{\mathrm{s}} + \left.\frac{dv_{\mathrm{diode}}}{di_{\mathrm{diode}}}\right|_{\mathrm{OC}} = R_{\mathrm{s}} + \frac{\eta N_{\mathrm{s}} V_{\mathrm{th}}}{I_{\mathrm{SC}}}\,. \tag{7.2}$$

With the already adopted parametres of the PV panel model (Tab.2.1), $r_{\mathrm{ss,min}} \approx 0.65\,\Omega$. From the simulations, what emerges is that the current absorbed by the

converter is equal to $\frac{I_o}{2}$ during most of the switching period, and null during the short mode 3. As a result, the ripple current is $\frac{I_o}{2}$. It is of interest to reduce the ripple current provided by the PV panel:

$$\begin{cases} \Delta I_{\mathrm{PV}} = \dfrac{ESR}{ESR + r_{\mathrm{ss,min}}} \dfrac{I_o}{2} \\ \Delta I_{\mathrm{PV}} \overset{!}{=} 5\% I_{\mathrm{SC}} \end{cases} . \tag{7.3}$$

From Eq.7.3, applied to the worst case (maximum output current):

$$ESR \approx 45\,\mathrm{m\Omega}\,.$$

Assuming a 10 kHz cutoff frequency of the electrolytic capacitor:

$$C_{\mathrm{in}} = \frac{1}{2\pi ESR f_{\mathrm{cutoff}}} \approx 350\,\mu\mathrm{F}\,. \tag{7.4}$$

The voltage rating of the input capacitor must be selected according to the maximum PV panel voltage (around 30 V for a 48-cell panel.

Finally, the maximum *RMS* current that this capacitor must provide in the worst condition (maximum power operation), could be approximately computed by applying the quadratic-KCL at the input node (assuming that the entire AC part of the input current is provided by the capacitor):

$$I_{\mathrm{C_{in},RMS}} \approx 2C_1 f_{\mathrm{sw}} V_{\mathrm{in}} \sqrt{\frac{V_{\mathrm{in}}}{2V_{\mathrm{batt}}} - 1}\,. \tag{7.5}$$

This formula is, however, dependent on the non-linear PV panel characteristic. From simulation results in the maximum power operation, the maximum $I_{\mathrm{C_{in},RMS}}$ was measured to be around 0.9 A.

Nichicon UCZ1J751MNS1MS[8] Aluminum electrolytic capacitor was selected, exhibiting 63 V voltage rating, 750 µF capacitance, 68 mΩ ESR and 2.5 A ripple current rating.

For the output filter inductor, a similar approach was followed, based on the maximum allowed current ripple overimposed to the average charging current. Again, there is lack of precise documentation on ripple constraints. However, some recommendations can be found in application notes regarding a specific type of battery. The maximum allowed ripple current is usually recommended on the basis of the maximum heating for a safe charging/discharging operation. For VRLA (sealed lead-acid batteries), for instance, it is recommended to limit the ripple

[8] `https://www.mouser.it/datasheet/2/293/e_ucz-1903374.pdf`.

current below a value equal to 1/20 of the battery capacity, expressed in *ampere*[9]. For a 50 A h battery, for instance, the ripple current should be maintained below 2.5 A.

Adopting this value as design constraint, it is possible to derive an approximated expression of the output current ripple from the analysis of the output voltage waveform of the active rectifier. Assuming, as worst condition, to work in the low-frequency operating region, the secondary voltage exhibits a sawtooth behaviour, resulting in a parabolic ripple of the output current. The analytic integration of the filter inductor voltage, combined with suited approximations, leads to the following approximated formula for the output current ripple:

$$\Delta I_{\text{ripple}} \approx \frac{V_{\text{in}}}{12 f_{\text{sw}} L_{\text{o}}} \,. \tag{7.6}$$

Imposing this ripple to be lower than 2.5 A at 50 kHz operation, and at 28 V input voltage:

$$L_{\text{o}} > 19\,\mu\text{H}\,.$$

Considering this lower limit, and a maximum output current of 10 A (120 W operation with completely discharged battery), the following inductor was chosen for the implementation: Wurth Elektronik 74437529203470[10]. This ferrite-core, wire-wound inductor exhibits a 47 µH nominal inductance (±20% tolerance), 8.8 mΩ DC resistance, 13 A saturation current for 30% inductance decrease, and 17.5 A maximum current for a temperature increase of 40 °C.

Wurth Elektronik's website provides a tool to estimate DC and AC losses of its power inductors, RedExpert[11], when operating in the elementary DC-DC converter topologies (buck, boost and SEPIC). Unfortunately, it is not possible to define an ad-hoc topology to estimate the losses in the desired configuration. However, by defining an equivalent buck-based configuration for which the average and *RMS* currents are the same as in the proposed topology, it is possible to retrieve at least the order of magnitude of the inductor losses. For a 100% maximum charging current condition at 13.2 V battery voltage (same operating condition of the results i Tab.6.8), the DC and AC losses of this inductor are computed to be around 300 mW and 10 mW, respectively. As expected, due to the low contribution of the current ripple compared to the average value, the DC losses are dominant.

[9] `https://datacsi.com/wp-content/uploads/white-papers/Effects-of-AC-Ripple-Current-on-VRLA-Battery-Life-Technical-Note-TN-00008.pdf`.

[10] `https://www.mouser.it/datasheet/2/445/74437529203470-1721700.pdf`.

[11] `https://redexpert.we-online.com/we-redexpert/en/#/redexpert-embedded`.

7.1.3 Components for the acquisition of $v_{DS,2}$

The acquisition of M_2 drain-source voltage is a fundamental task of the control system to tune in real-time the half-bridge deadtime. The acquisition chain only needs to acquire the polarity of the drain-source voltage (not its actual value), since this information is enough to establish whether the MOSFETs was turned ON in soft or hard switching condition. As a consequence, a comparator-based acquisition chain is exploited.

In order to acquire the voltage polarity at the time instant at which the turn-ON signal is sent to the MOSFET, the comparator propagation delay should be minimised (no more than few ns). While the input voltages must be referenced to the input power ground, the digital output should be compliant to the FPGA supply domain. Thus, an isolated comparator should be preferred for this application. After comparing multiple solutions, the scheme in Fig.7.2 was adopted.

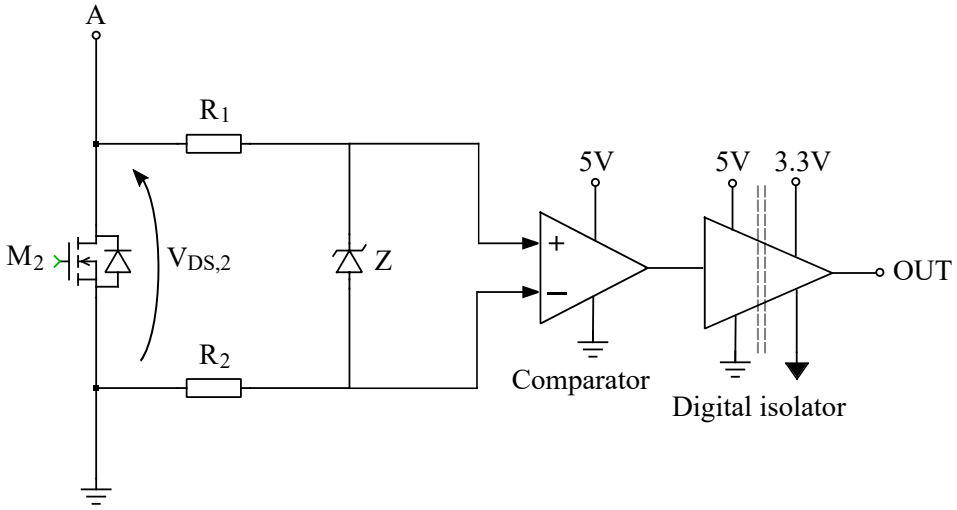


Figure 7.2: Simplified schematic of the $v_{DS,2}$ acquisition chain.

The voltage across M_2 is clamped by a Zener diode (Onsemi SZMMSZ4678T1G[12]) to limit the input differential voltage between $-0.9\,\mathrm{V}$ (forward voltage) and $1.8\,\mathrm{V}$ (Zener voltage), to make it compliant with the comparator maximum input voltage swing. Two $100\,\mathrm{k\Omega}$ resistors (Bourns CR0805-FX-1003ELF[13]) limit the maximum current, and thus the dissipated power, flowing in this branch:

$$I_{\max} \approx \frac{30\,\mathrm{V} - 1.8\,\mathrm{V}}{200\,\mathrm{k\Omega}} \approx 140\,\mu\mathrm{A}. \tag{7.7}$$

[12] https://www.mouser.it/datasheet/2/308/1/MMSZ4678T1_D-2316153.pdf.

[13] https://www.mouser.it/datasheet/2/54/cr-1858361.pdf.

For the resistances, a higher value was discarded to avoid increasing the delay in the acquisition of the voltage. The input side of the comparator, indeed, includes an equivalent capacitance constituting a 1^{st} order low-pass filter with the resistors. On the other hand, the filtering effect is partially desired, allowing to filter out the high frequency ringing linked to the MOSFET parasitics.

The choice for the comparator is Analog Devices LT1394IS8[14]. Its features, listed below, make it a suitable choice for this application:

- very low propagation delay (7 ns typical);
- the supply voltage range includes 5 V, allowing to re-use the same supply voltage of the half-bridge gate driver;
- the external Zener diode allows to limit the common mode voltage within the 3.5 V maximum value specified by datasheet;
- the comparator includes a latch pin whose task is to *freeze* the output when "high". This functionality is exploited in this application: the "latch" pin is connected, in the PCB, to the trace linking the second output of the gate driver to the gate of M_2. In this way, when the FPGA sends to the gate driver the signal to turn ON M_2, the "latch" pin is also activated to store the value of $v_{\mathrm{DS},2}$ immediately before its turn ON, as desired. The value is then made available for the entire half switching period, and can be processed by the FPGA until the MOSFET is turned OFF again.

This choice of comparator does not ensure galvanic insulation. A buffer is then necessary to isolate the input power domain from the digital domain, without altering the information from the comparator. A suitable choice for the isolator is Texas Instrument ISO7810DWR[15], whose supply domains are compliant with the desired ones (5 V input, 3.3 V output) and which in turns exhibits low propagation delays (10.7 ns typical). The digital output of the isolator is acquired by the FPGA.

7.1.4 Components for the acquisition of the input power

The P&O MPPT algorithm is based on the acquisition, at each cycle, of both the input voltage and current, to compare the currently measured power with the previous one. For a compact design, SMD isolated voltage/current sensors can

[14] `https://www.mouser.it/datasheet/2/609/1394f-2953697.pdf`.

[15] `https://www.ti.com/lit/ds/symlink/iso7810.pdf?ts=1662927422568&ref_url=https%253A%252F%252Fwww.google.com%252F`.

be adopted. The propagation delay, in this case, is not crucial, since the MPPT algorithm does not need to update the frequency at each switching cycle.

For the input voltage sensor, Broadcom ACNT-H87A-000E[16] is selected. It consists in an optically isolated voltage sensor with unitary gain ($\pm 1\%$) and 100 kHz bandwidth. The typical propagation delays to step inputs are around few μs, but this sensor is intended to measure the input DC voltage, stabilized by the input capacitor. The presence of an offset voltage around few mV is not critical from the point of view of the MPPT, since the goal is to measure a power difference between consecutive acquisitions. Due to the limited input voltage dynamics, an external voltage partition is needed to adjust the input voltage to the sensor swing. Two resistors of 100 kΩ and 1.5 MΩ ($\pm 0.5\%$) are included to realize a $\frac{1}{16}$ voltage ratio. In this way, an input voltage of 32 V is stepped down to the allowed input voltage swing of the sensor (2 V). The input and output sides of the sensor can be supplied by 5 V and 3.3 V (compliant with the other ICs of the input side and FPGA, respectively). The sensor is endowed with two differential outputs, with a $V_{\mathrm{DD}}/2$ offset: the datasheet recommends a differential-to-single ended unity gain amplifier, but, for a larger compactness, both the analog signals can be acquired and post-processed directly by the FPGA.

A suitable choice of current sensor is Texas Instrument TMCS1100A3QDRQ1[17]. It consists in a galvanically isolated, Hall-effect based current transducer with high precision (0.9% total error) and unidirectional current range up to 15.5 A, when supplied by 3.3 V. Its sensitivity is 200 mV/A.

Evaluation of uncertainty on the measurement of the MPP

Once the sensors for the input power measurement have been selected, it may be of interest to evaluate with what precision the MPP can be identified. Usually, this evaluation is extracted *a posteriori* in literature, by computing the already mentioned static MPPT efficiency, ratio between the measured and nominal maximum powers, within a specified time window:

$$\eta_{\mathrm{MPPT,\,static}} = \frac{\sum_i V_{\mathrm{i}} \cdot I_{\mathrm{i}} \Delta T}{P_{\mathrm{MPP}} T_{\mathrm{M}}} \,, \tag{7.8}$$

where V_{i}, I_{i} and T_{M} are the single input voltage measurement, input current measurement and measuring time window. According to EN 50530:2010, "the static MPPT efficiency describes the accuracy of an inverter to regulate on the maximum

[16] https://www.mouser.it/datasheet/2/678/ACNT-H87x-DS101-1827917.pdf.

[17] https://eu.mouser.com/ProductDetail/Texas-Instruments/TMCS1100A3QDRQ1?qs=QNEnbhJQKvbSpEPUTmmI9w%3D%3D.

power point on a given static characteristic curve of a PV generator"[41].

Here, an analytical approach is presented to try to estimate *a priori* the accuracy of the MPPT, on the basis of the analysis of the acquisition chain for the input voltage and current, and of the operation of the MPPT controller, but without the knowledge of the PV panel characteristic. It must be clarified that only an experimental evaluation can precisely determine the effectiveness of the control, but this preliminary analysis can give an insight about the expected performances, and guide the adaptive step P&O algorithm design. The following analysis does not ensure that the MPP is reached, but estimates the probability for the controller to correctly perform choices in presence of two close power measurements.

The starting question of the discussion is: given the tolerances and uncertainties of the acquisition chain of the input power, and given the fact that the MPPT controller updates the switching frequency on the basis of the difference between two consecutive power measurements, how likely is it that the controller will take the correct choice? This issue can be translated in the need for evaluating the uncertainty on the measurement of the difference between the power measurements at step $k-1$ and k. Let's denote by ΔP the difference between $P(k)$ and $P(k-1)$, and by $\delta(\Delta P)$ its absolute uncertainty. If $|\Delta P| < |\delta(\Delta P)|$, it is no longer possible for the controller to clearly distinguish the sign of the power difference, and the frequency update becomes inaccurate.

Fig.7.3 shows schematically the acquisition chains for the input voltage and current: as described in this section, the input voltage is rescaled with a voltage partition between R_1 and R_2 and amplified with unity gain through a voltage amplifier. On the other hand, a Hall-effect transducer directly provides an analog voltage from the input current. Both analog signals are converted by 12-bits ADCs available on the FPGA. Let's denote by δR_1, δR_2, δG_v and δG_i the absolute tolerances on the resistances, the gain error of the voltage amplifier, and the sensitivity error of the current transducer, respectively. ϵ_{R_1}, ϵ_{R_2}, $\epsilon_{\mathrm{G_v}}$ and $\epsilon_{\mathrm{G_i}}$ are the corresponding relative uncertainties. The voltage amplifier and the current transducer exhibit different output voltage offsets, denoted by $v_{\mathrm{v,\,OS}}$ and $v_{\mathrm{i,\,OS}}$, respectively. However, due to the fact that the controller takes decision on the basis of the subtraction of consecutive power acquisitions, systematic offsets added to the acquired signals are canceled and have no influence on the decision process.

From Fig.7.3, the input current and voltage can be derived from the output analog voltages v_i and v_v as:

$$\begin{cases} I_\mathrm{in} = \dfrac{v_\mathrm{i}}{G_\mathrm{i}} \\ V_\mathrm{in} = \left(1 + \dfrac{R_1}{R_2}\right) \dfrac{v_\mathrm{v}}{G_\mathrm{v}} \end{cases} \tag{7.9}$$

According to the designed controller algorithm (presented in Fig.6.18), the

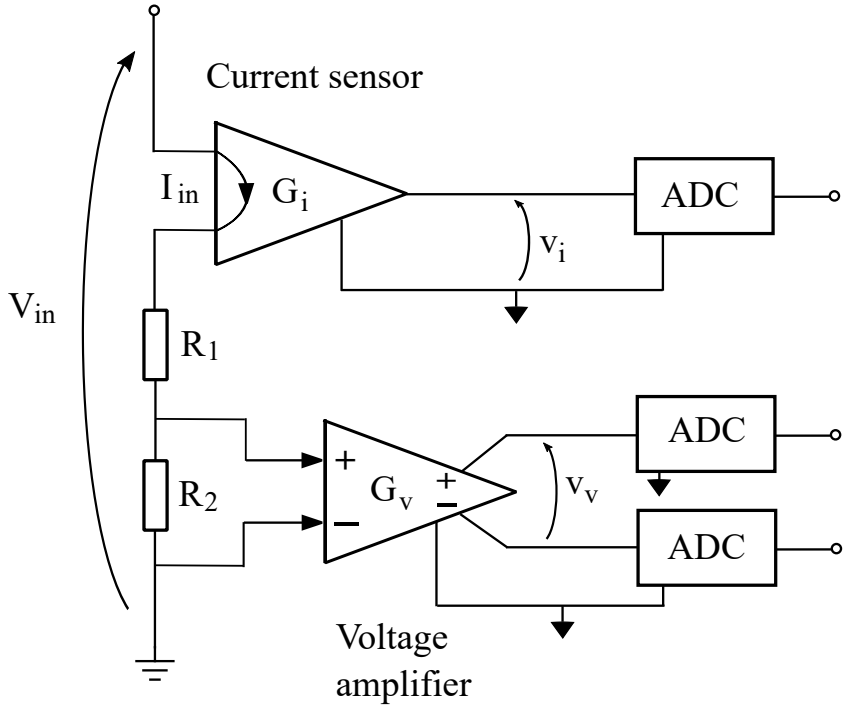


Figure 7.3: Simplified schematic of the acquisition chain for the input power.

difference between two consecutive measurements of power is then computed as follows:

$$\begin{aligned}
\Delta P &= I_{\mathrm{in}}(k)\cdot V_{\mathrm{in}}(k) - I_{\mathrm{in}}(k-1)\cdot V_{\mathrm{in}}(k-1) \\
&= \left(\frac{1}{N}\sum_{m=1}^{N} I_{\mathrm{in,\,m}}(k)\right)\cdot\left(\frac{1}{N}\sum_{m=1}^{N} V_{\mathrm{in,\,m}}(k)\right) - \left(\frac{1}{N}\sum_{n=1}^{N} I_{\mathrm{in,\,n}}(k-1)\right)\cdot\left(\frac{1}{N}\sum_{n=1}^{N} V_{\mathrm{in,\,n}}(k-1)\right) \\
&= \frac{1}{G_{\mathrm{v}}G_{\mathrm{i}}}\left(1+\frac{R_1}{R_2}\right)\left[\left(\frac{1}{N}\sum_{m=1}^{N} v_{\mathrm{i,\,m}}(k)\right)\cdot\left(\frac{1}{N}\sum_{m=1}^{N} v_{\mathrm{v,\,m}}(k)\right) - \left(\frac{1}{N}\sum_{n=1}^{N} v_{\mathrm{i,\,n}}(k-1)\right)\cdot\left(\frac{1}{N}\sum_{n=1}^{N} v_{\mathrm{v,\,n}}(k-1)\right)\right] \\
&= \frac{1}{G_{\mathrm{v}}G_{\mathrm{i}}}\left(1+\frac{R_1}{R_2}\right)\left(\overline{v_{\mathrm{i}}(k)}\cdot\overline{v_{\mathrm{v}}(k)} - \overline{v_{\mathrm{i}}(k-1)}\cdot\overline{v_{\mathrm{v}}(k-1)}\right) \\
&= \frac{1}{G_{\mathrm{v}}G_{\mathrm{i}}}\left(1+\frac{R_1}{R_2}\right)\Delta\overline{v^2}
\end{aligned} \tag{7.10}$$

The last definition is given just to provide a more compact notation. By applying the propagation of uncertainties on the measurement of $\delta(\Delta P)$, and performing some computations:

$$\begin{aligned}
\delta\left(\Delta P\right) &= \sqrt{\left(\frac{\partial(\Delta P)}{\partial G_{\mathrm{i}}}\,\delta G_{\mathrm{i}}\right)^2 + \left(\frac{\partial(\Delta P)}{\partial G_{\mathrm{v}}}\,\delta G_{\mathrm{v}}\right)^2 + \left(\frac{\partial(\Delta P)}{\partial R_1}\,\delta R_1\right)^2 + \left(\frac{\partial(\Delta P)}{\partial R_2}\,\delta R_2\right)^2 + \left(\frac{\partial(\Delta P)}{\partial(\Delta\overline{v^2})}\,\delta(\Delta\overline{v^2})\right)^2} \\
&\approx \sqrt{(\Delta P)^2\cdot\left[\epsilon^2_{\mathrm{G_i}} + \epsilon^2_{\mathrm{G_v}} + \left(\frac{R_1}{R_1+R_2}\right)^2\left(\epsilon^2_{\mathrm{R_1}} + \epsilon^2_{\mathrm{R_2}}\right)\right]^2 + \left(P^2(k) + P^2(k-1)\right)\left(\epsilon^2_{\overline{v_{\mathrm{v}}}} + \epsilon^2_{\overline{v_{\mathrm{i}}}}\right)}
\end{aligned} \tag{7.11}$$

where $\epsilon_{\overline{v_\text{v}}}$ and $\epsilon_{\overline{v_\text{v}}}$ are the relative uncertainties on $\overline{v_\text{i}}$ and $\overline{v_\text{i}}$, respectively. The last equality is based on the approximation that the relative uncertainties $\epsilon_{\overline{v_\text{v}}}$ and $\epsilon_{\overline{v_\text{v}}}$ do not change from step $k-1$ to k: this approximation, which is valid only when the output analog voltages acquired by the FPGA are sufficiently close, allows to greatly simplify the final expression.

What still remains to define is the expression for $\epsilon_{\overline{v_\text{v}}}$ and $\epsilon_{\overline{v_\text{i}}}$, which should take into account the quantization error introduced by the FPGA ADC and the averaging process on N samples of voltage/current. As explained, the sensors offsets do not impact the sign of the power difference. From the definition of relative uncertainty:

$$\begin{cases} \epsilon_{\overline{v_\text{v}}} = \dfrac{\delta\left(\overline{v_\text{v}}\right)}{\overline{v_\text{v}}} = \dfrac{1}{\overline{v_\text{v}}} \dfrac{1}{\sqrt{N}} \dfrac{LSB}{\sqrt{3}} \\ \epsilon_{\overline{v_\text{i}}} = \dfrac{\delta\left(\overline{v_\text{i}}\right)}{\overline{v_\text{i}}} = \dfrac{1}{\overline{v_\text{i}}} \dfrac{1}{\sqrt{N}} \dfrac{LSB}{2\sqrt{3}} \end{cases}, \tag{7.12}$$

where:

$$LSB = \frac{\text{Dynamic range}}{2^{ENOB}} = \frac{2.5\,\text{V}}{2^{11.33}} \approx 971\,\mu\text{V}\,. \tag{7.13}$$

The LSB computation in Eq.7.13 takes into account the effects of noise and distortion introduced by the ADC on the reduction of the *Effective Number Of Bits* ($ENOB$). As described in [45], the $ENOB$ can be computed from the *Signal-to-Noise and Distortion Ratio* ($SINAD$), usually reported in the datasheet of the ADC, as:

$$ENOB = \frac{SINAD - 1.76}{6.02}\,. \tag{7.14}$$

Notice that the adopted FPGA (Terasic De1-SoC[18]) allows to select the voltage range for the analog-to-digital conversions between $0\,\text{V} - 2.5\,\text{V}$ and $0\,\text{V} - 5\,\text{V}$. The first range allows to better exploit the ADC dynamic and is compliant with the maximum acquired signals from the selected voltage/current sensors. Thanks to this choice, it is possible to reduce the influence of the quantization error.

The following qualitative consequences emerge from Eq.7.11:

- the contributions of the resistors tolerances and of the gain errors become null when the difference between two consecutive power measurements ideally tends to zero. In this condition, only part of the contributions related to the averaged analog outputs remain:

$$\lim_{\Delta P \to 0} \delta\left(\Delta P\right) = P(k)\sqrt{2\left(\epsilon_{\overline{v_\text{v}}}^2 + \epsilon_{\overline{v_\text{i}}}^2\right)}\,. \tag{7.15}$$

[18] `https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=836`.

This phenomenon comes from the correlation between consecutive measurements of power, which allows to erase most of the contributions to the absolute uncertainty;

- the averaging on N samples of current and voltage allows to further reduce the overall uncertainty. Ideally, when ΔP tends to 0, its uncertainty becomes inversely proportional to $\sqrt{N}$.

Given the datasheet parametres of each component of the power acquisition chain, and given two consecutive power values, it is possible to provide a quantitative estimation of the uncertainty on the power difference. The result should be compared with the actual ΔP: when $|\Delta P| < \delta(\Delta P)$, the sign of the difference can no longer be known with precision, and the controller may take the wrong choice in the frequency update. In other words, $\delta(\Delta P)$ represents the smallest power step below which the controller operation cannot provide accurate results. $\delta(\Delta P)$, thus, provides information on the precision with which the controller works when two consecutive measurements are sufficiently close, regardless of whether they are around the nominal MPP or not. $\delta(\Delta P)$ could be used, in the proceeding of this work, to define the minimum step of the adaptive-step P&O scheme.

Parameter	**Value**
ϵ_{G_i}	1.15% (max.)
ϵ_{G_v}	1% (typ.)
ϵ_{R_1}	0.1%
ϵ_{R_2}	0.5%
$R_1/(R_1+R_2)$	15/16
N	16
$v_{i,\,OS}$	± 8 mV
$v_{v,\,OS}$	± 9.9 mV (3σ)

Table 7.2: Parameters adopted for the quantitative computation of $\delta(\Delta P)$.

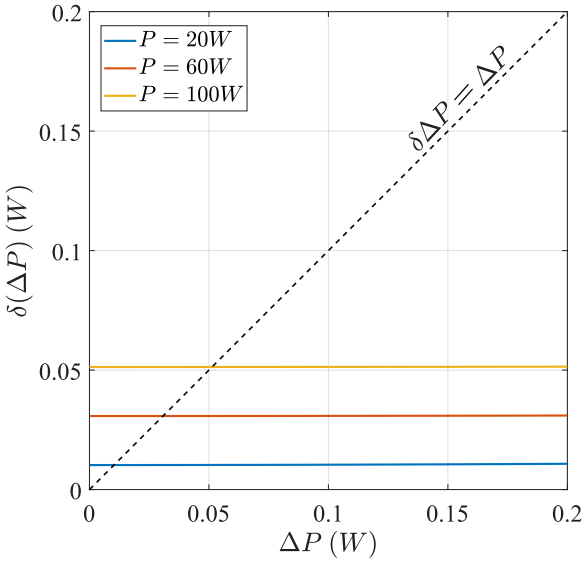


Figure 7.4: Quantitative evaluations of $\delta(\Delta P)$ for different power levels.

The plots of Fig.7.4 consider the worst case in terms of uncertainty on the gains.

The plots highlight a nearly constant behaviour, meaning that the most important contribution to the absolute error comes from the ΔP-independent term of its expression, related to the quantization error. The graphs should be read in this way: given a certain $P(k)$, wherever the corresponding $\delta(\Delta P)$ (coloured, solid line) is lower than ΔP itself (black, dashed line), the sign of the power difference can no more be established with precision. For instance, for $P(k) = 100\,\mathrm{W}$, the controller may take the wrong decision if $\Delta P < 50\,\mathrm{mW}$, corresponding only to the 0.05% of the measured power.

7.1.5 Supply domains

The ICs of the system require three different supply domains:

- the input gate driver, the input voltage sensor, the comparator and the input side of the digital isolator require a 5 V supply referenced to the input ground (negative terminal of the source);
- on the other hand, the rectifier MOSFETs gate drivers cannot be supplied with the same voltage, since the output negative rail voltage is floating with respect to the input ground. As a consequence, another 5 V supply must be generated, referenced to the battery negative terminal;
- the input side of the three gate drivers, the input voltage and current sensors, and the output side of the isolator need to be supplied by 3.3 V.

While the third supply voltage can be directly provided by the FPGA, the other two supply voltages need to be generated somewhere else. A possible approach could be to generate them externally, but this solution would require a power supply with two isolated outputs. A more compact solution, adopted in this PCB implementation, is instead to generate the two supply voltages directly on the PCB, from the input source. In this way, beside the external FPGA, the system is autonomously powered.

A compact solution to this requirement is the dual output DC-DC power supply Cui Inc. PRQ3W-Q48-D55-S[19]. The DC-DC converter steps down the input voltage (from 18 V to 75 V) to two isolated output voltages, 5 V each. The current capability for each output is 300 mA, which must be proved to be enough to supply the various ICs.

For the input side, the maximum absorbed current includes the following contributions:

[19] `https://www.mouser.it/datasheet/2/670/prq3w_s-1889826.pdf`.

- the input gate driver (quiescent and averaged driving current):

$$I_{\mathrm{GD}} = I_{\mathrm{quiescent}} + 2 f_{\mathrm{sw,max}} C_{\mathrm{gs}} V_{\mathrm{CC}} \approx 17.5\,\mathrm{mA}\,;$$

- the voltage sensor supply current (input side): 15 mA;
- the comparator supply current: 8.5 mA;
- the digital isolator supply current (input side): 1.9 mA.

The current absorbed by the input 5 V supply is around 43 mA overall, far below the 300 mA limit of the converter.

At the output side, the maximum current absorbed by the 5 V supply only consists of the quiescent and working currents of the gate drivers. As a result, the maximum required current is around 17.5 mA, once again far within the limit. As a consequence, the dual output DC-DC converter is capable of satisfying the supply requirements for all the ICs of the system.

It may be interesting to estimate also the current absorbed by the FPGA supply, to understand whether its output current is within the limits. The overall currents consists of the gate drivers input supply currents (2.5 mA each), the output side supply current of the voltage sensor (11 mA), the current sensor supply current (6 mA), the output side isolator current at 1 Mbps (1.1 mA). The total current is around 26 mA, far below the 1.5 A limit specified by the Terasic De1-SoC FPGA reference manual[20].

The not-yet mentioned components (connectors, bypass capacitors, resistors) were selected mainly according to the voltage and/or current ratings. Tab.7.3 reports the main components adopted in the final bill of materials.

7.2 PCB design

7.2.1 PCB schematic view

Altium Designer[21] was adopted as the design tool for both the schematic and layout views of the PCB prototype. This tool was selected among other choices for the intuitive user interface, the integration of both schematic and layout views windows

[20] `http://www.ee.ic.ac.uk/pcheung/teaching/ee2_digital/DE1-SoC_User_manual.pdf`.

[21] `https://www.altium.com/it/altium-designer`.

Component	Part code	Manufacturer
Half-bridge and rectifier MOSFETs $M_{1,6}$	TPH4R10ANLL1Q	Toshiba
Gate drivers	ADUM3223WARZ	Analog Devices
Resonant inductor L_r	IHLP5050CEERR33M01	Vishay
Dividing capacitors C_1/C_2	C1812C944J5JLC7805	KEMET
Input capacitor C_{in}	UCZ1J751MNS1MS	Nichicon
Output filter inductor L_f	74437529203470	Würth Elektronik
Clamping diodes D_1/D_2	V8PAL45HM3_A/I	Vishay
Comparator	LT1394IS8#PBF	Analog Devices
Digital isolator	ISO7810DWR	Texas Instruments
Isolated voltage sensor	ACNT-H87A	Broadcom
Isolated current sensor	TMCS1100A3QDRQ1	Texas Instruments
Isolated DC-DC converter	PRQ3W-Q48-D55-S	Cui Inc.

Table 7.3: List of the main components of the final BOM.

inside a single environment, and the possibility to build a BOM directly importing the components models from Mouser.

Figs.7.5-7.8 show the four pages of the complete schematic view of the PCB. The schematic is split into four pages for readability and according to a functional division.

Sheet 1 (Fig.7.5) reports the input half-bridge MOSFETs driven by the corresponding dual-output gate driver, *IC1*, and the dividing capacitors network connected to the clamping antiparallel Schottky diodes. The floating supply voltage for the high-side MOSFET is obtained through a bootstrap network consisting in Schottky diode *D3* and capacitors *C4* and *C5*. At the input side, the *DISABLE* pin, freezing both the outputs to a "low" state when active, is kept to ground to skip this functionality. It is important to notice the absence of external gate resistors, normally included in the gate trace to avoid too high pulse currents during the MOSFETs switching, which may be unbearable for the gate driver. This limiting resistor is not necessary bacause of the relatively low driving voltage of the MOSFETs (5 V), and because the sum of the output resistance of the driver and the internal gate resistance of the MOSFET is around 2.4 Ω (minimum value), sufficient to limit the pulse current below the peak 4 A allowed by the gate driver. Zener diodes *Z5* and *Z6* ($V_{\text{Z}} = 15\,\text{V}$) are connected between source and gate of the MOSFETs to protect them from overvoltages. Their Zener voltage is selected considering the maximum gate-source voltage of the MOSFETs (20 V).

Sheet 2 (Fig.7.6) reports the rectifier side of the circuit. The two legs of the full-bridge rectifier, equipped with the gate drivers, replicate in a modular way the same structure of the input half-bridge, with the difference that the gate drivers are fed by voltage VCC_OUT, referenced to the battery ground.

Sheet 3 (Fig.7.7) reports multiple sections of the complete schematic concerning the supply voltages generation (the dual output DC-DC converter in the upper-left side), and the interfaces with external systems. These include the connection with the source terminals through connectors *J1* and *J2*, with the battery through connectors *J3* and *J4*, and the two interfaces with FPGA *Altera De1-SoC* (through *J5* and *J6*). The 2x20 header is compliant with the two GPIO expansion headers available on the FPGA and is responsible for carrying digital signal from and to the FPGA, while also providing the VDD supply. The 1x4 header is instead added to collect the analog signals from the input current and voltage sensors: these are meant to be connected to dedicated pins of the FPGA equipped with internal ADC. The power side of the current sensor (*IC7*) is connected in series with the positive terminal of the source. Its *VREF* pin is set to ground to select the unipolar current range.

Finally, sheet 4 (Fig.7.8) represents the sections of the schematic devoted to the acquisition of $v_{\mathrm{DS},2}$ and V_{in}. Actually, as described, for the ZVS-tracking control only the polarity of the first voltage is required, while the analog value of the second is necessary for the MPPT scheme. This fact results in the considerable difference between the two acquisition chains. The drain-source voltage of M_2 is clamped by Zener diode *Z7* and feeds the input of the comparator *IC5*. Its *Latch Enable* pin is connected to the gate trace of M_2 to freeze the output when required, as already described. The digital isolator *IC4* simply buffers the comparator output, decoupling the power domains. The input voltage, on the other hand, feeds the input of voltage amplifier *IC6*, after being properly scaled down to be adjusted to the input dynamics. The isolated voltage amplifier provides a unitary gain between input and differential output.

Throughout all the schematic sheets, testpoints have been located along the most meaningful power and digital signals of the circuit, to allow their monitoring with an external oscilloscope.

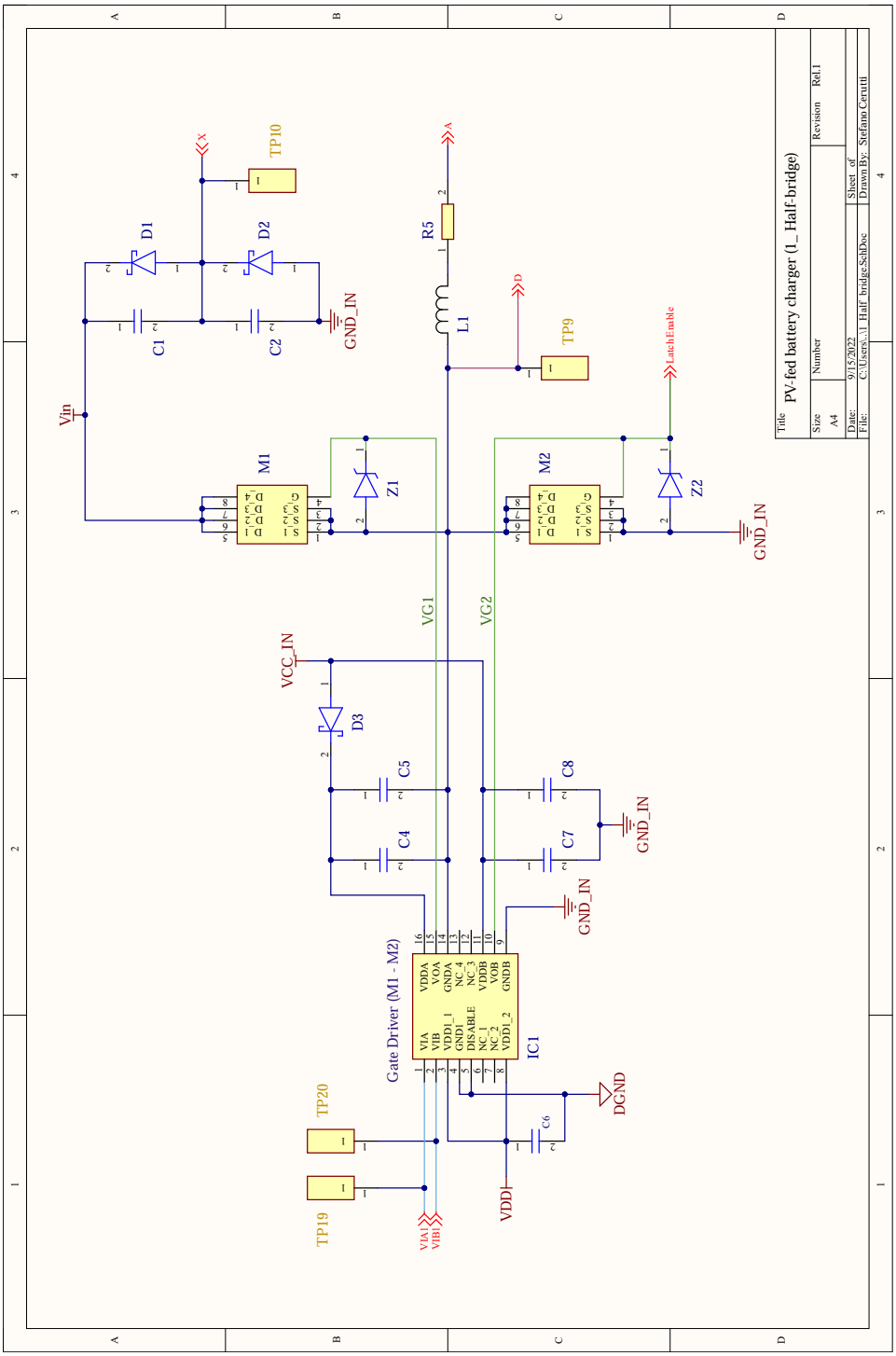


Figure 7.5: Sheet 1 of the *Altium Designer* schematic view (*Half-bridge*).

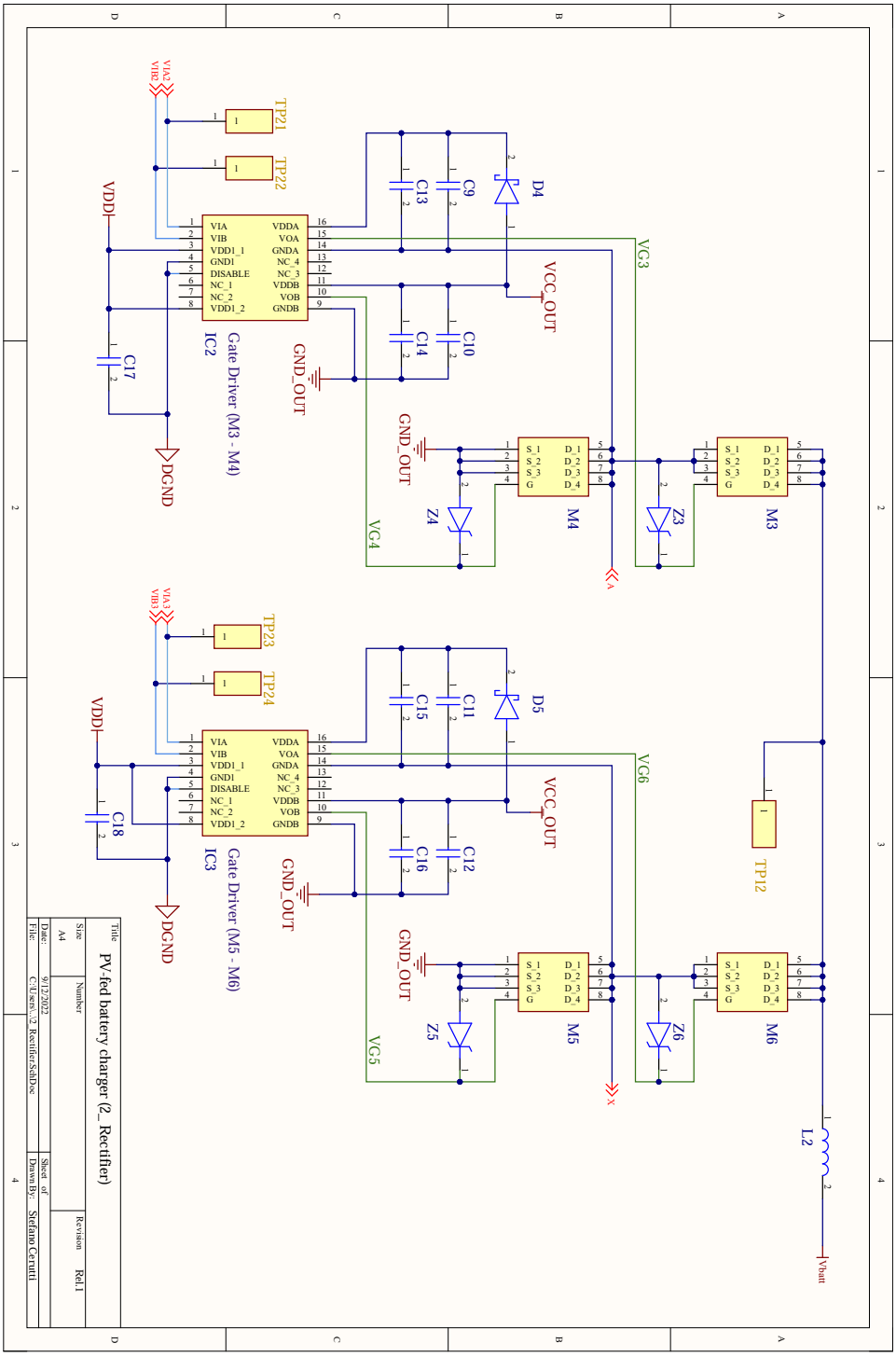


Figure 7.6: Sheet 2 of the *Altium Designer* schematic view (*Rectifier*).

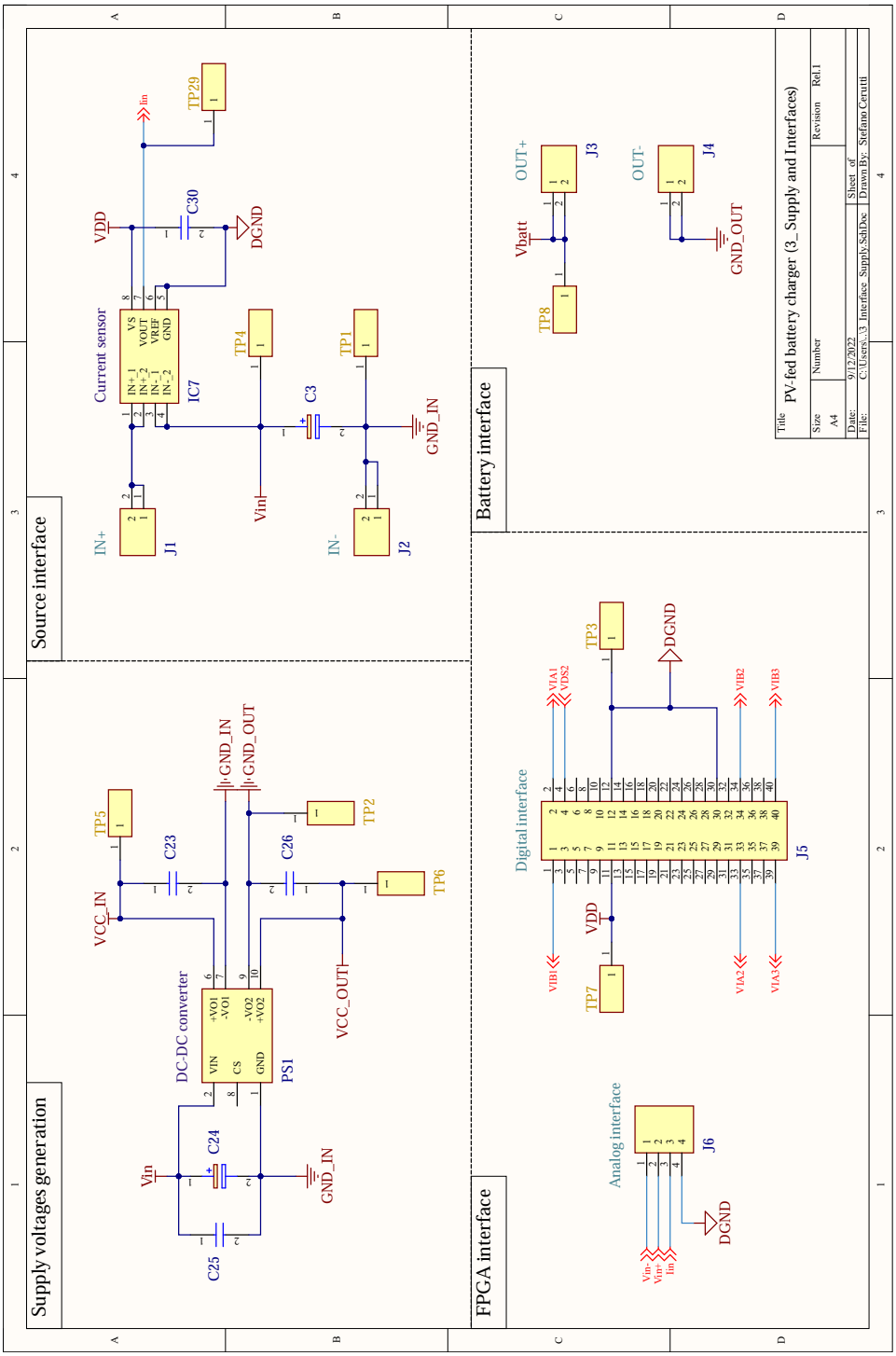


Figure 7.7: Sheet 3 of the *Altium Designer* schematic view (*Supply and interfaces*).

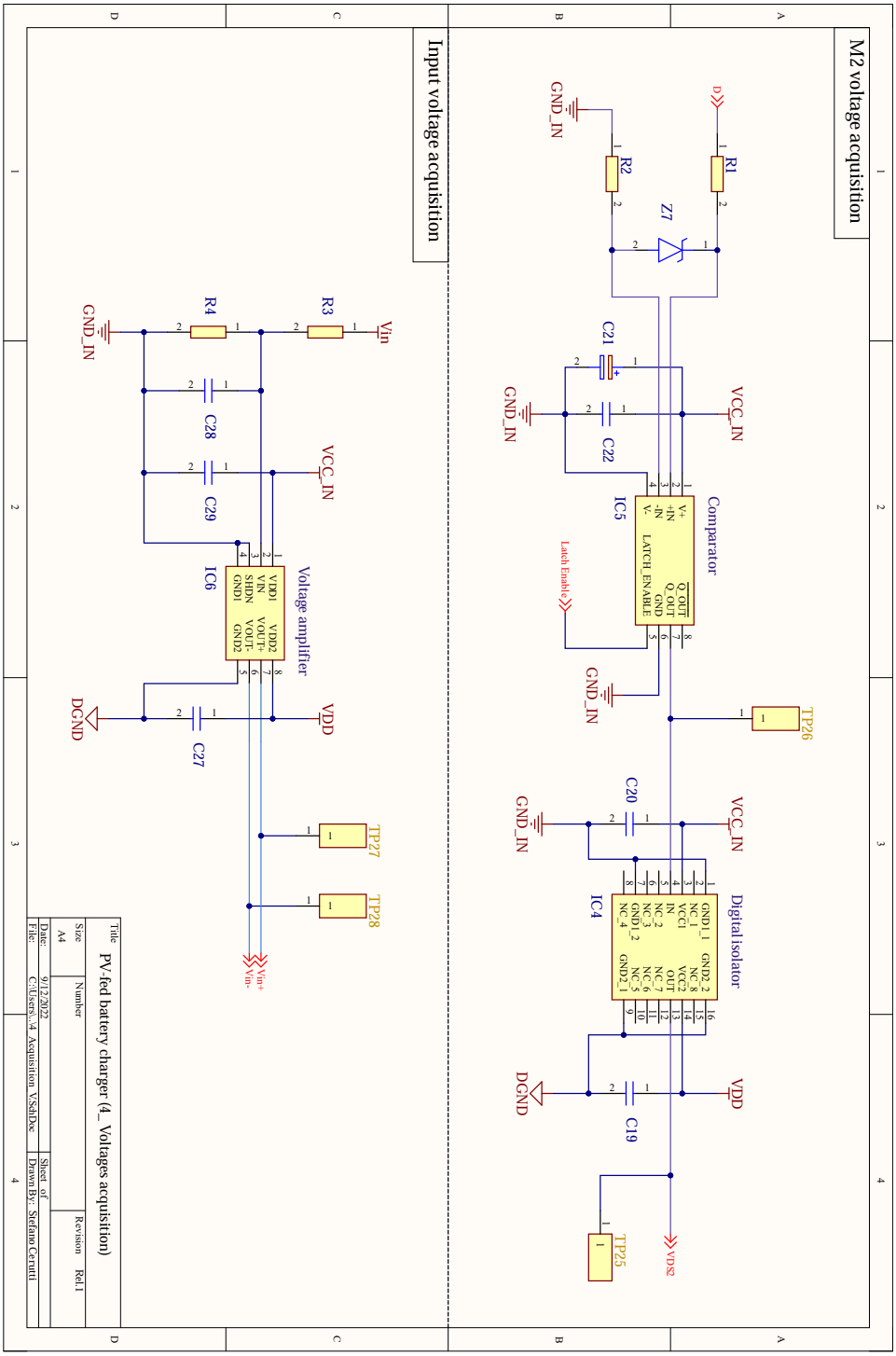


Figure 7.8: Sheet 4 of the *Altium Designer* schematic view (*Voltages acquisition*).

7.2.2 Layout design

In this section, the final designed PCB layout on *Altium Designer* is presented and described in its main design criteria. To speed up the design process and the error debugging, the design rules were imported from Eurocircuits at the beginning of the layout design. The design rules refer to the *pattern class* 6 and *drill class* C[22], and to a 2-layer, 1.55 mm-thick PCB.

The following list reports the main design criteria adopted for proper layout planning, components placing and trace routing;

1. the layout was planned to separate as much as possible the input, output and digital power domains. The ground planes were extended in the bottom layer in such a way to provide a reasonably straight and large return path for the currents, and to avoid copper isles;

2. the minimization of MOSFETs gate trace loops was a priority design criterion, to minimize the effect of stray inductances that may cause switching ringing. The configuration

3. the two inductors of the power circuit were located far from critical low power traces, to minimize interferences, and above copper cut-outs, to prevent the formation of eddy currents in the bottom ground planes;

4. traces carrying high-speed digital signals were routed as straight as possible, and entirely on the top-layer. As a more general rule, slower signals were moved to the bottom layer when in presence of unavoidable intersections with faster ones, to limit the impact of the stray inductances of VIAs;

5. the analog outputs of the current and voltage sensors were located far from the high-frequency switching power nodes;

6. the width of the traces was also selected according to the expected current, preferring thinner traces (0.2 mm) for digital and analog signals, and up to few millimeters for large current power traces;

7. to ensure a direct connection with the FPGA GPIO expansion header (male pins), the female side of the 2x20 connector was located in the bottom layer;

8. for convenience, the source and battery side connectors were placed at the opposite edges of the PCB, and as far as possible from the FPGA connector.

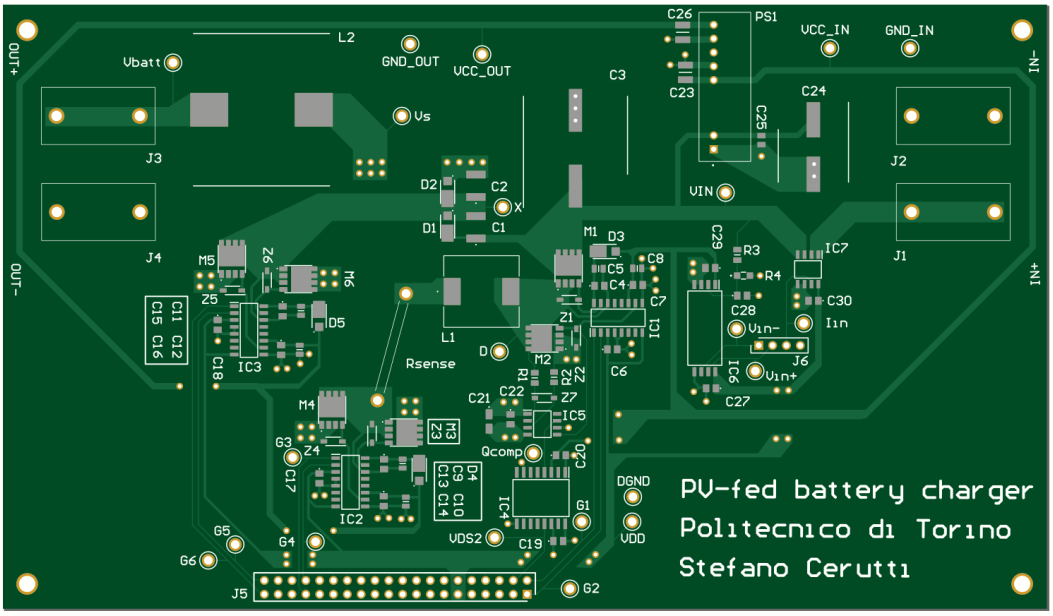
[22] `https://www.eurocircuits.com/pcb-design-guidelines/classification/` (accessed on 15/09/2022).

External spacers are meant to be screwed to the mounting holes on the uncostrained corners of the PCB, to provide mechanical support and balance to the PCB.

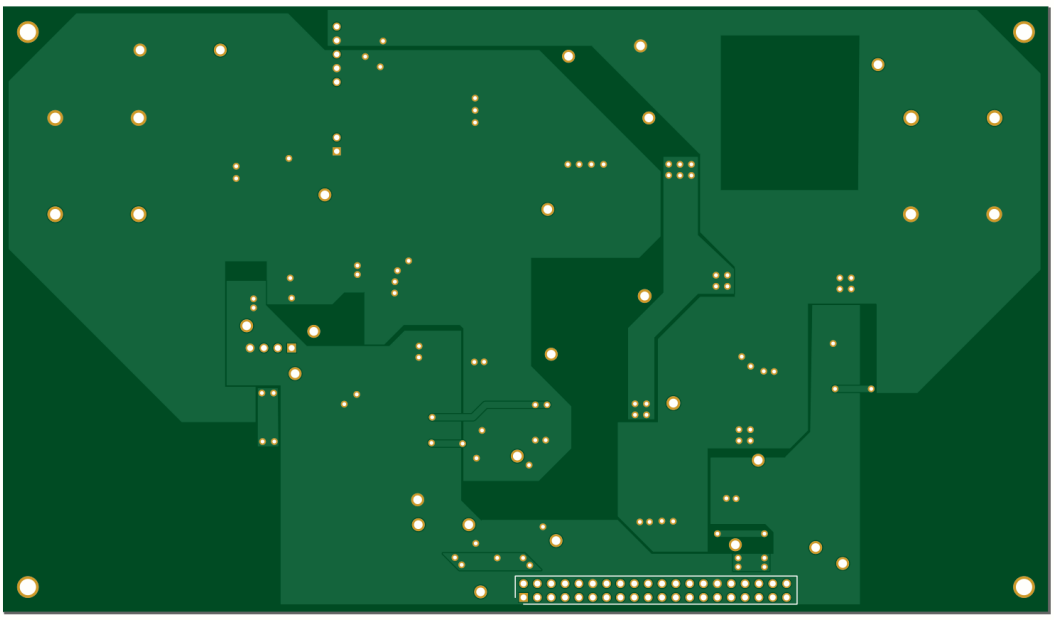
Fig.7.9 shows the appearance of top and bottom sides of the final PCB layout. The images clearly show that all the components and traces were located in the top layer: the bottom layer only includes the 2x20 header, the ground planes and few segments of traces in correspondence of unavoidable intersections.

For a better readability, Fig.7.10 shows again the top side view of the PCB layout, but highlighting clusters of components according to their functionality. The image shows the modularity of the three half-bridge legs with the relative gate drivers (red squares). The repeated configuration, as mentioned, was selected to minimize the gate traces length, and also to separate the digital and power domains. Moreover, it displays the designed solution for the placement of the dual-output DC-DC converter, *PS1*. In order to avoid intersections with high current traces, the two 5 V traces are routed along the borders of the PCB, above the corresponding power planes, and then extended to the ICs needing supply. Every supply pin of the ICs is equipped with at least one bypass capacitor, which should help maintaining a stable voltage despite the switching noise of the DC-DC converter.

Finally, Fig.7.11 reports the 3D view of the expected appearance of the PCB, equipped with the 3D models of the components, when available.



(a) Top side PCB view.



(b) Bottom side PCB view.

Figure 7.9: Top and bottom sides of the PCB layout view.

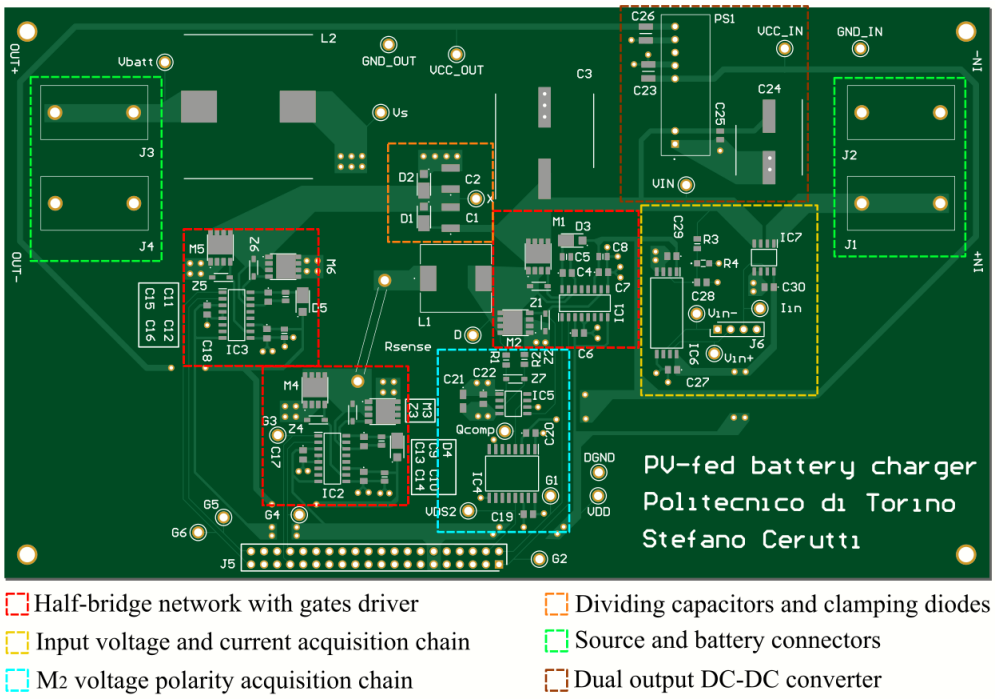


Figure 7.10: Top side PCB view with highlighted clusters of components.

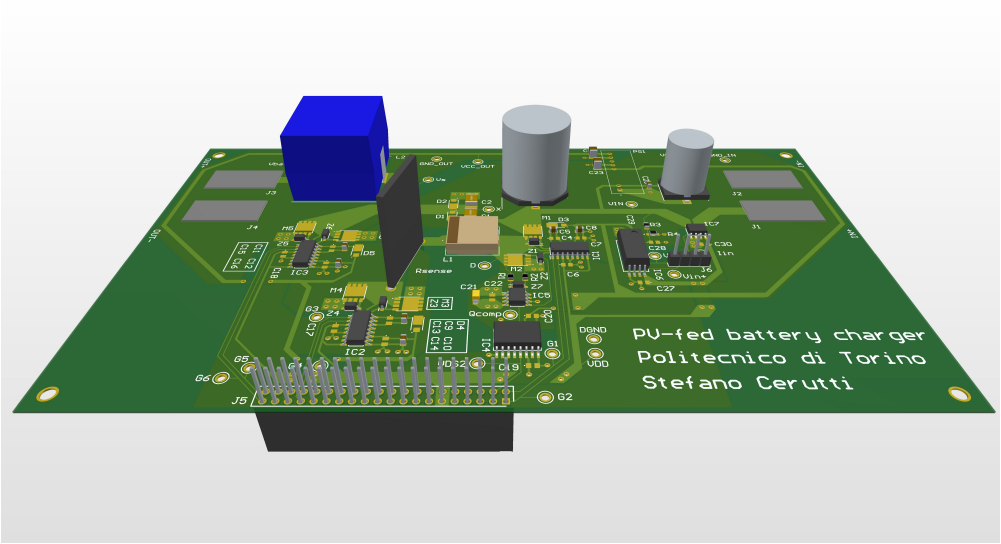


Figure 7.11: 3D view of the designed PCB.

Chapter 8

Conclusions

This work has proposed the analysis, design and implementation of a novel low-voltage battery charger in which a resonant inductor is exploited to assist the soft-switching of the main MOSFETs. At the beginning of the work, a literature review outlined the current state of the art of PV-fed microinverters, comparing resonant and non-resonant, single and dual stage topologies. The literature review helped identifying the main solutions (from the points of view of topology, technology and control) to achieve a high conversion efficiency on a wide input voltage range, necessary condition for an effective MPPT. A dominant design doesn't seem to emerge in this application field: most of the converters presented in the literature review are able to overcome the 96% efficiency peak relying on various solutions for stepping-up the input voltage.

A second literature review on resonant low-voltage battery chargers highlighted a more significant margin of improvement. The presented converters rely on resonant networks to assist the soft switching of the main switches, but are not designed for the interface with a PV panel. A single converter explicitly addresses this point, but relying on a dual stage topology that includes a conventional PWM boost. This research started from the single DC-DC stage battery charger in [38] to develop a novel frequency-modulated converter with improved efficiency and with the additional feature of the interface with a PV source. The starting topology, indeed, exhibits the desirable feature of ZVS of the input MOSFETs, and an intrinsic output power limitation to avoid overcharging the battery.

This work proposes two derived solutions, which differ in the value of the resonant inductance and in the nature of the output filter (inductive/capacitive). A full mathematical description is presented for both the topologies to detail the working operation within a switching cycle, and approximated models are derived to predict the static characteristic $P_{\mathrm{out}}(f_{\mathrm{sw}})$. The analysis allowed to outline, among other features, the necessary condition to be satisfied for a net power transfer from the source to the battery ($V_{\mathrm{in}} > 2V_{\mathrm{batt}}$) and the influence of the inductance value on the

available time window for the ZVS of the input MOSFETs. The first condition sets at 48 the minimum number of series-connected cells of possible PV panels suitable for this application: this constraint is necessary to set the GMPP at voltages above 24 V.

In order to improve the conversion efficiency, both topological and control solutions were explored: the passive rectifier in [38] was replaced by an active one, and a novel control algorithm was developed, for both the topologies, to track in real-time the ZVS condition of the input MOSFETs, and the ZCS condition of the rectifier MOSFETs. An adaptive-step Perturb & Observe MPPT scheme was also designed and implemented in *Simulink*. For the modelling of the PV source, the Single-Diode Model was applied to fit the electrical characteristic of a commercial 48-cell PV module; a simplified Thevenin equivalent circuit was instead adopted for the output battery, whose accurate modelling was out of the scope of this work.

The simulation results obtained in *LTSpice XVII* and *Simulink/PSIM* environments allowed to test the effectiveness of the control in ensuring the soft-switching condition at various irradiance operations, and tracking the MPP whenever possible. It was proved that the PV source characteristic, the battery voltage and the components selection of the converters impact the possibility to track the MPP in any irradiance condition. The converters were simulated in standard working operations defined in IEC 62509:2011 and EN 50530:2010 and compared on the basis of the EURO efficiency (higher than 97% in both the topologies) and charging efficiency (reaching 98% peaks in both). At higher power conditions, the use of a larger inductance and the larger RMS currents of the series-resonant operation decrease the efficiency of the SR topology, which was then discarded for a prototype implementation.

In the last part of this work, a complete design procedure for the main components of the power and control sections is proposed, also on the basis of the analysis of the share of losses from the simulation results. Finally, the schematic and layout views of a 100 W PCB prototype are described.

In conclusion, the innovation potential of this work consists in the combination of multiple design choices to realize a high-efficiency charging process from a PV source. This research investigation is meant to proceed in a PhD thesis project at Politecnico di Torino, during which the experimental validation of the PCB prototype will be carried out. The future steps of this research consist in the FPGA implementation of the control scheme and in the experimental testing of the complete system, aiming at the validation of the expected performances obtained in the simulations. A physical testing can also outline eventual limitations linked to the non-idealities of PV source and battery, only partially considered until now. The experimental results will be compared with the performances of the existing battery chargers of the state of the art, on the basis of the charging

efficiency and power density. The experimental phase is expected to set the basis for further improvements of this topology by outlining eventual deficiencies. Hopefully, this work will contribute to explore new possibilities in the field of PV-fed high-efficiency battery chargers, in perspective of more and more sustainable ways for the generation and distribution of electrical power.

Appendix A

Matlab codes

```
function G = SDM_system(P, Isc, Voc, Impp, Vmpp, Vt, Ns, V_exp, I_exp)
% Generates a system of 5 non-linear equations in 5 unknowns
% Legend: P=[Iph, Is, Rshunt, Rs, eta]

Area=-0.5*Isc+sum(I_exp);

% Computation of the parametric expression exploited in the fifth equation
F=0;
for k=1:length(V_exp)
    F=F+P(1)-P(2)*(exp((V_exp(k)+P(2)*I_exp(k))/(P(5)*Ns*Vt))-1)-1/P(3)*(V_exp(k)+P(4)*I_exp(k));
end

G=[Isc-P(1)+P(2)*(exp(Isc*P(4)/(P(5)*Vt*Ns))-1)+Isc*P(4)/P(3);
    P(1)-P(2)*(exp(Voc/(P(5)*Ns*Vt))-1)-Voc/P(3);
    Impp-P(1)+P(2)*(exp((Vmpp+Impp*P(4))/(P(5)*Ns*Vt))-1)+(Vmpp+Impp*P(4))/P(3);
    Impp-(Vmpp-Impp*P(4))*(P(2)/(P(5)*Ns*Vt)*exp((Vmpp+Impp*P(4))/(P(5)*Ns*Vt))+1/P(3))
    Area+0.5*Isc-F];
end
```

Listing A.1: Function for the generation of the system of 5 non-linear equations in five unknowns.

```
function F = PV_characteristic(Ipv, Vpv, Iph, I0, Rs, Rshunt, Ns, eta, Vt)
% Implicit-form equation describing the IV characteristic of a PV panel given the parametres of the single-diode model

F=Ipv-Iph+I0*(exp((Vpv+Rs*Ipv)/(eta*Ns*Vt))-1)+(Vpv+Rs*Ipv)/Rshunt;
```

```
end
```

Listing A.2: Function for the definition of the implicit equation describing the IV-curve of the panel in the single-diode model.

```
%% PV panel 5 parametres equivalent circuit derivation

% Experimental data from the IV characteristic (STC)
Vin=[linspace(0,29,30), 29.77];
Iin=[5.8*ones(1,23), 5.7, 5.6, 5.2, 4.5, 3.4, 2.4, 1, 0];

% Input data
Kb=1.380649e-23;
T=300;
q=1.60217663e-19;
Vth=Kb*T/q;
N=48;

% Datasheet parametres (mc-Si, 125cm2, Solar Innova: https://www.
    solarinnova.net/en/products/photovoltaic/modules/standard/
    monocrystalline/125mm/48#data)
Isc=5.78;
Voc=29.77;
Impp=5.52;
Vmpp=24.48;

%%% Evaluation of initial guesses (improved single diode model)
% Slope of the IV curve at SC
Rshunt0=300;

% Slope of the IV curve at OC (tuned iteratively)
Rs0=0.62;

% Using the OC and MPP operating points (ratio of IV equations)
eta0=(Voc-Vmpp-Rs0*Impp)/(Vth*N*log((Voc-Rshunt0*Isc)/(Rshunt0*(Impp-
    Isc)+Vmpp+Impp*Rs0)));

% Interpolation at OC/SC
Is0=(Isc-Voc/Rshunt0+Isc*Rs0/Rshunt0)/(exp(Voc/(eta0*N*Vth))-exp(Rs0*
    Isc/(eta0*N*Vth)));

% Interpolation at OC
Iph0=Is0*(exp(Voc/(eta0*Vth*N))-1)+Voc/Rshunt0;

P0=[Iph0, Is0, Rshunt0, Rs0, eta0];          % Initial guesses vector

%%% Solution of the non-linear system to derive the 5 parametres
eq=@(P) SDM_system(P, Isc, Voc, Impp, Vmpp, Vth, N, Vin, Iin);
Solution=fsolve(eq, P0);
```

```
Iph=Solution(1);
Is=Solution(2);
Rshunt=Solution(3);
Rs=Solution(4);
eta=Solution(5);

% Construction of the IV characteristic from the Single Diode Model
Vpv=linspace(0, Voc, 200);
Inum=zeros(1,200);
for k=1:200
    I_initial=2;
    equation=@(Ipv) PV_characteristic(Ipv, Vpv(k), Iph, Is, Rs,
    Rshunt, N, eta, Vth);
    Inum(k)=fsolve(equation, I_initial);
end

Vpv_RMSE=[24, 25, 26, 27, 28, 29, 29.77];
Ipv_RMSE=zeros(1,7);
for k=1:7
    I_initial=2;
    equation=@(Ipv) PV_characteristic(Ipv, Vpv_RMSE(k), Iph, Is, Rs,
    Rshunt, N, eta, Vth);
    Ipv_RMSE(k)=fsolve(equation, I_initial);
end

RMSE=sqrt(1/7*dot(Ipv_RMSE(:)'-Iin(25:31),Ipv_RMSE(:)'-Iin(25:31)));
```

Listing A.3: Matlab code for the derivation of the SDM parametres and the plot of numerical IV-curve.

```
function F = LargeLr_continuity_equations(S, Vin, Vo, Tsw, Vfd, Vfm,
    wres, wres2, C, Lr)
% System of equations useful to derive the unknowns of the Large Lr
    working
% operation

% Legend: S=[t1, t2, V1, V2, Il1, Il2]
% Assumptions: very short mode 2 (first order Taylor expansion of
% variables)
% Validity check: t2>t1, t1+t2<Tsw/2, V1,V2>0, Il2<Il1

F=[S(5)+2*C*wres2*(Vo+2*Vfd-Vin/2-S(3))*sin(wres2*S(1))
    (Vin-Vo-2*Vfd)+(-Vin/2-S(3)+Vo+2*Vfd)*cos(wres2*S(1))-Vin/2-S(4)
    1e4*(S(5)-S(6)-1/Lr*(Vo+2*Vfd-Vin/2+S(4))*(S(2)-S(1)))
    1e4*(S(2)-S(1)-(Vin+Vfm)/(Lr*S(5)*wres^2))
    Tsw/2-S(2)-1/wres2*atan(S(6)/(2*C*wres2*(Vo+2*Vfd+Vfm+Vin/2+S(4))
    ))
    (-Vo-2*Vfd-Vfm)+(Vo+2*Vfd+Vfm+Vin/2+S(4))*cos(wres2*(Tsw/2-S(2)))
    +S(6)/(2*C*wres2)*sin(wres2*(Tsw/2-S(2)))-Vin/2-S(3)];
```

```
16 end
```

Listing A.4: Function for the derivation of voltage and current waveforms in the modified larger L_r converter topology.

```
1
2 function F = static_char_LargeLr_FHA(Pout, Vbatt, r, C, fsw, wres,
      Vin)
3 % Implicit-form equation for the derivation of the static
      characteristic
4 % P(fsw) in the Large Lr topology
5
6 F=(8/pi^2*(Vbatt^2/Pout)+r)^2+1/(16*pi^2*fsw^2*C^2)*(1-(2*pi*fsw/wres
      )^2)^2-(4*Vin*Vbatt/(pi^2*Pout))^2;
7 end
```

Listing A.5: Implicit-form equation for the derivation of the static characteristic in the modified larger L_r converter topology.

Bibliography

[1] Jeffrey Sachs, Christian Kroll, Guillame Lafortune, Grayson Fuller, and Finn Woelm. *Sustainable Development Report 2022*. Cambridge University Press, 2022. DOI: 10.1017/9781009210058 (cit. on p. 1).

[2] Hania El-Kanj Baitie and Tarek Selmi. «Review of smart grid systems' requirements». In: *2015 Tenth International Conference on Ecological Vehicles and Renewable Energies (EVER)*. 2015, pp. 1–6. DOI: 10.1109/EVER.2015.7113004 (cit. on p. 2).

[3] Khalil Alluhaybi, Issa Batarseh, and Haibing Hu. «Comprehensive Review and Comparison of Single-Phase Grid-Tied Photovoltaic Microinverters». In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 8.2 (2020), pp. 1310–1329. DOI: 10.1109/JESTPE.2019.2900413 (cit. on p. 3).

[4] C. Riordan and R. Hulstron. «What is an air mass 1.5 spectrum? (solar cell performance calculations)». In: *IEEE Conference on Photovoltaic Specialists*. 1990, 1085–1088 vol.2. DOI: 10.1109/PVSC.1990.111784 (cit. on p. 10).

[5] E. V. Paraskevadaki and S. A. Papathanassiou. «Evaluation of MPP Voltage and Power of mc-Si PV Modules in Partial Shading Conditions». In: *IEEE Transactions on Energy Conversion* 26.3 (2011), pp. 923–932 (cit. on pp. 10, 11, 17, 18).

[6] Hitesh K. Mehta, Himanshu Warke, Kaushik Kukadiya, and Ashish K. Panchal. «Accurate Expressions for Single-Diode-Model Solar Cell Parameterization». In: *IEEE Journal of Photovoltaics* 9.3 (2019), pp. 803–810. DOI: 10.1109/JPHOTOV.2019.2896264 (cit. on pp. 12, 13, 15).

[7] Antony Xenophontos and Ali M. Bazzi. «Model-Based Maximum Power Curves of Solar Photovoltaic Panels Under Partial Shading Conditions». In: *IEEE Journal of Photovoltaics* 8.1 (2018), pp. 233–238. DOI: 10.1109/JPHOTOV.2017.2764488 (cit. on pp. 17, 18).

[8] Saeed H. Hanzaei, Saman A. Gorji, and Mehran Ektesabi. «A Scheme-Based Review of MPPT Techniques With Respect to Input Variables Including Solar Irradiance and PV Arrays' Temperature». In: *IEEE Access* 8 (2020), pp. 182229–182239. DOI: 10.1109/ACCESS.2020.3028580 (cit. on pp. 18, 20).

[9] Ibrahim Saiful Millah, Ramadhani Kurniawan Subroto, You Wei Chang, Kuo Lung Lian, and Bwo-Ren Ke. «Investigation of Maximum Power Point Tracking of Different Kinds of Solar Panels Under Partial Shading Conditions». In: *IEEE Transactions on Industry Applications* 57.1 (2021), pp. 17–25. DOI: 10.1109/TIA.2020.3029998 (cit. on p. 20).

[10] N. Mohan, T.M. Undeland, and W.P. Robbins. *Power Electronics: Converters, Applications, and Design (3^{th} edition)*. Wiley, 2002. ISBN: 978-0-471-22693-2 (cit. on pp. 23, 24, 26, 28, 29).

[11] M.K. Kazimierczuk and D. Czarkowski. *Resonant Power Converters*. Wiley, 2012. ISBN: 9781118585863. URL: https://books.google.it/books?id=MqZPnv47IagC (cit. on pp. 23, 24, 27, 29, 30, 104, 111).

[12] Muhammad H. Rashid. *Power Electronics: Devices, Circuits and Applications (4^{th} edition)*. Pearson India, 2014. ISBN: 9332584583 (cit. on pp. 24, 28).

[13] R.W. Erickson and D. Maksimovic. *Fundamentals of Power Electronics (2^{nd} edition)*. Springer US, 2001. ISBN: 9780792372707 (cit. on pp. 25, 29, 30).

[14] H. Bodur and A.F. Bakan. «A new ZVT-ZCT-PWM DC-DC converter». In: *IEEE Transactions on Power Electronics* 19.3 (2004), pp. 676–684. DOI: 10.1109/TPEL.2004.826490 (cit. on p. 29).

[15] E.X. Yang, F.C. Lee, and M.M. Jovanovic. «Small-signal modeling of series and parallel resonant converters». In: *[Proceedings] APEC '92 Seventh Annual Applied Power Electronics Conference and Exposition*. 1992, pp. 785–792. DOI: 10.1109/APEC.1992.228333 (cit. on p. 30).

[16] Samir Kouro, Jose I. Leon, Dimitri Vinnikov, and Leopoldo G. Franquelo. «Grid-Connected Photovoltaic Systems: An Overview of Recent Research and Emerging PV Converter Technology». In: *IEEE Industrial Electronics Magazine* 9.1 (2015), pp. 47–61. DOI: 10.1109/MIE.2014.2376976 (cit. on p. 31).

[17] Dmitri Vinnikov, Andrii Chub, Elizaveta Liivik, Roman Kosenko, and Oleksandr Korkh. «Solar Optiverter—A Novel Hybrid Approach to the Photovoltaic Module Level Power Electronics». In: *IEEE Transactions on Industrial Electronics* 66.5 (2019), pp. 3869–3880. DOI: 10.1109/TIE.2018.2850036 (cit. on p. 32).

[18] Thomas LaBella and Jih-Sheng Lai. «A hybrid resonant converter utilizing a bidirectional GaN AC switch for high-efficiency PV applications». In: *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*. 2014, pp. 1–8. DOI: 10.1109/APEC.2014.6803281 (cit. on pp. 33, 35, 36, 45–47).

[19] Matthias Kasper, Magdalena Ritz, Dominik Bortis, and Johann W. Kolar. «PV Panel-Integrated High Step-up High Efficiency Isolated GaN DC-DC Boost Converter». In: *Intelec 2013; 35th International Telecommunications Energy Conference, Smart Power and Efficiency*. 2013, pp. 1–7 (cit. on pp. 34, 35, 45–47).

[20] Dmitri Vinnikov, Andrii Chub, Elizaveta Liivik, and Indrek Roasto. «High-Performance Quasi-Z-Source Series Resonant DC–DC Converter for Photovoltaic Module-Level Power Electronics Applications». In: *IEEE Transactions on Power Electronics* 32.5 (2017), pp. 3634–3650. DOI: 10.1109/TPEL.2016.2591726 (cit. on pp. 35, 36, 45–47).

[21] Yuan Li, Joel Anderson, Fang Z. Peng, and Dichen Liu. «Quasi-Z-Source Inverter for Photovoltaic Power Generation Systems». In: *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*. 2009, pp. 918–924. DOI: 10.1109/APEC.2009.4802772 (cit. on p. 36).

[22] Christian P. Dick, Furkan K. Titiz, and Rik W. De Doncker. «A high-efficient LLCC series-parallel resonant converter». In: *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2010, pp. 696–701. DOI: 10.1109/APEC.2010.5433594 (cit. on pp. 37, 38, 47).

[23] Young-Ho Kim, Soo-Cheol Shin, Jung-Hyo Lee, Yong-Chae Jung, and Chung-Yuen Won. «Soft-Switching Current-Fed Push–Pull Converter for 250-W AC Module Applications». In: *IEEE Transactions on Power Electronics* 29.2 (2014), pp. 863–872. DOI: 10.1109/TPEL.2013.2258942 (cit. on pp. 37, 38, 47).

[24] Lin Chen, Ahmadreza Amirahmadi, Qian Zhang, Nasser Kutkut, and Issa Batarseh. «Design and Implementation of Three-Phase Two-Stage Grid-Connected Module Integrated Converter». In: *IEEE Transactions on Power Electronics* 29.8 (2014), pp. 3881–3892. DOI: 10.1109/TPEL.2013.2294933 (cit. on pp. 38, 44, 47).

[25] Chien-Ming Wang. «A novel single-stage full-bridge buck-boost inverter». In: *IEEE Transactions on Power Electronics* 19.1 (2004), pp. 150–159. DOI: 10.1109/TPEL.2003.820583 (cit. on pp. 39, 47).

[26] Shuai Jiang, Dong Cao, Yuan Li, and Fang Zheng Peng. «Grid-Connected Boost-Half-Bridge Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking». In: *IEEE Transactions on Power Electronics* 27.11 (2012), pp. 4711–4722. DOI: 10.1109/TPEL.2012.2183389 (cit. on pp. 40, 41, 45, 47).

[27] António Manuel Santos Spencer Andrade, Luciano Schuch, and Mário Lúcio da Silva Martins. «Analysis and Design of High-Efficiency Hybrid High Step-Up DC–DC Converter for Distributed PV Generation Systems». In: *IEEE Transactions on Industrial Electronics* 66.5 (2019), pp. 3860–3868. DOI: 10.1109/TIE.2018.2840496 (cit. on pp. 40, 41, 45, 47).

[28] Yu Fang and Xudong Ma. «A Novel PV Microinverter With Coupled Inductors and Double-Boost Topology». In: *IEEE Transactions on Power Electronics* 25.12 (2010), pp. 3139–3147. DOI: 10.1109/TPEL.2010.2087417 (cit. on pp. 42, 43, 47).

[29] Wu Wei-yang. «Research of Dual-Boost Single Stage DC/AC Converter based on SPWM». In: *IEEE Transactions on Power Electronics* (2007) (cit. on p. 42).

[30] Nikhil Sukesh, Majid Pahlevaninezhad, and Praveen Jain. «Analysis and Implementation of a Single-Stage Flyback PV Microinverter With Soft Switching». In: *Industrial Electronics, IEEE Transactions on* 61 (Apr. 2014), pp. 1819–1833. DOI: 10.1109/TIE.2013.2263778 (cit. on pp. 42, 43, 47).

[31] Jong-Woo Kim and Peter Barbosa. «PWM-Controlled Series Resonant Converter for Universal Electric Vehicle Charger». In: *IEEE Transactions on Power Electronics* 36.12 (2021), pp. 13578–13588. DOI: 10.1109/TPEL.2021.3072991 (cit. on p. 48).

[32] CLC/TC 82. *Battery charge controllers for photovoltaic systems - Performance and functioning*. en. Standard EN 62509:2011. 2011. URL: https://www.iso.org/standard/62711.html (cit. on p. 49).

[33] Ying-Chun Chuang and Yu-Lung Ke. «A Novel High-Efficiency Battery Charger With a Buck Zero-Voltage-Switching Resonant Converter». In: *IEEE Transactions on Energy Conversion* 22.4 (2007), pp. 848–854. DOI: 10.1109/TEC.2006.882416 (cit. on pp. 50–52, 61, 62).

[34] Ying-Chun Chuang and Yu-Lung Ke. «High-Efficiency and Low-Stress ZVT–PWM DC-to-DC Converter for Battery Charger». In: *IEEE Transactions on Industrial Electronics* 55.8 (2008), pp. 3030–3037. DOI: 10.1109/TIE.2008.921218 (cit. on pp. 50, 51, 61, 62).

[35] Ying-Chun Chuang. «High-Efficiency ZCS Buck Converter for Rechargeable Batteries». In: *IEEE Transactions on Industrial Electronics* 57.7 (2010), pp. 2463–2472. DOI: 10.1109/TIE.2009.2035459 (cit. on pp. 51, 61, 62).

[36] Ying-Chun Chuang, Yu-Lung Ke, Hung-Shiang Chuang, and Yu-Min Chen. «Analysis and Implementation of Half-Bridge Series–Parallel Resonant Converter for Battery Chargers». In: *IEEE Transactions on Industry Applications* 47.1 (2011), pp. 258–270. DOI: 10.1109/TIA.2010.2091613 (cit. on pp. 51, 52, 60–62).

[37] Yu-Lung Ke, Ying-Chun Chuang, Mei-Sung Kang, Yuan-Kang Wu, Ching-Ming Lai, and Chien-Chih Yu. «Solar power battery charger with a parallel-load resonant converter». In: *2011 IEEE Industry Applications Society Annual Meeting*. 2011, pp. 1–8. DOI: 10.1109/IAS.2011.6074300 (cit. on pp. 52, 53, 60–62).

[38] N.K. Poon, B.M.H. Pong, and C.K. Tse. «A constant-power battery charger with inherent soft switching and power factor correction». In: *IEEE Transactions on Power Electronics* 18.6 (2003), pp. 1262–1269. DOI: 10.1109/TPEL.2003.818823 (cit. on pp. 53, 54, 59–65, 67–69, 76, 84–86, 95, 98, 181, 182).

[39] N.K. Poon and M.H. Pong. «Computer aided design of a crossing current resonant converter (XCRC)». In: *Proceedings of IECON'94 - 20th Annual Conference of IEEE Industrial Electronics*. Vol. 1. 1994, 135–140 vol.1. DOI: 10.1109/IECON.1994.397765 (cit. on p. 55).

[40] A. Bucher and T. Duerbaum. «Extended first harmonic approximation in case of LLCC converters with capacitive output filter». In: *Melecon 2010 - 2010 15th IEEE Mediterranean Electrotechnical Conference*. 2010, pp. 1303–1308. DOI: 10.1109/MELCON.2010.5475963 (cit. on p. 111).

[41] *EN 50530:2010: Overall efficiency of grid connected photovoltaic inverters*. Avenue Marnix 17, B - 1000 Brussels: CSN, 2010 (cit. on pp. 134, 164).

[42] *IEC 62509:2011: Battery charge controllers for photovoltaic systems - Performance and functioning*. Avenue Marnix 17, B - 1000 Brussels: CLC, 2011 (cit. on pp. 134, 149).

[43] Shin-Li Lin, Gwo-Bin Wu, Wei-Chen Liu, and Chin-Sien Moo. «Ripple current effect on output power of solar-cell panel». In: *2012 International Conference on Renewable Energy Research and Applications (ICRERA)*. 2012, pp. 1–5. DOI: 10.1109/ICRERA.2012.6477439 (cit. on p. 158).

[44] Ahmad Elkhateb, Nasrudin Abd Rahim, Jeyraj Selvaraj, and Barry W. Williams. «The effect of input current ripple on the photovoltaic panel efficiency». In: *2013 IEEE Conference on Clean Energy and Technology (CEAT)*. 2013, pp. 478–481. DOI: 10.1109/CEAT.2013.6775680 (cit. on p. 158).

[45] *How to calculate ENOB for ADC dynamic performance measurement*. Application Note 6854. Maxim Integrated Products, Inc., 2019 (cit. on p. 166).