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Growth and Characterisation of in-plane Ge/Si core/shell nanowires

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Abstract

This work is focused on the development of a platform that can easily accommodate semiconductor spin Qubits. Among all the semiconductor materials, germanium (Ge) appears to be particularly suitable for this role. Parameters, such as high hole mobility, zero nuclear spin and strong spin-orbit interaction, are fundamental for this application, and Ge posses all these characteristics. Within this thesis, in-plane Ge/Si core/shell nanowires (NWs) grown with selective area growth (SAG) technique via MOVPE were studied. Crucial is the need of epitaxial and defects-free NWs, to minimise scattering and recombination sites. Several Ge core NWs grown at different growth parameters and fabrication method were compared using characterisation methods (principally SEM and TEM). NWs were then capped with a thin layer (nominally 5 nm) of Si, to protect the core and induce at the interface the type II band alignment. The Ge/Si interface and the cap crystal quality were investigated. At last, thought four-point measurements, some considerations regarding the NWs transport properties of both bare and capped NWs were discussed.

Keywords: Spin Qubits, Germanium, Ge/Si core/shell nanowires, MOVPE, Selective Area Growth, Surface passivation.

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Summary

Introduzione

L'implementazione di computer quantistici è una delle maggiori sfide che il mondo scientifico si trova ad affrontare al giorno d'oggi. Infatti, gli algoritmi di calcolo stanno diventando così complessi che con la computazione classica non possono essere risolti in tempi ragionevolmente brevi, ma addirittura in diversi anni con un notevole consumo di energia [1]. Un'ulteriore miniaturizzazione dei chip non è più tecnologicamente pensabile in quanto ci stiamo avvicinando al limite delle dimensioni dell'atomo, dove i fenomeni quantistici non possono più essere trascurati.

Una delle soluzioni proposte dai ricercatori ricade sull'informatica quantistica, che sfrutta, come unità elementare, il qubit (Qbit). La novità dei Qubit, rispetto ai classici bit, sta nel principio di "superposizione", ovvero possono contemporaneamente occupare gli stati "0" e "1" [2].

Ma cosa può essere un Qbit? I Qbit possono essere realizzati utilizzando materiali superconduttori, ioni isolati, singoli fotoni, difetti nella struttura cristallina o semiconduttori. In particolare, questa ultima categoria è studiata nell'ambito di questo progetto di tesi. I Qbit a semiconduttore consistono nell'andare ad isolare un singolo elettrone (o una lacuna) all'interno di un materiale semiconduttore, formando localmente un "quantum dot" (QD). Il valore dello spin dell'elettrone (o della lacuna) isolato è utilizzato per definire i due stadi computazionali: "up" (1) e "down" (0). Questo tipo di qubit è tipicamente chiamato "Spin Qbit". Il lavoro di questa tesi si focalizza sull'implementazione di una "piattaforma" nella quale i portatori, ed in particolare le lacune, possano essere facilmente isolate [2].

Tra i semiconduttori, i materiali più adatti per questo ruolo tra gli elementi del gruppo IV ed, in particolare, il germanio (Ge). La sua caratteristica principale che lo rende un candidato ideale per ospitare "Spin Qubit" è il suo elevato valore di mobilità delle lacune (1900 $cm^2/(V\ s)$) [3]. Tale valore è direttamente legato alla facilità di confinamento dei portatori nella struttura: maggiore è il valore della

mobilità, minore è il valore della massa efficace e, di conseguenza, maggiore sarà la possibilità di confinamento, anche per strutture di dimensioni maggiori [4]. Inoltre, il Ge, possiede la capacità di essere purificato isotopicamente per ottenere un valore di "nuclear spin" pari a zero, normalmente impossibile per i materiali III-V, che, sommato ad una bassa interazione iperfine, garantisce una elevata "coherence length" delle lacune. Infine, il Ge, mostra una forte interazione spin-orbita (SOI) per le lacune, che comporta potenzialmente un rapida velocità di calcolo [4].

Per questi motivi, le nanostrutture a base di Ge sono molto studiate ed in particolare le eterostrutture con il silicio, che non solo consentono l'ottenimento di maggiori valori di mobilità, ma rendono anche più agevole la loro implementazione nell'attuale mercato incentrato sul silicio. In questo lavoro di tesi, l'attenzione è rivolta allo studio di un particolare gruppo: Ge/Si core/shell nanowires (NWs).

Per riuscire ad isolare i portatori all'interno di un NW, è necessario modificare la struttura del classico transistor MOSFET (con "source", "drain" e "gate") andando ad aggiungere due o più gate separati come mostrato nella figura 1. In questo modo, agendo sul potenziale tra "source" e "drain", si agisce sulla formazione dei minimi di potenziale, mentre variando la tensione sugli elettrodi di gate, è possibile controllare la profondità del minimo e quindi il numero di portatori che possono entrare nel quantum dot. A temperature inferiori ai 4 K, l'energia termica è sufficientemente bassa per evitare uno scambio di portatori tra la source e il minimo del potenziale [5][6].

Idealmente, in ogni minimo energetico risiede un solo elettrone (o una lacuna) e, applicando un campo magnetico esterno, il suo spin può essere facilmente controllato, diventando un tipico qubit [5][6].

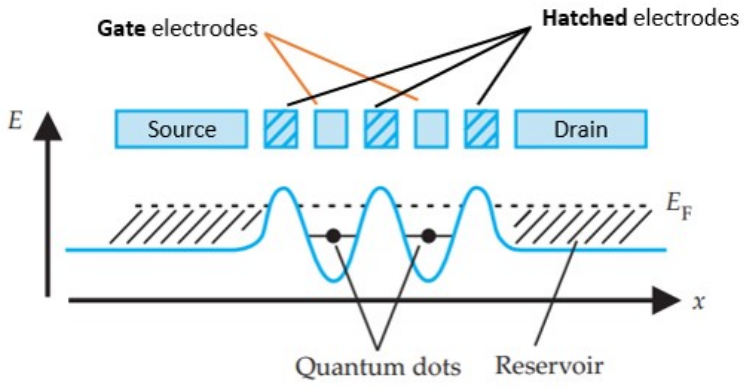


Figure 1: Esempio dell'ottenimento di due quantum dot in un nanowire. Adattato da [5].

Novità ed obiettivi della tesi

Focalizzando dunque l'attenzione sui NWs, l'attuale metodo di fabbricazione più utilizzato per ottenere tali strutture è il Vapour-Liquid-Solid (VLS). Questa tecnica, schematizzata in figura 2, consiste nel depositare una goccia di catalizzatore (tipicamente Au) di dimensioni nominalmente comparabili al diametro di interesse dei NWs e successivamente inserire dapprima i precursori per la crescita del core in Ge e poi per la shell in Si [7].

Seppur efficace, in quanto permette di fabbricare NWs fino a 30 μm di lunghezza con un buon controllo delle dimesioni del diametro (3-100 nm), questa tecnica presenta tuttavia alcune problematiche. In primis, viene utilizzato come catalizzatore l'oro che rende i NWs fabbricati incompatibili con la tecnologia dei semiconduttori a causa dell'inevitabile contaminazione presente. Inoltre, per i NWs fabbricati con questo metodo, che risultano essere "free-standing", è previsto un passaggio di "pick-and-drop" dove i NWs vengono manualmente prelevati e trasferiti sul substrato sul quale devono essere depositati (il device finale). Questo passaggio, che può solo essere fatto manualmente, riduce drasticamente la scalabilità del processo [8][7].

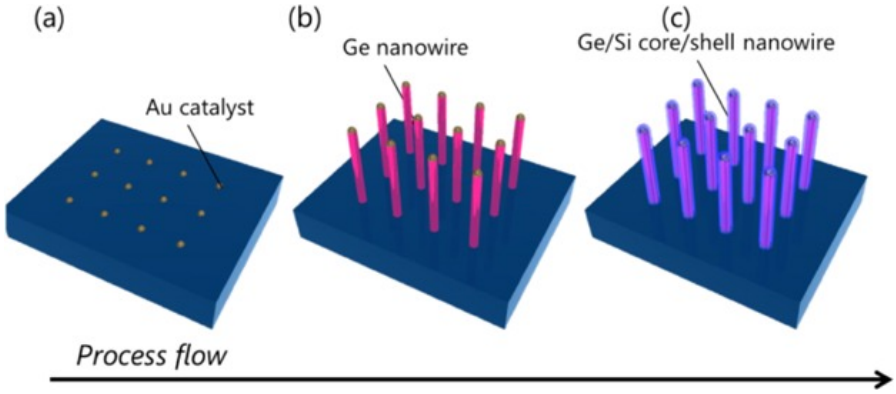


Figure 2: Ge/Si core/shell NWs fabbricati con il metodo VLS : (a) deposizione del catalizzatore (b) VLS crescita del Ge (c) ed CVD della shell di Si [7].

Selective Area Growth (SAG)

Per superare queste problematiche, molto promettente risulta essere un metodo di fabbricazione chiamato "Selective Area Growth" (SAG) per la fabbricazione di "in-plane" NWs. L'approccio SAG consiste nel depositare il materiale di interesse direttamente su di un substrato di silicio in zone prestabilite, di svariate forme e dimensioni. Così facendo, il device può essere fabbricato a partire dagli in-plane NWs prodotti. Una maschera in materiale dielettrico viene depositata su di un substrato (in Si) sulla quale, tramite l'utilizzo di tecniche di microfabbricazione,

vengono formate le aperture secondo uno specifico pattern [9]. Quindi il campione viene inserito nel reattore di crescita per ottenere il riempimento selettivo delle aperture e, di conseguenza, i NWs. Per notare una buona selettività, la maschera dielettrica deve soddisfare alcuni requisiti:

1) Termicamente stabile per resistere alle alte temperature di crescita.

2) Inerte a contatto con il gas carrier e il gas precursore nel reattore.

3) Compatibilità con le successive fasi di fabbricazione.

4) Il coefficiente di aderenza degli adatomi sulla maschera deve essere basso per ridurre la probabilità di avere nucleazioni parassite sulla maschera stessa (figura 3a) [9].

L'ossido di silicio (SiO_2) è un candidato ideale per questo ruolo.

L'approccio SAG è molto adatto per l'eteroepitassia tramite MBE, MOVPE (Metallorganico in fase di vapore) o CBE (Chemical beam epitaxy). Infatti, lo stress indotto dovuto al differente valore del parametro di cella (Si/Ge hanno una differenza di circa 4%), oltre un certo numero di layer, può portare alla formazione dislocazioni che solitamente terminano in superficie. Tali difetti abbattono le prestazioni del semiconduttore perché agiscono come centri di ricombinazione e scattering, riducendo le proprietà optoelettroniche del materiale. Grazie all'approccio SAG, le dislocazioni generate si propagano fino ad annichilirsi sul lato, all'interfaccia Ge/maschera. Questo fenomeno, chiamato aspect ratio trapping (ART), lascia la parte superiore dei NW priva di difetti (figura 3b) [10][11].

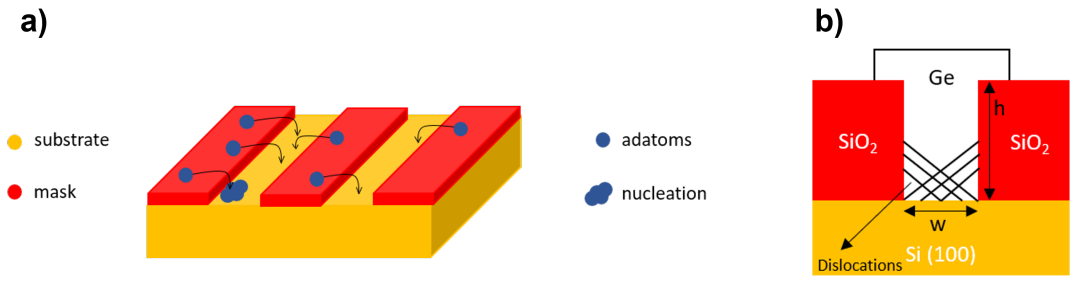


Figure 3: (a) Buon materiale scelto per la maschera: gli adatomi non si adsorbono sulla maschera ma diffondono nelle aperture (b) Schema del fenomeno dell'aspect ratio trapping (ART) [10].

Obiettivo della tesi

L'obiettivo della tesi consiste nell'ottimizzazione sia della fabbricazione del substrato, cioè tutto ciò che riguarda il processo per ottenere le aperture sulla maschera di SiO_2, sia dei parametri della crescita da precursori organici (MOVPE). In particolare, è stato studiato l'effetto dei parametri geometrici che determinano le dimensioni dei nanowires stessi, ossia la larghezza nominale delle aperture. Inoltre, solamente le due direzioni cristallografiche di crescita ad elevata simmetria sono state prese maggiormente in considerazione nello studio, <100> e <110>, in quanto nelle direzioni intermedie, per le stesse condizioni di crescita, è stata osservata una maggiore rugosità superficiale. L'obiettivo è quello di ottenere NWs con una quantità di difetti (quali stacking faults, dislocazioni e difetti planari) minimizzata, in quanto, come citato in precedenza, agiscono come punti di scattering e ricombinazione che abbattono le proprietà elettroniche.

Dopo l'ottimizzazione del core di Ge, un layer di circa 7 nm di Si è depositato sui NWs, sia per proteggerli, passivando la superficie, evitando la formazione di ossido di germanio, sia per garantire l'allineamento delle bande del tipo II che garantisce un confinamento delle lacune nel core.

Metodo

Nella figura 4 è raffigurato uno schema dl processo di fabbricazione a partire dal substrato, fino allo step di crescita nel reattore MOVPE. Tutti gli step sono stati eseguiti all'interno del CMi (EPFL cleanrrom) [12].

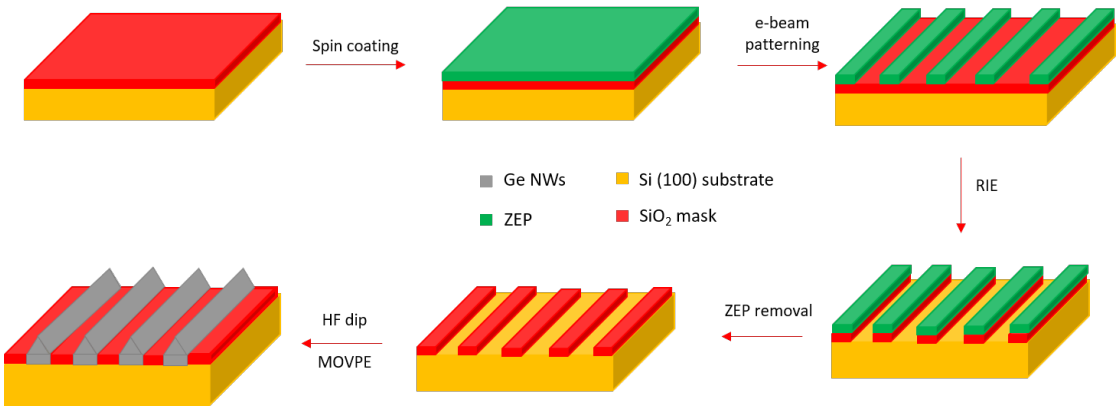


Figure 4: Schema del processo di fabbricazione

Vediamo ora, più nel dettaglio, ogni step. Innanzitutto al substrato di Si (100) viene svolto un processo chiamata "pulizia RCA" che consiste nell'andare a rimuovere

dalla superficie qualsiasi tipo di contaminante presente [12].

Una volta rimosso, il substrato è inserito in un forno dove la superficie si ossida in modo controllato andando a formare 25 nm (o 175 nm) di SiO_2 che funzionerà come maschera dielettrica nell'approccio SAG.

Lo step successivo consiste nel traferire il pattern sul wafer. Tra le varie tecniche di litografia, quella e-beam risulta essere la più adatta grazie ad un maggiore controllo delle dimensioni raggiunte. Il valore di dimesione nominale delle aperture (width), che influenza direttamente le dimensioni dei nanowires, parte da 50 nm fino a 250 nm. Naturalmente, per facilitare il confinamento delle lacune, l'obiettivo sarà di diminuire la dimensione critica.

Dunque, un layer di ZEP (un polimero a base di stirene metil acrilato) di 175 nm è depositato tramite spin-coating sulla maschera. Il fascio di elettroni dell'e-beam scansiona tutta la superfice del substrato dove è presente lo ZEP, secondo uno specifico pattern definito precedentemente da un CAD. Gli elettroni, inviati ad alta velocità sul polimero, impattano con lo stesso inducendo una rottura delle catene. La depolimerizzazione, dunque, è avvenuta solamente nei punti di interesse. Inserendo il substrato in un solvente apposito, le zone depolimerizzate vengono disciolte e rimosse.

Successivamente, il pattern impresso sul resist deve essere trasferito sulla maschera. Per farlo, è necessario uno step di etching anisotropo ("dry etching" o RIE). Il processo consiste nel collocare il campione in una camera dove viene generato un plasma che, grazie ad un campo elettromagnetico, viene accelerato e direzionato sul substrato. Il plasma è costituito da ioni reattivi che rimuovono selettivamente una specie chimica con un certo "etching rate". A questo punto, critico è il valore del tempo in cui il substrato rimane all'interno del reattore. Infatti, la velocià con cui la maschera viene rimossa dipende dall'ampiezza (width) delle aperture: aperture più grandi necessitano di tempo minore nel reattore. Nella maggior parte dei casi, il processo di RIE è stato condotto, sulla maschera spessa 25 nm, per poter ottimizzare le aperture più piccole (50 nm). Tale ottimizzazione risulta ottenuta con 23 s di etching.

Una volta trasferito il pattern sulla maschera, il resist rimanente può essere rimosso, prima con acetone e IPA e successivamente mandando sul campione del plasma ad ossigeno per 10 minuti.

Dopo questi passaggi, si ottengono le aperture desiderate nella maschera ed il

campione è potenzialmente pronto per essere caricato nel reattore MOVPE. Tuttavia, a causa dell'esposizione con l'aria, sul fondo delle aperture, è presente un layer sottile di SiO_2 naturale che deve essere rimosso per ottenere una buona interfaccia Si/Ge senza ossigeno. Per rimuoverla il campione viene immerso per 120 secondi in una soluzione di 1% HF [13].

Infine, per evitare una risuccessiva ossidazione non voluta, il campione è velocemente caricato nel reattore MOVPE.

In breve, l'epitassia da fase gassosa consiste nell'inviare precursori metallorganici della specie di interesse in un reattore dove viene posto il substrato. Ad una temperatura specifica, i gas precursori si decompongono separando la parte organica, che rimane in fase gassosa, dalle specie meno volatili che vengono adsorbite sul substrato. Gli atomi, una volta adsorbiti, si diffondono sul substrato solitamente verso i difetti superficiali (step, kinks etc.), fino a formare un cluster di nucleazione che crescerà nel tempo. La temperatura nel reattore deve essere sufficientemente alta per scindere i precursori e favorire la diffusione dei adatomi adsorbiti.

Il parametro di maggior impatto durante la procedura di crescita è la temperatura nel reattore, in quanto non solo influenza la decomposizione dell'isobutilgermanio (IBGe), ossia il precursore utilizzato, ma agisce anche sulla diffusione degli atomi di Ge, che migrano dal punto in cui sono adsorbiti, al cluster in crescita. Uno schema dei processi fisici che avvengono nel reattore e nei pressi della superficie sono raffigurati nella figura 5.

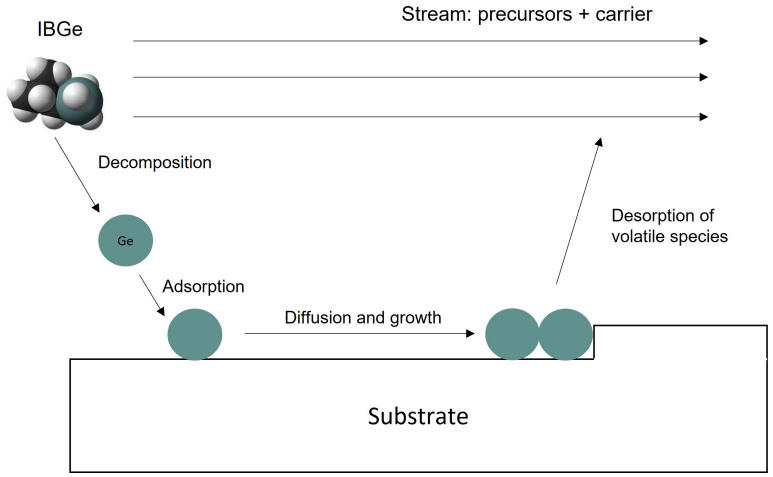


Figure 5: Schema dei processi fisici che avvengono nel reattore MOVPE.

Risultati

Uno degli obiettivi della tesi consiste nell'ottimizzazione della crescita del core di Ge per poter ridurre la concentrazione dei difetti, che si formano principalmente nei momenti iniziali della crescita. Per questo motivo, è stato preso in considerazione lo stadio di nucleazione del core di germanio all'interno delle aperture nella maschera, per investigare come essa avviene. In particolare, è stato studiato l'andamento e il meccanismo della formazione del core fissando la temperatura di crescita a 750°C e modificando il tempo di residenza all'interno del reattore. Nella figura 6a è presentata un'immagine SEM nel caso di 15 secondi di crescita, che rappresenta il primo tempo sufficiente nel quale è possibile notare al SEM i cluster di Ge.

La nucleazione avviene nella aperture ed è influenzata dalla rugosità della superficie del silicio dopo lo step di RIE durante il processo di fabbricazione del substrato. Infatti, il plasma, oltre a rimuovere anisotropicamente l'ossido di silicio, quando impatta sul substrato lascia una rugosità non trascurabile sul fondo delle aperture. Scansionando superficialmente con l'AFM sulle aperture nel momento precedente al caricamento del substrato nel reattore MOVPE, si è notata la presenza di una rugosità piuttosto marcata ($R_q = 3$ nm). Questa rugosità può essere la causa del meccanismo di nucleazione del germanio notato nell'immagine SEM, in quanto le valli presenti possono agire come sito di nucleazione preferenziale.

Dopo lo step di nucleazione, mantenendo nel reattore il substrato per più tempo, questi cluster di Ge di uniscono per formare, dopo 90 secondi di crescita, un wire continuo come mostrato in figura 6b. La temepratura di crescita impostata all'interno del reattore influisce sulla qualità finale del core di germanio. Una serie con differenti temperature di crescita è stata studiata e le immagini SEM sono rappresentate nella figura 6c. 750°C risulta essere la temperatura alla quale i NWs appaiono meno difettosi: aumentando a 775°C rugosità superficiale inizia ad essere notata, fino a 800°C dove, a causa dell'elevata temperatura, il germanio inizia a desorbirsi. A temperature inferiori di 750°C, a causa della bassa energia termica, è favorita la formazione di stacking faults che raggiungono la superficie formando dei gradini facilmente osservabili al SEM.

Alcune modificazioni al processo stesso sono state attuate per poter ulteriormente minimizzare la densità di difetti. Per esempio, a valle del processo di crescita, sempre all'interno del reattore, è stato aggiunto un "post-growth annealing" a 800°C per 3 minuti. Dalle immagini SEM e TEM e dalle analisi Raman, nessuna formazione di rugosità superficiale e/o intermixing all'interfaccia Si/Ge è stata notata, evidenziando un core con una buona qualità cristallina.

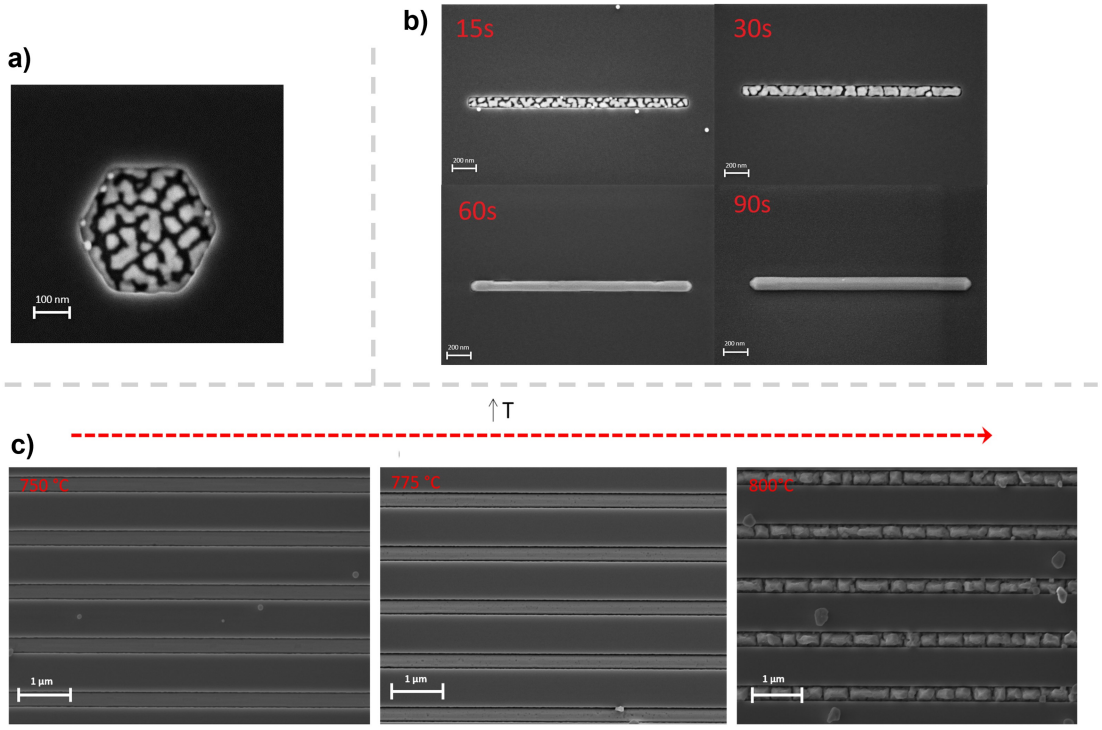


Figure 6: (a) Immagine SEM di un'apertura a forma di esagono nella maschera di SiO_2 dopo 15 secondi di crescita MOVPE. (b) Immagini SEM dello stadio di crescita di NWs con 80 nm di larghezza nominale: da 15 s a 90 s di tempo di permanenza nel reattore. (c) Immagini SEM dei NWs con larghezza nominale 200 nm nella direzione <110> cresciuti a differenti temperature: 750°C, 775°C e 800°C.

Come anticipato in precedenza, a causa di questa superficie non omogenea post-RIE, aumenta la probabilità di formazione di difetti (difetti planari, stacking faults e/o dislocazioni). Per questo motivo si è cercato di evitare la formazione di questa rugosità, in particolare ottimizzando la preparazione del substrato stesso.

Tra le vie studiate per ottenere una superficie piatta, la più promettente consiste nel depositare, sul substrato di silicio, un layer sacrificale, di circa 5 nm, di Al_2O_3 via "Atomic Layer Deposition" (ALD) che funga da "etch-stop" layer successivamente da rimuovere o con KOH o con BHF (schema del processo rappresentato nella figura 7. In questo modo, durante il processo RIE, il plasma, dopo aver rimosso la maschera, incontra il layer sacrificale, senza raggiungere il substrato di silicio sottostante. Come maschera, in questo caso, viene depositato via "Plasma Enhanced Chemical Vapour Deposition" (PECVD) 30 nm of SiN. Per entrambe le tipologie di wet etching utilizzate, in entrambi i casi la rugosità risulta essere decisamente diminuita raggiungendo valori di $R_q = 0.4$ nm (KOH) e $R_q = 0.6$

nm (BHF). La riduzione della rugosità è evidenziata grazie alle immagini 3D delle misure di AFM rappresentate in figura 7c e 7d.

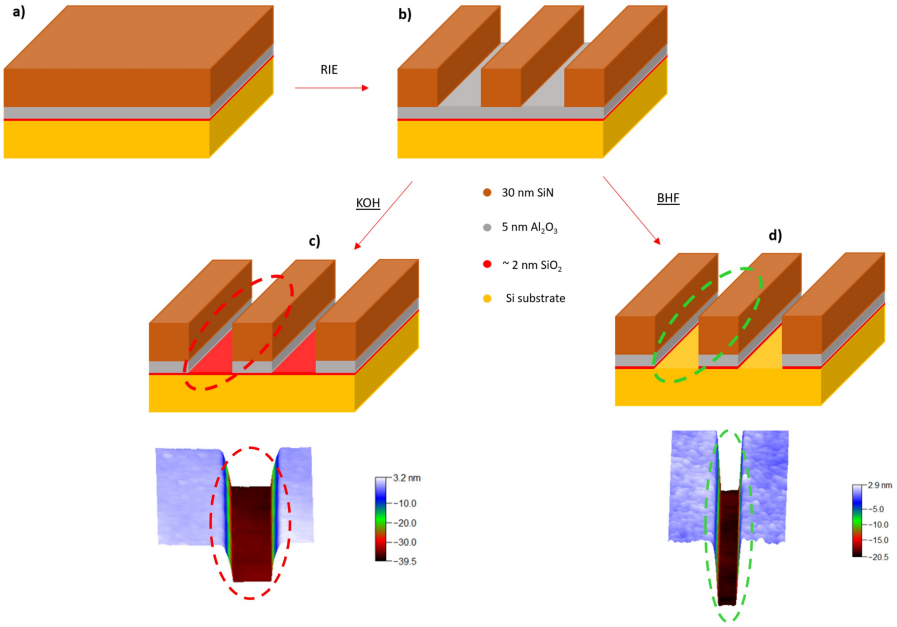


Figure 7: Schema del processo di fabbricazione utilizzato con il'introduzione dell'"etch-stop" layer. (a) Thin film di partenza. (b) Step di RIE e rimozione dell'"etch-stop" layer con (c) KOH o (d) BHF con le rispettive immagine 3D AFM che evidenzia la superficie piatta ottenuta.

Dopo aver ottimizzato la crescita del core di germanio, una shell di silicio di circa 7 nm è depositata sui NWs. Il Si ha la duplice funzione di proteggere fisicamente il germanio, evitando la sua ossidazione, e garantire un allineamento delle bande di tipo II, che favorisce il confinamento delle lacune nel core. Due differenti tipi di approccio sono stati studiati: il primo consiste nel depositare un layer sottile di Si amorfo via PECVD e successivamente cristallizzarlo con uno step di annealing a 600°C [14].

Il secondo, invece, consiste nel mantenere il substrato all'interno del reattore MOVPE e di depositare direttamente, flussando il disilano, Si cristallino sul core di Ge. Quest'ultimo approccio risulta essere quello che ha mostrato risultati preferibili [15][7]. Come mostrato in figura 8, che rappresenta una cross-section TEM-EDX di un NW con larghezza nominale di 50 nm, con l'andamento della frazione atomica lungo l'interfaccia Ge/Si, circa 5 nm di shell di Si sono stati depositati con successo. Qui la deposizione è stata compiuta a 620°C per 60 secondi e si può notare che l'interfaccia è brusca, con una quantità di ossigeno pressochè nulla, e con un elevato

contenuto di Si (circa 90%) che è tradotto con un basso intermixing tra le due specie.

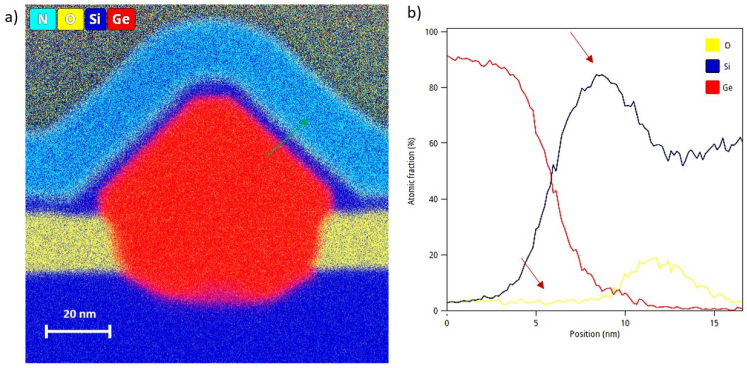


Figure 8: A sinistra, immagine TEM-EDX di un core/shell NW con 50 nm di larghezza nominale nella direzione <100>, con core cresciuto a 750°C. A destra, shell a 620°C e andamento della frazione atomica lungo l'interfaccia Ge/Si.

Conclusione e sviluppi futuri

Come accennato, lo scopo del presente lavoro è stato quello di trovare i giusti parametri sia per la fabbricazione stessa del substrato sia per la crescita epitassiale dei NWs utilizzando l'approccio SAG. Riguardo quest'ultima, i NWs di migliore qualità sono stati ottenuti a 750°C. Lo step di annealing post-crescita a 800°C potrebbe aver migliorato ulteriormente la qualità dei NWs favorendo la migrazione e annichilimento delle dislocazioni.

Aggiungendo un layer sacrificale di Al_2O_3 e sostituendo la maschera con SiN, è stato possibile ottenere una superficie di Si con una rugosità notevolemte ridotta. Su questo tipo di superficie, può verificarsi un meccanismo di crescita Stranski-Krastanov potenzialmente puro, a causa della non trascurabile differenza di valore di parametro di cella tra Ge e Si, che può comportare all'ottenimento di NWs di qualità superiore, senza formazione di stacking faults all'interfaccia Si/Ge. Inoltre, la minore velocità di crescita riscontrata utilizzando SiN come maschera è da considerare positiva, in quanto si traduce con un maggiore controllo sulle dimensioni e sulla forma dei NWs stessi. Ulteriori studi di nucleazione e crescita su questo tipo di struttura sono tuttavia necessari per poter avere un'idea più chiara del fenomeno fisico.

Inoltre, depositando direttamente nel reattore MOVPE la shell di Si a 620°C, l'interfaccia tra Ge e Si risulta essere brusca senza alcun intermixing e/o ossigeno.

Alcune misure di resistenza sono state condotte sui NWs con solo core e su NWs con la shell. I risultati mostrano che i NWs conducono e mostrano valori di resistenza comparabili dell'ordine di grandezza delle decine di kΩ.

Table 1: Valori di resistenza calcolati con il metodo a due e a quattro punti per NWs con solo core e core/shell

		Ge core		**Ge/Si core/shell**	
Orientazione	**Ampiezza nominale (nm)**	**R_{2pt} (kΩ)**	**R_{4pt} (kΩ)**	**R_{2pt} (kΩ)**	**R_{4pt} (kΩ)**
<100>	50	142	42	137	45
	80	95	34.3	114	38
	120	80	28	94	30
<110>	50	120	40	149	51
	80	100	33	138	45
	120	73	25	100	33

I valori di resistenza a due punti risultano superiori a quelli ottenuti dal test a quattro, in quanto per i primi si tiene conto della somma di un NW lungo 3 µm con le due resistenza di contatto, mentre per il secondo solamente un NW lungo 1 µm. I valori per i NWs core/shell risultano essere leggermente superiori.

Per sapere se la causa di questa discrepanza è dovuta a variazioni nella concentrazione dei carrier (lacune) e/o nella mobilità, misurazioni Hall sono necessarie. Una volta definiti e notati questi due parametri, essi vengono comparati con i risultati preliminari ottenuti da Santhanu et al. [16] utilizzando Ge NWs solo core cresciuti all'interno delle aperture e dunque "undergrown" i quali avevano notato una bassa mobilità e dunque basso "mean free path" ($\sim$400 $cm^2/(V\ s)$ e $l_e \approx 10$ nm) e un'elevata concentrazione di lacune ($\sim 5x10^{18}$ cm^{-3}) [16]. Qualora i risultati fossero promettenti, lo step successivo sarebbe quello di depositare sui NWs l'ossido di gate per formare un MOSFET-like device e studiare per quale valore di tensione applicata al gate si abbia uno svuotamento dei NWs dai carrier. Più bassa è tale tensione, più facile è il successivo isolamento delle lacune stesse per l'ottenimento dei qubits (con un minore consumo energetico).

Chapter 1

Introduction

Quantum computing and the subsequent implementation of quantum computers is one of the biggest challenge that the scientific world finds itself facing nowadays. In fact, state-of-the-art computational algorithms are becoming so complex that with classical computation they cannot be solved in a reasonable short time but even in several years with a huge energy consumption [1].

One approach to solve the situation might be to speed up the classical computation by further pushing the miniaturisation of the chips, by increment the number of transistors that can fit in a single chip. This "technological progress" is well described by the famous Moore's law. This law define the defines the increasing rate of the number of transistors during the years on integrated circuits. The number doubled more or less every 18 months [17].

However, we are approaching the limit in which a further decreases in size results in reaching the dimension of the atom and at this point, quantum phenomena are predominant. It is therefore clear that we are reaching the limit and so new technologies and new solution are needed to further improve this field.

One of the solution that scientist come up with is quantum computing where its "core" is represented by the qubit (Qbit). The novelty of the Qbits is that they can simultaneously occupy "0" and "1" state and can be somehow entangled with each other [2]. However, what can be a Qbit? Qbits can be made using superconducting materials, trapped ions, single photons, defects in the crystal structure or semiconductor quantum dots. The latter are the one studied within this project and consist in isolate a single electron (or hole) inside the semiconductor material where its spin can be switched between "up" (1) or "down" (0). These type of qubits are typically called "spin qubits" [2].

Create a platform where these carriers can be easily isolated to form qubits is therefore necessary.

The early stage of the research was conducted studying III-V materials, such gallium arsenide, as a host due to their low degree of disorder that enhance the ease of formation of well controlled local quantum dots. However, commonly III-V materials present a nuclear spin that reduce the coherence between qubits. For this reason, the research moved on materials from the group IV and, in particular, on germanium (Ge). In fact, as discussed in more detail in the Chapter 2, germanium presents very interesting characteristic and properties that place it as one of the best candidates for the role of hosting qubit, such as low disorder, high mobility, strong spin-orbit interaction, zero nuclear spin, low hole effective mass, and, most importantly, the ease of implementing germanium in the current Si-based classic chip [4].

Different Ge-based structures have been studied by researcher in the last years and the most successful turned out to be planar Ge/Si heterostructures and Ge/Si core/shell nanowires (NWs). The latter are the structures of interest within the scope of this thesis.

Chapter 2

History work and novelty

2.1 State of the Art

In this section a review of the current knowledge and technology to implement spin qubits in semiconductor will be presented. We begin by providing a brief theoretical explanation about spin qubit in semiconductor quantum dots (QDs). Then, a review of the current Ge/Si heterostructures is presented and, to conclude, the heterostrustures studied in this project are introduced: in-plane Ge/Si core/shell nanowires (NWs).

2.1.1 Spin qubits in semiconductor quantum dots

Electrons and holes in a semiconducting materials are charged particles which can be easily manipulated by applying suitable bias [5]. For instance, in the classical field effect transistor (FET) the conductivity of the channel, that is the space between the source and the drain, can be controlled by applying a specific gate voltage. In fact, by modify the gate voltage it is possible to control the amount of carriers in the channel: positive (negative) voltage attract electrons (holes) to the channel that increase the current flow, while applying a negative (positive) one, deplete the channel in a way that the source-drain current is hindered [5][6].

Now, if the classical transistor structure is modified by adding three separately biased elecrodes (hatched electrodes) as shown in 2.1, the electronic potential between the source and the drain can be tuned to form potential energy minimums where electrons (or holes in the opposite case) can be isolated [5].

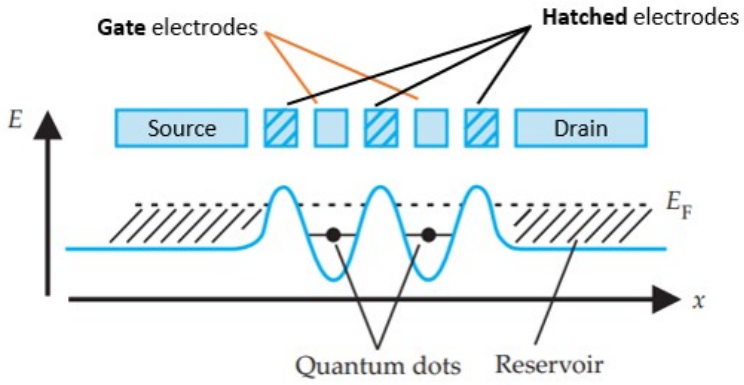


Figure 2.1: Example of a two tunnel coupled quantum dot. Adapted from [5].

At temperature below 4 K, the thermal energy is low enough to avoid carrier exchange from the "reservoir" to the potential minimum. Only a discrete number of carriers can be confined in this minimum that take the name of quantum dot (QD) in the nanowire.

By varying the the voltage on the gate electrodes it is possible to control the depth of the minimum and so the number of carriers that can fit in the quantum dot, while by acting on the voltage between the hatched electrodes, it is possible to tune the tunnel barriers [5][6]. Ideally, in every quantum dot, only one electron (or hole) resides and by applying an external magnetic field, its spin can be easily tuned becoming a typical quantum bit (Qbit) [5].

2.1.2 Ge/Si heterostructures

Among all the elements in the periodic table, germanium (Ge) turns out to be a really interesting material to host a spin-based quantum device.
Firstly, Ge and especially related Ge-based structures show one of the highest hole mobility. High mobility values are fundamental for qubits application. In fact, mobility is related to the value of effective mass (m^*) of the carrier by the following equation n. 2.1 [18][19]:

$$\mu = q\tau/m^* \tag{2.1}$$

Where q is the elementary charge of the electron (or hole), τ represent the the time between two carriers collision and μ is the carrier mobility. So, higher is the mobility, lower is the value of the effective mass of the carriers.

Low values of effective mass are a target because it correspond to a larger energy splitting in the QDs formed and, therefore, to a higher value of the De Broglie

wavelength (equation n. 2.2), that enhance the ease to confine the carrier [18][20].

$$\lambda_{DB} = h/\sqrt{2\pi m^* K_b T} \tag{2.2}$$

In the equation, h is the Plank constant, K_b is the Boltzman constant and T is the temperature. Quantum confined is observed once that the dimensions of the material is comparable to the De Broglie wavelength of the carrier. So, if higher De Broglie wavelength values can be reached, confinement can be obtained for larger structures (larger size of the quantum dots) [21].

Germanium, as a material from the IV group of the periodic table, like Si, posses the ability to be isotopically purified to obtain a value of zero nuclear spin, normally greater that zero for III-V, that summed to a low hyperfined interaction, allows to achieve long hole coherence length [16][22]. Furthermore, Ge shows a strong spin-orbit interaction (SOI) for the holes that leads to a potentially fast qubits operation. Finally, the Fermi level pinning observed when Ge is in contact with most of the metals, facilitate a carrier (holes) injection without the use of ion implantation or local doping.

For these reasons, Ge-based nanostructures are heavily studied and in particular its heterostructures with silicon. Thanks to the lattice mismatch between the two elements, when coupled together and if the layer thickness is below the critical to form defects, a compressive strain is induced in Ge. This strain further increases the hole mobility since scattering events are reduced. Moreover, strain induce splitting of the heavy hole (HH) and light hole (LH) valence band, that leads to a decrease of the effective mass (m^*) that improve the mobility once again [23][8].

These structures are typically formed by an "active layer" in Ge, where the holes are confined, and a "barrier layer" in GeSi or Si. GeSi as a barrier layer is chosen because it can bring two main advantages: firstly it facilitates the integration in the current "state-of-the-art" electronic technology based on silicon. Secondly, by varying the relative composition of the layer, it is possible to control both compressive strain induced in the active layer, and the band alignment [22].

Planar Ge/GeSi heterostructures

In the case of planar Ge-rich Ge/GeSi heterostructures the compressive-strained active layer of Ge is typically "sandwiched" by two relaxed SiGe layers, as figure 2.2 depicts. In this case, the band alignment is type I where the Ge valance band maximum is energetically at an higher level than the one in SiGe and in this way, holes will accumulate in the active layer creating a 2D hole gas (2DHG).

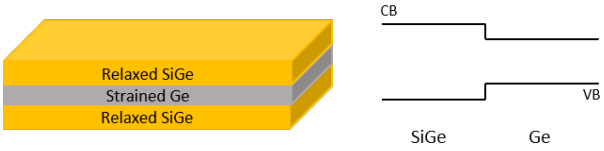


Figure 2.2: Depiction of a typical Ge/GeSi heterostructure (image not in scale) and the type I band alignment.

Ge content in the barrier layer is high (0.6-0.9) to have reasonable layer thickness (up to 30 nm) without having the formations of defects due to plastic deformation [22][8].

Besides these promising properties, some criticality where still present such as integration of the stack on Si substrates that, due to the lattice mismatch between Si and GeSi leads to increase roughness and thread dislocations density. Efforts to improve growth have been faced by engineering the substrate such as introducing a grade in the composition in the SiGe. Forward grading and reverse grading configurations have been studied and, in particular for the last one, good values of mobility (10^6 cm^2/(V s)), also for undoped structures, are obtained. These structures, in particular, are really interesting because without doping impurities there are not be leakages paths or charge noises during qubits operations (figure 2.3) [8].

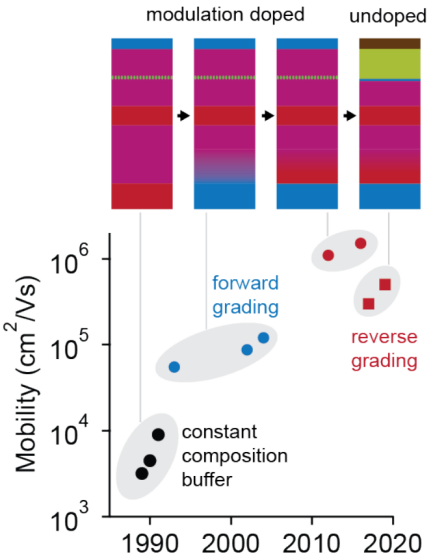


Figure 2.3: Improvement of SiGe heterostructures on holes mobility. Adapted from [8].

Ge/Si core/shell NWs

a) Out-of-plane Ge/Si NWs (free-standing)

Other interesting heterostructures are Ge/Si core/shell nanowires. These structures consist in a Ge core surrounded by a Si shell. The contact point is an abrupt Ge/Si interface, where an alignment of type II is formed (figure 2.4). In this configuration, holes are strongly confined in the Ge core while electrons will tend to stay in the Si shell. With these structures, scientist menage to achieve mobility value of 4200 $cm^2/(V\ s)$ [8].

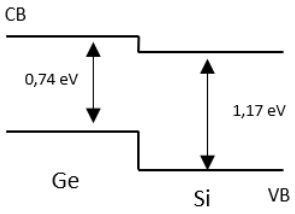


Figure 2.4: Type II band alignment in the case of Ge/Si interface.

The development and fabrication of Ge/Si core/shell NWs is typically carried out using the vapour-liquid-solid (VLS) approach. This technique is a really powerful method to grow long wires (up to 30 μm) with a specific diameter range (3-100 nm) and with a really control on the position where the nanowires grow.

However, it presents two big issues that lead to the need to explore new fabrication techniques. Firstly, Au drops are used as a catalyst to chose the nucleation site. This makes manufactured nanowires incompatible with semiconductor technology due to inevitable metal contaminations in the heterostructure. Secondly, it was observed a dependence of the NWs growth direction with the diameters values, for bigger wires, <111> direction is preferred, while for diameters smaller than 20 nm, <110> and <112> are favoured. This leads to a less versatility and control on the growth (schematic process in figure 2.5) [8][7].

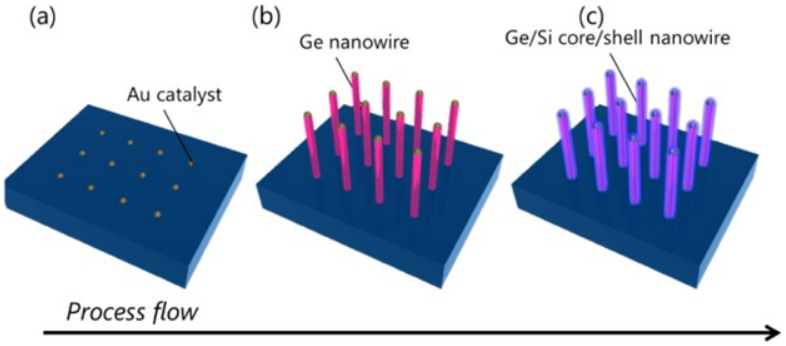


Figure 2.5: Ge/Si core/shell NWs grown with VLS method: (a) catalyst deposition (b) VLS Ge growth (c) and CVD of the Si shell. Adapted from [7].

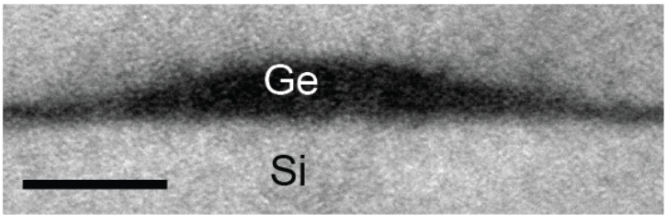
b) Ge Hut wires (HWs)

The first successful attempt to fabricate Ge nanowires catalyst-free is the case of Ge hut-wires (HWs). These structures can be defined as "three dimensional (3D) self-assembled Ge quantum dots (QD)" and they are obtained on Si(001) substrate using MBE (Molecular Beam Epitaxy) as a growth technique [8].

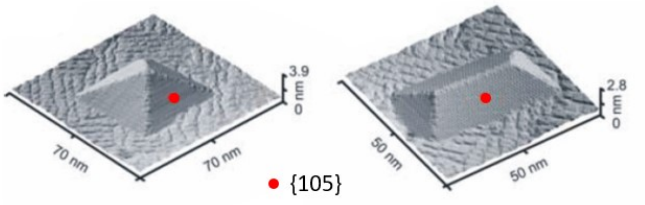
The growth of these structures exploits the self-assembly of Ge atoms and the lattice mismatch of 4%. In facts, as mentioned before, epitaxial growth of Ge on Si substrate will proceed with a Stranski-Krastanow (SK) growth mechanism: the first stage of the growth, typically only for approximately 4 monolayers, consists in a layer-by-layer mechanism, while once the energy is too high, growth mechanism will change in islands (or clusters) formation [8][24].

These Ge clusters shows a height of about 2 nm, a rectangular base and four {105} facets (figure 2.6b) and therefore their cross section is triangular (figure 2.6a). By varying the Ge flux inside the MBE system, it is possible to control the length of the structures, that can be grown up to 2 μm for low Ge flux [8].

Then, Ge HWs are capped with few nm (usually 5) of Si in order to form a core/shell structure with the type II alignment to coherently strain the Ge NW core. Mobility results obtained using these structures are not comparable to the VLS core/shell NWs or the planar heterostructures, but it is a good start for the fabrication of catalyst-free NWs [8][24].



(a) Triangular cross section of a Ge Hut wire, capped with Si [8].



(b) STM images of the HWs with in evidence the {105} facets [24].

Figure 2.6: Ge Hut wires (HWs).

2.1.3 SAG - Selective Area Growth

A promising alternative to grow Ge/Si core/shell NWs catalyst-free, consist in exploiting Selective Area Growth (SAG) technique to fabricate in-plane NWs.

In the SAG approach the material of interest is only deposited in pre-defined locations. To achieve this, a dielectric mask is deposited on the substrate and then using nanolithography techniques, typically DUV (Deep UV) or e-beam, openings that leave the underlying substrate exposed are impressed. Then the sample is loaded in the growth reactor to obtain the NWs [9]. To achieve properly the selective growth, the dielectric mask has to fulfill some requirements:

1) Thermally stable to resist at the high growth temperatures.

2) Inert in contact with the gas carrier and gas precursor in the reactor.

3) Compatible with the following fabrication steps [9].

4) The sticking coefficient of the adatoms on the mask has to be low to reduce the probability of having parasitic nucleation on the mask itself (figure 2.7).

Silicon oxide (SiO_2) is a very suitable candidate for this role. So, picking the right mask and by choosing the correct growth conditions in the reactor, the nucleation of the material occurs only in the openings regions [9]. Just by modifying the lithography pattern it is possible to form also complex shape openings.

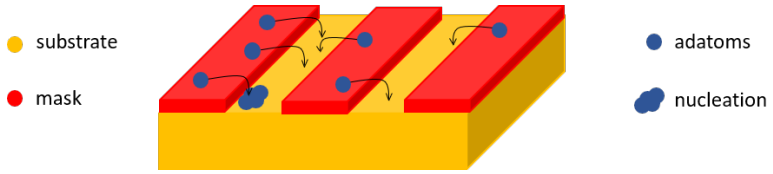
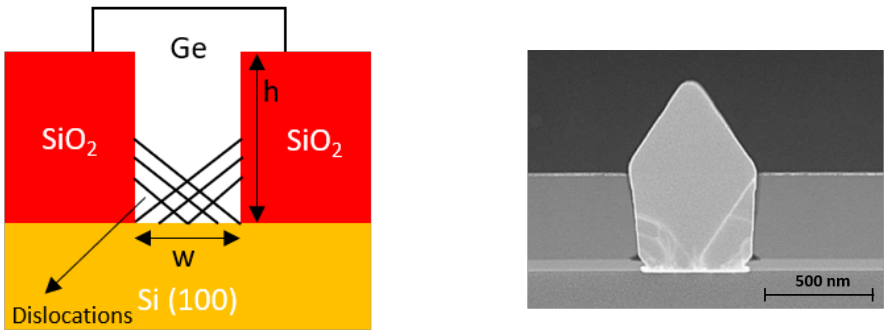


Figure 2.7: Good dielectric mask: adatoms do not stick on it but they diffuse in the openings.

Moreover, SAG is really suitable for heteroepitaxy using MBE, MOVPE (Metal-lorganic vapour-phase epitaxy) or CBE (Chemical beam epitaxy). In the case of heteroepitaxy usually the main issue is the lattice mismatch between the substrate and the material epitaxially grown on it. If the thickness of the heteroepitaxial layer is beyond a certain value (that depends on the lattice mismatch), the epilayer cannot stand anymore the strain and there will be a formation of misfits dislocations that usually terminate at the surface as threading dislocations [10]. This defects formation reduce the performance of the semiconductor because they act as recombination and scattering centers reducing the optoelectronic properties of the material.

Thanks to the dielectric mask, dislocations that are generated at the substrate/epilayer interface, will propagate until they annihilate at the mask side. This phenomenon, called aspect ratio trapping (ART), leaves the upper part of the NWs, beyond the critical thickness, defects-free [11].

The ART depends on the crystallographic geometry of the material where the dislocations propagates. For the case of cubic materials, such as Ge and the majority of III-V materials, dislocations formed glide along the <110> direction to form an angle of ∼55° with the substrate. For this reason, if the height (h) of the silicon oxide mask is at least 1.4 times greater than the aperture (width), dislocation will be annihilated in the oxide mask [25]. In the case of Ge on Si substrate, since germanium has a lattice parameter of 0.566 nm that is 4% larger that the Si one this phenomena is evident [11] and in the figure 2.8a is represented a schematic depiction of what happens. In addition, in figure 2.8b is presented a SEM image of a cross section of GaAs grown on Si.



(a) Scheme of how dislocations are removed. NWs will have the top part defects-free if the aspect ratio (h/w) is at least 1.4. Adapted from [10].

(b) SEM image of GaAs NWs on Si. Dislocations do not propagate in the upper part leaving the NWs defect-free. Adapted from [25].

Figure 2.8: SAG: annihilation of dislocations [10].

2.1.4 Previous results

Thanks to the SAG approach, the major problem of scalability of these devices can be overcome. Conventionally, Ge nanowires are grown "out-of-plane" using the VLS growth method. This approach has two main issues.
Firstly, as mentioned before, for the use of Au drops as a catalyst and secondly, because NWs are grown on a certain substrate and so they need to be manually transferred onto another one where the device can be fabricated [16]. This drastically reduce the throughput of the process [7].

With the SAG approach, it is possible to grow nanowires in pre-defined positions where the device can be easily grown on it, with a high degree of control over the geometry and crystal phase, eliminating the step of "pick and drop" of the NWs [16].

S.P.Ramanandan et al.[16] successfully demonstrate SAG for in-plane Ge NWs grown at 700°C on Si(100) using MOVPE. In particular, NWs along the <100> and <110> directions were evaluated to compare the defects density and the different final shape of the final wire. Lowest value of aperture in the mask (width) evaluated is 80 nm [16]. Figure 2.9, shows the TEM/STEM-EDX image of a cross-section of a Ge nanowire grown along <110> direction, while figure 2.10 shows the TEM image of the wire grown along <100>.

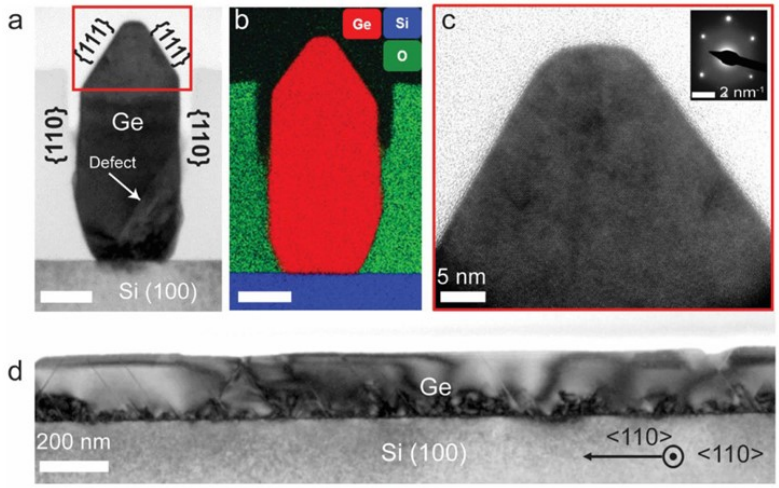


Figure 2.9: TEM/STEM-EDX images of in-plane Ge NWs growth along <110> direction.

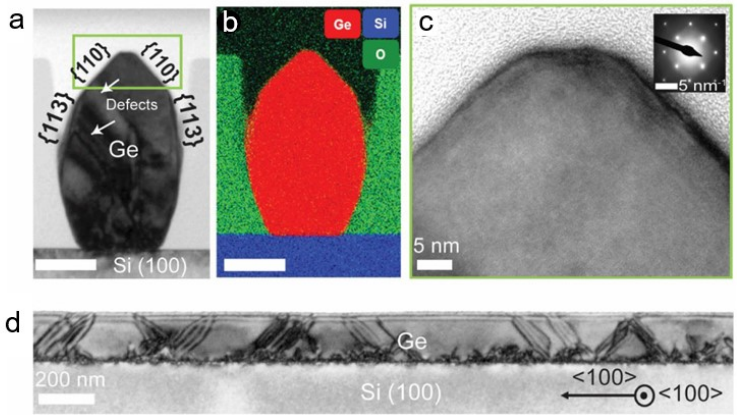


Figure 2.10: TEM/STEM-EDX images of in-plane Ge NWs growth along <100> direction.

For both directions, the cross-sections show a triangular facet morphology. However, in the case of figure 2.9, the nanowires exhibit two sides {110}, two inclined {111} and the top flat {100}. On the contrary, in the case of 2.10, sidewalls shows {113} while the inclined are {110} [16].
In addition, looking at the crystal quality, especially from the (a) and (d), it is clear that NWs grown along the <100> shows an higher concentration of defects and the majority of the dislocations is not annihilated by the SiO_2 mask but migrate also in the top part of the wire [16].

Electronic characterisation is also performed by fabricating Hall bars along the <110> direction and at room and low temperature. Results shows that the transport occur in the part of the NWs where there is more concentration of defects. Moreover, it was demonstrate that the wires are unintentionally heavily p-doped with an hole density of $\sim$5x10^{18} cm^{-3}, possibly due to vacancy defects or surface states [16]. Most importantly, magneto-resistance measurement shows coherent hole transport phenomena, an indispensable property for future application as a platform for spin-qubits [16].

However, despite the results obtained some problems are still present and need some improvements:

1) Defects are not minimised;

2) Nanowires are grown inside the slits create by the mask: it is difficult to gate them to further isolate the holes and make qubits;

3) Doping level is too high due to presence of surface states. This leads to a reduced mobility ($\sim$400 cm^2/(V s)) and low mean free path ($l_e \approx 10$ nm);

4) NWs are big, that increases the probability of defects and reduce the ease of hole confinements [16].

2.2 Novelty, improvement and thesis organisation

This thesis work starts from the results illustrated in the chapter 2.1.4 focusing on the problems arose. A part of the thesis is dedicated to optimize the growth of Germanium nanowires. We tried to understand the effect of different growth parameters and geometrical parameters on the NWs. In fact, the openings in the mask are fabricated with different geometrical features, as represented in figure 2.11.

The most important one is the width (w) that defines the size of the aperture in the dielectric mask. It is directly related to the size of the NWs. In fact, to reduce the size in a controlled way, it is necessary to act on the width. Then, the length (l) defines how long the wires can grow while the pitch length (p) indicate the distance between two nearest apertures.

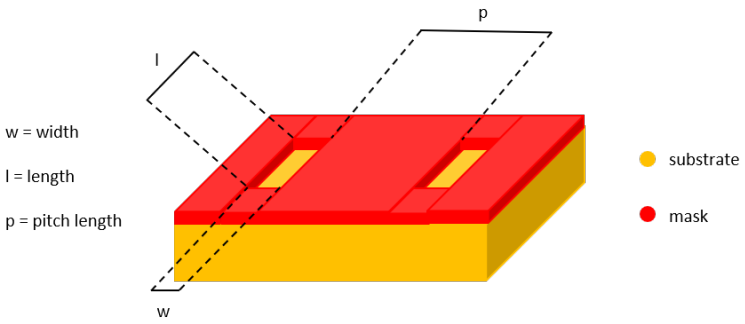


Figure 2.11: Geometrical parameters on the substrate: width (w), length (l) and pitch length (p).

Moreover, defects and high doping density induced by surface states are decreased by capping the NWs with a Si passivation layer that will act as shell that will simultaneously protects the Ge surface and confines holes in the core.

Efforts to improve crystal quality and electrical properties have been performed and methods and results are presented within this thesis.

In **Chapter 3**, fabrication processes and characterisation techniques used are presented.

In **Chapter 4**, results are discussed following this order:

4.1. Nucleation mechanism of Ge cluster on Si(100) substrate with SAG technique.

4.2. Methods designed to minimize the presence of defects: modified growth parameters and modified substrate preparation.

4.3. Techniques for surface passivation: motivation, methods, problems and results.

4.4. Transport measurements results: bare Ge vs Ge/Si core/shell NWs.

Chapter 3

Process flow and methods

The fabrication process of preparing the Si substrate to obtain the desired pattern, where subsequently Ge NWs will be grown, will be presented in this section. All the steps were conducted in the CMi cleanrooms in EPFL campus [12].

3.1 Substrate preparation

Starting with a 2in Si(100) wafer, the first step consist in removing all the contaminants that can be present on the surface (both organic and inorganic). This procedure is called "RCA cleaning". The procedure can be divided in three different steps, based on the type of contaminant to be removed (more details in Appendix A).

After the clean, a controlled thermal oxidation to obtain a thin layer of SiO_2 is performed. We fabricate two types of samples, one with 25 nm oxides thickness and one with 175 nm [12].

3.1.1 E-beam patterning

Once the oxide mask is grown, the next step is to transfer the patterns needed on the wafer. In order to do so, e-beam lithography is chosen above others due to its high control over the low dimensions reachable (more details of this technique in Appendix A). Before the exposure, it is necessary to deposit the polymer resist on the wafer. In fact, the high energy electrons from the beam interact with the polymer de-polymerizing it (positive resist) or inducing crosslinking (negative resist). The resist choose for our pattern is ZEP, a positive Styrene Methyl Acrylate based polymer [12]. The resist is deposited on the wafer via spin-coating after a substrate dehydration for 5 mins at 180°C. For the case of the ZEP, the ideal thickness is at least the value of the silicon oxide layer thermally grown to be sure

that in the subsequent etching step, the ZEP is not completely lost. This thickness is inversely proportional to the rpm set in the spin coater, as we can see from the Table 3.1. After the deposition, the layer is baked for 5 mins at 180°C.

Table 3.1: Rpm set as a function of the thermally grown.

ZEP thickness (nm)	Rpm	Resist
175	2000	ZEP 50%

To reduce the number of variables in the process, also for the case of 25 nm silicon oxide, 175 nm of ZEP is deposited. Now, the wafer is inserted in the substrate holder of the e-beam and it is ready for the exposure. Once the exposition is complete, the substrate has to be developed in order to remove all the polymer impressed by the electron beam.

3.1.2 RIE - Reactive Ion Etching and ZEP stripping

After the development, the schematic of what the substrate looks like is depicted in the figure 3.1.

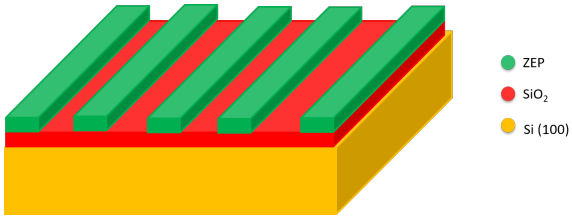


Figure 3.1: Schematic depiction of the substrate after ZEP development.

The pattern, represented in the figure as horizontal trenches, is impressed only in the polymer resist. To place such a pattern also in the silicon oxide mask, an anisotropic etching step is necessary. Anisotropic dry etching is chosen over the isotropic wet, to maintain a high aspect ratio of the trenches.

To achieve this, SPTS APS machine is used. The process consist in placing the sample in a chamber and, after evacuating the air, a plasma is generated by an electromagnetic field is directed vertically relative to the substrate. Moreover, the plasma consists of reactive ions that selectively remove one chemical species over another with a given etching rate value. Thanks to the combination of physical and chemical etching, higher control over the SiO_2 aperture is obtained.

At this step of the fabrication process, really important is the value of the etching

time performed on the sample. In fact, ideally, the purpose is to etch away all the SiO_2 layer and, as soon as the Si substrate is reached, stop the RIE. The complication is that the etching rate is dependent on the width of the slits. In particular the larger the slits, the higher the etching rate will be. Since one of the goal of the project is to reduce the dimensions of the NWs, RIE timing was chosen to optimize the smaller apertures and in particular 50 nm, 80 nm and 100 nm (for this last value overetching defects started to appear). In the Table 3.2 are shown the optimised values of etching for the two different SiO_2 thickness.

Table 3.2: Optimised RIE time for the two different oxide thickness.

Oxide thickness (nm)	RIE time (s)
175	110
25	23

Now that the pattern is transferred on the silicon oxide, the ZEP remained can be removed. This process is based on two steps: first a "raw" stripping of the polymer is performed using acetone and IPA. Then the sample undergoes a more accurate cleaning via oxygen plasma to be sure that all the polymer left is stripped. The last step is done with the machine Tepla GiGAbatch that uses a high frequency plasma at 600W for 10 mins [12].

Schematic illustration of the growth substrate after the processing steps is shown in figure 3.2.

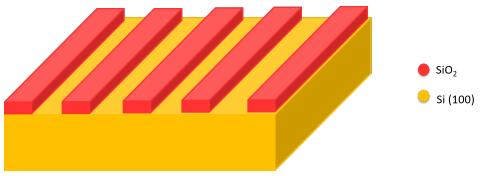


Figure 3.2: Schematic depiction of the substrate after RIE and ZEP stripping.

3.1.3 Wet etching

Since the bottom of the openings, formed by bare Si is exposed to air, one last step before the growth is necessary and consist in removing the 1-2 nm of natural SiO_2 formed [13]. To eliminate this layer, the sample is subjected to a 1% HF dip for 120 sec.

3.2 Growth method: MOVPE - Metallorganic Vapour-Phase Epitaxy

As mentioned in the previous chapter, now that the SiO_2 mask with all the openings is fabricated, the the Ge growth step can be performed. Among all deposition methods, it is necessary to choose one that ensures epitaxial growth on the Si substrate. The choice falls on vapor-phase epitaxy (MOVPE).
The figure 3.3 shows the MOVPE facility used for the grown at LMSC2 in the EPFL physic department.

(a) MOVPE Reactor. **(b)** MOVPE tubing of the gas precursor.

Figure 3.3: Parts of the MOVPE facility.

In short, this method consists in sending metallorganic precursors of the species of interest in a reactor (figure 3.3a) where the substrate is placed. The precursors gasses are sent in the chamber thanks to a complex series of tubing (figure 3.3b). At a specific temperature, the precursor gas decompose leaving the organic part in the gas phase while the less volatile species are adsorbed on the substrate.

Atoms, once adsorbed, will diffuse on the substrate usually towards step-egdes of the surface, till forming a nucleation cluster that will grow over time.

MOVPE, coupled with SAG, has many advantages over others epitaxy deposition, mainly due to the fact that it offers a larger selectivity window.

Moreover, in the MOVPE, the key parameter is the cracking temperature of the precursors molecules on the substrate that permit to free the species of interest

that can diffuse over the substrate. This temperature, that will become the temperature of processing, is typically lower compared to the other nanodeposition technique, such as MBE.

In our case, the precursor used in our case is IBGe, whose chemical formula is presented in the figure 3.4

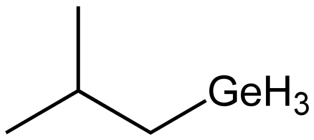


Figure 3.4: Chemical structure of IBGe.

In the figure 3.5 is depicted a scheme of the physical processes that take place into the reactor for the case of Ge growth.

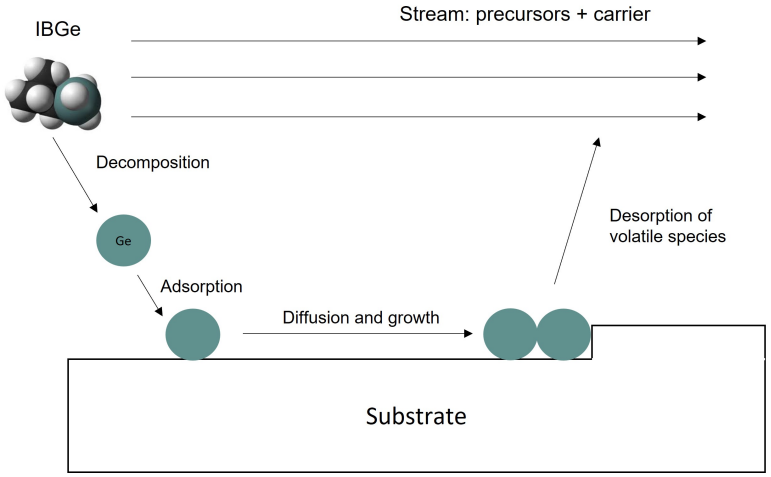


Figure 3.5: Scheme that depicts how precursors decompose in the MOVPE growth method.

The most impactful parameter during the growth procedure is the temperature set in the reactor and for this reason that influence not only the decomposition if the IBGe, but act also on the diffusion of the Ge atoms that migrate from the point they are adsorbed to the cluster that is growing. In fact, diffusion coefficient, equation 3.1, shows a influence on the temperature Arrhenius-type: increasing the temperature, atoms diffuse faster and consequently will have longer diffusion length.

$$D = D_0 exp(-\Delta E_g / RT) \tag{3.1}$$

In chapter 4.2 this temperature dependence will be analysed.

To conclude, in the figure 3.6 is illustrated the summary of the whole fabrication process with all the steps analysed, from the thermal oxidation to the MOVPE growth.

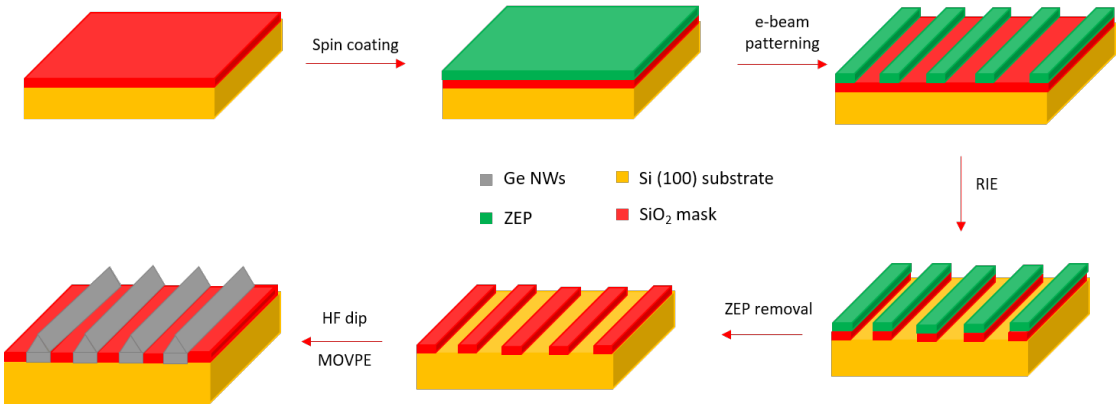


Figure 3.6: Summary of all the fabrication process.

Moreover, in the figure 3.7 is represented how it appear the sample after all these steps, before characterisation.

Figure 3.7: 1/4 of a 2in sample obtained after the process. This sample is grown at 750°C for 30 sec.

3.3 Characterisation techniques

Characterisation techniques are an extremely powerful tool to probe surfaces and patterns at micro- and nano-scale. Depending on the type of property to be analysed, the technique has to be chosen correctly. The ones used in this project are mainly physical characterisation such as SEM (Scanning Electron Microscopy), TEM (Transmission Electron Microscopy) or AFM (Atomic Force Microscopy) and physico-chemical such as Raman spectroscopy.

3.3.1 SEM - Scanning Electron Microscope and TEM - Transmission Electron Microscopy

SEM is widely used in materials characterisation because it is possible to obtain information about the topography of the surface with a resolution of about 1 nm [26].
To obtain images of the surface, SEM Zeiss Merlin in the CIME (Centre Interdisciplinaire de Miocroscopie Électronique) department in EPFL is used.
The structure of this tool, represented in the figure 3.8 on the left, is really similar to the ebeam one (figure A.1).

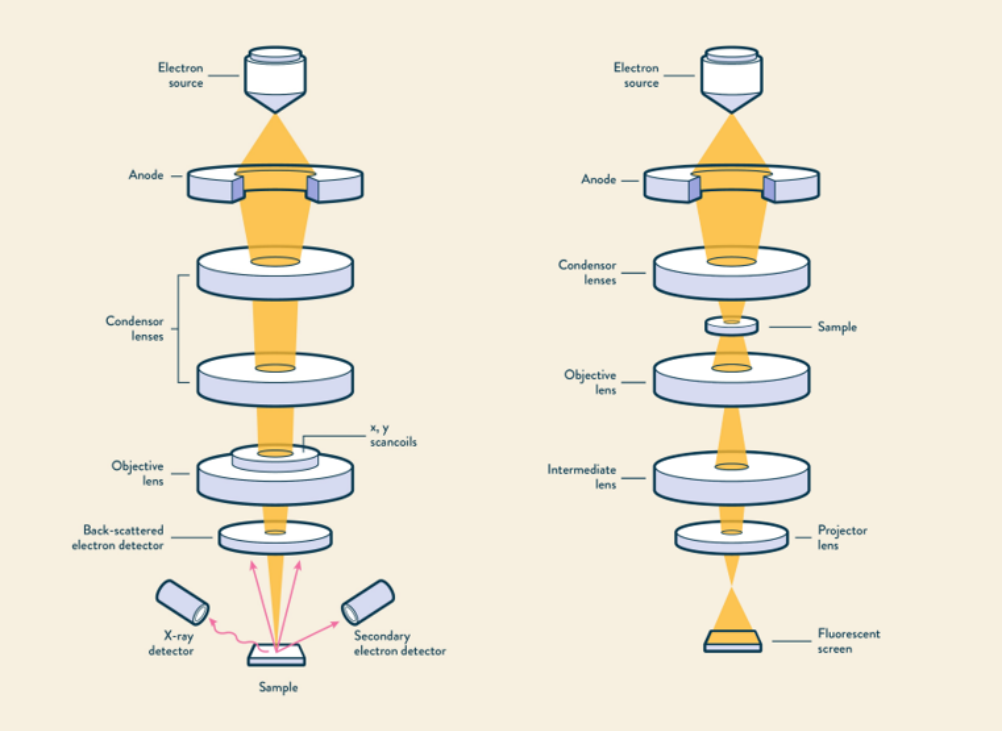


Figure 3.8: Scheme of the SEM (on the left) and TEM (on the right) [27]

In fact, similarly, electrons are generated by an "electron gun" exploiting the Field Emission effect. This consist in applying a high electric field on the metal "gun" that enhance the electrons to tunnel into the vacuum and create the beam [19]. With this method, the electrons generated have a less dispersion of energy, compared to the thermionic emission, and so it is easier to focalized them on the surface of the sample by the electromagnetic and electrostatic lenses.

Compared to the ebeam tool, the electrons are accelerated with a voltage of maximum 30 keV (but usually the voltage for the structure we are probing is around 3 keV). With this amount of energy the electrons impact on the surface and they interact with the atoms on the surface. In particular for the case of "secondary electrons", that are the ones that give the information about the topography, the incoming electron collide with an electron in the shell of the atom at the surface of the sample (figure 3.9)[19].

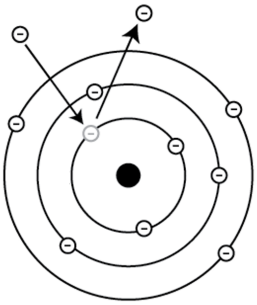


Figure 3.9: Ejection of the secondary electrons [28].

The electron hit is ejected from the sample and collected by a detector that transforms the signal into a grayscale image [19].

Regarding TEM (figure 3.8 on the right), the structure of the microscope is really similar to SEM because the principle on which it is based is the same. However, in this case, the electron collected and analysed are the transmitted thought the sample, at the bottom of the column. So, it is important that the primary electrons (the ones colliding) are able to pass through the sample. To enable this, more energy is given to electrons (typical voltage applied 100 keV) and the thickness of the sample has to be sufficiently low, usually around 150 nm [27].
To achieve this thickness, the sample is milled with FIB (Focus Ion Beam), a microscope similar to SEM but equipped with a Ga ions beam instead of electrons. The TEM used is the Tecnai Osiris in CIME.

3.3.2 AFM - Atomic Force Microscopy

This technique differs from the previous ones because it does not use an electron beam to probe the sample but it exploits Van der Waals repulsion and attraction forces [29]. The tool used in the project is the AFM FastScan commercialised by Bruker. In the figure 3.10 is schematised how it works.

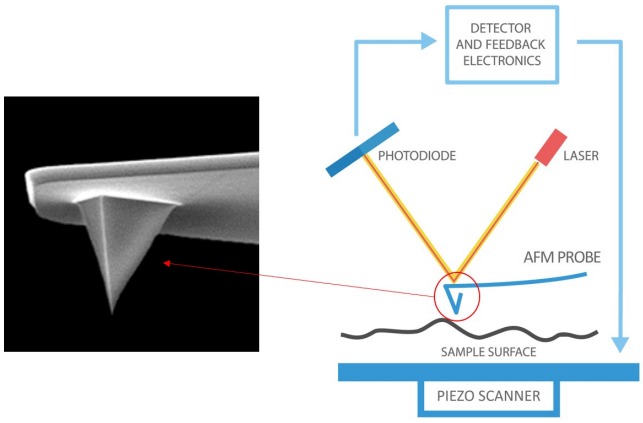


Figure 3.10: Scheme of the AFM probe with the ScanAsyst-Fluid+ tip in Si used. [30][31].

The tool consists in a cantilever in the end of which there is a very sharp tip (figure 3.10) that ideally end with a single atom. The tip approaches the surface and an interaction is established. Depending on the nature of the interaction (attractive or repulsive) the cantilever is deflected and/or tilted and this affect the laser spot position in the photodiode. The photodiode communicate with the feedback electronics that translate this variation of signal into a topographical mapping. The cantilever is moved across the whole region of interest using a piezoelectric material [29]. The result is a topographical mapping highlighting the roughness and height difference of the sample with a z-resolution of fraction of Amstrong. The most common way to use the tip is in non-contact mode (or tapping mode), where the cantilever oscillate at its resonant frequency ω_0. While moving across the the surface, due to the presence of force gradient, the spring constant of the cantilever is modified according to the nature of tip-substrate interaction (F_{ts}) and as a consequence a shift in the resonant frequency is noted (formula n.3.2) [29][32].

$$\omega = \omega_0 \sqrt{1 - F_{ts}/k} \tag{3.2}$$

Where ω is the new resonant frequency and k is the spring constant of the cantilever.

3.3.3 Raman spectroscopy

The method consist in studying the interaction of a laser with chemical bonds of the structures. The light incident is scattered by the molecules and most of it is at the same wavelength of the laser source. However, a small amount of the source is scattered at different wavelength (higher or lower) depending on the chemical nature of the bond [33].

So, each type of bonds have a specific "Raman shift" and it is possible to perform a chemical characterisation of the types of bonds present in the spot analyzed. Moreover, the shape of the peaks obtained give a further information about the physical status of the sample such as: presence of crystalline or amorphous phase, presence of strain (or compression) results in a shift at lower (or higher) Raman shift and the presence of defects that act on the broadening of the peaks. For this reason, Raman spectroscopy is a really powerful tool because it can gives correlation between the chemical composition. The peaks in which we monitor in our case are reported in the table 3.3.

Table 3.3: Raman wavelength studied

Chemical bond	Wavenumber
Ge-Ge	$\sim$310 cm^{-1}
Ge-Si	$\sim$360 cm^{-1}
Si-Si	$\sim$460 cm^{-1}

3.3.4 Other nanodeposition technique: ALD (Atomic layer deposition) and PECVD (Plasma-enanched Chemical Vapour Deposition)

ALD

ALD is a deposition technique that permits to deposit very thin films of material, such as just few nanometers of thickness. The deposition in made in a reactor where the temperature can be adjusted and it consist in a cicle formed by four separate steps, also schematised in figure 3.11:

1) Injection in the reactor of the first gas precursor and chemisorption on the substrate.

2) Purge of the reactor with nitrogen.

3) Injection in the reactor of the second gas precursor and reaction with the outermost layer.

4) Purge of the reactor with nitrogen.

ALD used within this thesis is BENEQ TFS200 and it was used mainly to deposit Al_2O_3, with TMA as Al precursor, and H_2O as O precursor, at 200°C.

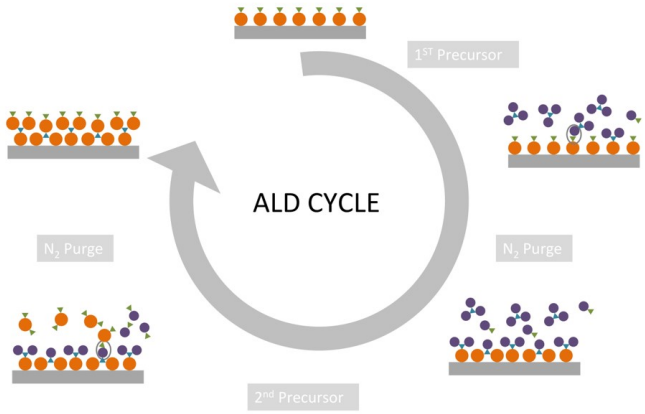


Figure 3.11: ALD growth cycle [34].

PECVD

PECVD technique is very similar conceptually to a MOVPE because also in this case the precursors of the material desired are in their gas-phase. In this case, in the reactor are present two electrodes that, by applying a DC or AC current, accelerate the gas precursors and induce the formation of a plasma. This plasma promotes chemical reaction and the subsequent thin film deposition. A scheme of the reactor is shown in figure 3.12.

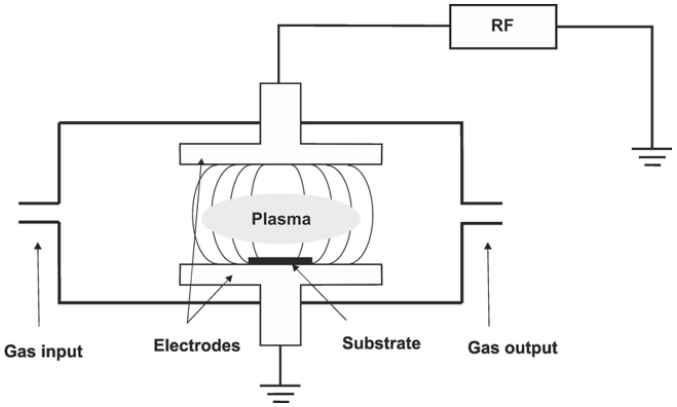


Figure 3.12: Scheme of the PECVD reactor [35].

Chapter 4

Results and discussion

In this section, results obtained regarding the growth optimisation are presented and discussed: from the nucleation step to the evaluation of the electronic properties.

4.1 Nucleation of Ge

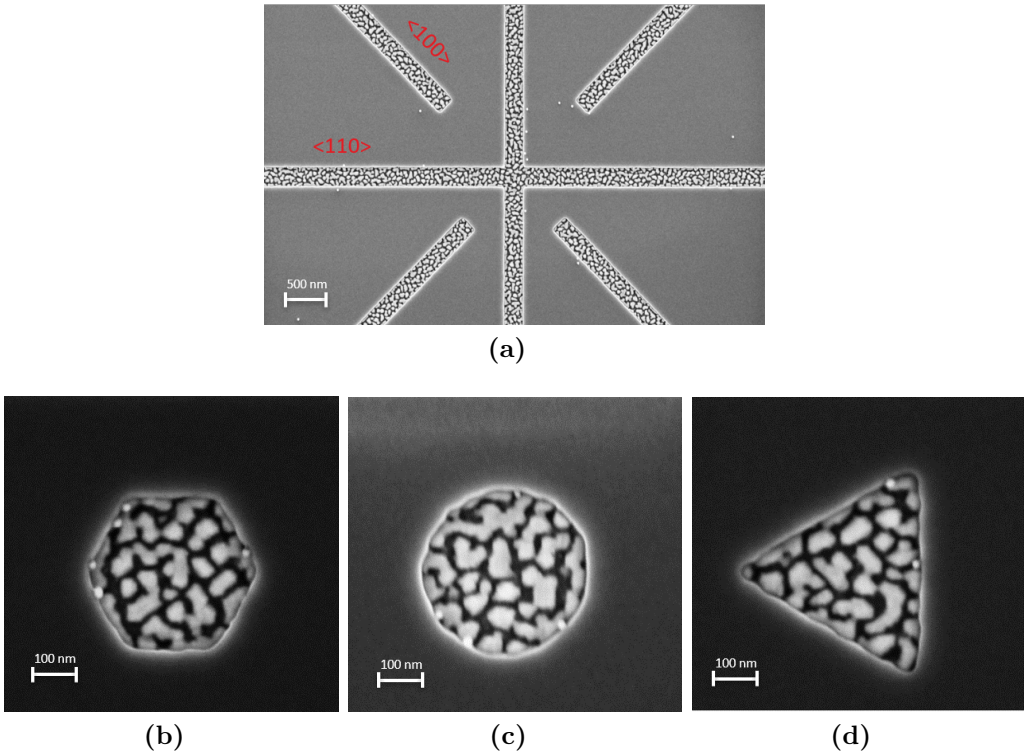
One of the main objective of thesis, as mentioned before, consists in optimising the Ge growth in order to reduce the density of defects in the NWs. For this reason, a good starting point will be having an understanding of how Ge atoms nucleate and grow after the gas precursor decomposes in the MOVPE reactor.

To understand it, a growth series at the nucleation stage is evaluated. The growth parameters and substrate type are presented in the table 4.1.

Table 4.1: Nucleation growth parameters.

Temperature	**Time**	**SiO_2 thickness**
750°C	15 sec	25 nm

The temperature set is 750°C, while the time is set at 15 sec, because it represents the first time where a sufficient nucleation can be observed in SEM image. A top-view SEM image of the nucleation stage of the Ge NWs after 15 seconds of growth at 750°C is presented in the figure 4.1.



(a)

(b) **(c)** **(d)**

Figure 4.1: Top view SEM image of Ge nucleation stage for (a) <100> and <110> direction and for particular shapes: (b) hexagon, (c) circle, (d) triangle.

As represented in the images, nucleation takes place inside the nanoscale openings made in the SiO_2 mask and, in particular, as can be seen especially in the figure 4.1b, in the interface Si/SiO_2.

Our initial objective was to understand the observed nucleation behaviour. We started by investigating the surface morphology of the NWs by performing AFM measurements. In figure 4.2 is presented the topography of the Si after the substrate fabrication step, on the left before the HF dip and on the right right after.

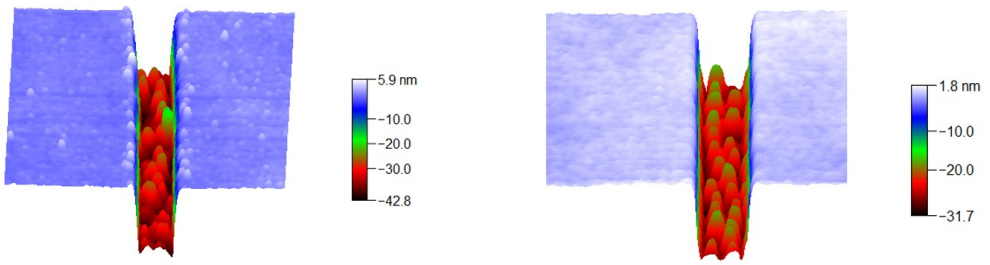
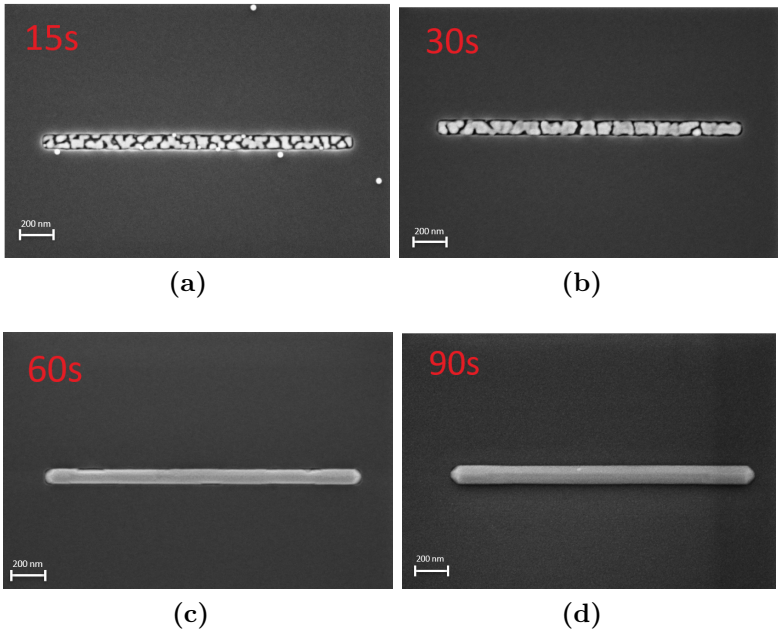


Figure 4.2: 3D AFM for 100 nm nominal width with the roughness in evidence, before (left) and after (right) HF dip.

From this picture, the value of the root mean square roughness (R_q) is evaluated using the software Gwyddion. The results shows $R_q = 4.2$ nm in the slit for the left case and $R_q = 3$ nm for the right. In fact, the HF dip before the growth, not only has the role to remove the native oxide, but also to smooth the Si surface, decreasing the roughness value.

We speculate that the surface roughness of the surface of the Si due to RIE step, is the main cause of the observed nucleation behaviour. In fact, fluorine plasma, while etching the silicon oxide, can also reach the Si substrate, leaving the surface rough. The valleys formed due to the roughness might act as a preferential nucleation spot.

After the nucleation step, with time these nuclei of Germanium merges to forms islands which eventually forms a continuous wire after 90 seconds of growth. The results are presented in the figure 4.3.



(a) **(b)**

(c) **(d)**

Figure 4.3: Top view SEM image of the growth evolution of the NWs for (a) 15, (b) 30, (c) 60 and (d) 90 seconds in the reactor.

Four growth time are compared: 15 seconds, the nucleation stage, 30, 60 and 90 seconds. What is clear is that the cluster grows until they merge with their neighbors to form a continuous nanowire (90 seconds).

Moreover, more complex structures can be grown depending on the pattern impressed on the substrate. For example, interconnected structures, as represented in the figure 4.4, are studied to evaluate how nanowires grown on different orientation behave when their path crosses.

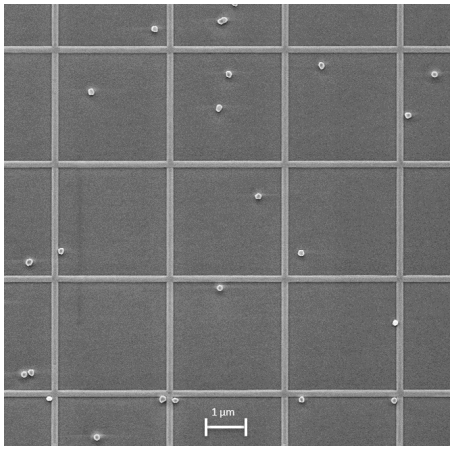


Figure 4.4: Top view SEM image of interconnected NWs structures.

When the clusters merge, as well as the crossing point of the interconnected structures, there is a probability of defects and dislocation formation. Thanks to the SAG approach and by optimising the growth condition (more details in Chapter 4.2), the threading dislocations, even if still present, can be minimised.

4.2 Defects Minimization

4.2.1 Growth parameters optimisation

After investigating the effect of substrate roughness on the nucleation stage, we now turn our attention to understand the effect of the growth parameters. The most influential one results to be the growth temperature in the MOVPE reactor. A series of sample with different growth temperature is conducted to evaluate the best one. Top view SEM images of all the combination evaluated for nominal 200 nm width are presented in the figure 4.5. The study is conducted with Si with 175 nm of thermal silicon oxide focusing on the optimisation of the smallest features.

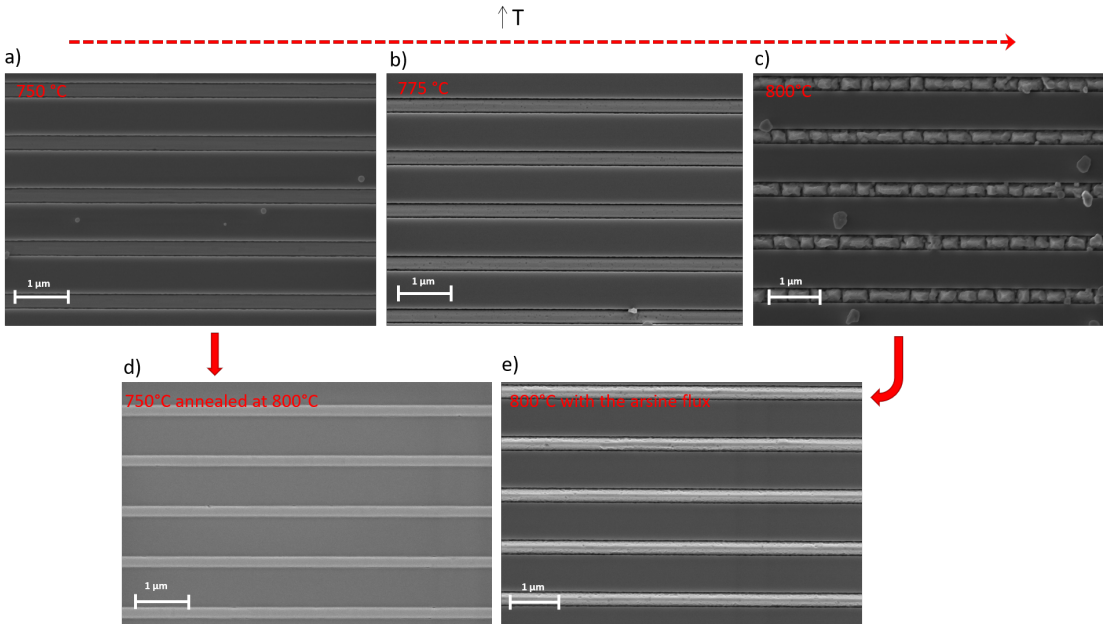


Figure 4.5: Top view SEM images of 200 nm nominal width NWs grown with the "classic" recipe at: (a) 750°C, (b) 775°C, (c) 800°C and (d) 750°C with post-annealing step. Sample (e) is grown with the "modified" method.

Going from (a) to (c) the growing method is kept constant, it has been used the "classic" one (details in Appendix B) with the only change in the growth temperature in the reactor.

From the SEM, defective NWs can be recognised if they present, on the surface, roughness and/or black lines. This is how stacking faults can be detected because once they are formed and they reach the surface, their presence will promote the formation of steps that are easily detected from the SEM. An example of these stacking faults is observed in the figure 4.6 for the case of 50 nm nominal width NWs grown at 700°C.

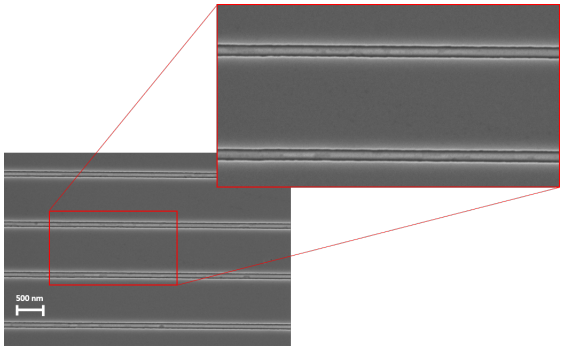


Figure 4.6: Top view SEM image of 50 nm nominal width NWs grown at 700°C with an magnification highlighting the presence of stacking faults.

From the SEM presented previously in figure 4.5, the growth conducted at 750°C turned out to be the best solution since the surface seems clean and smooth. Compared to the case at 700°C, at 750°C atoms have more thermal energy and they can reach equilibrium stacking more easily. Moreover, dislocation that may form have more energy to glide and be annihilated in the SiO_2 mask.

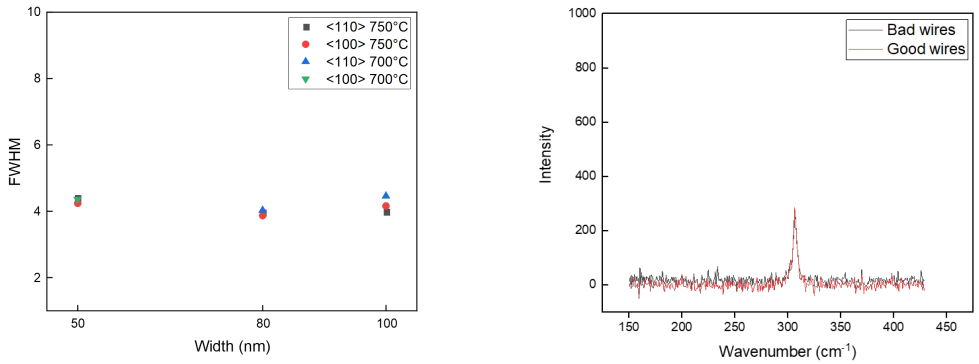
However, by raising the temperature to 775°C and then to 800°C, the surface start to became rough until they begin to form very defective NWs. What happens is that, the more the temperature rise, the more the desorption rate of the Ge atoms increases leaving the NWs rough, for the 775°C case, or half-formed, for the 800°C case.

Further modifications to the growth process itself have been tried and the results are exhibited in figure 4.5d and 4.5e.

The modifications attested in case (d) consist of adding downstream of the growth at 750°C, 3 minutes of annealing at 800°C, in order to allow any dislocations to glide to the mask. From the SEM, no roughening was noted after this step.

For the case (e) the "classic" growth method was changed by continuing fluxing arsine during the cooling down after the de-oxidation step (more details in the Appendix B as "modified" MOVPE growth method). The growth was still conducted at 800°C. From the SEM it can be clearly seen that there is an improvement in the NWs growth since for this case continuous NWs are grown. However, still some roughening is present on the surface comparable to the case grown at 775°C. Nevertheless, in this case is difficult to fully understand what is happening on the surface. Arsine might be adsorbed and change the polarity of the surface promoting the growth while inhibiting desorption.

A method for discriminating which nanowires are most defective compared to others, consist in analyse their Raman spectra. Raman spectroscopy is performed using a 488 nm wavelenght laser. As mentioned previously, presence of defects will act on the broadening of the peak and in particular of the value of full width half maximum (FWHM). In the figure 4.7a is shown the values of FWHM obtained for different NWs width for the case of 700°C and 750°C. Unfortunately, the amount of Ge in the slits is too low that the presence of defects do not affect the value of FWHM making a classification impossible. Also the case, shown in the figure 4.7b, where two nanowires with totally different growth condition: one with optimised parameters, the other one full of defects, did not show any trend.



(a) **(b)**

Figure 4.7: (a) FWHM values of the Ge-Ge peak in the Raman spectra for NWs grown at 700°C and 750°C. (b) Raman spectra comparison between NWs with optimised parameters and others full of defects. In both cases the spectra was obtained by subtracting the signal obtained from the substrate with that obtained on the NWs. In this way, the large signal of Si at 500 cm^{-1} is removed.

However, for all cases studied, the characteristic peak of Ge-Si binding was not observed. This means that the Si/Ge interface is sharp and no intermixing occurs at the growth temperatures. The same result was observed in the case of nanowires grown at 750°C and annealed at 800°C (spectra in the Appendix B).

Since Raman spectroscopy could not help to distinguish low defects wires from high defective ones, only from the SEM images obtained, best growth temperature of 750°C is chosen upon the others. From this sample, cross-section is cut using FIB (Focused Ion Beam) to obtain the thin lamellae to be analysed in with the TEM. In the figure 4.8a is represented the TEM image obtained from a 80 nm

nominal width nanowire grown at 750°C and in figure 4.8b, is presented a TEM image of a 50 nm nominal width nanowire, grown at 750°C with post-annealing at 800°C, both along <100> direction.

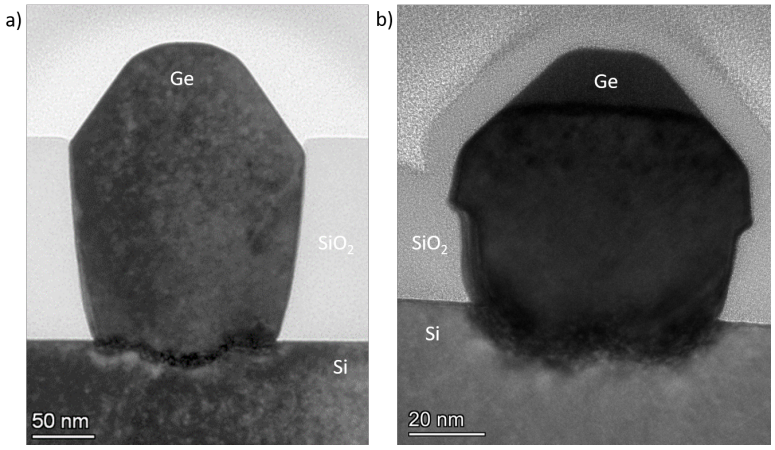


Figure 4.8: TEM cross-section images of (a) 80 nm nominal width NW grown at 750°C and (b) 50 nm nominal width NW grown at 750°C with post-annealing at 800°C grown along <100> direction.

The NWs appear to be stacking faults-free and with low amount of defects. On the right side of figure (a), a planar defect can be visualised, but it is totally annihilated by the SiO_2 mask.

As already previously pointed out, the Si/Ge interface is crucial. In fact, in the TEM image can be clearly seen that in the RIE step, once all the silicon oxide is removed, fluorine plasma starts to attack the Si substrate by etching and wrinkling it. Since the etching rate is width dependant, so smaller width needs to be etched for more time to reach the Si substrate, it is difficult to optimise the RIE step for every structure on the sample. The non-homogeneity of the interface can leads to more easily defects formation that can propagate through the NW.

For this reason, efforts have been made to avoid this roughness formation, in particular optimising the substrate preparation.

4.2.2 Substrate preparation optimisation

Different ways to reduce the openings roughness were studied within the project, but only the most promising one will be presented.

The idea consist in depositing a thin layer of few nanometers that acts as a

etch-stop layer. This means that the fluorine plasma during the RIE process, once all the mask is etched, will not end up directly to the Si substrate, but on the "buffer" layer specially deposited. Then, the buffer layer is etched away, leaving the smooth bare Si exposed and the growth is performed.

In the figure 4.9 is presented the new stack structure.

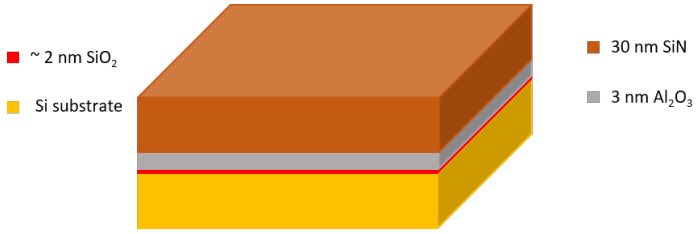


Figure 4.9: Scheme of new thin film deposited.

On the Si (100) structure, with about 2 nm of natural silicon oxide, is deposited 5 nm of Al_2O_3 via ALD (Atomic Layer Deposition). This layer will be the "etch-stop" where the RIE plasma will end up after the mask is fully etched. In fact, alumina, as later will be demonstrate, has low tendency to be etch by the the fluorine plasma used.

Then, 30 nm of SiN are deposited via PECVD (Plasma-Enanched Chemical Vapour Deposition) using SiH_4 and NH_3 as gas precursors in the chamber. For this case, SiN was chosen over SiO_2 because on the 5 nm Al_2O_3 buffer layer is not possible to thermally grow silicon oxide like it was done while fabricating the substrate. PECVD SiN was chosen over PECVD SiO_2 because it presents an higher value of dielectric constant that leads to a lower contacts loss in the device.

At this point, two ways are possible: either BHF (Buffered Hydrofluoric Acid) etching to remove Al_2O_3 and SiO_2 together, or separate the step removing before the Al_2O_3 with KOH, without having the problem of etching the SiN while removing alumina. BHF consists in a 1:7 mixture of HF 49% with ammonium fluoride (NH_4F) at 40%, added to have a better control on the etching step.

A scheme of the process described is presented in the figure 4.10.

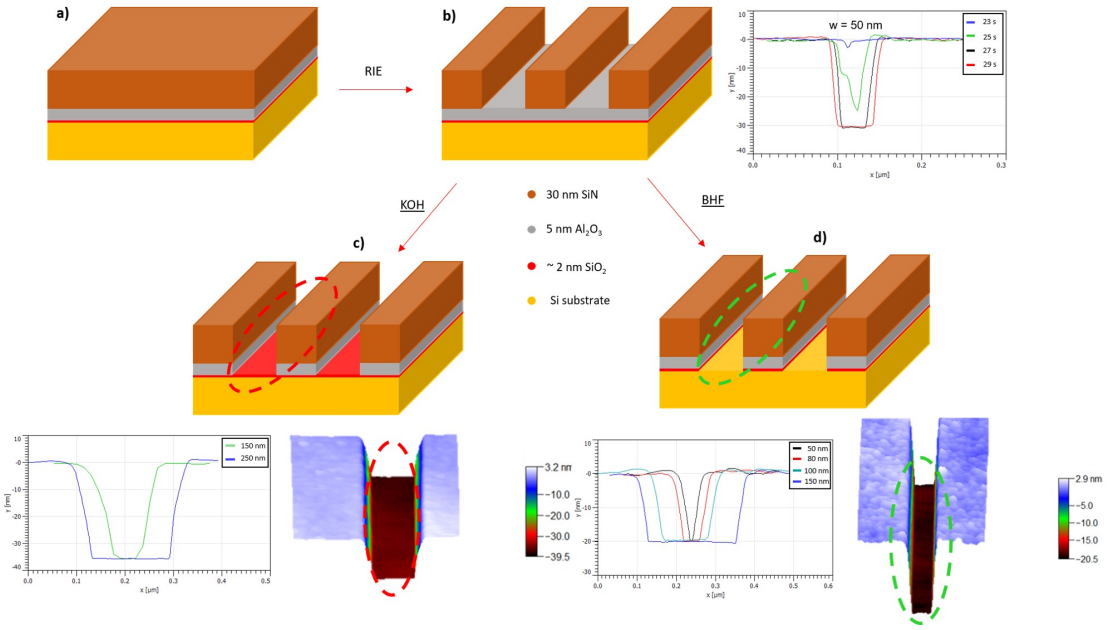


Figure 4.10: Scheme of the fabrication process used with the new stack. (a) Starting stack, spin coating of the resist, e-beam patterning and development are not depicted, (b) RIE step with AFM measurement conducted for different time for 50 nm nominal width, and etching step with AFM measurements for different widths for (c) KOH and (d) BHF.

Firstly, a series of increasing etching time were evaluated to understand if the "buffer" layer is working properly to stop the RIE. AFM measurements to check the depth reached were done on different values of nominal width. Only the result for the case of 50 nm width is presented in figure 4.10b, while the other widths are included in the Appendix B.

As the AFM profiles shows, for RIE time greater than 27 seconds, a depth of about 30 nm is obtained. This depth value is easily referable to the thickness of the SiN deposited, meaning the all the SiN is removed. Moreover, while increasing the RIE time to 29 seconds, the depth remains constant at 30 nm indicating the successful working of the etch-stop layer.

Now, as schematised previously in figure 4.10, the Al_2O_3 layer is removed.

C) KOH

The first approach consist in selectively remove Al_2O_3 with KOH. In fact, KOH etching rate for SiN and SiO_2 is much lower than the one for Al_2O_3 [12]. Moreover,

the native silicon oxide is thick enough to avoid unintended etching of the silicon substrate itself. AFM profiles of the slits after 5 seconds of etching are shown in the figure 4.10c. For higher nominal widths (150 nm and 250 nm), a 35 nm depth is reached. This means that all the etch stop layer is correctly removed. Now the flat part a the bottom of the slits, circled in red in the figure 4.10c, results to be the Si substrate, covered by its native oxide. So, a roughness evaluation was performed. The calculated value results to be $R_q = 0.4$ nm, much lower than the "standard" case previously presented.

D) BHF

The second approach consist in directly etch the "buffer" layer and native silicon oxide in one step using BHF. However, it can etch also the SiN mask and so the time value turns out to be a crucial parameter to reduce the loss in mask height. On the sample, etching was conducted for 6 seconds and in the figure 4.9d the AFM profiles for different widths are shown.
For both small and large widths, the slits shows a dept of 20 nm. What happened is that while the etch-top layer was removed, SiN mask was vertically (and laterally) etch of about 15 nm. The bottom of the slits appears to be rather smooth and so a roughness calculation was implemented. The value obtain for R_q is 0.6 nm.

In the table 4.2 are compared the roughness values of the four cases evaluated where thanks to the "etch-stop" layer approach there is a evident improve in the surface roughness.

Table 4.2: Roughness value for the different sample evaluated.

Sample	**Wet etch type**	**Roughness (R_q)**
Standard	-	4.2 nm
Standard	HF	3 nm
Etch-stop	KOH	0.4 nm
Etch-stop	BHF	0.6 nm

One first growth with the approach (d) was conducted. The growth parameter were kept the same (temperature 750°C for 90 seconds) in order to compare with the case of the standard substrate. However, in the sample analysed, the NWs were still in their nucleation stage and for this reason a comparison between the 15 seconds growth is conducted in figure 4.11.

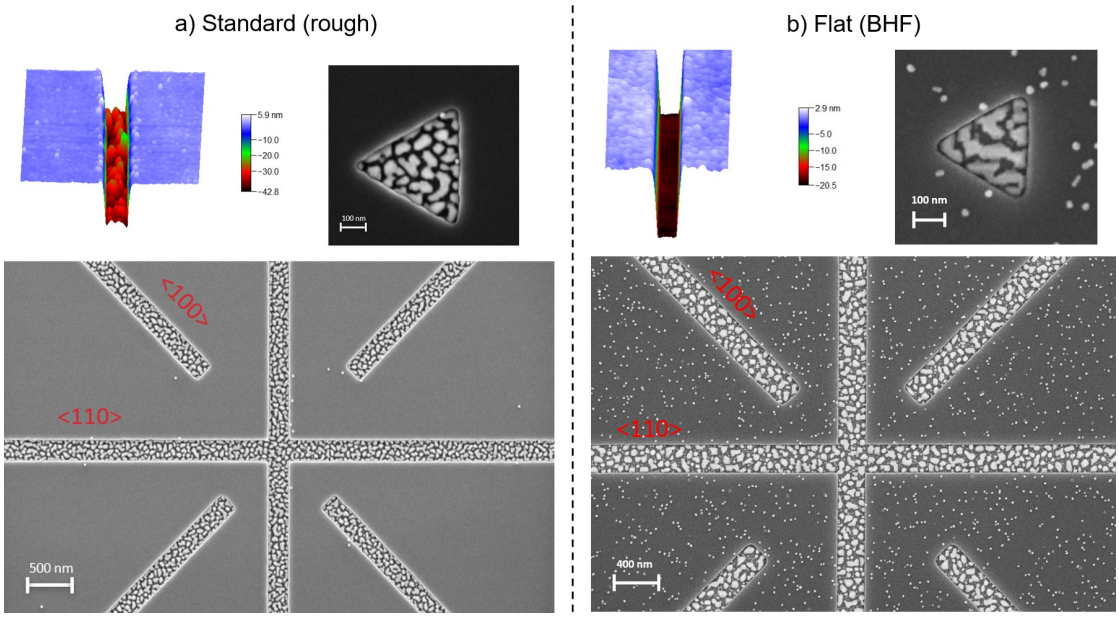


Figure 4.11: 3D AFM image and top view SEM nucleation images for (a) standard substrate with 15 seconds of growth and (b) optimised substrate with BHF etching with 90 seconds of growth.

Even if the growth time is kept at 90 seconds, for the case of the flat surface the nanowires are still in their nucleation stage. This might be an effect of the different type of mask used that can modify the growth rate of the NWs themself. Comparing the nucleation in the triangular aperture between the standard and the flat case, in the last case it seems to be in a further state of nucleation since less and bigger clusters can be visualised. However, as the "standard" case, no difference can be noted between the two growth directions.

Further growth to obtain fully-grown NWs are necessary to see if their quality is improved.

4.3 Surface Passivation

4.3.1 Motivation

As also mentioned in the previous chapters, Ge shows high electronic properties, in particular for this case p-type mobility value, compared to most group IV semiconductors, particularly Si.

However, one of the biggest problem related to the use of Ge is the formation of

the natural germanium oxide when in contact with air [36]. Germanium oxide layer is characterised by a large amount of defects that break down the electronic properties by acting as trap states and recombination sites that lower the electrons (or holes) mean free path [37]. Surface effects, for nanowires, are very significant since these structures have a high surface-to-volume ratio. In our structures, the Ge NWs are in contact with the atmosphere and therefore they develop a thin layer of GeO_2, as depicted in the figure [36].

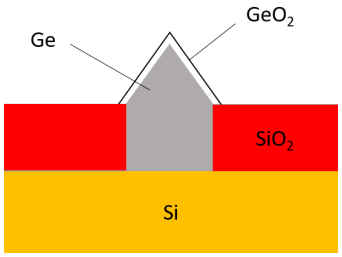


Figure 4.12: Scheme of the presence of the GeO_2 in the NWs.

4.3.2 Si capping: approaches

The presence of this GeO_2 layer is therefore problematic and its presence needs to be avoided. A possible solution consist to deposit a capping layer that can passivate the nanowires, preserving the electronic and transport properties.

Silicon is a suitable candidate for this role. A thin layer is deposited not only to protect physically the surface from the oxidation, but also to confine carriers (holes) in the Ge core, thanks to the type II band alignment that will be formed (figure 2.4) [38].

In order to deposit the Si thin film, two different approach were studied:

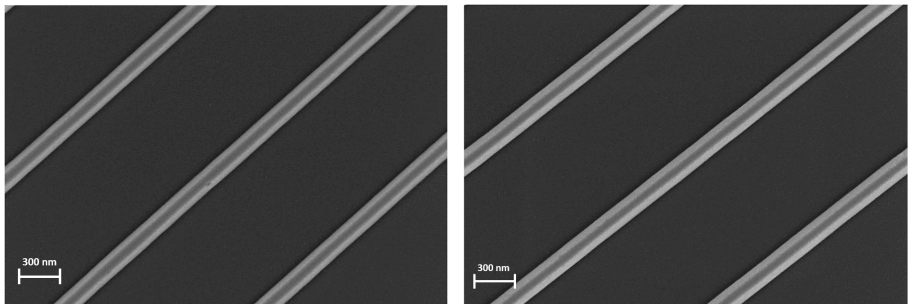
1) Deposit amorphous Si (a-Si) via PECVD followed by an annealing step [14];

2) Flux directly into the MOVPE reactor the Si precursor (Si_2H_6) after the Ge growth to form directly a crystalline Si layer (c-Si) [15][7].

1) a-Si and annealing

Before starting depositing the Si layer, it is necessary to remove the GeO_2 native oxide on the structures and therefore an HCl 37% dip is performed [39]. Subsequently,

the NWs are quickly transferred in the PECVD machine where a deposition of 5 nm of Si capping will be performed. The precursor used is a Si-rich plasma made of 2% of SiH_4. After the deposition, annealing is performed in forming gas at 600°C for 1 minute to crystallise the Si.



(a) **(b)**

Figure 4.13: Top view SEM image of 50 nm nominal width Ge/Si core/shell NWs (a) after PECVD of a-Si and (b) after 1 minute annealing at 600°C.

From the SEM results, it is possible to understand that deposition of the a-Si (left image) is conformal and no problems of de-wetting occurs. Moreover, this conforming coverage of the NWs is kept after the annealing step, since no differences can be noted between the two images.

2) c-Si

The other approach consists in directly deposit crystalline silicon (c-Si) on the Ge NWs right after the growth in the same MOVPE reactor. This consists in sending silane, that will decompose and free Si, without breaking the vacuum and not permitting Ge to oxidise quickly. Critical parameter results to be the temperature set for the Si deposition. A fist attempt to the growing the Si shell was made at 675°C that is the optimised deposition temperature for Si deposition in the MOVPE facility used. The growth was conducted for 30 seconds to deposit 5 nm of Si shell.

In the figure 4.14 is depicted the EDX-TEM image for two <100> NWs with 5 nm of a-Si (a) and 5 nm of c-Si (b). On the right side is plotted an evaluation of how the concentration of various atomic species changes at the interface.

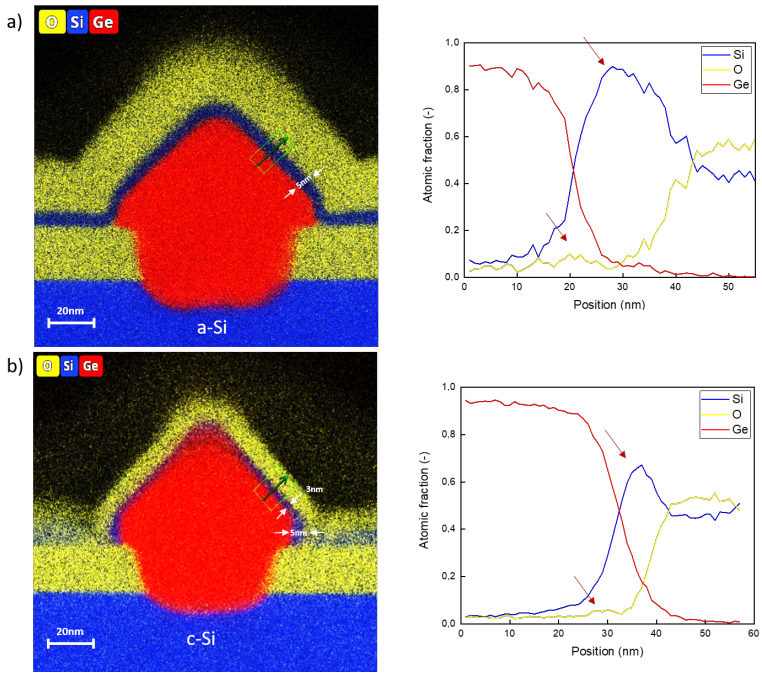


Figure 4.14: TEM-EDX cross-section of 50 nm nominal width NW and respective atomic concentration along the Ge/Si interface for the case (a) a-Si, annealed at 600°C and (b) c-Si, grown at 675°C.

Analysing the case of a-Si, what can be seen is that HCl, plus 3 seconds of Ar milling, works well to remove the native Ge oxide and a 5 nm of Si is successfully deposited on the Ge core with a good homogeneity of the thickness in all the crystalline faces that the NWs shows. Moreover, the Ge/Si interface formed is abrupt. In fact, high content of Si (around 90%) are registered at the interface, that means low intermixing between the two species.

However, despite the HCl dip, a non-negligible amount of oxygen is (around 10%) is still present at the Ge/Si interface, surface treatment was not enough to remove the native GeO_x mixed oxides formed. This results to be critical because the oxide, as mentioned before, will continue to act as a trap state and continuing to react with the Ge core [40].

For the case of c-Si, there is not a sharp interface with high Si content, like the case of a-Si, but is evident the presence of an intermixing region of SiGe that leads to a measured Si content of about 65%. This means that the shell results to be SiGe alloy that, when exposed to air, oxidise easily, not in a passivizing way like the case of Si, but by permitting oxygen to migrate to diffuse till reach the Ge core.

Moreover, what can further be noted is that in the case of c-Si, the deposition is not conformal because thickness of the deposited shell depends on the exposed crystalline face. Different crystalline faces exhibit a different growth rate: on vertical {100} facets the shell appear to be thicker (5 nm) than on {110} oblique ones (3 nm).

From the two approaches presented, the one that seems more promising results to be the direct deposition of the c-Si. For this reason, we decided to stick with this path.

In order to remove the intermixing and to deposit a high Si content shell, the growth temperature was reduced to 620°C for a 60 seconds deposition. In fact, in this case, since we were outside the optimised growth conditions, the exact Si growth rate was unknown. With the new temperature and the new time, 7 nm of shell is successfully deposited.

In the figure 4.15 is presented the EDX-TEM of the <100> NW with the c-Si shell grown at 620°C with the atom concentration profile at the interface and the SEM images of the NWs for the two direction studied after sample is taken out from the MOVPE reactor.

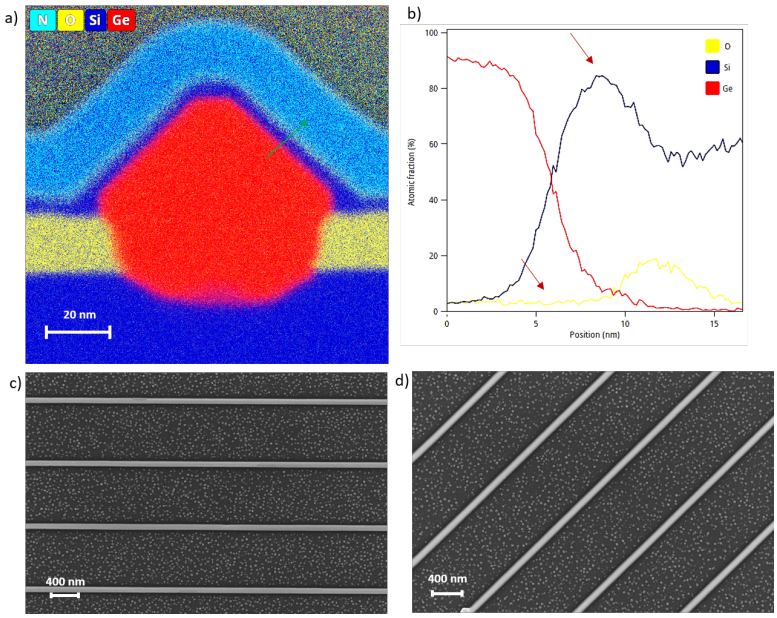


Figure 4.15: (a,b)TEM-EDX cross-section of 50 nm nominal width NW and respective atomic concentration along the Ge/Si interface for the case c-Si shell grown at 620°C and top view SEM images of (c) <110> and (d) <100> Ge/Si NWs.

The most evident and successful result obtained for this case is seen in the atom profile concentration at the interface. In fact, for this case as opposed to the case of c-Si shown in figure 4.14, high Si content are observed (90%) that leads to a pure formation of a Si shell without, or with minimised, intermixing with the Ge core. Moreover, oxygen content at this point results to be practically zero: the shell successfully protect the core from the oxygen diffusion.

In the table 4.3 are presented pros and cons of the two approaches and if the the respective problems are critical or whether they can be resolved in any way.

Table 4.3: Pros and cons of the two approaches used to deposit the Si shell

Approach	**Pros**	**Cons**	**Critical?**
a-Si	Conformal deposition Sharp Ge/Si interface	Natural GeO_2 to remove	Yes, difficult to remove: Ge easily oxidate
c-Si	Same MOVPE reactor No oxygen at the interface	Non conformal and presence of intermixing	No, by decrease the temperature deposition problems are solved

Now, more TEM images of the NWs cross-section grown along <110> and <100> direction from the c-Si sample grown at 620°C are presented respectively in figure 4.16 and 4.17 to further investigate the quality of the Si shell deposited. FFT (Fast Fourier Transform) is evaluated on the Si shell for every different crystalline plane that the capped NW show. Further information and typical results obtained about FFT are reported in the Appendix B.

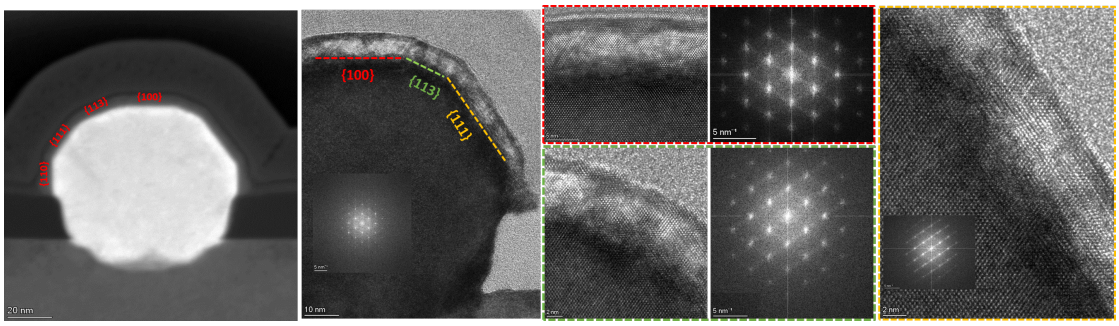


Figure 4.16: HRTEM of NW grown along <110> direction with the FFT evaluated on the Ge core and on the Si shell on the crystalline facet.

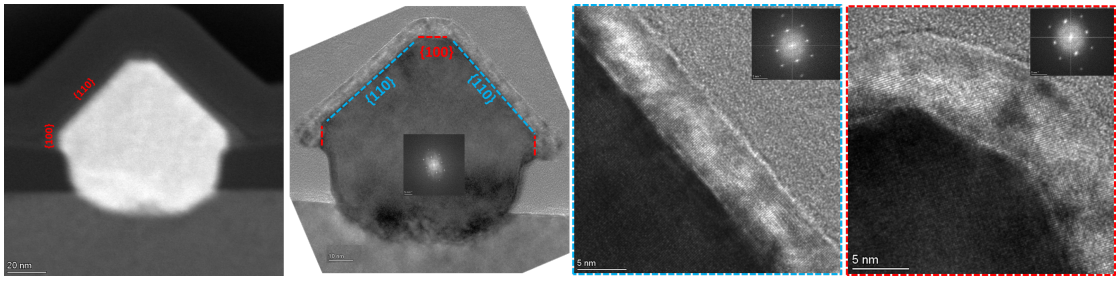


Figure 4.17: HRTEM of NW grown along <100> direction with the FFT evaluated on the Ge core and on the Si shell on the crystalline facet.

From the HRTEM results can be noted that the NWs shape outside the slits strongly depends on the growth direction: <110> NWs present a trapeizoidal shape while for <100> a more triangular-like. In fact, NWs show a different equilibrium shape, depending on the growth direction, with different crystalline planes showed. Concerning the case of the NW grown on <110> direction, by calculating the angle that are formed with the Si substrate, the NW show a top {100} facet and two oblique and high-energy {111} and {113} facets. In the case of the NW grown along the <100> direction, the main crystalline planes exposed is {110} that shows a 45° angle with the substrate. Where the NW touches the mask and for the top-facet, Ge atoms rearrange themselves to form {100} plane.

HRTEM images permit to analyse how the shell grows onto those different crystalline planes. For the the case of the NW grown on <110> direction defects, such as stacking faults, can be easily spotted. Moreover, the FFT measurement evaluated on the Si cap confirm the presence of stacking faults since all the diffraction dots, that confirm the presence of monocrystalline Si, are connected by diffraction lines. These diffraction lines represent how stacking faults typically appear in the FFT (see Appendix B). These lines are particularly presented in the FFT done on the high-energy {111} plane. In contrast, FFT conducted on the core confirm the good quality of the Ge obtained.

In the case of the the NW grown along the <100> direction, especially along oblique {110} facet, a really sharp interface can be noted with a really good continuity between germanium and silicon atoms. FFT also confirms the goodness of the measurement because only diffraction spots, typical of the case of a crystalline material, are depicted with no traces of defects such as stacking faults, twin planes or dislocations. What can be said is that for NWs grown on this direction, defects might be hidden. In fact, stacking faults and dislocation most likely propagate on high-index {111}. For geometrical reason, this plane cannot be seen from the cross-section of a <100> oriented NW [41].

4.4 Transport Properties

In this section, transport evaluation of the the bare Ge NWs will be evaluated.

As reported by S.P. Ramananadan [16], Ge in-plane nanowires grown with the SAG technique turn out to be intrinsically p-doped. This characteristic was already pointed out by S. Zhang et al. [42] for Ge NWs grown by VLS method. What they noticed is that the p-type character is induced by the presence of surface states.

In order to get an understanding of the effect of surface passivation, we tried to compare the room temperature transport properties of Ge NWs with and without Si passivation layer. For this purpose, we fabricated Hall bar devices of Ge and Ge/Si core/shell NWs of varying widths, 50, 80 and 120 nm for both growth direction <100> and <110>, and measured the electrical resistance. The fabrication technique for the device samples results to be the same as the process flow presented in Chapter 3 with some final steps in addition that allow the deposition of the contacts. More details about these steps are presented in the Appendix A. A SEM image of one of these devices, for the case of 50 nm width without Si capping grown on <100> direction is shown in figure 4.18a. Two and four points measurements with a Keithley probe station are conducted to evaluate if these NWs can conduct and which order of magnitude of resistance show. The four point measurement consist in applying a certain voltage between two outermost probes to induce a current. With this current, the voltage between the inner probe is evaluated. By this approach, it is possible to get rid of the contact resistance and having a clean measure of the NWs resistance.

In the figure 4.18b is shown the probe station with the four probes that are approaching the sample. For the case of uncapped NWs, contacts are in Ti/Al/Ti/Au, while for the case of the core/shell the contacts are in Pd. The elements are chosen to ensure an ohmic contact with low resistance for both cases. In figure 4.18c, instead, is plotted a typical I-V curve obtained.

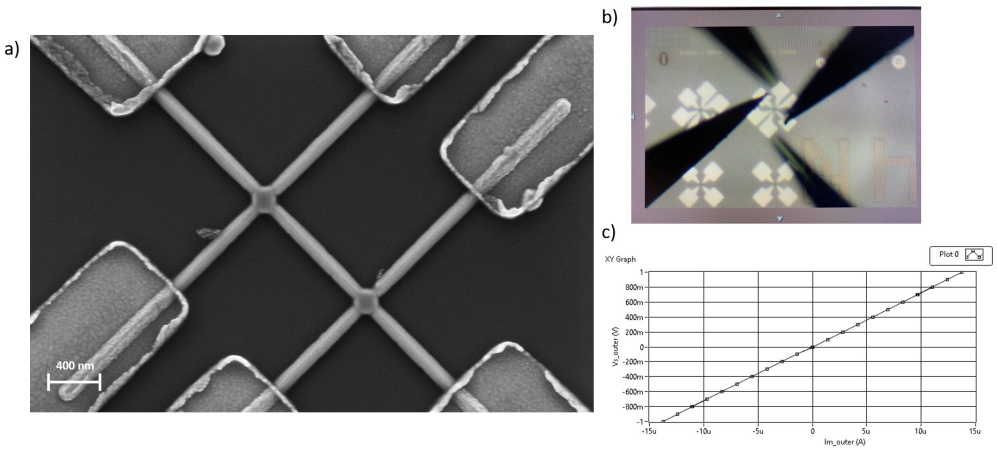


Figure 4.18: (a) Top view SEM image of device sample with 50 nm nominal width, (b) probe station with the four tips approaching the contacts and (c) typical I-V graph obtained when the contact is ohmic.

From the slope of an I-V curve it is possible to extrapolate the value of the resistance (R) of the section through which the current passes. For all the samples evaluated, the classical ohmic I-V curve, a first-order line, was obtained with values of resistance of the order of magnitude of kΩ. This is a confirmation that the NWs conduct and that the contact is ohmic. In the table 4.4, are shown the resistance values obtained for the all the devices measured, for only the Ge core and for the Ge/Si core/shell NWs.

Table 4.4: Resistance values of the NWs

		Ge core		**Ge/Si core/shell**	
Orientation	**Nominal width (nm)**	**R_{2pt} (kΩ)**	**R_{4pt} (kΩ)**	**R_{2pt} (kΩ)**	**R_{4pt} (kΩ)**
<100>	50	142	42	137	45
	80	95	34.3	114	38
	120	80	28	94	30
<110>	50	120	40	149	51
	80	100	33	138	45
	120	73	25	100	33

As expected, the resistance value obtained with the two probe measurement are higher than the ones obtained with the four probes ones. In fact, for the first case, the results is the sum of the resistance of a 3 μm NW and the two contacts, while in the latter it is measured only a 1 μm long NW. Moreover, resistance values scales with the NWs nominal width: larger width shows smaller resistance according to

the formula 4.2.

$$R = \rho(l/A) \tag{4.1}$$

ρ is the NWs resistivity (constant), l represent the NWs length (constant) and A represent the NWs cross-sectional area (not constant). In fact, bigger widths have bigger cross-section that leads to a decrease of the resistance. Moreover, differences between the Ge core sample and the Ge/Si core/shell one can be noticed, in particular, capped NWs present slightly higher values. This increase in the resistance can be addressed to a decrease in the carrier concentration. Finally, NWs grown along the two directions (<100> and <110>) shows comparable behaviour.

From the resistance value of bare Ge NWs, using AFM results to evaluate the cross-sectional area, the order of magnitude of the resistivity can be evaluated (more details in Appendix B).

4.5 Outlook and Future Paths

Thanks to this work, some roads have been investigated but, of course, some questions there are still present and needed to be solved.

Concerning the flat-surface study, further growth for different times, in particular the very nucleation stage and when the wire is fully grown. Moreover, since due to the lattice mismatch between Si and Ge, the growth results to be Stranski–Krastanov (SK) type with layer by layer growth for the first few layers and then switching to island-mode. The switching between the two different modes is because the system can no longer maintain the stain and relaxes by continuing with island growth. At the nanoscale, since low amount of material is present, layer by layer growth-type can be induced without release the stress. If this occur, interesting might be which is the threshold dimension to force this growth behaviour. In figure 4.19 is illustrated how a pattern could look like to study it.

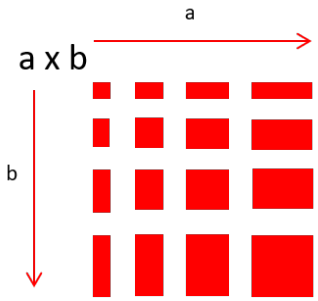


Figure 4.19: Sketch of a possible layout to impress on a Si wafer to study the growth change from SK to LbL (Layer by layer).

Concerning the Si-capped wires, now that the Si growth is optimised, more devices with Ge/Si core/shell NWs can start to be fabricated. Hall measurement can start to be conducted in both Ge bare and Ge/Si NWs in order to obtain information about the evolution of the carrier concentration and the mobility of the holes in the NWs. What can be expected is a decrease of the carrier concentration even though type II band alignment at the interface injects hole in the core. In fact, thanks to the cap, surface states are strongly annihilated and the doping can be easier controlled.

Chapter 5

Conclusion

As mentioned in the previous chapters, the present work was meant to improve the quality of the NWs grown outside the slits using selective area growth approach. Efforts have been made to both improve growth conditions and the substrate preparation. By varying the growth temperature, NWs with the best quality were obtained for 750°C. Post-growth annealing at 800°C might further improve the crystal quality by promoting the dislocations to glide. By adding Al_2O_3 buffer layer and replacing the mask with SiN, smooth and flat Si surface is successfully achieved. On this kind of surface, a potentially pure Stranski-Krastanov growth mechanism can occur and, compared to what happen in the standard fabrication process, it can lead to obtaining higher quality NWs with no stacking faults formation at the critical Si/Ge interface. In addition, lower growth rate found while using SiN as a mask can be used to our advantage since more control over the size and shape of the NWs can be achieved.

Moreover, with the c-Si approach at 620°C previously explained, a thin Si shell around Ge core is successfully deposited without any oxygen trapped at the interface and any intermixing between Si and Ge. However, the shell appear to be defective due to the presence of stacking faults, especially for the NWs grown along <110> on high-energetic facets.

Preliminary transport evaluation conducted on the both uncapped and capped samples shows that the NWs can conduct and posses resistance value comparable, with the order of magnitude of dozens of kΩ. Further Hall measurement are however necessary to evaluate the carrier concentration and mobility, to check whether for both grown-optimised bare Ge core and Ge/Si core/shell samples, any change can be noticed from the values obtained in Santhanu et al. work [16].

Appendix A

Appendix: Process-flow

1) RCA cleaning

1st step: removal of organic residues and organic particles. The wafer is inserted in a mixture of 5 parts of deionised (DI) water, 1 part of ammonia water at 28% in weight and 1 part of aqueous H_2O_2 with 30% of hydrogen peroxide for 15 minutes at 75°C.

2nd step: removal of thin oxide layer. The wafer is dipped in a mixture of 10 parts of DI water and 1 part of HF diluted at 49% for 15 sec at room temperature.

3rd step: removal of metallic species. The wafer is immersed in solution made of 6 parts of DI water, 1 part of HCl at 37% and 1 part of H_2O_2 at 30% for 15 minutes at 75°C [12].

2) E-beam lithography

E-beam tool used within this project is Raith EBPG5000 in the CMi cleanroom. In the figure A.1 is presented a scheme of a e-beam tool and how it works.

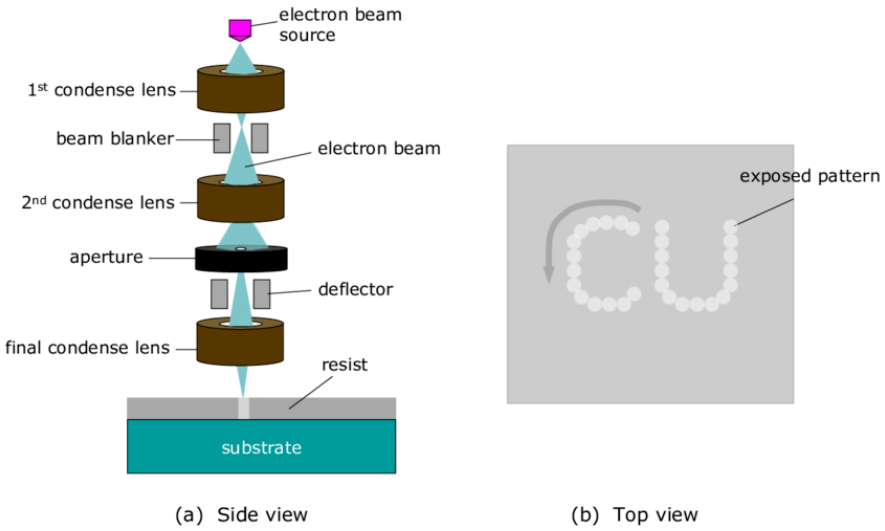


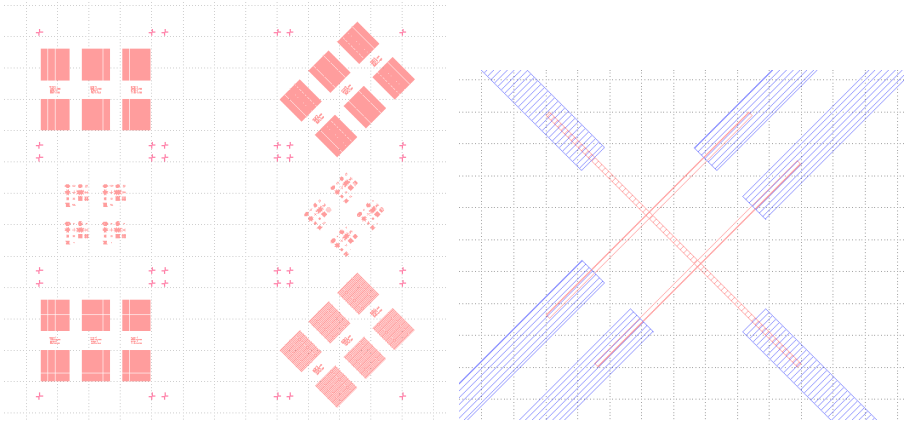
Figure A.1: Scheme of the e-beam column [43].

The machine is equipped with an electron source, similar to the one in the electrical microscope, from which electrons are extracted. The electrons emitted are then accelerated by applying a voltage of 100 keV and the beam is stabilised by a series of electrostatic and electro-magnetic lenses placed around the beam itself. In the final stage, before converging on the substrate, the beam is moved by a final condenser lens that deflect the electrons according to the pattern defined by the .gds file. The beam is kept in UHV to avoid scattering of the electrons with the atom of the air that can reduce the accuracy of the writing.

For our work, we fabricate two different type of substrate:

1st - "Growth substrate": to study the NWs growth by varying geometric parameters and growth direction (focusing on <100> and <110>) depict in figure A.2a.

2nd - "Device substrate": to fabricate the Hall bars to then evaluate the electrical properties depict in figure A.2b.



(a) "Growth" pattern **(b)** Particular of the "Device" pattern

Figure A.2: .gds files of the pattern impressed.

3) Device fabrication: additional steps

After the NWs growth in the shape of Hall bars in order to fabricate the devices, metal contacts need to be deposited at the NWs edges. For this reason, additional fabrication steps need to be added. In figure A.3 those additional steps are schematised.

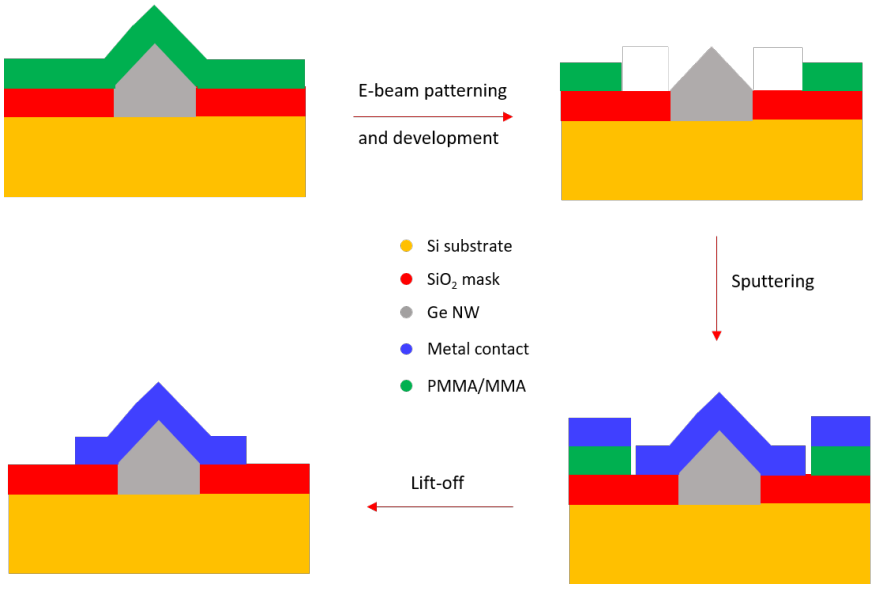


Figure A.3: Scheme of the additional steps of lift-off to deposit contacts to fabricate devices.

So, on the device sample, a layer of PMMA/MMA polymer resist is spin-coated on the whole chip. Then an e-beam exposure is conducted all over the place where the metal contact will be deposited and subsequently the development is performed. Now, a quick HF dip at 1% is performed before putting the sample in the sputtering machine where the particular metal is deposited uniformly all over the chip. Finally, lift-off step is performed: the sample is inserted in a small baker full of acetone and it is subject to ultrasonic sonification for 2 minutes. Acetone will dissolve what is left of the resist and as a consequence, also the metal deposited on the polymer itself will be removed. In the end, on the chip, the metal will stay only in the aperture specially made with the e-beam patterning.

Appendix B

Appendix: Results

1) Growth parameters optimisation: "Classic" and "Modified" MOVPE growth method and

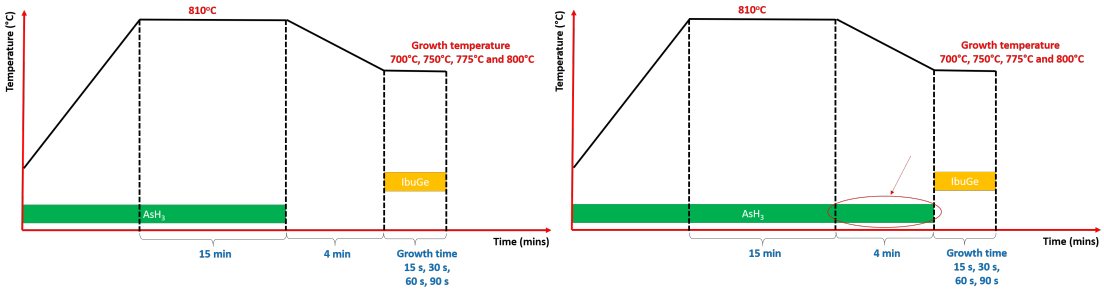


Figure B.1: Graph of the temperature scaling before the MOVPE growth: (left) "Classic" and (right) "Modified"

For both cases, a 15 minutes de-oxidation step at 810°C with arsine flux is performed before the growth. The only difference between the two cases is that in the "Modified" method arsine is kept flow also during the 4 mibutes of cool-down at the growing temperature.

2) Growth parameters optimisation: Raman spectra of the annealed sample at 800°C

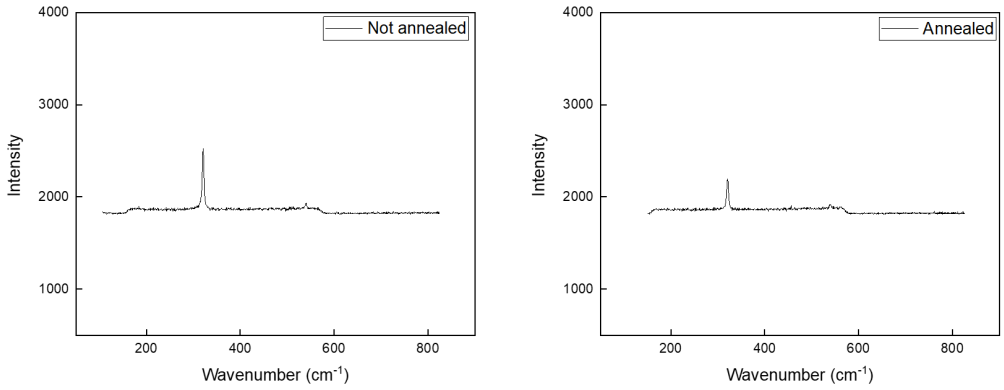


Figure B.2: Raman spectra made on NWs (left) not annealed and (right) annealed at 800°C after the growth sample. In both cases the Ge core is grown at 750°C

The Raman spectra of the annealed sample does not reveal the presence of intermixing at the Ge/Si interface since the peak at 360 cm^{-1} (Ge-Si peak) cannot be noticed.

3) Substrate preparation optimisation: RIE step

Figure B.3 report the AFM profiles for wider width after the RIE step.

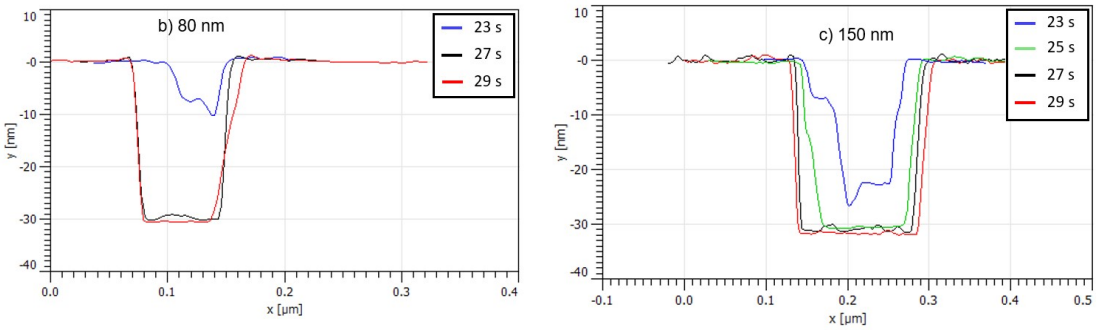


Figure B.3: AFM profiles of (left) 80 nm and (right) 150 nm nominal width after the RIE step.

Also in the case of 80 and 150 nm, for RIE time grater than 25 seconds, 30 nm of depth is reached.

4) FFT (Fast Fourier Transform)

FFT conducted on a TEM image, represent the diffraction pattern of the sample

studied and gives us an idea of the crystallographic structure of material, as shown in figure B.4.

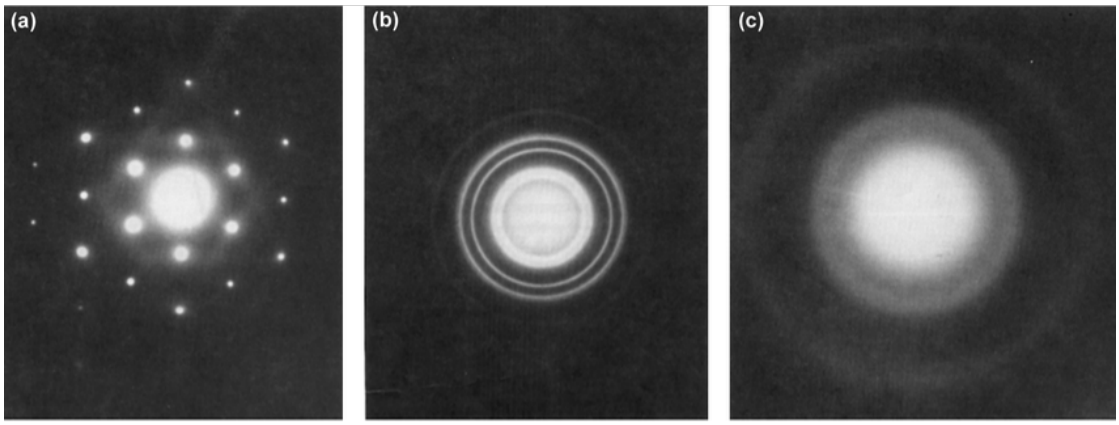


Figure B.4: FFT pattern of (a) mono-crystalline, (b) poly-crystalline and (c) amorphous [44]

In the case of mono-crystalline, the distance between the diffraction dots is related to the interplanar distance in the structure. Any change in the patterns is related to crystallographic defects that can occur in the structure as presented in figure B.5.

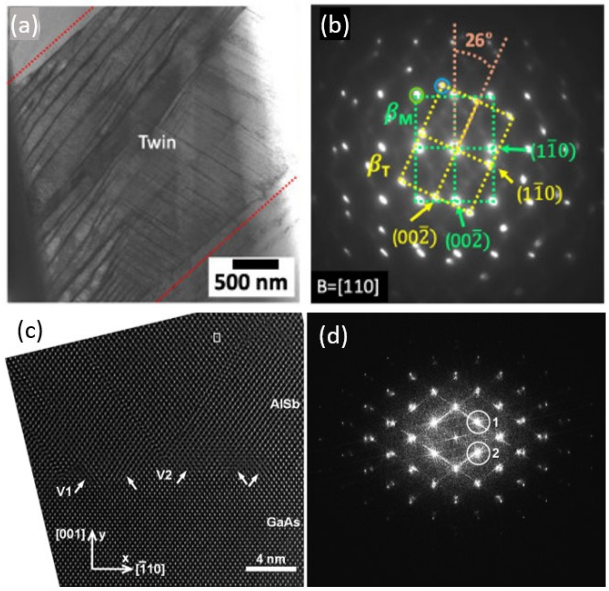


Figure B.5: TEM image of a twin (a) and stacking faults (c) and their respective FFT (b,d) [45][46]

Twins can be spotted by the partial rotation of the diffraction signal while stacking faults are projected in the reciprocal space as lines between the dots.

5) Resistivity and depletion width calculation of the bare Ge devices

For the way of our devices are fabricated, the length where the current flows during the four probe measurement is 3 μm. Using the AFM results performed on these structures, it is possible to calculate the effective cross section where the current flows and, through geometric calculations of the cross-sectional area of the NWs, derive the order of magnitude of the resistivity.

In the figure B.6 are reported the resistivity values obtained for the cases studied.

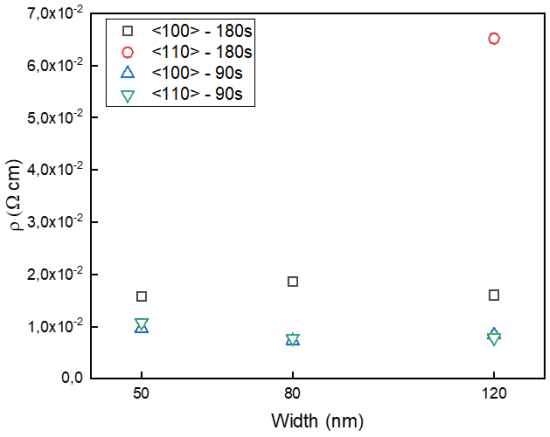


Figure B.6: Resistivity values of the NWs as a function of the nominal width and growing time.

Ge NWs shows a resistivity of the order of magnitude in the range of 10^{-2} comparable to a doped Ge structure that confirm the presence of unintentional doping. In the graph are analysed not only the devices grown for 90 seconds, but also the ones grown for the double of time, 180 seconds, that results to be overgrown. In agreement with the hypothesis, since these structures shows a more extended surface and more defects concentration, their resistivity is increased.

Moreover, with the data from the electrical measurements of the Hall bars grown for 90 seconds, it is possible to evaluate the longitudinal conductance (G*L) with respect to the "real width". The "real width" represent the value of the actual width of the slits in the mask that, due to the fabrication process and in particular the

RIE step, results to be lager than the nominal case.

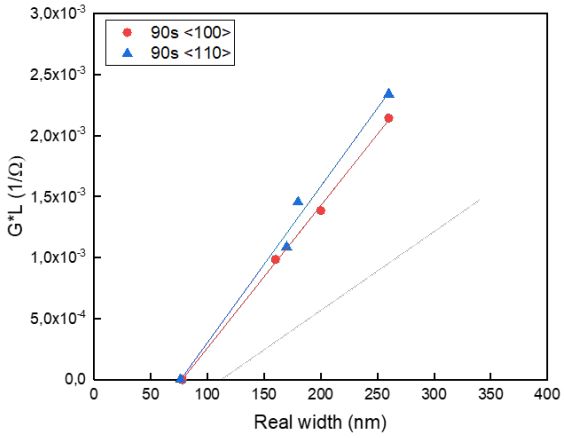


Figure B.7: Longitudinal conductance as a function of the real width of the NWs, highlighting the intercept of the interpolated line with a conductance value equal to zero.

Since the data used to obtain the results plotted are taken from an AFM scan of the devices, aberration due to the tip scan were still present. In order to have a more precise result, deconvolution of the tip is therefore recommended. However, the purpose of this plot is to understand if the NWs can conduct and, in particular, what is the subsequent value of "real width" below which nanowires no longer conduct. For the case reported, this value is around 80 nm for both direction, indicating a depletion region of 40 nm from the interface.

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