POLITECNICO DI TORINO

Master's Degree in Electronic Engineering

Master's Degree Thesis

Tunneling Field-Effect Transistor: digital circuit analysis and ambipolarity impact

Supervisors
Prof. Gianluca Piccinini
Dr. Chiara Elfi Spano
Dr. Fabrizio Mo

Candidate
Roberta Antonina Claudino

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To my brother, who always
encourages me to do my best

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Summary

In the past decades, searches to overcome the limits of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has been carried out. Tunneling Field-Effect Transistors (TFETs) have been considered as a possible candidate to replace MOSFET. Based on band-to-band tunneling, TFET can achieve lower Subthreshold Slope, below the 60mV/dec limit of the MOSFETs, higher I_{ON}/I_{OFF} ratio and so has been considered for low power application. A drawback of TFET is the ambipolarity: the device turns on for both positive and negative voltages applied to the gate. The first part of this work presents the TFET with a description of the qualitative behaviour of the device and the list of advantages and disadvantages. Then, the Notre Dame model is illustrated and an explanation of the work flow for the simulation is shown. The second part of the work consists in the simulation performed in Cadence Virtuoso and the analysis of the results. To understand the impact of ambipolarity in circuit based on TFETs, all the main logic gates were addressed. Some devices affected by ambipolarity shows errors in the logic operations. Thus, ameliorated devices were considered. In particular, devices with symmetric ambipolar transcharacteristics show a correct logic behavior but still have the drawback of a significant greater dissipated power during switching operations in comparison with CMOS logic gates. Only when technological ameliorations are capable of strongly reduce ambipolarity the basic gates permit to achieve all the main advantages of TFET tecnology, e.g., extremely low dissipated power. Future works should be oriented to overcome the intrinsic low I_{ON} of TFET technology to achieve high performance and low power digital circuits.

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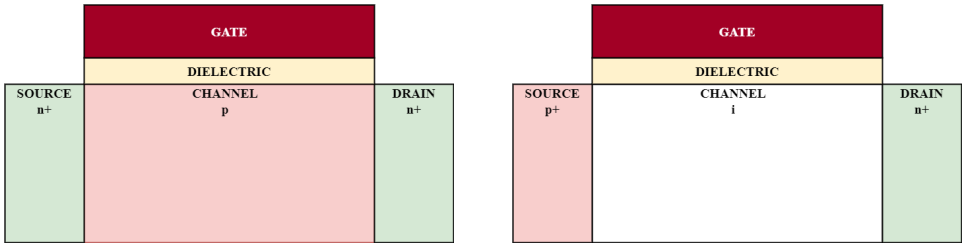
List of acronyms and abbreviations

BTBT	Band to Band Tunneling
FA	Full Adder
FOM	Figures of Merit
HA	Half Adder
LP	Low Power
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SCE	Short Channel Effect
SS	Subthreshold Slope
TFET	Tunnel Field-Effect Transistor

Chapter 1

Introduction

The power consumption and the Subthreshold Slope (SS) are two limits of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) in integrated systems. The request for lower energy consumption leads to a reduction in the power supply (V_{DD}), due to the dependency of the power on V_{DD}^2. These requests causes a progressively scaling of devices. The device scaling leads to an increase in the effect of the Short Channel Effects (SCEs). Research on a possible substitute has been carried out in the past decades. A novel steep SS device has been considered [1]: the Tunneling Field-Effect Transistor (TFET). This device, based on quantum mechanical tunneling, is a promising candidate for overcoming the 60 mV/dec SS limit of MOSFET.



(a) MOSFET (b) TFET

Figure 1.1: Structures of MOSFET and TFET

The TFET structure is shown in fig.1.1 and it is similar to the MOSFET, therefore the fabrication is compatible with CMOS technology. The main difference between the two structures is that in TFET source and drain are doped with opposite types.
The mechanism of carrier injection in MOSFET depends on temperature by thermionic emissions, this limits the minimum operating voltage. TFETs instead are based on Band to Band Tunneling (BTBT) which is a quantum effect where the carriers tunnel from an energy band to another one. A brief comparison of the two carriers injection has been analyzed in [2]. To illustrate the comparison between the two different mechanism transport is possible to refer to the images below. Fig. 1.2 shows the principle of the thermionic emission: the carriers from the source have to overcome the energy barrier

modulated by the gate voltage. Only the carriers in the tails of Fermi-Dirac distributions that have enough energy contribute to the subthreshold current, see fig.1.2. This limits the SS of the MOSFET. On the right of the figure is reported the logarithmic scale of the drain current in the function of the gate voltage, in the corresponding left is reported the energy barriers of the MOSFET.

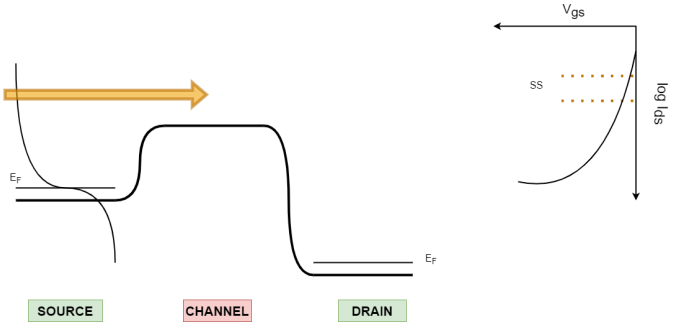


Figure 1.2: Graphic explanation of carrier injection in MOSFET

In fig.1.3 are represented the bands of a TFET on the left, and the logarithmic scale of the current in the function of the gate voltage on the right. To understand why in TFETs the SS is lower we have to look at the valence band at the source in fig.1.3. Only carriers with energy near the Fermi level can tunnel to the channel. The current on the logarithmic scale is not linear dependent on the gate voltage, because the equation of the current depends on the transmission probability to the barrier and the available states in the channels. This is the reason why the SS of TFET is lower than the SS of MOSFET. By changing the transport mechanism , the limit of SS is overcome, indeed the SS of a TFET is lower than the SS of a MOSFET.

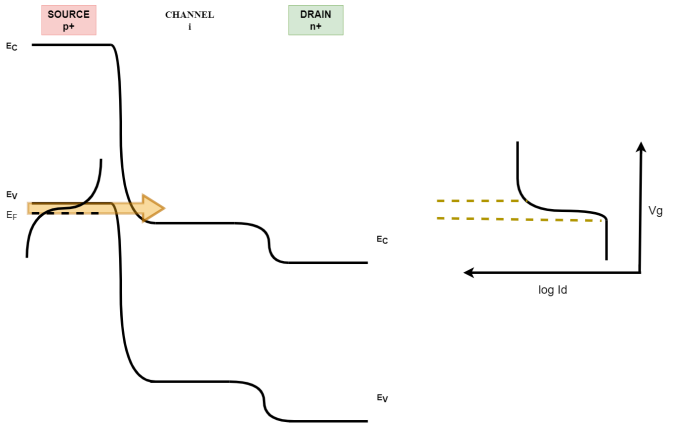


Figure 1.3: Graphic explanation of carrier injection in TFET

Even though these are good characteristics, the TFET presents two drawbacks: the ambipolar current and a low I_{on}. A brief introduction of Tunneling FET is presented in the next chapter.

1.1 Thesis outline

This work aims to understand the impact of ambipolarity on TFET-based digital circuits. To achieve this intent a brief introduction of the working principle of TFETs is necessary and it is presented in the next chapter. Then the model used to perform the simulation is described in chapter 3 and the workflow of the simulations is shown. The results of the simulations are illustrated and commented on in chapter 4. The devices affected by strong ambipolarity for lower positive values v_{gs} show errors in the evaluation of the output. In terms of power, even the devices that shows weak ambipolarity for lower positive values of v_{gs} exhibit an increased dynamic power. It is possible to assert that ambipolarity affects the performance of digital circuits and it is better to reduce it. The other big drawback of TFET is the low I_{ON}. Future works can be focused to improve the ON current.

Chapter 2

Tunneling Field-Effect Transistor

2.1 Device structure

The Tunnel Field-Effect Transistor (TFET) is a gated P-I-N device. The source and the drain region of a TFET are heavily doped of opposite types. In a n-type TFET the source is p-doped and the drain is n-doped. The TFET is based on Band To Band Tunneling (BTBT) phenomenon.

Fig.2.1 shows the n-type structure of a TFET.

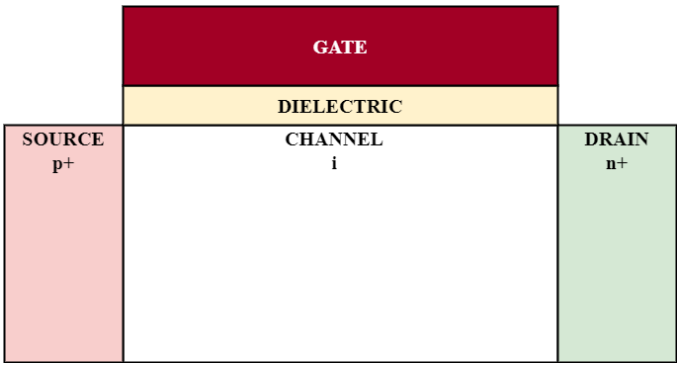


Figure 2.1: n-type TFET.

In a TFET, interband tunneling can be switched ON and OFF abruptly by controlling the band bending in the channel region by means of the gate bias.
The basic device is divided into three regions, the source, the channel, and the drain. The source region is the source of the majority carriers, the channel usually is an intrinsic region and it is used to turn ON the device, and the drain collects the majority carriers. The Tunneling (or Transmission) Probability T is given by the Wentzel-Kramer-Brillouin (WKB) approximation:

$$T_{WKB} \approx \exp\left(\frac{-4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g + \Delta\Phi)}\right)$$

where

- λ is the screening tunneling length
- m^* is the effective mass
- E_g is the energy gap
- q is the charge of the electron
- $\hbar$ is the Plank constant
- $\Delta\Phi$ is the overlap of the energy bands

The Transmission probability strongly depends on the device geometry and material choice. Different materials of the body cause a different E_g and effective mass. Instead the selection of the dielectric, in material and thickness, results in a variation of the value of the screening tunneling length:

$$\lambda = \sqrt{\frac{\epsilon_{si} \cdot t_{si} \cdot t_{ox}}{\epsilon_{ox}}}$$

Due to the large energy band gap, the silicon is not the best choice as channel material. The I_{on} current could be improved by using a material with a small E_g since the dependency of the tunneling probability is exponential.

2.2 Qualitative behaviour

In this section, the qualitative behavior of the band diagrams has been analyzed to define the different working regions of an n-type TFET.

2.2.1 Thermal equilibrium

In the following image is shown the band diagram of the structure at the thermal equilibrium. Since the device is heavily doped, for the p+ region the Fermi level is placed closely to the valence band, for the n+ region it is placed closely to the conduction band. Without external bias, the Fermi levels are aligned and there are two depletion regions, one on the source-channel region and one on the drain-channel region, as shown in Fig. 2.2

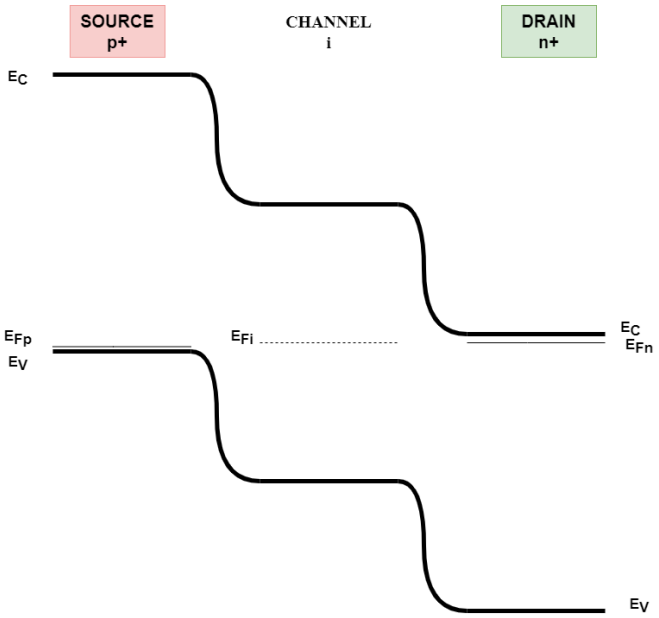


Figure 2.2: nTFET band diagram in thermal equilibrium

Since there is no overlap between the bands of the source and the gate, there is no possibility of tunneling in the structure.

2.2.2 OFF state

The OFF region is shown in fig.2.3 when a positive v_D is applied. In this OFF state, there is no tunnel effect since the valence band of the source is above the valence band of the channel and under the conduction band of the channel, there are no available energy states for the electrons. In an nTFET, there are few electrons in the conduction band of the source since it is p-type, so few electrons can be injected in the channel. This leads to a very low OFF current collected in the drain.

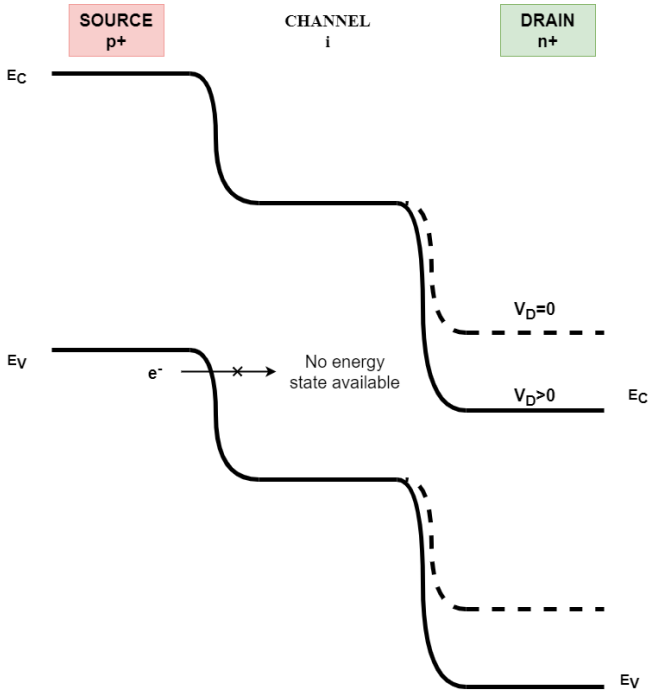
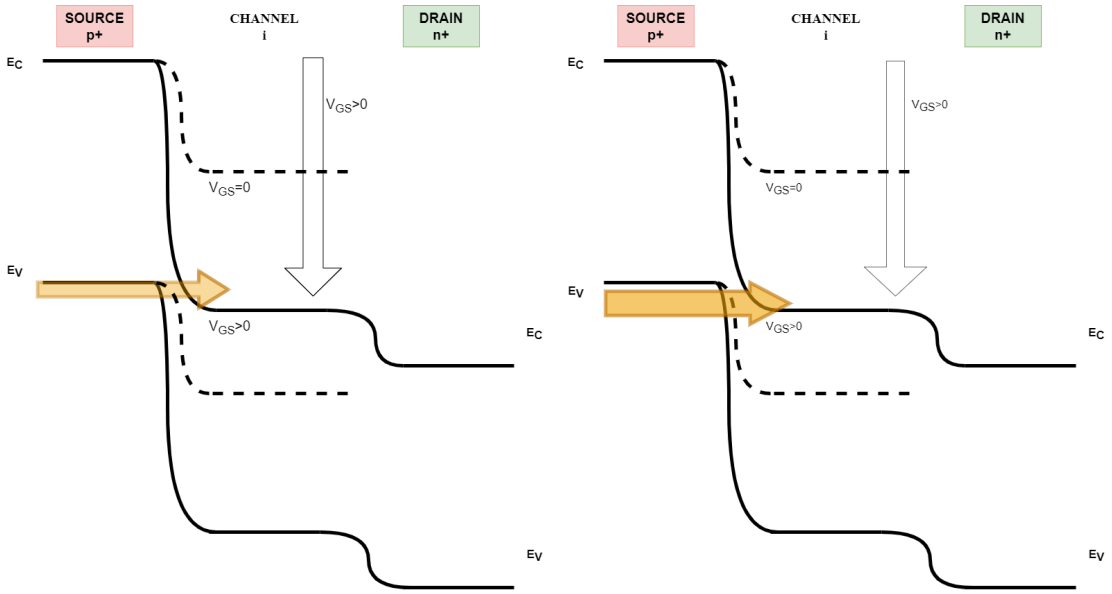


Figure 2.3: nTFET band diagram in OFF state

2.2.3 ON state

When a voltage is applied to the gate, this causes bending in the band diagrams. In particular, if a positive v_{GS} is applied this will push down the barrier under the gate. This operation will result in an alignment in the bands, the conduction band of the channel with the valence band in the source, as shown in fig.2.4. With increasing v_{GS} a band-to-band tunneling phenomenon appears between the electrons in the valence band of the source and the conduction band of the channel, leading in a current flow exiting from the drain. So when a higher positive v_{GS} is applied, the carriers in the conduction band of the channel are swept to the drain terminal by the positive bias of the drain, generating a current flow. An higher v_{GS} will produce an increase in the current since the tunneling length will decrease. The effects of a positive v_{GS} can be observed in fig. 2.4



(a) inital of ON state

(b) deep on ON state

Figure 2.4: nTFET band diagram in ON state

2.2.4 Ambipolar state

If a negative v_{GS} is applied, the bands under the gate will be pushed up, leading in a current flow due to tunneling in the carriers from the valence band of the channel to the conduction band of the drain as shown in fig. 2.5. This behaviour is called ambipolarity because the device is ON both for positive and negative gate voltages.

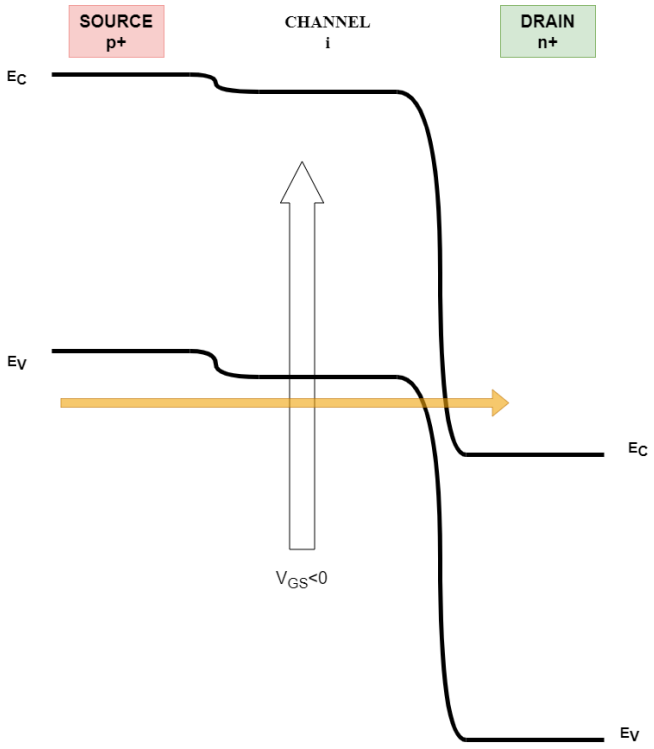


Figure 2.5: nTFET band diagram in ambipolar state

2.3 Issues and solutions

TFETs are promising devices in terms of SS, power consumption, and I_{OFF}. Two of the major drawback of this device are the low I_{ON} and the ambipolairty. The drain current from Launder's equation is described as

$$I_d = A \int_{E_c}^{E_v} [F_S(E) - F_D(D)] \cdot T(E) \cdot N_S \cdot N_D dE$$

Where $F_S(E)$ and $F_D(E)$ are the source and the drain Fermi-Dirac distribution, N_S and N_S are the density of States and T(E) is the transmission probability [3]. From the formula of the current, some consideration can be taken to increase the drain current. The strong dependence on the WKB approximation suggests an analysis to exceed the drawback of the low ON current.

$$T_{WKB} \approx \exp\left(\frac{-4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g + \Delta\Phi)}\right)$$

To increase the value of the current, λ and E_g has to be the lowest possible. Both the parameters are dependent on the utilized material. In [4] is established that the WKB approximation works properly in structure with direct bandgap semiconductors, such as InAs, but has limited accuracy in indirect bandgap semiconductor materials or where other quantum effect phenomena, such as PAT (phonon-assisted tunneling), become dominant. For TFET usually a hetero-structure is chosen, the direct bandgap and the low E_g are suitable for the device. Another possible solution to enhance the I_{on} current is a high-k dielectric for the gate insulator. This will increase the electrostatic coupling between the gate and the tunneling junction [5]. This is because if we use an high k material, with a thinner layer we are increasing the capacitance $C_{OX} = \frac{\epsilon_{OX}}{t_{OX}}$. The advantage of using a high-k material in a TFET is that a low equivalent oxide thickness can be obtained without decreasing the physical thickness of the gate, thus avoiding the problem of direct tunneling of the carriers through the gate. Another solution to increase the current could be the double gates, this solution will improve the electrical coupling of the gate with the channel.
Due to ambipolarity the devices conduct current even for negative values of v_{GS}. This is an undesired effect for circuits based on complementary logic. Since the advantages of TFET, low SS and I_{OFF}, bring the device to be an optimum candidate for low power and high-frequency application, many solutions have been carried out to solve this issue [6], some of them are reported below:

- Gate Engineering: consists of a split into two regions the gate. The gate region that controls the tunneling in the source-channel region is the tunneling gate, the gate region that prevents the tunneling in the drain (i.e. ambipolarity) is the auxiliary gate. The two gates are characterized by a different choice of a metal gate, in this way, even if the same voltage is apply the banding of the bands is different.

- Gate-drain Underlap Engineering: consists of a gate shorter than usual. The gate does not reach the drain, in this way the bands are not so influenced by the voltage applied and the ambipolar current is suppressed.

- Spacer Engineering: the coupling between drain and gate is decreased by the presence of a low-k spacer.

The reported solutions are only some of the many possible technological solutions. There is the possibility to combine more techniques together.

Chapter 3

Methodology

The aim of this chapter is to present the model used in the simulation, the well-established Notre Dame TFET Model[7], and to describe the work flow in Cadence Virtuoso.

3.1 Notre Dame TFET Model

To allow performance evaluation in low power applications a universal analytical TFET spice model has been developed by Lu et al. [8]. This model includes equations for the descriptions of the behaviour of a TFET device in the all operating region, and it is implemented in Verilog-A. The Notre Dame TFET model is a semiempirical model: starting by the data obtain from a device simulation, by mean of several fitting parameters, a set of equation is implemented in Verilog-A to allow circuit simulation. The model includes also a charge-based capacitance model, a gate tunneling current model and a noise model [9].

3.1.1 Drain current

The drain current of a TFET depends on both V_{GS} and V_{DS},in this model four different working conditions are described :

- $V_{GS} > 0$ and $V_{DS} > 0$ defining the drain-source tunneling current I_{dst}
- $V_{GS} < 0$ and $V_{DS} > 0$ defining the drain-source ambipolar current I_{dsa}
- $V_{GS} < 0$ and $V_{DS} < 0$ defining the diode current
- $V_{GS} > 0$ and $V_{DS} < 0$ defining the Esaki drain-source tunneling current

In this work only the drain-source tunneling and ambipolar currents are analyzed. For the sake of simplicity the other parameter and equations of current are not reported in this work,it is possible to refer to the model [7].

Drain-source tunneling current I_{dst}

The equation of the drain current in the TFET model is an experimentally well-established expression for band to band tunneling:

$$I_{dst}(V_{gs}, V_{ds}) = a \cdot f \cdot E \cdot U \cdot \ln\left(1 + e^{\frac{V_{gt}}{U}}\right) \cdot e^{-\frac{b}{E}}$$

with

$$a = \frac{W \cdot TCH \cdot q^3}{8\pi^2\hbar^2}\sqrt{\frac{2m^*}{qE_g}}$$

and

$$b = \frac{4\sqrt{2m_r^*}E_g^3/2}{3q\hbar}$$

where

- m_r^* is the reduced effective mass;
- E_g is the semiconductor band gap;
- W is the channel width;
- TCH is the channel thickness;
- f is a undimensional parameter based on the Fermi function;
- E is the elctric field in the tunneling junction;
- U is the Urbach factor, linear function of the gate-source voltage;
- $V_{gt} = V_{gs} - V_{th}$.

Ambipolar drain-source tunneling current I_{dsa}

The ambipolar current is modelled ad a scaled and shifted version of I_{dst}

$$I_{dsa} = s \cdot I_{dst}(-V_{gs} + 2V_{OFF}, V_{ds})$$

3.1.2 Library

The model includes a library with three different structure based on device simulation

- a planar InAs double-gate TFET [11]
- an AlGaSb/InAs in-line TFET [10]
- a GaN/InN/GaN heterojunction [12]

In this work the circuit evaluation of the AlGaSb/InAs structure was implemented in Cadence Virtuoso.

3.1.3 Model Issues

In this work the main issue with the model was the absence of parameters that allow to exploit structures with different doping concentration, geometries or gate variations. In the following table are listed the parameter included in the model to describe the I_{dst} and the I_{dsa}. As shown in the table, there are no parameters that include different metal gate or dielectric gate choice. Being a semiempirical model, without data from device simulations, there is no possibility to generate a simulation of a device from scratch.

Name	Parameter description	Unit	Default
DELTA	Transition width parameter	-	5
E0	Built-in electrical field	V/m	5.27E7
EG	Semiconductor bandgap	eV	0.35
ETA	NDR drain-source voltage sensitivity parameter	-	0.1
GAMMA	Saturation shape parameter	V	0.06
J0	P-n junction saturation current density	A/m^2	1E7
JP	NDR current density parameter	A/m^2	2E8
K	NDR current scale factor	V^-1	2
LAMBDA	Saturation voltage parameter	V	0.19
MR	Reduced effective mass	-	0.012
N1	Sub-threshold ideality factor	-	1.8
N2	Ideality factor of the RTD	-	1.1
R0	Tunneling window parameter	-	0.5
R1	Electrical field parameter	1/m	0.01
R2	Electrical field parameter	1/m	1.3
RDW	Drain access resistance per unit width	$\Omega\mu$m	0
RGWL	Gate access resistance per gate square	Ω	0
RSW	Drain access resistance per unit width	$\Omega\mu$m	0
S	Ambipolar current attenuation	-	1.0
TCH	Channel thickness	m	5E-9
VOFF	Minimum valid gate-source voltage	V	0.01
VP	NDR parameter	V	0.05
VTH	Threshold voltage	V	0.17

Table 3.1: List of parameters

3.2 Work flow

The device used for the simulation was AlGaSb/InAs [10], shown in the fig 3.1. In this structure the gate electric field is oriented to be in the same direction as the tunnel junction field. This structure is optimized to suppress ambipolar current. As described in chapter 2, many solutions to face drawbacks are combined together: the structure is an heterostructure to obtain a lower E_g and so an higher I_{ON}, there is the presence of the spacer and also the gate-drain underlap to suppress ambipolarity.

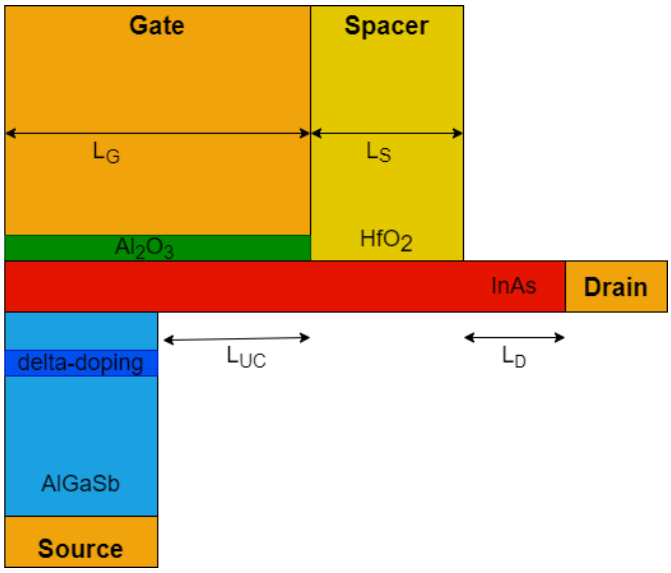


Figure 3.1: Cross section of the device AlGaSb-InAs

The structure in Fig 3.1 is characterized by :

- metal gate ($\Phi_M = 4.93eV$) with a length of L_G
- gate oxide Al_2O_3, $EOT = 0.6nm$ thickness=1.4nm
- spacer HfO_2 with a length of L_S and an underlap L_D
- source p-type AlGaSb doping $4 \cdot 10^{18} cm^{-3}$, there is a $\delta-$doping plane doping $6 \cdot 10^{12} cm^{-3}$
- channel n-type InAs doping $5 \cdot 10^{17} cm^{-3}$ undercut of L_{UC}

The undercut L_{UC} allows a steep subthreshold. To reduce the ambipolarity an underlap spacer was used to reduce the gate-drain coupling. In the following table 3.2 are resumed the value of the parameters:

L_G	L_{UC}	L_S	L_D	EOT	T_{InAs}
20nm	10nm	10nm	10nm	0.6nm	4nm

Table 3.2: Structure AlGaSb/InAs Parameters

The device AlGaSb/InAs in the library is optimized to reduce the ambipolarity. Since the aim of this work is to exploit ambipolarity and understand the problem that it causes, the data in [10] were used as starting point, then the parameters were modified to obtain a characteristic with ambipolarity. In this way a comparison between structure with same performance is possible.
Two different conditions have been taken into account:

a) the device is not optimized for ambipolarity suppression

b) the metal choice of the gate is not optimized to have a symmetric characteristic.

If the device is not optimized to ambipolarity, the s factor present on the formula of the ambipolar current I_{dsa} is set equal to 1. So the characteristic in this case is symmetric respect to the voltage $v_{GS} = 0$. For $v_{GS} < 0$ the device turns ON as for $v_{GS} > 0$.
For the condition b) suppose to have two different work functions $\Phi_{G1} > \Phi_{G2}$. The band diagram of Φ_{G2} results lower than Φ_{G1} leading to a steeper source-channel junction. If the metal work function is different from the chosen one in the structure above, the characteristic can shift to the left or to the right. This because a different choice of the metal causes a different band diagram below the gate in the channel. If the work function is higher or lower the conduction band of the channel will results in different position, this leading to a lower or higher tunneling probability. So the voltage that has to be applied to the gate can be higher or lower, leading to a shift. This results are reported in some article where a structure device simulation has been performed, such as in [11] and [13].
To implement the different structures and emulate the shift due to the different metal gate, a dc voltage, V_{shift} is put in series on the input voltage gate as in Fig 3.2. This simulations result in a shift.

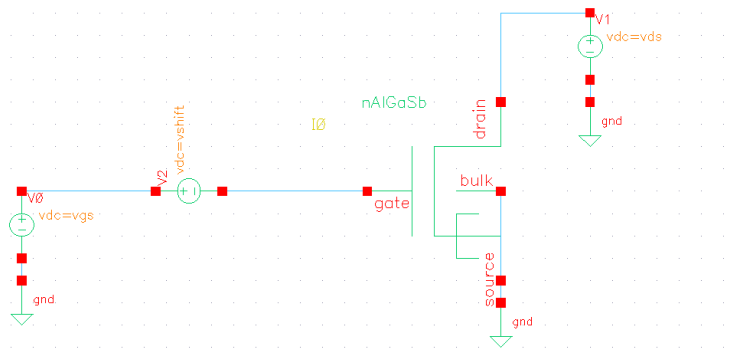


Figure 3.2: Circuit implementation to shift the characteristic

3.3 Figures of Merit extraction

To obtain a comparison between different structures that suffer of ambipolarity and understand the impact of this problem in the circuit evaluation, for each similated device were determined:

- I_{ON} : evaluated as I_{ds} when $v_{GS} = v_{DS} = V_{DD}$
- I_{OFF} : evaluated as I_{ds} when $v_{GS} = 0, v_{DS} = V_{DD}$
- v_{th}: as $\frac{\partial^2 I_d}{\partial v_{gs}^2}$, the method of the peak of the second derivative of the current [14]

For the simulation V_{DD} is chosen equal to 0.5V to allow a fair comparison in term of power between the different structures.
The basic logic cells have been analyzed: INV, NAND, NOR, HA, and FA. For each implemented gate was evaluated the output to ensure the proper functioning and also the consumption power was calculated by the formula

$$P_{switch} = \frac{1}{T}\int_0^T i_{DD} \cdot V_{DD} dt$$

These operations were allowed by the Calculator tool in Cadence Virtuoso. For the logic gates also the digital logic values have been evaluated: $V_{OH}, V_{OL}, V_{IH}, V_{IL}$. The values are represented in figure 3.3.

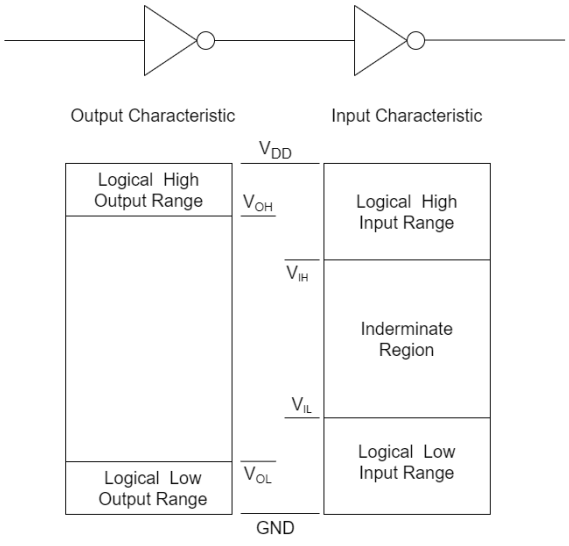


Figure 3.3: Digital Logic values

These values are defined as:

- V_{OH}: minimun HIGH output voltage;
- V_{IH}: maximum HIGH input voltage;

- V_{IL}: maximum LOW input voltage;
- V_{OL}: maximum LOW output voltage.

The method that has been exploited to evaluate these values was the calculation of the points where the derivative of the transfer characteristic of the inverter gate was -1. This work has been done to define when the output of the gates has been considered an error.

Chapter 4

Simulations

In this chapter different TFETs have been simulated. To achieve the aim of the thesis and obtain a comparison of devices that suffer from ambipolarity and the device that have a reduction of this issue, the device AlGaSb/InAs described in the previous chapter is exploited. The main digital cells are analyzed: INV, NAND, NOR, XOR, HA, FA.

4.1 Ambipolar Heterojunction AlGaSb/InAs TFET

To perform the simulation of the devices with ambipolarity the parameter s in the formula of the ambipolar current is set equal to 1 in the model Verilog-A. In this way, the transcharacteristic of the TFETs hold a current even for values of $v_{GS} < 0$. In addition, the transcharacteristic are shifted by the presence of the voltage generator v_{shift}, and simulations have been performed for the values of v_{shift}= 0, 40 mV, 80 mV, 120 mV, 160 mV, 200 mV.

4.1.1 DC Characteristics

In the following figures are reported the simulated transcharacteristics of the n-type TFETs susceptible to ambipolarity. To obtain the graph two generators are placed, one between the gate and the source, v_{GS}, and another between the drain and the source, v_{DS}. Also, the generator v_{shift} is added to shift the transcharacteristic, as shown in fig. 4.1. To obtain the graph in fig 4.2 a DC analysis has been performed. The value of v_{DS} has been imposed, v_{GS} has been swept between $-0.5V$ and $0.5V$ and a parametric analysis has been performed by v_{shift}. In this way it is possible to see in an n-type device, the ambipolar region where the current is also flowing for negative voltages of the gate.

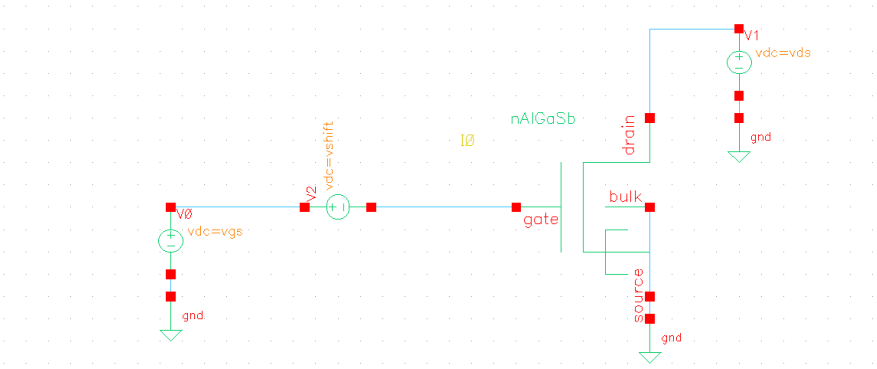


Figure 4.1: Circuit schematic to obtain the transcharacterisic of the devices

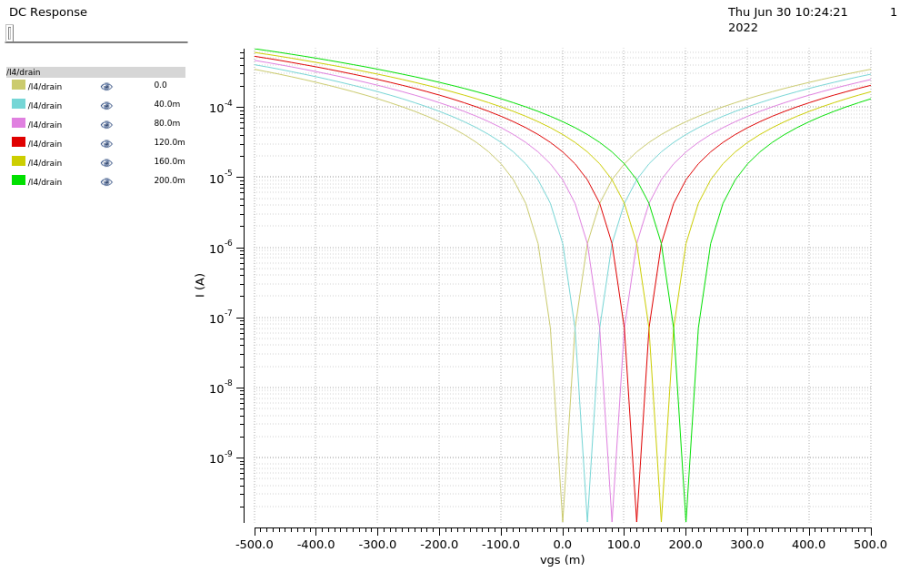


Figure 4.2: Transcharacterisic of the devices for different values of V_{shift}

Fig. 4.2 shows the ambipolarity behavior of the devices: also for negative voltages of the gate, the drain current is flowing. The value of the current is of the same order of magnitude as the I_{ON}. To evaluate the consequences of the presence of ambipolarity, different values of v_{shift} have been chosen. In the case of $v_{shift} = 0\,\text{mV}$ the transcharacteristic is symmetric by the value $v_{GS} = 0\,\text{mV}$ and the device suffers from remarkable ambipolarity. Fig. 4.2 shows the transcharacteristics for v_{shift} =0 mV, 40 mV, 80 mV, 120 mV, 160 mV, 200 mV. When the value of v_{shift} has been increased, the transcharacteristic shifts causing a progressively increase of the I_{OFF}, degrading the I_{ON}/I_{OFF} ratio.

FOMs	V_{shift} [mV]					
	0	40	80	120	160	200
$I_{OFF}[\mu A]$	121.97E-6	1.42	9.30	23.23	41.17	62.73
$I_{ON}[\mu A]$	351.19	298.53	250.54	207.04	167.9	132.93
$V_{th}[mV]$	60	100	140	180	220	260

Table 4.1: FOMs of different structures

Table 4.1 shows these relevant results. The ambipolar device with $v_{shift} = 0\,\text{mV}$ has a low I_{OFF} and an high I_{ON}/I_{OFF}. The other devices, even with a small shift, have a bad I_{ON}/I_{OFF} leading a not so well performance in digital analysis. The transcharacteristic of all the devices have the same performance in terms of I_{ON} and I_{OFF} in case of a p-device or a n-device. This is because the BTBT phenomenon, which regulates the carriers transport, does not depend on mobility, as in the case of a MOSFET. In the following picture, Fig.4.3 are plotted the drain currents of a n-device and the absolute value of the drain current of a p-device, the values of the current are the same.

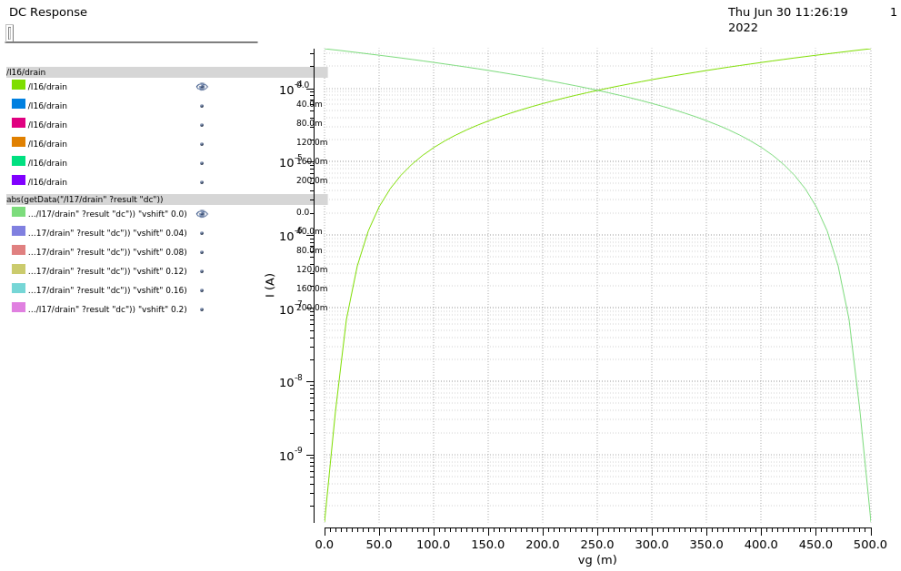


Figure 4.3: Transcharacterisic of a n-device and a p-device with $V_{shift} = 0$

For simplicity, the cases for v_{shift} different from 0 mV are not reported, but the behavior of the couple p-n devices is the same for each value of v_{shift}.

4.1.2 Performance evaluation of basic cells

In this chapter has been evaluated the basic cells: INV, NAND, NOR, XOR, Half Adder (HA) and Full Adder (FA). For each gate, an analysis of the correct functioning and also an evaluation of the power consumption have been performed.

INVERTER

The topology implemented to perform the inverter gate is CMOS-like. In Fig.4.4 is reported the schematic to simulate the devices with the shifted transcharacteristics. Two simulations have been performed: a DC analysis and a transient analysis. The input and the output signals are respectively A and Y. The input signal A is a square wave of 0.5 V amplitude, 1 ns period, and rise time and fall time of 5 ps. The power supply is realized by the voltage generator v_{DD} and it is equal to 0.5 V. Before each transistor it is placed the voltage generator v_{shift}.

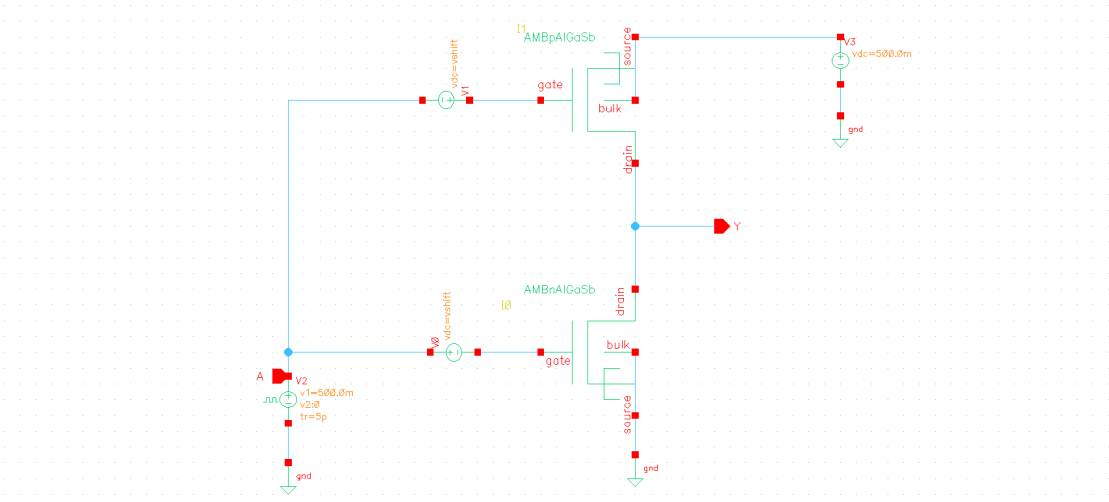


Figure 4.4: Inverter schematic for simulations

A DC evaluation of the gates has been executed to analyze the output and calculate the logic levels. In fig. 4.5 is reported the transcharacteristic of the inverter gate. The red curve shows the output for $v_{shift} = 0\,\text{mV}$. The slope of the curve is not steep. For values of v_{shift} higher than 80 mV is possible to notice a steeper curve, but also a degradation of the outputs. Despite the presence of these lower values of the outputs, the logic operations of the gates are correct.

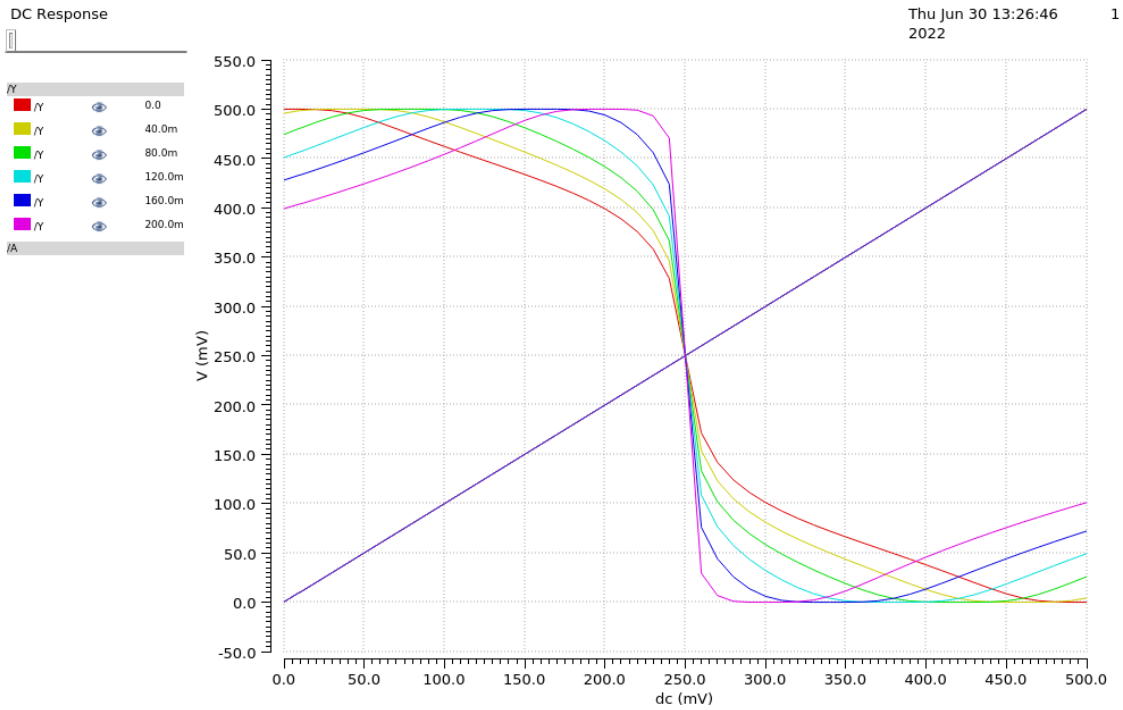


Figure 4.5: Transfer characteristic of INV for different v_{shift}

With the increase of the v_{shift} the slope of the transfer characteristic becomes steeper, but also the outputs are degraded. The logic levels have been evaluated as a reference to understand, for each device, when the output is consider a high or a low value in the logic. This work is useful to understand when hte output is considered an error in that logic. In the table 4.2 are reported the logic values V_{IL}, V_{IH}, V_{OH} and V_{OL} evaluated as described in chapter 3.

Logic Values	V_{shift} [mV]					
	0	40	80	120	160	200
$V_{IL}[mV]$	209.07	206.48	203.3	203.15	215.31	232.47
$V_{IH}[mV]$	300.89	303.5	306.69	306.86	294.68	277.52
$V_{OH}[mV]$	389.72	412.12	437.94	464.33	479.95	487.59
$V_{OL}[mV]$	100.3	77.89	52.07	25.67	10	2.41

Table 4.2: Logic Values of inverter gates in ambipolar device AlGaSb/InAs

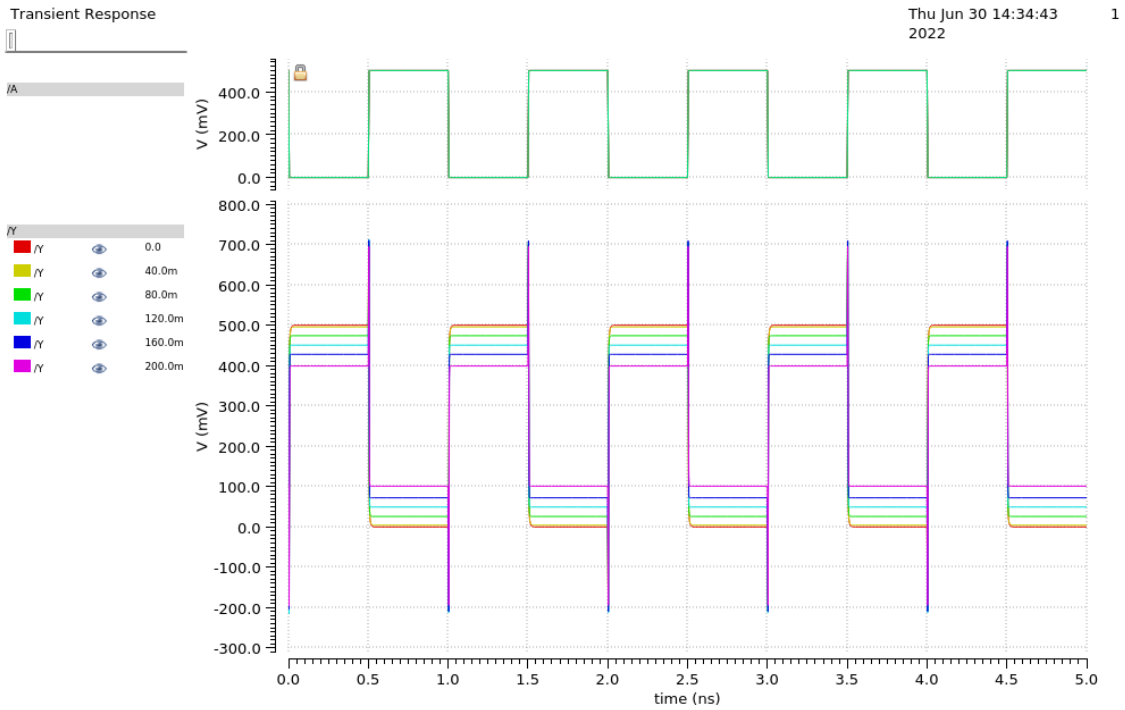


Figure 4.6: Transient analysis of INV for different v_{shift}

The input A and the output Y resulting from the simulation are reported in Fig. 4.6. From the plot is possible to see the correct behavior of the gate: when the input is high the output is low and when the input is low the output is high. As described before, there is a degradation of the outputs for values of v_{shift} higher than 0 mV. The gate with $v_{shift} = 0.2V$ shows the worst behavior, indeed there is a degradation of the logic values, nevertheless, the inverter gate works properly.

NAND

Fig. 4.7 reports the NAND schematic implemented with ambipolar devices for different values of v_{shift}. A and B are the input signals, they are squarewaves of amplitude 0.5 V, and period respectively 1 ns and 2 ns, the rise and the fall time are chosen equal to 5 ps. Before each transistor, there is placed the v_{shift} generator. The output is Y. The supply voltage is the generator $v_{DD} = 0.5$ V. A parametric analysis in function of v_{shift} has been performed to look at the output of each NAND.

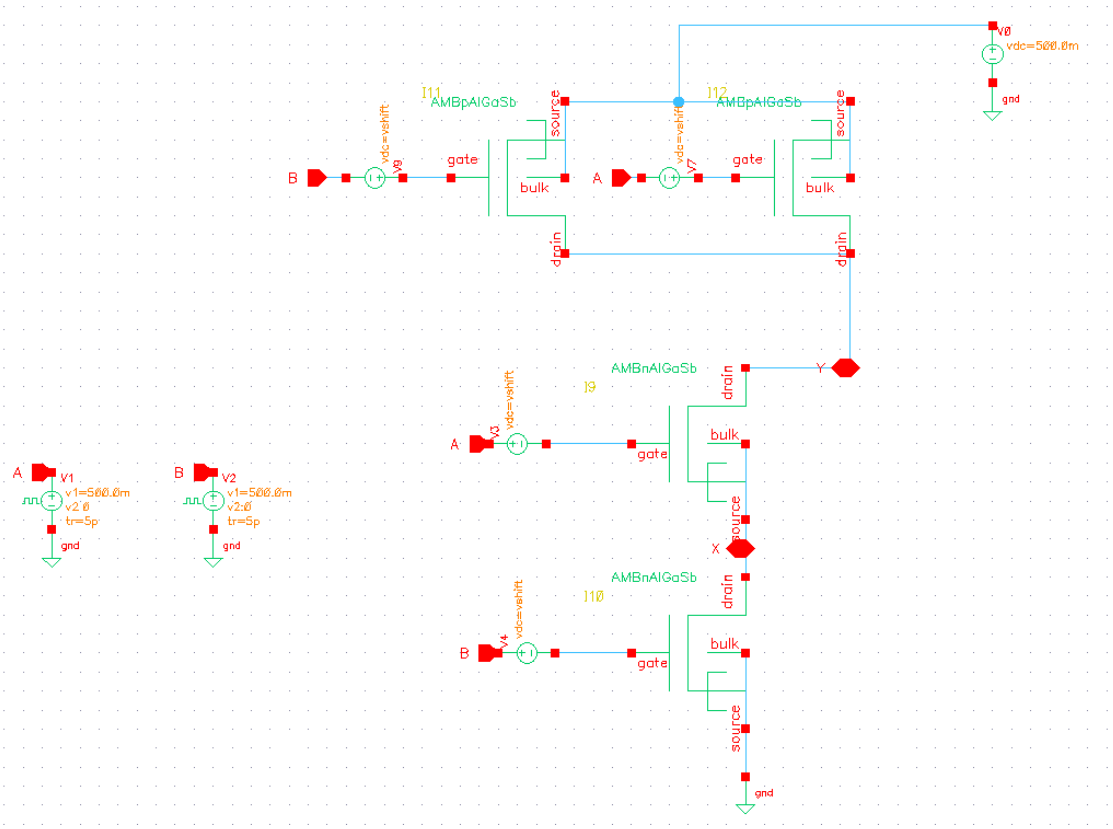


Figure 4.7: Nand schematic for simulation

Table 4.3 reports the inputs and output logic values of a NAND.

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

Table 4.3: NAND truth table

The results of the transient simulation of the NAND gates are reported in the figure below 4.8. The inputs A and B, and the output Y are plotted in the fig. 4.8. The NAND gate based on ambipolar devices present a correct behavior for several values of v_{shift}. For v_{shift} higher than 160 mV there are errors in the output evaluations.

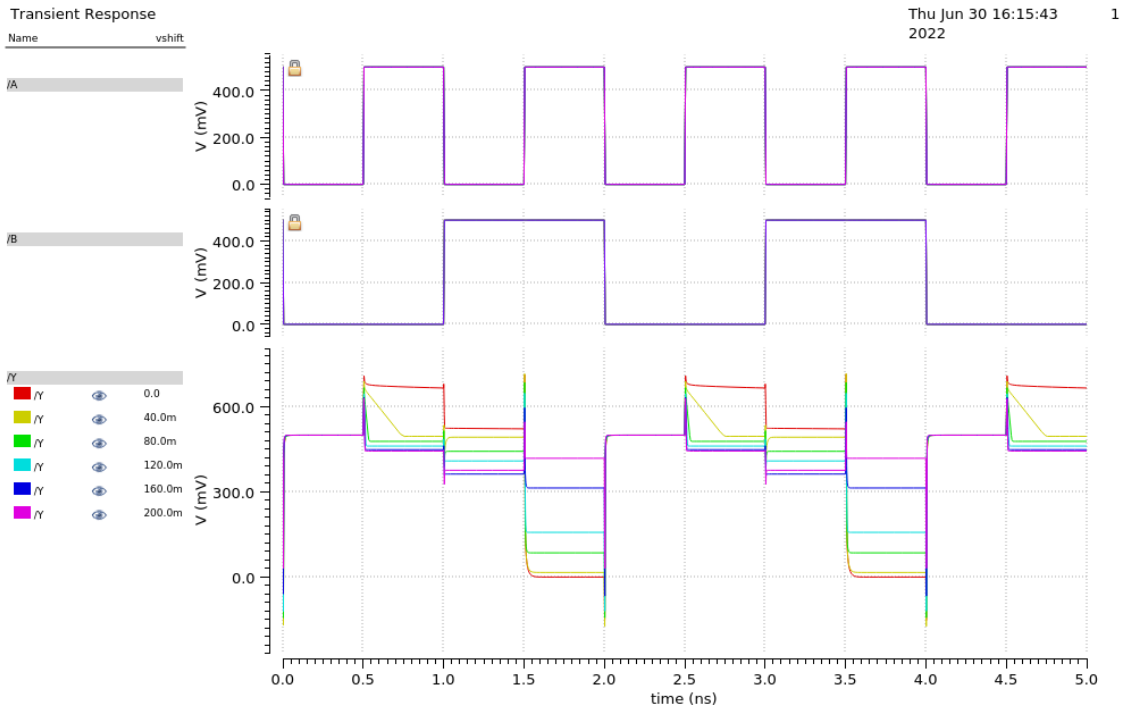


Figure 4.8: Transient analysis of NAND for different v_{shift}

Input		V_{shift} [mV]					
		0	40	80	120	160	200
$A=0$	$B=1$	523.07	492.85	443.06	409.11	362.88	376.23
$A=1$	$B=1$	24.28E-3	16.22	85.34	157.51	313.86	418.44

Table 4.4: Values of the NAND outputs in mV

The table 4.4 shows the values of the outputs when an error shows up for different combinations of the inputs. In particular, when $A=0$ and $B=1$ it is possible to see a decrease in the value of the output as increases of v_{shift}. This is because the n-type device that has as input A, should be OFF, but due to ambipolarity turns ON. This causes a drop on the output voltage for these cases, as shown in the table 4.4, for $v_{shift}=200$ mV $Y=376.23$ mV.
In the case $A=1$ and $B=1$ the output of the NAND should be $Y=0$ logic value as shown in table 4.3. For $v_{shift}=160$ mV and 200 mV, table 4.4 reports the output

values respectively 313.86 mV and 418.44 mV, considered high logic values. This happens because the output is pulled up from the pTFETs, that in this cases are ON due to ambipolarity. This result is also reported in the fig. 4.9 where is represented the current sunk by the voltage supply, it is possible to notice the presence of the current as leakage.

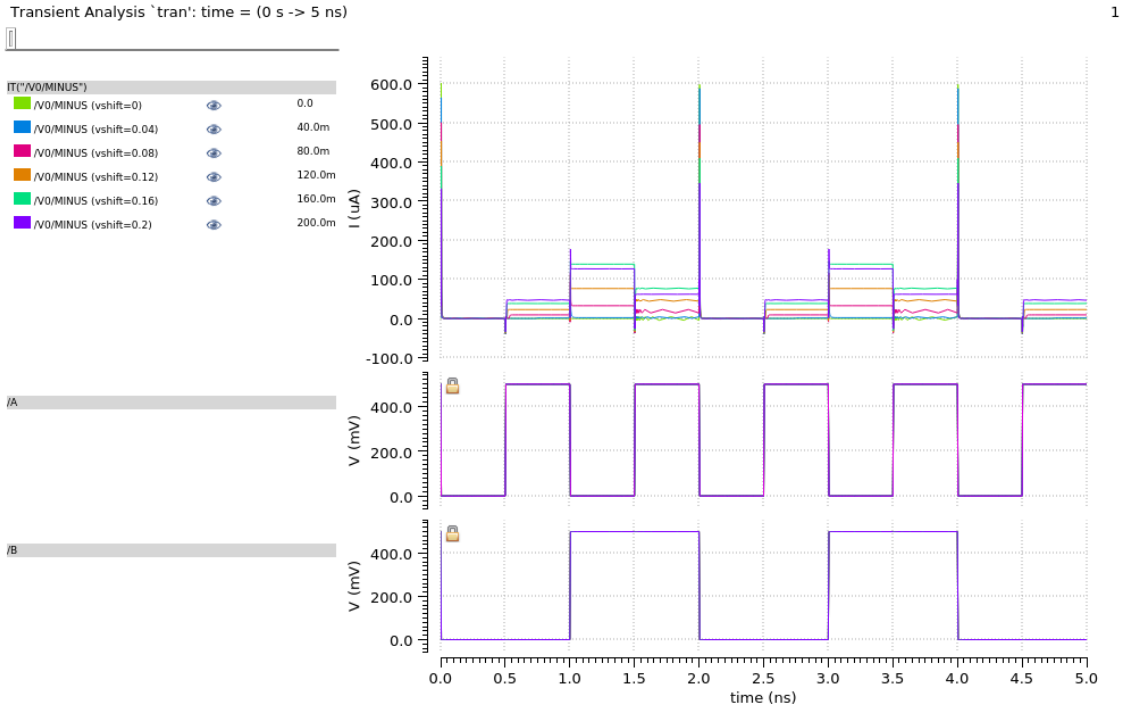


Figure 4.9: Current sunk by the supply voltage in a NAND gate for different values of v_{shift}

FOM	V_{shift} [mV]					
	0	40	80	120	160	200
$P_{dyn}[\mu W]$	413E-3	1.036	7.76	18.24	31.61	29.41

Table 4.5: NAND Dynamic Power

Looking at the current sunk by the supply voltage, it is possible to evaluate the dynamic power as described in Chapter 3. Figure 4.9 shows a static consumption for the devices with v_{shift} higher than 0 mV, this is because there are some devices ON due to ambipolarity. Table 4.5 are reported the calculated dynamic power. The impact of ambipolarity on the dynamic power is evident, there is an increase of three orders of magnitude. As the table shows, there is a significant increase of the power, because there is a leakage of current due to the ambipolar condition.

NOR

The CMOS-like NOR schematic implemented with ambipolar devices for different values of v_{shift} is reported in fig. 4.10. A and B are the input signals, they are squarewave of amplitude 0.5 V, and period respectively 1 ns and 2 ns, the rise and the fall time are chosen equal to 5 ps. The output is Y. Table 4.6 shows the logic values of the NOR gate. A parametric analysis of the function of v_{shift} has been performed to look at the output of each NOR. V_DD is the power supply and value chosen is 0.5 V. Before each transistor, a voltage generator v_{shift} is included to perform the shift of transcharacteristic.

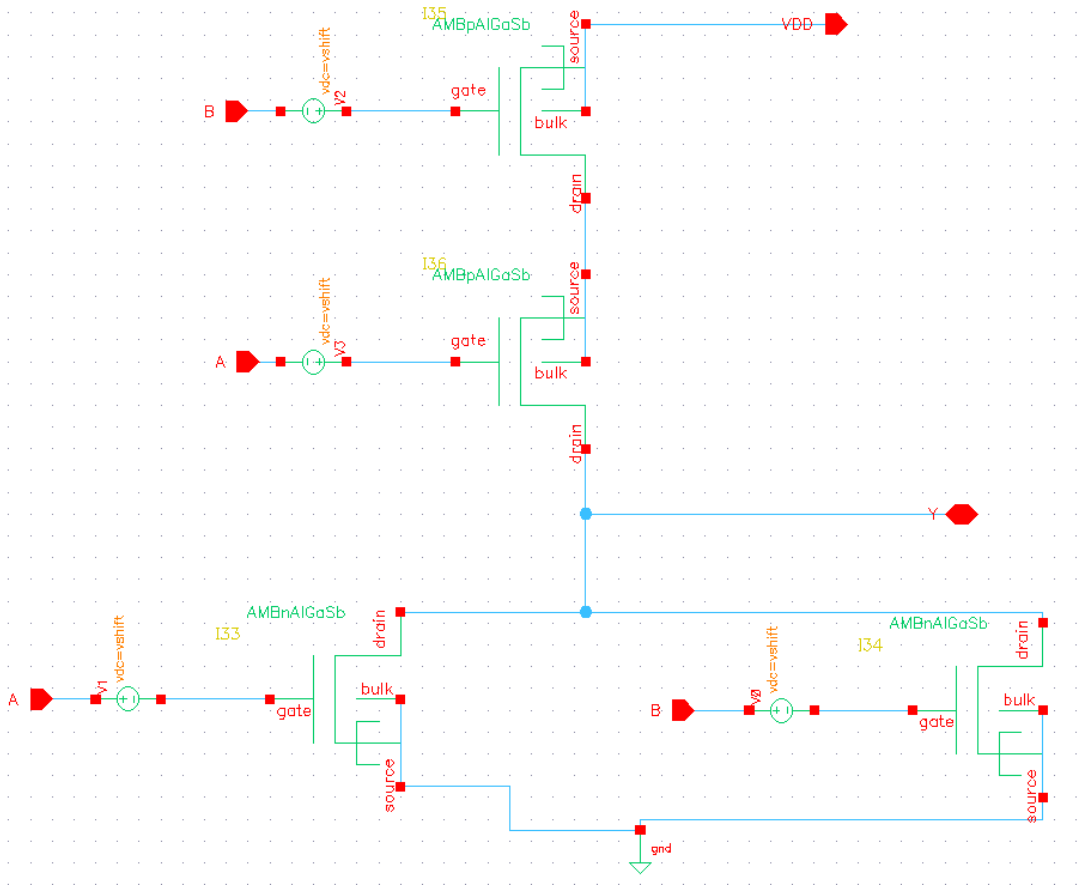


Figure 4.10: NOR schematic for simulations

A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Table 4.6: NOR truth table

Fig. 4.11 displays the transient analysis of the NOR gate. The figure reports the inputs and the output, highlighting errors in the evaluation of the output for value of v_{shift} higher than 160 mV. In particular, when A=0 and B=0 the output has to be high. Increasing the value of v_{shift}, figure 4.11 shows a decreasing in the Y value. This happens because the two nTFET in this condition are on ambipolar condition and so pull down the output. In the table 4.7 are reported the values of the dynamic power of the gates evaluated as described in chapter 3.

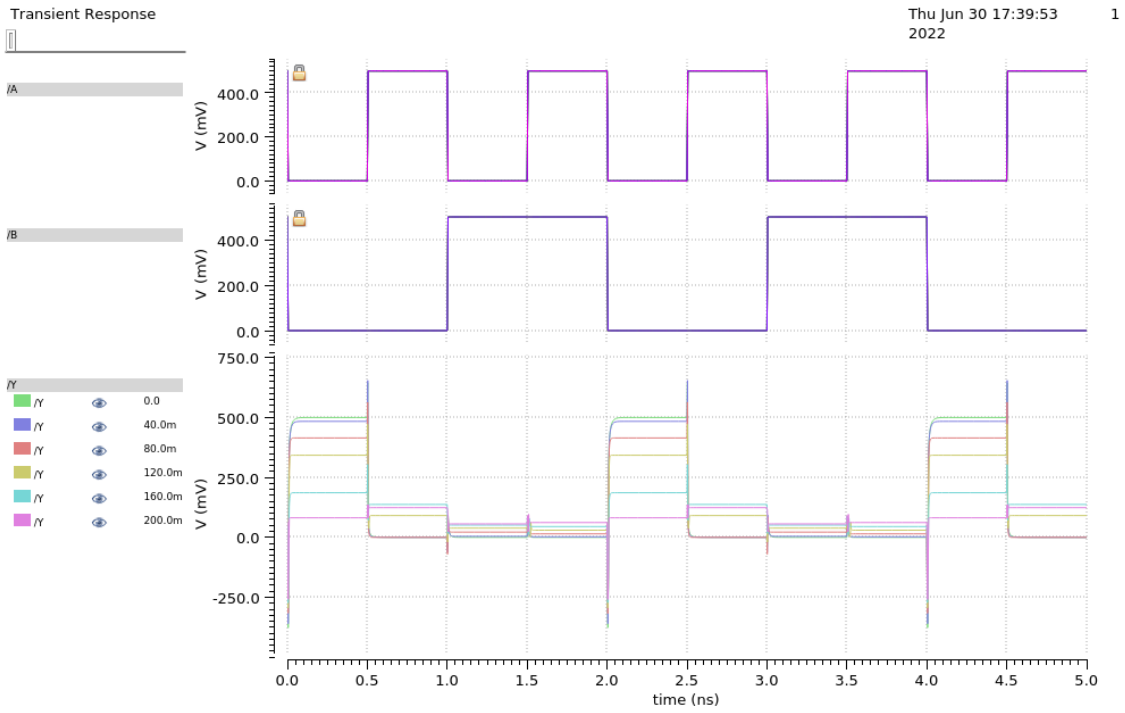


Figure 4.11: Transient analysis of NOR for different v_{shift}

FOM	V_{shift} [mV]					
	0	40	80	120	160	200
$P_{dyn}[\mu W]$	464E-3	957E-3	4.91	20.92	36.53	37.02

Table 4.7: NOR Dynamic Power

The current employed to evaluate the dynamic power sunk by the supply voltage is shown in fig. 4.12. The image reveals a static consumption of power, that show up by ambipolarity.

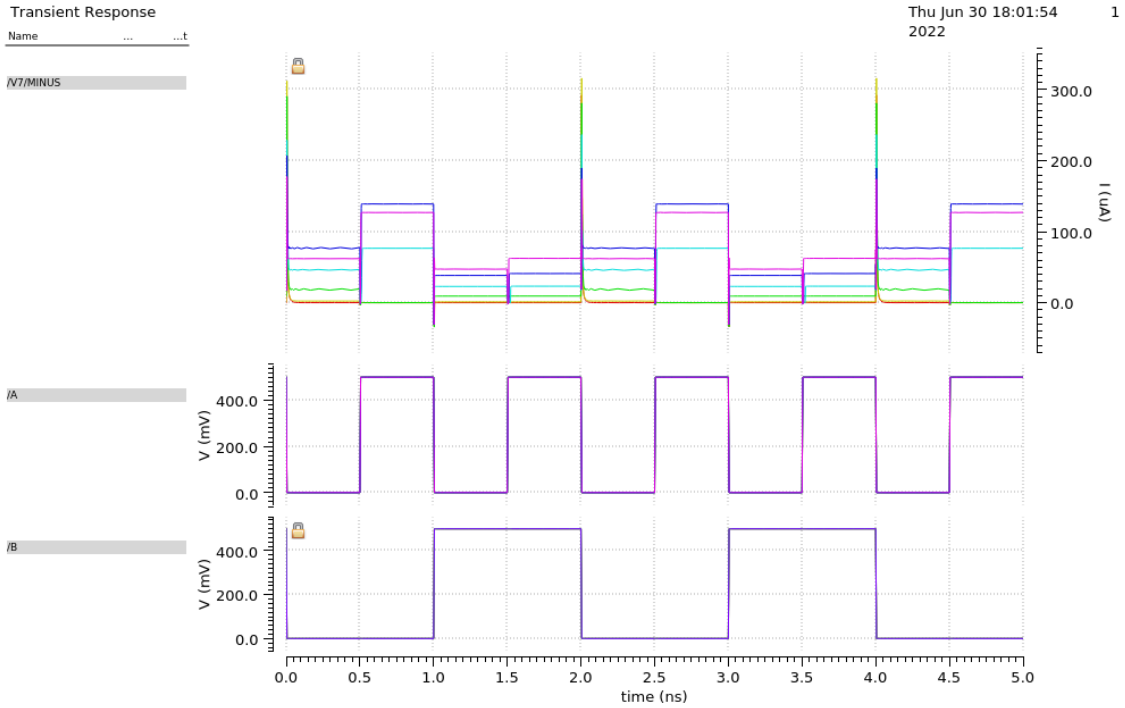


Figure 4.12: Current sunk by the supply voltage in a NOR gate for different values of v_{shift}

XOR

In fig. 4.13 is reported the CMOS-like XOR schematic implemented with ambipolar devices for different values of v_{shift}. Y is the output signal and A and B are the input signals. They are squarewave of amplitude 0.5 V, and period respectively 1 ns and 2 ns, the rise and the fall time are chosen equal to 5 ps. A parametric analysis in function of v_{shift} has been performed to look at the output of each XOR. The supply voltage V_{DD} is chosen equal to 0.5 V. The voltage generator v_{shift} are implied to shift the transcharacteristic. To implement the gate XOR, some input goes through an inverter gate. This choice is taken to simulate a gate implemented as in an integrated circuits.

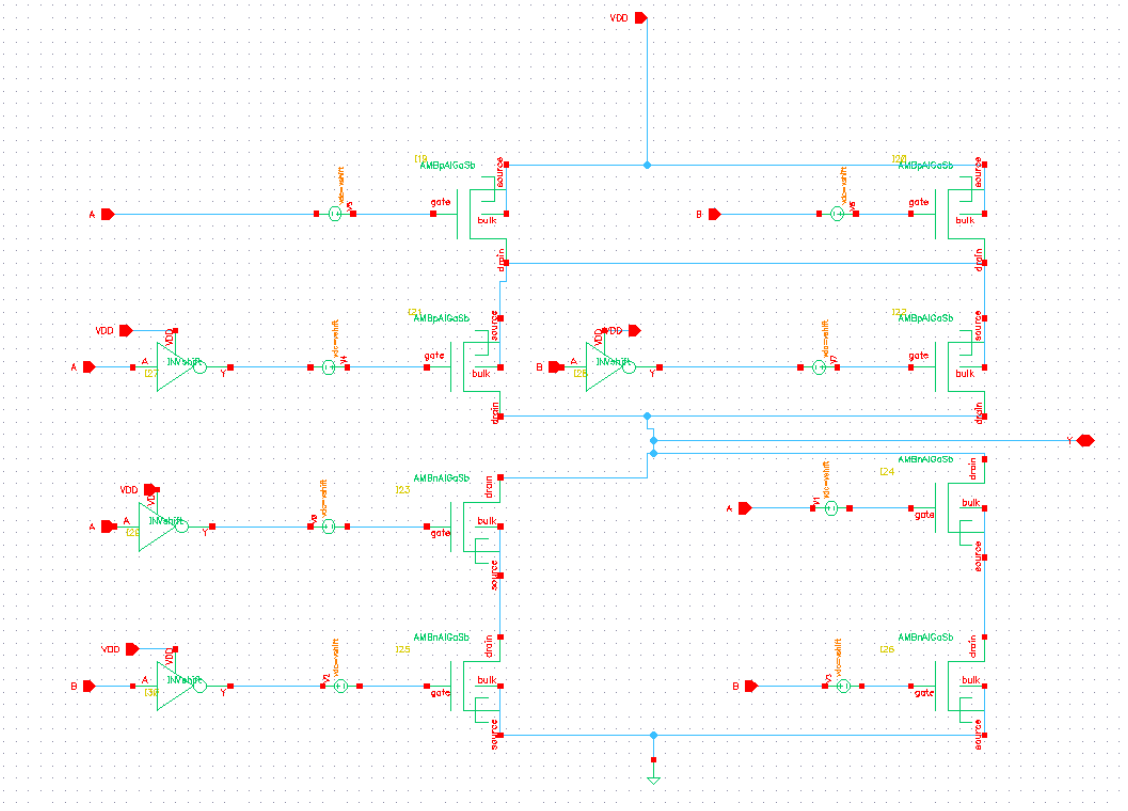


Figure 4.13: XOR schematic for simulations

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Table 4.8: XOR truth table

In table 4.8 are reported the inputs and the output of a XOR gate. Figure 4.14 shows the results of the transient analysis of the simulated XOR gate. In the image are reported A,B, and Y.

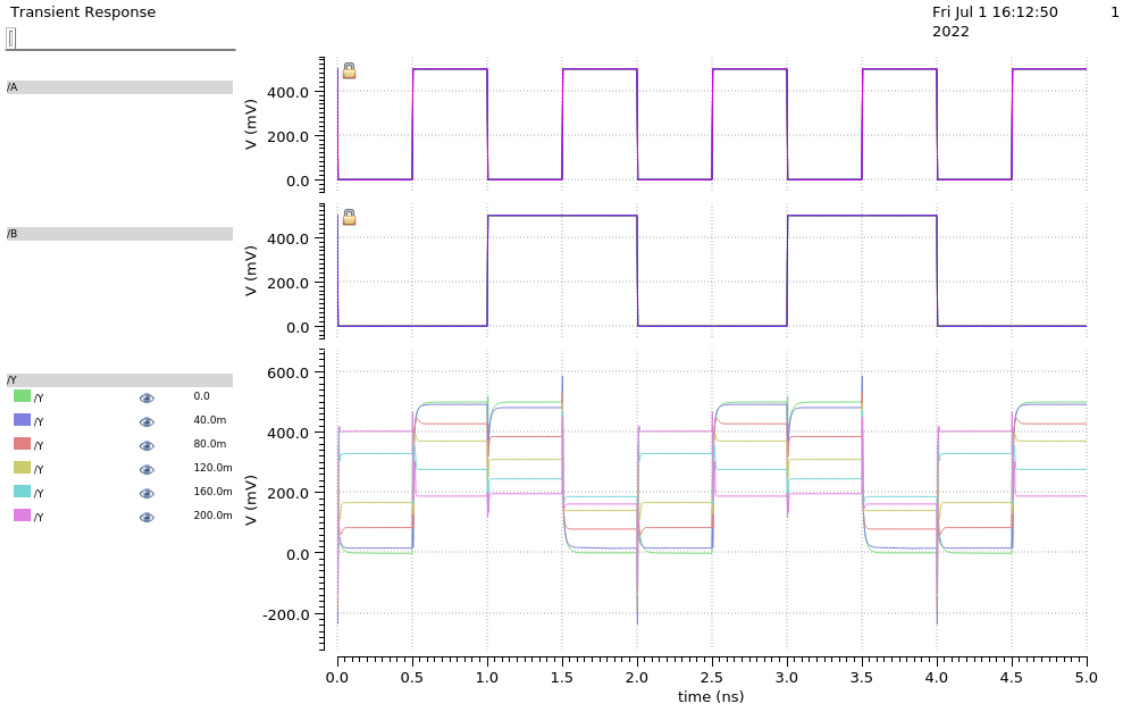


Figure 4.14: Transient analysis of XOR for different v_{shift}

The gate exhibits errors in the evaluation of the output for v_{shift} higher than 160 mV, as shown in the transient analysis in fig.4.14. In fig.4.15 are reported the currents sunk from the supply voltage used to evaluated the dynamic power as described in chapter 3. The results of the power are reported in the table 4.9, it is possible to notice that the consumption of power increases as increase v_{shift}.

FOM	V_{shift} [mV]					
	0	40	80	120	160	200
$P_{dyn}[\mu W]$	2.326	5.422	31.29	73.56	117.4	152.46

Table 4.9: XOR Dynamic Power

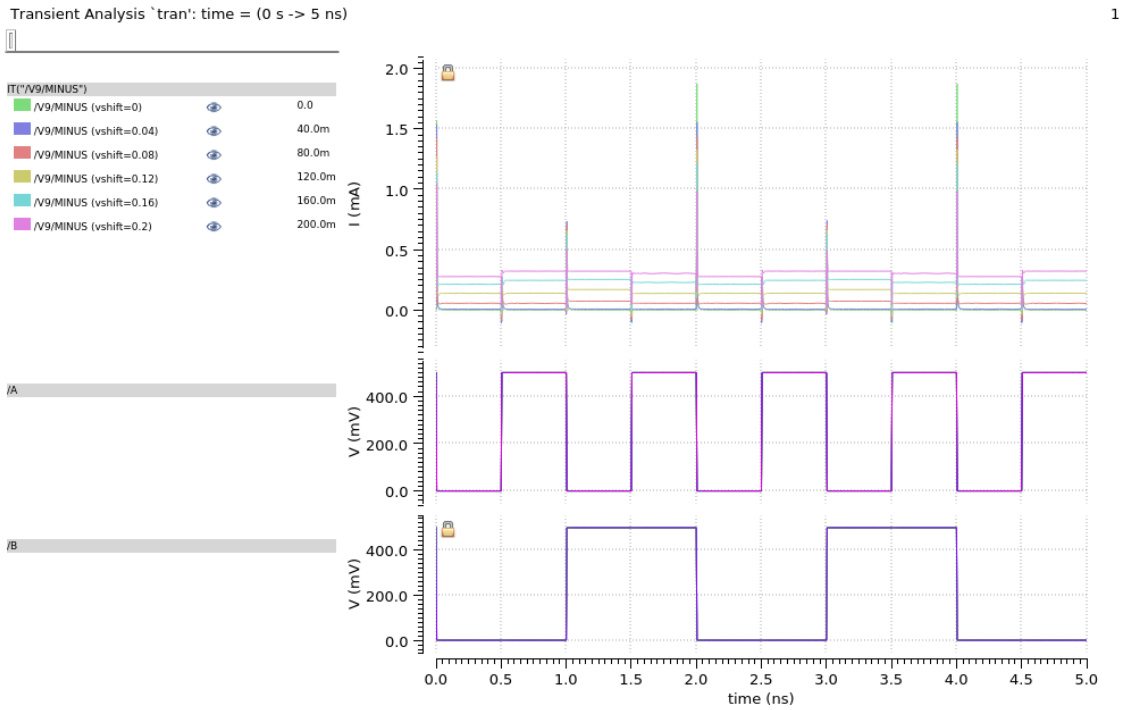


Figure 4.15: Current sunk by the supply voltage in a XOR gate for different values of v_{shift}

Half Adder

In fig. 4.16 is reported the HA schematic implemented with ambipolar devices for different values of v_{shift}. A and B are the input signals, they are squarewave of amplitude 0.5 V, and period respectively 1 ns and 2 ns, the rise and the fall time are chosen equal to 5 ps. A parametric analysis in function of v_{shift} has been performed to look at the output of each HA. The outputs are the signals S and C. The truth table of a generic HA is reported in table 4.10.

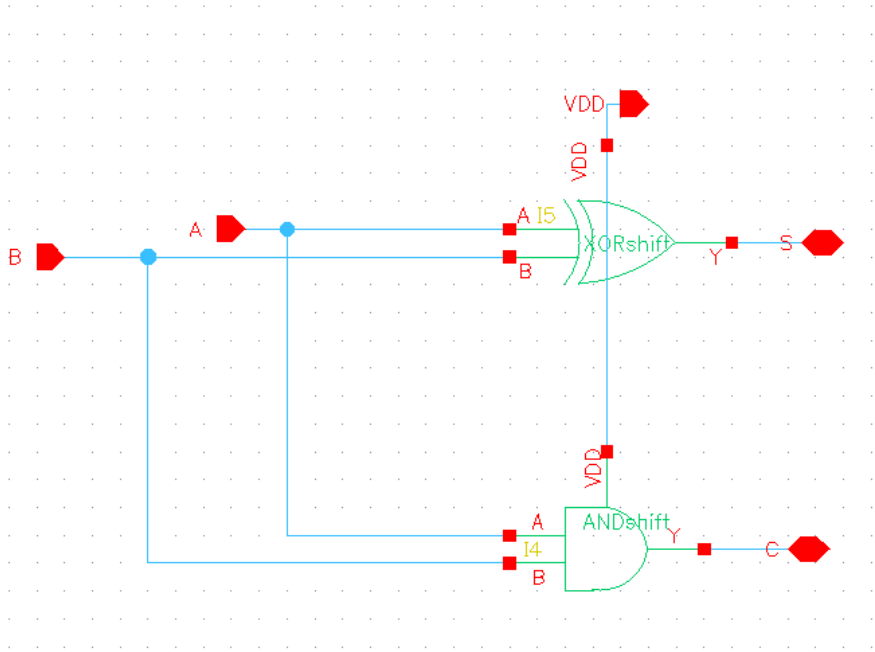


Figure 4.16: Half Adder schematic for simulations

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 4.10: HA truth table

Figure 4.17 shows the inputs and the outputs results of the transient analysis performed. As the transient analysis shows in fig. 4.17, the gate for v_{shift} higher than 160 mV includes errors, also the gate with $v_{shift} = 120$ mV has outputs on the limits of the logic values.

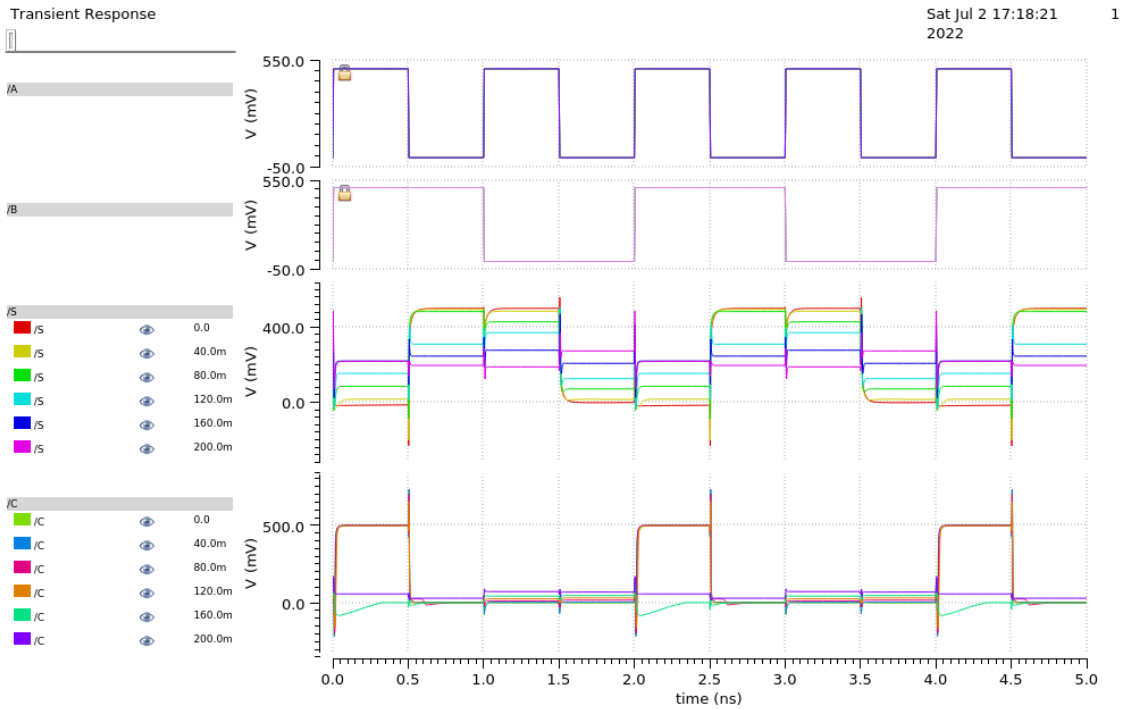


Figure 4.17: Transient analysis of HA for different v_{shift}

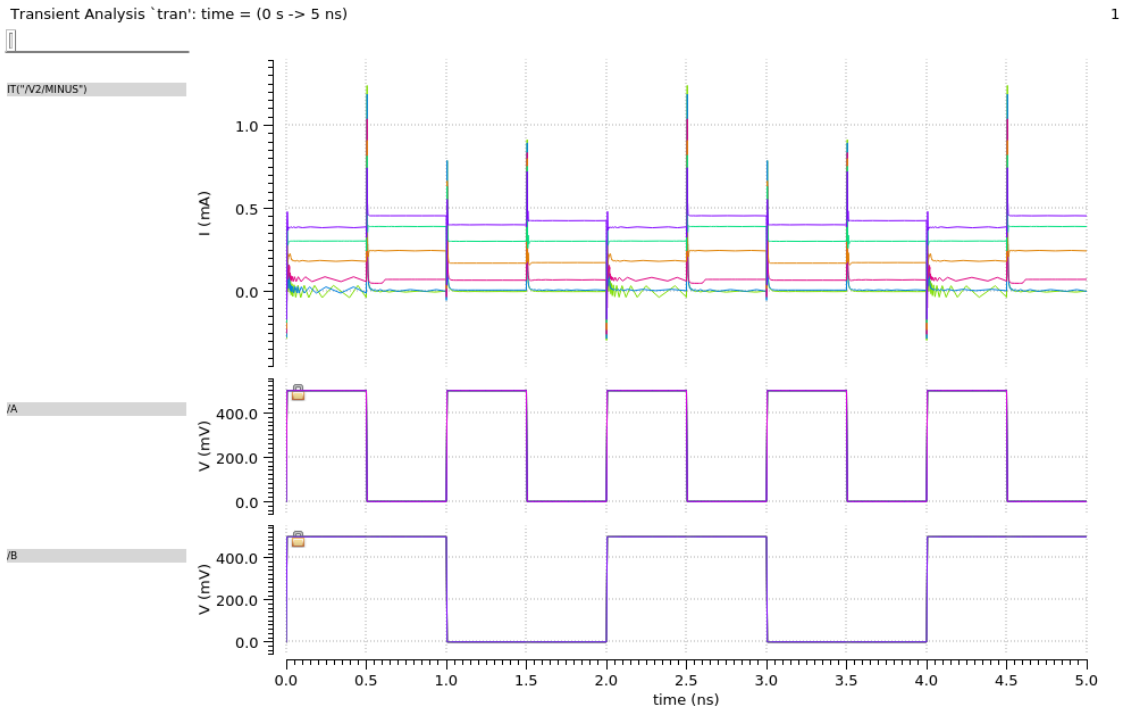


Figure 4.18: Current sunk by the supply voltage in a HA gate for different values of v_{shift}

In fig.4.18 are reported the currents sunk from the supply voltage used to evaluated the dynamic power as described in ch. 3. The results of the power in reported in the table 4.11, it is possible to notice that the consumption of power increases as increase v_{shift}.

FOM	V_{shift} [mV]					
	0	40	80	120	160	200
$P_{dyn}[\mu W]$	3.58	7.32	37.36	97.97	162.7	208.5

Table 4.11: Half Adder Dynamic Power

Full Adder

In fig. 4.19 is reported the FA schematic implemented with ambipolar devices for different values of v_{shift}. C_{n-1}, A_n and B_n are the inputs signals, C_n and S_n are the outputs. The inputs are squarewave of amplitude 0.5 V, and period respectively 4 ns, 2 ns and 1 ns, the rise and the fall time are chosen equal to 5 ps. A parametric analysis in function of v_{shift} has been performed to look at the output of each FA. V_DD is the power supply and the value imposed is 0.5 V.

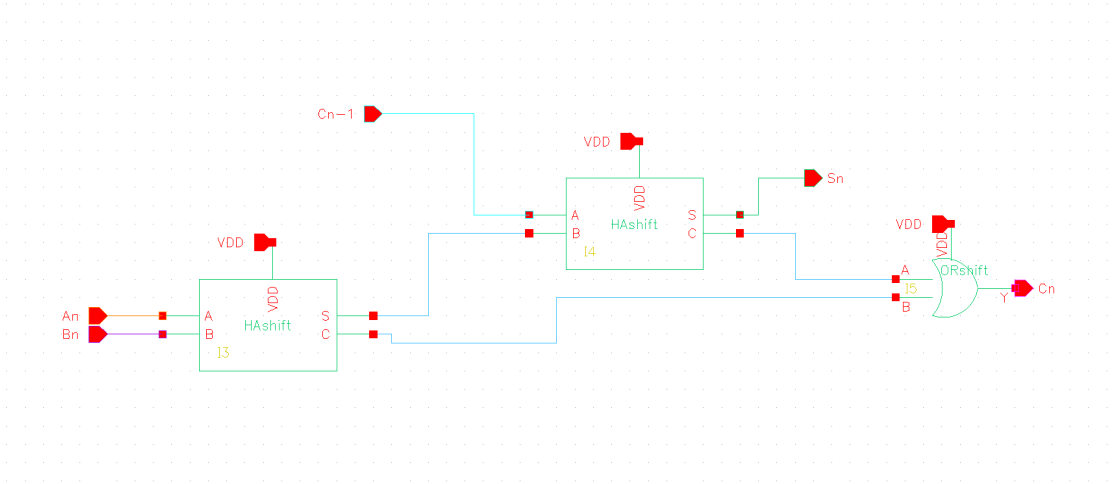


Figure 4.19: Full Adder schematic for simulations

C_{n-1}	A_n	B_n	C_n	S_n
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 4.12: FA truth table

Table 4.12 reports the truth table of a generic FA.
Fig.4.20 shows the simulation of the transient analysis, where all the inputs and outputs are reported. Combining more gates the errors becomes dominant, infact this gate shows error for v_shift higher than 120 mV. Moreover, the output at $v_shift = 120$ mV exhibit values of the output near the logic values evaluated in chapter 4.

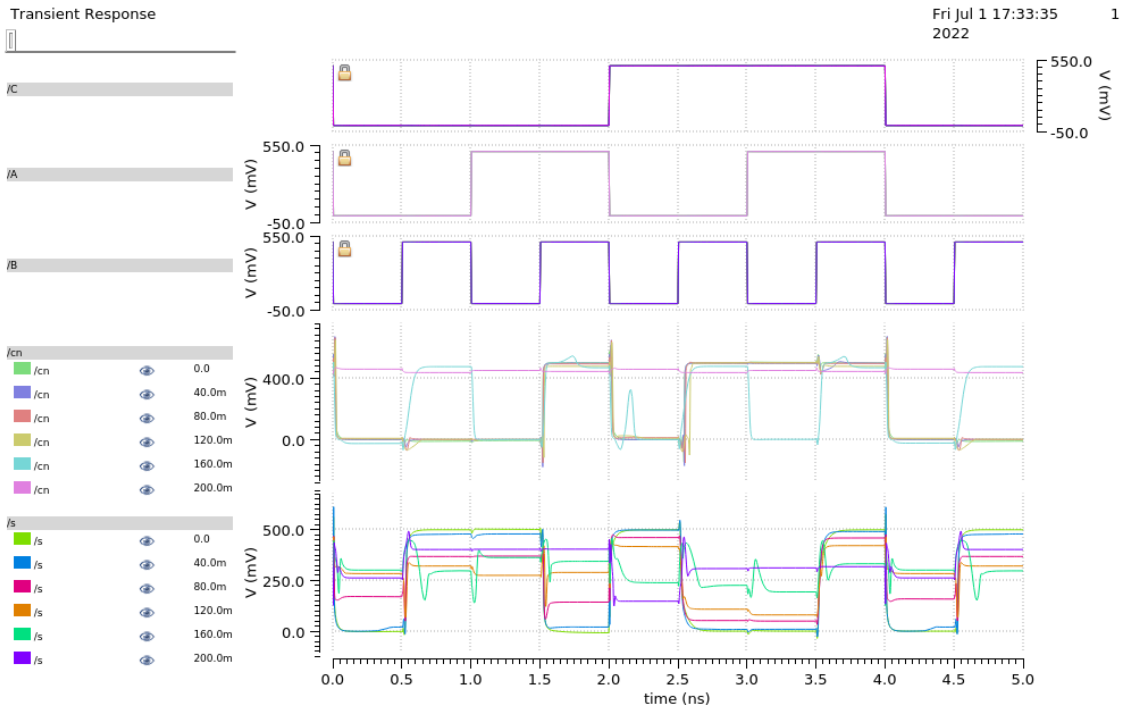


Figure 4.20: Transient analysis of FA for different v_{shift}

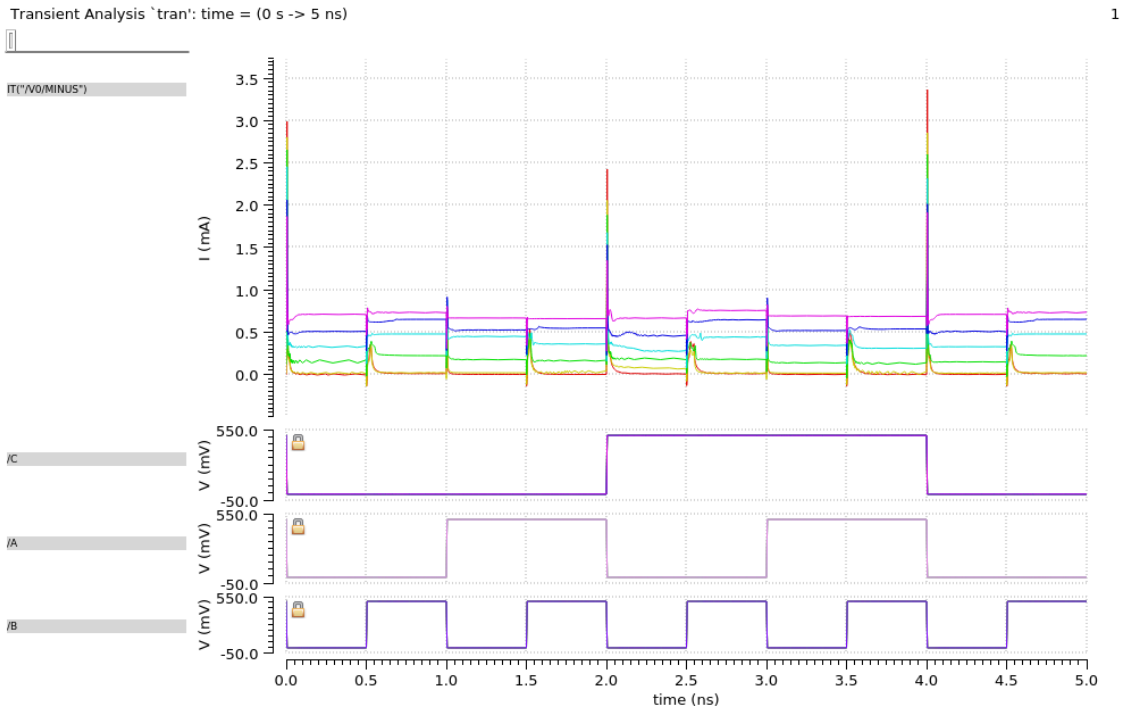


Figure 4.21: Current sunk by the supply voltage in a FA gate for different values of v_{shift}

FOM	V_{shift} [mV]					
	0	40	80	120	160	200
$P_{dyn}[\mu W]$	11.67	18.03	95.18	203.7	277.9	345.1

Table 4.13: FA Dynamic Power

In fig.4.21 are reported the currents sunk from the supply voltage used to evaluated the dynamic power as described in ch. 3. The results of the power in reported in the table 4.13, it is possible to notice that the consumption of power increases as increase v_{shift}.

4.2 AlGaSb/InAs TFET with reduced ambipolarity

In this chapter the device described in [10] has been exploited and the DC performance of the single TFET and the main logic gates have been analyzed. The structure is optimized to reduce the ambipolar current.

4.2.1 DC Characteristics

Transcharacteristic in Fig. 4.22 and characteristic in Fig. 4.24 are obtained from DC simulations on Cadence Virtuoso.

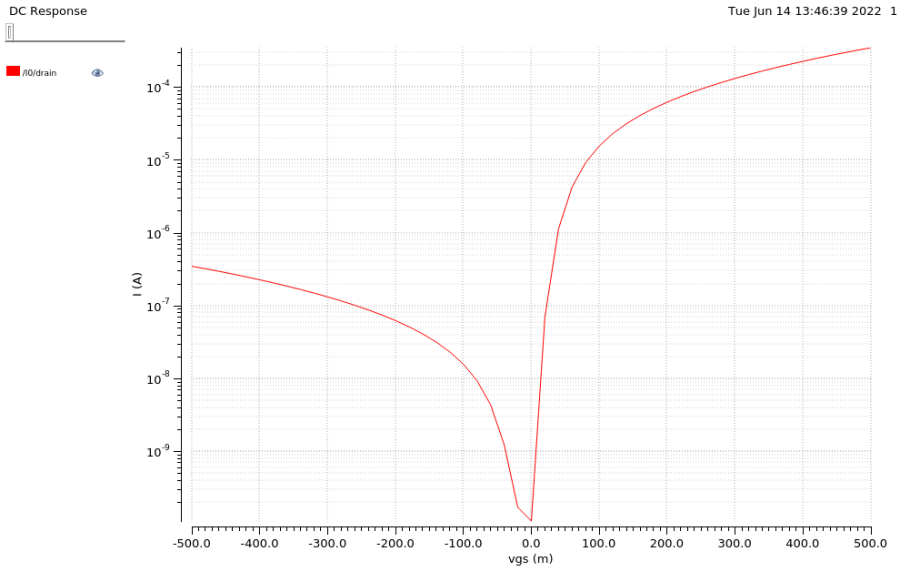


Figure 4.22: Transcharacteristic of AlGaSb/InAs

Figure 4.22 reports the transcharacteristic in logarithmic scale, showing a current also for negative values of v_{GS}. In this case, the ambipolar current is decreased by the peculiar structure.

$I_{ON}[\mu A]$	$I_{OFF}[pA]$
351.19	111.229p

Table 4.14: I_{ON} and I_{OFF} of AlGaSb/InAs

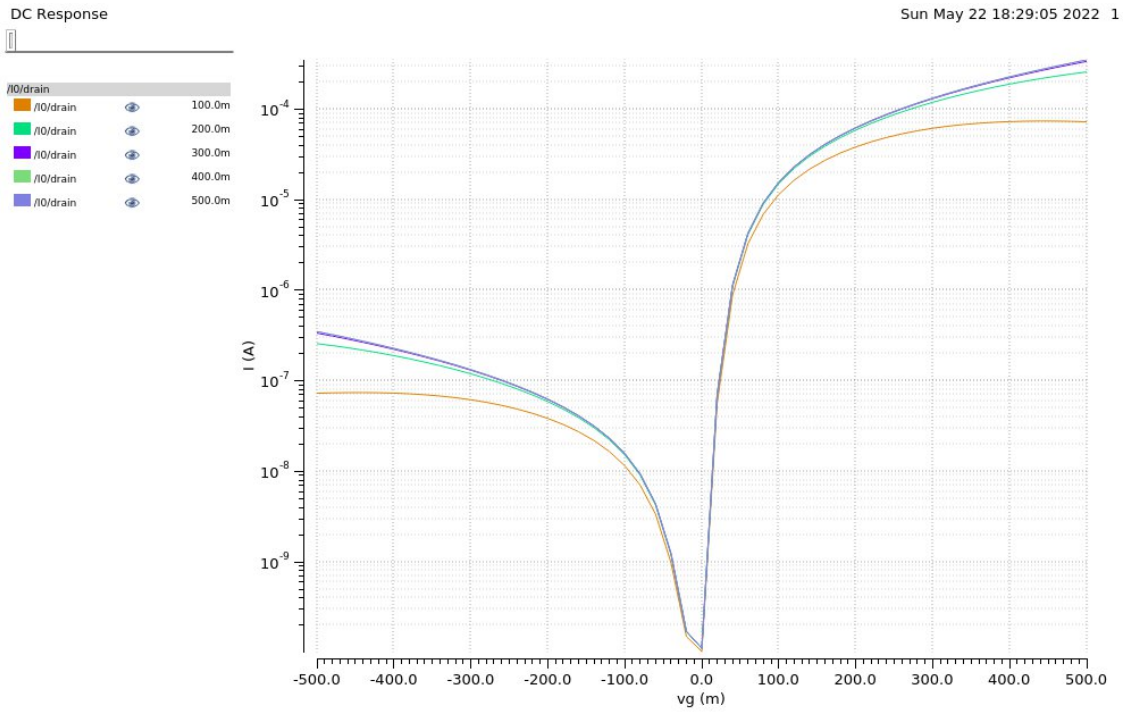


Figure 4.23: AlGaSb/InAs Transcharacteristic for different values of v_{DS}

In fig. 4.23 is reported the transcharacteristic for several values of v_{DS}. The curve in red is for v_{DS} =100 mV, it shows the lowest values of current. The graph indicates an increase in current I_{DS} as v_{DS} increases.

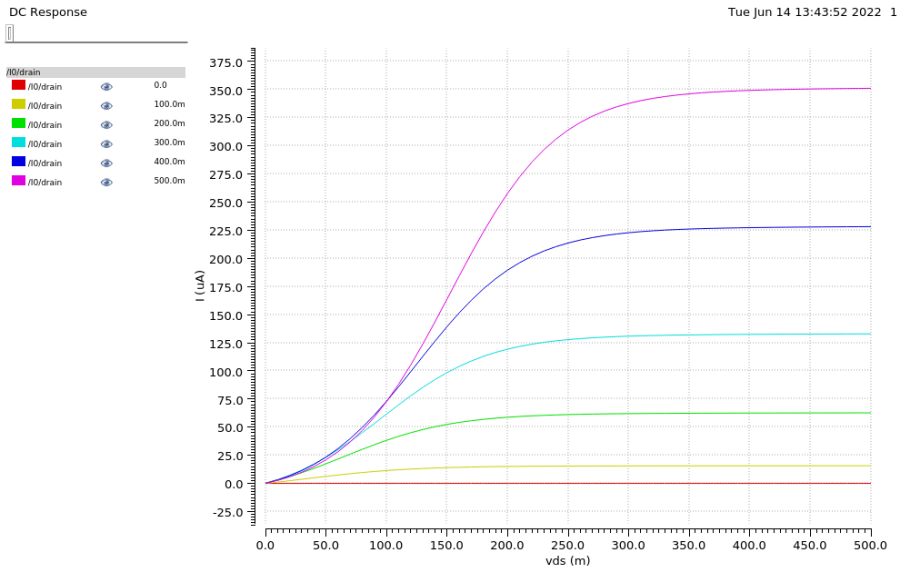


Figure 4.24: Characteristic of AlGaSb/InAs

The current I_{DS} in the function of v_{DS} for several values of v_{GS} is reported in fig. 4.24. For higher values of v_{gs} a remarkable increase of current shows up. It is possible to notice that the current saturates for high values of v_{DS}. To evaluate the v_{th} of the transistor, the method described in chapter 3 is utilized. The second derivative of the current in the function of the v_{GS} is assesses. The result is reported in fig. 4.25. The peak proves to be the value of v_{th}. This value is also exploited to evaluate the SS as

$$SS = \frac{V_{th}}{\log \frac{I(V_{gs}=V_{th})}{I_{OFF}}}$$

The results of the evaluated SS and v_{th} are reported in table 4.15 with the other figures of merit.

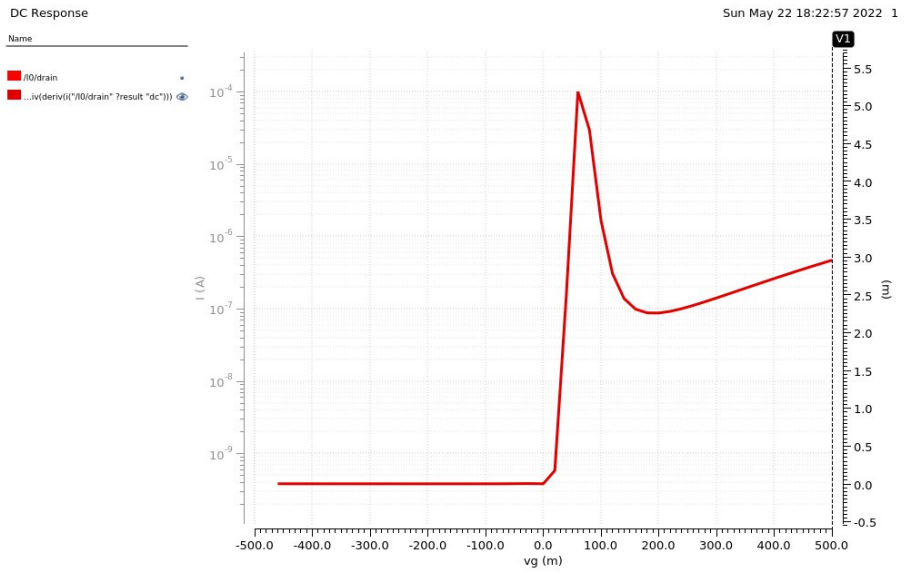


Figure 4.25: $\frac{\partial^2 I_d}{\partial v_{gs}^2}$ of AlGaSb/InAs to evaluate the threshold voltage

In fig.4.26 are reported in logarithmic scale the values of the currents of an nTFET and the absolute values of a pTFET. The current provided by the two transistors is the same. In the case of MOSFETs, due to the dependency of the current from the carriers mobility, the pFET and the nFET are chosen of different wide to have the same current. In TFET it is not necessary, because the current does not depend on the mobility, but depends on BTBT. These results are shown in fig.4.26 with a symmetry in the transcharateristics of a n-type (red) and a p-type(green).

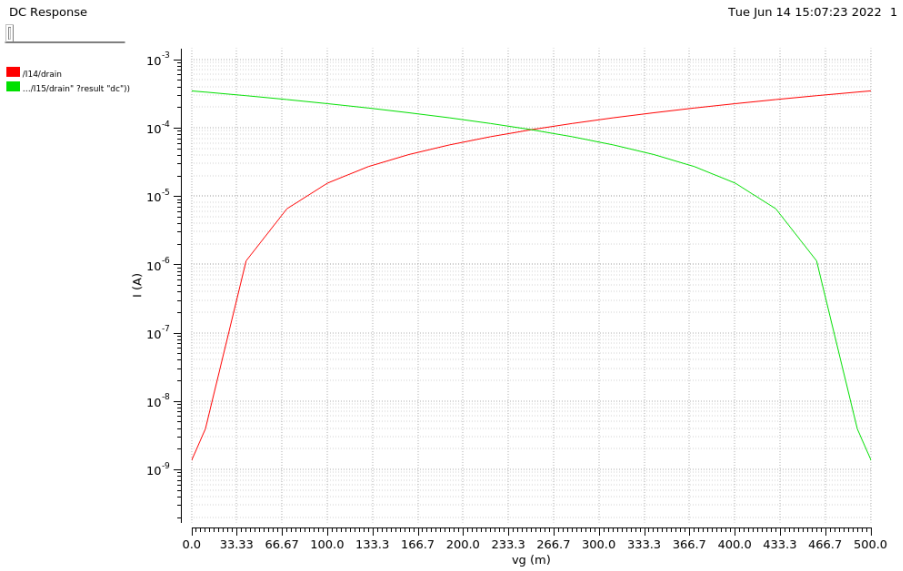


Figure 4.26: Comparison n-type and p-type transcharacteristic of AlGaSb/InAs

$I_{ON}[\mu A]$	$I_{OFF}[pA]$	v_{th} [mV]	$\frac{I_{ON}}{I_{OFF}}$	SS [mV/dec]
351.19	111.229	60	$3 \cdot 10^6$	13

Table 4.15: FOMs of AlGaSb/InAs

4.2.2 Performance evaluation of basic cells

In this chapter has been evaluated the basic cells: INV, NAND, NOR, XOR, Half Adder (HA) and Full Adder (FA). For each gate, an analysis of the correct functioning and also an evaluation of the power consumption have been performed.

INVERTER

In fig. 4.27 is reported the schematic of the INVERTER gate that was used for the simulation in Cadence Virtuoso. the input signal is A and it is a squarewave of amplitude 0.5 V, period 1 ns, rise and fall time of 5 ps. The power supply is V_{DD} and the value is 0.5 V. The topology is CMOS-like.

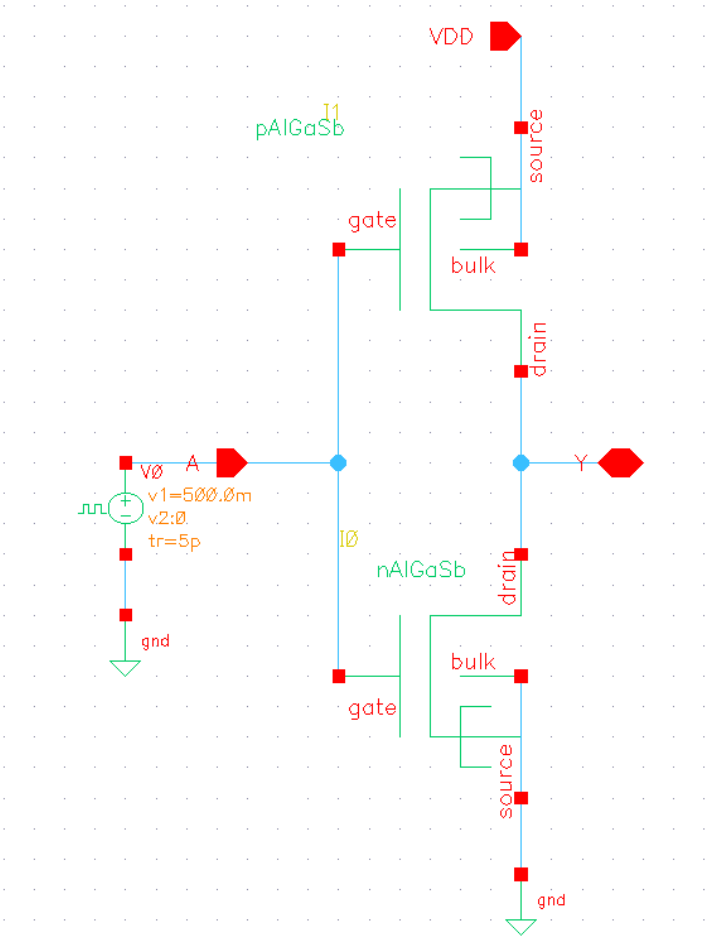


Figure 4.27: INV gate schematic

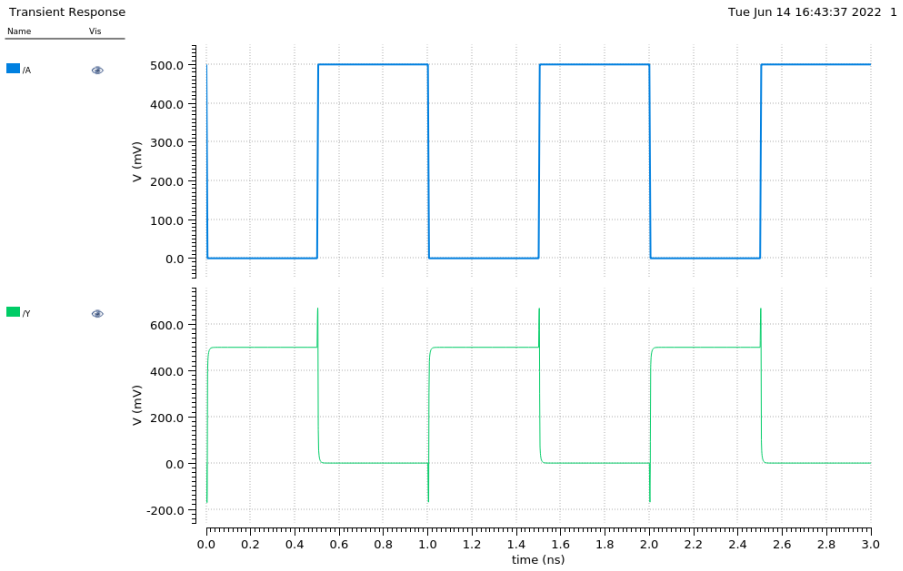


Figure 4.28: Transient analysis of Inverter gate

Fig. 4.28 shows the results of the transient analysis. The picture displays the correct behavior of the gate: when the input is low the output is high, when the input is high the output is low. The transfer characteristic of the inverter is illustrated in fig.4.29. The slope of the curve is not steep, a behavior desirable for a good inverter gate. Even if the transfer characteristic is not the best, the gate presents a correct functioning.

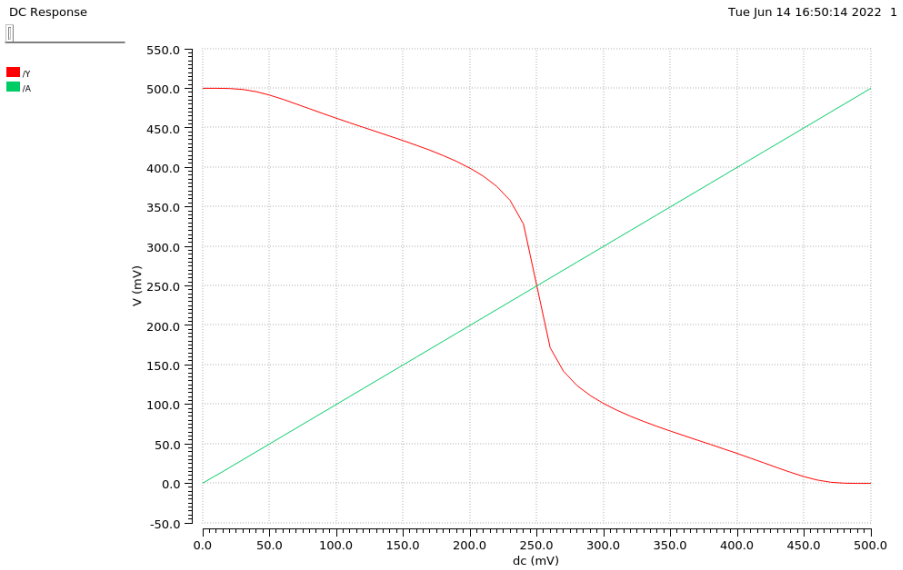


Figure 4.29: INV dc

From fig.4.29 the logic values of the inverter gate are evaluated and reported in 4.16. The method employed to calculated the logic values is described in chapter 3.

V_{OH} [mV]	$V_{IH}[mV]$	$V_{IL}[mV]$	$V_{OL}[mV]$
389	300	209	44.19

Table 4.16: Logic values of a INV AlGaSb/InAs

NAND

In fig. 4.30 is reported the NAND schematic CMOS-like used to perform the simulation on Cadence Virtuoso. Y is the output signal, A and B are the input signals, they are squarewave of amplitude 0.5 V, and period respectively 1 ns and 2 ns, the rise and the fall times are chosen equal to 5 ps. The power supply is chosen equal to 0.5 V and is realized with the voltage generator placed on the sources of the p-devices.

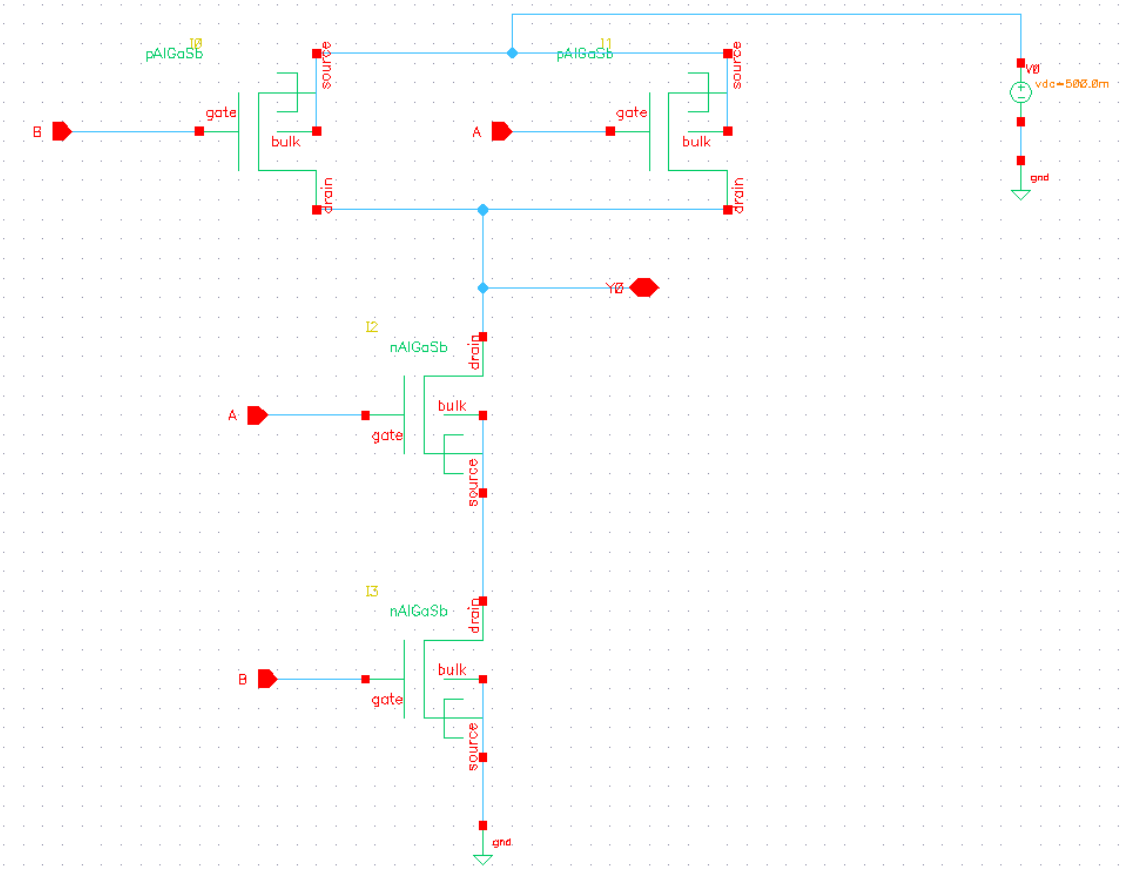


Figure 4.30: NAND schematic for simulations

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

Table 4.17: NAND truth table

In table 4.17 is reported the truth table of the function NAND. Using the table as a reference is possible to analyze the results of the simulation. The transient analysis of the NAND gate is reported in fig. 4.31. Comparing the Y with the values in table 4.17 is possible to assert that the NAND gate implemented with AlGaSb/InAs with reduced ambipolarity shows a correct behavior.

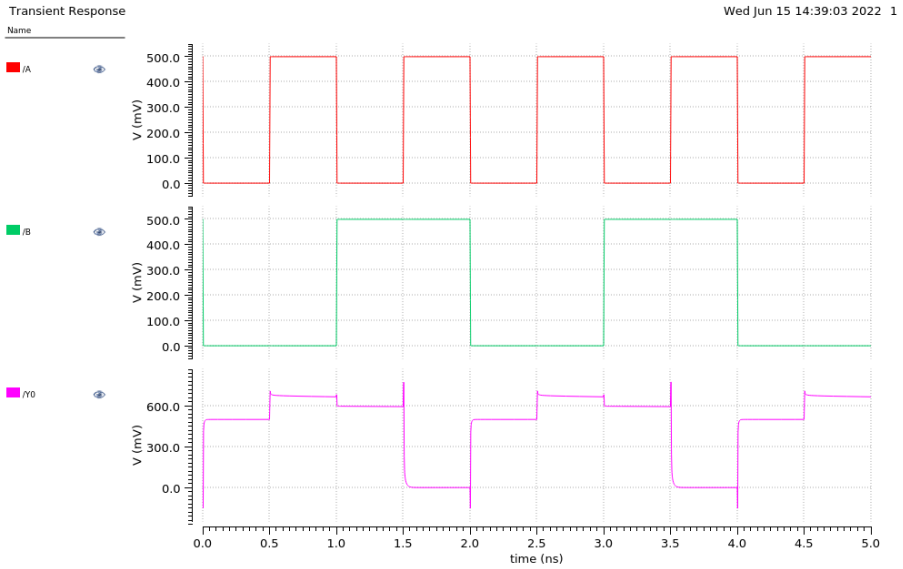


Figure 4.31: Transient analysis of NAND

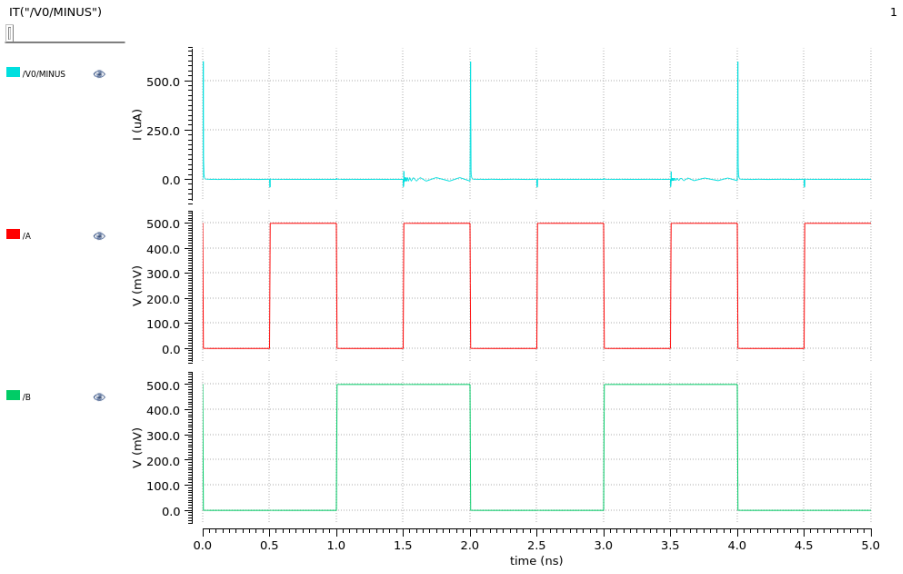


Figure 4.32: Current sunk from supply voltage of NAND

The evaluation of the dynamic power has been carried out by the current sunk by the supply voltage shown in fig. 4.32.It is possible to note that, a difference from the previous case where the ambipolarity is prevalent, in the evaluation of the current there is no presence of a static leakage. The calculated power as described in 3 is 412.3 nW.

NOR

In fig. 4.33 is reported the NOR schematic CMOS-like. The voltage supply is imposed equal to 0.5 V and the output signal is Y. A and B are the input signals, they are squarewaves of amplitude 0.5 V, period respectively 1 ns and 2 ns, and the rise and the fall time are 5 ps.

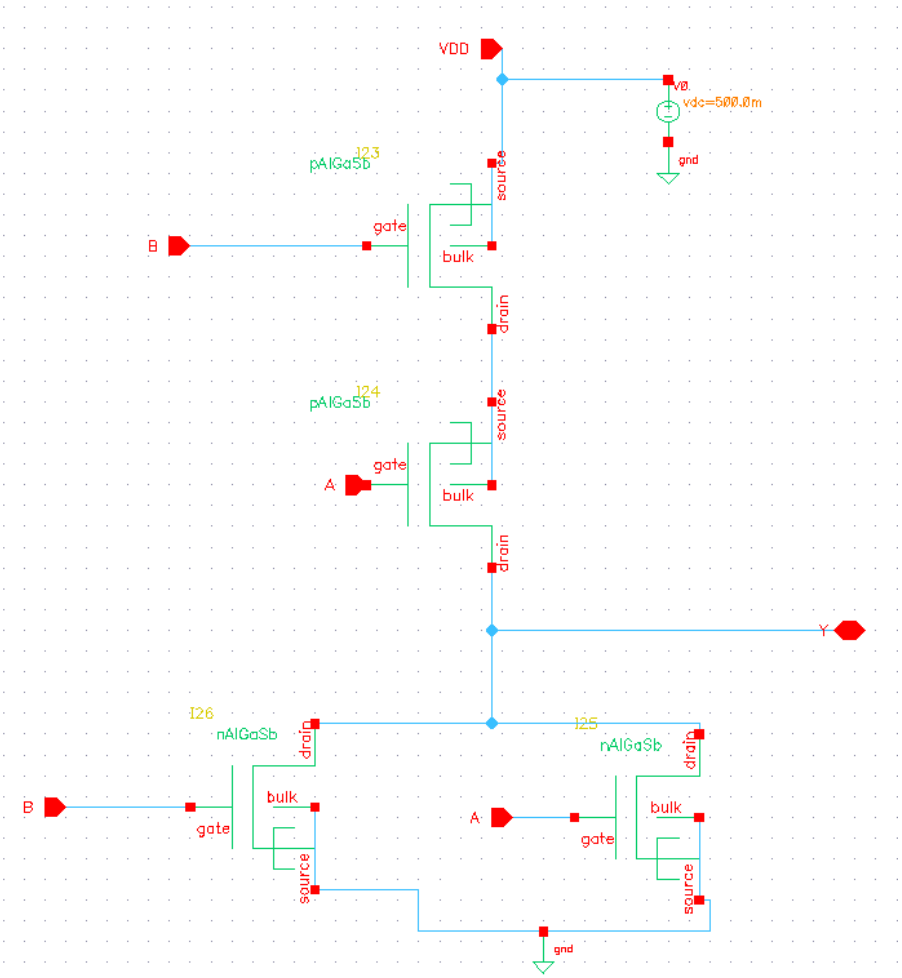


Figure 4.33: NOR schematic for simulation

A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Table 4.18: NOR truth table

In table 4.18 are reported the values of the function NOR. Fig.4.34 shows the simulation of the transient analysis of the NOR gate. Comparing the values of Y and the values of the table, it is possible to see that the NOR gate work properly.

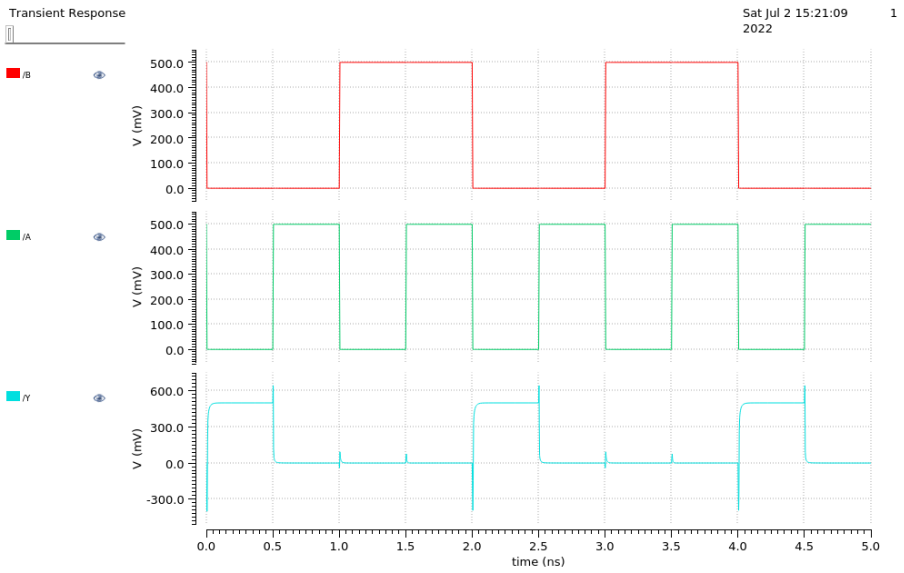


Figure 4.34: Transient analysis of NOR

The evaluation of the dynamic power has been carried out by the current sunk by the supply voltage shown in fig. 4.35. There is no static leakage current and the evaluated dynamic power is 463.5 nW.

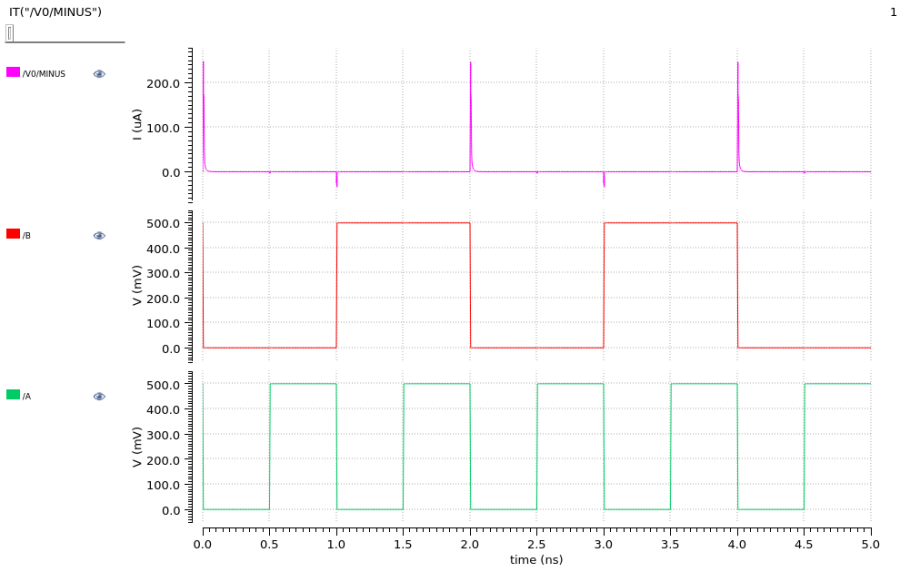


Figure 4.35: Current sunk from supply voltage of the NOR

XOR

In fig.4.36 is reported the XOR schematic implemented for the simulations. To realize a schematic that could be used in an integrated circuit the inverter gates are employed. The output signal is Y and the supply voltage is $V_{DD} = 0.5\,\text{V}$. A and B are the input signals, they are squarewaves of amplitude 0.5 V, and period respectively 1 ns and 2 ns, the rise and the fall times are chosen equal to 5 ps.

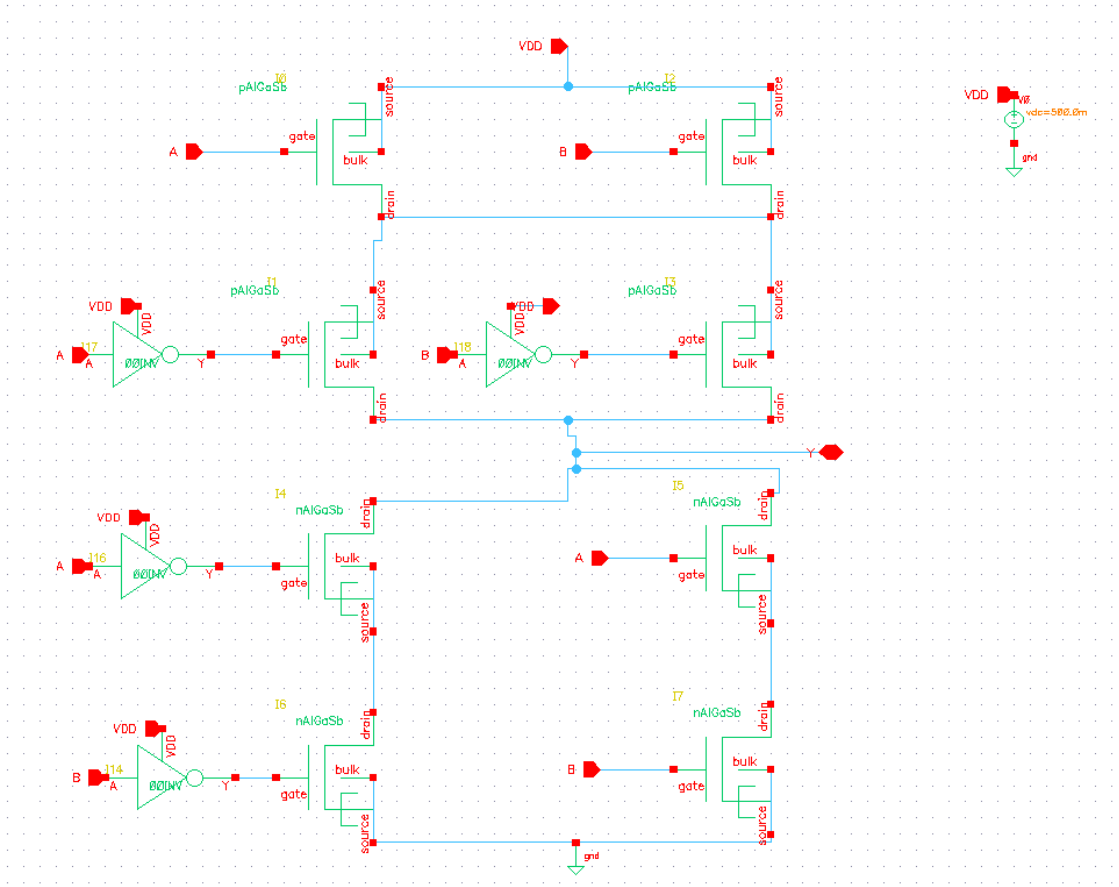


Figure 4.36: XOR schematic for simulations

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Table 4.19: XOR truth table

The truth table of an XOR gate is reported in table 4.19. Comparing the output of the table with the results of the simulation is possible to assert that the XOR gate works properly. The transient analysis is reported in figure 4.37.

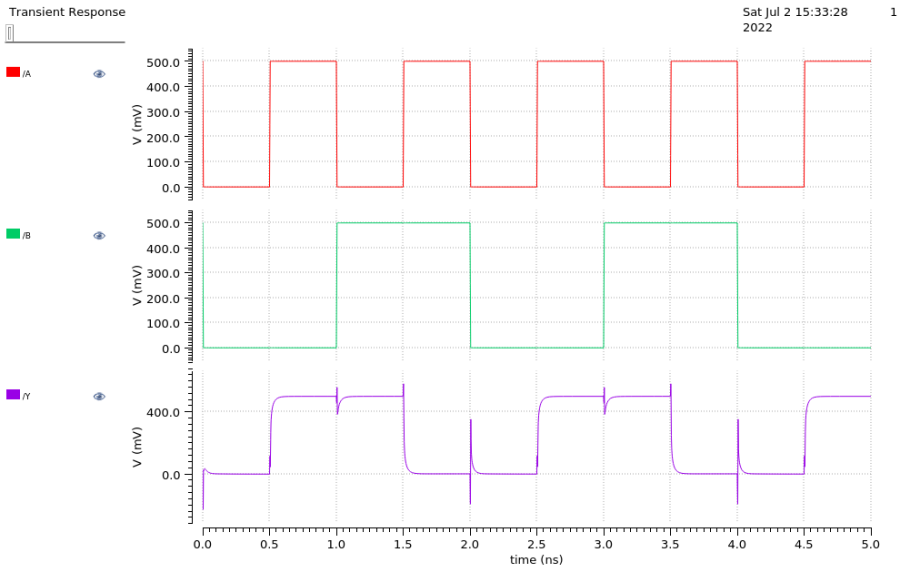


Figure 4.37: Transient analysis of XOR

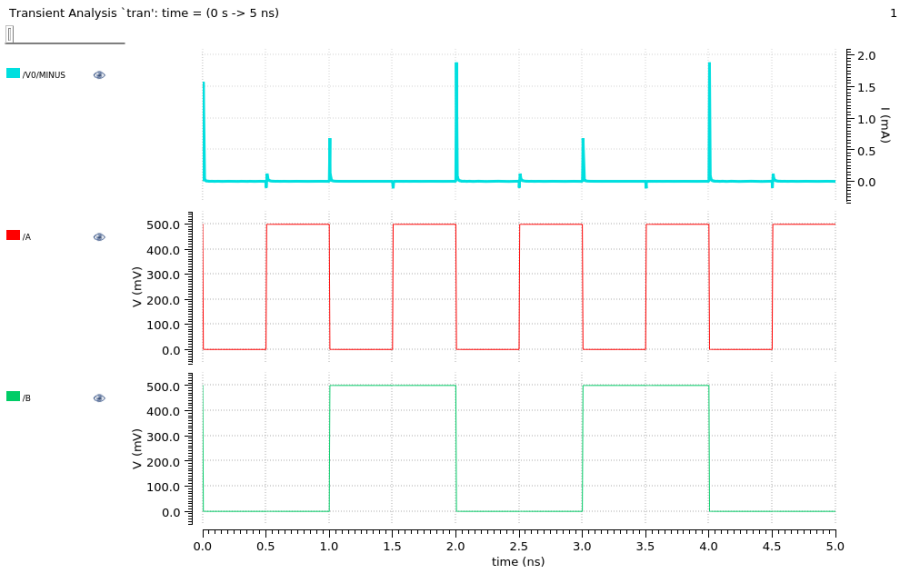


Figure 4.38: Current sunk from power supply of XOR

The evaluation of the dynamic power has been carried out by the current sunk by the supply voltage shown in fig. 4.38. The evaluated power is 2,307μW.

HA

In fig. 4.39 is reported the HA schematic. A and B are the input signals, they are pulse of amplitude 0.5 V, period respectively 1 ns and 2 ns, the rise and the fall times are chosen equal to 5 ps. The output signals are C and S. The supply voltage is $V_{DD} = 0.5\,\text{V}$.

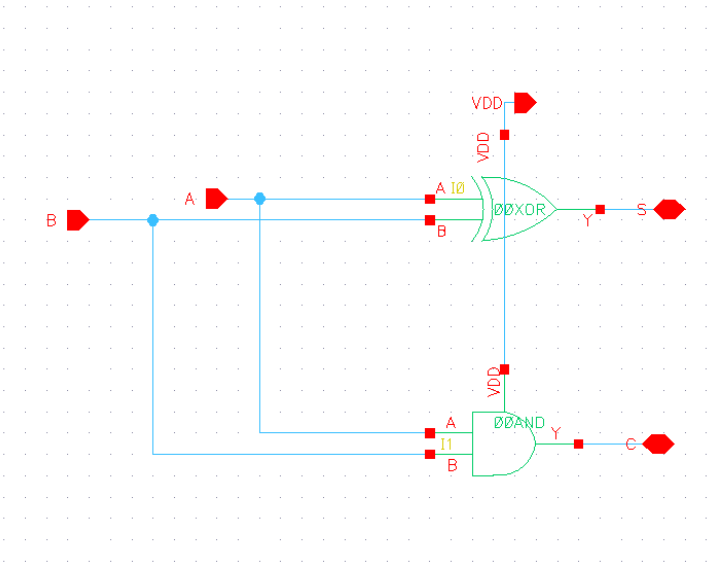


Figure 4.39: HA schematic for simulations

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 4.20: HA truth table

In table 4.20 are reported the values of the function HA. The results of the transient analysis are shown in fig.4.40. Comparing the outputs of the simulation and the the values of the table it is possible to see that the HA gate works properly.

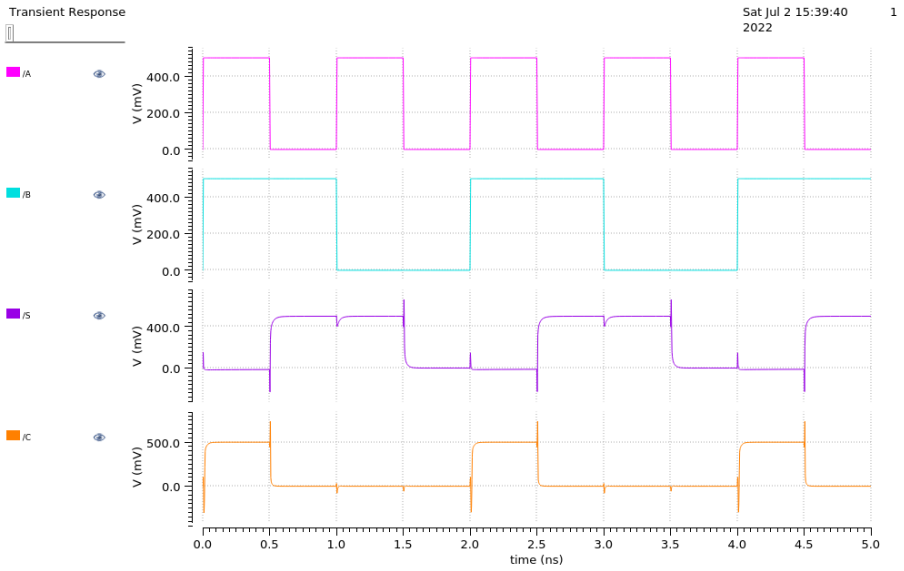


Figure 4.40: Transient analysis of HA

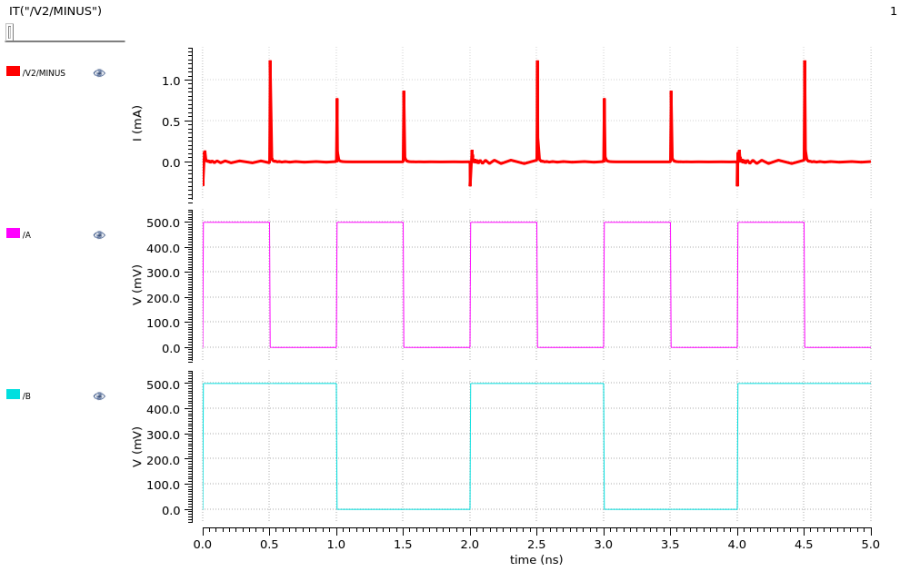


Figure 4.41: Current sunk from supply voltage of HA

The evaluation of the dynamic power has been carried out by the current sunk by the supply voltage shown in fig. 4.41. The evaluated power is 3,48 μW.

FA

In fig. 4.42 is reported the FA schematic. A_n,B_n and C_{n-1} are the input signals, they are squarewaves of amplitude 0.5 V,period respectively 4 ns, 2 ns and 1 ns, the rise and the fall times are chosen equal to 5 ps. The output signals are S_n and C_n. The power supply V_{DD} is equal to 0.5 V.

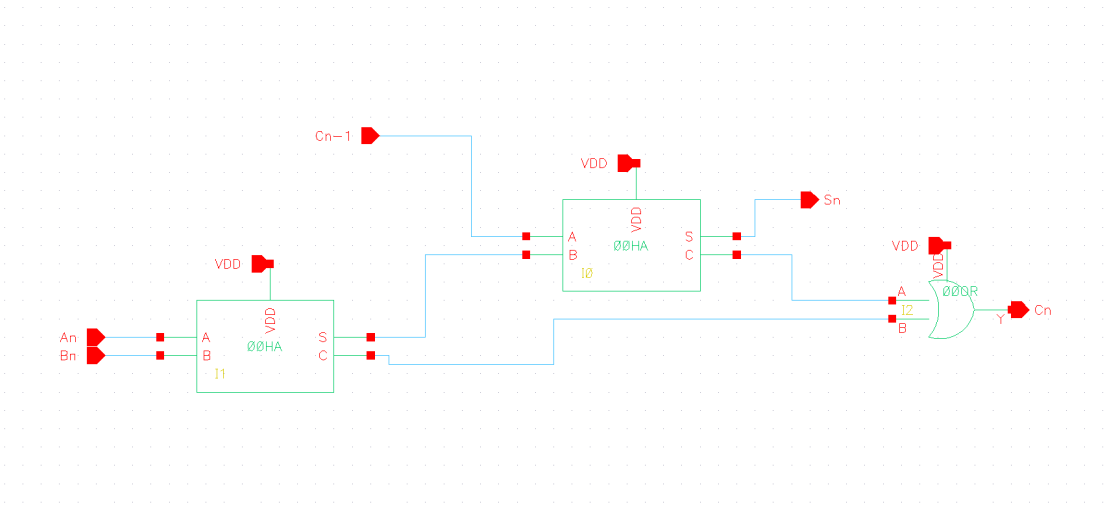


Figure 4.42: FA schematic for simulations

C_{n-1}	A_n	B_n	C_n	S_n
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 4.21: FA truth table

In table 4.21 is reported the truth table of the FA. In fig 4.43 are reported the results of the transients analysis. Comparing the outputs of the simulation with the values of the function in the table above, is possible to conclude that the FA gate implemented with the reduced ambipolarity works properly.

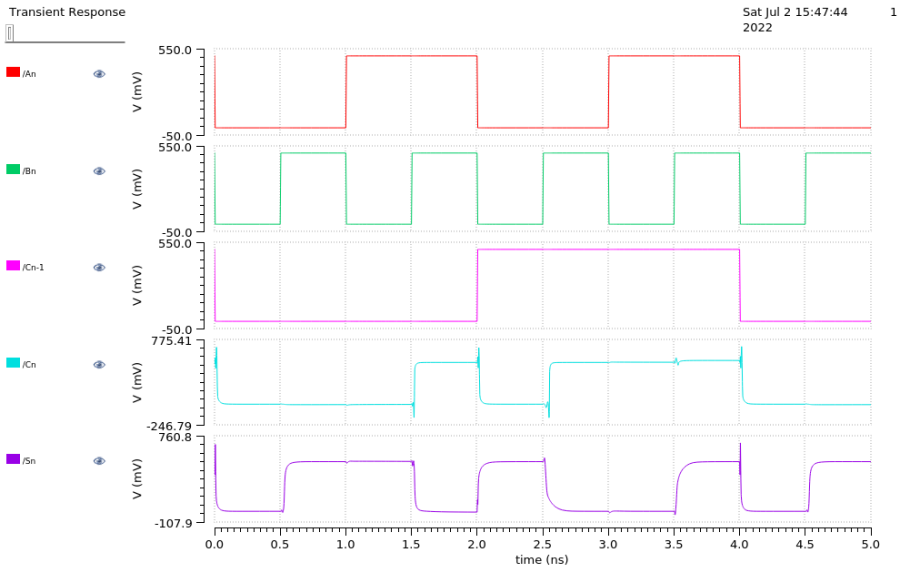


Figure 4.43: Transient analysis of FA

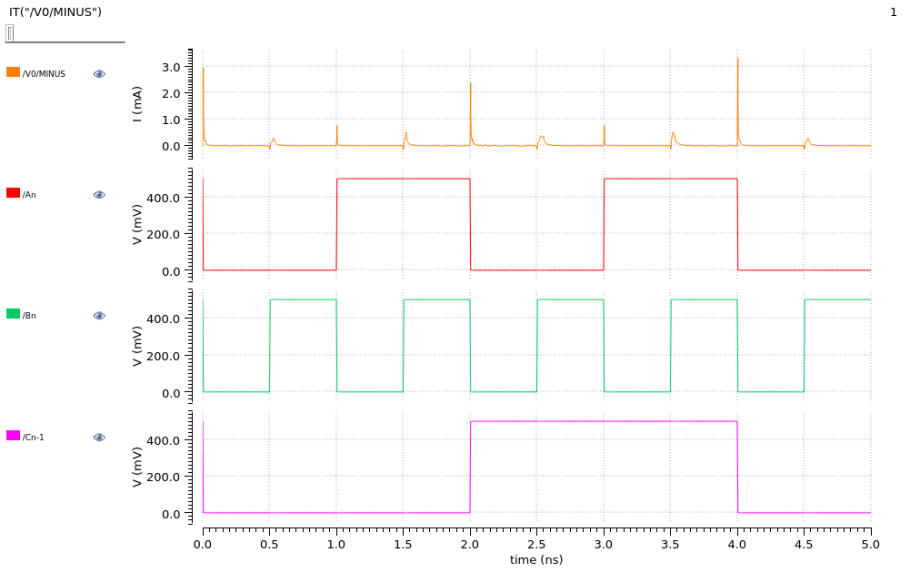


Figure 4.44: Current sunk from power supply by FA

The evaluation of the dynamic power has been carried out by the current sunk by the supply voltage shown in fig. 4.44. The evaluated power is $10\,27\mu W$.

4.3 Result summary

The simulations show that the ambipolarity has for sure an impact on the behaviour of the gates when the transcharacteristics are symmetric for values higher than 160 mV. Furthermore, if the gates are combined, such as in a full adder, the errors show up in the evaluation of the output also for lower values of v_{shift}, i.e. 120 mV. The most important result is the one about dynamic power. In table 4.22 are reported the summary results of the evaluated dynamic powers.

	V_{shift} [mV]						AlGaSb/InAs
	0	40	80	120	160	200	
NAND	413e-3	1.036	7.76	18.24	31.61	29.41	412.3e-3
NOR	464e-3	957E-3	4.91	20.92	36.53	37.02	463e-3
XOR	2.326	5.422	31.29	73.56	117.4	152.46	2.30
HA	3.58	7.32	37.36	97.97	162.7	208.5	3.48
FA	11.67	18.03	95.18	203.7	277.9	345.1	10.27

Table 4.22: Dynamic Power of the main gates in μW

The dynamic power consumption in the devices AlGaSb/InAs with ambipolarity and suppressed ambipolarity is similar for device with symmetry at 0 V. The device that has a transcharacteristic translated by 40 mV dissipates almost double of the power by the devices with the transcharacteristic symmetric on 0 V. The table shows an increase of the power consumption as v_{shift} increases.
Typical values of power consumption for main digital circuits, for example for gates NAND, NOR and XOR of 45 nm CMOS technology are of the order of μW. For these gates the TFET-based circuits show a better performance in terms of dynamic power. Typical values of dynamic power in 45 nm CMOS technology are tens of microwatt for HA and twenty of microwatt for FA. In these cases, the TFETs consumes half of the power dynamic.

Chapter 5

Conclusion and future perspectives

The entire work is focused on the evaluation of the impact of ambipolairty on digital circuits based on TFET.
First of all, an introduction of the reason to explore this device is reported in chapter 1, the limits of CMOS circuits have to be overcome and TFETs seem to be a possible candidate to replace them since the performance of power and SS are promising.
Once the reasons have been illustrated an introduction to the working principle of the device has been shown in chapter 2. Based on band-to-band tunneling, the TFETs can be switched ON or OFF abruptly by the gate voltage. The peculiar carrier injection mechanism of the device lead also to an undesired behavior that is ambipolarity. This is one of the main drawbacks of TFET, the other one is the low I_{ON}. Several technological solutions have been illustrated to reduce these issues.
Chapter 3 was aimed to explain the work flow of the simulation. The well-established Notre Dame model was implemented and so a brief explanation is shown. To perform simulations with ambipolar devices the model was modified and the limits of the model are outlined. The extrapolation of the principal figures of merit are described.
In chapter 4 the simulations of the basic logic cells: INV, NAND, NOR, HA, FA are carried out. The simulations are performed for devices affected by different ambipolarity. Main FOMs, such as I_{ON}, I_{OFF}, v_{th} and the dynamic power were extracted using Cadence Virtuoso. Simulations underlined an increase of power with the raise of the point of symmetry of the transcharacteristic. This demonstrate the effect of ambipolarity on digital circuits. The devices affected by strong ambipolarity for lower positive values v_{gs} shows errors in the evaluation of the output. In terms of power, even the devices that shows weak ambipolarity for lower positive values of v_{gs} exhibit an increased dynamic power. In conclusion ambipolarity affects the performance of digital circuits and it is better to reduce it.
This was a short summary of the work done. The main issues was the exploited model utilized because it is a semi empirical models and without device simulations it is not possible realize a model accurate. Futures work can be related to the optimization of the model. Furthermore emerging structure can be studied to optimized the low I_{ON}

current.

Appendix

```
//#############################################################################
//#
//#  File :  ndtfet2.va
//#  Version: 1.0
//#  Date : July 10, 2015
//#  Author : Trond Ytterdal
//#  Description : University of Notre Dame TFET Model
//#
//#############################################################################

`include "discipline.h"

`define n_type 1
`define p_type -1
`define CHARGE 1.6021918e-19
`define M0 9.1095e-31
`define H 6.62606957e-34
`define HBAR 1.05458e-34
`define KB 1.3806488E-23
`define PI 3.141592653
`define EPS0 8.85418782e-12
`define VDSMIN 1e-12
`define DELTA 5
`define VMIN 0.0001
`define AMIN 1u

module ndtfet2(drain, gate, source, bulk);
  inout drain, gate, source, bulk;
  electrical drain, gate, source, bulk;
  electrical drainprime, gateprime, sourceprime;
  // instance parameters
  parameter real w = 1e-6;
  // model parameters
  parameter real adq1 = 0.04295;
  parameter real adq2 = 0.056735;
```

```
parameter real agate = 0.85;
parameter real asq1 = -0.00479;
parameter real asq1n = 0.019037;
parameter real asq2 = 0.0070874;
parameter real asq2n = 0.012071;
parameter real bdq1 = 1.2197;
parameter real bdq2 = 0.29892;
parameter real bsq1 = 2.4745;
parameter real bsq1n = 2.2383;
parameter real bsq2 = 8.9262;
parameter real bsq2n = 5.2229;
parameter real cdbew = 0;
parameter real cdq1 = 0.08567;
parameter real cdq2 = -0.076568;
parameter real cfdw = 0.5e-15;
parameter real cfsw = 0.5e-15;
parameter real cgbew = 0;
parameter real cgdew = 0;
parameter real cgsew = 0;
parameter real csbew = 0;
parameter real csq1 = -0.21747;
parameter real csq1n = -3.245;
parameter real csq2 = -4.3895;
parameter real csq2n = -1.274;
parameter real ddq1 = 0.0109;
parameter real ddq2 = 0.10549;
parameter real dsq1 = 0.078998;
parameter real dsq1n = 0.03108;
parameter real dsq2 = 0.030767;
parameter real dsq2n = 0.043905;
parameter real e0 = 0.527e8;
parameter real ef = 1;
parameter real eg = 0.35;
parameter real epsi = 3.9;
parameter real esq1 = -0.037973;
parameter real esq1n = 0.21722;
parameter real esq2 = 0.11597;
parameter real esq2n = 0.09701;
parameter real eta = 0.1;
parameter real fnsid1hz = 1e-28;
parameter real gamma = 0.06;
parameter real j0 = 1e7;
parameter real jp = 2e8;
parameter real k = 2;
```

```
parameter real l = 2e-8;
parameter real lambda = 0.19;
parameter real mc = 2;
parameter real mr = 0.012;
parameter real mrg = 0.225;
parameter real n0 = 2;
parameter real n1 = 1.8;
parameter real n2 = 1.1;
parameter real na = 14;
parameter real nt = 2;
parameter real phi = 2.65;
parameter real r0 = 0.5;
parameter real r1 = 0.01;
parameter real r2 = 1.3;
parameter real rdw = 0;
parameter real rgwl = 0;
parameter real rsw = 0;
parameter real s = 1;
parameter real tch = 5e-9;
parameter real tox = 2e-9;
parameter integer type = `n_type;
parameter real va = -3.4;
parameter real voff = 0.01;
parameter real voffg = 0.36;
parameter real vp = 0.05;
parameter real vth = 0.17;

real vds, vsd, vdse, vsde, vgs, vgd, mrvalue, egvalue, u0, a, b, ag, bg,
eps, ru, gi, r0p, deltas;
real vgt, vgo, vgoe, vgoen, f, u, e, id;
real vgta, vgoa, vgoea, vgoena, fa, ua, ea, ida, idr;
real rd, rg, rs, gd, gg, gs;
real cdbe, cgbe, cgde, cgse, csbe;
real sid;
real igd, igd0, u0g, uag, vgde, vdge, n, c, apow, apowe;
real vgse, qs, qsn, qsp, qd, asq, bsq, csq, dsq, esq, adq, bdq, cdq, ddq,
asqn, bsqn, csqn, dsqn, esqn, t, sign;

analog
  begin
    @(initial_step or initial_step("static"))
      begin
        u0 = n1*$vt;
        mrvalue = mr*`M0;
```

```
    egvalue = eg*‘CHARGE;
    ru = r0*u0;
    gi = 1/gamma;
    r0p = 1-r0;
    deltas = ‘DELTA*‘DELTA;
    a = w*tch*‘CHARGE*‘CHARGE*‘CHARGE/(8*‘PI*‘PI*‘HBAR*‘HBAR)*
    *sqrt(2*mrvalue/egvalue);
    b = 4*egvalue*sqrt(2*mrvalue*egvalue)/(3*‘CHARGE*‘HBAR);
    eps = epsi*‘EPS0;
    ag = ‘CHARGE*‘CHARGE/(8*‘PI*‘H*eps*phi);
    bg = 8*‘PI/(3*‘H*‘CHARGE)*pow(‘CHARGE*phi,1.5);
    u0g = $vt*nt;
    uag = $vt*na;
    cdbe = cdbew*w*1e6;
    cgbe = cgbew*w*1e6;
    cgde = cgdew*w*1e6;
    cgse = cgsew*w*1e6;
    csbe = csbew*w*1e6;
    rd = rdw/(w*1e6);
    rg = rgwl*w/l;
    rs = rsw/(w*1e6);
    if(rd > 0)
      gd = 1/rd;
    else
      gd = 0;
    if(rg > 0)
      gg = 1/rg;
    else
      gg = 0;
    if(rs > 0)
      gs = 1/rs;
    else
      gs = 0;
  end
vds = type*V(drainprime,sourceprime);
vgd = type*V(gateprime,drainprime);
vgs = type*V(gateprime,sourceprime);
vgt  = vgs-vth;
vdse = ‘VDSMIN*(0.5*vds/‘VDSMIN+sqrt(deltas+(0.5*vds/‘VDSMIN-1)*
*(0.5*vds/‘VDSMIN-1))-sqrt(deltas+1));
// main drain-source tunneling current
vgo  = vgs-voff;
vgoe = ‘VMIN*(1+0.5*vgo/‘VMIN+sqrt(deltas+(0.5*vgo/‘VMIN-1)*(0.5*vgo/‘VMIN-1)));
vgoen = vgoe/(vth-voff);
```

```
f = (1-limexp(-vdse*gi))/(1+limexp((lambda*tanh(vgo)-vdse)*gi));
u = ru+r0p*u0*vgoen;
e = e0*(1+r1*vdse+r2*vgoe);
id = a*f*u*ln(1+limexp((vgt)/u))*e*limexp(-b/e);
// ambipolar drain-source current
vgta = -vgs+2*voff-vth;
vgoa  = -vgo;
vgoea = `VMIN*(1+0.5*vgoa/`VMIN+sqrt(deltas+(0.5*vgoa/`VMIN-1)*
*(0.5*vgoa/`VMIN-1)));
vgoena = vgoea/(vth-voff);
fa = (1-limexp(-vdse*gi))/(1+limexp((lambda*tanh(vgoa)-vdse)*gi));
ua = ru+r0p*u0*vgoena;
ea = e0*(1+r1*vdse+r2*vgoea);
ida = s*a*fa*ua*ln(1+limexp((vgta)/ua))*ea*limexp(-b/ea);
// RTD drain-source current
vsd = -vds;
vsde = `VDSMIN*(0.5*vsd/`VDSMIN+sqrt(deltas+(0.5*vsd/`VDSMIN-1)*
*(0.5*vsd/`VDSMIN-1))-sqrt(deltas+1));
idr = -w*tch*(jp*vsde/vp*k*vgoe*limexp(1+(-vsde+eta*vgs)/vp)+
+j0*(limexp(vsd/n2/$vt)-1));
id = id + ida + idr;
// charge
vgse = `VMIN*(1+0.5*vgs/`VMIN+sqrt(deltas+(0.5*vgs/`VMIN-1)*(0.5*vgs/`VMIN-1)));
adq = adq1*vds + adq2;
bdq = bdq1*vds + bdq2;
cdq = cdq1*vds + cdq2;
ddq = ddq1*vds + ddq2;
asq = asq1*vds + asq2;
bsq = bsq1*vds + bsq2;
csq = csq1*vds + csq2;
dsq = dsq1*vds + dsq2;
esq = esq1*vds + esq2;
asqn = asq1n*vds + asq2n;
bsqn = bsq1n*vds + bsq2n;
csqn = csq1n*vds + csq2n;
dsqn = dsq1n*vds + dsq2n;
esqn = esq1n*vds + esq2n;
qd = -(-adq*ln(1+limexp((vgse-bdq)/adq))+cdq*vgse +
+ddq)*w*l*epsi*`EPS0/tox+cfdw*w*1e6*vgd;
qsp = -(asq*ln(1+tanh(bsq*vgse+csq))+dsq*vgse +
+esq)*w*l*epsi*`EPS0/tox*1e15;
qsn = -(asqn*ln(1+tanh(bsqn*vgse+csqn))+dsqn*vgse +
+esqn)*w*l*epsi*`EPS0/tox*1e15;
if(qsn == 0) begin
```

```
  t = qsp*1e-15;
end else if(qsp == 0) begin
  t = qsn*1e-15;
end else begin
  t = 1/pow(qsp,13)+1/pow(qsn,13);
  if(t < 0) begin
    sign = -1;
  end else begin
    sign = 1;
  end
  t = sign/pow(sign*t,1.0/13)*1e-15;
end
qs = -t+cfsw*w*1e6*vgs;
// Noise calculations
sid = 2*‘CHARGE*id;
// Gate leakage current
vgde = ‘VMIN*(1+0.5*vgd/‘VMIN+sqrt(deltas+(0.5*vgd/‘VMIN-1)*(0.5*vgd/‘VMIN-1)));
vdge = ‘VMIN*(1+0.5*(-vgd)/‘VMIN+sqrt(deltas+(0.5*(-vgd)/‘VMIN-1)*
*(0.5*(-vgd)/‘VMIN-1)));
apow = 1-(vgde+vdge)/phi;
apowe = ‘AMIN*(1+0.5*apow/‘AMIN+sqrt(deltas+(0.5*apow/‘AMIN-1)*
*(0.5*apow/‘AMIN-1)));
n = eps/tox*(u0g*ln(1+limexp((vgd-voffg)/u0g))+
+uag*ln(1+limexp(-(vgd-va)/uag)));
c = vgd/tox*limexp(20/phi*pow((vgde+vdge)/phi,agate)*
*(1-(vgde+vdge)/phi));
igd0 = n0*ag*c*n;
igd = igd0*limexp(-tox*bg/(vgde+vdge)*sqrt(2*mrg*‘M0)*
*(1-pow(apowe,1.5)))*l*w;
// Augment the matrix
I(gateprime,sourceprime) <+ type*ddt(qs);
I(gateprime,drainprime) <+ type*(ddt(qd)+igd);
I(drain,bulk) <+ type*ddt(cdbe*V(drain,bulk));
I(gate,bulk) <+ type*ddt(cgbe*V(gate,bulk));
I(gate,drain) <+ type*(ddt(cgde*V(gate,drain)));
I(gate,source) <+ type*ddt(cgse*V(gate,source));
I(source,bulk) <+ type*ddt(csbe*V(source,bulk));
I(drainprime,sourceprime) <+ type*id;
// the next lines should have read: I(drainprime,sourceprime) <+
white_noise(sid,"id")
// and I(drainprime,sourceprime) <+ flicker_noise(fnsid1hz,ef,"1overf")
// but that construct messes up ac analysis in both eldo and spectre
I(drain,source) <+ white_noise(sid,"id");
I(drain,source) <+ flicker_noise(fnsid1hz,ef,"1overf");
```

```
      if(rd > 0)
        begin
          I(drain,drainprime) <+ gd*V(drain,drainprime);
          I(drain,drainprime) <+ white_noise(4*`KB*$temperature*gd,"thermal");
        end
      else
        V(drain,drainprime) <+ 0.0;
      if(rs > 0)
        begin
          I(source,sourceprime) <+ gs*V(source,sourceprime);
          I(source,sourceprime) <+ white_noise(4*`KB*$temperature*gs,"thermal");
        end
      else
        V(source,sourceprime) <+ 0.0;
      if(rg > 0)
        begin
          I(gate,gateprime) <+ gg*V(gate,gateprime);
          I(gate,gateprime) <+ white_noise(4*`KB*$temperature*gg,"thermal");
        end
      else
        V(gate,gateprime) <+ 0.0;
    end
endmodule
```

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