Aalto University
School of Electrical
Engineering

HUAWEI

Master Thesis

PROGRAMMING TRANSCEIVERS FOR A 5G MILLIMETER-WAVE MOBILE PHONE ANTENNA TEST-BED

submitted in partial fulfillment of the requirements to obtain the academic degree

Master of Science in Communication and Computer Networks

Politecnico
di Torino

Dipartimento di Elettronica e Telecomunicazioni

Author	Ali KOURANI
Student ID	s277824
Supervisor	Prof. Roberto GARELLO
University	Politecnico di Torino
Institute	Dipartimento di Elettronica e Telecomunicazioni
Supervisor	Prof. Katsuyuki HANEDA
University	Aalto University
Institute	Department of Electronics and Nanoengineering

Helsinki, Feb 2022

Abstract

With the development of wireless communication technologies, the Fifth Generation of mobile communication (5G) systems emerges introducing new aspects of exploiting the mmWave spectrum frequencies to serve different services (concerning mMTC and URLLC), and to deliver higher channel capacity and throughput supporting extremely growing number of devices. Upon this technological growth in the wireless communications systems, the antenna system rises to play a crucial role in extending the service capabilities in the latest generations upon being the interface between the User Equipment (UE) electronic system and air which signal traverses using mmWave spectrum. With new spectrum-related challenges such as higher carrier frequencies (millimeter waves operating at 28 GHz and 39 GHz, wider transmission bands) imposing different impairments (Higher frequencies face strong Doppler impairments because of the linear dependency of Doppler shift with carrier frequency, higher Free Space Path Loss (FSPL) which is proportional to the carrier frequency) and electromagnetic (EM) waves travelling behaviours, the need of effective testing methods for antennas systems reserves an important spot of focus.

Over-The-Air (OTA) testing is seen as inevitable for 5G antenna systems. The Multi-Probe Anechoic Chamber (MPAC) setup, being one of the OTA methods, is a potential method for the evaluation of 5G antenna systems under real-world propagation conditions. Validation of emulated channel models in the practical MPAC setup is essential, since it is important to ensure that the target channel models are correctly emulated.

The course of this thesis work focuses on implementing a basic component of the MPAC setup, the fading emulator, using off-the-shelf devices being Software- Define Radio (SDR) devices in our work. The method emulates electromagnetic environments of 5G mobile communications devices trying to mimic real link conditions through excitation of the Device Under Test (DUT) from multiple dynamic angles of illumination, thus representing realistic operating conditions for 5G New Radio (NR). Therefore, a system of Universal Software Radio Peripheral (USRP) devices delivering 5G realistic signals mimicking 5G electromagnetic environment has been implemented.

Acknowledgements

First and foremost, I would like to express my gratitude to my supervisor at Aalto University Professor Katsuyuki Haneda for giving me the opportunity to work in this futuristic project. His support and guidance has been instrumental in this work. I would also like to thank Dr. Clemens Icheln for continuously providing me with his invaluable feedback besides Professor Haneda. I would also gratefully thank Prof. Roberto Garello, my academic supervisor at Politecnico di Torino, for assessing my master thesis work. I am also thankful to Dr. Pasi Koivumaki for his help and vivid advices of different topics.

Last but not the least, I would like to thank my colleagues at Aalto University, my friends and my family for supporting me throughout this project helping me keep an eye with strong will on being a future contributing hand in scientific development and extension of human kind capabilities.

Contents

1 Introduction **1**
- 1.1 Motivation . . . 1
- 1.2 Thesis Outline . . . 1

2 Literature Review **3**
- 2.1 Reverberation chamber (RC) . . . 3
- 2.2 Multi-Probe Anechoic Chamber (MPAC) . . . 5

3 System Model **7**
- 3.1 Architecture of the proposed OTA antenna evaluation technique . . . 7
- 3.2 5G signals . . . 8
  - 3.2.1 Orthogonal Frequency-Division Multiplexing (OFDM) . . . 8
  - 3.2.2 Orthogonal Frequency-Division Multiple Access (OFDMA) . . . 10
  - 3.2.3 Signal Weighting . . . 11
- 3.3 RF models . . . 14
  - 3.3.1 Probe Antennas . . . 14
  - 3.3.2 Device Under Test (DUT) . . . 14

4 Implementation **15**
- 4.1 Hardware . . . 15
  - 4.1.1 Software Defined Radio . . . 15
  - 4.1.2 Clock Distribution Device: CDA-2990 . . . 17
  - 4.1.3 Cabled Switch Device : CPS-8910 . . . 18
- 4.2 Software: LabVIEW Communication System Design Suite . . . 19
  - 4.2.1 Introduction to Labview programming . . . 19
  - 4.2.2 Host Programming . . . 20
  - 4.2.3 FPGA Programming . . . 20
- 4.3 Synchronizing Multiple USRPs . . . 21
  - 4.3.1 Clock synchronization . . . 22
  - 4.3.2 Time synchronization . . . 22
- 4.4 Programming a Single Transmitter Channel . . . 22
  - 4.4.1 Initialization of USRPs and Bit Streams . . . 23

4.4.2 HOST-USRP Communication: HOST-to-Target FIFO 24
4.4.3 FPGA: Digital Part: OFDM TX 25
4.4.4 FPGA: Analog part: Transmitter core 28
4.5 Programming the Receiver Channel 29
4.5.1 FPGA: Analog Part: Receiver Core 29
4.5.2 FPGA: Digital Part: OFDM RX 30
4.5.3 USRP-HOST Communication: TARGET-to-HOST FIFO 32
4.5.4 HOST: Offline post-processing of Received Symbols 34
4.6 Single TX Single RX System Implementation Summary 34
4.7 Programming Two TX Channels on a single USRP 35
4.7.1 Additions to the HOST TX Code 35
4.7.2 Additions to the FPGA TX Code 36
4.8 Programming Four TX Channels on a Two USRP 38
4.8.1 Further Additions to the HOST TX Code 38
4.8.2 Further Additions to the FPGA TX Code 39
4.9 Programming the Receiver 41
4.9.1 Additions to the FPGA RX code 41
4.9.2 Additions to the HOST RX code 42
4.10 Multiple TX Single RX System Implementation Summary 42
4.11 Calibration 43
4.11.1 HOST: Precoding Weights Generation 43
4.11.2 FPGA: Calibrator Block 44

5 Evaluation of the System **47**
5.1 Results 47
5.1.1 RX Constellation of a Single Channel 47
5.1.2 Manual Calibration of Two TX channels 48

6 Conclusion & Outlook **51**
6.1 Thesis Contributions 51
6.2 Improvement and Future Works 51

Acronyms **53**

Glossary **57**

Bibliography **59**

List of Figures

2.1 Reflective walls of the RC. . . . 3
2.2 RC equipped with mechanical stirrers. . . . 4
2.3 MPAC system setup. . . . 5
2.4 Anechoic chamber at Aalto University. . . . 6

3.1 Proposed MPAC system experimental setup. . . . 8
3.2 OFDM. . . . 9
3.3 Cyclic Prefix. . . . 10
3.4 Example of how frequency subcarriers is distributed for 2-TX case. . . . 11
3.5 TX and RX antenna distribution. . . . 12

4.1 USRP-2954 device. . . . 16
4.2 USRP-2954 device front panel. . . . 16
4.3 USRP-2954 device back panel. . . . 16
4.4 USRP-2954 block diagram. . . . 17
4.5 OctoClock-G CDA-2990. . . . 18
4.6 OctoClock-G CDA-2990 front panel. . . . 18
4.7 CPS-8910 front panel. . . . 18
4.8 Connection between the common clock CDA-2990 and the USRPs for synchronization. . . . 21
4.9 Block diagram of the HOST TX code for single channel. . . . 22
4.10 User to the "Open and Configure" code. . . . 23
4.11 Random bit stream generator. . . . 24
4.12 HOST to USRP data transfer using the WRITE DMA FIFO block. . . . 24
4.13 FPGA code receiving data bits from HOST through "Tx Stream 0" FIFO . 25
4.14 Block diagram of the "OFDM TX" code. . . . 26
4.15 "OFDM TX" code. . . . 26
4.16 QPSK mapper code. . . . 26
4.17 Interleaved sequence of pilot and data subcarriers. . . . 27
4.18 Single OFDM frame subcarriers composition. . . . 27
4.19 "OFDM mod" code. . . . 28

4.20 Portion of transmitter core code where samples are read and forwarded for processing to be prepared for output transmission. 28
4.21 Block diagram of the FPGA RX code. 29
4.22 Portion of receiver core code where received symbol's samples are acquired and forwarded for OFDM processing. 29
4.23 "OFDM RX" code. 30
4.24 OFDM demod code. 31
4.25 OFDM RX block inputs samples from "Rx Samples" and outputs processed data "Rx CH Estimates" and "RX UNEQ Symbols" for USRP-HOST communication. 32
4.26 Read DMA FIFO blocks inputting received data from the corresponds FIFOs. 33
4.27 Queuing of channel estimates and unequalized symbols. 33
4.28 Equalizer. 34
4.29 QPSK demapping. 35
4.30 Block diagram of the implemented single TX single RX system. 35
4.31 HOST TX code update for 2 TX channels system. 36
4.32 HOST TX code update for 2 TX channels system. 37
4.33 Subcarrier distribution of OFDM frame emitted from RF0 channel. 37
4.34 Subcarrier distribution of OFDM frame emitted from RF1 channel. 37
4.35 Updated HOST TX code block diagram to serve 4 TX channels. 38
4.36 Subcarrier distribution of OFDM frame emitted from U1 RF0 channel. . . 40
4.37 Subcarrier distribution of OFDM frame emitted from U1 RF1 channel. . . 40
4.38 Subcarrier distribution of OFDM frame emitted from U2 RF0 channel. . . 40
4.39 Subcarrier distribution of OFDM frame emitted from U2 RF1 channel. . . 41
4.40 Subcarrier distribution of combined OFDM frames emitted from all channels. 41
4.41 Updated "OFDM RX" block diagram. 42
4.42 Block diagram of the multiple TX single RX implemented system. 43
4.43 Weights are generated from queued Channel estimates and are fed to TX code. 44
4.44 Calibrator block is inserted into the "OFDM TX" block code. 45
4.45 Block diagram of the Calibrator. 45
4.46 Calibrator code. 45

5.1 Received QPSK Symbols after equalization for Single-TX Single-RX system. 47
5.2 Received QPSK Symbols testing reception from different implemented channels. 48
5.3 Received QPSK Symbols with two channels transmitting instantly showing constructive interference. 49

CHAPTER

1 Introduction

1.1 Motivation

With the on-going deployment of 5G, the number of devices for radio communications will be exploding; 5G and beyond will exploit available spectrum aggressively from legacy below-6 GHz to new above-6 GHz radio frequencies (RF). When compared to sub-6 GHz spectrum, these higher frequencies incur greater attenuation due to path loss and blockages, necessitating the use of directional antennas at both ends of the communications link [1].

With the aim of evaluating overall communication performance that combines the performances of the mobile terminal antenna and the RF transceiver section in the device important challenges are to be faced. The challenges for example are: lack of statistical properties of the electric field distributions over our living spaces that a radio device exploits for communications compared to below-6GHz, which hence requires more measurement-based studies of the differences (e.g., mmWaves are short-range waves, they could be absorbed by gases and moisture in the atmosphere compared to sub-6GHz waves, besides different reflection behavior based on the dependency between wavelength and object size), arrangement of the most accurate and flexible test facility is so costly in terms of required hardware that it is unaffordable as a practical test method. In the face of these challenges, OTA stands out as a suitable operational test method revealing the new spectrum performance and operability. OTA testing methods have some advantages over field trials such as repeatability, measurement, and cost efficiency, thus the evaluation method ought to mimic realistic propagation conditions to accurately assess the performance of the DUT in the field [2].

1.2 Thesis Outline

This section gives the outline of this thesis work. The introduction is exhibited in Chapter 1 where the motivation and goals are elaborated. A literature review is presented

in Chapter 2, for emphasizing the field of study of this thesis and the target aim concept followed during the course of this thesis. The latter explains:

- The different paradigms of test methods, which are necessary for understanding how testing techniques could serve our purpose.

- The overview of the necessary improvement in the existing OTA antenna test setup. The improvement is addressed in this thesis as later explained in Chapter 3.

Chapter 3 describes the system model of the entire OTA test setup. It also explains the baseband system model and the paradigm followed in the improvement of an MPAC testing setup. Chapter 4 exhibits the full implementation of the target improvement (fading emulator) from both hardware and software aspects. Finally, the implemented baseband setup test results are shown in Chapter 5 and the conclusion with the outlook, follows in Chapter 6.

CHAPTER

2 Literature Review

As mentioned, the increasing demand for higher data rates from end-users of wireless devices has led to the emerging of new wireless terminals based on advanced antenna systems. Characterization of antenna performance had been performed in anechoic chambers in a point-to-point sense. However, since modern wireless devices require a multipath environment to reach the intended performance, new upgrades are needed. Assessment of the overall performance of multi-element antenna systems thus requires new measurement methodologies, which in some way can emulate a multipath environment. Under the scope of this course, Reverberation Chamber (RC) and Multi-Probe Anechoic Chambers (MPAC) emerge as major OTA testing methods.

2.1 Reverberation chamber (RC)

The RC has traditionally been used for electromagnetic compatibility (EMC) tests. In the last two decades it found application in various OTA tests of antennas and wireless devices. The RC is an electrically large cavity, where mechanical mode stirrers are employed to stir the electromagnetic field to create a random-like multipath environment [3].

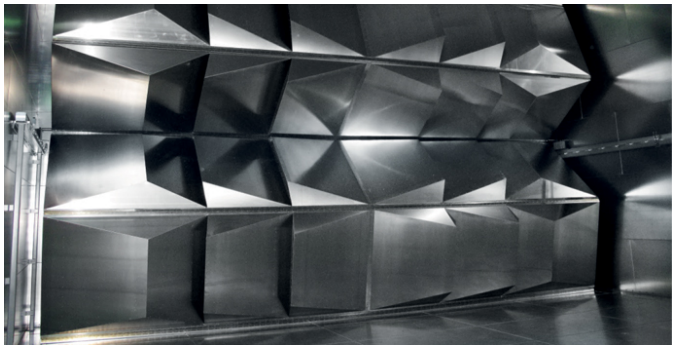


Figure 2.1: Reflective walls of the RC.

Being inside an RC is being inside a Faraday cage, the walls and the ceiling are completely reflective. That is all what is needed so that for any device turned on, there is going to be zero Radio Frequency (RF) getting inside. If we introduce a transmitter, depending on its position, the reflections are going to come from everywhere. Having what is called RF stirrers (see Figure 2.2), they constantly rotate thus literally stirring RF waves reproducing instantaneous dynamic electric fields over space in a metallic box. Waves reverberate inside the box and create a standing wave like a realistic operational environment, either indoor or outdoor. The reverberation chamber easily creates angularly uniform incoming fields over receiving angles of plane waves at DUT, leading to a typical spatial electric field distribution of below-6GHz practical cellular environments [4]. The cited paper [4] shows that the chamber is also capable of creating angularly selective incoming fields, which is required for emulating spatial field distributions for above-6GHz.

Figure 2.2: RC equipped with mechanical stirrers.

However, a major drawback of the RC is its limited control of the Power Angular Spectrum (PAS) of the emulated channel. It is usually regarded that the PAS in a well-stirred RC is statistically 3D isotropic [5]. Anisotropy can be achieved by partially covering internal walls of the RC with electromagnetic absorbers , i.e., [6], [7]. It is usually believed that the RC is not suitable for measuring radiation patterns of antennas. Recently, radiation characteristics have been measured in the RC by using the K-factor, i.e., [8], [9] or Doppler shift [10].

2.2 Multi-Probe Anechoic Chamber (MPAC)

Another compelling method as mentioned earlier is the MPAC method [11]. MPAC provides a shielded environment for performing over-the-air testing of mobile devices. MPACs provide the means to measure Multi-Input Multi-Output (MIMO) and radio resources management performance under fading conditions to verify and validate antenna performance parameters. Those chambers are configurable with different numbers and positions of probe antennas to support different use cases. With this method it is possible to reproduce time-varying spatial field distributions of any realistic condition in an anechoic chamber. The intended field distributions for a DUT are created by fields transmitted from a large number of probe antennas with help of a fading emulator, as illustrated in the Figure 2.3 below.

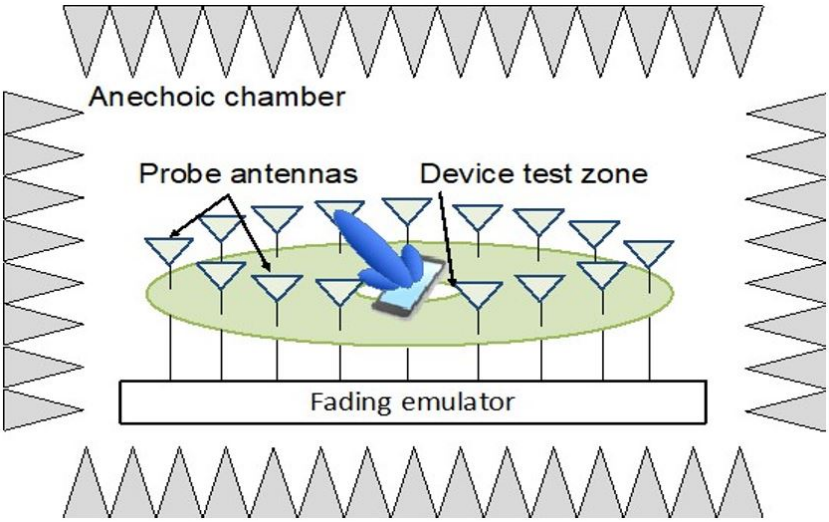


Figure 2.3: MPAC system setup.

The output ports of the fading emulator are connected to the respective antenna probes of the chamber. This same test system configuration can be used to test the BS when the BS is the DUT.

The method is accurate and fully controllable in reproducing realistic spatial electric field distributions in the test zone of DUT but becomes exceedingly difficult to implement at above-6GHz RF due to extensive hardware requirements. For example, the number of dual-polarized probe antennas must be at least 20 when evaluating a physically small printed inverted-F antenna at 28 GHz [12]. Recent studies of MPAC-based OTA antenna testing appear in standardization discussions of cellular industry, i.e., 3GPP RAN4 meetings e.g., [R4-1705831, R4-1814835, R4-2002478] among others. The studies report

feasibility of reproducing 28 GHz multipath environment when beamforming is used at the base station.

The overall goal of this project is to demonstrate that realistic spatial electric field distributions can be emulated in an anechoic chamber using a reduced-complexity MPAC based method utilizing loaded reflectors alongside the active probes using a reduced complexity fading emulator upon which this thesis work focuses. Using off-the-shelf devices, the fading emulator is to be implemented to a basic part of the OTA MPAC testbed being developed.

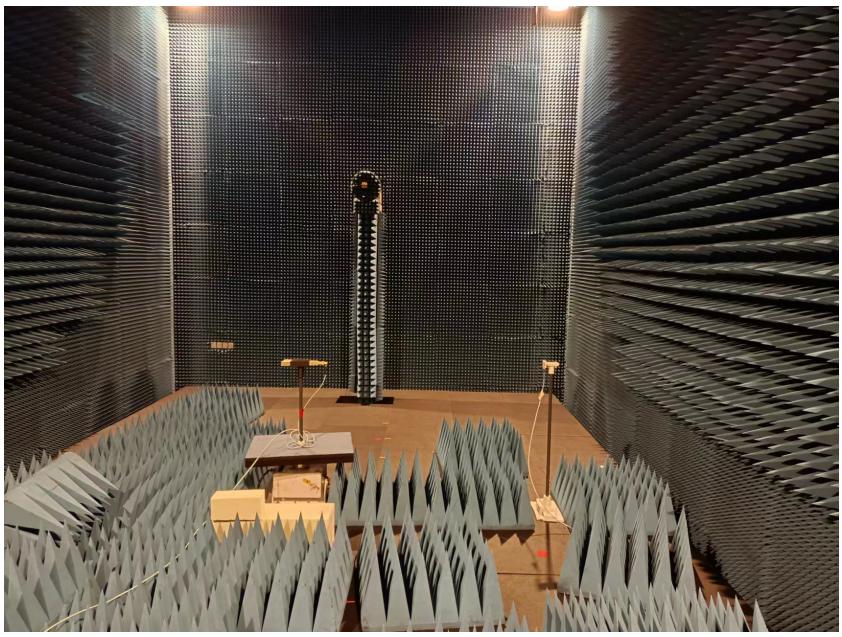


Figure 2.4: Anechoic chamber at Aalto University.

CHAPTER

3 System Model

This chapter proposes a system model for the OTA testing method which this thesis work is about. First, an overview on the MPAC method setup we aim at implementing is presented. A glance about the antenna test environment and setup upgrade that we aim to implement is given. Afterwards, an overview is exhibited on the baseband processing section of the signals aimed to traverse the test zone. Those signals are meant to mimic realistic 5G signals and to create a medium multipath rich environment surrounding the UE and base station (BS). Later, some of the system components are presented shedding light on their role in the functioning system.

3.1 Architecture of the proposed OTA antenna evaluation technique

As we expressed earlier, the aim of the project which this thesis work involved in is to implement an MPAC system setup using off-the-shelf devices. For this purpose, SDRs are used replacing the fading emulator playing the same role with less complexity, dynamic, and cost-effective setup. The system setup design is expressed in Figure 3.1.

Apparently the system setup is to be installed in an anechoic chamber where Aalto's large anechoic chamber serves the purpose. The experimental setup includes a limited number of USRPs, dual-polarized probe antenna arrays, and loaded reflectors, all of which are installed in an anechoic chamber. The USRP synchronously send intended waveforms to the probe antennas. The emulated spatial field distributions are compared with target field distributions representing realistic channels for above-6GHz. The demonstration includes emulating channels with varying multipath richness. Those USRPs are connected to a synchronization, triggering, and control setup, which is to be detailed later in Chapter 4. A main component of this controlling block is the HOST PC having the programming environment needed to program the USRPs to operate as desired processing, transmitting, and receiving waveforms intended to traverse the test zone.

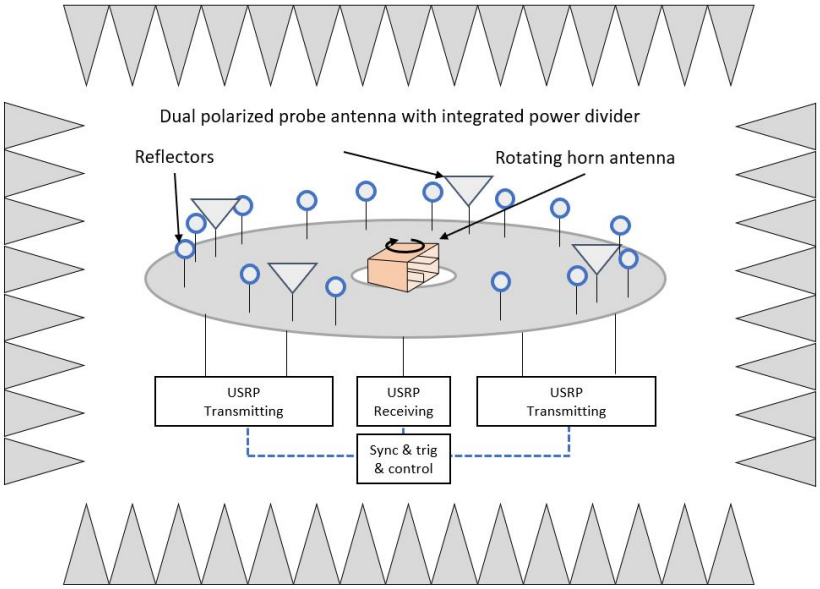


Figure 3.1: Proposed MPAC system experimental setup.

3.2 5G signals

Creating a multipath rich RF environment for OTA testing of new technologies requires that the signals emitted by the fading emulator and equivalent setup traversing the test zone should mimic those used in the technology under which the antenna performance is to be studied. So the focus will fall on the baseband signal generation to be as realistic as those in 5G.

3.2.1 Orthogonal Frequency-Division Multiplexing (OFDM)

Orthogonal Frequency-Division Multiplexing (OFDM) has been the transmission scheme used for 3GPP LTE and is also used for several other radio-access technologies, for example Worldwide Interoperability for Microwave Access (WiMAX) and the Digital Video Broadcasting (DVB) broadcast technologies. It continued to be an efficient modulation format used in modern wireless communication systems of 5G. OFDM combines the benefits of Quadrature Amplitude Modulation (QAM) and Frequency-Division Multiplexing (FDM) to produce a high-data-rate communication system.

OFDM is a combination of multiplexing and modulation technique where multiplexing points to method of sharing a Bandwidth (BW) by independent data channels and

modulation points to mapping the information on the change in amplitude, phase, frequency, or a combination of that. It evolves from the FDM transmission scheme in which the available band is divided into smaller sub-bands hence multiplexing different transmission sub-channels to serve the overall data transmission scheme.

The basic concept of OFDM was first proposed by R. W. Chang [13], presuming a broad definition of OFDM as FDM in which sub-channels overlap without interfering. The subcarriers are separated such that they physically overlap in frequency, but the first zero crossings of one subcarrier fall on the peaks of the two adjacent subcarriers. In fact, all zero crossings of a subcarrier fall on the peaks of all adjacent subcarriers as shown in Figure 3.2. Because OFDM recovers the data symbol at the peak of each subcarrier, the subcarriers are orthogonal to each other and there is no interference hence the term orthogonal FDM (OFDM) [14].

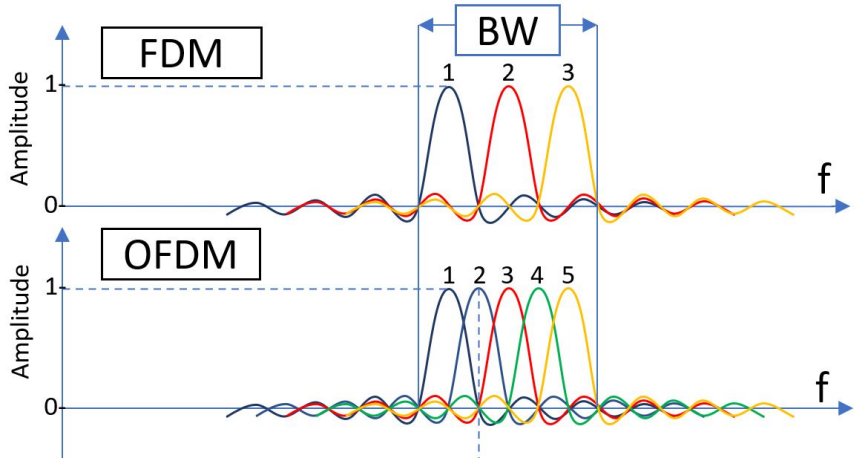


Figure 3.2: OFDM.

OFDM, through substituting the BW of transmission by an array of narrow bands with orthogonal subcarriers, limits the Intersymbol Interference (ISI) phenomena by increasing the symbol time where it becomes significantly large compared to delay spread of the channel.

Further upgrade on the transmission scheme included the addition of Cyclic Prefix (CP). CP is adding a copy of the symbol tail into the beginning of the symbol where this copy acts as a guard interval between symbols eliminating ISI. In our task implementation, Cyclic Prefix Orthogonal Frequency-Division Multiplexing (CP-OFDM) transmission scheme has been adopted.

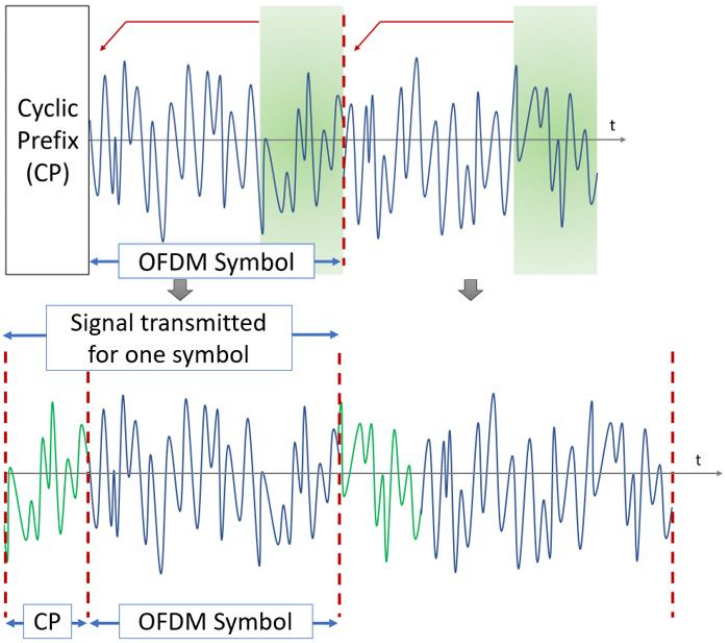


Figure 3.3: Cyclic Prefix.

3.2.2 Orthogonal Frequency-Division Multiple Access (OFDMA)

Whereas OFDM assigns one block (in time) to one user, Orthogonal Frequency-Division Multiple Access (OFDMA) is a scheme that assigns different groups of subcarriers (in frequency) to different users. In this way, more than one user can access the air interface at the same time. Recent studies of MPAC-based OTA antenna testing appearing in standardization discussions of cellular industry, i.e., 3GPP RAN4 meetings e.g., [15], [16], [17], report feasibility of reproducing 28 GHz multipath environment when beamforming is used at the base station. They conclude 6 single-polarized probes would be sufficient to emulate standardized channels i.e., cluster delay line CDL-A models [18] using a fixed installation of probes in a chamber. In our system implementation, four dual-polarized probe antennas beside the loaded reflectors designed in other task of the full project are involved in creating the intended multipath channel profile to emulate. For this sake, an OFDMA approach has been used as a multiple access scheme assigning resources for channels' estimates.

Our system will be exploiting a band of transmission of 2.3 MHz consisting of 512 subcarriers divided into 470 data and reference subcarriers (pilot) and 42 guard subcarriers. Over two sets of 235 orthogonal subcarriers distributed over the transmission band, the resources are allocated in a repeated manner of consecutive subcarriers. Each one of

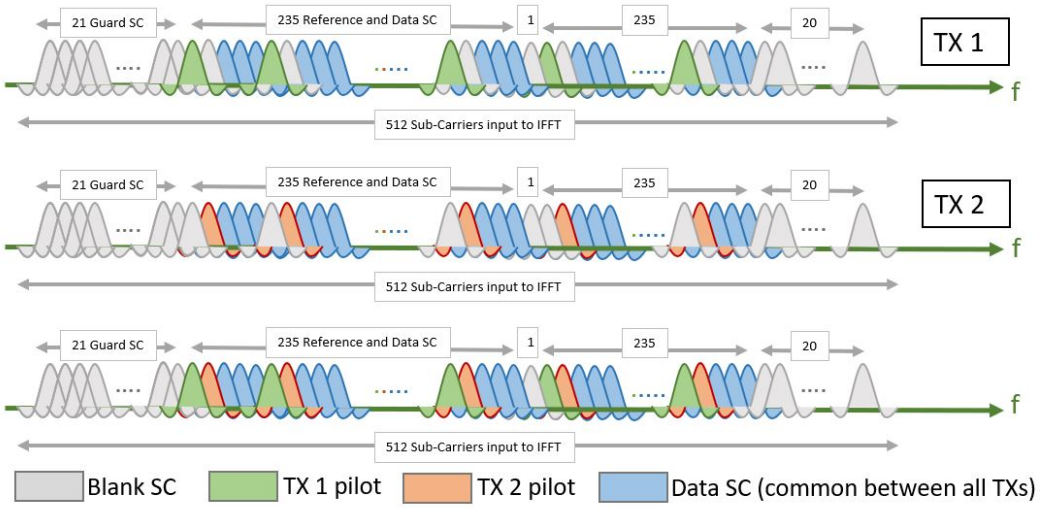


Figure 3.4: Example of how frequency subcarriers is distributed for 2-TX case.

the first four subcarriers is assigned to one of the different transmission channels to transmit its pilot symbol on. Pilot also called reference symbols are symbols known at both the transmitter and receiver sides. They are used for channel estimation. The fifth subcarrier will be a data subcarrier shared by all the channels. Hence, data symbols from different channels which will be holding the same data will be interfering over air. This is an attempt to prepare the system for later calibration and beamforming applications. Figure 3.4 shows how the resources are allocated based on the OFDMA scheme.

3.2.3 Signal Weighting

To meet the increasing rate demand in wireless networks, multiple antennas have been employed at the the transmitting and the receiving ends. That led to Multi Input Single Output (MISO), Single Input Multi Output (SIMO), and MIMO systems have been developed and found their application in the 4th generation of mobile networks and beyond. For example in MISO systems, the channel capacity is increased according to Equation (3.1) when Signal to Noise Ratio (SNR) is improved by exploiting multiple antennas transmitting over multipath-rich channels. Hence, under the application of beamforming algorithms, those systems exploit spatial diversity of the channels. Copies of the signal holding the same message are transmitted over different channels.

Considering transmitter diversity scenarios, those signals are weighted at different transmitters depending on each transmitter-receiver channel. Weighting is applied to

compensate channel effect causing amplitude distortion and phase rotation uniquely depending on the channel traversed by each transmission. This results in a constructive interference of different copies arriving from different paths at the receiver with a Maximum Ratio Combining (MRC). Power is thus collected from different copies serving higher signal level. The above introduced approach shows the need of communication channel knowledge which is done on OFDMA basis in our implemented setup explained in Section 3.2.2.

Let us assume that the transmitted signal X is mapped into antennas' signals $X_i = w_i X$ by using, at different TX antenna's different weights $w_i, i = 1, 2, 3, ..., N$

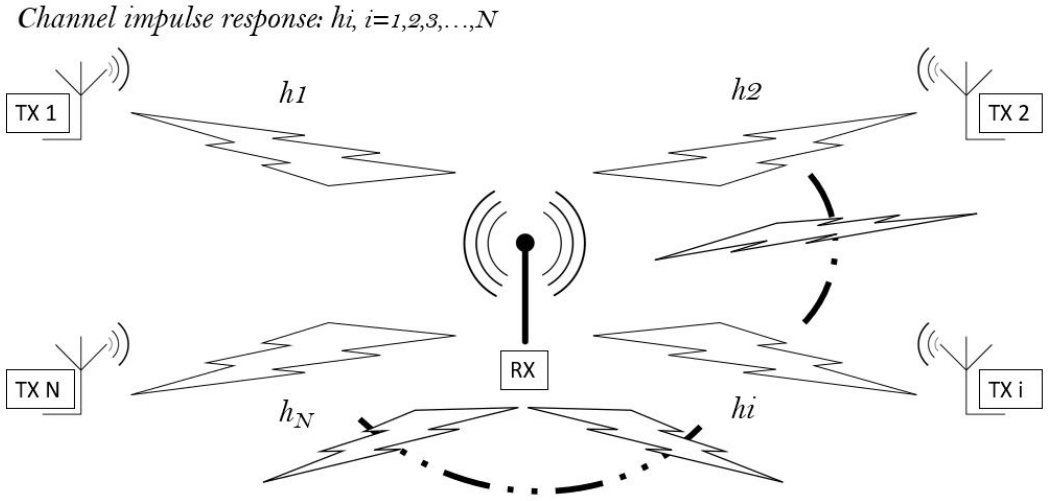


Figure 3.5: TX and RX antenna distribution.

Then the channel equation for a $N \times 1$ MISO system will be will:

$$Y = \sum_{i=1}^{N} h_i X_i + Z$$

where Z refers to noise We consider operating in a Rayleigh multipath channel and zero-mean iid transmitted symbols. Let $X \sim CN(0, P_x)$ and $Z \sim CN(0, P_z)$ where P_x is the symbol power and P_z is the noise power.

The average SNR is:

$$SNR = \frac{|\sum_{i=1}^{N} h_i w_i|^2 P_x}{P_z}$$

Let $\mathbf{h} = (h_1, h_2, \cdots, h_N)$ and $\mathbf{w} = (w_1, w_2, \cdots, w_N)$

According to Cauchy Schwarz inequality:

$$|\mathbf{h}^T\mathbf{w}|^2 \leq \|\mathbf{h}\|^2\|\mathbf{w}\|^2$$

$$|\sum_{i=1}^{N} h_i w_i|^2 \leq (\sum_{i=1}^{N} |h_i|^2)(\sum_{i=1}^{N} |w_i|^2)$$

This implies:

$$SNR = \frac{|\sum_{i=1}^{N} h_i w_i|^2 P_x}{P_z} \leq \frac{(\sum_{i=1}^{N} |h_i|^2)(\sum_{i=1}^{N} |w_i|^2)P_x}{P_z}$$

For the above inequality, equality case is achieved for $w_i = h_i^*$ meaning the optimum SNR is achieved when weights applied are equal to channel response conjugates.

Then the optimum SNR in the cosidered MISO system is:

$$SNR = \frac{|\sum_{i=1}^{N} h_i w_i|^2 P_x}{P_z}$$

$$SNR = \frac{|\sum_{i=1}^{N} h_i w_i| P_{TX}}{P_z} = \frac{(\mathbf{h}^T\mathbf{h})P_{TX}}{P_z}$$

where P_{TX} is the total transmitted power of symbols X_i output from each Transmitter (TX) antenna. Hence we get:

$$R_b \leq C = B\log_2(1 + \frac{(\mathbf{h}^H\mathbf{h})P_{TX}}{P_z}) \quad bits/sec \tag{3.1}$$

$$R_b : Bit \quad Rate \quad C : Channel \quad Capacity \quad B : Bandwidth$$

When the signal is weighted by the channel response conjugate normalized, the channel effect imposed by the distance between the TX and the Receiver (RX) will be eliminated as if the distance between the TX and RX is zero. Hence, weighting each transmitter output signal by the corresponding weight calculated from the channel estimate associated with it will result in scheme where all the transmitters are at zero distance from the receiver. All those signal's copies are adding constructively "only" at the position of the receiver or in the direction of the receiver in other beamforming or beam steering approaches.

This process is called conjugate beamforming, or we can also address it by calling it calibration. Later after our system implementation, we will consider weighting each transmitter output signal with the normalized channel estimate conjugate to reach our far goal of achieving maximum ratio combining in future work.

3.3 RF models

As emphasized, testing is performed where a set of probe antennas are placed in a ring distribution inside surrounding the DUT. Each antenna connected to the channel emulator system transmits signals with a specific resources distribution according to OFDMA to accomplish the desired channels' estimates and multiple access scheme.

3.3.1 Probe Antennas

Probe antennas are used in a wide variety of applications due to their high-power handling capability, low loss, high directivity, and near constant electrical performance across a broad BW. A separate project task focuses on the design of the probe antennas concerning their operation frequency and the radiation pattern trying to mimic antenna systems willing to be deployed in 5G and beyond systems.

In addition, some probe antennas that would have been connected to an active device (e.g., a fading/channel emulator) are replaced by specific geometrical bodies – to be designed in separate work- with reflective properties capable of producing coherent phase-rotating scattered fields at the location of the DUT. This contributes to complexity reduction in the testbed implementation. An example of similar work is exhibited in [19] where ellipsoidal reflectors are used in the test method in study.

3.3.2 Device Under Test (DUT)

A mobile phone antenna is the RF component the test-bed target to evaluate. It plays the role of the DUT. This mobile phone antenna would be connected to the receiving USRP employed as the baseband unit processing signals received from different paths which performs channel estimation and loads the estimates and the data symbols to the HOST laptop for later data processing.

CHAPTER

4 Implementation

This chapter gives a full explanation of the baseband implementation of the system generating the realistic 5G signal. The explanation exhibits the components of hardware setup and software drivers and programming environments used where the programming of different system stages is also expressed.

4.1 Hardware

4.1.1 Software Defined Radio

With the outstanding growth in the means of data communications, control communications, wireless and remote autonomous services etc, modifying radio devices easily and cost-effectively has become business critical. Traditional hardware-based radio devices limit cross-functionality and can only be modified through physical intervention. This results in higher production costs and minimal flexibility in supporting multiple waveform standards. By contrast, software defined radio technology provides an efficient and comparatively inexpensive solution to this problem. It defines a collection of hardware and software technologies where some or all the physical layer functions are software defined or modified by means of firmware operating on programmable processing technologies.

These devices include Field Programmable Gate Array (FPGA), Digital Signal Processing (DSP), General Purpose Processor (GPP), System on Chip (Soc) or other application specific programmable processors. The use of these technologies allows new wireless features and capabilities to be added to existing radio systems without requiring new hardware [20].

Under the scope of mentioned capabilities introduced by the SDR, We use in our baseband system implementation National Instruments (NI) USRP-2954 devices for the generation of realistic 5G signals needed in the test zone. The USRP-2954 provides

Figure 4.1: USRP-2954 device.

an integrated hardware and software solution for rapidly prototyping high-performance wireless communication systems.

Built on the Laboratory Virtual Instrument Engineering Workbench (LabVIEW) reconfigurable I/O (RIO) architecture, USRP RIO delivers an integrated hardware and software solution, so researchers can prototype faster and shorten time to results. A range of advanced research applications that include MIMO can be prototyped; synchronization of heterogeneous networks; LTE relaying; RF compressive sampling; spectrum sensing; cognitive radio; beamforming; and direction finding.

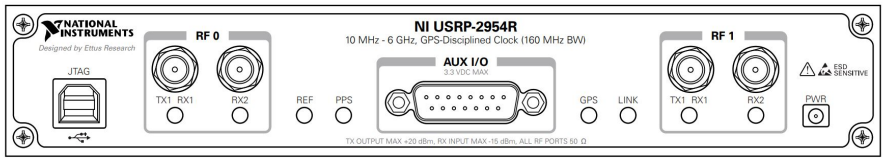


Figure 4.2: USRP-2954 device front panel.

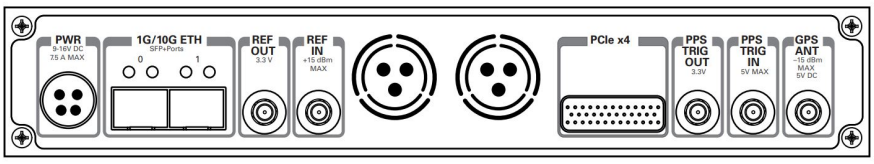


Figure 4.3: USRP-2954 device back panel.

The USRP-2954 has 2 channels (RF0 and RF1) each with a transmitting and receiving port. Frequency of operation ranges from 10 MHz to 6 GHz with a maximum instantaneous real-time bandwidth of 160 MHz and with a maximum I/Q sample rate of 200 MS/s. It is equipped with a GPS-disciplined 10 MHz Oven-Controlled Crystal Oscillator (OCXO) reference clock. The GPS disciplining delivers improved frequency accuracy and synchronization capabilities [21].

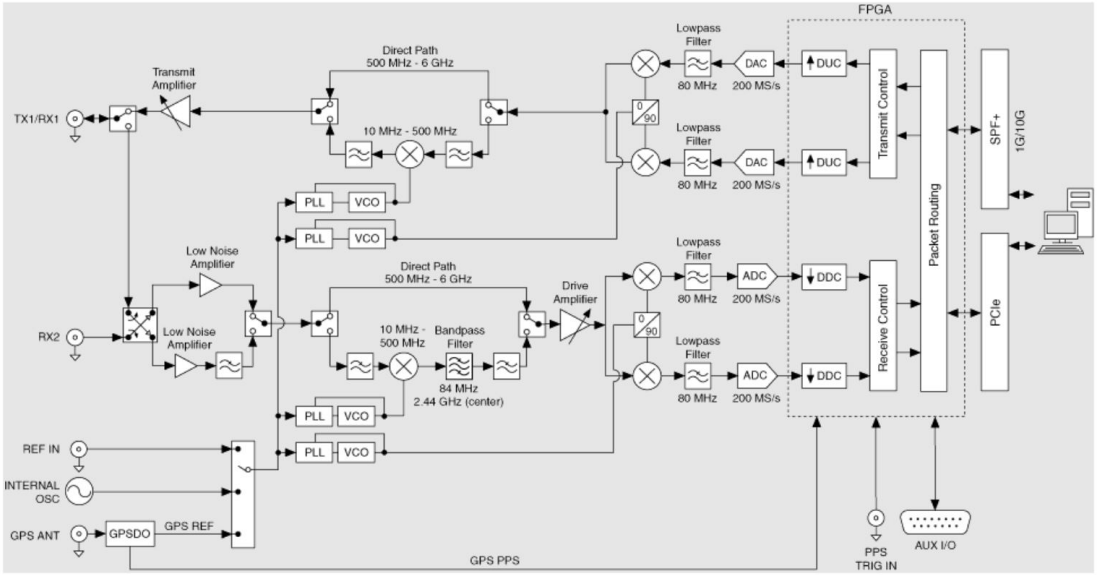


Figure 4.4: USRP-2954 block diagram.

4.1.2 Clock Distribution Device: CDA-2990

The OctoClock-G CDA-2990 is an affordable, high-accuracy timing reference and distribution system. This is a useful accessory for users that would like to build multi-channel systems that are synchronized to a common timing source. For example, the OctoClock-G CDA-2990 can be used to synchronize a system of USRP N210s for coherent operation. This can enable phased array applications such as beamforming, super-resolution direction-finding, diversity combining, or MIMO transceiver design.

The OctoClock-G CDA-2990 distributes 10 MHz and 1 PPS signals generated from an internal GPS-disciplined, oven-controlled oscillator (GPSDO), or an external source. The user can switch between these sources with a front-panel switch, and there is an automatic switch-over capability in case of failure or source disconnect [22].

Figure 4.5: OctoClock-G CDA-2990.

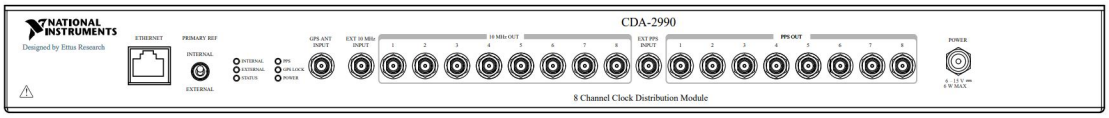


Figure 4.6: OctoClock-G CDA-2990 front panel.

4.1.3 Cabled Switch Device : CPS-8910

The CPS-8910 is designed for large MIMO expansion configurations and system control on the PXI platform or software defined radio devices. The CPS-8910 provides two PCI Express upstream ports and eight downstream ports for seamless system expansion. Downstream ports can be connected to external devices, such as a SDR reconfigurable device, to create large multichannel MIMO systems.

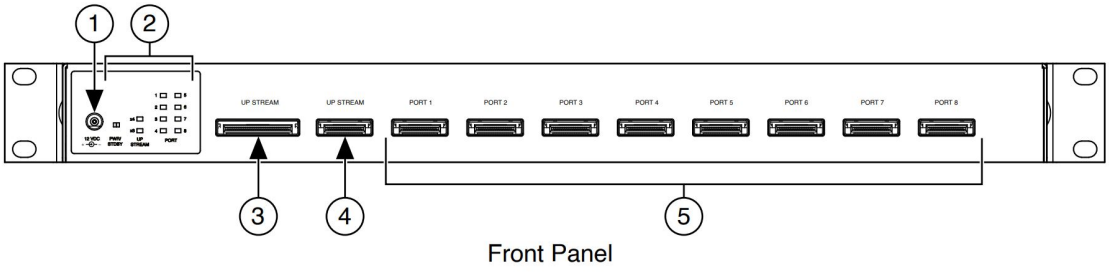


Figure 4.7: CPS-8910 front panel.

1: 12V Power Supply Input
2: LED Indicators
3: x8 Gen 2 Upstream Port
4: x4 Gen 1 Upstream Port
5: x4 Gen 1 Downstream Ports

Multiple CPS-8910 switch boxes can be connected to a single PXI Express chassis to create massive MIMO systems with a Software Defined Radio Reconfigurable Device. The large data throughput capacity makes the CPS-8910 an ideal data aggregator for massive MIMO systems. CPS-8910 can be used with copper or fiber-optic cables [23].

4.2 Software: LabVIEW Communication System Design Suite

Graphical programming stands out to be more interactive and easier in error handling and code bugs over text-based programming. It also provides better ability to design algorithms using Visual Blocks and data and control flow connections helping non-coders to be able implement algorithms. In other words, Graphical Programming Technique is a technique where visual block connections are used to code instead of text.

4.2.1 Introduction to Labview programming

LabVIEW is one of the first implementations of graphical programming; it continues to be the dominant graphical programming implementation. It provides a powerful and integrated environment for the development of various instrumental applications. An efficient LabVIEW application is designed without unnecessary operations, with minimal occupation including code, data, block diagram, front panel, and GUI updates. It eliminates human errors in data collection and process operations. It reduces data transcription errors and more reliable data available makes better quality control of products and new discoveries. LabVIEW programs are also called Virtual Instruments (VIs), because their appearance and operation imitate physical instruments. It contains a comprehensive set of VIs and functions for acquiring, analyzing, displaying, and storing data, as well as tools to help troubleshooting codes. LabVIEW provides the tools required for most applications and is also an open development environment [24].

The software platform we have chosen to program our SDRs is NI's LabVIEW. Despite the flexibility offered by SDR hardware for rapid prototyping, today's software tools

impede innovation by imposing a disjointed and difficult path from concept to real-world signals. The LabVIEW Communications System Design Suite (LV-CSDS) remedies this by offering a design environment featuring tight hardware integration with NI SDR systems to help rapidly prototype communications systems and outpace the competition.

LV-CSDS offers a single design environment to program processors and FPGAs for NI software defined radio hardware that includes NI USRP, FlexRIO, and selected Ettus Research branded USRP. Throughout our project work, inside the LV-CSDS, the programming environment is divided into 2 parts: a HOST side and an FPGA where each sub-environment has its own functionalities assigned to as what will be introduced in the following [25].

4.2.2 Host Programming

HOST programming environment refers to where control and some data processing functions are embedded. Those functions are meant to compose the control PC role in managing the USRPs by initialization, data feeding, triggering and synchronization and other control tasks over the USRPs.

4.2.3 FPGA Programming

FPGA programming environment refers to where codes to be embedded for execution in the USRP devices are found. This allows us to utilize the high speed of the FPGA for heavy computational data processing especially that found in OFDM modulators and demodulators. Those codes are loaded from the programming environment to the FPGA board by means of a bitfile specifying the configuration of the programmable gates.

Bitfile Generation

Several sample FPGA codes controlling the functioning of the USRPs are already present in the USRP FPGA programming environment by NI. Usually, the signal processing is all implemented at the host side and only time samples are loaded to the USRP for analog transmission thus not touching FPGA side codes. In our work this is different, as mentioned, we will be exploiting the high computational power of FPGA to manage our signal generation. Hence, we need to upgrade the way the “Programmable gates arrays” are configured to execute different tasks depending on our demand. Inside the FPGA

programming environment, FPGA codes are updated based on our demand and this will be explained more in the sections of TX and RX. After codes are ready, a bitfile is generated from the designed codes where this bitfile by then has the new configuration the FPGA should hold.

After upgrading the FPGA codes as desired and then generating the corresponding bitfile, it will be time to load this bitfile to the USRPs to configure their FPGAs in the new design. This is done through "FPGA reference nodes" which are assigned the bitfiles generated. Those nodes are found in the HOST code VI responsible for USRPs initialization blocks thus initializing the USRP with new configuration loaded via reference nodes.

4.3 Synchronizing Multiple USRPs

Having several transmission and reception node, it is critical that those nodes are well synchronized over frequency and time. For this sake, the common clock distribution device CDA-2990 described is employed. Figure 4.8 shows the connection between the USRPs back panel and the CDA-2990.

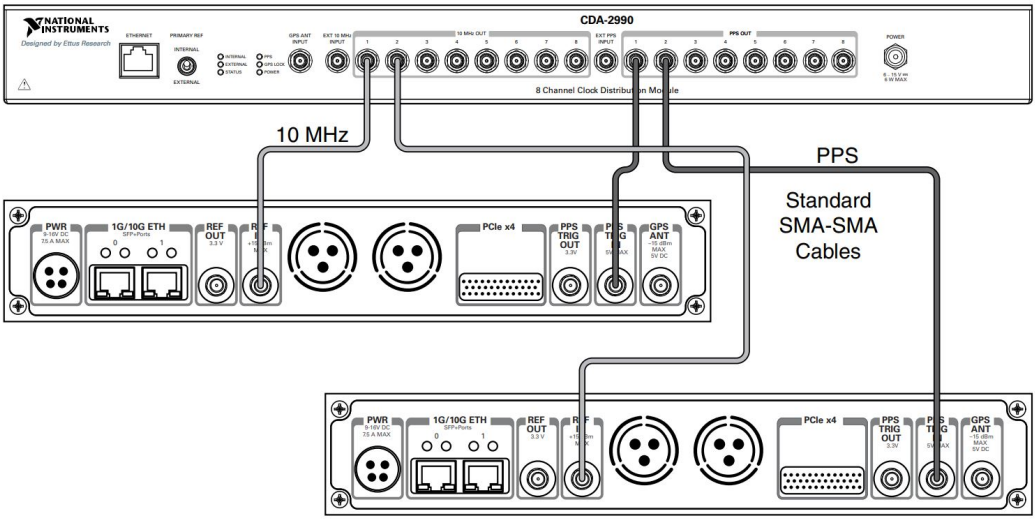


Figure 4.8: Connection between the common clock CDA-2990 and the USRPs for synchronization.

4.3.1 Clock synchronization

A 10 MHz reference clock signal is generated internally by the CDA-2990 and output from the 10 MHz output ports to the REF IN ports in the USRPs. This serve having 10 MHz reference to provide a single frequency reference for all devices; hence they are frequency synchronized and able to generate the same carrier frequencies used in the transmission scheme.

4.3.2 Time synchronization

The pulse per second PPS signal generated internally in the CDA-2990 feeds all the USRPs by connecting the PPS OUT ports form the CDA-2990 to the PPS IN ports in the back panel of the USRPs as shown in Figure 4.8. The purpose of the PPS signal is to synchronously latch a time into the device. All the devices share the same PPS source and hence they are all triggered at the same time by the HOST VIs responsible for the initiation of transmission and reception phases.

4.4 Programming a Single Transmitter Channel

The programming scheme of the baseband system stages is distributed over different programming environments (HOST and FPGA) as introduced earlier. Focusing on the TXs part, Figure 4.9 shows the road map of the TX code in its early stages which is implemented in the host environment.

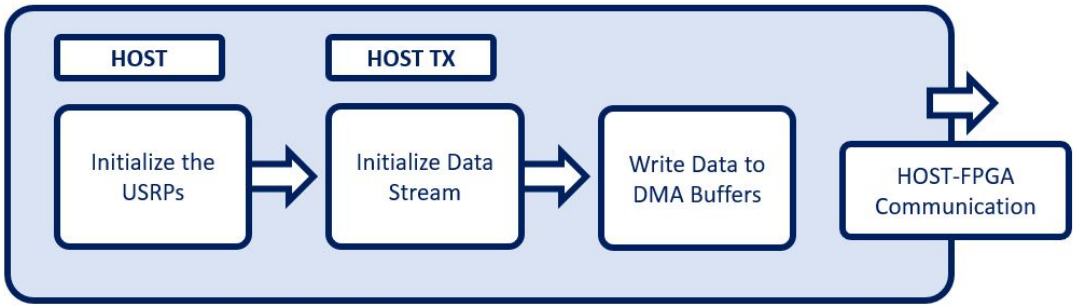


Figure 4.9: Block diagram of the HOST TX code for single channel.

4.4.1 Initialization of USRPs and Bit Streams

USRPs Initialization

The first step corresponds to starting up the USRPs with the desired configuration and parameters. This step is exclusively in the HOST environment and is common for both TX and RX. Having the devices connected to the HOST PC using CPS-8910, every device connected is detected through the LV-CSDS panel and could be addressed for programming. The devices are initialized using "Open and Configure" VI which receives the unique name or address of the USRP to initialize and pass desired parameters which are passed through user controlled panel shown in Figure 4.10.

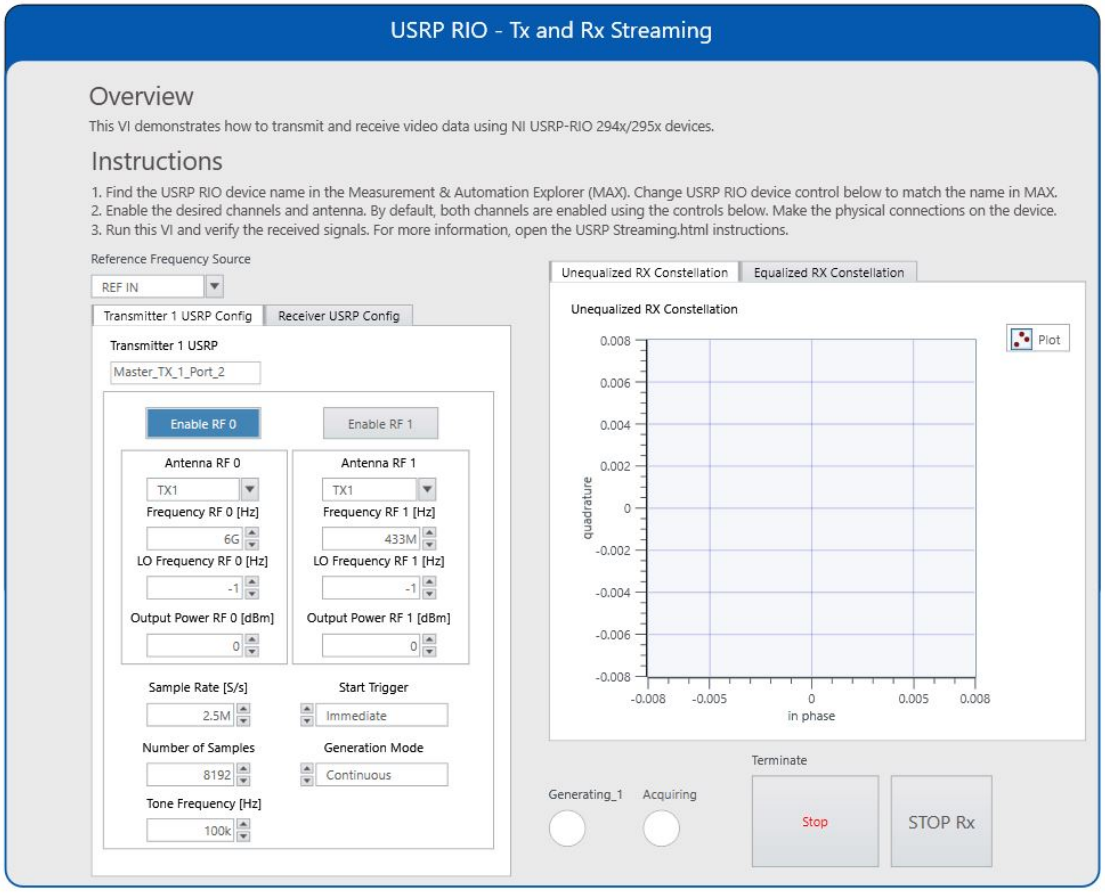


Figure 4.10: User to the "Open and Configure" code.

"Open and Configure" VI has in its core program other sub-VIs which receive bitfile referencing mentioned in section thus getting the USRPs initialized with desired configuration depending on the bitfile referenced.

HOST: Bit Stream Initialization

The consecutive piece of code corresponds to the creation of data frames. This is carried out through a random bit stream generator VI Figure 4.11. It creates arrays of unsigned 8-bits elements (bytes) and forwards them to the next stage of the TX HOST code.

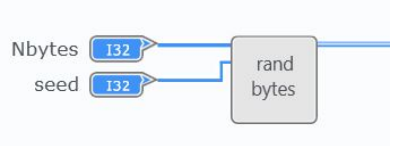


Figure 4.11: Random bit stream generator.

4.4.2 HOST-USRP Communication: HOST-to-Target FIFO

HOST: Write to Direct Access Memory (DMA)

The bit arrays created are forwarded inside the TX code reaching at its final phase the HOST-USRPs communication point. Using a "Write DMA FIFO" block, data arrays are written to a HOST-to-TARGET First Input First Output (FIFO) buffer accessible by the FPGA module to receive data frames from the HOST for OFDM processing. The "Write DMA FIFO" block shown in Figure 4.12 receives also a reference node attributed to the bitfile configuring the FPGA for proper addressing of resources and ports allocated on the FPGA. The FIFO used here is named "Tx Stream 0" with reference to the channel RF0 of the USRPs being enabled in Figure 4.10.

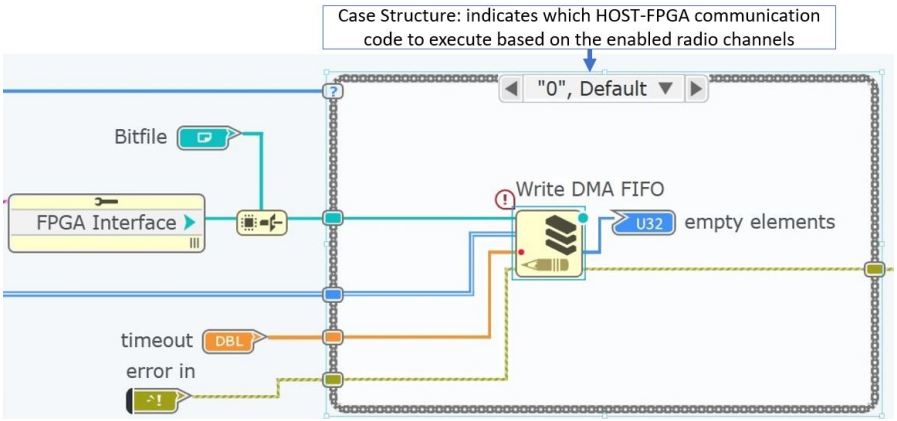


Figure 4.12: HOST to USRP data transfer using the WRITE DMA FIFO block.

FPGA: Read from HOST-to-TARGET FIFO

Figure 4.13 shows how the FIFO buffer "Tx Stream 0", which has been loaded with data at the HOST side, is being connected to a "READ FIFO" block which forwards data to a "WRITE FIFO" block inputting data to the "OFDM TX" block responsible for OFDM processing.

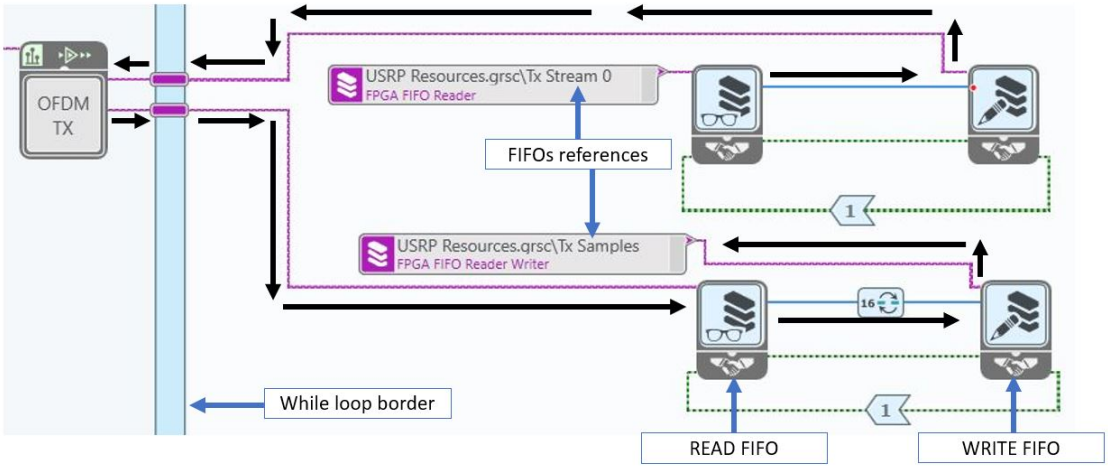


Figure 4.13: FPGA code receiving data bits from HOST through "Tx Stream 0" FIFO .

4.4.3 FPGA: Digital Part: OFDM TX

Being fed with data bits, the "OFDM TX" block appearing in the left part of Figure 4.13 processes data through multiple stages exhibited in Figure 4.14.

QPSK Mapper Block

Bytes enter the Quadrature Phase Shift Keying (QPSK) mapper block where they are split in pairs of bits (Figure 4.16). Every pair is then loaded into a lookup table (LUT) returning the complex amplitudes (real and imaginary coordinates) of the constellation point corresponding to the two bits to be mapped. From the complex amplitudes, the complex symbol is generated and output for next stage.

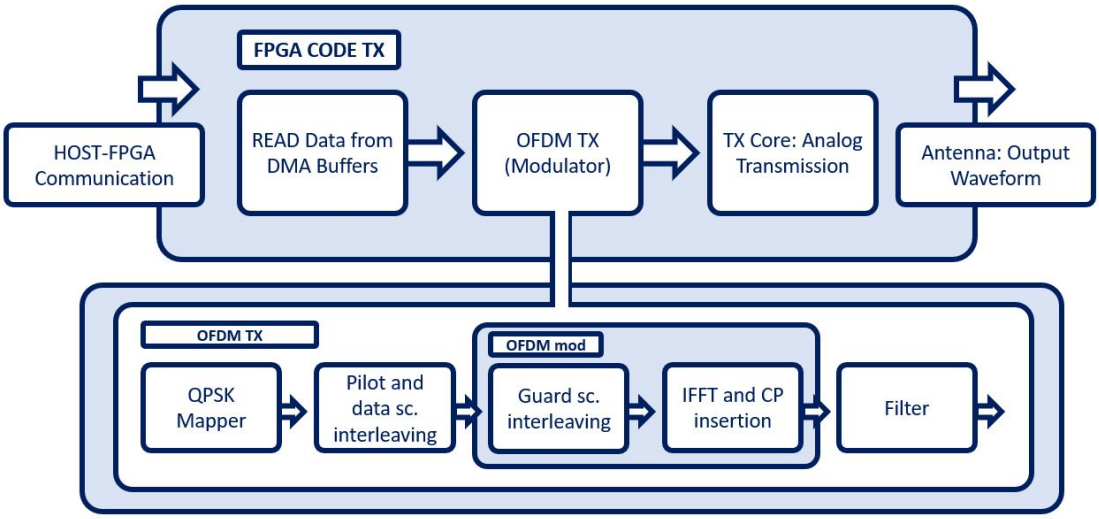


Figure 4.14: Block diagram of the "OFDM TX" code.

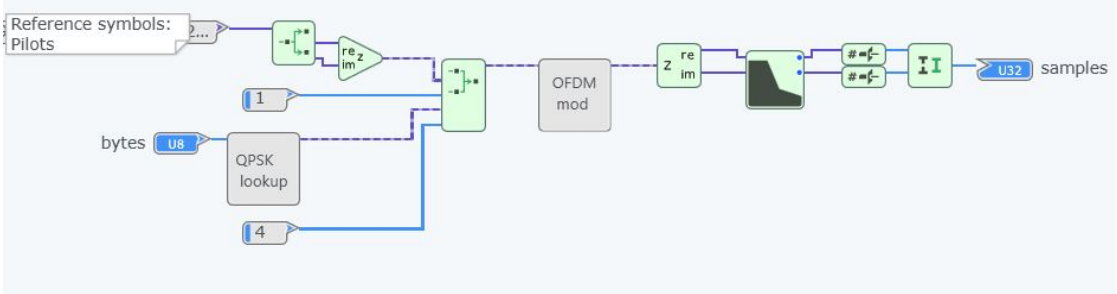


Figure 4.15: "OFDM TX" code.

Interleaver

After QPSK complex symbols are generated, which will correspond to data subcarriers, an interleaver block receives the stream of data subcarriers (generated QPSK symbols) as input and another pilot symbols source which are extracted from an external file source known at the RX side. The interleaver interleaves the pilot and data subcarriers in the

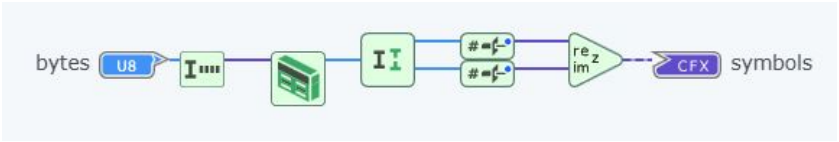


Figure 4.16: QPSK mapper code.

sequence pattern shown in Figure 4.17. it outputs a stream of interleaved pilots and data subcarriers. In each 5 symbols we have 1 pilot followed by 4 data.

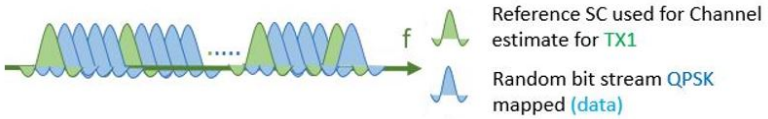


Figure 4.17: Interleaved sequence of pilot and data subcarriers.

A second stage of interleaving (Figure 4.19) follows inside the "OFDM mod" block shown in Figure 4.15 and whose block diagram is exhibited in the lower part of Figure 4.14. At this level, the interleaved pilot and data subcarriers are interleaved with guard subcarriers with the distribution shown in Figure 4.18 where the outputs of the interleavers are sets of 41 subcarriers with 42 guard subcarriers, and 470 pilot and data subcarriers composed of 94 pilots and 376 data subcarriers.

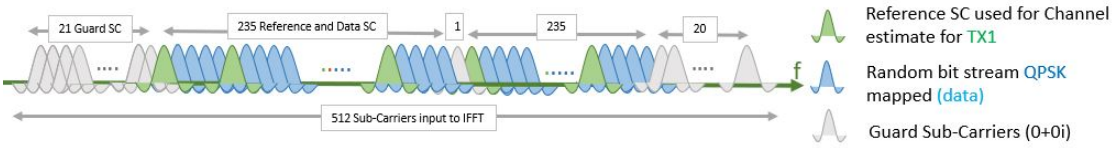


Figure 4.18: Single OFDM frame subcarriers composition.

IFFT and CP Insertion

The Inverse Fast Fourier Transform (IFFT) block receives the streams of 512 interleaved subcarriers corresponding to a single OFDM frame. This block performs 512 point IFFT and adds CP of length = 128 in the time domain ending up with 640 samples of a single OFDM frame ready to move into analog conversion and transmission.

Filter Block

Referring back to Figure 4.15, the samples output from "OFDM mod" (after IFFT and CP block) are fed to an Finite Impulse Response (FIR) filter block to improve spectral mask roll-off. After that, samples are output from the "OFDM TX" block.

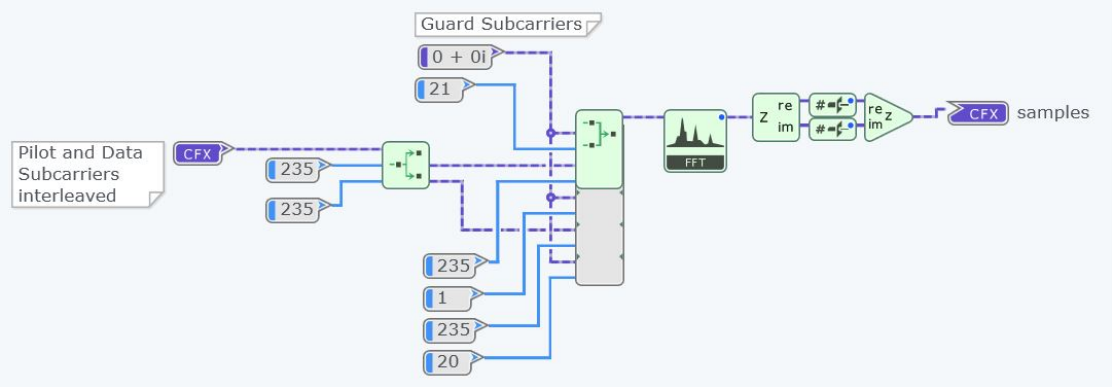


Figure 4.19: "OFDM mod" code.

4.4.4 FPGA: Analog part: Transmitter core

The discrete time samples output from the "OFDM TX" are then read and written to an FPGA local FIFO buffer called "TX samples" (see Figure 4.13) to be transferred to the FPGA TX core code.

TX Core Code

Navigating to the TX core code. A FIFO buffer reader inputs samples of a single OFDM frame from the local FIFO "TX samples". Those samples are loaded into a Digital Up-Converter (DUC) containing DSP blocks processing samples to be loaded for the analog Input Output (IO) writer block responsible for outputting the waveform from an enabled and selected channel output (RF0 TX output) according to the settings in Figure 4.10.

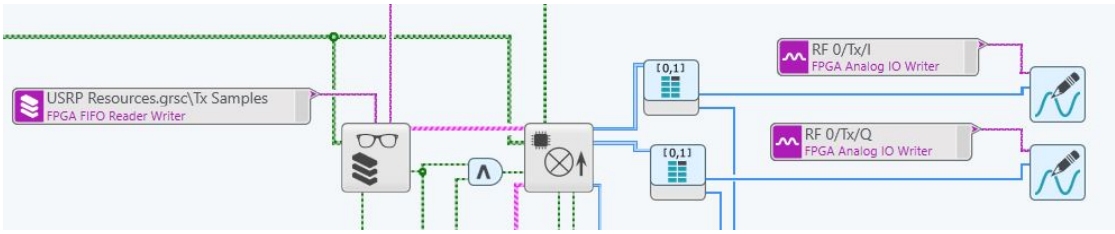


Figure 4.20: Portion of transmitter core code where samples are read and forwarded for processing to be prepared for output transmission.

4.5 Programming the Receiver Channel

The programming scheme of the receiver will be exhibited following the trace of the data frames from received samples then FPGA processing and finally reaching HOST processing.

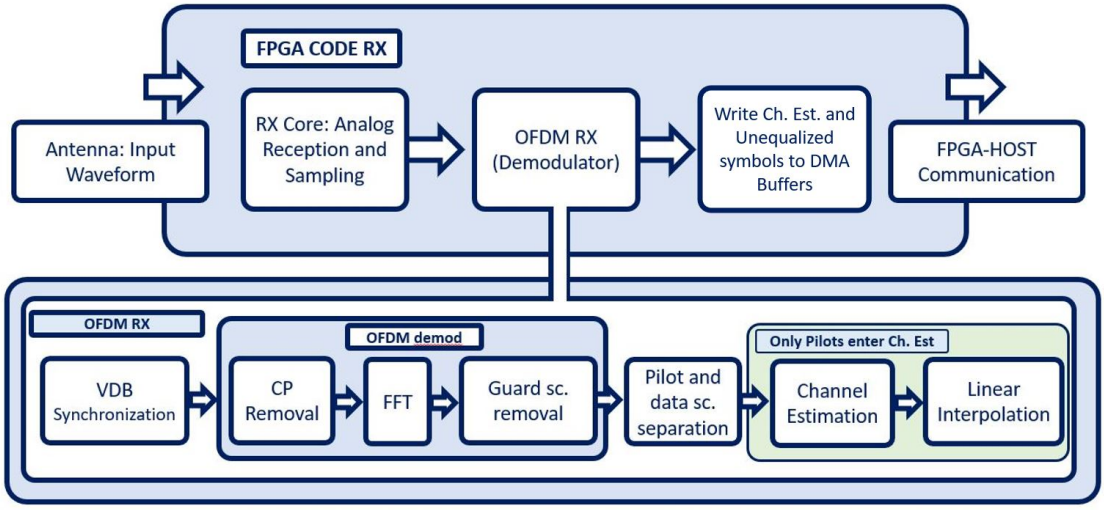


Figure 4.21: Block diagram of the FPGA RX code.

4.5.1 FPGA: Analog Part: Receiver Core

The analog RF signal arrives at the receiver antenna port and is sampled. After discretization in the DSP appearing in Figure 4.22, it passes into a Digital Down-Converter (DDC) before samples are written into "RX Samples" local FPGA FIFO buffer which forwards it for FPGA OFDM processing of the received signal samples.

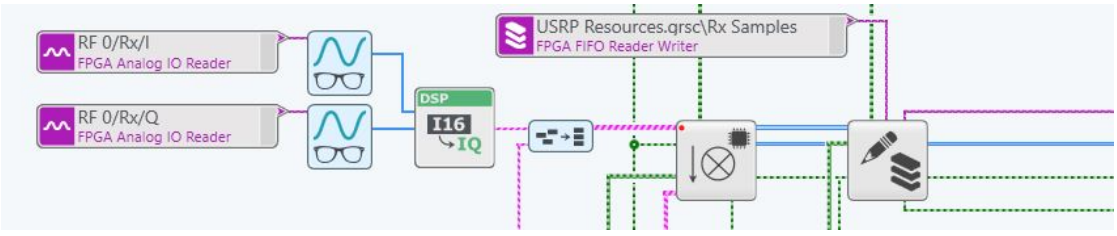


Figure 4.22: Portion of receiver core code where received symbol's samples are acquired and forwarded for OFDM processing.

4.5.2 FPGA: Digital Part: OFDM RX

After samples start filling the "RX samples" local FPGA FIFO buffer, an FPGA FIFO reader and writer blocks transfer the samples to be input into the "OFDM RX" block for OFDM processing. This can be seen in the piece of code expressed in the upper branch in Figure 4.25.

Frame Synchronization: Van De Beek (VDB) Algorithm

Having it critical to know the starting point of the OFDM frame, the time samples are input into a frame synchronizer block executing VDB algorithm [26] which determines maximum likelihood estimation of the symbol time and frequency offset by utilizing the correlation properties of the cyclic prefix.

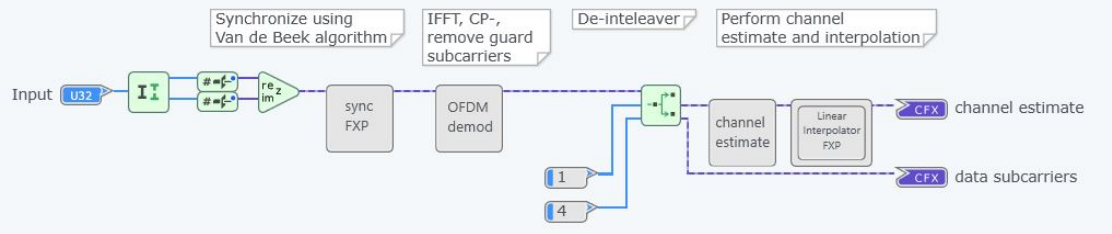


Figure 4.23: "OFDM RX" code.

CP removal

After frame synchronization and the determination of the start index of a single OFDM frame, 640 time samples are loaded into "OFDM demod" block which has its block diagram expressed in lower part of Figure 4.21. The 640 time samples input are processed removing the 128 cyclic prefix samples.

FFT Block

The 512 samples forwarded after CP removal correspond to a single OFDM frame. Those samples are input into Fast Fourier Transform (FFT) block which recovers the sequence of 512 frequency subcarriers having the distribution shown in Figure 4.18.

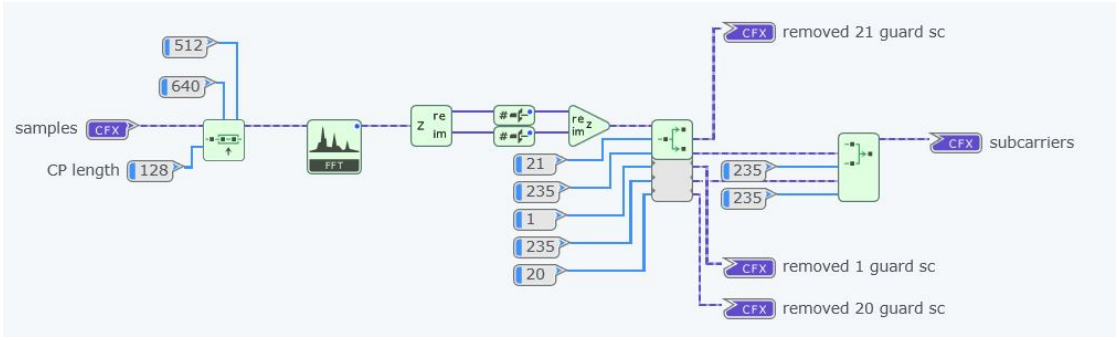


Figure 4.24: OFDM demod code.

Separator/ De-interleaver

After the sequence of interleaved guard, pilot, and data subcarriers is retrieved, it undergoes two stages of separation or de-interleaving. The first stage corresponds to removal of guard subcarriers. The output sequence composed is forwarded out of the "OFDM demod" block to enter the second stage of separation of subcarriers where pilot and data subcarriers are separated and each loaded to separate branch (see Figure 4.23). Data symbols are output into the "Rx UNEQ symbols" for the HOST processing. Pilot subcarriers are forwarded into channel estimation block.

Channel Estimation

Pilot symbols enter the channel estimation block contains an input node of the node referring to the external file containing the reference symbols used in the FPGA TX code. Channel estimates at the pilot subcarrier positions are recovered according to the Equation (4.1). This results in channel estimates over the 94 pilot subcarrier positions found in a single OFDM frame.

$$X_T.h = X_R \Rightarrow h = \overline{X_T}.X_R \tag{4.1}$$

$$X_T : Transmitted \quad Pilot \quad h : Channel \quad Estimate$$

$$X_R : Received \quad Pilot \quad \overline{X_T} : Transmitted \quad Pilot \quad Complex \quad Conjugate$$

Linear Interpolater

The channel estimates calculated in the previous stage enter the linear interpolater block. The interpolater calculates channel estimates across the rest of the band i.e., the channel estimates across the data subcarriers positions which is needed for equalization process at the RX HOST code (Figure 4.25).

4.5.3 USRP-HOST Communication: TARGET-to-HOST FIFO

FPGA: Write to TARGET-to-HOST FIFO

After the calculation of the channel estimates across all the data subcarriers through linear interpolation of the channel estimates at the pilot positions, the calculated 376 channel estimates and the 376 unequalized symbols are written into TARGET-to-HOST FIFO buffers "Rx Ch Estimates" and "Rx UNEQ symbols" respectively to be accessed by the receiver HOST code.

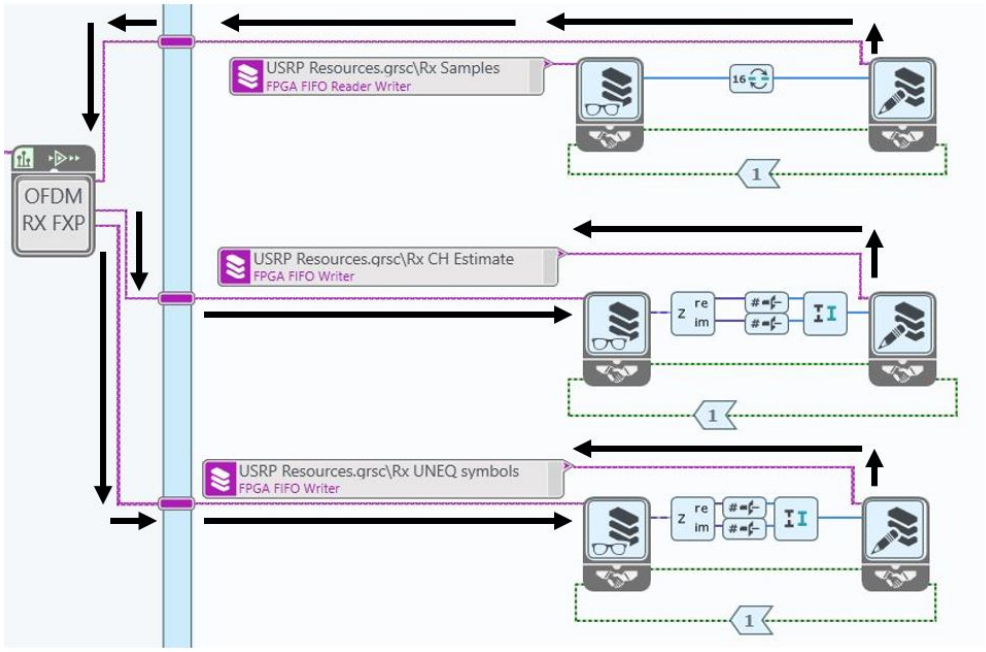


Figure 4.25: OFDM RX block inputs samples from "Rx Samples" and outputs processed data "Rx CH Estimates" and "RX UNEQ Symbols" for USRP-HOST communication.

HOST: Read DMA FIFO

At the HOST code side, channel estimates and unequalized symbols are read from their corresponding TARGET-to-HOST FIFO buffers through READ DMA FIFO blocks (Figure 4.26) and they are then queued into HOST local queues (Figure 4.27) and prepared for offline post-processing phase.

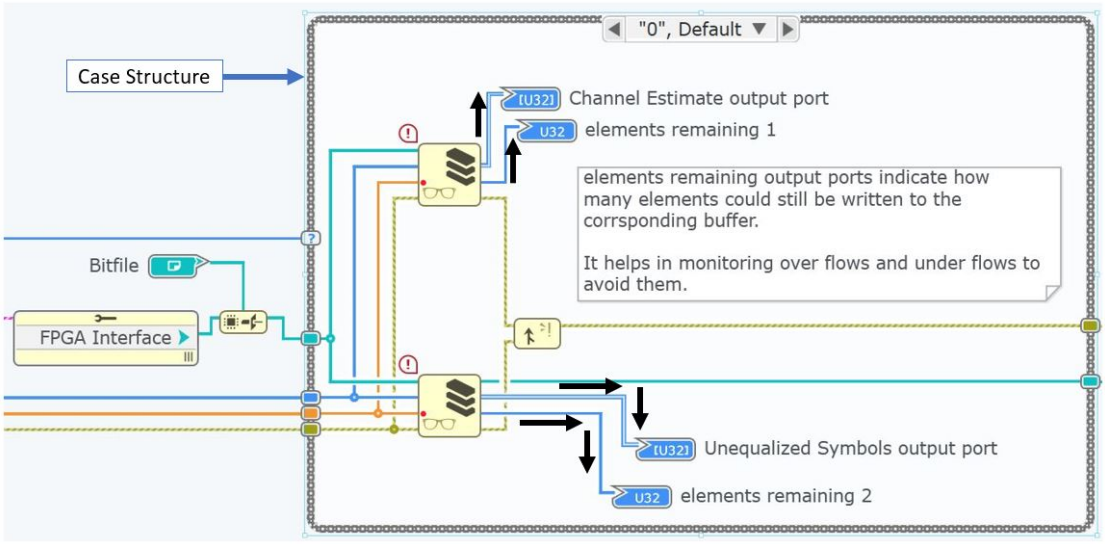


Figure 4.26: Read DMA FIFO blocks inputting received data from the corresponds FIFOs.

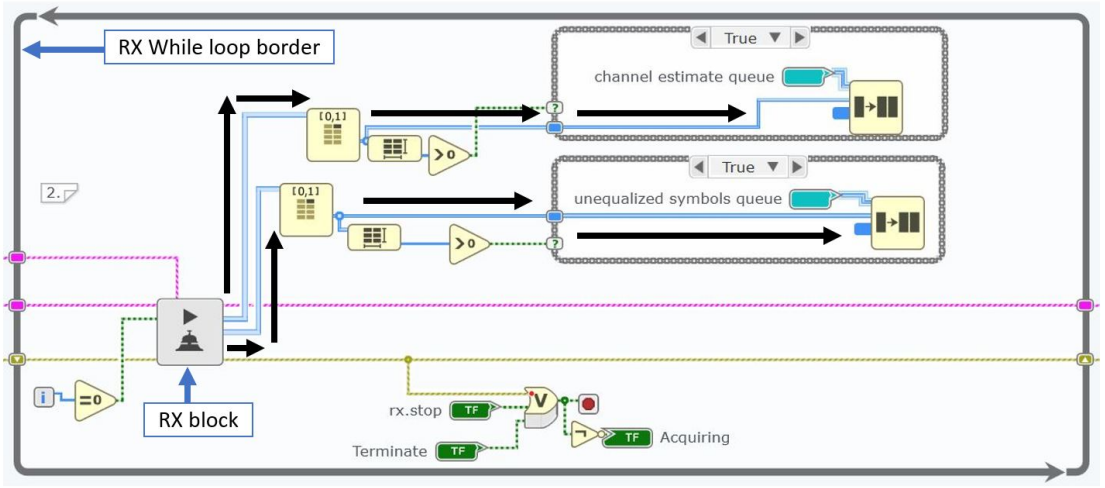


Figure 4.27: Queuing of channel estimates and unequalized symbols.

4.5.4 HOST: Offline post-processing of Received Symbols

Equalization

Queued channel estimates and unequalized data symbols are input into a Zero-Forcing equalizer [27] to equalize data symbols before demapping and recovery of data bit streams. Normalized complex conjugate of the channel estimates are multiplied by the complex representation of the unequalized symbols. The equalized output symbols queued in a local HOST will feed the demapper block in case the bit sequence is needed and also feed a constellation I/Q diagram graph probe which allows visualizing the equalized symbols constellation points to confirm whether we had successful reception and equalization or not.

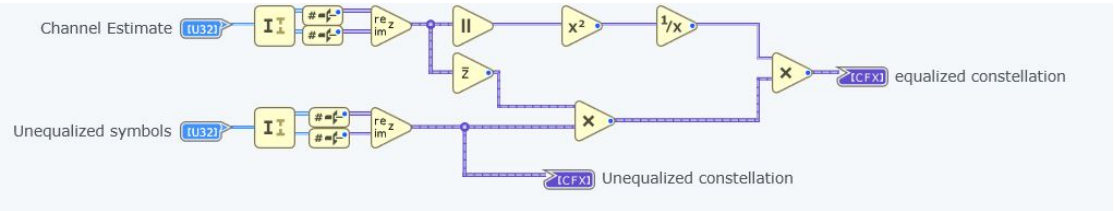


Figure 4.28: Equalizer.

QPSK Demapper

The queued equalized symbols output from the equalizer enter a QPSK demapping code block in which the complex amplitudes are recovered to check out in which I/Q quadrant the constellation point is located. This will then the 2 bits represented by the demapped symbol (Figure 4.29).

4.6 Single TX Single RX System Implementation Summary

The map of the implemented system to this point is summarized in Figure 4.30.

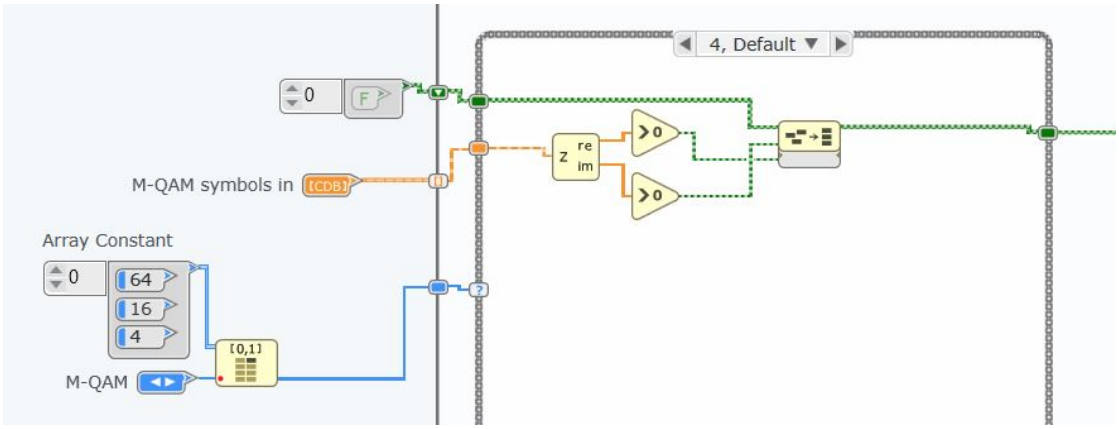


Figure 4.29: QPSK demapping.

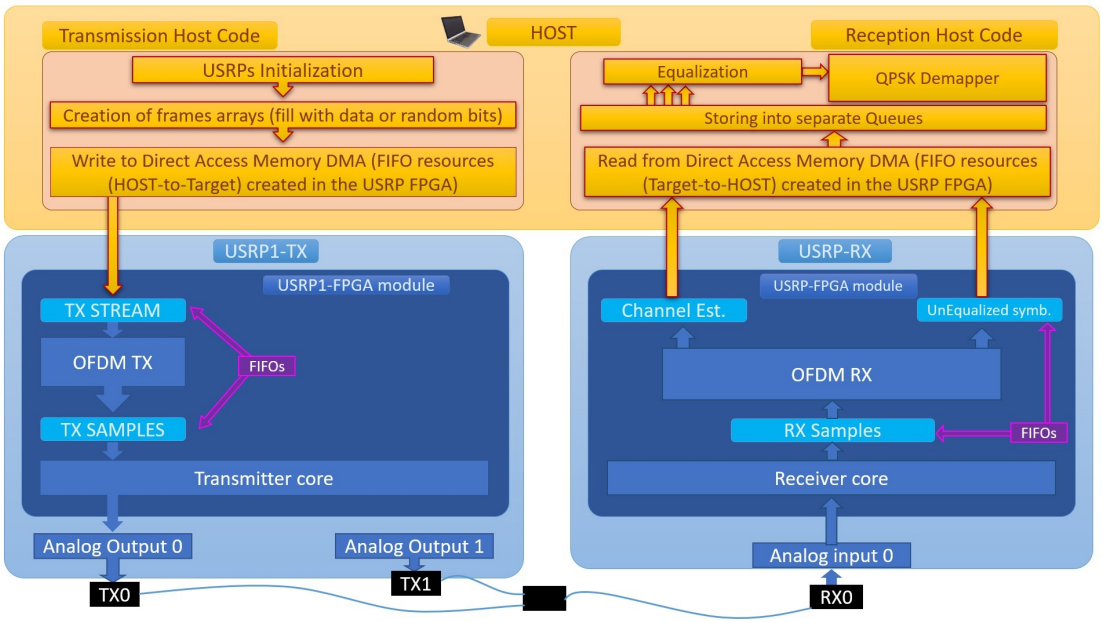


Figure 4.30: Block diagram of the implemented single TX single RX system.

4.7 Programming Two TX Channels on a single USRP

4.7.1 Additions to the HOST TX Code

To establish the proposed MISO system architecture expressed in Figure 3.1, the next step lie in extending the system into multiple transmitters. At the level of writing bit arrays to DMA for HOST-USRP communication, an additionally created HOST-to-TARGET

FIFO type buffer will be filled with bit arrays. The two HOST-to-TARGET FIFO buffers filled with bits will now serve separate branches of processing each corresponding to a single TX channel. HOST-to-TARGET FIFOs are named "U1 TX Stream 0" for serving RF0 channel of the first USRPs device and "U1 TX Stream 1" for serving RF1 channel of the first USRPs.

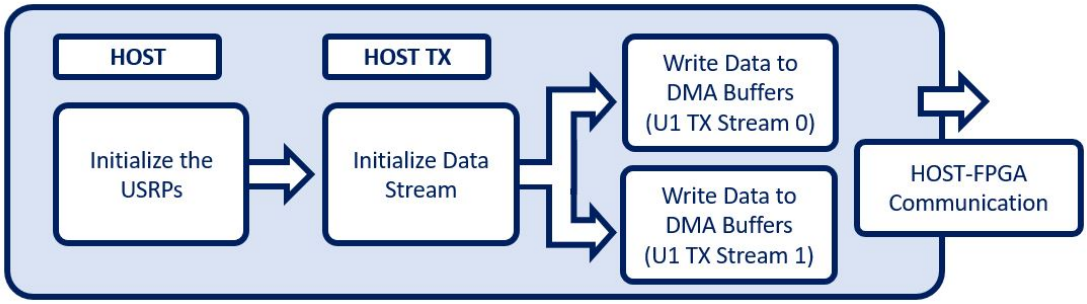


Figure 4.31: HOST TX code update for 2 TX channels system.

4.7.2 Additions to the FPGA TX Code

A duplicate of the previous FPGA code is created. Now two identical codes are updated to serve a different channel as follows:

Reading bits from HOST

Channel 0 code inputs data bits from "U1 TX Stream 0", passes them for processing into "U1 OFDM TX 0", and outputs OFDM samples into "U1 TX Samples 0".

Channel 1 code inputs data bits from "U1 TX Stream 1", passes them for processing into "U1 OFDM TX 1", and outputs OFDM samples into "U1 TX Samples 1".

OFDM TX code: Insertion of different pilots

"U1 OFDM TX 0" code interleaves, in a repeating set of five subcarriers, where a pilot is followed by a blank subcarrier reserving its place for other channel pilot and then followed by three data subcarriers (Figure 4.33).

"U1 OFDM TX 1" code interleaves, in a repeating set of five subcarriers, a blank subcarrier where this subcarrier position has been occupied by the first channel pilot followed by a pilot of the second channel and then by three data subcarriers (Figure 4.34).

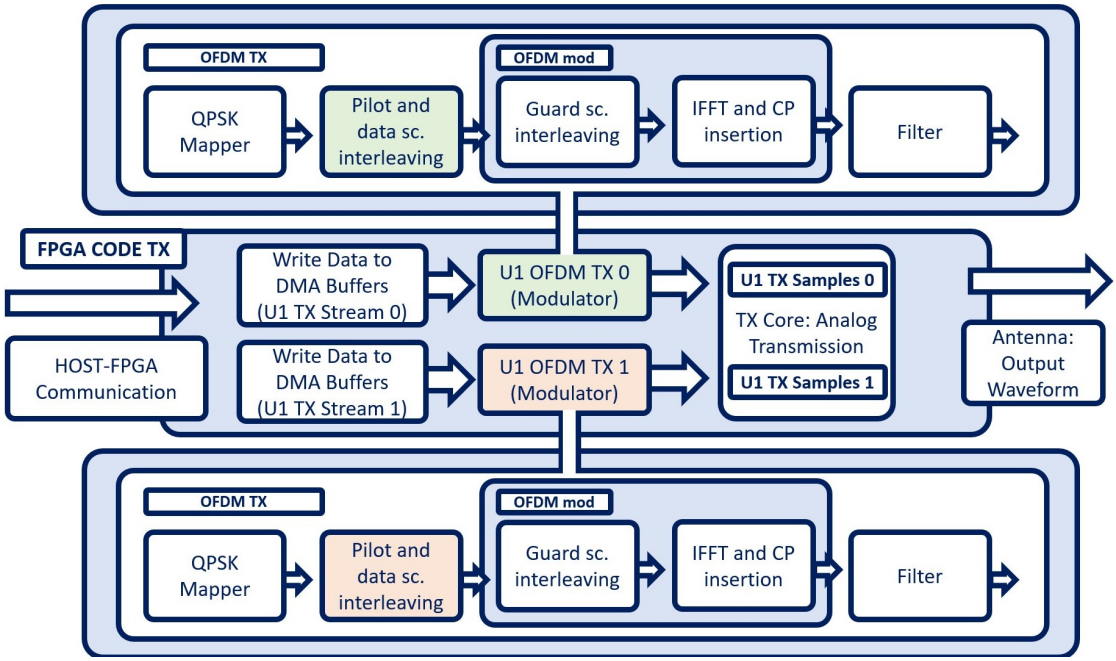


Figure 4.32: HOST TX code update for 2 TX channels system.

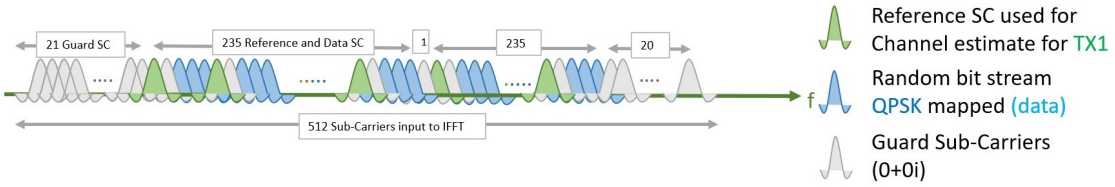


Figure 4.33: Subcarrier distribution of OFDM frame emitted from RF0 channel.

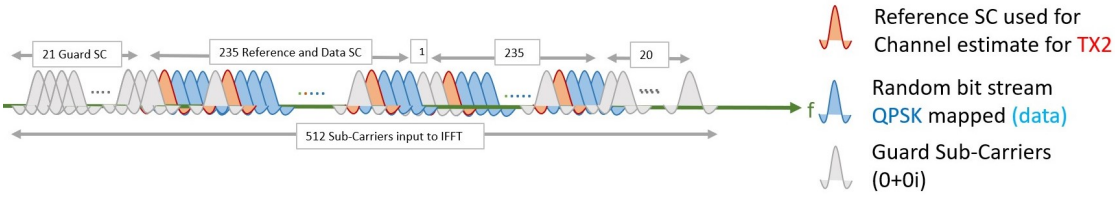


Figure 4.34: Subcarrier distribution of OFDM frame emitted from RF1 channel.

4.8 Programming Four TX Channels on a Two USRP

4.8.1 Further Additions to the HOST TX Code

Initialization

An additional block for USRPs initialization is added where the name of the newly connected USRPs device is passed and will be ready for configuration.

HOST TX code

A full duplicate of the previous TX code of Section 4.7 for 2 channels is created. The newly created HOST TX code is connected to the newly created initialization block. At the HOST-USRPs communication level, data bits are written onto two new separate HOST-to-Target FIFO buffers. The first FIFO buffer is called "U2 TX Stream 0" corresponding to channel RF0 of the second added TX USRPs device, and the second FIFO buffer is called "U2 TX Stream 0" corresponding to channel RF1 of the second added TX USRPs device.

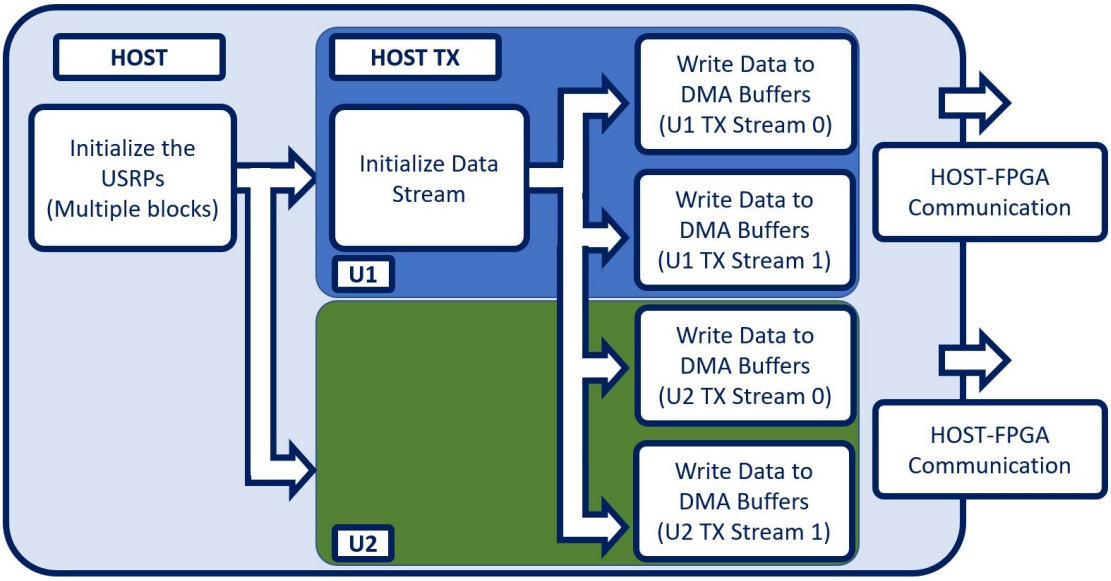


Figure 4.35: Updated HOST TX code block diagram to serve 4 TX channels.

4.8.2 Further Additions to the FPGA TX Code

Each of the two connected TX USRPs devices will have two codes triggered for execution summing up to a 4 transmission channels system. The FPGA codes for the newly added TX channels are an "updated" duplicate of the previous implementation of two TX channels in Figure 4.32. The four FPGA TX code will differ from each other through the following updates:

Reading bits from HOST

Considering USRPs-1:

Channel 0 code inputs data bits from "U1 TX Stream 0", passes them for processing into "U1 OFDM TX 0", and outputs OFDM samples into "U1 TX Samples 0".

Channel 1 code inputs data bits from "U1 TX Stream 1", passes them for processing into "U1 OFDM TX 1", and outputs OFDM samples into "U1 TX Samples 1".

Considering USRPs-2:

Channel 0 code inputs data bits from "U2 TX Stream 0", passes them for processing into "U1 OFDM TX 0", and outputs OFDM samples into "U2 TX Samples 0".

Channel 1 code inputs data bits from "U2 TX Stream 1", passes them for processing into "U1 OFDM TX 1", and outputs OFDM samples into "U2 TX Samples 1".

OFDM TX code: Insertion of different pilots

Considering USRPs-1:

"U1 OFDM TX 0" code interleaves, in a repeating set of five subcarriers, a pilot followed by 3 blank subcarriers reserving its place for other 3 channels pilots and then by a data subcarrier Figure 4.36).

"U1 OFDM TX 1" code interleaves, in a repeating set of five subcarriers, a blank subcarrier where this subcarrier position has been occupied by the first channel pilot followed by a pilot and then by 2 blank data subcarriers reserving its place for other 2 channels pilots and finally by a data subcarrier Figure 4.37).

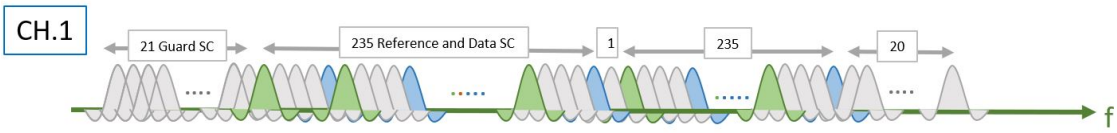


Figure 4.36: Subcarrier distribution of OFDM frame emitted from U1 RF0 channel.

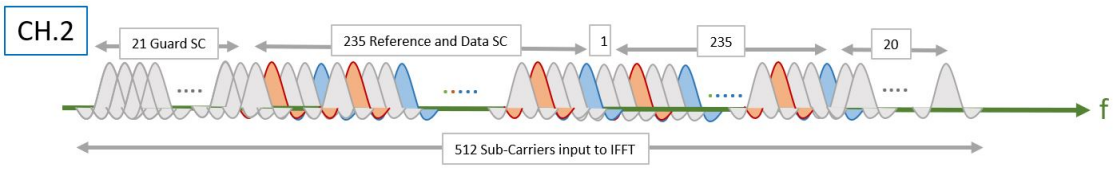


Figure 4.37: Subcarrier distribution of OFDM frame emitted from U1 RF1 channel.

Considering USRPs-2:

"U2 OFDM TX 0" code interleaves, in a repeating set of five subcarriers, 2 blank subcarriers where these subcarrier position has been occupied by the first 2 channels pilots followed by a pilot and then a blank subcarrier reserving its place for the fourth channel pilot and finally by a data subcarrier Figure 4.38).

"U2 OFDM TX 1" code interleaves, in a repeating set of five subcarriers, 3 blank subcarriers where these subcarrier position has been occupied by the first 3 channels pilots followed by a pilot and by a data subcarrier Figure 4.39).

The expected desired full spectrum we aim at for the combined signals from the four channel is shown in Figure 4.40.

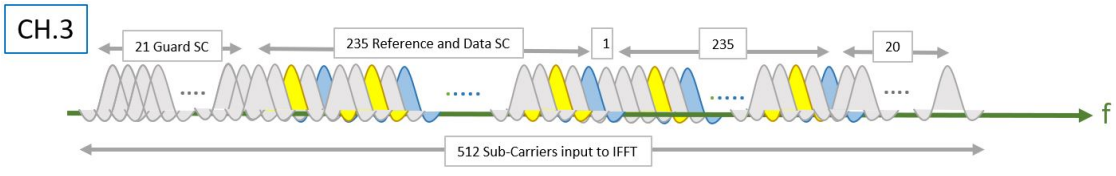


Figure 4.38: Subcarrier distribution of OFDM frame emitted from U2 RF0 channel.

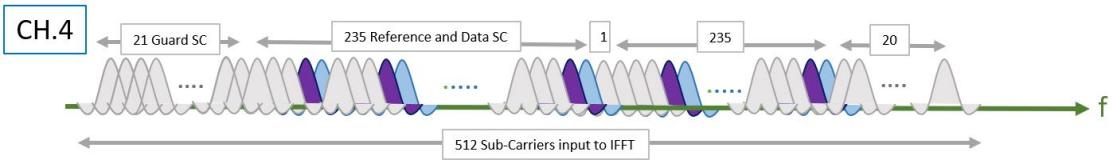


Figure 4.39: Subcarrier distribution of OFDM frame emitted from U2 RF1 channel.

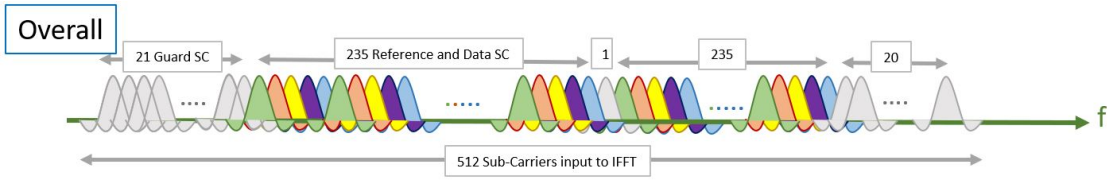


Figure 4.40: Subcarrier distribution of combined OFDM frames emitted from all channels.

4.9 Programming the Receiver

4.9.1 Additions to the FPGA RX code

OFDM RX code: New Pilot Separation Scheme

In the "OFDM RX" block, the interleaver block has to deal with subcarrier positions, for every set of 5 interleaved pilots and data symbols, as 4 different pilots (each corresponding to a channel) and a common data subcarrier. For this sake, the "RX OFDM" code has been updated as the block diagram in Figure 4.41.

Pilots are separated into separate branch where each pilot undergoes its channel estimate and interpolation processes to output the corresponding channel estimates.

OFDM RX code: Write Symbols to the HOST RX code

Channel estimates and unequalized symbols are output from the upgraded OFDM RX code written into TARGET-to-HOST FIFO buffers for the HOST code to access it for any HOST or offline processing.

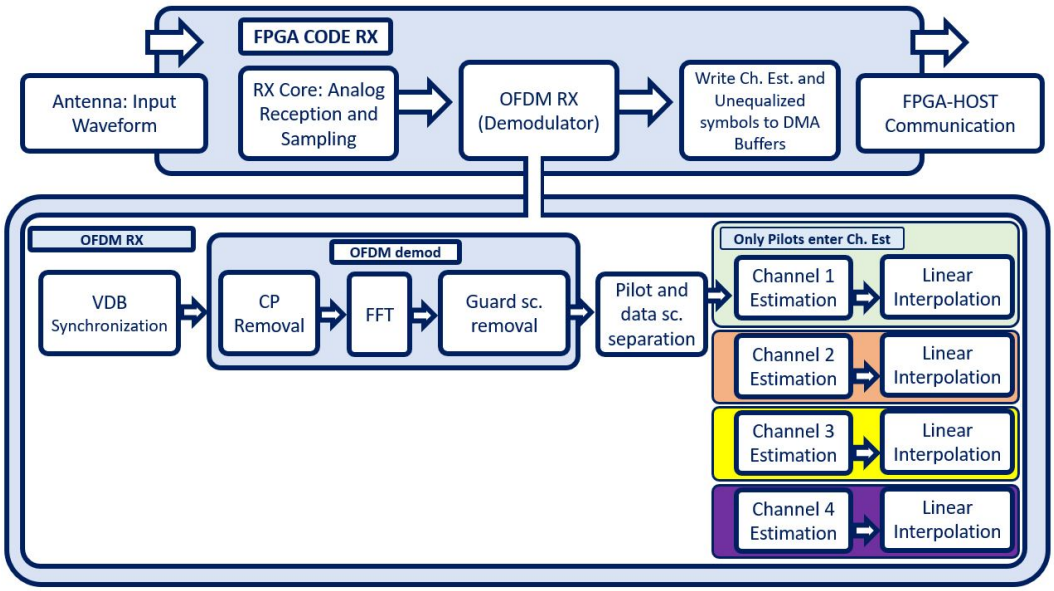


Figure 4.41: Updated "OFDM RX" block diagram.

4.9.2 Additions to the HOST RX code

Read Symbols from the FPGA RX code

Five separate READ DMA FIFO blocks will receive the channels' estimates and the unequalized symbols written into TARGET-to-HOST FIFO buffers at the FPGA RX code side.

Channel estimates are output from the HOST RX code and stored into HOST local queues for any future steps (e.g., calibration).

4.10 Multiple TX Single RX System Implementation Summary

The map of the implemented system to this point is summarized in Figure 4.42

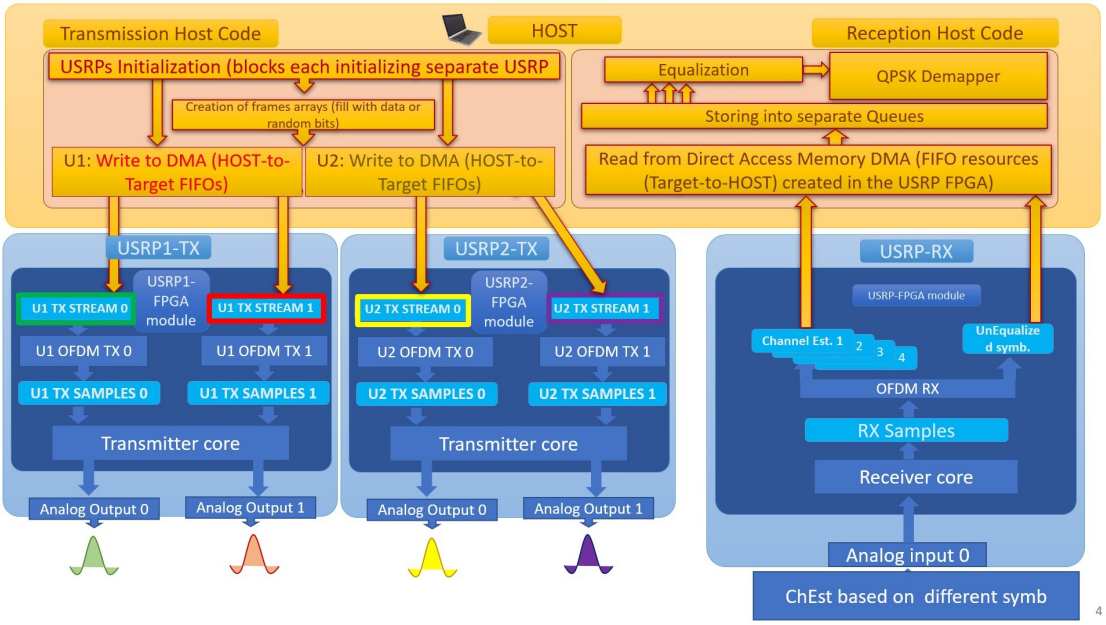


Figure 4.42: Block diagram of the multiple TX single RX implemented system.

4.11 Calibration

As a recall, radio signal undergoes amplitude fluctuation and phase rotation, which differ over different channels. One of the future steps related to the baseband system is implementing a conjugate beamforming scheme. The scheme which is introduced in Section 3.2.3 will lead to a constructive interference at the receiver. The scheme performs beamforming at base station of the MPAC OTA testbed.

4.11.1 HOST: Precoding Weights Generation

Channel estimates which are already queued after being received from the receiver FPGA code specify the channel response. Those estimates are used to generate the channel response conjugate which will act as the calibrating weights for the data subcarriers. The normalized weights are generated from the channel estimates according to Equation (4.2).

$$w = \frac{\overline{\hat{h}}}{|\hat{h}|} \tag{4.2}$$

$w : Weight \quad \hat{h} : Channel \quad Estimate \quad \overline{\hat{h}} : Channel \quad Estimate \quad Complex \quad Conjugate$

Weights are stored then in local HOST queues. Those weights' queues then transfer the weights to the the HOST TX code to the level of HOST-USRP communication. Weights are written to HOST-to-TARGET FIFO buffers to communicate the weights with FPGA code to apply to data subcarriers.

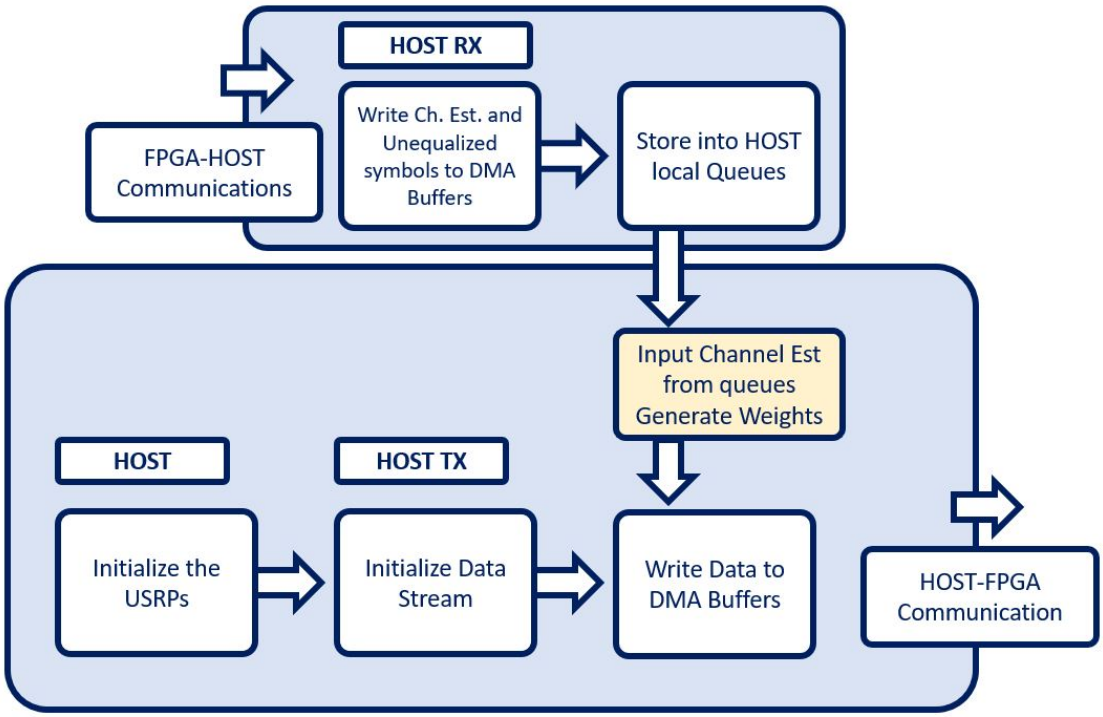


Figure 4.43: Weights are generated from queued Channel estimates and are fed to TX code.

4.11.2 FPGA: Calibrator Block

* At the level of the FPGA code, weights are read from the weights' HOST-to-TARGET FIFO and then input to the "OFDM TX" code. Inside the "OFDM TX" code, a calibrator block is introduced where the input weights are fed to this block. The calibrator block receives as a second input the QPSK symbols output from the QPSK mapper as complex symbols.

Inside the calibrator block, the weights turned to complex symbols are split into polar coordinates in parallel to the QPSK symbols also where the radii are multiplied and the phases are added to output the polar coordinates of the calibrated (weighted) data symbols.

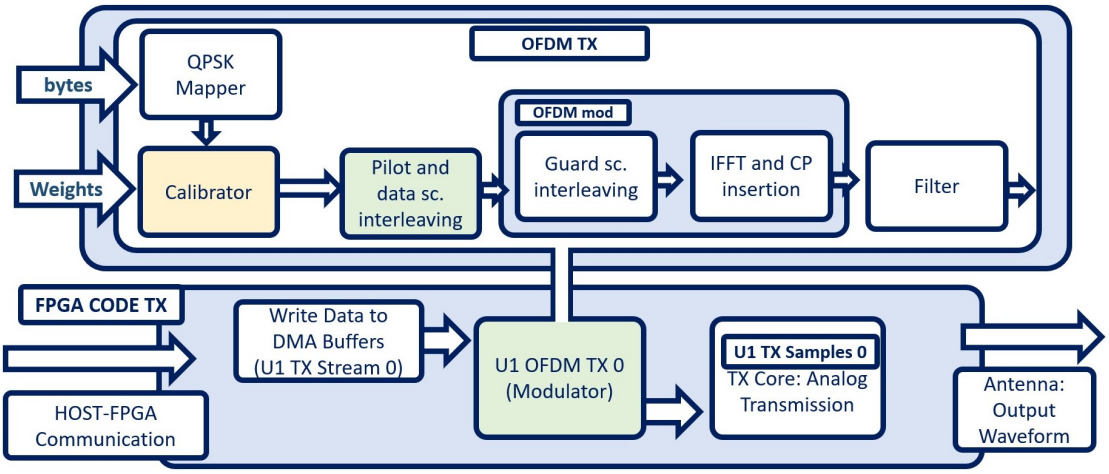


Figure 4.44: Calibrator block is inserted into the "OFDM TX" block code.

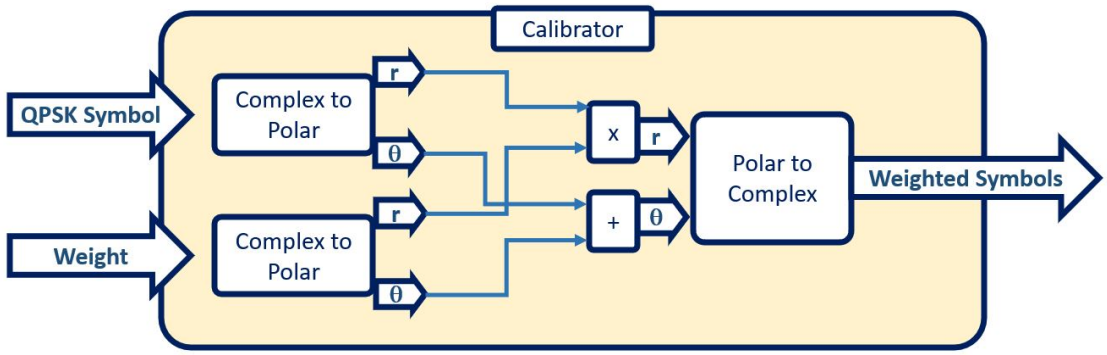


Figure 4.45: Block diagram of the Calibrator.

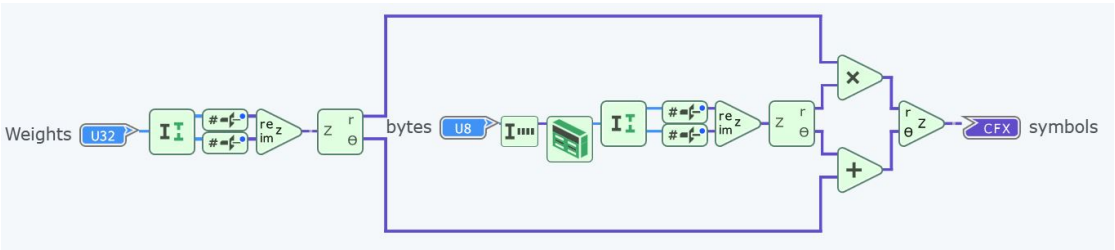


Figure 4.46: Calibrator code.

CHAPTER

5 Evaluation of the System

This chapter covers the evaluation of the implemented different transmission schemes by visualizing the results of the reception codes.

5.1 Results

5.1.1 RX Constellation of a Single Channel

The system implementation in sections 4.4 and 4.5 resulted in successful reception of the desired QPSK constellation. After equalization stage expressed in section 4.5.4.1, the equalized symbols were fed to an output display probe which gave the results shown in Figure 5.1.

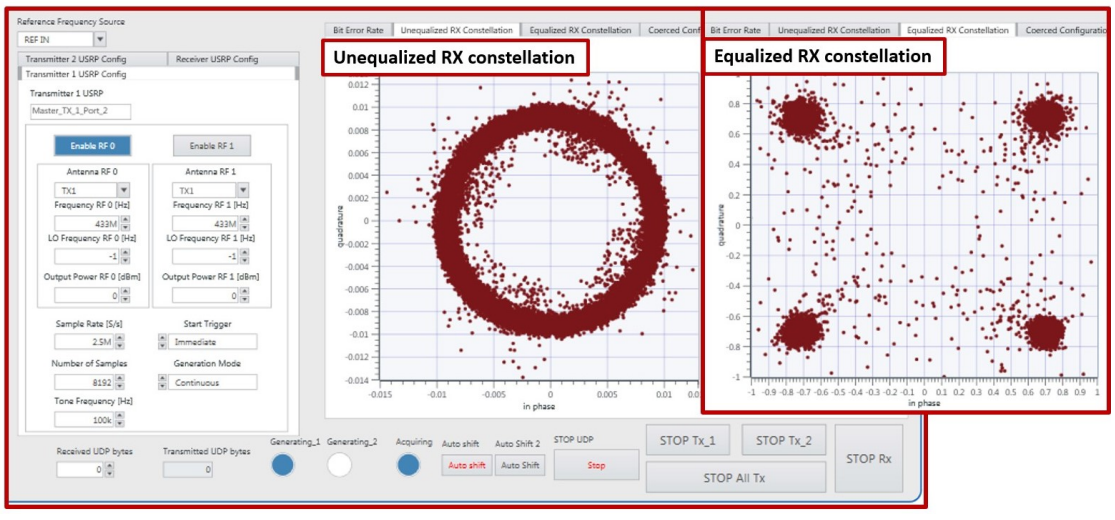


Figure 5.1: Received QPSK Symbols after equalization for Single-TX Single-RX system.

After extending the system to four TX channels each with unique pilot subcarriers, the channels were tested separately with the receiver code compatible for the reception from all the channels. This test gave the desired results emphasizing the successful implementation a 4 TX channels baseband system for the creation of the desired RF environment in the test zone. The results of testing each TX channel separately gave the results in Figure 5.2. We note that the clouds in the middle of the constellation correspond to applying equalization on blank subcarriers where pilots of other channels are sent. It could have been simply dropped through the de-interleaver block, but it was kept confirming the compatibility between the blocks.

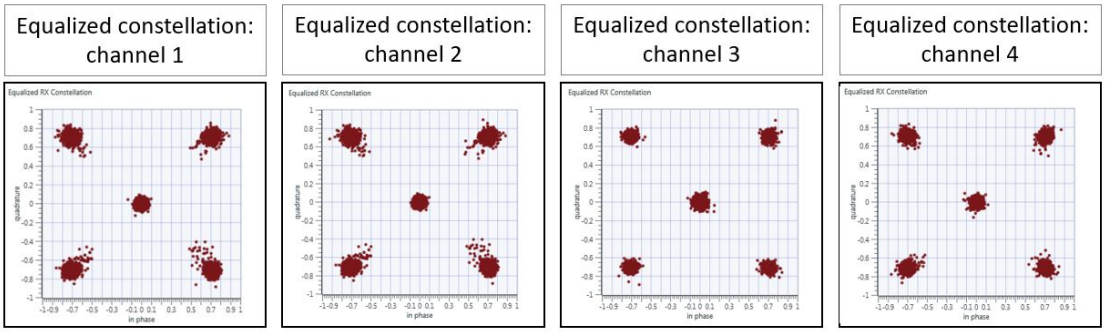


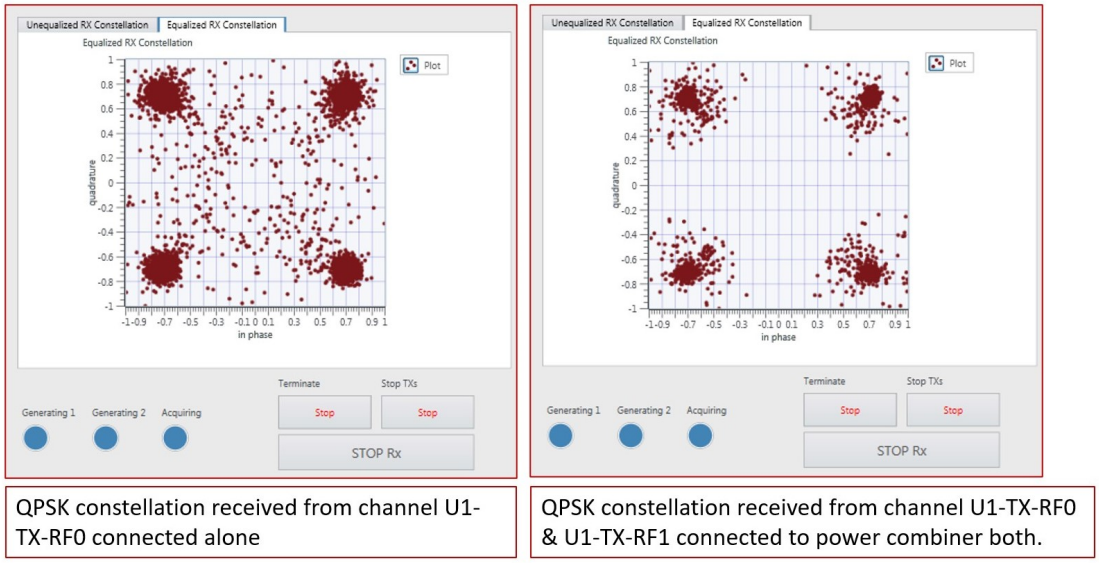
Figure 5.2: Received QPSK Symbols testing reception from different implemented channels.

In case of estimating all the channels in parallel when the channels are active, we speculate that the scheme implemented in Figure 4.41 functions as desired and the channel estimates of different channels are obtained successfully. This speculations would be confirmed in the future work of the calibration scheme being developed. Successfully obtained estimates of different channel will lead to the proper calibrating weights which lead to constructive interference at the receiver. This will result in a QPSK constellation diagram for symbols carried by the common data subcarriers between all the channels.

5.1.2 Manual Calibration of Two TX channels

At the level of implementing two TX channels from a single USRP device, after duplicating the first single channel code before updating the "OFDM TX" code, the two channels where being tested to check whether the establish links are functioning. Trying to test the two channels adopting same pilot position would cause corruption of channel estimates because of pilots' interference. However, if the two signals arrive constructively, a better SNR will be observed. This depends on the starting phase of each channel and the phase rotation through each channel. For this sake, using cabled connection with a power

combiner we utilized same length cables by several trials, both channels' signals arrive constructively. In the mentioned trial, both channels transmitting instantly and still we had a successful reception of the QPSK constellation as seen in Figure 5.3 below.



QPSK constellation received from channel U1-TX-RF0 connected alone

QPSK constellation received from channel U1-TX-RF0 & U1-TX-RF1 connected to power combiner both.

Figure 5.3: Received QPSK Symbols with two channels transmitting instantly showing constructive interference.

CHAPTER

6 Conclusion & Outlook

This chapter presents the work summary of this thesis, by which the target setup was implemented. In addition, an outlook is exhibited where some possible improvements and additional implementation ideas are covered.

6.1 Thesis Contributions

A system of four transmitter channels and a single receiver has been developed and implemented using software defined radios where the signals transmitted are realistic 5G signals. Bits are mapped as QPSK symbols sent over OFDM frames. Channel estimation has been carried out utilizing pilot symbols sent over specific subcarrier positions uniquely assigned for each channel. The developed system of transmitters contribute in the goal of creating an RF environment in the test zone inside the anechoic chamber where the main project aims at developing an MPAC OTA testbed.

6.2 Improvement and Future Works

After successfully implementing a real-time baseband system establishing 4 transmission channels, work will be focused on exploiting the successful channel estimation across different channels to establish conjugate beamforming scheme. The future work can be pointed to as follows:

- Implement and test a calibration scheme for a single TX single RX system and test the implemented scenario. This improvement has been with the implementation of the calibration scheme in section Section 4.11.

- Extend the calibration scheme to cover the four different TX channels instantly, hence we can say that a conjugate beamforming system is accomplished. Upon testing, the unequalized symbols shown will correspond to data subcarrier overlapping between channels, Results are expected to show nominal transmitted constellation points with a high SNR.

Fulfilling the above steps will conclude an improved baseband system with beamforming internally embedded and would then pave the way to move to MPAC OTA testing of the mobile phone antennas.

Acronyms

5G	Fifth Generation of mobile communication
BS	base station
BW	Bandwidth
CP	Cyclic Prefix
CP-OFDM	Cyclic Prefix Orthogonal Frequency-Division Multiplexing
DDC	Digital Down-Converter
DMA	Direct Access Memory
DSP	Digital Signal Processing
DUC	Digital Up-Converter
DUT	Device Under Test
DVB	Digital Video Broadcasting
EM	electromagnetic
EMC	electromagnetic compatibility
FDM	Frequency-Division Multiplexing
FFT	Fast Fourier Transform
FIFO	First Input First Output
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
FSPL	Free Space Path Loss
GPP	General Purpose Processor
IFFT	Inverse Fast Fourier Transform
IO	Input Output
ISI	Intersymbol Interference

LabVIEW	Laboratory Virtual Instrument Engineering Workbench
LUT	lookup table
LV-CSDS	LabVIEW Communications System Design Suite
MIMO	Multi-Input Multi-Output
MISO	Multi Input Single Output
MPAC	Multi-Probe Anechoic Chamber
MRC	Maximum Ratio Combining
NI	National Instruments
NR	New Radio
OCXO	Oven-Controlled Crystal Oscillator
OFDM	Orthogonal Frequency-Division Multiplexing
OFDMA	Orthogonal Frequency-Division Multiple Access
OTA	Over-The-Air
PAS	Power Angular Spectrum
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RC	Reverberation Chamber
RF	Radio Frequency
RX	Receiver
SDR	Software- Define Radio
SIMO	Single Input Multi Output
SNR	Signal to Noise Ratio
Soc	System on Chip
TX	Transmitter
UE	User Equipment
USRP	Universal Software Radio Peripheral
VDB	Van De Beek
VI	Virtual Instrument

WiMAX Worldwide Interoperability for Microwave Access

Glossary

3GPP	The 3rd Generation Partnership Project (3GPP) is an umbrella term for a number of standards organizations which develop protocols for mobile telecommunications.
anechoic chamber	An anechoic (which means non-reflective, non-echoing, or echo-free) chamber is a room that is designed to completely absorb reflections of sound or electromagnetic waves.
CN	complex normal distributions, denoted, characterizes complex random variables whose real and imaginary parts are jointly normal.
fading emulator	A fading emulator or radio channel emulator is a tool used to reproduce the actual signal propagation channel environment in a lab for testing in wireless communications.
Faraday cage	is an enclosure usually earthed metallic screen used to exclude electrostatic and electromagnetic influences..
LTE	Long-Term Evolution (LTE) is a standard for wireless broadband communication for mobile devices and data terminals.
mMTC	Massive Machine-Type Communications: is a new service category of 5G that can support extremely high connection density of online devices.

PCI	Peripheral Component Interconnect (PCI) is a local computer bus for attaching hardware devices in a computer and is part of the PCI Local Bus standard.
PXI	PXI is an abbreviation for PCI eXtensions for Instrumentation. PXI is based on the PCI architecture, which is a commonly-used standard in personal computers, and uses the industrial CompactPCI (cPCI) connector.
URLLC	Ultra-Reliable Low-Latency Communication: is a new service category of 5G that makes it possible to support use cases that require very high reliability and extremely low latency.
USRP RIO	"USRP RIO" is a term that is used to describe USRP Software Defined Radio Devices that contain an FPGA, such as the USRP-294x and USRP-295x.

CHAPTER

6 Bibliography

[1] Theodore S Rappaport, Yunchou Xing, George R MacCartney, Andreas F Molisch, Evangelos Mellios, and Jianhua Zhang. Overview of millimeter wave communications for fifth-generation (5g) wireless networks—with a focus on propagation models. *IEEE Transactions on antennas and propagation*, 65(12):6213–6230, 2017.

[2] Pekka Kyösti, Wei Fan, and Jukka Kyröläinen. Assessing measurement distances for ota testing of massive mimo base station at 28 ghz. In *2017 11th European Conference on Antennas and Propagation (EUCAP)*, pages 3679–3683. IEEE, 2017.

[3] Xiaoming Chen, Jiazhi Tang, Teng Li, Shitao Zhu, Yuxin Ren, Zhihua Zhang, and Anxue Zhang. Reverberation chambers for over-the-air tests: An overview of two decades of research. *IEEE Access*, 6:49129–49143, 2018.

[4] Ryan J Pirkl and Kate A Remley. Experimental evaluation of the statistical isotropy of a reverberation chamber's plane-wave spectrum. *IEEE transactions on electromagnetic compatibility*, 56(3):498–509, 2013.

[5] Kent Rosengren and Per-Simon Kildal. Study of distributions of modes and plane waves in reverberation chambers for the characterization of antennas in a multipath environment. *Microwave and optical technology letters*, 30(6):386–391, 2001.

[6] Maria G Becker, Robert D Horansky, Damir Senic, Vincent Neylon, and Kate A Remley. Spatial channels for wireless over-the-air measurements in reverberation chambers. In *12th European Conference on Antennas and Propagation (EuCAP 2018)*, pages 1–5. IET, 2018.

[7] Magnus Otterskog and Kent Madsén. On creating a nonisotropic propagation environment inside a scattered field chamber. *Microwave and Optical Technology Letters*, 43(3):192–195, 2004.

[8] Philippe Besnier, Christophe Lemoine, Jérôme Sol, and Jean-Marie Floc'h. Radiation pattern measurements in reverberation chamber based on estimation of coherent and diffuse electromagnetic fields. In *2014 IEEE Conference on Antenna Measurements & Applications (CAMA)*, pages 1–4. IEEE, 2014.

[9] Christophe Lemoine, Emmanuel Amador, Philippe Besnier, Jean-Marie Floc'h, and Alexandre Laisné. Antenna directivity measurement in reverberation chamber from rician k-factor estimation. *IEEE transactions on antennas and propagation*, 61(10):5307–5310, 2013.

[10] Miguel Á García-Fernández, Cyril Decroze, and David Carsenat. Antenna radiation pattern measurements in reverberation chamber using doppler analysis. In *2014 IEEE Conference on Antenna Measurements & Applications (CAMA)*, pages 1–4. IEEE, 2014.

[11] Afroza Khatun, Veli-Matti Kolmonen, Veikko Hovinen, Dristy Parveg, Markus Berg, Katsuyuki Haneda, Keijo I Nikoskinen, and Erkki T Salonen. Experimental verification of a plane-wave field synthesis technique for mimo ota antenna testing. *IEEE Transactions on Antennas and Propagation*, 64(7):3141–3150, 2016.

[12] Afroza Khatun, Katsuyuki Haneda, Mikko Heino, Linsheng Li, Pekka Kyosti, and Ruiyuan Tian. Feasibility of multi-probe over-the-air antenna test methods for frequencies above 6 ghz. In *2015 Loughborough Antennas & Propagation Conference (LAPC)*, pages 1–5. IEEE, 2015.

[13] Stephen B Weinstein. The history of orthogonal frequency-division multiplexing [history of communications]. *IEEE Communications Magazine*, 47(11):26–35, 2009.

[14] Samuel C Yang. *OFDMA system analysis and design*. Artech House, 2010.

[15] Keysight Technologies. "metrics for evaluating rrm/demodulation measurement setup", May 2017. R4-1705831, 3GPP TSG-RAN WG4 Meeting 83,.

[16] Keysight Technologies. "on feasibility of mpac systems for fr2", Nov 2018. R4-1814835, 3GPP TSG-RAN WG4 Meeting 89,.

[17]

[18] TR 38.827 (V1.3.0) 3GPP. "study on radiated metrics and test methodology for the verification of multi-antenna reception performance of nr user equipment (ue)", Apr 2020. Available on:"https://www.3gpp.org/ftp/Specs/archive/38_series/38.827/".

[19] David A Reyes Paredes. *Low Cost Millimetre Wave Over-the-Air Testing Method For 5G and Beyond*. PhD thesis, University of Bristol, 2021.

[20] Stephanie Hamill. Introduction to software definied radio: Winnforum sdr 101. Available at https://www.wirelessinnovation.org/Introduction_to_SDR.

[21] Usrp-2954. Available at https://www.ni.com/en-lb/support/model.usrp-2954.html.

[22] Ettus Research, a National Instruments Brand. OctoClock Clock Distribution Module with GPSDO. Available at https://www.ettus.com/all-products/OctoClock-G/.

[23] CPS-8910. Available at https://www.ni.com/en-lb/support/model.cps-8910.html.

[24] GeeksforGeeks. What is LabVIEW?, 04. Available at https://www.geeksforgeeks.org/what-is-labview/.

[25] Ettus Research, a National Instruments Brand. LabVIEW Communications Systems Design Suite.

[26] Jan-Jaap Van de Beek, Magnus Sandell, and Per Ola Borjesson. Ml estimation of time and frequency offset in ofdm systems. *IEEE transactions on signal processing*, 45(7):1800–1805, 1997.

[27] Nisha Wadhwa, Savitasindhu Rangi, and Dheeraj Rathee. Intersymbol interference reduction and bit error rate reduction in wireless channels using zero forcing equalizer. *IOSR Journal of Electronics and Communication Engineering*, 9:82–85, 01 2014.