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Master of Science in Mechatronic Engineering

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Virtual Capacitors for Single Phase Power Electronics Converters

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Contents

List of Tables v

List of Figures vi

Introduction 1

1 Active Front End: Active Rectifier With Boost PFC Stage 3
- 1.1 The Need for Power Factor Correction in AC/DC Power Supplies 3
  - 1.1.1 Power Factor Issues in Passive Rectifiers 4
  - 1.1.2 Power Factor 5
  - 1.1.3 Power Factor Correction 7
- 1.2 Design of the Active Front End 8
  - 1.2.1 Ripple Analysis and Sizing of the DC Link 9
  - 1.2.2 Control of the Active Front End 11

2 Active Capacitor 19
- 2.1 Circuit and Operating Principle 20
- 2.2 Active Capacitor Control Strategy 22
  - 2.2.1 Control Block Diagram 25
- 2.3 Sizing of the components 35
  - 2.3.1 Sizing of the Buffer Capacitor C_s 35
  - 2.3.2 Sizing of the Auxiliary Inductor L_s 38
- 2.4 Power Switches Thermal Analysis 41
  - 2.4.1 Choice of the Semiconductor 42
  - 2.4.2 Power Switches Losses and Thermal Modelling 43

3 Simulation Results 51
3.1 PFC Converter Simulation 53
3.1.1 PFC Control Code 55
3.1.2 Preliminary Tests on the Active Front End 57
3.2 Active Capacitor Simulation 62
3.2.1 Active Capacitor Control Code 64
3.2.2 Validation of the Active Capacitor Control Strategy 66
3.2.3 Thermal Simulation 76

4 Experimental Tests 83
4.1 Experimental Set-up Realization 83
4.2 Experimental Tests 88
4.2.1 Test 1: PLL Performance 89
4.2.2 Test 2: Charging of the DC-Link and System Startup 90
4.2.3 Test 3: Load Variation on the PFC 91
4.2.4 Test 4: Precharge and Startup Phases of the Virtual Capacitor . 93
4.2.5 Test 5: Load Variation on the DC-bus with Virtual Capacitor . . 94
4.2.6 Test 6: Disconnection of the Virtual Capacitor During Load . . 98
4.2.7 Comparison of Capacity Utilization Between Active and Passive Method 99

Conclusions 101

Bibliography 104

List of Tables

1.1 PFC Design Parameters. 9
2.1 DCM current control signals. 34
2.2 Analogy between electrical circuits and thermal phenomena. 46
3.1 PFC simulation parameters. 57
3.2 Virtual capacitor simulation: controllers parameters for each tested configuration. 66
3.3 Virtual capacitor simulation: electrical parameters. 67
3.4 Cauer model components value for junction-case thermal impedance. . 78
4.1 GUASCH MTL-CBI0040F12IXHE: Power stack general characteristic . 85
4.2 Test set-up: electrical parameters. 88
4.3 Test set-up: PFC control parameters. 88
4.4 Test set-up: VC control parameters. 89

List of Figures

1.1 Full bridge rectifier operating principle. 5
1.2 Voltage and current on a full bridge rectifier filter capacitor. 5
1.3 PFC converter connected to the grid 8
1.4 PFC Control block diagram 12
1.5 PLL block diagram. 12
1.6 PFC current loop small signal diagram. 13
1.7 PFC voltage loop small signal diagram. 14
1.8 DC bus filter comparison 17
1.9 Spectral analysis of the DC bus filter comparison 18
1.10 Precharge circuit schematic 18
2.1 QV characteristic of a nonlinear capacitor 20
2.2 Active capacitor circuit. 21
2.3 Different active capacitor topologies. 23
2.4 Active capacitor small signal diagram. 25
2.5 Active capacitor current control block diagram. 25
2.6 G regulator comparison 28
2.7 Active capacitor small signal diagram. 29
2.8 Duty generation strategy 31
2.9 Load variation protection block diagram. 34
2.10 Capacitor voltage and current for different values of k. 37
2.11 L_s sizing boundaries. 40
2.12 MOSFET C3M0120065K by Wolfspeed. 42
2.13 Conduction losses for the chosen MOSFET. 44
2.14 Energy loss during commutation. 45
2.15 Schematized structure of the switches mounted on the heatsink 45

2.16 Thermal equivalent circuit for the converter setup 46
2.17 C3M0120065K Transient Thermal Impedance 47
2.18 C3M0120065K Package dimensions 48
2.19 C247-050 Heatsink from Ohmite manufacturer. 49
3.1 Active Front End PLECS model 53
3.2 Analog Conditioning and ADC PLECS model for PFC 53
3.3 Microcontroller PLECS model for PFC 55
3.4 PWM modulator PLECS model for PFC 55
3.5 PLL test simulation on a clean waveform 58
3.6 PLL test simulation on a distorted waveform 58
3.7 Results of the PLECS simulation for the PFC converter 59
3.8 Results of the PLECS simulation for the PFC converter 60
3.9 Grid side voltage and absorbed current 61
3.10 PLECS model of the active capacitor connected to the PFC. 62
3.11 Analog Conditioning and ADC PLECS models for VC 63
3.12 Microcontroller PLECS model for VC 63
3.13 PWM modulators PLECS models for VC 64
3.14 DC link voltage comparison between passive and active method 67
3.15 Working phases of the virtual capacitor 68
3.16 DC bus and buffer capacitor voltage 69
3.17 DC bus voltage waveforms comparison between the presented control strategy 71
3.18 Dead time duty compensation block diagram 72
3.19 Load reduction effects 73
3.20 Load increasing effect 74
3.21 Inductor current in CCM 75
3.22 Inductor current in DCM 75
3.23 Virtual capacitor PLECS thermal model 77
3.24 Thermal impedance model extrapolation on PLECS 77
3.25 Cauer model of the junction-case thermal impedance 78
3.26 PLECS LUTs to compute conduction losses 78
3.27 PLECS LUTs to compute switching losses 79
3.28 Junction temperature simulation results 80

3.29 Heatsink Temperature simulation results 81
3.30 MOSFET dissipated power 81
4.1 Schematic representation of the experimental setup 84
4.2 Virtual capacitor control panel created on ControlDesk 86
4.3 Experimental setup 87
4.4 Test 1: PLL Performance 89
4.5 Test 2: Charging of the DC-Link end System Startup 90
4.6 Test 3: Load Variation on the PFC DC-Link 91
4.7 Test 3: Load Variation on the PFC DC-Link 92
4.8 Test 3: Grid side quantities 93
4.9 Test 4: Charging of the buffer capacitor end System Startup 93
4.10 Test 5: Load Variation with activated virtual capacitor. 95
4.11 Test 5: Steady state waveforms on 3.3kW load with activated virtual capacitor. 96
4.12 Test 5: Load Variation Protection triggered at the transient start. 97
4.13 Shutdown of the virtual capacitor under load conditions 98
4.14 Comparison between classic DC-Link and Virtual Capacitor approach . 99

Introduction

Nowadays more and more electronic loads are connected to single phase grids, from power supplies for personal computers or laptops, to larger appliances with motors controlled by inverters, such as washing machines or air conditioning systems. Moreover, with the ongoing electrification of mobility, new technologies such as on-board battery chargers for electric cars are becoming increasingly popular in everyone's life.

All this electric appliances requires a conversion stage at the design stage to transform the alternating current supplied by the network to a direct current.

The classic method of single-phase AC/DC conversion involved the use of a full-wave rectifier which allows the passage of the positive half-wave, as well as the passage of the inverted negative half-wave, obtaining an output voltage exclusively positive with period double that of the network. The output voltage can subsequently be filtered to reduce its ripple and "smoothed" by one or more capacitors.

Although this method is one of the simplest and cheapest, it has some criticalities that cannot be ignored. The amplitude of the ripple, and therefore the average voltage on the DC bus, is strictly related to the capacity of the DC-link and to the load current. Furthermore, since there is no conduction of the diodes as long as the grid voltage is lower than the bus voltage, the current absorbed by the network has a pulsed and strongly distorted form, with a high THD, which therefore causes harmonic distortion in the network.

Through the use of active rectifiers part of these problems can be solved: an active bridge with PFC and boost stage allows a cleaner AC / DC conversion from the point of view of the network, with an output voltage that is adjustable, and maintaining a unity power factor at the input side. The dependence between the ripple amplitude and the capacity of the DC bus and load remains, but in this type of converter the ripple is mostly at twice the grid frequency, and the average value is fixed at the one imposed by the

control algorithm.

In both cases, one or more capacitors are used to reduce the low-frequency ripple. However, this involves an increase in the size of the converter and therefore a lower power density, which is becoming an index of fundamental importance for the new generations of converters. The most used capacitors for this function on the DC link are usually of the electrolytic aluminium type, because these guarantee a good compromise between cost and energy density. However, these capacitors are known to be bulky and have a relatively low reliability [1], therefore making it necessary to search for a more effective solution, which allows for a higher power density, with a more reliable type of capacitors and with reduced capacitance.

Several active methodologies have been explored over the years to deal with second harmonic ripple of the AC side in single-phase applications, namely ripple eliminator, ripple reduction circuit, active capacitors, virtual infinite capacitor. Each of these methods has an auxiliary circuit and an auxiliary energy storage device.

The goal of this thesis is to design a similar device and study a control strategy to apply to it. The experimental validation will be performed by using an IGBT inverter in a configuration such that the first two inverter legs are used as a single-phase active rectifier with PFC and boost stage, while the third leg will be used as a bidirectional buck-boost for the auxiliary circuit, together with a buffer capacitor in which to store the ripple energy.

In the first chapter the working principle of a single phase active rectifier is described, as well as the sizing of the passive components and the control scheme.

In the second chapter, the analysis of the auxiliary circuit for the active capacitor is carried out, with sizing of passive components and control algorithm, together with a thermal model of the setup.

The third chapter presents the simulation results.

In the fourth chapter the experimental setup is presented, as well as the experimental results.

Finally, the conclusions are presented and the personal contributions to this work are summarized.

Chapter 1

Active Front End: Active Rectifier With Boost PFC Stage

1.1 The Need for Power Factor Correction in AC/DC Power Supplies

Power factor is defined as the ratio of active power a device is capable of transmitting to the output versus the total amount of apparent power it takes from the input power source. It is a key figure for the design of electrical devices, especially due to the regulations put in place by countries and international organizations like the EU, which define the minimum power factor or maximum level of harmonics a device must have in order to be sold in the European market. The reason why these organizations are so invested in improving power factor is because low power factor is a real threat to the power grid, increasing heating losses and potentially causing a power failure. There are two main causes of poor power factor:

- Phase displacement: This occurs when a circuit's voltage and current waves are out of phase, usually due to the presence of reactive elements such as inductors or capacitors.
- Distortion: Defined as the alteration of the wave's original shape, this is usually caused by nonlinear circuits, such as rectifiers. These nonlinear waves have a lot of harmonic content, which distorts the voltage in the grid.

The term Power factor correction (PFC) identifies the series of methods used to try to improve a device's power factor. In order to fix displacement issues, external reactive components are commonly used to compensate the circuit's total reactive power.

To solve distortion problems, there are two options:

- Passive power factor correction: Improves PF by filtering out harmonics using passive filters. This is typically used in low-power applications, but is not enough at high power [2].
- Active power factor correction (PFC): Uses a switching converter to modulate the distorted wave in order to shape it into a sine wave. The only harmonics present in the new signal are at the switching frequency, so they are more easily filtered out. This is considered the best PFC method, but adds complexity to the design.

A good power factor correction circuit is a crucial element for any modern design, because a device with a bad power factor is going to be inefficient, will put an unnecessary strain on the grid, and possibly cause problems to the rest of connected devices.

1.1.1 Power Factor Issues in Passive Rectifiers

As mentioned before, an AC/DC power supply is made up of several circuits that transform an input AC voltage into a stable DC voltage at the output. The first step is the rectification of the input voltage, that is the process of converting a signal from AC to DC, and is done using a rectifier. The negative voltage in the AC wave can be either cut off using a half-wave rectifier, or inverted using a full-wave rectifier. In the latter configuration diodes switch on and off as the voltage from the power supply goes from negative to positive, inverting the negative half-wave's polarity and turning the AC sine wave into a DC wave

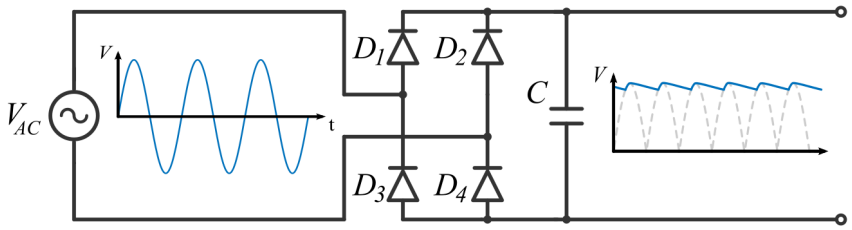


Figure 1.1: Schematization of the operation of full bridge rectifier.

The output wave has a large voltage variation, called ripple voltage, so a filtering capacitor is connected in parallel to the diode bridge to help smooth the output voltage ripple. However, observing the waveform of the rectifier's filtering capacitor, it shows that the capacitor is charged during a very short time, from the point where the voltage at the input of the capacitor is greater than the capacitor's charge, to the rectified signal's peak. This creates a current waveform characterized by pulses, which has an high harmonic content.

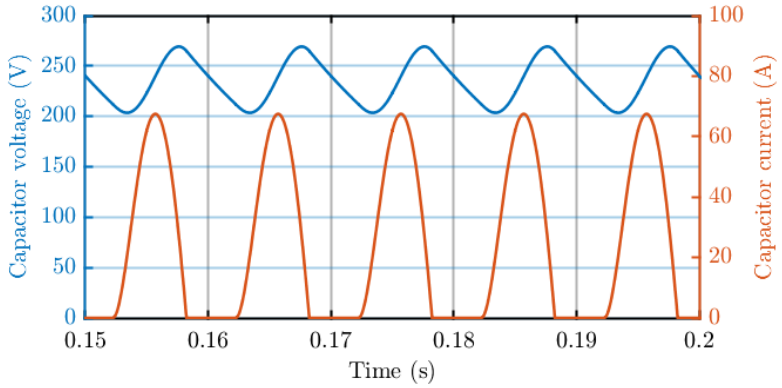


Figure 1.2: Voltage and current on a full bridge rectifier filter capacitor.

1.1.2 Power Factor

The power factor (PF) is a combination of two factors: displacement and distortion. The first, also known as $\cos\varphi$, is due to the presence of reactive components that make the current and voltage waves fall out of phase. The effect that the phase difference between the voltage and current has on the total power factor is defined by the displacement factor, which is calculated as the cosine of the angle between waves using

$$PF_{DISP} = \cos\varphi = \cos(\theta_V - \theta_I) \tag{1.1}$$

However, power factor is not only affected by the phases of current and voltage, but also by the fact that the current waveform could become a nonlinear function, like a pulse train. This means that the multiplication of the voltage and current, also known as power, is also nonlinear and highly inefficient. This occurs when a circuit has nonlinear loads, such as fluorescent lights, electronic devices, and full-bridge rectifiers. These loads draw current in very short and abrupt bursts, which generates a very large quantity of harmonics, adding distortion to the signal. The most frequent way of describing the amount of distortion present in a signal due to the presence of harmonics is through the magnitude of total harmonic distortion (THD), which represents the proportion of harmonic current relative to the fundamental current. THD can be calculated using

$$THD = \frac{X_{RMS,ripple}}{X_{RMS,1}} = \frac{\sqrt{\sum_{i>1}^{n} X_{RMS,i}^2}}{X_{RMS,1}} \tag{1.2}$$

Where n is the last harmonic considered with in the calculation (in Europe, up to the 40th). The correlation between THD and distortion power factor is described by the equation

$$PF_{DIST} = \frac{1}{\sqrt{1 + THD^2}} \tag{1.3}$$

The product of the displacement factor and the distortion factor makes up the power factor, calculated with equation

$$PF = PF_{DIST} \cdot PF_{DISP} = \frac{\cos\varphi}{\sqrt{1 + THD^2}} \tag{1.4}$$

Power factor does not often significantly affect a device's operation, but when the current is fed back into the grid, it brings with it some long terms issues, such like losses due to heating in cables, capacitors and electrical machines.

Understandably, power suppliers have put forward limitations into the amount of power interference a device can apply to the grid. The first attempt to do this was in 1899, with the start of electric lighting, when they realized that interference from other devices

was making incandescent lights flicker. Then, in 1978, a regulation from the International Electrotechnical Commission (IEC) was put forward to force the introduction of power factor correction in consumer products. Since then, different countries have created their own guidelines and regulations on power factor limitations. In the United States, the voluntary Energy Star guideline states that any computing equipment must have a PF of at least 0.9 when working at its maximum rated output. In the EU, the legislation (IEC61000-3-2) is more stringent, dividing electrical devices into four categories: appliances (A), power tools (B), lighting (C), and electronic devices (D). Each category has specific limitations on the relative weight that each harmonic can have with respect to the fundamental frequency. Other countries have their own specific versions of this legislation, such as the Chinese GB/T 14549-93 or the international IEEE 519-2014.

1.1.3 Power Factor Correction

Power factor correction (PFC) is a series of methods that manufacturers of electronic devices use to improve their power factor.

The negative effect of displacement on the power factor is relatively simple to solve, because capacitors drag the phase forward, while inductors drive it back. If a system's current wave is lagging behind the voltage, it can be easily solved by adding a capacitor with the right impedance to the circuit, and the current wave's phase will be pulled forward until it is in phase with the voltage. On the other hand, improving a system's distortion factor, which is usually present in nonlinear circuits, is slightly more complicated than compensating the displacement factor found in linear circuits. To do so, there are two options:

- Filtering out harmonics: it does not solve the loss in efficiency, but reduce the number of harmonics injected into the grid by adding filters at the input. This is called passive PFC, and uses a low-pass filter aimed at eliminating the higher order harmonics, ideally leaving only the 50Hz fundamental frequency. In practical applications, it is not very effective at improving a device's PF, and is also impractical for high-power solutions, because of the loss of efficiency and the loss of power density due to the size of the necessary capacitors and inductors. It is not typically used in applications with powers above hundreds of watts.

- Active power factor correction: this method changes the current waveform's shape,

making it follow the voltage. This way, the harmonics are moved to much higher frequencies, multiples of the switching frequency, making them much easier to filter out. The most widely used circuit for these cases is a boost converter.

1.2 Design of the Active Front End

Over the years, various topologies of single-phase active PFCs have been studied in the literature, from the simplest such as the Single-phase boost PFC converter, which integrates a boost phase at the output of a diode bridge, to the most complex such as semi-boost converter, half-bridge converter, interleaved converter, which integrate power switches and diodes in different configurations according to the needs in terms of efficiency, dimensions, output voltage or load, allowing in some configurations a bidirectional use of the converter [3].

All of them follow the same principle of operation, divided in two stages. In the first stage, when the switch is closed, the input inductor is charged by the voltage source which, in this case, is the grid. When the switch opens, the inductor's magnetic field collapses injecting the current it had stored in the previous stage into the circuit, increasing the voltage at the output. This current also charges a capacitor, which is responsible for maintaining the voltage level at the output while the inductor recharges. A free-wheeling diode is required, be it discrete or integrated into the power switch as a body diode in full active topologies, to prevent capacitor charges from flowing back into the grid when the switch is closed.

For the purpose of the report, it was chosen to use a Single-phase voltage source converter type topology, which includes a power switch H-bridge.

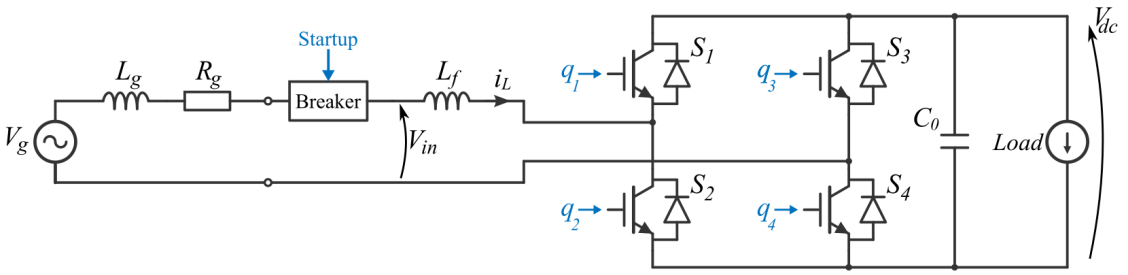


Figure 1.3: Circuit schematic for the PFC converter connected to the grid.

The design requirements are reported in Table 1.1.

Table 1.1: PFC Design Parameters.

Grid Voltage	V_g	$\sqrt{2}$ 230	[V]
Grid Frequency	f_g	50	[Hz]
Grid Inductance	L_g	2	[mH]
Grid Resistance	R_g	0.15	[Ω]
Inductance	L_f	2.2	[mH]
DC Bus Voltage	V_{dc}	400	[V]
DC Bus Voltage Ripple	ΔV_{dc}	± 2%	[V]
Output Power	P_0	3.3	[kW]

1.2.1 Ripple Analysis and Sizing of the DC Link

Since the power source is the grid, the AC supply voltage v_g and current i_s are assumed to be sinusoidal, as shown in the equations:

$$v_g(t) = V_g \sin(\omega t) \tag{1.5}$$

$$i_g(t) = I_g \sin(\omega t + \varphi) \tag{1.6}$$

where V_g and I_g are the voltage and current peak values; ω and φ are respectively the supply angular frequency and the angle between the supply voltage and current. By means of the Werner formulas, the power absorbed from the grid can be expressed as follows:

$$P_{in}(t) = v_g(t) i_g(t) = \frac{V_g I_g}{2} \cos\varphi - \frac{V_g I_g}{2} \cos(2\omega t - \varphi) \tag{1.7}$$

The energy of the input inductor L_f can be expressed as (1.8) and the corresponding power as (1.9)

$$E_L = \frac{1}{2} L_f i_g^2(t) = \frac{1}{2} L_f I_g^2 \sin^2(\omega t - \varphi) \tag{1.8}$$

$$P_L = \omega L_f I_g^2 \sin(\omega t - \varphi)\cos(\omega t - \varphi) \tag{1.9}$$

The input power of the converter after the inductor can be obtained subtracting (1.7)) and (1.9)) and rewritten with the duplication formulas as

$$P_{in}(t) = \frac{V_g I_g}{2}\cos\varphi + \left(\frac{V_g I_g}{2}\cos(2\omega t - \varphi) - \frac{\omega L_f I_g^2}{2}\sin(2\omega t - 2\varphi)\right) \tag{1.10}$$

From (1.10) we can see that the instantaneous power is composed by two component: a constant power P_0 that feeds the load and a ripple power P_r that evolves in time with the form of a second harmonic. here the reciprocal definitions are highlighted:

$$P_0 = \frac{V_g I_g}{2}\cos\varphi \tag{1.11}$$

$$P_r = \frac{V_g I_g}{2}\cos(2\omega t - \varphi) - \frac{\omega L_f I_g^2}{2}\sin(2\omega t - 2\varphi) \tag{1.12}$$

Assuming, also, an ideal power converter without losses, the output power is P_0 equals to the constant power in (1.11). The peak AC-side supply current can then be defined as

$$I_g = \frac{2P_0}{V_g \cos\varphi} \tag{1.13}$$

We can now use the ripple power (1.12) and the peak current (1.13) to determine the ripple energy:

$$E_r = \frac{\hat{P}_r}{\omega} = \frac{\sqrt{P_0^2 + ((2\omega L_f P_0^2/V_g^2\cos^2\varphi) - P_0(\sin\varphi/\cos\varphi))^2}}{\omega} \tag{1.14}$$

Where $\hat{P}_r$ is the peak value of the ripple power.

From here we can see that the ripple the relationship between the ripple energy, the AC input voltage and frequency, the input inductor and the output power. Since we are

talking about a PFC it is reasonable to assume that, in the end, the angle φ is about zero, and this allows us to simplify (1.14) obtaining

$$E_r = \frac{\sqrt{P_0^2 + (2\omega L_f P_0^2 / V_g^2)^2}}{\omega} \tag{1.15}$$

To prevent this ripple to affect the load, an alternative ripple storage device or component must be provided, which should simply act as a ripple filter. [4].

Broadly speaking, both capacitors and inductors can be used as components to store ripple energy. However, the latter ones have lower characteristics than capacitors in terms of energy density, for low frequency applications, so our choice will be capacitive. With fixed voltage rating for the DC bus, the choice of the capacitor is based on two aspects: capacitance and current rating. With the single-phase ripple energy requirement derived in (1.15) and the voltage ripple requirement ΔV_{dc}, the DC bus capacitance needed can be calculated as:

$$C_0 = \frac{\sqrt{P_0^2 + (2\omega L_f P_0^2 / V_g^2)^2}}{2 V_{dc} \Delta V_{dc} \omega} \tag{1.16}$$

Then, for the converter requirement specified in Table 1.1 of 2% ripple, a 1.6 mF capacitance is needed. The current rating of the capacitor can then be computed as:

$$i_{bus_{RMS}} = \frac{\hat{P}_r}{\sqrt{2}\, V_{dc}} \tag{1.17}$$

Which give us a current rating of 5.84 A_{RMS}.

1.2.2 Control of the Active Front End

The control of the PFC converter will be designed to work in CCM, meaning that the current in the inductor will not became null during a switching period. The switching frequency is set to be 20 kHz. Here, a picture shows the block diagram of the control algorithm.

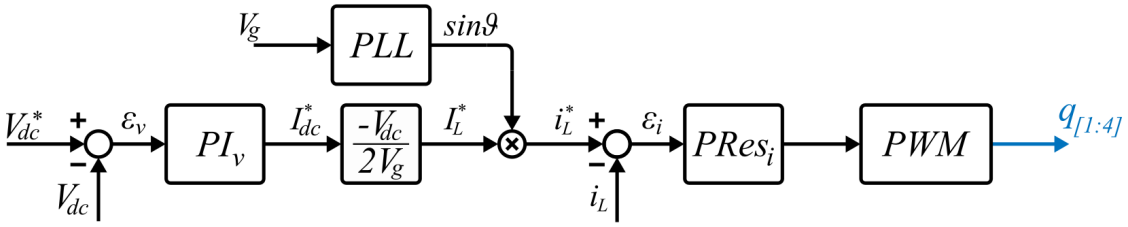


Figure 1.4: PFC Control block diagram composed by a voltage loop in cascade with a current loop, and a PLL for grid synchronization.

As we can see from the control figure, the control philosophy consists of two cascaded controls, with a current loop within a voltage loop. The quantities that must be measured, necessary for the operation of the control, are the mains voltage v_g, the voltage on the DC bus V_{dc} and the current in the filter inductor i_L. A Phase Locked Loop (PLL) block is used to sense the mains voltage and derive its phase, which is used to generate the current reference. In the following subsections the stages of the control system will be explored.

Grid Synchronization: Phase Locked Loop

Since the current in the input inductor must have a sinusoidal waveform in phase with the grid voltage, a phase locked loop in the form of a second order general integrator (SOGI) with a quadrature signal generator (QSG) is implemented [5].

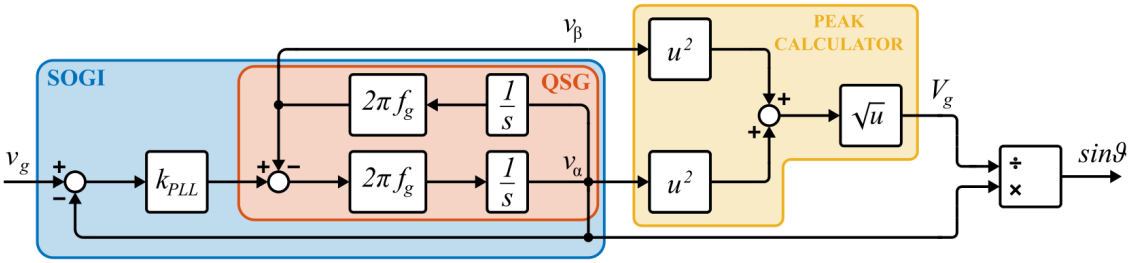


Figure 1.5: PLL block diagram.

The SOGI provides a filtered grid voltage v_α which represent the first harmonic at the grid frequency, while the QSG generate a signal shifted by 90 electrical degrees, named v_β. The peak value of the grid voltage is then derived by means of the root sum square of the two signals. By dividing v_α by the peak value, a new signal representing

the $sin(\theta(t))$, where $\theta(t)$ is the instantaneous angle of the grid voltage, is obtained. The tunable gain k permits to regulate the selectivity of the resonant filter and adjust the dynamical performance.

Current Loop and Duty Generation

Since we are dealing with a sinusoidal reference, generated by the product of the voltage regulator and the PLL block outputs, to ensure a fast tracking of the signal, a proportional-resonant (P-Res) controller is chosen for the application. The small signal diagram used for the calibration of the controller parameters is shown in Fig.1.6.

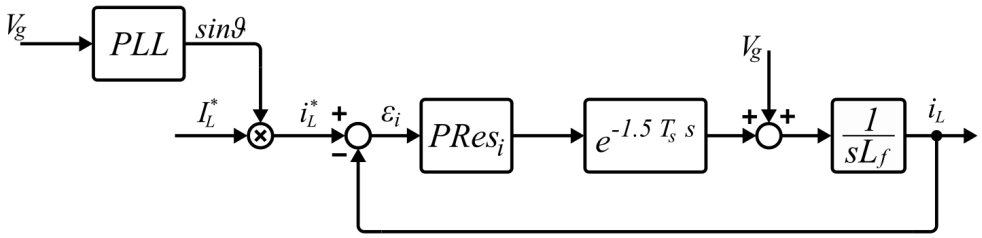


Figure 1.6: PFC current loop small signal diagram.

It is established that the term K_{p_i} of a P-Res is closely related to the counterpart of a more common PI regulator, therefore the procedure for the calculation is the same. Starting from the desired bandwidth for the current loop f_{BW_i}, that should be at most a decade lower with respect to the converter pole, the K_{p_i} is calculated in 1.18.

$$K_{p_i} = 2\pi f_{BW_i}\ L_f \tag{1.18}$$

The resonant part is based on the same kind of filter used in the PLL block, where the gain K_{r_i} is manually adjusted to find the right compromise between dynamics and filtering.

An anti windup limit equal to the DC bus voltage has been imposed on the controller, to improve dynamics and prevent overvoltages on the bus. The possibility of adding a feed-forward has been explored, however it has been showned to increase significantly

the sensitivity of the control, making it more prone to instability. To avoid spikes in the start-up phase due to the lack of a feed-forward term, the integral parts of the resonant branch have been initialized to the values of v_α and v_β generated by the PLL.

The duty signal is subsequently generated in the optics of a unipolar PWM, normalizing the output value of the regulator to the voltage on the DC bus, as shown in the following formula:

$$d(t) = \frac{1}{2}\left(1 + \frac{V_{Ref}}{V_{dc}}\right) \tag{1.19}$$

Subsequently, before being sent to the modulator, the duty signal is saturated between 0 and 1.

Voltage Loop

The Voltage loop is controlled by a Proportional Integral (PI) regulator with a fixed reference at the value of 400 V. The DC bus voltage is sensed and used as feedback to generate the error to feed as input in the PI. The K_{p_v} and K_{i_v} parameters has been calculated based on the small signal diagram in Fig.1.7, starting from the desired bandwidth f_{BW_v}. For this computation the current loop is treated as a unitary gain.

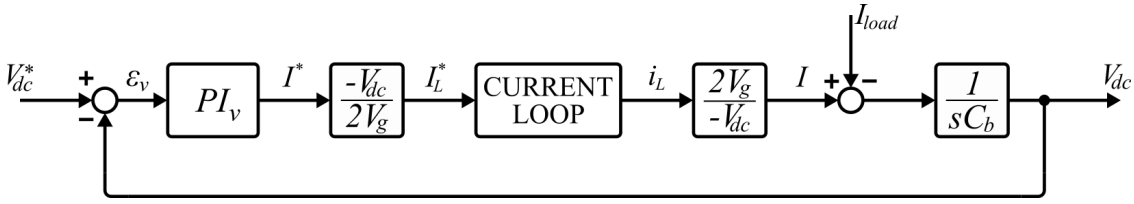


Figure 1.7: PFC voltage loop small signal diagram.

$$K_{p_v} = 2\pi f_{BW_v}\, C_{bus} \tag{1.20}$$

Where $2\pi f_{BW_i}$ is the crossover angular frequency ω_{c_v}. Recalling the ZPK format of the transfer function of a PI regulator

$$PI = K_p + \frac{K_i}{s} = K_p \frac{s + \omega_z}{s} \tag{1.21}$$

we can see that the controller has a zero in $\omega_z = K_i/K_p$. Knowing K_{p_v}, our intention is to set this zero sufficiently lower with respect to the crossover frequency so that the controller has a good phase margin, hence good stability and dynamic response. Technically, a correction factor of $1/\sqrt{3}$ should give us a margin phase equal to 60° anyway, to be conservative, a correction factor of $1/5$ is applied. The computation of the K_{i_v} term is expressed by (1.22).

$$K_{i_v} = \omega_{z_v} K_{p_v} = \frac{\omega_{c_v}}{5} K_{p_v} \tag{1.22}$$

An anti windup term limits the output current to a value of 10 amps, equal to the required current for a 3.3 kW device plus 20% of margin.

Since the output signal of the regulator gives us the reference current for the DC side (I_{dc} in (1.23)) it has to be normalized to the AC side peak value, where is measured and controlled. Considering the converter as ideal (i.e., no losses) we have that

$$P_{in} = \frac{V_g I_g}{2} \cos\varphi = V_{dc} I_{dc} = P_{out} \tag{1.23}$$

As already mentioned before, we can neglect the $\cos\varphi$ term, as φ is approximately equal to zero. By rearranging (1.23) and adding a minus sign to be coherent with the direction of the inductor measured current we obtain

$$I_g^* = -2 I_{dc} \frac{V_{dc}}{V_g} \tag{1.24}$$

Choice of the Filter on the DC-Bus Voltage Signal

As demonstrated in the formula (1.12) the ripple power, and therefore the ripple voltage in the DC side of a PFC tends to an oscillation frequency of twice that of the grid (second harmonic). However, in the first simulations, after having sized the voltage

and current loop to reasonable bands with respect to the switching frequency, with a connected load the bus voltage was characterized by a mean value that did not reach the reference and a strongly distorted waveform with respect to the expected second harmonic, as shown in Fig.1.8.a.

This was due to the fact that the feedback signal from the DC-bus brought these oscillations back to control, generating an error signal that was higher than expected and more difficult for the voltage loop to follow correctly. This results mostly in fourth harmonic distortion on the DC-bus and saturation of the controller output, leading to the failure to reach the average reference value. To overcome the problem it was decided to insert a digital filter in the feedback branch of the bus voltage, in order to bring back to the control only the average value of V_{dc}. Being aware of the ripple pulsation, the attempts were focused specifically on filters in able to act selectively on set frequencies. The choices were mainly three:

- Moving Average Filter: by setting the filter interval to an integer multiple of the ripple frequency, the output value will be the average of V_{dc}. This filter has been discarded as filling the memory vector to calculate the average of requires $N = T_r/T_s = 200$ samples, meaning that the controller has to work with the same input for 200 cycles. This places a serious limitation on the bandwidth of the control loop, and therefore has been discarded as option.

- Continuous Moving Average Filter: works with the same principle of the moving average but the memory vector is updated at each cycle. At every sampling period, the last element of the memory vector is deleted and replaced with the last sampled, and the average is recalculated. The only downtime is at startup where there are 200 cycles where the filter stays idle.

- Notch Filter: this is based on the same principle of the resonant filter discussed above. The operation foresees that the output generated by a resonant filter, set to work at the ripple frequency, is subtracted from the feedback signal V_{dc}, effectively eliminating only the 100Hz component.

Figure 1.8 shows the bus voltage waveforms at steady state in different conditions along with the current absorbed from the grid: without filter with control loop at 80Hz

(a) and 50Hz (b), with notch and 80Hz bandwidth (c) and with continuous moving average filter (d) with 50Hz bandwidth. The respective spectral analysis are shown in fig. 1.9. For reasons of scale, the continuous component has been omitted.

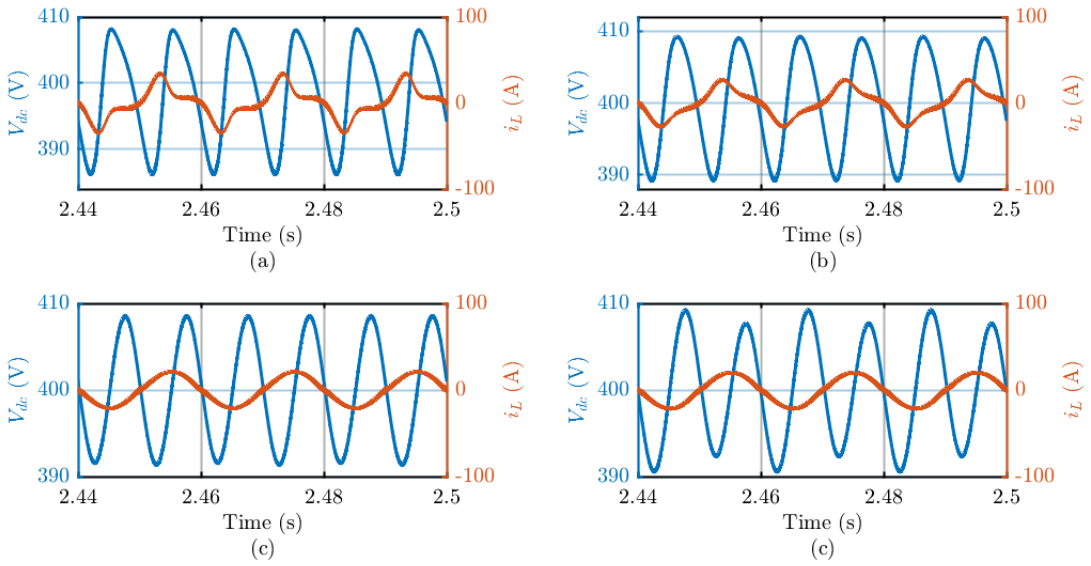


Figure 1.8: DC bus voltage waveform on different bandwidth and filter condition, along with the current absorbed from the grid: (a) is without filter and the bandwidth of the voltage loop is 80Hz; (b) is without filter and the bandwidth is 50Hz; (c) is filtered by a Notch filter and the bandwidth is 80Hz; (d) is filtered by the Continuous Moving Average and the bandwidth is 50Hz.

As we can see from the waveforms in unfiltered conditions the harmonic content of the signal is much greater than in the filtered counterparts. A reduction in bandwidth can, in fact, improve the situation but at the price of an overall less responsive system. The notch and continuous moving average filters, on the other hand, in addition to considerably reduce the harmonics of higher degrees, also have an effect on the amplitude of the 100Hz ripple.

The continuous moving average, however, has limits on the band which, even if lower than non-continuous, if pushed lead to the appearance of a 50Hz component. For this reason, the notch filter has been chosen for the purpose.

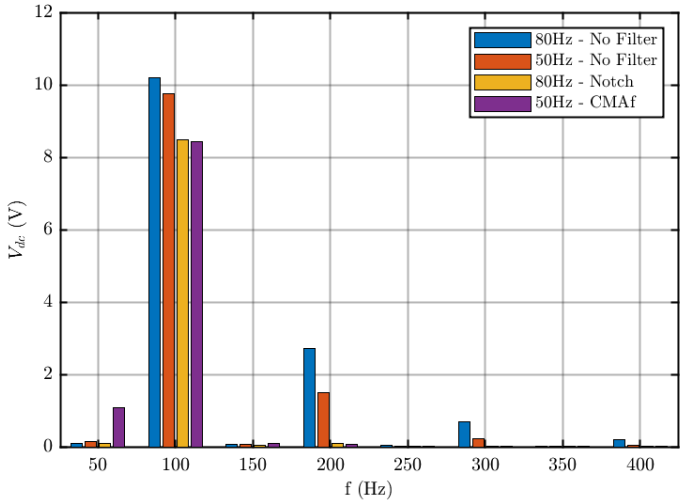


Figure 1.9: Spectral analysis of the DC-bus voltage in different conditions.

Precharge

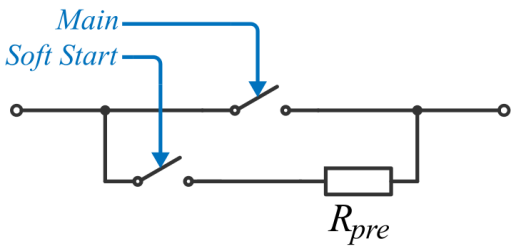


Figure 1.10: Schematic of the precharge circuit.

Since at the beginning of the transient the DC link capacitors behave like a short circuit, a precharge state has been added to avoid overcurrents. The operating principle is simple: when the control is started, the precharge relay on the power resistor ($R_{pre} = 15\Omega$) is closed; the power switches are all kept open, leaving it to the body diodes to function as a normal rectifier bridge. When the voltage on the DC bus reaches 300V, the main switch is closed, excluding the precharge resistor, and the system waits for the GO command to start modulation, following a ramp reference that goes from a value equal to $1.05V$ up to the target voltage value, with a slope decided in the design phase.

Chapter 2

Active Capacitor

As mentioned before, it is known that single-phase active rectifiers have second-order harmonics current and corresponding ripple voltages on the DC bus. For battery powered system, large ripple currents and voltages could reduce the life of battery considerably, as well as with fuel cells. Generally speaking, current ripples should be less than 10% of the batteries rated current. Usually, a bulk electrolytic capacitor on the bus is used to filter these low frequency harmonics resulting in low power density, which can be a problem for weight-critical and/or volume-critical application. Moreover, electrolytic capacitor are well known for their poor reliability despite the high cost [6].

It has been observed, over the years, how the energy fluctuations inside the filter capacitors are very limited when compared with the average stored energy, to the point that most of the energy is in fact idle [7]. This small ripple energy could also be stored in an smaller buffer capacitor by means of an an auxiliary power circuit tied to the DC bus, with large voltage fluctuation. furthermore, having a reduced capacity as it is exploited to the maximum, the buffer capacitor could be of a more reliable type such as ceramic or film.

This situation led to various circuits known as "ripple eliminators", "ripple energy storage", "active capacitors", "virtual infinite capacitors", see for example [6], [8], [9], [10] or [11]. Each of this circuit use small buffer capacitor and a bidirectional converter, controlled to make it transfer only ripple energy from the DC bus to the capacitor, and back.

A big problem with early examples of active capacitor control is that they required a fixed reference voltage. To make sure that the equilibrium voltage to be reached on the DC bus was the same for the active converter, the charge control of the active capacitor had to be connected in some way with the host power system. This required modifications to the power converter source and thus required a specialist to install. Some new control approaches, on the other hand, are aimed at making this type of technology plug-and-play, which therefore allows the connection of the auxiliary circuit directly to the DC bus by means of only two terminals.

In this chapter a brief introduction to the concept of active capacitor will be given, both from the hardware and software point of view, along with a more in-deep analysis in which the passive components will be sized and a control technique will be explored, both for Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM).

2.1 Circuit and Operating Principle

The idea standing at the base of this application is the nonlinear capacitor. Where a normal capacitor has a linear dependence between voltage V and charge Q, the $Q - V$ plot of the proposed circuit has a plane region for $Q \in [Q_{min}, Q_{max}]$, (Fig.2.1).

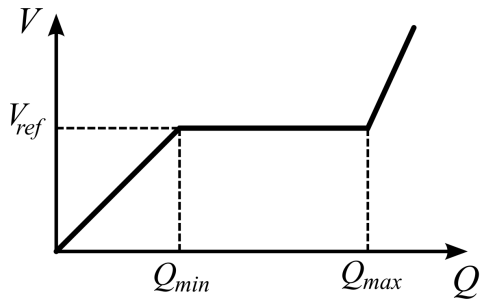


Figure 2.1: QV characteristics of a nonlinear capacitor. The normal operating range is where $Q \in [Q_{min}, Q_{max}]$. V_{ref} is chosen by the user.

For charge fluctuation inside this interval the voltage remains at the predefined level V_{ref}, which is the equilibrium voltage of the DC bus. Since the dynamical capacitance C at a given Q can be defined as (2.1)

$$\frac{1}{C} = \frac{dV}{dQ} \tag{2.1}$$

a flat region in the $V - Q$ characteristic will translate to a virtually infinite capacitance, charged at the voltage V_{ref}. To function properly, the charge Q must be measured and controlled in this circuit, to prevent it from leaving the desired range $[Q_{min}, Q_{max}]$.

Speaking of circuitry, there are many ways to obtain this kind of behaviour, but for the purpose of this thesis we will only explore the one based on the bidirectional DC/DC converter (canonical switching cell), as shown in the simplified circuit in Fig.2.2. Here, the smaller capacitor C is used to filter the high-frequency switching noise on the DC bus, while the buffering capacitor C_s is used to store the ripple energy of the low frequency harmonics.

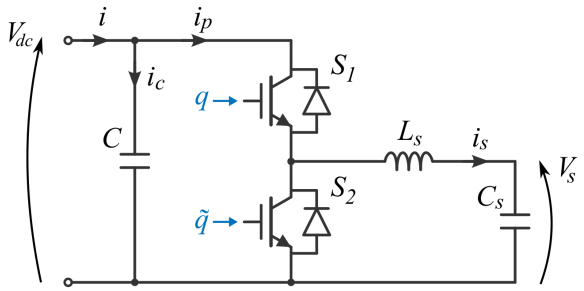


Figure 2.2: Approximate realization of the active capacitor, showing only the main circuit elements without showing the sensing and control circuits. q and $\tilde{q}$ are binary signals coming from the controller, which determine the ON or OFF status of the switches.

The signals q and $\tilde{q}$ drives the switch at a fast rate so that the upper switch is ON when if $q = 1$, and similarly for the lower one. A software limitation must impose that in no case both the switches are getting the ON signal, to prevent a short circuit on the DC bus. By means of this converter, charge fluctuations are moved from the DC bus to the buffer capacitor C_s, as long as they are included in the range $[Q_{min}, Q_{max}]$ and their frequency is much lower than the controller sampling frequency $1/T_s$.

In this way, the voltage V_s will vary, while the bus voltage will remain stable at the equilibrium value, which is the goal of the circuit. By defining $[V_{s_{min}}, V_{s_{max}}]$ as the maximum interval in which the voltage on the buffer capacitor can vary while $Q \in [Q_{min}, Q_{max}]$, it is imposed that $0 < V_{s_{min}} < V_{s_{max}} < V_{ref}$

$V_{s_{min}}$ is the lowest voltage value at which the converter could work properly in boost mode. It must not be set too low, because it would make the converter work with a high voltage ratio, leading to low efficiency. Typically it is imposed at a quarter of the equilibrium voltage on the DC bus. $V_{s_{max}}$ should be chosen lower than V_{ref}, in our case $V_{s_{max}} = 390\ V$ has been imposed. We can now understand how Q_{min} is the charge Q that causes V_s to reach the value of $V_{s_{min}}$. The same concept is applicable to Q_{max} and $V_{s_{max}}$.

Referring to the circuit of Fig.2.2, it is possible to better analyze the working phases of the non-linear capacitor shown in the graph of Fig.2.1. In the first region, $Q < Q_{min}$, the precharge takes place, usually in power up process. To avoid overcurrents inside the capacitor C_s a duty signal equal to (2.2) is used.

$$D_{pre}(t) = \frac{V_{pre}(t)}{V_{ref}} \tag{2.2}$$

where $V_{pre}(t)$ varies linearly from 0 to the value $(V_{s_{min}} + V_{s_{max}})/2$, with a slope decided in the design stage. In this phase the dynamical capacitance of the circuit equals to

$$\frac{dQ(t)}{dV} = C + D_{pre}^2(t)\ C_s \tag{2.3}$$

The second region, $Q \in [Q_{min}, Q_{max}]$, is the normal operating range of the active capacitor. Here, the dynamic capacitance is virtually infinite and Q will vary while V will remains almost constant.

The third region, $Q > Q_{max}$, must be avoided: here the voltage on the buffer capacitor is greater than $V_{s_{max}}$ and the control cannot work as it should. Both switches are opened and the only capacity connected to the DC bus is that of capacitor C [8].

2.2 Active Capacitor Control Strategy

As already mentioned above, the objective of this thesis concerns the study of an active capacitor that allows a type of Plug-and-Play (PnP) application, which guarantees ease of installation to the end user. This type of object should ideally only need two terminals to connect to the DC bus, like the passive counterpart. The choice of this type of design obviously involves several complications in the study of the control which,

being decentralized in nature, is blind with respect to the primary power source to which it is connected, from which it receives only the bus voltage as input signal.

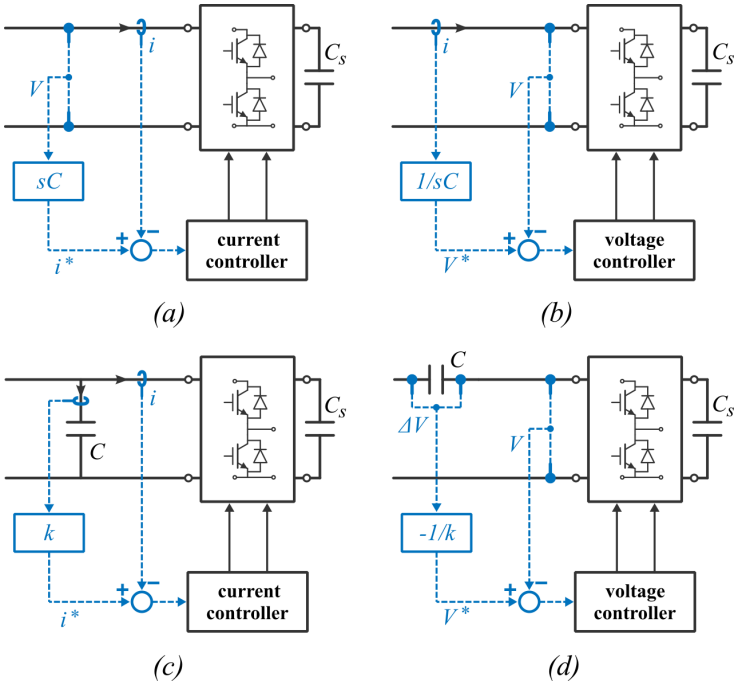


Figure 2.3: Topologies of active capacitors according to [12]: voltage controlled current source (a), current controlled voltage source (b), current controlled current source, with $k > 0$, (c) and voltage controlled voltage source, with $k \geq 1$ (d).

The idea is, therefore, to take advantage of the few data available to set the control so that it emulates an impedance for a certain range of frequencies: this application being mainly dedicated to active conversion methods, e.g. PFC, in addition to voltage of bus we know that the low frequency ripple to be filtered will be a second harmonic with respect to the mains voltage, so the controller can be designed following the internal model principle [13] [14].

According to [12], active capacitors can be divided into 4 types, as shown in Fig.2.3: voltage controlled current source (a), current controlled voltage source (b), current controlled current source, with $k > 0$, (c) and voltage controlled voltage source, with $k \geq 1$ (d). The reference signals are generated by means of a digital differentiator or integrator in the first two cases, while in the last two a physical capacitor is used, in order to

avoid numerical problems in the implementation. The scheme in Fig.2.3.c can be interpreted as a current capacitance multiplier: the current in the capacitor C multiplied by a gain k generates the reference for the converter connected in parallel, which behaves as a capacitance of value kC, resulting in a equivalent capacity equal to $(1+k)C$, with $k > 0$.

All these 4 control topologies can be used for PnP applications for the active capacitor, as seen in for example in [15], [16] or [17], and correspond to a type of direct approach, in which the bidirectional converter together with the buffer capacitor have the function of "power source" and the control targets are DC bus voltage and current. Several methods have been tested in the course of this thesis, but the best results have been obtained through the indirect approach proposed in [18].

In this case the control target is the direct regulation of the voltage on the buffer capacitor, and consequently on its energy according to $1/2CV_s^2$, in order to indirectly influence the bus voltage. In this case the converter group plus capacitor is seen by the DC bus as a load. Although it is not exactly the same, the type of control can be compared to that in Fig.2.3.c, but instead of controlling a current it controls the voltage V_s. The result will be a capacitance multiplier with a gain k, where k must be carefully crafted to be frequency dependent, in a way that very low frequencies get less amplification with respect to the range that have to be filtered.

In the following subsection the control block diagram is examined, both for the case of CCM and DCM, then an analysis of the dynamical impedance is performed.

2.2.1 Control Block Diagram

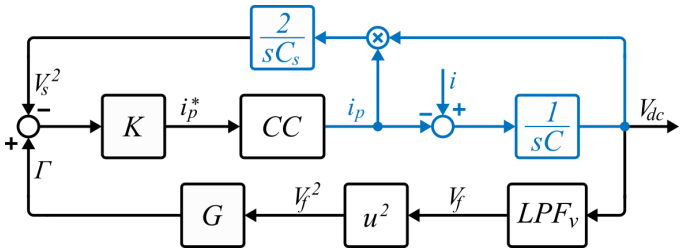


Figure 2.4: Active capacitor small signal diagram. The plant is represented in blue, the control in black.

In Fig.2.4 the small signal for the active capacitor is proposed. The CC block represent the current control, the content of which varies according to the operating principle, as shown in Fig.2.5: in DCM (Fig.2.5.a) the control is modelled exclusively as the converter, while in CCM (Fig.2.5.b) it also includes a feedback control loop to regulate the inductor current.

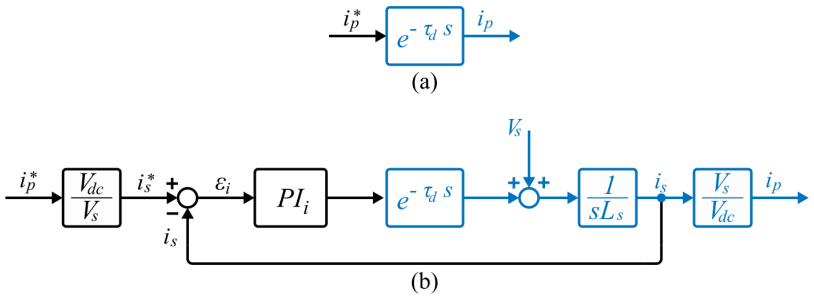


Figure 2.5: Modelling of current control for DCM (a) and CCM (b) application.

The converter is schematized as a pure delay $e^{-s\tau_d}$ where

$$\tau_d = 1.5\, T_s = \frac{1.5}{f_{sw}} \tag{2.4}$$

Here T_s is the switching period of the PWM process, same as the sampling period, and the factor 1.5 takes in account the delay of one sampling time, inevitable in digital control, together with the sampling process, A/D conversion, control and duty generation. Current control will be examined in more detail below, to emphasize the different approaches of CCM and DCM.

The controller of the active capacitor is composed of all the parts external to the plant, which is represented in blue, and receives as input the bus voltage V_{dc} and the voltage on the buffer capacitor V_s for DCM, while inductor current i_{L_s} is also needed only for CCM application. An analog Low-Pass Filter (LPF) is used on the DC bus voltage feedback, identified with the block LPF_v to mitigate the switching noise. For this filter the band is set to 4 kHz, one fifth of the switching frequency.

Generation of V_s^2 Reference Signal Γ

Based on the circuit in Fig2.2, the control philosophy can be analyzed as follows. The voltage on the DC bus, and therefore on the capacitor C, can be defined as (2.5).

$$\dot{V_{dc}} = \frac{d}{dt} V_{dc} = \frac{i_C}{C} = \frac{1}{C} (i - i_p) \tag{2.5}$$

By considering ideal the bidirectional converter, and so neglecting the losses within it, the power balance between the two side can be expressed as:

$$i_p \, V_{dc} = i_s \, V_s \tag{2.6}$$

Hence

$$\frac{d}{dt} V_s^2 = 2V_s \, \dot{V}_s = 2V_s \, \frac{i_s}{C_s} = \frac{2}{C_s} \, V_{dc} \, i_p \tag{2.7}$$

By expressing (2.7) in the frequency domain, the top branch of the block schemed is obtained as (2.8).

$$V_s^2 = \frac{2}{sC_s} \, V_{dc} \, i_p \tag{2.8}$$

In practical implementation the value of V_s is measured and squared in the control code.

Since we're trying to obtain a capacitance multiplier, with equivalent capacitance equals to $(1 + k)C$, we would like to share the ripple current from the DC bus between the passive capacitor and the bidirectional converter as shown in (2.9).

$$i_p = k\ i_c \tag{2.9}$$

Combining (2.9) and (2.5), we get

$$C_s \frac{d}{dt} V_s^2 = k\ C \frac{d}{dt} V_{dc}^2 \tag{2.10}$$

which, solved with indefinite integrals, returns

$$V_s^2 = k \frac{C}{C_s} V_{dc}^2 + const \tag{2.11}$$

This relationship between V_s^2 and V_{dc}^2 highlights how the two voltages oscillate in synchronous manner, but with different amplitude and offset. Using (2.11) and knowing V_{dc}^2, the reference signal for V_s^2 can be computed. At this point it is necessary to work on the gain k which must be frequency dependant and have the following characteristics:

- For very low frequency values it must be small, to ensure that the converter does not go out of the preset working range $[V_{s_{min}}, V_{s_{max}}]$.
- Must be very high, about 25 times compared to that in low frequency, in the frequency range in which it is expected to have to filter the ripple.
- Must have a phase of about -90 electrical degrees for the input impedance, in the frequency range of interest, to have a behaviour comparable to a capacitor.

To meet these requests, a lead-lag transfer function is proposed in [18] and has been used as a starting point for this thesis. The transfer function is shown in (2.12).

$$G(s) = a\ \frac{c^3 \tau s + 1}{c^2 \tau s + 1}\ \frac{c\tau s + 1}{\tau s + 1} \tag{2.12}$$

Basically, it's a second order lead-lag that reflects the characteristics of a first order one as regards the gain at high and low frequencies, but has a more attenuated, although longer, transient in the phase change. The first order counterpart could be defined as:

$$G^I(s) = a\,\frac{b\tau s + 1}{\tau s + 1} \tag{2.13}$$

The transient difference between (2.13) and (2.12) is shown inFig.2.6.

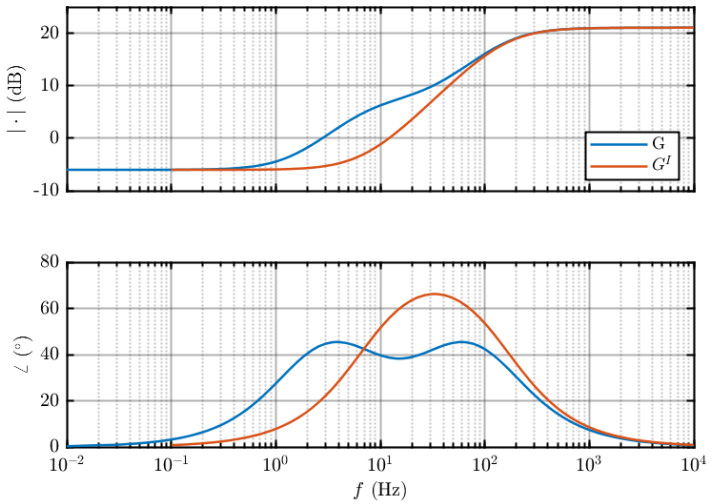


Figure 2.6: Comparison between regulator G in its first order form (red) and the second order form (blue) used in the control.

For DC values the average value of the signal Γ will be a times the average value of the square of the bus voltage V_{dc}^2, while for the frequencies of interest the gain will be equal to ab, with $b = c^2$ and b approximately equal to 30. In an optimal situation, where there is no bottleneck on the bandwidth caused by the switching frequency, a should be set to make V_s oscillate around the midpoint value of the voltage range, to maximize the ripple amplitude of voltage on the buffer capacitor and therefore the energy transferred. The optimal value of a can be computed as

$$a = \frac{1}{V_{dc}}\,\frac{V_{s_{min}} + V_{s_{max}}}{2} \tag{2.14}$$

With the values of $V_{s_{min}}$ and $V_{s_{max}}$ established before, the optimal working point would be 0.6125. In practice, as will be shown in the next chapter, the limits due to the switching frequency have forced us to keep a lower value to avoid control instability. The poles

of the transfer function are defined by the value τ that must be chosen so that $1/\tau$ is the starting point of the range of interest for the ripple frequency, in rad/s.

Energy Control Loop

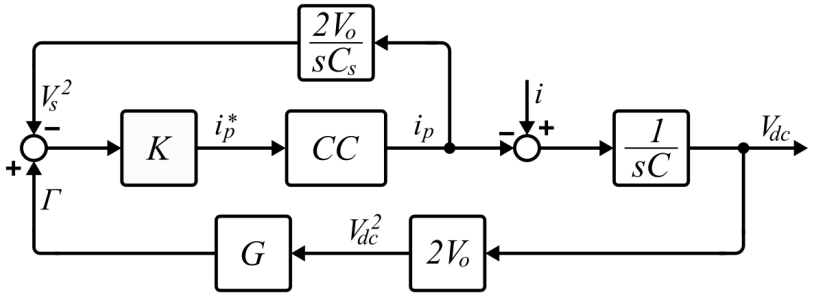


Figure 2.7: Small signal diagram of the active capacitor, linearized around the equilibrium voltage V_0.

Whit the reference signal Γ, an energy controller K can be designed for the stored energy, represented by the signal V_s^2, with the reference current i_p^* as its output. Given V_0 as the equilibrium point of V_{dc}, by using (2.7) the transfer function between i_p and V_s^2 can be derived as (2.15).

$$\frac{\hat{V}_s^2}{\hat{i}_p} = \frac{2\,V_0}{s\,C_s} \tag{2.15}$$

Also in this case the current controller together with the converter are represented with a CC block. For this controller a proportional gain K could be used to track the reference Γ, but with higher K, and therefore higher bandwidth, the system may be more prone to instability.

For this purpose, another lead-lag controller is presented in [18] and reported in (2.16).

$$K(s) = K_0 \frac{1 + \epsilon\theta s}{1 + \theta s} \tag{2.16}$$

Where ϵ is the factor by which the loop gain at high frequencies is decreased, so it must

be less than one, and θ is chosen so that $1/\theta$ in in the frequency range of interest (in rad/s).

Along with the proposed controller, a PI controller has been designed, and the performance differences will be examined in the simulation chapter.

CCM Current Control

Control the current in CCM is a closed loop approach for which the controller needs a feedback signal from the inductor current. The current must be sensed in a synchronous way with respect to the positive (or negative) peaks of the PWM carrier wave, so that the sensed value is the moving average of the current. This process is obtained thanks to the Interrupt Service Routine (ISR), a signal that trigger the code on the microprocessor to run at each rising edge of the square wave,which is synchronized with the carrier's triangular wave.

As seen in the previous subsection, the energy control loop has the reference signal for i_p at the output, while the current that we want to control is i_s. To overcome this problem, the reference current i_s^* is calculated considering the bidirectional converter as an ideal circuit. The power balance between the two sides of the switches will therefore be

$$V_{dc} i_p = V_s i_s \tag{2.17}$$

Hence

$$i_s^* = i_p^* \frac{V_{dc}}{V_s} \tag{2.18}$$

The difference between the reference signal obtained with (2.18) and the current feedback is fed to a PI controller, whose parameter has been calculated as follow.

Considering the switch frequency it is possible to place the pole of the converter at $1/\tau_d \cong 13\ kHz$ using (2.4). A good practice is to place the bandwidth of the current loop (f_{BW_i}) at least a decade lower than the converter pole. The value of $f_{BW_i} = 1kHz$ has been chosen to keep some margin. The computation of the K_{p_i} and K_{i_i} terms follow

the same principle examined in (1.20) and (1.22), but in this case the crossover frequency locations depends on L_s. The formulas are reported in (2.19) and (2.20).

$$K_{p_i} = 2\pi f_{BW_i} L_s \tag{2.19}$$

$$K_{i_i} = \frac{2\pi f_{BW_i}}{5} K_{p_i} \tag{2.20}$$

Again, the $1/5$ term is for a better phase margin.

The duty signal is then generated by normalizing the controller output on the value of the voltage on the DC bus and, after a saturation between 0 and 1, it is sent in output to the modulator.

DCM Current Control

Working in DCM means that the inductor is only used as energy transfer component, therefore no energy is left stored in it at the end of the switching period, hence the current goes to zero as shown in Fig.2.8.

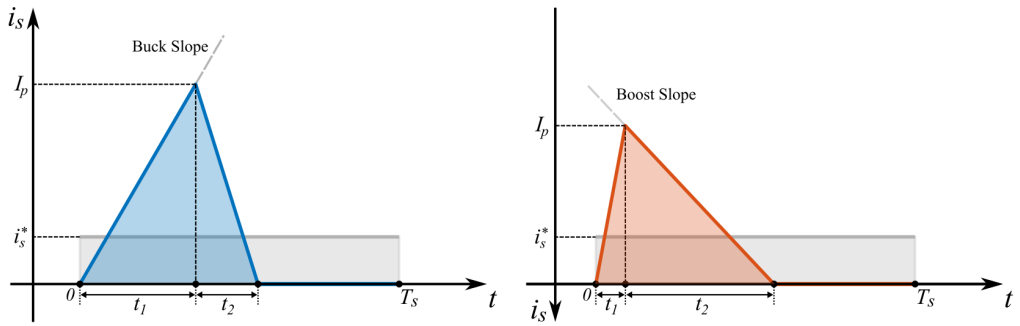


Figure 2.8: Buck charging (left) and boost discharging (right) duty-cycle generation strategy.

This is an open-loop approach where the bidirectional switching cell is driven as a buck or a boost depending on whether the buffer capacitor needs to be charged or discharged. The working phases depend on the current reference i_p^* and the voltage on the buffer capacitor V_s:

- $V_s < V_{s_{min}}$: the converter works in precharge mode with a duty equal to D_{pre}, see (2.2).
- $V_s \in [V_{s_{min}}, V_{s_{max}}]$ and $i_p^* > 0$: The converter has to work in buck mode, only the upper switch is modulated, the lower one is always OFF and the body diode works as freewheeling.
- $V_s \in [V_{s_{min}}, V_{s_{max}}]$ and $i_p^* < 0$: The converter has to work in boost mode, the lower switch is modulated and the higher one's body diode is used as freewheeling.
- $V_s > V_{s_{max}}$: situation of overcharge for the buffer capacitor, both switches are OFF.

Defined Q_{pulse} the charge flowing through the current i_s in a period, represented in Fig.2.8 as the blue area in the buck phase and the red area in the boost phase, the goal of the regulator is to make sure that Q_{pulse} is equal to the charge corresponding to the reference current i_s^* multiplied by a switching period T_s, graphically represented as the grey area. From a geometric approach we can then derive the duty.

In the hypothesis of a switching frequency much higher than the one of i_p^*, during a switching period it is possible to consider the bus voltage and that on the buffer capacitor constant. This allows us to consider, with excellent approximation, the trend of the charge and discharge of the inductor as linear, with a constant slope according to the working phase. By defining the slopes as S_{bk} and S_{bt}, respectively for the buck (bk) and boost (bt) phase, these can be calculated as:

$$S_{bk} = \frac{V_{dc} - V_s}{L_s} = \frac{I_{p_{bk}}}{t_{1_{bk}}} \tag{2.21}$$

$$S_{bt} = \frac{V_s}{Ls} = \frac{I_{p_{bt}}}{t_{2_{bt}}} \tag{2.22}$$

where I_p is the maximum value, in absolute terms, assumed by the current in a switching period T_s. According to the control aim, the area of the triangle must be equal to the average value of i_s multiplied to the switching period.

$$\frac{1}{2}(t_1 + t_2)I_p = \bar{i}_s T_s \tag{2.23}$$

From (2.21) and (2.22) we can express the relationship between the time intervals t_1 and t_2 for buck and boost phase respectively as:

$$t_{2_{bk}} = \frac{S_{bk}}{S_{bt}} = \frac{V_{dc} - V_s}{V_s}\, t_{1_{bk}} \tag{2.24}$$

$$t_{2_{bt}} = \frac{S_{bt}}{S_{bk}} = \frac{V_s}{V_{dc} - V_s}\, t_{1_{bt}} \tag{2.25}$$

The area of the triangles equal to Q_{pulse} can then be defined as (2.26) and (2.27).

$$Q_{pulse_{bk}} = i_s^*\, T_s = \frac{1}{2}\, t_{1_{bk}}^2\, \frac{V_s L}{V_{dc}(V_{dc} - Vs)} \tag{2.26}$$

$$Q_{pulse_{bt}} = i_s^*\, T_s = \frac{1}{2}\, t_{1_{bt}}^2\, \frac{(V_{dc} - V_s)L}{V_{dc} V_s} \tag{2.27}$$

By applying the duty cycle definition, $d = t_1/T_s$, and the converter power balance principle defined in (2.18), the duty signal for each working condition can be computed.

$$d_{bk} = \sqrt{\frac{2L\, i_p^*}{(V_{dc} - V_s)\, T_s}} \tag{2.28}$$

$$d_{bt} = \sqrt{\frac{2L(V_{dc} - V_s)\, |i_p^*|}{V_s^2\, T_s}} \tag{2.29}$$

To adapt this control at the modulator shown in Fig.3.13 some adjustments have to be made. The signal EN, used to enable the PWM, is now replaced by two new signals, EN_H and EN_L, that enable respectively the high switch when $i_p^* > 0$ and the low switch when $i_p^* < 0$. since the signal for the low switch is inverted by a NOT gate, the signal d_{bt} is substituted with its complement to one. A summary of the current control is provided below in table 2.1.

TABLE 2.1: DCM CURRENT CONTROL SIGNALS.

Working phase	**d**	**EN_H**	**EN_L**
$V_s < V_{s_{min}}$	D_{pre}	1	1
$V_s \in [V_{s_{min}}, V_{s_{max}}]$ and $i_p^* > 0$	d_{bk}	1	0
$V_s \in [V_{s_{min}}, V_{s_{max}}]$ and $i_p^* < 0$	$(1 - d_{bt})$	0	1
$V_s > V_{s_{min}}$	0	0	0

Startup Process and Load Variation

To maximize the performance of the active capacitor in steady state, the proportional gains of regulators G and K must be sufficiently high. However, this can create problems under certain conditions, in particular during startup process on a DC bus with no load and during load variation.

To overcome the first problem, the control is started with the regulators gains reduced to 20% of their nominal value, to ensure a soft start. After the system reaches equilibrium, i.e. the bus voltage remains in a sufficiently small range around the reference value for a certain time decided in the design phase, the gains nominal values are restored.

Sudden changes in the load, on the other hand, can cause oscillations in the DC value of V_s^2, possibly leading V_s to hit the upper or lower limit of its working range [$V_{s_{min}}$,$V_{s_{max}}$]. This situation can be avoided by reducing the gain for high frequency in $G(s)$, but the low frequency gain must stay the same. A block diagram is proposed in Fig.2.9.

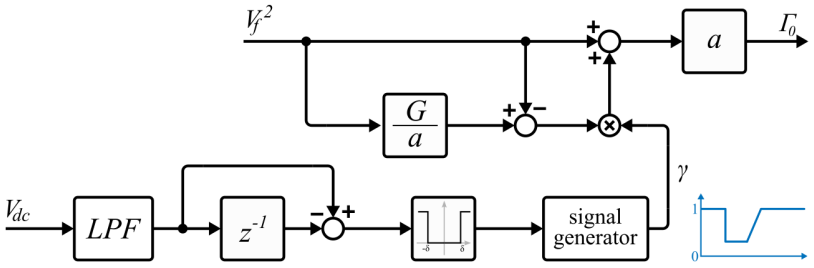


Figure 2.9: Block diagram of the load variation protection.

To detect a load variation a Continuous Moving Average filter is used to extract the voltage mean value on the DC bus: if two consecutive sensed values have a sufficiently

large difference ($|V_{dc_k} - V_{dc_{k-1}}| > \delta$), the control is triggered into a more damped mode in which the high frequency gain of $G(S)$ is reduced to a quarter of it's initial value until the end of the transient, then is slowly restored. In this way the system remains stable and oscillations on V_{dc} and V_s during the transient are avoided, at the price of worse operating condition, hence higher ripple on the DC bus, for a short amount of time. From the block diagram in Fig.2.9 we can see how the reference Γ_0 is computed as:

$$\Gamma_0 = a\left(V_f^2 + \gamma(V_f^2 G(s)/a - V_f^2)\right) \tag{2.30}$$

So that when $\gamma = 1$ we have $\Gamma_0 = \Gamma$, and for $\gamma < 1$ only the response of the high frequencies is damped.

2.3 Sizing of the components

2.3.1 Sizing of the Buffer Capacitor C_s

In the paragraph concerning the dimensioning of the DC Link for the PFC, the total energy of the current ripple (1.14) has been obtained. If our goal were to store this energy exclusively, regardless of the application, the current and voltage of the necessary capacitor could be obtained with the following equations.

Suppose the ripple power going into the capacitor is expressed like

$$P_r = \hat{P}_r \sin(2\omega t) \tag{2.31}$$

By calling V_s the voltage across the capacitor, on the basis of the power equilibrium relationship, it is possible to derive the following differential equation.

$$\frac{dV_s^2}{dt} = \frac{2\hat{P}_r}{C_s}\sin(2\omega t) \tag{2.32}$$

V_s can then be derived by solving (2.32), obtaining

$$V_s = \sqrt{\frac{\hat{P}_r}{C_s\omega}(k - \cos(2\omega t))} \tag{2.33}$$

Where $k = (V_{s_{max}} C_s \omega / \hat{P}_r) - 1$, with $k \geq 1$. The low frequency capacitor current can be then expressed as

$$i_s = \frac{\hat{P}_r \sin(2\omega t)}{\sqrt{(\hat{P}_r / C_s\omega)(k - \cos(2\omega t))}} \tag{2.34}$$

Comparing (2.33) with the maximum energy that C_s is capable to store, $E_{C_s,max} = 0.5 C_s V_{s_{max}}^2$, we can also define k as:

$$\frac{k+1}{2} = \frac{E_{C_s,max}}{Er} \tag{2.35}$$

In this context we can define k as the energy storage margin coefficient: the higher is k, the more unused energy is stored in the system. For $k = 1$ the maximum energy storable in the capacitor is equal to the total energy ripple. With a standard setup like the one examined in subsection 1.2.1 we get

$$E_{C_{bus},max} = 128\ J$$

$$E_r = 10.51\ J$$

By applying (2.35) we get the coefficient $k \approx 23$, meaning that more of the 90% of the energy stored in the buffer capacitor is redundant.

Although $k = 1$ may seem the most efficient solution in terms of power density, since we have the complete charge and discharge of the capacitor from zero to the maximum value of V_s, this situation leads to highly distorted current, with the highest peak and RMS values, as shown in the graph in Fig.2.10.

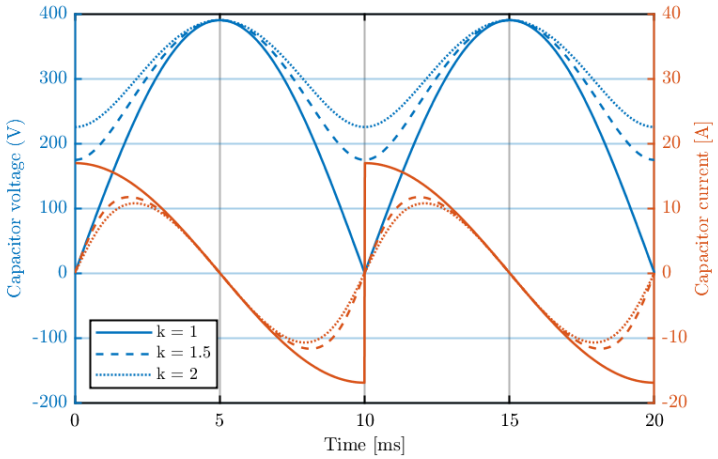


Figure 2.10: Capacitor voltage and current for different values of k.

Here, the behaviour of voltage and current are displayed for different values of k, with a fixed maximum voltage, so that to every iteration corresponds a different capacitance. From this graph we can see how by increasing the value of the coefficient k both voltage and current assume a more sinusoidal trend, aiming to a pure second harmonic. That is because with high energy storage capability, the ripple energy term from the filter inductor become more and more negligible. Also, for higher k, the capacitor current decreases, and consequently the voltage ripple.

As mentioned previous chapter, given a certain voltage rating, the capacitance and current rating are the two major factors that influence the selection of capacitors. Even though there are control techniques that use higher voltages on the buffer capacitor with the aim of increasing its filtering effect, in this elaborate it has been preferred to opt for solutions that do not involve dealing with voltages larger than the DC bus voltage. Knowing therefore that the theoretical maximum voltage on C_s is equal to V_{dc}, the minimum necessary capacitance can be computed as 130 μF using (2.36).

$$C_s = \frac{2\hat{P}_r}{V_{dc}^2 \omega} \tag{2.36}$$

This is the theoretical minimum, with $k = 1$. However this would result in higher and distorted current, coupled with the fact that a complete charge and discharge of the buffer capacitor would be much more complex to control than a sinusoidal ripple. To leave some

margin, a more relaxed choice of $k = 2$ has been made. We also mentioned in the previous subsection that, in order for the control to work properly, the active capacitor maximum voltage must be lower than the bus voltage. Using $V_{s_{max}} = 390\ V$, and rearranging (2.35), a more realistic value of C_s can be computed using (2.37).

$$C_s = \frac{(k+1)E_r}{V_{s_{max}}^2} \tag{2.37}$$

The computed capacitance is equal to 208 μF. Choosing the nearest commercial value of 200 μF we obtain a coefficient $k = 1.89$, meaning that with optimal control techniques we could obtain equal filtering performance with a capacitor 8 times smaller.

The trade-off with this reduction of the DC capacitance is, as we already mentioned, the increase in the peak and RMS values of the current. The latter can be computed as expressed in (2.38).

$$i_{s,RMS} = \sqrt{\frac{\omega}{\pi}\int_0^{\pi/\omega}\left(\frac{\hat{P}_r \sin(2\omega t)}{\sqrt{(\hat{P}_r/C_s\omega)(k-\cos(2\omega t))}}\right)^2 dx} \tag{2.38}$$

The calculated value is $i_{s,RMS} = 7.69A$, which is about a 31% increase over the current a normal DC link would draw, with a peak value of approximatively 11 A.

2.3.2 Sizing of the Auxiliary Inductor L_s

When sizing an inductor in a power converter, it is necessary to consider the possibility of working in Continuous Conduction Mode or Discontinuous Conduction Mode. These terms refer to whether the current in the energy storage element (inductor) goes to zero each switching cycle or not. In CCM it does not reach zero so at the end of every switching cycle there is some energy left which is then topped up in the next cycle to provide enough energy for the output. In DCM, all the energy is used each cycle and the inductor sits with no current and no stored energy for part of the time. Obviously, the stored energy relates to the load, so if a converter is designed to work in CCM at nominal power, it will shift to DCM with lighter loads, while if the converter is designed to work in DCM at maximum loads, it will always operate in DCM.

Both working methods have their pros and cons: for example, from a power density perspective, a DCM control would be preferable as it requires a smaller inductance value, and possibly less space for the inductor, and being an open loop control no sensors are required to measure current. On the other hand, however, because DCM charges and discharges the inductor completely, the primary current ripple is logically much greater than in CCM, especially in heavier loads, requiring higher values in switches and rectifier diodes maximum current. This current ripple also generates a variating signal, which is then propagated due to the antenna-like behaviour of the different components in the primary current loop, generating significant levels of Electro-Magnetic Interference (EMI), that would not be a problem in CCM.

Inductor for DCM Operation

As seen in Fig.2.8, in order to stay in DCM mode, the condition $t_1 + t_2 < T_s$ must be satisfied. Combining (2.21) and (2.22) in (2.23), the auxiliary inductor limits for DCM application can be set as

$$L_s \leq \frac{T_s}{2\bar{i}_s} \frac{V_{dc}V_s - V_s^2}{V_{dc}} \tag{2.39}$$

Equation (2.39) highlights how, for a certain switching frequency, the inductance has a maximum value to make sure the circuit works in DCM.

At the same time, since the auxiliary circuit has one phase leg, a maximum current rating requirement (I_{peak})is needed to protect the switch. As shown in Fig.2.8, the peak current value in the buck charging phase and boost discharging phase can be expressed as

$$I_p = S_{bk}t_2 \leq I_{peak} \tag{2.40}$$

$$I_p = S_{bt}t_1 \leq I_{peak} \tag{2.41}$$

To make sure the peak current is lower than the requirement, the auxiliary inductance needs to be bigger than a certain value, described by the following inequality

$$L_s \geq 2\frac{\bar{i}_s T_s}{I_{peak}^2}\frac{V_{dc}V_s - V_s^2}{V_{dc}} \tag{2.42}$$

By combining (2.39) and (2.42), the auxiliary induction range is plotted in fig. 2.11.

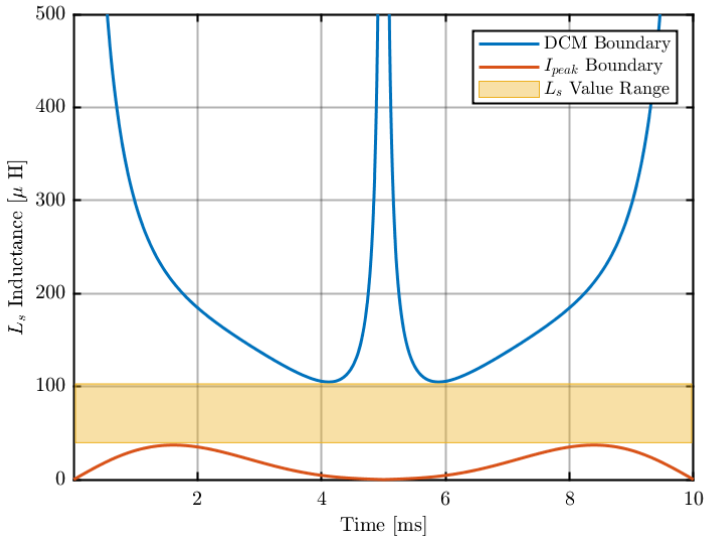


Figure 2.11: Boundaries for the sizing of L_s.

For DCM application the selected inductance is 68 μH, with a switching frequency of 20 kHz and a peak current of 50 A.

Inductor for CCM Operation

Working in DCM requires a higher value inductance than in CCM control as part of the energy is also stored in the inductor, which is no longer just a component dedicated to energy transfer. This type of control also requires a feedback on the inductor current, which must be sampled in a synchronous manner with respect to the peaks of the PWM carrier in order to always obtain the moving average value in the switching period. This synchronism is achieved through the Interrupt Service Routine (ISR).

The inductor current has two components in CCM, the first one which follows the reference current generated by the outer loops, and a second one in a form of a ripple current, that depends on the input and output voltage of the converter (V_{in} and V_{out}), the

switching period (T_s), the duty cycle (d) and the inductance value (L_s). The peak-to-peak current ripple definition varies according to the buck or boost operation of the converter and is respectively expressed as (2.43) and (2.44).

$$\Delta i_L = \frac{1}{L_s} \left(V_{in} - V_{out}\right) \left(d\ T_s\right) \tag{2.43}$$

$$\Delta i_L = \frac{1}{L_s} \left(V_{in} - V_{out}\right) \left[(1 - d)\ T_s\right] \tag{2.44}$$

For both cases, the maximum value of Δi_L is obtained with $d = 0.5$. Using this condition for a more conservative approach, the formula can be rewritten as

$$L_s = \frac{1}{i_{s,max}\ \Delta i_{L\%}} \left(V_{in} - V_{out}\right) \left(0.5\ T_s\right) \tag{2.45}$$

With an educated guess on the difference between V_{in} and V_{out}, by imposing $\Delta i_{L\%} = 5\%$ the auxiliary inductance can be computed as 5.6 mH with a switching frequency of 20 kHz.

2.4 Power Switches Thermal Analysis

In the outlook of a prototype, a semiconductor selection and a thermal design has been performed. Knowing the stresses on the devices and knowing that a higher switching frequency could allows us to improve the performance of the control strategy, the optimal choice for power switches turned out to be Silicon Carbide (SiC) MOSFETs.

Silicon carbide, a semiconductor compound consisting of silicon (Si) and carbon (C), belongs to the Wide BandGap (WBG) family of materials and has emerged as the most viable candidate for next-generation, low-loss semiconductors due to its low ON resistance and their low reverse recovery, which contribute to significantly lower energy consumption, and superior high-temperature, high-frequency, and high-voltage performance when compared to silicon.

The steps taken for this analysis will be shown in the next sections, from the choice of the semiconductors up to the sizing of the heatsink.

2.4.1 Choice of the Semiconductor

To size the semiconductors we must consider the maximum voltage and current to which they are subjected. Referring to the circuit shown in Fig.2.2 we can see that the maximum voltage applied to the switch is the DC bus one, equal to 400 V, while the current for CCM application is equal to the one calculated for the buffer capacitor with 2.38, $I_{cs} = 7.69\ A_{RMS}$.

For a reliable sizing, it's important to take in account overvoltages due to to parasitic phenomena and/or failures, therefore devices with a maximum sustainable voltage of about 650V are chosen. For what concerns the current, working at this power rating permits us to choose power switches with a Drain-Source ON state resistance relatively high, which gives us a good compromise between costs and losses.

Based on the above, the most eligible power switch for this device turned out to be the C3M0120065K by Wolfspeed, a SiC N-Channel Ehnancement MOSFET with high blocking voltage (650 V) with low ON resistance (120 $m\Omega$), high-speed switching with low capacitances, fast body diode with low reverse recovery and a maximum rated current equal to 22 A @25° C. [19]

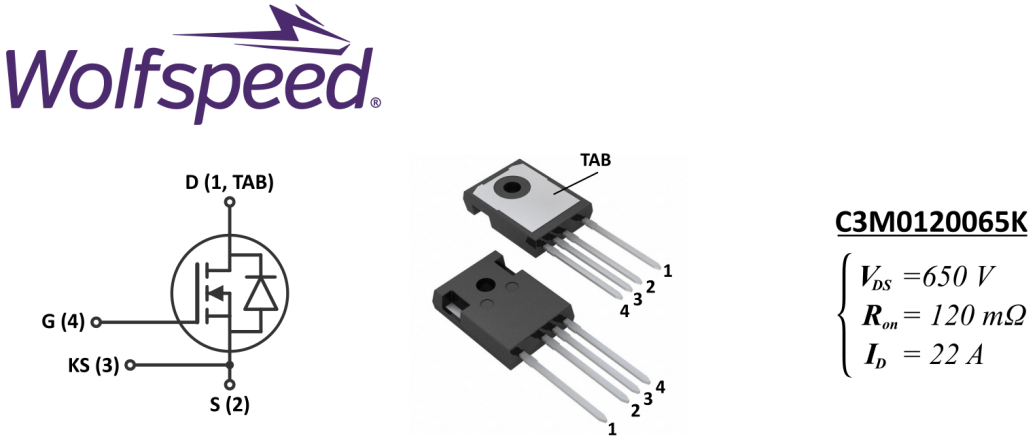


Figure 2.12: MOSFET C3M0120065K by Wolfspeed.

This device is offered in a TO-247-4 package, where the last 4 in the code indicates the presence of a Kelvin Source pin. Its task is to decouple the power source pin from the signal source pin. The advantage is that the inductive voltage drop related to the switched current is not seen on the gate circuit. The result is an improved switching performance, which is what is needed in this kind of application (higher possible switching frequency). Moreover, due to its size, this package offers optimal thermal resistance, which allows for easy heat dissipation.

2.4.2 Power Switches Losses and Thermal Modelling

During the design phase, the thermal simulation is a very important tool as it allows to calculate the dissipated power of the converter in order to guarantee a correct sizing of dissipation and/or cooling systems and find the right compromise between cost, size, circuit complexity and control.

In general, a device is designed to have high reliability, meaning that it must have a low incidence of failure and to ensure the expected functional characteristics for its entire life. The reliability of the component is related to the operating temperature: the higher the temperature, the lower the reliability, since excessive thermal stress can cause expansions and/or contraptions that could cause the connections between die and external pins to break. Consequently, the manufacturer provides the maximum operating temperature which represents the upper extreme of the correct functioning of the device.

More specifically, it must be ensured that the temperature at the hottest point of the component is lower than the maximum temperature indicated by the manufacturer: in the MOSFET it is located in the channel region (between terminals D and S). In the discussion of the thermal model, this temperature will be referenced as the junction temperature T_j. For the chosen device, the maximum junction temperature indicated by the manufacturer is equal to $T_j^{MAX} = 175°C$.

Power components dissipate due to their non-idealities. Losses can be caused by the intrinsic ohmic resistance of the component during the on state (conduction losses) and by non-linear parasitic phenomena during the change of state (switching losses). The dissipated power is equal to $P_d = P_{cond} + P_{sw}$, where

$$P_{cond} = R_{DS,on} I^2_{D,RMS} \tag{2.46}$$

and

$$P_{sw} = (E_{on} + E_{off}) f_{sw} \tag{2.47}$$

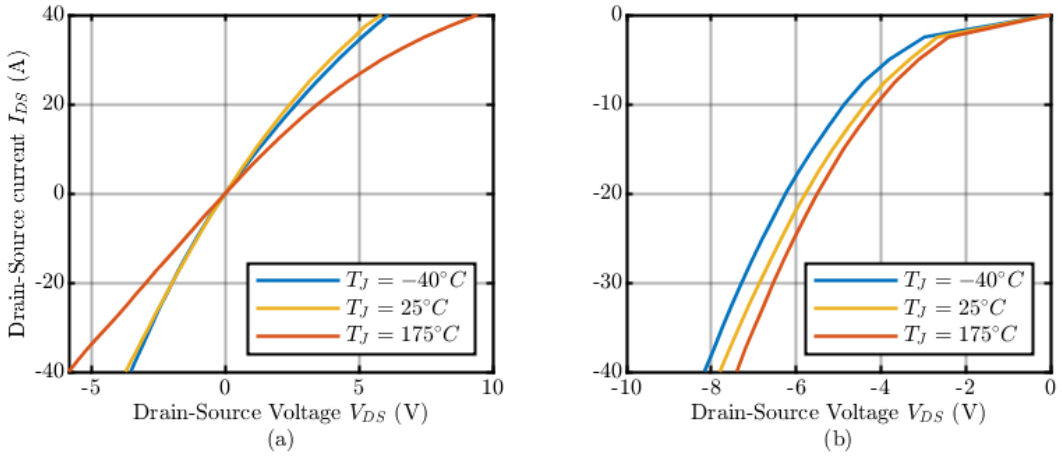


Figure 2.13: Conduction losses for the chosen MOSFET: in (a) are plotted the losses for $V_{GS} = 15V$ (switch ON), in (b) are plotted the losses for $V_{GS} = -4V$ (switch OFF, body diode losses).

The power dissipated in conduction by the MOSFET can be calculated by knowing the quantities of voltage and current during the on state through the conduction curves provided by the manufacturer. On the datasheet [19] it is possible to find the trend of the conduction characteristics for different control voltages of the MOSFET V_{GS} (Fig,2.13): in our situation, the component is controlled at a voltage $V_{GS} = 15\ V$ for turn-on and at a voltage $V_{GS} = -4\ V$ for turn-off.

As for the conduction losses, for the switching losses we can find on the datasheet the values of the necessary energy for the commutation. As suggested by the datasheet, an external gate resistance $R_{G(ext)} = 10\ \Omega$ will be considered to limit noise and ringing in the gate drive path.

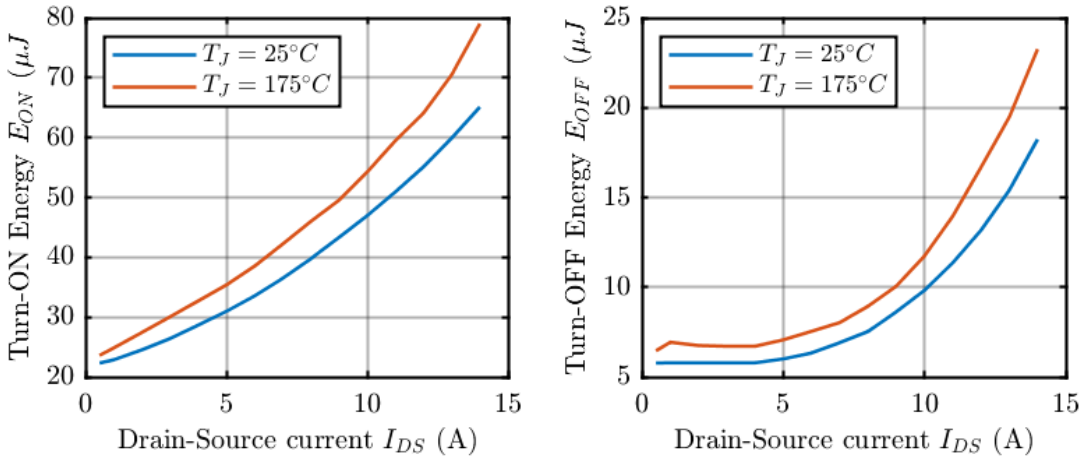


Figure 2.14: Energy loss during commutation.

The sum of conduction and switching losses will be the input for our thermal circuit.

Thermal Circuit

To build the thermal circuit, it is necessary to know how many and which semiconductors will be used for the converter, how they will be mounted on the heat sink and what the external environment, with which the latter will exchange heat, will be. Assuming the external environment as isothermal at a temperature of $T_a = 25°C$, and considering each individual element of the system as an isothermal one, the structure of the switches mounted on the heat sink can be schematized as in Fig.2.15.

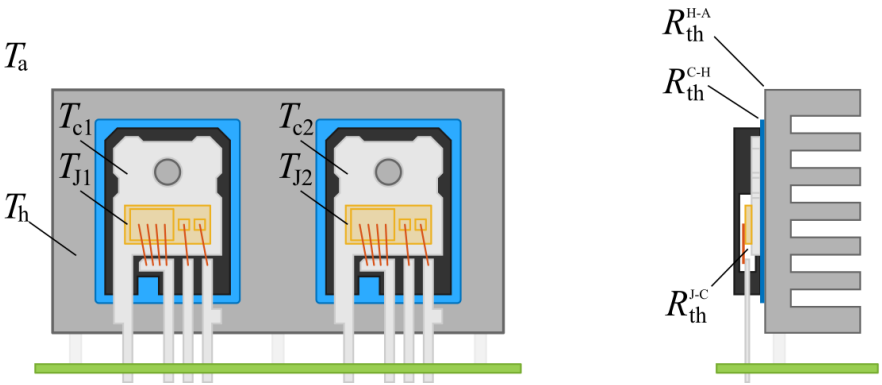


Figure 2.15: Schematized structure of the switches mounted on the heatsink: in the frontal view (left) the temperature of the components are highlighted while, in the side view, the thermal resistances' physical counterpart are highlighted.

Where j indicates the junction, c indicates the switch case, h the heatsink and the environment is indicated with the letter a. From the image it can be seen how the use of a Thermal Interface Material (TIM) was taken into consideration for the setup, inserted between the power switches and the heatsink to improve the heat conduction and to electrically insulate the heatsink from the drain. From the setup in Fig.2.15 it is possible to build a thermal circuit of the converter using the electrical analogy shown in Table 2.2.

TABLE 2.2: ANALOGY BETWEEN ELECTRICAL CIRCUITS AND THERMAL PHENOMENA.

Electrical circuits		**Thermal phenomena**	
Voltage V	V	**Temperature** T	$°C$
Current I	A	**Power loss** W	W
Electrical Resistance R	Ω	**Thermal Resistance** R_{th}	$°C/W$
Electrical Capacitance C	F	**Thermal Capacitance** C_{th}	$J/°C$

By considering that the contact between two neighbouring elements is characterized by thermal resistance and that each element, given its mass, has the ability to accumulate heat and store it in its thermal capacity, the equivalent electrical model of the system con be built as shown in Fig.2.16.

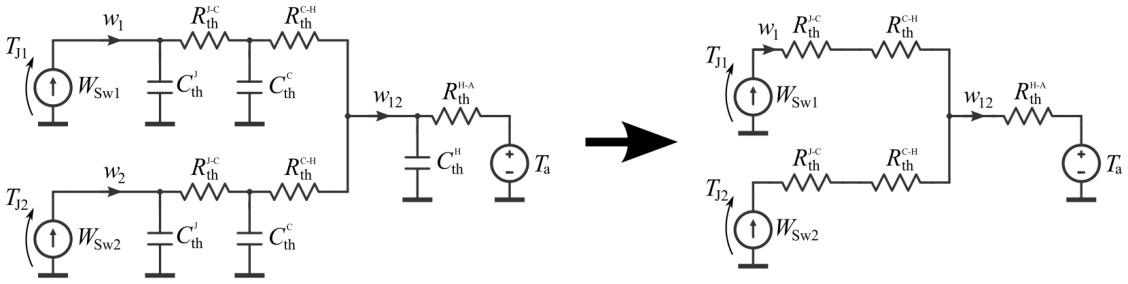


Figure 2.16: Thermal equivalent circuit for the converter setup. On the right, the simplified steady state model without the thermal capacitances.

Here, the junction's loss power to be dissipated on the heatsink is represented as a DC current generator and the isothermal environment, considering that it has infinite capacitance, like a voltage generator at the ambient temperature T_a. If a sufficiently long time passes, allowing the transients to run out, the thermal capacitances can be omitted

from the computation, thus obtaining a simplified circuit that can be used for sizing the thermal resistances (Fig.2.16, right).

Modelling of the Thermal Resistances

Starting from the innermost level, the thermal characteristic between the junction and the case is provided on the datasheet by the manufacturer, both in the form of resistance, useful for steady state evaluations such as sizing a heatsink, and as transient thermal impedance as shown in Fig.2.17, much useful to implement thermal model in simulation programs. The transient thermal impedance is a measure of how the device behaves when pulsed power is applied to it. This is important for determining the behaviour of low duty cycle, low frequency pulsed loads.

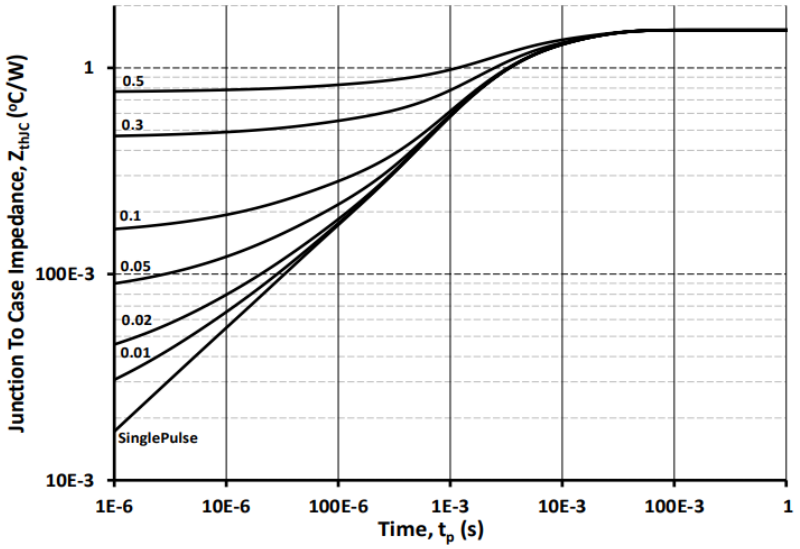


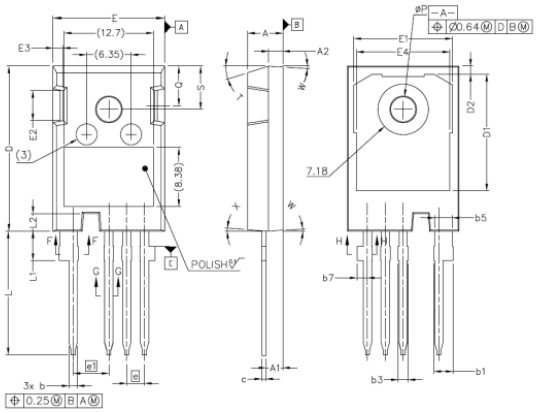
Figure 2.17: C3M0120065K Transient Thermal Impedance (Junction - Case).

Since the heatsink sizing is performed in steady state, for a conservative choice, the thermal resistance $R_{th}^{j-c} = 1.53\ °C/W$ will be used, which is the steady-state value of the thermal impedance.

The next step concerns the connection between the power switch case and the heatsink: since the component surfaces are not as smooth, but have some roughness, mounting the case on the heatsink creates air zones are that worsen thermal conductivity. To overcome this problem, a TIM in a thermal pad form is inserted between the case and the heatsink,

which improves the thermal coupling between the two components. A possibility is the HI-FLOW 300P from the Bergquist manufacturer [20]. It is a thermal pad made of a 55°C phase change polyamide compound. For a thickness of 25.4 μm it has a specific thermal impedance of 84 $°C \cdot mm^2/W$ at the mounting pressure of 1.7 bar (or 0.13 $°C \cdot in^2/W$ @25 psi).

To obtain the actual resistance of the thermal pad, it is necessary to calculate the contact area between the switch tab and the heatsink, referring to Fig.2.18.



SYM	MILLIMETERS	
	MIN	MAX
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b`	1.07	1.28
b	1.07	1.33
b1	2.39	2.94
b2	2.39	2.84
b3	1.07	1.60
b4	1.07	1.50
b5	2.39	2.69
b6	2.39	2.64
b7	1.30	1.70
c`	0.55	0.65
c	0.55	0.68
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13

SYM	MILLIMETERS	
	MIN	MAX
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
N*	4	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
Ø P	3.51	3.65
Q	5.49	6.00
S	6.04	6.30
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

Figure 2.18: C3M0120065K Package dimensions from the datasheet [19].

According to the nomenclature in the table in Fig.2.18, the useful area for heat transmission can be roughly calculated as:

$$A_{th}^{c-h} = D1 \cdot E4 - \pi \frac{7.18^2}{4} \approx 180\, mm^2 \tag{2.48}$$

Considering the specific thermal impedance and the area just calculated, the case-heatsink contact thermal resistance will be equal to $R_{th}^{c-h} = 0.47\ °C/W$.

The last thermal resistance concerns the sizing of the heatsink. Writing the KVL equation to the circuit mesh in Fig.2.16 and neglecting the capacitances, the resistance of the heatsink is directly related to the maximum temperature difference between the heatsink and the environment and the power to be dissipated according to the formula

$$R_{th,max}^{h-a} \leq \frac{T_{j,1} - T_a - (R_{th}^{j-c} + R_{th}^{c-h})w_1}{w_1 + w_2} \tag{2.49}$$

In this particular case the the high switch junction temperature is considered as the maximum limit ($T_{J,1}$) since, due to the typical duty cycle range of the converter, it tends to work more than the lower one and, therefore, to produce more losses in the form of heat.

For this fact, the loss values w_1 and w_2 were obtained through a simulative approach, by imposing a junction temperature equal to 150 $°C$ (precautionary choice with respect to $T_J^{max} = 150\ °C$) and measuring the power dissipated by the switches thanks to the PLECS thermal simulation tools. The values obtained correspond to $w_1 = 7.45\ W$ and $w_2 = 3.27\ W$.

Setting the ambient temperature equals to $T_a = 25\ °C$, from the (2.49) we obtain $R_{th}^{h-a} \leq 10.3\ K/W$.

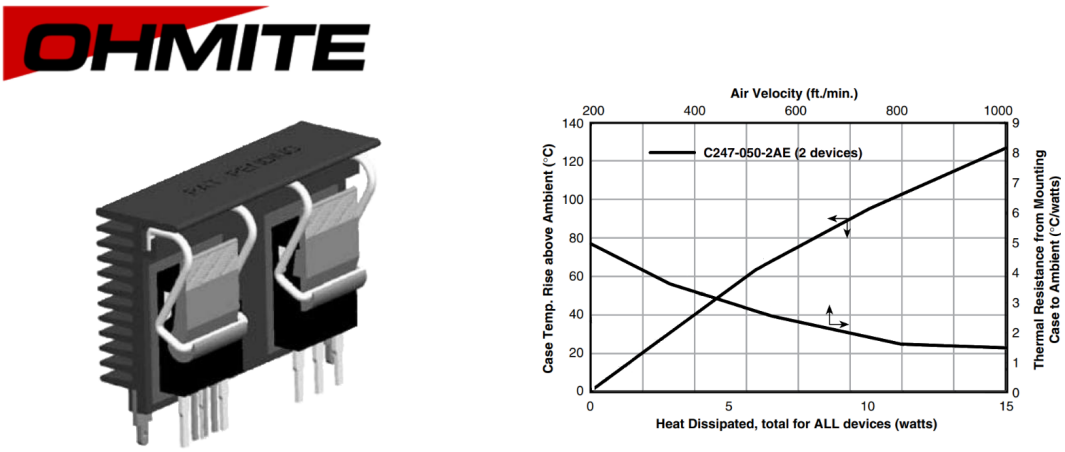


Figure 2.19: C247-050 Heatsink from Ohmite manufacturer.

The heatsink chosen is C247-050 from the Ohmite manufacturer [21]. It is a natural convection heatsink able to accommodate two integrated with TO247-4 package, with a thermal resistance equal to $R_{th}^{h-a} = 6.5\ °C/W$ @ 10W of heat dissipation. This analysis will be validated using PLECS in the Thermal Simulation subsection (3.2.3)

Chapter 3

Simulation Results

In the following chapter the analysis of the simulation results is performed. The simulations were conducted with PLECS, a software developed by Plexim, especially designed for power electronics application, with the possibility to model controls and different physical domains like thermal, magnetic and mechanical. MATLAB has also been used for the calculation addressed in the course of the thesis, for the post-processing of the data obtained through the simulations and for the generation of the plots. A brief introduction will be given regarding the modelling of the system for the simulation, then the results will be shown and commented.

System Modelling

Supply system (grid)

Under normal operating condition the grid can be modelled as a voltage source with sinusoidal waveform of amplitude V_g and frequency f_g. The instantaneous voltage is defined as:

$$v_g(t) = V_g \sin(\omega t) \tag{3.1}$$

where $\omega = 2\pi f_g$ is the electrical pulsation in rad/s and t is instantaneous time.

Equivalent grid impedance modelled with a resistor and an inductor in series with the sinusoidal voltage generator, with respective value $R_g = 150\ m\Omega$ and $L_g = 2.2\ mH$.

Passive elements

Inductor are modelled as linear inductances L. An arbitrary small series resistance is added to the auxiliary inductor L_s to prevent unwanted oscillation in the simulation, due to the absence of damping components. Similarly, capacitor are modelled with a pure capacitance C along with an Equivalent Series Resistance (ESR).

Semiconductor and power switches

Semiconductor switches, IGBT S and diode D are modelled as pure ON–OFF switches. No snubbers or non-idealities in the switches are modelled. More sophisticate model is implemented only for the thermal analysis on the active capacitor circuit.

Load

The simulated loads are modelled with controlled current source. Load variation are limited with a "Rate Limiter" block.

The control strategy is implemented through scripts in C programming language that can be inserted into the PLECS environment through the "C-script" block.

3.1 PFC Converter Simulation

The active front end PLECS model is shown in Fig.3.1.

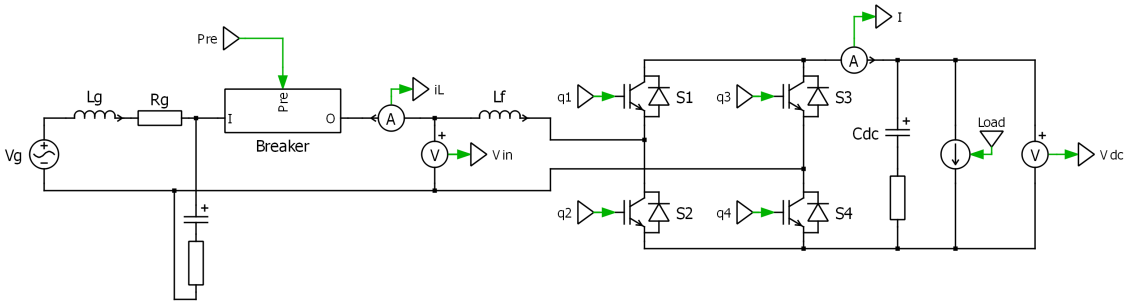


Figure 3.1: PLECS model of the active front end connected to the grid.

The measurement points necessary for the control are highlighted by an ammeter in series with the filter inductor on the AC side and by two voltmeters, one at the input to measure the mains voltage and one in parallel to the filter capacitor on the DC side to measure the bus voltage. The measurements collected from the circuit ideal blocks then pass through an analog conditioning subsystem where the signals are filtered by blocks of continuous transfer functions (Fig.3.2). In this case the only filtered signal is the filter inductor current i_L, as V_{in} is digitally filtered by the PLL and V_{dc} is digitally filtered by the Notch. The subscript f identifies the filtered output signals.

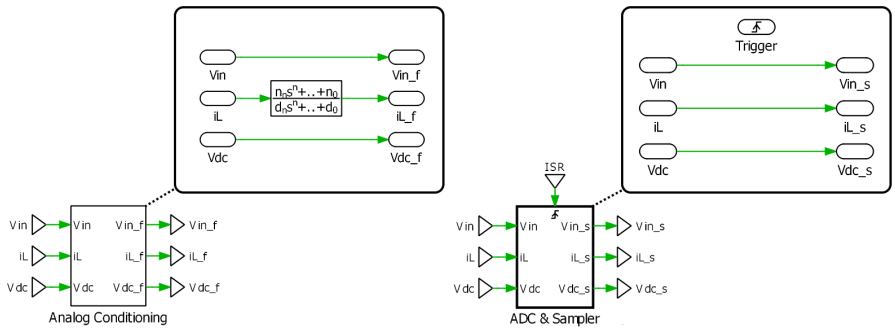


Figure 3.2: Subsystems in PLECS model for the analog conditioning of the measured values (left) and to simulate Analog to Digital Conversion (right), with the respective content.

In a similar way, the filtered signals are then sampled by a triggered subsystem, synchronously with the rising edge of the ISR in order to sample the moving average of the measured quantities. The output sampled signals, characterized by the subscript s, are then sent to the microcontroller block.

To represent the microcontroller in the way most similar to reality in PLECS it is necessary to use the "C-Script" block in which it is possible to write the control code in C language. Various input signals belong to this block:

- *Measured quantities*: these are the signals from the sensors used to acquire the measurements of the quantities useful for the control code: current and voltage on the AC side of phase (i_L and V_{in});
- *State machine hardware control signals*: these signals are used to simulate the control panel of the microcontroller that allows you to switch from one state to another within the state machine;
- *Trigger*: this signal consists of a train of pulses that defines the clock with which the microcontroller operates. From the theory of digital control it is considered that the triggers are in perfect synchronization with the triangular carrier waveform signal to which the PWM modulation refers

The output signals, on the other hand, consist of the quantities resulting from the processing of the code that must interface with the hardware part of the system. These consist of the duty-cycle signal (d) and the switching activation signals (EN), both delayed by one sampling step to simulate the output delay of the micro. It is also possible to have as an output any other quantity processed by the microcontroller which can be useful for monitoring the system, such as the working phase of the state machine and the references of the controllers, or the debugging of possible problems. The PLECS model of the micro is represented in Fig.3.3.

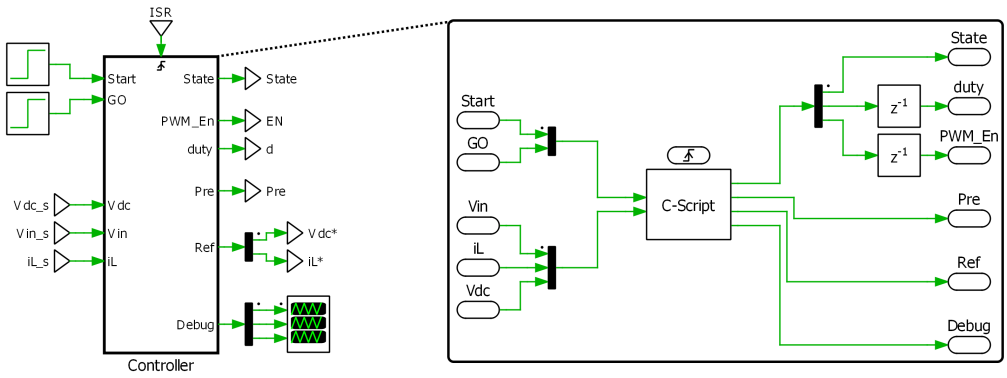


Figure 3.3: Realization in PLECS of the microcontroller.

The power switches' drive signals are obtained from the modulation block which receives the enabling signal and the duty cycle as input. The latter is compared to the triangular carrier in a comparator and the resulting signal is split so that each switching leg receives a signal and its inverted counterpart, thus avoiding short circuit on the converter leg. As shown in Fig.3.4, the vector containing the four switches' driving signals is multiplied by the enable signal (ON = 1, OFF = 0) and a dead time is also included to prevent one switch from start the ON commutation before the other on the same leg has finished the OFF. The output of the modulation block will be, therefore, the driving signals for the IGBTs and the ISR signal, also generated in this block.

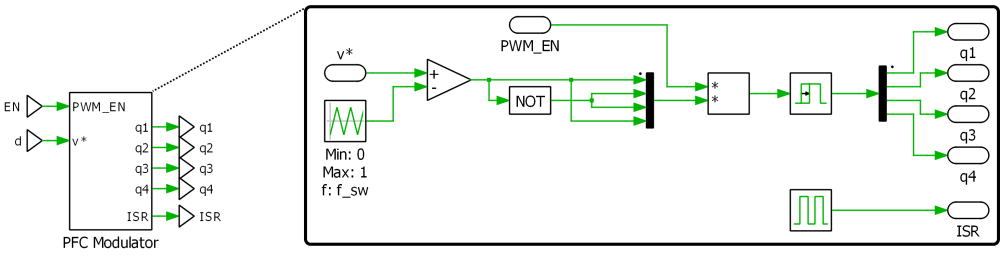


Figure 3.4: Realization in PLECS of the PWM modulator, along with the ISR signal generator.

3.1.1 PFC Control Code

The control code loaded in the "C-Script" block is executed every time it receives a pulse signal from the trigger. It is organized in two parts: the first part is always executed

and contains the commands relating to the reading of the inputs, the processing of quantities to be used for the control code, the application of digital filters and the verification of the system protection thresholds. This is a software protection that compares some quantities with limit values and if these values are exceeded by the measured quantities then the system goes into protection by disabling the converter switching. In particular, the quantities observed for the active front end are:

- $i_L < AC\_CRT\_MAX$: the system goes into protection if the instantaneous value of the measured phase current exceeds the threshold defined by the maximum value of the current sustainable by the converter.
- $V_{dc} < DC\_VLT\_MAX$: the system goes into protection if the instantaneous value of the voltage on the DC-bus exceeds the threshold defined by the limit value of the sustainable voltage on the DC-link

The second part of the code is represented in a state machine in which various sequential operations are carried out for each state, useful for the correct implementation of the control and management of the system by the user. The state machine consists of the following points:

- *ERROR*: it is the starting state of the system or the state it enters in case there are errors due to the activation of the protections (overcurrent in the phase or overvoltage on the DC bus). The modulation is disabled and the duty-cycles are reset, then the converter is deactivated by "turning off" the system. In this state, all the quantities used in the code are also reset to avoid any settings in the memory of previous activities. By pressing the "Start" button it is possible to go to the next state.
- *PRECHARGE*: in this state the DC-link is charged. The precharge relay closes and the converter works without modulation as a diode bridge. When the pre-set value of 320V is reached on the DC bus, it automatically continues in the following states.
- *READY*: in this state the enable signal is turned on and modulation begins. The duty signal is fixed at a constant value equal to 1.05 times the voltage read at the last switching period in the previous state. The control now waits for the GO signal to proceed to the next state.

- *GO*: this state contains the actual control illustrated in paragraph 1.2.2 and translated into C code. The voltage reference in given in a ramp form.

3.1.2 Preliminary Tests on the Active Front End

These preliminary tests were carried out to verify the correct functioning of the implemented models, the code and the control parameters of the PFC. The positive results obtained from the tests can be seen below. The parameters of the regulators are showned in table 3.1.

TABLE 3.1: PFC SIMULATION PARAMETERS.

Electrical parameters					
V_g	230	[V]	f_g	50	[Hz]
L_g	2	[mH]	R_g	0.15	[mΩ]
R_{pre}	15	[Ω]	L_f	2.2	[mH]
C_{dc}	1.6	[mF]	P_{out}	3.3	[kW]
Controller Parameters					
K_{PLL}	210		ω_{PLL}	$2\pi 50$	[rad/s]
K_{notch}	200		ω_{notch}	$2\pi 100$	[rad/s]
$K_{p,i}$	11.0584	[V/A]	$K_{r,i}$	100	[V/As]
$K_{p,v}$	0.8042	[A/V]	$K_{i,v}$	80.8518	[A/Vs]

PLL Operating Test

In this case we want to test the synchronization algorithm with the mains voltage. The response of the filter to a distorted mains voltage is also tested with the addition of a fifth harmonic $V_{g,5} = 0.1V_g$. In both cases the PLL is started at 0.01s.

As we can see in Fig.3.5 and Fig.3.6, the PLL has a good dynamics and manages to align itself with the mains voltage after about two periods. The filtering effect also works really well, as showned in the results in Fig.3.6.

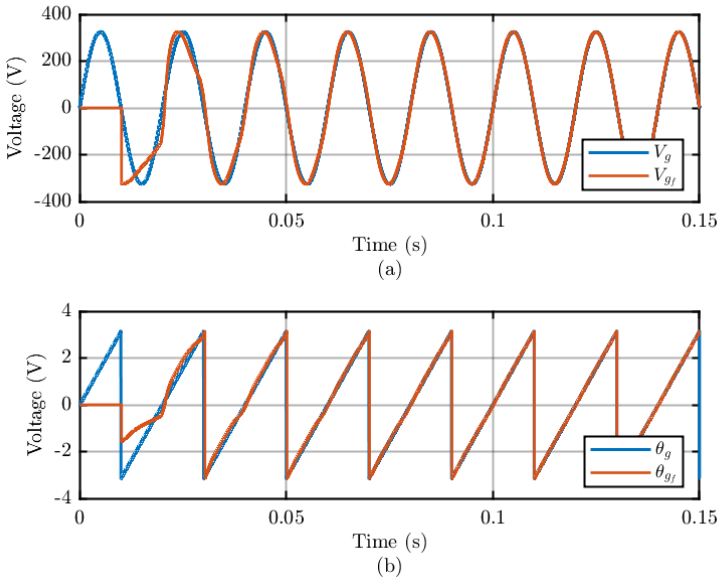


Figure 3.5: PLL test 1: (a) Comparison between input and output of the resonant filter, (b) Comparison between the angle of the mains voltage and the angle obtained from the PLL.

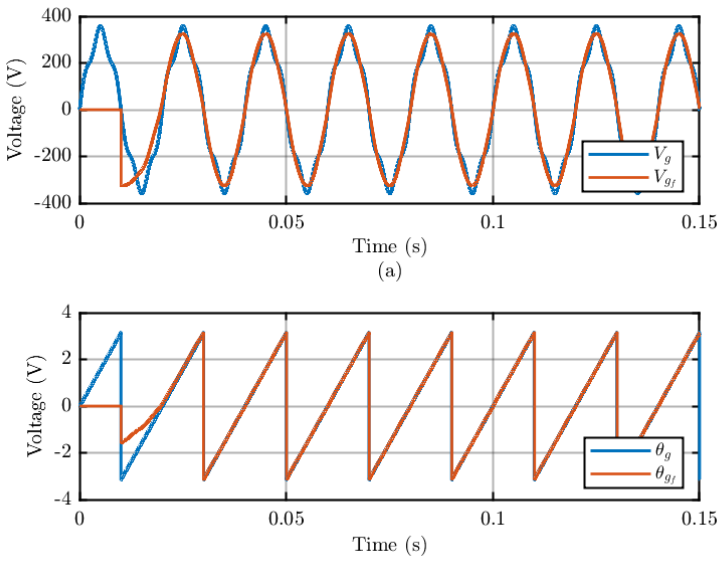


Figure 3.6: PLL test 2: Distorted supply voltage with fifth harmonic.(a) Comparison between input and output of the resonant filter, (b) Comparison between the angle of the mains voltage and the angle obtained from the PLL.

Voltage Control on the DC-Bus Test

the test involves starting the generator side system with relative DC-link charging, response to a load ramp up to 3.3 kW (8.25 A @t = 1.1s) and subsequently to a load step variation up to 5 kW (12.5 A @t = 2s).

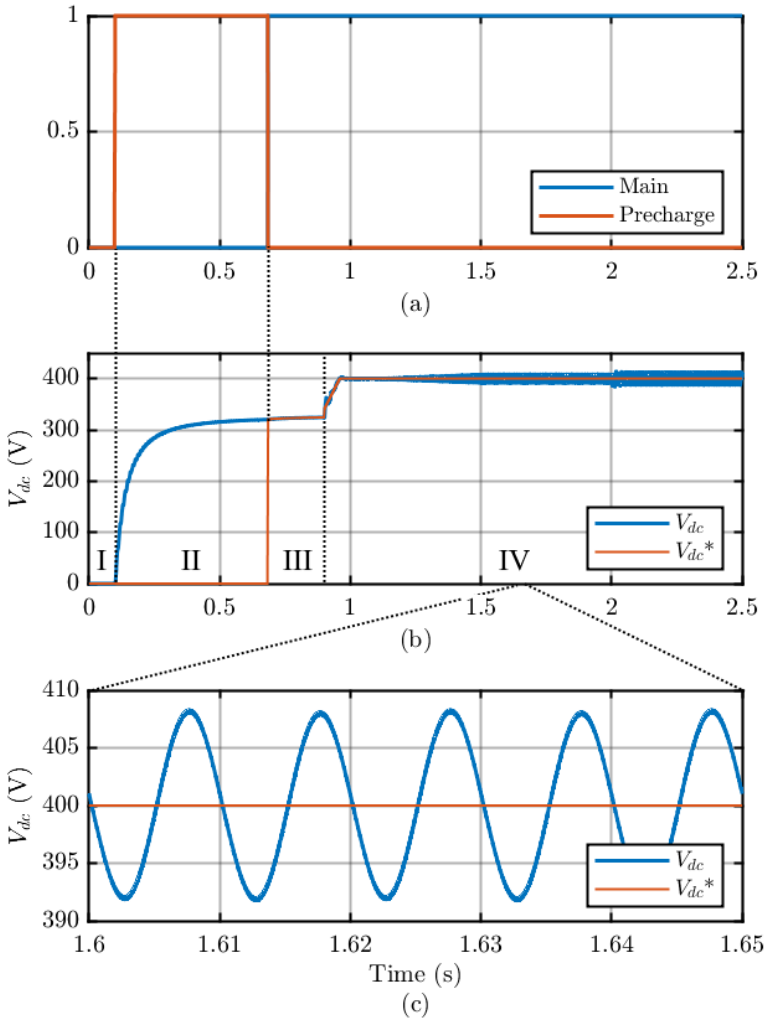


Figure 3.7: Results of the PLECS simulation for the PFC converter. (a) Precharge relay control signals; (b) Voltage on the DC bus; (c) Zoomed voltage on the DC-bus during steady-state working point at 3.3 kW.

Fig3.7.a shows the command signal for the precharge relay, while in Fig3.7.b we can see the voltage on the DC-bus and its trend from the start-up process. The graph

is divided into four regions, each identified with a Roman number, which represent the working states of the state machine, respectively ERROR, PRECHARGE, READY and GO. Fig3.7.c shows a zoomed version of the working phase at 3.3 kW. Here we can see that the computation for the DC-link capacitance are validated by the 8 V amplitude on the sinusoidal ripple, or 2% as per specification.

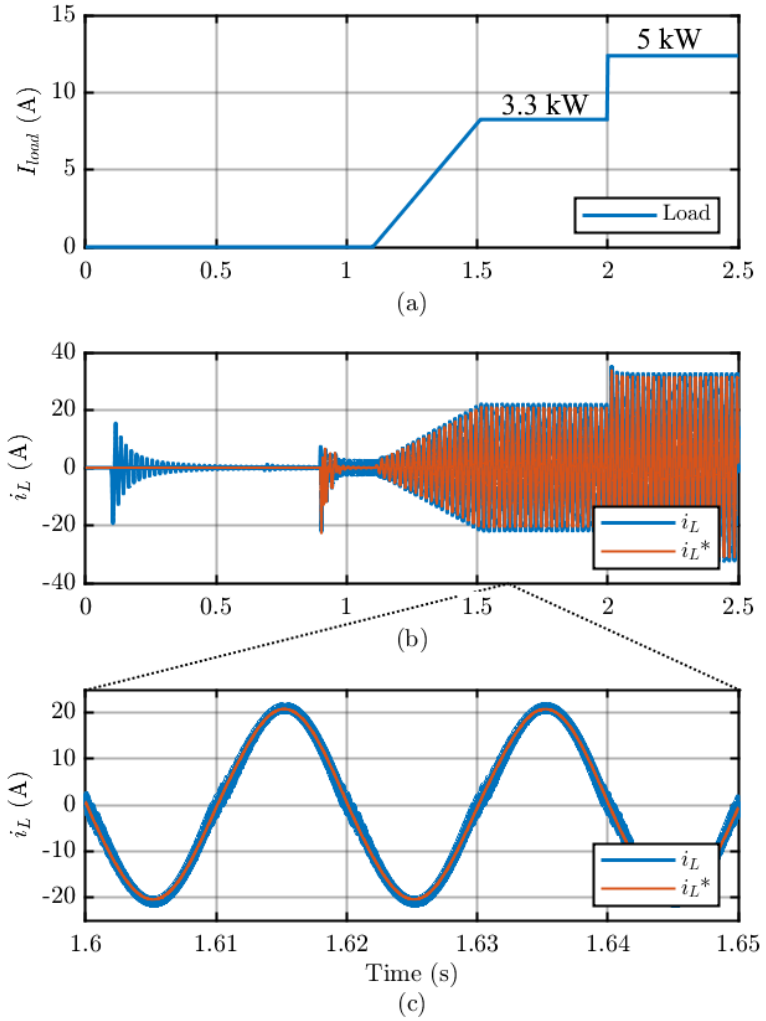


Figure 3.8: Results of the PLECS simulation for the PFC converter. (a) Load variation; (b) Current in the filter inductor with its reference; (c) Zoomed inductor current at steady-state working point at 3.3 kW.

Fig. 3.8 shows the current in the inductor (b and c) in relation to the load current (a). From here it is possible to see how the proportional-resonant regulator optimally follows

the reference generated by the voltage loop. On the waveform of the current it is also possible to observe the presence of distortion around the zero-crossing points, this is due to the dead time inserted to avoid short circuits in the switching phase.

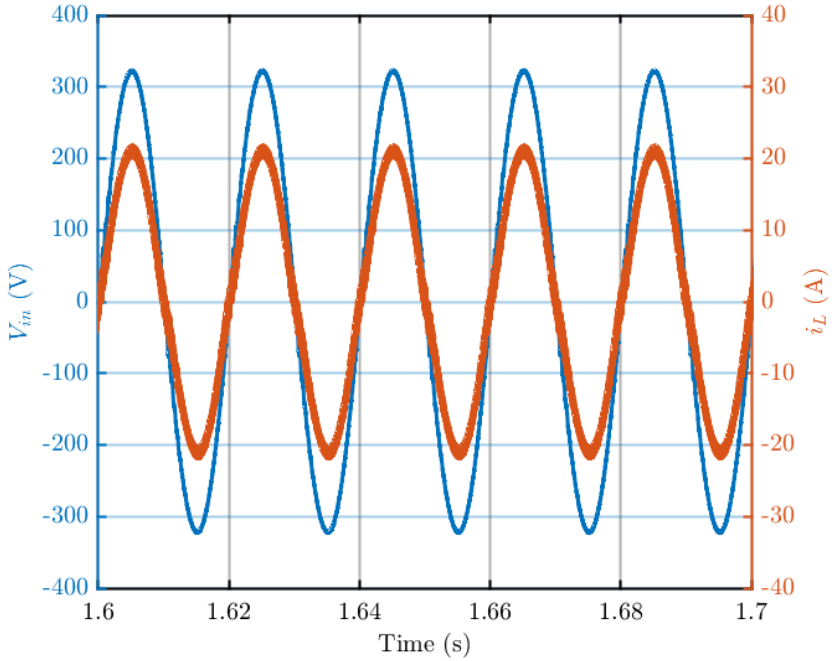


Figure 3.9: Comparison between the voltage on the grid side of the converter and the absorbed current.

Finally, in Fig.3.9, it is possible to observe the electrical quantities on the network side of the active front end. As shown in the graph the voltage and current are perfectly in phase, which means that the PLL is working properly. The maximum THD recorded during steady-state simulations is equal to 4.3%, mostly due to switching noise and dead time distortion.

3.2 Active Capacitor Simulation

As previously mentioned, the auxiliary circuit used to emulate the capacitance of the virtual capacitor is based on a bidirectional converter (canonical switching cell). Although the simulation also included all the PFC part, in fig. 4 is shown, for a cleaner view, only the model concerning the active capacitor circuit.

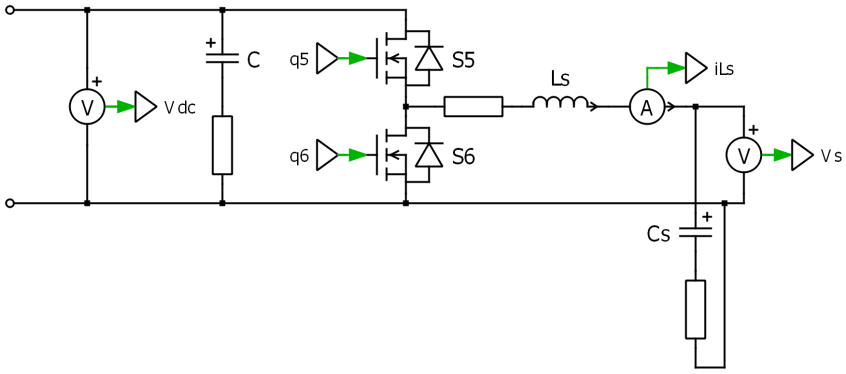


Figure 3.10: PLECS model of the active capacitor connected to the PFC.

Again, we can identify on the schematic the measurement points necessary for the control algorithm through the voltmeter and ammeter blocks inserted in the model. In particular we will have the voltage on the DC-bus V_{dc}, the only measurement external to the device, the voltage on the buffer capacitor V_s and the current in the auxiliary inductor i_{L_s}, used only in the CCM control.

Since the control of the virtual capacitor is decentralized by nature, the measurement acquisition blocks, such as Analog conditioning or ADC and Sampling, have been kept separate from those of the active front end, as well as the simulation block for the micro-controller or the modulator. This approach is fundamental as it allows to work at different sampling frequencies between the control of the PFC and that of the auxiliary circuit. To distinguish the quantities used for the virtual capacitor, the prefix VC has been added to the respective labels.

As for the previous control, therefore, the measured quantities are filtered through continuous transfer functions within a subsystem and are then discretized with the aid of a triggered subsystem. The ISR signal in this case is identified with the label VC_ISR.

The blocks just discussed with their respective contents are shown in Fig.3.11.

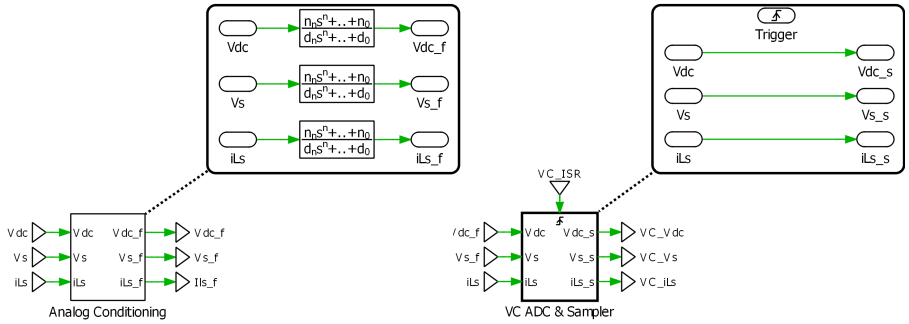


Figure 3.11: Subsystems in PLECS model for the analog conditioning of the measured values (left) and to simulate Analog to Digital Conversion (right), with the respective content, for virtual capacitor quantities.

The microcontroller is again modelled as a "C-Script" block that runs the code every time it is triggered by the VC_ISR signal. The block receive as an input the sampled quantities V_{dc}, V_s and i_{L_s} as well as control signal "Start" to simulate the user input. At the output we found the duty signal VC_d and the enable signal for the PWM modulator VC_EN. A debug output permits to check on the desired quantities processed by the micro.

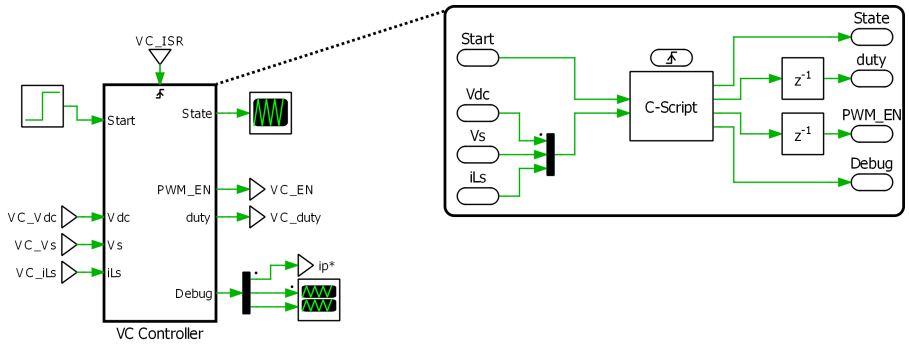


Figure 3.12: Realization in PLECS of the microcontroller for the virtual capacitor.

As regards the modulator we have two versions, based on whether the control is in CCM or in DCM, Fig.3.13. The duty signal is processed in the same way but for the DCM version the enable signal is a vector of two components (EN_H and EN_L) which respectively control the high switch and the low switch, to allow alternating operation in the buck and boost phases.

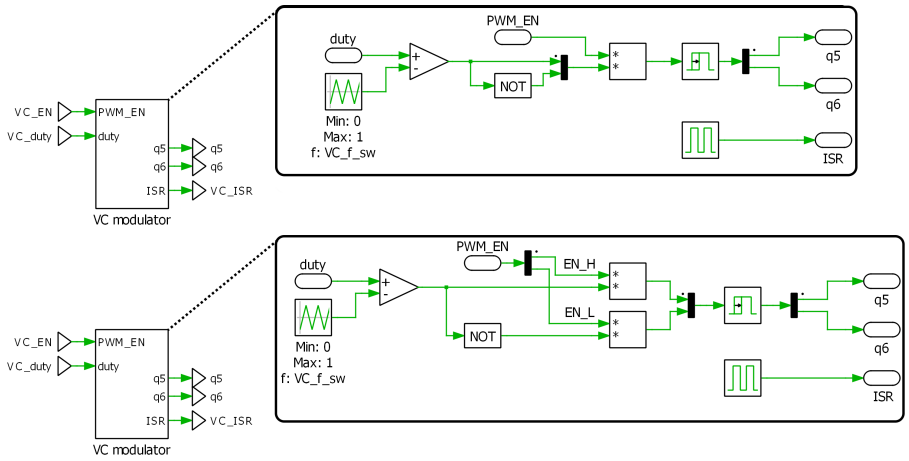


Figure 3.13: Different versions of modulator for the virtual capacitor: above the modulator for the CCM control where there is a single enable signal, below the modulator for the DCM control in which each switch has its enable signal.

3.2.1 Active Capacitor Control Code

The code for the control on the virtual capacitor follows the same base philosophy adopted for the PFC regulator: the first part register the input signals, perform some basics calculations to adapt them for the purpose of the control and check them for a software protection. Being the device decentralized with respect to the main converter, it is not possible to carry out an emergency action on the DC bus, therefore the quantity control is limited to i_{L_s}, if this is measured, and V_s:

- $i_{L_s} < ILS\_CRT\_MAX$: the system goes into protection if the instantaneous value of the measured inductor current exceeds the threshold defined by the switch maximum current rating.
- $V_s < VS\_VLT\_MAX$: the system goes into protection if the instantaneous value of the voltage on the buffer capacitor exceeds the threshold defined by by its voltage rating.

If any of these two conditions were violated, the device would instantly enter an error state. The second part of the code is a state machine, consisting of the following states:

- *ERROR*: it is the starting state of the system or the state it enters in case there are errors due to the activation of the protections. The modulation is disabled, the

duty-cycle is set to zero and the quantities used in the code are resetted to avoid any settings in the memory of previous activities. The "Start" signal triggers a series of operation in which the voltage on the bus is sensed through a digital continuous moving average filter and the limits of the operating range are computed, as well as the midpoint for the precharge process. In addition, the initial conditions of the transfer function are initialized. After these operations the code moves to the next state.

- *PRECHARGE*: in this state the modulation start and the buffer capacitor is charged to a voltage equal to the range $V_{ref} = (V_{s,min} + V_{s,max})/2$. The duty signal is represented by a ramp from zero to V_{ref}/V_{dc}. Reached the value, the machine goes to the next state.

- *STARTUP*: in this state the control is started with the overdamped parameters to avoid large or long-lasting oscillations due to the absence of load. If the voltage recorded by the microcontroller remains within a tolerance range around the bus value recorded at the output from the ERROR state for a certain amount of time, the parameters of the regulators are returned to the nominal value by means of a ramp. At this point, it is possible to proceed to the next state.

- *GO*: this state contains the actual control illustrated in paragraph 2.2 and translated into C code.

As we can see from the working principle of the state machine, for this algorithm to work, it is essential that the active capacitor is started on a stable, no-load DC bus. It is possible to generalize even more the starting phase but this would require a longer start up time, in order to have more precise evaluations on the equilibrium value of the voltage V_{dc} or to avoid starting the control during transients on the DC bus.

3.2.2 Validation of the Active Capacitor Control Strategy

The validation of the control strategies is carried out in the following section. These consist of the tests carried out on four controls, two in CCM and two in DCM, and in each of the pairs the K regulator is proposed both in the lead lag version seen in (2.15) and in the PI version. The tuned parameters for the controllers are presented in Table 3.2: (a) and (b) refers to the tests performed in discontinuous conduction mode, respectively with the Lead Lag and the PI as the regulator K, while (c) and (d) refers to the tests in continuous conduction mode.

TABLE 3.2: VIRTUAL CAPACITOR SIMULATION: CONTROLLERS PARAMETERS FOR EACH TESTED CONFIGURATION.

Lead Lag - DCM

a	0.5	K_0	0.0003
c	4.75	θ	$1/(2\,\pi\,200)$
τ	$1/(2\pi\ 25)$	ϵ	0.25

(a)

PI - DCM

a	0.475	$K_{p_{V_s}}$	0.00028
c	5	$K_{i_{V_s}}$	0.05625
τ	$1/(2\pi\ 25)$		

(b)

Lead Lag - CCM

a	0.59	K_0	0.00015
c	4.75	θ	$1/(2\,\pi\,200)$
τ	$1/(2\pi\ 25)$	ϵ	0.25
K_{p_i}	45.7416	K_{i_i}	12454

(c)

PI - CCM

a	0.6	$K_{p_{V_s}}$	0.00008
c	4.75	$K_{i_{V_s}}$	0.02
τ	$1/(2\pi\ 25)$		
K_{p_i}	28.1487	K_{i_i}	4716.4

(d)

The electrical parameters computed in the previous chapter and used in the simulation are reported in Table 3.3. Here we also found the t_D term, which refers to the dead time inserted in the switching gating signal to prevent short-circuits between the upper and lower switches of power converters from over-current protection. Working with IGBTs, the dead time is set to a value equal to 1μs.

TABLE 3.3: VIRTUAL CAPACITOR SIMULATION: ELECTRICAL PARAMETERS.

Electrical parameters					
C_s	200	[μF]	C_0	100	[μF]
$L_{s,DCM}$	68	[μH]	$L_{s,CCM}$	5.6	[mH]
f_{sw}	20	[kHz]	t_D	1	[μs]

For the validation of the control strategies, the simulation was set up to have the following phases:

- Startup process on a 400V DC bus with no load @$t = 0.35\ s$;
- Connection of a 3.3 kW ramp load (8.25 A) with a slope of 100 A/s @$t = 0.8\ s$;
- Step variation of the load from 3.3 kW to 1.65 kW @$t = 1.2\ s$
- Step variation of the load from 1.65 kW to 3.3 kW @$t = 1.6\ s$

In Fig.3.14 a first comparison of the waveforms on the DC bus is presented: the red waveform represent the bus voltage with the active capacitor connected, the blue one represent the bus voltage with the same total system capacitance connected as a classic DC link.

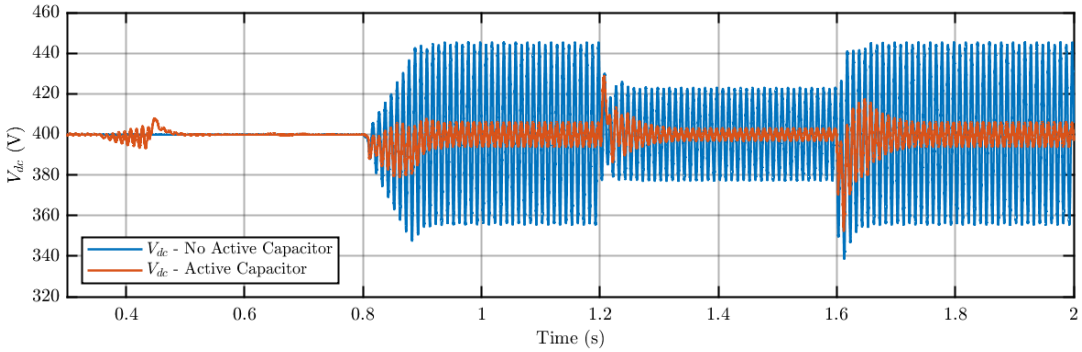


Figure 3.14: Comparison of the DC bus voltage waveform with a classic DC link (blue) and with the active capacitor.

In the following sections, the individual work phases will be analyzed in more detail.

Working Phases

This section analyzes the work phases of the state machine in relation to the main quantities used by the control, as shown in Fig.3.15.

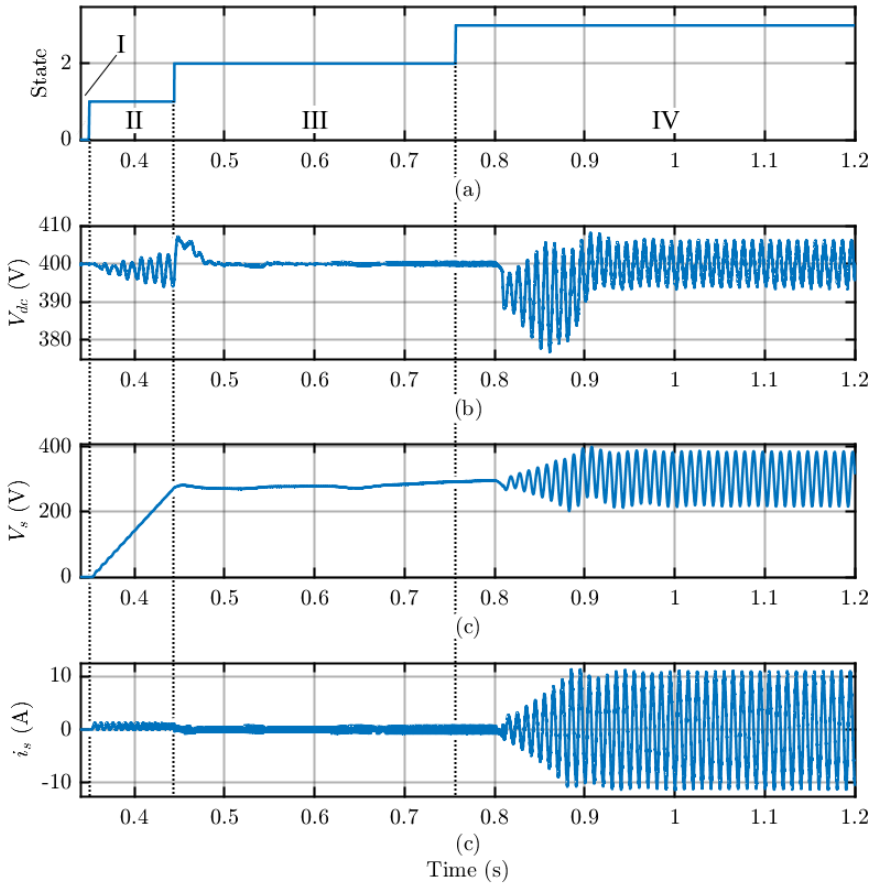


Figure 3.15: Working phases of the virtual capacitor: (I) Error, (II) Precharge, (III) Start-up, (IV) Go.

Phase II represent the state of *PRECHARGE*, in which the duty is linearly increased to limit the inrush current. The precharging of the buffer capacitor creates oscillations on the DC bus, with a subsequent small overshoot while entering the third phase, due to starting the control in a system with no load. The overshoot is quickly dissipated due to the overdamped control strategy used in this phase and, after the bus voltage reaches the equilibrium value and remains within the range $V_{dc} \in [V_0 - \delta,\ V_0 + \delta]$, with $\delta = 1V$, for

a time equal to 50 ms, the gains of the regulators are resetted to the nominal value and phase IV can start.

In phase four, at $t = 0.8\ s$, the load ramp causes a sudden variation on the DC bus voltages that triggers the temporary protection described in the previous chapter. As we can see in Fig.3.15.c, in fact, during the transient the amplitude of the ripple is larger because of high frequency gain reduction by means of the signal γ. After the transient the system goes in normal operating condition at the equilibrium voltage. As expected V_{dc} and V_s have similar waveform but, of course, the oscillation on V_s have a much larger amplitude (Fig.3.16).

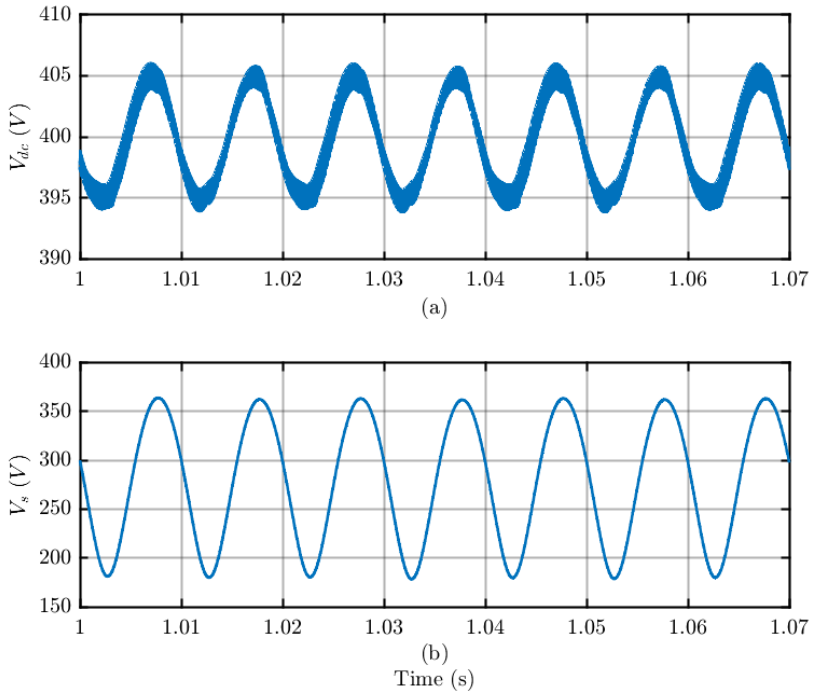


Figure 3.16: Zoomed view on the DC bus voltage (a) and the buffer capacitor voltage (b).

The energy variation in the active capacitor, without considering the energy in L, can be expressed as

$$\Delta E = \frac{1}{2}C_s((\max V_s)^2 - (\min V_s)^2) + \frac{1}{2}C((\max V_{dc})^2 - (\min V_{dc})^2) \tag{3.2}$$

By defining $\bar{V}_{dc}$ as the average value between max V_{dc} and min V_{dc}, and similarly for $\bar{V}_s$, it is possible to rewrite (3.2) as

$$\Delta E = C_s \, \Delta V_s \bar{V}_s + C \, \Delta V_{dc} \bar{V}_{dc} = C_{eq} \, \Delta V_{dc} \bar{V}_{dc} \tag{3.3}$$

Hence

$$C_{eq} = C + C_s \, \frac{\Delta V_s \bar{V}_s}{\Delta V_{dc} \bar{V}_{dc}} \tag{3.4}$$

From here, the equivalent capacitance C_{eq} at 100 Hz can be computed. From Fig.3.16 we have $\bar{V}_{dc} = 400 \; V$, $\Delta V_{dc} = 12 \; V$, $\bar{V}_s = 270 \; V$ and $\Delta V_s = 180 \; V$. Thus, using (3.4), we obtain

$$C_{eq} = 2.1 \; mF$$

Meaning that the total capacitance seen from the system is 8.5 times the real capacitance installed in the circuit.

Steady-State Performance

In this section the steady state performance of the converter will be confronted for each controller strategy. In Fig.3.17 we can observe the waveforms of the voltage on the DC bus.

As we can see from the figure, in steady state we obtain excellent results as regards the reduction of ripple. In fact, using the same amount of capacitance present in the system as a normal DC link, we would obtain a ripple on the DC bus with a peak amplitude of about 48V, Fig. 3.17.e, while with the active capacitor we are able to more efficiently exploit the total capacity of the system and reduce the ripple, in the worst case scenario, Fig. 3.17.d, to an amplitude oscillation with a peak of about 10V.

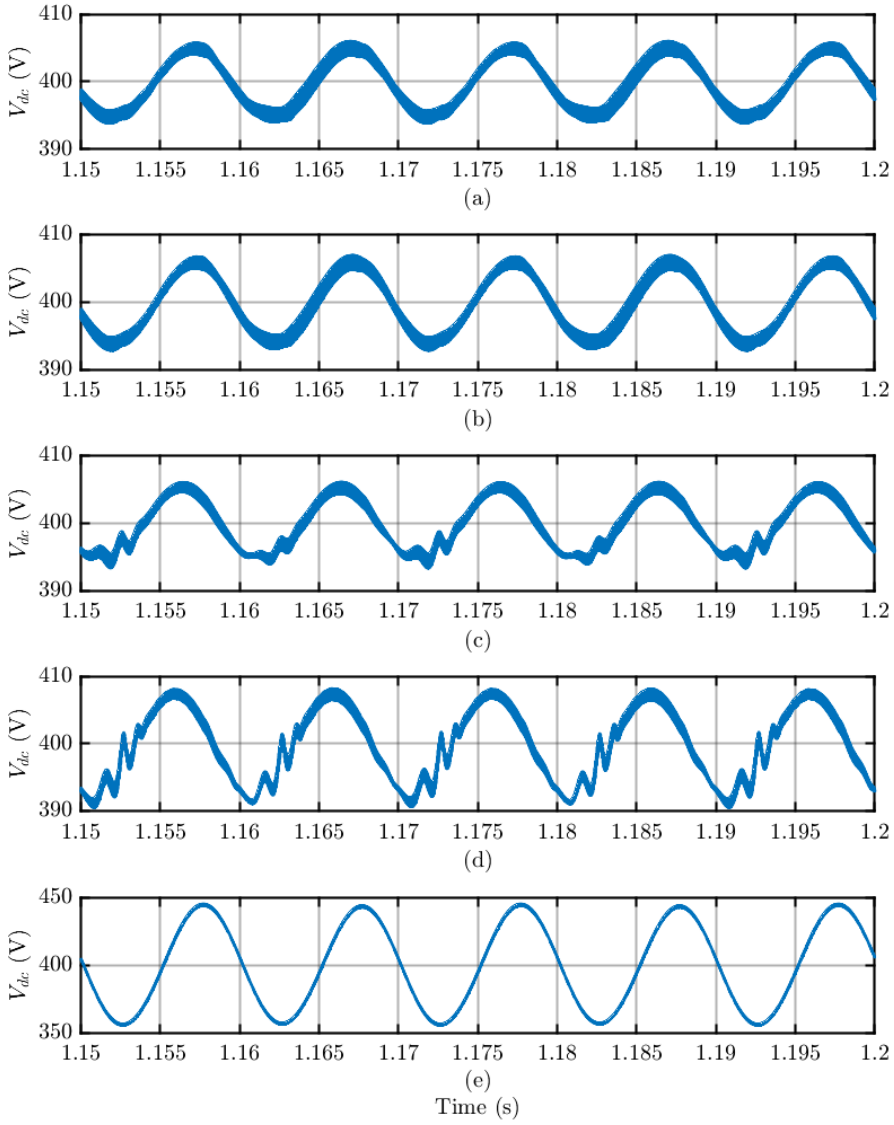


Figure 3.17: DC bus voltage waveforms comparison between the presented control strategy: (a) and (b) refers to the tests performed in DCM while (c) and (d) refers to the tests in CCM, each respectively with the Lead Lag and the PI as the regulator K. (e) shows the voltage waveform with a normal DC link with the same total capacitance.

It is also possible to observe how, in the working conditions presented, the CCM are affected by distortions due to dead time that are not present in the DCM simulations. That is because dead time can cause discontinuous conduction mode when the output current is near the zero-crossing, generating low order harmonics and non-linearities at the converter output which compromise current control.[22]

A compensation based on average value theory, in which the lost volt-seconds are averaged over an entire cycle and added to the current controller output, has been implemented in software to mitigate this effect: considering the dead time t_D and the switching frequency f_{sw} we can calculate a ΔV^* value, which represents the percentage of the current regulator output lost because of the dead time, such that

$$\Delta V^* = f_{sw}\, t_D\, V_{dc} \tag{3.5}$$

The compensation is then applied by adding the ΔV^* value to the regulator output if the reference current is positive, or by subtracting it if it is negative, as shown in Fig.3.18.

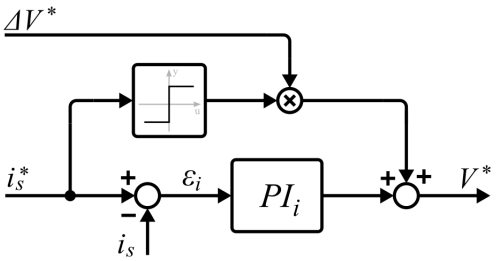


Figure 3.18: Block diagram representation of the duty compensation.

However, the effects of the compensation remain limited, as the IGBTs need a dead time which corresponds to a non-negligible percentage of the switching period in use, but it still has allowed to obtain better performance and stability for the system.

In any of the proposed cases, the resulting THD of the current absorbed from the grid at steady state functioning is lower or equal to 1%.

Load Variation

To prevent abrupt changes of V_s due to load variation from leaving the optimal working range $[V_{s,min}, V_{s,max}]$, a protection has been implemented in software. Each time the code is compiled, a temporary variable is generated as

$$tmp = |\bar{V}_s^{\,k} - \bar{V}_s^{\,k-1}| \tag{3.6}$$

Where $\bar{V_s}^k$ is the output value of a digital continuous moving average filter on V_s read in the current cycle, and $\bar{V_s}^{k-1}$ is the output value of the cycle before. This variable is then compared with a threshold value and, if exceed it, triggers a function that reduce the value of the signal γ from Fig.2.9 for a short period of time. After that event, γ is slowly increased back to 1, and the ripple on the DC bus decreases gradually.

The effects of the load variation protection system are shown in Fig.3.19 and Fig.3.20.

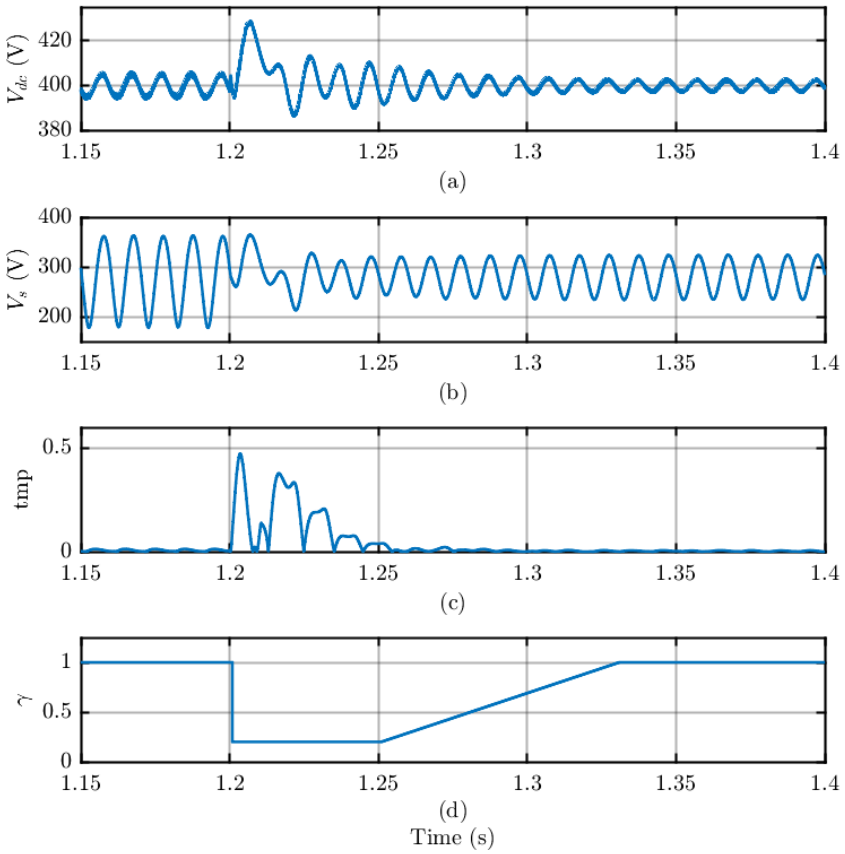


Figure 3.19: Effects of a 50% step reduction of the load (@t = 1.2 s) on V_{dc} (a) and V_s (b). (c) shows the triggering signal and (d) the variation of the γ signal.

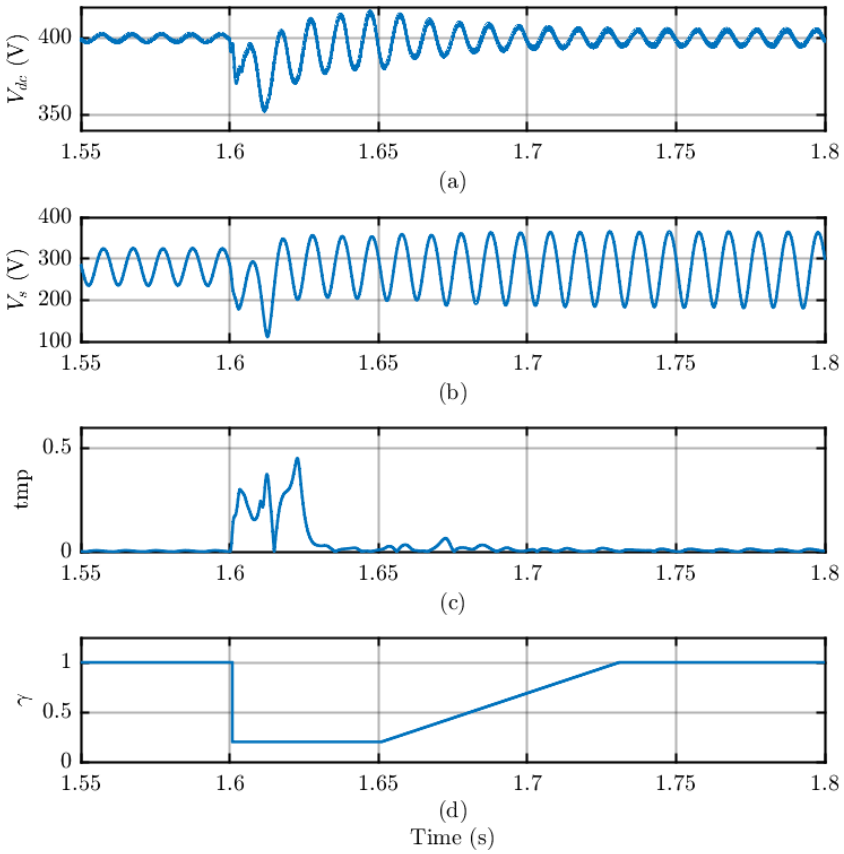


Figure 3.20: Effects of a 100% step increase of the load (@t = 1.6 s) on V_{dc} (a) and V_s (b). (c) shows the triggering signal and (d) the variation of the γ signal.

As it can be noticed in Fig.3.19, the step variation @t = 1.2 s causes an overshoot on the DC bus of about 30V but the damping effect of γ limits the variation on the buffer capacitor voltage, preventing it from leaving the working range. On the down size the ripple on the DC bus is increased for a short period of time. Similarly, in Fig.3.20, the positive load variation causes an undershoot of about 50V.
In both cases, thanks to the temporary damping, the system returns to the equilibrium voltage relatively quickly, without oscillations.

Inductor currents

Here we take a brief look at the current in the inductor compared with its reference, both in continuous (Fig.3.21) and discontinuous conduction mode (Fig.3.22).

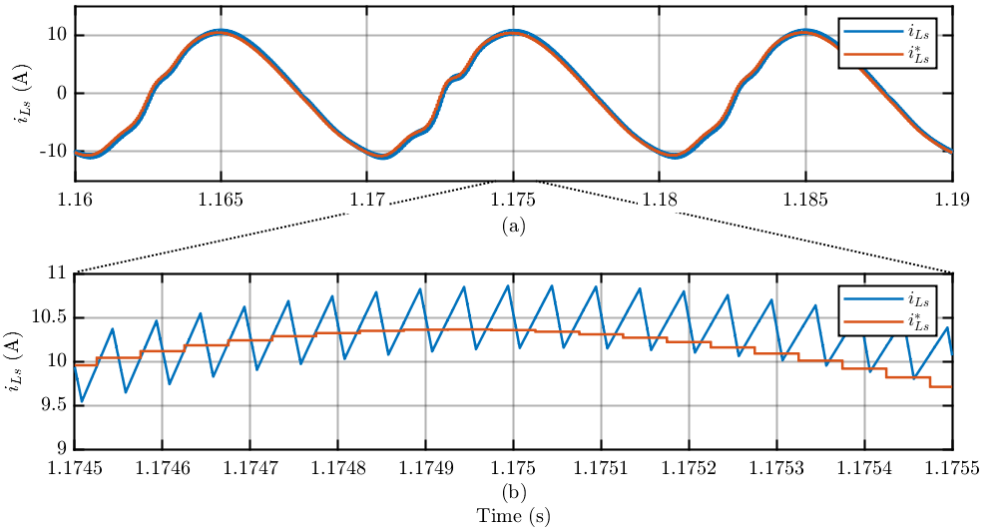


Figure 3.21: Current in the inductor along with the reference current for the CCM control. (b) shows a more zoomed version of (a).

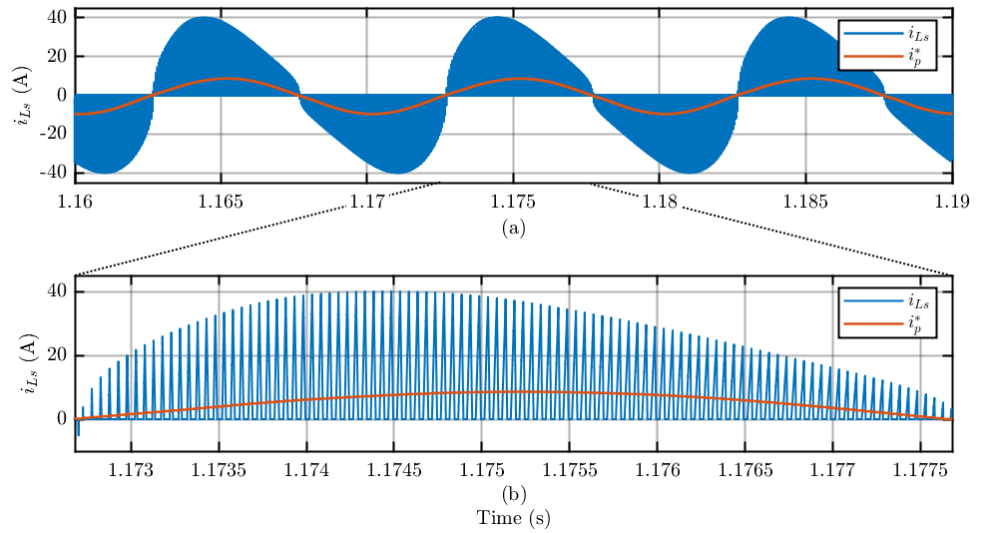


Figure 3.22: Current in the inductor along with the reference current for the DCM control. (b) shows a more zoomed version of (a).

From Fig.3.21 we can observe the validation of the inductor value computed in 2.3.2. In fact, given inductor current reference peak value of $\hat{i}_{Ls} = 10.5\ A$, the peak to peak current ripple equals to $\Delta i_{Ls} = 0.6\ A$ which correspond to a 5.7% fluctuation, coherent with the 5% chosen in design stage. The offset between the reference and the actual moving average value of the current, on the other hand, is due to the duty cycle compensation analyzed in the previous section.

In Fig.3.22, instead, we can observe the inductor current i_{Ls} along with the reference for the converter input current i_p^*. The behaviour of the current in discontinuous conduction mode can be easily spotted in Fig.3.22.b, in which it is characterized by peaks of short duration and high amplitude, which always cancel out over the course of the period.

3.2.3 Thermal Simulation

The core component of the thermal library in PLECS is an idealized heatsink depicted as a semitransparent blue box. The heatsink absorbs the thermal losses dissipated by the components within its boundaries and, at the same time, defines an isotherm environment and propagates its temperature to the components which it encloses. Heat conduction from one heatsink to another or to an ambient temperature is modelled with lumped thermal resistances and capacitances that are connected to the heatsink through one or more terminals.

The model in question was built starting from the thermal model of the semiconductor, connected to the environment (modelled as a continuous and ideal temperature generator T_a) by means of thermal resistances that represent the case-heatsink contact point and the exchange between heatsink and environment. The scheme used in the simulation is shown in figure 3.23.

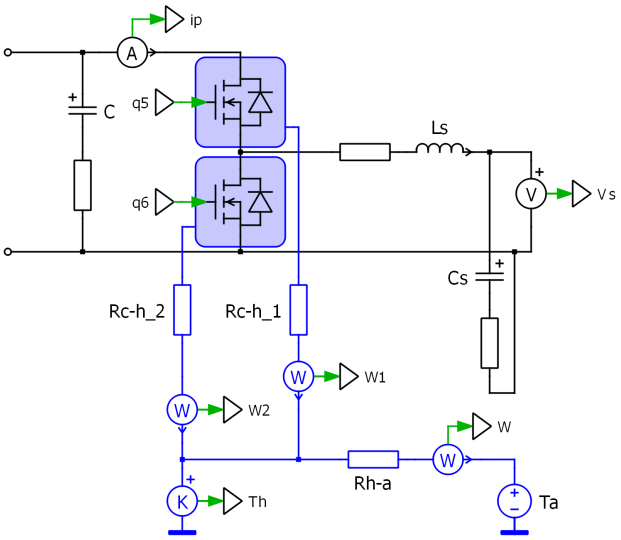


Figure 3.23: PLECS model of the active capacitor connected to the PFC, with thermal analysis components.

The junction-case thermal impedance has been implemented in the thermal model thanks to a PLECS tool, that permits to extrapolate from the datasheet curve the values of thermal resistances and capacitance needed to build a Cauer model.

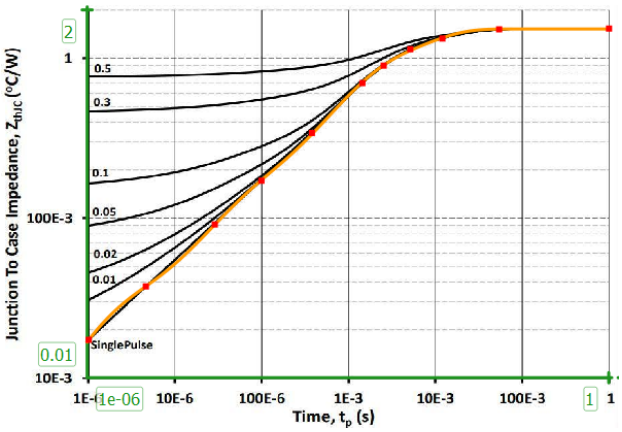


Figure 3.24: Extrapolation of the Cauer model from the thermal impedance curve provided by the manufacturer.

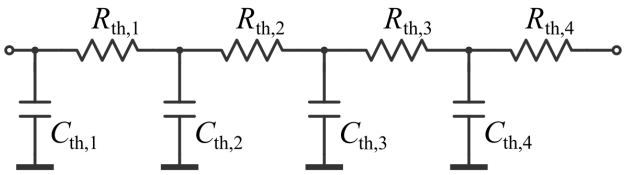


Figure 3.25: Cauer model of the junction-case thermal impedance.

Referring to Fig.3.25, the obtained values are reported in Table 3.4.

TABLE 3.4: CAUER MODEL COMPONENTS VALUE FOR JUNCTION-CASE THERMAL IMPEDANCE.

	1	**2**	**3**	**4**
R_{th} $(°C/W)$	0.03209	0.1485	0.8292	0.5092
C_{th} $(J/°C)$	4.285e-05	0.0003216	0.001303	0.01568

In addition to the thermal impedance, the Look-Up Tables (LUTs) must be entered in PLECS which will be used by the software through a linear interpolation of the input values (I_d,V_{DS},T_J and sw), to calculate the system losses. For the power lost in conduction, the trend of the voltage and current in conduction must be entered in the thermal library for various temperature values and, in the case of the MOSFET, for various values of the gate voltage. In Fig.3.26 are reported the conduction losses LUTs for $V_g = 15\ V$ (switch ON) and $V_g = -4\ V$ (switch OFF, body diode losses).

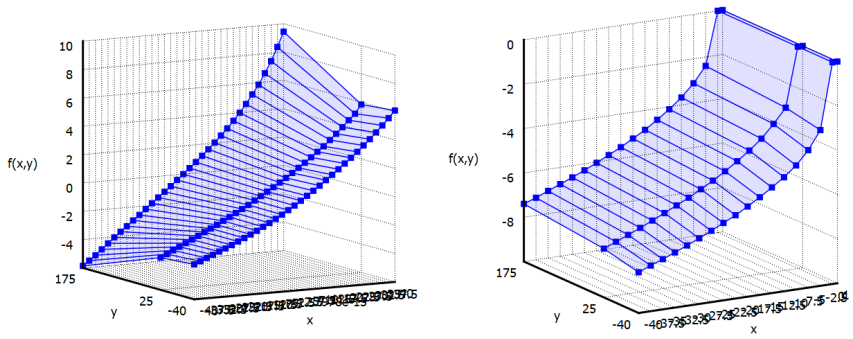


Figure 3.26: PLECS LUTs to compute conduction losses: x variable is the current I_d, y variable is the junction temperature T_J and z is the voltage V_{DS}. The gate voltage is $V_g = 15\ V$ in the left LUT and $V_g = -4\ V$ in the right one.

The conduction losses are then calculated with the following code:

```
(sw==0)*lookup('Von_Vg0V(x:Id,y:Tj)',i,T)+(sw!=0)*lookup('Von_Vg15V(
  x:Id,y:Tj)',i,T)
```

where *sw* is the signal that turn ON or OFF the switch. (sw==0) and (sw!=0) are boolean condition that permits to select which table must be used at each instant, according with the command signal at the MOSFET gate.

In the same way the LUT for switching losses are inserted, as a function of I_d and T_J, considering an external gate resistance equal to $R_{g,ext} = 10\ \Omega$ and $V_{DS} = 400V$. The LUTs are showned in Fig.3.27.

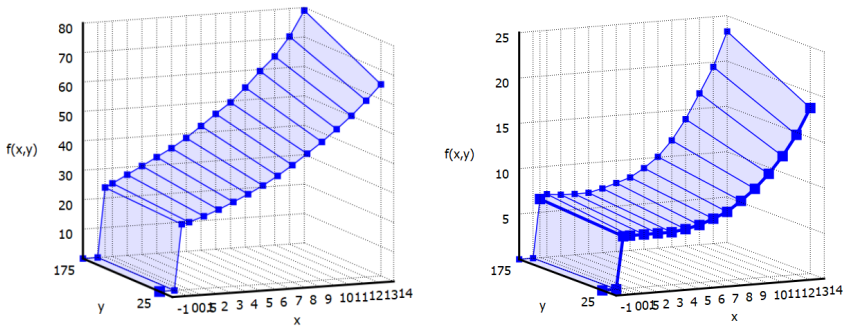


Figure 3.27: PLECS LUTs to compute switching losses: x variable is the current I_d, y variable is the junction temperature T_J and z is the energy needed to turn ON the switch E_{ON} (Left) or the energy needed to turn OFF the switch E_{OFF}. The external gate resistor is $R_{g,ext} = 10\ \Omega$ and the blocking voltage is $V_{DS} = 400V$.

Since these LUTs are referred to a blocking voltage equal to $V_{DS} = 400V$ the Energy value is calculated at each instant with the following codes, for E_{ON} and E_{OFF} respectively, which normalize them to the actual V_{DS} value at each instant.

```
lookup('Eon(x:Id,y:Tj)',i,Tj)*v/400*1e-6
```

```
lookup('Eoff(x:Id,y:Tj)',i,Tj)*v/400*1e-6
```

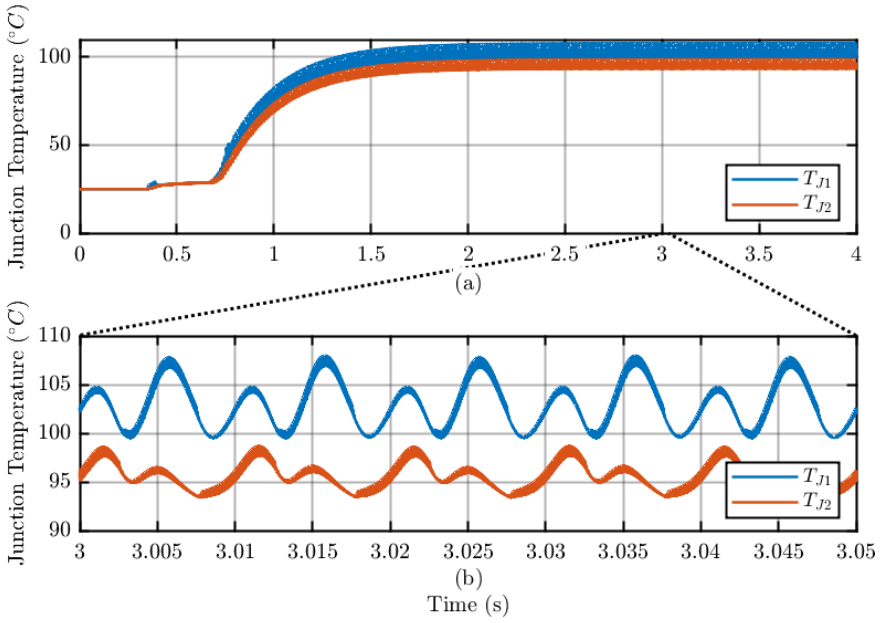
The term "1e-6" scales the LUT energy in mJ.

Thermal Simulation Results

From the simulations of the thermal model in nominal conditions, the temperature trend in the junctions was obtained. It is possible to observe the transient in Fig3.28.a while in Fig.3.28.b there is a zoomed version of the steady state temperature trend.

It can be easily spotted that the temperature are at an optimal level, being $T_{J1} = 103\,°C$ and $T_{J1} = 96\,°C$ on average, thus ensuring a long life to the converter. The average temperature on the heatsink, at steady state conditions, is equal to $T_h = 89.4\,°C$ and the temperature trend on the heatsink is shown in Fig3.29.

[



][H]

Figure 3.28: Temperature trend in the MOSFET junction: in (a) it is possible to observe the entire transient, in (b) a zoom of the situation at steady state is shown.

From the thermal model in PLECS it is also possible to derive the trend of the power dissipated by the individual switches (Fig.3.30.a) and of the total dissipated power, shown in Fig.3.30.b.

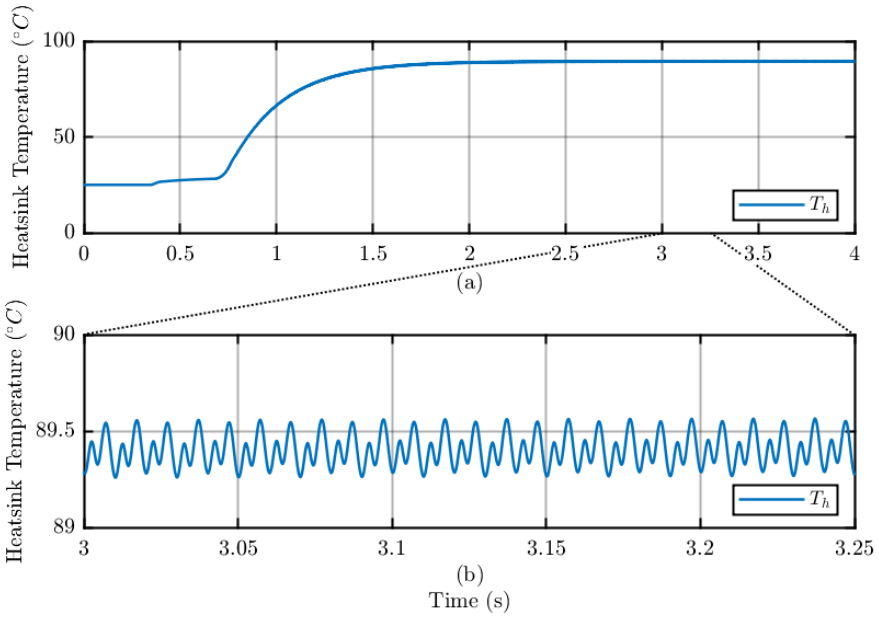


Figure 3.29: Temperature trend in the heatsink: in (a) it is possible to observe the entire transient, in (b) a zoom of the situation at steady state is shown.

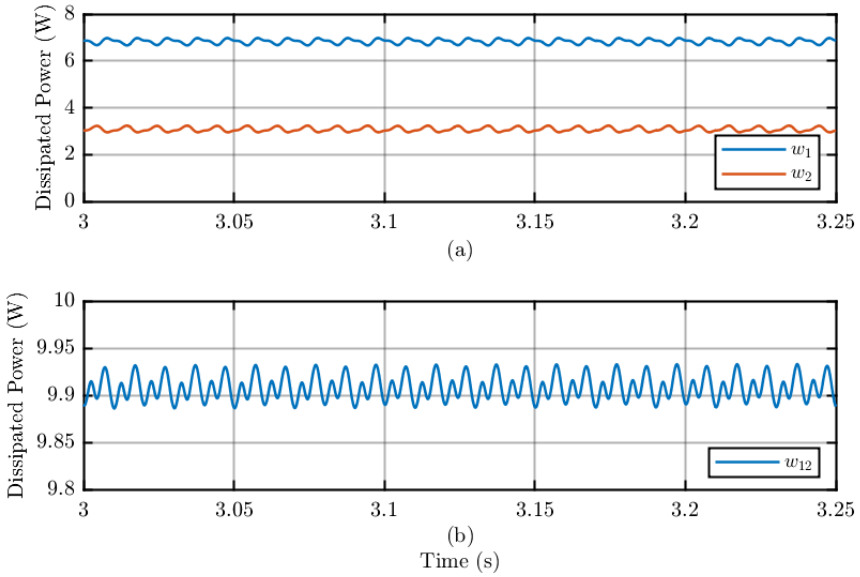


Figure 3.30: Dissipated Power trend in the MOSFET: in (a) it is possible to observe the losses for each switch, in (b) the total losses are shown.

These results, obtained through the simulation, validate the design choices.

Chapter 4

Experimental Tests

This chapter will deal with the realization in the laboratory of the experimental set-up carried out within the PEIC (Power Electronics Innovation Center), implementing everything that has been described in the previous chapters. It will then be possible to observe and comment the final results obtained and evaluate the behaviour of the system.

4.1 Experimental Set-up Realization

Before presenting the results obtained in the experimental phase, it is necessary to summarize the characteristics of the test setup. First, an overview of the system will be provided, then the individual components will be described.

In order to carry out the tests described in chapter 3 experimentally, a preliminary phase of preparation for the tests of the systems in use, assembly of the components and verification of the correct functioning of each part of the system was necessary.

As for the hardware part, the test bench exploit a standard three-phase inverter: two of the three inverter legs were connected to the power distribution grid to be used as an active rectifier, the load was connected to the DC link and the third inverter leg was used as a bidirectional converter, after having connected auxiliary capacitors and inductances to it. On the software side, the MicroLabBox rapid prototyping platform developed by dSpace, managed through a Graphical User Interface (GUI) developed on Control Desk,

was used to control the converter in real time. A schematic representation of the experimental set-up is shown in Fig.4.1.

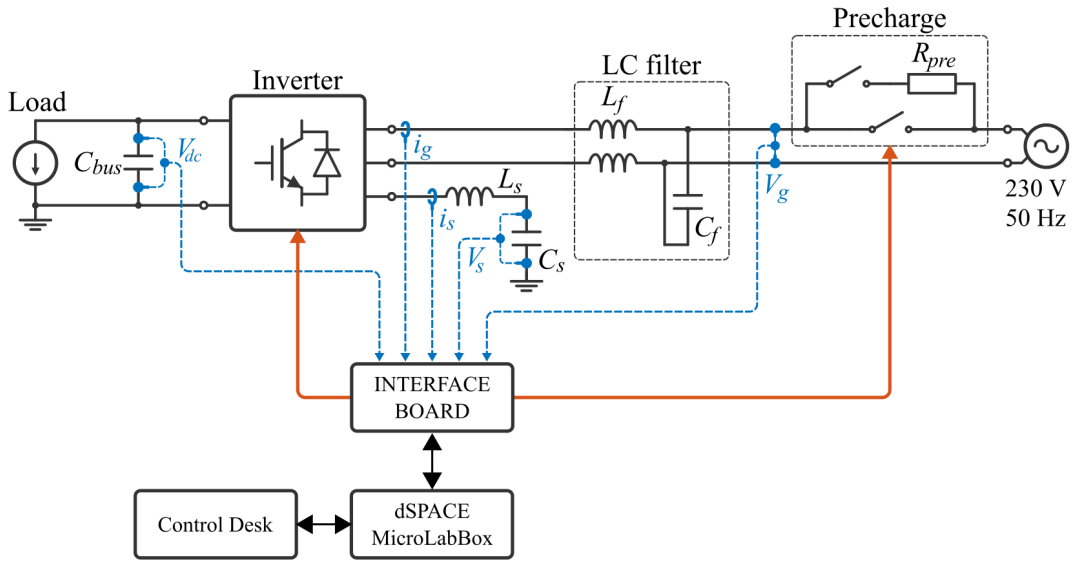


Figure 4.1: Schematic representation of the experimental setup.

Converter: GUASCH MTL-CBI0040F12IXHE

The converter used in the set-up is the GUASCH MTL-CBI0040F12IXHE. It is an IGBT inverter which in addition to the three inverter legs also contains a three-phase rectifier (not used in our case), a "brake leg" used to unload the voltage on the DC link, and a capacitor bank mounted on the DC-link. These features make it a converter suitable for different applications: driving electrical machines, managing renewable resources, powering welding machines, UPSs and more [23]. Improvements have also been made by the PEIC concerning the insertion of an LCL filter on the AC side and switches that simplify the configuration variation from inverter for grid connection to inverter for motor control and vice versa, as well as switches dedicated to pre-charge phase and an FPGA board used to interface the inverter with the control hardware [24]. The inverter characteristics are summarized in Table 4.1.

TABLE 4.1: GUASCH MTL-CBI0040F12IXHE: POWER STACK GENERAL CHARACTERISTIC. [23]

Switching Frequency	f_{sw}	20	[kHz]
Maximum DC-Link Voltage	$V_{DC,max}$	750	[V]
Nominal AC Voltage	$V_{n,RMS}$	400	[V]
Maximum AC Voltage	$V_{max,RMS}$	440	[V]
Maximum phase current	$i_{max,RMS}$	25	[A]
DC-Link capacitance	C_{DC}	1	[mF]
Maximum AC Voltage	$V_{max,RMS}$	440	[V]

As already mentioned, for our application the converter will be used as an active front end, therefore further modifications have been made, in particular the inductors on the grid side of the LCL filter have been excluded, moreover the DC-link capacitors have been removed to allow us to use only the capacity necessary for our purposes: in particular, a series of three 680 μF ($\pm 20\%$) electrolytic capacitors with a maximum voltage of 450 V was connected to the DC-link, resulting in a total measured capacity equal to $C_{bus} = 210\ \mu F$.

Auxiliary circuit

Having chosen to implement the CCM control in order to have a way to control the currents, the auxiliary circuit connected between the third leg of the inverter and the ground of the DC-bus was built using an inductor with a value equal to $L_s = 6\ mH$ and a parallel of capacitors having a total measured value $C_s = 220 \mu F$. In addition, an antiparallel diode has been added to the capacitors to avoid destructive failures in case an incorrect operation of the control imposes a negative voltage.

Control Interface: dSpace Environment

To be able to control the system, it is necessary to create an interface system that puts the PC on which the user control of the system takes place, via Control Desk, and the system itself in constant communication. For this purpose the dSpace MicroLabBox [25] is used, which has the task of executing the control code, transmitting the feedback signals from the converter to the PC and, vice versa, transmitting the control signals from the PC to the converter, all in real time.

In this phase, the adaptation of the control code template of the inverters used with the code already implemented in the C-Script block in the simulation of the microcontroller took place. The structure and commands remain similar, while lines of code have been added to communicate with the Simulink S-function block, to normalize the measured values, and to control the "brake leg", which allows activation of the "braking chopper", applied to the DC-link in case of uncontrolled overvoltages.

A new .trc type variable trace file is also added, useful for communicating the MATLAB/Simulink script with the Control Desk GUI, and then displaying internal code values for debugging or setting parameters directly from Control Desk in real time.

The C code is then implemented in MATLAB and loaded via the S-function block onto the integrated Simulink software.

To complete the experimental set-up it was necessary to customize the user interface to better adapt to the preliminary tests performed on the control and for the tests. The software used, Control Desk, is combined with the dSpace platform and allows you to control the system in real time both by simulating the hardware interface (stop/reset/start/go buttons) but also to modify parameters within the control code. It is also possible to view the values processed in the code via oscilloscopes or displays. Fig.4.2 shows, for example, the control panel created to control the virtual capacitor.

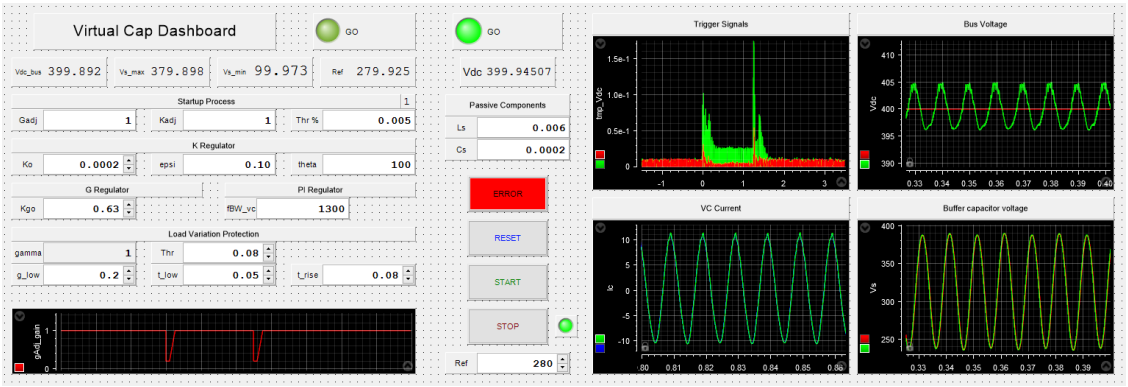


Figure 4.2: Virtual capacitor control panel created on ControlDesk.

Load: IT8332

In order to simulate the load on the converter an iTech IT8332 was used [26], a three-phase regenerative DC electronic load capable to simulate various load characteristics, and return the consumed energy back to the grid. It can be set to operate at constant power, voltage, current or resistance, or it can be programmed with transient load curves, as was done in our case.

Laboratory setup

The complete wired setup used in laboratory, composed of all the components discussed so far, is shown in Fig.4.3.

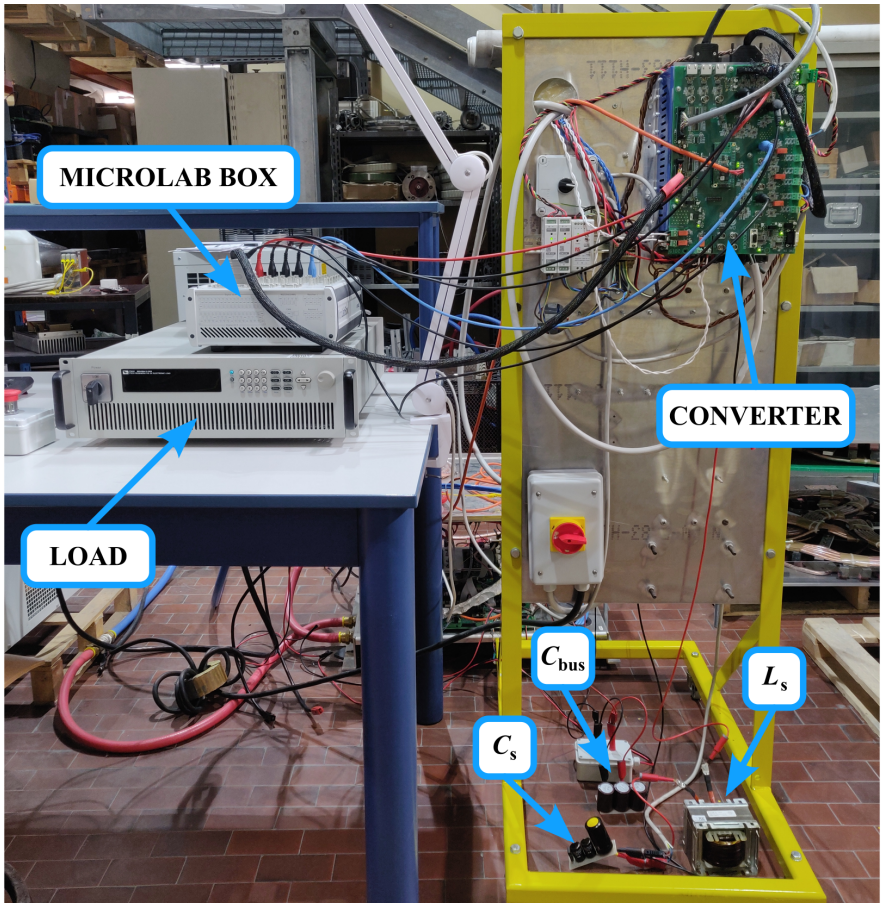


Figure 4.3: Experimental setup used for control validation.

4.2 Experimental Tests

Before going into the tests of the generation system, a general summary of the relevant parameters of the entire experimental set-up is presented.

TABLE 4.2: TEST SET-UP: ELECTRICAL PARAMETERS.

Grid side			
Grid voltage	$V_{g,RMS}$	230	$[V]$
Grid frequency	f_g	50	$[Hz]$
Precharge resistance	R_{pre}	15	$[\Omega]$
Filter capacitance	C_f	5	$[\mu F]$
Filter inductance (2x)	L_f	2	$[mH]$
Inverter			
Switching frequency	f_{sw}	20	$[kHz]$
DC-Link capacitance	C_{bus}	210	$[\mu F]$
Dead Time	t_DT	1.1	$[\mu s]$
Virtual Capacitor			
Auxiliary inductance	L_s	6	$[mH]$
Buffer capacitance	C_s	220	$[\mu F]$

TABLE 4.3: TEST SET-UP: PFC CONTROL PARAMETERS.

Current Controller - P-Res			
Bandwidth frequency	$f_{BW,i}$	600	$[Hz]$
Resonant gain	K_{pr}	100	$[V/As]$
Resonant gain 5^{th}	K_{pr_5}	80	$[V/As]$
Resonant gain 7^{th}	K_{pr_7}	25	$[V/As]$
Voltage Controller - PI			
Bandwidth frequency	$f_{BW,i}$	80	$[Hz]$
Filter Gains			
Notch filter	K_{notch}	200	[ ]
PLL filter	K_{PLL}	210	[ ]

TABLE 4.4: TEST SET-UP: VC CONTROL PARAMETERS.

Current Controller - PI			
Bandwidth frequency	$f_{BW,vc}$	1300	$[Hz]$
G Regulator			
Static gain	K_{g0}	0.63	
High frequency gain	b	20.25	
Frequency range start	$1/\tau$	$2\pi 25$	$[rad/s]$
K Regulator			
Static gain	$K0$	0.0002	[A/V]
Frequency range start	$1/\theta$	$2\pi 100$	[rad/s]
High freq. attenuation	ϵ	0.1	

As we can see from Table 4.3, in the testing phase it was decided to add two resonant branches to the PFC current control, dedicated respectively to the fifth and seventh harmonic, to improve the waveform of the current absorbed from the grid.

4.2.1 Test 1: PLL Performance

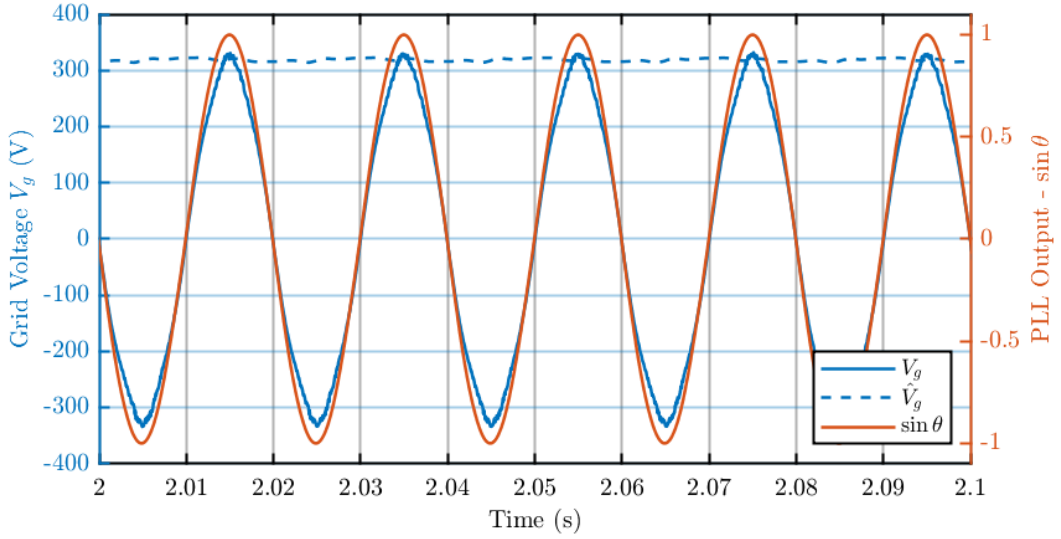


Figure 4.4: Comparison between the voltage grid V_g and the grid angle obtained from the PLL. The dashed line is the Voltage grid peak $\hat{V}_g$ calculated inside the PLL block.

The first test performed concerns the filtering performance of the PLL, to be sure that the angle and the peak value used for generating the current reference are clean. As we can see in Fig.4.4, although the mains voltage presents a certain level of distortion, the angle obtained from the PLL filtering effect turns out to be a clean sinusoid, and the peak value remains constant in an acceptable range of values.

4.2.2 Test 2: Charging of the DC-Link and System Startup

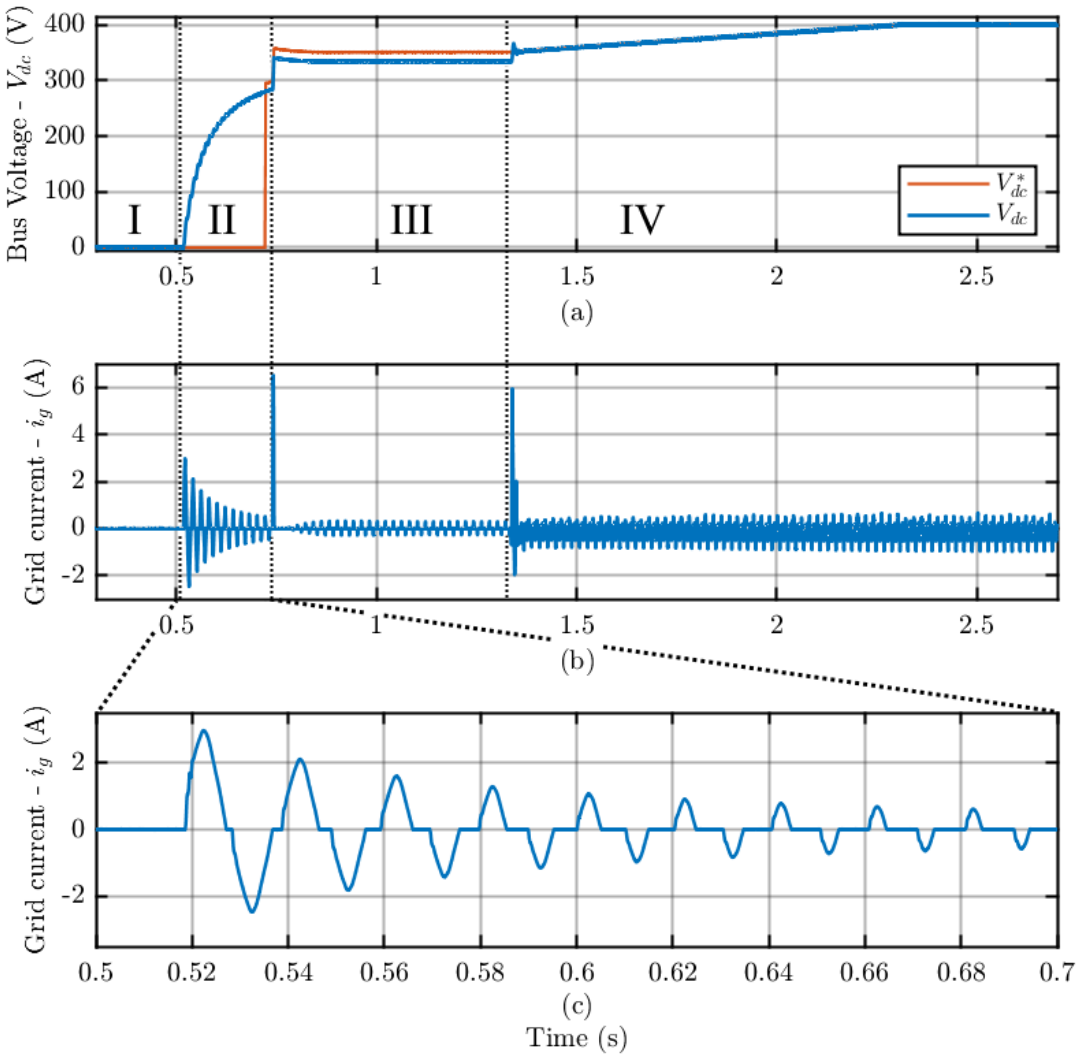


Figure 4.5: Bus Voltage (a) and grid current (b) in precharge and startup process. (c) shows the current in detail during precharge.

The second test to be carried out concerns the start-up of the system through the precharge of the DC-link capacitor and until the continuous voltage is reached at the reference value. From the results obtained shown in Fig.4.5 it can be observed that the start-up procedure is carried out as expected. The "error" state (I) is followed by the phase of pre-charge of the capacitor (II): in this phase the body diodes of the open switches behave as full bridge rectifier and charge the capacitor up to 280 V, while the current is limited by the pre-charge resistance. in Fig.4.5.c the typical waveform of a current entering a diode bridge can be clearly seen. Reached the value of 280 V, the PFC goes into the "ready" state (III): the reference voltage is kept 5% higher than the bus voltage while waiting for the "Go" command. In the "Go" State (IV) the ramp reference is given to the control, up to the steady state value equal to $V^*_{dc} = 400\ V$.

4.2.3 Test 3: Load Variation on the PFC

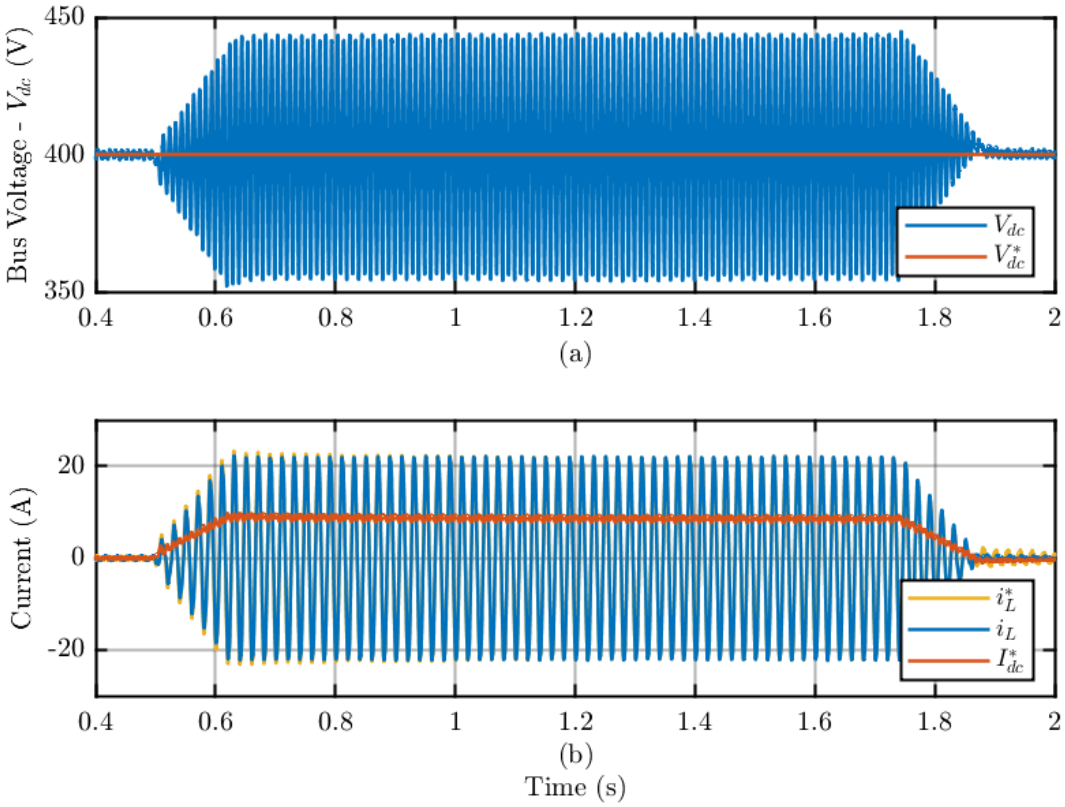


Figure 4.6: Bus voltage along with its reference (a) and grid current along with its reference and with the DC current reference during a load variation.

This test is useful to verify that the voltage control on the DC-link is effective and is able to manage load variations and follow the set reference, starting from a steady state condition. The imposed load is 8.25 A (3.3 kW) pulse of a duration of 1.25 s, with an upward and downward slope equal to 50 A/s in module.

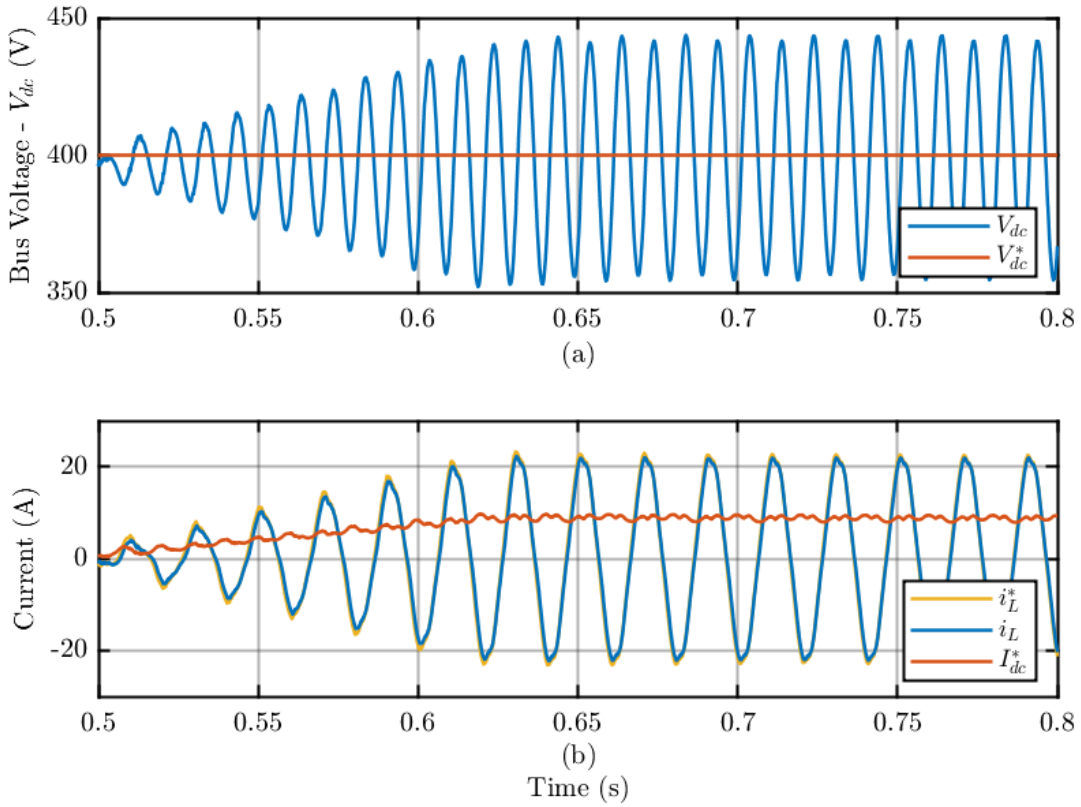


Figure 4.7: Detail of bus voltage along with its reference (a) and grid current along with its reference and with the DC current reference during a load variation.

From Fig.4.6 it is possible to see all the transient, while fig.4.7 focuses in detail on the load taking. It is clearly visible how the voltage loop is able to maintain the average value of the bus voltage at the reference value, but with high amplitude second harmonic oscillations. The current reference is also followed quickly, but has some irregularities that generate slight distortions in the absorbed phase current. These are mainly due to the grid voltage distortion which is reflected in the peak value calculated by the PLL, and used to generate the reference, and to the presence of unwanted inductances in the test setup. The THD calculated on the network current is equal to 3.8%.

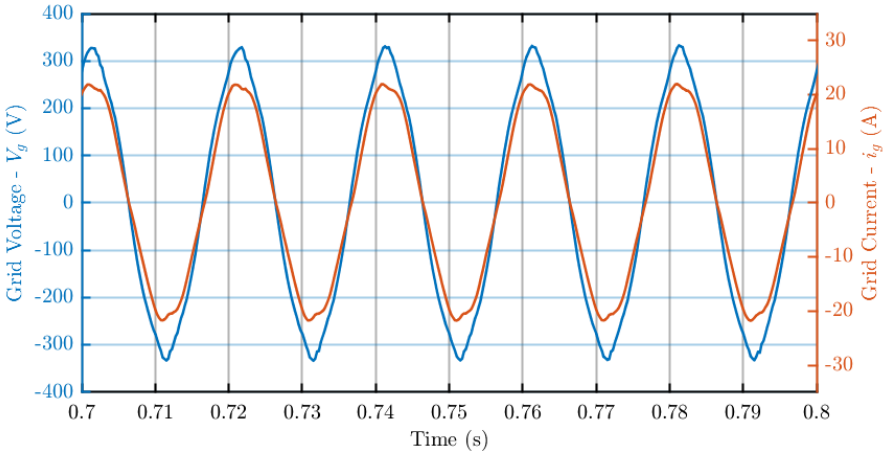


Figure 4.8: Comparison between the voltage and current waveforms on the grid side of the converter.

4.2.4 Test 4: Precharge and Startup Phases of the Virtual Capacitor

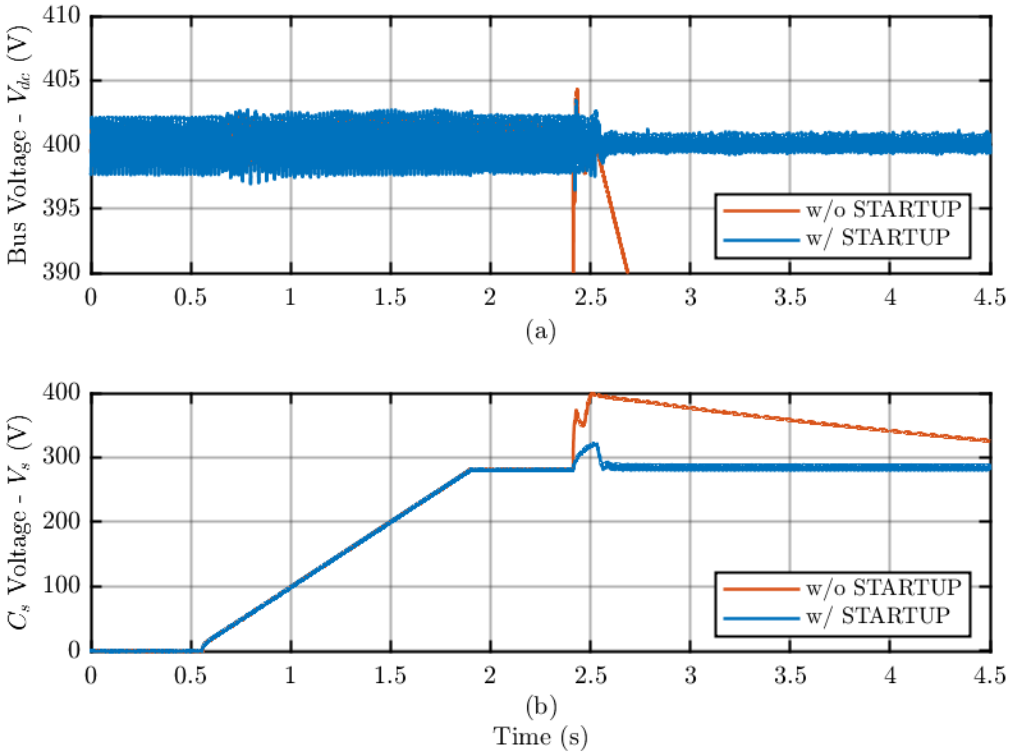


Figure 4.9: Comparison of the start-up process with and without the STARTUP state.

The next test concerns the starting of the virtual capacitor, then the passage from the ERROR state to the GO state, passing through pre-charge with variable duty and the phase with damped gains. As can be seen in Fig.4.9, starting directly from the PRECHARGE state to the GO state generates a condition of instability due to the absence of damping elements (red signal $@t = 0.24\ s$), leading the system to go into protection for overvoltage on the buffer capacitor. With the STARTUP phase, on the other hand, the response is dampened enough so that the system equilibrium is not lost, and the virtual capacitor starts up without problems at $@t = 0.26\ s$.

As soon as it is started, it is possible to see how the capacitive nature of the control affects the oscillations present on the DC-bus (Fig.4.9.a).

4.2.5 Test 5: Load Variation on the DC-bus with Virtual Capacitor

In this test, the control of the virtual capacitor is tested with a load variation equal to that described in the previous section, so a 8.25 A (3.3 kW $@V_{dc} = 400\ V$) pulse of a duration of 1.25 s, with an upward and downward slope equal to 50 A/s in module.

In Fig.4.10 we can see how the total transient, while in Fig.4.11 the steady-state waveforms are shown. It can be seen how the steady state ripple is significantly reduced, as it passes from a value of about 85V peak-to-peak to a value of about 10V peak-to-peak.

Based on this last value, it is possible to calculate the equivalent capacity seen by the system as it was done for the results of the simulations in paragraph 3.2.2 with (3.4), thus obtaining

$$C_{eq} = 2.85\ mF$$

Meaning that the total capacitance seen from the system is 6.6 times the real capacitance installed in the circuit. The effects are also detectable on the grid current (Fig.4.11.b) which has a less distorted shape than in the previous tests, in fact the calculated THD drops to 2.5%.

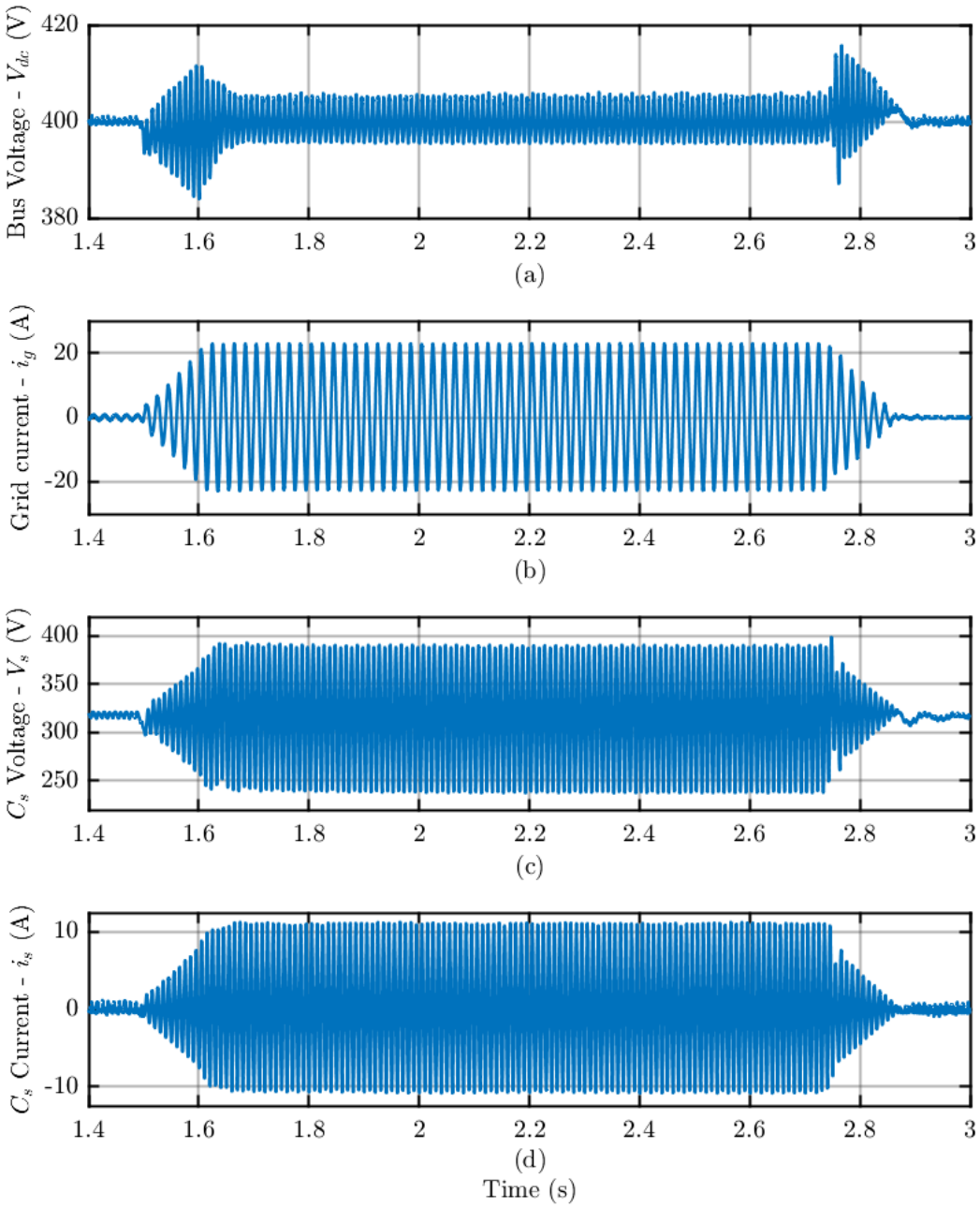


Figure 4.10: Complete effect of a load pulse variation on the DC-bus voltage (a), on the grid current (b), on the buffer capacitor voltage (c) and current (d).

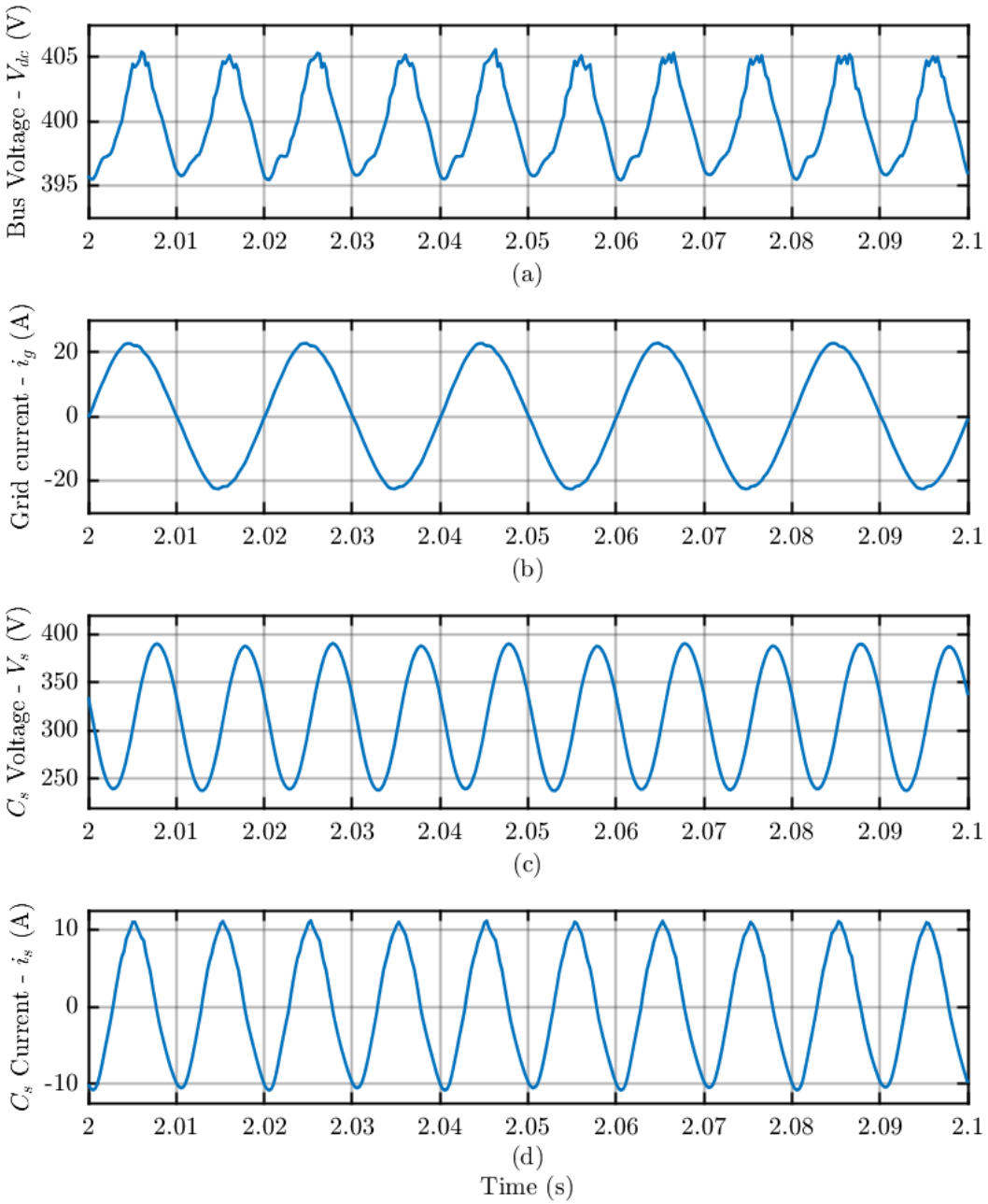


Figure 4.11: Steady state waveforms on the DC-bus voltage(a), on the grid current (b), on the buffer capacitor voltage (c) and current (d) with a 3.3 kW load.

In Fig.4.12 we can see, instead, a detail on the functioning of the protection for the load variation described in section 2.2.

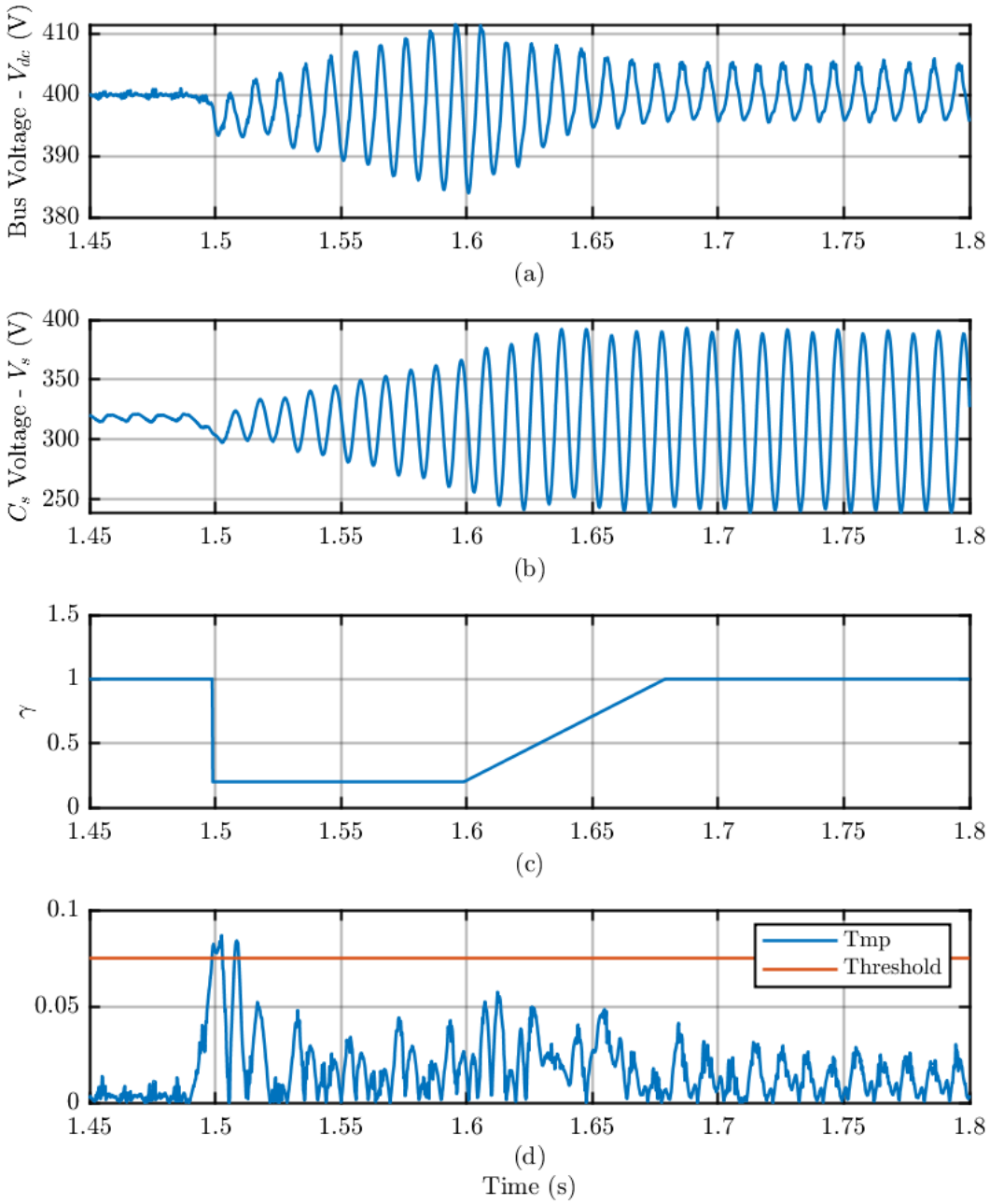


Figure 4.12: Load Variation Protection triggered at the transient start: effect on the DC-bus voltage (a) and on the buffer capacitor voltage (b). The variation of the signal γ is shown in (c) and the triggering signal Tmp in (d).

It can be easily spotted how, when the load variation causes the DC-bus voltage to drop, the peak on the Tmp signal exceeds the threshold value triggering the reduction of γ and, consequently, the reduction of the high frequency channel of the regulator G. This prevents V_s from going out of the working range but causes a temporary increase of the ripple on the DC-bus. When γ starts to rise again ($@t = 1.6\ s$) the ripple on the DC-bus is reduced accordingly. The same thing happens when the load is disconnected $@t = 2.7\ s$.

4.2.6 Test 6: Disconnection of the Virtual Capacitor During Load

For this next test it was decided to try to disconnect the virtual capacitor under load. This test was carried out both to better visualize the difference of a DC bus under load with and without Virtual capacitor, and to test the soft-stop implemented in the state machine. In case of "Stop" signal, in fact, to avoid stressing too much the PFC control, the system impose a duty with in the form of a decreasing ramp, starting from the last calculated duty to a value equal to zero.

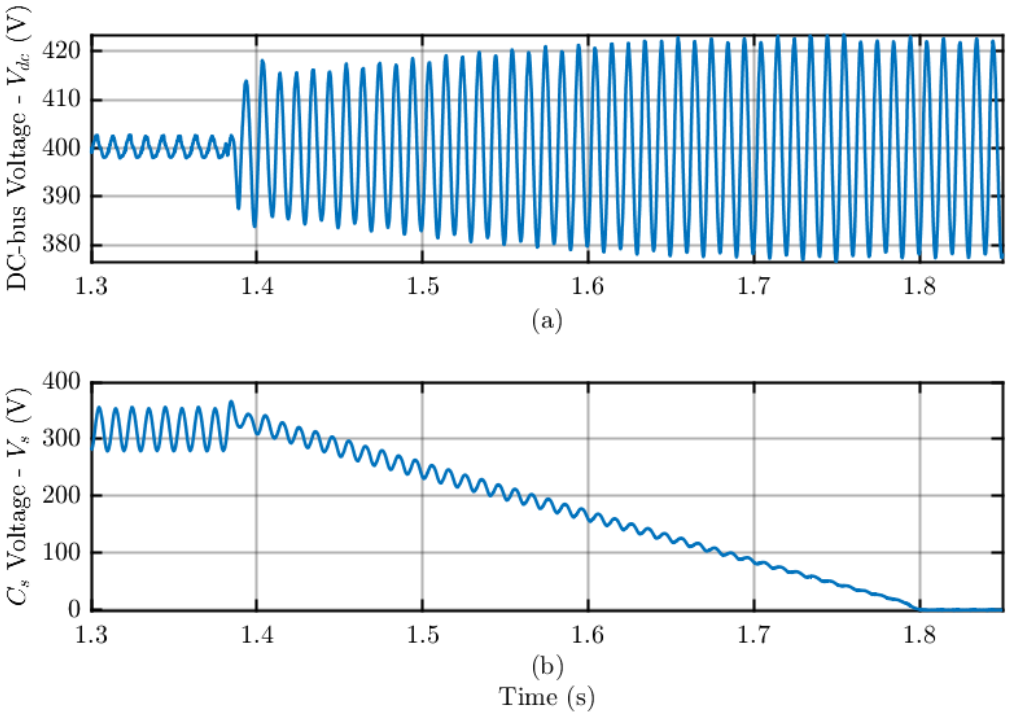


Figure 4.13: Shutdown of the virtual capacitor under load conditions: in (b) we can see how C_s discharges linearly, while in (a) the effects on the DC bus voltage are shown.

In this way the buffer capacitor is slowly discharged and eventual occurrences of overvoltages on the DC bus are avoided. The test shown in Fig4.13 has been carried out with a load of 1.7 kW (4.25 A), which means a peak-to-peak value equal to $\Delta V = 5\ V$ on the DC bus with the virtual capacitor activated. When it is turned off @$t = 1.38\ s$ we can see how the voltage on C_s decrease linearly while the amplitude of the DC bus voltage ripple increase up to a value equal to $\Delta V = 48\ V$.

4.2.7 Comparison of Capacity Utilization Between Active and Passive Method

At this point the setup has been changed and the buffer capacitor C_s has been connected in parallel to C_{bus}, obtaining a DC link with a total capacitance equal to $C'_{bus} = C_{bus}+C_s = 430\mu F$ and the modulation on the virtual capacitor leg has been disabled. The same load variation with respect to Test 5 has then been applied and the comparison between the two transient is shown in Fig.4.14.

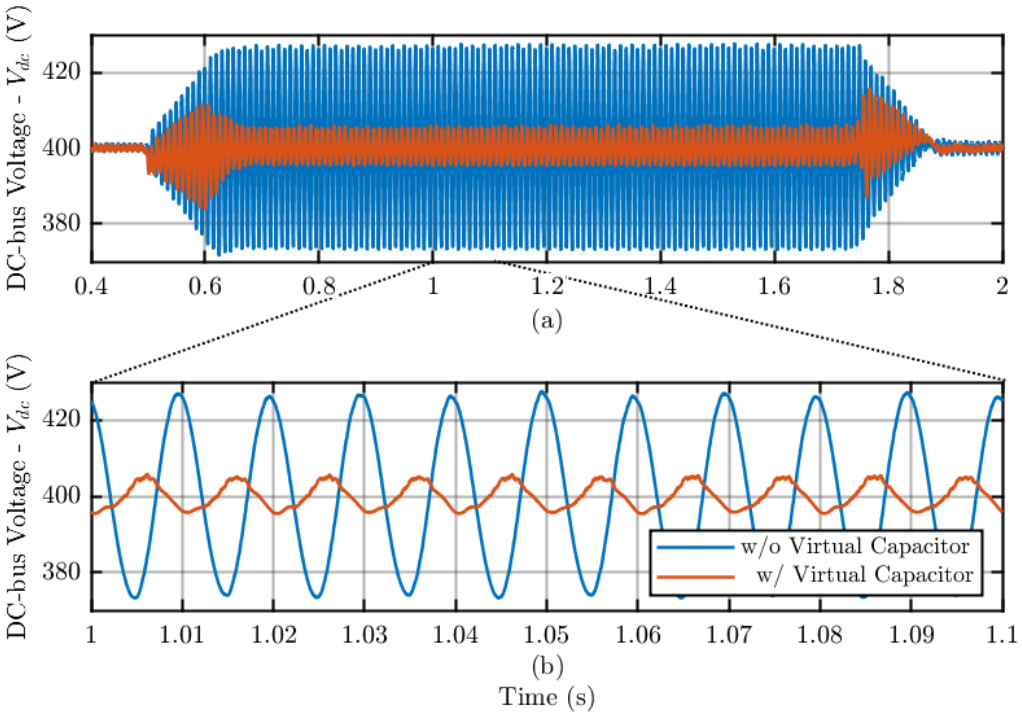


Figure 4.14: Comparison between classic DC-Link and Virtual Capacitor approach: in (a) we can see all the transient while in (b) a zoomed version at steady state is shown.

From Fig.4.14 it can be clearly seen how the difference in the use of capacitance through a passive (DC-link) and an active (virtual capacitor) method involves better exploitation of the capacitance used in the system, resulting in a ripple difference from 60 V to 10 V peak to peak on the DC bus voltage.

Conclusions

In this thesis, the sizing and control selection phases for an active AC/DC converter with boost PFC stage and for a virtual capacitor were presented, simulated and finally validated through experimental tests in the laboratory.

During the experiments in the laboratory we encountered problems due to the non-ideality of the system, such as oscillations due to parasitic inductances in the connections made, which were mitigated by inserting filters ad hoc.

The results obtained during the experimentation in the laboratory have validated the design and control of the device which has good characteristics both in terms of steady-state and dynamic performance, thanks to the load variation protection, for a plug'n'play type of use. Anyway, a big limitation of the implemented system is given by the switching frequency, which limits the dynamic of the controller, forcing us to act on the average value of V_s to store ripple energy instead of on its oscillations amplitude.

Further improvements can be made in the future using a MOSFET type technology that would allow to implement the control with a higher switching frequency and lower dead time, thus reducing the distortions on the bus voltage and the size of the auxiliary inductance. Surely that of the virtual capacitor is confirmed to be a valid alternative to better exploit the total capacitance of a system and therefore improve its power density.

To obtain this result it was necessary to follow progressive steps, preliminary to the experimentation of the set-up in the laboratory. In particular, my personal contributions to the thesis were:

- Study of the literature concerning active AC/DC conversion, which allowed me to

model the PFC converter, calibrate the voltage and current loops and analyze the ripple energy nature on the DC side of the converter.

- Study of the literature concerning active impedances and the control strategies applied to them, thanks to which I was able to adapt the control for the designed device and size the components necessary for its operation.
- Definition of the control logic to be implemented separately on the two devices (PFC and VC) with consequent writing of the code in C language for the control of the PFC and for a Plug'n'Play use of the virtual capacitor.
- Modelling of the constituent elements of the system and validation of the models and control strategies by means of simulations, both electrical and thermal, in the PLECS environment, through specific tests according to the experimental study.
- Realization of the experimental set-up and adaptation of software elements, such as control code in MATLAB/Simulink, setting of the inputs/outputs of the dSpace interface platform.
- Laboratory experimentation of the PFC + VC system to determine its correct functioning, thus validating the simulation model and allowing a study of the real characteristics.

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