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Master's Degree in Biomedical Engineering



Master's Degree Thesis

Biocomputing models of combinatorial and sequential logic circuits using neuron-astrocyte networks

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Abstract

Biocomputing is a novel research area, in which biological entities are manipulated to perform computations. The highly specialized mechanisms that neurons adopt to elaborate thousands of synaptic signals could make them an outstanding platform to realize such technologies. Hence, recently researchers have been attracted by the possibility of designing logic gates and digital circuits with neurons. Several challenges arise from this ambition, mainly associated to the stochastic nature and noise of neural signalling. Additionally, there is still a partial lack of comprehension related to the processes of encoding/decoding of neural information. Therefore, the search of strategies that could make these systems more controllable is crucial. Since it has been demonstrated that astrocytes play a fundamental role in the regulation of neural activity, these could be employed to increase the reliability of neuronal biocomputing systems. Furthermore, the computing power of traditional digital devices is made possible also by the use of memory elements, realised through sequential logic circuits. However, most of the efforts in literature concentrate about the implementation of combinatorial logic, while the development of sequential circuits with neurons has been only partially investigated.

In this thesis we propose a mathematical model of neuronal logic gates based on Izhikevich model. First, neural OR and AND gates are developed by regulating the synaptic strengths. These systems are further coupled with astrocytes feedback through the tripartite synapse model by Postnov et al., in order to achieve improved gating robustness. Bit error ratio and accuracy are used to assess the OR and AND gates performances at different synaptic gaussian noise levels. Then a larger library of neural logic gates, comprising buffer AND NOT, NOT and NAND gates, is developed exploiting synaptic inhibition. These building blocks are after connected together to realise sequential circuits, both asynchronous and synchronous, including SR latch, gated SR latch and D flip-flop. Finally, the initial validation of their operability with increased firing frequency is provided.

Our results demonstrate the effectiveness of astrocytes regulating activity as denoising mechanism. Furthermore, we initially validate that sequential circuits can be built with interconnected neuronal logic blocks, representing an outstanding chance for developing extremely elaborate biocomputing systems. The examination of the current model could give useful insight about how biological cells can be engineered to perform computations and could be taken as inspiration for further in-vitro experiments. The development of neuronal biocomputing systems will pave the way for the realisation of innovative medical technologies, as neuroprosthesis and neuronal implantable chips, directly made by biological cells. Hence these devices will display optimal biocompatibility and will be able to treat diseases by restoring the altered physiological communication of biological cells.

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Chapter 1 Introduction

1.1 Motivations

Since the dawn of computer science, scientists have always been fascinated by the brain capabilities of performing computations. Our brain constantly receives many sensory stimuli from the external environment, rapidly processes them to take decisions that allow the actuation of complex tasks. As an example, when we grab an object, our nervous system integrates the information coming from the visual system and the tactile mechanoreceptors located in our hand and regulates the response based on the shape and the fragility of the object. This allows us both to hold a stone, or an egg without breaking it, a complex problem that is still challenging for robotic hands. Moreover this is simultaneously executed during several ongoing involuntary processes, as regulation of heart and respiratory rate, with an high level of parallelism. Even if neurons are slower respect modern computers, brain computational rate exceed computers, thanks to the extremely high level of connectivity [1]. This result could also be related to the fact that the brain is a much more flexible computational system than computers. Indeed the nervous system displays convenient features as concurrency, fault-tolerance and adaptive learning [1].

Although the principles that govern our nervous system remain not fully understood, existing knowledge of the human brain has influenced information and communication technologies (ICT) from many points of view. The development of artificial intelligence systems (AI) which try to replicate typical brain learning and problem solving mechanisms, has displayed a strong impact on most engineering technologies. Artificial neural networks (ANN) could be considered the most representative example of bio-inspired computing system and constitute one of the most powerful tools of machine learning.

In their pioneering work published in 1943 [2], McCulloch and Pitts theorized

that the brain could be modelled using simple interconnected building blocks, which symbolize the neurons. Each of them is described using boolean algebra and, based on thresholding functions, they manage to perform logical operation as logic AND and logic OR. This constitutes the first attempt to formalize neurons as computing units with logic gating capabilities.

Interestingly, the fundamental computational units of digital electronics, the logic gates, and the physiological units of the nervous systems, the neurons, share some similarities [1]. In digital electronics, any digital circuit can be built using the same basic logic gates as building blocks. Similarly, neurons, keeping the same principles of operation, i.e. the action potential generation, menage to realize diverse cognitive mechanisms. Furthermore, both of them constitute information processing systems that receive multiple inputs and produce a single output. Nevertheless, the number of inputs tolerated by a unit (fan-in) and the number of units that could be driven by an output (fan-out) are much larger in the nervous system respect digital electronics, reaching values in the range 1000-10000. Another difference is represented by the fact that the internal dynamic of neurons is much more complex than the logic gate's one. Specifically logic gates can be considered static, meaning that outputs are well-defined respect input's values. Instead neurons internal state is influenced by a large number of variables, as inputs synchronization, proximity with the sender neuron, characteristic of the synapses, etc.

Based on the outstanding computational capabilities of the human brain, the question arises whether it could be possible for science to use neurons, in a controllable manner, similar to what is done with logic gates. This could open the frontier for the development of biological computing systems, by applying the computing tools of digital electronics into the biological nervous system. *Biocomputing* is a novel research paradigm which try to manipulate biological entities, as neurons, through synthetic biology techniques, to perform human defined computations [3].

But why could engineers be interested in realizing computer-like systems using biological cells? In the future such technologies may lead to the development of innovative biomedical solutions acting at cellular level. Neurodegenerative diseases are provoked by the progressive loss of functionality of specific neurons populations. Especially engineered cells with biocomputing abilities could be implanted to restore the physiological behaviour by directly communicating with the ill cells. Furthermore, in the last years we have seen the rising in the interest of the scientific community in the design of brain implantable chips. The application of these technologies are various, among all, brain stimulators used as neurodiseases therapies, brain computer interfaces or neuroprosthesis. The research on neuron biocomputing could open the frontiers for the development of innovative brain chips entirely made by reprogrammed cells.

Why devices made by cells could provide an alternative to traditional silicon chips? In the same manner as research on tissue engineering is trying to do, fully

biocompatible solutions could be developed by engineered cells directly extracted from the patient. Additionally, the use of the same biological medium could overcome the difficulties related to the interface between electronics and biological tissues, which often cause the lost of performances of the device and the aggressive response of the biological environment respect the device, followed by the final rejection of the device.

The starting point toward the realization of neuron biocomputing technologies is the development of logic gates, the basic units of digital electronics, made by neurons. A neuronal logic gates should be composed by a network of neurons, in which the input signals are generated by a first layer of neurons, elaborated according to the graph of synaptic connections and eventually by other intermediate layers of neurons, and finally mapped into outputs by an output layer of neurons. The input-output relationship should follow the logic rules defined by Boolean algebra. If a such device could be developed, neuronal logic gates could be used as building blocks, and larger computing systems could be realized by cascading multiple modules.

Several challenges arise toward the realization of neuronal logic gates. We mainly address to the following three types of issues.

- Stochastic nature of neurons signalling: neurons signalling is intrinsically stochastic and can be understood only using a probabilistic approach. As a consequence, from the same input values, different output responses could be elicited. Furthermore, in biological networks, neurons can also fire without any synaptic inputs [4] and with poor synchronization, resulting in an enormous background noise that make difficult to process neuronal messages.
- Control over synaptic connections: biological neuronal networks display high levels of connectivity. The development of synaptic connections is ruled by complex activity-dependent mechanisms. Therefore controlling the topology of in-vitro biological network constitutes a complex task. However, this could be required for designing neuronal network that behave accordingly to a desired logic response.
- Dynamics of membrane excitability: while for digital logic gate fixed thresholds can be used to define the logic outputs, neuronal dynamics are much more complex. As will be further discussed in Section 1.2, neuron excitation both depends on the number of received inputs and also on their frequency, due to the spatial and temporal summation mechanisms. Consequently, if the operating frequency does not belong to a certain range, the neuronal gate could not follow the expected logic function.

In this thesis we will investigate about the design of networks of cells belonging to the nervous system, in which input spike patterns are mapped in output spike patterns following predefined logic gating relationships. The instruments of mathematical modelling will be used to capture valuable information about the dynamics of neuronal logic gates, and define an effective design paradigm that can be used to build such complex systems.

1.2 A biological framework of neurons signalling

1.2.1 Neurons electrophysiology

Neurons can be considered as the fundamental computational unit of human nervous system. The brain is organised as an enormous network architecture made by billions of these elementary units. Each of them receives incoming input signals from other units, elaborates them and produces an output. This output is generated in the form of brief sudden electrical impulses called *action potentials* (APs).

To obtain a better understanding about the nature of these neuron signals, first we will focus on their relationships with the electrical properties of the cell membrane. When neurons are at rest, a stable difference in the electrical potential between the two sides of the membrane is maintained. This stable state is called the *resting membrane potential* and its typical values are in the range between -60 and -70 mV [4]. The resting potential is associated to the continuous action of protein pumps, that keep an unequal distribution of ion species (K⁺ and Na⁺) at the extremities of the membrane. Variations in the membrane potential occur when the neuron receives electrical stimuli from the other cells. Specifically, an excitatory stimulus produces an increase in the potential, called *depolarization*, which enhances the cell's probability to fire an AP. In constrast, an inhibitory stimulus produces a negative deflection respect the baseline, i.e. *hyperpolarization*, and reduces the firing probability. When the membrane potential exceeds a critical threshold, an AP is generated.

Action potentials are often defined as *all-or-none* signals [4]. This means that neurons can only spike or not spike, because if an AP is generated it has always the same amplitude. A further increase in the amplitude of a suprathreshold input does not influence the amplitude of APs, but rather the frequency of the sequence of spikes (called train of APs). Instead the duration of the stimulus is proportional to the number of APs elicited [4]. Therefore the information of neuronal signalling is not represented by the amplitude of APs, but instead in their timing, number and frequency.

1.2.2 Bipartite synapses

Once understood which are the signals used by neuron to convey the information, now we will focus on how this information can be transmitted between more neurons. Neuron communication is made possible by the presence of specialized structures called *synapses*. We refer to the neuron which transmits the message as *presynaptic neuron*, while the receiver neuron is called *postsynaptic neuron*. Synapses involving only these two kind of 'actors' are often called *bipartite synapse*, differently from the case that will be discussed in the next Subsection, in which another type of cell come into play.

The most common class of bipartite synapse, namely chemical synapses, make use of neurotransmitters, which are substances that act as chemical messengers. The firing of the presynaptic neuron triggers its release of neurotransmitter, which reaches the receptors located in the postsynaptic neuron. This chemical bond influences the permeability of ions channels located on the postsynaptic cell. Hence, the postsynaptic membrane potential is affected, eliciting a subthreshold signal called *postsynaptic potential*. Depending on the type of neurotransmitter and receptors, this signal can be either a small depolarization, namely excitatory postsynaptic potential (EPSP), or a small hyperpolarization, called inhibitory postsynaptic potential (IPSP). The generation of an AP can not be triggered by a single EPSP, but rather requires many of them. At the same time, IPSPs prevent the firing. Therefore the neuron needs to evaluate the contribution of all the receiving inputs and decide if firing an AP or not. This is what is called *neuronal integration.* It can be seen as a "voting" mechanism, in which each EPSP represents a positive contribution that increases the firing probability, while each IPSP represents a negative contribution that decrease this probability. Neuronal integration is based on two concurrent mechanisms, the *temporal summation* and the *spatial summation*. The temporal summation occurs due to repeated stimuli coming from the same presynaptic neuron. If a first EPSP does not totally decay by the time the second EPSP is generated, the two effects are summed together, and the firing threshold can be reached. We refer instead as spatial summation to the integration of inputs coming from many presynaptic neurons acting on the same postsynaptic neuron. Furthermore, each synapse can be characterised with its on strength in increasing or decreasing the postsynaptic membrane potential and this can be enhanced or weakened by cellular activity. This phenomenon, called synaptic plasticity, is fundamental for complex brain functions related to memory and learning.

As previously anticipated, different species of neurotransmitter participate in the transmission of the chemical information. Chemical neurotransmitters can directly or indirectly affect the opening of ion channels, depending on their complementary receptor [4]. Ionotropic receptors are part of the channels that they regulate, and the binding with the neurotransmitter induces a conformational change in the receptor structure that provokes the channel opening. On the other hand, metabotropic receptors are distinct from the channels, and their regulation function is performed indirectly through the activation of second messengers. The latter process generally

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takes more time. Based on the ion species associated to the specific channel, its opening can have an excitatory or inhibitory effect on the postsynaptic cell. Even though most neurotransmitters can bind with both excitatory or inhibitory receptors [4], some of them prefer to perform their action in one of the two types. The major excitatory neurotransmitter is the glutamate, which predominantly act on ionotropic receptors AMPA and NMDA [5]. Even if both AMPA and NMDA are ionotropic receptors, NMDA are considerably slower. Instead most of the inhibitory synapses involve a neurotransmitter called GABA (γ -aminobutyric acid). This one can operate ionotropically on GABA_A receptors or metabotropically on GABA_B receptors.

1.2.3 Tripartite synapses

Our nervous system is not only populated by neurons, but also by non-excitable cells called neuroglia. Astrocytes are a specific type of glial cells, which mainly fulfill supplementary functions respect to neurons. Specifically their main roles include providing structural support to neurons, supplying them with nutrients and oxygen, insulate them and protect them from pathogens through the blood-brain barrier (BBB). Even though astrocytes have long been thought as passive elements, recently it has been demonstrated that they can also directly communicate with neurons and regulate their activity [6][7][8]. In particular, they are able to modulate the amount of neurotransmitter released in the synaptic cleft, contributing to the synaptic current regulation and providing feedback to the neuronal activity. Recent experiments demonstrated that astrocyte activity does not simply mirror neurons patterns but seems to produce frequency or amplitude modulation of the neuronal activity [9]. The functional unit involving a presynaptic neuron, a postsynaptic neuron and an astrocyte is defined as *tripartite synapse* [6].

As previously observed, astrocytes are non-excitable cells, meaning that they are not able to generate APs, but instead they encode information through oscillations in Ca^{2+} concentration. This ionic messenger is mainly stored inside an organelle structure called endoplasmic reticulum (ER). Considering a tripartite synapse, the presynaptic firing induces the release of glutamate in the synaptic cleft. The glutamate binding to astrocyte receptors triggers astrocyte activity. At that point a secondary signalling molecules, called 1,4,5-trisphosphate (IP3), is involved. Indeed the IP3 intracellular concentration increases [9]. As a consequence, IP3 binds the receptors placed on the astrocyte endoplasmic reticulum and Ca^{2+} is realised from the ER to the cytoplasm. Since the opening of IP3 channels increases with increasing Ca^{2+} concentrations, this leads to a self-amplifying release mechanism, called calcium-induced calcium release (CICR). With high Ca^{2+} concentrations, the astrocyte responds releasing 'glion mediators' (or 'glion transmitters'), which are excitatory neurotransmitters as ATP and glutamate. This contributes to the synaptic transmission [10] enabling a feedback mechanism. Moreover, this could be whether a positive or negative feedback, depending if the astrocyte mediator release happens near an excitatory or inhibitory interneuron [11]. Although several mediators are involved in the neuron-glion interaction, we can define two main pathways of astrocyte activation [12]: the slow activation pathway and the fast activation pathway. The previously explained mechanism of activation via IP3 production is defined as slow activation pathway. In addition astrocytes can be activated due to the increasing of K⁺ extracellular concentration. Since this astrocyte depolarisation can be considered instantaneous, this mechanism is called fast activation pathway. Even though the molecular pathways concerning neuronastrocyte communication are well defined, the physiological meaning of astrocyte signalling remains substantially not clear.

1.3 Research questions

In this thesis, a paradigm for the design of neuronal networks with logic gating responses will be investigated. This will be done through the use of numerical simulations, based on the versatile neuron model proposed by Eugene M. Izhikevich [13]. Main efforts will be associated to the design of a library of elementary neuronal logic gates, which can be further interconnected as building blocks for the realisation of larger digital-like circuits.

Through the thesis we will address to the following research questions.

1) Is there a network structure of Izhikevich neurons that manage to simulate OR and AND logic gates?

With the term 'network structure' we mean the graph that describes the network, characterized by the number of neurons and their interconnections. These are represented by the synapses, which information processing capability is mostly encoded in their synaptic strength. Thus neuronal logic gates can be differentiated based on the number of neurons, their linking and the regulations of the synaptic strengths.

- 2) Can tripartite synaptic transmission improve logic gates reliability? In Subsection 1.2.3 the mechanisms of regulation of neuronal activity played by astrocyte has been discussed. Hence tripartite synapses could be used as a strategy to design more controllable biocomputing solutions, addressing to the challenges related to the stochasticity of neuron signalling.
- 3) How can the network structure be modified to simulate other logic functions?

A large library of neuronal logic gates could be developed, further exploring physiological process involved in the nervous system, as the synaptic inhibition.

Otherwise, the examination of digital electronics principles could provide inspirations. Clearly, new logic functions could be achieved by cascading the existing ones, that means by interconnecting more neuronal logic gates together. Furthermore, digital tools as digital buffers could be exploited. These allow to increase the number of logic gates that can be driven by a logic gate output, and they are also used to restore degraded logic signals.

4) Can neuronal logic gates be connected to realise sequential circuits as latches and flip-flops?

Contrary to combinatorial logic, whose output is simply defined by the inputs at the present instant, in sequential logic the outputs depends also on the previous inputs values. That means that sequential logic has storage capabilities. All common digital devices serves of sequential circuits, to realize tasks that require memory, as for instance pipeline architectures, registers, counters and adders. The possibility of developing biocomputed circuits with data storage properties could pave the way to extremely powerful biocomputing technologies, toward the realization of biological finite-state machines. However, the actual state of art of neuronal biocomputing mostly includes examples of simple combinatorial circuits, while the development of much complex neuronal sequential circuits is only at the beginning.

1.4 Contributions

We summarise our main contributions as follows.

- 1) Design of neuronal OR/AND gates by synaptic weights regulation: our network consists in three Izhikevich neurons, with excitatory bipartite synapses described by a conductance-based model with instantaneous rise and single-exponential decay. The simulated neuronal responses display OR and AND gating, based on the chosen values of synaptic weights. Furthermore the logic gating is extended both to phasic and tonic spiking behaviours.
- 2) Astrocyte-based denoising of synaptic channel: the neuronal OR/AND gates are tested involving tripartite synapses described by the Postnov et al. model [14][12] modified using the aforementioned synaptic conductance-based model. We quantify the astrocyte-denoising effect using accuracy and bit error ratio (BER) at different levels of gaussian synaptic noise. The success of the denoising is validated by the significant increase in the accuracy and decrease in the BER.
- 3) Design of novel neuronal logic gates through AND NOT architecture, cascading and neuronal buffers: synaptic inhibition is used for the

modelling of AND NOT gate and NOT gate, as theorised by L. Yoder [15]. All bipartite synapses are modelled using the conductance-based model with synaptic conductance as difference of two exponentials. We simulate a neuronal NAND gate, by neuronal AND and NOT gates cascading. Furthermore, a strategy for input synchronization based on the use of neuronal buffers is here initially validated.

4) AND NOT gate-based sequential circuits: a realistic simulation of the neuronal SR latch, as formulated by L. Yoder [16], is achieved. Finally we propose and simulate the realisation of gated SR latch and D flip-flop, by the use of interconnected building blocks from our neuronal logic gate library. Additionally we demonstrate the functioning of the D flip-flop with increased firing frequency by re-adjusting the synaptic weights.

We plan to submit the following paper:

 Giulio Basso and Michael Taynnan Barros. "Biocomputing Model Using the Tripartite Synapses Provides Reliable Neuronal Logic Gating with Spike Pattern Diversity" - To be submitted to IEEE Transactions Selected Topics in Computing. 2022.

1.4.1 Summary of the thesis

In Chapter 2 we provide an overview about the state of art of biocomputing. We start by introducing the molecular communication paradigm used to carry biological information. After we investigate the origins of biocomputing and provide some examples, first based on DNA signalling within bacteria and then based on nervous system cells. Chapter 3 covers the main instruments of mathematical modelling required in our work, concerning the simulation of neurons, bipartite synapses, tripartite synapses and synaptic noise. Chapter 4 examines the proposed methods for the modelling of the simplest neuronal logic gates, that is the OR and AND gates. Here we start describing the proposed modifications of the tripartite synapses model and the general network structure adopted for both the gates. Afterwards, we focus on the realisation of the gates, first with bipartite and then with tripartite synapses. In Chapter 5 we illustrate the methods used for the design of the AND NOT-based gates and the sequential circuits. After describing the AND NOT gate and NOT model, we investigate the employ of cascading architecture and neuronal buffers, in relation to the neuronal NAND gate. Then these neuronal logic gates are combined for the development of sequential circuits. Chapter 6 reports the results of the simulations, which are then analysed in Chapter 7. Finally Chapter 8 concludes the work.

Chapter 2 Literature Review

2.1 Molecular communication

In biological systems, as cells, the information is exchanged and processed through sophisticated communications mechanisms, that allow the systems to make fundamental decisions, as differentiation, proliferation and apoptosis. These communications processes often employ molecules, and the chemical message is mainly encoded through the specific type of molecule and its concentration. A clear understanding and human control over biological communications mechanisms could represent an outstanding chance for the development of novel biomedical technologies, both for diagnostic and therapeutic purpose. Furthermore, since molecules live at the nanoscale, these processes could be exploited for *nanonetworks*, namely interconnections of nano-machines. Indeed at that scale, traditional electromagnetic technologies often fail due to issues related to the size and the power consumption [17]. For these reasons, the research interesting about communication mechanisms involved in nature is rising.

Molecular communication (MC) is a new bio-inspired paradigm of communication engineering that uses molecules to carry information between transmitters and receivers [18][17][19][20][21]. Examples of candidate information molecules are DNA/RNA strands, intracellular messengers as Ca^{2+} , neurotransmitters, hormones and other small proteins [21]. Among all effective reviews, Farsad et al. comprehensively analysed molecular communication using the formalism of traditional communication engineering [19]. Any communication system can be analyzed in its main components, namely the transmitter, the channel and the receiver. The transmitter is the device that generates the signal by encoding the information and sends it, the channel represents the environment in which the signal propagates, while the receiver is the device that collects and decodes the information. In MC, transmitter and receiver can be biological cells (e.g. presynaptic and postsynaptic neurons respectively), cells genetically engineered or artificial cells, i.e. simplified synthetic cells with well-controllable behaviours. The main function of the transmitter cell is the production and release of the information molecules. This can be engineered by manipulating the metabolic pathways of the cell, e.g. with viral vectors, which then synthesizes the desired signaling molecules. The channel is the biological aqueous or gaseous medium where the information particles propagate. The propagation to the receiver is made possible by biological transport processes as free diffusion, or flow assisted propagation. Afterwards, the receiver cell needs to show the receptors complementary to the information molecules. The receiver the chemical signals, acting as antennas in traditional communication engineering. Once the information molecules are captured, the receiver decodes the information contained in the signal.

An interesting example of such biological communication systems is depicted by neuronal communication. Communication in the nervous systems is mainly fulfilled via two types of propagation mechanisms, one that involves signalling within neurons, while the other concerning signalling between neurons [22, 23]. Therefore the transmitter and the receiver can be identified as two portions of the same neurons, or as the presynaptic and postsynaptic neurons. The channel can be abstracted as the neuron axon, or as a synaptic connection. The propagation within neurons takes place as action potentials that travel along neurons axons. These local changes in the electrical potential of the membrane are amplified by the presence of voltage gated ion channels (associated with K^+ and Na^+ ions), which open following a positive feedback mechanism that permits the propagation without attenuation. After the passage of the electrical wave, they remain closed during the so-called refractory period, that ensures the proceeding of signals in only one direction. The propagation between neurons occurs at the level of the synapses, through processes of reaction and diffusion. At chemical synapses, the signal is transmitted by the presynaptic neuron with the realising of neurotransmitter, which diffuses across the synaptic cleft until the binding with the receptors located on the postsynaptic membrane. The generation of the two forms of neuron signals marks the transduction between them. Action potentials generation is controlled by the opening of the voltage gated ion channels, which in turn are triggered by the binding of neurotransmitter. Symmetrically, when APs reach the axon terminal induce the fusion with the presynaptic outer membrane of the synaptic vesicles containing neurotransmitter, and so the release. Overall, the information is carried by the number and timing of action potential spikes. However, how this information is encoded and decoded by neurons is not completely understood. Evidences seems to show that the information is quantified in the number of spikes over some periods, or in the length of intervals with absence of spikes, or even in the frequency of spike trains. An experimental demonstration on how digital data can be externally transferred to an in vivo nervous system exploiting neuronal molecular

communication is depicted by [24]. In this work they managed to transmit digital signals into the nervous system of earthworms using electrical stimulation and analyzed the receiving signal which has propagated along the nerve cord.

The realisation of communication systems using biological principles results in several benefits. First of all, by using molecules already involved in biological systems, fully-biocompatible devices can be developed, overcoming the issues related to the aggressive response of the immune system respect the artificial implant. Additionally, biological communication exhibits an extraordinary high efficiency and low heat dissipation [25]. Since the reaction space in which this processes occur are at the nano-scale, time constants, as diffusion times, are significantly reduced, and therefore chemical reactions are facilitated. Moreover molecular communication devices could directly be supplied with the power coming from the catabolic physiological processes [19].

However, molecular communication research has to deal with many challenges. Compared with the performances of traditional electromagnetic technologies, molecular communication is considerably slower. For instance the speed of diffusion processes can be in the order of micrometers per millisecond [26]. Other remarkable issues are associated to the noise and stochastic nature of biological channels [27]. Molecules movements can be unpredictable, and noise can be introduced due to several phenomena, as the degradation of the information molecules or the interference with other molecules in the biological environment [28].

Nonetheless molecular communication technologies display numerous powerful applications in the biomedical field. As instance they can be used for both tumour diagnosis and therapy [29, 18]. The sensing of the concentrations of biomarkers, as proteins excessively produced by the abnormal cells, can be used to detect and assess the disease. As far as concern anti-tumour therapies, cancer cells can display specific receptors over-expressed respect the healthy cells, which can be exploited through ligand-receptor reactions to transport the anti-tumour drug in the target site, minimising the toxic effects in the surrounding healthy tissues. Other recent application of MC concerns regenerative engineering, where the control of cells differentiation, proliferation and migration can be obtained by manipulating cells communication processes [30]. Finally MC technologies may potentially be used to restored the impaired processing and transfer of information on the nervous system when affected by neurodegenerative diseases [31].

2.2 Biocomputing

Molecular Communication allows to transfer signals between bio-nanomachines. A further step toward the realization of powerful molecular technologies is represented by the possibility of making these devices process the received signals with elementary operations, i.e. *computations*. As observed in Section 1.1, this is the objective of a research area called *biocomputing*. Main research efforts are concerned with the developing of some sort of processing units, eventually located both on transmitters and receivers, which elaborate the biological inputs and produces an output according to predefined relationships [3].

Even though the concepts of making computations with atoms and molecules date back to the so-called "There's Plenty of Room at the Bottom" lecture by Richard Feynman in 1959 [32], the biocomputing principle was firstly actualized by Leonard Adleman in 1994 [33]. In its groundbreaking work, by showing the solution of the Hamiltonian paths problem using molecular operations with strands of DNA, he demonstrated the feasibility of implementing human-defined computations with molecules. Since that, numerous implementation of digital-like devices as switches, oscillators and logic gates have emerged. Most of the examples of biocomputing technologies presented in literature serve of proteins and DNA strands as information molecules. Indeed by controlling the genes transmitted between two bio-nanomachines, one could manipulate the synthesis of proteins and therefore the cells functionalities [21]. Prehoda et al. [34] pointed out that operations which can be interpreted as logic gating are already implemented in the biological environment. Specifically, the N-WASP protein, which contributes to the polymerisation during cell motility, manifests its activity only in the case in which two specific ligands bind together its domains. Since individually each of these ligands are weak activators, i.e. they are not able to elicit the N-WASP activation, but together yield potent activation, this protein circuit act similarly to an AND gate. This mechanism ispired Dueber et al. [35], who synthetically engineered the N-WASP managing to develop a library of gates, which includes several realisation of AND gate and OR gate. Even though these circuits of proteins exhibit an high flexibility for the design of biocomputing solutions, their outputs do not always result in simple binary responses, because they depend on the input proteins concentrations [35]. Therefore this could preclude the usage of the existing binary gating techniques.

DNA molecules are recognize as another possible candidate for the construction of biocomputing devices, because of the many operations that scientists are able to implement with them. Instances of such operations are the cut-and-paste, achievable through the use of restriction enzymes, the synthesis of target DNA strands, the exponential copying of DNA molecules with polymerase chain reaction (PCR) and the readout of DNA strands using the selective hybridization with probes [36]. An example of DNA biocomputing is provided in [37], in which they realized a DNA circuit capable of logic gate operations (AND, OR, XOR), with patterns of microRNA (miRNA) as inputs and fluorescence outputs.

Other biocomputing technologies regard the development of logic circuits using whole-cells, as bacteria. Moon et al. [38] developed an AND gate in Escherichia coli based on transcription factors, which are proteins that bind to specific sequences of DNA called promoter and regulate the transcription of the DNA into messenger RNA [39]. The AND gate receive as inputs two promoters and its output is still a promoter that can be used as input of another gate, enabling the design of cascaded structures. Since both input promoters are required for activating the output promoter expression, the gate behaves as an AND gate. A more complex transcriptional circuit is proposed in [40], in which they realized a toggle switch in Escherichia coli, using promoters in a mutual inhibitory network. The aforementioned results represent only few examples of the achievements of biocomputing through bacteria. Since prokaryotic cells could be considered as structurally simple organisms, a more challenging ambition is realizing such biocomputed solutions with eukaryotic cells as neurons.

2.3 Biocomputing with excitable cells

As previously anticipated in Chapter 1.1, researchers have tried to apply the biocomputing paradigm with cells belonging to the nervous system. Several contributions have been presented, most of them relying on the use of mathematical modelling (in-silico models), but also few attempts of in-vitro experiments has been investigated.

One of the first examples of in-silico model of logic gating realized with neurons, is represented by the work of T. P. Vogels and F. Abbott [41]. Although their main objectives concerned the understanding of signals propagation mechanisms within the brain, once established such signal transmission in networks of integrateand-fire neurons, they explored whether the networks could perform computations. Specifically, they built sparsely and randomly connected networks, they searched for candidate pathways in the networks and adjust their synaptic strengths achieving interesting computing circuits as NOT gate, switch, XOR gate and flip-flop. An attractive point of this work is the fact that they did not build the network architectures by hand, that is drawing the synaptic connections of the neurons, but rather found the logic circuits within random networks, adopting a solutions which may be also convenient in in-vitro experiments. One critical choice is that they encoded the logic levels through the firing frequency, namely AP trains with low frequencies are classified with the logic level 0, while trains with higher frequencies are classified with the logic level 1. Even if this rate coding is often considered a biologically plausible hypothesis belonging brain signal propagation, it is not effective for the biocomputing task, since the change in neurons frequency could not always be abrupt, and therefore it could be difficult to clearly define the state transitions [42]. More recently Adonias et al. [43, 44] defined mathematical models of neuronal logic gates, and they simulated their possible applications as a treatment for epileptic seizures. The logic gates were made by three neurons, described by the Hodgkin-Huxley model and using fixed synaptic strengths between neurons, but varying their connection probabilities. Their results demonstrated that the accuracy in performing the logic tasks decreases with increasing firing-rate levels. Although they developed a biologically detailed model of neurons, reproducing the morphological and electrical characteristics of specific neurons populations, they only implemented the simple AND and OR gates, without investigating more complex logic functions. A different strategy toward the development of neuronal logic gate is the one depicted in [42]. Here they adopted an encoding method in which each logic variable is represented by two distinct neurons. If the first of these, named Neuron 0, is firing, the logic variable is regarded as a logic 0, instead if the second neuron is firing, named Neuron 1, it is regarded as a logic 1. Based upon this encoding, they implemented a neuronal network of leaky-integrate-and-fire neurons, made by three layers, and with a supplementary teaching layer that is used to teach the network in reproducing the desired logic functions. Interestingly, in this training phase, the synaptic weights of the network were trained using the spike-timing-dependent plasticity rule (STDP). In that way they managed to develop all the principle logic gates (AND, OR, NAND, NOR, XOR, XNOR) and cascaded them to realize more complex combinatorial circuits as a rounding logic network of 8421-binary-coded decimal (BCD) code, an half adder and a full adder. However, they hardly simplified the model by using neurons which fire only single spikes, which is biologically unrealistic. Furthermore, their logic encoding is disadvantageous because it doubles the number of neurons required and it is also less intuitive than the much simpler encoding with the presence of APs as logic level 1 and the resting state as logic level 0. Another stimulating framework is presented in the work by L. Yoder [16]. Here he theorized a novel gate model made by three neurons with one inhibitory and one excitatory synapse, named neuronal AND NOT gate, and he designed a SR latch by connecting two these gates with mutual inhibitory feedback loops. Nevertheless, his theoretical methods have not been supported by simulations with realistic biological model of neurons. In our work we will take inspiration from this model, combined with more plausible neurons modelling, and further expand it toward the realization of other types of logic gates and more complex flip-flop circuits. Finally, with an approach more oriented toward machine learning applications, other models based on recurrent neuronal networks (RNN) have been presented, with examples of realization of numerous logic gates types (AND, OR, NOT, XOR, NOR, NAND, and XNOR)

[45] and also a 3-bit flip-flop [46].

As far as concern the applicability of logic gating techniques to in-vitro experiments, accomplishments have been already made by researchers. In [47], based on the observations that the neurons response latencies increase with ongoing stimulations, they proposed that the brain may consist in *dynamic logic gates* (DLGs), i.e. with time-dependent truth tables. With this hypothesis, they defined an experimental setup using in-vitro cortical cells and built AND, OR, NOT, XOR dynamic logic gates. The operating mode of the DLGs varies with the delay between inputs and outputs stimulations, that means that the desired logic functions is reproduced only within a certain range of delays. Furthermore, they originally defined the gates architecture using neuronal chains that are made by consecutive neurons connected in series. This solution seem enhancing the dynamic range of supported time-lags. Lastly, [48] addressed the biocomputing research using a different type of cells belonging to the nervous system, the astrocytes cells. They proposed an AND gate and OR gate implementation with astrocytes, engineered through synthetic genes to manipulate their Ca^{2+} signaling threshold. Moreover, a reinforced learning platform were implemented to optimize the Ca^{2+} activation level and the input transmission period that minimise the noise and the delay. Their methods were validated by wet-lab experiments involving human astrocytomas. From the literature analysis, it is clear that the research about the exciting themes of biocomputing is still at an early stage, and many other aspects need to be explored.

Chapter 3

Mathematical models of neurons electrophysiology

The processes of neuron electrical excitability are made possible by the presence of two main ion species, the Na^+ and K^+ ions. The typical shape of an action potential is illustrated in Fig. 3.1. At the resting state, the inner side of the neuron is characterized by a larger concentration of K^+ ions, while the outer side sees a higher concentration of Na⁺s, and this unbalanced condition is maintained by the Na^+/K^+ protein pumps. Whenever the neuron is sufficiently stimulated, the membrane depolarization causes the opening of the voltage-gated Na⁺ channels, which results in an inward Na⁺ current that further depolarize the cell. Therefore the membrane potential rapidly overshoots, leading to the well-known spike shape. The inactivation of Na⁺ channels, followed with some delay by the opening of K⁺ channels which similarly produces an outward current, causes the membrane repolarization. Afterward, a phase of hyperpolarization occurs, during which the membrane potential undershoots below the resting membrane potential, due to the slow dynamic that rules the K^+ channels closure. The process of generation of action potential is also characterized by the presence of a period of diminished excitability called refractory period. This is further subdivided into an initial absolute refractory period, during which it is impossible to re-excite the neuron, and a relative refractory period, during which a new AP can be generated only by a stronger stimulus.

In this Chapter we will summarize the primary mathematical instruments used to describe such dynamic of excitability. We will start by reviewing the first model of spike-generation, introduced by A. Hodgkin and A. Huxley in 1952 [50]. The historical importance of the Hodgkin-Huxley model (HH model) is attributed to the fact that for first it conceptualizes neurons as dynamical systems [51] and that many other models can be interpreted as simplified reformulation of HH model dynamics.



Figure 3.1: Voltage trace of an action potential and its physiological phases. (Source: [49])

For the treatise about this mathematical method we referred to [52]. After that, we will illustrate the much simpler Izhikevich model of spiking neuron [13]. Once understood how the membrane potential can be modelled, we will further explore some mathematical models of synaptic transmission through bipartite synapses [53][5] and tripartite synapses [14][12].

3.1 Hodgkin–Huxley model

Before illustrating the Hodgkin–Huxley model, we need to briefly introduce some concepts about channel gating, i.e. the dynamic of opening and closure of ion channels. A simple model of two-state channel is depicted by the following kinetic model:

$$C \stackrel{\alpha(v)}{\underset{\beta(v)}{\rightleftharpoons}} O$$

The channels can assume two alternative states, the open state (O) and the closed state (C); $\alpha(v)$ and $\beta(v)$ are the kinetic constants (with dimensions $[s^{-1}]$) that regulate the opening and closure of the channels respectively, and they depend on

the electrical membrane potential (for clarity this dependence with v will be later omitted). That means that the ionic channels can pass from the C state to the Ostate with a rate constant α and in the opposite direction with a rate constant β . Such dynamic process can be described by the following differential equation:

$$\dot{g} = \alpha(1-g) - \beta g \,, \tag{3.1}$$

where we denotes with g the proportion of channels in the O state, with \dot{g} its derivative respect the time, while 1 - g is the proportion of channels in the C state. Therefore the first term on the right side of Eq. 3.1 represents a source term and the second term is a sink of O channels. Equation 3.1 is often reformulated as follow:

$$\dot{g} = \frac{g_{\infty} - g}{\tau_g} \,, \tag{3.2}$$

defining

$$g_{\infty} = \frac{\alpha}{\alpha + \beta} \,, \tag{3.3}$$

$$\tau_g = \frac{1}{\alpha + \beta} \,. \tag{3.4}$$

According to Eq. 3.1 g tends towards a steady state following a first order law. However, physiological channels dynamics typically do not follow a such simple rule, but are rather described as made by multiple subunits, called *gates*. Each of them can be open or closed, and ions can pass through a channel if and only if all its gates are open. Thus the gates can be modelled with the previous two-state model. The potassium channels consists of four identical gates, defined *activation gates*, because their permeability increases with the depolarization. The conductance of K^+ ion channels can be formulated as:

$$g_K = \overline{g}_K n^4 \,, \tag{3.5}$$

$$\dot{n} = \alpha_n (1 - n) - \beta_n n \,, \tag{3.6}$$

with \overline{g}_K constant value. Since each gate is independent, and n can be interpreted as the probability to find one gate open, the channel opening probability is regarded as a joint probability, and so it is proportional to n^4 which is the product of the marginal probabilities. Instead the modelling of Na⁺ channels needs to account a second mechanism, called *inactivation*. Specifically the sodium channels are represented as made by three activation gates m, and another gate h, which is called *inactivation gate* because it closes with the ongoing depolarization, triggering the repolarization phase. The overall sodium conductance can be written as:

$$g_{Na} = \overline{g}_{Na} m^3 h \,, \tag{3.7}$$

where, as before, m and h are described with the two-state model:

$$\dot{m} = \alpha_m (1 - m) - \beta_m m \,, \tag{3.8}$$

$$\dot{h} = \alpha_h (1 - h) - \beta_h h \,. \tag{3.9}$$

Equations 3.8 3.9 could be further rewritten as previously done with Eq. 3.2.

In the Hodgkin–Huxley model, the neuronal membrane is locally schematized using the equivalent circuit reported in Fig. 3.2. The capacitor C_m accounts for the capacitive effects of the membrane phospholipid bilayer. The contribute of each ions is represented through a conductance and a voltage source reporting its Nernst potential. It can be noted that here also the contribute of the chlorine ion is accounted for. Differently from potassium and sodium conductance, which are voltage-gated and can be described with the gating model previously analysed (Equations 3.5 and 3.7), the chlorine conductance is often assumed as constant. The current contribute of a specific ion species can be modelled as the product between its conductance and the *driving force*, that is the difference between its Nernst potential and the membrane potential v:

$$I_i = g_i(v - E_i) \,. \tag{3.10}$$



Figure 3.2: Hodgkin–Huxley model equivalent circuit used to describe a patch of the cell membrane.

According to Kirchhoff's current law, the total current I flowing through a patch of the cell membrane can be obtained as the sum of the membrane capacitive current and the current passing through each ion channel (I_{Na}, I_K, I_{Cl}) :

$$I = C_m \dot{v} + g_{Na} (v - E_{Na}) + g_K (v - E_K) + g_{Cl} (v - E_{Cl}).$$
(3.11)

Collecting together all the equations that constitute the Hodgkin–Huxley model:

$$\begin{cases}
I = C_m \dot{v} + g_{Na}(v - E_{Na}) + g_K(v - E_K) + g_{Cl}(v - E_{Cl}) \\
\dot{n} = \frac{n_\infty - n}{\tau_n} \\
\dot{m} = \frac{m_\infty - m}{\tau_m} \\
\dot{h} = \frac{h_\infty - h}{\tau_h}
\end{cases}$$
(3.12)

3.2 Izhikevich model

The high biological accuracy of the Hodgkin–Huxley model is paid by its mathematical complexity. Indeed it is a four-dimensional system of ODEs with non linearities due to the conductance-voltage dependence. However, in certain case the precise shape of the action potential can be regarded as less important than the overall excitation dynamic [51], therefore simplified model can be preferred.

A valid trade-off between biological plausibility and computational cost is represented by the model proposed by Eugene M. Izhikevich [13]. Here, differently from the HH model in which each state variable has a precise physiological meaning, Izhikevich adopted a modelling approach which uses the instruments of dynamical system and bifurcation theory to capture the overall dynamic of the spiking system. This model makes use of only two state variables. The first variable is the fast variable v that represents the membrane potential. The second variable u is a slow variable, called recovery variable. Multiple mechanisms are described by this single variable. Indeed u accounts for the activation of K⁺ channels (as n in the HH model), the inactivation of Na⁺ channels (as h in the HH model) and also it provides negative feedback to v [13]. The Izhikevich model is defined by the following set of equations:

$$\dot{v} = 0.04v^2 + 5v + 140 - u + I, \qquad (3.13)$$

$$\dot{u} = a(bv - u), \qquad (3.14)$$

with the auxiliary after-spike resetting:

if
$$v \ge +30 \text{ mV}$$
, then $\begin{cases} v \leftarrow c \\ u \leftarrow u + d \end{cases}$, (3.15)

where I is the stimulating current, which could be a synaptic current or an external injected current, and a,b,c,d are model dimensionless parameters. The condition in 3.15 is true when the neuron is firing. In that case, first v is set to 30, in order to have all the spikes with this same amplitude. Then the membrane potential is ripolarized by setting v to c and u is updated. Noticeably the model does not have a fixed firing threshold, but rather its value depends on the history of the membrane potential. The numerical values that compare in Eq. 3.13 were obtained by fitting experimental data. Hence, the model is rescaled in a such way that vunits correspond to mV, I units to pA and time units to ms. The model parameters a,b,c,d can be interpreted as follows:

- *a*: can be considered as the time constant of the recovery variable. Smaller values of *a* correspond to slower recoveries.
- b: represents the sensitivity of the recovery variable u to the membrane potential v. This coupling is increased by increasing values of b, possibly resulting in subthreshold oscillations and low spiking threshold.
- c: defines the after-spike resetting of v, which depends on fast high-threshold K⁺ conductances
- d: defines the after-spike updating of u, which depends on slow high-threshold Na⁺ and K⁺ conductances.

By varying the model parameters a,b,c,d different physiological spiking and bursting behaviours can be reproduced. Examples of spiking behaviours successfully reproduced are the phasic spiking pattern, which occurs when a neuron fires a single spike at the onset of the stimuli and then remains at the resting state, or the tonic spiking pattern, in which the neuron continues to fire as long as the stimulating current active [54]. Instead a burst consists in rapid trains of APs followed by periods of silence longer respect the typical inter-spike interval in the firing phase [51].

3.3 Bipartite synapses model

During the process of synaptic transmission involving chemical synapses, the binding of the neurotransmitter molecules to the postsynaptic receptors influence the conductance of the ligand-gated ion channels located on the postsynaptic cell. These changes in ion permeability result in the increase of ionic currents, consequently altering the membrane potential.

Mathematical models of chemical synapses generally can be divided in methods that abstract synapses as ohmic conductances or as sources of currents [53]. Methods belonging to the first class are called conductance-based models. In that case, the synaptic current I_{syn} is modelled similarly as done with ionic currents in the Hodgkin-Huxley model. That means that I_{syn} is described as the product of a conductance g_{syn} with the driving force, which is the difference between the postsynaptic membrane potential v and the reversal potential E_{syn} :

$$I_{syn} = g_{syn}(t)[v(t) - E_{syn}].$$
(3.16)

Similarly to the Nernst potential, which is the membrane voltage at which there is no net flow of a particular ion across the membrane [55], the reversal potential is defined as the membrane potential of a post-synaptic neuron at which the action of a given neurotransmitter causes no net current flow [56]. Excitatory synapses are modelled with E_{syn} values above the resting potential, while for inhibitory synapses E_{syn} is chosen with values below the resting potential. For example commonly shared values are $E_{syn} = 0$ for excitatory synapses and $E_{syn} = -75$ for inhibitory synapses [57]. The ohmic model can be considered a good approximation for AMPA-type glutamate receptors and γ -aminobutryic acid type A (GABA_A) receptors, since when their channels are open their current-voltage relationship is close to be linear. In other cases, a second class of synapses models, called current-based model, is used. In these models, the dependence with the membrane potential v is substituted by a fixed values V_{rest} , which represents the resting potential:

$$I_{syn} = g_{syn}(t)[V_{rest} - E_{syn}].$$

$$(3.17)$$

For small excitatory synapses, in which the driving force hardly changes during the excitation, this can be considered a valid simplification [53]. Moreover, since each postsynaptic neuron can be involved in multiple synapses with several presynaptic neurons, the synaptic current models depicted in Equations 3.16 3.17 can be extended for networks modelling. Generally, considering a postsynaptic neuron with n synapses, the overall synaptic contribution $I_{syn_{tot}}$ is modelled as a weighted sum of the synaptic currents I_{syn_i} coming from each synapse i:

$$I_{syn_{tot}} = \sum_{i=1}^{n} w_i I_{syn_i} , \qquad (3.18)$$

where the synaptic weights w_i are dimensionless numbers representing the strength of the synapses.

It can be noted so far that the modelling of neurotransmitter-gated channels involved in synaptic transmission share some similarities with the gating of ionic voltage-dependent channels. Therefore the same two-state model, expressed by Eq. 3.1, can be used to describe g_{syn} [5]. Here the closing rate β is usually assumed to be constant, while the opening rate α depends on the neurotransmitter concentration. Specifically during the first phase of the synaptic event, the arrival of an AP at the presynaptic terminal triggers the release of neurotransmitter. This phase is simulated by setting α much larger than β , such that the term depending on β in Eq. 3.1 can be ignored. Consequently, assuming null initial neurotransmitter concentration $(g_{syn}(0) = 0)$, the solution of the differential equation corresponds to an increasing function of the type $1 - exp(-\alpha t)$. The second phase saw the neurotransmitter diffusion and consecutive uptake. This is modelled by setting α to zero, and hence the solution becomes an exponential decay of the type $g_{max}exp(-\beta t)$, where g_{max} is defined as the maximum reached at the end of the first phase. Since the release is faster than the uptake, the time constant of the first phase is smaller than the one of the second phase, namely $1/\alpha < 1/\beta$.



Figure 3.3: Examples of time course of the synaptic conductances g_{syn} with different models. In each simulation a presynaptic spike occurs at time $t_0 = 5$ ms. In simulations 3.3a and 3.3b the unique synaptic time constant is set as $\tau = 5$ ms, while in simulations 3.3c the two constants are $\tau_r = 2.64$ ms and $\tau_d = 3.96$ ms.

Especially in the case of large networks, the modelling of synaptic transmission processes becomes challenging from the computational point of view. For that reason, usually some further simplification are adopted [53]. One of the simplest but widely used model reduces the gating dynamic previously discussed as an initial instantaneous rise of the synaptic conductance, followed by an exponential decay:

$$g_{syn}(t) = \begin{cases} 0, & t < t_0 \\ g_{max} e^{-\frac{(t-t_0)}{\tau}}, & t \ge t_0 , \end{cases}$$
(3.19)

where t_0 is the time of the presynaptic spike and τ is the decay time constant. An example of such synaptic dynamic is reported in Fig. 3.3a. This simple model is considered a valid approximation for synapses in which the release phase is much faster than the uptake phase, as in certain types of inhibitory synapses or in AMPA-mediated excitatory synapses. In other cases, models which account also for a prolonged rising time are necessary. One of these is the so-called *alpha function*:

$$g_{syn}(t) = \begin{cases} 0, & t < t_0 \\ g_{max} \frac{(t-t_0)}{\tau} e^{1 - \frac{(t-t_0)}{\tau}}, & t \ge t_0. \end{cases}$$
(3.20)

This model uses the same synaptic constant τ for both the rise and decay phases. Fig. 3.3b reports an example of synaptic conductance modelled with the alpha function. An intuitive extension of this model is represented by the possibility of setting the time constants of the two phases independently. This can be done by defining the synaptic conductance as the difference of two exponentials, one regulating the rising phase, the other the decay phase:

$$g_{syn}(t) = \begin{cases} 0, \quad t < t_0 \\ g_{max} B(e^{-\frac{(t-t_0)}{\tau_d}} - e^{-\frac{(t-t_0)}{\tau_r}}), \quad t \ge t_0 \,, \end{cases}$$
(3.21)

defining the normalization factor B and the time of the conductance peak t_{peak} :

$$B = \frac{1}{-e^{-\frac{(t_{peak}-t_0)}{\tau_r}} + e^{-\frac{(t_{peak}-t_0)}{\tau_d}}},$$
(3.22)

$$t_{peak} = t_0 + \frac{\tau_d \tau_r}{\tau_d - \tau_r} \ln\left(\frac{\tau_d}{\tau_r}\right).$$
(3.23)

The normalization ensures that g_{syn} peak equals to g_{max} and that it occurs at $t = t_{peak}$. An example of synaptic conductance simulated using this model is shown in Fig. 3.3c. Setting τ_r and τ_d according to experimental data, most chemical synapses can be realistically described by this model. However, experimental data
presented in literature display an extremely high physiological variability and often there is no consensus about the fitted values of the synaptic time constants. As instance, decay time constants of GABA_A receptors are proved to vary from 1 to at least 50 ms across diverse types of neurons [58]. This biological diversity makes the simulation task even more demanding.

3.4 Tripartite synapses model



Figure 3.4: Schematic representation of the tripartite synapse model. The main state variables of each compartment are represented by circles. The arrows describe the dependence relationships. The light blue line shows the astrocyte slow activation pathway, regulated by the control parameter β , whereas the red line indicates the fast activation pathway, regulated by α . Control parameters γ and δ influence the astrocyte response.

We consider the tripartite synapse model defined by Postnov et al. [14][12], coupled with presynaptic and postsynaptic Izhikevich neurons, as proposed in [59]. Defining the state variable z as the synaptic activation variable [60], I_{syn} as the

synaptic current and I_{glion} as the astrocyte-induced current, the synaptic coupling is described by the following equations:

$$\tau_s \dot{z} = [1 + tanh(s_s(v_1 - h_s))](1 - z) - \frac{z}{d_s}, \qquad (3.24)$$

$$I_{syn} = (k_s - \delta G_m)(z - z_0), \qquad (3.25)$$

$$I_{glion} = \gamma G_m \,, \tag{3.26}$$

where v_1 is the presynaptic neuron potential and τ_s describes the time delay. Parameters h_s , s_s , d_s control the activation and relaxation of z, k_s is the conductance and G_m is the glion mediator concentration. Control parameters δ and γ regulate the strength of the astrocyte influence on synapse and postsynaptic neuron respectively. z_0 represents the reference level for z (e.g. when the presynaptic neuron is silent, $z(t) = z_0$). If $v_1 < h_s$ the synapse is inactive (z = 0), while when $v_1 - h_s$ term is positive the synapse is active, and z generates the postsynaptic current I_{syn} . The sum of I_{syn} and I_{glion} is used as stimulating current in the Izhikevich model of the postsynaptic neuron (Eq. 3.13). Dynamics of calcium concentration c within the astrocyte and calcium concentration c_e in the ER are described by the following modified two-pool model:

$$\tau_c \dot{c} = -c - k_4 f(c, c_e) + (r + \alpha u_2 + \beta S_m), \qquad (3.27)$$

$$\varepsilon_c \tau_c \dot{c_e} = f(c, c_e) \,, \tag{3.28}$$

with
$$f(c, c_e) = k_1 \frac{c^2}{1+c^2} - \left(\frac{c_e^2}{1+c_e^2}\right) \left(\frac{c^4}{k_2^4 + c^4}\right) - k_3 c_e$$
. (3.29)

In Eq. 3.27, the term -c represents the contribution of Ca^{2+} pumps, which pumps ions out the cell. The term r is a steady flux of Ca^{2+} into the cell without external influence (when $\alpha = 0, \beta = 0$). The term αu_2 , with u_2 postsynaptic neuron recovery variable, represents the calcium influx from the extracellular space due to glion depolarisation (fast activation pathway). The term βS_m is the influx sensitive to IP3 mediator S_m production (slow activation pathway). The function $f(c, c_e)$ is a nonlinear function that describes the Ca^{2+} fluxes between cytoplasm and ER [52]. Its first term, often called uptake, is an Hill-type law indicating the increasing of ER calcium concentration depending on cytoplasmatic concentration, with the aim of calcium storage in the ER. The second term, called release, indicates the release of calcium from ER reticulum to the cytoplasm: its second factor is an Hill-type law related to the CICR phenomenon and the first factor is another Hill-type law which represents the flux dependence in the ER calcium concentration (e.g. if there is no calcium in it, nothing can be released, while in the opposite case if there is lot of calcium the flux saturates at its maximum value). Finally, the third term in $f(c, c_e)$ represents the loss of ER calcium by leakage channels. Furthermore, this system is coupled with the description of glion mediator production G_m and IP3 mediator S_m :

$$\tau_{S_m} \dot{S}_m = [1 + tanh(s_{S_m}(z - h_{S_m}))](1 - S_m) - \frac{S_m}{d_{S_m}}, \qquad (3.30)$$

$$\tau_{G_m} \dot{G}_m = [1 + tanh(s_{G_m}(c - h_{G_m}))](1 - G_m) - \frac{G_m}{d_{G_m}}, \qquad (3.31)$$

where S_m production is triggered by increasing z (similarly as in Eq. 3.24), while G_m production is triggered by increasing calcium cytoplasm concentration c. By changing control parameters α , β , γ , δ several neuron-astrocyte dynamics can be simulated [14]. Parameters α and β regulate fast and slow activation pathway respectively. While the fast mechanism produces a fast but short term response, occurring as a single calcium spike, the slow mechanism elicits long-term activity, since that by increasing β the number of calcium spikes increases. Control parameters γ and δ allow to control the astrocyte feedback performed on the postsynaptic neuron. The parameter γ regulates the depolarising current I_{alion} , thus it controls the positive feedback mechanism. This can support the postsynaptic firing activity also after the end of the stimulus. The parameter δ influences the negative contribution subtracted to the synaptic strength k_s , thus represents a negative feedback which can inhibit the transmission of the stimulus. In [12] they showed how different calcium dynamics can be simulated by choosing astrocytes control parameters α , β , γ and δ . An overall representation of the tripartite synapse model is shown in Fig 3.4

3.5 Synaptic noise model

In physiological networks, each synapse is influenced by the activity of thousands of neighbouring synapses, resulting in a background synaptic noise. With the simplifying assumption of sources as independent and identically distributed random variables, the sum of these noisy synaptic effects converges to a Gaussian probability distribution, in accordance with the central limit theorem. For us noise represents an arbitrary effect on the information of the spikes, but is not focused on particular parts of the brain, or specific scenarios that the presented noise model may need to be readjusted. Synaptic noise can be simulated using a normal distributed random variable [61], with zero mean and standard deviation σ , which contributes in the stimulating current of the postsynaptic neuron:

$$I_{noise} \sim N(0, \sigma) \tag{3.32}$$

Chapter 4

Biocomputing models using tripartite synapses

In the following Chapter, the objectives related to the first two research questions will be investigated. We will start by presenting some modifications related to the tripartite synapse mathematical description, required for the logic gates implementation. Then we will define the overall network structure of tripartite synapse logic gates. The research question number 1, which focus on the design of simple OR and AND gates with Izhikevich neurons, will be investigated by disabling the astrocytes influence on the tripartite synapse, and hence only considering the neurons activity. Afterward the scheme behind research question number 2, namely the design of the OR and AND gate with asctrocytes contribution, will be examined. We will conclude the Chapter by introducing a simple synaptic noise model to account for the neuron signalling stochasticity.

The first step toward the design of neuronal logic gates is to formalize a rule which defines the logic levels. In Section 2.3, the examples found in literature display several different types of encoding method, as the rate coding, or the encoding based on distinct neurons proposed in [42]. In our work we decided to adopt an encoding based on the presence or not of APs: the neuron resting state is marked with the low logic level, instead the presence of APs is marked with the high logic level. This method appears to be as the most intuitive encoding method. Moreover its convenience is also related to the fact that the sequence of spikes can be easily translated in a binary sequence, by segmenting the signal in bins and considering each bin as a bit 1 or 0 depending if the neuron is firing or not.

4.1 Modified synaptic coupling

For the development of an in-silico model of neuronal logic gates, we adopt the Izhikevich model reviewed in Section 3.2. This choice is motivated by the fact that it provides a versatile computational framework for the description of neurons behaviour with minimal computational complexity while keeping biological plausibility. Instead the synaptic coupling is described using the tripartite synapse model of Postnov et al., presented in Section 3.4. One of the most prominent features of the Izhikevich model is its ability in accurately reproducing different neuron spiking behaviours, as tonic/phasic spiking and bursting. Instead, our preliminary experimental tests showed that the Postnov model, coupled with Izhikevich neurons, manage to simulate only the most common type of spiking pattern, which is the tonic spiking. Hence we propose the following modifications. Instead of using the z activation variable, as reported in Eq. 3.24, we use the most common approach based on a synaptic conductance with instantaneous rise and single-exponential decay, expressed in Eq. 3.19. This can be alternatively described by the following differential equation with an update condition:

$$g_{syn} \leftarrow g_{syn} + flag$$
 with $flag = \begin{cases} 1 \text{ if the presynaptic neuron is firing} \\ 0 \text{ otherwise}, \end{cases}$ (4.1)

$$\dot{g}_{syn} = -\frac{g_{syn}}{\tau} \,, \tag{4.2}$$

where τ is the time constant of the conductance decay and *flag* indicates if the presynaptic neuron is firing or not. When a presynaptic neuron is firing, the corresponding synapse is activated by the instantaneous increase of g_{syn} , and then the conductance is extinguished with an exponential decay. Notice that here the conductance maximum g_{max} in Eq. 3.19 is set to 1. Nevertheless, this definition realistically reproduces the temporal summation mechanism, since if another presynaptic spike arrives before that the previous exponential has totally decayed, the two contributes are summed and therefore g_{syn} can also be higher than 1. Since the variable z is here substituted by g_{syn} , also Eq. 3.30 describing the IP3 concentration needs to be modified as follows:

$$\tau_{S_m} \dot{S}_m = [1 + tanh(s_{S_m}(g_{syn} - h_{S_m}))](1 - S_m) - \frac{S_m}{d_{S_m}}.$$
(4.3)

Moreover, we expand the model for the case of multiple tripartite synapses, that means more than one presynaptic neuron and one astrocyte connected with the same postsynaptic neuron. Considering a tripartite synapse involving n presynaptic neurons and the only one postsynaptic neuron, the resulting synaptic current is computed as:

$$I_{syn_{tot}} = \sum_{i=1}^{n} \left(w_i g_{syn_i} (E_{syn_i} - v_{post}) - \delta_i G_{m_i} \right) , \qquad (4.4)$$

where w_i , g_{syn_i} , E_{syn_i} represent respectively the weight, the synaptic conductance and the reversal potential of the i-th synapse (i.e. the synapse between the i-th presynaptic neuron and the postsynaptic neuron), v_{post} is the membrane potential of the postsynaptic neuron and $\delta_i G_{m_i}$ is the i-th astrocyte negative feedback contribution. In addition, the postsynaptic neuron is also stimulated by the astrocyte mediator through I_{glion_i} as expressed in Eq. 3.26.

4.2 Network structure

In this Section, we describe the general network structure used for both the neuronal OR and AND gate. That means that we define how many cells are involved and how they are interconnected. As can be observed in Fig. 4.1, the network consists in two presynaptic neurons, with their membrane potentials v_1 and v_2 as the logic inputs, and a postsynaptic neuron, whose membrane potential v_3 is the logic output. The presynaptic neurons are connected to the postsynaptic neuron through two distinct tripartite synapses. Therefore two astrocytes are included. The OR gate and the AND gate developed involving only excitatory synapses. The presynaptic neurons are described using Equations 3.13 3.14 3.15. Both of them are stimulated by external currents (I in Eq. 3.13) chosen as rectangular functions, which define when the logic inputs are ON or OFF. The astrocytes and the corresponding tripartite synapse models are adapted as explained in Section 4.1. The synaptic current, given by Eq. 4.4, consists in the sum of the contributions I_{syn_1} and I_{syn_2} coming from each synapse. The overall current that stimulates the postsynaptic neuron is given by the sum of the synaptic current and the currents coming from the two astrocytes:

$$I_{tot} = I_{syn_1} + I_{syn_2} + I_{glion_1} + I_{glion_2} \,. \tag{4.5}$$

For the modelling of synapses with the presence of noise, also the contribution of noise, expressed according to Eq. 3.32, is accounted:

$$I_{tot} = I_{syn_1} + I_{syn_2} + I_{glion_1} + I_{glion_2} + I_{noise} \,. \tag{4.6}$$

Finally, the postsynaptic neuron Izhikevich model can be formulated using I_{tot} as stimulating current:

$$\dot{v}_3 = 0.04v_3^2 + 5v_3 + 140 - u_3 + I_{tot}, \qquad (4.7)$$

$$\dot{u}_3 = a(bv_3 - u_3), \qquad (4.8)$$

if
$$v_3 \ge +30 \text{ mV}$$
, then $\begin{cases} v_3 \leftarrow c \\ u_3 \leftarrow u_3 + d \end{cases}$. (4.9)



Figure 4.1: Schematic representation of the logic gate model involving two tripartite synapses. Each neuron and astrocyte is described by its state variables, and the arrows indicates the dependence relationships between variables. For both astrocytes, the slow activation pathway is highlighted with a light blue line, while the fast activation pathway with a red line. The control parameters that describe these processes are reported in bold type close to the lines. In this final network, the postsynaptic membrane potential v_3 is influenced by the stimuli received by two distinct tripartite synapses.

4.3 Neuronal logic gates

4.3.1 Bipartite synapse logic gates

First of all, the tripartite synapse logic gates are tested using only neurons and blocking astrocytes activity. Indeed, here we focus only on the logic gating, meaning that we want to understand how a set of inputs represented by firing patterns can be transformed into an output firing pattern implementing a Boolean function. Only in the next Section we will examine how this system can be improved by the astrocytes contribution. As previously explained in Section 3.4, the dynamic of the astrocyte model is ruled by the control parameters. We saw that α and β define the dependence of Ca^{2+} signalling on the postsynaptic and presynaptic activities through the fast and slow activation pathways. Instead parameters γ and δ define how the Ca^{2+} concentration can positively or negatively affect the postsynaptic activity, closing the feedback loop. Hence, if all the control parameters are set to zero, all the connections between neurons and astrocyte (which are clearly visible in Fig. 3.4) are removed. The glion current due to astrocyte mediator, depicted in Eq. 3.26, becomes null, because $\gamma = 0$. Since $\delta = 0$, the equation of the total synaptic current of the tripartite synapse in Eq. 4.4 becomes equivalent to the conductance based model of bipartite synapses described by Equations 3.16 and 3.18. Therefore the general case of the tripartite synapse is reduced to the simplest case of the bipartite synapse. Notice that the difference between the postsynaptic potential and the reversal potential in Equations 3.16 and 4.4 have different signs due to the fact that the stimulating current in Izhikevich model (Eq. 3.13) is added with a positive sign. Other neuron models adopt different sign conventions.

The OR gate defines an input-output relationship in according to the logical disjunction. As shown in the Truth Table 4.1, its output is high (i.e. 1) if one of the inputs or both of them are high. Therefore, in the neuronal logic gate that implements the OR gate, the firing of one input neuron must produce a



Figure 4.2: Symbol of the OR gate

Table 4.1: Truth table of the OR gate.The operator + defines the OR logicoperation.

sufficiently strong stimulation such that it causes the firing of the postsynaptic neuron. This could be done by regulating the synaptic weights w_i , because they represent the strength of the synapses, namely how much a presynaptic input affects its corresponding postsynaptic neuron. Evidently, since the OR gate act symmetrically, meaning that the result of the input sequence $[1 \ 0]$ is the same of the sequence [0 1], the two synaptic weights w_i need to be equal. The value of w_i is here computed empirically considering the neuronal logic gate with only one external stimulating current ON, and increasing the weight until the postsynaptic neuron is high. The AND gate implements the logical conjunction. Therefore its output is at the high level only if both of its inputs are at the high level, as indicated in the Truth Table 4.2. The basic idea of the neuronal AND gate design is that we need to make synaptic inputs less influential, such that both two input neurons have to be at the high level to make the level of the output neuron high too. This can be obtained by decreasing the synaptic strength. As previously observed with the OR gate, the two synapses needs to have the same w_i . The empirical procedure that we adopt consists in searching for the minimum value of w_i that makes the output neuron firing in the condition with both inputs high.

In Fig. 4.4, an example of functional scheme of logic gate is reported, showing the graphical conventions adopted in this work. The dashed arrows indicate the external stimulating current I_{ext_i} , always chosen as step or rectangular functions. Neurons which cover only a presynaptic role (i.e. they do not form any synapses in which they represent the postsynaptic neuron) are depicted by ellipses, characterized by their membrane potential variable. The circles stand for the postsynaptic neurons. Excitatory synaptic connections are represented by simple arrows and characterized by their synaptic weight w_i . The equivalent traditional symbol of the logic gate is reported with dotted line. Since the same scheme of Fig. 4.4 can be used to model both the neuronal OR and AND gates, in this example a simple box with dotted line is reported. One of the key aspect about the design of neuronal logic gates is the possibility of cascading, that is connecting more of them using the gates outputs as the inputs of another consecutive gate. Hence here we formalise the neuronal



Figure 4.3: Symbol of the AND gate

Table 4.2:Truth Table of the ANDgate.The operator \cdot defines the ANDlogic operation.

logic gates as a made only by the postsynaptic neuron and its synapses with the adjusted weights w_i . Notice that the presynaptic neurons are not part of the gate. The inputs of the logic gates are represented by the membrane potential v_1 and v_2 , while the external current I_{ext_i} are only used in the first layer to communicate the input pattern to the network. With such definition, these building blocks can be intuitively layered to build more complex circuits. For instance, the membrane potential v_3 , can be used as one of the two inputs of another neuronal logic gate.



Figure 4.4: Functional scheme of a generic neuronal logic gate.

4.3.2 Tripartite synapse logic gates

Once understood the design paradigm used to build small networks of neurons with logic gating capabilities, these could be coupled with the astrocyte regulation activity involved in tripartite synapses. Specifically, the main mechanisms that can influence the gate response are the positive feedback and negative feedback, regulated by the control parameters γ and δ . Moreover, since the G_m concentration that appears in the positive feedback term (I_{glion} in Eq. 3.26) depends also on the calcium concentration (Eq. 3.31), calcium signalling is required for the feedback effect. Therefore at least one of the two parameters α and β must be non-null, in order to trigger one of the two activation pathways.

With the setting of the astrocytes control parameters, the contribute of each input stimulus can be reinforced or weakened to characterize the gating response. The OR gate and AND gate design follows the same approach based on the regulation of the influence of the stimuli, as explained in the previous Subsection. The difference respect the bipartite synapse biocomputing is that with tripartite synapse logic gates, the gating response can be characterized both by the tuning of the synaptic weights, but also adapting the astrocytes regulation mechanism. Furthermore, we expect the astrocytes feedback to enhance the neuronal response while reducing the contribution related to noise, acting similarly to a denoising technique. The underlying assumption is that the noise contribution is weaker than the stimulating inputs, and so the negative feedback mechanism should mainly affect the noise, while its influence on the inputs should be neglectable.

Chapter 5

From combinatorial to sequential neuronal logic circuits

In the previous Chapter we presented a model of neuronal logic gate based on tripartite synapses, able to reproduce the simplest logic gating, namely the AND and OR gates. Here we investigate the possibility of developing larger logic circuits. Hence, in order to have a paradigm more flexible and friendly from the computational complexity point of view, we restrict to the use of simpler bipartite synapses. Neurons are still described with the Izhikevich model and bipartite synapses are described using the conductance-based model. Differently respect the previous implementation, the synaptic conductances are not defined with the instantaneous rise and exponential decay model, but rather with the difference of two exponentials model (Equations 3.21, 3.22 and 3.23).

We will start by focusing on the objectives of the third research question. Specifically, we will examine other types of logic gates, useful for the design of sequential circuits. This will be done by including also inhibitory synapses in the logic gates networks. Then, according to the last research question, we will use these novel neuronal logic gates as building blocks for the development of circuits with memory capabilities, i.e. sequential circuits. Even though sometimes the term flip-flop is used in common language to referring to all the families of 1-bit storage elements made by logic gates, in our work we will use the following terminology: the term latch will be used for indicating level-sensitive devices, while edge-sensitive devices will be defined as flip-flops. This convention is often adopted in digital electronics textbooks [62].

5.1 Neuronal AND NOT gate and NOT gate

In [15] L. Yoder theorized a novel type of logic gates, particularly suitable for biocomputed implementations with neurons, and which can be flexibly used to develop several computational solutions. As shown in Fig. 5.1, it consists in an AND gate in which one of its two inputs is inverted. L. Yoder referred to this special type of logic gate as AND NOT gate. Considering a traditional AND gate, its output is 1 if and only if both inputs are 1. Instead, for the statement X AND NOT Y, the high output requires X to be 1, while Y need to be 0, because of the logical negation. In any other cases the output is 0, as depicted in the Truth Table 5.1. Notice that, differently respect traditional gates, as AND and OR gates, the AND NOT gate is not symmetrical respect its inputs. L. Yoder proposed that the gating behaviour of the AND NOT gate could be consider similar to a neuron response based on the following modelling assumption. Lets consider a neuron, with one excitatory synapse and one inhibitory synapse.

- the inhibitory effect of an inhibitory stimuli is able to perfectly counterbalance the excitation elicited by an excitatory stimuli. That means that if the neuron simultaneously receives both an excitatory input and an inhibitory input, the output response is repressed, and so the neuron remains at the resting state;
- the inhibitory input is not able to make the postsynaptic neuron firing, i.e. particular case of spiking behaviour, as rebound spike [54], are excluded;
- the firing of the only presynaptic excitatory neuron is enough to elicit the firing of the postsynaptic neuron. This can be achieved with a strong synaptic strength.

Therefore the neuron will fire if and only if the excitatory input is firing and the inhibitory input is quiet, while in any other case it will remain in the resting state. This neuronal response is curiously similar to the truth table of the AND NOT



X	Y	$X \cdot \overline{Y}$
0	0	0
0	1	0
1	0	1
1	1	0

Figure 5.1: Symbol of the AND NOT gate

Table 5.1: Truth Table of the AND NOT gate. The AND NOT operation can be written as $X \cdot \overline{Y}$.



Figure 5.2: Functional scheme of the neuronal AND NOT gate. The excitatory synapse is characterised by the synaptic weight w_x , while the inhibitory synapse by w_y .

gate. The excitatory input can be considered as the logic variable X, while the inhibitory input as the logic variable Y. Hence, a neuronal AND NOT gate can be developed considering a neuron with an excitatory synapse and an inhibitory synapse, as illustrated in Fig. 5.2, where the bar-headed arrow stands for the inhibitory connection. The synaptic weight w_i of the excitatory synapse has to be chosen such that if the excitatory input is high (the presynaptic neuron 1 is firing) then the postsynaptic neuron fires. This can be done empirically by considering the AND NOT gate with only the excitatory input high, and increasing its w_i until the postsynaptic neuron is at the high level. From now, we will refer to the weight value of the excitatory AND NOT gate synapse obtained with such empirical procedure as w_x . On the other hand, the synaptic weight associated to the inhibitory synapse must be set such that if both excitatory and inhibitory inputs are high, then the postsynaptic neuron must be at the resting state. Now, the value of w_i can be computed considering the AND NOT gate with the weight of the excitatory synapse w_x previously found, setting both inputs high and increasing the inhibitory weight until the postsynaptic response is repressed. We call w_u the value of the weight found for the AND NOT gate inhibitory synapse.

A fundamental type of logic gates, which is essential for the development of most logic circuits, is the NOT gate. It consists on a single input gate, which implements the logical negation. That means that if its input is 0, the output response is 1,



Figure 5.3: Functional scheme of the neuronal NOT gate.

and vice versa. It can be noticed that, the NOT gate can be directly obtained from the neuronal AND NOT gate [16]. Indeed, looking at the AND NOT gate Truth Table 5.1, the output of the last two conditions, where X = 1, corresponds to the negation of Y. Therefore an AND NOT gate in which the input X is always high implements a NOT gate respect the input Y. Adopting the aforementioned scheme, a neuronal NOT gate can be design by using an excitatory input that is always at the high level, namely a neuron that is always firing. Spontaneously and continuosly active neurons are demonstrated to exist in the brain [15][63]. For instance they are involved in the awake condition, and the sleep requires their inhibition. Notice that, since the logic NOT gate has only one input, here the "effective" input is represented by the inhibitory input. Figure 5.3 depicts the functional scheme of the NOT gate. The continuously active neuron is implemented as a presynaptic neuron whose external stimulating current is always ON. Since we are interested only in the state of the inhibitory input, the continuously firing neuron is simply represented by an 'H', which stands for high level. Since the NOT gate shares the same network structure of the AND NOT gate, the synaptic weights assume the same values w_x and w_y .

5.2 Logic gates cascades and neuronal buffers

Our preliminary tests displayed that the inhibition is highly sensitive to inputs timing. Indeed, considering the neuronal AND NOT gate, if the excitatory and inhibitory inputs are not well-synchronized, the inhibition could be not effective. Therefore even though both inputs are high, the output response could not be the desired resting state, but rather the firing state. Synchronization becomes a critical issue in the case of logic gates cascade. Considering more logic gates consecutively connected, the implementation of each Izhikevich neurons elaborates the received synaptic inputs to compute the resulting membrane potential. Certainly, these operations are not performed instantaneously, but rather require a finite time. Therefore each neuron block inevitably introduce a delay on the chain of signals transmission. As a consequence, the inputs synchronization is not always ensured. Here we address to the aforementioned challenges as follows. First, the time constants related to the synapses are increased, such that the variations of the conductances require more time and so the inhibitory and excitatory effects last more. Secondly, using an approach inspired by digital electronics, we introduce the use of *neuronal buffers*. In digital electronics a digital buffer is a gate whose output state is equal to its input state. Digital buffers are commonly used for electrical isolation, impedance matching and for restoring degraded digital signals after the propagation over long distances. For our purpose, the buffer can be used to simply introduce a delay in the input signals and counterbalance their asynchronization. A neuronal buffer can be developed as a neuron with a unique excitatory synapse, with a value of synaptic weight chosen such that if its associated intput neuron is firing, also the output neuron fires. Notice that also the AND NOT gate receives only one excitatory input that is able to make its output firing. Hence the buffer synaptic weight can be chosen as the weight of the excitatory synapse of the AND NOT gate w_x . The input synchronization along the neuronal circuits is guaranteed ensuring the following condition: when more gates are connected together, logic gate inputs must pass through the same number of neuron layers in order to introduce the same delay. Whenever a branch of the neuronal circuit does not respect this condition, neuronal buffers are added. Examples of logic circuits with poor synchronization, fixed with the use of neuronal buffers, will be further discussed in appendix B.

Digital electronics often benefits from the use of NAND gates. Specifically their importance is related to the fact that any Boolean function can be implemented with a combination of NAND gates. This powerful feature, which characterizes also



 $\begin{array}{c|cccc} X & Y & \overline{X \cdot Y} \\ \hline 0 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{array}$

Figure 5.4: Symbol of the NAND gate

Table 5.2: Truth Table of the NAND gate. The NAND operation can be written as $\overline{X \cdot Y}$.



Figure 5.5: Functional scheme of the neuronal NAND gate. The NAND gate can be obtained using an AND and NOT gates cascading, as in Fig. 5.5a. The synchronization of the inputs of such neuronal circuit can be achieved with the addition of a neuronal buffer, as shown in Fig. 5.5b.

the NOR gates, is called functional completeness. The NAND gate is defined as an AND gate followed by a negation operation. Consequently its output is low only if both its inputs are high, while it is high in any other cases (Table 5.2). Since we already discuss how to develop the neuronal AND gate (Subsection 4.3.1) and the neuronal NOT gate (Section 5.1), a straightforward implementation of the neuronal NAND gate can be achieved by cascading a neuronal AND gate with a NOT gate. This simple cascaded structure is depicted in Fig. 5.5a. The same values of synaptic weights w_x and w_y of the AND NOT gate implementation can be used. Instead we refer to the synaptic weight value of the AND synapses as w_z . Now lets focus on the synchronization of the scheme in Fig. 5.5a. Consider the neuron related to the NOT gate, with membrane potential v_4 . Its inhibitory synaptic input passes through two layers of neurons, specifically the one associated to the presynaptic neurons (with membrane potentials v_1 and v_2) and the one related to the AND

gate (with membrane potential v_3). On the contrary, the excitatory synaptic input pass only through one layer of neurons, which is the continuously firing neuron. Hence the synchronization condition is not fulfilled and the logic circuit could not follow the desired behaviour. The circuit can be adjusted by adding a neuronal buffer in the branch related to the excitatory synapse of the NOT gate, as depicted in Fig. 5.5b. Since now both synaptic inputs pass through two layers of neurons, the condition is satisfied.

5.3 Neuronal latches

All the neuronal implementations of logic circuits considered so far make use of combinatorial logic. In combinatorial circuits, their outputs are fully defined by the present values of the inputs. Therefore they could be defined as static, meaning that they do not depend on the previous values of inputs and outputs. Differently in sequential logic circuits, the definition of the outputs relies also on the sequence of past inputs. For this reason the logical outputs are often referred as *states*, which recall the storage capability of sequential logic.

One of the simplest sequential circuits is the *set-reset latch* (SR latch). It consists in a 1-bit memory, in which its state is defined asynchronously. SR latches are commonly built using NOR gates or NAND gates. Even though we already presented a model of neuronal NAND, here we discuss the realization based on AND NOT gates, formulated in [16]. This choice is motivated by the fact that the NAND gate implementation involves a larger number of neurons respect the AND NOT gate, and hence its computational cost is higher. The logic scheme of the AND NOT gate based SR latch is shown in Fig. 5.6. As can be observed, it is made by two AND NOT gates in which each inverted input (the Y input of the



Figure 5.6: Logic circuit of the SR latch based on AND NOT gates.



Figure 5.7: Symbol of SR the latch.



original AND NOT gate in Fig. 5.1) is obtained using the output of the other gate. Here the not inverted inputs (the X input in 5.1) are called set (S) and reset (R). The behaviour of the latch is summarized in Table 5.3. For instance, lets consider the case with S = 1 and R = 0. Since R = 0 the response of the AND NOT gate 2, namely Q, will certainly be 0, because its X input is 0 (see the AND NOT gate Truth Table 5.1). The gate 1 has inputs S = 1 and Q = 0, therefore its output \overline{Q} is 1. Similarly it can be demonstrated that with S = 0 and R = 1, Q is 1, while \overline{Q} is 0. Consequently this realization consists in an active low latch, that means that when it is activated by setting the set equal to 1 and reset to 0, its output Q is at the low level. Now considering the case with S = 1 and R = 1, since each of the two gates have X input as 1, they behave as inverters. Suppose that in the instant before the setting of S = 1 R = 1 the latch presented outputs $Q_{-1} = 1$ and $\overline{Q}_{-1}=0$. Once chosen S and R to 1, the gate 1 has inputs S=1 and $Q_{-1}=1$, and so \overline{Q} is 0; the gate 2 has inputs R = 1 and $\overline{Q}_{-1} = 0$ and so Q is 1. Therefore the outputs are unchanged. Similarly one could demonstrate the case with $Q_{-1}=0$ and $Q_{-1}=1$. This inputs configuration is called the *memory state*, because the latch stores the 1-bit information which represents its state. Finally in the case with S = 0 and R = 0, since both X inputs are 0, both Q and Q_{-1} are 0. This combination is often called *not allowed* condition (or forbidden condition), because now the fundamental relationship that \overline{Q} corresponds to the negation of Q is not valid anymore. Even though this condition does not damage the device, it must be avoided because the latch is not following the desired logic behaviour. A neuronal SR latch can be design using two neuronal AND NOT gates with mutual inhibitory feedback, meaning that the response of the output neuron of each gate is used as the inhibitory input of the other gate. The functional scheme of the neuronal SR latch is displayed in Fig. 5.8. The synaptic weights of the excitatory and inhibitory synapses can be chosen according to the AND NOT gate implementation. A critical point of the neuronal latch is that here, since inhibitory inputs are obtained from the outputs of the gates, they will always be delayed respect the excitatory inputs. Indeed the rule based on the number of neuronal layers is not respected, and there is no neuronal buffer configuration that can re-equalize them. As instance, if we



Figure 5.8: Functional scheme of the neuronal SR latch.

add a buffer in the branch related to the excitatory input of AND NOT gate 1, this gate will now satisfy the rule, but the inhibitory input of the AND NOT gate 2 will be delayed even more. The strategy that we adopt here to solve this issue consists in making the inhibitory effect last more, and so relaxing the synchronization requirement. This can be achieved exploiting the temporal summation mechanism, obtained with increased time constants of the inhibitory synapses.

As previously observed, the SR latch is always transparent. This circuit can be further modified with an additional input, called *latch enable* (LE), to develop a latch which becomes transparent only for a specific level of such input. This type of latch is often called as *gated SR latch*. It represents an example of synchronous



Figure 5.9: Logic circuit of the gated SR latch. The SR latch within this circuit is represented by its symbol.



Figure 5.10:Symbol of the gated SRTable 5.4:Truth Table of the gatedlatch.SR latch.

circuit, and specifically defined as level-sensitive, because its transparency depends on the level of the clock signal *LE*. The logic scheme of the gated SR latch is depicted in Fig. 5.9. It is composed of a SR latch in which the S and R inputs pass through a first layer of NAND gates. The NAND gates take as inputs the actual set and reset of the gated latch, that here we call S' and R', and the LE input which is in common between both the gates. Observing the NAND Truth Table 5.2, it can be noticed that if LE = 0 the NANDs outputs are always 1. Hence the following SR latch is forced in the memory state, namely it is not transparent respect the inputs. On the contrary if LE = 1, the NANDs outputs correspond in the negation of their other inputs (S' or R'). Therefore in that condition, the SR latch receives the inputs $\overline{S'}$ and $\overline{R'}$, and so its behaves as an active high latch, i.e. the setting of S' = 1 and R' = 0 results in a high output Q. The overall behaviour of such device is shown in Truth Table 5.4. A neuronal gated SR latch can be developed connecting the neuronal building blocks which implement the NAND gates and the SR latch following the same scheme of the gated SR latch, as illustrated in Fig. 5.11.



Figure 5.11: Functional scheme of the neuronal gated SR latch.

5.4 Neuronal flip-flops

In the previous Section the implementation of one of the simplest synchronous circuit, i.e. the gated SR latch, has been analysed. We observed that this device is level-sensitive: adopting the clock signal (LE) as a periodic square wave, the latch is transparent only during the high semi-periods of the clock [62]. Instead, flip-flop circuits are defined as edge-sensitive, meaning that they become sensitive only for a brief time which is triggered by the transition of the clock between the two levels. In other words, the device 'take a picture' (*sample*), the input values at the clock edge. Depending on the type of flip-flop, this could be the rising edge (*positive-edge flip-flop*), the falling edge (*negative-edge flip-flop*) or both of them (dual-edge flip-flop).

Most of digital flip-flops are obtained from a fundamental architecture, called *master-slave*. Figure 5.12 shows a master-slave flip-flop, which comprises two gated SR latches connected in cascade. The first of them is called *master*, because it is used to transmit the input values. The second latch is called *slave*, because it can only sample the outputs of the master or hold them in memory. This is achieved with a shared clock signal CLK, which is directly sent to the slave and inverted to the master. When the clock signal is low (CLK = 0), the *LE* signal seen by the master latch is high, and so changes in the inputs levels influence the



Figure 5.12: Logic circuit of the master-slave flip-flop.



Figure 5.13: Logic circuit of the D flip-flop.

master outputs. On the contrary, the slave is forced in the memory condition because its LE is low, hence its outputs remain stable. When the clock signal switches to the high level (CLK = 1), the master is locked and maintains the previous outputs levels. At the same time, the slave becomes transparent, and sets its outputs according to the received inputs, which are the fixed outputs held by the master. Since after the rising of the clock the master is not sensitive to the inputs variations anymore, the flip-flop outputs correspond to the inputs values at the instant of the rising edge. Therefore this device represents a positive-edge flip-flop, because it is sensitive at the rising edge of the clock. Similarly could be demonstrated that placing the not gate only in the slave clock, the device behaves as a negative-edge flip-flop. Although the clock signal regulates the operation computed by the flip-flop, the device could still encounter the not allowed condition, in the case of both high inputs.

A straightforward modification of the master-slave flip-flop can be done in order to avoid the the not allowed condition. The S' and R' signals are substituted by an unique input signal D, which is sent directly for the S input and inverted for the R input, as depicted in Fig. 5.13. The above-mentioned flip-flop is called D*flip-flop*, where D stands for data, because it requires a unique data input, or for delay, because the variations of the input are reported in the output after a certain delay defined by the next clock edge. The network structure that implements the neuronal D flip-flop is illustrated in Fig. 5.14. With this large circuit, the use of neuronal buffers becomes fundamental, especially in the neuronal NOT gates, due to the additional connection with the continuously firing neurons. Notice that all the sequential circuits presented in the current and the previous Sections can be implemented by using AND NOT gates, NOT gates, AND gates and neuronal buffers. Therefore all the values of synaptic weights can be chosen according to the ones defined in each building block. On the whole, three values of synaptic weights are needed, especially w_x and w_y , which are in common between the AND NOT gates, the NOTs and the buffers, and w_z , which is used for the synapses of the AND gates.



Figure 5.14: Functional scheme of the neuronal D flip-flop. For simplicity, when n neuronal buffers are connected in cascade, the number of buffers (x n) is reported and only one buffer is represented.

Chapter 6

Results

6.1 Simulations

6.1.1 Numerical simulations

All the numerical simulations reported in Section 6.2 were obtained in MATLAB R2019b. The equations of the model were implemented using the explicit Euler method with step size dt = 0.5 ms. Table 6.1 reports the chosen values of the parameters that characterize the tripartite synapse model, according to the modifications proposed in Section 4.1. Since all the synapses involved in the above-mentioned simulations are excitatory synapses, for all of them the reversal potential E_{syn} is set as 0. The time constant τ of the single-exponential synaptic model is equal to 10 ms.

 Table 6.1: Parameters of the tripartite synapse model in common between all tripartite synapse logic gates.

$k_1 = 0.13$	$k_2 = 0.9$	$k_3 = 0.004$	$k_4 = 2/\varepsilon_c$
	$\varepsilon_c = 0.04$	r = 0.31	
$\tau_c = 8$	$\tau_{S_m} = 100$	$\tau_{G_m} = 50$	$\tau_g = 10$
	$s_{S_m} = 100$	$s_{G_m} = 100$	
	$h_{S_m} = 0.45$	$h_{G_m} = 0.5$	
	$d_{S_m} = 3$	$d_{G_m} = 3$	

6.1.2 Simulink simulations

The simulations related to Sections 6.3 and 6.4 were computed using MATLAB R2021b Simulink. The equations are discretised using the explicit Euler method with step size dt = 0.5 ms. The Simulink parameter sample time, which indicates when a Simulink block produces outputs and updates its internal state, is chosen equal to dt. The Izhikevich neurons involved in the model are characterized with the tonic spiking behaviour. The reversal potential E_{syn} is set as 0 for excitatory synapses and as -75 for inhibitory synapses. All the logic circuits are driven by an external stimulating current equal to I = 4 pA. Finally, also an example of logic circuit with higher stimulating current I = 7 pA is provided.

6.2 Neuronal OR and AND gates

6.2.1 Logic gates with different spiking patterns

This Subsection reports the results of the bipartite synapse logic gates, obtained by blocking astrocytes activity of the tripartite synapses, as discussed in Subsection 4.3.1. The OR gate and AND gate are developed investigating two possible firing patterns, specifically phasic spiking and tonic spiking patterns. Phasic spiking occurs when a neuron fires a single spike at the onset of the stimuli and then remains at the resting state [54]. In the first realisation, all the three neurons in the logic gate network communicate using phasic spiking. This can be done by setting the initial values of all the voltage potentials v_i , the recovery variables u_i and the values of the model parameters a, b, c, d as indicated in [13]. The stimulating current of both presynaptic neurons is chosen as a rectangular function, with amplitude equals to I = 0.5 pA between 0.5 and 1.5 seconds and null otherwise. Then OR and AND gates are developed regulating the influence of the stimuli, through the synaptic strength w_i , as discussed in 4.3.1. For this purpose, OR gate synaptic strength is chosen as $w_i = 0.02$, while the AND gate synaptic strength is chosen as $w_i = 0.01$. Figures 6.1 and 6.2 report the AND gate and OR gate operations with phasic spiking pattern. With tonic spiking pattern, the neuron continues to fire as long as the stimulating current is ON. The combination of neuron model parameters that allows to simulate tonic spiking pattern can be found in [13]. The high level current amplitude is chosen as I = 4 pA. The OR gate is realised using $w_i = 0.9$, while the AND gate synaptic strength is $w_i = 0.05$. Figures 6.3 and 6.4 depict the AND gate and OR gate dynamics using tonic spiking.



Figure 6.1: Phasic pattern OR gate involving only neurons, with stimulating current I = 0.5 pA and synaptic strength $w_i = 0.02$



Figure 6.2: Phasic pattern AND gate involving only neurons, with stimulating current I = 0.5 pA and synaptic strength $w_i = 0.01$



Figure 6.3: Tonic pattern OR gate involving only neurons, with stimulating current I = 4 pA and synaptic strength $w_i = 0.09$



Figure 6.4: Tonic pattern AND gate involving only neurons, with stimulating current I = 4 pA and synaptic strength $w_i = 0.05$

6.2.2 Logic gates using astrocytes

In Fig. 6.6 an example of the dynamic of a tripartite synapse logic gate is provided. The fast activation pathway is blocked by setting $\alpha = 0$, while the slow activation pathway is enabled with $\beta = 0.05$. With this choice, the activity of each astrocyte reflects the state of the associated input neuron. When the presynaptic neuron is not firing, the associated astrocyte displays damped calcium oscillations, while when the presynaptic neuron is firing, also the calcium signal shows spiking activities. Moreover, astrocytes activation continues also when neurons firing has already stopped. Here, the astrocyte control parameters γ and δ , which reflect the positive feedback and negative feedback mechanism respectively, are empirically chosen so that the output neuron replicates the desired logic gating. Specifically $\gamma = 1.5$ and $\delta = 10$.



Figure 6.5: Mismatched AND gating due to the too high synaptic strength $(w_i = 0.11)$. The logic gate is obtained involving only neurons and with stimulating current I = 4 pA.



Figure 6.6: Simulation of AND gate with enabled astrocytes activity ($\alpha = 0$ $\beta = 0.05 \ \gamma = 1.5 \ \delta = 10$), synaptic strength $w_i = 0.11$ and stimulating current I = 4 pA. The astrocytes calcium signals are reported.

6.2.3 Effect of noise in the logic gates

In this Subsection we want to explore the effects of noise to the information encoded in spikes, that ultimately can effect the output of the logic gates. This approach also allows us to develop an improved verification of our models, and investigate how astrocytes can handle noise through its feedback mechanisms. The bipartite synapse logic gates are tested with the presence of noise, using the noise model described in Section 3.5. All the noisy simulations reported in Figs. 6.7, 6.8, 6.9 and 6.10 are generated using the same observation of synaptic noise, with $\sigma = 5$. The stimulating current is chosen as a rectangular function, with amplitude I = 4pA between 0.5 and 1.5 seconds (ON phase) and null between 1.5 and 2.5 seconds (OFF phase). In that way, the logic gates are equally evaluated both with the high and low level responses. In the following Figures (from Fig. 6.7 to Fig. 6.10), the ON phase is highlighted using light gray background, while the OFF phase using dark gray background. All neurons are modelled using the tonic spiking pattern.

To assess how noise influences the logic gating, first of all the definition of a grid in which evaluate the response is needed. This is defined using one of the two input signals, that specifically needs to be at the high level. In the ON phase, the signals are segmented, dividing each interspike interval in halves. Since the duration of ON and OFF phases is the same, in the OFF phase the segmentation previously defined for the ON phase is replicated. The first bin represents a special case. In order to define all bins as symmetric, with a spike at the center, the beginning of the first bin precedes the first peak with an interval equal to the half of the distance between the first and second peak. An example of this signal segmentation can be observed in Fig. 6.7. Each of the two phases consists in 8 bins, and so the overall signal can be interpreted as a binary signal made by 16 bits. Note that the first 0.5 seconds, where no neurons are stimulated, are not assessed.

Once defined the grid, the output response accuracy is evaluated and signal errors are assessed using the bit error ratio (BER). First of all, the signals are encoded into a bit streams, classifying a spiking bin as 1, while a resting bin as 0. The bit error ratio is calculated as the number of wrong bits divided by the total number of transferred bits, expressed as a percentage. For binary classification problems, the accuracy can be defined as [43]:

$$accuracy = \frac{TP + TN}{TP + TN + FP + FN},$$
(6.1)

where TP represents the number of true positives, FP the number of false positives and FN the number of false negatives. For our purpose, the spiking state is considered as the positive class, while the resting state is the negative class. For instance, in the case of the OR gate with one or both inputs at the high level, since the output response needs to be high, an output bin with a spike is considered as a TP while a bin without any spike is considered as a FN. Given that spikes are assessed individually, if instead of one spike two spikes are found in the same bin, one spike counts as a TP and the other as a FP. When both inputs are low, also the output response has to be low, therefore an output bin without any spike is considered as a TN, whereas a bin with one spike is considered as a FP.

Figs. 6.7 and 6.8 show an example of bipartite synapse OR gate and AND gate affected by noise, with standard deviation $\sigma = 5$, and assessed using the aforementioned quality metrics.



Results

Figure 6.7: Simulation of OR gate involving only neurons, with synaptic strength $w_i = 0.09$, stimulating current I = 4 pA and affected by gaussian synaptic noise with $\sigma = 5$. The stimulation current ON phase is marked with light gray background, while the OFF phase with dark gray background. The quality indexes values are: accuracy = 0.81, BER=18.75% for both simulation 6.7a and 6.7b



Figure 6.8: Simulation of AND gate involving only neurons, with synaptic strength $w_i = 0.05$, stimulating current I = 4 pA and affected by gaussian synaptic noise with $\sigma = 5$. The stimulation current ON phase is marked with light gray background, while the OFF phase with dark gray background. The quality indexes values are: accuracy=0.50, BER=50.00% for simulation 6.8a, and accuracy=0.81, BER=18.75% for simulation 6.8b

6.2.4 Astrocyte-based denoising

In this Subsection, the astrocyte denoising method is tested on the neuronal OR and AND gates, with the same observation of noise used in the previous simulations involving only neurons (Fig. 6.7 and Fig. 6.8). Fig. 6.9 shows the logic gate response of the OR gate with astrocytes-based denoising. The astrocytes control parameters are set as $\alpha = 0$, $\beta = 0.05$, $\gamma = 0$ and $\delta = 15$. Fig. 6.10 reports the results of the astrocyte denoising applied to the AND gate. Here the control parameters are chosen as $\alpha = 0$, $\beta = 0.05$, $\gamma = 1.5$ and $\delta = 10$. Since now both γ and δ are nonzero, both positive and negative feedback are exploited.

Finally the logic gates performances are evaluated for increasing noise levels. The analysis is performed using noise standard deviation from 1 to 10, with 10 noise observations for each noise level. For each observation OR gate, OR gate with astrocyte denoising (ORd), AND gate and AND gate with astrocyte denoising (ANDd) are assessed using accuracy and BER. The results of the noise sensitivity analysis are reported in Fig. 6.11.

Results



Figure 6.9: OR gate astrocyte-based denoising. The synaptic strength is set as $w_i = 0.22$, the stimulating current as I = 4 pA, while the astrocyte control parameters are chosen as $\alpha = 0$ $\beta = 0.05$ $\gamma = 0$ $\delta = 15$. The stimulation current ON phase is marked with light gray background, while the OFF phase with dark gray background. The quality indexes values are: accuracy=1.00, BER=0.00% for simulation 6.9a, and accuracy=0.94, BER=0.00% for simulation 6.9b



Figure 6.10: AND gate astrocyte-based denoising. The synaptic strength is set as $w_i = 0.11$, the stimulating current as I = 4 pA, while the astrocyte control parameters are chosen as $\alpha = 0$ $\beta = 0.05$ $\gamma = 1.5$ $\delta = 10$. The stimulation current ON phase is marked with light gray background, while the OFF phase with dark gray background. The quality indexes values are: accuracy=0.75, BER=25.00% for simulation 6.10a, and accuracy=1.00, BER=0.00% for simulation 6.10b


Figure 6.11: Noise sensitivity analysis. Noise standard deviation changes between 1 to 10 and for each noise level 10 observations are generated. The graphs report the BER and accuracy averages and standard deviation of the output response for OR gate, OR gate with denoising mechanism (ORd), AND gate and AND gate with denoising mechanism (ANDd).

6.3 Neuronal AND NOT-based logic gates

This Section reports the results related to the fundamental neuronal logic gates introduced in Sections 5.1 and 5.2, that will be later used as building blocks for the development of sequential circuits. In the simulations of the current and the next Sections, the networks are stimulated by input membrane potentials computed synthetically to reproduce desired input patterns, as will be further discussed in appendix A. Figure 6.12 displays the input and output membrane potentials of the neuronal AND NOT gate. The excitatory and inhibitory synaptic weights are set as $w_x = 0.06$ and $w_y = 0.18$ respectively. Synapse models are also characterized by the synaptic time constants of rise and decay (τ_r and τ_d in Eq. 3.21). Their values are chosen as $\tau_r = 15\% ISI = 19.80$ ms and $\tau_d = 20\% ISI = 26.40$ ms for the excitatory synapse, and $\tau_r = 15\% ISI = 19.80$ ms and $\tau_d = 45\% ISI = 59.40$ ms for the inhibitory synapse, where ISI = 132 ms is the average interspike interval. The input patterns are chosen accordingly to the traditional incremental order used in truth tables, and the input levels are changed every half of a second. In the first interval both input neurons are silent, corresponding to input levels $[0 \ 0]$, in the second interval and third interval only one input neuron is firing, corresponding to [0, 1] and [1, 0], while in the fourth interval both input neurons are firing, i.e. [1, 1].

Afterwards, the neuronal NOT gate is tested, as shown in Fig. 6.13. As observed in Section 5.1, the neuronal NOT gate consists in a special case of AND NOT gate, hence the synaptic parameters w_x , w_y , τ_r and τ_d are chosen as in the case of the AND NOT gate. The input pattern is generated as a sequence that toggles between the two state every 0.5 seconds.

Lastly, Fig. 6.14 depicts the dynamics of the neuronal NAND gate, which is stimulated using the aforementioned incremental input pattern. The AND gate included in the NAND cascaded architecture makes use of the following synaptic parameters. The synaptic weights are set as $w_z = 0.065$ and the synaptic time constants are defined as $\tau_r = 2\% ISI = 2.64$ ms and $\tau_d = 3\% ISI = 3.96$ ms for both synapses. The NOT gate within the NAND architecture makes use of the same synaptic parameters of the AND NOT gate. Similarly, the neuronal buffers are realised using the synaptic parameters of the excitatory synapse of the AND NOT gate.



Results

Figure 6.12: Example of gating response of the neuronal AND NOT gate. For the excitatory synapse, the synaptic parameters are set as: $w_x = 0.06$, $\tau_r = 19.80$ ms and $\tau_d = 26.40$ ms. For the inhibitory synapse, they are chosen as: $w_y = 0.18$, $\tau_r = 19.80$ ms and $\tau_d = 59.40$ ms. The amplitude of the stimulating current is I = 4 pA.



Figure 6.13: Example of gating response of the neuronal NOT gate. For the excitatory synapse, the synaptic parameters are set as: $w_x = 0.06$, $\tau_r = 19.80$ ms and $\tau_d = 26.40$ ms. For the inhibitory synapse, they are chosen as: $w_y = 0.18$, $\tau_r = 19.80$ ms and $\tau_d = 59.40$ ms. The amplitude of the stimulating current is I = 4 pA.



Results

Figure 6.14: Example of gating response of the neuronal NAND gate. The synaptic parameters of the AND gate are $w_z = 0.065$, $\tau_r = 2.64$ ms and $\tau_d = 3.96$ ms; for the NOT gate excitatory synapse $w_x = 0.06$, $\tau_r = 19.80$ ms and $\tau_d = 26.40$ ms; for the NOT gate inhibitory synapse $w_y = 0.18$, $\tau_r = 19.80$ ms and $\tau_d = 59.40$ ms. The amplitude of the stimulating current is I = 4 pA.

6.4 Neuronal latches and D flip-flop

In this Section, the results related to the sequential circuits developed using the library of neuronal AND NOT, NOT, NAND and buffers are reported. Since latches and flip-flops are simply built connecting the fundamental neuronal logic gates as building blocks, the values of the synaptic parameters are unchanged.

Figure 6.15 shows the dynamics of the neuronal SR latch. Here each membrane potential is labelled with reference to the digital logic signals that it represents. As instance v_s is the membrane potential that is used as the set signal of the latch. The two outputs of the devices are represented by the membrane potentials v_Q and $v_{\overline{Q}}$. Notice that the condition with both set and reset neurons at the resting state is avoided, since it represents the not allowed condition of the SR latch (see Table 5.3).

Next, the results related to the neuronal gated SR latch are illustrated in Fig. 6.16. The membrane potential v_{LE} is associated to the LE signal which drives the front gating stage. Differently from the previous SR latch, now the not allowed condition corresponds to the case with both set and reset neurons at the high level, and hence it is excluded in the input pattern.

Figure 6.17a displays the membrane potentials of the neuronal D flip-flop. In that case, the input pattern consists of the single D signal, whose role is played

Results

by membrane potential v_D . Since this device is an example of synchronous edgesensitive circuit, it is triggered by a clock signal, depicted by membrane potential v_{CLK} . Specifically this implementation corresponds to a positive-edge flip-flop. Hence the triggering rising edges of the clock are highlighted with arrows in v_{CLK} , and reported with dashed lines in the other signals. The D flip-flop is also tested with an increased stimulating current equals to I = 7 pA, as shown in Fig. 6.17b. The values of the synaptic weights are recomputed following the same procedures explained in Sections 4.3.1 and 5.1. The weights of the AND NOT gates are $w_x = 0.11$ and $w_y = 0.67$ for the excitatory and inhibitory synapses respectively, while the weights of the AND gates are set as $w_z = 0.099$.



Figure 6.15: Example of gating response of the neuronal SR latch, with stimulating current I = 4 pA.



Figure 6.16: Example of gating response of the neuronal gated SR latch, with stimulating current I = 4 pA.



Figure 6.17: Examples of gating response of the neuronal D flip-flop with different amplitudes of the stimulating current.

Chapter 7 Discussion

Our biocomputing research has started by examining the modelling of the simplest logic gates, namely the OR and the AND gates, with the use of bipartite synapses. As predicted in Subsection 4.3.1, the empirical tuning procedure resulted in a smaller synaptic weight for the AND respect the OR gate. Observing the neuronal OR gate simulation with phasic spiking (Fig. 6.1), one firing input neuron is enough to trigger the spiking of the output neuron. Hence, this neuronal logic gate follows correctly the gating response of the OR gate. Instead in Fig. 6.2, the output neuron is at the level 1 only if both input neurons are at the level 1, implementing an AND gating. Therefore, according to research question number 1, the results demonstrate that the developed network of Izhikevich neurons is able to display the desired gating responses. Furthermore the gating has been extended through the tonic spiking behaviour, after recomputing the values of the synaptic weights w_i . Particularly in Figs. 6.3 and 6.4, the OR and AND gates are implemented involving multiple spikes with the tonic spiking behaviour.

Afterward we have investigated about the use of tripartite synapses. Since the system complexity of the astrocyte dynamics is considerably high, we tested this mechanism on the OR and AND gates, which represent the simplest logic responses and can be achieved with few neurons. From Fig. 6.5 and 6.6, we can observe the astrocyte effect in regulating neurons activity. These two simulations are generated using the same network parameters, but with astrocytes activity disabled (Fig. 6.5) and enabled (Fig. 6.6). In particular, an AND gate is designed using synaptic strength $w_i = 0.11$, which is larger than the one used in paragraph 6.2.1, where it was set as $w_i = 0.05$. In Fig. 6.5, with one input at level 1 and the other at level 0, the output response is at 1. Therefore the logic gate with only neurons does not correctly reproduce the AND function, due to the increased synaptic strength. Then the astrocytes negative feedback is used to correct the response, setting $\alpha = 0$, $\beta = 0.05$, $\gamma = 1.5$ and $\delta = 10$. As can be observed in Fig. 6.6, the negative feedback mechanism is able to reduce the influence of the inputs and make the logic gate

behaviour more similar to the AND logic function. Although the overall response approximately follows the behaviour of a logic AND, in the case with one input 1 and the other 0 (Fig. 6.6a) the output shows an initial spike which should not be present. This can be caused by the fact that the astrocyte dynamic is slower than the neuron dynamic, and so the astrocyte regulation mechanism activates with a delay after the neuron excitation. Moreover only the slow activation pathway of astrocytes is exploited here, because the astrocyte feedback induced through the fast activation pathway was too strong.

In spite of that, the use of tripartite synapses results in significant benefits. Indeed, we have tested the astrocyte regulating activity as a mechanism of reduction of synaptical noise. In Figs. 6.7 and 6.8, we evaluate the performance of bipartite synapse logic gates, with the presence of noise. Most of these simulations have the same values of accuracy and BER, probably due to the fact that the same noise observation was used. However, the AND gate with inputs [1 0] (Fig. 6.8a) is significantly more sensitive to noise respect the other cases. This is proven by the fall of the accuracy to 0.50 and the rise of the BER to 50.00%. Generally, it has been observed that with the chosen synaptic noise model, noisy contributions often occur as spurious spikes rather than as the suppression of the true spikes. For this reason, in the case in which the logic response is high, since the output neuron is already spiking, the noise effect could reinforce the spiking activity, but the errors introduced are not relevant to the interpretation of the binary message. By the contrast, when the output needs to be at the resting state, as for the case of the AND gate with inputs [1 0], the presence of noisy spikes significantly compromises the binary message. The astrocyte-based denoising mechanism is tested in Figs. 6.9 and 6.10. When applied to the OR gate, the denoising method is able to noticeably reduce the noise contribution. Indeed, with inputs [1 0], the output perfectly matches the desired response (accuracy=1.00, BER=0.00%). Instead, with inputs [1 1], the denoised OR gate displays slightly lower values of accuracy, due to the fact that the first firing bin consists in two rapid spikes. However, this fact does not represent an effective binary error, since it reinforces the true response. The BER, which is not affected by additive true spikes, is still optimal (BER=0.00%). As far as concern the AND gate, even though the results with inputs [1 1] perfectly match the desired response, the case with inputs [1 0] remains a critical point. One possible interpretation could be related to the reduced synaptic strength. Indeed, since the AND gate w_i is smaller than the OR one, the inputs that stimulate the postsynaptic neuron are less strong, and so it is difficult to set the astrocyte negative feedback without removing also the correct gating response.

The effectiveness of astrocyte denoising is further validated by Fig. 6.11, where the logic gates undergo increasing levels of noise and multiple observations are averaged. In the case of both inputs at level 1, AND and OR bit error ratio increases with noise levels, but remains below 55. Similarly as said before, noisy

spikes during the high phases of the output signals do not cause relevant errors in the binary sequence, and so noise mainly affects the low phase. For this reason the BER values remain controlled. Instead, the accuracy values decrease fast with the noise levels, because this index is also influenced by additive spurious spikes during the low phases. For both quality metrics, the performances with astrocyte denoising (ORd and ANDd) clearly overcome the realisations with only neurons (AND and OR). As far as concerned the case with inputs [10], generally the two metrics reflect worse results than the case of $[1 \ 1]$, because when the output must be low, both of the signal phases are at the low level, hence evidently affected by the presence of noisy spikes. The AND gate with inputs [1 0] confirms to have the worst performances between all the logic gates. The denoising mechanism is able to enhance its BER and accuracy, but the ANDd remains still more sensitive to noise than the simple OR gate without denoising. By contrast the denoising technique clearly improves the OR gate outcomes, obtaining the best results in terms of BER and accuracy. According to the aforementioned outcomes, the tripartite synapse-based strategy constitutes a valid solution to research question number 2, since it improves the logic gates robustness in term of sensitivity to noise.

Once developed a reliable paradigm to design simple OR and AND gating responses with Izhikevich neurons, the rest of our work has been concentrated about the development of more complex logic circuits. The use of inhibition provides an effective answer to research question number 3, since our library of gating responses has been enlarged with the realisation of AND NOT, NOT and NAND gates. The input and output membrane potentials of these neuronal logic gates are reported in Figures 6.12, 6.13, 6.14, and they correctly fulfil the associated truth tables. The realisation of each gate involved different choices regarding the synaptic model parameters. For the AND NOT gate, we can observe that the value of the weights related to the inhibitory synapse ($w_y = 0.18$) is higher respect the one of the excitatory synapse ($w_x = 0.06$). The reason of this could be related to the fact that when an excitatory and an inhibitory stimuli occur nearby, for our purpose the inhibition must overcome the excitation, resulting in the resting state. As far as concern the synaptic time constants, their choice is also driven by the objective of defining a model able to operate with different level of stimulating currents, and hence different operating frequencies. Surely if the synaptic decay takes to much time respect the ISI, the synaptic conductance continues to increase due to the temporal summation, and possibly leading to the failure of the neuron models. Therefore by working at higher frequency (smaller ISIs) the synaptic dynamic must be faster. For this reason we defined the synaptic time constants as function of the ISI. Specifically for the AND NOT gate, the decay time constant of the inhibitory synapse ($\tau_d = 45\% ISI = 59.40$ ms) is chosen larger respect the one of the excitatory synapse ($\tau_d = 20\% ISI = 26.40$ ms), because we addressed to the issues related to the mismatched synchronization by relaxing the dynamic of

the inhibition. Furthermore, it can be noticed that the synaptic time constants related to the AND gate ($\tau_r = 2\% ISI = 2.64$ ms and $\tau_d = 3\% ISI = 3.96$ ms) are significantly smaller respect the case of the AND NOT gate. A possible reason could be due to the fact that the AND gate needs to be designed avoiding the temporal summation effect. Indeed with the temporal summation, prolonged stimuli are reinforced and even a single firing input could provoke the output neuron activation, leading to the undesired high state. Nonetheless, the chosen values of synaptic time constants belong to the range of physiological values found in literature. For instance fastest AMPA receptors display a time constant of 0.18 ms, while for NMDA receptor of pyramidal cells it is up to 89 ms [53].

The final aim of our biocomputing research was the realisation of sequential circuits. The versatility of our paradigm is represented by the fact that these larger circuits are simply built starting from the elementary logic gates which are already trained. Therefore the tuning of the synaptic parameters does not need to be repeated. From Fig. 6.15, the memory condition related to the SR latch can be regarded. When both inputs set and reset are at the high level, the membrane potential v_Q remains at the resting state, while $v_{\overline{Q}}$ continues to firing, hence the previous output levels are kept in memory. In the gated SR latch of Fig. 6.16, the LE signal defines when the latch is transparent to the inputs. Hence, additionally to the memory condition with set and reset $[0 \ 0]$, the outputs correctly remain unchanged also when the LE signal is low. The last neuronal logic circuit here implemented is the D flip-flop, whose dynamic is displayed in Fig. 6.17a. Here, as expected, the input membrane potential v_D is sampled at the rising clock edge and replicated by the output membrane potential v_Q . It can be noticed that, nearby the first clock edge, the output response results in an unstable state. This could be interpreted similar to a metastable state, meaning that the output assumes an undefined state which is neither the high nor the low level. The reason of this is related to the fact that the neuronal flip-flop is not initialized yet, and hence the output is well-defined only after the first clock edge. Similarly in digital electronics, when the flip-flop is turned on, it can not be predicted if the initial state is the low or high level. This is the reason why often supplementary inputs, often called preset and clear are used to initialize the device. Furthermore, in Fig. 6.17a we can observe that, as in digital flip-flops, the output of the neuronal flip-flop changes after a certain delay respect the clock edge. This is defined as the propagation delay, which is the time needed between the clock edge and the resulting change at the flip-flop output Q [64]. Finally Fig. 6.17b reports and example of the behaviour of the D flip-flop with increased stimulating current I = 7pA, which results in an higher neurons firing frequency. Our simulations regarding the neuronal latches and flip-flops provide a straightforward design paradigm for the realization of sequential circuits made by neuronal cells, fulfilling the requests related to the research question number 4.

Discussion

Focused examinations of neuronal biocomputing systems with mathematical modelling will provide useful insight in how networks of biological cells could be engineered to display well-defined responses comparable to digital computations. Future efforts of the research community must concern the validation of biocomputing mathematical models with in-vitro experiments. At this purpose, recent advancements on cellular lithography are currently aiming to the control over the development of cultured networks. Cells cultures are grown over micro-electrodes, which offer the possibility of recording the biological electrical signals, even of single neurons, and electrically stimulate the network to control the neurons activity and hence also affecting their connectivity. The surface engineering of such devices is fundamental for the cellular growth, and involves the use of nanotechnologies to define the surface chemistry and the structural patterns. At this point, the in-vitro networks could benefit from the use of astroglia cells. According to recent experiments, neurons cultures display limited firing activities, while the addition of astroglia increases the neuronal activity and prevents the progressive reduction of cells sensitivity to glutamate [65]. Moreover, effects of regularisation of the neuronal messages through astrocytes-neurons communication, similar to the ones shown in our in-silico model, could be explored.

In our work we only explored the noisy dynamic of neuronal signalling with the model of synaptic gaussian noise. This phenomenon could be further characterize by the use of more complex and biologically plausible models of synaptic noise, for example with poisson-distributed noise. In addition to the noisy dynamic, the reliability of neuronal biocomputing systems needs to be characterised regarding many other complex neuronal dynamics. Among them, the nervous system displays the dependence of distinct regions accounted for different physiological functions. Hence, this mechanism, called functional brain connectivity, is crucial for the comprehension of neuronal information processing, since the inputs of a certain regions of the network could also interfere with the outputs of distant regions. Furthermore, other open questions result from the fact that the ultimate networks topology of neuronal populations is often unknown and it strictly depend on the neuronal activity due to the processes of neuronal plasticity.

Chapter 8 Conclusion

In this thesis, we proposed a mathematical model of biocomputed logic gates, exploring the computing potential of neurons and astrocytes. First, the gating capabilities of Izhikevich neurons connected with bipartite synapses where demonstrated. Then, we presented a tripartite synapse-based method used to improve the neuronal logic gates reliability. The coupling through tripartite synapses were described using a modified Postnov model coupled with a traditional synaptic conductance-based model. We showed the realization of both AND and OR gates, characterized their performance in relation to noise and quantified the denoising effects of astrocytes. Furthermore, starting from the fundamental logic gates AND NOT, NOT and NAND gates, we increased the computing power of the neuronal systems by design large neuronal circuits. Especially, we showed the capability of such in-silico networks to implement sequential circuits. This could open the way for the design of powerful biological devices with storage capabilities. Our future efforts could concern the development of an automatic method of tuning of the synaptic parameters with respect to different stimulating currents. Indeed, in Chapter 7 we showed that a change in the chosen stimulating current implicate the recomputing of the synaptic weights values. Therefore an automatic optimization algorithm, which could require non linear techniques, could be developed. Alternatively, also the application of biological processes of synaptic learning, as synaptic time dependent plasticity (STDP), could be employed for developing of intelligent systems able to reproduce the desired logic response. Main challenges related to these procedures arise due to the presence of inhibitory synapses, since the application of learning rules as STDP to inhibitory synapses is still under investigation.

The proposed design paradigm represents a valuable step toward the realisation of reliable neuronal logic gates and powerful neuronal circuits. Research efforts on this exciting area will pave the way to the development of innovative medical solutions, thanks to the use of biological computing machines.

Appendix A Generation of synthetic input patterns

In this appendix we summarise the strategy used to generate the synthetic input patterns used in the simulations of Sections 6.3 and 6.4. All the input signals of these networks, included the clock and LE signals, are obtained modifying by hand the firing pattern of the same neuron. This is a continuously firing, stimulated by a constant external current, with amplitude I = 4 pA in all the simulations of Sections 6.3 and 6.4, with the exception of Fig. 6.17b which uses an increased current I = 7 pA. The firing pattern is described by the variable flag in Eq. 4.1, which assumes value 1 at the firing instants and 0 during the resting states. Specifically, a first Simulink block receives flaq as input and counts the number of fired APs. The output of this counter block is used to trigger a switch system, which deviates between 0 and the original firing pattern flaq depending if the number of APs exceeds a certain threshold. Furthermore a second threshold, larger than the previous one, is used to reset the count of APs, in order to repeat the process periodically. Therefore, by regulating the two thresholds, different periodic firing patterns can be designed. Notice that the generation of all the input patterns from the same continuously firing neuron ensures their synchronization. As instance considering the two input patterns in Fig. 6.12, the second train of the INPUT neuron 2 is perfectly aligned with the ongoing train of the INPUT neuron 1. Alternatively, these input patterns could also be generated by using periodic stimulating currents, as a square waves. However, the synchronization of the firing patterns would be achieved only if the stimulating periods are multiple of the interspike interval. Hence, the implementation of such solution is much more complex than the solution based on switches, because the values of ISI depend on the current amplitude and they could also slightly vary during the stimulation.

Appendix B Synchronization issues

As mentioned in Section 5.2, the neuronal gating response is strongly affected by the synchronization of the input signals. Here we report two example of neuronal logic circuit with poor synchronization and we illustrate how neuronal buffers can be used to address this issue. The first example concerns about the sensitivity to



Figure B.1: Neuronal logic circuit consisting in an AND NOT and NOT gates cascade. In Fig. B.1b a neuron buffer is added to improve the inputs synchronization.



Figure B.2: Gating responses and synaptic conductances signals of the NOT gate in the neuronal circuit in Fig. B.1. Specifically, Fig. B.2a and B.2b are associated to the neuronal circuit in Fig. B.1a, while Fig. B.2c and B.2d to the circuit in Fig. B.1b.

synchronization of inhibitory synapses. Fig. B.1a depicts a neuronal logic circuit made by the cascade of an AND NOT gate and a NOT gate. Lets consider the inputs of the NOT gate. The signal at its inhibitory synapse passes trough two layers of neurons, which are the layer associated to the AND NOT gate and the layer used to generate the input pattern. Instead the signal at the NOT excitatory synapse passes only trough one layer, which is the one of the continuously firing neuron. Therefore the condition based on the balanced number of layers is not ensured, hence we expect the inhibitory input to arrive later respect the excitatory input. This can be verify looking at the synaptic conductances g_{syn} in Fig. B.2a. As a consequence, the overall gating response is affected by the presence of a



Figure B.3: Neuronal logic circuit consisting in an AND gate receiving one input from the output of a NOT gate. In Fig. B.3b a neuronal buffer is added to improve the inputs synchronization.

wrong spike, highlighted in Fig. B.2b. Notice that here, only the first inhibitory stimuli fails, since for the following stimuli the temporal summation occurs and hence the inhibitory effect is reinforced. However, if such error occurs in much complex circuits, as flip-flops, it can propagate generating other errors and possibly causing the failure of the device. In order to equalize the number of neuron layers, a neuronal buffer can be added in the branch related to the excitatory input of the NOT gate, as shown in Fig. B.1b. In that way the excitatory input is delayed, and so it is realigned respect the inhibitory input, as depicted in Fig. B.2c. With this strategy, the inputs synchronization is restored and the final output replicates the desired response (Fig. B.2d).

The second example of synchronization issues is related to the AND gate. We saw that, for the AND NOT gate and NOT gate, the presence of errors related to poor synchronization is also limited by the effect of the temporal summation, which is obtained using large synaptic time constants. Instead the AND gate is characterised by smaller synaptic time constants, hence the signal synchronization



Figure B.4: Gating responses and synaptic conductances signals of the AND gate in the neuronal circuit in Fig. B.3. Specifically, Fig. B.4a and B.4b are associated to the neuronal circuit in Fig. B.3a, while Fig. B.4c and B.4d to the circuit in Fig. B.3b.

becomes crucial because the temporal summation mechanism is not used. Fig. B.3a reports a neuronal logic circuit which consists in an AND gate with one input obtained from the output of a NOT gate. Therefore this circuit should implement the same logic behaviour of the AND NOT gate. As can be observed in the synaptic conductances of Fig. B.4a, the second input of the AND gate is delayed, because it passes though the additional layer of the NOT gate. Consequently in Fig. B.4b, the output of the AND gate does not follow the desired logic function. Again, by adding a neuronal buffer in the branch of the first input of the AND gate (Fig. B.3b), the synchronization of the neuronal circuit is fixed (Fig. B.4c) and the correct logic response is achieved (Fig. B.4d).

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