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Design and development of a gate driver for testing systems of SiC modules

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Abstract

The rushing demand for higher performances in electronics is constantly pressing the market. Nowadays the technology at our disposal has reached high levels of improvement and complexity and day by day new solutions are found.

For decades, silicon devices have dominated the power electronics market thanks to their breakthroughs in material quality, improvement of the fabrication techniques and processes, and in the architecture of the devices.

By now, unfortunately, silicon exploitation is reaching a limit and for power application this material has saturated its capabilities, having no chances to tackle the new technologies based on wide bandgap material, as an example silicon carbide (SiC) and gallium nitride (GaN), which development is mainly linked to the increased demand of renewable energy, electrification of the powertrain in the automotive systems and the growing demand for miniaturization of dimensions and increased device efficiency in power management applications.

This dissertation is focused on the design and realization of a gate driver to test silicon carbide MOSFETs devices and modules for application such as high power inverters, that allow to reach higher switching frequencies and reliability compared to the previous silicon IGBTs, with the aim of implement such a solution in a testing platform, where SiC modules and devices are contacted through needles and tested. After a brief preface to introduce the novelties and advantages that silicon carbide can offer, the design of a gate driver for a SiC half bridge is be presented. The prototype realized on a PCB has been tested and the results are discussed and commented, analyzing the pros and cons of this technology and the fundamental aspects to keep in mind when dealing with silicon carbide design.

This project is the result of collaboration with Loccioni, a family company sited in Angeli di Rosora (AN), Italy, founded by Enrico Loccioni and Graziella Rebichini 50 years ago. It designs and builds systems for measuring, managing and developing data to improve the quality and the efficiency of products and processes for industry, healthcare, environment and mobility. It fosters networks for work, education and hospitality, to sustain value exchange among different communities through connection and collaboration. Loccioni is a scientific and technological ecosystem, where projects and solutions are generated by the integration of people, visions and knowledge coming together.

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Chapter 1

A brief introduction to Silicon Carbide

Despite silicon carbide has started its employment in the electronic field since just the last decades and seems nobody have never noticed its existence before, it is not a new material at all to man. In fact, its first use goes back to the last years of the 19th century, when the American inventor Edward G. Acheson was trying to find a way to produce artificial diamonds, and invented a process to synthesise silicon carbide from silica, carbon and other additives, known as the *Acheson process*, the first industrial SiC application.
Thereinafter, many studies on the physical properties have been done, discovering the electroluminescence of SiC in the yellow frequencies. More than half a century has been needed to obtain a SiC crystal with a high enough purity level to be possible to start a research activity on this material: in 1955, Jan Anthony Lely from Philips Electronics was able to grow high purity SiC crystal through a sublimation technique named *Lely method*, launching five years later in 1960 the first research program on SiC for high temperature devices and LEDs.
Due to the limited size of the platelets and the large amount of defects that Lely methods introduced, SiC development has been set aside few years later, while another well-known material that constitutes the base of modern electronics was becoming established: the silicon.
At the turns of the '80s Yu M. Tairov and Valeri F. Tsvetkov found a way to grow SiC boule (*modified Lely method*) and successively more and more refined boules, larger in diameters and poor of defects have been obtained allowing for the first SiC wafer commercialization in 1991. From that years on, the first SiC devices such as p-n and Shottky barrier diodes came out and have been improved, besides the fabrication of SiC switching devices.

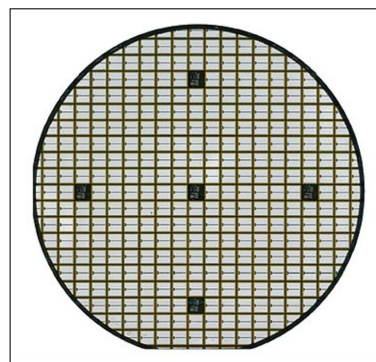


Figure 1.1: *150 mm SiC wafers*

The first SiC power transistor was a JFET released by SemiSouth in 2008. Then in 2011 came the MOSFET manufactured by Cree, considered not suitable with SiC technology in the very beginning due to interfacing problems with the MOS structure. After the initial issues with the wafer production in terms of yield and epitaxial layer defects, now the quality of manufacturing has reached high reliability levels, even if several improvements in performance and cost reduction are needed.
Nowadays the major vendors of SiC devices and modules, among which Infineon, ST, Cree, Rohm, offer a wide variety of SiC solutions at the level of the most mature silicon ones, and many companies are investing resources on this new field. Currently SiC devices are used in a large variety of power applications, for example renewable energies (photovoltaic converters, wind turbines), transportation (electric cars, trains) and many other high power demanding facilities.

Chapter 2

The SiC transistor: static and dynamic properties

Power electronics made an important step with the arrival of the Insulated Gate Bipolar Transistor (IGBT) in the early 1980s: such transistors allowed for the design of power circuits with the requirements of high blocking voltage, low on-resistance and high switching frequencies for that years, and have been the primary choice for designing these kind of circuits for many years.
As time went by, higher performances and requirements in switching speed have been more and more tight and IGBTs started showing their lacks with high losses and consequently heavy heat dissipation problems. New solutions had to be found: silicon carbide (SiC) was a material under studies since many years, but only in the late 1980s it has been tried to utilize it in power applications.
Silicon carbide is a wide bandgap material and its benefits and advantages compared to traditional silicon semiconductor are several, for example:

- the SiC energy gap is around 3 times higher than that of silicon allowing for higher breakdown voltage and electric field around 10 times higher than silicon devices; nowadays 1700 kV SiC devices are available in the market. For an equivalent silicon breakdown voltage, smaller die size are needed, reducing parasitic capacitances and the circuit dimension;
- the higher thermal conductivity makes it possible to operate at very high temperatures without damaging the device, reducing the weight and dimension of heat sinks. In some cases, with accurate package design, temperatures above 200 °C can be reached;

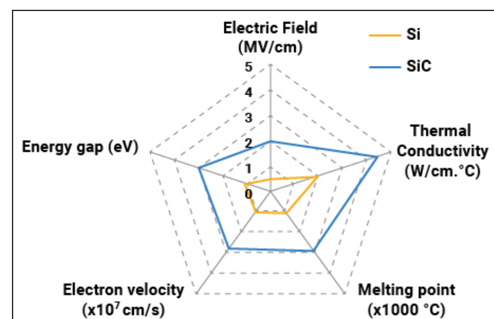


Figure 2.1: *SiC vs Si stats*

- very high switching frequencies can be obtained, reaching hundreds of kilohertz, whereas IGBTs stop just at some tents of kilohertz because of losses increase. As a consequence of the frequency increase, the size of capacitors and inductors for filters can be reduced dramatically.
- unlike IGBTs, SiC transistors do not show tail currents in their turn-off transient due to minority carrier recombination, so the transition edge is sharper, allowing for low losses and fast commutations;

In contrast, SiC MOSFETs need some expedients to work correctly. Figure 2.2 shows an example of comparison between the I-V characteristic of an IGBT and a SiC MOSFET: it can be easily noticed that the IGBT curves have a sharp transition between saturation and active state, while the SiC curves are globally smooth and exhibit a more linear behaviour without evident transition. Moreover, the IGBT curves reach high current

values at lower gate voltages. Normally, SiC transistors have smaller transconductance g_m, and thus a lower gain, therefore they must be driven at higher gate voltages as 20 V or beyond.
Another motivation to drive the SiC transistor at high gate voltages is to achieve low R_{DSon}, in order to obtain faster transitions and avoid thermal runaways: figure 2.3 depicts the dependence of the R_{DSon} on V_{GS} and temperature of a Si and SiC MOSFET. While for a Si MOSFET the increase of V_{GS} leads only to a higher switching speed, in SiC devices it also reduce conduction losses.
For what concerns temperature, yet at 25°C the SiC MOSFET shows a lower R_{DSon} that, due to its negative temperature coefficient, does non increase with such a high rate as in the Si device.
The choice of the gate resistance has an important role in a SiC transistor: current peaks from the gate driver may cause switching losses due to the SiC MOSFET high sensitivity to the common source inductance and switching loop parasitic inductance. Therefore sizing a gate resistance, not too high to slow down the commutations and not too low to have ringings, is a necessary part of the design [6].
Even if the devices are fully turned off at 0 V, a negative bias is preferable to facilitate the discharge of the gate capacitance; globally the total voltage swing that the gate driver must provide can be quite large, and the fast variations across this voltage interval might trigger undesired turn-on of these devices due to Miller effect, which can cause heavy short circuit and damages to the device if not considered. Therefore a negative bias reduces crosstalk due to high dv/dt and di/dt in half-bridges that may induce false turns-on.
Due to its smaller size compared to the IGBT, SiC MOSFETs have less thermal dissipation capability, and this aspect is critical when facing with surge currents in short circuit conditions.
Another important advantage of Silicon Carbide is the very small reverse recovery time of SiC diodes. When a diode has entered a reverse-biased state, it does not immediately turn off completely, and a reverse current flows for a while: t_{rr} is the recovery time in which the reverse current is flowing. The lack of minority carrier injection and the temperature independence, leads to a very fast turn-off and low switching energy with respect to a silicon device (fig.2.4), low di/dt and therefore low electromagnetic noise. For these reasons when silicon devices are still a solution, they may come with a SiC intrinsic diode.
However, one drawback of SiC transistors are the higher switching losses compared to the silicon FET: the input capacitance C_{iss} of the SiC device is smaller, and therefore the on-off gate switching is faster, but the reverse capacitance C_{rr} is similar for Si and SiC transistors. The last ones unfortunately show a smaller transconductance g_m as stated before, and this leads to a slower discharge of the reverse capacitance at every switching cycle, so higher switching losses.

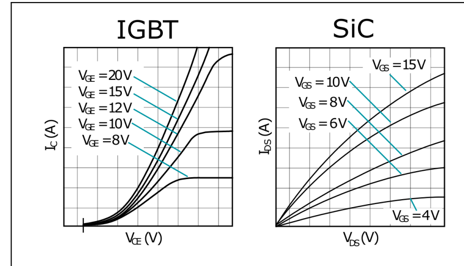


Figure 2.2: *$I_{DS} - V_{DS}$ curves comparison for IGBT and SiC MOSFET.*

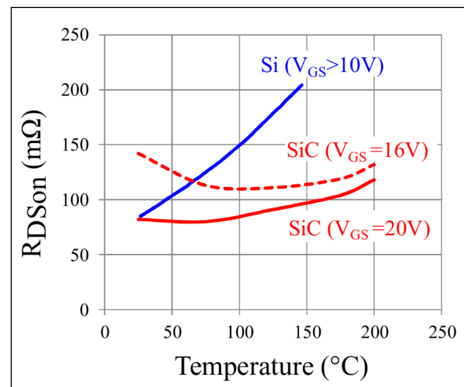


Figure 2.3: *R_{DSon} of a Si CoolMOS and a SiC DMOSFET [4].*

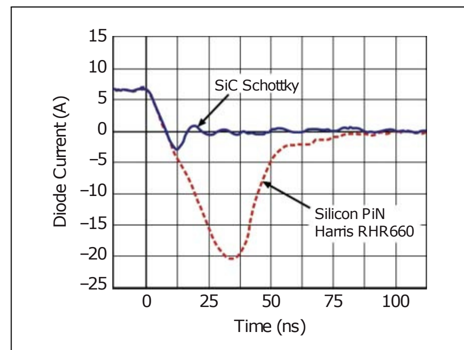
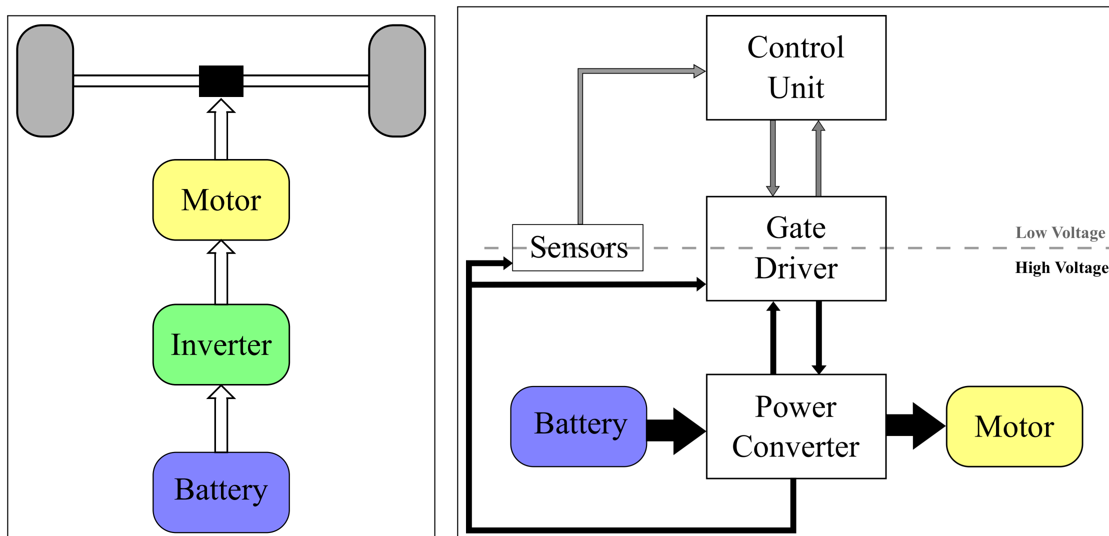


Figure 2.4: *Reverse recovery time of a Si and SiC diode at 150°C [10].*

Chapter 3

Gate drive state of the art

With the rise of electric cars on the market, power electronics has found new horizons and new challenges to face: the use of high power modules in environments such as vehicles, in close contact with people and in continuous movement, defines stringent criteria in terms of reliability, performance and safety, which promoted the growth and development of this sector.
The critical component in an electric vehicle, where most of the electronics relies on high power modules, is the inverter. As shown in figure 3.1a, the inverter is the block that connects the battery pack to the motor and converts the DC voltage supplied by the batteries to an appropriate AC voltage suitable for the motor.
Inside the inverter, low and high power electronics cooperate to control the amount and the quality of the power delivered to the motor, surrounded by sensing and protection circuitry to avoid faults.
A basic scheme of the inverter main blocks is reported in figure 3.1b. The control unit performs functions such as communication (input/output), data storage, signal/data processing, control algorithms and commands, and provides an interface to the gate driver, which task is to amplify the command signals from the microprocessor and make them suitable to drive the gates of the power transistor or modules of the power converter. This block operates as interface with digital and power signals, therefore proper attention is required to let the system work fine.



(a) *Simple electric vehicle core scheme.*

(b) *Main building blocks of an automotive inverter.*

Figure 3.1: *Main components of an electric vehicle*

3.1 Three-phase Inverter working principle

The typical three-phase power converter (figure 3.4) consists in principle of 3 branches each of which have a High-Side and a Low-Side transistors controlled by the output of the gate driver. The motor (load) is connected to the switching node of each branch. It is common to use more transistor in parallel in each side to carry more current, or more transistor in series to increase the maximum voltage drop.

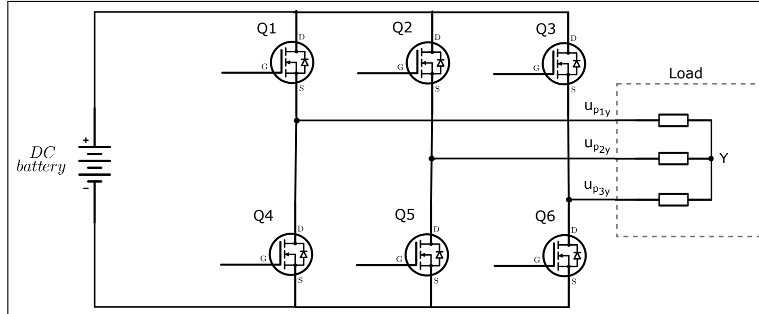


Figure 3.2: *Basic scheme of a power converter*

Applying an appropriate PWM pattern to each couple of gates in the branches, in counter-phase between High-Side and Low-Side, and phase-shifted by 120° among each phase, it is possible to modulate the duration of the driver pulse. One of the most used modulation is the SPWM (Sinusoidal PWM): a comparator is used to compare three sine waves 120° phase-shifted with a triangular wave at higher frequency (fig. 3.3a). The result is a PWM output which pulses has a duration proportional to the time during which each of the sine wave amplitude is higher then the triangular wave one. This pattern is given at the gate driver that switches the power transistor on and off, obtaining the half bridge voltages shown in fig. 3.3b-d). By subtracting two phase voltages in one period, three combination of bipolar PWM pulses are obtained (fig. 3.3e-g). The PWM pattern is then filtered to obtain an AC voltage at the same frequency of the previous sine wave, depicted in black.

The gate driver is a power amplifier that converts the low power signal from the controller into high current signal for the switches and is the most crucial part, since it interfaces with both the low voltage control signals and the high power signals of the converter. Therefore an electric isolation is required to create different ground references and avoid high voltage interference that may lead to damages to the control side and to electric shocks to humans, since the low voltage side is accessible.

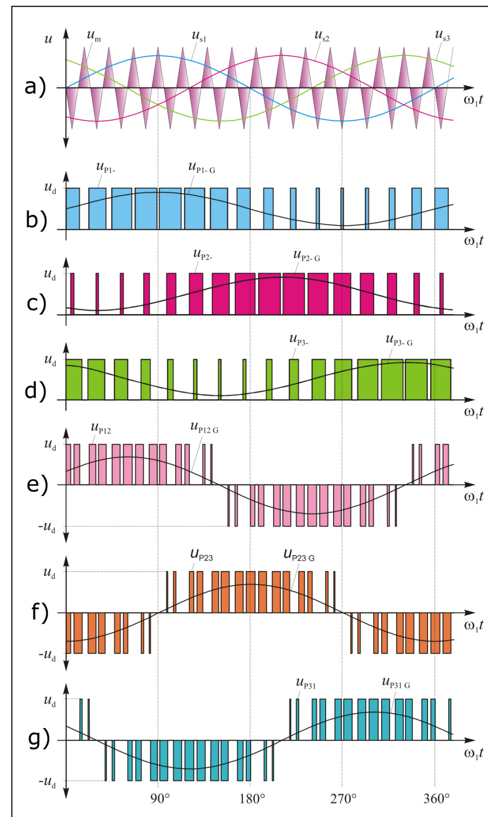


Figure 3.3: *Pulse control scheme of a three-phase inverter [15].*

3.2 Isolation and CMTI

As soon as power densities and frequencies increase in power devices due to the demand and availability of information transaction, and circuit dimensions scale down, an integrated solution to allow data and power transfer among the low-power and high-power ICs is needed. Isolation is a means to break the ground loops created in circuits that have high power in play. Modern gate drivers chips have an integrated isolation system that merges the benefits of an external gate driver transformer (low propagation delay) and of an isolator IC (small size and reliability).
Integrated isolation can be achieved through three main techniques: optical, magnetic and capacitive. Optical isolation consists in transmitting the signal with a LED from the control side to a phototransistor receiver on the high voltage stage. The photonic signal coming out from the LED acts as isolation barrier. Magnetic isolation uses transformer coils, separated by an air gap, to transfer the signals between the two sections. Capacitive isolation transfers signals through the electric field across two metal plates of the control and high voltage section.

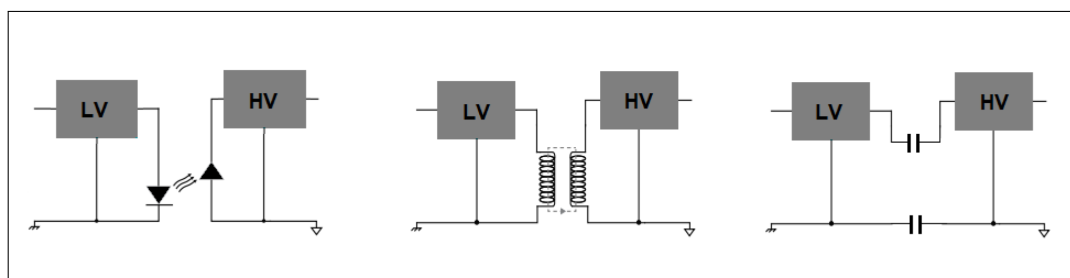


Figure 3.4: *Isolation methods. From left to right: optical, magnetic, capacitive.*

Among these techniques, the magnetic isolation offers higher isolation voltage up to tens of kilovolt, is more robust and can withstand overvoltages better than optical or capacitive devices, but usually is the most expensive solution. Capacitive isolation uses a physical barrier with insulating materials and allow high speed signal transfer and good noise immunity, but the current consumption is greater than the case of magnetic isolation. The optical isolation is the oldest and most mature technology, it uses physical barrier with insulators as well as the capacitive solution, but is the most sensible to aging and propagation delay variation due to temperature influence and it needs a relatively high current for driving the LED.
There are three main categories of isolation: functional, basic and reinforced. Functional isolation guarantees correct operation of the circuit, but no protection against shocks. Basic isolation provides sufficient protection against electric shock as long as the isolation barrier does not break. Reinforced isolation is recommended for safety guidelines, providing redundancy and doubling the basic isolation level.
The choice of the isolation technique is based on the required isolation level, performances, Common Mode Transient Immunity (CMTI) and lifetime.

CMTI is defined as is the ability of an isolator in the gate driver IC to tolerate high-slew-rate rise and fall time transient between its two isolated grounds blocking corrupting signals passing through it, and is an important parameter to consider when switching frequencies become high. It is measured in V/ns or kV/µs and a high value of CMTI means that the two isolated parts of the circuit can work fine at high positive and negative slew rates. The criteria to test CMTI are called static and dynamic and the aim is to verify that the output of the circuit behaves correctly in presence of a CMT pulse: in the static test the output should stay in the right high or low level while the input is fixed, in the dynamic test the correctness of the output is verified with the input switching.

3.3 Drive strength

The gate driver should supply the correct current to the power switches to charge and discharge their input capacitance in the right time, therefore knowing the gate charge Q_g, the right amount of current is given by $I_G = \frac{Q_g}{t_{rise/fall}}$, where $t_{rise/fall}$ is the desired gate voltage rise or fall time.
The critical part is the Miller plateau, where the gate voltage is constant due to the switch turn on, and the gate-drain capacitance C_{gd} start charging, while the drain-source V_{ds} is still high and starts falling. Here, beside a turn-on slowdown there is a dynamic power consumption due to the fact that the drain voltage start falling after the drain current is already high. Figure 3.5 shows the gate charge plot and the drain current and voltage during the turn-on. The red shaded area represents the dynamic power in correspondence to the Miller plateau. To reduce these drawbacks the gate driver must supply the maximum current during the Miller plateau, and this depends on the gate resistance and the driving voltage.

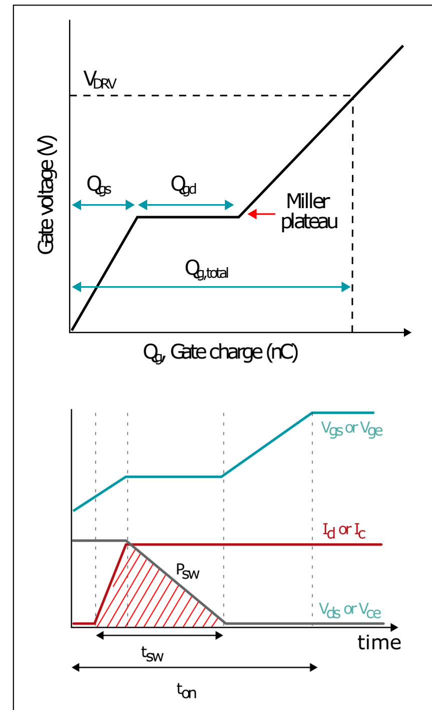


Figure 3.5: *Top: gate charge plot. Bottom: device turn-on waveforms [1].*

3.4 Split outputs

The gate driver has usually two outputs to control separately the turn-on and turn-off of the power switch. This is useful to select the desired rise and fall time based on the gate resistance, since it is usually required a fast turn-on transient to have fast response and low losses (so a low R_{gON}) and a slower turn-off due to voltage overshoot caused by high di/dt.

3.5 Dead time and Interlock protection

The two transistors in the half-bridge configuration must not be in conduction at the same time to avoid short circuit fault, therefore a dead time between the commutation of the High-Side and Low-Side driver must be present. In this period of time none of the switches is turned on. It is clear that this period should be as short as possible to minimize delays, but there are some aspects to consider for choosing the right dead time: the propagation delay mismatch of the rising and falling edge (pulse-width distortion), the propagation delay of the pulses and the duration of the rise and fall time.
During the dead time the current flows through the body diode that has a larger voltage drop with respect to the switch, so a large dead time means high conduction losses due to heat, reducing the efficiency. In SiC transistor, where the frequencies are very high, it is very important to control the dead time, since dynamic power is proportional to frequency. It should be at least equal to the propagation delay, defined as the time required from 50% of the input to 50% of the output. A further safety measure is usually implemented by Interlock Protection, a feature integrated in gate drivers to prevent shoot-through, usually a logic circuit that combines positive and negative input signals to avoid their simultaneous activation: in case of failure in the user-programmed dead time, the Interlock makes sure that the driver inputs do not switch at the same time.

3.6 Bootstrapping

To drive the High-Side switch, the gate driver takes the switching node of the half bridge as reference (the source of the High-Side or the drain of the Low-Side), therefore, if the two sides have no separated power supply, the High-Side driver has to provide a voltage that is higher than the threshold voltage to turn on the High-Side MOSFET. A Bootstrap circuit allows the increase of the gate voltage of the High-Side switch above the positive supply rail while the High-Side driver is turned on. Following the schematic in figure 3.6(left), the circuit consists of a diode and a capacitor C_{BST}: when the Low-Side is active, the capacitor charges up through the diode to the supply voltage minus the diode voltage; when the Low-Side turns off and the High-Side turns on, the bottom node of the capacitor is disconnected from the negative supply voltage and keeps the DC voltage source across the High-Side driver, resulting in a High-Side switch gate voltage greater than the supply rail.
However this solution is not practical, and two separated gate drivers for each side are preferred; in this way the High-Side and Low-Side switches take as reference their own sources, separated and isolated, avoiding the cumbersome voltage increase above the supply rail.

3.7 UVLO

As stated above, the SiC MOSFET must be driven with a minimum gate voltage to prevent overheating and loss of performances. The Under Voltage Lock-Out feature (UVLO) monitors the supply pins of a gate driver to guarantee that the voltage is above a certain threshold and ensures correct operation. Since the low output voltage of the driver is usually negative to switch off the transistor faster, the UVLO might be referred to negative supply voltage or to the common node as shown in figure 3.6(right).

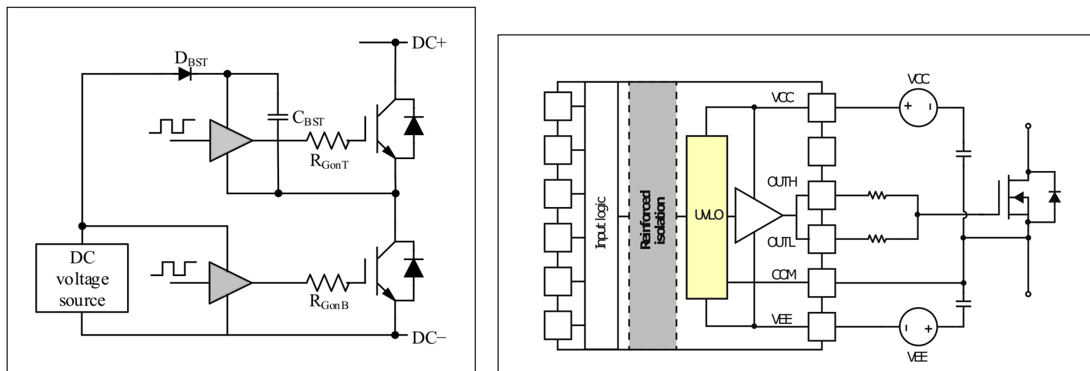


Figure 3.6: *Left: Bootstrap circuit [9]. Right: Example of UVLO section referred to common node in a gate driver circuit [2]*

3.8 Snubbers

High voltages and currents may cause noise glitches that couple with the gate drivers, leading to unwanted spikes at the input of the power switches that might turn suddenly on if the magnitude of these spikes is sufficiently high. To avoid this, an input deglitch filter is used to eliminate spikes at the output of the gate driver; usually it filters pulses of some tens of nanosecond (around 50 MHz), a frequency much higher than the switching frequency of the MOSFET.
When a MOSFET turns on, the parasitic inductance of the PCB layout couples with the parasitic capacitances of the transistor: the current stores energy in these parasitics and the stray inductance resonates with the capacitances, producing ringings and overshoots. A snubber circuit properly designed and placed close to the power switches can be used to dampen this effect. The simplest snubber consists of a capacitor connected in parallel

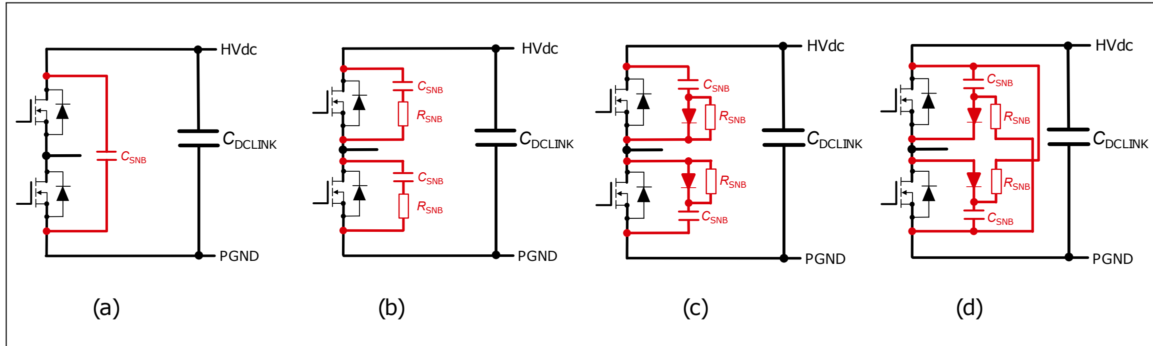


Figure 3.7: *Snubber circuits. (a) C snubber, (b) RC snubber, (c) Discharge RCD snubber, (d) Non-Discharge RCD snubber [14].*

across the phase leg (figure 4.16(a)): this solution is the cheapest but it may be not well suited for discrete components due to the long wire that introduce stray inductance.
A second solution is to place a RC series across each power MOSFET as shown in figure 4.16(2), in this way the snubber can be placed closer to the single switch. The capacitor has to dissipate its energy through the resistor every switching transient, but if the switching frequency is high, the resistor would dissipate a high amount of power, up to several watts, therefore the capacitance must be reduced, as the effectiveness of the snubber.
An improvement can be introduced by adding a diode as in figure 4.16(c) with the Discharge RCD snubber: during the turn-on the power dissipated by the resistor is the same, but the capacitor dampening is more effective since surge currents flow through the diode. In this case particular attention has to be put in the recovery characteristic of the diode and to the high di/dt that may arise. The same circuit can be rearranged by putting the resistor in parallel with the capacitor.
The last kind of snubber considered is the Non-Discharge RCD snubber in figure 4.16(d), where the resistor dissipates the energy of the capacitor produced only on the overvoltages, and not in all the switching transient as before, limiting the energy consumption of the resistor with increasing switching frequencies. A large capacitor can be used but this solution requires a complex wiring that requires more PCB layers.

3.9 Miller Clamp

Another cause of unwanted turn on is the dv/dt-induced turn on that takes place when a switch is to be turned off by a low voltage on its gate and its drain voltage raises rapidly to the high voltage value, resulting in a high voltage variation across the drain-gate capacitance C_{gd}. This event causes the gate voltage to increase due to Miller effects by a quantity $V = C_{gd} \cdot \Delta t$, and if this voltage is higher than the threshold voltage of the transistor, it turns on causing short circuit. In this case the Miller Clamp helps to discharge the transistor to be turned off avoiding Miller effect. It consists on a low resistance path between gate and ground or negative supply voltage made by a transistor (in blue) as shown in figure 3.8. The Miller clamp may be placed externally to the driver or internally: the first solution reduces the cost of the components but it must be placed close to the switch to reduce parasitics along the discharge path, the external solution is still controlled by the driver and is more suitable with very high dv/dt, because it can be placed very close to the gate.

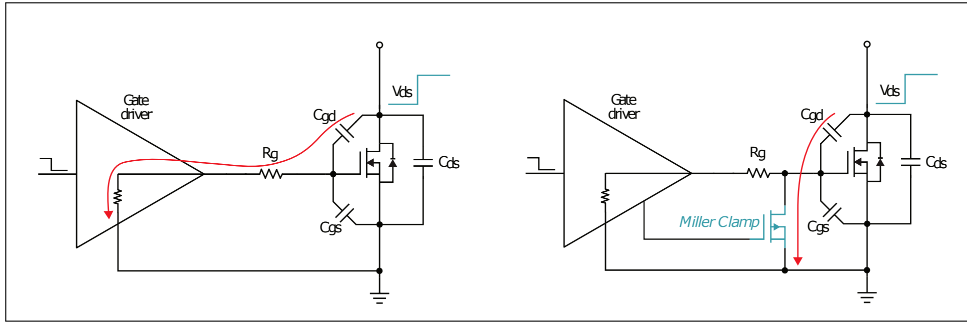


Figure 3.8: *Active Miller Clamp, internal (left) and external (right) [1].*

3.10 Short circuit protection

One of the main causes of failure of power circuit are short circuits and therefore a good control is essential. SiC MOSFETs need a special care in this aspect due to their fast switching capability and due to the smaller dimension compared to the IGBTs, that lead to a lower short circuit withstand time. A good short circuit protection must be reliable and provide a fast response in order to interrupt the current flow in a short time and prevent damages due to overheating.

3.10.1 Desaturation

There are different ways to control the current flow. The most common is the desaturation control, but while this method is easy to apply to IGBTs, it is more critical for SiC MOSFET because of the different I-V curves: referring to figure 2.2, desaturation control in IGBTs consists on monitoring the collector-emitter voltage V_{ce} and detect when it reaches the threshold voltage V_{DESAT}, correspondent to the neighbourhood of the current knee, as shown in figure 3.9, usually around 7-10 V, approaching the active region. When this threshold is reached, after a short delay time, the circuit is shut down to prevent damages.

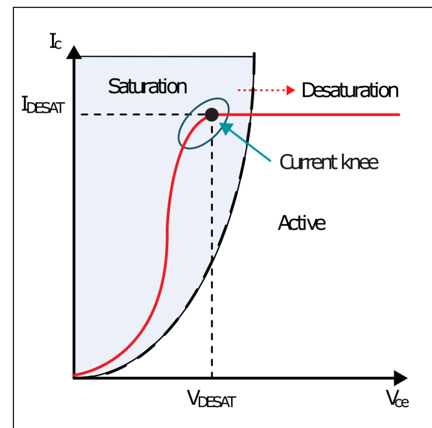


Figure 3.9: *Desaturation in IGBTs [1].*

The delay time (also called blanking time) must be long enough to prevent false short circuit detection but shorter than the short circuit withstand time (SCWT), and for IGBTs it is a safe technique since the current does not present a high slope out of saturation because the device is out of the ohmic region. A common technique to pull down the gate voltage and switch off the transistor in case of short circuit is the soft turn-off, which consists on draining the current gradually from the gate to limit the di/dt and the power overshoot, preventing the device breakdown.

Since a SiC MOSFET does not show a sharp transition, it is difficult to establish a threshold for detecting desaturation. When a SiC MOSFET reaches the established desaturation voltage, the current continues increasing. Applying a delay time to avoid false triggering can be dangerous because of the linear increase of I_{ds} during this time and due to the fast switching speed of the SiC devices, that may lead to a not in-time short circuit intervention. For a high frequency power converter, numerous switching cycles can occur before a desaturation fault is recognized [8].

3.10.2 Current monitoring through a shunt resistor

A more accurate method to monitor the current in a SiC device is using a shunt resistor. This requires less components compared to the desaturation technique and this implies faster response, but also leads to a high power consumption due to the voltage that arises across the shunt. Some device reduces this problem by integrating a second source pin (sense) where the current flow is a portion of the total drain current, and then to this pin is connected the shunt. Manufacturers provide the drain current scaling factor and it is possible to obtain the total current saving a conspicuous amount of power and avoid overheating [3].

3.10.3 Current monitoring through a Rogowski coil

A further method to monitor the current, particularly suited for AC and impulsive currents, is by means of a Rogowski coil. It consists on a conductor wrapped in helical fashion where one end of the conductor returns back through the core of the coil (usually an insulator like plastic) reaching the other lead. In this way one has the two leads on the same side of the coil, which surrounds the wire from which the current has to be measured, as shown in figure 3.10a. The output voltage of a Rogowski coil is given by:

$$v(t) = \frac{-An\mu_0}{l}\frac{di}{dt}$$

where $A = \pi r^2$ is the area of the small loops, n is the number of the loops, μ_0 is the magnetic permeability and l is the circumference of the coil. Since the voltage $v(t)$ is proportional to the derivative of the current to be measured, an integrator after the coil is needed to obtain the original waveform. Rogowski coil has the advantage to have high linearity, wide current range measurement and very fast response above tens of megahertz, with no magnetic saturation due to the absence of a magnetic core. It forms an open loop, so it is flexible and can be wrapped around the conductors. On the counterpart, the need for an integrator is a limiting part because this last circuit must have a fast response to follow the coil signal and, on the other side, the low frequency range is limited because of the discharge of the integrator capacitor that reduces the integrator accuracy if the pulse width is too long.
Even if the cost of this setup is globally low, high accuracy is required to design a Rogowski coil layout onto a PCB. To prevent interferences of nearby high currents, the coil can be designed with two wire loops in two layers of the PCB, wounded in opposite direction to cancel electromagnetic interference (fig. 3.10b), otherwise other layers can be added on top and bottom of this structure as ground planes for shielding (fig. 3.10c): in this design described by [13], the coil is printed around the connection hole of a half bridge module in a 6 layers PCB: top and bottom layers are the ground planes, the following two internal layers are used to construct the winding and the last middle layers for the return wire.

3.10.4 Hall sensors and current sense transformers

Hall sensors are metal stripes along which the current to be monitored is applied. In the presence of a magnetic field, the electrons in the metal strip are deflected toward one edge, producing a voltage across the short side of the strip (perpendicular to the feed current). these sensors can measure DC currents unlike inductive sensors as current sense transformers, where the current to be measured is fed into the primary coil and scaled down by the turns ratio on the secondary coil. Inductive sensors offer an intrinsic isolation due to its structure, and it makes the measurement free from noise generated by the board and from common mode disturbs.
Measurements of power signals require isolation, therefore using isolated sensors or isolators is necessary: as an example it is possible to measure a current through a Hall sensor and then amplify the voltage output through an isolated op-amp, or using ICs that include the sensor with the isolation.

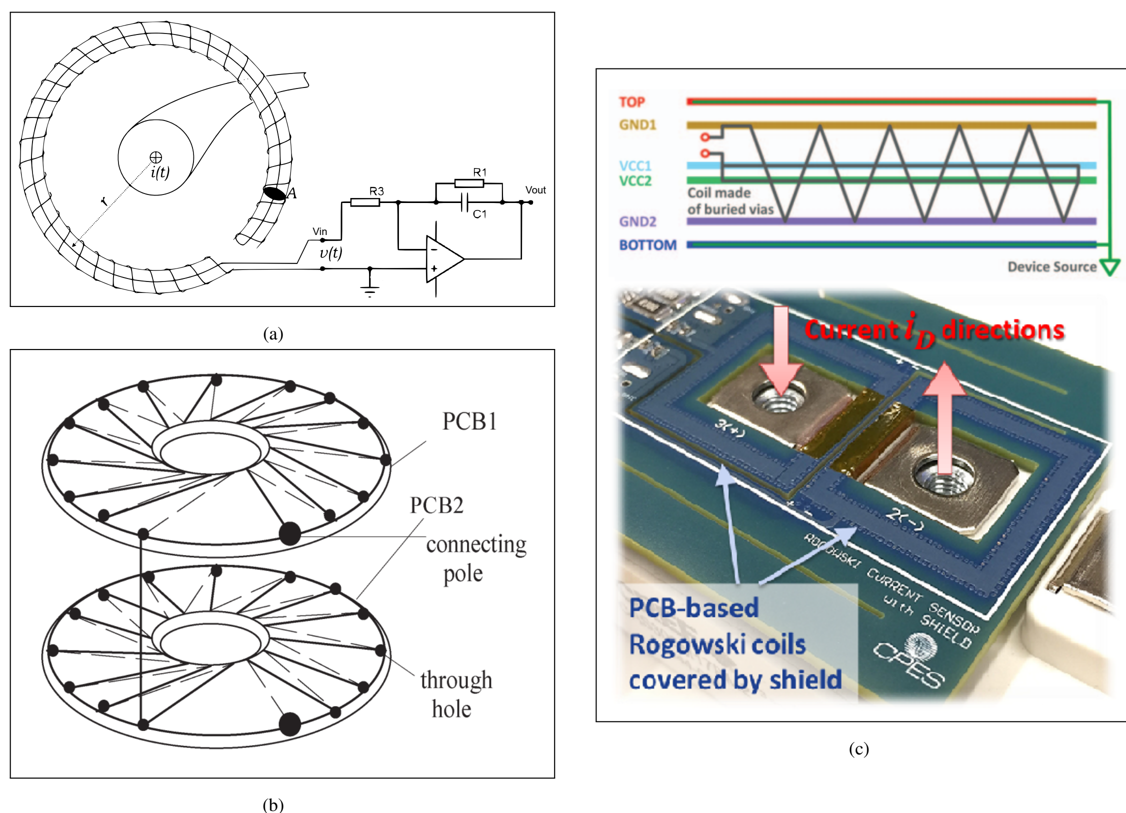


Figure 3.10: *(a): Rogowski coil measurement system [11]. (b): Two-layers Rogowski coil [12]. (c): Example of a 6-layers Rogowski coil design [13].*

3.11 Layout expedients

The switching speed of SiC MOSFETs makes it critical to provide a good layout of the gate driver circuit: at such frequencies, every single centimetre of PCB trace added is critical and the stray inductance introduced is not negligible at all.
The driver IC should be placed as close as possible to the power device to reduce the gate loop inductance.
The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high di/dt and voltage spike on the parasitic inductance of PCB traces.
The ground pin of the driver IC should be connected as close as possible to the source terminal of the transistor to separate the gate loop from the power ground loop. If the transistor provides the Kelvin connection, connect the driver ground to this pin.
Metal connections or traces below the driver IC have to be avoided; to better reduce noise coupling between input and output side and compromise the isolation barrier, a PCB cutout is suggested between the input and output side.
When a high-side and a low-side drivers or paralleled transistors are used, symmetric gate drive path design is a key point to achieve a correct signal distributions.
Components with different supply voltages must be grouped together and be isolated from the others. If a signal must cross areas with different supply voltages, isolators are required to avoid interference, as an example when acquiring power signals through sensors and carry them to the microcontroller.

Chapter 4

Gate driver design

The aim of this project is to let switch the transistors with a DC bus voltage up to 800 V and analyzing the behaviour of the switching transients varying different circuit parameters. The circuit topology adopted for this project is the half-bridge configuration, that includes two power switches (High-Side and Low-Side) connected in series between the DC rail, and the load (an inductor) connected between the switching node and the positive or negative rail of the bus DC, as shown in figure 4.1. Each gate is driven by its driver circuit that sends the PWM pulses: in this case where the load is connected to the positive rail, when the Low-Side is ON and the High-side is OFF the current flows through the load and the Low-Side, in the opposite case the load discharge itself through the High-Side. During the dead time, when both the MOSFETs are OFF, the current flows through their intrinsic diode.

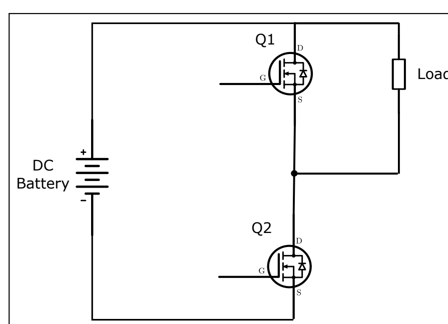


Figure 4.1: *Design circuit topology.*

4.1 Transistor choice

The main aspects that determined the choice of the device under test are the availability on the market, the possibility to obtain a Spice model to take into account all the parasitic parameters as best as possible, and a high breakdown voltage.

Considering these main requirements, the transistor adopted for this project is the C3M0016120K[16] from Cree/Wolfspeed. Its main characteristics are a blocking voltage of 1200 V, a continuous drain current rating of 115 A and a on-resistance $R_{DS_{ON}}$ of 16 mΩ at 25°C in a TO-247-4 package. The peculiarity of this device is the presence of the Kelvin source terminal, made for splitting the gate ground loop and the power ground loop and so avoiding the stray inductance sharing between the two paths.

In a 3-pin device, during every switching cycle, the stray inductance of the source wire bonding, that could be around few nanohenries, coupled with the slope of the current, generates a voltage signal opposite to the driving signal (V_{GS}) of a MOSFET, when the current is interrupted. The effect of this opposing signal is to slow down the switching cycle, which in turn increases the switching loss cycle by cycle. Looking at figure 4.3, the effective driving voltage is:

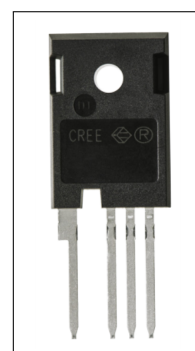


Figure 4.2: *C3M0016120K SiC MOSFET*

$$V_{GS} = V_{DRV} - V_{LS} = V_{DRV} - L_{Source}\frac{di}{dt}$$

The introduction of the Kelvin source pin allows separating the path of the power from that of the driving signal and to refer the driving network to the Kelvin source, where no current is supposed to flow. In this situation, it is possible to obtain a driving signal which is immune to any disturbance deriving from the very large and fast current variation flowing though the power path. This results in the reduction of the overall power loss in the transistor, and consequently a lower operating temperature and potentially more reliable and longer lasting power systems.

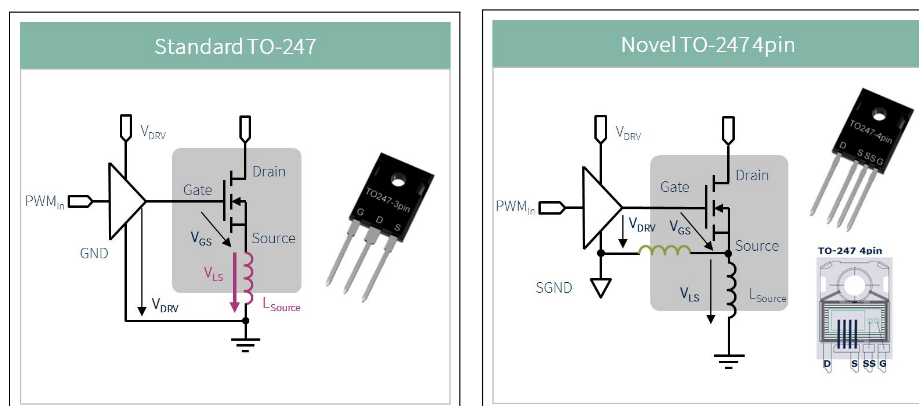


Figure 4.3: *Gate drive schematic with parasitics in a 3-leads (left) and 4-leads (right) MOSFET package.*

4.2 Gate driver IC

Due to the significant gate capacitance of the transistor (around 6 nF), a strong driving current is necessary. The UCC21710QDWQ1[17] from Texas Instruments is a single channel gate driver for IGBT/SiC with a ±10 A peak source/sink drive current and 5.7 kV_{RMS} single channel reinforced isolation and a capacitive isolation technology between input and output side of 1.5 kV_{RMS}. The main features of this chip are:

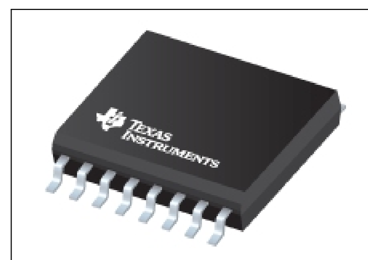


Figure 4.4: *UCC21710-Q1 driver IC*

- split outputs for turning ON and OFF the gate through separate paths, respectively with a voltage VDD and VEE referred to a common node (COM) in the isolated side;
- internal active Miller clamp which activates a pull-down internal MOSFET to force the output of the driver low (VEE) when it raises above 2 V VEE when the MOSFET is supposed to be off;
- overcurrent protection with soft turn-off through the sensing pin OC, which activates the fault when its voltage raises above an internal threshold of 0.7 V. The soft turn-off allow for a smooth decrease of the gate voltage to avoid high dv/dt. This system allows for desaturation method, by designing a proper R-C network to set the current limit and the blanking time, or shunt-based protection by sensing the voltage across the shunt resistor and compare it with the internal reference voltage;
- isolated analog sensing pin with PWM output suitable for temperature sensing through a NTC or thermal diode or for power supply voltage monitoring. The output duty cycle can be directly measured by the microcontroller and it is proportional to the analog sensed magnitude.
- inverting and non inverting PWM input for implementing interlock between two switches of a phase leg;
- UVLO below 12 V, minimum CMTI of 150 V/ns, enable/disable and fault alarm pin on over current;
- interlock protection feature, by cross-connecting the PWM input of a couple of driver ICs.

4.3 LTSpice simulation

At this point a simple LTspice simulation has been performed to estimate the behaviour of the system during the switching cycles.
From the Wolfspeed website it is possible to download the libraries necessary to include the transistor model and a documentation on how to simulate it. This model provides the four pins plus two more pins for the junction and case temperature, which at least one of them must be connected to a voltage source to fix the junction temperature or to a heat sink model to have convergence in DC simulation. In this case, a heat sink model has been used, with real data taken from a heat sink that has been used for this project.
The model include the parasitic inductance and resistance of the electrodes, and the transistor capacitances.
The spice model of the driver IC is not available, therefore it has been modelled as described into the datasheet (figure 4.5) for the gate driving side, by adding the two internal resistors R_{OH} and R_{OL}. The values for the VDD and VEE have been taken referring to the maximum values indicated in th MOSFET datasheet for the gate voltage (15/−4 V).
The load data are taken from a coil wound in air on a carton tube, which has been measured through the RLC meter obtaining values of 101 µH and a series resistance of 140 mΩ, also used as load to further test the circuit.
The simulated circuit is reported in figure 4.6a. The two ideal diodes have been used to elucidate the split output characteristic of the driver. Since the voltage drop across the diodes is about 0.66 V, the gate voltages have been raised to 15.66/−4.66 V in order to have the correct levels decided previously at the transistor gate terminals.

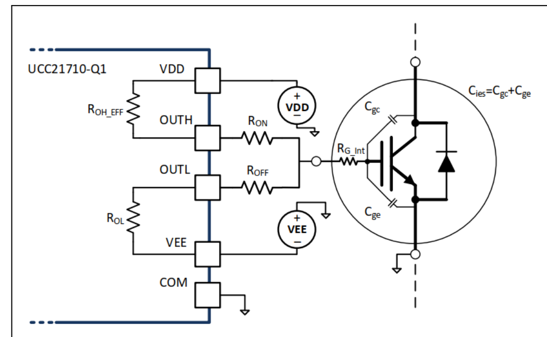
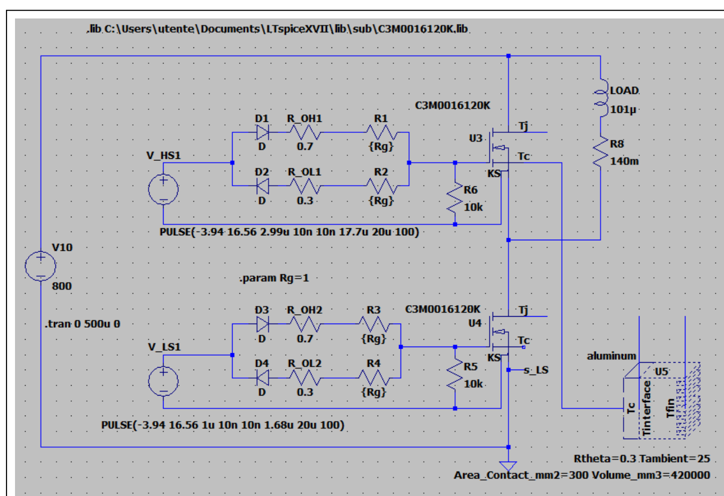
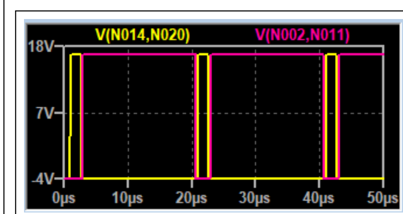


Figure 4.5: *Internal driver IC circuit*

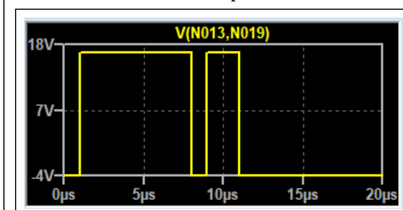
The driving signals are two complementary PWM with frequency 50 kHz, duty cycle 10%, and dead time of 300 ns. As first approach, a 1 Ω gate resistor has been used.
Other simulations have been made with a double pulse test (DPT) pattern, which consist on a first long pulse to charge the load up to a certain current, and a second short pulse to observe the commutation of the device at that current level. The DPT is applied to the device under test, in this case the low-side MOSFET since the high side is used as freewheeling path, while keeping the V_{GS} of the high-side low.
In the following figures are depicted the voltages and currents obtained from the simulation.



(a) *LTSpice simulation circuit*



(b) *PWM test pattern*



(c) *DPT test pattern*

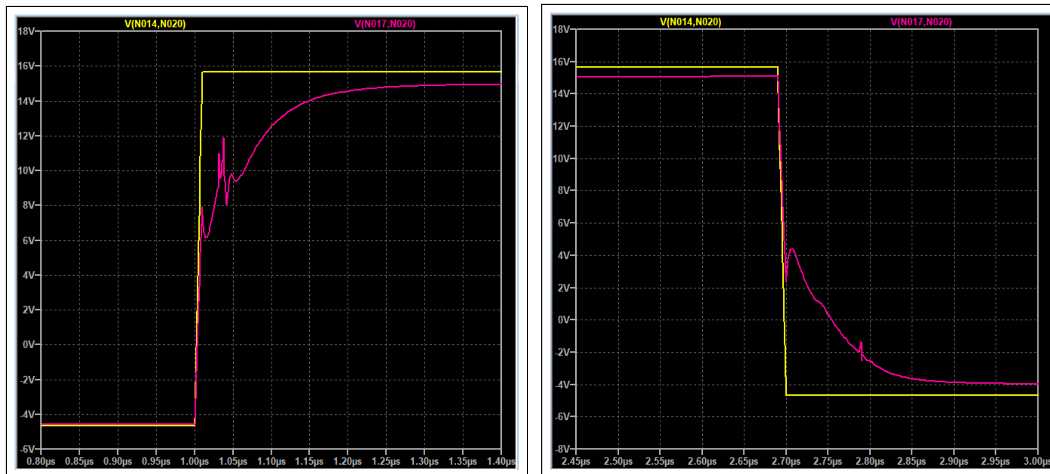


Figure 4.7: *LTSpice simulation. Yellow: PWM signal. Magenta:* V_{GS} *low-side*

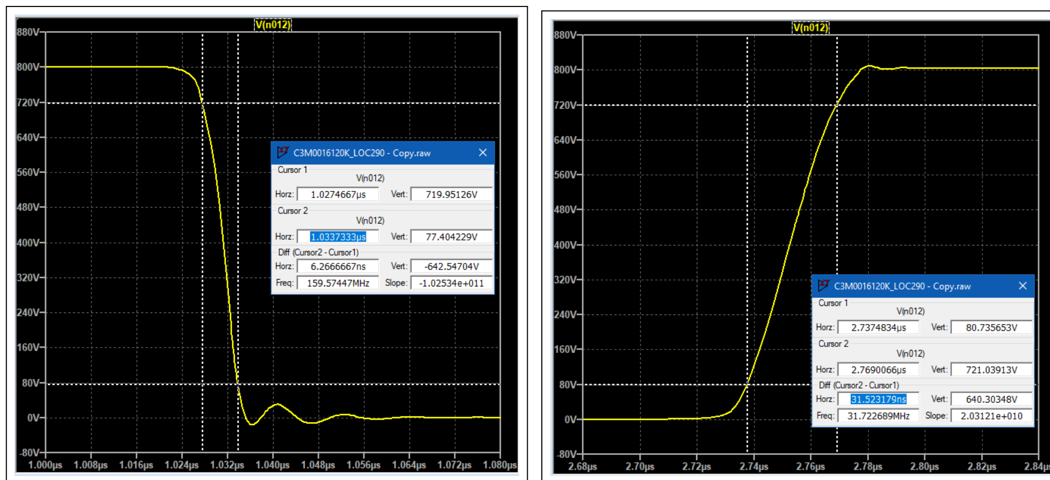


Figure 4.8: *LTSpice simulation. Yellow:* V_{DS} *low-side at gate turn-on (left) and turn-off (right)*

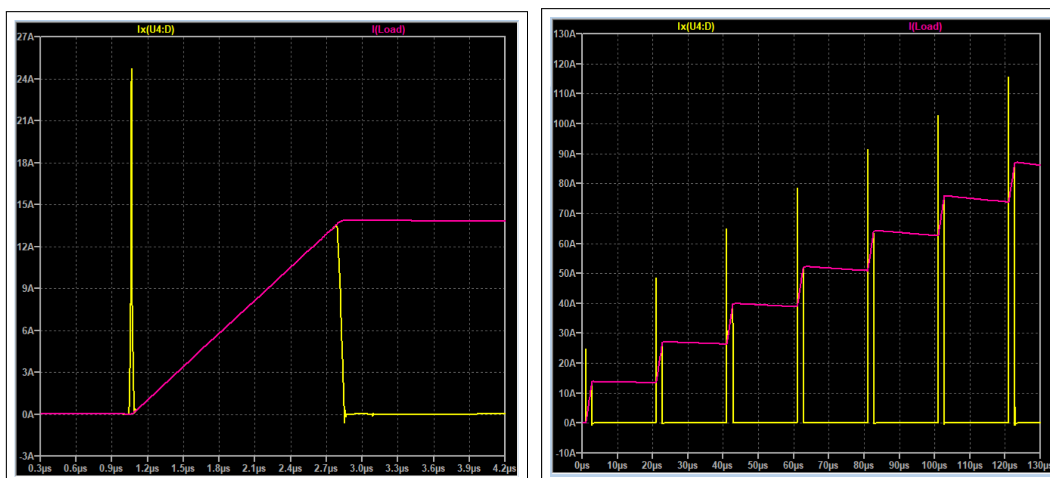


Figure 4.9: *LTSpice simulation. Yellow:* I_{DS} *low-side at gate turn-on. Magenta: load current*

The previous images are taken in correspondence of the first PWM pulse, all referred to the low-side. For what concerns the V_{GS}, the Miller plateau can be noticed at the rising edge when the gate voltage drops for a while, due to the Miller effect at the V_{DS} falling edge. The V_{DS} exhibits some oscillation at the end of the falling edge due to resonance with the parasitic inductances of the source terminal included in the model. The rising and falling edge are very steep: 6 ns for the falling time and 31 ns for the rising time, measured from 10% to 90% of V_{DS}. To be noticed is the fact that this first simulation does not takes into account the parasitic inductances of the transistor leads and PCB traces that could be of the order of several nanohenries and have a strong impact on overshoots and ringings.
The last waveforms are the load and transistor current: with this load configuration there is a current overshoot on the transistor turn-on that reaches a maximum of 40 A in successive commutations. The slope of the load current is around 8 A/µs.

PCB traces and leads inductance effect

A next simulation has been performed introducing some stray inductance on the transistor terminals to simulate the effect of the leads and PCB traces: as a rule of thumb it has been considered 10 nH/cm and a total of 20 nH have been added to each terminal taking into account a possible path length of 1 cm for the leads length and for the PCB traces. In figure 4.10 is depicted the simulation circuit with the added inductances (the two 1 pH inductances have been added due to convercency problems). The measurements are shown in the next images. Evident ringings around 34 MHz can be observed at the gate voltages, that raises above 16 V and below −4 V, still a safe value for the transistor which has a maximum dynamic V_{GS} swing allowed of 19/−8 V. More important and severe are the oscillations at the V_{DS} that reaches more than 1500 V, far beyond the maximum voltage allowable for this transistor.
The oscillation of the I_{DS} are relevant as well, the maximum peak current is increased and the ringing lasts for more than half a microsecond.

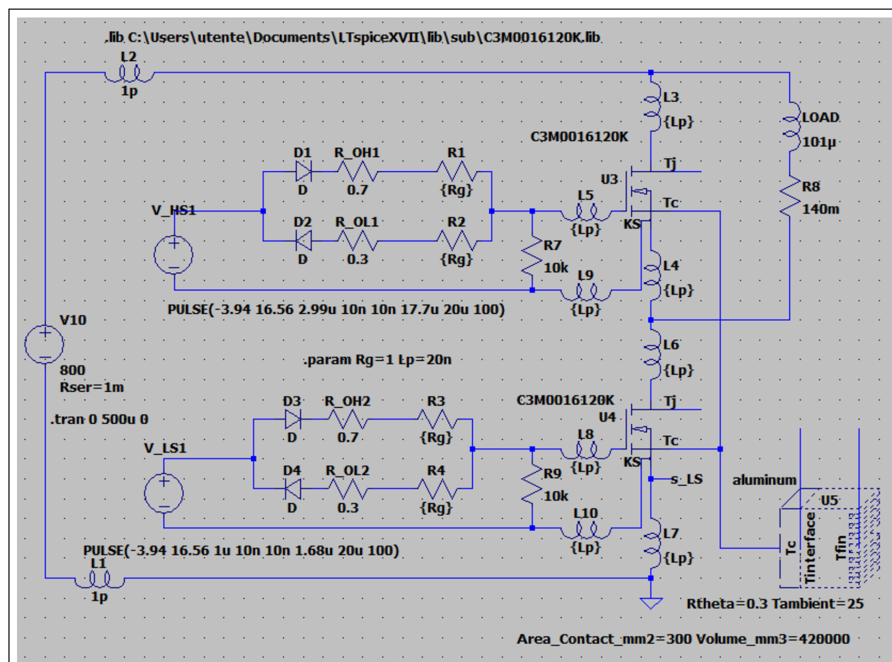


Figure 4.10: *LTSpice simulation circuit*

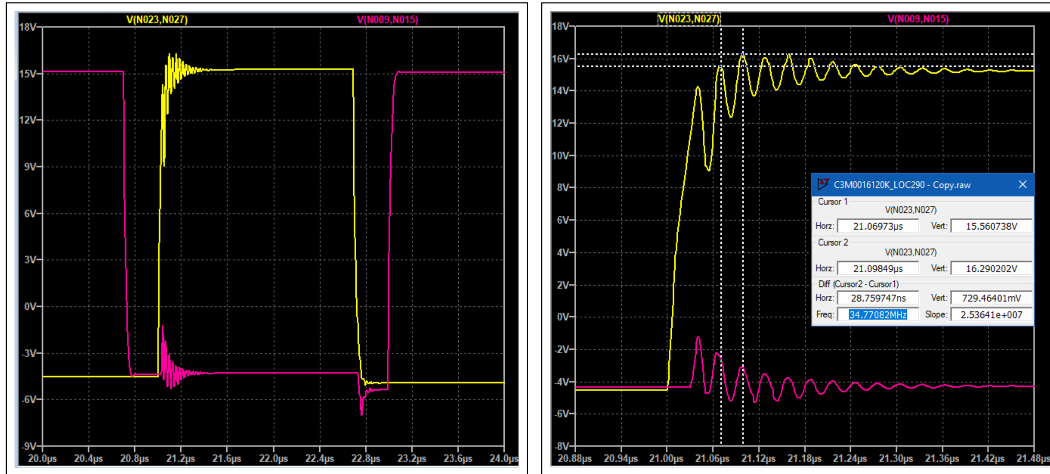


Figure 4.11: *LTSpice simulation. Yellow:* V_{GS} *low-side. Magenta:* V_{GS} *high-side.*

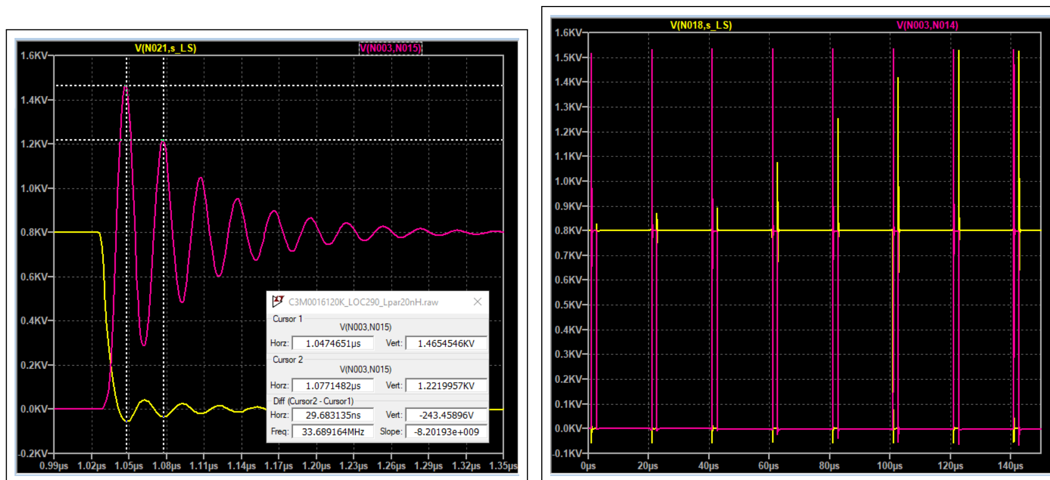


Figure 4.12: *LTSpice simulation. Yellow:* V_{DS} *low-side. Magenta:* V_{DS} *high-side.*

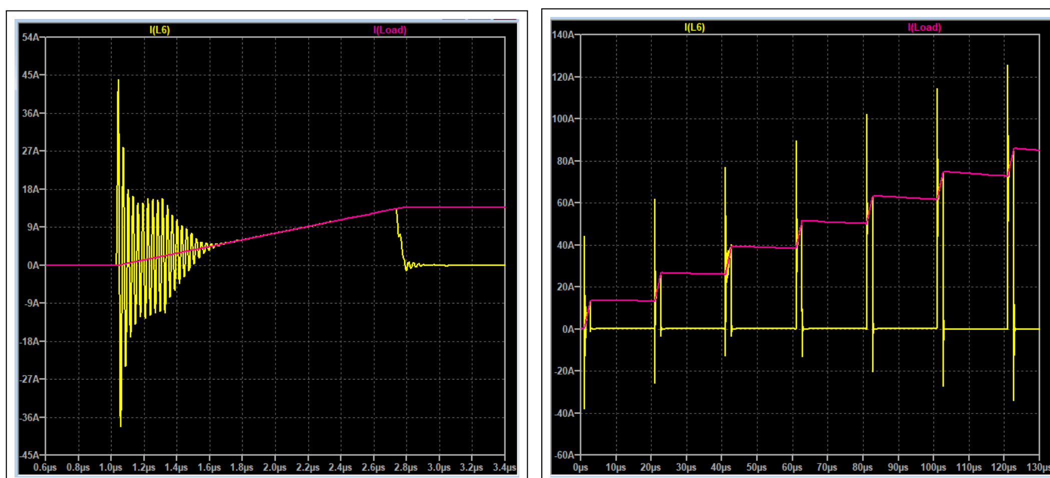


Figure 4.13: *LTSpice simulation. Yellow:* I_{DS} *low-side at gate turn-on. Magenta: load current*

Snubber simulation

To suppress the ringing effect it has been added a snubber in parallel to each transistor. Among the large variety of snubbers existing in literature, some of them described in section 3.8, the R-C topology has been chosen due to its simplicity. The procedure described in [18] has been followed.
To design a snubber, the parasitic inductance of the power loop must be known; in this case it corresponds to the $4 \times 20\,\mathrm{nH}$ added to each source and drain terminal, plus the parasitic inductance of the MOSFET model, which are equal to 4.377 nH for the drain and 2.658 nH for the power source, for a total inductance of 93.484 nH. At this point, taking the resonance frequency of 33.7 MHz obtained from the previous simulation, the loop capacitance, that corresponds to the output MOSFET capacitance C_{oss}, can be obtained by:

$$C_{oss} = \frac{1}{L_{par}(2\pi f)^2} = 238.599\,\mathrm{pF}$$

This value is in accordance to the datasheet value of 230 pF. Now the resistor can be sized by selecting the desired damping factor ζ, as shown in figure 4.14. In this calculation, $\zeta = 1$ has been decided. At this point the resistor value is obtained as follows:

$$R_s = \frac{1}{2\zeta}\sqrt{\frac{L_{par}}{C_{oss}}} = 9.9\,\Omega \rightarrow 10\,\Omega$$

The cut-off frequency of the snubber must be low enough to effectively short-circuit the oscillation frequency f, but not so low to present a significant conduction path at the operating frequency of the circuit (50 kHz in this case). A starting point has been chosen at the resonance frequency as the cutoff. In the end, the capacitor value is obtained with:

$$C_s = \frac{1}{2\pi R_s f} = 477.198\,\mathrm{pF} \rightarrow 470\,\mathrm{pF}$$

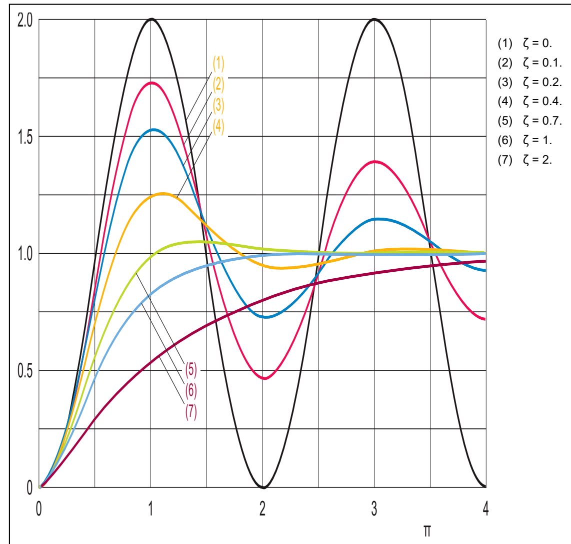


Figure 4.14: *Step response of an RLC circuit for various values of ζ*

The R-C snubber has been added to the circuit as shown in figure 4.15, taking into account that it will be connected physically after the transistor terminals, therefore the parasitic inductances will remain inside the snubber loop. Then the simulation of the circuit with snubbers will be compared to the previous one to verify the improvements in figure 4.16. This simulation has been done with DPT to evaluate the ringings at a current regime condition.

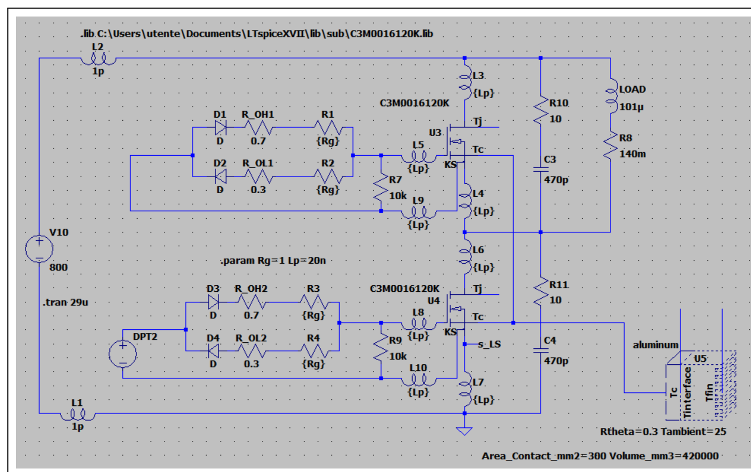


Figure 4.15: *LTSpice simulation circuit with R-C snubbers*

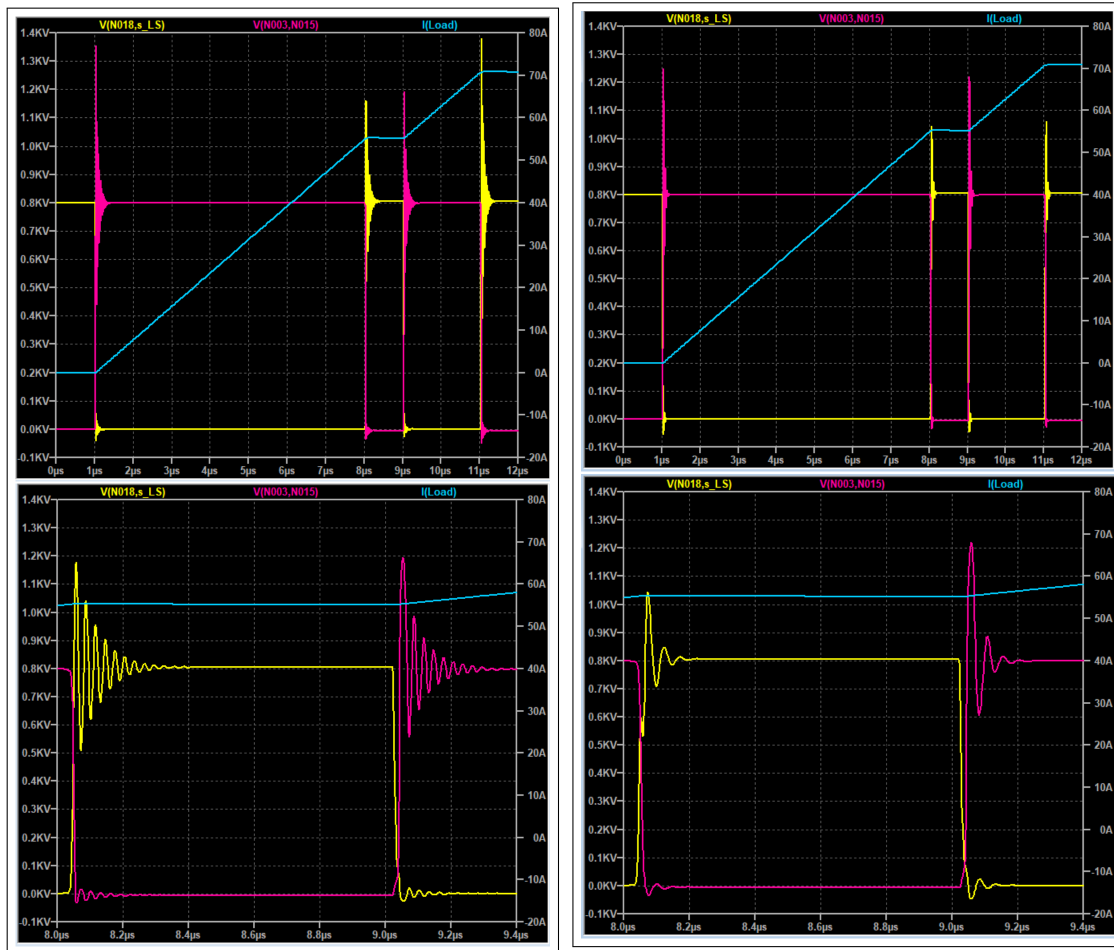


Figure 4.16: *LTSpice simulation without snubber (left column) and with snubbers (right column). Yellow: V_{DS} low-side. Magenta: V_{DS} high-side. Blue: load current.*

The snubbers help to reduce the ringings and the overvoltage, but not as expected. one of the cause might be the fact that the parasitic inductances are still inside the snubber loop and their effect is reduced.

The simulation on the right side (figure 4.17) shows the power consumption of the snubber resistor (low-side) R_s for the current snubber configuration. The two peaks are in correspondence of the rising and falling edge of the second DPT pulse. Since they are 2 µs apart, averaging on a 20 µs window interval it can be obtained the average power for an equivalent PWM pulse at 50 kHz with duty cycle 10%, obtaining a value around 9.5 W.

Next, in figure 4.18 a sweep analysis among different R_s and C_s values are reported to evaluate the damping effect and power consumption for different resistance and capacitance values.

The plots show that increasing the resistance or the capacitance value, the damping effect is more effective, but the power dissipation increases dramatically. Moreover, a large capacitance slows down the dv/dt, degrading the advantages of the SiC transistor.

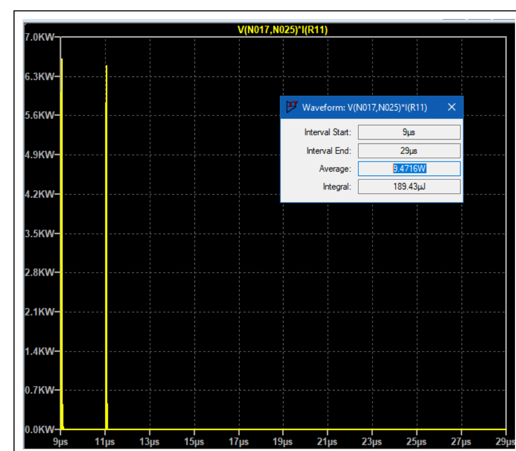


Figure 4.17: *Average power dissipated by the snubber resistor ($R_s = 10\,\Omega, C_s = 470\,\text{pF}$)*

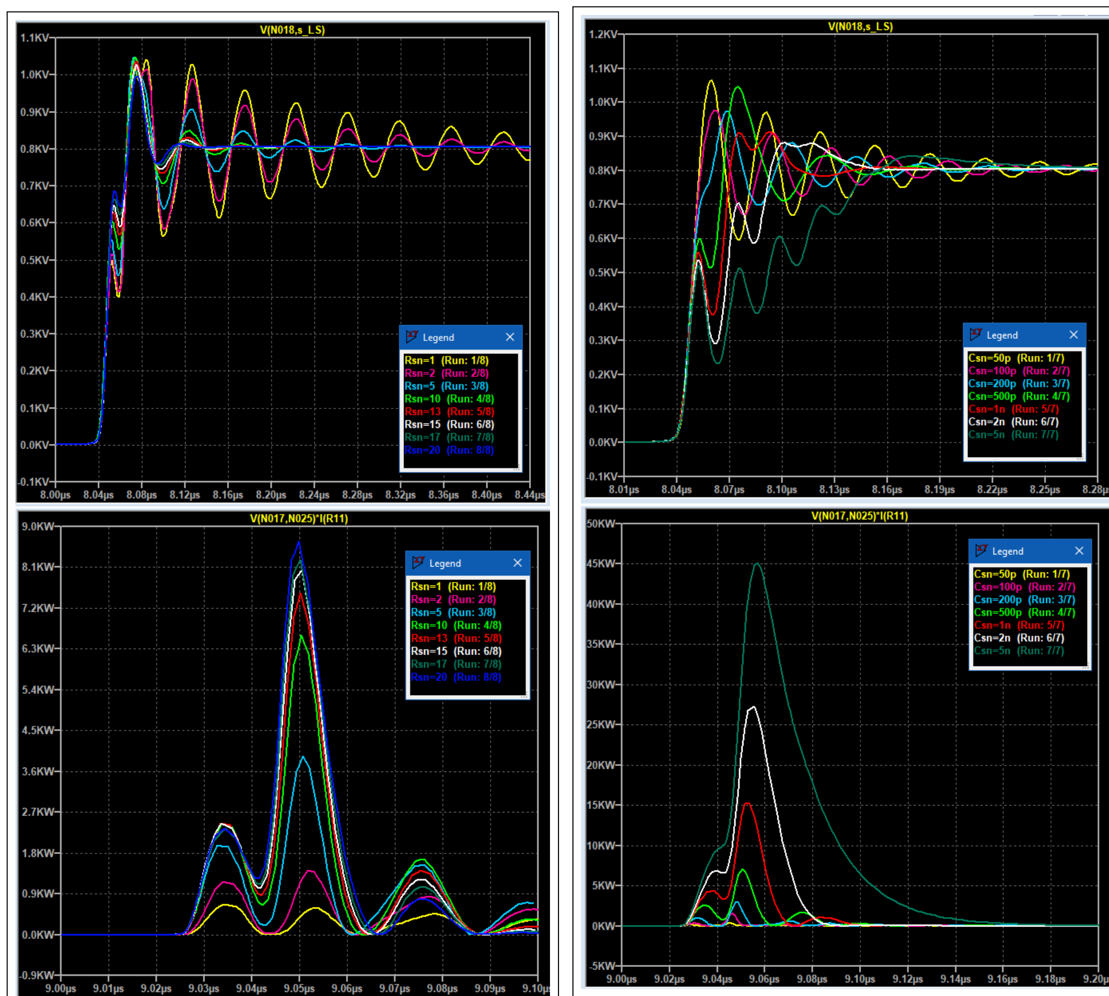


Figure 4.18: *LTSpice sweep simulation of R_s (left column, $C_s = 470\,\text{pF}$) and C_s values (right column, $R_s = 10\,\Omega$). Top row: V_{DS} low side rising edge. Bottom row: R_s power dissipation in correspondence of the second DPT pulse rising edge (low-side turn-on)*

Since the parasitic elements are unknown until the effective realization and testing of the board, the prototype has been tested without snubber at first, and then with measured data, a snubber has been designed.

4.4 Function Block Diagram

In figure 4.19 the block scheme is reported. On the right the two drivers ICs (UCC21710-Q1) powered by their own isolated DC-DC converters (R12P21503D), driving the transistor terminals, besides the current monitoring and control circuit comprising the desaturation and shunt current sensing circuit and the isolated amplifier (SI8920BC-IP). Moving to the top-left corner, the DC bus voltage monitoring system can be found, made by the voltage divider, the isolated amplifier (ACPL-C870) and its own DC-DC converter (ADuM6028). These blocks sends the isolated digital (CTRL) and analog signals (ADC±) to the microcontroller, and this sends the PWM signals to the driver ICs through the buffer. The logic side is powered by the 5 V DC-DC regulator TSR1-2450.

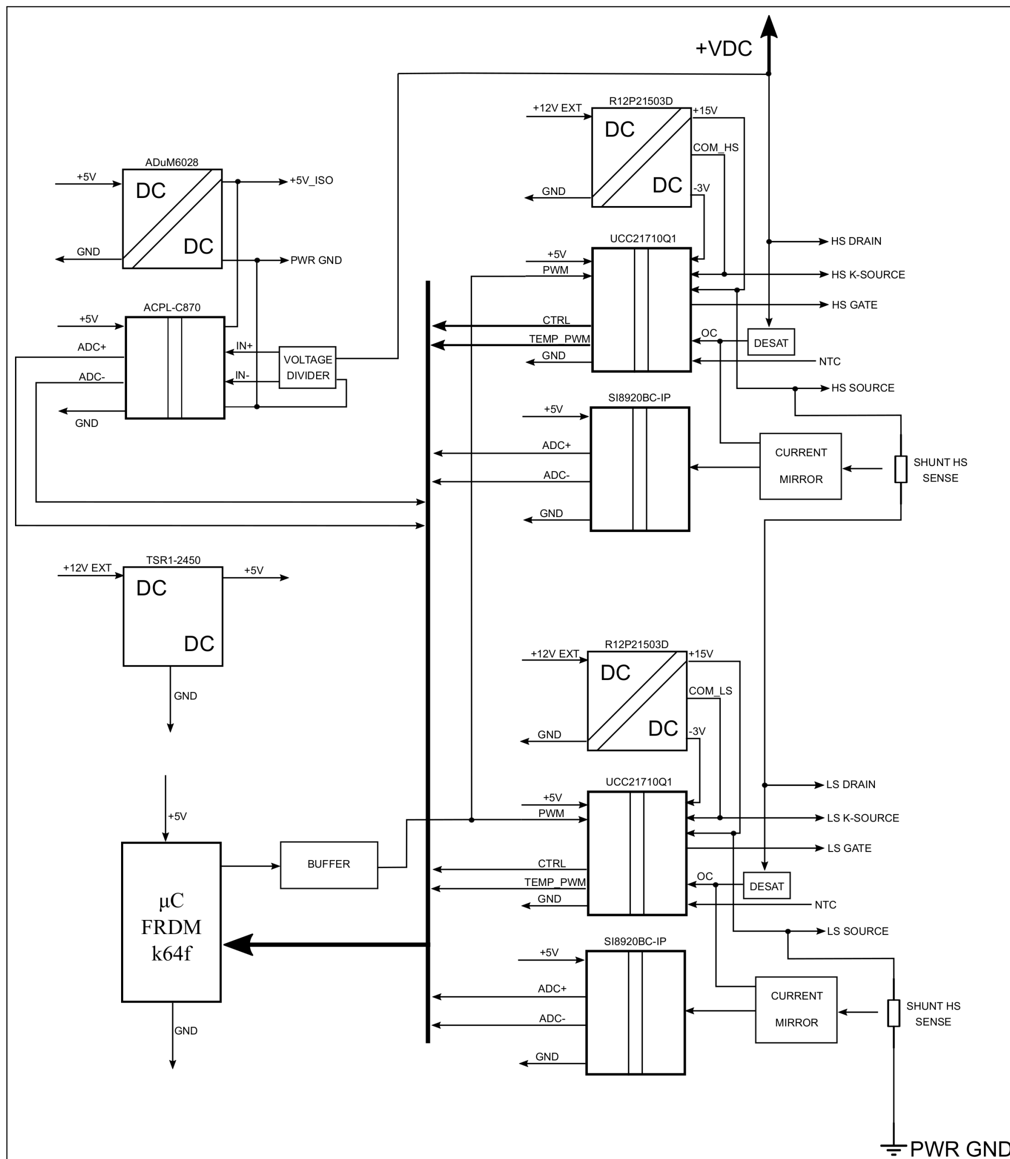


Figure 4.19: *Function Block Diagram*

4.5 Components selection and schematic

The whole circuit has been designed on the basis of the core components, the SiC transistor and the gate driver IC. In the following sections, the building blocks of the gate driver are described.

4.5.1 Power supplies

The board takes as input power supply a 12 V DC from an external bench power supply and then regulated through the TSR 1-2450 to 5 V, 1 A output, to supply the following components:

- microcontroller board FRDM-K64F (110 mA);
- buffer IC (30 mA);
- DC bus voltage sensing circuit (an isolated DC-DC plus an isolated amplifier, 190 mA + 15 mA);
- the two gate driver ICs (61× 2 mA);
- two isolated amplifiers for current sensing (5.5× 2 mA);

Figure 4.20: *TSR 1-24XX DC-DC converter*

for a maximum total current demand of 478 mA. A 4.7 µF capacitor has been used at the input and output of the regulator.
The two drivers need also an isolated asymmetric supply voltage to drive the gates (a positive VDD, a negative VEE). The R12P21503D is a 2 W isolated DC/DC converted that supplies a 15/−3 V output with a 12 V input, specific for IGBTs and SiC MOSFETs. It has a 6.4 kVDC isolation barrier and a maximum capacitance of 10 pF. Each driver has its own R12P21503D DC-DC converter. To calculate the necessary input and output capacitance, it has been proceeded as suggested in the application note [20] from MuRata: given the gate charge $Q_G = 211$ nC and the supply voltage swing $V_S = VDD - VEE$, in this case 18 V, it is calculated the gate driver energy E added and removed per cycle

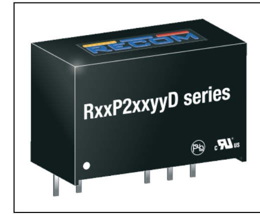


Figure 4.21: *RXXP2XXYYD DC-DC converter*

$$E = Q_G \times V_S = 3.796\,\mu J$$

of which $E_{VDD} = 3.163\,\mu J$ due to the positive VDD, and $E_{VEE} = 0.363\,\mu J$ due to the negative VEE, making simply the proportion. The energy is also proportional to the square of the capacitor voltage $E = \frac{1}{2}CV^2$ and assuming a maximum voltage drop of 5% during the switchings, it can be found the minimum capacitance needed at the voltage regulator output by reversing the formula:

$$E = \frac{1}{2}C(V_{init}^2 - V_{final}^2) = \frac{1}{2}C\left(V_{init}^2 - (0.05 \times V_{init})^2\right)$$

The result is a minimum capacitance of 28.18 nF for VDD and 3.23 nF for VEE. As a conservative choice, a 4.7 µF capacitor has been used for both the outputs, placed as close as possible to the output pins.

4.5.2 Current sensing and protection

The current sensing has been made through a shunt resistor in series to each source terminal of the transistors. Due to the high current rating of the transistor, a low resistance value must be chosen in order to avoid power dissipation and consistent voltage drop across the shunt. The shunt resistor used in this circuit is the CSS2H-5930R-L500F, a 500 µΩ, 8 W shunt with temperature coefficient of 100 ppm/°C and a parasitic inductance lower than 3 nH. To calculate the power dissipation, a maximum duty cycle of 50% and current of 150 A has been assumed, obtaining:

$$P_{max} = (R_{shunt} \times I_{DS}{}^2)/dc = 5.625\,\mathrm{W}$$

The voltage of the shunt resistor is then sensed by the SI8920BC-IP, an amplifier for shunt measurements with differential input and output and fixed gain of 8.1 and then sampled by the microcontroller ADC. The maximum input range of this IC is 200 mV, therefore it is necessary to match the output voltage of the shunt resistor. The short circuit threshold has been fixed to 150 A corresponding to a shunt voltage of 75 mV. To match this voltage range to the full scale input range of the amplifier, a mirror current circuit has been used as shown in picture 4.23: this solution has been taken by a reference design of a gate driver from Texas Instruments [19], using the same driver IC family of this project. This circuit performs a negative current detection, suggested for power switches with split source (kelvin source). The KS terminal is connected to the COM of the driver IC, and the sensing input of the circuit (node IN) is connected to the power ground. at the overcurrent detection, the voltage divider made by R47 and R63 ensures a voltage of 200 mV at the input of the amplifier, that provides a differential output voltage from 0 to 1.62 V to the microcontroller, and 0.7 V at the node OC, that is connected directly to the driver overcurrent sensing input. The isolated amplifier needs two separated 5 V supply voltages: for the isolated side, a 5.1 V zener diode has been used to obtain the right voltage from the VDD provided by the R12P21503D, while the low voltage side is supplied by the 5 V regulated by the TSR 1-2450. In conclusion, this circuit performs a current sensing.

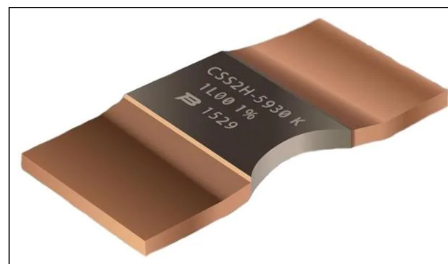


Figure 4.22: *CSS2H-5930R-L500F shunt resistor*

In the same reference design, all the calculation needed to determine the value of the resistors can be found.

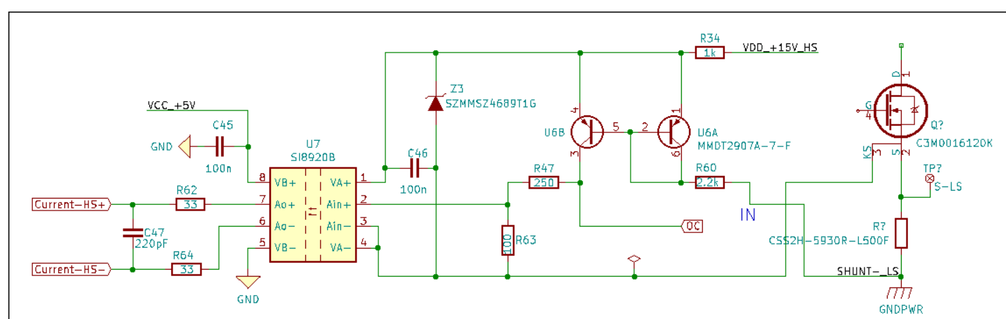


Figure 4.23: *Current sense and protection circuit*

The desaturation method has been also implemented. By looking at the output characteristic of the transistor datasheet (figure 4.24), first has been set the V_{DS} at which a drain current of 150 A corresponds: for a V_{GS} of 15 V, the desired voltage is slightly below 3 V (red line).

The resistor and capacitor network has been calculated through the calculator tool [17] provided by Texas Instrument with the Gate driver IC documentation: by selecting as input the resistor values, capacitor value and diode forward voltage, the blanking time and the desaturation voltage can be obtained. The diode used is the US1MFA fast recovery diode, with breakdown voltage of 1 kV, current rating of 1 A. For this circuit the calculated values shown in figure 4.25 lead to a desaturation voltage of 2.90 V and a blanking time of 325 ns. This last value has been chosen on the basis of the response time of the overcurrent detection declared on the datasheet of 270 ns, so in total the theoretical intervention time is around 600 ns, not too short to trigger false faults and not too long to delay the protection.

The protection method is selectable by soldering the central pad of jumper JP2 with one of the adjacent pad for desaturation or shunt based protection, as shown in figure 4.25; the two methods cannot be implemented at the same time.

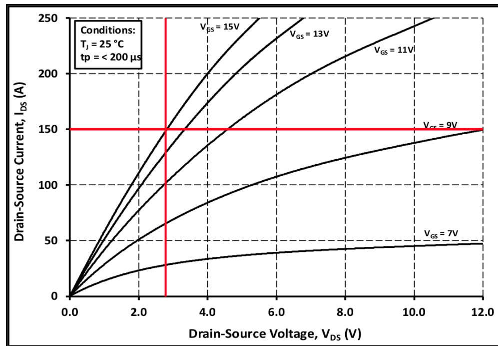


Figure 4.24: *Output characteristic of the C3M0016120K*

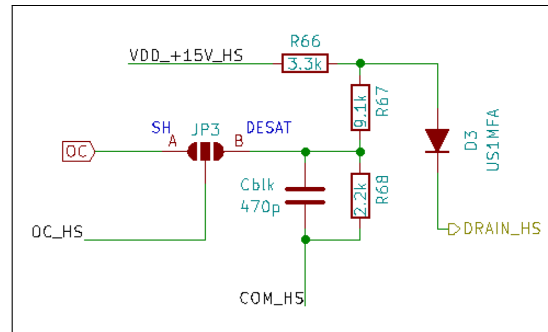
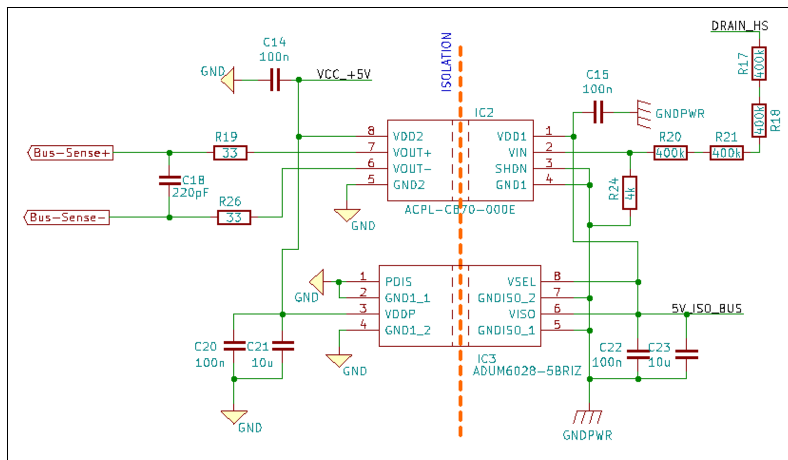


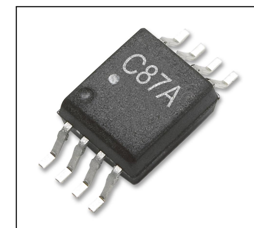
Figure 4.25: *Desaturation circuit*

4.5.3 DC voltage sensing

The DC voltage measurement is obtained through a voltage divider with resistor ratio 4/1600 to let correspond the 800 V DC to a 2 V, and sensing the voltage with the optically isolated voltage sensor ACPL-C870, that has a 2 V input range and unitary gain. The output is then sampled by the microcontroller.
The voltage sensing circuit needs a 5 V reference with respect to the bus DC power ground and, since the low side driver reference node is connected to the kelvin source of the MOSFET, a separate voltage is required. The ADuM6028 is an isolated DC-DC converter which takes 5 V supply input (regulated by the TSR 1-2450) and provides a 5 V output supply voltage referred to another ground, in this case the power ground.



(a) *DC voltage sensing circuit*



(b) *ACPL-C870*

(c) *ADuM6028*

4.5.4 Temperature sensing

The analog sensing pin of the driver IC has been exploited for temperature sensing. The solution adopted is the one suggested into the driver datasheet, using the 4.7 kΩ NTC thermistor NTCS0805E3472FMT in series with a 3 kΩ resistor. The sensed voltage from the AIN pin is passed through the isolation barrier to the input side and transformed to a 400 kHz PWM signal. A capacitor in parallel to the AIN pin is suggested, with cutoff frequency below the PWM frequency. Temperature is not a rapidly varying quantity; a 47 nF capacitor is therefore sufficient.
The duty cycle of the PWM changes linearly from 10% to 88% when the AIN voltage changes from 4.5 V to 0.6 V and can be represented using the following equation:

$$dc_{APWM}(\%) = -20V_{AIN} \times 100$$

The sensed voltage of the NTC thermistor connected in series with the 3 kΩ resistor ranges from about 1.5 V to 0.6 V from 25 °C to 135 °C, corresponding to 70% to 88% duty cycle.
All the ADC samplings are taken in correspondence of the centre of each PWM pulse, in order to be in the furthest point between each commutation and avoid noise.

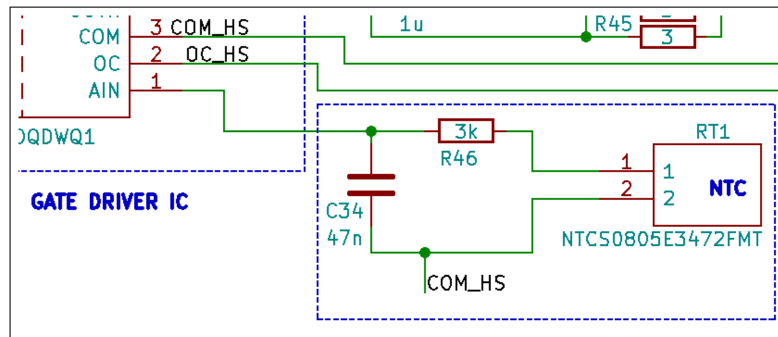


Figure 4.27: *Temperature sensing circuit.*

4.5.5 Snubbers

The choice of the resistor and capacitor for the RC snubber has been made on the basis of the theoretical calculation of the previous section, therefore a 470 pF, 1 kV capacitor in a 0805 case, and a 10 Ω, 1.5 W resistor in a 2512 case. Since the prototype has not been tested for a continuous use, the power rating can be decreased, reducing the footprint and being able to make the snubber path as much compact as possible.
As explained in the previous section, this snubber value is just the result of an estimation of the parasitic inductances, and the circuit has been tested first without snubber.

4.5.6 DC capacitor bank and power supply

The DC link capacitor must ensure a stable constant voltage value at every cycle, and have low ESR and ESL parameters. To size the capacitance needed, reference has been made to [21]. First it has been calculated the maximum ripple current of the capacitor in the worst case condition, that is a 50% duty cycle PWM at the working frequency of 50 kHz:

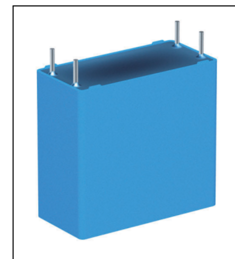


Figure 4.28: *B32778Z0406K000 DC link capacitor*

$$\Delta I_{50\%} = \frac{V_{BUS}}{4fL_{LOAD}} = \frac{800}{4 \times 50 \times 10^3 \times 100 \times 10^{-6}} = 40\,A$$

Next, the maximum peak to peak ripple voltage across the bus capacitor is given by:

$$\Delta V_{50\%} = \frac{V_{BUS}}{32L_{LOAD}Cf^2} = \frac{800}{32 \times C \times (50 \times 10^3)^2 \times 100 \times 10^{-6}}$$

For a 1% maximum voltage drop, a 12.5 µF capacitance is necessary. For a conservative choice a 100 µF total capacitance has been chosen, obtaining a maximum voltage drop of 1 V.
The capacitor use for this application is the B32778Z0406K000, a 1000 V, 40 µF capacitor, with ESR of 6.2 mΩ, ESL of 15 nH and maximum RMS current of 21.5 A. A total of 3 parallel capacitors are used to reach the desired and to reduce the series parasitics.
To generate the DC voltage, the system shown in figure 4.29 made of a voltage varistor and a high voltage transformer has been used. The former takes as input the 230 Vac line voltage and provide a 0÷230 Vac. Successively this voltage is transformed to a 0÷2500 Vac by the second transformer and rectified in the end by a full bridge rectifier and a filter output capacitor. The voltage can be regulated by rotating the potentiometer of the variac.

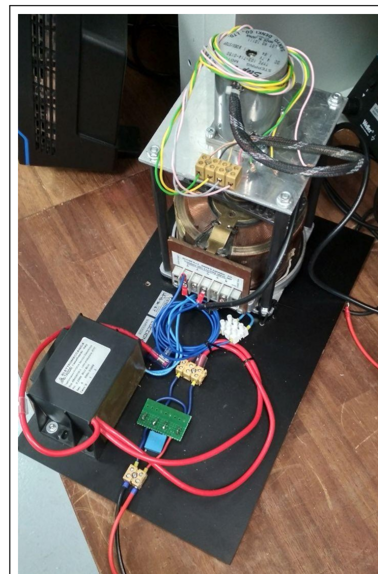


Figure 4.29: *DC power supply*

4.5.7 Microcontroller board and firmware development

The microcontroller board used for this application is the FRDM-K64F from NXP, chosen for its availability of a FlexTimer module oriented to the PWM management for motor control and power conversion, which includes duty cycle and hardware deadtime insertion, polarity, fault control, output forcing and masking, complementary output enable and more.
The board generates the two PWM pulses in complementary mode from the same 60 MHz timer module on two output channels, and provides a reset signals to restart the drivers from a fault condition or simply to restart the pulse pattern for a new test. Besides, the board acquires the two current measurements from the shunts resistors and the bus voltage measurement through three differential input ADCs, and the fault flags from the drivers.

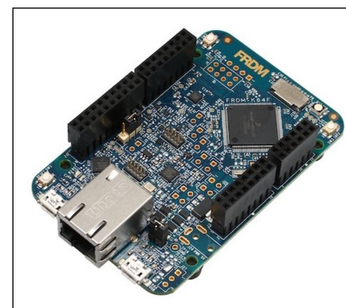


Figure 4.30: *FRDM-K64F developmend board*

The four output signals of the board are sent to the SN74ABT125D quadruple bus buffer with 3-state outputs, that shifts the high logic level from 3.3 V to 5 V guarantee a robust command signal with up to 20 mA output current.
The firmware has been developed in C language and follows the flowchart in figure 4.31.
At the turn on, the program initialize the peripherals and the board pin to be used, set the PWM configuration for complementary outputs, dead time insertion and fault control enable, send the enable signal to the drivers and turns on the gren LED. All the settings about physical pin to enable, clock frequency, PWM duty cycle, type of PWM and so on can be set directly through the graphical user interface provided by the IDE, and all the functions for these configuration are auto-generated and included in the initialization functions.

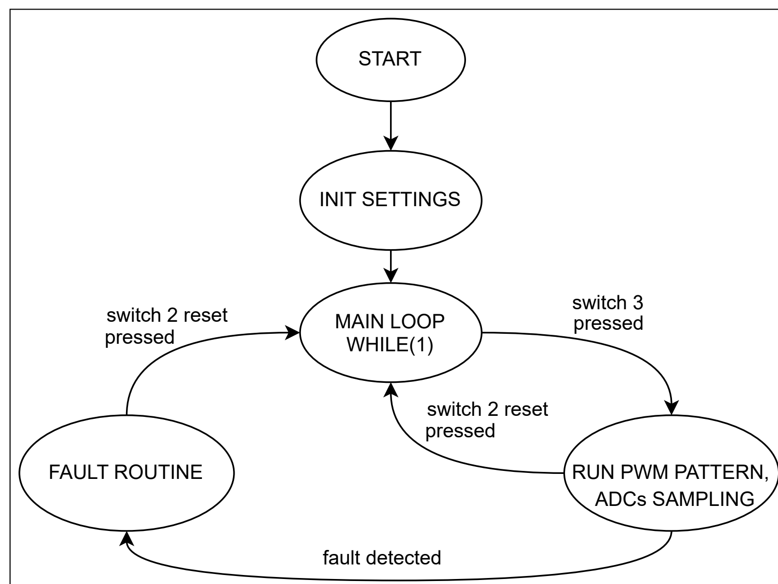


Figure 4.31: *Firmware flowchart.*

The main loop is a while loop where the microprocessor waits for an interrupt, that can come from the switch 3 (SW3) to start sending the PWM pulses, or the switch 2 (SW2) to reset the flow.
If SW3 is pressed the PWM pattern is started, and it can be:

- finite number of complementary pulses at 50 kHz, duty cycle 10%, dead time 300 ns;
- double pulse test on the low-side with first pulse of 4 µs, pause for 1 µs, second pulse for 2 µs, while the high-side gate pulse is masked, keeping the gate voltage low.

At the end of the pulses, if no faults have been detected, the routine stops and turns on the blue LED, waiting for the reset signal from the SW2 to reset the PWM counter and return to the main loop with the green LED on. If a fault is detected, the program stops the PWM pulses and forces both the output at low level, indicating the fault with the red LED on. The program is reset by the SW2.

4.6 Schematic, layout and board

In this section, the schematic and the 3D model of the board realized with KiCad are shown.

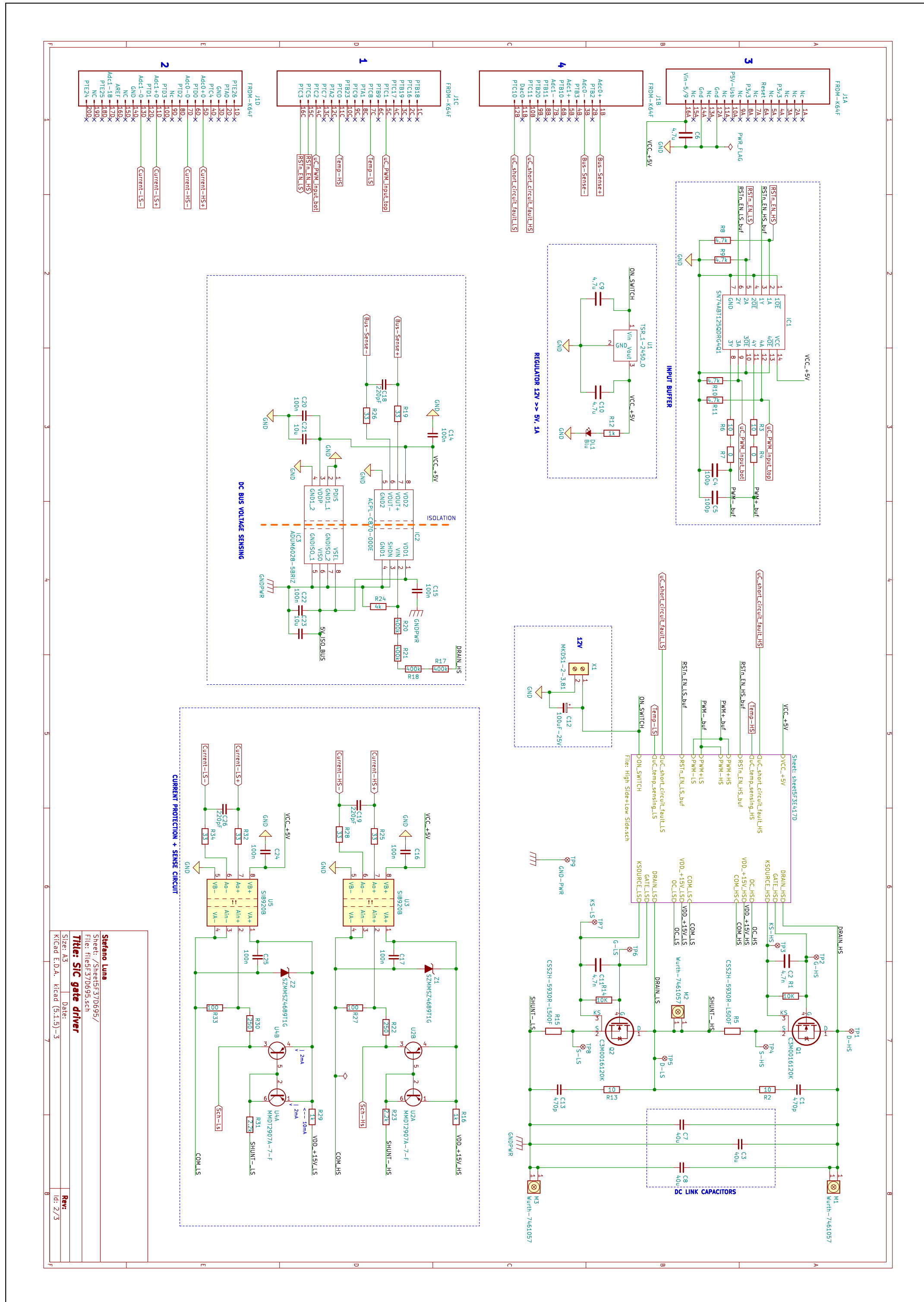


Figure 4.32: *Schematic: microcontroller and input buffer, DC voltage and current sensing, SiC half bridge.*

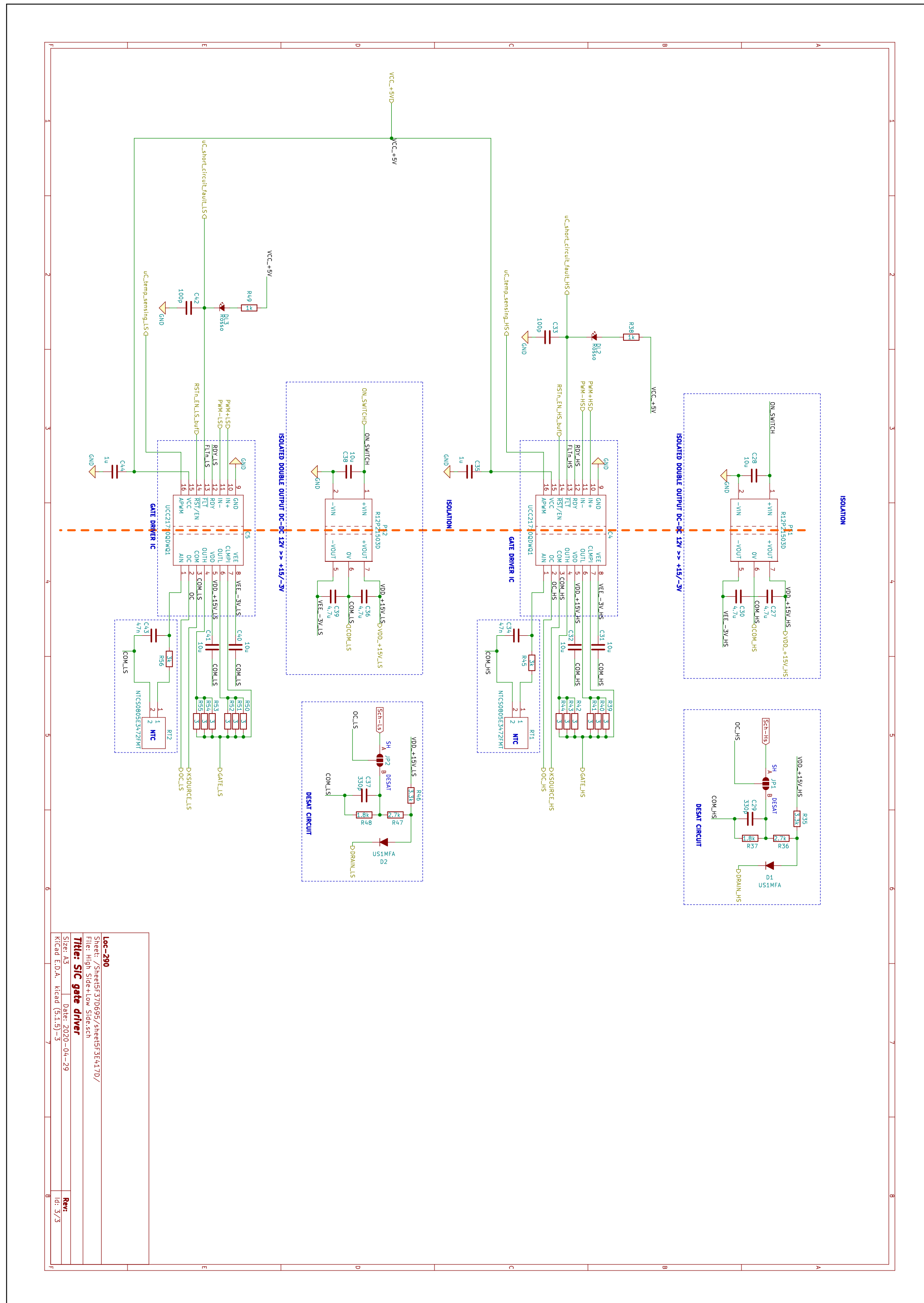


Figure 4.33: *Schematic: gate driver ICs.*

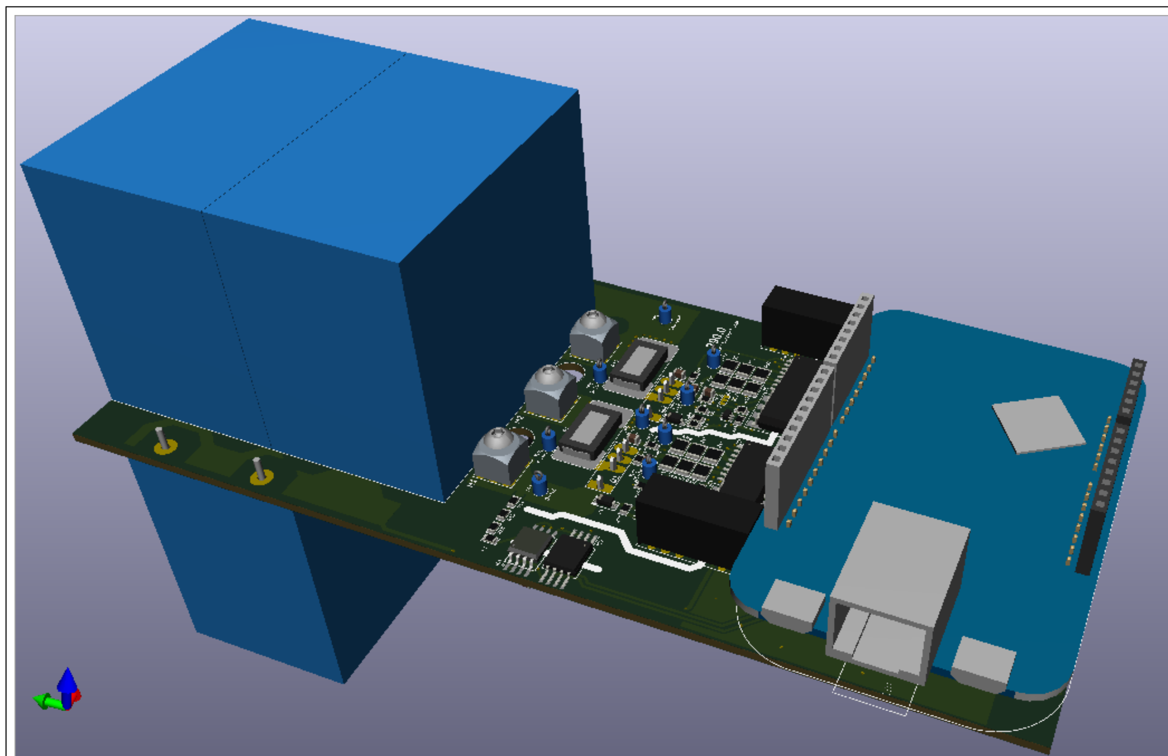


Figure 4.34: *Top view of the 3D rendering*

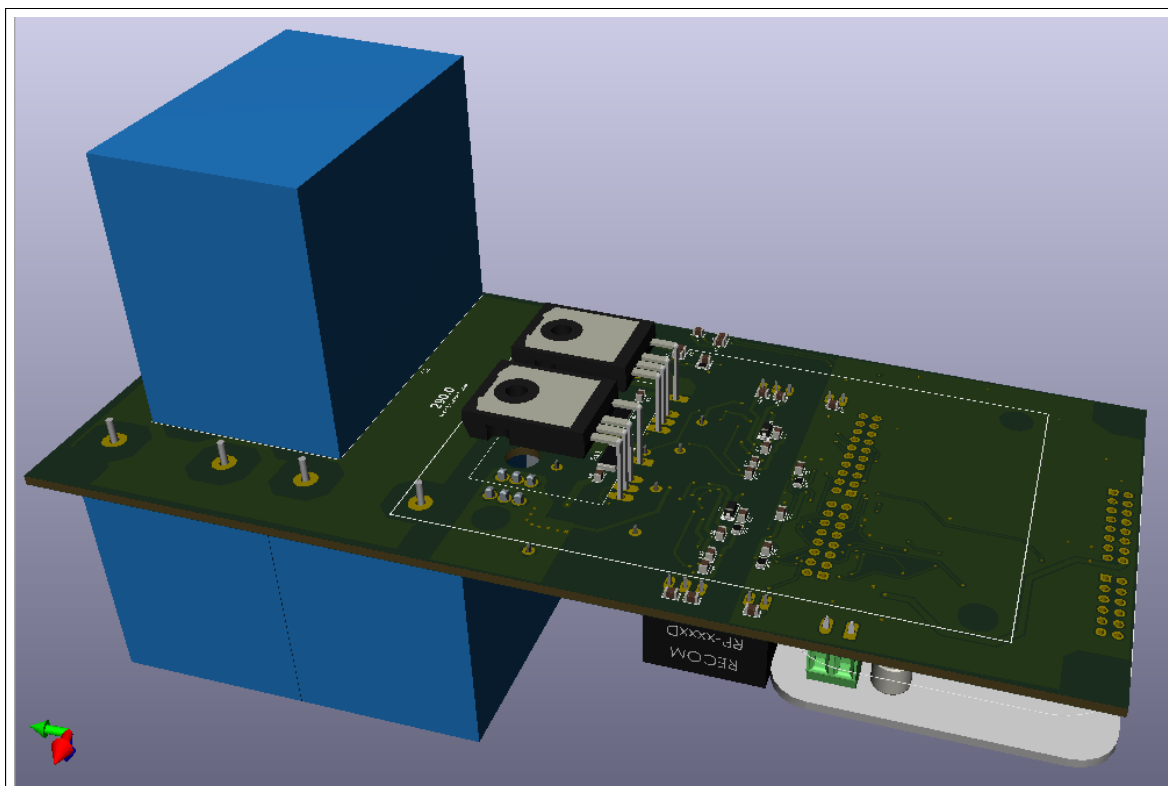


Figure 4.35: *Bottom view of the 3D rendering (heat sink not included.)*

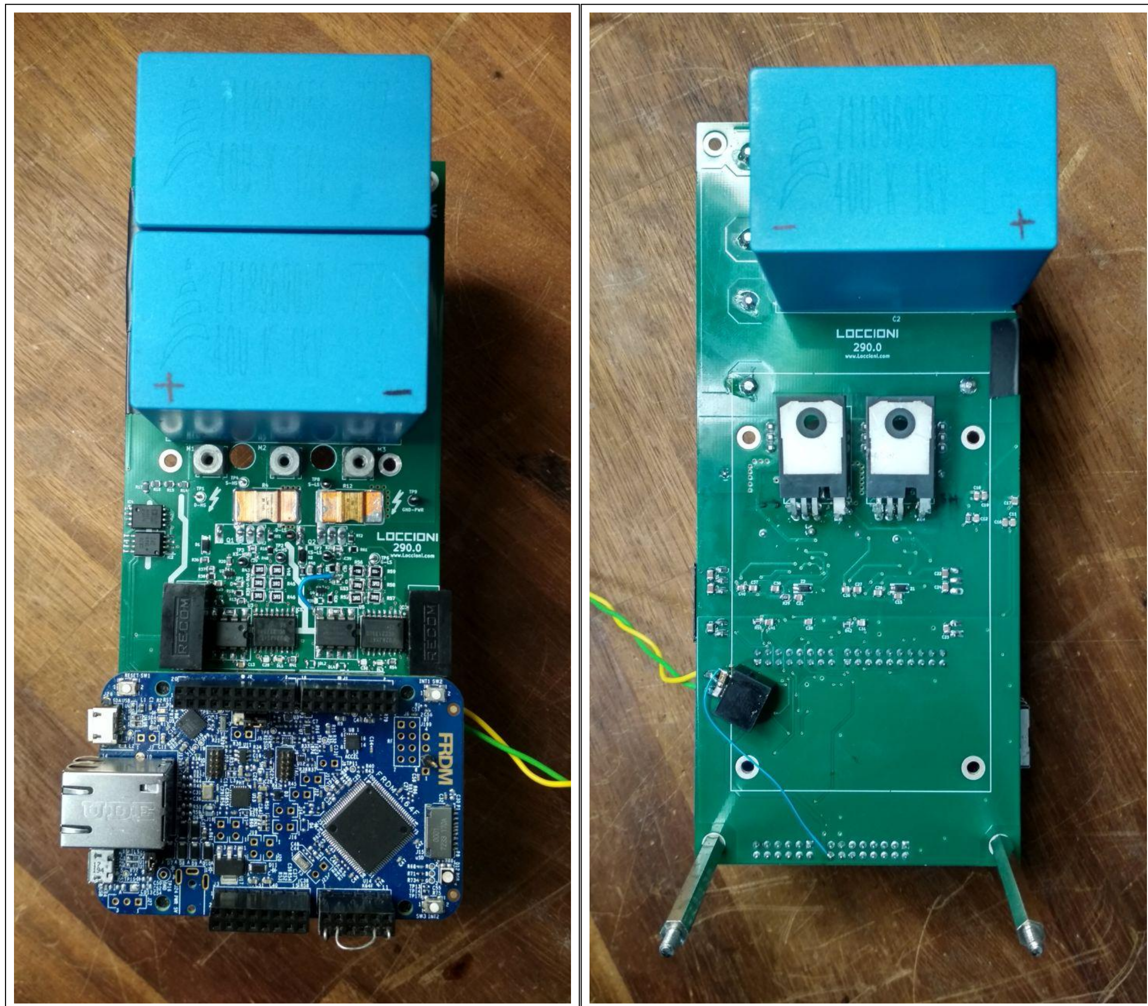


Figure 4.36: *Left: top view of the board. Right: bottom view of the board (heat sink removed). PCB size:*

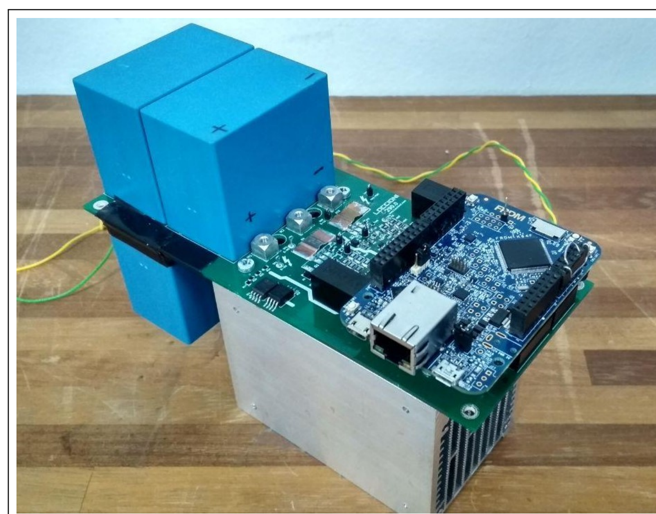


Figure 4.37: *Gate driver board.*

Chapter 5

Prototype Testing and results

5.1 Instrumentation

In this section, the laboratory equipment used for this project is described in the following list:

- Bench Power Supply EX1810R, mixed mode regulated, adjustable, 1 output, 0 V 18 V, 0 A 10 A;
- Digital Multimeter Fluke 87-IV, 1000 Vac, 10 A ac, CAT III, true RMS;
- Teledyne LeCroy WAVESURFER 3024, 200 MHz, 4-channel, 4 GS/s, Digital storage Oscilloscope;
- Passive probes PP007-WR-1, 500 MHz, 10 MΩ, 9.5 pF, attenuation 10:1;
- ADP305 LeCroy high-voltage active differential probes, 1000 V RMS common mode, 1400 Vpk, 100 MHz bandwidth;
- CP030A LeCroy high sensitivity current probe, 30 A continuous, 50 A peak, 50 MHz;
- LS50 LEM universal current probe, 30 A continuous, 50 A peak, 50 MHz;
- Agilent 4263B RCL meter 100 Hz to 100 kHz;

5.2 Results

In this section are shown the results obtained from the measurements and testing of the gate driver board. It will be analyzed first the control signal delay that involves the microcontroller-buffer-gate chain, moving successively to an analysis of the circuit behaviour when changing the gate resistance, gate capacitance and when using the snubber or not. In these two last tests, repetitive DSO acquisitions have been collected and processed in a spreadsheet format to be eventually overlapped for a better comparison of the parameters variation effect.
A further analysis has been done monitoring the DC bus voltage during the transistor switchings. Then it has been proceeded to test the short circuit protection by forcing a long enough PWM pulse to reach a current value necessary to trigger the fault.
Next, the circuit has been modified by removing the low-side shunt and soldering a piece of wire across its two soldering pads to allow the transistor current sensing through a current probe.
In the end, the LTSpice simulation has been adjusted in terms of parasitics to obtain a plausible estimation of these circuit parameters.

5.2.1 Driving signals delay

In this section are shown the waveforms of the driving signals from the microcontroller to the gates in the isolated side, at the low-side transistor turn-on. In figure 5.1 from top to bottom are depicted the microcontroller PWM output signal in magenta, the buffer output signal in blue and the V_{GS} low-side in green. The measurement has been taken with RC snubber (10 Ω, 470 pF) and 1 Ω gate resistance. In the second picture a zoom is shown to enhance the delays among these signals: It is remarkable the effect of the buffer that, although it has almost 10 ns delay with respect to the microcontroller signal, reaches the high logic level sligtly before the former, providing a 5 V strong signal.
In the bottom-right corner of the second figure it is possible to read the total delay of around 85 ns measured between the cursors from the beginning of the microcontroller signal to the beginning of the rising edge of the gate voltage. The measurements are coherent with the driver IC propagation delay stated in the datasheet.
The point where the gate voltage starts dropping is the moment in which the V_{DS} starts falling: here some spikes can be seen back to the digital side, probably due to an unwanted probe coupling.

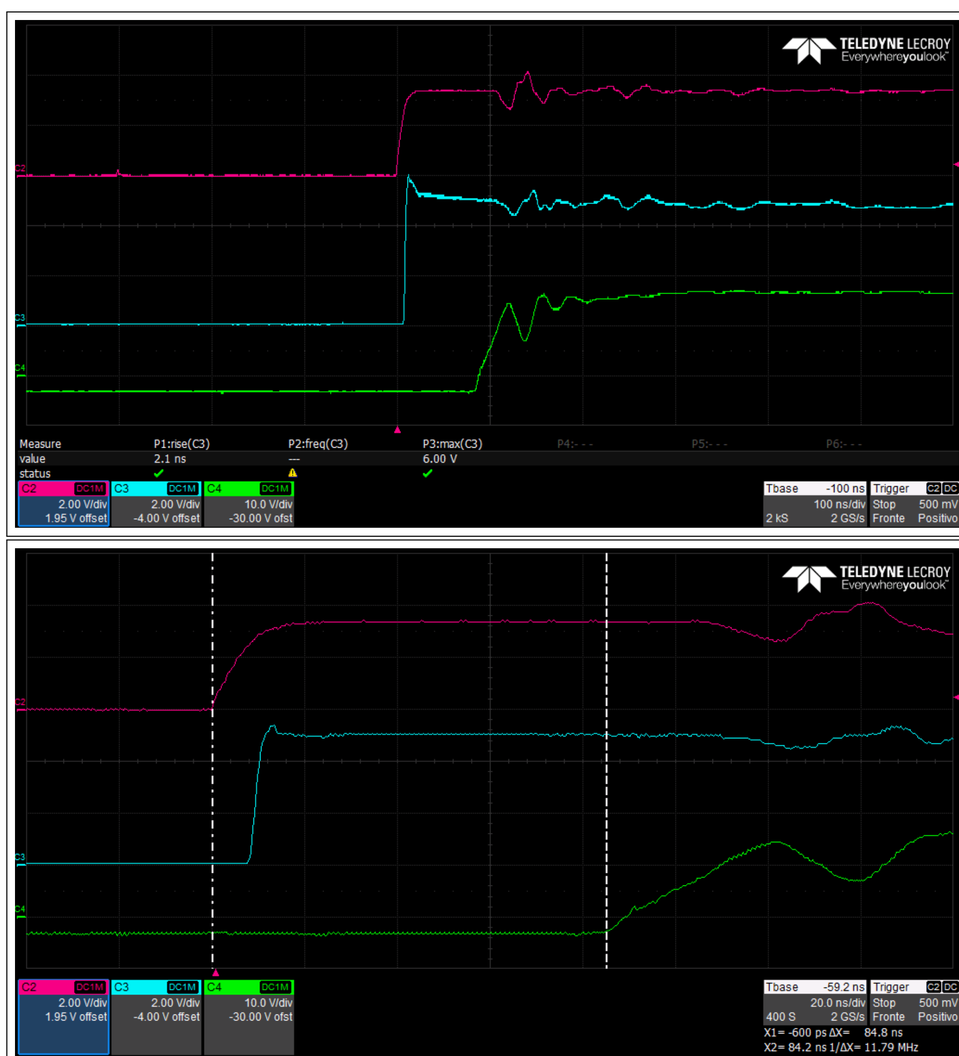


Figure 5.1: *PWM-to-gate signal delay. Magenta: PWM microcontroller output. Blue: buffer output signal. Green:* V_{GS} *low-side signal.*

5.2.2 Effect of gate resistance change

The data represented here show the behaviour of the V_{GS} and V_{DS} low-side at the turn-on and turn-off when changing the gate resistance value among six values: 0, 1, 3, 7, 10 and 15 Ω. The measurement has been taken with RC snubber (10 Ω, 470 pF)
Data have been collected separately for each resistance value through the DSO and then extracted in .csv format to be post-processed as spreadsheet and overlapped with the same voltage and time scale.
The gate resistors used are all SMD 1210 case, power rating 0.5 W and have been measured through the multimeter before the testing, and their value has been rounded to the integer value for a straightforward comparison.
In figures 5.2 and 5.3 are shown respectively the rising edge and falling edge of the V_{GS}: the measurements have been split into two graphs to have a better fit with the time scale, since for resistance values of 0, 1, and 3 the edge is faster and with more ringings and for the other is slower and smoother. In fact, ringings are much more important for lower resistance value and for 0 Ω the gate voltage shows a maximum peak value of almost 20 V during the rising edge, and a negative voltage peak below 5 V, not a safe value to guarantee the transistor reliability. Comparing this curve with the 1 Ω data, it can be seen that this value is yet enough to limit the overshoots with a slight edge slow down. Increasing the resistance, oscillations are almost negligible, but the rise and fall time increases considerably.
One remark has been made when no resistance is used: testings have been made removing all the SMD resistors and shorting with a wire the resistance pads from the driver to the gate. This introduces stray inductance for around 1 cm wire length. With no external gate resistors, the only resistance is the one of the transistor (2.6 Ω from the datasheet) and the output resistance of the driver IC 0.7 and 0.3 Ω respectively for pull-up and pull-down resistance.
Next, in figure 5.4 is shown the V_{DS} low side behaviour. While during the rising edge no remarkable overshoot appeared, the falling edge shows undervoltages up to −150 V out of a 600 VDC bus for the lowest gate resistance value. It is supposed the complementary behaviour for the high-side V_{DS}, so that similar overvoltage entity during the rise time on the basis of the previous LTSpice simulation of figure 4.16.
Here, a value of 3 Ω can be a right compromise to suppress the ringings keeping a good falling time.
In general, the rising time is more affected by the gate resistance increase than the falling time.

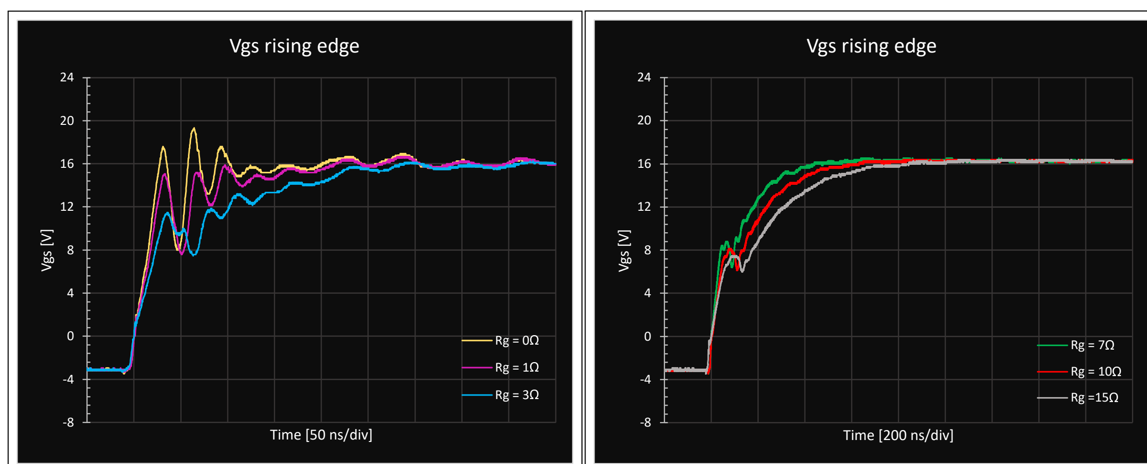


Figure 5.2: V_{GS} *rising edge for different gate resistance value.*

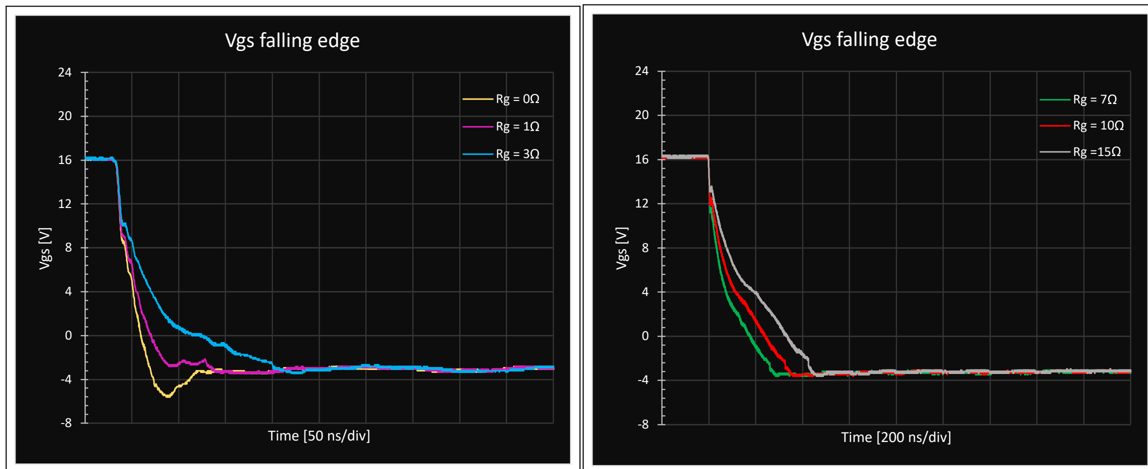


Figure 5.3: V_{GS} *falling edge for different gate resistance value.*

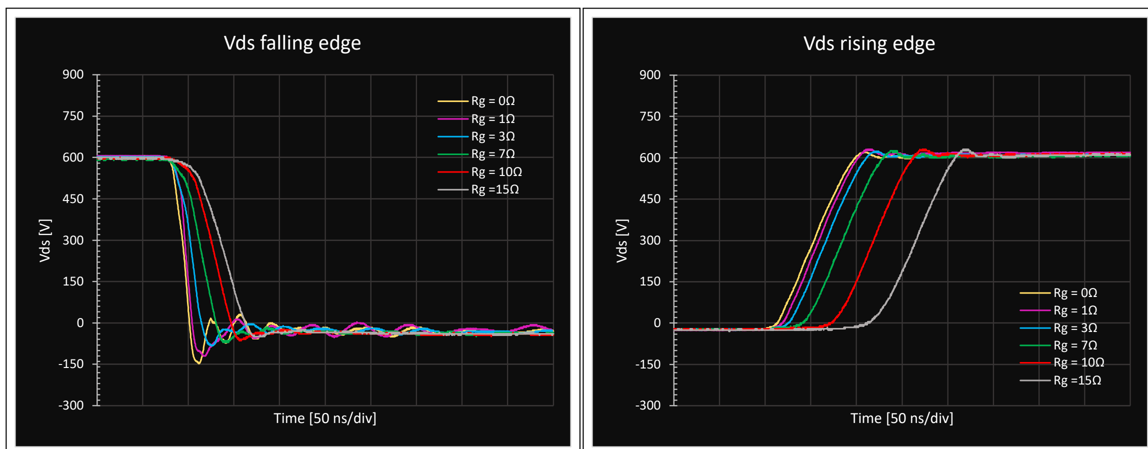


Figure 5.4: V_{DS} *falling (left) and rising (right) edge for different gate resistance value.*

5.2.3 Effect of an added gate capacitance

The gate voltage behaviour has been analyzed by introducing an external gate capacitance and control the transistor turn-on.
The internal transistor input capacitance is about 6 nF and the external added capacitances are 4.7 nF and 10 nF. This test has been done with a gate resistance of 1 Ω, and with RC snubber (10 Ω, 470 pF).
In figure 5.5 it is reported the rising edge of the V_{GS}: as expected, it is noticeable that the rise time increases for higher gate capacitance, but the benefits are in a better suppression of the ringings and overshoots.
Compared to the previous test, it can be observed both a gate resistor and a capacitance increases helps in ringings suppression, with some differences in the steepness of the edge that is sharper without gate capacitance.

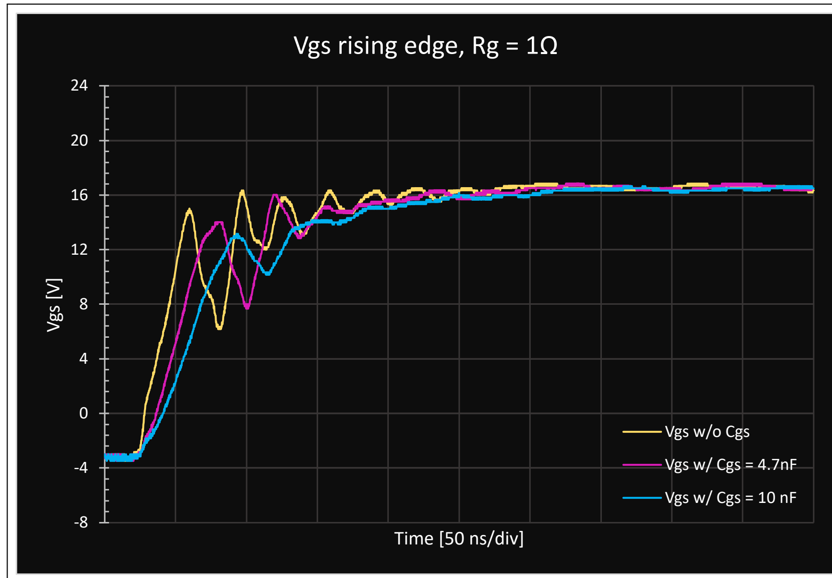


Figure 5.5: V_{GS} *rising edge for different gate capacitance value.*

5.2.4 Effect of snubbers

The next analysis includes the study of the circuit when snubbers are present or absent. Here the first test is made on the critical edge for the low-side transistor, the turn-on. In figure 5.6 are depicted two plots showing data collected from the DSO in the correspondence of the V_{GS} rising edge and V_{DS} falling edge and then exported in .csv format to be post processed. The board has been powered with 600 V DC for this test, the gate resistance has been fixed to 1 Ω and the RC snubber used is a 10 Ω resistor and a 470 pF.
As it can be seen, strong oscillations lasting several hundreds of nanoseconds are present when no snubber is used (yellow), leading also to overvoltages up to 20 V on the gate, and undervoltages below −150 V on the drain. With snubbers (magenta), the oscillations are still present, but strongly dampened and the maximum peak is lower, especially on the gate.
A DPT test, shown in figure 5.7, has been also performed, where it has been monitored the V_{DS} (magenta) and the load current (yellow) with the DSO. Here the benefit of the snubber are more evident, and also the load current exhibits a cleaner waveform.

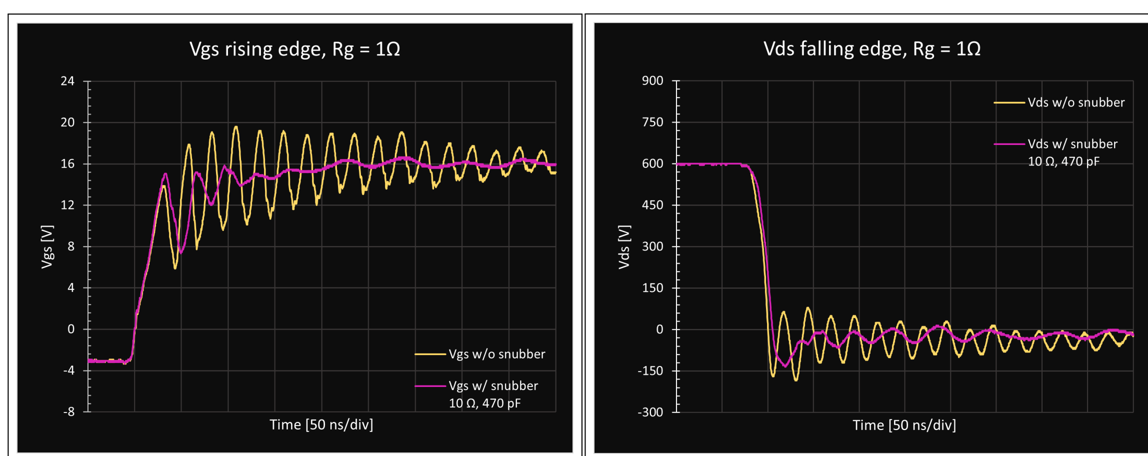


Figure 5.6: V_{GS} *rising edge (left)* V_{DS} *and falling edge (right) without snubber (yellow) and with snubber (magenta).*

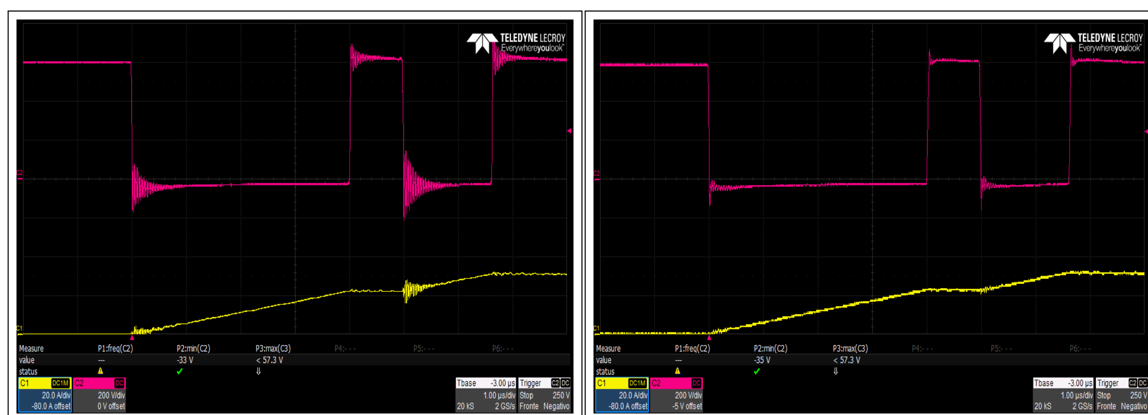


Figure 5.7: *Double pulse test:* V_{DS} *low side (magenta) and load current (yellow). Left: without snubber. Right: with snubber.*

In the end, figure 5.8 shows a test performed ad 800 VDC with a PWM pulse. The waveform shown are V_{GS} in green, V_{DS} in blue and the load current in yellow.

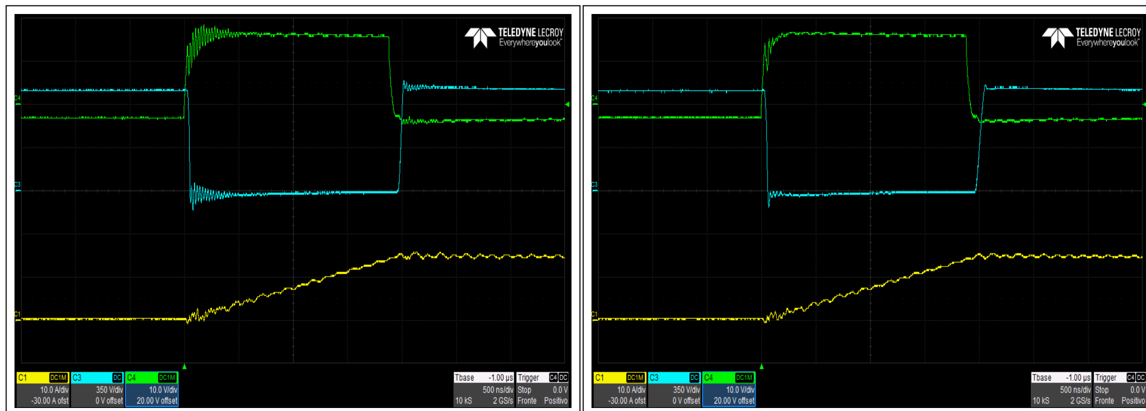


Figure 5.8: *Low side PWM pulse. Green:* V_{GS}. *Blue:* V_{GS}. *Yellow: load current. Left: without snubber. Right: with snubber.*

5.2.5 DC bus voltage monitoring

The DC bus voltage has been monitored through the differential probes to observe any variation. It has been discovered that the long terminals of the probe clips influence significantly the measurement. Therefore the test have been performed trying to improve the acquisition system by removing the clips which add stray inductance to the path, and shielding the probe cables with metallic tape, as shown in figure 5.9.

Figure 5.9: *Differential probe with shielding.*

Figure 5.10 shows the DSO data of the bus voltage on the left and a zoom on the first oscillation acquired with two standard differential probes, where the magenta waveform has been obtained shielding the probe cables with metallic tape and removing the clips, while the blue waveform is obtained through the standard probe setup.

The perturbation introduced by the probes is noticeable, both in amplitude (few tents of volts) and in oscillation damping. Taking as reference the magenta curve, for the first oscillation the bus voltage shows variations about ±60 V over the nominal value of 600 V, so a ±10% variation.

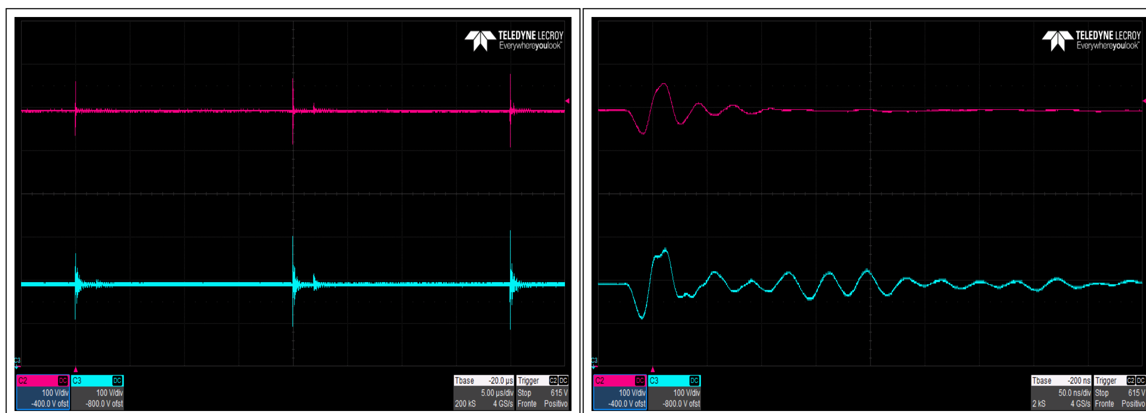


Figure 5.10: *600 VDC bus voltage ringings during successive PWM pulses (left) and a zoom on the first ringing (right). Magenta: measurements with shielded cables and without clamps. Blue: measure with standard differential probes.*

In table 5.1 it has been reported the voltage sensed with this system for DC bus voltages values from 100 V to 800 V. The sensing circuit shows a good linearity and a maximum error of 6.6 mV. The readings have always a smaller value than the expected, so this is a systematic error probably due to the voltage divider resistors tolerance.

VDC [V]	EXPECTED VALUE [V]	READING [V]	ERROR [V]
100	0.25	0.2435	0.0065
200	0.50	0.4947	0.0053
300	0.75	0.7467	0.0033
400	1.00	0.9947	0.0053
500	1.25	1.2453	0.0047
600	1.50	1.4954	0.0046
700	1.75	1.7465	0.0035
800	2.00	1.9934	0.0066

Table 5.1: DC bus voltage sensing results

5.2.6 Measurements with a wire for monitoring the transistor current

Since the system does not allow for a direct current measurement of the transistor current, it is experimented an alternative solution: a piece of wire has been substituted to the low-side shunt, creating a small loop around which it has been possible to hook a current probe, as shown in figure 5.11. The drawback of this system is the high increase of the stray inductance of the power loop, and the expecting result is in stronger oscillations. It has been calculated an increase of 56 nH for the wire length of 6 cm and section 1 mm [22].

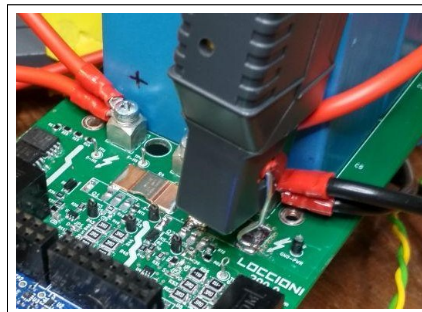


Figure 5.11: *Drain current measurement setup.*

Measurement has been taken at 600 VDC and without snubber. Figure 5.12 depicts clearly this effect: here it is shown the V_{GS} in green, V_{DS} in blue and the transistor I_{DS} in magenta.
Oscillations dramatically increases in amplitude, reaching almost −500 V of undervoltage on the V_{DS} and causing the gate voltage to bounce back to 0 V during the ringings. The overshoot on the drain current is even higher than the value at the end of the pulse.

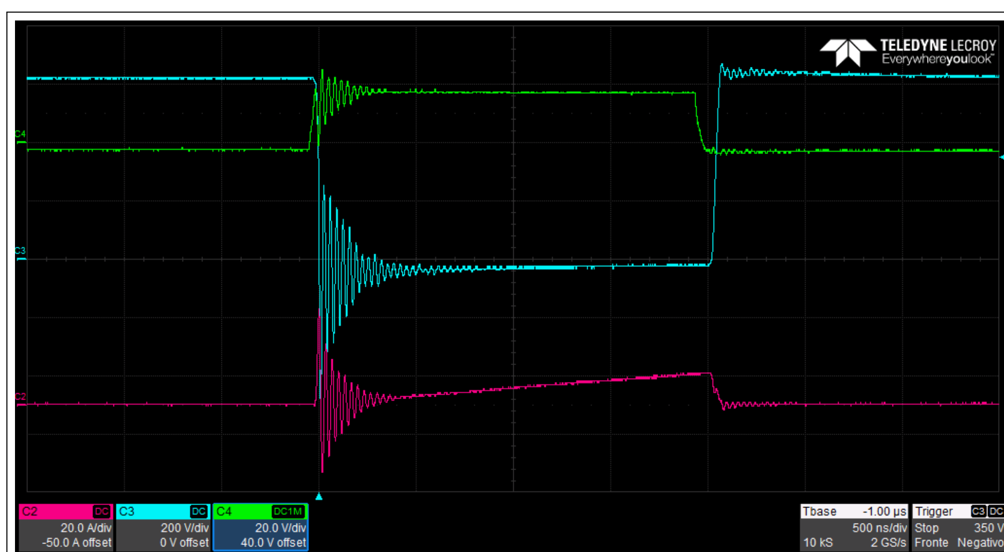


Figure 5.12: *Magenta: I_{IS} measurement with wire extension. Green: V_{GS}. Blue: V_{DS}.*

5.2.7 Short circuit fault test

This section describes the test made to verify the current monitoring and protection system behaviour, both through shunt resistor and desaturation by connecting the jumper pads on the desired position.
First, it has been verified the correct functioning of the current sensing circuit made by the current mirror and the isolation amplifier of figure 5.13, recalled here for clarity. It came out that the differential voltage at the input of the amplifier is always close to the maximum input range of 0.2 V yet when the circuit is simply powered on but not switching, and the same occurs for the voltage at the OC node, which was supposed to swing from 0 to 0.7 V. As soon as the PWM pulses are sent to the circuit, the drivers signal immediately the overcurrent fault and proceed with the soft shutdown.

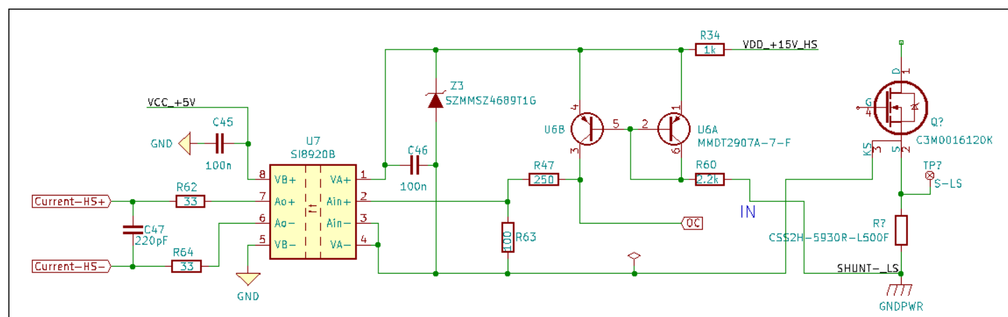


Figure 5.13: *Current sense and protection circuit*

At this point, the shunt resistor voltage has been acquired during the transistor turn-on, to verify any failure. In figure 5.14 the shunt voltage is sensed during the transistor commutations (magenta curve), and it can be seen that it is characterised by strong oscillations for all the pulses duration, with peak voltage above 100 mV. Recalling that the shunt is designed to reach 75 mV with a drain current of 150 A, it is clear that its voltage is strongly sensible to every transistor commutation and the small resistive part of the component seems to be completely masked by its inductive behaviour. This may cause disturbances to the other nearby measurements, even if the oscillation frequency should be filtered by the internal capacitances.

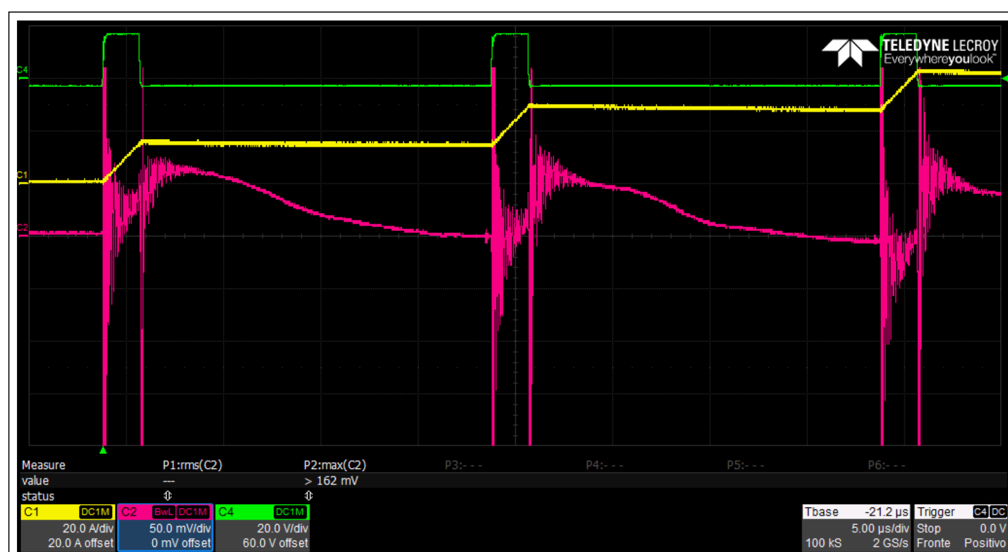


Figure 5.14: *Magenta: shunt resistor voltage. Green: gate voltage. Yellow: load current*

At this point it has been tried to simulate the current mirror circuit by using an ideal shunt resistor without inductive part. The simulation result is shown in figure 5.15: the current generator sweeps the drain current from 0 to 150 A, but no significant variation occurs on the OC node and across the ISO node, on the contrary their voltage settles respectively at values above 700 mV and 200 mV, both over the maximum range for the short circuit detection. For this reason, as soon as the first PWM pulse is sent, the system detects the inductive spike on the shunt resistor as a fault signal.
At the end of this result, it can be supposed that a small shunt resistance and/or a high current to be detected is not suitable with this system taken from a reference design. Moreover, shunt resistors introduce high noise in application due to the high dv/dt in play, that makes their parasitic inductances not negligeable.

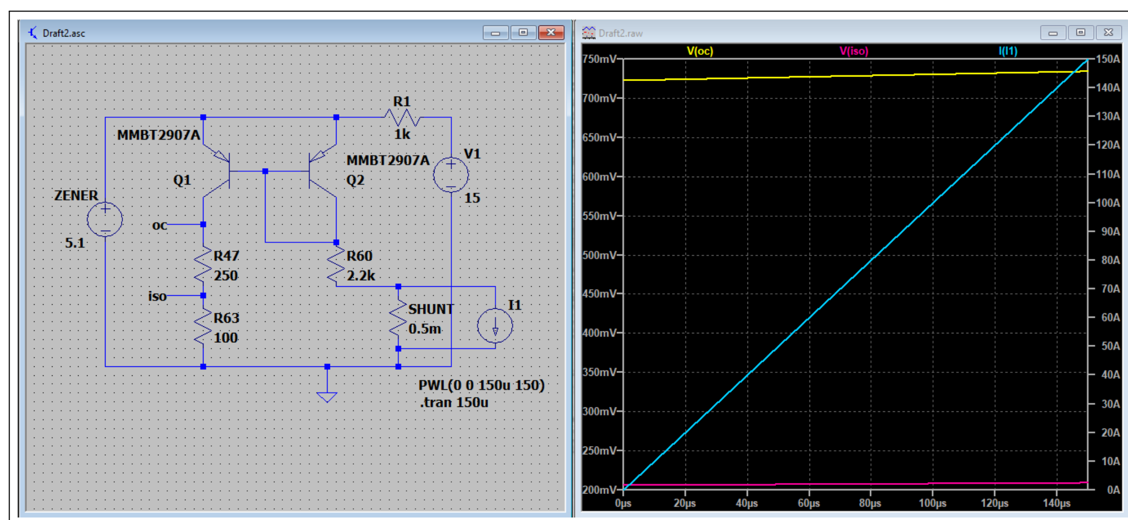


Figure 5.15: *LTSpice simulation of the current sensing and protection circuit.*

Next, the desaturation method has been tested. As a first test, the resistor network has been resized in order to achieve a fault in correspondence of a drain current of 60 A and a blanking time of 100 ns, then it has started with a DC bus voltage of 60 V and an inductive load of 3 µH. With these data it is possible to calculate the time for the current to rise up to the overcurrent threshold with the formula:

$$t = L_{load}\frac{I_{DS_{fault}}}{V_{DC}} = 3\,\mu H\frac{60\,A}{60\,V} = 3\,\mu s$$

and so, a 4 µs pulse has been generated for this test. Moreover the measurement has been made with the wire instead of the low-side shunt resistor, in order to analyze the drain current at the occurrence of the fault. The image 5.17 shows the V_{GS} in green, V_{DS} in blue and I_{DS} in magenta.
As soon as the current reaches 60 A, the gate voltage starts decreasing after less than 200 ns with the soft turn-off procedure, managed by the driver in order to avoid dangerous spikes due to high dv/dt on the drain node. Despite this feature, the high inductance of the wire added to measure the current causes an overshoot of about 156 V over the DC bus voltage. From the moment in which the fault is detected (V_{GS} falling edge beginning) to the moment when the drain current stops increasing and therefore the transistor is shut down, a current increment of less than 10 A is obtained, corresponding to about the 10% of the overcurrent threshold.
In figure 5.16, a zoom on the time interval in which driver shuts down due to fault detection is shown, highlighting the di/dt in order to estimate the parasitic inductance of the power loop.
In the end, the same test (figure 5.18) has been performed with the low side shunt connected instead of the wire: this allows to obtain the voltage overshoot to be compared to the previous setup, being able to estimate by difference the inductance of the two paths, by supposing the same di/dt.
Further tests have been made with higher DC bus voltage, but above 120 VDC, the driver always detects a fault

as soon as the PWM pulse is sent, similarly to the previous case for the shunt resistor based method. Here, on the OC driver pin, strong oscillations with high peak voltage establish at the transistor switching instants, and even if they have a frequency higher than the cutoff, can be detected as fault.
The problem occurs even if neither the SHUNT nor the DESAT pad is connected to the OC pin through the SMD jumper, and the result is that the circuit results always in fault condition as soon as it is switching, even with low drain current detected. To solve this problem, the OC pad has been forced to the driver IC COM terminal, forcing a zero voltage on that pin, with the drawback of having no protection activated for the tests at higher voltages.

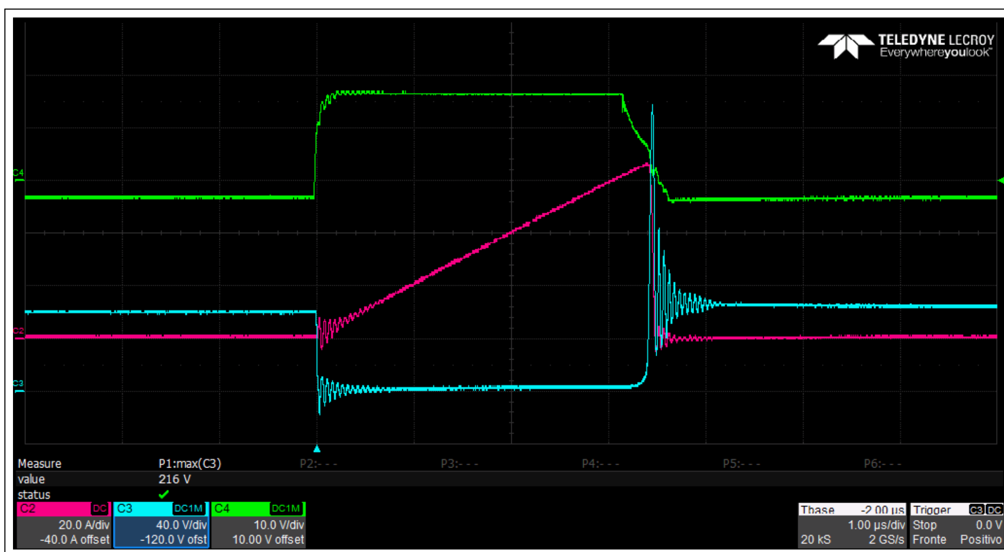


Figure 5.16: *Short circuit test with wire. Green:* V_{GS}. *Blue:* V_{DS}. *Magenta:* I_{DS}. *The maximum peak voltage is 216 V out of a 60 VDC bus voltage.*

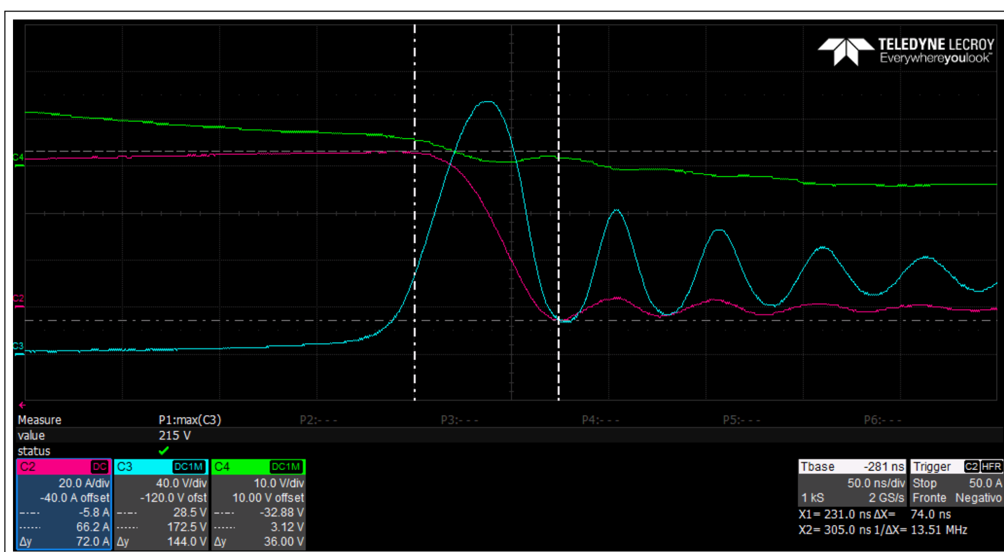


Figure 5.17: *Short circuit test with wire zoom. Green:* V_{GS}. *Blue:* V_{DS}. *Magenta:* I_{DS}.

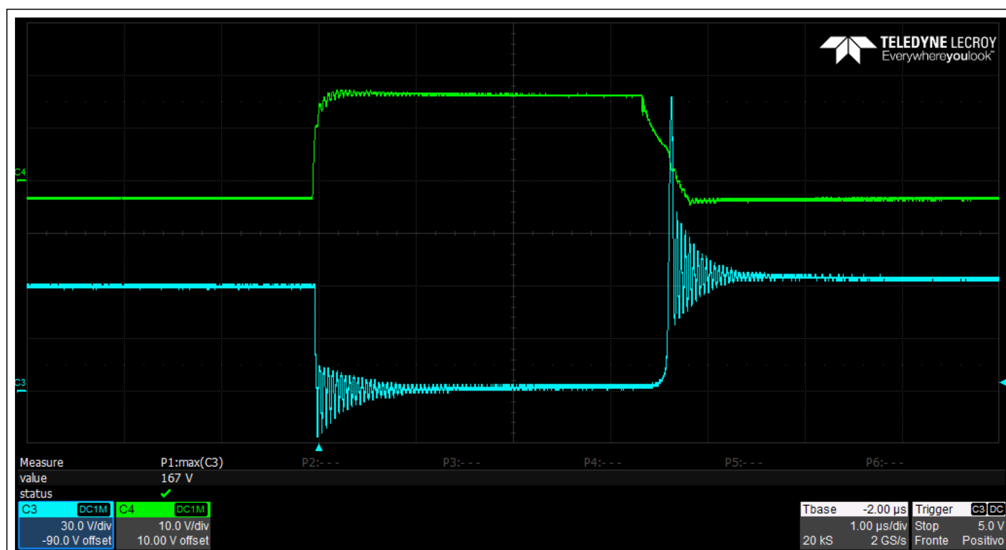


Figure 5.18: *Short circuit test with shunt resistors. Green:* V_{GS}*. Blue:* V_{DS}*. The maximum peak voltage is 216 V out of a 167 VDC bus voltage.*

5.2.8 Parasitics estimation and simulation adjustment

As anticipated in the previous paragraph, in this section is described the procedure adopted to have an estimation of the parasitics of the circuit. Since stray inductance has a relevant influence in such applications, it is fundamental to have an idea of the entity of their value.
From figure 5.17, the ΔI and Δt at the transistor turn-off can be read. The total inductance is obtained as the voltage overshoot multiplied by the $\frac{\Delta I}{\Delta t}$ as follows:

$$L_{stray_with_wire} = \Delta V \frac{\Delta I}{\Delta t} = 156\,V \times \frac{72\,A}{74\,ns} \simeq 152\,nH$$

This is the inductance comprising the four transistor terminals (two drains and two power sources), the internal parasitic inductances of the transistor bondings described in the spice model, the high-side shunt resistor, the wire and the PCB traces.
By performing the same calculation using the same $\Delta I/\Delta t$ and the voltage overshoot obtained from figure 5.18 $\Delta V = 107\,V$, the inductance of the original circuit with both the shunt resistors can be obtained. The result obtained here is $L_{stray} = 104\,nH$. By assuming as shunt parasitic inductance the maximum value declared into the datasheet of 3 nH, it is possible to obtain the loop inductance of the added wire by difference:

$$L_{wire} = L_{stray_with_wire} - L_{stray} + L_{shunt} \simeq 51\,nH$$

This result is in agreement with the previous wire parasitic inductance estimation.
The sum of the terminals inductance and the PCB traces can be now computed by subtracting the value of the two shunt parasitic inductance and the internal device inductances to L_{stray}, leading to:

$$L_{leads} + L_{PCB} \simeq 84.5\,nH$$

The parasitic inductance estimated is close to the previously estimated in section 4.3, therefore those values of snubber capacitance and resistor confirmed the expectations.

Another method to estimate the loop inductance is the one suggested in [23] and consists in measuring the oscillation frequency f_0 of the circuit first without snubber, and then adding a known capacitance C_1 across the transistor and measuring the second oscillation frequency f_1. Doing the math, the following relation is obtained:

$$C_0 = \frac{C_1}{x^2 - 1} \qquad x = \frac{f_0}{f_1}$$

Where C_0 is the capacitance of the initial circuit, i.e. the transistor output capacitance C_{oss}. At this point it is possible to calculate the stray inductance L_{stray} of the circuit as follows:

$$L_{stray} = \frac{1}{(2\pi f_0)^2 C_0}$$

As a proof of the correctness of the result, the inductances calculated with C_0 and f_0 or C_1 and f_1 remains unchanged. The snubber resistor and capacitor are then found by using the formulas of section 4.3.
This method has been applied to the gate driver board, and the results obtained are reported in table 5.2: the measurements are obtained using a test capacitor $C_0 = 555\,pF$ (measured value), at three different DC bus voltage, chosen on the basis of the output capacitance data of the transistor datasheet, which assumes an almost constant value for DC voltages above 600 V.

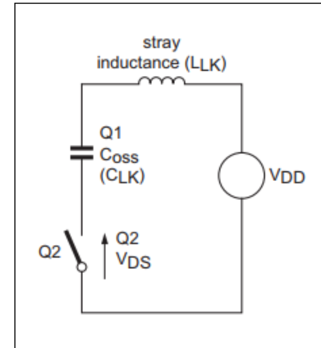


Figure 5.19: *Schematic representation of the loop capacitance and inductance.*

V_{DC} [V]	f_0 [MHz]	f_1 [MHz]	x	C_0 [pF]	C_1 [pF]	L_{stray0} [nH]	L_{stray1} [nH]
600.000	39.700	30.375	1.307	783.635	555	220.134	128.866
700.000	40.160	31.000	1.295	818.248	555	202.407	120.604
800.000	40.402	31.875	1.268	914.949	555	171.213	106.569

Table 5.2: Values obtained with the method described in [2].

The method does not give satisfactory results, since the prof of the two inductances values is not verified. Moreover the output capacitance (C_0) obtained is different from the 230 pF value of the datasheet, probably due to the fact that the added capacitance has been placed in parallel after the transistor terminals, which inductance compromise the measurement.

The parameters of the first estimation have been added to the LTspice simulation distributing 21 nH for each transistor terminals. The circuit has been completed by adding the DC bus capacitors with their parasitics, as shown in figure 5.20.
In the successive pictures, simulated waveforms of the V_{GS}, V_{DS}, I_{DS}, bus DC voltage and shunt resistor voltage are taken and compared to the real data obtained through the DSO.

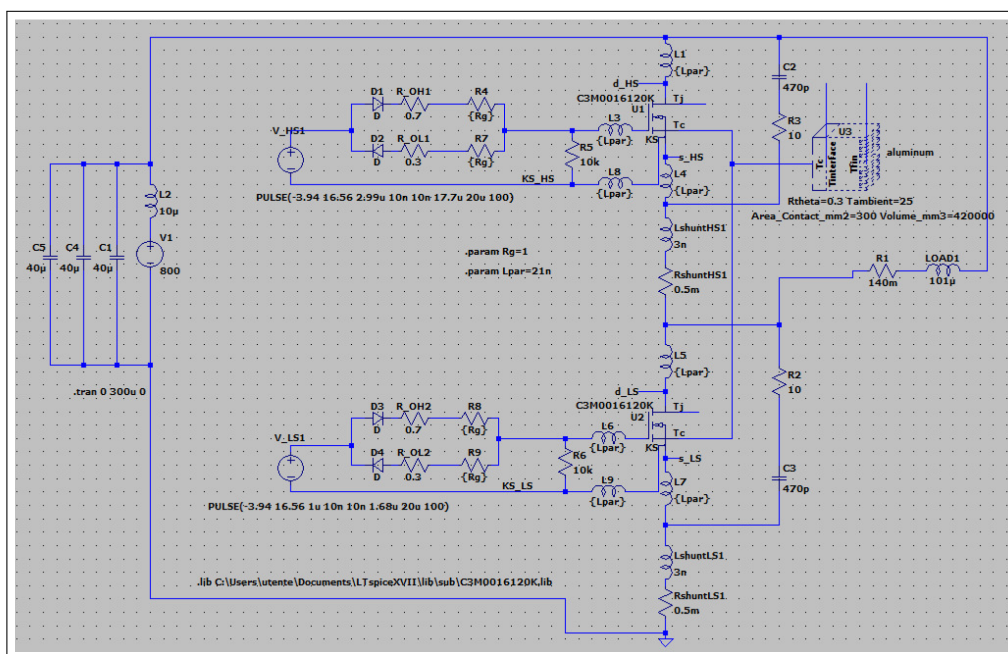


Figure 5.20: *LTSpice simulation complete circuit.*

Simulation data have been acquired with a bus DC voltage of 600 V and on the low-side, to match the previous measurements settings taken with the DSO. In figure 5.21 it is shown the V_{GS} voltage: from the comparison with the waveform in figure 5.4 correspondent to a 1 Ω gate resistance, correspondences are noticeable for the presence of the two voltage peaks in the rising edge, while for the falling edge, the simulation shows a more remarkable Miller effect than the DSO data.
Different is the situation for the V_{DS} (figure 5.22): a much higher undervoltage peak is obtained in correspondence of the falling edge (−300 V vs. −150 V from the comparison with figure 5.4), a probable hint of an overestimation of the parasitic inductance of the power loop.
Next, in figure 5.23 it is shown the DC bus voltage during the transistor commutations: what the simulation shows are overvoltages of few tents of volt around the bus voltage, while from the DSO data in figure 5.10 the overvoltages amplitude measured is the double. Moreover the second lower overvoltages peaks of the simu-

lated circuit are almost unnoticeable in the real measurements.

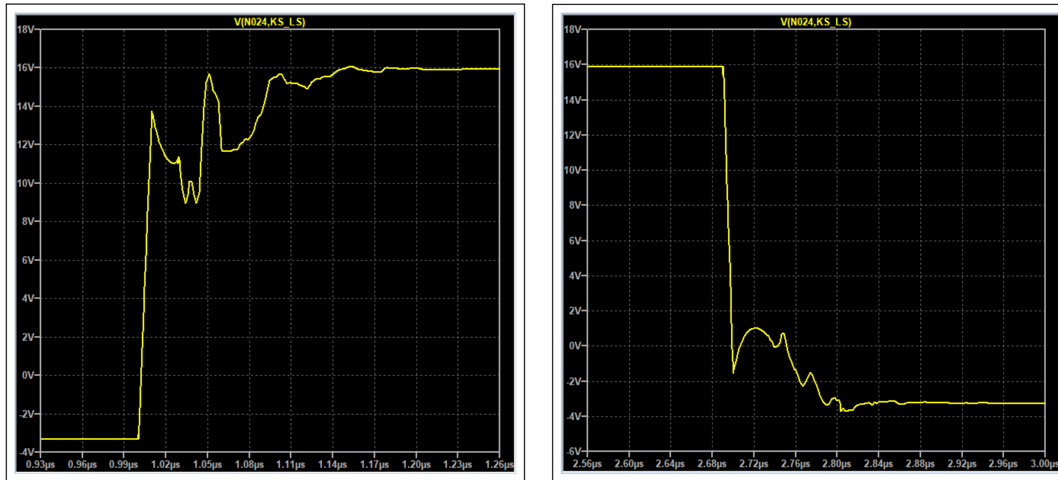


Figure 5.21: *LTSpice simulation with parasitics:* V_{GS} *rising edge (left) and falling edge (right).*

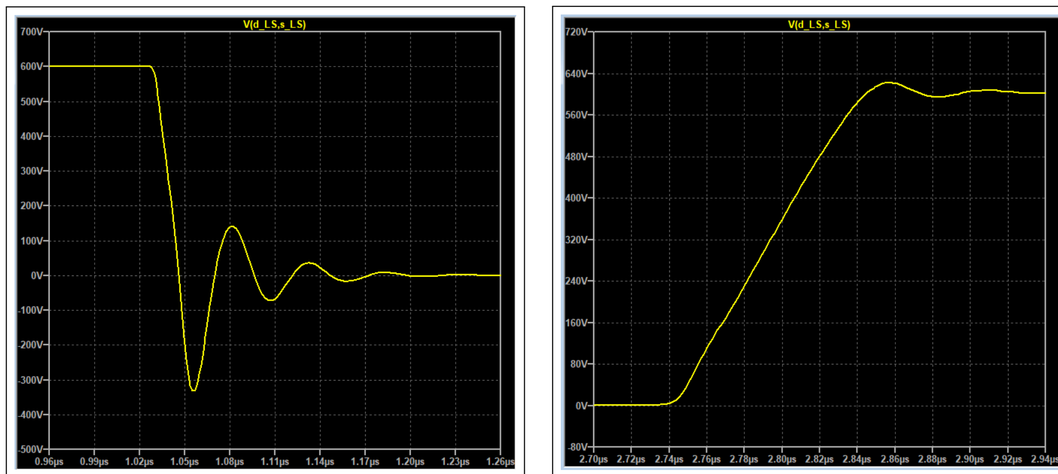


Figure 5.22: *LTSpice simulation with parasitics:* V_{DS} *rising edge (left) and falling edge (right).*

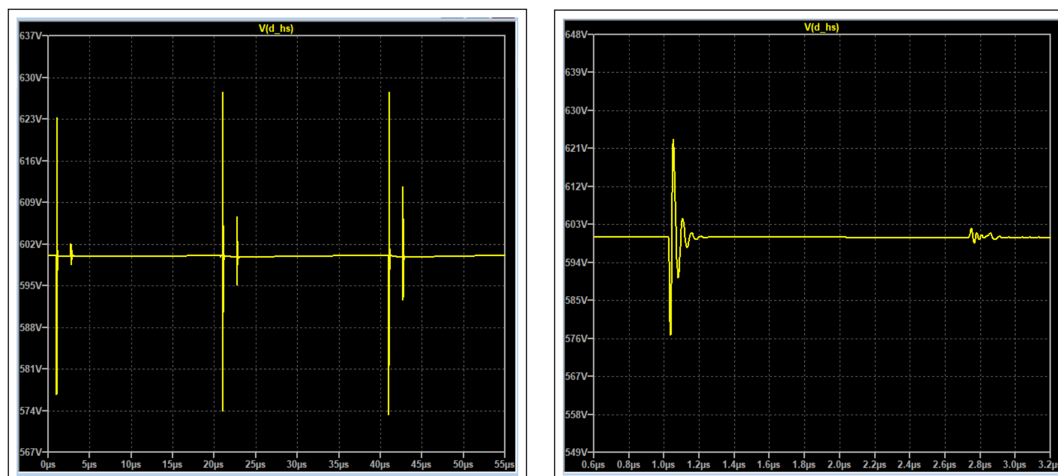


Figure 5.23: *LTSpice simulation with parasitics: 600 VDC bus voltage ringings during successive PWM pulses (left) and a zoom on the first ringing (right).*

A last attempt has been made to find a possible value for the parasitics by trying different parasitic inductance values that better fits with the results obtained. It has been found that the best combination of parasitics values is:

- transistor terminal inductance: 4 nH;
- shunt resistor parasitic inductance: 1 nH;
- DC source inductance: 1 µH

The improvements obtained with this further refinements are shown in figures 5.24 and 5.25: the correspondence with the measured data are found in the undervoltage peak of around −150 V and in the resonance frequency of around 31 MHz. Gate voltage and DC bus oscillation instead does not show significant variations: the simulated overvoltages on the DC bus set around 50 around the supply voltage, slightly increased with respect to the previous simulation, while the gate voltage shown a similar behaviour.

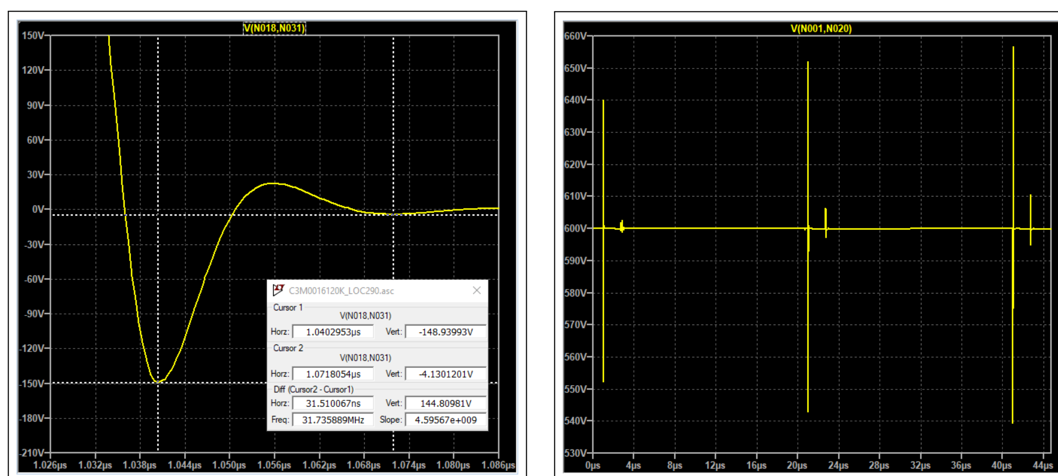


Figure 5.24: *LTSpice simulation with refined parasitics:* V_{DS} *falling edge (left) and 600 VDC bus voltage ringings during successive PWM pulses (right).*

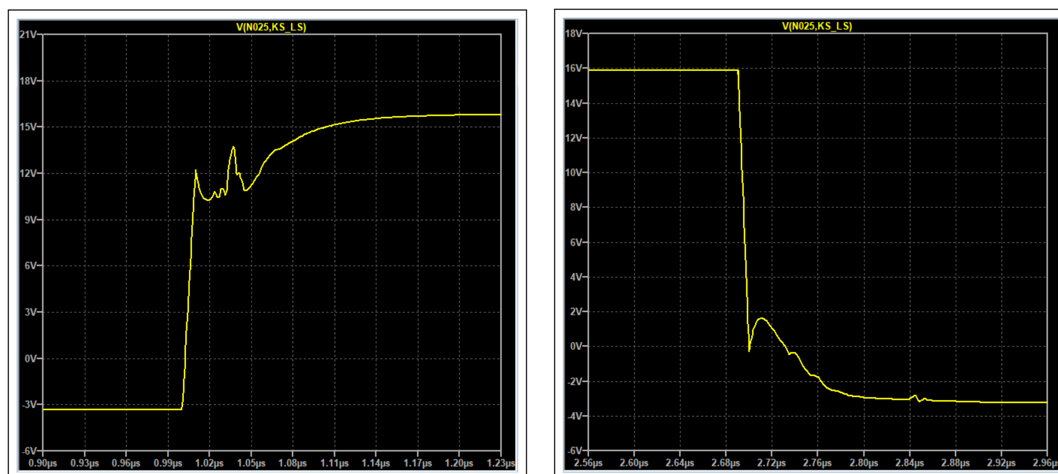


Figure 5.25: *LTSpice simulation with refined parasitics:* V_{GS} *rising edge (left) and falling edge (right).*

Chapter 6

Future work

The aim of this project is to realize a gate driver to be implemented in a system for testing application of power transistor devices or modules. The devices under test will be contacted through needles by the driver that has to be designed ad-hoc to be used is such an environment, in order to perform the required tests pattern necessary to validate the compliance of the device, such as short circuit test and double and multi-pulse test.
Several improvements can be done to this gate driver prototype, first of all the protection system must be revisited, finding a suitable method to sensing the current and studying deeper the best method to prevent fault. The next step is to model the effect of the needles and the limit as much as possible the overshoots due to parasitic inductances; devices under test have their own characteristics, and whether they are single devices, power modules or bare die components, they introduce different parasitics in the testing system, that must be taken into account.
Up to know this prototype allowed to acquire knowledge and awareness of the problematics and requirements to be taken into account when dealing with silicon carbide, still an emerging technology nowadays, that requires effort to be exploited as best as possible, but for sure an opportunity to make a breakthrough in electronics.

Chapter 7

Conclusions

In this thesis, the design of a gate driver for SiC MOSFETs has been presented, describing and the design choices and realizing the prototype on a PCB in order to be tested and characterized by analysing its behaviour under different test conditions.

It has been shown how parasitic inductances influences the circuit response during the commutation, causing ringings and overvoltages by far above or below the supply voltage, therefore the first focus is to optimize the PCB layout to reduce the power loop path length as much as possible.
Estimating the parasitics is a hard task and not always it is possible to obtain precise results just from simulations, even after adjustments made from comparison with the real circuit.

To control these unwanted effect, snubbers plays an effective role in suppressing the ringings. Different and more complex typologies of snubbers can be implemented, accompanied by clamp circuits to suppress the overvoltages, but taking into account to minimize the circuit complexity to keep parasitics under control.
It has been analyzed how to control the high dv/dt on the gate and drain voltage by choosing a suitable value of gate resistance, even choosing different values for ON and OFF resistance to adjust separately falling and rising times, or adding an external gate capacitance to keep the fast transients under control. In some application it is common to add also a ferrite bead around the gate terminal to suppress the gate ringing at high frequency.

Protection methods need particular attentions since the SiC devices operates at high speed, and high dv/dt makes difficult to measure currents and voltages in a fast and reliable way. Isolation is fundamental whenever a power signal needs to be sensed, avoiding conflicts between signals of different power loops.
Short circuit protection methods must take action in very few microseconds to avoid the current to increase too much, since the SiC output characteristic is almost linear and does not show a saturation point for the current.
The shunt resistor method adopted here has revealed not suitable due to its strong noise detected, probably because its resistance value is too small to predominate the inductive behaviour. Moreover the solution adopted with the current mirror is not a general solution suitable for every design.
Different methods, such as the Rogowski coil, can offer a high reliability in terms of quality of measurement and response speed in these kind of applications, with the drawback of a higher cost and complexity of implementation.
Desaturation based protection method has revealed good despite several contrary opinions found in literature, further improvements need to be performed to make this circuit fully reliable for this gate driver design.
Choosing the right component is also important, especially paying attention to what the market can offer in terms of the availability, documentation and support from the manufacturer. The availability of a simulation model helps greatly to have an as much as possible affordable simulation model and better estimate the real component behaviour.

Measurement equipment plays a fundamental role: any time an instrument is used to monitor a signal, it disrupts the circuit altering the measurement, and sometimes the data are so corrupted by the external instruments to be impossible to extract any information.
Especially in these situations, where the power density of the circuit is concentrated in few square centimetres of the PCB and the measurement instruments are placed closed on to each other, obtaining information from the instruments may be a hard task.
In the case of this project, heavy differences have been found by substituting the grounding pigtail with the spring-tip: the ground loop created by the pigtail collects all the radiated energy originated from the high dv/dt commutations, masking all the useful signal.
Also using the differential high voltage probes it has been necessary to reduce as much as possible the length of the sensing terminals by removing the clips, in order to decrease the inductance of the measurement loop, and performing a shielding of the cables to obtain cleaner measurements.
All the measurements taken during these tests may be more or less altered by the measurement equipment, therefore performing more measurements of the same parameter to reduce the risk of a corrupted data is always a good practice.

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