POLITECNICO DI TORINO

Department of Electronics and Telecommunications

Master's Degree in Electronic Engineering

Master's Thesis

A study on low-power high-voltage step down AC – DC converters

Supervisor

Prof. Franco Fiori

Candidate

Matteo Di Placido

October, 2018

to my grandfather
Bruno

Ringraziamenti

Arrivare a questo traguardo è stato davvero impegnativo e questo percorso di sei anni mi ha cambiato parecchio. Quando scelsi il Politecnico di Torino ero sicuro che ce l'avrei fatta, ma ero troppo pieno di me. Il primo anno è stato un trauma, ho pensato un paio di volte di aver completamente sbagliato strada e ho creduto di non farcela. Mi sono messo alla prova senza mollare e alla fine, dopo aver dovuto imparare da capo un nuovo metodo di studio, sono riuscito piano piano a migliorare. Lasciando da parte l'aspetto didattico, venire a Torino mi ha permesso di "imparare a vivere". A diciannove anni sono uscito di casa e ho dovuto imparare a cavarmela da solo, iniziando a saggiare la vita da persona adulta. Credo che questo sia uno degli aspetti che più mi è piaciuto di questo percorso: crescere.
Non sarei mai riuscito in questa fase della mia vita se non avessi avuto al mio fianco delle persone speciali e se non avessi incontrato professori in grado di stimolarmi.

Vorrei ringraziare in primo luogo il prof. Franco Fiori, relatore di questa tesi. Il tempo dedicatomi è stato fondamentale alla buona riuscita di questo lavoro e i suoi suggerimenti sono stati utilissimi nei momenti di maggior difficoltà. Vorrei ringraziare anche Erica, Michele e Vincenzo; siete stati sempre disponibili ad aiutarmi.

Mamma e papà, senza il vostro supporto tutto questo non sarebbe stato possibile. Mi avete sempre sostenuto e ad ogni mio dubbio mi avete sempre consigliato nel migliore dei modi, vi voglio bene.

Nonna Teresa e nonno Bruno, siete i nonni migliori che un nipote possa desiderare e siete stati un supporto insostituibile alla mia crescita. Mi dispiace non avervi con

me oggi, ma sono sicuro che vi abbraccerò presto.

Tiziano, tu avresti dovuto aiutarmi a fare i “conti” per questo lavoro, ma anche se non lo hai fatto ti ringrazio lo stesso. Forse è meglio così, spero però che il livello d’inglese sia di tuo gradimento.

Non so davvero dove iniziare per dirti quanto di questo lavoro è stato possibile anche grazie a te, Serena. Il tuo è stato il supporto più vicino e vivo, non solo in questo periodo conclusivo, ma in tutti questi anni che siamo stati insieme. Per tutte le volte che mi hai sopportato, grazie. Per tutte le volte che mi hai sostenuto, grazie. Per tutte le volte che, in un modo o in un altro, hai reso un “tediosa” giornata di studio un momento per passare del tempo insieme, grazie. Per tutte le nostre piccole conquiste, grazie. Potrei continuare ancora e ancora, ma quello che voglio dire è che tu sei stata fondamentale per me. Abbiamo intrapreso un nuovo cammino insieme e sono certo che avremmo tante soddisfazioni. Continueremo a crescere insieme e voglio continuare ad essere la tua roccia, il tuo sostegno, in ogni momento.

Un grazie profondo anche a tutti gli amici conosciuti durante questo percorso: Francesco, Arianna, Federica, Guido, Edoardo, Davide, Antonio, Fabrizio e Riccardo.

Grazie anche a Marco, Bryan, Wassim, Fabiano, Eugenio e Arek. Potreste vincere il premio “peggior compagno di stanza” di sempre. Vi ho risparmiato possibili post sulla pagina Il Coinquilino di M..

Abstract

One of the main topics of nowadays research is the efficiency improvement of various electronic systems, powered with a rechargeable battery or directly connected to the main power grid. This interest should be supported by the will to abandon energy generation methods typical of the past two centuries, like non-renewable sources, first among everything coal and liquid or gaseous fossil fuels. These sources have reached their life cycle end and damaged the environment. For these reasons the world is encouraging the use of energy derived form renewable sources, moreover reducing losses is also a main concern. Following this trend, more stringent requirements have been developed like the U.S. Energy Star or the European Code of Conduct (ECoC), which apply also to power supplies. Due to the increasing number of consumer electronics, the aforementioned standards have been starting to consider not only the efficiency of a device in maximum load conditions, but also in no load or light-load ones. These requirements involve more effort, for hardware engineers, in the design steps.

The scope of this work is to design and simulate a circuit able to convert power from the main power grid (AC domain) to a much lower constant voltage ($3.3\,V$) and which could provide up to one hundred milliamps in full load condition, at the same time a comparison between different integrated circuits is required. The most recent of them have been searched on different product selector guides of various manufacturers, in order to obtain a proper comparison in terms of availability and marketability. Among all the topologies used, the most simple and suitable for the required specifications has been chosen: a non-isolated buck converter. Its working principle has been described in detail, as well as its control system.

A device, in order to be sold on the market, should comply important standards; one of the most characteristic, for a switching mode power supply (SMPS) like the chosen buck, is the electromagnetic compatibility (EMC). The device is required to not generate too much electromagnetic noise, both radiated and conducted. The first one is mainly solved by proper placement of components and suitable enclosure, whereas the second one is dealt with an electromagnetic interference (EMI) filter. In the end, also this filter has been discussed, designed and simulated in LTSpiceXVII.

Among all the possible integrated circuits founded, the first choice has been the VIPer01 from STMicroelectronics. Its internal structure has been discussed, a buck converter designed with it, simulated in different working condition and then the efficiency has been computed at various loads. In order to compare different circuits and find better results in terms of efficiency, an additional research has been conducted focusing attention on buck input voltage reduction methods. The previous research result led to the use of a capacitive voltage divider. This approach not only provides a reduction of stress over components and switching losses, but increases also the number of possible integrated circuits that can be used.

In the end, various devices have been simulated under similar working conditions, their efficiencies compared as like as their overall cost and number of components. As expected the best result has been obtained with a synchronous non isolated buck converter. It has been shown how a good research and proper selection of components leads to good results and efficiency improvements.

Contents

1 Introduction **1**

2 State of Art **7**

2.1 Market oriented research 8

2.2 High voltage step-down problem 11

2.3 Reduced number of components solutions 15

2.4 Conclusions 16

3 Found solutions' working principle **17**

3.1 Buck 17

3.2 Boost 27

3.3 Buck-Boost 31

3.4 Flyback 37

3.5 Transformerless power supplies 41

3.6 Conclusions 43

4 Ideal buck design **44**

4.1 Ideal buck design 44

4.2 Power losses 48

4.3 Simulations 50

4.3.1 Ideal buck 50

4.3.2 Considering real switch and diodes 54

4.3.3 Efficiency considerations 58

4.4 Conclusions 59

5 EMC for SMPS **60**

5.1 What is the meaning of EMC? 60

5.2 Conducted emission, radiated emission and standards 61

5.3 Common mode currents, differential mode currents and EMI filter . . 63

5.4 EMI filter design procedure 67

5.5 EMI filter frequency response 70

5.6 Conclusions 72

6 VIPer01 based solution **73**

6.1 VIPer01 73

6.2 Real buck design 77

6.2.1 Feedback design 77

6.2.2 Simulations 84

6.2.3 EMI considerations 89

6.3 Conclusions 93

7 Proposed solution to improve efficiency **94**

7.1 Proposed solution 94

7.1.1 Reducing the high input voltage 95

7.1.2 Capacitive divider simulation 101

7.1.3 Conclusions 103

7.2 Using the capacitive divider in real circuits 103

7.2.1 VIPer01 with capacitive divider 104

7.2.2 LT8630 with capacitive divider 106

7.2.3 LTC3638 with capacitive divider 109

7.2.4 Comparison of all the results 111

7.3 Solutions' cost 113

7.4 Conclusions 117

8 Conclusions **118**

References 119

CHAPTER 1

Introduction

The world of power supplies is changed quite a bit since the availability of high voltage bipolar power transistor ('60). These devices, in fact, allowed the realization of switching mode power supplies (SMPS). Linear power supplies, which were the only solution before the advent of power transistors, are now used in limited applications and the market is mainly covered by SMPS. This is happened because of the high volume and weight reduction provided by SMPS, in fact they do not need the bulky line transformer typical of linear power supplies.
Nowadays power MOSFETs (which started to appear in '70) have pushed the switching frequency in the hundred-kilohertz/megahertz rage and this has reduced the size of magnetic components further more with respect to what was possible with power bipolar junction transistors (BJT). Starting from the growth of the Internet ('90), data processing capability demand has continued to increase, a larger and larger number of consumer electronic devices is appeared on market and, as a consequence, the number of power supplies has been increased. Not only the number is increased, but also the power density, which is the capability to deliver a specific amount of power in a given volume. This aspect is clearly discussed in [1] and figure 1.1 shows trends for server, desktop and notebook power supplies. This growth led to the introduction of more stringent requirements for efficiency also at light load, the European one is the ECoC (European Code of Conduct) and the United States have the U.S. Energy Star requirement. There are many more of them and now they require the hardware engineer to consider different aspect during the design steps.

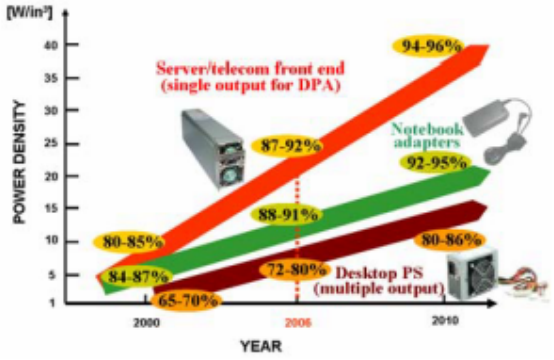


Figure 1.1: Power supplies densities and efficiencies, for various applications in [1]

The European energy consumption has been reduced by more than 10 %, during 2005-2015, thanks to green politics and the application of the previously mentioned requirements [2]. Losses reduction and the use of renewable sources is an unavoidable aspect of nowadays environmental problems. For example, Europe aims to use 20 % of the total gross power from renewable sources, in 2020.

To better understand why the efficiency problem is so important, let's consider data reported in the "Ericsson Mobility Report" of 2018 [3]: 5.5 billion is the number of mobile subscriptions in June 2018. This means that there are almost the same number of devices connected to these subscriptions and a similar amount of power supplies powering them. Supposing now to have an output power for each of them equal to $10\,W$, the ECoC will require them to have an average efficiency around 75 %. This means that $2.5\,W$ are lost as heat, if this power is multiplied by the number of devices, the total power lost is around $14\,GW$ and, since electric energy has a cost, the outcome is clear.

To have a better overview of the problem, let's consider the same $2.5\,W$ of lost power and a number of people per household in Italy equal to 3.75, obtained as Italian population $(60 \cdot 10^6)$ over number of households $(16 \cdot 10^6)$, the lost energy per household will be approximatively $9\,W$. Then the cost of electric energy is around $0.08\,€/kWh$, so, if the devices are supposed to work per $2\,h$ per 30 days, the cost per month will be around $0.043\,€$ and $0.52\,€/year$. This is not a big number for a single household, but it will increase to $8.3\,million\,€/year$ considering all the households in Italy.

It is clear that power saving is unavoidable and, as already said, standards become more and more stringent over time. Considering for example the *EC No 278/2009*

[4], the no-load power consumption of AC-DC external power supplies shall not exceed $0.3\,W \div 0.5\,W$, depending on the power rating of the device, and the average active efficiency is required to be as reported in figure 1.2. For example, a $1\,W$

	AC-AC and AC-DC external power supplies, except low voltage external power supplies	Low voltage external power supplies
$P_O \leq 1{,}0$ W	$0{,}480 \cdot P_O + 0{,}140$	$0{,}497 \cdot P_O + 0{,}067$
$1{,}0$ W $< P_O \leq 51{,}0$ W	$0{,}063 \cdot \ln(P_O) + 0{,}622$	$0{,}075 \cdot \ln(P_O) + 0{,}561$
$P_O > 51{,}0$ W	0,870	0,860

Figure 1.2: Average active efficiency limits from [4]

output power AC-DC external power supply should have an average active mode efficiency greater than 62 %, whereas a low voltage external power supply ($V_O < 6\,V$ and $I_O \geq 550\,mA$) should show an efficiency greater than 56.4 %. In [4] the average active mode efficiency is defined as the average of the efficiencies computed at different load conditions (25 %, 50 %, 75 % and 100 % of nameplate output current).

The scope of this work is to design and simulate a circuit able to convert power from the main power grid (AC domain) to a much lower constant voltage ($3.3\,V$) and which could provide up to one hundred milliamps in full load condition, at the same time a comparison between different integrated circuits is required. Small area, reduced cost and good efficiency are the main requirements. Isolation is not a main concern for this work. Due to the very low output power required for this application, the efficiency improvements is an hard task, because there is a very small margin for power savings. Different aspects and power loss contributions will be analysed during this work, in order to obtain the previously mentioned efficiency improvements.

The required AC-DC converter is a particular device able to convert an AC power source (like the mains) to a DC one, which is much more suitable for powering different kind of circuits (like micro-controllers, phone charger, LED driver, metering applications and so on). The first question is: "why is power transferred with AC?" The answer lies in the past, in particular in the late 1880s, when the, so called, "War

of the Currents" was fought by *Thomas Edison* and *Nikola Tesla*, as reported in [5]. The outcome of this war was, as everyone know, decided by economic reasons and the winner was *Nikola Tesla* with his AC high voltage solution. Nowadays some companies are looking for High Voltages DC current solutions (HVDC), since now technology is evolved and DC current offers some benefits that are not present with AC one, like an higher stability. So, the match may not be over yet.
An AC-DC converter, also called *rectifier*, should have different characteristics, depending on the particular application it is going to power, and some examples are: *multiple outputs*, *output voltage ripple*, *fault protection*, *isolation* and many more. These are only some of the possible requirements and they can change from one device to the other. Every converter is formed by different building blocks and they are: filters, rectifiers (like single diode or Graetz's bridge), storing energy elements (capacitors, inductors and transformers) and switches.

In the following chapter multiple aspect of this work will be discussed and in particular there will be:

Chapter 1: Introduction in this chapter the scope of this thesis will be presented, a brief introduction of the efficiency problem and a short historical tour to the SMPS world given. It is also possible to understand here why requirements have become more and more stringent over time.

Chapter 2: State of Art in this chapter a set of possible solutions will be considered, deriving them from application notes or datasheets. In this way, the most recent devices will be considered, because the main sources will be the *Product Selection Guides* from different manufacturers. On top of that, this approach will give an hint of what are the main topologies used nowadays for a real marketable application, like this one pretends to be.

Chapter 3: Found solutions' working principle an explanation of the solutions found in Chapter 2 will be given here and, starting from them together with given requirements, the most suited one is selected: the buck converter. This topology is one of the easiest in terms of behaviour and, moreover, has a deeply studied control system. The number of components can be very small, which

will help reducing the complexity, the Bill Of Materials (BOM), the area and the cost. Other solutions are considered, like Capacitive Power Supplies, and the reasons why they are not suited for this application given.

Chapter 4: Ideal buck design in this chapter an ideal buck will be designed in order to obtain a reference point for future considerations. Hints will be given on how to properly select the input and output capacitor values. Secondly, the main losses contributions will be analysed and, then, some simulations will be performed. Finally, the effect of a real switch and a real diode will be considered.

Chapter 5: EMC for SMPS the electromagnetic compliance is essential for any device with a switching frequency greater than $9\,kHz$, that is able to generate electromagnetic noise. Requirements exist for SMPS, like *CISPR 22*, and they express the amount of conducted/radiated emission allowed for a given device, that should be placed on the market. An explanation of these requirements is given, in this chapter, and the difference between conducted and radiated emissions provided. The Line Impedance Stabilization Network (LISN) is introduced, since it should be used during tests for conducted emissions. At the end, the need of an Electromagnetic Interference (EMI) filter is explained, together with a procedure to design it.

Chapter 6: VIPer01 based solution among all the possible devices found in chapter 2, the VIPer01 is selected as a starting point. Its internal structure is described here, then a circuit is designed and, finally, simulations are carried on. A start-up phase, the steady state and a fault condition are simulated; secondly, the effect of the EMI filter is considered. In the end, the efficiency is computed at various load conditions, in accordance with ECoC or U.S. Energy Star standards.

Chapter 7: Proposed solutions to improve efficiency in this chapter various solutions, to get an improvements in terms of efficiency, are given. In particular, a capacitive voltage divider is used before a full-wave rectifier in order to reduce the input voltage at used integrated circuits. This will help to reduce stresses over components, but allows, also, to increase the set of available de-

vices. Starting from this, a synchronous buck converter is considered and an efficiency improvement obtained, thanks to the substitution of the free-wheeling diode with another MOSFET. The other main big contribute to power loss is the in-rush current limiting resistor, this one should act only at start-up phase, during steady state operation it will only dissipate power. The use of a *photo-triac* and a Solid State Relays (SSR) are considered as a possible solution to the previous problem.

Chapter 8: Conclusions in this last chapter the conclusions are presented, highlighting pros and cons of the various found solutions. The BOMs are compared and possible further improvements suggested.

CHAPTER 2

State of Art

The scope of this thesis is to design and simulate an AC-DC converter, with reduced occupied area, good efficiency and low output power. The specifications are here recalled: It can be seen that this converter is a low power high-voltage step-down one,

Specifications	**Value**
Input Voltage	$220\,V$ $50\,Hz$ for the EU market and $120\,V$ $60\,Hz$ for the US one
Output Voltage	$V_O = 3.3\,V$
Output Current	$I_{O_{MAX}} = 100\,mA$
Average efficiency	in accordance with the ECoC, see figure 1.2, this quantity should be $\geq 30\,\%$
No load consumption	in accordance with the ECoC, it should be $\leq 0.3\,W$
Area	smallest possible
Cost	reduced cost will help the device to be sold on the market

the maximum output power is about one third of a Watt. It can be also noticed that *galvanic isolation* is not a primary requirement, which means that the final circuit should not provide isolation between the high voltage AC side to the low voltage side. Caution should be taken when dealing with high voltages.

First of all, an initial research is conducted on *Product Selection Guides* from different manufacturers, various solutions are obtained: in particular, SMPS are mainly

used and, among all the possible topologies, *buck*, *buck-boost* and *flyback* are the most employed. From this initial analysis, it is possible to roughly select the best suited topology for this work: a buck converter. It is simple, well studied and do not require a transformer, which will increase the cost, the area and add the non-required isolation feature.
Secondly, another literature research is conducted in order to get an overview of possible new topologies used to solve the high voltage step-down AC-DC problem. The outcome of this study has shown how the issue is faced, but mainly for higher power rates than the one required in this case.
Finally, the last research step is focused onto reduced number of components solutions. *Capacitive power supplies* have been found and will be discussed in the next chapter along with the other possible solutions.

2.1 Market oriented research

The target application should be in line with market requirements, so to get an idea of what are the main topologies used today, websites and product selector guides of some companies have been analysed, in particular the following ones are considered:

- *Power Integrations*;
- *STMicroelectronics*;
- *Texas Instruments Incorporated*.

Starting from the first one, the following tables, in figure 2.1, are taken from the *Power Integrations*' product selector guides in [6] and [7]. As one can easily see, the proposed topologies are: *non-isolated buck*, *buck-boost* and *flyback*. The devices that should be considered are the ones covered by red rectangles in figure 2.1.
Moving to the *STMicroelectronics* and considering their *Power management Guide 2017* [8], one can find devices for applications like auxiliary SMPS (up to $20\,W$) and battery chargers. Tables, reported in figure 2.2, should be considered; it can be seen that, also in this case, the previous topologies are suggested: *buck*, *buck-boost* and *flyback*. *Texas Instruments* have a similar table, reported in figure 2.3, and taken from

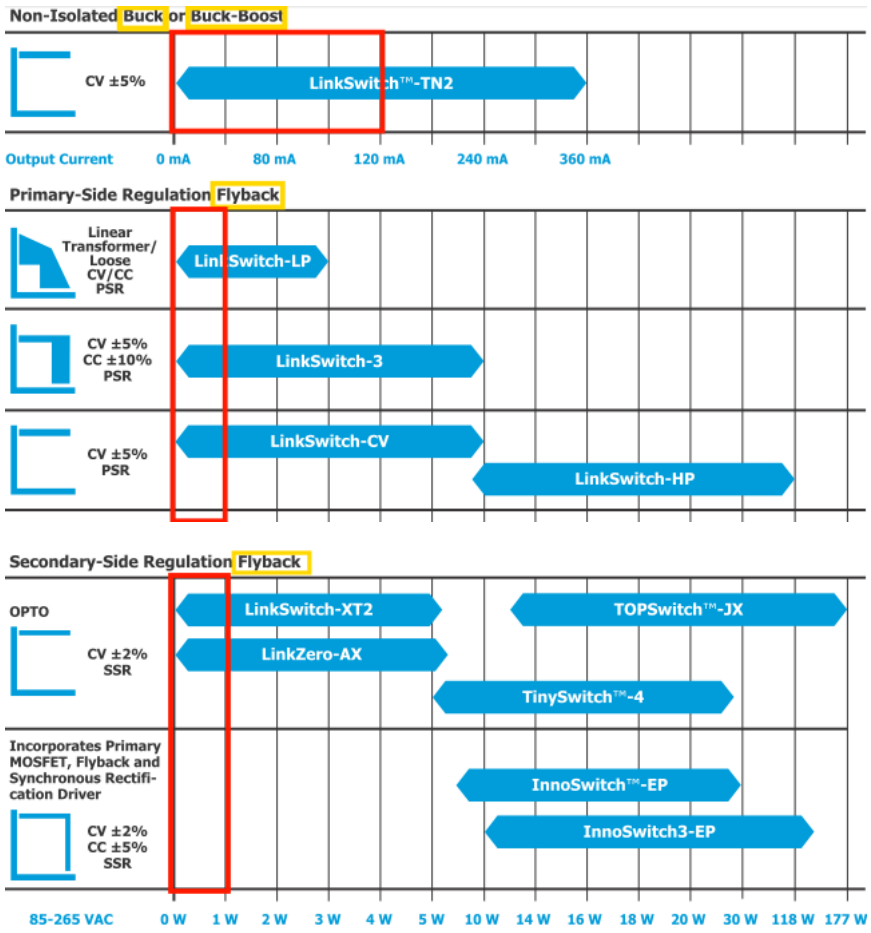


Figure 2.1: possible topologies from Power Integrations highlighted in yellow and power/current range of interest in red

its *Power management guide* [9]. Also in this case, *buck* and *flyback* are suggested, but *SEPIC* and *Ćuk* are also mentioned.

This analysis has pointed out three most used topologies available on the market and for the given power range: *buck*, *buck-boost* and the *flyback*. The latter one requires a transformer and for this reason can be already abandoned, in fact it will increase the cost and the occupied area. The final solution should not be too much overrated in terms of possible output power, for this reason devices up to few Watts should be only considered.

		Offline converters	
Buck		VIPer0P VIPer*1 VIPer*6	
Buck-boost			
Non-isolated flyback			
Isolated flyback	PSR-CV	-	VIPer0P VIPer*1 VIPer*6 ALTAIR*
	Regulation with optocoupler	VIPer*5 VIPer*7 VIPer*8	

(a) auxiliary SMPS.

			Offline converters	
Wall side	Flyback	SSR-CV/CC	VIPer*5 VIPer*7 VIPer*8	VIPer0P VIPer01V VIPer*6
		PSR-CV	-	
		PSR-CC	-	
		PSC CV/CC	ALTAIR*	
		Synch Rect	-	

(b) battery charger.

Figure 2.2: possible topologies from STMicroelectronics highlighted in yellow

Device[1]	Typical Power Level (W)	Control Method: Voltage Mode	Control Method: Current Mode	Control Method: Avg. Current Mode	Topologies
Green Mode PWM Controllers					
UCC28710/1/2	Up to 30		✔		PSR Flyback
UCC28700/1/2/3	Up to 30		✔		PSR Flyback
UCC28704	Up to 30		✔		PSR Flyback
UCC28720	Up to 30		✔		PSR Flyback
UCC28722	Up to 30		✔		PSR Flyback
UCC28730	Up to 30		✔		PSR Flyback
UCC28740	Up to 30		✔		SSR Flyback
UCC28610	10 to 65		✔		SSR QR Flyback, Buck
LM5023	5 to 65		✔		SSR QR Flyback
UCC28630/1/2/3	Up to 150		✔		PSR Flyback Controller w/700-V startup
UCC28600	50 to 150		✔		SSR QR Flyback
Switchers with Integrated FETs					
UCC28880	<3				High Voltage Switcher for Non-isolated AC/DC Conversion
UCC28881	<4.5				700-V, 225-mA Low Quiescent Current Off-Line Converter
UCC28910	7.5		✔		High Voltage Flyback Switcher w/PSR
UCC28911	10		✔		High Voltage Flyback Switcher w/PSR
General-Purpose Single-Ended Controllers					
UCC3889	<10	✔			Flyback, SEPIC, Cuk

Figure 2.3: proposed topologies from Texas Instruments highlighted in yellow and the red rectangle suggest the proper power range of interest

2.2 High voltage step-down problem

The buck converter, as like as the buck-boost or flyback, has problems when dealing with an high step down ratio. The efficiency is reduced, the switching frequency may not be high enough and, then, heavy loads affect the behaviour for the worse. For this reason, the high voltage step-down problem is faced in literature, since its resolution will provide some benefits like: voltage stress reduction, increased duty cycle and also reduced switching losses, as it will be clearer later on.

The topology considered for this research is only the buck one, since it is simpler than a flyback, for example, and is also the first one studied. A classical buck converter shows some limits, those ones are related to the high step down ratio, the conduction mode and the switching losses. *High step-down ratio* means that the switch has a very small on-time, this can be a problem if the switching frequency is high and the PWM resolution is not so good [10]. The situation gets even worse, when the output load increases and so the current reduces, in this case the duty cycle is further reduced. At the same time, the free-wheeling diode has to provide a current path for most of the switching period, this reflects onto a dissipated power, which can count for some tens of output power.
Buck's working modes affect the MOSFET dissipated power, remember that switching losses become more and more important as the frequency increases, whereas the conduction losses, which depends mainly on the R_{DS_ON} of the switch, are smaller. Among the available working modes, it is possible to distinguish the following main ones:

CCM this is a standard operating condition, in which the switch switches with a current different from zero both at turn-on and turn-off. Switching losses are higher with this mode, but on the other hand lower current stresses can be appreciated.

DCM this is another standard operating condition, the switch switches with initial current value always zero and so the switching dissipated power is almost reduced by half. Current stresses are higher in this case.

ZVS this mode is called *zero-voltage-switching* and the power MOSFET switches with a zero V_{DS} voltage. This leads to, ideally, zero switching power and so the frequency can be increased [11], this is an advantage since the magnetic components' dimensions can be reduced.

ZCS this mode is called *zero-current-switching* and it is similar to ZVS, but now the quantity kept at zero value, during commutations, is the current.

ZVS and **ZCS** belongs to the, so called, *soft-switching techniques*, **CCM** and **DCM**, instead, are also referred to *hard-switching* modes. *Soft-switching techniques* have also the benefit to reduce the EMI, with respect to (CCM and DCM) modes.
Switching frequency is limited by losses and there is a linear relation between them, but the use of a *soft-switching techniques* allows the converter to work with higher frequency and, then, reduced area can be accomplished.

Multiple solutions have been considered and the research's scope was, not only to find a possible already available solution, but also to get a better overview of some techniques already in use.
One of the first topology found in literature is the one in [12] and the proposed circuit is also reported in figure 2.4. Solution (b) has too many elements and so it is not particularly suited for our design, since small area is one of the requirements. Topology (a) is quite interesting, the capacitive voltage divider behaviour depends onto MOSFET's state: during conduction, the current path is provided by diodes D_5 and D_7, so capacitors C_1 and C_2 goes in parallel; during the MOSFET off state, the previous capacitors goes in series with the input rectified voltage and are charged with half of peak value. The MOSFET will switch with half of the input voltage for $4/3\pi$ of a line period and then with a sine wave portion for the remaining time. This happen because the rectifier conducts when the input AC source has a value higher than the voltage kept by the capacitors. The duty cycle of the converter is increased, when the input voltage is half of the peak value, resulting in better performance during this period of time, but, when voltage follows the input sine wave, the buck is forced to work with reduced duty cycle and so the situation is like the normal case. It is clear that the efficiency can not be improved too much with this solution and, at the

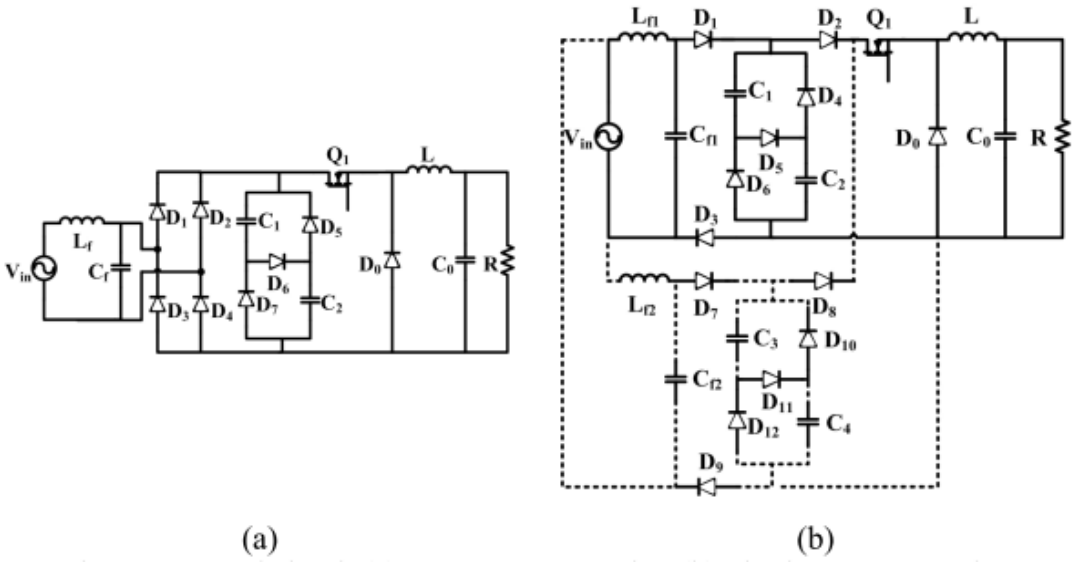


Figure 2.4: proposed topology in [12]: (a) rectifier plus capacitive voltage divider and (b) dual-phase solution

same time, it is not possible to select devices with reduced voltage ratings, because of the different behaviours within a line period.

There exists solutions for high power high-step down buck converter, like in [13], this is an *interleaved buck converter* and consists of multiple bucks working in parallel with different phases. The input voltage, around $400\,V$, is stepped down to $24\,V$ and $500\,W$ of power. A part from not be designed for low power application, the circuit shows again a capacitive voltage divider at the input side to reduce the stresses over subsequent components and then blocking capacitors (C_A and C_B) for uniform current sharing between the four phases. This topology has too many components and so it can not be used as a starting point for future implementations, but gives hints on the possibility to extend the duty cycle of a converter with an interleaved buck solution.

Another interesting solution is the one in [10]. This topology combines a buck power factor correction (PFC) circuit and a step down converter. The good property is that PFC and buck converter shares a single switch, this helps reducing the components' number. The integration of two buck cells reduces the voltage stresses over components of the proper buck cell. The switch has to handle only the real buck current and an high step down can be accomplished. This circuit has been designed

for a large output power, around $100\,W$, for an output voltage of $19\,V$ and an input voltage similar to the one required in this case.
In [14] there is a solution similar to the one proposed in [13], where the pre-charging problem of the capacitors is considered. A snubber circuit is used to bring the voltages across capacitive voltage divider to proper values, during the start-up phase. This topology was only simulated in Simulink and not tested. The design is meant for a large output power ($200\,W$), an output voltage of $22\,V$ and should be translated to lower power values.
The last topology seen is the one in [11], this is a synchronous buck converter with Tapped-Inductor, also called TI-buck converter. The proposed circuit is reported in figure 2.5 and has a little change, with respect to typical TI converters, which allow to reduce the voltage stresses over the switches. The proposed circuit works at $2\,MHz$,

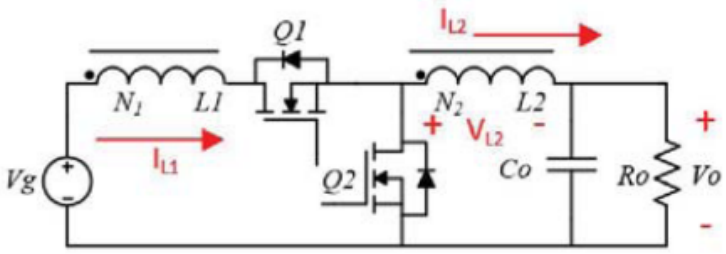


Figure 2.5: tapped-inductor ZVS buck converter in [11]

so the magnetic components area is highly reduced and this is confirmed also from the resultant prototype area. The input voltage ($24 \div 48\,V$) is reduced down to $5\,V$, so the input does not correspond to the target one, but the device works in ZVS and so switching losses are minimal.
There is also the *switched capacitor* power supply world, in which the energy transfer is associated to a capacitor connected, for a period of time, at the input port and then, for the remaining time period, to the output side. An example is the one in [15], which can obtain very high efficiency (over $90\,\%$), when used for stepping down the input voltage (around $\approx 40\,V$) to $3.3\,V$ at the output and with a current of $\approx 40\,mA$. This circuit has been fully integrated and the resulting area is equal to $4.53\,mm^2$, for this reason and for the rated output power the switched capacitor converter could be taken into account as a possible solution, if the high AC input voltage problem is solved.

2.3 Reduced number of components solutions

There are different ways to step down the high sinusoidal voltage coming from the main, among them it is possible to recall: $50\,Hz$ transformers, which are quite large and heavy, resistive divider, affected by power dissipation and too high dependence on load, and finally capacitive divider, with almost null power losses but with limited output current.

An input transformer would be the easiest solution, a proper turn ratio design allows to obtain an isolated sinusoidal voltage with reduced peak-to-peak value, that can be easily rectified on the secondary side. As already said, those kind of device has a large volume and weight, for these reasons can not be considered as a possible solution to the voltage reduction problem.

Resistive divider are a very bad choice in this application, because resistors dissipate powers and, since it is desirable to obtain a good efficiency, every possible loss should be avoided. Without mentioning, that resistors are not able to keep a constant voltage when the load requires more current.

The last possibility is a capacitive divider, capacitors are reactive elements and for this reason dissipate ideally no power. In this kind of circuit a capacitor is connected to the mains and in series with other components; [16], [17], [18], [19] and [20] call them *transformer-less power supply*, providing formulae and explanations on how to properly design this kind of circuit. [17] and [16] relay onto a zener diode to regulate the output voltage, but this can cause some power issues. Let's consider the circuit in [16], reported also in figure 2.6. Those circuits works well when the output required

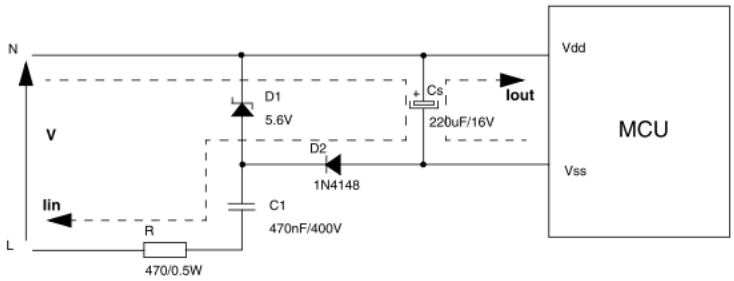


Figure 2.6: capacitive power supply from [16]

current I_{out} is almost equal to the input one I_{in}, but when the load demands less

current the voltage onto the C_s capacitor increases and so the zener diode becomes reversed biased. In this way the output voltage is regulated, but the zener dissipates power in accordance with equation (2.1), as reported in [19].

$$P_{Zener,max} = V_{Zener} I_{out,max} \tag{2.1}$$

Let's suppose to require a voltage onto C_S of $48\,V$ and the load demands around $30\,mA$, if the loads goes in idle state, this current flows in the zener and dissipated power is $P_{Zener,max} = 1.44\,W$. It is also important to consider safety, when dealing with high voltage AC lines, as reported in [21], and so the capacitor in series with the line should be a safety approved one.

2.4 Conclusions

In this chapter different solutions from various sources have been considered; application notes, datasheets, product selection guides and articles have been used for the scope. The result of this research is a set of possible topologies, like the buck, buck-boost, flyback and transformer-less power supplies, but also hints, obtained from articles, on what are the possible techniques to reduce the losses and improve the efficiency. In the next chapter, the found topologies will be discussed and, after having acquired a good knowledge on them, the one which matches better the requirements will be selected as a starting point for further discussions.

CHAPTER 3

Found solutions' working principle

As seen in the previous section, suggested topologies have been derived from *product selector guides* and *application notes*, now it is time to better understand them in order to select the proper one, depending on the required specifications. Textbooks, like [22] and [23], starts the description of switching power topologies from the **buck** one, also for this thesis the latter topology will be the starting point. This is done for two main reasons: first of all the buck topology is quite easy to be studied and then it is the basis for both the buck-boost one and its derived isolated topology, the flyback.

3.1 Buck

The buck topology, reported in figure 3.1, is obtained combining, in a proper way, a switch, a diode, an inductor and a capacitor. Some assumptions are needed in order

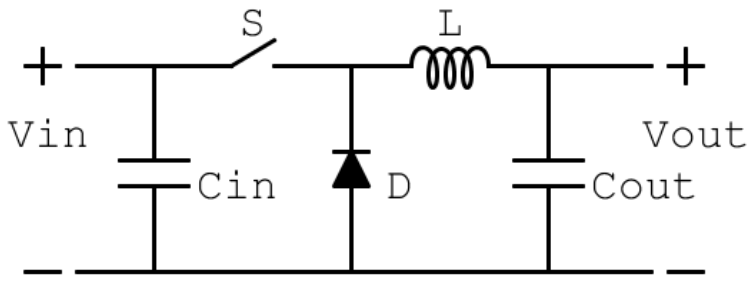


Figure 3.1: buck topology

to make a simple analysis:

ideal switches diodes and switches are ideal, which means that they do not show a voltage drop when conducting current;

switching time far smaller than time constants any electrical quantities with exponential or sinusoidal behaviour can not be appreciated and, so, it can supposed to be linear;

constant output voltage even if the output voltage has a ripple over-imposed it can be neglected;

cyclostationary condition all the cycles repeat in the same way, so a steady state condition is present.

Let's suppose to have a square wave signal controlling the switch switching activity and call it $q(t)$. Two quantities can describe $q(t)$: the *switching period* and the *duty cycle*. An example of a $q(t)$ function is reported in figure 3.2, the switching period is $T_{SW} = f_{SW}^{-1}$ and the duty cycle is the amount of time for which the function is positive:

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T_{SW}} \tag{3.1}$$

The circuit works into two different conditions, described below, which are deter-

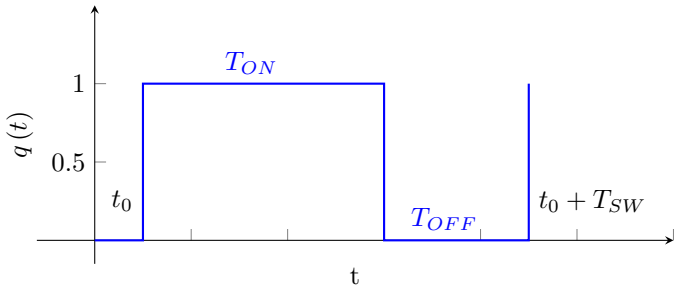


Figure 3.2: $q(t)$ switching controlling signal

mined by the switch state and the inductor current behaviour is also represented in figure 3.3, since it is the most characteristic quantity of the converter:

closed switch here the switch is conducting and the diode is reversed biased, the only path for the current will be through the inductor. From previous assumptions, the voltage drop across the inductor is $V_{IN} - V_{OUT}$, this is constant and

so the current will rise linearly, as derived from the constitutive equation of an inductor (3.2):

$$v_L = L \cdot \frac{di_L(t)}{dt} \tag{3.2}$$

open switch now the switch is not conducting, the diode provides a path for the inductor current, this is a state variable and so it will continue to flow in the same direction as it was flowing before opening the switch. The diode is also called **free-wheeling diode**, under the hypothesis of ideal switches and constant output voltage, the voltage drop onto the diode is zero and so the inductor voltage is opposite in sign with respect to the previous phase. This means that now the inductor current is decreasing with a different slope.

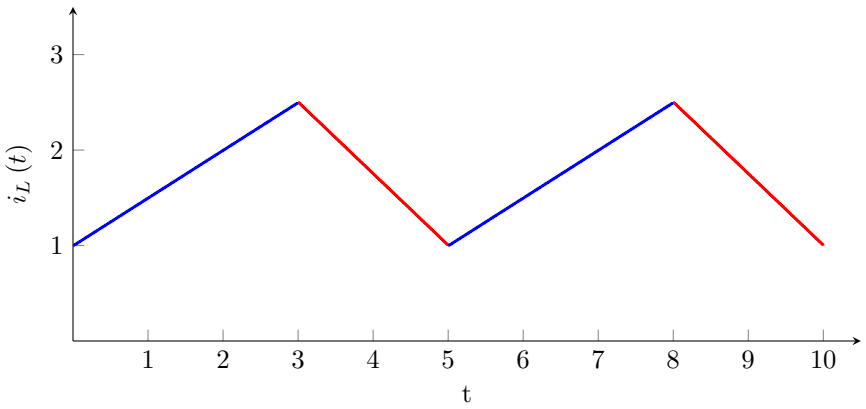


Figure 3.3: $i_L(t)$ example

The cyclostationary condition has also been used, since the inductor current has the same value at the beginning of each cycle; this means that equations (3.3) and (3.4) can be written:

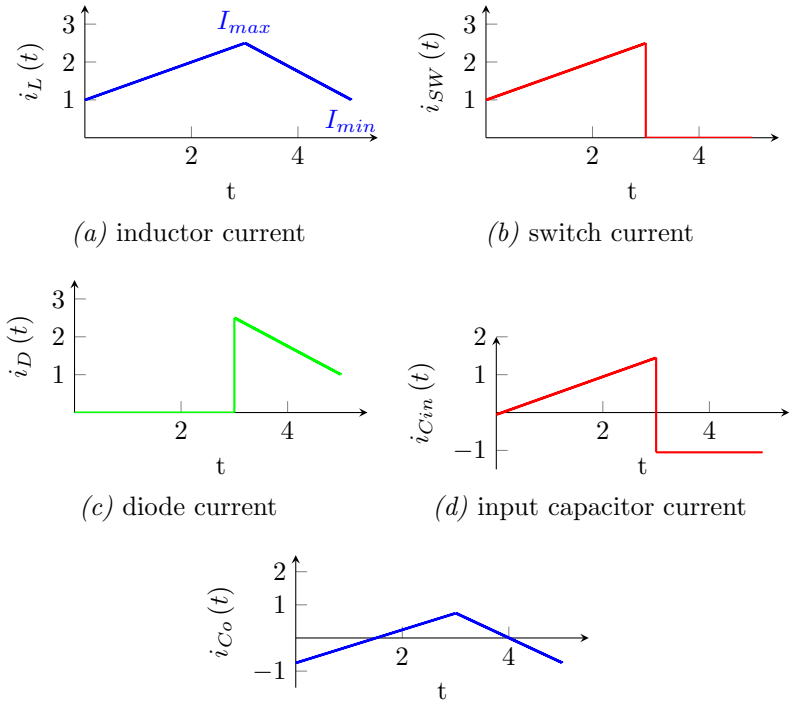
$$\frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} + \frac{-V_{OUT}}{L} \cdot T_{OFF} = 0 \tag{3.3}$$

$$(V_{IN} - V_{OUT}) \cdot T_{ON} - V_{OUT} \cdot T_{OFF} = 0$$

$$\frac{V_{OUT}}{V_{IN}} = M = \frac{T_{ON}}{T_{ON} + T_{OFF}} = D \tag{3.4}$$

Once understood the inductor current behaviour, any other one can be easily derived and are reported in figure 3.4: the switch current is the inductor one during the on phase of the switch itself, the diode one is equal to the inductor current with the

switch open, capacitive currents are obtained remembering that capacitors have no DC current. The hypothesis of real switches can be easily removed, then the voltage



(a) inductor current

(b) switch current

(c) diode current

(d) input capacitor current

(e) output capacitor current

Figure 3.4: buck waveforms

drops onto diode and switch should be considered, but the final result is still obtained as done in (3.4).

The next step is finding the components' stresses, since they will be used to design the SMPS itself and understand which is the most suitable topology for the required design. The inductor current is the first quantity that has to be analysed, in particular the interest is focused on maximum and minimum values, considering the inductor current behaviour in figure 3.4a, the following equation can be written:

$$I_{max} - I_{min} = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF} = \frac{V_{OUT}}{L} \cdot \frac{(1-D)}{f_{SW}} \tag{3.5}$$

Another equation is needed to solve for I_{max} and I_{min}, this is obtained considering a mean value KCL at the output node of figure 3.1, where a resistive load R_L is

supposed to be connected:

$$I_{OUT} = \frac{V_{OUT}}{R_L} = \frac{I_{max} + I_{min}}{2} \cdot D + \frac{I_{max} + I_{min}}{2} \cdot (1 - D) = \frac{I_{max} + I_{min}}{2} \tag{3.6}$$

Solving (3.5) and (3.6), maximum and minimum current expressions are obtained:

$$I_{max} = \frac{V_{OUT}}{R_L} + \frac{V_{OUT} \cdot (1 - D)}{2 \cdot L \cdot f_{SW}} \tag{3.7}$$

$$I_{min} = \frac{V_{OUT}}{R_L} - \frac{V_{OUT} \cdot (1 - D)}{2 \cdot L \cdot f_{SW}} \tag{3.8}$$

Now the ideal switch can be substituted with a real device, typically an MOS. This one will be characterized by maximum drain-source voltage, maximum current, average current and RMS current. Starting from figure 3.4b, the average switch current can be found remembering that the input capacitor has no DC component:

$$\overline{i_{SW}} = I_{IN} = \frac{I_{max} + I_{min}}{2} \cdot D = \frac{V_{OUT}}{R_L} \cdot D = I_{OUT} \cdot D \tag{3.9}$$

The RMS current computation is not practical, if definition is directly used. The formula is reported for the sake of completeness in (3.10). To get a good result with less effort an approximation is needed: the current can be considered constant, where it is defined, and its value will be equal to the mean of variation.

$$I_{RMS} = \sqrt{\frac{1}{T} \cdot \int_0^T i\,(t)^2 \; dt} \tag{3.10}$$

To better understand the previous statement, figure 3.5 can be considered. In this way, $i\,(t)^2$ is a constant value and can be moved outside of the integral and square root, what remains is only the duty cycle:

$$I_{SW_{RMS}} \approx \frac{I_{max} + I_{min}}{2} \cdot \sqrt{D} = I_{OUT} \cdot \sqrt{D} \tag{3.11}$$

The maximum drain-source voltage is obtained when the switch is open or when the diode is conducting and the maximum current, important to define the R_{DS_ON} of the MOS, is equal to the maximum inductor one.
The diode's electrical quantities can be derived with similar considerations; equations

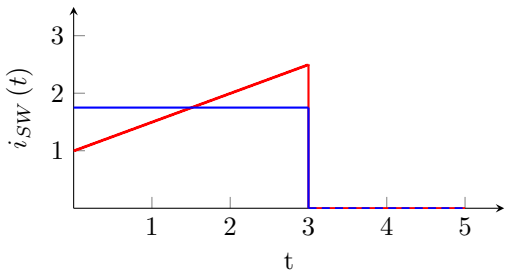


Figure 3.5: $i_{SW}(t)$ approximation for RMS computation

(3.12) and (3.13) are obtained:

$$\overline{i_D} = I_D = \frac{I_{max} + I_{min}}{2} \cdot (1 - D) = I_{OUT} \cdot (1 - D) \tag{3.12}$$

$$I_{D_{RMS}} \approx I_{OUT} \cdot \sqrt{(1 - D)} \tag{3.13}$$

The input capacitor highly stressed from the current standpoint of view. This can be better appreciated considering the current peak to peak variations in 3.4d, moreover the voltage across its nodes can be quite high since it is at the input side of the converter. To obtain the current stresses, the **quadratic KCL** rule should be used; this one is derived considering the fact that each current can be written ad a sum of a DC component and an AC one:

$$\begin{aligned}
i(t) &= i_{TOT}(t) = I_{DC} + i_{AC}(t) \\
I_{TOT_{RMS}} &= \sqrt{\frac{1}{T} \cdot \int_0^T i_{TOT}(t)^2 \, dt} \\
I^2_{TOT_{RMS}} &= \frac{1}{T} \cdot \int_0^T [I_{DC} + i_{AC}(t)]^2 \, dt \\
&= \frac{1}{T} \cdot \int_0^T I^2_{DC} \, dt + \frac{2}{T} \cdot \int_0^T I_{DC} i_{AC} \, dt + \frac{1}{T} \cdot \int_0^T i_{AC}(t)^2 \, dt \\
I^2_{TOT_{RMS}} &= I^2_{DC_{RMS}} + I^2_{AC_{RMS}}
\end{aligned} \tag{3.14}$$

Now, given the buck topology in figure 3.1, the $I^2_{TOT_{RMS}}$ is equal to $I^2_{SW_{RMS}}$ and the $I^2_{DC_{RMS}}$ is $\overline{i_{SW}}^2 = I^2_{IN}$. The input capacitor RMS current is obtained:

$$\begin{aligned} I^2_{Cin_{RMS}} &= \left(I_{OUT} \cdot \sqrt{D}\right)^2 - (I_{OUT} \cdot D)^2 \\ &= I^2_{OUT} \cdot \left(D - D^2\right) \\ I_{Cin_{RMS}} &= I_{OUT} \cdot \sqrt{D - D^2} \end{aligned} \tag{3.15}$$

It can be shown that the RMS inductor current has the expression reported in (3.17), this is obtained remembering the formula of the area underneath a parabola and using the quadratic KCL at the output node.

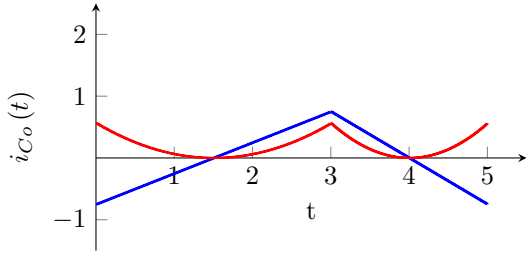


Figure 3.6: inductor RMS current calculation

$$A_1 = \frac{Peak \cdot Base}{3} \tag{3.16}$$

$$I^2_{L_{RMS}} = I^2_{OUT_{RMS}} + I^2_{Cout_{RMS}}$$

$$I^2_{L_{RMS}} = I^2_{OUT} + \frac{\Delta i^2_L}{12} \approx I^2_{OUT} \tag{3.17}$$

In (3.17) the approximation holds, since the Δi_L is typically very small and negligible if compared to the output current value. The discarded quantity represent in fact the RMS current across the output capacitor. It can be seen that, in a buck, this is not so stressed ad the input one.

$$I_{Co_{RMS}} = \frac{\Delta i_L}{\sqrt{12}} \tag{3.18}$$

$$\Delta i_L = I_{max} - I_{min} = \frac{V_{OUT}}{L}\frac{(1-D)}{f_{SW}} \tag{3.19}$$

The discussion on stresses over the various components, forming the buck, ends here and what remains is to understand the two possible ways a buck can work: *continuous*

conduction mode (**CCM**), *discontinuous conduction mode* (**DCM**) and a *boundary conduction mode* (BCM). Those two can be distinguished by the inductor current waveform, as reported in figure 3.7. Using the minimum inductor current expression

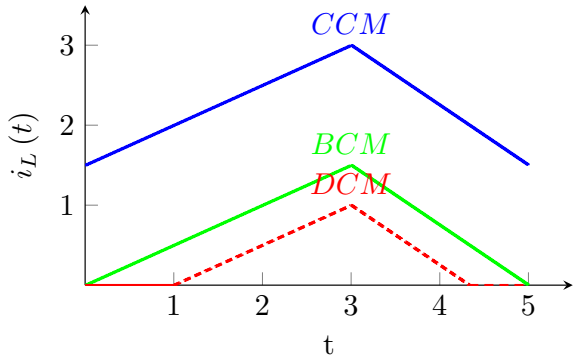


Figure 3.7: how inductor current behaviour defines the mode of operation of a buck converter

(3.8) and imposing it to be equal to zero, it is possible to obtain an expression for the inductance, this one will represent the boundary value between CCM and DCM working conditions:

$$L_{BCM} = \frac{(1-D)\cdot R_L}{2\cdot f_{SW}} \tag{3.20}$$

here R_L represent an ideal resistive load and the values of R_L and D, that have to be used in the formula changes if we want to guarantee CCM or DCM. For example in CCM an L larger than the L_{BCM} one should be provided, so D_{min} and $R_{L_{max}}$ will be used.

There is still something that can be noticed here and that is useful for further design choices: the buck topology, thanks to the position of the switch in series with the input source, is able to handle *short circuit* at the output, by simply keeping the switch open until this condition is expired. This is important, otherwise the inductor current would continue to increase, at a certain point the magnetic core saturates and the inductor will simply act like a piece of wire, after this point the switch could fail.

The *soft start* and the *in-rush current* are strictly connected to the previous concept; the in-rush current occurs at first start of the circuit, because all the capacitances, input, output and parasitics ones, are not charged. In order to avoid having too much current at start up in a very short amount of time, the soft start behaviour should be

implemented: the duty cycle of the switch will be slowly increased in order to limit the input current and, in this way, the output voltage will reach the final value in a safe way.

Inductor	Switch	Diode	C_{in}	C_{out}
$I_L = I_{OUT}$	$I_{SW} = I_{OUT} \cdot D$	$I_D = I_{OUT} \cdot (1-D) \approx I_{OUT}$	$i_{C_{inRMS}} = I_{OUT} \cdot \sqrt{D - D^2}$	$i_{C_{outRMS}} = \frac{\Delta i_L}{\sqrt{12}}$
$\Delta i_L = \frac{V_{OUT} \cdot (1-D)}{L \cdot f_{SW}}$	$i_{SW_{pk}} = i_{L_{pk}}$	$i_{D_{pk}} = i_{L_{pk}}$		$\Delta v_{C_{out}} = \Delta i_L \cdot ESR$
$i_{L_{pk}} = I_L + \frac{\Delta i_L}{2}$	$i_{SW_{RMS}} = I_{OUT} \cdot \sqrt{D}$	$i_{D_{RMS}} = I_{OUT} \cdot \sqrt{1-D}$		
$i_{L_{RMS}} \approx I_L$	$R_{DS_ON}(hot) = \frac{V_{SW}}{i_{SW_{pk}}}$	$V_{D_{max}}$		
	BV_{DSS}			

Table 3.1: buck formulae for components stresses

3.2 Boost

The boost converter is the next topology that has to be discussed and, since the description is not so different from buck, the explanation will be shortened. In particular the circuit will be reported, the overall behaviour, together with the waveforms, described and a table with the component stresses formulae presented.
A boost, as the one reported in figure 3.8, is a topology able to "boost" the output voltage with respect to the input one, its behaviour can be described considering the circuit into two possible operative conditions defined by the switch condition:

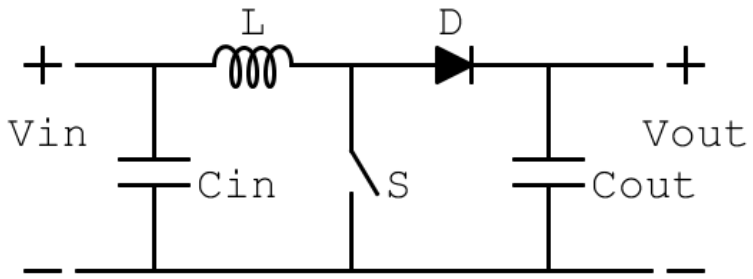


Figure 3.8: boost topology

closed switch in this condition the inductor is connected to the V_{IN} on one side and to GND to the other, thanks to the closed switch. In this phase, the inductor starts to store energy and its current increases until the T_{ON} time lasts, at the same time the diode is reversed biased and the output capacitor holds the previously stored charge.

open switch now the switch is open and inductor current, that was flowing from left to right, continue to flow in the same direction, but with a decreasing slope, since now the voltage drop is $V_{IN} - V_{OUT} < 0$. The diode provides a path for this current and energy will be moved from the inductor to the output capacitor. This phase last for a time T_{OFF} and at the end of a cycle the inductor current value is equal to the starting one, since cyclostationary condition holds.

A first consideration is related to the fact that in this topology the output capacitor is mandatory, otherwise the circuit will not be able to hold the output voltage. Now,

imposing the cyclostationary condition, the main equation for a boost can be derived:

$$\begin{aligned} &\frac{V_{IN}}{L} \cdot T_{ON} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{OFF} \\ &\frac{V_{OUT}}{V_{IN}} = M = \frac{T_{ON} + T_{OFF}}{T_{OFF}} = \frac{1}{1 - D} \end{aligned} \tag{3.21}$$

Here it should be noticed that the M factor will tend to infinity for $D \to 1$. This is something unreasonable, in fact the maximum value is limited to $M_{MAX} = 3 \div 5$ and can not be even reached, otherwise the efficiency will be affected. A possible real behaviour of the M_D is represented in figure 3.9. Notice how the slope of the red curve change sign and this can cause some problems once the device is inserted in a feedback loop. The waveforms of the boost are quite similar to the one of the

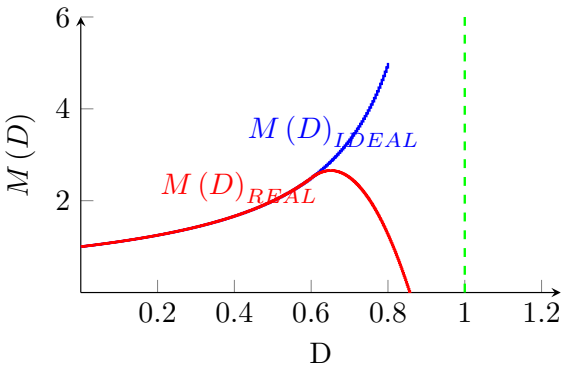
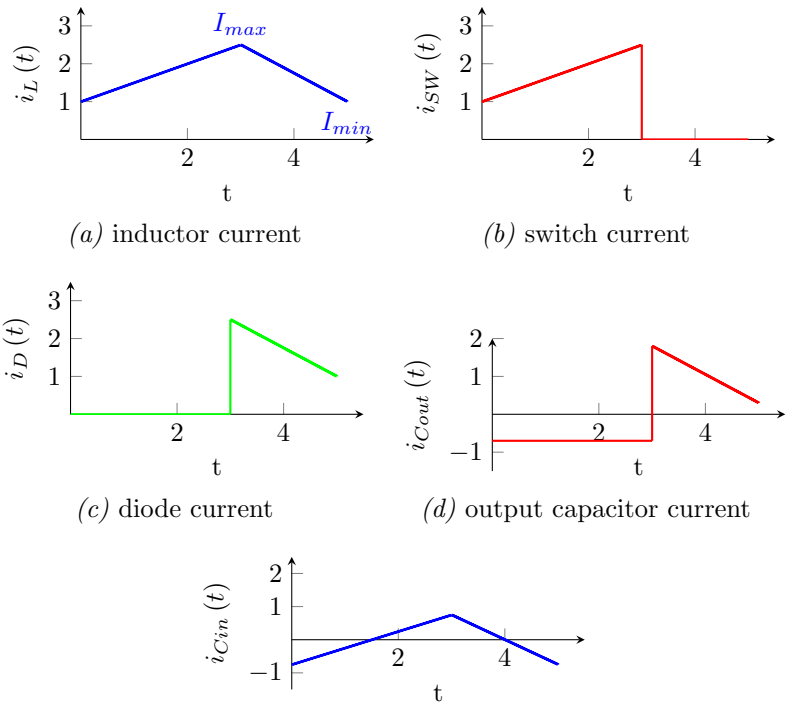


Figure 3.9: $M(D)$ ideal and real behaviour

buck and can be derived starting from the usual waveform of the inductor current, for the sake of completeness they are reported in figure 3.10. Here the most evident difference, with respect to the buck waveforms, are the higher stresses over the output capacitor, because it has an higher RMS current. Also for the boost is possible to derive an expression for the BCM inductance, the procedure is still the same: identify the minimum inductor current equation and impose it to be zero. The final result is reported in (3.22):

$$L_{BCM} = \frac{R_L \cdot D \cdot (1 - D)^2}{2 \cdot f_{SW}} \tag{3.22}$$

Soft start, in-rush current protection and short circuit are features not available for a boost converter, since the switch is not in series with the input port. Boost has another important characteristic, related to the inductor position: *surge/spike over-*



(a) inductor current

(b) switch current

(c) diode current

(d) output capacitor current

(e) input capacitor current

Figure 3.10: boost waveforms

voltage protection. Now, since the inductor is in series with the input port, any voltage variation will be firstly applied to it, for this reason the current will not change fast. Moving to the components stresses, the passages used to obtain the following expressions, in table 3.2, have been overlooked on purpose, because they are easy to obtain following the same procedure as in the buck case.

Inductor	Switch	Diode	C_{in}	C_{out}
$I_L = I_{IN}$	$I_{SW} = I_{IN} \cdot D$	$I_D = I_{IN} \cdot (1-D) = I_{OUT}$	$i_{C_{inRMS}} = \frac{\Delta i_L}{\sqrt{12}}$	$i_{C_{outRMS}} = I_{OUT} \cdot \sqrt{\frac{D}{1-D}}$
$\Delta i_L = \frac{V_{OUT} \cdot D \cdot (1-D)}{L \cdot f_{SW}}$	$i_{SW_{pk}} = i_{L_{pk}}$	$i_{D_{pk}} = i_{L_{pk}}$		$\Delta v_{C_{out}} = \Delta i_L \cdot ESR$
$i_{L_{pk}} = I_L + \frac{\Delta i_L}{2}$	$i_{SW_{RMS}} = I_{IN} \cdot \sqrt{D}$	$i_{D_{RMS}} = I_{IN} \cdot \sqrt{1-D}$		
$i_{L_{RMS}} \approx I_L$	$R_{DS\_ON}(hot) = \frac{V_{SW}}{i_{SW_{pk}}}$	$V_{D_{max}}$		
	BV_{DSS}			

Table 3.2: boost formulae for components stresses

3.3 Buck-Boost

The buck-boost converter, as the one reported in figure 3.11, can be seen as the combination of a buck at the input port and a boost at the output, for this reason it will combine benefits and disadvantages of both of them. Also in this case the analysis will be reduced to a brief presentation of the circuit, a description of its waveforms and a final table reporting useful formulae.
A buck-boost converter is a device able to reduce or increase the output voltage level, depending on the value of the duty cycle; the circuit behaviour can be described considering the same hypothesis made so far and the two possible switch conditions.

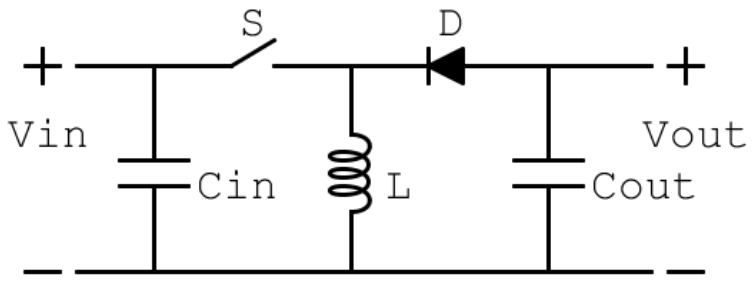


Figure 3.11: buck-boost topology

closed switch in this condition the inductor is connected between V_{IN} and GND. A current starts to flow through the inductor and in this phase the energy is stored, this lasts until the T_{ON} time is expired. The diode is not conducting during this phase, because the current can not flow from left to right.

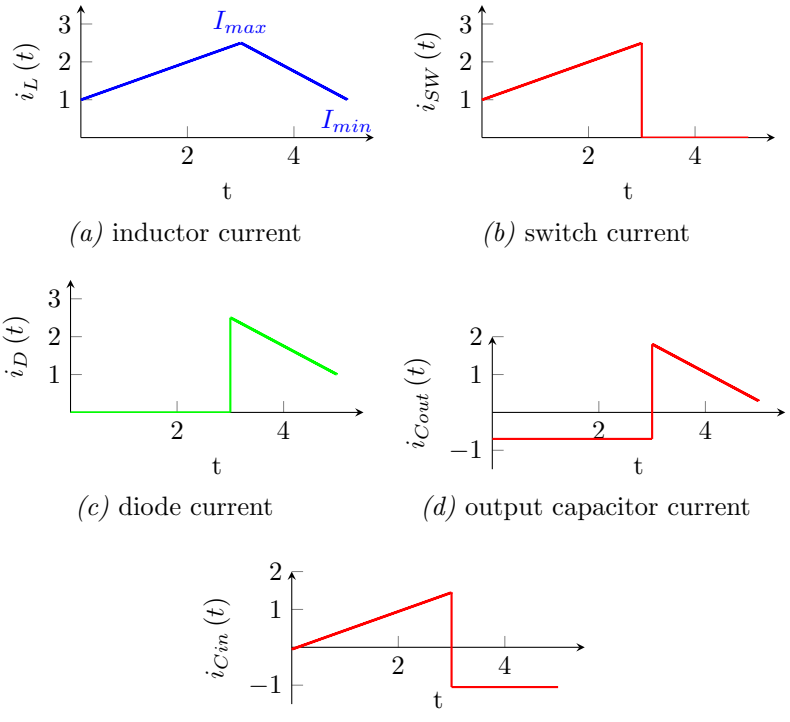
open switch in this phase the inductor is connected to the output voltage by the diode, because the inductor current, which is a state variable, has to continue to flow in the same direction it was flowing before the switch has been opened. This interval lasts for T_{OFF} and the voltage applied onto the inductor is $-V_{OUT}$. The V_{OUT} has a negative sign, with respect to figure 3.11 sign convention.

This circuit will have both input and output capacitor highly stressed; another characteristic is the *indirect* conversion, because there is not a direct passage of power

from input to output, as it was for buck and boost converters, which are called *direct* converters. Also in this case, imposing the cyclostationary condition, the main equation of a buck-boost can be obtained; notice that here CCM is the supposed working condition, even if a buck-boost works typically in DCM.

$$\begin{aligned} \frac{V_{IN}}{L} D &= -\frac{V_{OUT}}{L} (1 - D) \\ M &= \frac{V_{OUT}}{V_{IN}} = \frac{D}{D - 1} \end{aligned} \tag{3.23}$$

Since D is less than 1, the ratio in (3.23) has a negative sign and this confirms the fact that the output voltage has an opposite sign with respect to the given convention. Also for this topology all the waveforms are reported in figure 3.12, here there is a graphical proof of the stresses over input and output capacitor. Also for the buck-



(a) inductor current

(b) switch current

(c) diode current

(d) output capacitor current

(e) input capacitor current

Figure 3.12: CCM buck-boost waveforms

boost is possible to derive an expression for the BCM inductance and the procedure is still the same: identify the minimum inductor current equation and impose it to

be zero. The final result is reported in equation (3.24).

$$L_{BCM} = \frac{R_L \left(1 - D\right)^2}{2 f_{SW}} \tag{3.24}$$

As already said, this circuit works mainly in DCM condition and so a better description of this behaviour should be given. Starting from the inductor current, it is known that, during the whole switching period, there is an interval (T_3) with zero inductor current value. This behaviour is shown in figure 3.13. An equivalent expression, like

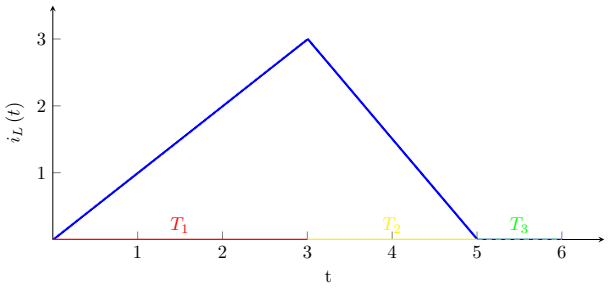


Figure 3.13: DCM inductor current behaviour

the (3.23), is needed for the DCM case, in this case the approach used is focused on the power standpoint of view. The first assumption is to consider a lossless device ($P_{IN} = P_{OUT}$), then it is possible to write the input power as the stored inductor peak energy per second and the output one as the power delivered to a resistive load (R_L). The peak energy can be computed from the typical inductor energy formula ($E_L = 0.5 \cdot L \cdot i^2$), substituting the current with peak value, this will represent the

amount of energy deliverable to the load per cycle.

$$E_{L_{pk}} = \frac{1}{2} \cdot L \cdot I_{pk}^2 \tag{3.25}$$

$$I_{pk} = \frac{V_{IN}}{L} \cdot T_1$$

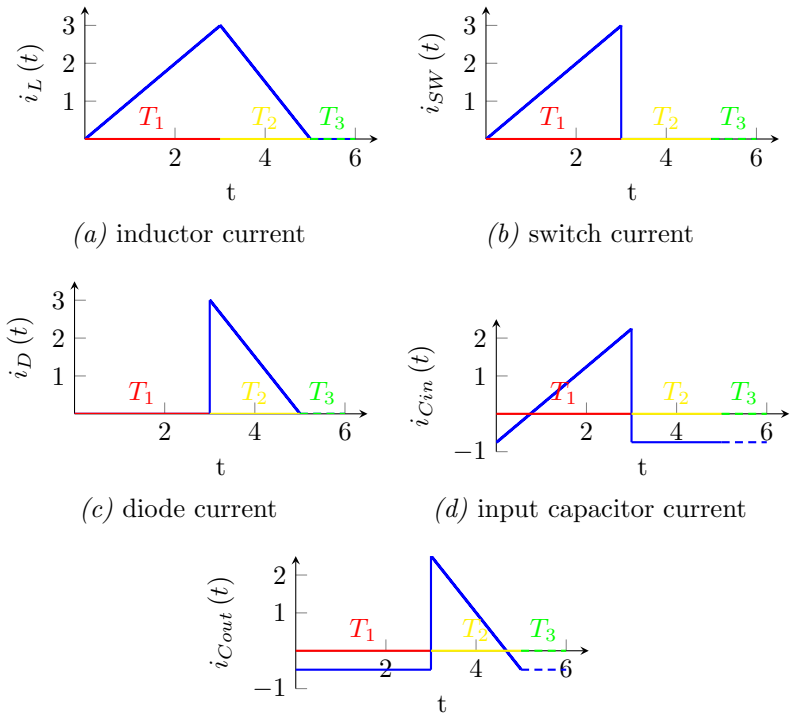
$$P_{IN} = E_{L_{pk}} \cdot f_{SW} = \frac{1}{2} \cdot L \frac{V_{IN}^2 \cdot T_1^2}{L^2} \cdot f_{SW} = \frac{V_{IN}^2 \cdot D^2}{2 \cdot L \cdot f_{SW}} \tag{3.26}$$

$$P_{IN} = \frac{V_{IN}^2 \cdot D^2}{2 \cdot L \cdot f_{SW}} = \frac{V_{OUT}^2}{R_L} = P_{OUT}$$

$$\frac{V_{OUT}^2}{V_{IN}^2} = M^2 = \frac{R_L \cdot D^2}{2 \cdot L \cdot f_{SW}}$$

$$\frac{V_{OUT}}{V_{IN}} = M = -D \cdot \sqrt{\frac{R_L}{2 \cdot L \cdot f_{SW}}} \tag{3.27}$$

Notice that, in the last equation (3.27), the minus sign comes from the opposite sign convention of the V_{OUT} with respect to figure 3.11. For the sake of completeness the DCM waveforms are reported in figure 3.14. Notice how the buck-boost topology



(a) inductor current *(b)* switch current

(c) diode current *(d)* input capacitor current

(e) output capacitor current

Figure 3.14: DCM buck-boost waveforms

shows the same feature of a buck, in terms of *soft-start*, *in-rush current* and *short*

circuit protection.

The passages, to obtain the expressions in table 3.3, have been overlooked on purpose, because they are easy to obtain following the same procedure of the buck case. It should be noticed that there are two duty cycles in the formulae and they are defined as reported in the following equations:

$$D_1 = \frac{T_1}{T_{SW}} = \frac{T_1}{T_1 + T_2 + T_3}$$
$$D_2 = \frac{T_2}{T_{SW}} = \frac{T_2}{T_1 + T_2 + T_3}$$

Inductor	Switch	Diode	C_{in}	C_{out}
$\Delta i_L = \frac{V_{IN} \cdot D_1}{L \cdot f_{SW}}$	$I_{SW} = \frac{i_{L_{pk}}}{2} \cdot D_1$	$I_D = \frac{i_{L_{pk}}}{2} \cdot D_2 = -\frac{V_{OUT}}{R_L}$	$i_{C_{inRMS}} = i_{L_{pk}} \cdot \sqrt{\frac{D_1}{3} - \frac{D_1^2}{4}}$	$i_{C_{outRMS}} = i_{L_{pk}} \cdot \sqrt{\frac{D_2}{3} - \frac{D_2^2}{4}}$
$i_{L_{pk}} = \Delta i_L$	$i_{SW_{pk}} = i_{L_{pk}}$	$i_{D_{pk}} = i_{L_{pk}}$		$\Delta v_{C_{out}} = \Delta i_L \cdot ESR$
$I_L = \frac{\Delta i_L}{2} \cdot (D_1 + D_2)$	$i_{SW_{RMS}} = i_{L_{pk}} \cdot \sqrt{\frac{D_1}{3}}$	$i_{D_{RMS}} = i_{L_{pk}} \cdot \sqrt{\frac{D_2}{3}}$		
$i_{L_{RMS}} =$	$R_{DS_{ON}}(hot) = \frac{V_{SW}}{i_{SW_{pk}}}$	$V_{D_{max}}$		
	BV_{DSS}			

Table 3.3: buck-boost formulae for components stresses

3.4 Flyback

The flyback converter is the buck-boost derived topology, once the inductor is substituted with a transformer or, more precisely, with *coupled inductors*. The use of such a magnetic component will add both advantages and disadvantages, which are summarized in table 3.4. The flyback is one of the most used topology all over the

Advantages	Disadvantages
Galvanic isolation, which is required whenever a direct current path between input and output has to be avoided, like for safety reason.	*Higher cost* and *larger area* are obvious consequences.
No limitation on voltage ratio (V_{OUT}/V_{IN}), the number of turns of the transformer windings is used to increase the design possibility.	*Frequency limitations* are related to the parasitic inductances, that comes for free when adding a transformer, and only few hundreds of kHz can be reached.
Extra degree of freedom related to the turn ratio (N_S/N_P). It can be seen that, changing the turn ratio, is possible to move stresses over the components.	*No DC* transformation.
Multiple outputs are much more easy to realize.	*Cross-regulation* is quite a problem in multiple outputs, in particular it is easy to control well one output, but the others can experience fluctuations.

Table 3.4: advantages and disadvantages of flyback converter

world and it is used for chargers, auxiliary supplies, notebook power supply and many other fields of application. A large numbers of papers, books, application notes, online resources and other counterparts cover this subject, as done in [24], [25] and [26]. A first rough scheme of a flyback converter is reported in figure 3.15, here the structure of a buck-boost can be easily recognized. Lets start by describing the circuit behaviour during the two possible switch working conditions:

closed switch in this phase energy is stored into the transformer and the current continues to rise until the switch is closed (T_1). The output diode will prevent the current to flow and so the output capacitor has to keep the output

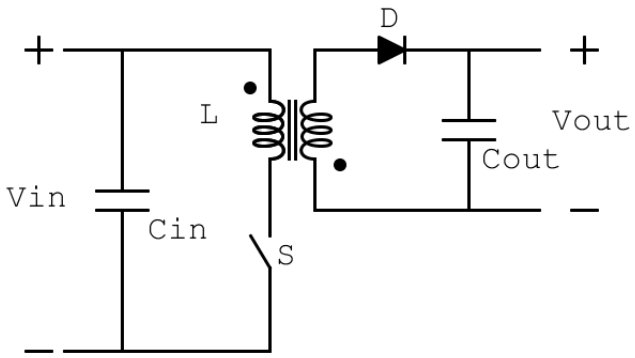


Figure 3.15: basic flyback topology

voltage constant, just like it was for a buck-boost. The only difference now is the possibility to have a positive output, thanks to the dot convention of the transformer.

open switch as it was for the buck-boost, during this phase, the energy previously stored in the transformer is moved to the output.

The flyback can work in three different ways and their typical waveforms are reported in figure 3.17. There is a very good table in [24, p.5], that should be kept in mind when selecting the proper mode of operation and highlights pros and cons of the three modes. A brief description of them is:

- the **CCM** is not really used, but basically is like having a current across the transformer never equal to zero, as it was for a buck in the same working condition;
- the **DCM** is quite common and consists in having, within a switching period, a complete transfer of energy to the output and a third time interval (T_3) is used to completely reset the transformer energy. During T_3 the drain voltage starts to resonate, since there is the leakage inductance of the transformer and parasitic capacitance associated to the drain node;
- the **BCM** is very similar to the DCM one, but the T_3 interval is basically removed and the switch is turned on with the lowest possible voltage, reducing the turn-on switching losses. This is obtained by letting the drain node resonate

and turning on the switch at the first valley, for this reason this mode is called *valley switching*, *transition mode* (**TM**) or *quasi-resonant*.

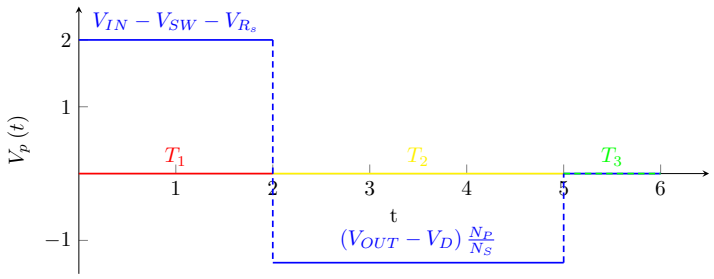


Figure 3.16: $V_p\,(t)$ voltage

The first thing to understand is the **flux runaway problem**, look at [23, p.133-139] for more details: every magnetic material has a flux limit and, once reached, the magnetic property of the device are lost, this means that the current can increase without control causing obvious problem to the external circuit. To limit this, the primary side voltage (V_p), which is the one onto the left side winding, should have a mean value equal to zero, otherwise within few cycles the energy stored in the magnetic will saturate. The behaviour of the primary side voltage is reported in figure 3.16 and the null mean value can be written as reported in equation (3.28):

$$(V_{IN} - V_{SW} - V_{R_s}) \cdot D_1 = (V_{OUT} - V_D) \cdot \frac{N_P}{N_S} \cdot D2 \tag{3.28}$$

$$\frac{N_P}{N_S} = \frac{(V_{IN} - V_{SW} - V_{R_s}) \cdot D_1}{(V_{OUT} - V_D) \cdot D_2} \tag{3.29}$$

$$\frac{N_P}{N_S} = \frac{(V_{IN_{min}} - V_{SW} - V_{R_s}) \cdot D_{1_{MAX}}}{(V_{OUT} - V_D) \cdot D_{2_{MAX}}}$$

In the previous formulae, the following mathematical notations are used: V_{SW} is the drain-source voltage drop during conduction, V_{R_s} is the current sensing resistor voltage drop (if used) and V_D is the output rectifier voltage drop. In the last equation, the *turn ratio* is defined for a known condition, which is the one that occurs when the input voltage is at minimum value and, as a consequence, the duty cycle should be the maximum available, remembering that the flyback typically works in DCM and so $D_1 + D_2 < 1$.

There is one last passage that has to be covered: the definition of the primary side inductance L_p. This one should have a value suitable to store enough energy within

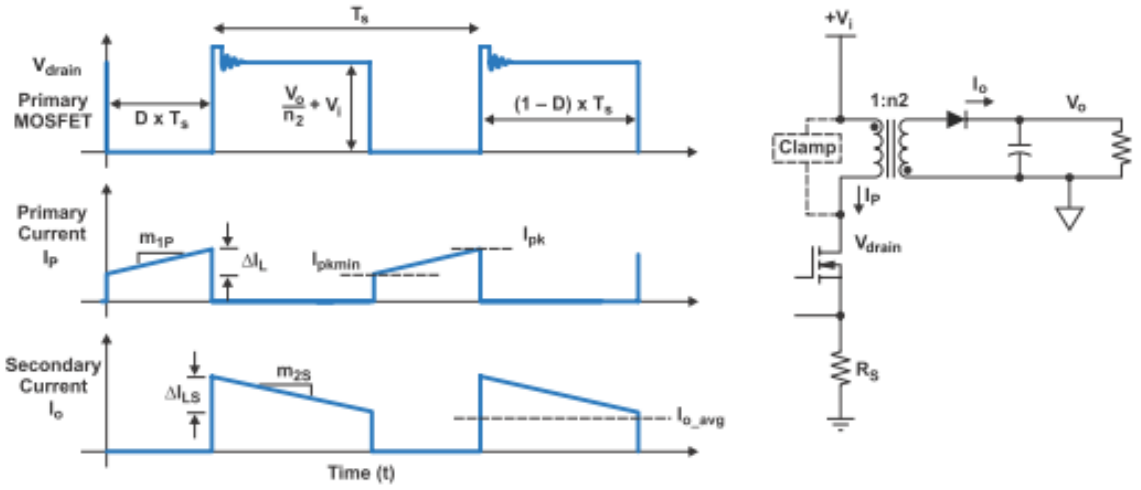


Fig. 1. Operation in CCM.

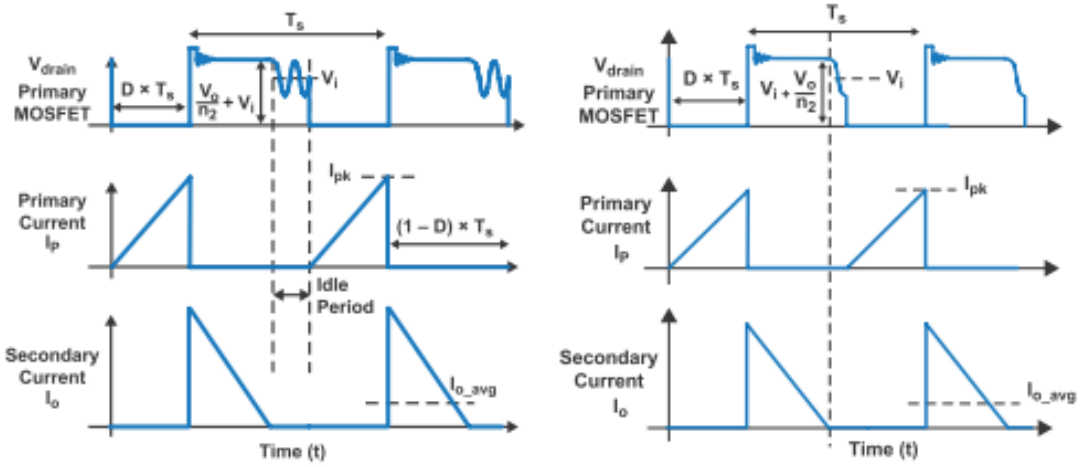


Fig. 2. Operation in DCM (left) and TM (right).

Figure 3.17: CCM, DCM and BCM operating flyback mode taken from [24]

one on time. The passages are similar to the one of the buck-boost, in particular,

starting from equation (3.25) it is possible to write what follows.

$$E_{L_p} = \frac{1}{2} \cdot L_p \cdot I_{pk}^2$$

$$I_{pk} = \frac{V_p \cdot D_1}{L_p \cdot f_{SW}}$$

$$P_p = E_{L_p} \cdot f_{SW}$$

$$P_p = \frac{P_s}{\eta_{MAG}}$$

$$P_s = \sum_{i=1}^{m} I_{Oi} \cdot (V_{Oi} + V_{Di}) \tag{3.30}$$

$$\frac{(V_{IN_{min}} - V_{SW} - V_{R_s})^2 \cdot D_1^2}{2 \cdot L_p \cdot f_{SW}^2} \cdot f_{SW} \cdot \eta_{MAG} = \sum_{i=1}^{m} I_{Oi} \cdot (V_{Oi} + V_{Di})$$

$$L_p = \frac{1}{2} \cdot \frac{(V_{IN_{min}} - V_{SW} - V_{R_s})^2 \cdot D_1^2}{f_{SW}} \cdot \eta_{MAG} \tag{3.31}$$

Here the E_{L_p} is the peak energy in the primary inductance, then the P_s is the secondary side power and can be related to the primary one, considering the magnetic efficiency η_{MAG} ranging from 80% to 95%. The P_s is expressed as the sum of the powers at all secondary windings, so finally the L_p expression is obtained in (3.31), where the minimum input voltage condition is used.
The stresses over the components can be derived, as already done, and are similar to the one obtained for the buck-boost case in table 3.3, for this reason they are skipped here.

3.5 Transformerless power supplies

The transformerless power supplies are of two main types: resistive and capacitive. The first type is not suggested, because a resistor will dissipate too much power and then resistive voltage division is affected by input fluctuations and load current variations. For these reasons, the considered solution is a *capacitive power supply* (**CPS**), an example is reported in figure 3.18 and taken from [19]. This kind of circuit is based onto energy stored in the series connected capacitor with the mains

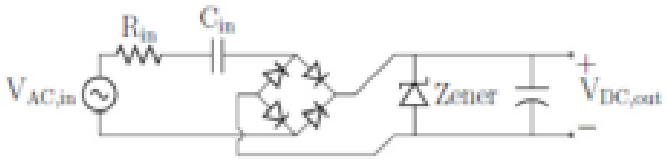


Figure 3.18: capacitive full-wave rectification (pre-zener) taken from [19]

(C_{in}). Let's recall the typical constitutive relation of a capacitor,

$$i_{C_{in}} \approx C_{in} \cdot \frac{dV_{C_{in}}(t)}{dt} \tag{3.32}$$

from equation (3.32), the first thing to notice is that the higher the capacitance the higher the output current will be.
In [19], a formula for the maximum output current available with this kind of circuit is given and it is reported in (3.33).

$$i_{out,max,fullwave} = \frac{\frac{2}{\pi} \cdot V_{pk} - V_{zener}}{\sqrt{R_{in}^2 + \left(\frac{1}{2 \cdot \pi \cdot f \cdot C_{in}}\right)^2}} \tag{3.33}$$

In (3.33), V_{pk} is the peak value of the input voltage, V_{zener} is the breakdown voltage of the zener diode or also the $V_{DC,out}$, R_1 is the inrush current limiting resistor and f represents the line frequency. These kind of devices can deliver up to some tens of milliampere.
The capacitor will limit the input current with its reactance, which is very high at line frequency. The R_{in} is used to limit the inrush current at start-up, when the device is connected to the mains and all the capacitors are discharged. The full wave rectifier will rectify the input sinusoidal waveform, whenever its value is higher than the Zener voltage, the Zener will start to conduct and the output voltage will be regulated in this way. The output capacitor should be quite large, in order to maintain the output voltage.

This circuit is very simple, requires only few components and provides a regulated output. The main problem is the zener power dissipation and the voltage stress the C_{in} is supposed to support. In particular this kind of capacitor should be rated for a

voltage higher than the AC one ($> 220\,V$ and so $400\,V$), but their cost is quite high. It is also important to remember that the Zener voltage should be selected taking into account the voltage drop caused by conducting diodes.

3.6 Conclusions

In this chapter various SMPS's topologies have been considered, among with capacitive power supplies. Then buck, buck-boost and flyback have been described in detail and, finally, the capacitive power supply solution is explained.
Among all those previously described topologies, the ones that will be considered in the next sections is the buck one. Buck-boost and flyback will not be considered, because the buck is easier and simpler to control. Capacitive power supply is also a possibility that should be considered, due to its simplicity and its efficiency will be compared with the one obtained with other circuits.

CHAPTER 4

Ideal buck design

This chapter will provide some useful details on how to properly design a buck converter. The first step will be an ideal buck design, the input/output capacitors will be designed and the switching/conduction losses will be described. Secondly, the designed converter will be simulated.
Non-ideal components, like real switch and diode, will be considered and also their effect onto the converter's duty cycle. Finally, the circuit will be simulated again and the efficiency computed in various load conditions.

4.1 Ideal buck design

The ideal buck circuit design will be used as a reference point for future comparisons and will provide a good guide for subsequent design. The design of this circuit will follow the formulae shown in section 3.1 and table 3.1.
Let's recall the requirements, reported in table 4.1. From them it is possible to

Specifications	**Value**
Input Voltage	$220\,V$ $50\,Hz$ for the EU market and $120\,V$ $60\,Hz$ for the US one
Output Voltage	$V_O = 3.3\,V$
Output Current	$I_{O_{MAX}} = 100\,mA$

Table 4.1: buck converter requirements

compute the maximum (4.1) and minimum (4.2) duty cycle values, that should be

used to obtain the V_{out} with different V_{AC} conditions.

$$D_{MAX} = \frac{V_{out}}{\sqrt{2} \cdot V_{AC\_min}} \tag{4.1}$$

$$D_{min} = \frac{V_{out}}{\sqrt{2} \cdot V_{AC\_max}} \tag{4.2}$$

Considering a $\pm 10\,\%$ AC voltage fluctuation in the two required input voltage cases, the table 4.2 is obtained and reports the minimum, maximum and nominal duty cycle. The proper *switching frequency* (f_{SW}) selection should be carried out considering the

Nominal voltage	Voltage	Duty cycle
$120\,V$	$V_{AC\_min} = 108\,V$	$D_{MAX} = 0.0216$
	$V_{AC\_nom} = 120\,V$	$D_{nom} = 0.0194$
	$V_{AC\_MAX} = 132\,V$	$D_{min} = 0.0177$
$220\,V$	$V_{AC\_min} = 208\,V$	$D_{MAX} = 0.0112$
	$V_{AC\_nom} = 220\,V$	$D_{nom} = 0.0106$
	$V_{AC\_MAX} = 132\,V$	$D_{min} = 0.0096$

Table 4.2: duty cycle values for the two different required markets

minimum on time (t_{ON_MIN}), of chosen device, and it should guarantee the D_{min}. Let's suppose to have a switching frequency $f_{SW} = 30\,kHz$, then the minimum on time will be:

$$t_{ON\_MIN} = D_{min}/f_{SW} = \frac{0.0096}{30 \cdot 10^3\,Hz} = 320\,ns$$

The buck converter can work in **CCM** or **BCM** and the inductor value can be obtained from (3.20):

$$L_{CCM\_220V} \geq L_{BCM\_MAX} = \frac{3.3\,V\,(1 - 0.0106)}{2 \cdot 30\,kHz \cdot 10\,mA} = 5.44\,mH$$

$$L_{CCM\_220V} = 6.8\,mH$$

$$L_{CCM\_120V} \geq L_{BCM\_MAX} = \frac{3.3\,V\,(1 - 0.0194)}{2 \cdot 30\,kHz \cdot 10\,mA} = 5.39\,mH$$

$$L_{CCM\_120V} = 6.8\,mH$$

here the minimum output current is supposed to be $10\,\%$ of the maximum and $6.8\,mH$ is the chosen value for the inductance, both for $V_{AC} = 120\,V$ and $V_{AC} = 220\,V$. For the sake of completeness, the values for **DCM** condition are reported below, but in

this chapter the **CCM** is the main focus.

$$L_{DCM\_220V} \leq L_{BCM\_min} = \frac{3.3\,V\,(1-0.0112)}{2\cdot 30\,kHz\cdot 100\,mA} = 543.8\,\mu H \tag{4.3}$$
$$L_{DCM\_220V} = 330\,\mu H$$
$$L_{DCM\_120V} \leq L_{BCM\_min} = \frac{3.3\,V\,(1-0.0216)}{2\cdot 30\,kHz\cdot 100\,mA} = 538.1\,\mu H \tag{4.4}$$
$$L_{DCM\_120V} = 330\,\mu H$$

In this phase is also important to compute the output and input capacitance values: the computation is quite straightforward and follows the capacitance definition. A capacitance is defined as the ratio between the stored charge variation and the voltage one. Let's start form the output capacitor, the stored charge variation can be computed by looking at the current waveform in figure 3.4e, which is again reported here in figure 4.1. Considering the ΔQ as the charge variation associated to the area

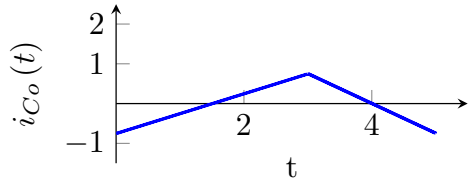


Figure 4.1: buck output capacitor's waveform

underneath the positive part of the waveform and ΔV_{out} as the required output voltage ripple, which is in this particular case not given and so a free choice, the output capacitance can be simply computed as reported in equation (4.5).

$$C_{out} = \frac{\frac{\Delta i_L}{2}\frac{T_{SW}}{2}}{2\cdot\Delta V_{out}} \tag{4.5}$$
$$C_{out} \approx 404\,nF$$

The ΔV_{out} has been chosen to be 5 % of the nominal V_{out} and for the Δi_L equation (3.19) has been used. From ΔV_{out} and Δi_L, also the maximum output capacitor ESR can be computed. For the input capacitance, the reasoning is very similar, but it is not possible to use the waveform like in figure 3.4d, because this capacitor "lives" into two time domains: one is related to the switching activity and the other is connected to the line frequency. It is still possible to use the capacitance definition and compute

the charge variation as the average input current by the ΔT, representing the time interval for which the charge should be maintained with a required ΔV_{in}.

$$\begin{aligned} C_{in} &= \frac{\Delta Q_{in}}{\Delta V_{in}} \\ \Delta Q_{in} &= I_{in} \cdot \Delta T \\ I_{in} &= \frac{P_{in}}{V_{in}} \\ P_{in} &= \frac{P_{out}}{\eta} \\ C_{in} &= \frac{P_{out} \Delta T}{\eta V_{in} \Delta V_{in}} \end{aligned} \tag{4.6}$$

In equation 4.6 the η is the converter's efficiency, supposed to be at least 70 %, and ΔT is the *hold-up time*, or the time for which the capacitor is required to maintain the voltage. This time can be considered to be the maximum time period, so the minimum line frequency, then the maximum C_{in} is obtained considering also the maximum output power and the minimum input voltage. The ΔV_{in} is chosen arbitrarily to be around $20\,V$.

$$\begin{aligned} C_{in\_220V} &\geq \frac{0.33\,W \cdot (50\,Hz)^{-1}}{0.7 \cdot \sqrt{2} \cdot 220\,V \cdot 20\,V} = 1.53\,\mu F \\ C_{in\_120V} &\geq \frac{0.33\,W \cdot (60\,Hz)^{-1}}{0.7 \cdot \sqrt{2} \cdot 120\,V \cdot 20\,V} = 2.34\,\mu F \end{aligned}$$

Once found this value, it is possible to pick up a capacitor with a nominal value larger than this, in order to guarantee that the condition on the ΔV_{in} is verified. Now it is possible to fill the table 3.1, to obtain the components' stresses for a buck converter working in **CCM** condition and $V_{AC} = 220\,V$.

Inductor	Switch	Diode	C_{in}	C_{out}
$I_L = 100\,mA$	$I_{SW} \approx 1.1\,mA$	$I_D \geq 100\,mA$	$i_{C_{inRMS}} \geq 10\,mA$	$i_{C_{outRMS}} \geq 5\,mA$
$\Delta i_L = 16\,mA$	$i_{SW_{pk}} \geq 108\,mA$	$i_{D_{pk}} = 108\,mA$	$V_{C_{in}} \geq 400\,V$	$V_{C_{out}} \geq 3.3\,V$
$i_{L_{pk}} \geq 108\,mA$	$i_{SW_{RMS}} \approx 10.3\,mA$	-	$C_{in} \geq 1.53\,\mu F$	$C_{out} \geq 404\,nF$
$i_{L_{RMS}} \approx 100\,mA$	$R_{DS_{ON}}(hot) \leq 9\,\Omega$	$V_{D_{max}} \geq 400\,V$	-	$ESR \leq 10\,\Omega$
-	$BV_{DSS} \geq 400\,V$	-	-	-

Table 4.3: table containing the ideal buck components' values and stresses, computed for a nominal input voltage of $220\,V$ and **CCM** condition

4.2 Power losses

It is important, before going into the simulation's phase, to have an idea on what are the main contributes to the losses and from them evaluate an approximative efficiency. In an ideal buck, like the one designed so far, there are two main source of losses: the diode, when it is conducting, and the MOSFET, when it is switching and when it is in conduction.
The diode losses can be computed as a simple product between its voltage drop and the average conducted current, since the duty cycle is particularly small will not be wrong to consider this current as the output one, as done in 4.7.

$$P_{diode} = V_D \cdot I_D \approx V_D \cdot I_{out} \tag{4.7}$$

The switch losses are divided into two kind: one is when the switch is conducting, acting like a resistor ($R_{DS_{ON}}(hot)$), and the other is related to the switching activity.

$$P_{SW\_cond} = r_{ds_{ON}}(hot) \cdot i^2_{SW_{RMS}} \tag{4.8}$$

$$P_{SW\_switching} = \frac{1}{2} \cdot f_{SW} \left(V_{before} \cdot I_{after} \cdot t_{on} + V_{after} \cdot I_{before} \cdot t_{off}\right) \tag{4.9}$$

While the 4.8 is straightforward, the 4.9 needs a little bit of explanation. Consider the figure 4.2, it represents the approximated behaviour of the current and voltage across the switch, during the switching action. The red curve represents the voltage across the switch, during the switching action, and the blue one the current. Their

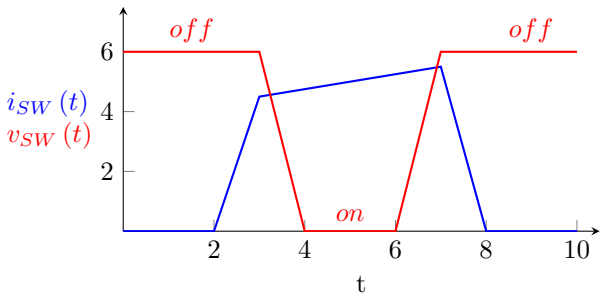


Figure 4.2: approximated behaviour of switch quantities

product is the instantaneous power, which ideally should have a triangular shape, when the two previous curves are both different from zero. Now the area of these triangular shapes is the energy lost during each cycle, due to switching action, so, multiplying it by the frequency, it is possible to obtain the power losses related to commutations.

$$P_{SW\_switching} = E \cdot f_{SW} = \left(\frac{1}{2} \cdot V_{before} \cdot I_{after} \cdot t_{on} + \frac{1}{2} \cdot V_{after} \cdot I_{before} \cdot t_{off}\right) \cdot f_{SW} \quad (4.10)$$

In 4.10 it is possible to associate to the V_{before}, the value of the switch's voltage before closing it, to the I_{after}, the switch's current after closing the same, and the same reasoning is applied to V_{after} and I_{before}.
Let's suppose to have the switch working with the maximum input voltage, the $t_{on} = t_{off} = 50\,ns$, $V_{before} = V_{after} = \left(220\sqrt{2} + 0.7\right)\,V = 311.8\,V$, $I_{after} = i_L - \Delta i_L/2 = 92\,mA$ and $I_{before} = i_{L_{pk}} = 108\,mA$. Equation 4.9 will give the following switching losses and conduction losses are also obtained, using 4.8 and values in table 4.3.

$$P_{SW\_switching} \approx 47\,mW$$
$$P_{SW\_cond} \approx 955\,\mu W$$

Diode's losses are computed considering a voltage drop of $0.7\,V$ and they are equal to $P_{diode} \approx 70\,mW$. From these values an approximated value of the expected efficiency will be the one reported in equation 4.11.

$$\eta_{\%} = \frac{P_{out}}{P_{out} + P_{diode} + P_{SW\_switching} + P_{SW\_cond}} \approx 73.8\,\% \quad (4.11)$$

Notice that this is only the ideal efficiency in maximum V_{AC} condition; if the input voltage is lowered, it is possible to expect an increase of the efficiency, since the switch

is forced to commute at a lower voltage and so the $P_{SW\_switching}$ contribute will be reduced. Also the diode losses are lowered if the input voltage is reduced, because the average diode current depends on $(1 - D)$ and D increases if V_{in} lowers.

4.3 Simulations

At this point it is important to verify if the design is correct and this will be done with the *LTSpiceXVII* simulator. Simulations are meant to exploit the effects of non-ideal components, which will affect the response of the buck converter; some of them are the voltage drop onto the rectifying input diode, the one onto the free-wheeling diode or the voltage drop onto the switch, during conduction. All of the previous mentioned quantities become less important once a feedback loop is added. This will control the output voltage, regulating the duty cycle of the switch.

4.3.1 Ideal buck

In order to carry on a simulation, the schematic, reported in figure 4.3, has been realized. There are few things that should be noticed:

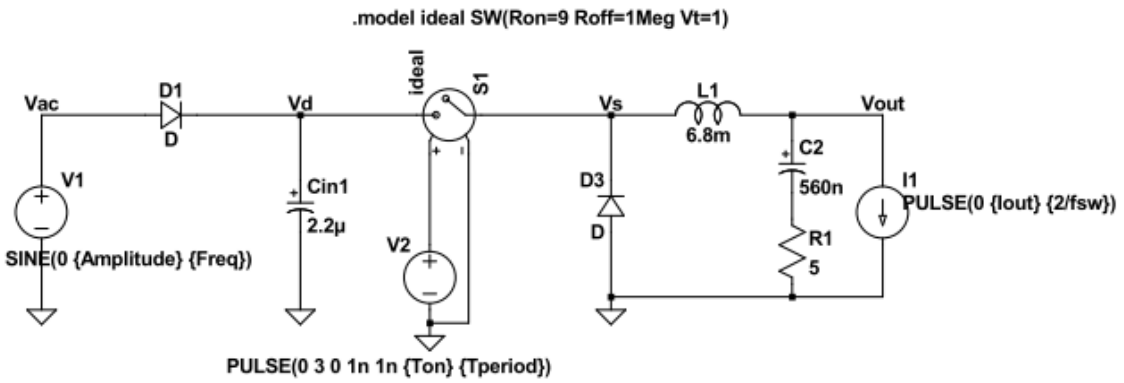


Figure 4.3: ideal buck schematic for LTSpiceXVII simulation

rectifier is a single wave one and this solution is chosen to reduce the Bill Of Material (BOM), with respect to a full wave rectifier, and to reduce the power losses, since in this way there is only one diode conducting at a time;

ideal switch this component should mimic the behaviour of the designed switch, for this reason the model's values are the ones from table 4.3;

diodes the used diodes, at this stage, are all ideal;

output capacitor for this component the ESR value as been added manually and the chosen value is $ESR = 5\,\Omega$, which respects the given specifications.

The circuit should be simulated considering different cases:

case 1 $V_{AC} = 120\,V$, the nominal duty cycle $D_{nom} = 0.0194$ and a load current of $100\,mA$;

case 2 $V_{AC} = 120\,V$, the nominal duty cycle $D_{nom} = 0.0194$ and a load current of $10\,mA$;

case 3 $V_{AC} = 220\,V$, the nominal duty cycle $D_{nom} = 0.0106$ and a load current of $100\,mA$;

case 4 $V_{AC} = 220\,V$, the nominal duty cycle $D_{nom} = 0.0106$ and a load current of $10\,mA$;.

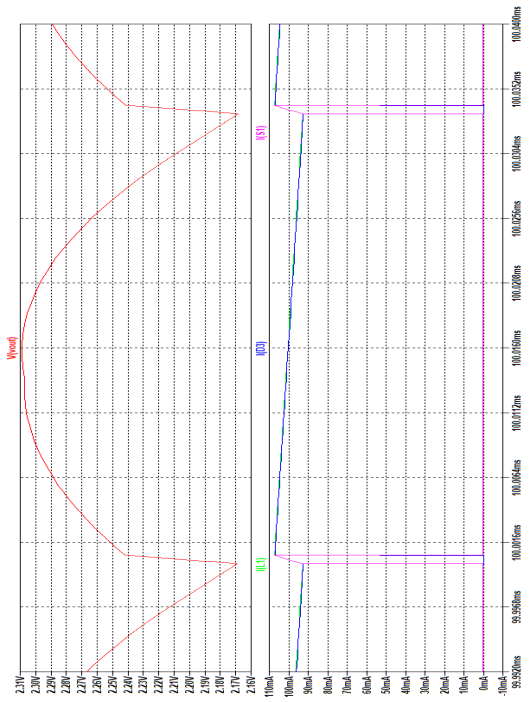
For each of those cases the most important electrical quantities will be reported and, in particular, the main focus will be onto the output voltage V_{out}, the inductor, diode and switch currents. In figure 4.4, it can be seen that the device is not working as required, in particular the output voltage does not met the requirements: both the average value and the ripple are missed. The first one is related to a wrong estimation of the duty cycle and this is caused by having supposed to have ideal switches, so no voltage drops. The second one, instead, is linked directly to the output capacitor: both the ESR and the C_{out} values should be reconsidered.
Nevertheless the device is correctly working in CCM as designed, in fact, the inductor current (green trace) never reach $0\,A$ even in the low current condition (case 2 and 4) and all the other waveforms are similar to the ones reported in figure 3.4. The behaviour of the output voltage (the red trace) is the one expected until the switch is conducting the current, then it shows an almost quadratic behaviour. This fact can

be linked to the output capacitor, what is known is the following:

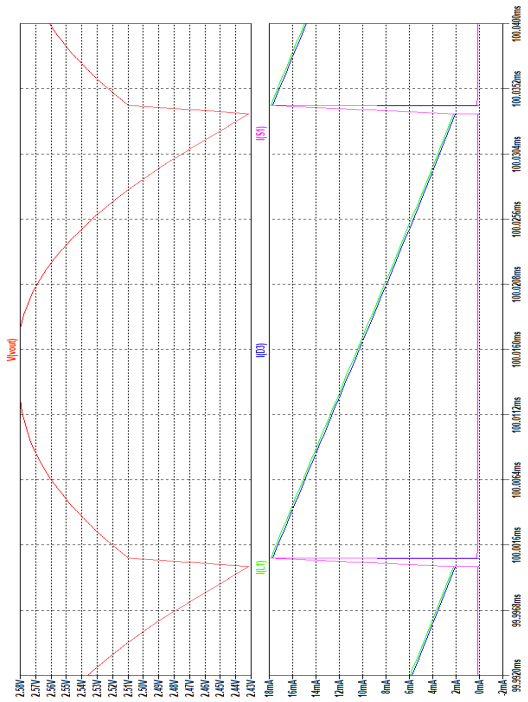
$$i_C = C \cdot \frac{dv_C}{dt} \tag{4.12}$$

$$v_C(t) = \frac{1}{C} \cdot \int_0^t i_C(t)\, dt \tag{4.13}$$

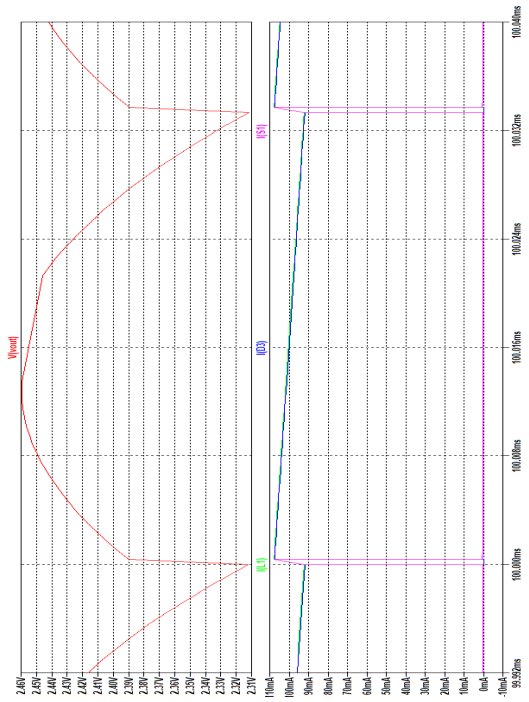
Now, since the output capacitor current is linearly changing with time, it is like the inductor one without the DC component, the voltage has a quadratic behaviour. To reduce this effect, the formula 4.13 suggests to increase the capacitance. Then the ESR could be further reduced to lower the voltage ripple and respect better the requirement of 5 % of V_{out}.



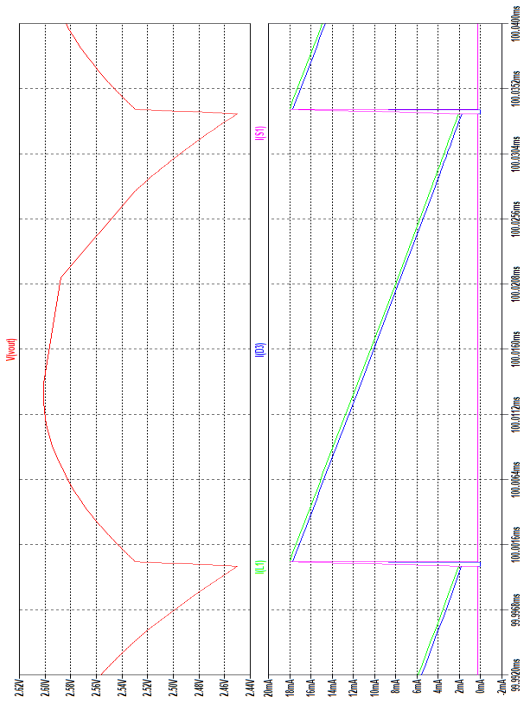
(a) $V_{AC} = 120\,V$, $D = 0.0194$ and $I_{load} = 100\,mA$



(b) $V_{AC} = 120\,V$, $D = 0.0194$ and $I_{load} = 10\,mA$



(c) $V_{AC} = 220\,V$, $D = 0.0106$ and $I_{load} = 100\,mA$



(d) $V_{AC} = 220\,V$, $D = 0.0106$ and $I_{load} = 10\,mA$

Figure 4.4: these are the four cases analysed to verify the correct behaviour of the buck in CCM condition, it can be seen that the output voltage does not met the requirements in any case and this can be related to a wrong estimation of the duty cycle, connected to the unconsidered real devices.

4.3.2 Considering real switch and diodes

It has been seen, in the previous section, that the device is not working as expected and this is related to the ideal switches assumption. If this hypothesis is removed, then the duty cycle formula 3.4 has to be modified. Again everything starts by considering the cyclostationary condition and so by imposing that the inductor current variation during T_{ON} is equal to the one during T_{OFF}.

$$\begin{aligned} \Delta i_{L1} &= \frac{V_L}{L} T_{ON} = \frac{V_{IN} - V_{SW} - V_{out}}{L} T_{ON} \\ \Delta i_{L2} &= \frac{V_L}{L} T_{OFF} = \frac{V_{out} + V_D}{L} T_{OFF} \\ \Delta i_{L1} &= \Delta i_{L2} \\ D &= \frac{V_{out} + V_D}{V_{IN} - V_{SW} + V_D} \end{aligned} \tag{4.14}$$

In 4.14, the V_{IN} is the input voltage or the one which is present at the drain terminal of the switch (the Vd one onto the schematic in figure 4.3). This one is the AC peak voltage reduced by the rectifier drop (V_{RECT}), which has been measured within the simulation and results to be $V_{RECT} = 0.64\,V$. The diode voltage drop can be supposed to be $V_D = 0.7\,V$ and the switch voltage drop is the one given by the product between $R_{DS_{ON}}(hot)$ and the $i_{SW_{pk}}$, which will result around $1.1\,V$. Using those values, both $120\,V$ and $220\,V$ duty cycle result to be:

$$D_{nom\_120V} = \frac{3.3 + 0.7}{120 \cdot \sqrt{2} - 0.64 - 1.1 + 0.7} = 0.0237 \tag{4.15}$$

$$D_{nom\_220V} = \frac{3.3 + 0.7}{220 \cdot \sqrt{2} - 0.64 - 1.1 + 0.7} = 0.0129 \tag{4.16}$$

notice that now the losses help the system working with a larger duty cycle. The circuit has been simulated again, in the same cases as before, but only after having changed the output capacitor's value. This one has been increased, according to equation 4.13, to $1\,\mu F$ and its ESR reduced down to $1\,\Omega$. In figure 4.5 it is possible to see the result of applied changes, in particular it should be noticed that, now, the output voltage is closer to the required one. There are still cases where the output voltage does not reach the specified $3.3\,V$, but this problem will be solved once a feedback loop will be added to the final circuit. If needed, a finer tuning

for the duty cycles can be done, but this is not something on which time should be spent, considering that this is not the final circuit. Something much more interesting is related to the output voltage ripple, which has been reduced, as can be seen by comparing figure 4.4 and 4.5, but has a behaviour far from the expected one, derived from theory. The output capacitor has been increased up to $33\,uF$, but a larger value can be still chosen, and this leads to two consequences:

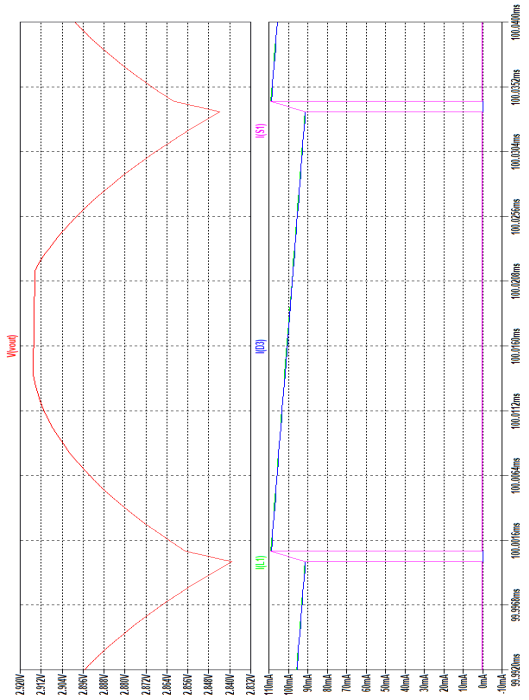
1) more ideal V_{out} waveform;

2) lower frequency resonances.

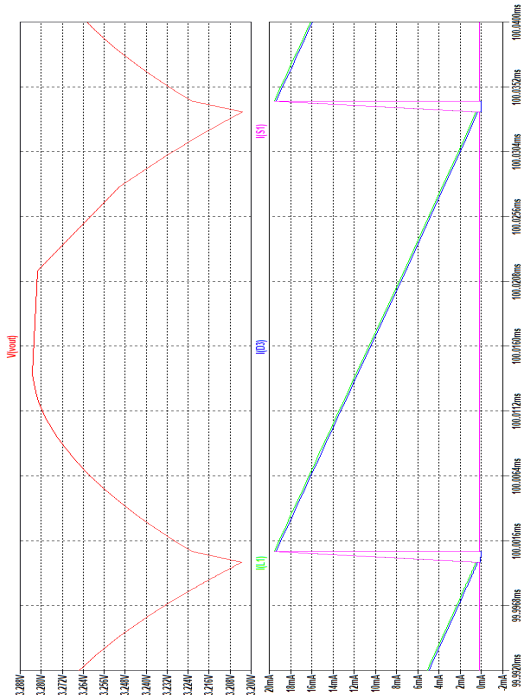
The output voltage waveform has been improved into two ways: the first is a reduction of the output voltage ripple, but not in the expected extent, and the second is a much more linear response. This can be seen in figure 4.6, where a $\Delta V_{out} \approx 130\,mV$ has been measured. As a consequence, it is possible to say that the output voltage ripple is linked to the output capacitance, but mainly to the capacitor ESR. The second improvement is related to the voltage behaviour with open switch. In the same figure as before, it is possible to see a much more linear response, which is related to equation 4.13, since now the output capacitor is so large that only the ESR will contribute to the output voltage ripple and the capacitive response can be neglected.
On the other hand, it is possible to see the low frequency resonance, by looking at the output voltage behaviour over at least a line period ($T_{LINE} = 1/f_{LINE} = 20\,ms$), as in figure 4.7, where also a bad line regulation can be seen. The output stage is like a second order LCR filter and, as it is well known, the resonant frequency is given by equation 4.17.

$$f_0 = \frac{1}{2\,\pi\,\sqrt{LC}} \tag{4.17}$$

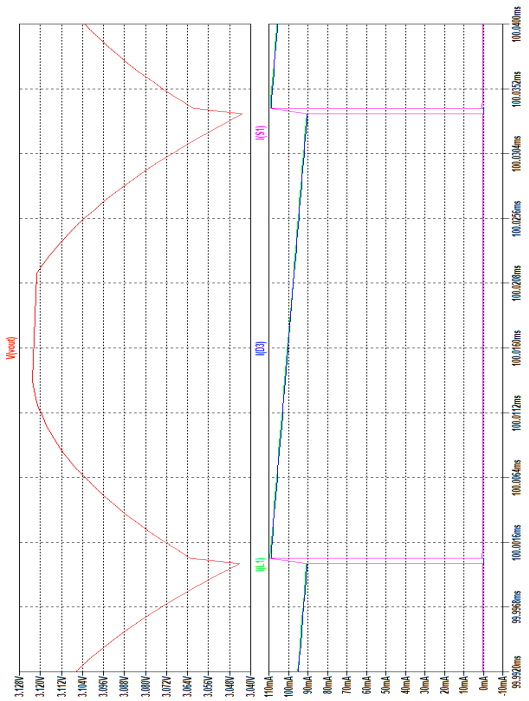
As a consequence, the output capacitor should not be increased too much, but it should also be remembered that the final circuit will have a feedback loop, controlling the output voltage: every time that the controlled quantity exceeds the limitation, then the feedback will change the duty cycle of the switch. This will solve both the low frequency resonance problem and the bad line regulation.



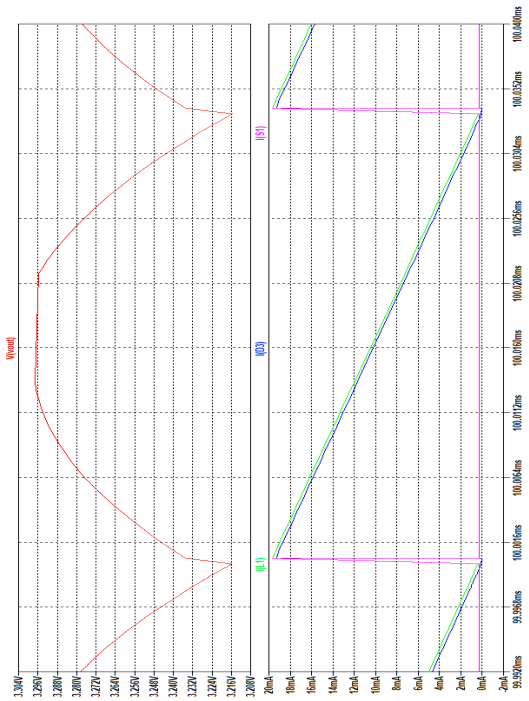
(a) $V_{AC} = 120\,V$, $D = 0.0237$ and $I_{load} = 100\,mA$



(b) $V_{AC} = 120\,V$, $D = 0.0237$ and $I_{load} = 10\,mA$



(c) $V_{AC} = 220\,V$, $D = 0.0129$ and $I_{load} = 100\,mA$



(d) $V_{AC} = 220\,V$, $D = 0.0129$ and $I_{load} = 10\,mA$

Figure 4.5: these are the four cases analysed to verify the correct behaviour of the buck in CCM condition, with $C_{out} = 1\,\mu F$. It can be seen that the output voltage does not met the requirements in all cases, so a finer duty cycle tuning should be done. The output voltage ripple is still out of requirements and, as a consequence, the output capacitor should be enlarged.

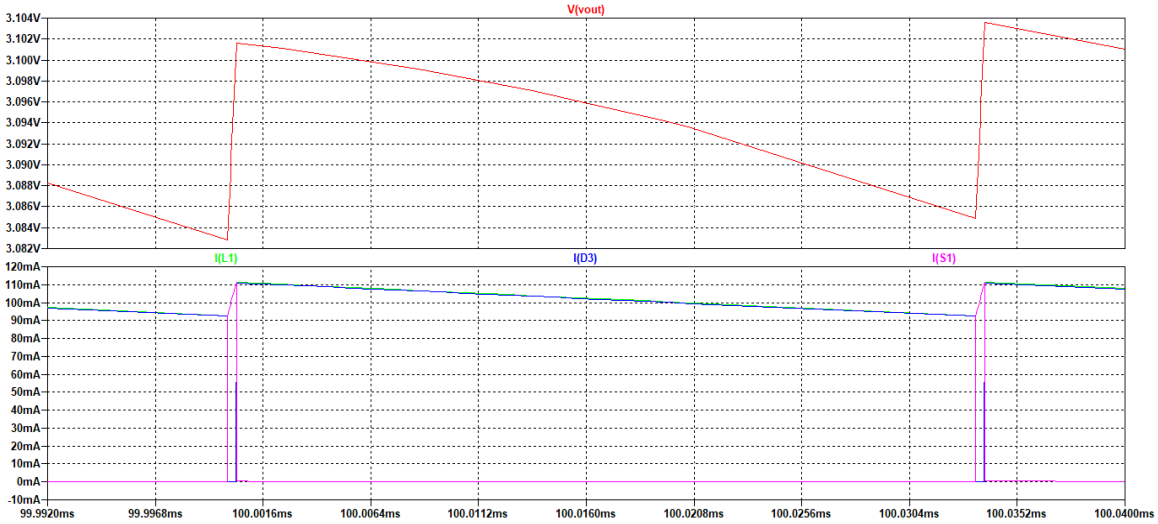
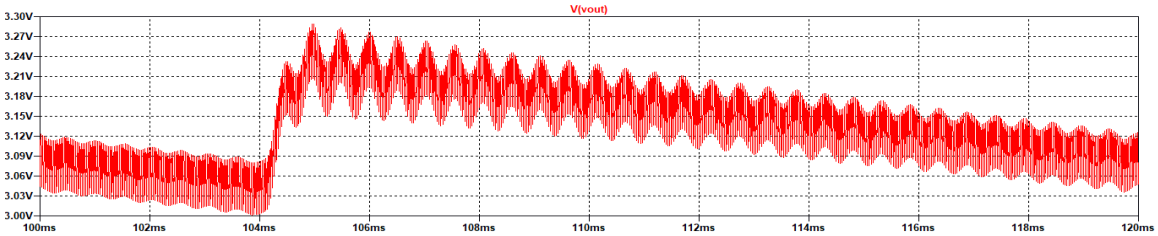
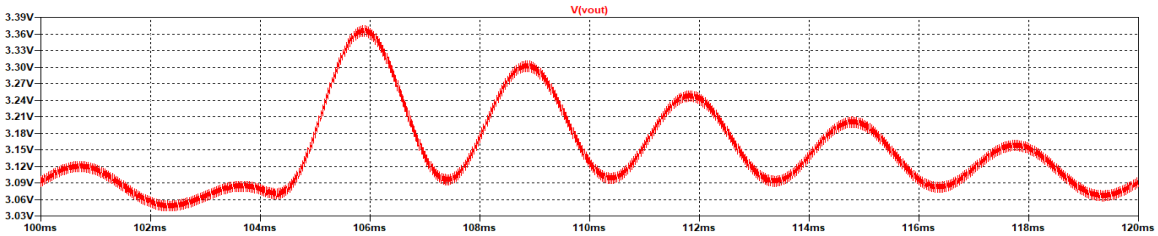


Figure 4.6: simulation with $V_{AC} = 220\,V$, $I_{load} = 100\,mA$ and $C_{out} = 33\,uF$



(a) $V_{AC} = 220\,V$, $I_{load} = 100\,mA$ and $C_{out} = 1\,\mu F$



(b) $V_{AC} = 220\,V$, $I_{load} = 100\,mA$ and $C_{out} = 33\,\mu F$

Figure 4.7: low frequency resonance occurs when the output capacitor has a larger value, since the output is like a second order LCR filter.

4.3.3 Efficiency considerations

Now it is possible to simulate the circuit in different load conditions and input voltages, then evaluate the efficiency for each point. The tested circuit is the same as the one reported in figure 4.3, with the changes obtained is the previous section:

- $C_{out} = 33\,\mu F$;
- $ESR = 1\,\Omega$;
- $D_{nom\_120V} = 0.0237$;
- $D_{nom\_220V} = 0.0129$.

The simulation is implemented within the *LTSpiceXVII* simulator, ".meas" and ".step" directives have been used for the scope. As already said, the efficiency has been computed in different conditions and those are:

- $V_{AC} = 120\,V$ and $V_{AC} = 220\,V$;
- $I_{load} = [0 \div 100]\ mA$ with steps of $25\,mA$;

so basically, there are 5 simulations for each condition of the input voltage. The efficiency is computed by looking at the input/output quantities of the circuit, taking the instantaneous input/output power, averaging them over a multiple of line periods and then using the definition of efficiency. Following this procedure, the graph in figure 4.8 has been obtained. The red curve is the one associated with the minimum AC voltage, or in the same way to the maximum duty cycle, and it has quite a good efficiency: from more than 60 % in *light load* condition (25 % of the maximum current), to more than 70 % in *heavy load* (full current). The blue curve is related to the maximum AC voltage, or the minimum duty cycle, and in this case the efficiency has very low values, in particular in *light load* conditions (at 25 % of maximum current: $\eta \approx 40\,\%$). This bad efficiency is mainly related to the high voltage excursion between input and output, this one affects the switching and diode losses, like already suggested when discussing equation 4.9.
This is quite a big problem, because it means that the device will never work properly and has to dissipate most of the power, with resulting self-overheating problem to

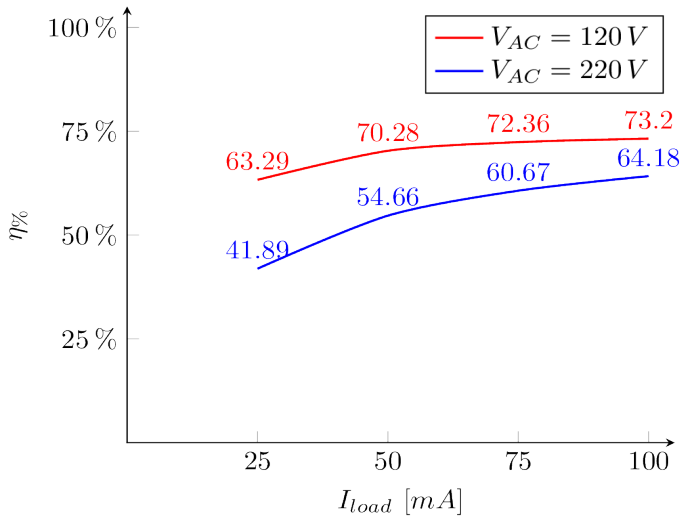


Figure 4.8: efficiency curves evaluated for two possible input AC voltage: $120\,V$ *(in red) and* $220\,V$ *(in blue)*

solve. To improve the efficiency, the first idea is to work with a lower input voltage, but this is something that can not always be accomplished, since depends on standard main voltage value. Then it is possible to reduce the switching losses, in particular working with a variable frequency device; with a too large input voltage, the switching frequency should be lowered, to keep the losses within a reasonable value.

4.4 Conclusions

This first analysis has highlighted some pros and cons of an ideal basic buck converter, but it was also possible to improve the knowledge of the basic circuit and understand its limits. In particular, it has been seen that a fixed frequency design is not the best solution, if the input voltage is larger than the output one. This first rough and ideal solution has to be considered only as a milestone and reference point for future comparisons.

In following section, a more complex design will be simulated and a variable frequency solution considered: the *VIPer01* will be the centre of a new design.

CHAPTER 5

EMC for SMPS

The Electro Magnetic Compatibility (EMC) issue will be discussed in this chapter, with a particular attention to SMPS field. At first, the EMC concept will be defined, then the difference between conducted and radiated emission will be highlighted, after that, standards are going to be briefly described and, finally, the Line Impedance Stabilization Network (LISN) will be introduced. The last sections will regard the Electro Magnetic Interference (EMI) filter design and simulation.

5.1 What is the meaning of EMC?

Electro Magnetic Compatibility (EMC) refers to the "generation, transmission and reception of electromagnetic energy" [27]. This means that it is possible to define a source, a path and a receiver for this energy. The source and the receiver can be desired or undesired, then the receiver can be reached by wanted or unwanted signals. When a source (emitter) generates electromagnetic energy and this one is coupled by a path to a receiver (receptor), it is possible to talk about *interference*; on the other hand a receptor, that receives the electromagnetic energy from the outside world, is said *susceptible* to that energy. So, EMC requires that an object: "does not cause interference with other systems; is not susceptible to emission from other systems and does not cause interference with itself" [27].

Those requirements covers also legal aspects, if the designed object has to be sold in a particular country with respect to another one. There exist standards, which provide the amount of interference acceptable for a particular application and describe, also,

how to realize the measurements, in order to get the same results during a possible validation test.
There are different ways to minimize the interference, but the simplest one regards the reduction of the electromagnetic energy at the source. This happens because the emitter is under the designer control, the coupling path and the receiver, instead, depends on different aspects and situations. Objects or systems, containing switching electrical quantities, can create electromagnetic interference due to high dv/dt or di/dt, which are related to high electric field and magnetic one respectively.
Very long wires act like antennas, that can both radiate or receive electromagnetic energy and this is one aspect that should always be considered in EMC problems.

5.2 Conducted emission, radiated emission and standards

Any object can be seen both as a source of electromagnetic energy and a receiver, for this reason it is possible to distinguish:

radiated emission they are those generated by the source and can be measured by an antenna;

radiated susceptibility emissions are generated from other objects and the considered one acts like an antenna;

conducted emission they are generated by the source and are conducted by a path provided by wires;

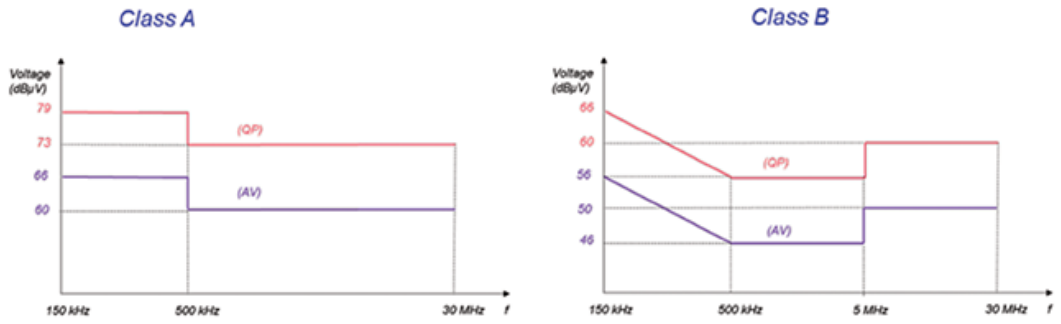
conducted susceptibility emissions are generated from other systems and reaches the one in exam running through wires.

As already said, susceptibility is not at all under the control of the designer, so the main focus will be onto *radiated emission* and *conducted* one. For this reason, standards of different countries cover those two aspects and define limit values over different frequency ranges. Basically, any device working with a switching electrical quantity at a frequency higher than $9\,kHz$ have to undergo those standards. Limitations can changes depending on the application filed; for example, the Federal

Communications Commission (FCC) defines **class A** and **class B** devices, where the first one refers to commercial, industrial or business environment and the second one to residential applications. Class B devices have more stringent requirements, because residential users is not supposed to have the knowledge over EMC issue.
Now it is possible to define better the *conducted* and *radiated emissions*:

conducted emission they are currents generated by the device in exam, which reach the AC power cord and are placed on the common node net. This node is basically a very long wire and, so, those currents can radiate with high efficiency. Conducted emissions are measured over a frequency range that extends from $150\,kHz$ to $30\,MHz$ and limits are given in μV or $dB\mu V$. Depending on the measurement device, it is possible to find two different sets of limit: **QP**, which stands for Quasi-Peak detector, and **AV**, which stands for Average detector. An example of those limits can be found in figure 5.1.

radiated emission refers to electric and magnetic field produced by the switching action of the device in exam. Here the frequency rage extends from $30\,MHz$ to $40\,GHz$ and limits are given in $dB\mu V/m$, so the distance is an important parameter in the measurement setup.



Frequency (MHz)	µV QP (AV)	dBµV QP (AV)
0.15 – 0.5	8912.5 (1995)	79 (66)
0.5 - 30	4467 (1000)	73 (60)

Frequency (MHz)	µV QP (AV)	dBµV QP (AV)
0.15	1995 (631)	66 (56)
0.5	631 (199.5)	56 (46)
0.5 - 5	631 (199.5)	56 (46)
5 - 30	1000 (316)	60 (50)

Figure 5.1: class A and class B conducted emission limits taken from [28]

Standards, like **CISPR 22** or the equivalent **CEI EN 55022**, defines also how to perform measurements, this is done in order to obtain the same result in different places. For radiated emissions, measurements have to be done in a *semi-anechoic chamber* or in *open-area test site* (OATS); the device under test (DUT) should be place in a well defined position in the chamber and the antenna at a well known distance.

Conducted emissions test requires a particular device to be performed, this one is called Line Impedance Stabilization Network (LISN) and its job is to adjust the main impedance to $50\,\Omega$ value. This is done, because the main impedance value can change quite a lot from place to place and this will affect the test results. A typical circuit representing a LISN is reported in figure 5.2, here $C1$ and $L1$ are used to block noise coming from the AC source, then $C2$ provides a path for the current coming from the DUT. $C2$ is discharged by $R1$ and the $50\,\Omega$ is where the spectrum analyser is connected. Typical values are: $L1 = 50\,\mu H$, $C1 = 1\,\mu F$, $R1 = 1000\,\Omega$ and $C2 = 0.1\,\mu F$. Standards can then require a device to pass also other tests, like

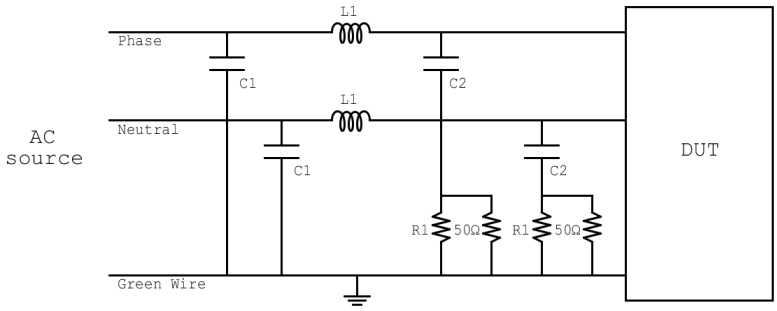


Figure 5.2: typical LISN scheme

Electro Static Discharge (ESD), *surge immunity*, *pulse magnetic field immunity* and others.

5.3 Common mode currents, differential mode currents and EMI filter

In the EMC field, distinction between *common* and *differential mode currents* can be found. Both the two quantities contributes to conducted emission and, to keep them

within the DUT, an Electro Magnetic Interference (EMI) filter is needed. Common mode currents are those flowing from the *Phase* and the *Neutral* to the *Green Wire*; differential mode currents, instead, are the ones flowing from the *Phase* to the *Neutral*. This behaviour is summarised in figure 5.3, where there is a DUT on the right and a simplified circuit of a LISN, with only the two 50 Ω resistors. Common mode currents

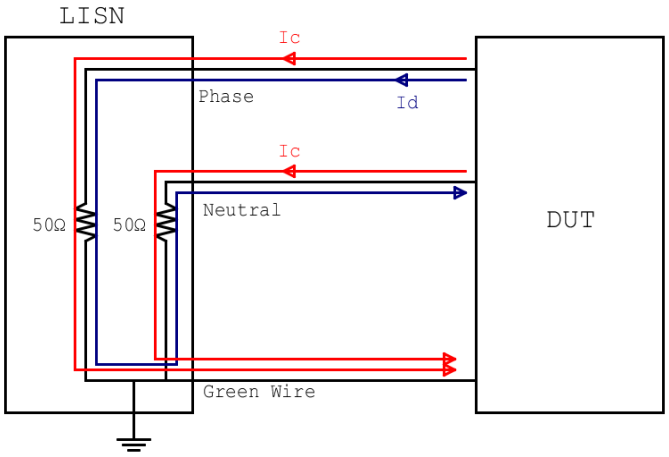


Figure 5.3: common mode currents in red and differential mode ones in blue

can have a major impact onto conducted emissions with respect to differential mode one [27], but there are methods to deal with them. The "common-mode choke" usage, is one of them, and consists of two inductors coupled onto the same magnetic core in opposite way, resulting in higher impedance for common mode currents, which are then blocked. An example of this device can be seen in figure 5.4. In SMPS the major

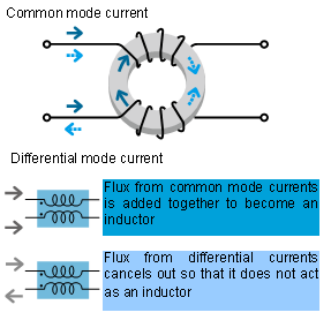


Figure 5.4: Common mode choke example, taken from [29]

contribute to common mode currents is given by parasitic capacitance to ground onto the primary side of the converter. In [30], the main contributions to this capacitance are: the parasitic capacitor between the power MOSFET's heat-sink and ground, the

inter-winding capacitance (if there is a transformer) and a stray capacitance onto the primary side winding. Common mode currents see the two $50\,\Omega$ of the LISN in parallel and [30] defines a formula, reported in (5.1), for computing the common mode voltage values onto them:

$$V_{CM} = 100 \cdot V_P \cdot f_0 \cdot C_P \tag{5.1}$$

here V_P represents the peak voltage onto the input capacitor of the SMPS, the one after the rectifier, f_0 is the switching frequency of the converter and C_P the parasitic capacitance discussed earlier. The C_P value ranges from $50\,pF$ to $500\,pF$ [30]. The common mode voltage frequency behaviour is like a low pass response, where the pole frequency depends onto the *rise/fall time* of the power MOSFET. This rising time is typically around $50\,ns$, thus the pole frequency is in the MHz range. Supposing to have an $f_0 = 30\,kHz$, a $V_P = \sqrt{2} \cdot 220\,V = 311.1\,V$ and $C_P = 500\,pF$, it is possible to compute the V_{CM} up to the pole frequency:

$$V_{CM} = 100 \cdot \sqrt{2} \cdot 220\,V \cdot 30\,kHz \cdot 500\,pF \approx 467\,mV$$
$$V_{CM}|_{dB\mu V} = 20 \cdot \log(V_{CM}/1\,\mu V) \approx 104\,dB\mu V$$

It is possible to see that **CISPR 22** defines limits also for common mode currents, expressed in $dB\mu V$, and, in the case of a class B device, the maximum value allowable is $84\,dB\mu V$, which means that, with the previous condition, the device will not satisfy the requirements. It is clear that an EMI filter is needed.
Differential mode currents in SMPS arises when the input capacitor, designed to work as an energy storage and so with large value ($\approx \mu F$), has to withstand high frequency current components. This kind of capacitor is characterized by high values of ESR and ESL, parasitic resistance and inductance, and so at high frequency it is not able to damp the current. This kind of currents, as reported in figure 5.3, sees twice the $50\,\Omega$ of the LISN and [30] defines a formula (5.2) for computing the differential mode voltage.

$$V_{DM} = 2 \cdot f_0 \cdot L_F \cdot I_P \tag{5.2}$$

In the previous formula, the f_0 is the switching frequency of the converter, L_F is the ESL of the SMPS input capacitor and I_P the peak value of the current, this one depends onto the converter output power. Supposing to have $f_0 = 30\,kHz$, $ESL = 30\,nH$ and $I_P = 500\,mA$, the resulting differential mode voltage will be equal to:

$$V_{DM} = 2 \cdot 30\,kHz \cdot 30\,nH \cdot 500\,mA \approx 900\,\mu V$$
$$V_{DM}|_{dB\mu V} = 20 \cdot \log(V_{DM}/1\,\mu V) \approx 59\,dB\mu V$$

Comparing this result with the limits reported in figure 5.1 results is no need for attenuation of the differential mode current, but it is always a good habit to reduce them, if the cost is not a deal.
Up to this point, it is clear that an EMI filter is needed too reduce both the differential mode currents and the common mode ones. The filter structure can differ, depending on various aspect and requirement, but it should act like a low pass filter with an attenuation given by the previous calculations. The inductor should act like a blocking impedance for high frequency currents and the capacitor should absorb them. The resulting structure is a π one, which can be also recognized in figure 5.5. It is possible to see C_X and C_Y capacitors, they are tested and approved by safety

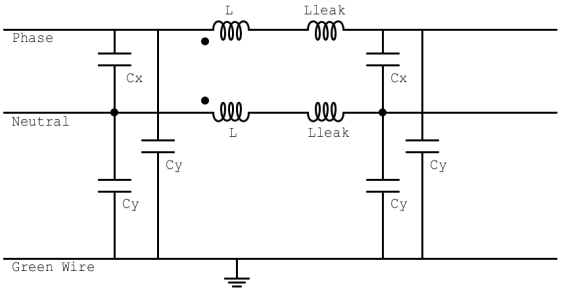


Figure 5.5: π structure EMI filter

agency, because, when they fail, they should fail like open circuit. C_X capacitors are connected between *Phase* and *Neutral*, whereas C_Y ones are connected between *Phase* or *Neutral* and *Green Wire*. If the first ones fail like a short-circuit, the risk is fire, the second ones, instead, can provoke shock hazard.
It is possible too see also the *common mode choke*, discussed earlier, and the leakage

inductance associated to it, which can help reducing the differential mode currents.

5.4 EMI filter design procedure

It has been seen that an EMI filter is needed in a SMPS, because there is a switching quantity that creates high dv/dt changes or di/dt ones and they can cause Electro Magnetic Interference (EMI). In order to keep this noise inside the SMPS, it is important to place a filter between the AC source and the switching device, the closer to AC side the better the results. Consider a simple AC to DC converter structure, like the one reported in figure 5.6, this will be the reference structure for the following considerations. The first step in the design procedure is to select a proper *common*

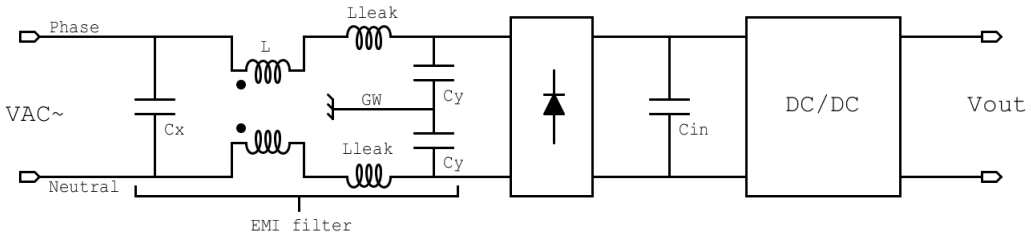


Figure 5.6: simple AC to DC converter, with EMI filter

mode choke, this one should be rated to support the $V_{AC} \geq 220\,V$ and a current larger than the one required by the other part of the circuit (e.g.: $I \geq 1\,A$). A possible choke is the *RN 102-2-02-1M1*, with $2\,A$ of rated current and an inductance of $1.1\,mH$. In the datasheet it is possible to see that the leakage inductance is $1\,\%$ of the total one.

The second step is to design the C_Y capacitors, in order to do this consider the following equivalent circuit, in figure 5.7, for the common mode currents. It is possible to recognize the common mode current source, part of the filter seen in figure 5.6 and the $50\,\Omega$ load offered by the LISN. The scope of this filter is to reduce the common mode current to the previous mentioned resistors and a possible way to solve this problem is to work with current partition. At this point the design is quite easy, because it is clear that, to divert current away from the resistors, the following condition should

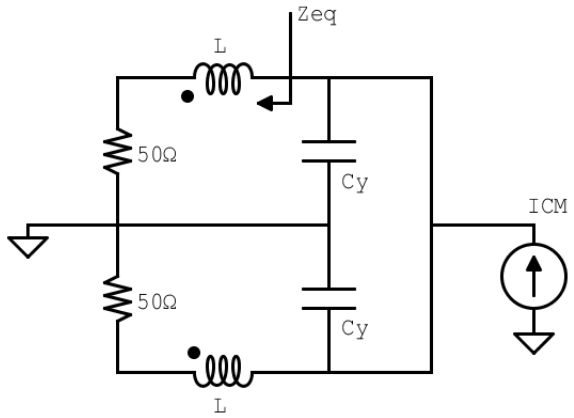


Figure 5.7: equivalent circuit for the common mode currents

be met:

$$|Z_{C_Y}| << |Z_{eq}| \tag{5.3}$$

$$Z_{C_Y} = \frac{1}{j\omega C_Y} \tag{5.4}$$

$$Z_{eq} = j\omega L + R_{LISN} \tag{5.5}$$

substituting (5.4) and (5.5) into (5.3), it is possible to derive the required value of C_Y, given L and the frequency range. L has typical values raging from $1\,mH$ to $10\,mH$, consider for example the previous one $1.1\,mH$, and the frequency range is the one defined in the **CISPR 22**: from $150\,kHz$ to $30\,MHz$. From (5.5) it is clear that the main contribute is given by the L inductance, since it is multiplied by the frequency; the reactance, associated to the capacitor, is inversely proportional to frequency instead.

$$C_Y >> \frac{1}{2\pi f_{min}\,|Z_{eq}|} \geq \frac{10}{2\pi f_{min}\sqrt{(\omega L)^2 + R_{LISN}^2}} \tag{5.6}$$

$$C_Y > 1.02\,nF \rightarrow C_Y = 2.2\,nF \tag{5.7}$$

This capacitor, as already said, should be a Y rated type and realized with metallized polypropylene or paper. The *PHE850EA4220MA01R17* ia a possible solution; it is characterized by a $V_{AC} > 220\,V$, $V_{DC} = 1.25\,kV$, 20 % of tolerance and a $\tan\delta$ that ranges from 0.2 % @1 kHz to 0.6 % @100 kHz. It is possible to compute the ESR of

the capacitor, from the $\tan\delta$ parameter, with the equation (5.8) reported below.

$$ESR = \tan\delta \cdot \frac{1}{2\pi f C} \tag{5.8}$$

Substituting the values, the obtained ESR is equal to $145\,\Omega$ at $1\,kHz$ and $4.3\,\Omega$ at $100\,kHz$. The ESL is supposed to be mainly associated to the capacitor's leads, for this reason its typical value is $6\,nH/cm \div 12\,nH/cm$.
The C_X capacitor design is similar to the previous case, the equivalent circuit is the one reported in figure 5.8, where everything from the capacitor to the SMPS has been modelled as a current generator. Also in this case the current should be diverted away

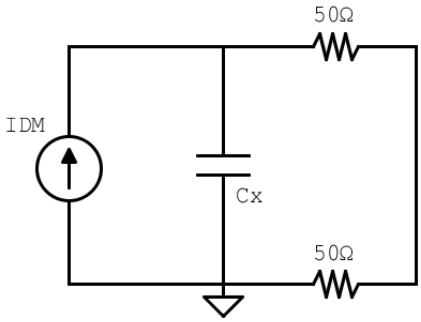


Figure 5.8: equivalent circuit for the differential mode currents

from the $50\,\Omega$ load, in order to accomplish this goal, the following condition should be satisfied:

$$|Z_{C_X}| << 2R_{LISN} \tag{5.9}$$

$$Z_{C_X} = \frac{1}{j\omega C_X} \tag{5.10}$$

Substituting (5.10) into (5.9), a condition onto the C_X value can be found, as reported in (5.11). The limit values for C_X can be found using the lowest frequency ($150\,kHz$), which is the one defined by th **CISPR 22** as in the previous case.

$$C_X >> \frac{1}{2\pi f 2R_{LISN}} > \frac{10}{2\pi f 2R_{LISN}} \tag{5.11}$$

$$C_X > \frac{10}{2\pi 150\,kHz 100\,\Omega} = 106\,nF \rightarrow C_X = 150\,nF \tag{5.12}$$

A possible capacitor, corresponding to the previous requirement, is the X1 type *F862BK154K310Z* by *KEMET*. It has a $150\,nF$ capacitnce value, with 10 % of tolerance, rated for a $V_{AC} = 300\,V$, a $V_{DC} = 630\,V$, and with a $\tan\delta = 1.3\,\%$ @$1\,kHz$, corresponding to an ESR equal to $13.8\,\Omega$, using (5.8). The final circuit for the EMI filter is then reported in figure 5.9, this circuit will be simulated in the next section and all the parasitics will be added.

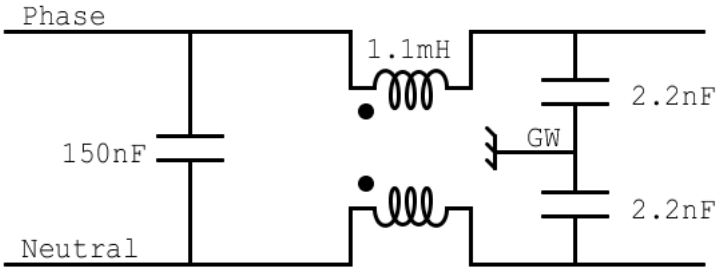


Figure 5.9: EMI filter with components values

5.5 EMI filter frequency response

Once designed, the EMI filter should be simulated and it is important to verify the response for both common mode current and differential mode one.
For the common mode case it is important to see how much the EMI filter attenuates the input current, then in order to get a more realistic response of the filter all parasitics have been considered, like the series resistance and leakage inductance of the choke, the ESR and the ESL of the capacitors. The simulated circuit is reported in figure 5.10, it is possible to see that the C_Y capacitor has an increased value with respect to the $2.2\,nF$ found earlier. An higher values corresponds to a lower reactance and this has been required because the current attenuation onto the *green wire* was not sufficient, only $10\,dB$ instead of the required $20\,dB$. An attenuation of $\approx 25\,dB$ is provided at the *green wire* node with the $10\,nF$ capacitor (*PHE850EB5100MB04R17*), this one has a smaller ESR, which is computed with (5.8). The attenuation of this current is considered over the frequency range typical for common mode conducted emission ($150\,kHz$ to $30\,MHz$) and the simulation result can be appreciated in figure 5.11. A voltage source is applied between *Phase* and

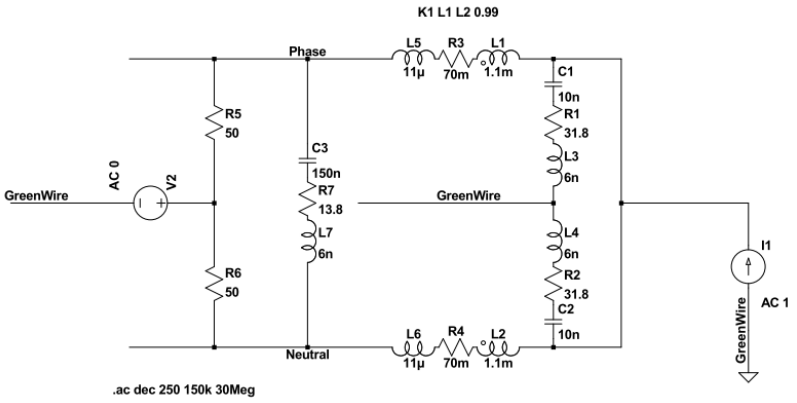


Figure 5.10: common mode EMI filter test circuit

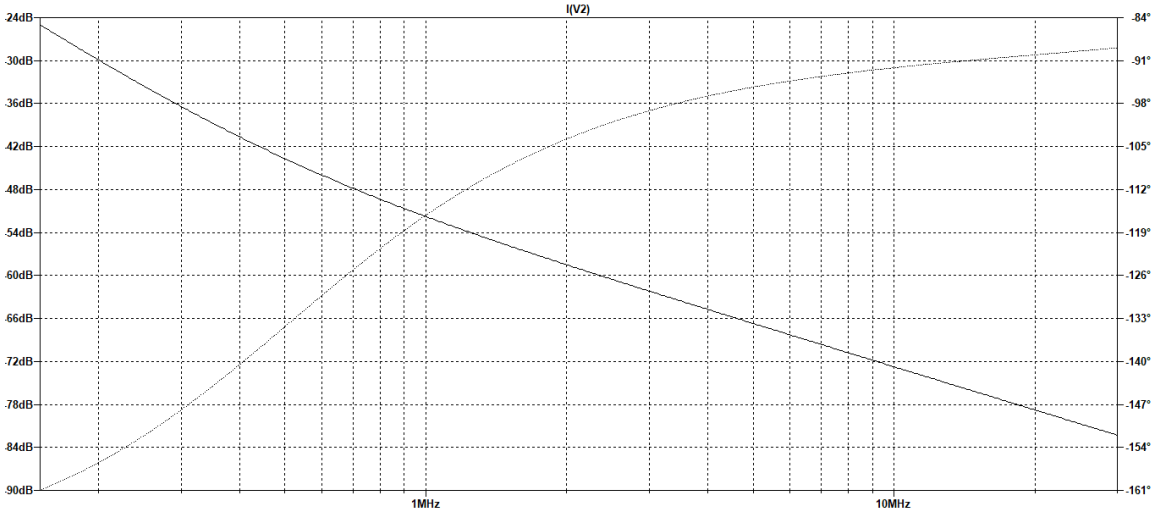


Figure 5.11: frequency response of the current injected into green wire

Neutral, for the differential mode circuit, then the frequency response of the voltage onto 50 Ω resistor is considered. It is possible to accept a lower attenuation in this case, due to the previous computations onto the differential mode voltage. Consider, in this case, the circuit in figure 5.12, here there is no need for the null voltage source applied at the *green wire*, as it was in the previous case, since the stress is no more onto the current. The simulation result can be seen in figure 5.13, the resulting minimum attenuation, at $150\,kHz$, is around $15\,dB$, which should be enough in this case. All previous calculations are no more valid if the converter frequency is changed, in fact, both (5.1) and (5.2) depends on frequency.

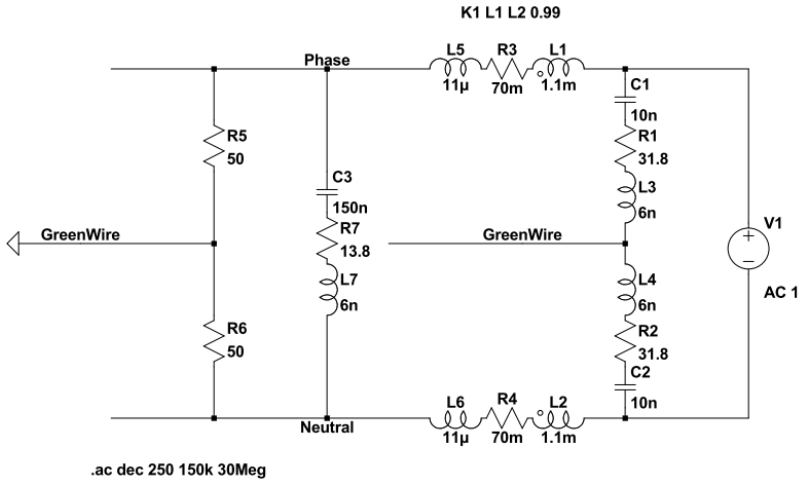


Figure 5.12: differential mode EMI filter test circuit

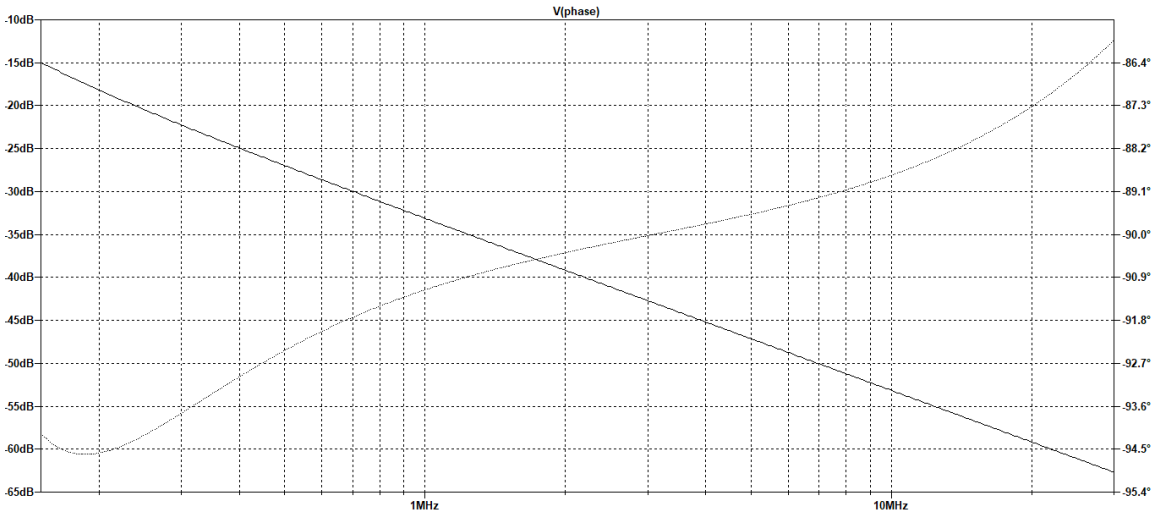


Figure 5.13: frequency response of the voltage onto the $50\,\Omega$ *resistor*

5.6 Conclusions

The EMC problem has been discussed in this chapter and some of the fundamental topics have been covered; like different kind of emissions, standards, LISN, common and differential mode currents, safety capacitors and others. During the discussion, accent has been placed onto the importance of structures to avoid EMI propagation, in particular filters design for SMPS. At the chapter's end, an EMI filter design procedure has been discussed and simulation results presented. It is important, once designed the target converter, to verify the damping efficiency of the designed EMI filter and redesign it, if needed.

CHAPTER 6

VIPer01 based solution

In the previous chapter an ideal buck converter has been designed, now a real device will be used in the design. Among all the possible ICs considered in Chapter 2, the *VIPer01* from *STMicroelectronics* is the chosen one. The choice is due to the availability of a Spice model for this IC, whereas the other manufacturers, like *Power Integrations*, do not always provide them. The first part of this chapter will regard the integrated circuit's explanation, then the "real" buck will be designed, taking also into account the feedback loop problem, in the end various simulations are performed.

6.1 VIPer01

The *VIPer01* family, in [31], provides an $800\,V$ breakdown voltage power MOSFET with a PWM current mode control, everything integrated on a single chip. This is a 6 pins device, whose characteristics are going to be reported here, and its block diagram is represented in figure 6.1. The six pins are placed on the two longest side of the package and, as typically done in power applications, the drain shows multiple pins for the power MOSFET, which are collected on one single side of the device. This is done in order to be able to provide enough copper area underneath them, for thermal dissipation issue.
The description of pins' functionalities can be found in the datasheet, but here they will be, in any case, reported together with some associated block diagram insight:

GND this is the **source** contact of the internal power MOSFET and it is also the

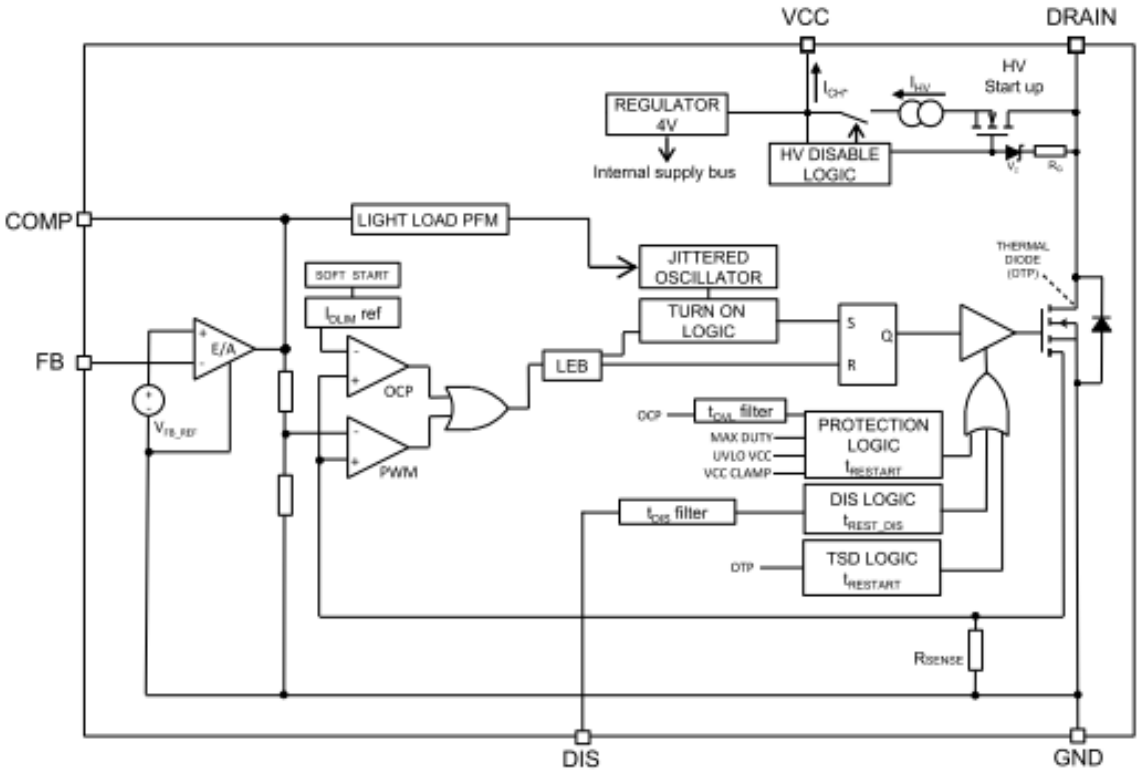


*Figure 6.1: block diagram of **VIPer01** in [31]*

pin at which all the voltages are referred (e.g.: the feedback voltage or the supply one);

VCC this is the controller **supply** pin. The device can work in *self-supply* or in *external-supply*: in the first case an external storage capacitor, together with a small bypass one ($0.1\,\mu F$) for noise filtering, should be provided; in the second case instead the storage capacitor can be charged by the output or with an auxiliary winding. When *self-supply* mode is selected, the device will charge the capacitor in a cyclic way, using the upper-right most part of the block diagram: it senses the VCC voltage level and, whenever the value falls below $V_{CC_{son}} = 4.25\,V$, the high voltage current source (I_{HV}) is turned on and the capacitor is charged with the I_{CH3} current level. This value is the highest possible, instead at start-up the current level is lower (I_{CH1} and then I_{CH2}), this is done because the capacitor is initially discharged and to avoid damaging the device. Notice that the high voltage current source can be enabled only during the turn off phase of the power MOSFET. The *external-supply* method

and other informations are well discussed in [31];

DIS this is the **disable** pin, when a voltage greater than the reference ($V_{DIS\_th} = 1.2\,V$) is applied for more than $T_{DEB} \approx 1\,ms$ then the PWM is disabled. It can be used to implement a *line over-voltage protection* in isolated/non-isolated topologies, with a voltage divider connected between the input and the GND, or an *output over-voltage protection* in non-isolated ones;

FB this is the **feedback** pin and it is connected to the inverting input of an error amplifier (EA), which is referenced to V_{FB_REF} with respect to GND. The internal EA can be also disabled if the pin is connected to GND, this allow the user to connect an external EA if needed. The EA's output is scaled down and connected to the PWM, which is basically a comparator that compares the voltage drop on the non-inverting pin, resulting from the drain current onto the R_{SENSE}, and the previous output. In this way it is implemented a *current mode control*. The FB pin is strictly related to the $COMP$ one, at which a compensation network should be connected;

COMP this the EA's output and is used to create a compensation network to improve stability and dynamic of the loop gain, this network should be connected between this pin and the GND one;

DRAIN this is the drain of the internal power MOSFET and it is also used to charge the VCC storage capacitor, during *start-up* and *steady-state*;

The **VIPer01** provides a set of additional features, which can be seen from the block diagram, and they are meant to improve the behaviour of the converter in different working conditions. It comes with *soft-start*, *jittering* on the oscillator frequency, a *pulse-skipping* capability, *pulse frequency modulation* (PFM) and some *protection* capabilities. In more detail:

Soft-start at start-up or after any fault condition, which will be followed by a restart phase, the maximum output current will be limited from $0\,A$ to I_{DLIM} in 8 steps. This is done to limit the *in-rush current* and so saving the converter life; the soft start time t_{SS} lasts for $8\,ms$;

Frequency jitter the internal oscillator works with *fixed-frequency*, whose value depends on the selected device ($30\,kHz$, $60\,kHz$ and $120\,kHz$ respectively for X, L and H type), and jitter is added to reduce the conducted emission. Jittering will spread the spectrum and this will distribute the energy of each switching frequency harmonic on an higher number of bands;

Pulse-skipping when the drain current reaches the upper limit I_{DLIM}, during the minimum on-time of the transistor T_{ON_MIN}, then a cycle will be skipped. The switching frequency is reduced, in this way, up to the minimum value $F_{OSC\_MIN} = 15\,kHz$). This technique is used to avoid the *flux-runaway* problem: during the turn-on time the inductor is charged by a certain voltage, then during the off-time it will be discharged by another voltage, if energy is not the same in the two phases, then there will be a residual DC current. If this behaviour lasts for too many cycles, the current can reach high values and the inductor will be saturated, as a consequence it will no more behave like an inductor, rather like a piece of wire. To avoid this the pulses are skipped and the turn-off time will be increased, letting the inductor discharge properly;

Pulse frequency modulation this function allow the device to lower the switching frequency up to some hundreds of Hz and, as consequence, reduce all the related losses. This is done when the output load is reduced and so to not damp down the efficiency in light loads condition. This function is directly related to the feedback loop response: if the load is reduced, then also the voltage at the $COMP$ pin will be reduced, at the V_{COMPL} threshold will correspond the I_{DLIM_PFM} current limit. If the load is further decrease, so that the V_{COMP} is below the V_{COMPL}, the PFM function is enabled;

Protections the device has different kind of protections like *overload*, *maximum duty cycle* limitation, *VCC clamping* and also *thermal shutdown*. All of them are meant to avoid critical working condition for the device, but for the mere design procedure are not necessary and can be considered/tested in further passages.

STMicroelectronics provides models for this device, for both **LTspice** and **PSpice**; then there are also two evaluation board: *STEVAL-ISA177V1*, which is a flyback

converter for $4.25\,W$ rated output power, and *STEVAL-ISA178V1* in [32], which is a buck for $1\,W$ rated output power. The last one, in particular, can be used as a starting point and a reference for this particular buck design.

6.2 Real buck design

The buck topology will now be implemented and simulated with the *VIPer01*'s model, the [32] will be used here as a guide and as starting point for the design. Up to this point, no considerations have been made on the feedback implementation, but this can no more be avoided now and will be discussed in detail. The simulations are meant to highlight the device working behaviour and efficiency. It is also important to consider the EMI problem at this stage and verify if the design is able to pass the requirements imposed by different institutions all over the world. Those authority provides a set of rules that any possible marketable device must pass, before entering the market. For these reasons, the effect of the EMI filter will be considered and a comparison with a circuit without it will be done.

6.2.1 Feedback design

As already said, the real buck have to work with a feedback loop in order to stabilize the output voltage and regulate the duty cycle depending on different working conditions. Looking at the *VIper01*'s datasheet in [31], it is possible to understand that this device works in *current mode*, because both the output voltage and the switch current are used to determine the duty cycle. A basic scheme of the circuit with controlling section is reported in figure 6.2, here it is possible to see: an *error amplifier* (EA) used to compare the output voltage with a reference one, a *compensation* network used to stabilize the feedback, a *pulse width modulator* (PWM) used to generate the duty cycle depending on the measured current level, a *SR latch* used to sample the signal, a *MOSFET driver* to correctly drive the switch and a *sensing resistor* (R_S) used to convert the current into a voltage.
Every time that the sensed current, converted into a voltage by the R_S factor, is higher with respect to the reference, generated by the EA, then the latch will be reset. The latch's set occurs instead every T_{SW} period. The compensation is needed,

because there is a loop and the system should not oscillate or create instability during operation. In order to get a stable system, the *phase margin criteria* should be considered: the loop gain phase have to be around 60 °, at the *crossover frequency*, to get a stable system. At this point, it is possible to see this structure as formed

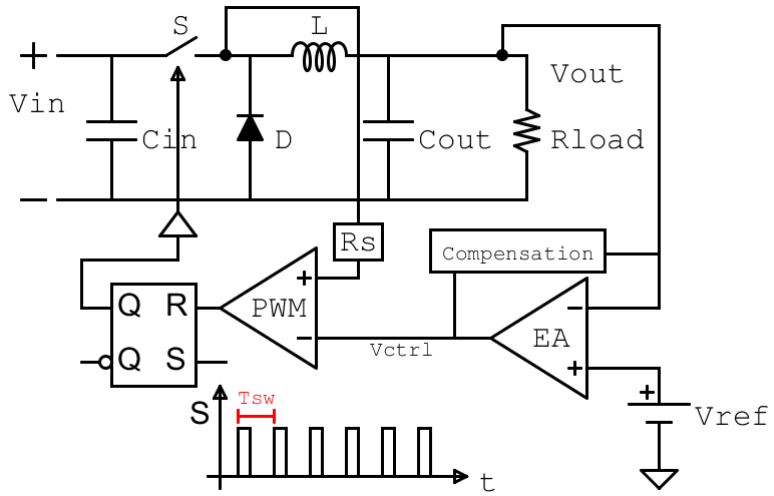


Figure 6.2: a buck circuit with a Current Mode control section

by three sub-system: the power stage, the compensation network and the controller. Every one of them have its own transfer function and it is necessary to find them for the compensation network design, a representation of this kind of control loop is reported in figure 6.3. The $PWR(f)$ block represents the power stage and, in *current*

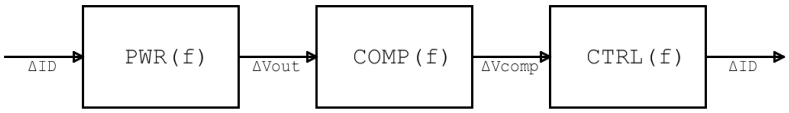


Figure 6.3: control loop diagram

mode, the transfer function computation is quite easy: it is possible to consider the inductor as a controlled current source, since this quantity is the one monitored by this method. Making this substitution, it is possible to simplify the output of the buck as reported in figure 6.4. Notice that the circuit is considered in the *Laplace domain* and the transfer function is $V_{out}(s)/I_L(s)$, which can be easily computed, giving the result in 6.1:

$$PWR(s) = \frac{V_{out}(s)}{I_L(s)} = R_{load} \cdot \frac{1 + sC_{out}ESR}{1 + sC_{out}(ESR + R_{load})} \tag{6.1}$$

This transfer function, like the one reported in figure 6.5, has one pole and a zero,

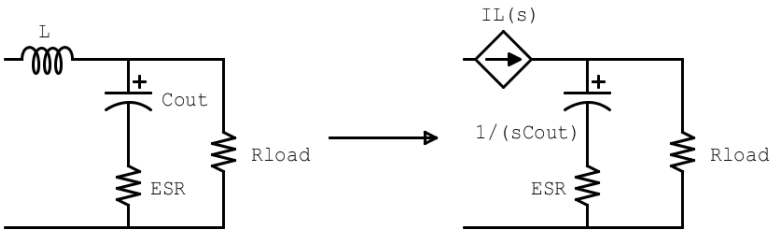


Figure 6.4: output equivalent circuit

whose values are given by the following formulae:

$$f_P = \frac{1}{2\pi C_{out}\left(ESR + R_{load}\right)} \tag{6.2}$$

$$f_Z = \frac{1}{2\pi C_{out} ESR} \tag{6.3}$$

The $\Delta V_{comp}(s)/\Delta V_{out}(s)$ transfer function is the one that has to be designed to

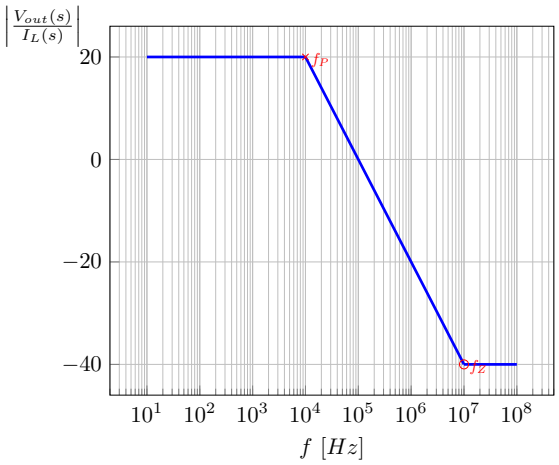


Figure 6.5: one pole and one zero transfer function

make the device stable, what is left to find is the $CTRL(f)$ one: this is the inductor current variation over the V_{comp} one. Now, since the current is measured at the switch side in the *VIPer01*, this one should be considered, but *current mode* aims to control the maximum peak current into the inductor, which is also the one in the switch and so everything is consistent. The previous consideration simplify the computation of the $CTRL(f)$, in fact the current limits and the V_{comp} ones are reported in the

datasheet:

$$V_{COMPH} = 3\,V \quad @ \quad I_D = I_{DLIM} = 240\,mA$$
$$V_{COMPL} = 0.8\,V \quad @ \quad I_D = I_{DLIMPFM} = 65\,mA$$

remember that the **VIPer012X** is the chosen device of the family, because of the I_{DLIM} higher w.r.t. the peak inductor current, obtained in table 4.3. The lower value of the V_{COMP} has been chosen in order to avoid the **PFM** working condition, where the switching frequency will be changed. Given those values, it is possible to compute the transfer function of the controlling section:

$$CTRL(s) = \frac{\Delta I_D}{\Delta V_{COMP}} = \frac{240\,mA - 65\,mA}{3\,V - 0.8\,V} = 79.54\ \left[mAV^{-1}\right] \tag{6.4}$$
$$I_D\,(s) = CTRL(s) \cdot V_{COMP}\,(s) \tag{6.5}$$

Combining the 6.1 and the 6.5, it is possible to obtain the transfer function $V_{out}\,(s)\,/V_{COMP}\,(s)$, which will be then used to design the compensation network. In particular the following equation 6.6 is obtained:

$$\frac{V_{out}\,(s)}{V_{COMP}\,(s)} = CTRL(s) \cdot R_{load} \cdot \frac{1 + sC_{out}ESR}{1 + sC_{out}\,(ESR + R_{load})} \tag{6.6}$$

The loop gain transfer function should be like the one of an integrator, as reported

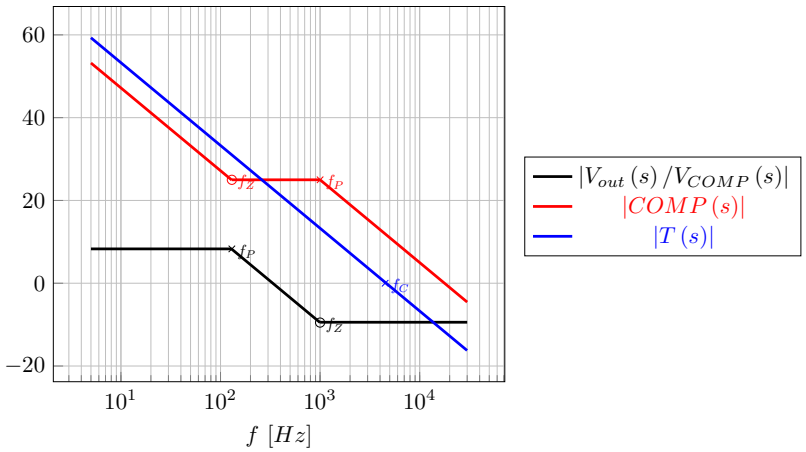


Figure 6.6: Bode plot representing the open loop gain $|T\,(s)|$, the compensation network frequency response $|COMP\,(s)|$ and the $|V_{out}/V_{COMP}|$

in figure 6.6, in this way a *stable* system is obtained, since the *phase margin* is almost $\varphi \approx 90\,^{\circ}$, and then it will be also *accurate*, because any possible *steady state error* will be reduced by the very high DC gain. The crossover frequency f_C is a suggestion of the speed of response of the overall system, but if increased too much can cause the noise to be an issue.

Once understood this, the design of the compensation network results straightforward: whenever there is a pole in the $|V_{out}/V_{COMP}|$ transfer function, the $|COMP\,(s)|$ one should exhibit a zero and vice versa. The resultant circuit, implementing the required transfer function, is a *type 2 compensator*, like the one represented in figure 6.7. The final circuit, developed at the end of the previous section, is needed, together with some small changes coming from the application note [32], to compute the components' values present in figure 6.7. The final circuit is reported in figure 6.8 and the main changes, w.r.t. the one in figure 4.3, are described here:

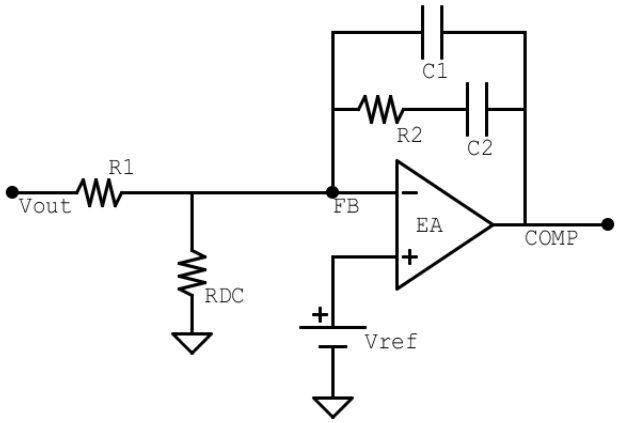


Figure 6.7: type 2 compensator, notice the presence of the labels FB and $COMP$, referring to the VIPer01 pins

bleeder resistor as suggested in the application note, this resistor provides a minimum load ($1\,mA$) to avoid overvoltages if the output load is removed;

STTH1L06A diode this diode is an ultra fast one [34] and its model has been obtained directly from *STMicroelectronics* website. The ultra fast capability is needed in order to reduce the reverse recovery time, during which the diode can conduct current in the opposite way, even if it should be able to block it, causing damages to the rest of the circuit;

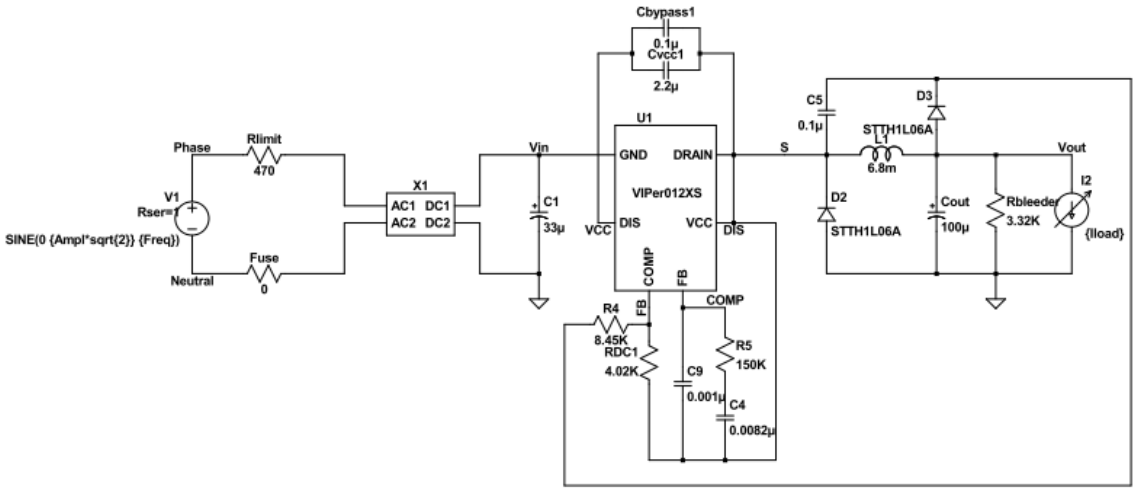


Figure 6.8: buck realized with the VIPer012X, working in CCM and self-supply mode

output voltage feedback the output voltage is copied onto the $C5$ capacitor and this one is used for the feedback loop;

full-wave rectifier is obtained with *MRA4007T3G* [33] diodes available from *ON Semiconductor*, which satisfy specifications obtained in table 4.3, and suggested in the application note;

VCC capacitor is like the one reported in the application note: 2.2 $[\mu F]$.

Now it is possible to compute the compensation network components values, the first step is to evaluate the main quantities of the $|V_{out}/V_{COMP}|$ transfer function:

$$DC_{gain} = CTRL(s) \cdot R_{load} \,||\, R_{bleeder} = 79.54 \left[mAV^{-1}\right] \cdot 32.67\ [\Omega] = 2.599 \tag{6.7}$$

$$f_P = \frac{1}{2\pi C_{out}\left(ESR + R_{load} \,||\, R_{bleeder}\right)} \geq 130\,Hz \tag{6.8}$$

$$f_Z = \frac{1}{2\pi C_{out} ESR} \geq 1\,kHz \tag{6.9}$$

The crossover frequency should be chosen high enough, in order to have quite a fast response, but not too high to avoid too much noise to pass into the system. The typical range in *current mode* is $f_{SW}/10 \leq f_C \leq f_{SW}/4$, where the f_{SW} is the switching frequency of the converter $(30\,kHz)$.

$$f_C = f_{SW}/5 = 6\,kHz \tag{6.10}$$

The flat gain of the $|COMP(s)|$ transfer function is obtained from simple consideration on the Bode plot in figure 6.6:

$$|T(f_P)| = |T(f_C)| \cdot \frac{f_C}{f_P} = 46.15$$
$$|T(f_P)| = DC_{gain} \cdot |COMP(f_P)|$$
$$|COMP(f_P)| = \frac{46.15}{2.599} = 17.76$$
$$f_{Pc} = f_Z = 1\,kHz \quad f_{Zc} = f_P = 130\,Hz$$

Looking at the circuit in figure 6.7, there are 4 unknowns, without considering the R_{DC}, but only three equations. This means that one of the four element can be chosen arbitrarily: typically C_1 is selected to be in the range $[56\,pF, 1\,nF]$, in this case $C_1 = 1\,nF$. The relations, linking the other unknowns to the equations, are the following ones and can be easily obtained by hand.

$$f_Z = f_{Pc} = \frac{1}{2\pi R_2 C_1} \quad \rightarrow \quad R_2 = 159\,k\Omega \rightarrow 150\,k\Omega \tag{6.11}$$
$$|COMP(f_P)| = \frac{R_2}{R_1} \quad \rightarrow \quad R_1 = 8.44\,k\Omega \rightarrow 8.45\,k\Omega \tag{6.12}$$
$$f_P = f_{Zc} = \frac{1}{2\pi R_2 C_2} \quad \rightarrow \quad C_2 = 8.16\,nF \rightarrow 8.2\,nF \tag{6.13}$$

Notice that the right hand side values, after the arrow, in the previous expressions are the normalized values. The R_{DC} is computed considering the whole system seen by the V_{REF} voltage source: in this case it is like having a non-inverting operational amplifier, whose output is the V_{out} of the converter. From this consideration, it is possible to obtain the following last expression 6.14 and the result, using the EA internal $V_{REF} = 1.2\,V$, is:

$$V_{out} = V_{REF}\left(\frac{R_1}{R_{DC}} + 1\right) \quad \rightarrow \quad R_{DC} = 4.83\,k\Omega \rightarrow 4.87\,k\Omega \tag{6.14}$$

The R_{DC} and the $R1$ should be resistor at 1 % of tolerance, since they define the output voltage value. The R_{DC} value has been corrected to $4.02\,k\Omega$ with some initial simulations.

Everything has been designed now and the next step will be the circuit simulation, with verification of correct behaviour and efficiency evaluation with the *LTSpiceXVII* simulator. During simulations the circuit will be optimized, so the final version will differ from the one presented in figure 6.8.

6.2.2 Simulations

In this section the simulation results are going to be reported, the circuit proposed in figure 6.8 will be simulated in different operating conditions and its correct behaviour will be verified. The first thing to recall is the switching losses' formula (4.10), which is also reported here:

$$P_{SW\_switching} = \left(\frac{1}{2} \cdot V_{before} \cdot I_{after} \cdot t_{on} + \frac{1}{2} \cdot V_{after} \cdot I_{before} \cdot t_{off}\right) \cdot f_{SW}$$

this equation suggests to work in DCM, because in this condition the switch current always starts from a zero value. This translates into having the $I_{after} \approx 0\,A$ and then half of the switching losses are saved, increasing the overall efficiency. For this reason, it is possible to immediately say that the previous circuit, in figure 6.8, is not the best solution, even more if the low output power level is considered. As an evidence of what has been said here, the efficiency curve, as a function of the load current, has been obtained with the simulator. Those curves are reported in figure 6.9, notice that the circuit has been tested in different conditions, before computing the efficiency and this was done in order to provide valid data.

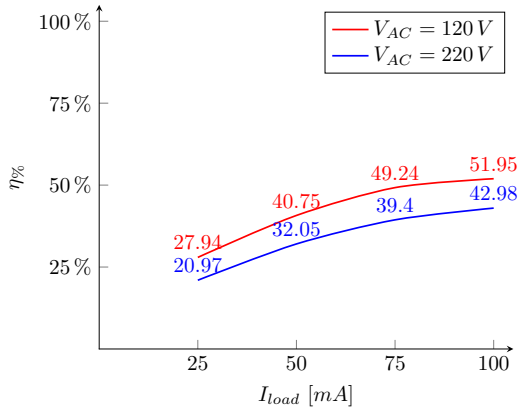


Figure 6.9: VIPer012XS efficiency in CCM working condition, self-supply mode, different loads and input AC voltages

The efficiency never exceeds the 55 % in minimum input voltage, corresponding to best working condition or maximum duty cycle, and never exceeds 45 % in maximum input voltage, the worst working condition. Then the efficiency decreases with the reduction of the load current, because feedback reduces the duty cycle to keep the output voltage constant. Some significant waveforms are reported in figure 6.10, 6.11 and 6.12, where it is possible to notice that the correct behaviour of the circuit has been verified and can be compared to the datasheet ones.

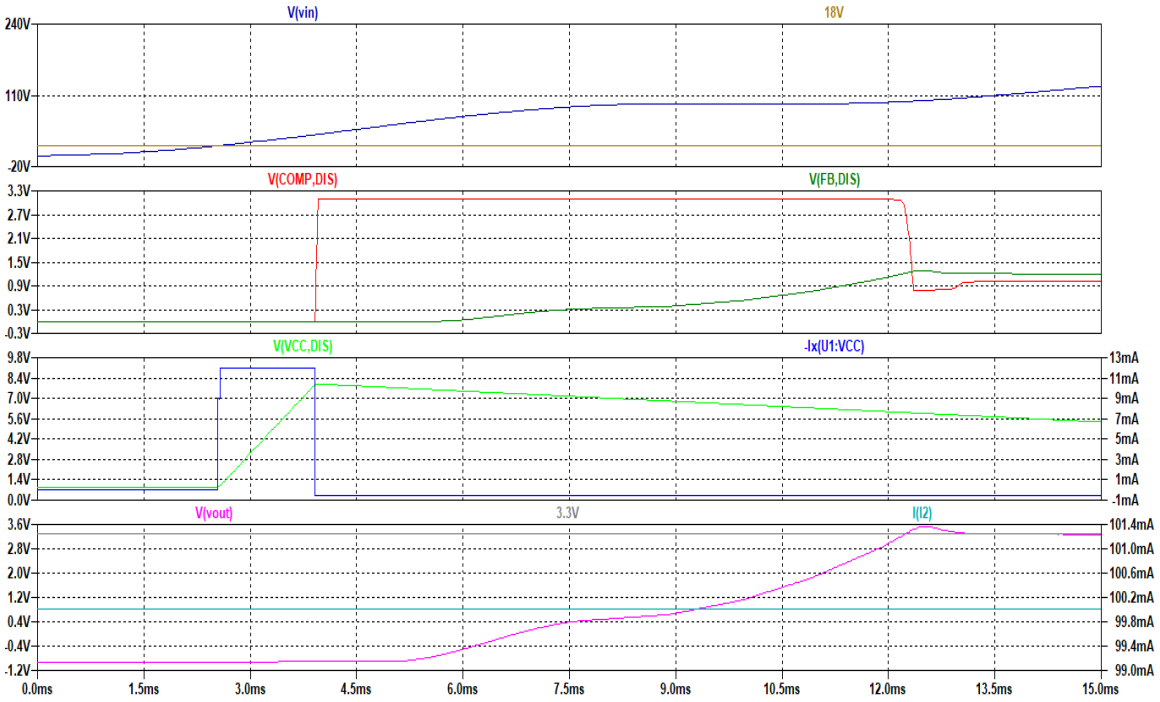


Figure 6.10: VIPer012XS start-up phase at 220 V input RMS voltage, CCM and self-supply

Working in DCM condition will improve the converter efficiency, but at the same time it will increase the peak current through the inductor and switch. As further proof of this fact, it is possible to recall equation (3.7), where it is clear that a reduction of the inductance, necessary to move the system into DCM, will increase the current stresses.

$$I_{max} = \frac{V_{OUT}}{R_L} + \frac{V_{OUT}\,(1-D)}{2Lf_{SW}}$$

The inductance value, that is able to keep the system in DCM for every conditions, can be obtained from equation (3.20) minimization, as already done in (4.4) and

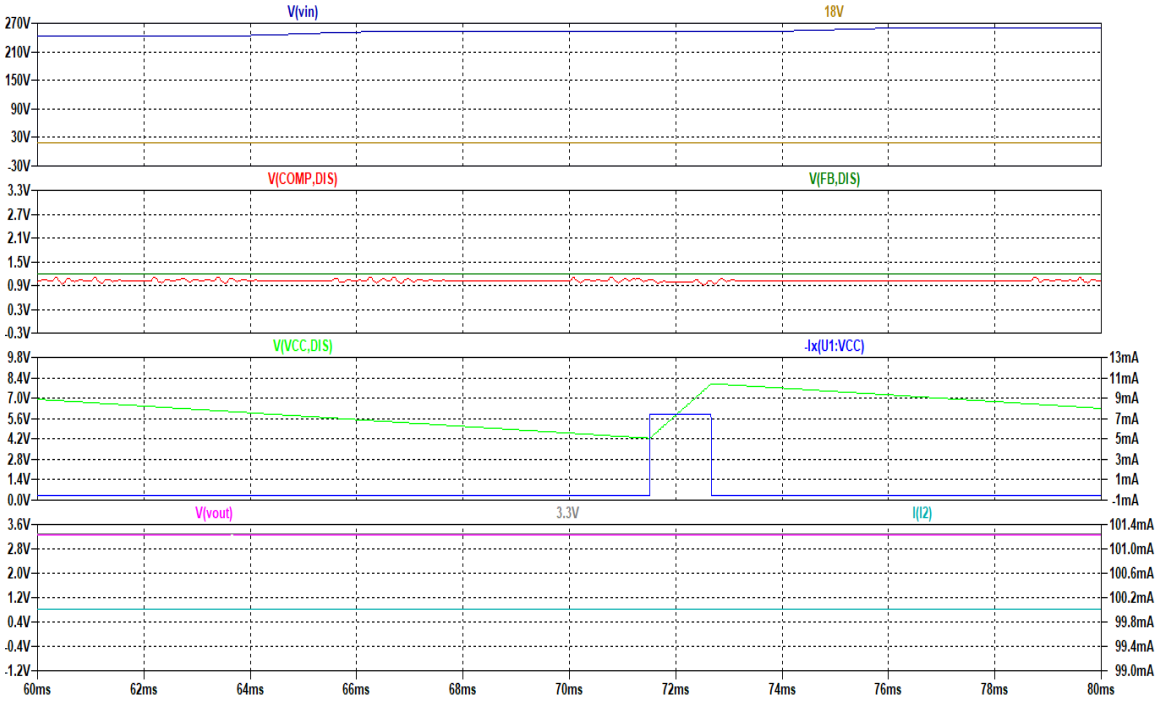


Figure 6.11: VIPer012X steady-state phase at 220 V input RMS voltage, CCM and self-supply

(4.3). The result is reported below:

$$L_{DCM} = 330\,\mu H$$

Using this value into equation (3.7) and the nominal duty cycle for $V_{AC} = 220\,V$, the peak inductor current results to be almost doubled with respect to the load one:

$$I_{L_{pk}} = 0.1\,A + \frac{3.3\,V \cdot (1 - 0.0129)}{2 \cdot 330\,\mu H \cdot 30\,kHz]} \approx 264\,mA$$

This value is higher than the I_{DLIM} one of the *VIPer012XS*, which is $\approx 240\,mA$, so to avoid the possibility to undergo *overload protection* (OVL), the *VIPer013XS* should be used instead, since it has $I_{DLIM} = 360\,mA$. This condition's occurrence has been tested with the *VIPer012X*. It is possible to see from simulation that the V_{COMP} voltage stays at V_{COMPH} for some intervals of time, this is the condition for drain current limitation. An internal counter counts the number of cycles for which this condition is met and, once reached its limit, the overload protection is enables, which will disable the PWM for $t_{RESTART}$ time period.

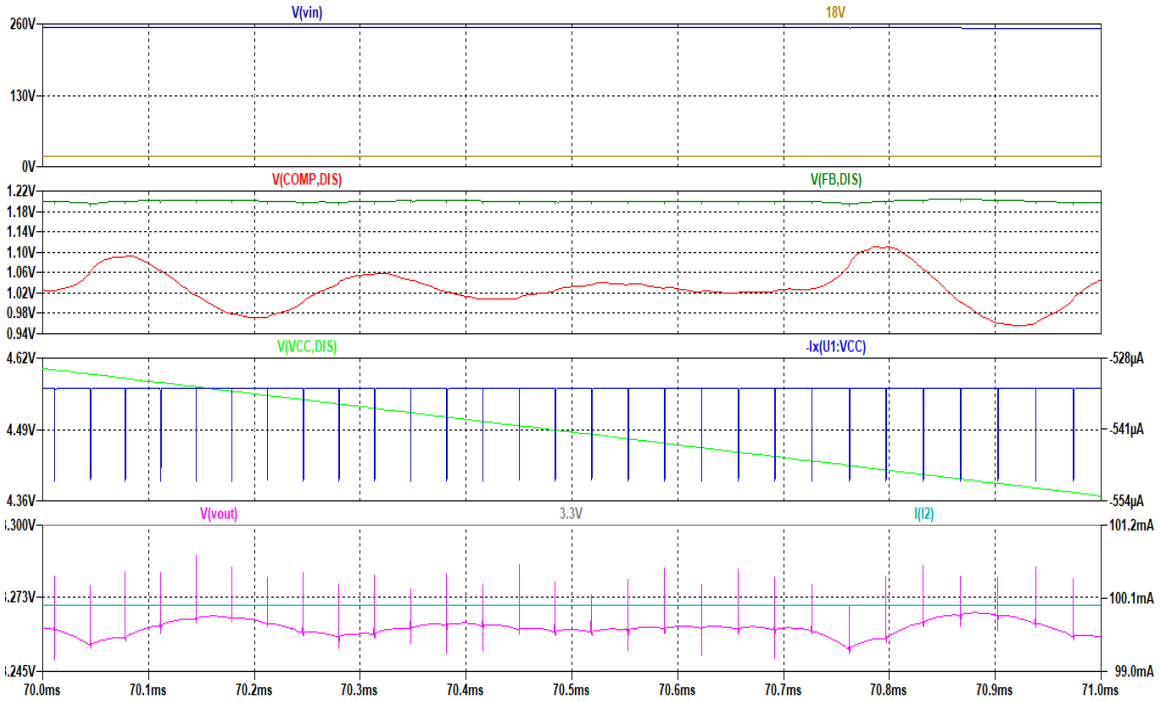


Figure 6.12: VIPer012X steady-state detail at 220 V input RMS voltage, CCM and self-supply

The *VIPer013X* is needed, as a result of the previous considerations, but does this change affect the circuit design? No, it does not, because the main change would regard the DC_{gain} of the power stage and, so, the $|COMP(f_P)|$ value, but this is like an error in a feedback system, that will be removed by the high gain. A final tuning could be needed on some elements, but this is something not so important now. The circuit used in the following step is the one reported in figure 6.13, where it is possible to see:

- the presence of the R_{limit} resistor, used to limit the inrush current, even if the *VIPer013XS* provides this feature;
- the $X2$ block, which is the *Spice* netlist of the EMI filter, designed in Chapter 5.

The **load regulation** should be considered before going any further in the simulation description, this is the converter's capability to hold the output voltage at designed value as the load changes. Circuit in figure 6.13 has been tested with different load condition, with a ".step param Iload LIST ... " *LTSpiceXVII* directive,

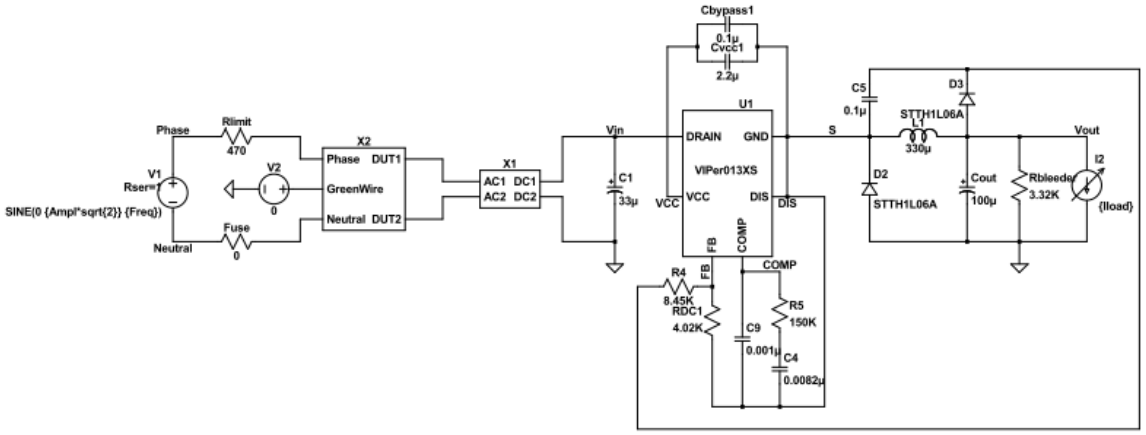


Figure 6.13: VIPer013XS used to realize a DCM buck converter

and input voltages. The results are reported in figure 6.14, where it is possible to see

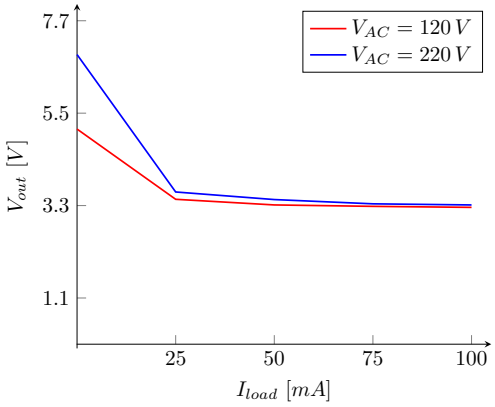


Figure 6.14: load regulation analysis for VIPer013X working in DCM and self supply mode

that, at very light load condition, the load regulation is lost, since the $3.3\,V$ value is not maintained. In this condition, only the *bleeder* resistor helps the converter to maintain a low voltage.

It is possible to evaluate the efficiency over the whole load range and, in order to do this, the *LTSpiceXVII* simulator has been used. The circuit has been simulated as if an ECoC should be respected and so five load conditions are tested (zero load current, 25 %, 50 %, 75 % and 100 % of the load maximum rated current). The resulting efficiency curves are reported in figure 6.15. Comparison between these curves and the ones in figure 6.9, it is possible to appreciate a little improvement in terms of efficiency. As expected the DCM working condition is better w.r.t. the CCM one, if this improvements is not so high, there is still an advantage, when using the first

mode: the inductance is smaller and so the area can be reduced.

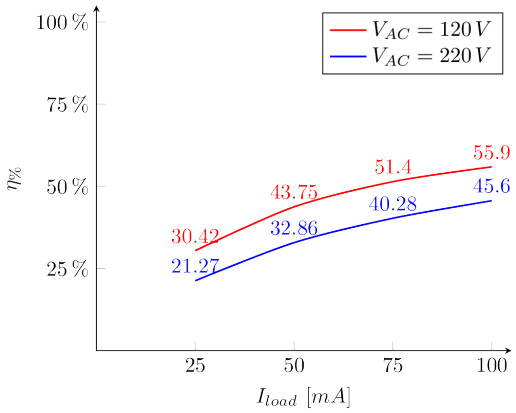


Figure 6.15: VIPer013XS efficiency in DCM and self-supply mode

6.2.3 EMI considerations

At the end of the previous chapter, an EMI filter was designed and its components have been computed having already in mind the *VIPer01* based solution. Now it is important to verify the effect of this filter, for this reason a LISN has been created in *LTSpiceXVII*, as the one discussed in Chapter 5. The LISN, as in an real measurement, will be placed between the AC power source and the *Device Under Test* (**DUT**). The circuit with the EMI filter and the LISN is reported in figure 6.16 and the one without the filter is simply omitted, for obvious reasons. The circuits have

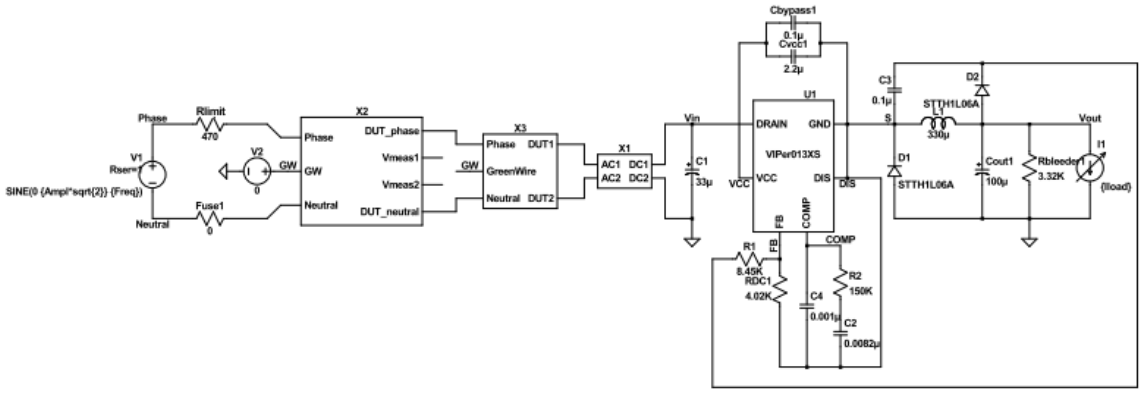


Figure 6.16: VIPer013XS buck converter, with EMI filter and LISN, to evaluate the effect of the presence of the filter

been simulated for a time period equal to 240 ms and the start-up phase is kept. Once

the simulation has been completed, the *Fast-Fourier Transform* (**FFT**) of the voltage onto the V_{meas1} and V_{meas2} has been computed, with the *LTSpiceXVII* simulator. The common mode conducted emission is related to the *FFT* of the $V_{meas1} - V_{meas2}$ difference and the differential mode one is related to the *FFT* of the $V_{meas1} - V(GW)$ difference, where *GW* stands for *Green Wire*.
An additional step should be considered before analysing the obtained results, the relationship between dB_V and $dB_{\mu V}$. Using the definition, it is clearly possible to say what reported in equation (6.15).

$$dB_{\mu V} = 20 \cdot \log(V) + 120\, dB \tag{6.15}$$

Equation 6.15 allows to scale the obtained results to the required limits, in accordance with *CISPR 22*, and vice versa. Simulation's results are reported in figure 6.17 and figure 6.18. It was not possible to cover the whole frequency range required,

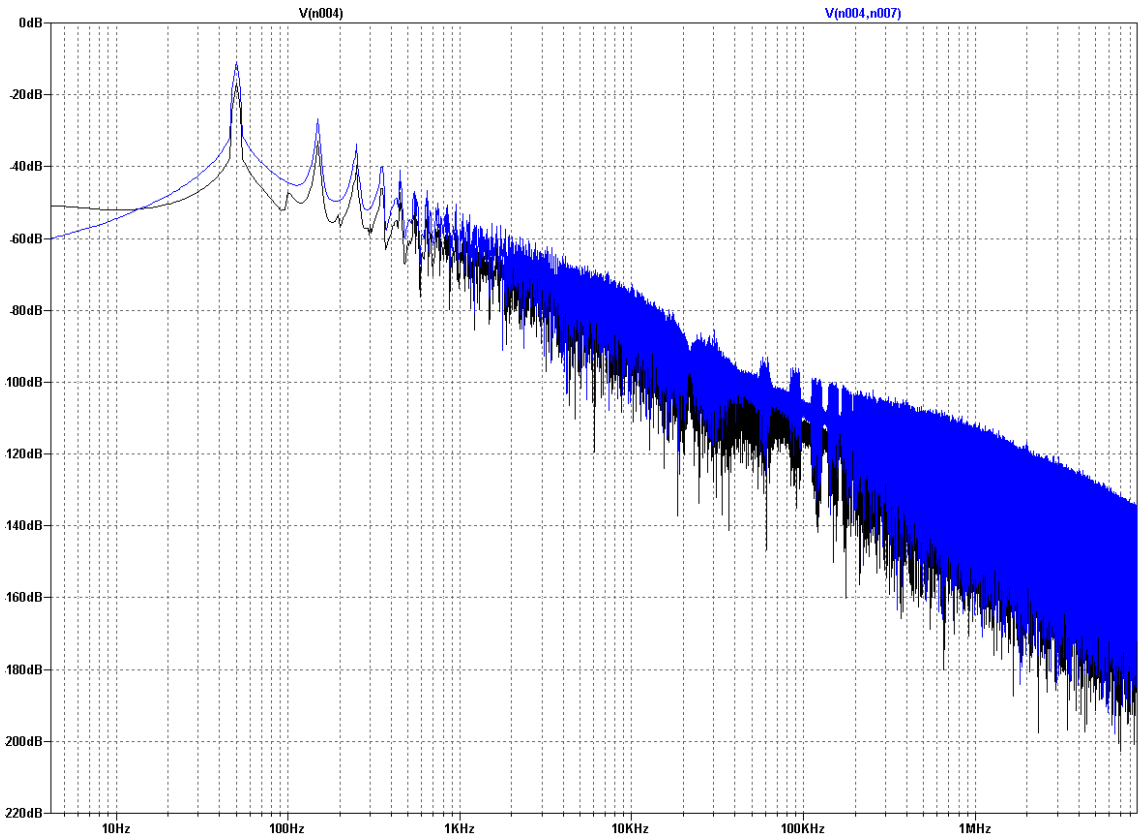


Figure 6.17: FFT of the common mode voltage, in blue, and the differential mode one, in black, without EMI filter

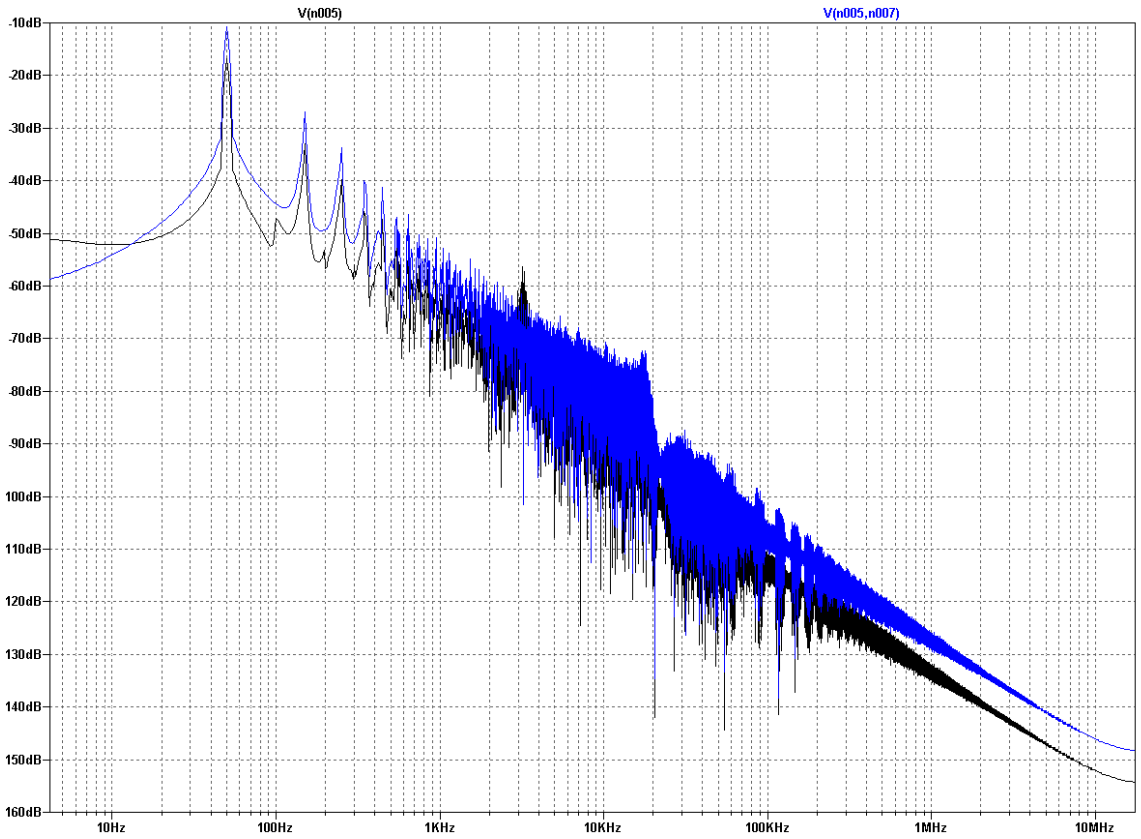


Figure 6.18: FFT of the common mode voltage, in blue, and the differential mode one, in black, with EMI filter

because increasing the number of points for the *FFT* causes the simulator to crush. In any case, the behaviour is understandable and the EMI filter's effect is clear. The translation of the *CISPR 22* limits, using equation 6.15, results in an accepted situation.

Following figure 6.19 and 6.20, represent the time domain behaviour of the common mode voltage and differential mode one, with and without the filter respectively.

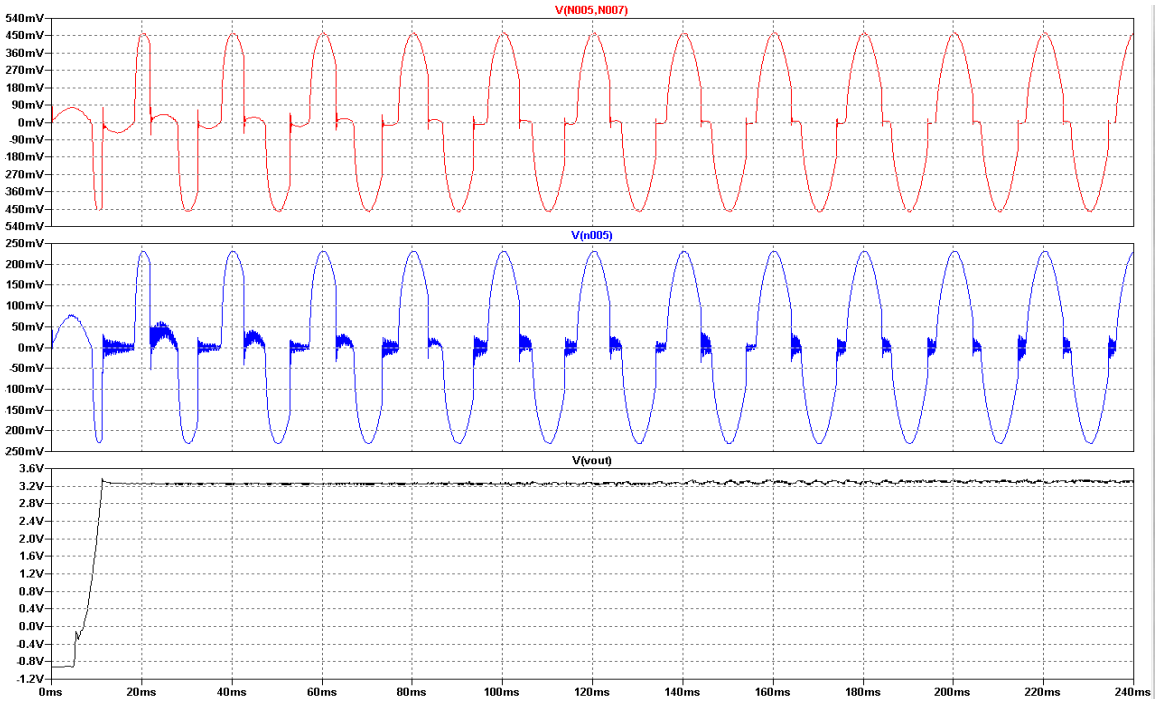


Figure 6.19: time domain response of the common mode voltage, in blue, and the differential mode one, in black, with EMI filter

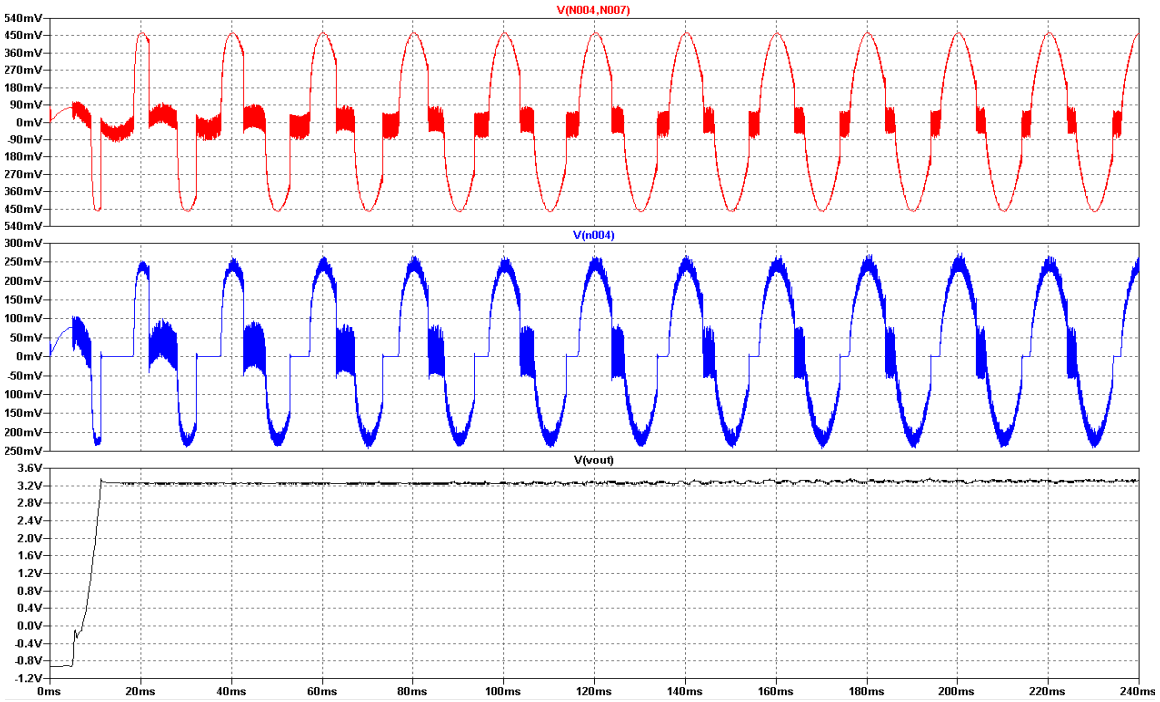


Figure 6.20: time domain response of the common mode voltage, in blue, and the differential mode one, in black, without EMI filter

6.3 Conclusions

In this chapter the *VIPer01* has been used to design and simulate a more realistic circuit, w.r.t. the one in Chapter 4. The feedback design problem has been faced and simulations have been carried out, in order to find the final circuit. CCM and DCM working conditions have been compared and the second one leads to better results. In the end, the effect of the EMI filter, designed in the final part of Chapter 5, has been analysed.

CHAPTER 7

Proposed solution to improve efficiency

In this chapter, a possible solution to the high step-down problem is presented and it has been derived from the research conducted in Chapter 2. In particular, a capacitive voltage divider is used at the input side of the converter, before the full-wave rectifier. This solution is explained in detail, formulae are derived and the circuit is simulated under different load conditions. Secondly, this circuit is applied to various buck converter integrated circuits and a comparison, between the different solutions, is given. Pros and cons are highlighted and the different solutions' costs are compared.

7.1 Proposed solution

The main problems, when facing a buck converter stepping down a very high voltage for low output power applications, are:

high voltage causes the converter to work with reduced duty cycle, components should be able to withstand this voltage level and it is possible to expect higher switching losses;

small duty cycle limits the working frequency, otherwise it is possible to not respect the minimum on time of the power switch, free-wheeling diodes dissipates more and the MOSFET is used for a reduced portion of time;

stringent power losses high efficiency requirements can not be easily accomplished. Consider for example the case in exam where $P_{out} = 1/3\,W$ and suppose

to require at least 90 % of efficiency, the resultant input power should be $P_{in} = 370\,mW$ and so the overall losses should be around $40\,mW$, which is a very small value. This means that proper design choices should be made and they can affect both converter operating modes, components selection and also topology choice.

High voltage and small duty cycle are clearly related at this point and a reduction of the input voltage can bring obvious advantages.

7.1.1 Reducing the high input voltage

In Chapter 2, the main solution to the high step-down problem is the use of a capacitive divider, but all the topology found in literature were meant for higher power applications. The solution presented here is a simple capacitive voltage divider, now the EMI filter will be neglected in order to simplify the following computation. Consider the circuit reported in figure 7.1, here it is possible to see a capacitive voltage divider formed by C_1 and C_2, a resistor R_1 used as an inrush current limiter, a resistor R_2 used to discharge C_1 once the device is disconnected form the AC line, a full bridge rectifier, the C_3 capacitor representing the input one for a typical buck and finally a current source I_{load}, modelling the current absorbed by the converter both for the output and supply current. The following assumption should be taken into

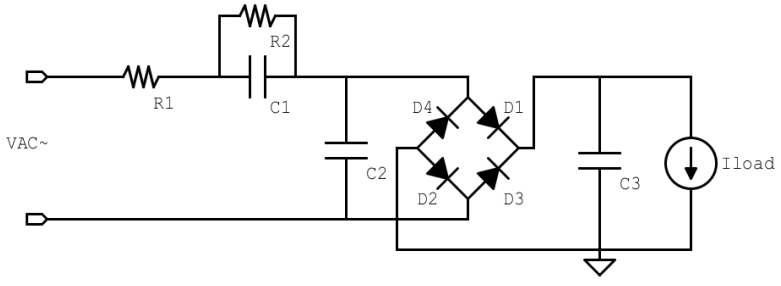


Figure 7.1: reference circuit used to derive the following results and modelling the buck converter as a constant current source

account:

V_{C_3} this voltage is supposed to be constant, with a small ripple superimposed;

I_{load} it is considered as a constant value;

V_{AC} is the line voltage and only half of a line period is analysed;

$v_{C_2}(t)$ is the voltage onto the C_2 capacitor and it is supposed to be a sine wave.

The analysis will be conducted considering an energy balance between the energy required by the buck at its input and the one provided by the capacitive divider. The first step is to consider the buck input side power, this one con be computed as reported in (7.1).

$$P_{IN} = V_{C_3} \cdot I_{load} \tag{7.1}$$

The I_{load} should take into account, as already said, both the load current and the supply one. It is important then to recall the ideal equations of a buck converter (7.2), in order to compute the load current needed back into the input side.

$$\begin{cases} V_{out} = D \cdot V_{in} \\ I_{out} = I_{in}/D \end{cases} \tag{7.2}$$

It is clear that $V_{in} = V_{C_3}$, for this reason the duty cycle is given and, as a consequence, also the I_{in}. The I_{load} is the sum of two components: the I_{in} one, previously calculated, and the supply current. The latter one can be obtained from datasheet, simulations or by simply increasing the I_{in} to a reasonable level.
The main focus is the energy, as already said, an this can be computed from (7.1) as reported in (7.3):

$$E_{IN} = P_{IN} \cdot \Delta T = \frac{P_{IN}}{2f_{line}} \tag{7.3}$$

This energy comes, for part of T_{line}, from the C_3 and, for the rest of the time interval from the left most part of the circuit. This is much more clear considering figure 7.2, here both the $v_{C_2}(t)$ voltage and the V_{C_3} one are plotted. The diodes D_1 and D_2 are forward biased only when $v_{C_2}(t)$ voltage is greater than the V_{C_3} and in that period of time energy is provided to the buck by the capacitive divider. For this reason it is possible to define a "line duty cycle", which will be denoted as D_{line} in the following passages, and it represents the period of time for which diodes are not conducting. As a consequence, the input energy can be divided in two contribution, as reported in (7.4).

$$E_{IN} = \frac{P_{IN} D_{line}}{2f_{line}} + \frac{P_{IN}(1 - D_{line})}{2f_{line}} \tag{7.4}$$

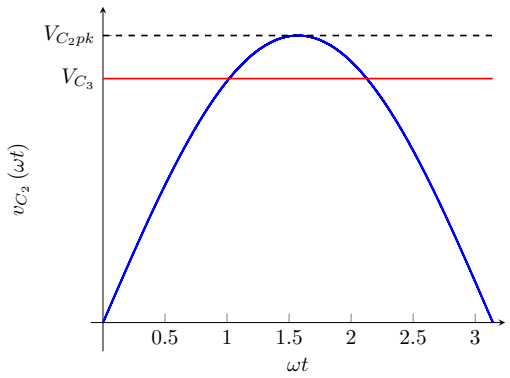


Figure 7.2: $v_{C_2}(t)$ behaviour on a line period

When only the C_3 capacitor provides energy to the buck converter, the equivalent circuit is the one reported in figure 7.3. This is a capacitor discharged by a constant current source and it is possible to obtain an inequality for the C_3 capacitor ripple, from its constitutive equation.

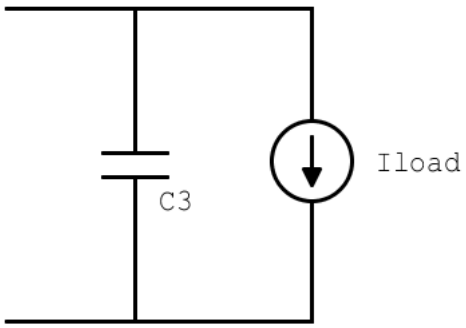


Figure 7.3: equivalent circuit when diodes are not conducting

$$\begin{cases} i_{C_3} = C_3 \frac{dv_{C_3}}{dt} \\ i_{C_3} = I_{load} \\ dv_{C_3} = \Delta V_{C_3} \\ dt = \Delta T = \frac{T_{line} D_{line}}{2} \end{cases} \rightarrow \quad I_{load} = C_3 \cdot \frac{\Delta V_{C_3} \cdot 2 \cdot f_{line}}{D_{line}} \tag{7.5}$$

$$D_{line} = \frac{2 f_{line} C_3 \Delta V_{C_3}}{I_{load}} \tag{7.6}$$

A duty cycle should always be less than 1 and, imposing this condition into (7.6), it is possible to find a limit for the ripple voltage onto the C_3 capacitor, as reported in 7.7. For example, let's suppose to have $I_{load} = 25\,mA$, $f_{line} = 50\,Hz$ and $C_3 = 330\,\mu F$,

with those values the voltage ripple should be lesser than $757\,mV$ and the resulting "line duty cycle" is 0.792.

$$\Delta V_{C_3} < \frac{I_{load}}{2 f_{line} C_3} \tag{7.7}$$

The energy lost by the C_3 capacitor, during the D_{line} phase, can be computed as reported in 7.9 and, for a better understanding, consider the waveform in figure 7.4.

$$\Delta E_{C_3} = \frac{1}{2} \cdot C_3 \cdot \left(V_{C_3 final}^2 - V_{C_3 initial}^2\right) \tag{7.8}$$

$$V_{C_3 final} = V_{C_3 initial} - \Delta V_{C_3}$$

$$\Delta E_{C_3} = \frac{1}{2} \cdot C_3 \cdot \left(\Delta V_{C_3}^2 - 2\Delta V_{C_3} V_{C_3 initial}\right) \tag{7.9}$$

The C_2 capacitor should provide the lost energy to C_3 and, at the same time, to the

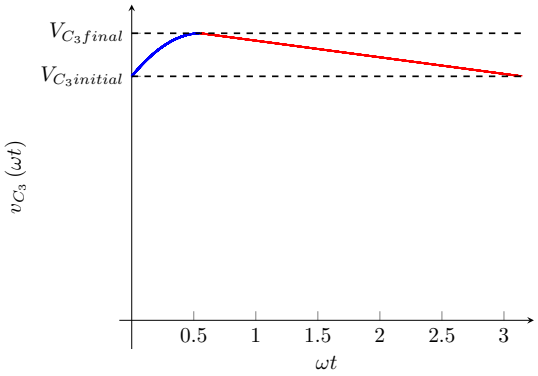


Figure 7.4: voltage waveform for the C_3 capacitor

buck, but the exchange should happen in a time period equal to $(1 - D_{line}) \cdot \frac{T_{line}}{2}$. This amount of energy is exiting from C_2, as a consequence, a negative value is expected and the equation is the (7.10) one, where the two contribution can be recognized.

$$\Delta E_{C_2} = \Delta E_{C_3} + \frac{P_{IN} \cdot (1 - D_{line})}{2 f_{line}} = \frac{1}{2} \cdot C_2 \cdot \left(V_{C_2 final}^2 - V_{C_2 initial}^2\right) \tag{7.10}$$

The $V_{C2initial} = V_{pk}$ value depends onto the capacitive partition between C_1 and C_2, it will be considered like the unknown in following passages. $V_{C2final}$, instead, is the voltage value the C_2 capacitor should reach in order to bring diodes in forward bias condition and will correspond to $V_{C_3 final}$, like in figure 7.4, plus two diode voltage

drops V_D, as reported in (7.11).

$$V_{C_2 final} = V_{C_3 initial} - \Delta V_{C_3} + 2V_D \tag{7.11}$$

Before going any further, another approximation should be considered and applied, to get a better result; during the diodes conduction, it is not only C_2 that provides energy to C_3 and the buck, but there is also the effect of C_1. It is possible to define an equivalent capacitance and substitute that one in place of C_2. To find its value, the circuit in figure 7.5 has been considered and some approximation have been performed: $R_1 < X_{C_1}$ and $X_{C_1} < R_2$, where $R_1 \leq 470\,\Omega$ and $R_2 = 1\,M\Omega$. Using the

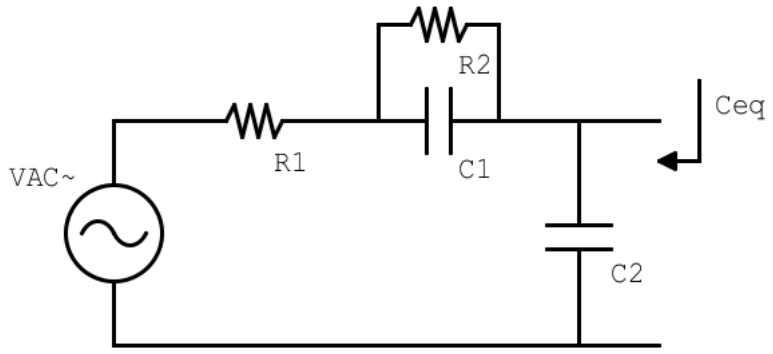


Figure 7.5

previous approximation, the equivalent capacitance is the parallel between C_1 and C_2, as reported in 7.12.

$$C_{eq} = C_1 + C_2 = C_1 \left(1 + \frac{C_2}{C_1}\right) \tag{7.12}$$

Substituting C_{eq} in place of C_2 in (7.10), together with the expression of C_3 lost energy in (7.9), it is possible to derive an expression for V_{pk}:

$$\begin{aligned} \Delta E_{C_{eq}} = \Delta E_{C_3} + \frac{P_{IN} \cdot (1 - D_{line})}{2 f_{line}} &= \frac{1}{2} \cdot C_2 \cdot \left(V^2_{C_2 final} - V^2_{C_2 initial}\right) \\ \frac{1}{2} C_{eq} \left[\left(V_{C_3 initial} - \Delta V_{C_3} + 2V_D\right)^2 - V^2_{pk}\right] &= \frac{1}{2} C_3 \left(\Delta V^2_{C_3} - 2\Delta V_{C_3} V_{C_3 initial}\right) + \\ &- \frac{P_{IN}\,(1 - D_{line})}{2 f_{line}} \end{aligned} \tag{7.13}$$

$$V_{pk}^2 = (V_{C_3initial} - \Delta V_{C_3} + 2V_D)^2 - \frac{C_3\left(\Delta V_{C_3}^2 - 2\Delta V_{C_3} V_{C_3initial}\right)}{C_1\left(1 + C_2/C_1\right)} + \\ + \frac{P_{IN}\left(1 - D_{line}\right)}{C_1 f_{line}\left(1 + C_2/C_1\right)} \tag{7.14}$$

Equation (7.14) can be written in a simpler readable way, as reported below in (7.15), notice also that, from (7.13) to (7.14), the sign of the term associated to the energy absorbed by the buck in the $(1 - D_{line})$ interval has been changed, because this energy should be extracted from the rest of the circuit.

$$V_{pk} = \sqrt{a + \frac{c - b}{1 + C_2/C_1}} \tag{7.15}$$
$$a = (V_{C_3initial} - \Delta V_{C_3} + 2V_D)^2$$
$$b = \frac{C_3}{C_1} \cdot \left(\Delta V_{C_3}^2 - 2\Delta V_{C_3} V_{C_3initial}\right)$$
$$c = \frac{P_{IN} \cdot (1 - D_{line})}{C_1 \cdot f_{line}}$$

The peak voltage onto C_2 can also be obtained with a simple capacitive voltage division of the V_{AC}, the resulting system is reported in (7.16).

$$\begin{cases} V_{pk} = \sqrt{a + \frac{c-b}{1+C_2/C_1}} \\ V_{pk} = \frac{V_{AC}\sqrt{2}}{(1+C_2/C_1)} \end{cases} \tag{7.16}$$

The best way to find a solution for this system is a graphical approach, for this reason MATLAB can be used and a typical result is reported in figure 7.6, after having imposed values to the whole set of parameters ($V_{C_3initial}$, V_D, I_{load}, etc...). Each colour is associated to a different C_1 value, notice that this kind of capacitor, connected in series with the mains, has to respect some standards like: stability, capability of self-healing, has to fail as an open circuit and can not be a polarized one, as reported in [21]. For those reasons its capacitance is limited to few μF and the cost is quite high.

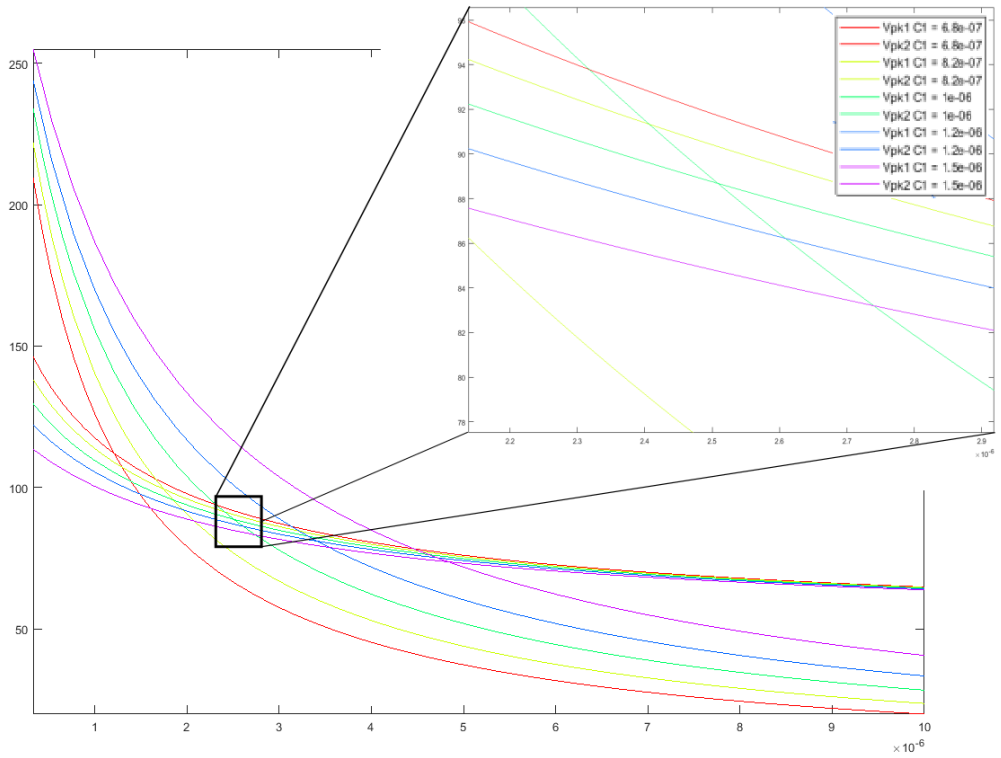


Figure 7.6: typical graphical result obtained with MATLAB, when solving system in (7.16)

7.1.2 Capacitive divider simulation

In the previous section the capacitive voltage divider solution has been discussed and now it is important to verify that the circuit is able to keep the voltage constant for the subsequent buck. This voltage is not required to be perfectly determined and is allowed to fluctuates, the output voltage of the buck should be regulated by some kind of feedback. A particular interesting fact to analyse is the output voltage of the divider as a function of the current load I_{load}, this can be easily simulated in LTSpice with a simple ".step" directive. The circuit under simulation is the one reported in figure 7.7, where it is possible to recognize both the full-wave rectifier (X1) and the EMI filter (X2). The first one is realized with 4 *MRA4007T3G* rectifiers and the second as reported in the dedicated section. The previous circuit has been simulated with $C_1 = 1\,\mu F$, $C_5 = 2.2\,\mu F$, $C_4 = 33\,\mu F$ and a current load changing from $0\,mA$ to $50\,mA$ with steps of $5\,mA$. The resulting behaviour is the one in figure 7.8, where it is clear that increasing the output current the steady state X voltage is

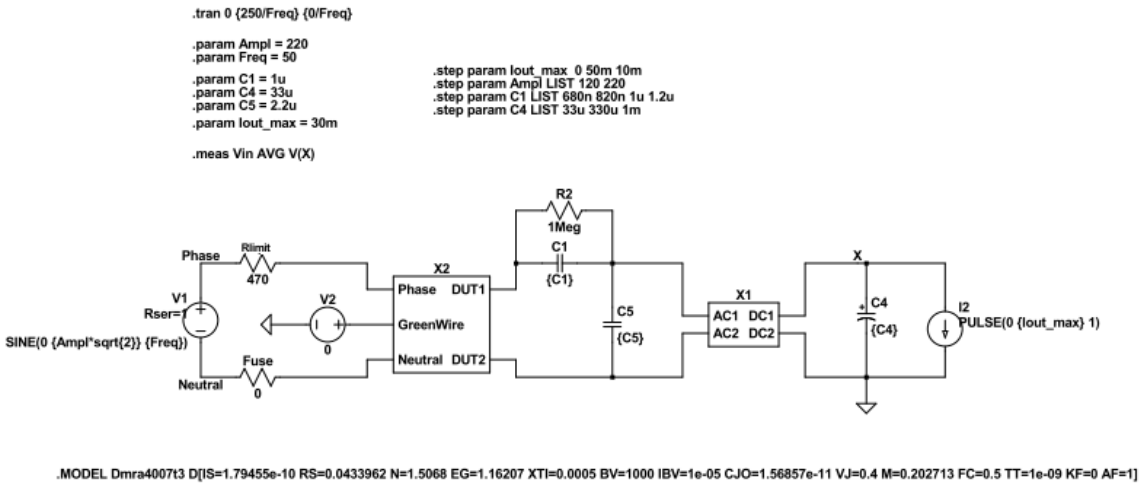


Figure 7.7: capacitive voltage divider simulation schematic

reduced and the ripple increased. On the other hand, when no load is applied, the X node voltage increases and can exceed the capacitor voltage rating, causing obvious problems. Another test that can be performed is the one where the load current is

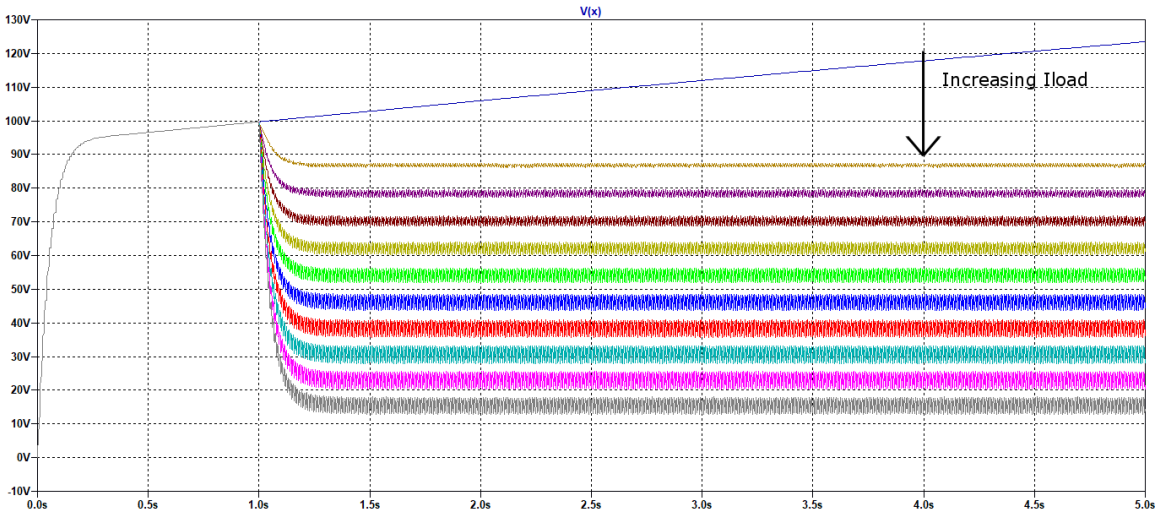


Figure 7.8: capacitive voltage divider output voltage response as a function of the output load

kept constant and the C_1 capacitor is increased. It is possible to expect an increase of the output voltage, because the reactance of C_1 is lower and thus more current can cross the capacitor, as reported also in [16], [18], [19] and [17]. The simulation result, reported in figure 7.9, is in accordance with what said earlier. The C_5 capacitance value can be used to change the X voltage value, as specified also by mathematical

results reported in the previous section, and the C_4 one can be increased to reduce the ripple and get, if needed, a much more stable output voltage.

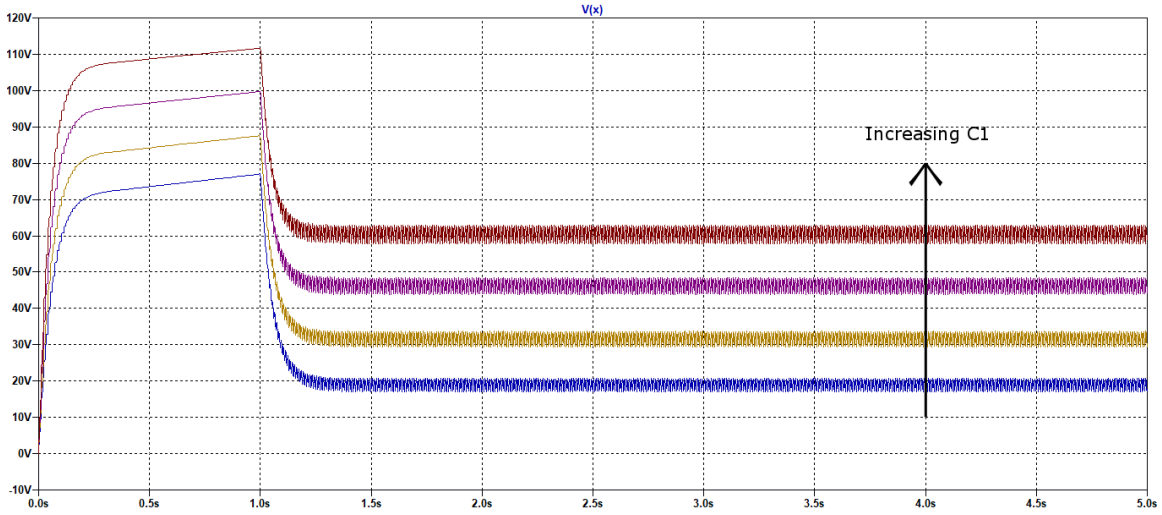


Figure 7.9: capacitive voltage divider output voltage response as a function of the C_1 capacitor

7.1.3 Conclusions

In this section, a possible solution to the high input voltage/high step down ratio problem has been found. It allows to reduce stresses over subsequent components, increase the efficiency of the converter and, at the same time, it enlarges the amount of possible devices that can be used for the scope. In the following passages, this solution will be tested with some converters and the results will be compared with the ones obtained with the *VIPer013X*.

7.2 Using the capacitive divider in real circuits

A capacitive divider can be used to reduce the high input voltage deriving from the main line, this approach can increase both efficiency and the pool of possible circuits available onto the market, giving more solutions to the problem in exam. Now the input voltage, to be fed to the converter, is almost a design choice; for example, if the converter supports an input voltage range from few volts to 100 V, the capacitive divider can be designed to provide this value. It is still important to verify that a

steady state condition can be reached: the converter should not absorb too much current from the cap divider, otherwise the input voltage will tend to $0\,V$ and then the circuit will not work any more.

7.2.1 VIPer01 with capacitive divider

The first step is to understand the effects of capacitive divider on the already designed buck converter, realized with the *VIPer013X*. The circuit reported in figure 6.13 is now modified as in figure 7.10, the main changes are:

Inrush current resistor the R_{limit} resistor is present to reduce the inrush current problem, that occurs at start-up when every capacitor in the circuit is discharged. Let's suppose to have the worst condition: $V_{AC} = 220\,V$ and the maximum allowable current around $1\,A$, then the R_{limit} should have a value around $330\,\Omega$ and, to play safe, $R_{limit} = 470\,\Omega$ is selected. This value is not the best solution in low power application, because, even with a small *RMS* current let's say around $60\,mA$, the dissipated power is very high $\approx 1.7\,W$. At the start-up it is acceptable, but in steady state it is not and to solve this problem the solution is to short it with a bidirectional switch, like an Solid-State-Relay (SSR), as the *VOR2142B8*. This relay shows an R_{on} resistance of few tens of Ω and so dissipated power is highly reduced, but the cost of this kind of devices is still quite high. For the previous reason, a *phototriac* could be used, like the *VO2223B-X017T*, and it should be driven directly by the output once steady state condition is reached;

Fast recovery diode the two diodes are now selected with a lower breakdown voltage, so *STTH1L06* are replaced by *STTH1R02*, which have $200\,V$ of breakdown voltage.

The efficiency evaluation is performed in a manner resembling what suggested by the *Europen Energy Efficiency Platform* (E3P) in [35], which follows [36] as a test method. In those documents, it is required to report at least 5 main points for the efficiency curve, as a function of the load current, and they are at 100 %, 75 %, 50 %, 25 % and no load input power. It is also required to define an average efficiency. The measurements are then performed after a *warm-up phase* and the device should have

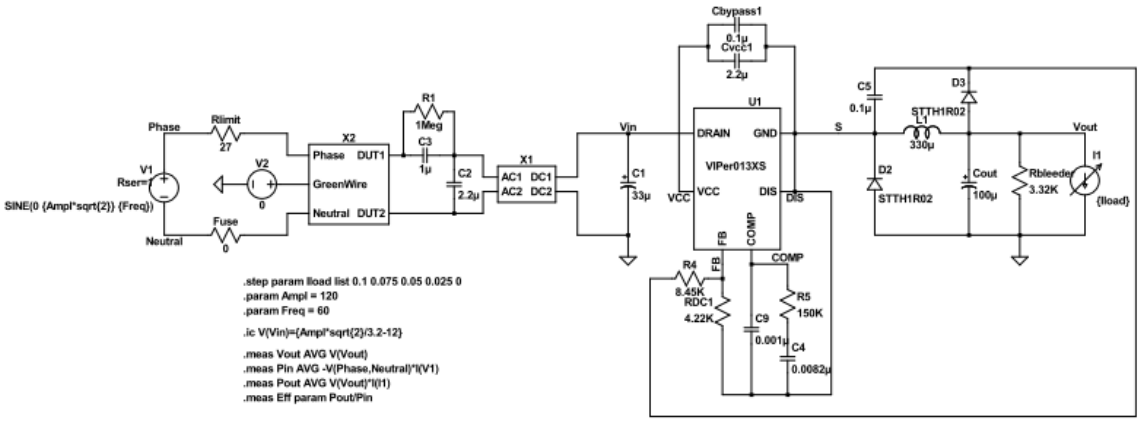
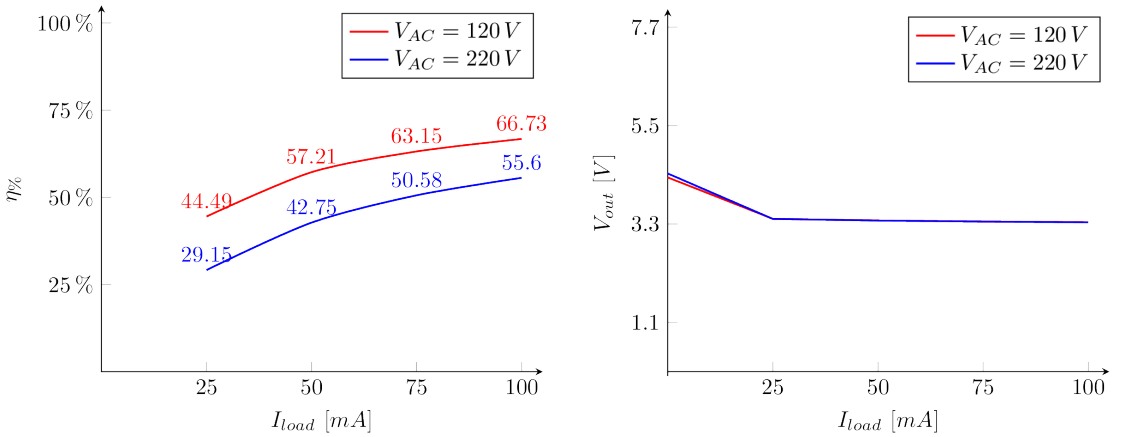


Figure 7.10: capacitive divider applied to the VIPer013X

reached a steady state condition.

In order to follow those requirements, the circuit is first simulated for a long period of time, in which the steady state condition for the input voltage is found, and then the initial condition onto the C_1 capacitor voltage is imposed. An ".ic" *LTSpiceXVII* directive is used for the scope. The efficiency is computed with a ".meas" directive, which can also be seen in figure 7.10, in the meantime the load current is changed from maximum to $0\,A$. Also the mean value of the output voltage is measured with a ".meas" directive, therefore a load regulation plot can be obtained. Figure 7.11 shows



(a) efficiency *(b)* load regulation

Figure 7.11: efficiency and load regulation of VIPer013X with the capacitive divider solution

the simulation results, the efficiency is shown as a function of the output current in 7.11a and the load regulation is plotted in 7.11b. The previous results are also shown

in table 7.1 for the $120\,V$ case and in table 7.2 for the $220\,V$ one. Those results

	No load	25 %	50 %	75 %	100 %	Average
DC output current (mA)	0	25	50	75	100	-
DC output voltage (V)	4.34	3.42	3.38	3.36	3.34	-
DC output power (mW)	0	85.4	168.9	251.8	334.1	-
AC input voltage (V)	120	120	120	120	120	-
AC input frequency (Hz)	60	60	60	60	60	-
AC input power (mW)	90.0	191.9	295.3	398.7	500.7	-
Power consumed by UUT (mW)	90.0	106.5	126.4	146.9	166.6	-
Efficiency	-	44.5 %	57.2 %	63.1 %	66.7 %	57.9 %

Table 7.1: *VIPer013X* simulation results for $120\,V$ case

	No load	25 %	50 %	75 %	100 %	Average
DC output current (mA)	0	25	50	75	100	-
DC output voltage (V)	4.43	3.41	3.38	3.35	3.34	-
DC output power (mW)	0	85.3	168.8	251.5	333.7	-
AC input voltage (V)	220	220	220	220	220	-
AC input frequency (Hz)	50	50	50	50	50	-
AC input power (mW)	188.8	292.8	394.9	497.3	600.3	-
Power consumed by UUT (mW)	188.8	207.5	226.1	245.8	266.6	-
Efficiency	-	29.1 %	42.7 %	50.6 %	55.6 %	44.5 %

Table 7.2: *VIPer013X* simulation results for $220\,V$ case

will be compared with the others, obtained with different circuits, at the end of this chapter and, at the same time, they will be compared with the solution without the capacitive divider.

7.2.2 LT8630 with capacitive divider

The *LT8630* is a synchronous buck converter, which integrates the control section and the high/low side power MOSFETs. This circuit has a wide input voltage range

(from $3\,V$ to $100\,V$) and it has a current load capability of $0.6\,A$. Since its input voltage range is well below the V_{AC} line, this circuit results particularly suited for a capacitive voltage divider test. In this case the maximum allowable input voltage is $100\,V$, so the divider should provide a lower value in worst condition, i.e. when the input $V_{AC} = 220\,V$. Using the formulae in (7.16) and with additional adjustment, the C_1 should be larger or equal to $1\,\mu F$ and their ratio (C_2/C_1) should be larger than 3.

The remaining part of the circuit is designed following the specifications provided in the datasheet [37] and the resulting circuit is reported in figure 7.12. The *LT8630* has also an enable-pin, that can be used to program a minimum input voltage threshold, and this is particularly useful in this case, if the input capacitor has to reach a particular value before turning on the device. This pin has a hysteresis which will cause the device to stop switching when the input falls a little bit below the threshold.

Also in this case, the efficiency is computed with a ".meas" directive, in the meantime

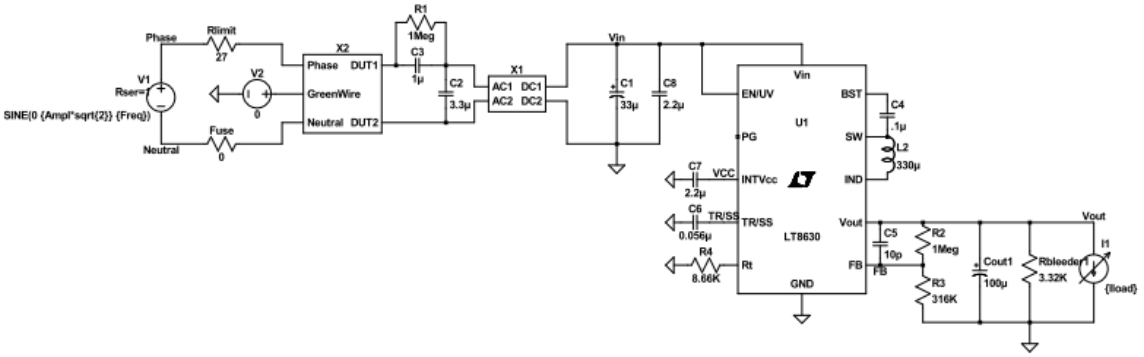
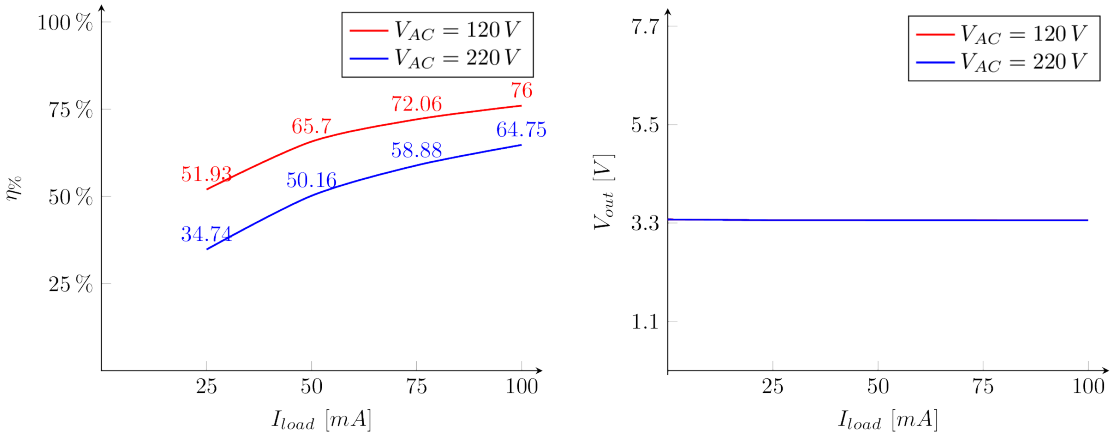


Figure 7.12: capacitive divider applied to the LT8630

the load current is changed from maximum to $0\,A$. Also the mean value of the output voltage is measured with a ".meas" directive, therefore a load regulation plot can be obtained.

Figure 7.13 shows the simulation results, the efficiency is shown as a function of the output current in 7.13a and the load regulation is plotted in 7.13b. The previous results are also shown in table 7.3 for the $120\,V$ case and in table 7.4 for the $220\,V$ one.



(a) efficiency *(b)* load regulation

Figure 7.13: efficiency and load regulation of LT8630 with the capacitive divider solution

	No load	25 %	50 %	75 %	100 %	Average
DC output current (mA)	0	25	50	75	100	-
DC output voltage (V)	3.38	3.36	3.36	3.36	3.36	-
DC output power (mW)	0	84.1	168.1	252.0	335.9	-
AC input voltage (V)	120	120	120	120	120	-
AC input frequency (Hz)	60	60	60	60	60	-
AC input power (mW)	68.7	161.2	255.9	349.7	441.9	-
Power consumed by UUT (mW)	68.7	77.1	87.8	97.7	106	-
Efficiency	-	51.9 %	65.7 %	72.1 %	75.9 %	66.4 %

Table 7.3: *LT8630* simulation results for 120 V case

	No load	25 %	50 %	75 %	100 %	Average
DC output current (mA)	0	25	50	75	100	-
DC output voltage (V)	3.38	3.36	3.36	3.36	3.36	-
DC output power (mW)	0	84.0	168.0	252.0	335.9	-
AC input voltage (V)	220	220	220	220	220	-
AC input frequency (Hz)	50	50	50	50	50	-
AC input power (mW)	157.7	241.9	335.0	428.0	518.8	-
Power consumed by UUT (mW)	157.7	157.9	167.0	176.0	182.9	-
Efficiency	-	34.7 %	50.1 %	58.9 %	64.7 %	52.1 %

Table 7.4: *LT8630* simulation results for 220 V case

7.2.3 LTC3638 with capacitive divider

The *LTC3638* is a step-down regulator, which integrates on the same chip both the control part and the power MOSFET. It is designed for a wide input voltage range, up to $140\,V$, and the maximum output current is $250\,mA$. Its specifications makes this circuit suited for a capacitive divider test. It also shows a reduced number of components to work, since the output voltage can be programmed by a proper connection of pins V_{PRG1} and V_{PRG2}, as declared in [38]. Also in this case there is a run-pin, that can be used as an enable-pin to decide when the input voltage is sufficient to let the conversion start. The final circuit is shown in figure 7.14, where it is possible to see the capacitive divider and the *STTH1R02* diode.

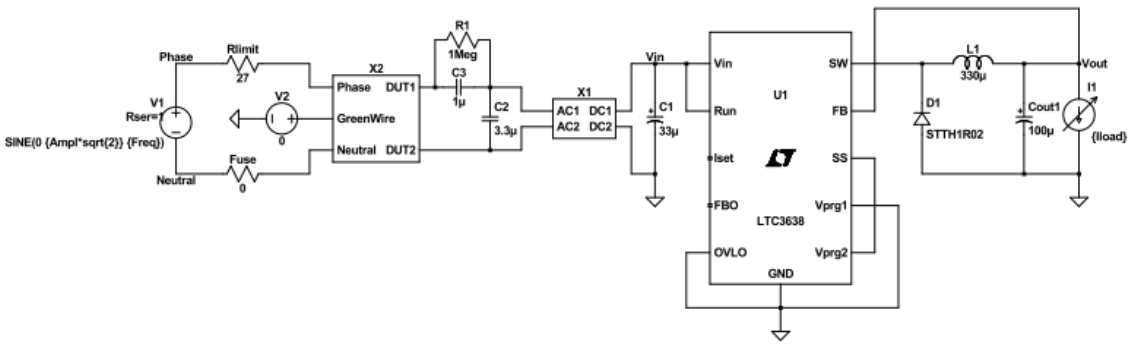
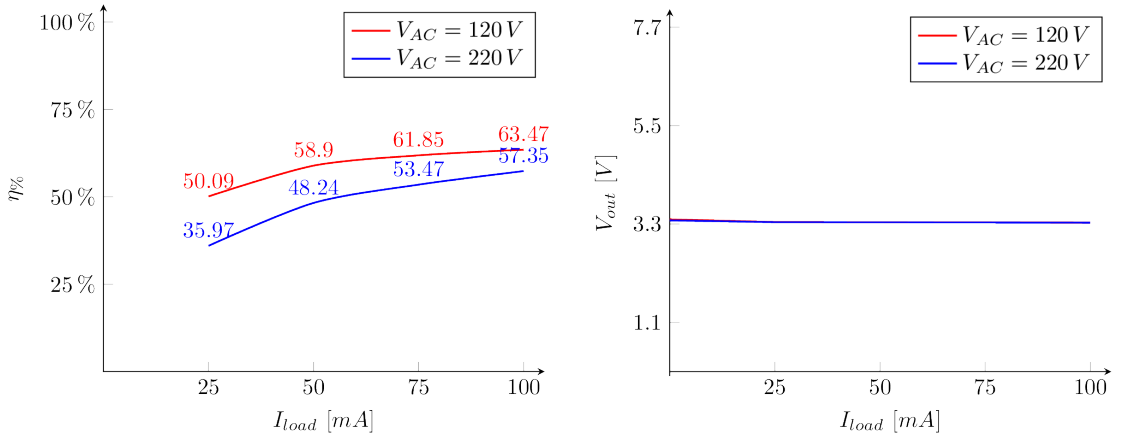


Figure 7.14: capacitive divider applied to the LTC3638



(a) efficiency

(b) load regulation

Figure 7.15: efficiency and load regulation of LTC3638 with the capacitive divider solution

The efficiency is computed with a ".meas" directive, in the meantime the load current is changed from maximum to $0\,A$. Also the mean value of the output voltage is measured with a ".meas" directive, therefore a load regulation plot can be obtained. Figure 7.15 shows the simulation results, the efficiency is shown as a function of the output current in 7.15a and the load regulation is plotted in 7.15b. The previous results are also shown in table 7.5 for the $120\,V$ case and in table 7.6 for the $220\,V$ one.

	No load	25 %	50 %	75 %	100 %	Average
DC output current (mA)	0	25	50	75	100	-
DC output voltage (V)	3.40	3.34	3.34	3.34	3.33	-
DC output power (mW)	0	83.6	167.0	250.2	333.2	-
AC input voltage (V)	120	120	120	120	120	-
AC input frequency (Hz)	60	60	60	60	60	-
AC input power (mW)	55.1	166.9	283.5	404.5	525.0	-
Power consumed by UUT (mW)	55.1	83.3	116.5	154.3	191.8	-
Efficiency	-	50.1 %	58.9 %	61.8 %	63.5 %	58.6 %

Table 7.5: *LTC3638* simulation results for $120\,V$ case

	No load	25 %	50 %	75 %	100 %	Average
DC output current (mA)	0	25	50	75	100	-
DC output voltage (V)	3.38	3.34	3.34	3.33	3.33	-
DC output power (mW)	0	83.5	166.8	250.0	333.0	-
AC input voltage (V)	220	220	220	220	220	-
AC input frequency (Hz)	50	50	50	50	50	-
AC input power (mW)	138.9	232.2	345.9	467.7	580.7	-
Power consumed by UUT (mW)	138.9	148.7	179.1	217.7	247.7	-
Efficiency	-	35.9 %	48.2 %	53.5 %	57.3 %	48.7 %

Table 7.6: *LTC3638* simulation results for $220\,V$ case

7.2.4 Comparison of all the results

The previous results can be easily compared by looking at figure 7.16; here all the efficiency curves, obtained by simulating the various circuits, are placed together and some results can be obtained. In the graph, solid lines are related to $120\,V$ input voltage and dashed ones to $220\,V$. It is clear that the *LT8630* solution is almost

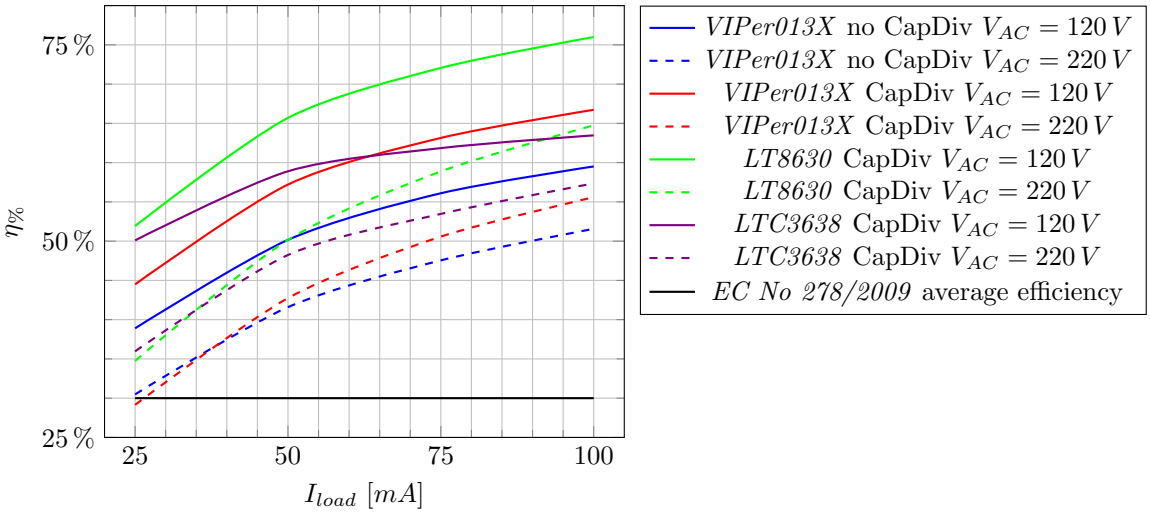


Figure 7.16: efficiency curves relative to all simulated circuits

the best one in any load condition; the advantage is mainly provided by the reduced conduction loss associated to the low side power MOSFET with respect to diode one. Suppose to have a diode, in a typical buck structure, with a $0.7\,V$ forward voltage drop and a mean value of the current that can be approximated with the output one of $100\,mA$, this condition is not so different with the one reported in previous cases, since the step-down ratio is quite large. The resulting dissipated power is around $70\,mW$, but, considering instead the low side power MOSFET, its r_{DSon} is of the order of $550\,m\Omega$ and, with an RMS current of $\approx 100\,mA$, the conduction loss is around $5.5\,mW$. It is also clear that switching losses are increased in the overall circuit, but the reduced input voltage keeps them well below the power dissipated by a diode, working in equivalent conditions.

It is also possible to appreciate the improved efficiency of the *VIPer013X* when the capacitive voltage divider is applied at its input, giving proof that the input voltage reduction is a key point to the better efficiency research. This effect is much more evident at low input voltage ($120\,V$), because diode losses are much more reduced

and switching ones depends directly onto the input voltage.

The last thing to notice is the result obtained with a properly rated device, the *LTC3638* shows a better response in lower load condition with respect to the *VIPer013X*. The *LTC3638* is rated for a maximum output current of 250 mA and the *VIPer013X* is instead designed to support a maximum of 2 A, in addition the first one has a lower on resistance (1.8 Ω) with respect to the second one (max value 30 Ω).

The *EC No 278/2009* required average efficiency is also reported in the graph and it is clear that every converters respect this requirement.

A final comparison can be performed considering a capacitive power supply, as the one reported in figure 7.17, this circuit can be easily designed following the equations provided in chapter 3. The resulting efficiency's plot, reported in figure 7.18, is ob-

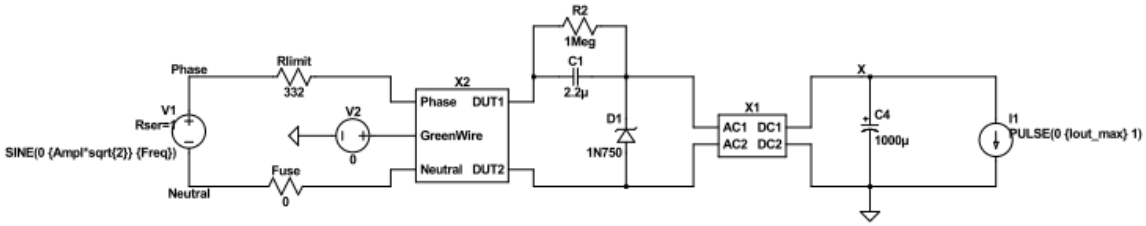


Figure 7.17: capacitive power supply used for further comparisons

tained only for the $V_{AC} = 220\,V$ case and a limited current range, otherwise the C_1 capacitor's cost will increase too much. It is clear that, this kind of circuit is not able

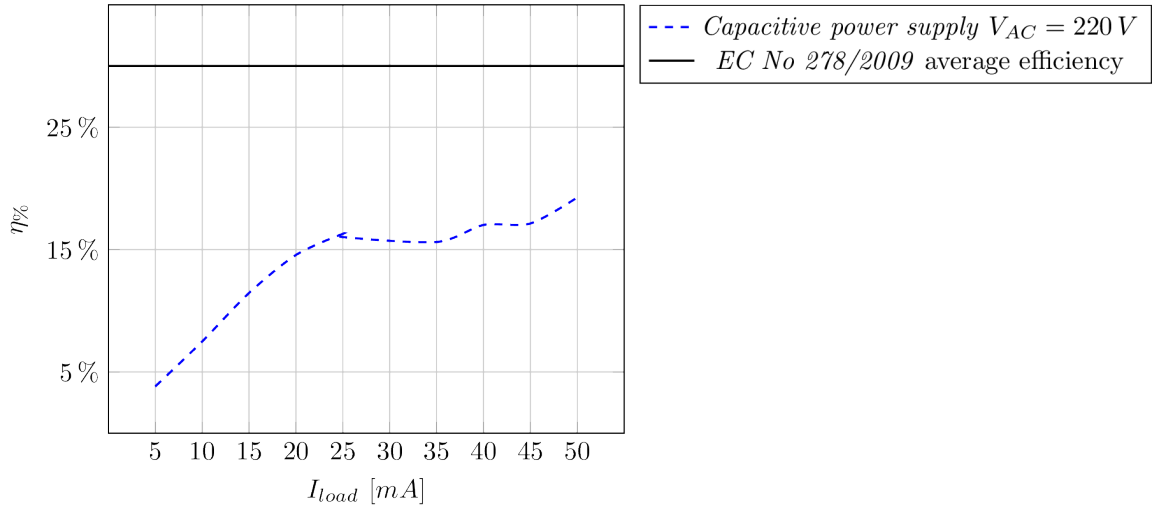


Figure 7.18: capacitive power supply efficiency at 220 V and various load currents

to satisfy the *EC No 278/2009* regulation and the efficiency is much lower w.r.t. a

SMPS based solution.

7.3 Solutions' cost

The cost of the various solutions should be considered in order to provide a more complete understanding of the design. Different vendors' websites can be chosen, for this work *Digi-Key Electronics* has been used. Evaluating the cost of a solution using only one realization is not meaningful at all, since the cost of single components lowers if they are ordered in large numbers. In order to take into account this aspect, the following *Bill Of Materials* (**BOM**) have been obtained supposing to realize 100 board for each solutions. The results are reported in figures 7.19, 7.20, 7.21, 7.22, 7.23, 7.24, 7.25 and 7.26.

Quantità	Codice componente	Codice produttore	Descrizione	Prezzo unitario (c€)
100	493-3930-1-ND	UCL1C102MNL1GS	CAP ALUM 1000UF 20% 16V SMD	49,770
400	S1A-FDICT-ND	S1A-13-F	DIODE GEN PURP 50V 1A SMA	9,850
100	1N750ABK-ND	1N750A BK	DIODE ZENER 4.7V 500MW DO35	19,560
100	EF4225-ND	ECQ-E4225KF	CAP FILM 2.2UF 10% 400VDC RADIAL	83,680
100	VR68J1.0MCT-ND	VR680000001004JAC00	RES 1M OHM 1W 5% AXIAL	36,880
100	BC2418-ND	NTCLE100E3331JB0	THERMISTOR NTC 330OHM 3560K BEAD	30,260
100	VO2223B-X017TDKR-ND	VO2223B-X017T	1A, 600V, PHOTOTRIAC, SMD	95,600
100	RNF14FTD221RCT-ND	RNF14FTD221R	RES 221 OHM 1/4W 1% AXIAL	2,330
100	817-2086-ND	RN102-2-02-1M1	CMC 1.1MH 2A 2LN TH	92,800
200	399-5419-ND	PHE850EB5100MB04R17	CAP FILM 10000PF 1.25KVDC RAD	24,960
100	399-12366-ND	F862BK154K310Z	CAP FILM 0.15UF 10% 630VDC RAD	30,520

Figure 7.19: Capacitive power supply solution's BOM, with phototriac. The total cost is 530.65 € *per 100 boards or* 5.3 € *per board.*

Quantità	Codice componente	Codice produttore	Descrizione	Prezzo unitario (c€)
100	399-18964-ND	SBC8-331-142	FIXED IND 330UH 1.4A 250 MOHM TH	152,390
100	399-9778-1-ND	T520D107M010ATE018	CAP TANT POLY 100UF 10V 2917	80,050
400	MRA4007T3GOSCT-ND	MRA4007T3G	DIODE GEN PURP 1KV 1A SMA	12,960
100	817-2086-ND	RN102-2-02-1M1	CMC 1.1MH 2A 2LN TH	92,800
200	399-5419-ND	PHE850EB5100MB04R17	CAP FILM 10000PF 1.25KVDC RAD	24,960
100	399-12366-ND	F862BK154K310Z	CAP FILM 0.15UF 10% 630VDC RAD	30,520
100	P3.32KHCT-ND	ERJ-3EKF3321V	RES SMD 3.32K OHM 1% 1/10W 0603	2,210
200	1276-1043-1-ND	CL05A104KA5NNNC	CAP CER 0.1UF 25V X5R 0402	1,190
100	490-10731-1-ND	GRM188R61E225KA12D	CAP CER 2.2UF 25V X5R 0603	5,190
100	497-16907-1-ND	VIPER013XSTR	IC OFFLINE CONV PWM 10SSOP	51,950
100	A103792CT-ND	CPF0402B150KE1	RES SMD 150K OHM 0.1% 1/16W 0402	16,170
100	P8.45KDACT-ND	ERA-6AEB8451V	RES SMD 8.45K OHM 0.1% 1/8W 0805	10,010
100	490-10677-1-ND	GJM0335C1E1R0WB01D	CAP CER 1PF 25V C0G/NP0 0201	5,400
100	712-1293-1-ND	500R07S8R2CV4T	CAP CER 8.2PF 50V C0G/NP0 0402	7,320
200	497-3241-1-ND	STTH1L06A	DIODE GEN PURP 600V 1A SMA	25,470
100	YAG2287CT-ND	RC0201FR-074K02L	RES SMD 4.02K OHM 1% 1/20W 0201	1,580
100	PCE3592TR-ND	EEV-EB2G330M	CAP ALUM 33UF 20% 400V SMD	189,600

Figure 7.20: Simple VIPer013XS based solution's BOM. The total cost is 800.27 € *per 100 boards or* 8 € *per board.*

Quantità	Codice componente	Codice produttore	Descrizione	Prezzo unitario (c€)
200	497-5254-1-ND	STTH1R02A	DIODE GEN PURP 200V 1.5A SMA	24,170
100	399-18964-ND	SBC8-331-142	FIXED IND 330UH 1.4A 250 MOHM TH	152,390
100	399-9778-1-ND	T520D107M010ATE018	CAP TANT POLY 100UF 10V 2917	80,050
400	MRA4007T3GOSCT-ND	MRA4007T3G	DIODE GEN PURP 1KV 1A SMA	12,960
100	399-17829-ND	C4AF3BU4100A1YK	FILM METALLIZED POLYPROPYLENE	164,080
200	YAG2022CT-ND	RT1206BRD071ML	RES SMD 1M OHM 0.1% 1/4W 1206	18,370
100	817-2086-ND	RN102-2-02-1M1	CMC 1.1MH 2A 2LN TH	92,800
200	399-5419-ND	PHE850EB5100MB04R17	CAP FILM 10000PF 1.25KVDC RAD	24,960
100	399-12366-ND	F862BK154K310Z	CAP FILM 0.15UF 10% 630VDC RAD	30,520
100	P3.32KHCT-ND	ERJ-3EKF3321V	RES SMD 3.32K OHM 1% 1/10W 0603	2,210
200	1276-1043-1-ND	CL05A104KA5NNNC	CAP CER 0.1UF 25V X5R 0402	1,190
100	490-10731-1-ND	GRM188R61E225KA12D	CAP CER 2.2UF 25V X5R 0603	5,190
100	497-16907-1-ND	VIPER013XSTR	IC OFFLINE CONV PWM 10SSOP	51,950
100	399-13011-ND	R60MR42205040K	CAP FILM 2.2UF 10% 400VDC RADIAL	89,770
100	A103792CT-ND	CPF0402B150KE1	RES SMD 150K OHM 0.1% 1/16W 0402	16,170
100	P8.45KDACT-ND	ERA-6AEB8451V	RES SMD 8.45K OHM 0.1% 1/8W 0805	10,010
100	311-4.22KDCT-ND	RT0603DRD074K22L	RES SMD 4.22KOHM 0.5% 1/10W 0603	5,770
100	490-10677-1-ND	GJM0335C1E1R0WB01D	CAP CER 1PF 25V C0G/NP0 0201	5,400
100	712-1293-1-ND	500R07S8R2CV4T	CAP CER 8.2PF 50V C0G/NP0 0402	7,320
100	493-6704-1-ND	ULR2D330MNL1GS	CAP ALUM 33UF 20% 200V SMD	53,290
100	VO2223B-X017TDKR-ND	VO2223B-X017T	1A, 600V, PHOTOTRIAC, SMD	95,600

Figure 7.21: VIPer013XS based solution's BOM, with capacitive divider and photo-triac. The total cost is 1045.74 € *per 100 boards or* 10.46 € *per board.*

Quantità	Codice componente	Codice produttore	Descrizione	Prezzo unitario (c€)
200	497-5254-1-ND	STTH1R02A	DIODE GEN PURP 200V 1.5A SMA	24,170
100	399-18964-ND	SBC8-331-142	FIXED IND 330UH 1.4A 250 MOHM TH	152,390
100	399-9778-1-ND	T520D107M010ATE018	CAP TANT POLY 100UF 10V 2917	80,050
400	MRA4007T3GOSCT-ND	MRA4007T3G	DIODE GEN PURP 1KV 1A SMA	12,960
100	399-17829-ND	C4AF3BU4100A1YK	FILM METALLIZED POLYPROPYLENE	164,080
200	YAG2022CT-ND	RT1206BRD071ML	RES SMD 1M OHM 0.1% 1/4W 1206	18,370
100	817-2086-ND	RN102-2-02-1M1	CMC 1.1MH 2A 2LN TH	92,800
200	399-5419-ND	PHE850EB5100MB04R17	CAP FILM 10000PF 1.25KVDC RAD	24,960
100	399-12366-ND	F862BK154K310Z	CAP FILM 0.15UF 10% 630VDC RAD	30,520
100	P3.32KHCT-ND	ERJ-3EKF3321V	RES SMD 3.32K OHM 1% 1/10W 0603	2,210
200	1276-1043-1-ND	CL05A104KA5NNNC	CAP CER 0.1UF 25V X5R 0402	1,190
100	490-10731-1-ND	GRM188R61E225KA12D	CAP CER 2.2UF 25V X5R 0603	5,190
100	VOR2142B8-ND	VOR2142B8	SSR RELAY SPST-NO 140MA 0-400V	320,010
100	497-16907-1-ND	VIPER013XSTR	IC OFFLINE CONV PWM 10SSOP	51,950
100	399-13011-ND	R60MR42205040K	CAP FILM 2.2UF 10% 400VDC RADIAL	89,770
100	A103792CT-ND	CPF0402B150KE1	RES SMD 150K OHM 0.1% 1/16W 0402	16,170
100	P8.45KDACT-ND	ERA-6AEB8451V	RES SMD 8.45K OHM 0.1% 1/8W 0805	10,010
100	311-4.22KDCT-ND	RT0603DRD074K22L	RES SMD 4.22KOHM 0.5% 1/10W 0603	5,770
100	490-10677-1-ND	GJM0335C1E1R0WB01D	CAP CER 1PF 25V C0G/NP0 0201	5,400
100	712-1293-1-ND	500R07S8R2CV4T	CAP CER 8.2PF 50V C0G/NP0 0402	7,320
100	493-6704-1-ND	ULR2D330MNL1GS	CAP ALUM 33UF 20% 200V SMD	53,290

Figure 7.22: VIPer013XS based solution's BOM, with capacitive divider and SSR. The total cost is 1270.15 € *per 100 boards or* 12.7 € *per board.*

Quantità	Codice componente	Codice produttore	Descrizione	Prezzo unitario (c€)
100	LTC3638EMSE#PBF-ND	LTC3638EMSE#PBF	IC REG BUCK ADJ 0.25A 16MSOP	382,540
100	497-5254-1-ND	STTH1R02A	DIODE GEN PURP 200V 1.5A SMA	24,170
100	399-18964-ND	SBC8-331-142	FIXED IND 330UH 1.4A 250 MOHM TH	152,390
100	399-9778-1-ND	T520D107M010ATE018	CAP TANT POLY 100UF 10V 2917	80,050
100	PCE3969CT-ND	EEE-2AA330P	CAP ALUM 33UF 20% 100V SMD	27,970
400	MRA4007T3GOSCT-ND	MRA4007T3G	DIODE GEN PURP 1KV 1A SMA	12,960
100	445-173636-1-ND	C3225X7S2A335K200AE	CAP CER 3.3UF 100V X7S 1210	57,830
100	399-17829-ND	C4AF3BU4100A1YK	FILM METALLIZED POLYPROPYLENE	164,080
100	YAG2022CT-ND	RT1206BRD071ML	RES SMD 1M OHM 0.1% 1/4W 1206	18,370
100	817-2086-ND	RN102-2-02-1M1	CMC 1.1MH 2A 2LN TH	92,800
200	399-5419-ND	PHE850EB5100MB04R17	CAP FILM 10000PF 1.25KVDC RAD	24,960
100	399-12366-ND	F862BK154K310Z	CAP FILM 0.15UF 10% 630VDC RAD	30,520
100	VO2223B-X017TDKR-ND	VO2223B-X017T	1A, 600V, PHOTOTRIAC, SMD	95,600

Figure 7.23: LTC3638 based solution's BOM, with capacitive divider and photo-triac. The total cost is 1228.08 € *per 100 boards or* 12.28 € *per board.*

Quantità	Codice componente	Codice produttore	Descrizione	Prezzo unitario (c€)
100	LTC3638EMSE#PBF-ND	LTC3638EMSE#PBF	IC REG BUCK ADJ 0.25A 16MSOP	382,540
100	497-5254-1-ND	STTH1R02A	DIODE GEN PURP 200V 1.5A SMA	24,170
100	399-18964-ND	SBC8-331-142	FIXED IND 330UH 1.4A 250 MOHM TH	152,390
100	399-9778-1-ND	T520D107M010ATE018	CAP TANT POLY 100UF 10V 2917	80,050
100	PCE3969CT-ND	EEE-2AA330P	CAP ALUM 33UF 20% 100V SMD	27,970
400	MRA4007T3GOSCT-ND	MRA4007T3G	DIODE GEN PURP 1KV 1A SMA	12,960
100	445-173636-1-ND	C3225X7S2A335K200AE	CAP CER 3.3UF 100V X7S 1210	57,830
100	399-17829-ND	C4AF3BU4100A1YK	FILM METALLIZED POLYPROPYLENE	164,080
100	YAG2022CT-ND	RT1206BRD071ML	RES SMD 1M OHM 0.1% 1/4W 1206	18,370
100	817-2086-ND	RN102-2-02-1M1	CMC 1.1MH 2A 2LN TH	92,800
200	399-5419-ND	PHE850EB5100MB04R17	CAP FILM 10000PF 1.25KVDC RAD	24,960
100	399-12366-ND	F862BK154K310Z	CAP FILM 0.15UF 10% 630VDC RAD	30,520
100	VOR2142B8-ND	VOR2142B8	SSR RELAY SPST-NO 140MA 0-400V	320,010

Figure 7.24: LTC3638 based solution's BOM, with capacitive divider and SSR. The total cost is 1452.49 € *per 100 boards or* 14.52 € *per board.*

Quantità	Codice componente	Codice produttore	Descrizione	Prezzo unitario (c€)
100	399-18964-ND	SBC8-331-142	FIXED IND 330UH 1.4A 250 MOHM TH	152,390
100	399-9778-1-ND	T520D107M010ATE018	CAP TANT POLY 100UF 10V 2917	80,050
100	PCE3969CT-ND	EEE-2AA330P	CAP ALUM 33UF 20% 100V SMD	27,970
400	MRA4007T3GOSCT-ND	MRA4007T3G	DIODE GEN PURP 1KV 1A SMA	12,960
100	445-173636-1-ND	C3225X7S2A335K200AE	CAP CER 3.3UF 100V X7S 1210	57,830
100	399-17829-ND	C4AF3BU4100A1YK	FILM METALLIZED POLYPROPYLENE	164,080
200	YAG2022CT-ND	RT1206BRD071ML	RES SMD 1M OHM 0.1% 1/4W 1206	18,370
100	817-2086-ND	RN102-2-02-1M1	CMC 1.1MH 2A 2LN TH	92,800
200	399-5419-ND	PHE850EB5100MB04R17	CAP FILM 10000PF 1.25KVDC RAD	24,960
100	399-12366-ND	F862BK154K310Z	CAP FILM 0.15UF 10% 630VDC RAD	30,520
100	VO2223B-X017TDKR-ND	VO2223B-X017T	1A, 600V, PHOTOTRIAC, SMD	95,600
100	LT8630EFE#PBF-ND	LT8630EFE#PBF	IC REG BUCK ADJ 100V .6A 20TSSOP	377,360
100	P3.32KHCT-ND	ERJ-3EKF3321V	RES SMD 3.32K OHM 1% 1/10W 0603	2,210
100	P316KDBCT-ND	ERA-3AEB3163V	RES SMD 316K OHM 0.1% 1/10W 0603	9,920
100	490-6112-1-ND	GRM0335C1H100JA01D	CAP CER 10PF 50V C0G/NP0 0201	540
100	1276-1043-1-ND	CL05A104KA5NNNC	CAP CER 0.1UF 25V X5R 0402	1,190
100	445-5207-1-ND	C3216X7S2A225K160AB	CAP CER 2.2UF 100V X7S 1206	36,140
100	490-10731-1-ND	GRM188R61E225KA12D	CAP CER 2.2UF 25V X5R 0603	5,190
100	490-3155-1-ND	GRM0335C1E560JA01D	CAP CER 56PF 25V C0G/NP0 0201	540
100	P8.66KDBCT-ND	ERA-3AEB8661V	RES SMD 8.66KOHM 0.1% 1/10W 0603	9,920

Figure 7.25: LT8630 based solution's BOM, with capacitive divider and photo-triac. The total cost is 1282.75 € *per 100 boards or* 12.83 € *per board.*

Quantità	Codice componente	Codice produttore	Descrizione	Prezzo unitario (c€)
100	399-18964-ND	SBC8-331-142	FIXED IND 330UH 1.4A 250 MOHM TH	152,390
100	399-9778-1-ND	T520D107M010ATE018	CAP TANT POLY 100UF 10V 2917	80,050
100	PCE3969CT-ND	EEE-2AA330P	CAP ALUM 33UF 20% 100V SMD	27,970
400	MRA4007T3GOSCT-ND	MRA4007T3G	DIODE GEN PURP 1KV 1A SMA	12,960
100	445-173636-1-ND	C3225X7S2A335K200AE	CAP CER 3.3UF 100V X7S 1210	57,830
100	399-17829-ND	C4AF3BU4100A1YK	FILM METALLIZED POLYPROPYLENE	164,080
200	YAG2022CT-ND	RT1206BRD071ML	RES SMD 1M OHM 0.1% 1/4W 1206	18,370
100	817-2086-ND	RN102-2-02-1M1	CMC 1.1MH 2A 2LN TH	92,800
200	399-5419-ND	PHE850EB5100MB04R17	CAP FILM 10000PF 1.25KVDC RAD	24,960
100	399-12366-ND	F862BK154K310Z	CAP FILM 0.15UF 10% 630VDC RAD	30,520
100	LT8630EFE#PBF-ND	LT8630EFE#PBF	IC REG BUCK ADJ 100V .6A 20TSSOP	377,360
100	P3.32KHCT-ND	ERJ-3EKF3321V	RES SMD 3.32K OHM 1% 1/10W 0603	2,210
100	P316KDBCT-ND	ERA-3AEB3163V	RES SMD 316K OHM 0.1% 1/10W 0603	9,920
100	490-6112-1-ND	GRM0335C1H100JA01D	CAP CER 10PF 50V C0G/NP0 0201	540
100	1276-1043-1-ND	CL05A104KA5NNNC	CAP CER 0.1UF 25V X5R 0402	1,190
100	445-5207-1-ND	C3216X7S2A225K160AB	CAP CER 2.2UF 100V X7S 1206	36,140
100	490-10731-1-ND	GRM188R61E225KA12D	CAP CER 2.2UF 25V X5R 0603	5,190
100	490-3155-1-ND	GRM0335C1E560JA01D	CAP CER 56PF 25V C0G/NP0 0201	540
100	P8.66KDBCT-ND	ERA-3AEB8661V	RES SMD 8.66KOHM 0.1% 1/10W 0603	9,920
100	VOR2142B8-ND	VOR2142B8	SSR RELAY SPST-NO 140MA 0-400V	320,010

Figure 7.26: LT8630 based solution's BOM, with capacitive divider and SSR. The total cost is 1507.16 € *per 100 boards or* 15.07 € *per board.*

7.4 Conclusions

In this chapter a solution to one of the problems affecting high step down converters for low output voltage has been proposed. The solution is based on a reactive voltage divider and an energy balance approach has been described for the design procedure. The solution has been then tested with different circuits, the first one is the basic *VIPer013X* already used in the previous chapter and, after that, other circuits have been simulated. In particular, the *LT8630* has shown the best results for both $120\,V$ and $220\,V$. As a conclusion, the use of a synchronous buck should be preferred in applications where the output power is below $1\,W$, because the almost constant conduction losses, related to free-wheeling diode, are drastically reduced by the use of another MOSFET. In the end, also the cost of the various solutions has been evaluated and reported.

CHAPTER 8

Conclusions

The design and simulation of an high-voltage step-down low power converter have been carried out for this thesis work. Thanks to that it was possible to examine in depth different aspects: standards for better efficiency (ECoC or U.S. Energy Star), how to perform a market oriented research, the electromagnetic compliance problem, design issue, simulations and comparison of different solutions, in terms of efficiency or cost.

The result of this analysis has conducted to prefer a synchronous buck converter based solutions, which shows a better efficiency due to lower losses. This solution is also the one with highest cost and, when cost is more stringent than efficiency, a simpler solution, like the one based on the *VIPer01*, can be considered, since efficiency requirements (ECoC average active efficiency) are respected for every analysed circuits.

The capacitive voltage divider usage leads to improved efficiency and future works could be addressed to enhance this kind of circuit. In particular, the no-load condition should be avoided or solved with additional circuitry. Other solutions, like *switching capacitors*, could be considered to complete the overall picture of this work.

Bibliography

[1] Milan M. Jovanović. "Power Supply Technology - Pas, Present and Future". In: *Power Electronics Laboratory Delta Products Corporation* (2014).

[2] European Environment Agency. "L'energia in Europa: situazione attuale". In: (2017). URL: https://www.eea.europa.eu/signals/signals-2017/articles/l2019energia-in-europa-situazione-attuale.

[3] Ericsson. *Mobility Report*. 2018. URL: https://www.ericsson.com/assets/local/mobility-report/documents/2018/emr-q2-update-2018.pdf.

[4] European Union. *COMMISSION REGULATION (EC) No 278/2009*. 2009. URL: https://publications.europa.eu/en/publication-detail/-/publication/07c8dae4-902b-4121-bd5d-744eea7cf61e.

[5] Allison Lantero. *The War of the Currents: AC vs. DC Power*. URL: https://www.energy.gov/articles/war-currents-ac-vs-dc-power.

[6] Power Integrations. *Product Selector Guide: AC-DC Products*. 2016. URL: https://ac-dc.power.com/design-support/product-documents/product-selector-guides/.

[7] Power Integrations. *Product Selector Guide - Appliance Power Supply ICs*. 2017. URL: https://ac-dc.power.com/design-support/product-documents/product-selector-guides/.

[8] STMicroelectronics. *Power management Guide 2017*. 2017. URL: http://www.st.com/en/power-management.html.

[9] Texas Instruments. *Power Management Guide*. 2016. URL: http://www.ti.com/lit/sg/slvt145q/slvt145q.pdf.

[10] Y. Chen, Z. Zhong, and Y. Kang. "Design and Implementation of a Transformerless Single-Stage Single-Switch Double-Buck Converter With Low DC-link Voltage, High Step-Down, and Constant Input Power Factor Features". In: *IEEE Transactions on Power Electronics* (Dec. 2014).

[11] Chih-Shen Yeh, Xiaonan Zhao, and Jih-Sheng Lai. "A MHz zero voltage switching (ZVS) tapped-inductor buck converter for wide-input high step-down low-power applications". In: (2017).

[12] M. A. M. Oninda, G. Sarowar, and M. M. H. Galib. "Single-phase switched capacitor AC-DC step down converters for improved power quality". In: (Dec. 2017).

[13] Ching-Tasi Pan et al. "A novel transformer-less interleaved four-phase high step-down DC converter with low switch voltage stress". In: (May 2014).

[14] D. K. Sasi and A. S. Haryhar. "A transformer-less high efficiency interleaved buck converter with improved step-down conversion ratio and a pre-charging setup through snubber circuit". In: (Aug. 2017).

[15] H. Meyvaert et al. "A Light-Load-Efficient 11/1 Switched-Capacitor DC-DC Converter With 94.7 Efficiency While Delivering 100 mW at 3.3 V". In: *IEEE Journal of Solid-State Circuits* (Dec. 2015).

[16] STMicroelectronics. *AN1476 Low-cost power supply for hoe appliances*. Ed. by STMicroelectronics. 2004.

[17] Reston Condit. *AN954 Transformerless Power Supplies: Resistive and Capacitive*. Ed. by Microchip Technology Inc. 2004.

[18] Stan D'Souza. *Transformerless power supply*. Ed. by Microchip Technology Inc. 200.

[19] LLC Designer Circuits. *DesignNote 001C Transformerless Power Supply Design*.

[20] V. M. Rajović and N. S. Jovičić. "The capacitive divider power supply and its design problem". In: *2011 19thTelecommunications Forum (TELFOR) Proceedings of Papers* (2011).

[21] VISHAY. *Application Note: AC Film Capacitors in Connection with the Mains*. Ed. by Inc. VISHAY Intertechnology. 2013.

[22] Robert W. Erickson. Dragan Maksimovic. *Foundamentals of Power Electronics*. 2004.

[23] Robert A. Mammano. *Foundamentals of power supply design*. 2017.

[24] J. Picard. *Under the Hood of Flyback SMPS Design*. Texas Instruments Incorporated. 2010. URL: www.ti.com/psds.

[25] L. Dinwoodie. *Exposing The Inner Behaviour of a Quasi-Resonant Flyback Converter*. Texas Instruments Incorporated. 2012. URL: www.ti.com/psds.

[26] B. King. R. Valley. *Control Challenges for Low Power AC/DC Converters*. Texas Instruments Incorporated. 2014. URL: www.ti.com/psds.

[27] Clayton R. Paul. *Introduction to electromagnetic compatibility*. Ed. by J. Wiley. 2nd. 2004.

[28] Dr. Bogdan Adamczyk. "Conducted Emissions Measurements: Voltage Method". In: *In Compliance Magazine* (July 2017).

[29] Yasuhiro Mitsuya. *Basics of Noise Countermeasures [Lesson 6] Common mode choke coils*. Ed. by Ltd. Murata Manufacturing Co. 2011. URL: https://www.murata.com/products/emiconfun/emc/2011/10/28/en-20111028-p1.

[30] Henry W. Ott. *Electromagnetic compatibility engineering*. Ed. by J. Wiley. 2009.

[31] STMicroelectronics. *VIPer01 datasheet*. 2016. URL: http://www.st.com/content/st_com/en/products/power-management/ac-dc-converters/high-voltage-converters/viperplus/viper01.html.

[32] STMicroelectronics. *AN4858 Application note: STEVAL-ISA178V1 5 V/1 W 30 kHz buck demo with VIPer01*. 2016. URL: http://www.st.com/content/st_com/en/products/evaluation-tools/solution-evaluation-tools/psu-and-converter-solution-eval-boards/steval-isa178v1.html.

[33] ONsemiconductor. *MRA4003T3G Series, NRVA4003T3G Series Surface Mount Standard Recovery Power Rectifier*. 2016. URL: https://www.onsemi.com/pub/Collateral/MRA4003T3-D.PDF.

[34] STMicroelectronics. *STTH1L06 Turbo 2 ultrafast high voltage rectifier*. 2009. URL: http://www.st.com/resource/ja/datasheet/stth1l06.pdf.

[35] EUROPEAN COMMISSION-DIRECTORATE GENERAL JRC-JOINT RESEARCH CENTRE-Institute for Energy and Transport-Renewable Energy Unit. *Code of Conduct on Energy Efficiency of External Power Supplies, Version 5*. 2013.

[36] Chris Calwell et al. *Test Method for Calculating the Energy Efficiency of Single-Voltage External Ac-Dc Power Supplies*. 2004.

[37] Linear Technology. *LT8630, 100V, 0.6A Synchronous Micropower Step-Down High Efficiency Switching Regulator*. 2016. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/8630f.pdf.

[38] Linear Technology. *LTC3638, High Efficiency, 140V 250mA Step-Down Regulator*. 2014. URL: http://www.analog.com/media/en/technical-documentation/data-sheets/3638fa.pdf.