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Development of electronics for precision pendulum oscillators

Relatori:

Sansoe' Claudio

Gregoretti Francesco

Candidati:

Mukhamedjanov Daud

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1.Introduction

In this thesis I would like to present an analog-based approach for precision pendulum control units.

Pendulums have a long history since dynasty of Han in 1st century used a seismometer. In 1602 Galileo Galilei was the first to study properties of pendulums (Ref.6) and he has discovered Isochronism: the period of the pendulum is approximately independent of the amplitude or width of the swing-that property would be used for pendulums as the timekeepers. However, as it became clear, with the work of Huygens, that there could be the possibility to build very good clocks with pendulums, it also emerged that the isochronism was not perfect and that something must be done to improve it to make a really good clocks. The reason is that in a mathematical pendulum the period is a parabolic function of the oscillation amplitude (a deviation from perfect isochronous behavior that is often called “circular error”) and as a consequence any amplitude instability produces period variations.

Huygens solved the problem, in theory, when he demonstrated (and obtained a patent for it) that a pendulum hanging from a thin ribbon pinched between two cycloidal profiles would be isochronous, but nobody was ever able to make a clock according to his design which would be so.

John Harrison, the (moral) winner of the Longitude prize, did better with a similar arrangement using circular profiles, because it turns out that they produce a parabolic minimum of the period at some useable oscillation amplitude (related to the radius of the circles), so he built pendulum clocks that were operated at an oscillation amplitude near that minimum, trying to make the clock

less sensitive to amplitude variations. His clocks remain to this age, after about 300 years, the most stable pendulums operated in air that were ever built. He claimed that they could remain exact better than one second during one hundred days, and a three-month trial made in Greenwich Observatory in 2014-2015(Ref. 16) with a clock made following his directions confirmed his statements.

Nevertheless, a more popular approach to pendulum clock improvement has been to operate at a very small oscillation amplitude the pendulum used as a clock regulator, exploiting in this way the reduced dependence on amplitude that the parabolic circular error offers, without trying to modify the amplitude dependence curve. Most clockmakers used this approach for three centuries, and in vacuum a few of them obtained stability results that surpassed the claims of Harrison. As a result, during the 18th and 19th century, these pendulum clocks had a role as the most accurate timekeepers and were the base for national time scales.

The subject of this thesis is to address the problem of amplitude stability in pendulum oscillations, which is obviously important in both approaches: in the more common small oscillation approach because of the locally linear dependence of period on amplitude, and in the Harrison approach because the amplitude should be fixed at the minimum of the parabolic curve. It seems possible that pendulum clocks may be improved with respect to the best historical results by using modern technology, both in mechanics and in electronics. In fact, research on pendulum clocks basically stopped when the first precision quartz oscillators became available and were perfected for warfare needs during WWII (the timekeeping accuracy of the pendulum was exceeded by the quartz crystal oscillator, invented in 1921. Quartz clocks, invented in 1927, replaced pendulum clocks as the world's best timekeepers. Pendulum clocks were used as time standards until World

War 2, although the French Time Service continued using them in their official time standard ensemble until 1954.

The underlying consideration of this work is that a pendulum clock with an electronic oscillation loop is basically very similar to a quartz oscillator, in which also you have an electronic circuit which sustains the oscillations of a mechanical resonator. There seems to be little reason why it could not be possible to build a pendulum clock with similar performance to a high-quality quartz clock. In fact, it could even be imagined that a pendulum clock might become better than a quartz clock, for the main reason that the level of strain imposed to materials in the mechanical oscillator is vastly smaller in a pendulum than in a quartz resonator.

In a quartz oscillator, even a high-quality metrological one, the very high Q factor of the quartz resonator imposes a very high level of stress to the quartz material, which is shaken so strongly that chips of quartz that are not very well attached to the surface of the resonator are eventually shot away, reducing slowly in this way the dimensions of the quartz crystal, and therefore increasing slowly its resonance frequency. Think for example of a 10 MHz oscillator whose quartz resonator may have surface points oscillating with an amplitude A. Their peak acceleration would then be given by $A\omega^2$ which would be of the order of 10^7 m/s^2 if A is a couple of nanometers. One million times the Earth's gravity acceleration!

This is the physical phenomenon that produces the well-known frequency drift of quartz oscillators and induces the need to control them by using an atomic resonance as a reference in order to make a stable clock.

On the contrary, the level of stress imposed on materials in a pendulum clock is much smaller than their yield threshold, except for some details which can be avoided in a thoughtful design, like the knife-edge sometimes used for the suspension of the pendulum.

Clearly, to fully exploit this possibility, it is necessary to solve environmental sensitivity issues and use only aged low creep materials, which exist. However, these problems have been very well addressed for pendulums in the long history of their development. In addition, some of these environmental problems, in particular the buoyancy shift and the deterministic periodic variations of earth gravity caused by the attraction of celestial bodies, can be corrected with a feed-forward approach because they are very well known.

Here we decided that, in designing for an improvement of at least a factor of one hundred better that the best pendulum clocks ever built, a critical point is to substitute the traditional mechanical driving system, based on pulsed pushes and a more or less complicated escapement mechanism for timing them, with an electronic system similar to the one used in quartz oscillators.

In the next section the guidelines for drawing specifications for such a system are spelled out and justified as a consequence of the reasoning developed here in the introduction.

2.General Principle

2.1. System Description

The purpose is to create a system in which the frequency used to drive a clock signal, can include corrections which are added in feed-forward mode and additional feature to speed up measurements, needed for trimming operations are serviced at the same time in this work by a system architecture quite similar to what is normally implemented in atomic clocks to lock a quartz crystal oscillator. This is set at 10 MHz so that it can easily drive a clock realized with simple counters and a display, to the chosen atomic resonance, which happens to have the frequency that it has and is obviously unrelated to any power of 10 of 1 Hz. The block diagram of such a locking scheme is shown in the figure 1, as referred to the case at hand of a quartz oscillator locked to the pendulum.

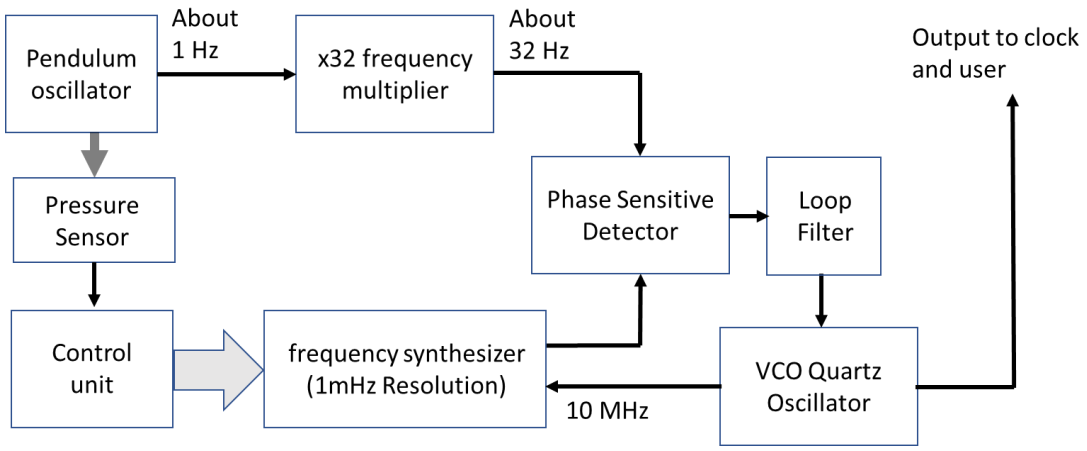


Figure 1- System description

The pendulum was shown on figure 2 provides a signal of 1Hz output frequency, as shown on Figure 1, and after frequency multiplication by 32 that signal is compared by a Phase Detector that at the other input has output of the Frequency Synthesizer.

The synthesizer can both be set by hand through the control unit in order to compensate whatever offset the pendulum may have from 1 Hz so that, when locked, the quartz be exactly at 10 MHz, and at the same time the control unit can manage the correction of the buoyancy effect on pendulum frequency by processing the pressure information coming from a pressure sensor placed close to the pendulum and inserting in the synthesizer a compensating variable frequency offset.

Given the 1 mHz resolution of the DDS synthesizer with an output frequency of 32 Hz, which is a relative resolution is $3x10^{-5}$, therefore the pullability specification for the 10 MHz oscillator for making sure that it stays locked is then 300 Hz, which of course requires a not excessively high Q of its resonator, not more than 10000. Clearly, it would be desirable to improve the resolution of the synthesizer in order to smooth down the corrected frequency (and hence increase the short-term stability) when the control unit must track for example an environmental pressure change, which can be easily of the level of few of these steps over a stretch of a few days.

The pendulum shown on figure 2, by itself is a mechanical device that was specifically constructed to provide a 1Hz output sine wave signal as shown on Figure 2. Pendulum has 3 neodymium magnets placed on both sides of the bob and the last one on the bottom, with specifically arranged coils to give a best possible output signal. It has a very high-quality factor.

Figure 2- Pendulum

Sensing coils are designed on PCBs because it is very difficult to use a lacquered wire for that kind of purpose, place precisely the centers of coils, make a reliable connection to other circuits that wouldn't fall off by any small movements. Moreover, coils on PCB are relatively cheap to produce since that cost of everything depends on amount of labor that was put in it: PCBs are more reliable, having a resolution of 0.0254mm (5 Mil), have a nice repeatability, costs less than 50 USD for a batch of 10 pieces. As the base was taken a production capabilities of the popular commercial producer. (Ref. 14) That's why we considered that as a good approach to make sensors.

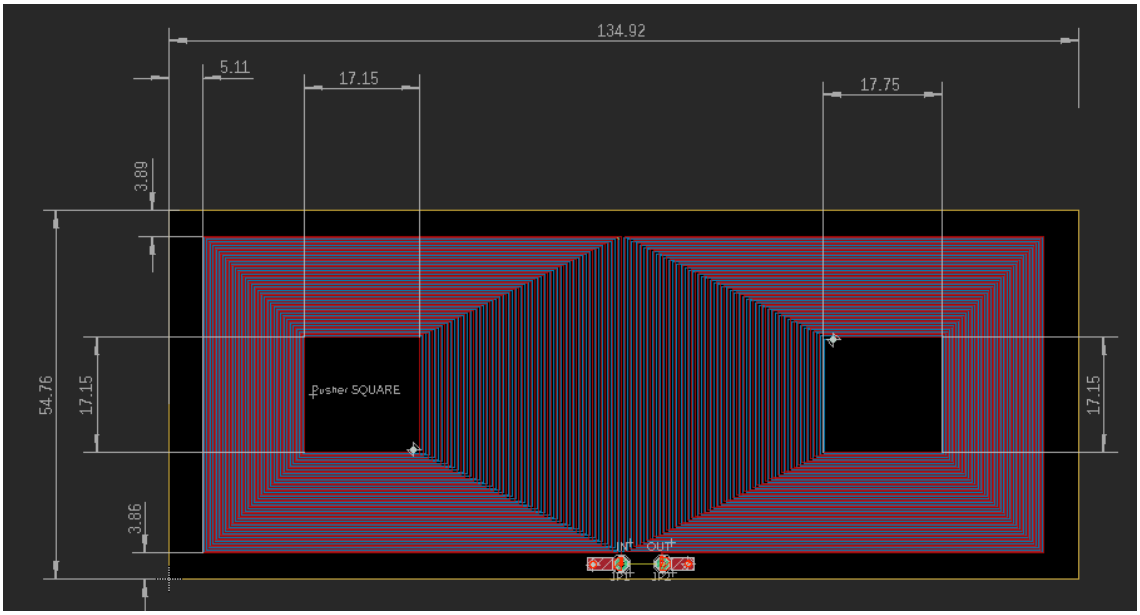


Figure 3 - Pushing coil PCB, Red-Top layer, Blue-Bottom layer

Because our pendulum has a large Quality Factor, but it is not ideal we can't have the pendulum swinging infinitely long time. We need an external source of energy in the pendulum, the pushing coil that is demonstrated on Figure 4 was used. The pushing coil is designed in a kind of way to not interfere with sensing coil, and it is placed horizontally at the bottom, under the bob. When we are measuring the signal going out of pendulum, specifically designed circuit pushes the pendulum's bob to support continuous oscillations. Pusher and Sensor coils are placed perpendicular to each other to exclude mutual inductance between Pusher and Sensor coils.

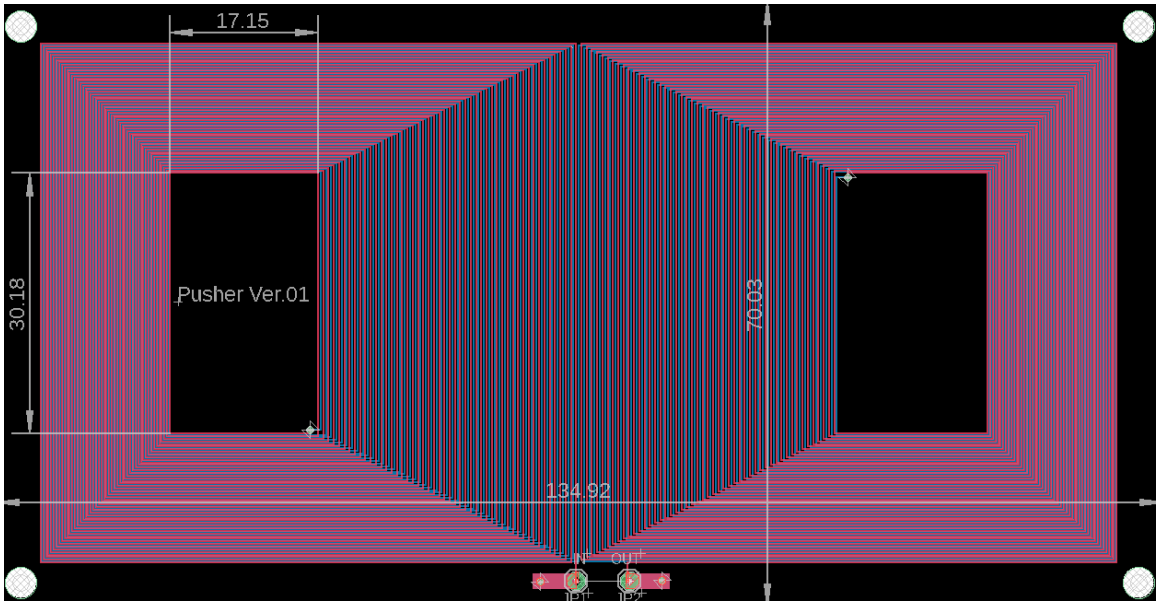


Figure 4 - Sensing coil, Red-Top layer, Blue-Bottom layer

For sensing of the movement of a bob, that has a magnet on it, we designed a coil that is shown on Figure 4, for that specific purpose coils are placed laterally at both sides of the pendulum along the movement of a bob to sense the velocity of a bob. But that should take into consideration that magnetic field of permanent magnet drops by time, dimension distortions of PCBs and so on.

That's why a temperature and pressure sensor is integrated into DDS signal generator.

Multiple coils could be stacked on top of each other to get more of a pushing force, if needed.

The Amplitude control board is a small subsystem that control the amplitude of the pendulum keeping it constant, compensating losses caused by non-idealities of device. But the device is constructed in such a way that it doesn't need dynamic level compensation, mainly, the amplitude control should compensate temperature changes and small disturbances like wind going out of window or someone's breathing: a trimmer and amplifier can be used for that small task to adjust signal to the required level.

The frequency multiplier takes 1Vp signal at the input and then to multiply frequency by 2 at each stage, the frequency multiplier has 4 stages of multiplication by 2(doubling) of 1 Hz input. Then it gives a 16Hz at the output stage. Then, that signal is used for later locking on PLL because 1Hz would take a lot of time to lock, moreover the pendulum's time constant is around 20 minutes-it would take too much time to lock on 1Hz. Lock time of any PLL is defined as the time required to get an output frequency which is within a small, but in a required range when a small frequency step is applied to PLL, locking time is inversely proportional to a PLL loop Bandwidth. But our synthesizer has a 1mHz resolution step that would take time to lock a PLL.

A Wien bridge oscillator is used for signal recovery because the 16Hz output is not perfect, and for a phase comparison we need a relatively good signal.

A Phase Sensitive Detector compares the 32Hz signal output, recovered by the Wien Bridge injection locked oscillator with an external frequency synthesizer providing a control signal to 10Mhz Oscillator that controls Synthesizer.

All those modules are connected on Mainboard that handles all interconnections between modules and has proper connections for the sensor coil and the pushing coil.

But at the same time Mainboard shouldn't have minimum of tracks in parallel with axe of pendulum's bob because they would affect a movement of the bob and take some induced voltage that is better to be kept at a minimum amount. Because a horizontal copper track would have a breaking effect to the movement of the bob and magnet on it would induce voltage that can affect at signal that are provided by those tracks.

2.2. Design Specifications

As argued in the introduction, the main tasks to be kept in mind for the new electronic system are:

1. Realizing an oscillator configuration that avoids the traditional mechanical impulsive push for maintaining oscillations, substituting it with an oscillation loop of the type of the Leeson model, in the way it is done in quartz oscillators, in a sinusoidal regime. The loop electronics should be such that the stability of the oscillation amplitude is guaranteed. In particular, this means that the closed loop gain stability should be adequately constant with ageing and variations of environmental parameters (temperature, pressure, humidity and the like).
2. Devising a structure for the system in which the frequency used to drive the clock can include corrections added in feed-forward to the natural pendulum frequency to eliminate form the clock signal frequency variations caused in a well-known way by well-modeled mechanisms affecting the pendulum frequency. Such effects are, for example, the buoyancy effect, which can be well described once the density of bob and air are known, and the deterministic part of earth gravity variations as induced by the attraction from celestial bodies, in particular the Moon and the Sun.

Additionally, it is considered to be extremely desirable to realize a system in which measurements needed to optimize the clock are fast. In fact, the slow measurements traditionally associated with pendulum trimming are by themselves an obstacle to the accuracy of adjustments because during the time needed for the measurements the conditions of the system may change, making then difficult to distinguish if observed variations are caused by the adjustment action or by system variations. Basically, what this means is that the frequency

used to drive the clock, and to take the measurements necessary for trimming, should be much higher than the pendulum frequency, but somehow slaved to it in a faithful way.

The chosen architecture of the two subsystems designed to fulfill these two requirements is spelled out in more detail below.

3.Design Subsystems

3.1. Oscillation Loop

The oscillation loop that is designed to function in sinusoidal regime, is based on sensors which translates into a voltage sinewave the velocity of the bob, by means of a coil kind of sensor, an interface amplifier, an attenuator which is needed for bringing the amplitude down at needed level, and another amplifier designed to drive the pusher coil.

The idea is that the external pushing force should be in principle provided so that it is proportional to the velocity, so that the injected power is always proportional to the power lost to friction. That is the most efficient way because it can guarantee that the velocity of the bob is exactly what it would be if there wasn't any friction.

The oscillation amplitude will then be determined by the open loop gain G_b of the oscillation loop, which includes the transfer functions of sensor, sensor interface amplifier, attenuator, pusher amplifier (all these together forming G), and pusher current to amplitude ratio (b). The latter depends obviously on the quality factor Q of the pendulum. Ideally, all the electronics cascade inside the loop should be wideband in order not to introduce any phase rotation in the loop gain, in order to guarantee to the frequency be centered on resonance. In fact, as is well known, the conditions for oscillation in such a loop are

$|G_b|$ =1 (condition for modulus)

$\angle G_b$ = 0 (conditione for phase)

the second of which implies that the phase of G to be zero if oscillation at resonance must guaranteed.

The first condition refers to the amplitude of oscillations after all the transients are extinguished. In order to start the oscillations, it is necessary that the loop gain should be greater than one $|G_b| > 1$, so that the amplitude may increase as the pusher injects more energy than necessary to keep it constant, but when the desired amplitude is reached the loop gain must reduce to one $|G_b| = 1$. To this aim, metrological quality oscillators are typically equipped with an AGC circuit (Automatic Gain Control) to avoid further amplitude increase.

A typical example of such a procedure is the traditional trick used in Wien oscillators, that include a temperature dependent resistor in the resistive divider that fixes the gain of the Operational Amplifier. An alternative approach that is sometimes used is to reduce b instead of G when the desired amplitude is reached, by exploiting the fact that in such oscillators b increases with the quality factor Q. This is the approach adopted by John Harrison in his pendulums when he used air resistance at wide oscillations to reduce the Q and stabilize the amplitude of oscillation.

A similar effect can be produced in a pendulum where a bob is hanging on a thin wire, or maybe a ribbon wire, where the periodical stretching of the suspension under the variable tension given by the combined action of centrifugal force and inclination from vertical increases the mechanical losses in the wire as the oscillation amplitude increases. In this case, as it turns out, that Q is inversely proportional to the square of the amplitude at large amplitudes, and this can be used in the same way as Harrison used air resistance to introduce a passive stabilization of the amplitude in that range. Basically, what this means for the

electronics of the oscillation loop is that the stability of G is necessary to keep the amplitude within an interval around of a desired value is reduced by the "negative feedback" that is practically introduced by the Q reduction. Given the first condition above for the oscillator, it can be seen that for small variations of G, given the proportionality of b to Q, and therefore to q^{-2}, it will be

$$\frac{dG}{G} - 2\frac{dq}{q} = 0$$

which means that a quite reasonable relative gain stability of 10^{-3} results in a relative amplitude stability of half that much. In turn, assuming for example that the amplitude where the minimum happens to be is about 0.1 rad, and that the ability to hit it is about 1% of it, it can be calculated that the relative frequency (or period) stability is below 10^{-8}.

This calculation comes from the shape of the parabolic circular error about the minimum, which is

$$\frac{DT}{T} = \frac{(q - q_{min})^2}{16}$$

and from the consideration of its slope at $q\text{-}q_{min} = 10^{-3}$ rad according to the assumption above.

It is possible to do it better by at least a factor of 10 for the gain stability, and with greater effort even better. So, it can be argued that it should not be excessively difficult to obtain a relative frequency stability of the order of 10^{-10}.

The actual realization of the oscillation loop can be done by inserting a permanent magnet in the bob and deploying a sensor coil and a pusher coil conveniently coupled to it so that an electromotive force is developed in the first one when the bob is moving, and a force is

generated that pushes the bob when current flows in the second one. An important detail that must be observed in realizing the two voice coils is that the coupling between the two must be zero, which imposes a vanishing mutual inductance.

The actual realization is discussed in detail in the following chapter, but it's based on the structure described in the block diagram below where an AGC (Automatic Gain Control) circuit is also included on the right side of the scheme, which may not to be necessary if the passive amplitude stabilization illustrated on Figure 5 is sufficient for the desired level of stabilization.

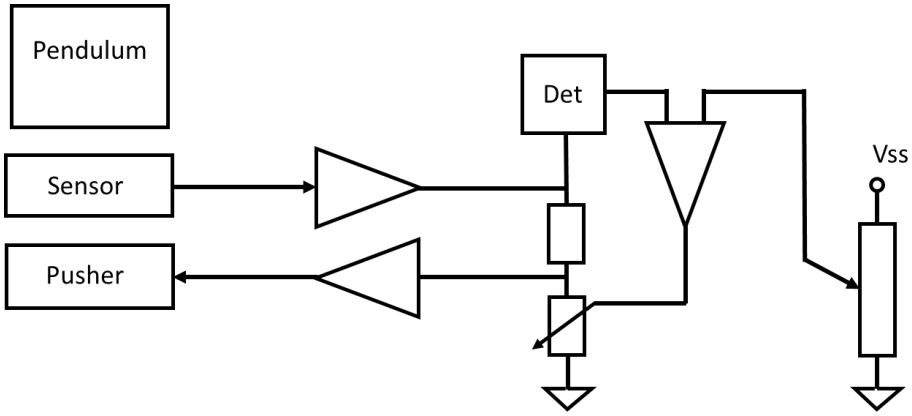


Figure 5 - Oscillation control functional diagram

Realization of functional diagram on figure was kept in mind to make a module on Figure 5.The module, that is demonstrated on Figure 5, contains an instrumentational amplifier U2 that takes the sensing signal: instrumentational amplifier was chosen to vanish a small mutual inductance and for noise reduction on sensing coils that could happen during the bob's movement. Then, that signal is amplified and inverted by 10 on U1 and moved to the external interface. Signal from U2 is

divided by precision resistor matrix or that could be adjusted through external trimmer P1 that is shown as connector. U3 is used as buffer stage. U4 has forming a pusher signal and could signalize about: Thermal Shutdown (TSD), Sinking Current Limit (ISCL), Sourcing Current Limit (ISRC) through LEDs installed on board.

LEDs are expected to use during adjustment in order not to saturate the output of the module and at the same time not to underdrive the pushing coil: once adjusted, it doesn't need to change much and expected to be substituted with a regular precision resistors.

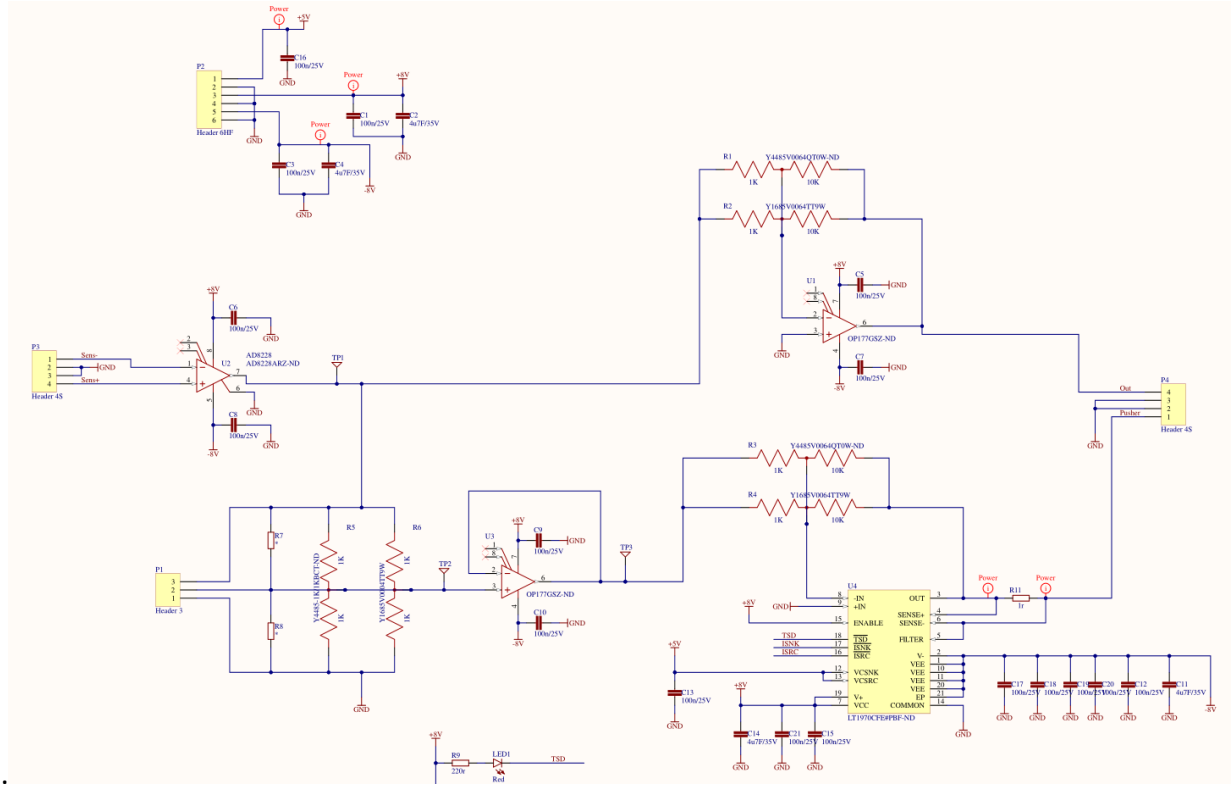


Figure 5- Oscillation loop module Schematics

Complete PCB assembly has the dimensions that are shown on Figure 6.

The dimensions were selected as half of other modules length, mentioned below. The trimmer P1, by idea, kept in mind to be connected through wires outside, adjusted and the then subsituted with R5,R6 and discrete R7 and R8 shown on Figures 5 and 6.

Sockets were choosen of their aviability, simplicity and those female BLS connectors were stiff enough to provide rigid connection to the motherboard. The thermal design was considered that amplifier U4 would dissipate heat through ground plane on PCB. Moreover, we don't push much of power: less than half a watt in peak. That's why everything remains cold.

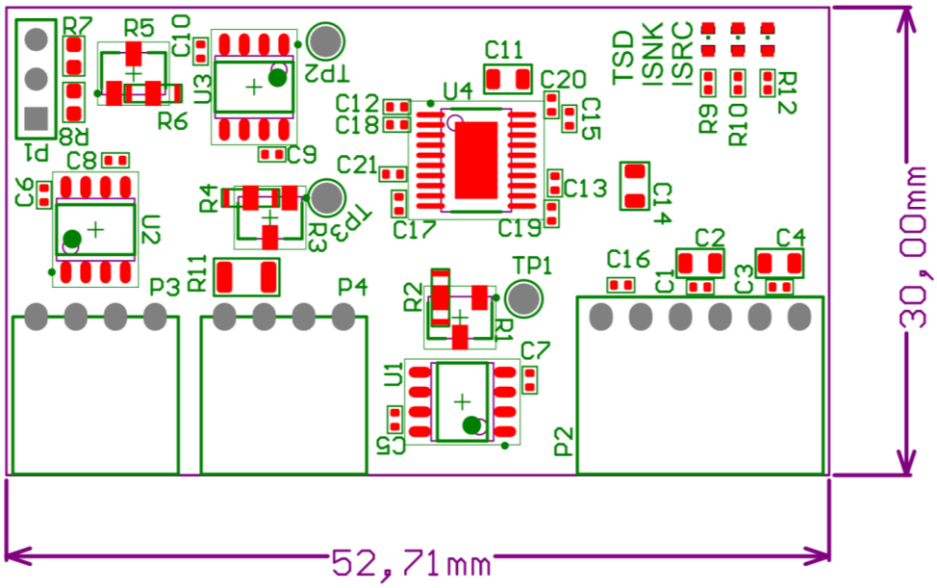


Figure 6- Oscillation loop PCB

3.2.1. Frequency Multiplier

The concept of frequency multiplier is based around property of multiplication of sinusoidal waveforms. During the discussions it was determined that Frequency Multiplier by 16 should be designed at first. The basic principle is around that mixer gives you

$$IF = A_1 \sin(w_1 t + \varphi_2) * A_2 \sin(w_2 t + \varphi_2)$$

Since that $\varphi_1 = \varphi_2 = 0$ and $w_1 = w_2 = w$, $A_1 = A_2 = A$ then:

$$IF = \frac{A^2}{2}(1 - \cos(2wt)) = \frac{A^2}{2} sin^2(wt)$$

In more simple terms $F_{RF} + F_{LO} = F_{IF1}$ AND $F_{RF} - F_{LO} = F_{IF2}$, but if the same frequency used at both inputs $F_{in} + F_{in} = 2F_{in} + DC$.

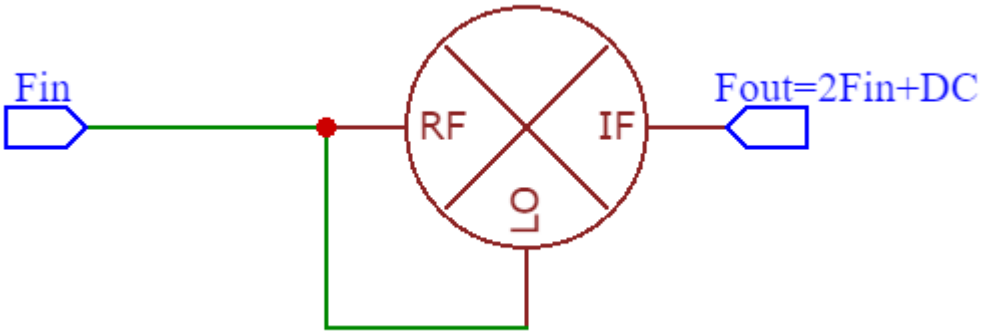
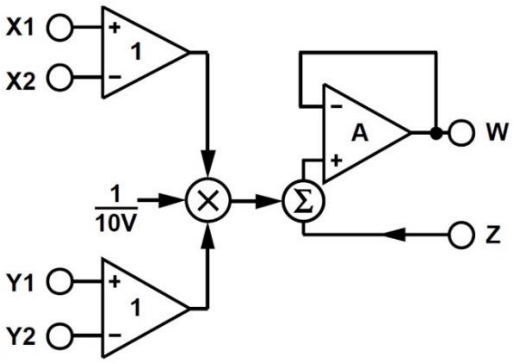


Figure 6- Doubler based on RF mixer

The Multiplication at the circuit level of two signals could be performed by a Gilbert Cell and after a search on the market, namely: AD633 on figure 7 and AD834 on figure 8. The main criteria were low noise, DC coupled (working from 1 Hz).



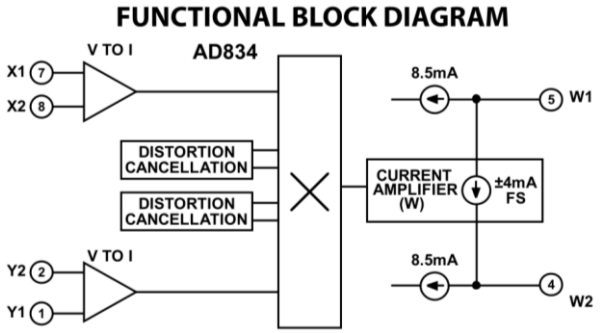


Figure 7 - AD633 Functional diagram

Figure 8-AD834 Functional diagram

The main difference between them is the output interface shown on Fig. 7 and 8 and the spectrum of output signals. AD633 gives a more distorted output then AD834, but both does it with odd harmonics of the input signal. Both multipliers at the output are giving DC. Since that we didn't knew characteristics of those ICs in our low frequency case-we had to prototype and select one of those as frequency multipliers. Many parameters are not or partially specified for 1-32Hz frequency range.

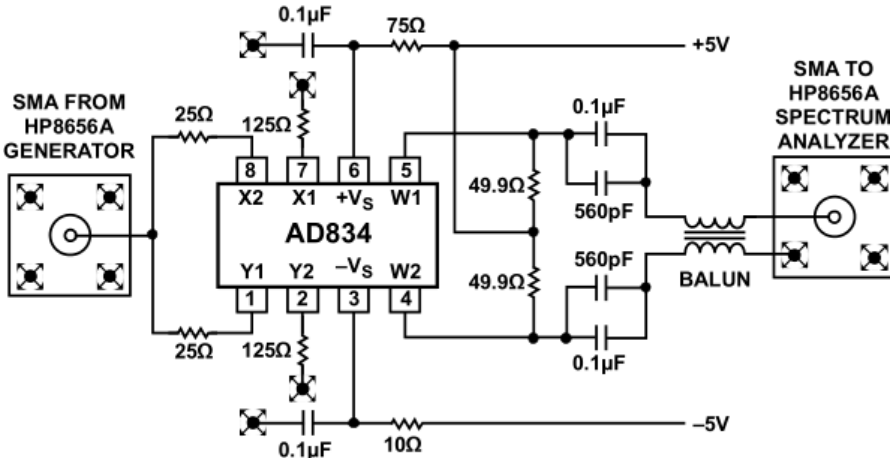


Figure 9 - AD834 reference schematics

AD834 setup that is shown on Figure 9 was used at start, but since that transformer that is used as balancing unit for conversion from balanced output of AD834 to unbalanced output (on the right side of Figure 9) for 1Hz input would be too big-we decided to use an instrumentational amplifier LT1067 instead (Ref.5). But both outputs are depended on 49.9Ohm resistors that in the ideal case shouldn't differ from each other: a single package for 2 trimmer resistors. But the signal after instrumental amplifier had a too large DC component output because of a resistor mismatch and internal structure of AD834 giving a huge DC offset of around 4.5V.

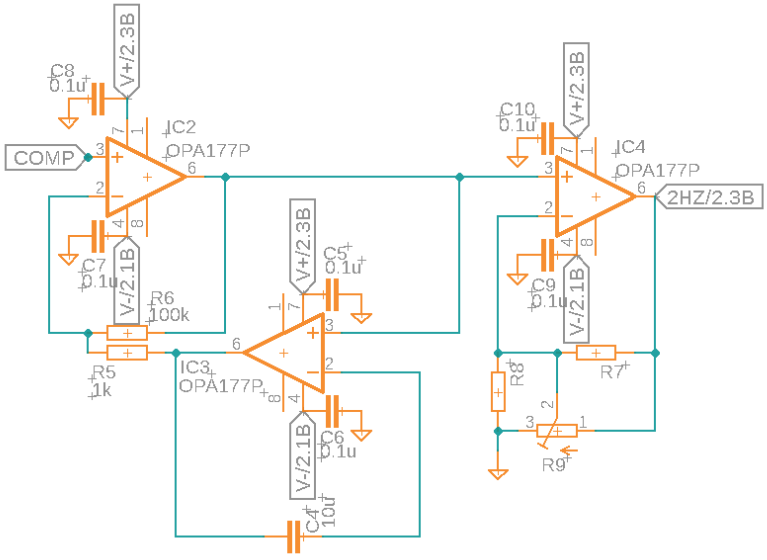


Figure 10 - DC compensation circuit

A small circuit that is shown on Figure 10 was proposed to make a DC compensation because when any amount of DC goes to the input of the next stage of very same frequency multiplier-it gives a signal with a high level of 2nd harmonic because of multiplication process of sinusoidal waves by a constant. That's why signal should be AC-coupled, but in our case, we need to reduce DC part as much, as we could do it.

The input of the circuit on figure 10 has the label “COMP”, and the output has the label “2HZ/2.3B”, where trimmer R9 is used to adjust an amplitude of output signal to the level of 1 Vpp. The OPAMP IC2 subtracts what was Integrated by the IC3 and then gives the AC signal with the DC offset less than 1mV. Moreover, that circuit needs a pure sine wave, otherwise it would give a distorted output. What was discovered next is that AD834 is a highly dependent on the input amplitude that should have around 15mVp-p window. Otherwise, distortions would be too high. Considering all the issues and the price of components for an entire unit we decided to try with AD633, moreover we had samples of those.

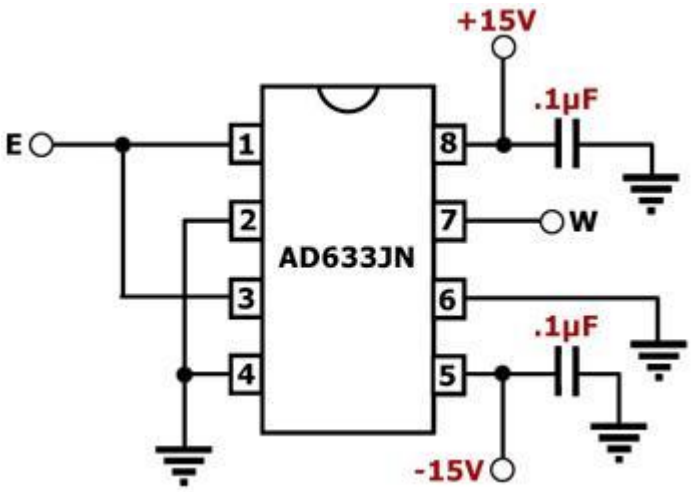


Figure 11 - squaring configuration of AD633JN

The circuit on figure 11 was used for all the measurements and had a great advantage:

1)Simpler design

2)Not relies on precision resistors

3)Unbalanced output and ease of interface

4)Wide range of input voltages (more than 1 Vp-p window)

5)Lower cost

But at the same time AD633 was giving at the output more distorted signal.

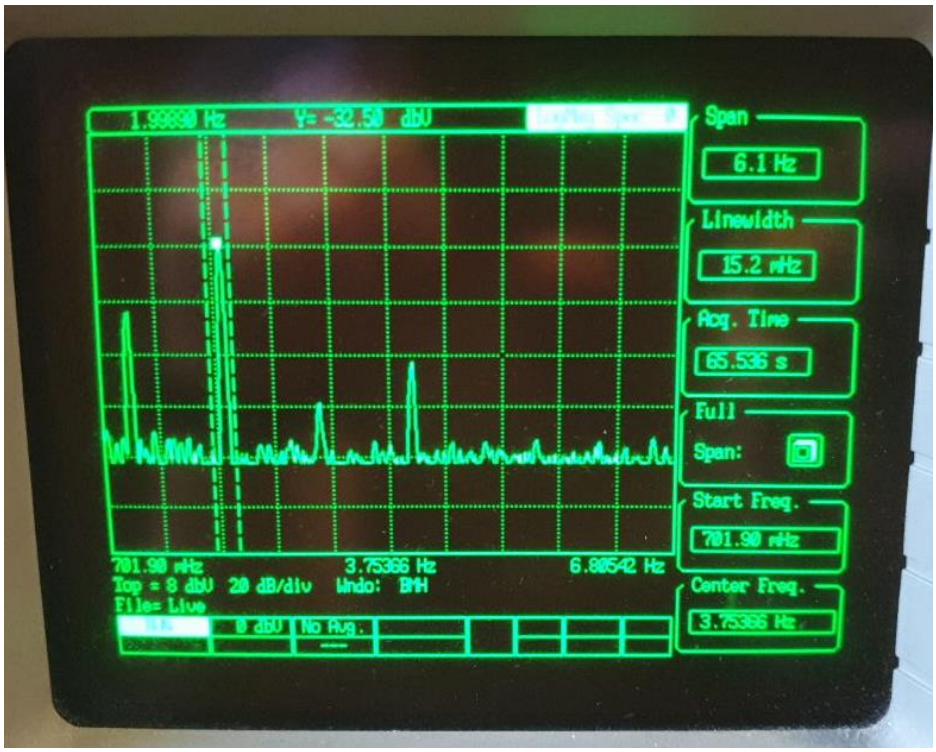


Figure 12- Spectrum components of a single stage

As you can see on figure 12 the 3Hz harmonic is lower than 4 Hz harmonic by 36dB that would require to recover the signal after multiple stages of multiplication: in our case we need at least 16Hz output on a single module, that is 4 stages.

Figure 13 -The multiplication by 2 without DC compensation circuit

Figure 14- Multiplication by 8 with the DC compensation circuit

Figure 15- Multiplication by 16 with the DC compensator circuit

As you can see on Figures 13-15 the problem of signal distortion of each stage becomes more and more important, at the end distortions would be too high for usage in PLL circuit. The problem is that any small DC component of a signal going through frequency multiplier will lead to heavily distorted signal.

To check the concept, a small board was designed for a frequency multiplier.

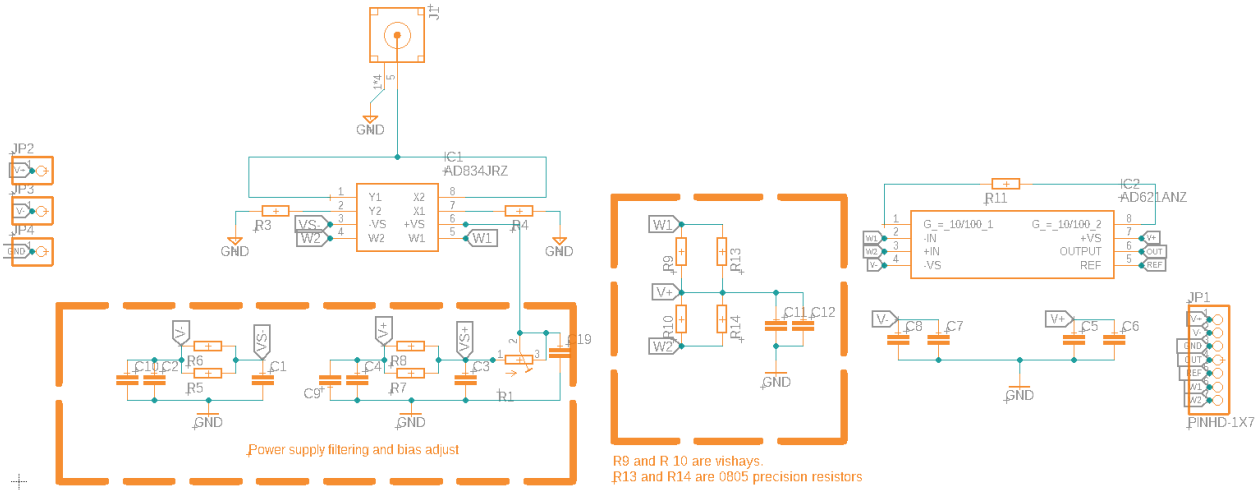


Figure 16- Schematics of the multiplier by 2

Mainly, the prototype was based around AD834 datasheet's reference schematics that is shown on Figure 9, but since than it has "BALUN"- the balancing unit in Output stage that would convert balanced output of AD834 to unbalanced and compensate for DC offsets at the outputs-there is no big problem at the frequencies higher than 100KHz because the dimensions of balancing unit transformer would have the size of around match's head. But in case of 2Hz it would be large, bulky transformer with a lot of parasitic components in it. That's why we decided to use instead two precise resistors that is shown on Fig. 16 (R9, R10 OR R13, R14) and the instrumentational

amplifier IC2 after those resistors. For the proper functioning of AD834 on Figure 8, the Biasing resistors on Figure 16 (R5, R6, R7, R8, R1) are needed in the positive power supply rail of the multiplier IC, also the resistors (R9, R10 OR R13, R14) mentioned above. Calculations followed by the datasheet(Ref.2) gave the values same as in the reference schematics, but they were giving poor results of the output mismatch. Then, the provided place for a trimmer(R1) on Figure 16 at the positive rail was used, according to the datasheet: only a positive rail should be biased. After a manual adjust of a trimmer(R1) to get the best signal output on oscilloscope, values were recorded and then used for other modules to get to the 16Hz output. Initially, AD621 instrumentational OPAMP was selected, but it was self-oscillating at any given input, and we substituted that one to LT1167, luckily it has the same pinout. To our surprise the circuit gave a large DC offset of around 1 V and around 200mVp of useful signal. Because of that, the circuit on figure 10 was made on prototyping part of PCB on figure 17.

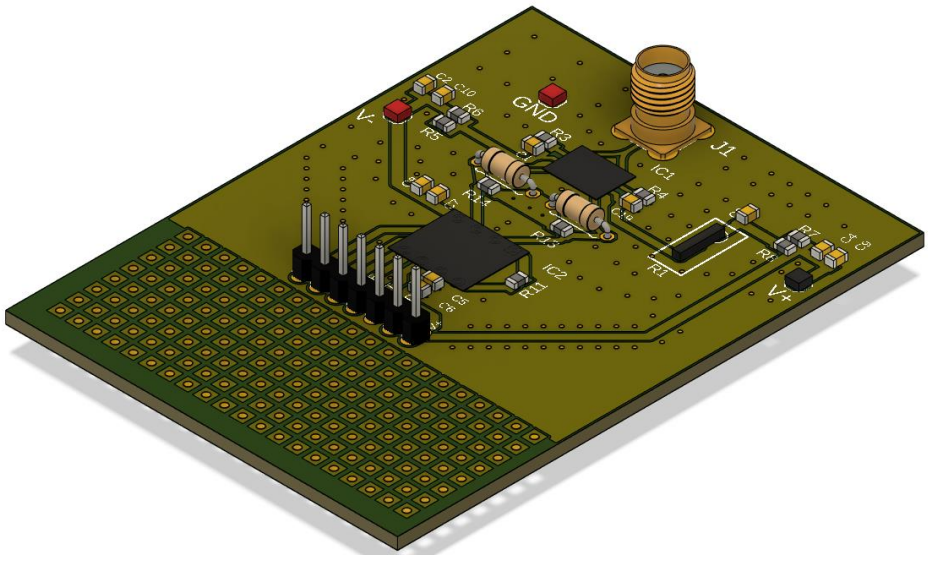


Figure 17- Multiplier by 2 PCB, 3D rendered

The board had everything in schematics, many of the components has an alternative footprint in case of the parallel combination to get an intended value. Choice of the precision resistors of the different surface mount sizes was wide: from 0402 to 1206-dimension types could be placed at the triangle in the center of board, shown on the center of figure 17 and 18. If any of Vishay's Z-foil series resistors that have 0.01% precision were selected-there is a place for those trough-hole components too. Down part of the board was intended to be used for prototyping of a small extra circuits instead of breadboards. The dimensions of pads and holes are taken in specific way to solder 0805 passive components, but at the same time DIP ICs could be soldered too as it seen on figures 16, 17 and 18.

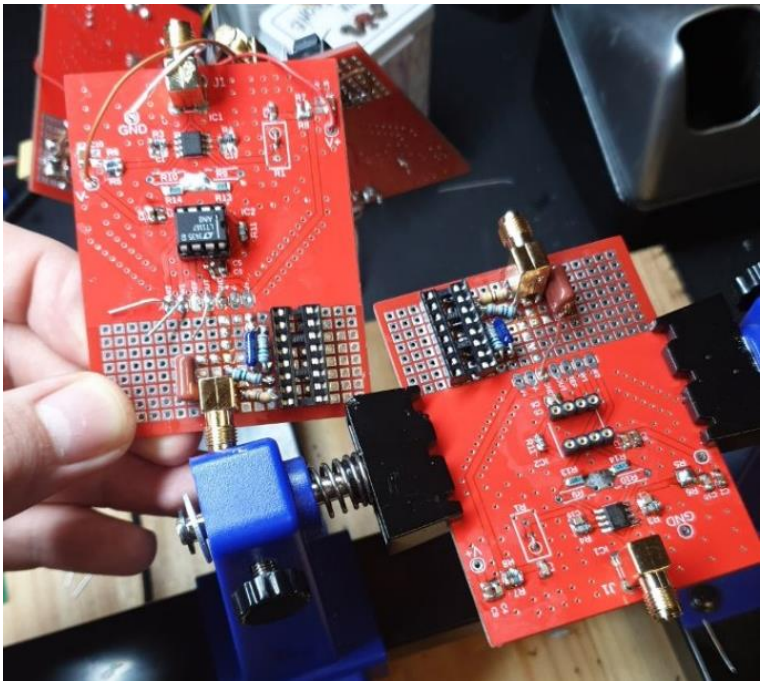


Figure 18 - multiplier PCBs with DC Compensator assembled in prototyping area

But at the same time those boards became cost and time consuming. They were giving a slight advantage in performance comparison with AD633 ICs. That's why we decided to try AD633 multipliers for the same approach. AD633 was a lot easier to adjust, doesn't needed much of

passive components: only decoupling capacitors and DC offset compensation circuit that is demonstrated on Fig. 11 and 10.

That's why a breadboard assembly was done for testing AD633 with some small filtering between stages, as shown on figure 18. The circuit shown on figure 10 had an extra low pass filter at the output of each multiplier's DC component compensator module to filter out noise and unwanted signal components.

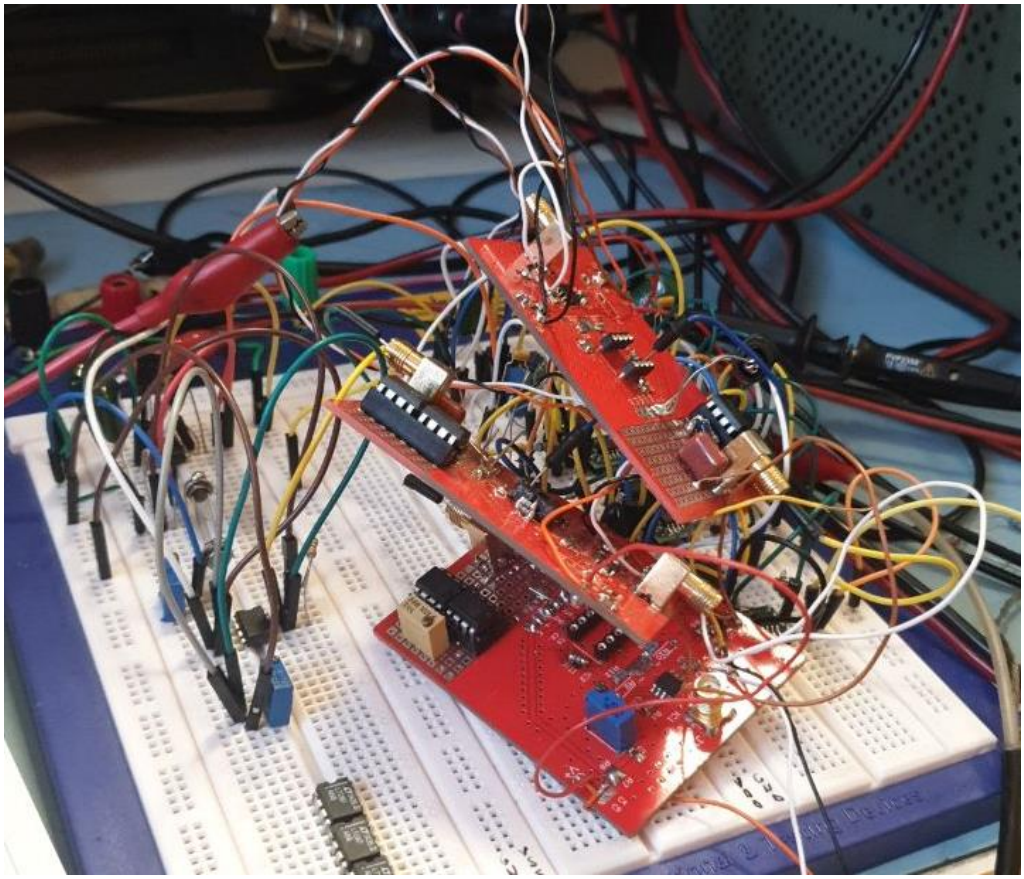


Figure 19 - Breadboard testing

The breadboard on figure 19 was utilizing ad633 multipliers and DC compensation circuits assembled before for AD834. According to schematics on Figures 10 and 16-it is only needed to pull out from the sockets instrumentational opamps IC2 on Figure 17 and use pin 6(output) of IC2 as an input for dc compensation between multiplier stages, the output of a DC compensator that was shown on figure 10 should be connected to the next multiplier stage. Assembly on figure 16 was done fast to test the circuit and compare results. If the signal at the output of entire multiplier's system would be too bad for a phase comparison, the circuits wouldn't make sense: at least it should have the shape that has a continuous phase value, amplitude differences would be acceptable or at least it could be dealt after multiplication. It could be desirable to try to lock on 1Hz frequency, but it would take too much time to lock. Moreover, it would need more resolution and stability for DDS sine wave generator, than the range of VCO quartz oscillator is limited. That's why 32 Hz was good enough or better would be to move up in frequency.

Figure 20 - 16Hz output of ad633 based multiplier

That quality of output signal on Figure 20 was acceptable for a phase comparison unit. The design based on AD633 ICs was selected for further development of multiplier modules.

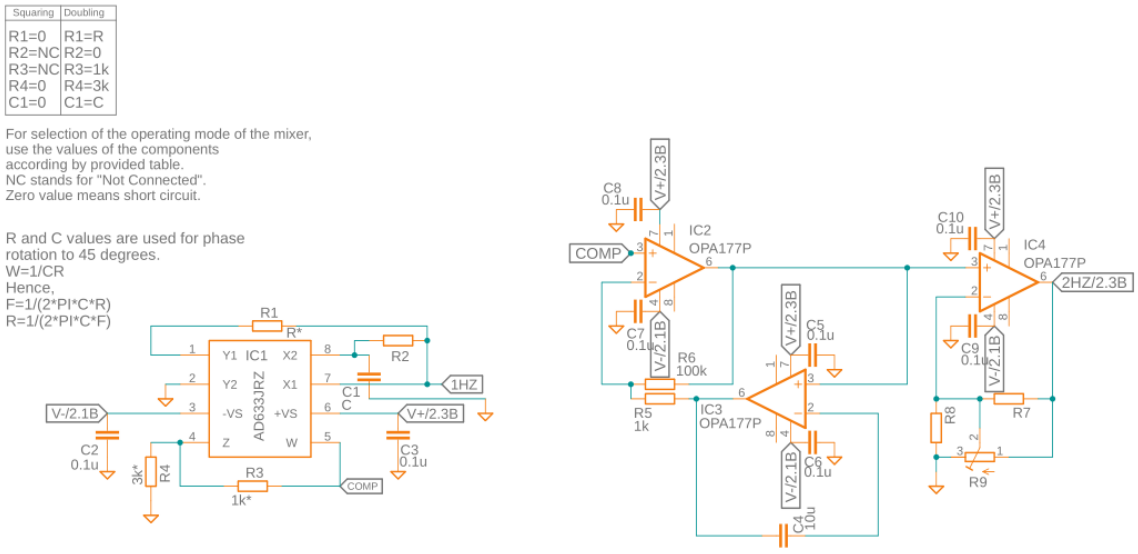


Figure 21 - schematics of a single stage multiplier

Each stage of a multiplier is configurable by two variants: squaring-type multiplier, that is shown on Figure 11, or another configuration of 45 degrees phase shifted multiplier (Ref. 3). By following table in schematics, it could be configured as specific type of the circuit. But we used only “squaring” configuration.

Then it goes to DC compensation circuit on Figure 21 (IC2, IC3), after that is an interfacing amplifier IC4 is used to recover the signal level for the next stage.

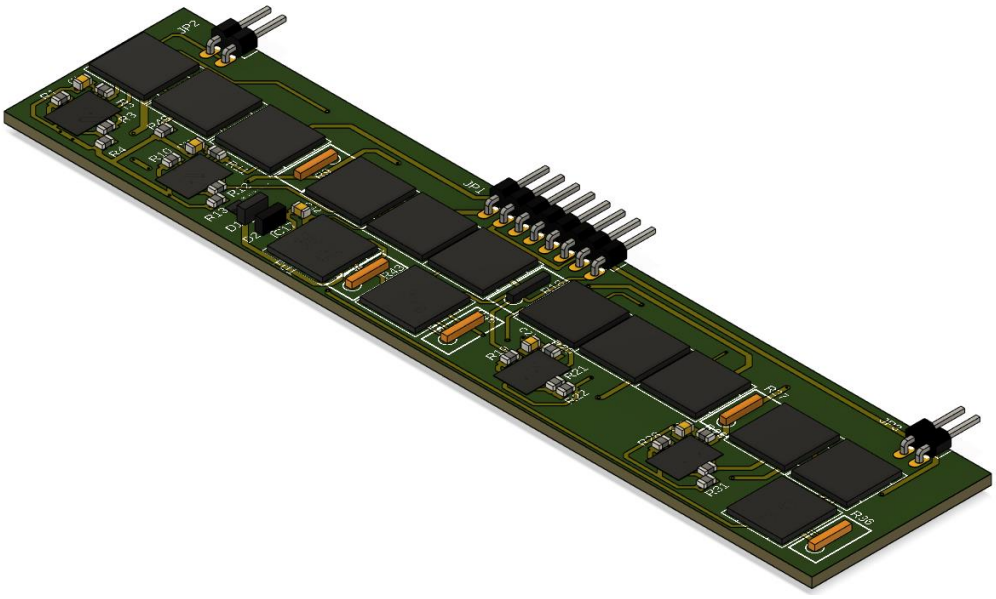


Figure 22 - AD633 multiplier PCB

The board's dimensions are shown on figure 22 are 135x30mm because that's an area that is available under the pendulum to connect everything to the motherboard.

The board has 4 stages of multiplication and a Wien Bridge Oscillator (described in the next chapter) used for the signal recovery after multiplication. Components are placed on the both sides, trimmers are used for the signal level adjustment in case if input was too small or too large, but the places for fixed-value resistors are foreseen. Those resistors R7, R8 on Fig.21 are used for gain selection after adjustments that were done by the trimmer R9.

The connectors at the corner are connected to GND and used for mechanical stability of the PCB, otherwise the connection on the central connector wouldn't be stable, and the board would sway around, then generate random spikes on pins. Moreover, each stage of output is connected to the central connector if lower frequency is needed. Board is placed among the movement of a pendulum's bob that wouldn't create problems.

3.2.2. Wien Bridge Injection Lock

Because of the specifics of the chosen multiplier approach by usage of AD633 Analog Multiplier signal going out of multiplier is not perfect as demonstrated on figure 23.

Figure 23 - 16Hz multiplier's stage output, yellow-1Hz, cyan-16Hz output of 4th stage multiplier

The situation of figure 23 probably happened due to large even harmonics and DC component in the output signal of the multiplier's 16Hz stage. The signal itself has problems caused by very small DC component of the signal caused by imperfections of compensator circuit shown on figure 10.

The problem of that circuit is that it should take ideal Sine wave signal, but in a case of distorted signal the compensation circuit wouldn't be perfect.

The solution is to recover the signal or make another compensator, that works better or both.

Even if entire DC component would be reduced to zero there would be still changes of the signal caused by multiplier IC's internal structure (Ref.3)

That's why an oscillator circuit was proposed on figure 24.

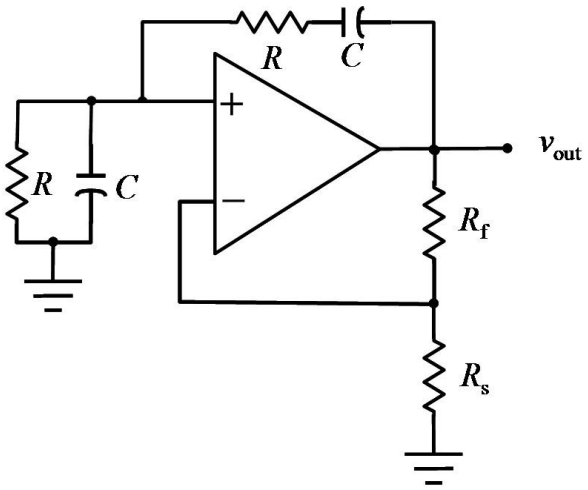


Figure 24 - Wien Bridge oscillator

Wien bridge is a type that was developed by Max Wien 1891(Ref.8).

At the time of the Wien bridge's invention, bridge circuits as Wheatstone bridge were a common way of measuring component values by comparing them to known values. An unknown component would be put in one arm of a bridge, and then the bridge would be nullified by adjusting the other arms or changing the frequency of the voltage source. For example: the Wheatstone bridge.

The Wien bridge is one of many common bridge circuits. Wien's bridge is used for precision measurement of capacitance in terms of resistance and frequency. It could be used to measure audio frequencies.

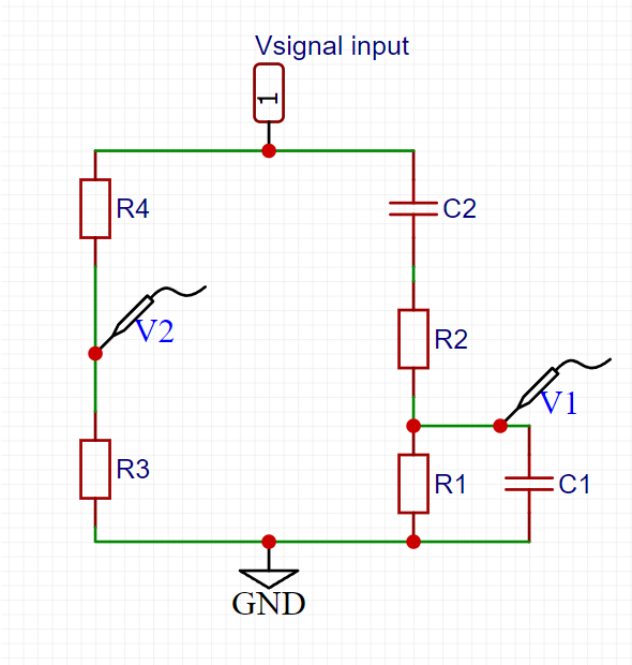


Figure 25 - Wien bridge

The bridge on figure 25 consists of a series RC circuit connected to a parallel RC, where R1=R2 and C1=C2 forming a High Pass Filter connected to a Low Pass Filter producing a second-order frequency dependent Band Pass Filter with a high Q factor at the selected frequency, ƒr.

At the low frequencies the reactance of the series capacitor (C2) is very high, so it acts like an open circuit, blocking any input signal at Vin resulting in virtually no output signal, Vout. Likewise, at high frequencies, the reactance of the parallel capacitor, (C1) becomes very low, so this parallel connected capacitor acts as a short circuit across the output, so again, there is no output signal.

There must be a frequency point between these two extremes of C2 being open-circuited and C1 being short-circuited where the output voltage, V1 reaches its maximum value. The frequency value of the input waveform at which this happens is called the oscillator's Resonant Frequency (ƒr). At this resonant frequency, the circuit's reactance equals its resistance, that is: Xc = R, and the

phase difference between the input and output equals zero degrees. The magnitude of the output voltage is at its maximum and is equal to one third (1/3) of the input voltage as shown on figure 26. Vsignal to allow for oscillations to occur. To understand why the output from the RC circuit on figure 26 needs to be one-third, that is 0.333xVin, we must consider the complex impedance (Z = R ± jX) of the two connected RC circuits. We know that the real part of the complex impedance is the resistance, R while the imaginary part is the reactance, X. As we are dealing with capacitors, the reactance part would be a capacitive reactance Xc.

As said previously that the magnitude of the output Voltage V1 as in it is maximum is (1/3) of input voltage.

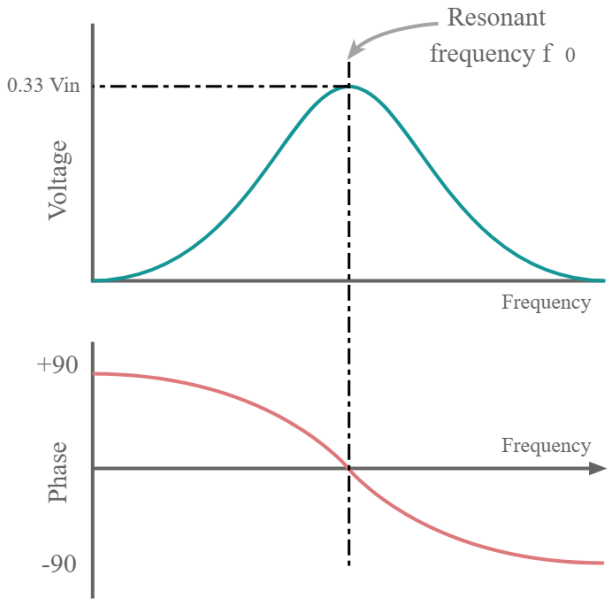


Figure 26 - Wien bridge phase and bode plot

It can be seen , on figure 26 ,that in low frequencies the phase between input and output signal is Phase Advanced, but at the high frequencies is Phase Delayed. In the middle there is a middle point fr with two signals being at zero phase shift. That point is defined by:

$$fr = \frac{1}{2\pi RC}$$

R is the value of R1=R2

C is the value of C1=C2

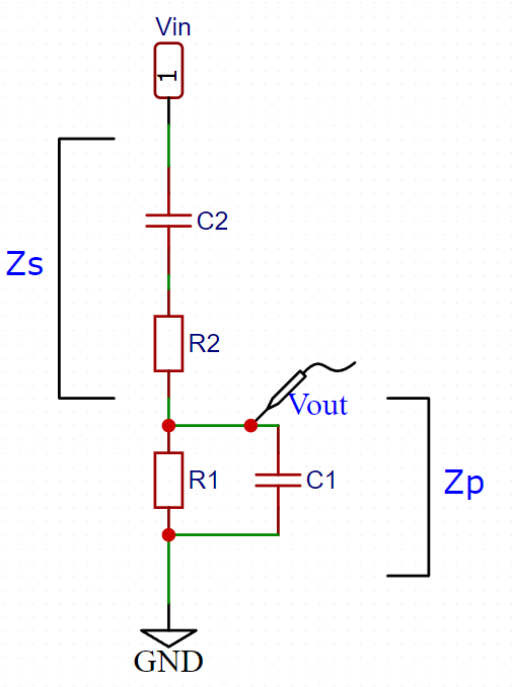


Figure 27 - RC Network part of Wien Bridge

After redrawing the figure 25 as shown on Fig. 27, it is visible that it consists of two RC circuits that are connected together: High pass filter and Low Pass filter.

We can recall that:

$$Z_s = \frac{R_2C_2s+1}{C_2s} \quad , \quad Z_p = \frac{R_1}{R_1C_1s+1}$$

Then, $Z_{out} = \frac{Z_p}{Z_p + Z_s}$ but when everything is chosen for Fr the Zout=1/3

For oscillator should be faced a condition when system becomes non-linear and self-oscillates.

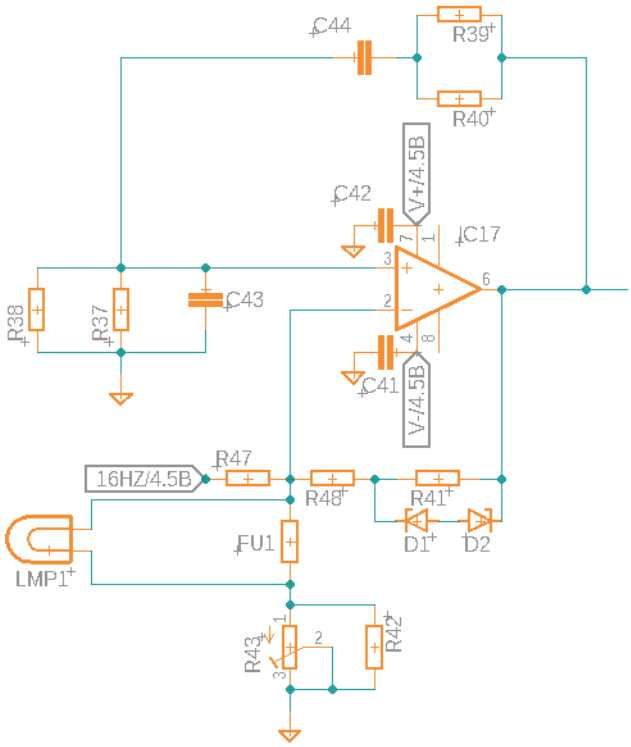


Figure 28 - Wien Bridge Oscillator

In that implementation, demonstrated on figure 28 , was chosen a classical approach with a Lightbulb LMP1 to stabilize amplitude because our criteria:

$$\frac{R_{41} + R_{48}}{R(LMP1) + R_{42}} > 2$$

But that kind of generator, shown on Figure 28, can saturate because of positive feedback and that's why lightbulb is used because it has Positive Temperature Coefficient and that changes the gain of the circuit.

But because of instability of class 2 capacitors (X7R type) that we use and because of their 10% precision we had to adjust values of resistors to get the 16Hz frequency (REF.9).

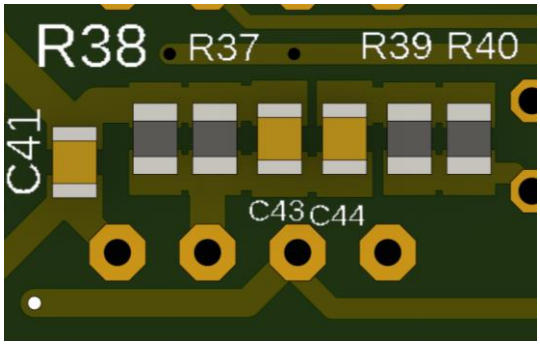


Figure 29 - PCB part with wien bridge

Wien bridge parts were put close to each other as shown on Figure 29 in order to have close temperature variation between components.

But that generator is not-in phase and works separately comparing to our circuit.

So, that's why we needed an injection locked oscillator to recover the signal(Ref. 13).

Oscillatory systems are generally prone to injection locking or pulling.(Ref.10).

It was observed that two pendulum clocks on the wall moved in unison close to each other or the same happens when you put two metronomes close to each other. In case of humans that were left in isolated bunkers reveal a sleep-wake period of about 25 Hours but when they were brought back in the nature, they are injection-locked to the Earth's cycle.

When an external ideal variable oscillator interacts with a self-sustainable oscillator, two cases can be obtained: a beat note, if two signals are available or a dead band, if self-sustainable oscillator is not detected. An ideal oscillator cannot be locked with a forced signal outside of the natural frequency of ideal oscillator due to its very narrow Q and at the same time it means that it has no losses. The sensitivity of oscillator to be locked is related to the amplitude of the locking signal and the energy stored in oscillator. If an oscillator is receiving small external forcing signal from outside and the difference in frequency is too high, a beating process would take a place due to presence of two signals at the same time: intrinsic frequency that supports natural frequency of an oscillator and external forcing frequency. If the external signal is near the natural frequency of an oscillator-only one signal would be observed with the frequency of the external signal and the oscillator dead band: such condition is called locking. To obtain two conditions mentioned above we will assume that only one signal is present in the oscillator, an instantaneous frequency with a variable envelope. Let's start with Kirchhoff's law for parallel RLC Circuit:

$$i_1(t) = c\frac{dv(t)}{dt} + \frac{v(t)}{R} + \frac{1}{L}\int_{-\infty}^{t} v(\tau)\mathrm{d}\tau$$

One of the solutions is to define an external signal as:

$$i_1(t) = I_1(t)\mathrm{e}^{i\omega_1 t} \text{ and the response as } v(t) = V(t)\mathrm{e}^{i(\omega_1 t+\phi(t))}$$

It is needed to be mentioned that response frequency is:

$$\omega = \omega_1 + d\phi(t)/\mathrm{d}t$$

For simplicity, a successive parts integral is performed for the inductor element and the two largest terms are retained (the exponent in the frequency and the order in the envelope derivative make the other terms negligible). By the definition of natural frequency of oscillator:

$$\omega_0^2 = \frac{1}{LC}$$

By keeping real and imaginary part separate, we are getting the expressions

$$\left(1 + \frac{\omega_0^2}{\omega_1^2}\right)\frac{\mathrm{d}V(t)}{\mathrm{d}t} + \frac{V(t)}{CR} = \frac{I_1(t)}{C}\cos\big(\phi(t)\big)$$

$$\left(1 + \frac{\omega_0^2}{\omega_1^2}\right)\frac{\mathrm{d}\phi(t)}{\mathrm{d}t} + \left(\omega_1 - \frac{\omega_0^2}{\omega_1}\right) = -\frac{I_1(t)}{CV(t)}\sin\left(\phi(t)\right)$$

The external signal introduce it is own frequency and amplitude because the phase can be set to zero, the response signal is determined by the signal envelope V(t) and instantaneous phase $\phi(t)$.After simplifications, it is possible to recognize the region where injection locking occurs:

$$\Delta\omega_{\text{beat}} = \omega - \omega_1 \equiv 0$$

This condition defines a region, where $\frac{\mathrm{d}\phi(t)}{\mathrm{d}t} = 0$ and it will simplify equation mentioned above that forces the other condition for the dead band bandwidth:

$$\omega_{+-} \cong \omega_0 \pm \frac{I_1}{2CV_0}$$

The synchronization could be analyzed by coupling two oscillators, an extension of previous solution is followed, assuming that: $v_1(t) = V_1(t)\mathrm{e}^{i\phi_1(t)}\mathrm{e}^{i\omega_1(t)t}$ and $v_2(t) = V_2(t)\mathrm{e}^{i\phi_2(t)}\mathrm{e}^{i\omega_1(t)t}$ total response is followed, having a natural frequency $\omega_{01}^2 = \frac{1}{L_1C_1}$ and $\omega_{02}^2 = \frac{1}{L_2C_2}$ we get:

$$\left(1 + \frac{\omega_{0i}^2}{\omega_1^2}\right)\frac{\mathrm{d}V_i(t)}{\mathrm{d}t} + \frac{V_i(t)}{C_iR_i} + \frac{V_i(t)}{C_iR_x} = \frac{V_j(t)}{C_iR_x}\cos\left(\phi_j(t) - \phi_i(t)\right)$$

$$\left(1 + \frac{\omega_{0i}^2}{\omega_1^2}\right)\frac{d\phi_i(t)}{\mathrm{d}t} + \left(\omega_1 - \frac{\omega_{0i}^2}{\omega_1}\right) = \frac{V_j(t)}{R_xC_iV_i(t)}\sin\left(\phi_j(t) - \phi_i(t)\right)$$

So, if two oscillators are defined, equations above are valid for small Rx, when indirect connection between two oscillators exists and only one final frequency goes at the output

$$\omega_f^2 = \frac{C_1\omega_{01}^2 + C_2\omega_{02}^2}{C_1 + C_2}$$

Non-linearity makes difficult to predict analytically beyond the approximations shown here. But those results show the capabilities of the circuit, and it is close connections to equations shown here. That's why that circuit needs to be adjusted manually to lock oscillators for the needed requirements. By decreasing the Rx resistor that couples' oscillators external signal could be injected better, but if it is too low-Wien bridge would work as an amplifier instead of a coupled oscillator. But if that Rx would be too large coupling would be too small, beating would occur or nothing would happen (dead band). At the same time Injection Locked Oscillators are modelled as first-order Phase Locked Loop. (Ref. 11,12)

3.2.3 Frequency Synthesizer

As an external frequency synthesizer was used a complete device used before for specific measurements of Z meter of thermoelectric Peltier devices (Ref. 1).

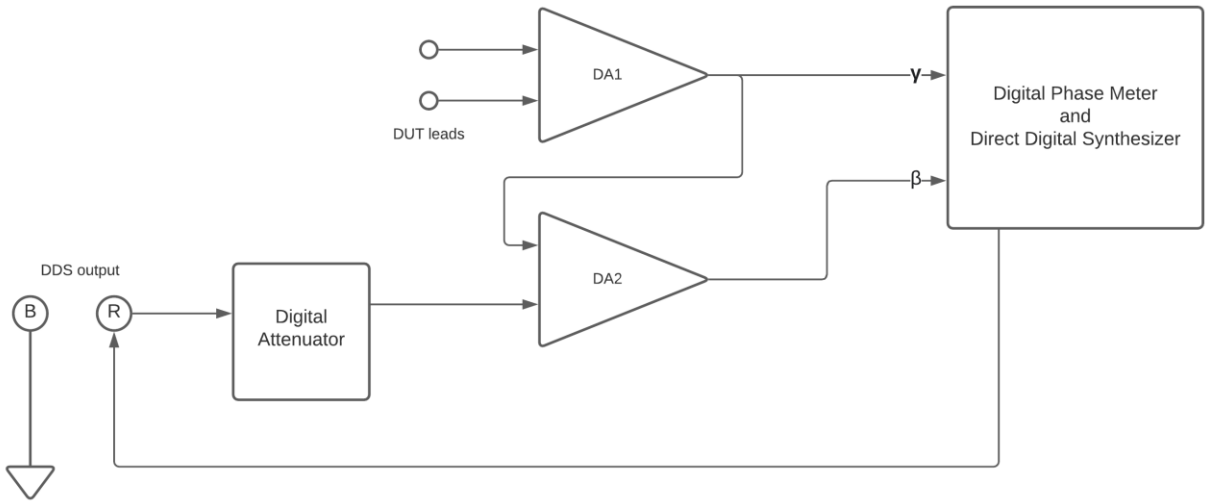


Figure 30-zT meter Functional Diagram

As shown on Figure 30 the instrument generates Sine Wave by Direct Digital synthesis approach and compares the phase of two signals through analog front-end DA1 and DA2, calculations and measurements are performed by a microcontroller. For adjustments of amplitude the precision digital attenuator with high resolution was introduced. The microcontroller manages the user interface too by using HMI embedded panel though UART protocol. Moreover, the instrument has external communication interfaces: USB and RS232 for data acquisition.

The DDS is realized from 80KHz internal clock signal with 16-bit resolution without usage of look-up table because the generated signal is slow enough and thanks to STM32F4 microcontroller used for that task: calculations are performed at each step. The output of digital-to-analog converter is filtered to 5 kHz to smooth the sine wave. The frequency range could be adjusted from 1 mHz to

200 Hz with 1 mHz step, but it could be extended by rewriting the firmware. The amplitude of DDS output can be regulated up to 4 V peak by using a 10 bit digitally controlled attenuator. For accuracy and stability, the array of precision Vishay resistors was used because measurements of that instrument is relying on injected current for Devices Under Test (DUT). The digital attenuator shown on figure 30 is made of two cascaded 10-bit digital attenuator ICs and can therefore finely regulate the attenuation with 20-bit equivalent resolution. That generator should be controlled externally via UART interface of zMeter by VCO quartz oscillator going after pendulum's Phase Sensitive Detector. It is needed to increase stability and resolution of the system.

In our case the measurement part of the Instrument is not needed: we are only interested in DDS sine wave generation.

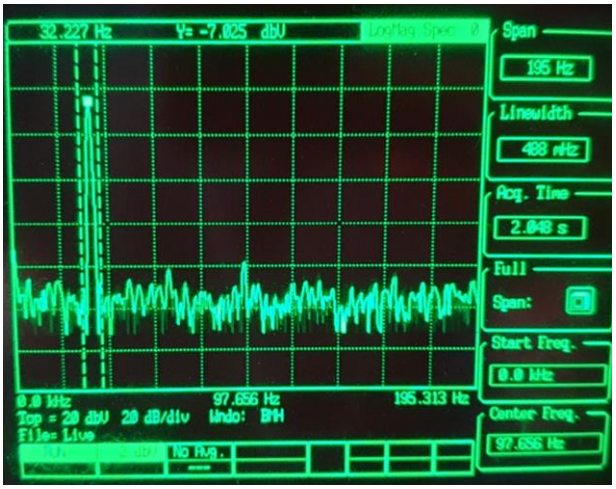


Figure 31- DDS synthesizer spectrum at 32Hz

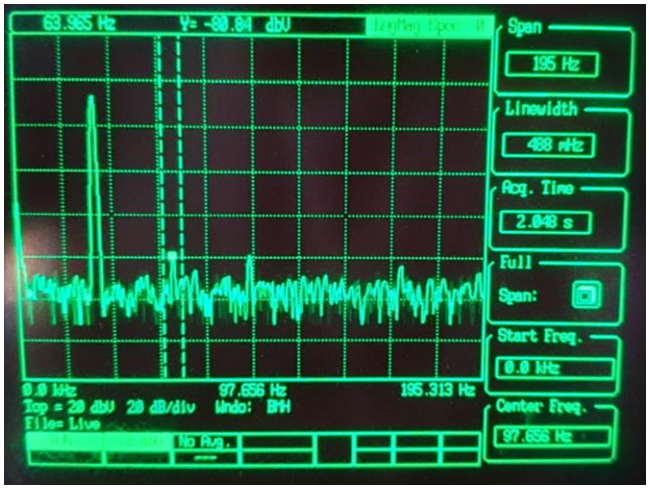


Figure 32- 2nd harmonic in the output

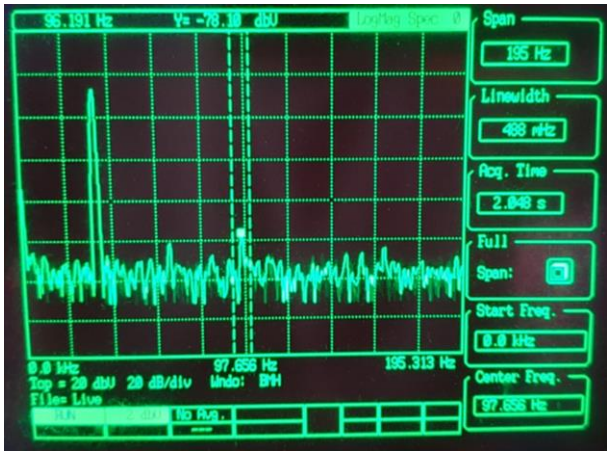
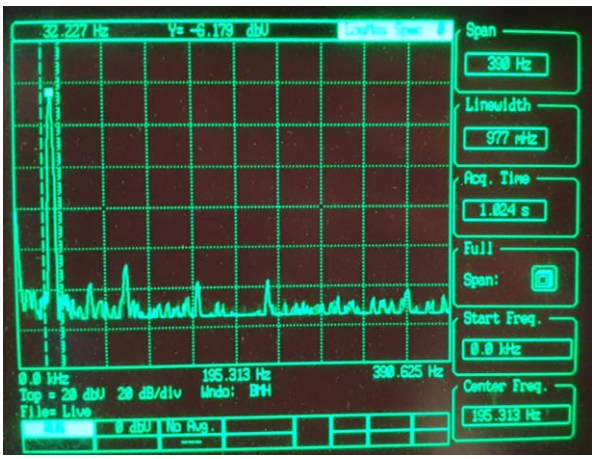


Figure 33-3rd harmonic in the output

As demonstrated on Figures 31,32,33 the spectrum of the signal on 32 Hz is acceptable: there is a 50Hz noise from AC network, a small 2nd and 3rd harmonic (more than 73 and 85 dB difference), probably caused by small impedance mismatch between spectrum analyzer and frequency Synthesizer.

For testing on a bench was used the internal function generator of Rigol DS2072 oscilloscope.



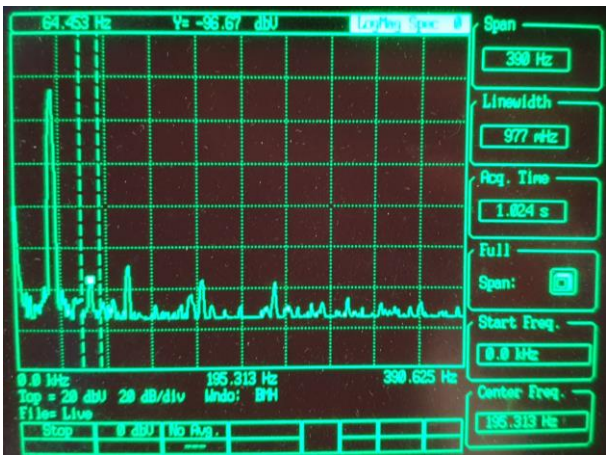


Figure 34- Rigol's generator spectrum at 32Hz Figure 35- 2nd harmonic of the scope's generator

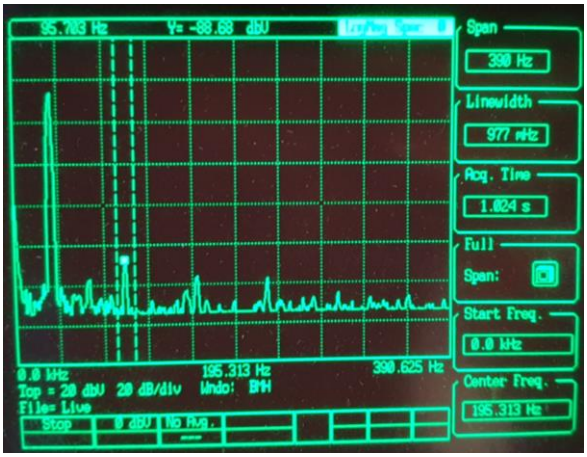


Figure 36-3rd harmonic of the scope's generator

As demonstrated on figures 34, 35, 36 the spectrum of Rigol's generator output is comparable to quality of the output signal of DDS described before. It has 2nd and 3rd harmonic difference more than 92db and 82db difference respectively. There could be errors due to mismatch of a signal generator, but those spectrum diagrams should give a good representation signal quality of DDS and commercial internal signal generator of Rigol DS2072 Oscilloscope.

The good signal quality is needed to get a better phase comparison because when the signal would have too much of even or odd harmonics in the output of both inputs of phase comparator: it could cause problems at the output of phase comparator. But at the same time small errors would be filtered out by the system, in a worst-case small adjustment should be made.

3.2.4. Phase Sensitive Detector

A phase detector, also called a phase comparator is a mixer-like circuit demonstrated on figure 37 that puts out a signal that is proportional to the phase difference between two input signals of the same frequency.

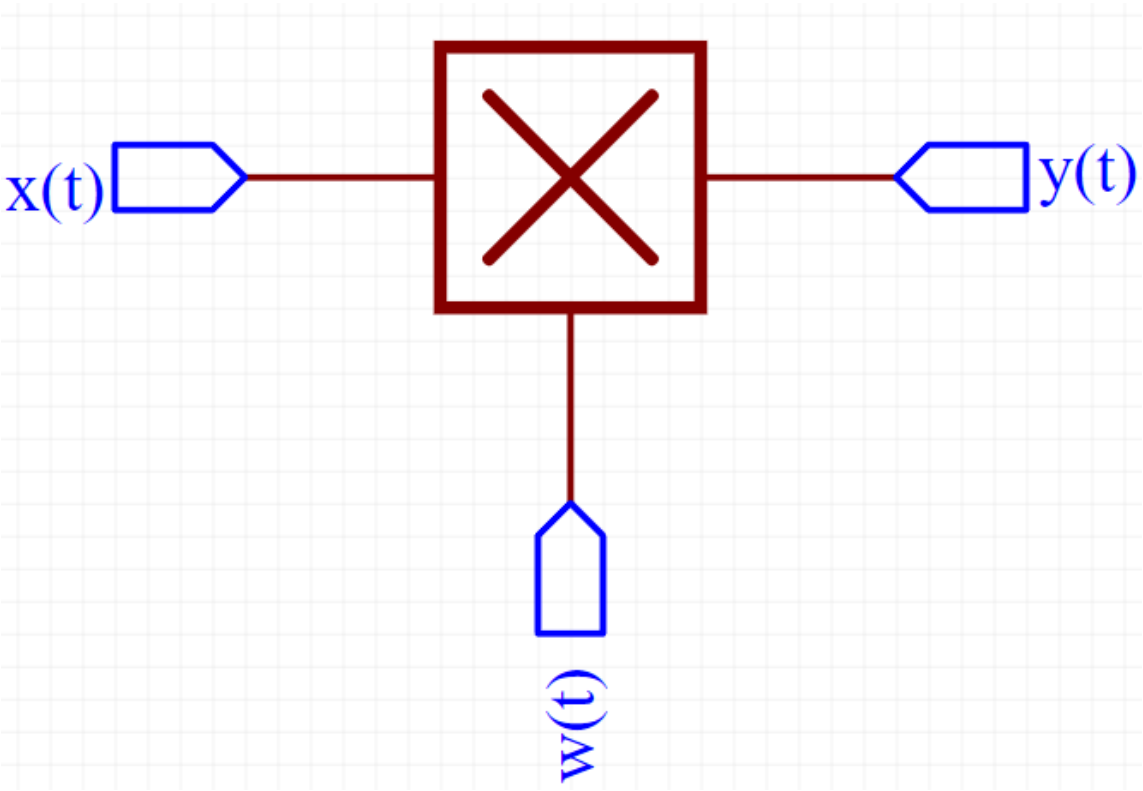


Figure 37 -Conceptual mixer used as a phase comparator

Were,

$$x(t) = A_x \sin(\omega_x t + \phi_x) \text{ and } w(t) = A_w \cos(\omega_w t + \phi_w)$$

Then, the output of a multiplier would be:

$$y(t) = A_x \sin(\omega_x t + \phi_x) A_w \cos(\omega_w t + \phi_w)$$

$$= \frac{1}{2} A_x A_w [\sin(\omega_x t + \omega_w t + \phi_x + \phi_w) + \sin(\omega_x t - \omega_w t + \phi_x - \phi_w)]$$

Usually, the frequencies of the two input signals are close so that $\omega_x = \omega + \frac{1}{2}\Delta\omega$ and $\omega_w = \omega - \frac{1}{2}\Delta\omega$, where $\Delta\omega$ is small and in most phase detector applications either $\Delta\omega = 0$ or a feedback loop attempts to set $\Delta\omega$ to zero so there is little frequency error. So, following lowpass filtering, the output of phase detector is

$$y(t) = \frac{1}{2} A_x A_w \sin(\Delta\omega t + \phi_x - \phi_w)$$

Now $\Delta\omega t$ can be considered as phase error and included in effective phases of the input signals, $\psi_x(t) = \frac{1}{2}\Delta\omega t + \phi_x$ and $\psi_w(t) = -\frac{1}{2}\Delta\omega t + \phi_w$. Then

$$y(t) = \frac{1}{2} A_x A_w \sin[\psi_x(t) - \psi_w(t)]$$

The output signal is proportional to the amplitudes of both the input signals and to their phase difference. In practice the amplitudes of both input signals are scaled to a constant amplitude so that the output only depends on the phase difference.

For Our design we couldn't use XOR or any other "Digital" phase detectors because the signal needs to be digitalized by comparators or Schmidt triggers that samples only one point. That's why mixers were chosen: we had AD834 and AD633, in datasheet it wasn't mentioned that we can use

those as phase detectors and we had to try each other, then choose that fits best, as it was done for Frequency Multipliers.

But because on the module of the Frequency multiplier there wasn't much of space, we had to put one more multiplier to get 32Hz and one more injection locked Wien Bridge Oscillator to recover the signal if it would be too bad for phase comparison as it was described previously.

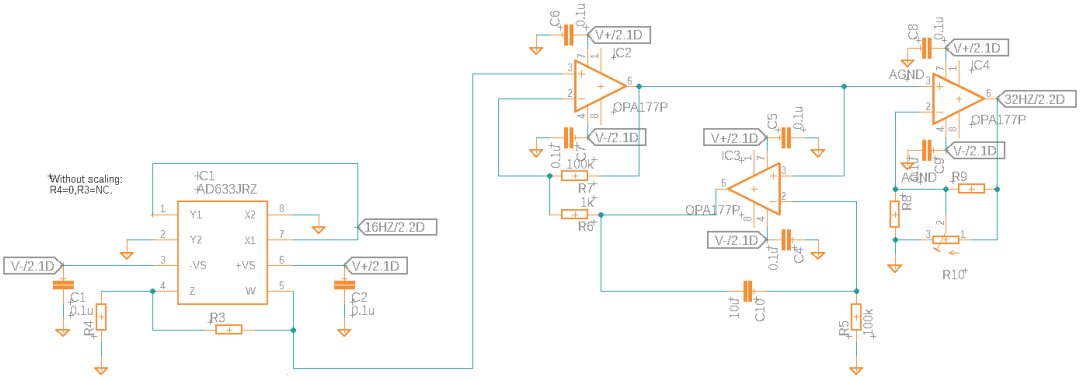


Figure 38 - 32Hz output Multiplier

In that case we decided to use directly "squaring configuration" to multiply the signal. But small area for adjusting was left as R4 and R3 to change "scaling coefficient". The output function of multiplier is:

$$W = \frac{(X1 - X2)(Y1 - Y2)}{10\text{V}} + Z$$

But according to the datasheet(Ref 3)-there is a way to change a scale factor in AD633 as demonstrated on figure 39.

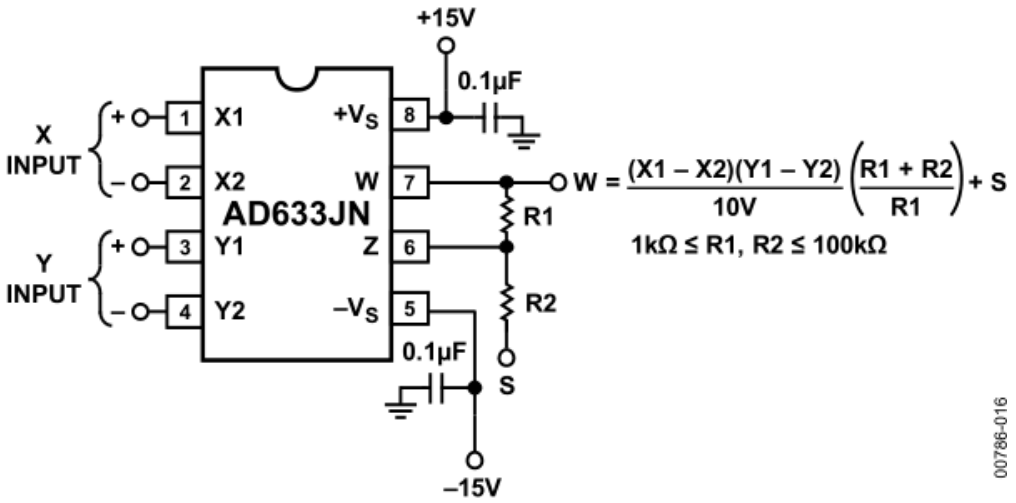


Figure 39 - variable scale factor feature

Then a DC compensator circuit that was described before on Fig.21 at the right side, to give an output voltage. Then, after this goes the Injection Locked Wien Bridge adjusted for 32Hz freewheeling frequency.

That oscillator should be adjusted manually to get the closest frequency 32Hz frequency because, as mentioned before, if injection frequency would be too far from the frequency of oscillator-we would get beating of the output signal. Moreover, the capacitors stability should be considered (Ref.9, 15). Wien bridge oscillator is not linear, and it could be adjusted a little by selection of proper Gain value and proper injection current to get stable output of desired amplitude. But then it would be better to use a buffer stage after what is shown on Figure 28. Because load resistance changes the parameters of injection locked Wien bridge-better to put a buffer. That buffer stage was implemented on board that is shown on Figure 44.

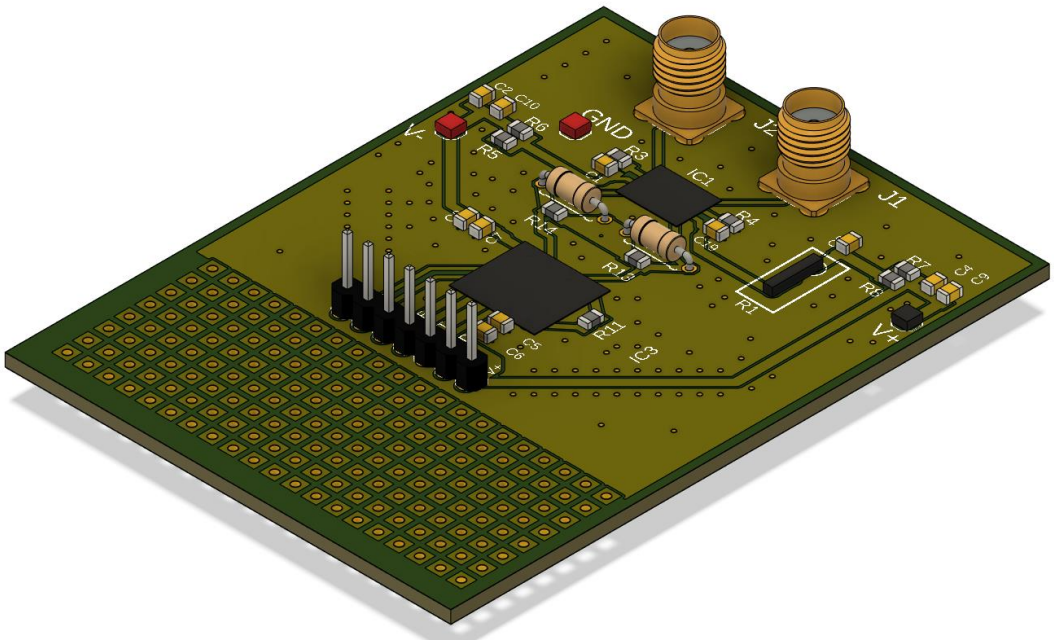


Figure 40 - AD834 phase detector prototype

For multipliers we had to decide which one is better, the prototype board was built and demonstrated on figure 40. It was designed is similar way as multiplier prototype demonstrated on figure 17. On figure 16 two inputs of AD834 are connected directly to single SMA connector, but on this board, shown on figure 37 both inputs are connected through 2 separate SMA connectors to make a phase detector.

By adjusting the AD834 phase detector shown on figure 40 it was giving a distorted, weak signal that couldn't be used as shown on figure 41. Then, after a simulation test it gave nearly the same signal that was meaning that this IC couldn't be used as a PSD in our case.

Figure 41 - AD834 phase detector output-pink, yellow-X input, Blue-Y input 90 degrees shifter

In addition, that setup had problems around passive components and biasing procedure as it was mentioned before, then it should have a proper instrumental amplifier and then it needs to compensate the DC part of the signal, that caused by a very small disbalance of the resistors and internal structure of AD834.

Moreover, AD834 wasn't giving an output connected to the phase difference, just a bad sine wave at the output without any changes, while the phase difference was changed.

But at the same time AD633 has no mentions in Datasheet (Ref.3) about Phase Detection using AD633, we assembled and tested on a breadboard a small testing circuit for it, and it has shown a result shown on Figure 42

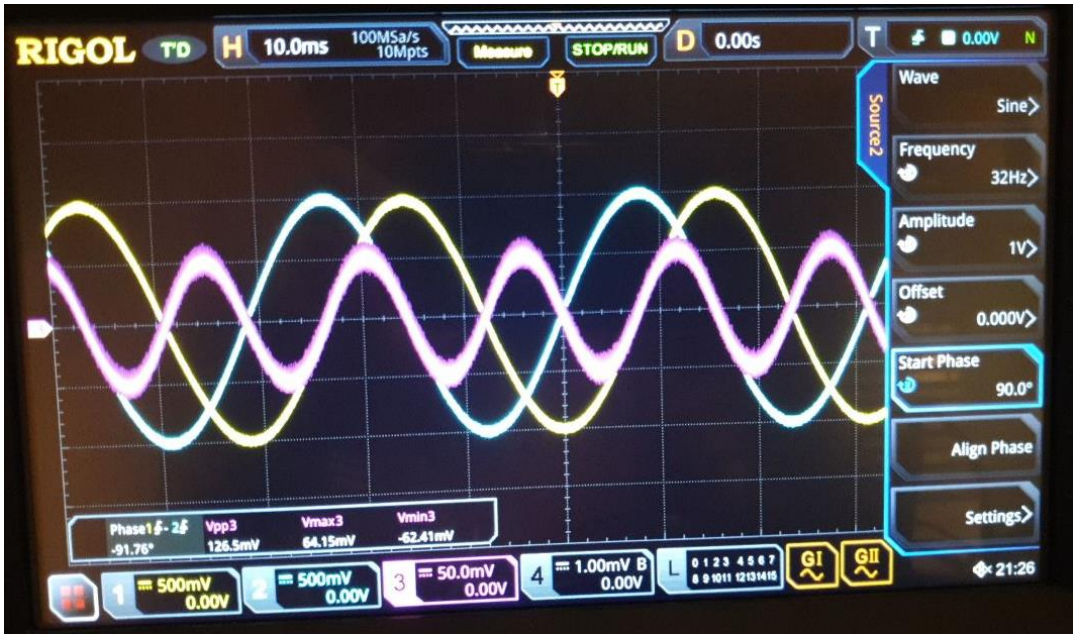


Figure 42 - AD633 output: Yellow X input, Blue Y input, Pink-Output(w)

As it seen on figure the DC part of the signal changes according to phase difference of the signal. Prototyping was done on the same manner as demonstrated on Figure 19. That approach was used as a fast prototype because another PCB order would take a lot of time or assembly on through-hole prototyping PCB would take almost the same amount of time. Moreover, we were limited on components and those components are used in modules: unsoldering can be too risky. Surface mount parts were connected through adapter PCBs: SOIC-8 to DIP-compatible pitch packages. It was estimated that phase gain is approximately equivalent to 45 mV/rad.

Measurements were done manually by changing the phase difference at the 2nd channel of signal generator with the same amplitude of both input signals of the PSD. PSD has a DC offset at the output of around 48.9mV at 0 degrees difference between signals and then voltage moves down to -109mV.

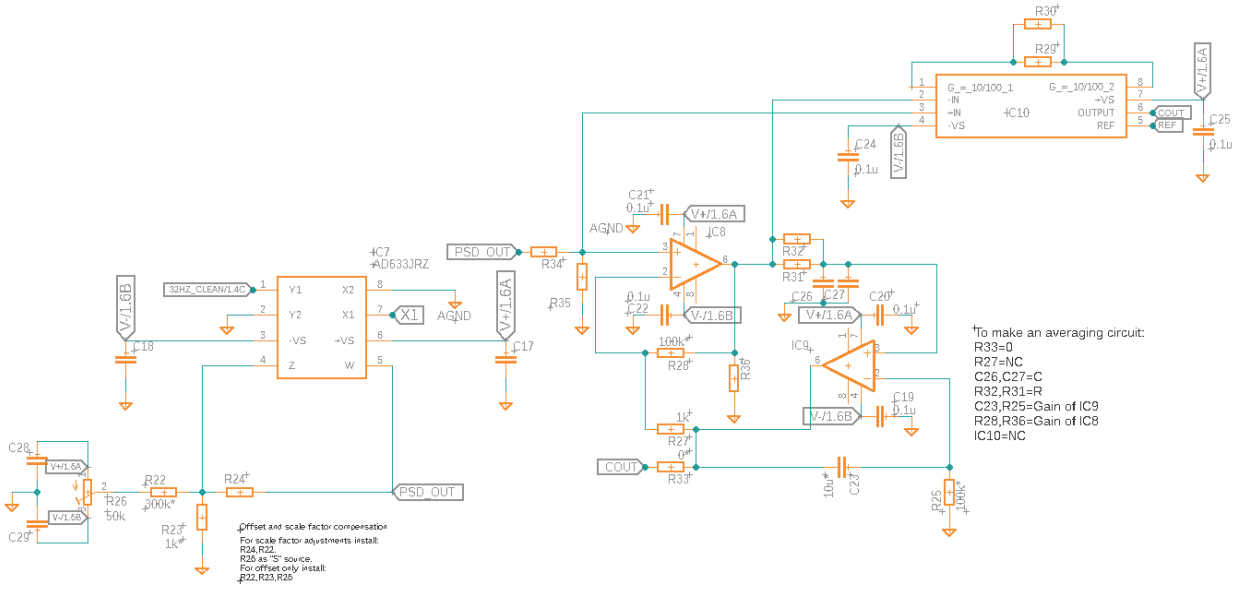


Figure 43 - Phase Sensitive Detector and Compensator

The circuit shown on figure 43, R22, R23, R24, R26 are used for the manual DC offset compensation, then that processed by averaging circuit because average of sine wave is zero or DC offset. But it is configurable to make a previous DC compensation circuit that was shown on Figure 11, but we can use instead an Instrumentational amplifier to subtract AC part of the signal.

The DC offset at zero is not important because that offset would be compensated by VCO and then change the phase difference. The compensation of AC waveform is not important because loop frequency turning of the system would be below 1 Hz. Any spectral component higher than loop frequency turning would have no effect to the 2nd input of phase comparator. A simple first order low pass RC filter should be enough for that.

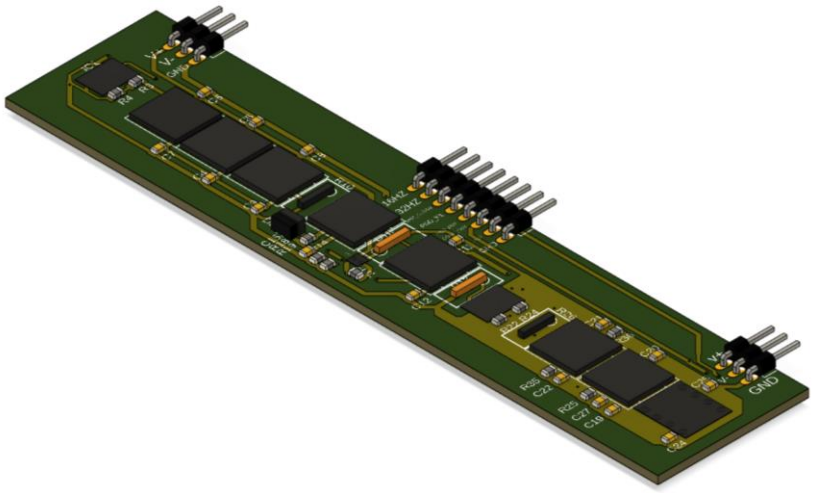


Figure 44 - PSD board

The PCB, that is demonstrated on Figure 44 is designed at the same manner as Frequency Multiplier Module, but it is not dense as frequency multiplier PCB and could be reduced after final justification of set of adjustments probably by half of the size or unite with multiplier PCB, but that may require to use a 4-layer board instead.

Connectors that are used at the edge of the board are used for power supply and mechanical stability to prevent board from swinging. The central connector is used for signals going in and out:16Hz X input, 32Hz multiplied, 32Hz recovered signal then connected to X input of a Phase detector IC, 32Hz Y input connected directly to Phase Detector IC, W pin of AD633 or Phase Comparator Output, Compensated Phase Comparator Output. All connections names are written on the PCB.

3.3 Motherboard

The Motherboard is used as carrier board that should do all interconnections as what was mentioned before.

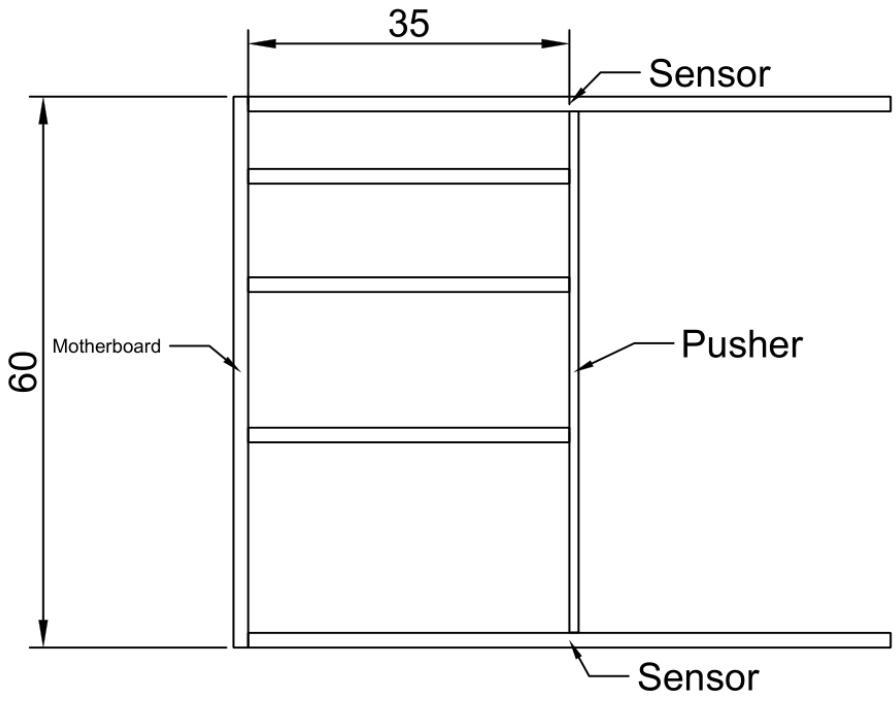


Figure 45- Configuration of assebled electronics

The entire electronic assembly should fit to the dimensuons shown on Figure 45, the pusher coil is under the bob, sensors are placed at both sides and motherboard is under the pusher. The entire assmbly could be reconfigured, if manual adjustments are needed: motherboard goes to the bottom base of pendulum, in the base of pendulum would be made a rectangular cut, where modules are placed, rear sides would have holes for adjustments that would be made by a screwdriver. Configuration that was shown on Figure 45 is more preferable.

4.Conclusions

In this thesis I describe the design of a new electronic system for the management of pendulum oscillators. The complete system includes two independent subsystems: one is an electronic oscillation loop that jump-starts the oscillations and keeps them going, and the other one is a user interface system that locks to the pendulum a quartz oscillator with a Phase Lock Loop which includes a synthesizer designed to introduce a frequency offset on the Quartz oscillator. That kind of systems could be used as measurement instruments, but at the same time easy to build, relatively cost-effective, doesn't need specific parts and give a lot of freedom in adjustments. As an example, those kinds of instruments could be used as gravimeters, inclinometers, altimeters, decoration and so on. Thesis was focused more on electronic design for a pendulum, because that could be used as an example for further designs, if there would be more interests in the area.

References

1. “A Novel zT Meter Based on the Porcupine Method and a Survey

on the Size of the Snout Correction Needed for Various

Thermoelectric Devices” ANDREA DE MARCHI VALTER GIARETTO, SIMONE CARON, ANDREA TONA

2.Datasheet AD834

3.Datasheet AD633

4. Circuits, Systems, and Signal Processing (2020) 39:4775–4791

5. Datasheet LT1167

6. “Galileo at Work: His Scientific Biography” Stillman Drake

7. https://web.archive.org/web/20120223142737/http://www.ecelab.com/wien-bridge.htm

8. Messung der Inductionsconstanten mit dem „optischen Telephon” Max Wien

9. Murata’s Catalog: “Chip Multilayer Ceramic Capacitors for General” C02E.pdf Jan. 18,2021

10. A study of injection locking and pulling in oscillators B.Razzavi

11. “A simple, unified phase noise model for injection-locked oscillators”

Sachin Kalia, Mohammad Elbadry, Bodhisatwa Sadhu, Satwik Patnaik, Joe Qiu, Ramesh Harjani

12. “An injection-locking scheme for precision quadrature generation” P. Kinget, R. Melville, D. Long, V. Gopinathan

13. “Injection-Lock a Wien-Bridge Oscillator” Glen Brisebois

14. https://www.pcbway.com/capabilities.html

15. Application note “Silicon PICS capacitors as replacement of MLCC and Tantalum capacitors” Rev1.1, Murata, AN431111614959

16.https://www.rmg.co.uk/stories/blog/second-one-hundred-days-results

17. “Designing Circuit Boards With EAGLE: Make High-Quality PCBs at Low Cost 1st Edition” Matthew Scarpino