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Coupling control in Si-MOS quantum dots

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Grenoble, August 2021
Victor Millory

Abstract

English

The demanding requirements of a practicable qubit implementation, summarized by the DiVicenzo criteria [4], illustrate the difficulty of qubit development. Amid the competing architectures, the recent Si-MOS spin qubit implementation [13] promises high integration by taking advantage of years of process development. Nevertheless, the higher integration sees the loss of coupling control between neighboring dots, which is yet needed to ensure that the qubits operate in an optimal regime and enable accurate readout [9, 7]. This document reports the fabrication of exchanges gates enabling to control this coupling. Although no fully functional device has yet been produced, the process flow experimented here was found to be promising, since none of the fabrication challenges were proven to be intractable.

Français

L'exigence des critères de DiVicenzo [4], établissant le cahier des charges d'un qubit viable, illustre le challenge que représente le développement d'une architecture de calcul quantique viable. Parmi les différentes architectures en concurrence, la récente implémentation en Si-MOS [13] promet une haute capacité d'intégration en tirant parti des procédés développés pour la microélectronique. La transition récente observée, des architectures expérimentales GaAs vers celles CMOS ne se fait pourtant pas sans pertes. La meilleur intégration se fait au détriment du contrôle du couplage entre les boites quantiques adjacente, et les réservoirs. Celle-ci s'avère pourtant requise pour permettre aux boites quantique de fonctionner dans un régime optimal et pour garantir une lecture des états fiable [9, 7]. Ce rapport présente un procédé de fabrication en post-process de grilles d'échanges permettant le contrôle de ce couplage. Bien que des dispositifs completement fonctionnels restent encore à produire, le procédé s'est avéré prometteur, la plupart des défis de fabrication ayant été surmontés.

Italiano

Le crescenti richieste di una fattibile implementazione del qubit, dettata dai criteri di DiVincenzo [4], dimostra la difficoltà dello sviluppo del qubit. Tra le differenti architetture possibili, la recente implementazione in CMOS [13] promette un alta capacità d'integrazione grazie alla conoscenza acquisita nel campo della microelettronica. Tuttavia, la transizione dalla tecnologia GaAs a quella CMOS non avviene senza un costo. Una migliore integrazione vede la perdita del controllo di accoppiamento tra le scatole quantiche adiacenti, necessario ad assicurare un funzionamento ad un regime ottimale e assicurare una accurata lettura degli stati presenti [9, 7]. Il documento presenta un processo di fabbricazione delle porte di scambio che permettono il controllo dell'accoppiamento. Anche se nessun dispositivo completamente funzionale è stato ancora prodotto, il processo di fabbricazione sperimentato si è rivelato promettente, poiché la gran parte delle ostacoli legati alla manifattura sono stati superati.

Keywords: silicon quantum dots, spin qubits, post-process fabrication, coupling control

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Acronyms

Acronym	Meaning
BOX	Buried OXide
CEA	Commissariat à l'Energie Atomique et aux énergies alternatives
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
DAC	Digital to Analog Converter
DMM	Digital MultiMeter
DQD	Double Quantum Dot
DUV	Deep Ultra Violet
EBL	Electron Beam Lithography
EDSR	Electrical Dipole Spin Resonance
FDMOSFET	Fully Depleted Metal Oxide Semiconductor Field Effect Transistor
FDSOI	Fully Depleted Silicon On Insulator
GUI	Graphical User Interface
ICP	Inductively Coupled Plasma
IPA	IsoPropanol Alcohol
IRIG	Institut de Recherche Interdisciplinaire de Grenoble
LATEQS	LAboratoire de Transport Électronique Quantique et Supraconductivité
Leti	Laboratoire d'Electronique et de Technologie de l'Information
PHELIQS	laboratoire de PHotonique ELectronique et Ingénierie QuantiqueS
MIBK	Methyl Isobutyl Ketone
PSB	Pauli Spin Blockade
PTA	Plateforme Technologique Amont
PVD	Physical Vapor Deposition
QD	Quantum Dot
RF	Radio Frequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
Si-MOS	Silicon Metal Oxide Semiconductor

1 Context of this internship

This internship took place in the Commissariat à l'Energie Atomique et aux énergies alternatives (CEA) of Grenoble, in the laboratory Photonique Electronique et Ingénierie Quantiques (PHELIQS), part of the Institut de Recherche Interdisciplinaire de Grenoble (IRIG). CEA is a French public government funded research organisation, aiming to be a bridge between the academic world and the industry. Its Grenoble center was founded in 1956 as the Centre d'Etudes Nucléaires de Grenoble (CENG) and rapidly diversified its research activities. The CEA Grenoble is now a major European research hub, recognized for its expertise in applied research for microelectronics and nanotechnologies [1]. The center is a cornerstone of the industrial and academic ecosystem of Grenoble, part of the GIANT campus (Grenoble Innovation for Advanced New Technologies), and the MINATEC (Micro and Nanotechnology Innovation Centre) innovation hub.

The PHELIQS laboratory is specialized in nanophysics and condensed matter physics with applications to quantum information processing [3]. Within PHELIQS, the LATEQS research group (LAboratoire de Transport Électronique Quantique et Supraconductivité) is focused on the study of semiconductor and semiconductor/superconductor devices at cryogenic temperature [2]. PHELIQS works in close collaboration with the CEA Leti (Laboratoire d'Electronique et de Technologie de l'Information), that provides the custom industrial grade Silicon MOS (Si-MOS) devices experimented as qubit plateform by the LATEQS team. Part of the devices provided are not fully finished in order allow the post-process fabrication of additional features (at the Plateform Technologique Amont, PTA cleanroom), which is the goal of this internship.

2 Introduction

Quantum representation of information enable the use of quantum algorithms that offer a complexity gain (number of computational step), for some specific yet critical computational problems. This information must be encoded on a two level quantum system that forms a qubit. The physical implementations chosen for this basic unit is crucial, since large numbers of qubits are necessary to fully take advantage of quantum algorithms. Spin qubits, that use the spin of electrons confined in quantum dots as information support, appears as a promising platform [11]. Such quantum dots can be fabricated using Si-MOS technology that ensure high scalability and well characterized devices, which is paramount for a qubit architecture (first DiVincenzo criteria [4]).

Coupling control between neighboring quantum dots and reservoirs revealed to be critical. First, the tunneling rate need to be tuned in order to operate the quantum dots in a suitable regime (weak coupling) [9]. Secondly, reflectometry, one of the main readout technique, rely on capacitance measurement that are directly related to the coupling between neighboring dots and reservoirs[7]. Coupling control can be achieved with dedicated "exchange" gates that need to be interleaved in between the gates used to define quantum dots. Such gates were common place in GaAs spin qubit implementation that is the historical experimental spin qubit platform [9]. The recent shift toward Silicon and Si-MOS implementation [13], motivated by scalability, has see the loss of those exchange gates due to fabrication challenges (geometry, alignment, resolution), making this an active research field [6].

This Master thesis reports the progress of a post-process flow aiming to fabricate exchange gates on industrial-grade Silicon Si-MOS devices provided by the CEA Leti. The first section introduces the basic principles of quantum dot spin qubits and the role of tunnel coupling. The second section presents the devices provided by the CEA Leti and the process flow put to the test. The third part details the early designs and process tests. At last, the final devices and their characterization are presented.

3 Theory

Some basics concepts of quantum dots for spin qubits application are explored in this section. It should be noted that although the device used in PHELIQS are based on holes, most of the concepts introduced here are explained using electron since most of the literature of the field concern electrons. Those concepts can, at the first order, easily be transposed to holes.

3.1 Introduction to qubits

Bit and quantum bits (qubits) are both used to store information by taking a state. A classical bit can take one of two possible states, traditionally called 0 and 1 while a qubit can take a superposition of two orthogonal quantum states, usually called $|0\rangle$ and $|1\rangle$. The qubit state is then equals to :

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle \tag{1}$$

Where α and β are complex coefficients, that satisfy $|\alpha|^2 + |\beta|^2 = 1$.

The physical implementation of a qubit needs therefore to be a two level system that can be initialized, manipulated and then measured, while remaining coherent long enough to perform the operations needed. Those conditions are the first step toward the completion of the DiVincenzo criterias [4].

Solid state spin qubit are one of the possible architecture envisioned to build a quantum computer. Its potential scalability, inherited from microelectronics and the possibility of building a universal set of quantum gate make it a promising candidate as a quantum computing platform.

As the name imply, spin qubits rely on the spin (up or down) of electrons or holes to create a two level system. Those spin carriers are here trapped into quantum dots based on Si-MOS transistors. Two suitable spin states can then be used to create a qubit.

As for most of the solid state qubit architectures, one of the main challenge to overcome is the coherence time of the system, that must be long enough to allow all the operations (initialization, manipulation and readout) required. Silicon offers several advantages compared to other solid state spin qubit plateforme such as AlGaAs-GaAs devices. For instance, its is possible to work with holes instead of electrons. Spin manipulation of holes can be accomplished via Electrical Dipole Spin Resonance (EDSR) thanks to the spin orbit coupling. Without EDSR, spin manipulation should be performed with electron spin resonance using magnetic fields (via radio frequency wire or micro magnets) that dramatically complicates the integration.

3.2 Quantum dot implementation

The devices employed here to form quantum dot are p type Fully Depleted Metal Oxide Semiconductor Field Effect Transistors (FDMOSFET) of small dimensions, produced by the CEA Leti. The channel is $60nm$ to $40nm$ long and is made of n doped Silicon. When $Vg = 0$, the transistor is blocked, but for $|V_G| > |Vth|$, a 2D electron/hole gas is formed in the active channel, allowing the carrier to flow through. The current direction is determined by V_{DS} since the structure is symmetrical. This structure is used here to confine holes using the gate to create a potential well, and obtain a quantum dot. A schematics of a FDMOSFET is provided in figure 1 with its I_D-V_{GS} characteristics and a representation of the potential felt by holes. Several gates can be placed in series along the channel in order to obtain chains of quantum dot that can interact. The main advantage of such a structure is its ease of fabrication since compatible with standard Silicon Si-MOS technology. Yet, such device suffers of one issue: its lack of control over the coupling between dots, which would require additional

dedicated gates. This is the subject investigated in this document.

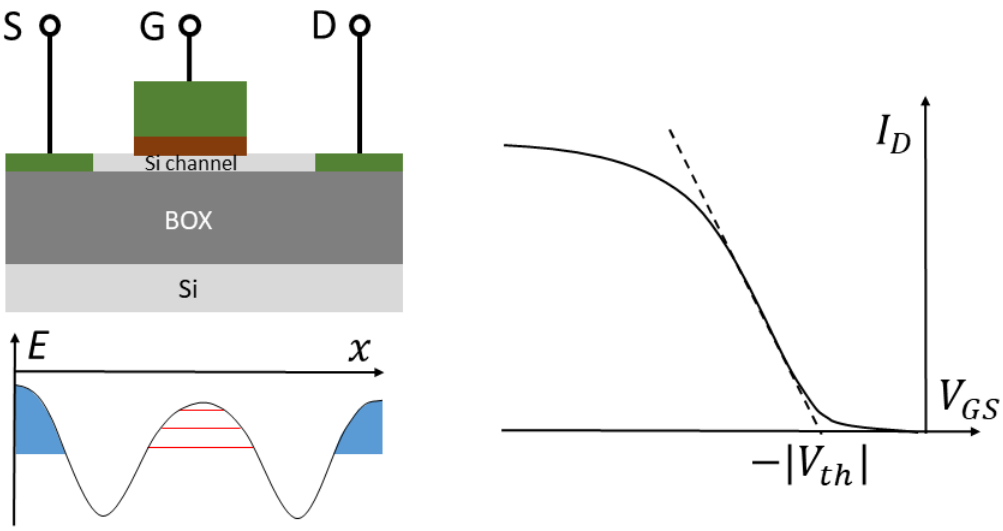
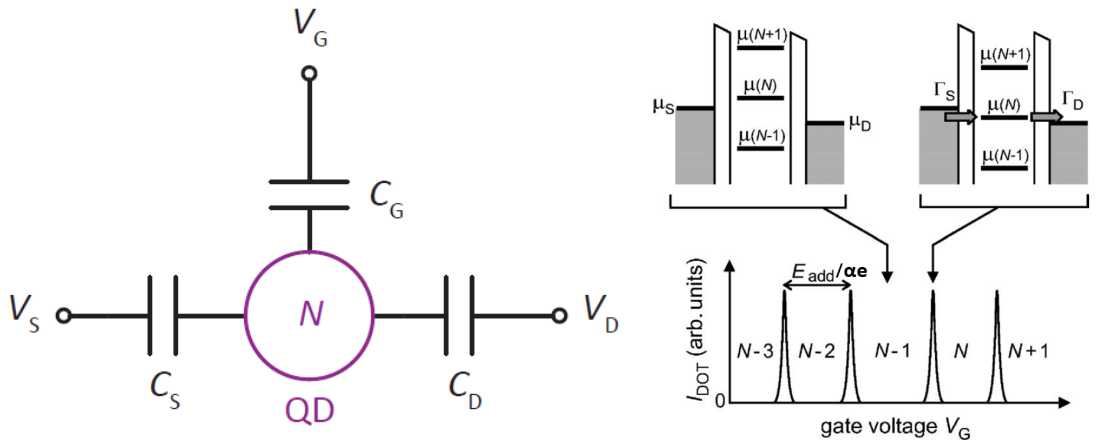


Figure 1: Left panel: Fully Depleted MOSFET employed to create a quantum dot, right panel: I_D-V_{GS} characteristics

3.3 Single quantum dots



(a) (b)

Figure 2: Single quantum dot, **a)** Capacitance model used for the quantum dot, adapted from [7] **b)** Coulomb peak observed at low temperature ($E_{add} > k_B T$) when one of the electrochemical potential is present in the bias window, adapted from [9]

A simple model of single quantum dot, known as the constant interaction model, is presented here. In this section, we consider in a first time spinless electrons trapped in a quantum dot, connected to

reservoirs (source and drain) through tunnel barriers, materialized by capacitances C_S, C_D. A third terminal, the gate, is employed to act on the dot potential through a capacitance C_G. A schematic of such a system is provided in figure 2a.

We then consider the energy of the N excess electrons trapped in the quantum dot. By taking into account the electrostatic contribution and the single particle energy level that electrons can occupy, one finds [9]:

$$U(N) = \frac{1}{2C}\left(-eN + C_S V_S + C_D V_D + C_G V_G\right)^2 + \sum_{n=1}^{N} E_n \tag{2}$$

Where N is the number of excess electron trapped in the dot, and $C = C_S + C_D + C_G$. The last term of the equation is the contribution of all the single particle energy level E_n occupied.

The electrochemical potential of the quantum dot for a given number of electron trapped $\mu(N)$, represent the energy needed to add a N^{th} electron to the dot already containing $N-1$ electrons. When considering only the ground states of $U(N)$ (all the quantum dot energy level filled up to the dot chemical potential), it can be shown [9] that:

$$\mu(N) = U(N) + U(N-1) = \left(N - \frac{1}{2}\right)E_c - \frac{E_c}{e}\left(C_S V_S + C_D V_D + C_G V_G\right) + E_N \tag{3}$$

Where $E_c = e^2/C$ is called the charging energy. This equation could also be written in terms of leverarm $\alpha_i = C_i/C$, that represents the ability of a gate i to act on the dot potential, therefore on its electrochemical potential.

This electrochemical potential "ladder", represented in the top pannel of figure 2b, can be moved up or down energywise by the different voltages. Because the voltages contribution to $\mu(N)$ are weighed by the capacitances ratios (leverarm) and that $C_g >> C_{S,D}$, V_g is the main voltage controlling $\mu(N)$. Consecutive electrochemical potential levels are separated by $E_{add} = E_c + \Delta E_{QD}$, where ΔE_{QD} is the energy spacing between two discrete single particle quantum levels stemming from the confinement (ΔE_{QD} can be null for instance in the case of degenerated single particle energy levels, and is in most of the case negligible with respect to E_c). This E_{add} represents the extra energy cost to add an extra electron to the dot, and is mainly caused by electrostatic interaction of the electrons.

When an electrochemical potential level is lower than the Fermi sea level of one of the reservoir (D or S), electrons can tunnel through the energy barrier to fill it, in a time inversely proportional to the tunneling rate between the dot and the reservoir. When a bias V_{SD} is imposed, electrons can flow through the dot using the electrochemical potential level aligned within the bias window. The simultaneous number of electron that can tunnel is given by the number of level aligned. At low bias ($V_{SD} < E_{add}/e$) electron can only flow one by one at the time, creating a Single Electron Transistor (SET). When no level is aligned within the bias window, no electron can flow through the device, this phenomenon is called Coulomb Blockade. Peaks of current are thus observed when sweeping V_G, as shown in figure 2b. All of this is valid only at low temperature $k_b T << E_{add}$, in order to prevent electrons from jumping between the levels.

A systematic study of the electrochemical potential level alignment with the reservoir potentials leads to the figure 3. The black lines represents the voltage values causing the potentials to align, and thus delimiting regions were the electron flow is blocked. The central orange regions are called Coulomb Diamonds and represents the V_{DS} and V_G values achieving Coulomb blockade and effectively trapping a given number of electrons. The other regions allow a discretized electron flow.

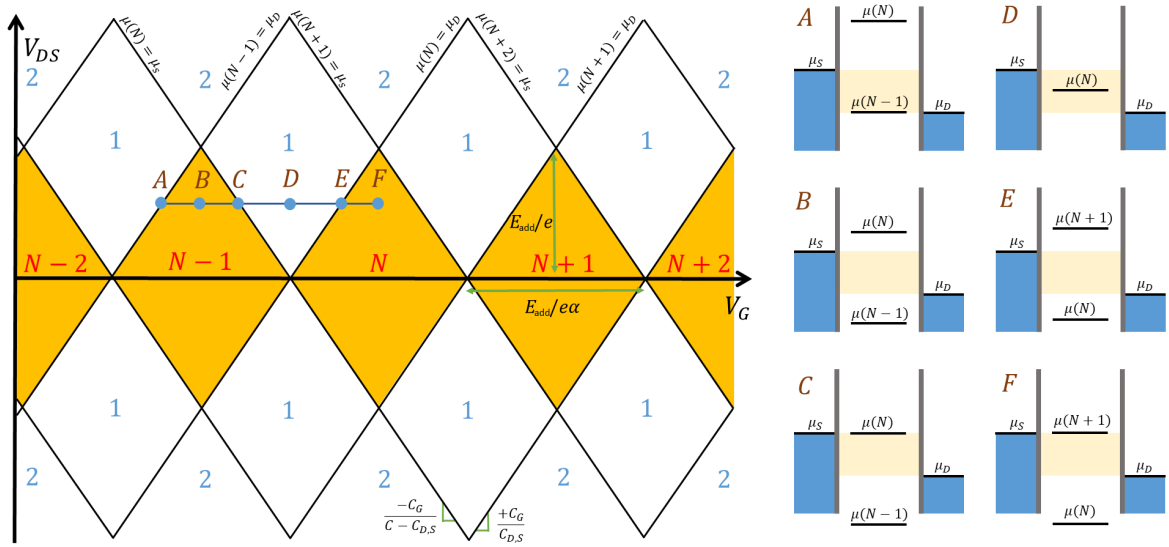


Figure 3: Coulomb diamonds, the number of electron allowed in the QD depends of the region. The black lines correspond to the values V_G and V_{DS} where the one level of the electrochemical potential ladder align with μ_S and μ_D. In the orange regions (the diamonds) electrons cannot flow, the red numbers indicates the number of electron allowed in the dot. The blue numbers indicates how many electrons can flow through the dot. The right panel shows the electrochemical potentials alignment evolution along the blue line. The bias windows is represented in yellow.

We have so far considered spinless electrons. Taking those into account allow to introduce new effects such as the Pauli Spin Blockade (PSB). This effect is the consequence of the Pauli exclusion principle that forbids electrons to have the same quantum number, therefore preventing electrons of same spin from existing in the same orbital. The introduction of spin selection rules on the possible transitions and thus on the $\mu(N)$ available to an electron, leads to spin blockade phenomenon. Electrons with a given spin cannot enter in the dot due to the presence of an electron with the same orientation. PSB can therefore be used to probe the spin state of a QD, as developed in the next sections.

The next logical step after single quantum dots is the case of double quantum dots (DQD), that enables to explore the effect of coupling between the dots.

3.4 Double quantum dots

3.4.1 Charge stability diagrams

We consider spinless electrons, trapped in a double quantum dot (DQD), represented the capacitance model provided in figure 4a. This DQD is made of 2 quantum dots in series, coupled via a C_m capacitance, and connected to reservoirs through C_S and C_D. The energy analysis applied to the single quantum dot can also be applied to DQD. The electrochemical potential $\mu_1(N_1, N_2)$, corresponding to the energy needed to add a $N_1^t h$ electron to the dot 1 while having respectively $N_1 - 1$ and N_2 electrons in the dot 1 and 2, can be expressed [18] as:

$$\mu_1(N_1, N_2) = U(N_1, N_2) - U(N_1 - 1, N_2) = \left(N_1 - \frac{1}{2}\right) E_{c1} + N_2 E_{cm} - \frac{1}{e}(C_{G1} V_{G1} E_{c1} + C_{G2} V_{G2} E_{cm}) \tag{4}$$

and for $\mu_2(N_1, N_2)$:

$$\mu_1(N_1, N_2) = U(N_1, N_2) - U(N_1, N_2 - 1) = \left(N_2 - \frac{1}{2}\right) E_{c2} + N_1 E_{cm} - \frac{1}{e}(C_{G2} V_{G2} E_{c2} + C_{G1} V_{G1} E_{cm}) \tag{5}$$

with the charging energies:

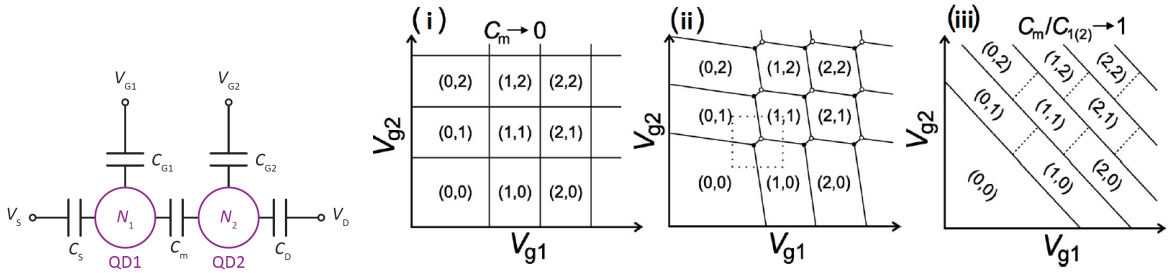
$$E_{c1(2)} = \frac{e^2}{C_{1(2)}} \frac{1}{1 - \frac{C_m^2}{C_1 C_2}} \tag{6}$$

$$E_{cm} = \frac{e^2}{C_m} \frac{1}{\frac{C_1 C_2}{C_m^2} - 1} \tag{7}$$

Where $C_1(2) = C_{S(D)} + C_{G1(2)} + C_m$.

As before, we obtain an electrochemical potential ladder, but in this case one dot influences the other. As before, the thermal energy needs to be smaller than the charging energies $Ec1$, $Ec2$ and Ecm to prevent electron from jumping between states. When the two electrochemical potentials are aligned, electrons can tunnel from one dot to the other.

A study at $V_{SD} = 0$ of the electrochemical potential alignment depending on the gate voltages yields the charge stability diagram (giving the number of charges allowed in each dot for a given set of Vg). For decoupled dots ($C_m = 0$): the gate voltages act only their own dot (orthogonal lines). In case of coupled dots ($C_m > 0$), the diagram becomes hexagonal, giving the so called "honeycomb" lattice where each crossing points are split into two triple points. At those triple points the electrochemical potential of the dots and reservoir are aligned and transport is possible. The two triple points are connected by the "interdot" line where $\mu_1(N_1, N_2) = \mu_2(N_1, N_2)$. Crossing this line means transferring an electron from one dot to the other. The triple point splitting is equals to E_{cm}/e. When the two dots are strongly coupled (large C_m), the dots behave as a single QD, the two gate voltages having the same impact on the dot potential [9].



(a) (b)

Figure 4: **a)** Double quantum dot capacitance model, adapted from [7] **b)** Charge stability diagrams giving the number of electrons in the dots depending on the voltages applied (with $V_{SD} = 0$), in absence of coupling (i), with coupling between the dots (ii), the area highlighted is an interdot transition, in between two triple points) forming a honeycomb pattern. In case of strong coupling, the double dot behave as a single dot as in (iii), and the two gates have the same effect. Adapted from [18]

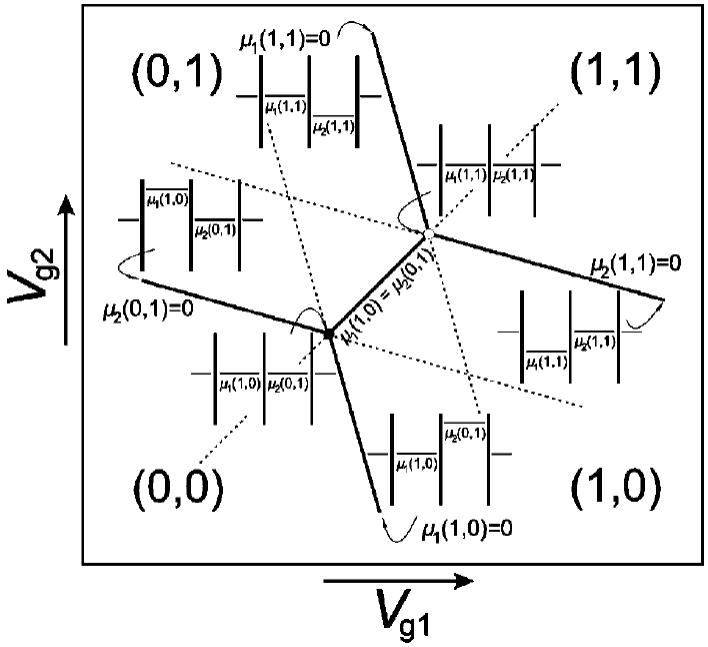


Figure 5: Charge stability diagram (with $V_{SD} = 0$), zoom on the "interdot" and the triple points. All the electrochemical potentials are aligned only at the triple points (black and white dots). Adapted from [18].

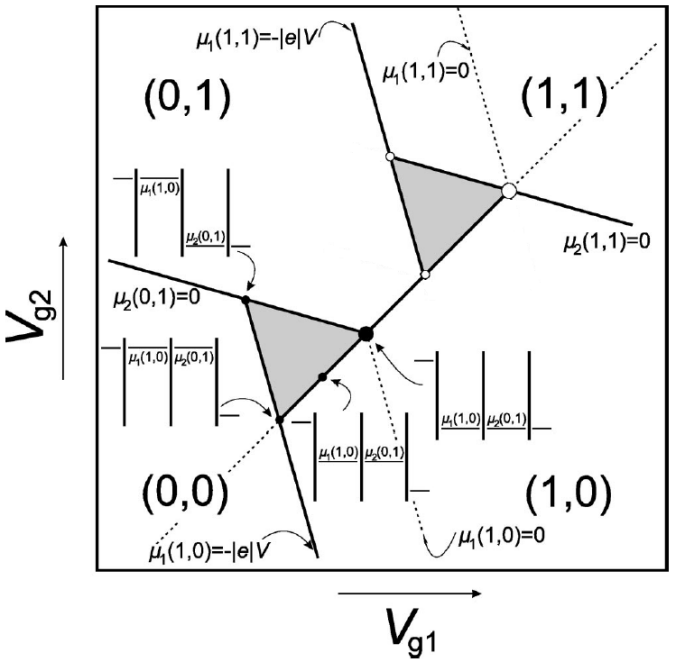


Figure 6: Charge stability diagram (with a negative bias V). The triple points turn into "bias triangle", whose lateral size depends on the bias. Adapted from [18]. The triple point separation is no effected, but the triangles can overlap if $|V| \geq E_{cm}/e$

What has been said so far is only valid for a low tunnel coupling (weak coupling regime) between the dots, if it's not the case, electrons are not fully localized in one of the QD due to their wave functions spanning over the two dots[9] (not discussed here).

When a bias V_{SD} is applied to the device, the gate voltage value allowing transport (due to electrochemical potential alignment) are less constrained with respect to the previous case. The triple points broaden into bias triangles. The triangle size is proportional to the bias, the two triangles can overlap if V_{SD} becomes comparable to E_{cm}/e.

3.4.2 Quantum capacitance

The motion of charges inside the dots causes capacitance variation that can yield information about QD and DQD states. One can express the charges trapped in a dot and obtain the differential capacitance [7]:

$$C_{dif} = \frac{dQ}{dV_{Gi}} = C_p + C_{geo} \tag{8}$$

With C_{geo} the geometric capacitance, a constant capacitance stemming from the reservoir capacitances and C_p, the parametric capacitance:

$$C_p = -e\alpha \frac{\partial \langle N \rangle}{\partial V_G} \tag{9}$$

This capacitance is related to the variation of the average number of charges present in a quantum dot. It is thus possible to apply a small gate voltage variation, causing electrons to move if they can, and observe a capacitance variation giving information on the available transitions.

To express this C in other parameters, we consider the simplest case possible with a single electron trapped in a DQD, forming a charge qubit based on the charge configuration (0,1) and (1,0). The bias is null, and we consider that the electron cannot tunnel to the reservoirs. A detuning (ie. an energy difference between the dots, induced with the two gates) is applied to the DQD, creating a two level system that can be used as a qubit. The two QD are kept apart by an energy barrier (as shown in the figure 7a), that can be tunneled through at a rate Δ_C. The Hamiltonian of such a system is [14]:

$$H = \frac{1}{2} \begin{pmatrix} \varepsilon & \hbar\Delta_c \\ \hbar\Delta_c & -\varepsilon \end{pmatrix} \tag{10}$$

Where ε is the detuning applied with the gates and Δ_c is tunneling rate (also called tunnel coupling) between the two dots. Its eigenvalues $E_\pm$ are given by:

$$E_\pm = \pm \frac{1}{2} \sqrt{\varepsilon^2 + (\hbar\Delta_c)^2} \tag{11}$$

This energy level spectrum is plotted in figure7b. In the non coupled case ($C_m = 0$), the eigenvalues are $E_1 = \varepsilon/2$ and $E_2 = -\varepsilon/2$. In the coupled case (showed here), the coupling causes the two eigenstates to anticross instead.

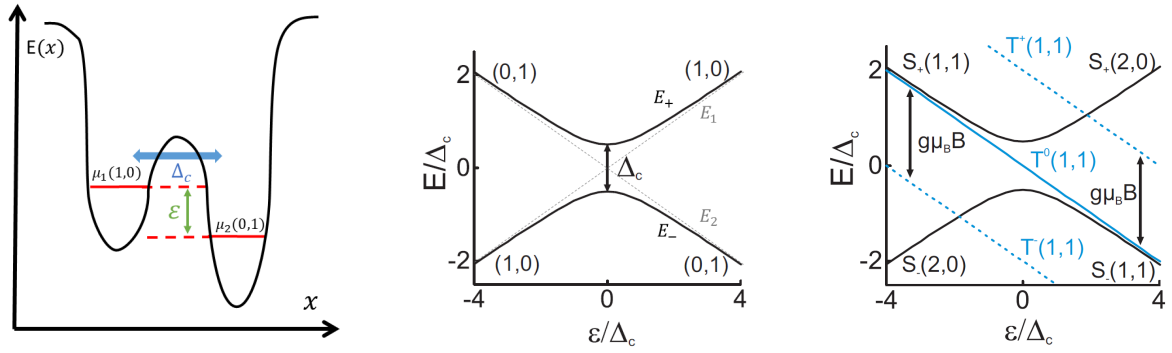


Figure 7: Potential applied to the DQD, and energy level spectrum for one and two electrons regimes **a)** Potential applied to the DQD, the detuning ε is the difference of voltage applied between the dots, Δ_c is tunnel coupling between the dots. **b)** Energy level spectrum for one electron regime. The dashed lines indicates E_1 and E_2: the energy spectrum for uncoupled dots. Adapted from [14] **c)** Energy level spectrum for two electron regime, with singlets and triplets states. The triplets are here non degenerated due to the presence of a magnetic field B, otherwise $T_0 = T_+ = T_-$. Adapted from [14]

When considering that we induce a variation on the DQD energy by applying a small oscillating voltage, and the occupation probability of the state, it can be showed [14] that:

$$C_p = C_{quantum} + C_{tunneling} = \frac{(\alpha e)^2}{2}\left(\frac{\Delta_c^2}{\Delta E(\varepsilon)^3}(P_+ - P_-) + \frac{\varepsilon}{\Delta E(\varepsilon)}\frac{\partial(P_+ - P_-)}{\partial\varepsilon}\right) \tag{12}$$

Where α is the gate lever arm, $\Delta E(\varepsilon) = E_+ - E_-$ is the energy gap between the two energy levels involved in the transition, which is in this case $\Delta E(\varepsilon) = \sqrt{\varepsilon^2 + \Delta_c^2}$, and P_+, P_- the occupation probability of the ground state $(-)$ or the exited state $(+)$.

C_p can be split into two terms; the quantum capacitance $C_{quantum}$, stemming from adiabatic transitions in systems presenting finite curvature of their energy bands [5], and the tunneling capacitance stemming from non adiabatic process (such as relaxation and thermal excitation) [8]. The contribution of $C_{tunneling}$ can be neglected at low temperature [14]. Equation 12 shows that C_p heavily depends on the barrier energy, in other terms on the coupling between the dots. In the one electron case exposed here, the energy band curvature is present at low detuning, while the curvature flattens at higher detuning. A capacitance variation, indicating an interdot charge transition (the electron tunnelling back and forth between the dots when the electrochemical potentials are aligned), can thus only be observed at low detuning.

The devices experimented in the team are not charge qubits as the one presented previously but spin qubits. Nevertheless the conclusion reached here regarding the impact of the coupling on the quantum capacitance, still applies [14]. At last, it should be noted that this case presented here only considered the interdot coupling, the capacitance variation obtained here are therefore only related to the interdot transition (the dots electrochemical potentials alignment). Capacitance variations could also, in some cases, originate from the coupling of the dots with the reservoirs, enabling to monitor dot-reservoirs charge transitions as well.

3.4.3 Spin states

In a two electron configurations, spin must be considered to explain the different states. Hence, electrons can form singlets (S) and triplets states (T_0, T_+, T_-, a magnetic field is necessary to lift the triplet degeneracy). An analysis similar to the one undertaken for the one electron case can be conducted and gives the energy spectrum in figure 7c. It can be demonstrated [14] that the quantum capacitance is identical to the one given in equation 12. It should be noted that in this case, the triplet states present no curvature, and thus cannot give rise to a capacitance variation.

As for single quantum dot, taken into account the electron spin gives rise to Pauli Spin Blockade (PSB). Because of the Pauli exclusion principles, electrons of same spin cannot exist in the same orbital (here the singlets of each dot), conditioning electron access to some electrochemical potential with spin selection rule. We consider the previous two electrons case, with one dot always occupied the DQD kept in configuration (0, 1), (1, 1) or (0,2), as in figure 8.This means for instance that the (0, 1) $\rightarrow$ (0, 2) transition cannot accept electrons having the same spin as the electron already present, to form a singlet state S(0,2) (ground state). This is true if the triplet transition (the exited orbital) are kept out of the bias window. PSB is not limited only to singlets-triplets states but can be observed in configuration with more states, and therefore be used to perform measurement of the DQD spin state. PSB can for instance be observed in transport, giving partial bias triangles as in figure 8 or with capacitance measurement since PSB can block the interdot transition discussed in the previous section.

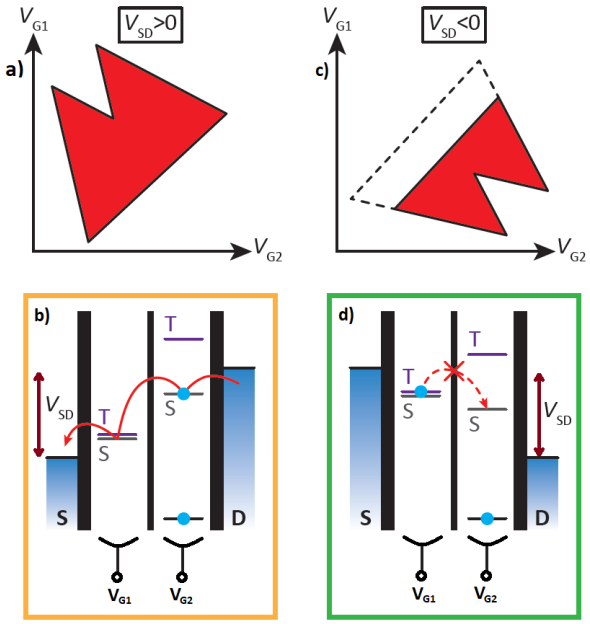


Figure 8: Effect of Pauli Spin Blockade on bias triangles. The red areas in a) and c) indicates current in the charge stability diagram, as in figure 6. In a) and b) the system is not spin blocked since a reservoir can provide any spin type, enabling the use of the singlet transition despite the presence of an electron in the right dot. In c) and d), the system is spin blocked by the presence of two identical spins, preventing the use of the singlet transition in the right dot in the case of identical spins. The DQD starts to conduct only when the triplet states enter the bias windows, cutting the basis of the triangles. Adapted from [7]

3.5 Spin qubits readout

Readout methods refer to the techniques allowing to probe the spin state of spin qubits. Spin cannot be directly measured but charge measurement can be performed on the device, either by transport or capacitance measurement (reflectometry). The idea is then to build a spin qubit made of quantum dots that enable to infer the spin state of the system from a charge state measurement (spin to charge conversion). Double quantum dots can be used to illustrate such readout methods.

We consider here a double quantum dot device, one dot is used to encode the information while the second dot allows to read the first one. Transport measurement can be performed to determine the spin state of a qubit by observing whether it is possible to transfer charges between the dots. In the case of identical spins, Pauli Spin Blockade can prevent such a transfer, blocking any current. In the case of opposite spins, transfer between the dot is possible and current can be observed. This technique suffers though from a major drawback: the need of averaging over many measurements (single shot readout not possible) [13].

On the other hand, reflectometry exploits the capacitance variations related to qubit state that was introduced in the previous section (in the context of gate reflectometry). The capacitance measurement is performed using a resonator (a circuit also known as tank circuit) connected to the device. A small capacitance change will cause the resonance frequency of the circuit to shift. By monitoring the phase variation around the resonance frequency, it is then possible to observe capacitance variations. Because those are related to the presence or absence (due for instance to PSB) of interdot transition, such measure can be used to determine the dot state and can be applied to the DQD spin qubit mentioned previously [7].

A big advantage of reflectometry is it short measurement time and accuracy with respect to DC measurement such as transport. This enables to get rid of $1/f$ noise and achieve single shot readout. The price to pay is that only some transitions are visible with such a technique depending on the dot coupling with other dots and reservoirs, and on the energy band curvature of the states involved.

3.6 Coupling control

The previous sections highlight the importance played by the coupling between dots, quantified by Δ_C and C_m. As shown before, coupling control is needed in several cases. First, the tunnel coupling must be kept low enough to ensure that the electrons are localized in one of the dots (weak coupling regime). Additionally, reflectometry (the main readout technique allowing to obtain information on the spin state of the qubits), relies on the quantum capacitance which depends itself on the coupling. Controlling this quantum capacitance is therefore highly valuable to achieve accurate readout and control of the qubit state.

The most obvious solution to achieve coupling control between dots is to use dedicated "exchange gates", interleaved in between the gates used to define the QD. The effect of those added exchange gates can be evidenced with capacitance variation (requiring reflectometry measures) and bias triangles spacing evolution (measured in transport). The fabrication of such gates is the purpose of this internship.

The next section introduces in details the concepts and tools employed to fabricate exchange gates on industrial-grade devices provided by the CEA Leti.

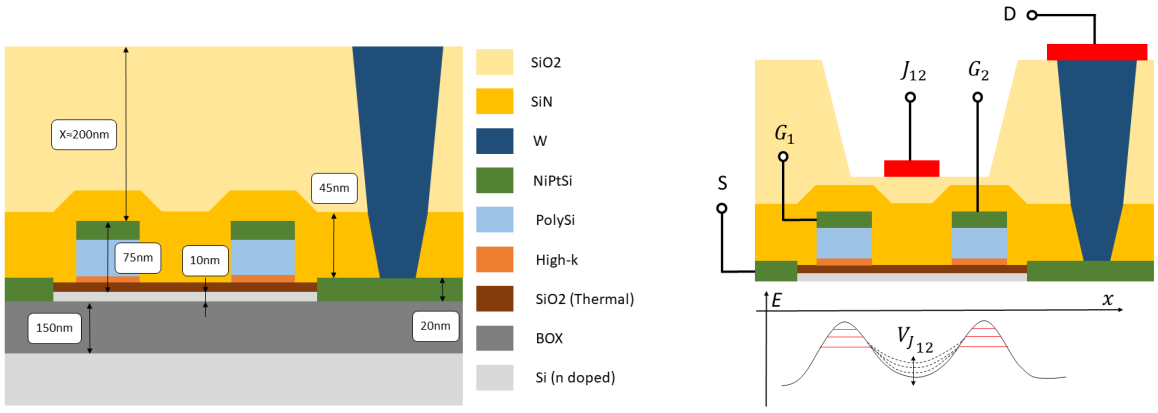
4 Initial devices, equipment and process flow overview

This section describes the devices provided by the CEA Leti, the process flow used, and a brief description of the machines employed at the PTA cleanroom to fabricate exchange gates in post-process on those samples.

4.1 Leti samples

The goal of this internship is to develop a post-process work flow, for industrial-grade Si-MOS devices produced by the CEA Leti, aiming to fabricate the exchange gates mentioned in the previous section.

The "Qbit reticle" mask set is dedicated to the production of devices required by different laboratories and projects working on quantum thematic, all compatible with the Si-MOS production line of the Leti. On this mask set, PHELIQS teams asked for N type nanowire fully depleted metal oxide semiconductor field effect transistors (FDMOSFET) with one to eight gates in series. Those gates are used to generate a chain of quantum dots (used to create hole spin qubits) in the silicon channel by applying a voltage. PHELIQS was provided with wafers that underwent the whole fabrication process, but also wafers stopped at the chemical-mechanical polishing (CMP) level just before the first metal layer. It is on this type of wafer that the post-process tests are conducted. Those wafer are provided with alignment crosses patterned with photoresist but not yet fabricated.



(a) (b)

Figure 9: Schematic cross section of the devices provided by the Leti and the expected cross section of the device after the post-processing steps **a)** Stack composition of the devices provided by the Leti stopped at the CMP level. The exact depth of the device is unknown but is expected to be of the order of $200nm$. Only one of the two vias is shown **b)** Stack composition after the post process steps, with terminals (wiring and vias not shown) and the expected effect of the exchange gates (J_{12}) on the electrostatic landscape felt by holes. The Aluminium layer added during the post-process steps is in red

The substrate is composed of heavily N doped FDSOI wafer, with a $10nm$ silicon layer and a $150nm$ BOX. A schematic of the stack is given in figure 9a. The devices are protected by a thick passivation layer of SiO_2. The exact thickness of this layer is unknown due to the CMP process, but is expected to be approximately 200nm thick. Because some plunging gates are as small as $40nm$, gate patterning requires an additional electron beam lithography (EBL) step in addition to the Deep UV lithographic process used for larger features. EBL being a direct writing method and therefore time consuming, only a handful of dies the wafer undergo the full plunging gate patterning process. Such dies are

labeled as "e-beam" and are the only ones electrically functional. Dies with incomplete plunging gates patterning (the plunging gates of those dies are merged in one block) are labeled as "DUV" and are reserved for process test (or for test with single plunging gates devices that).

4.2 Fabrication objectives and process flow overview

The objective of the process is to interleave exchanges gates (denoted as J_{xy}) in between the existing plunging gates G_x and G_y. Those exchange gates can be used to control the coupling between the quantum dots (localized in the silicon channel) realized by the plunging gates. In order to be effective, those additional gates need to be placed close to the active channel to ensure a good control of the coupling. To this end, it is necessary to etch away part of the SiO_2 before deposing the metal layer of the exchange gates as close as possible to the devices. The final expected stack is provided in figure 9b.

The idea of the process flow is to evaporate the alignment crosses already patterned, to etch areas on top of the devices, and then to pattern the exchange gates. A schematic of the process flow is provided in figure 10. The process flow is the following (the exact recipes are given in appendix):

1. Deposition of Platinum to form the crosses (already patterned by Leti with 1um of TARF-P9000 LA resist, part of the process done by Cécile Yu)
2. Lift-off of the crosses patterned (etyl lactate, ultrasounds and heating at 40°C) followed by a cleaning step
3. Patterning of the areas to be etched above the devices ($300nm$ to $500nm$ features), with Electron Beam Lithography (ZEP, $360nm$ thick, pure, done by Jean-Luc Thomassin and/or Romain Maurand)
4. Dry etching (RIE) the patterned area
5. ZEP stripping and cleaning
6. Patterning of the exchange gates, wiring and contacts pads with Electron Beam Lithography (PMMA, $90nm$ thick, done by Jean-Luc Thomassin and/or Romain Maurand)
7. Evaporation of a $40nm$ thick Aluminium layer
8. Lift-off of the pattern using acetone with ultrasound and heating (40°C), final cleaning with a bath of IPA

Several challenges have to be taken up in order to obtain a working device. First, the misalignment must not be larger than $15nm$ to interleave the exchange gates correctly. A good control on the exchange gate width is also required since some are very close to each other ($40nm$ close in the case of multiple exchange gates devices). A trade-off regarding the slope of the pit formed by etching the SiO^2 layer is needed. The exchanges gates must be continuous even across the pit sides. This implies that the pit sides cannot be fully vertical (or having sharp edges), to ensure that the metallic exchange gates deposited remains continuous. At the same time, the pit needs to fit in between the wiring of the device, meaning pit sides as vertical as possible. At last, the equipment availability must be taken into account, namely only one electron beam lithography per week in average can be done.

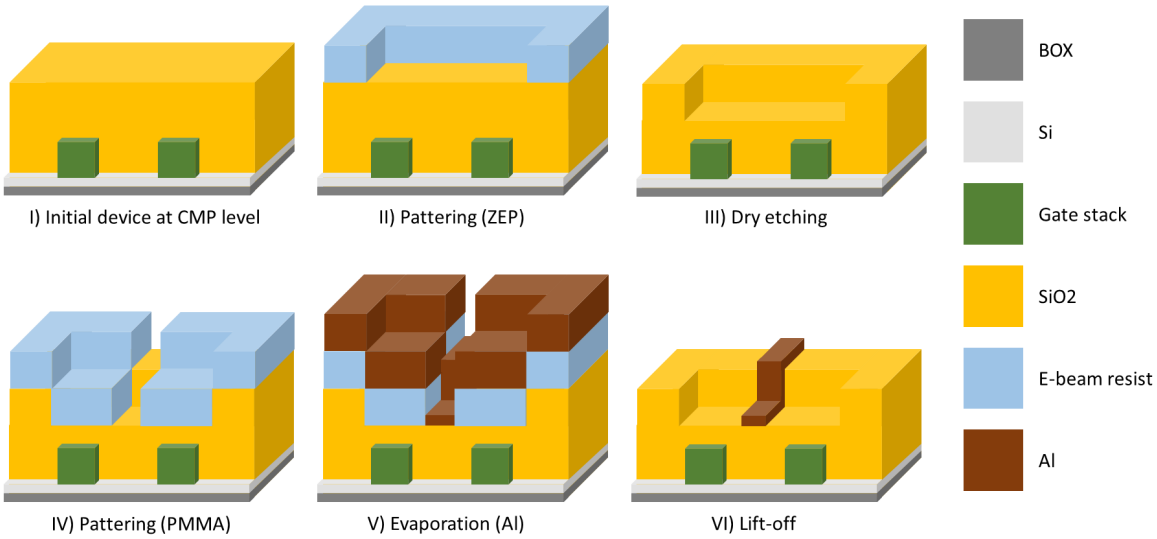


Figure 10: Illustration of the post-process flow with an "ebeam die"

4.3 Cleanroom processes

All of the cleanroom work was performed at the Plateforme Technologique Amont (PTA), in the 10.05 building of the CEA Grenoble. This cleanroom is used by several labs, the PTA staff provides machine training and technical assistance. The patterning step (including spin coating, exposition and development), part of the alignment cross fabrication and the evaporation of the first design were the steps realized by someone else due to the complexity of the tools and training delays. The other processes were performed by the author. It has to be noted that the cleanroom machine training took a large amount of time due to the sanitary measures.

4.3.1 Sample preparation

A chunk is first cut from the $300mm$ wafer and undergos the cross fabrication process (given in the appendix), the dies are then cleaved and individually cleaned.

4.3.2 Patterning

The patterning steps are critical since it allows to select the areas where to apply the processes following (etching, deposition...). Due to the small resolution required (10nm), Electron Beam Lithography (EBL) is employed. All of the EBL here have been realized on a JBX-6300-FS from Jeol by Jean-Luc Thomassin (including spin coating, exposition and development).

The sample is first covered with a layer of electron beam resist (organic compound that can dissolve after being exposed to an electron beam to achieve a patterned layer). The resist is evenly spread on the sample using the spin coating technique, the spinning speed and time allowing to control its thickness. The resist employed here are PMMA (suitable for lif-off) and ZEP 520A (preferred for etching) and are both positive. The sample is then placed in the tool and aligned using alignment crosses of known coordinates.

The sample is then exposed: a beam of electron accelerated (through the application of a $100kV$ bias) scans the sample pixel by pixel (vector scan along the design provided, in fields: area where the

alignment have been precisely calibrated) to deliver a precise amount of energy to activate the resist and give shape to the pattern. This energy dose is given by the formula:

$$D = \frac{I.t}{S} \tag{13}$$

Where D is the EBL exposure dose in uC/cm^2, I the current, t the exposure time, and S the total surface to expose. The current can take two value on the machine depending on the accuracy needed: $1nA$ and $5nA$ while the surface is fixed by the design. The dose to deliver can therefore be controlled with exposure time t.

This patterning methods enable to achieve high resolutions (electron diffraction being negligible) while offering the possibility to change the design as often as needed, which is critical for prototyping. On the downsize, unlike optical lithography that employs masks to achieve batch lithography, EBL is a direct writing methods and is therefore time consuming. It should be noted that the beam tends to drift in time, meaning a precision loss in large designs (their size making them long to expose). [12]

The sample is finally developed: in the case of positive resist such as the one used here, the area activated by the beam are removed using a specific solvent.

Electron beam lithography suffers from resolution limitations due to the proximity effect. The electron coming from the highly collimated beam penetrate the sample and interacts in a pear shape volume. The higher is the biasing voltage, the deeper the pear volume is located. Those high energy electrons are then backscattered toward the surface and contribute to activate resist areas surrounding the beam, broadening the original energy distribution. The spatial profile of the energy delivered to the resist thus becomes a thin peak -of the order of few nm- centered around the beam with a surrounding background stretching out on several um, as shown in figure 11. Dense design tends therefore to be broadened. On the other hand, isolated small features that are not bathed in this background, entailed by the proximity effect, can be underexposed. In those conditions, the dose must be chosen carefully to ensure an accurate reproduction of the design on the resist.

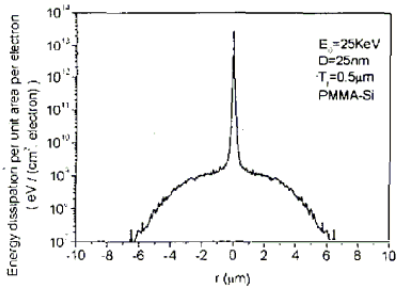


Figure 11: Energy delivered on the resist level around the beam - Adapted from [17]

In most of the cases here, it is preferable to obtain a small undercut of the resist (as shown in figure 12), this ensures a good liftoff by preventing deposition on the sidewalls and has no impact on the etching given the large size of this step's features.

During this internship, the procedure to get a sample patterned changed little. The design in a .gds format was presented to the weekly EBL meeting to be reviewed. Some modifications were sometimes necessary. After validation of the design and the sample provided, the spin-coating, exposure and development steps were carried out by Jean-Luc Thomassin or Romain Maurand and the patterned sample came back within a week. Most of the PhD students and interns are limited to one EBL per week, creating a bottle neck in the fabrication flow.

4.3.3 PVD: Evaporation

The deposition steps were done by evaporation with a MEB550 from Plassys. The principle is the following: the sample is placed in a vacuum chamber, vaporized atoms condense onto the cold sample

surface. The thickness of the layer is monitored using a piezoelectric resonator whose resonance shift gives the mass and hence the thickness deposited. An electron beam. accelerated using high electric fields and deflected with magnetic fields, hit a crucible containing the material to deposit. The deposition rates are of the order of few nm per seconds. The process time is dominated by the pumping steps of the chamber and the loadlock (that takes up to 30min). Aluminium, Chromium/Titanium and Platinum were employed here. Lift-off was employed to pattern those metal layers.

4.3.4 Lift-off

Lift-off processes are widely used in research cleanroom to pattern metals (in our case mostly Aluminium). It presents the advantage of offering a good resolution without the use of dangerous chemicals species required to etch metals. The sample is first patterned with a PMMA, before the deposition of a metal layer. The sample areas not covered by the resist receive thus a metal layer patterned as the resist (same polarity). The metal layer that have been deposed on top of the resist layer is removed during the so called lift-off step, as illustrated in figure 12.

Several points are critical to ensure the resist removal. As a rule of thumb, the resist thickness must be two to three times thicker than the layer to deposit. The resist sidewalls should not be perfectly vertical, but present a slight negative slope ("undercut"). This is necessary to prevent the deposition of metal on the sidewalls that would protect the resist in the final step. The removal of the resist can be accelerated with ultrasound (ease the resist and metal flakes lifting) and the sample can be heated up (speed up the chemical reactions). The lift-off recipes used are provided in the appendix.

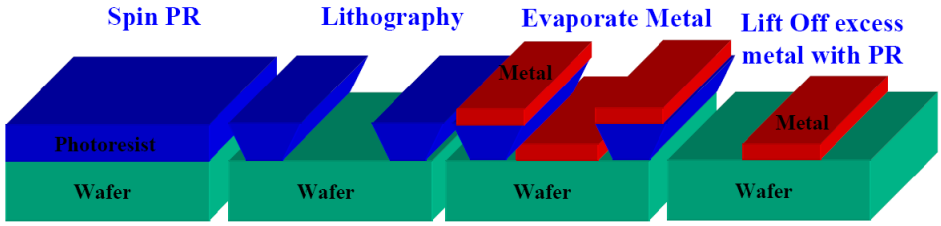


Figure 12: Lift-off principle - Adapted from [12]

4.3.5 Etching

The etching steps were realized using an ICP (Inductively Coupled Plasma) Etcher Plasmalab 100 from Oxford Instrument. The sample is first placed in a vacuum chamber. Gases are then introduced into the chamber, an RF excitation at $13.56MHz$ forces electrons to oscillate at high frequency, ionizing the gas, thus creating a highly reactive plasma. This RF exitation is combined with an RF bias that cause a directional bombardment on the sample, resulting in an anisotropic etching [12]. The equipment is fully automated, recipes can be programmed with the gas flow, timing, and RF power applied. The pumping steps on this tools are fairly quick (a few minutes), but the chamber must be cleaned before and after use by etching a clean Silicon wafer for 10 minutes.

Anisotropic etching is required in our process flow because vertical $SiO2$ sidewalls are required: undercut of $SiO2$ such as the ones produced with anisotropic processes would complicate the metal connection between the bottom of the pit and the surface. the etching recipe is provided in appendix.

4.3.6 Characterization: profilometer and SEM

Two tools were used to validate the processes results. The Dektak DXT E contact profilometer was employed to check the etching process. The sample surface is simply scanned by a stylus that applies a constant pressure on the surface, by lifting or lowering the tip using to a control loop. Such a tool enables a depth measurement of the order of 10nm. The tip has a 12um spherical shape that limits the lateral accuracy.

Because the subnanometric features are beyond the range of optical microscopes - due to light diffraction - a Scanning Electron Microscope (SEM) Zeiss Ultra Plus was necessary to observe the layout realized. The SEM shines an electron beam on the sample to observe instead of photons. Electrons are produced by a field emitter electron gun and focused using magnetic fields in place of lenses. The focused electron beam penetrates the sample and interacts in a pear shaped volume just like an electron beam lithography machine. The primary electron of the beam cause the ionization of atoms in the sample, generating thus secondary electrons of lower energy. This low energy induces a short mean free path, meaning that the only secondary electrons escaping the sample - and analyzed by the tool - are generated very close from the surface sample, yielding a highly spatialized information. Because the primary electrons - originated from the beam - are backscattered by the sample, some high energy electrons are also collected by the detectors and can gives information on the sample. The contrast is a function of the accelerating voltage (of the order of few kV), the chemical composition of the sample (atomic number) and working distance. [10]

It should be noted that the sample needs to be conductive in order to evacuate the electrons that otherwise accumulate and prevent the secondary electron and backscattered electrons collection, resulting in picture fading. High voltage can also damage the sample, creating pinholes. At last, extended observation of the same sample area can cause electron beam induced sample contamination. Such contamination originates from the alteration of organic molecules contaminant by the electron beam, that gradually grows a thin film on the surface sample and result in darker pictures [15].

Two detectors are available on the SEM used here: the SE2 and the inLens detector, both working with secondary electrons. The instruments offers many parameters that need to be tuned to obtain an image. For a given detector, voltage and WD (working distance, corresponds here to the focusing distance with respect to the magnetic lens in mm), the operator needs to play on magnification, focus, wobble (beam alignment) and astigmatism (different focal spot for different incidence angle, corrected by tuning the beam shape).

4.4 Design software: KLayout

The layouts were designed using KLayout, an open source layout edition software. Unlike full design suites such as Cadence Virtuoso, this program is solely focused on layout design, ie. drawing parametric shapes attached to a given layer (used to indicate different parameters or process step) organized hierarchically in cells.

A big advantage of KLayout is its powerful integrated script systems, working in python and ruby. For instance the main script used by the team gives the total selected surface, than can then be used to compute the exposition time of each layer of the e-beam lithography step. This exposition time has to be provided in a "jobfile" text file along with all the information necessary to the lithography, and is part of the design review process. In order to speed up the design process, a GUI script automatizing the jobfile generation (including the surface and exposition time calculation) was developed in python.

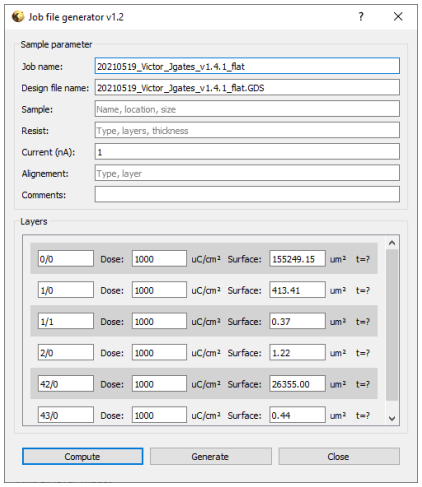


Figure 13: Screenshot of the jobfile generator GUI made

5 Fabrication: first design and process tests

This section aims to illustrate the iterative design process undertaken during this internship. A first test

5.1 A first exploratory design

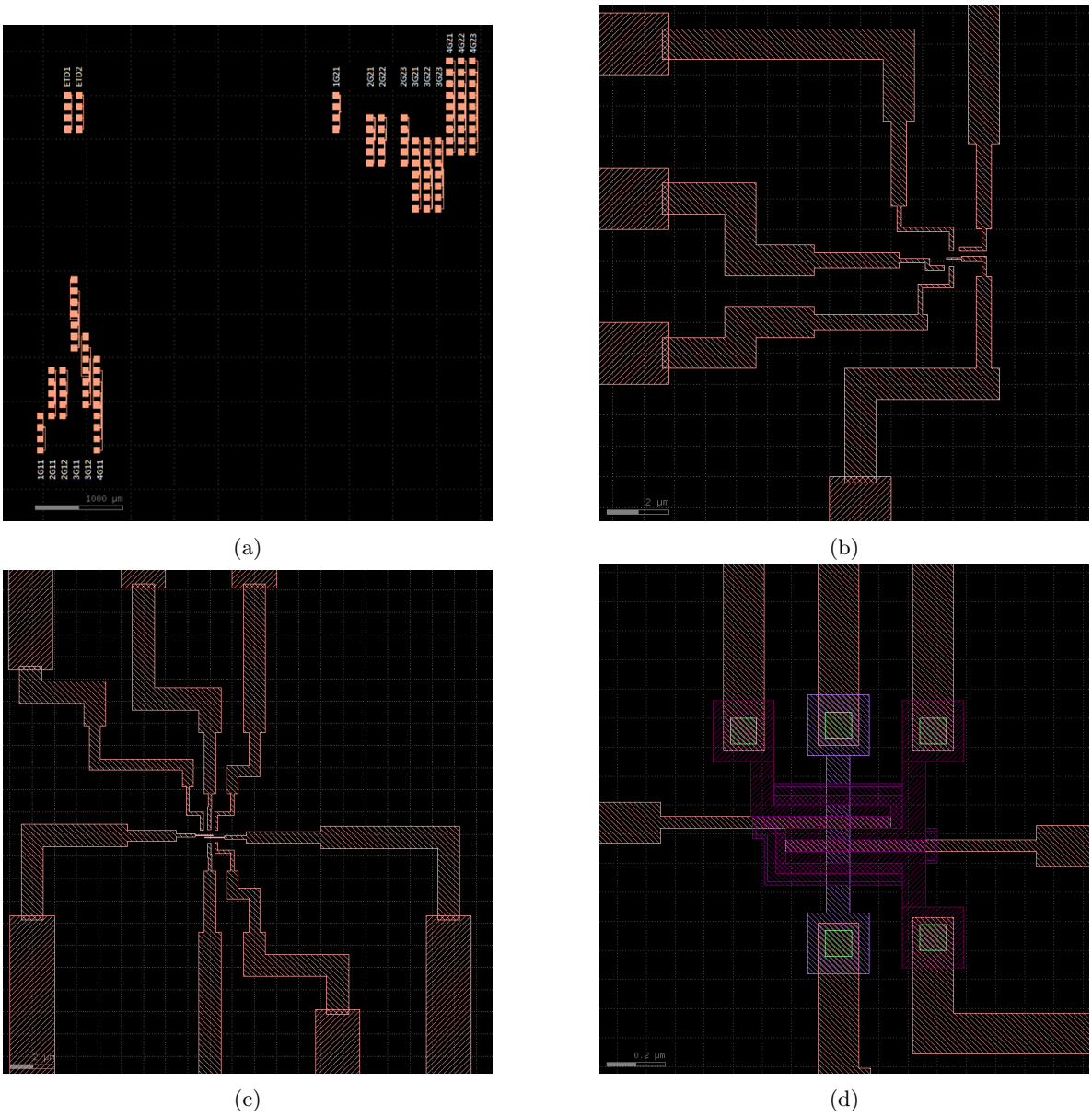
A first test was carried out to check our ability to align on the devices we selected (given in table 1 and assess the patterning resolution. Those devices were chosen due to their small size. It should be noted that the spacing between consecutive plunging gates is equals to the plunging gate length L_{device}.

Name	W_{device} (nm)	L_{device} (nm)	Number of plunging gates	Number of exchange gates
1G11	80	40	1	1 (top gate)
2G11	80	50	2	1
2G12	80	40	2	1
3G11	80	60	3	2
3G12	80	40	3	2
1G21	100	80	1	1 (top gate)
2G21	80	60	2	1
2G22	80	50	2	1
2G23	80	40	1	1
3G21	80	60	3	2
3G22	80	50	3	2
3G23	80	40	3	2
4G21	80	60	4	3
4G22	80	50	4	3
4G23	80	40	4	3

Table 1: List of the 15 devices selected to receive exchange gates. In the case of single plunging gate device, the exchange gate is actually a large "top gate"

5.1.1 Design and realization

The original metal layout, provided by the Leti, served as a starting point for the new design. The pads and wiring of the selected devices were kept and exchanges gates added in between the existing plunging gates (the exchange gates were designed with the same size as the plunging gates ie. 60 to 40nm). I was decided after a first review, to use different patterning doses: a $1000uC/cm^2$ for the features larger than 1um, and a dose of $1300uC/cm^2$ for the smaller features. The higher dose is required since the proximity effect is lowered in small designs, which leads to underexposure of the resist. One test cell with four points resistance measurement is also present.



(a) (b)

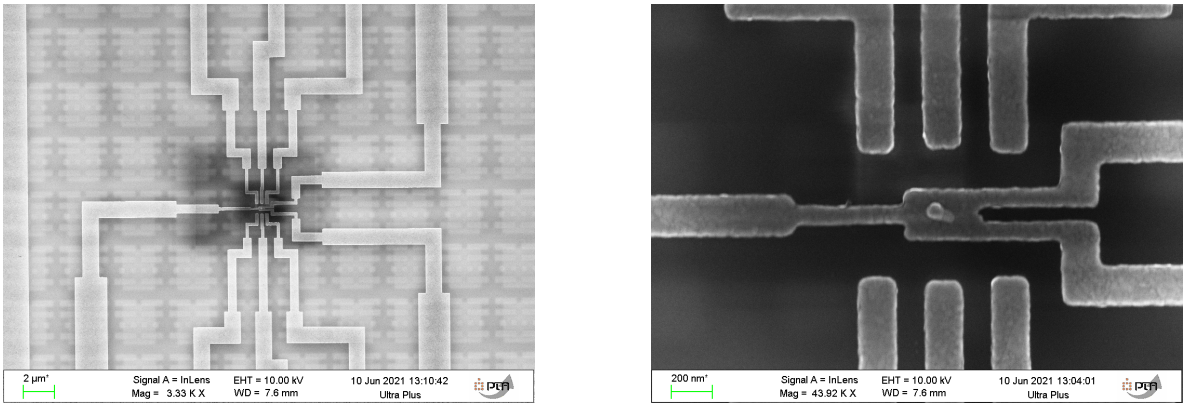
(c) (d)

Figure 14: First exchange gate design - Only the Aluminium layer is shown, **a)** Overview of the layout, annotated with devices **b)** Zoom on the 2G12 devices (1 exchange gate) **c)** Zoom on the 3G23 device (2 exchange gates) **d)** Zoom on the 3G23 device (2 exchange gates) superimposed with a view of the vias (green), active channel (purple) and plunging gates (pink)

This test was made on a "Deep-UV" die since no electrical tests were planned. After the patterning step, a 40nm thick Aluminium layer was evaporated and a lift-off realized. Aluminium was chosen to have bonding pads offering a good adhesion at the bonding step. Another advantage of Aluminium is that thanks to its relatively low atomic number, the devices tungsten vias beneath it can easily be seen with the SEM, making the contact check effortless.

5.1.2 Results

A SEM analysis revealed several issues on this sample. The first one is a pattern misalignment due to alignment crosses coordinates errors. The second and more concerning one is the exchange gate width, which is much larger than expected and leads in some case to gates merging. SEM pictures are provided in figure 15.



(a) (b)

Figure 15: SEM pictures of the first exploratory design **a)** Overview of the 4G11 device ($W_{target} = 60nm$), the center of the picture appears darker due to electron beam induced sample contamination, the structures in the background are dummy devices **b)** Zoom on the 4G11 device, the exchanges gates observed in the center are merged

The gate width oversize is thought to be caused by the dose used to pattern the smaller features. This first attempt shows that the exposure dose needs to be calibrated to obtain the expected result.

5.2 Process tests and calibration

This section develop the different process tests undertaken aiming to obtain a viable design. Two main test axis were explored: the etching axis whose purpose is to estimate the silicon dioxide thickness to etch and to calibrate an etching recipe, and a second test axis is dedicated to the patterning improvement.

5.2.1 Silicon dioxide etching calibration and thickness estimation

As highlighted in a previous section, the SiO_2 thickness protecting the device is unknown. The fastest way to estimate it was to cleave a die and to look for dummy devices that are present all over the design. Because those dummies lie at the same level than the devices, SiO_2 thickness can be measured by imaging the cross section of the die. SEM pictures of the cleaved die were realized. TEM picture would have provided better results, but were too complicated and costly to implement. A thickness of $t_{SiO_2} = 230 \pm 20nm$ was found, a picture is provided in figure 16.

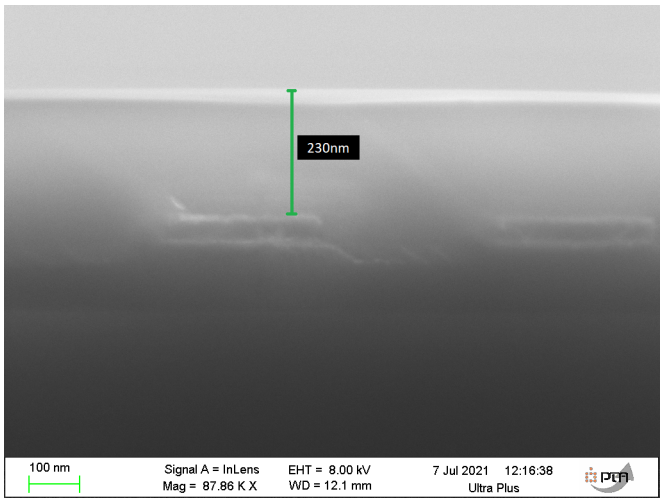
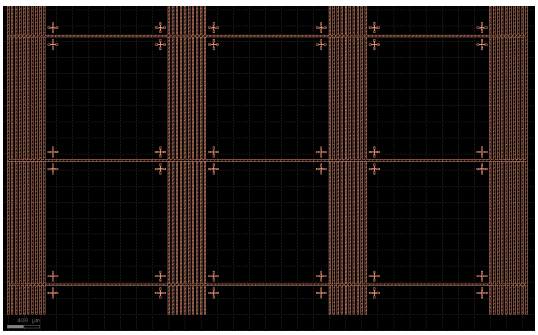


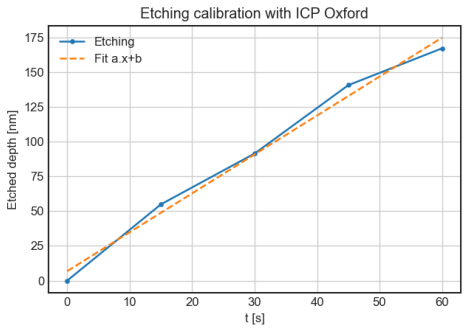
Figure 16: Cross section SEM picture of the wafer with a dummy device. The rectangular shape in the middle is the top of the dummy that lies at the same height as the active devices gate stack.

This gives us an idea of the depth to etch. A promising SiO_2 etching recipe (SF_4/CH_2F2 based) was found thanks to Frederick Gustavo. This CF_4/CH_2F_2 anisotropic etching process (isotropic etching gives problematic etching edges that prevent from a good contact between the bottom and the top of the pit) is detailed in appendix.

A design made of sequence of $20um$ wide strips were created to characterize the etching rate of the process using a profilometer. Four etching durations have been tested and measured, the result are provided in figure 17b. An etching rate of $168nm/min$ was measured, slightly higher than the one expected (around $150nm/min$) likely due too the poor quality of the passivation oxide. This etching recipe seem to suit the process flow needs.



(a)



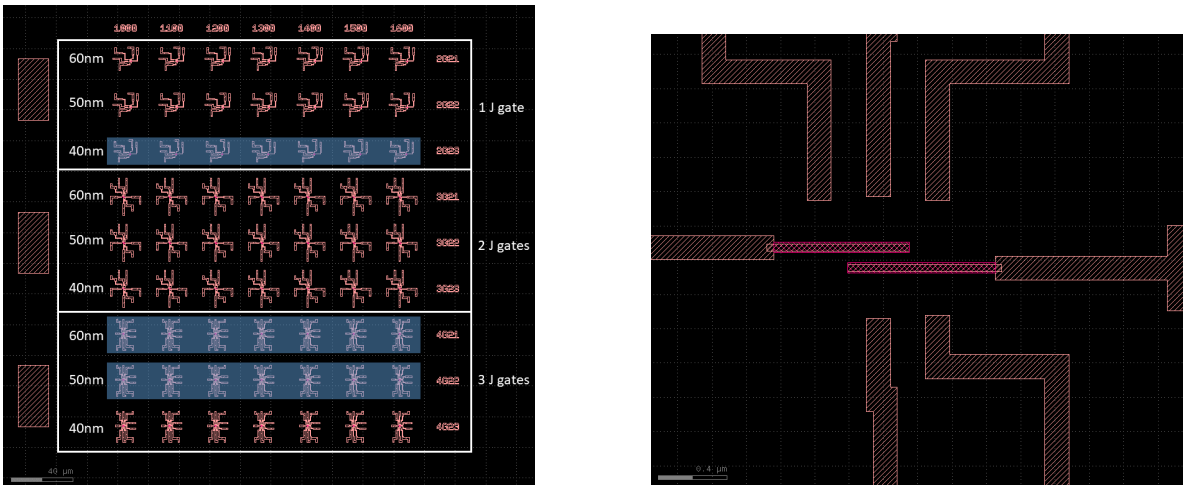
(b)

Figure 17: Etching test: layout and results **a)** Design used to characterize the etching recipe. The $20um$ wide strips can be characterized using a profilometer **b)** Calibration curve of the SF_4/CH_2F2 etching recipe used (SiO_2)

5.2.2 Patterning test

The first test highlight an exchange gate width issue, which is likely due to a wrong EBL dose and the proximity effect. To solve this problem, a dose test was required. A specific design was created for this

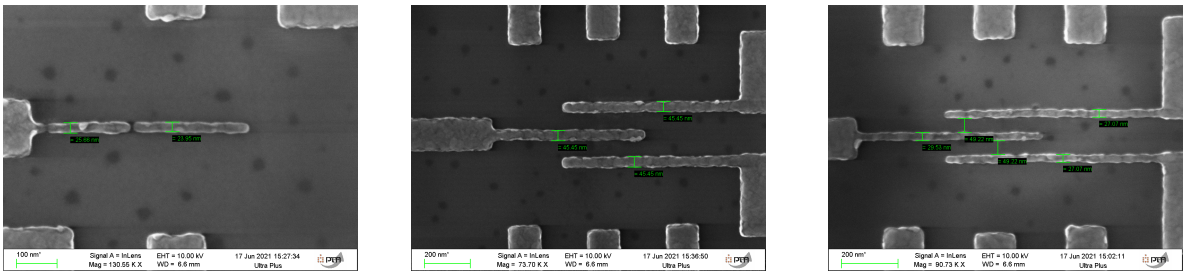
purpose, made of a cell containing all the critical features of the design to be tested with doses from $1000uC/cm^2$ to $1600uC/cm^2$ (the first test using a dose of $1300uC/cm^2$). Several copies of this test cell were placed along a Xnm wide dashed line making the test cell easier to find at SEM observation. The critical features of the design included in the test cell were the final device wiring (features inferior to $1um$) shot with a constant dose of $1000uC/cm^2$ and the exchange gates themselves shot with a variable dose. The latter were downsized by $20nm$ on the design. The idea is to downsize the feature width and to overexpose it in a controlled fashion, in order to increase the final size imprinted on the resist. This trick allows to minimize the proximity effect impact on the final width.



(a) (b)

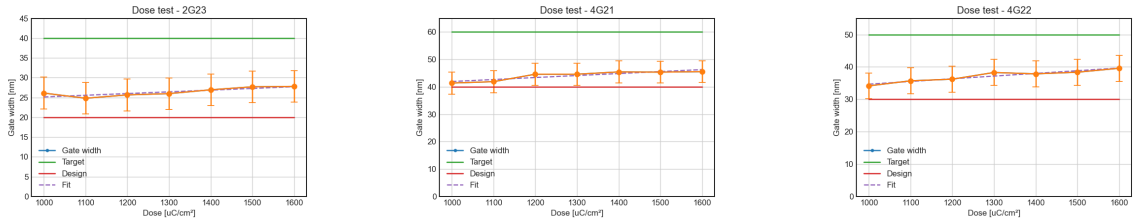
Figure 18: A few pictures of the dose test design - Only the Aluminium layer is shown **a)** Dose test cell, the dose is labeled on the top, the device type on the right. The devices measured for the graph in figure 20 are highlighted in blue. **b)** Zoom on the device 3G21 (2 exchange gates), the exchange gate (variable dose) and the wiring (constant dose) are on different layers. The pink layer indicates the expected size.

The design was then implemented on a sample using the patterning ($90nm$ of PMMA), evaporation (Aluminium, $40nm$) and lift-off processes already described. Pictures of a series of devices were then taken and the exchange gate width measured for the different EBL doses used. A selection of pictures is provided in figure 19 and the results of the measurements in figure 20.



(a) (b) (c)

Figure 19: A selection of SEM pictures taken to characterize the dose test sample. The darker dots are probably due to an incomplete stripping of the resist during the lift-off step, this has been solved in latter samples with a longer lift-off time and a better cleaning. **a)** 2G23 device ($W_{target} = 40nm$) for $D = 1100uC/cm^2$ **b)** 4G21 device ($W_{target} = 60nm$) for $D = 1400uC/cm^2$ **c)** 4G23 device ($W_{target} = 40nm$) for $D = 1400uC/cm^2$



(a) (b) (c)

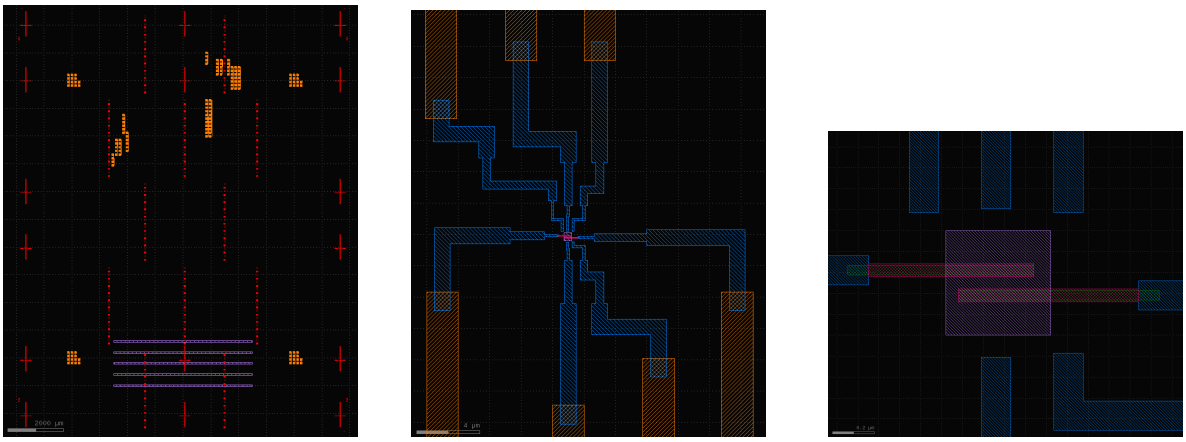
Figure 20: Gate widths obtained with the dose test using a 20nm gate width downsizing. Only some of the devices were measured due to the time taken by the measurement process **a)** Dose test results for the 2G23 device **b)** Dose test results for the 4G21 device **c)** Dose test results for the 4G22 device

As expected the exchange gate width increases with the dose. It is also observed that at low doses, several gates are broken or poorly defined. The downsizing of $20nm$ seems therefore slightly exaggerated. This dose test prompted us to choose a dose $D = 1450uC/cm^2$ for the gates with a downsizing of $15nm$, since it is preferable to have a higher dose with a smaller downsizing rather than a smaller dose and larger downsizing to counteract the proximity effect.

5.3 Improved design

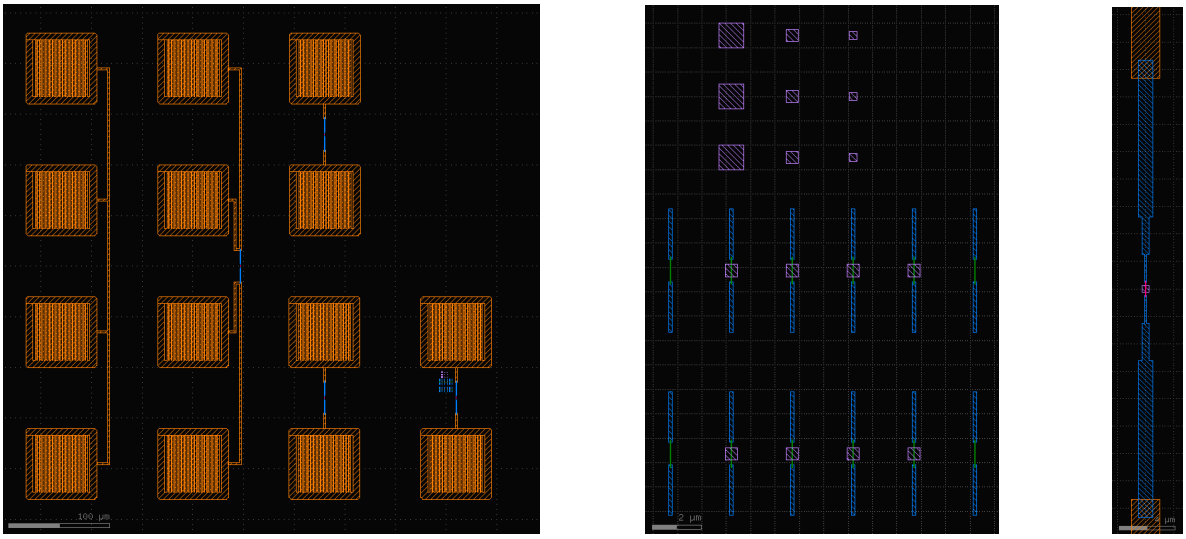
Piece by piece, the different process test realized helped to produce a better design. First, the devices with a large number of plunging gates were abandoned in order to save exposure time. To maximize the chance to obtain working device (in case of alignment or resolution issues), some exchange gates were replaced with larger "top gate" that cover the whole device (1G11, 2G11, 2G12, 3G11, 3G12). The patterning for the Aluminium evaporation was split into 3 successive shots:

1. One layer containing only the exchange gates, downsized by 15nm and patterned with a dose $D = 1450uC/cm^2$, performed first in a few seconds to prevent the tool from drifting in time
2. One layer containing the features smaller than 1um, with $D = 1000uC/cm^2$ performed in a second place, within a minute also to minimize the beam drift in time
3. One final layer with all the larger features, with $D = 1000uC/cm^2$ performed in one hour and half



(a) (b) (c)

Figure 21: A selection of pictures of the improved design - Alignment crosses are red. Aluminium evaporation is orange (low exposure dose, shot at the end), and blue (low exposure dose, shot in second) and green (high exposure dose, shot first). The expected gate size is pink while the area to etch are purple **a)** Global overview of the design. Each column of pad is a device, the groups of pads in the corner are test cells, the lower strips are test cells for cross section cut **b)** Zoom on a device (3G21, $W_{target} = 60nm$) with 2 exchange gates **c)** Zoom on the exchange gates part of a device (3G21, $W_{target} = 60nm$)



(a) (b) (c)

Figure 22: A selection of pictures of the improved design, test cell part, designed to allow SEM and electrical characterization, use same color code as figure 21. **a)** Overview of a test cell designed for two and four points resistance measures **b)** Zoom on test features for SEM check **c)** Zoom on test features (metal deposition across the edge of a pit)

The three layers overlap to ensure a good contact between the different sections, as shown for instance in figure 21c. Two new devices needed in other experiments were added at the team's request, with metal bond pads, wiring and top gates. Etching area -300 to 500nm rectangles- right over the

devices were also designed (figure 21). Finally, the choice was made to have four test cells compatible with four points and two points resistance measurement with etched area along the wire (figure 22. This allow to easily check if the connection is continuous without having to use a SEM. A transverse test cell is also present to realize cross section SEM analysis of the Aluminium layer on the pit edge.

This design was used to fabricate two samples, studied in the next section.

6 Devices obtained with the improved design

The improved design presented in the previous section was used to produce two samples. One, without the etching step aiming to bring the exchange gates closer to the device, was realized on an "ebeam die" (subsection 6.1, as in figure 23a). Another one was produced with the full process on a non electrically operational "Deep UV die" to put to the test our ability to fabricate continuous gates across the pit edges (subsection 6.2, as in figure 23b). This section presents the characterization of theses samples.

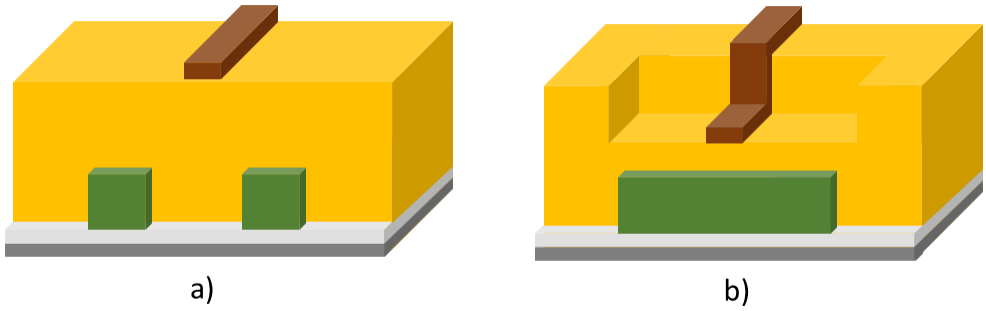


Figure 23: The two samples made with the improved design **a)** Device with gates at CMP level, made on a "ebeam die" having functional plunging gates **b)** Device with gates at pit level, made on a non functional "Deep UV die" with plunging gates in one block

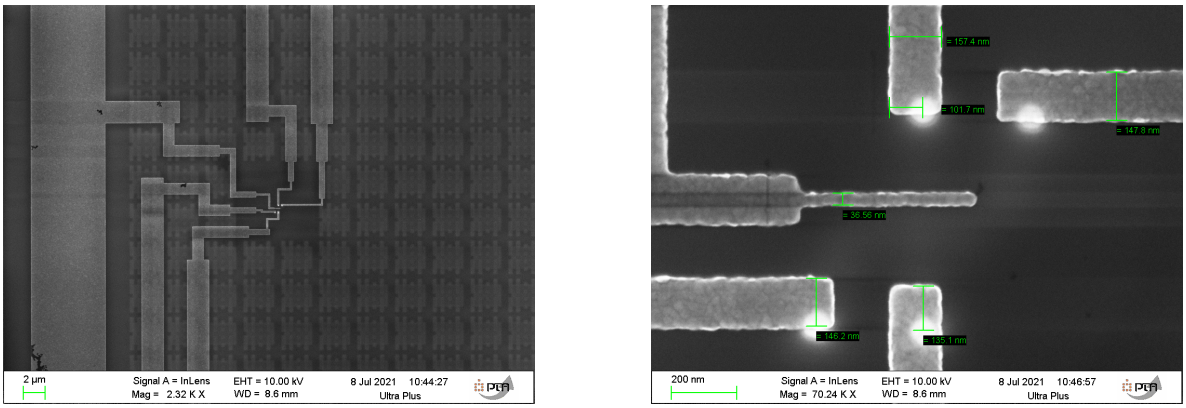
6.1 Device with gates at CMP level

A first sample was fabricated using an electrically functional "ebeam die". The etching step was skipped and the metal deposition was performed entirely at the CMP level. Because the exchange gates are far away ($\approx 250nm$) from the active channel, they are expected to have very little impact on the devices. This sample is though necessary to test our ability to accurately align, pattern and serves as a reference point over the exchange gates effect.

6.1.1 Post-fabrication characterization

SEM images were taken to check whether the EBL dose found in the previous tests produced the expected width, despite a different surrounding (the proximity effect being able to affect design over long distance). To prevent any damages that could be caused by the SEM, only some of the devices were observed. A selection of picture is provided in figure 24.

The exchange gates dimensions are close from the expected one and no broken gate has to be reported. The tungsten vias clearly stand out as bright dots (due to their much higher atomic number). The vias are contacted but a misalignment of $\Delta x \approx 20nm$ and $\Delta y \approx 70nm$ is observed. Since only one patterning step was performed, it is impossible to determine whether if this is a random misalignment or a constant offset. The vertical misalignment shifted the thin exchanges gates on top of the plunging gates, effectively screening them as on figure 23. In those conditions, only the large top gates (that are not completely screened out by the plunging gates) can effectively act on the electrostatic landscape in the active channel.



(a) (b)

(c) (d)

Figure 24: A selection of SEM pictures of the version with gates on CMP level **a)** 2G23 device, $W_{target} = 40nm$ **b)** Zoom on 2G23 device, $W_{target} = 40nm$ **c)** 3G23 device, $W_{target} = 40nm$ **d)** Zoom on 3G23 device, $W_{target} = 40nm$

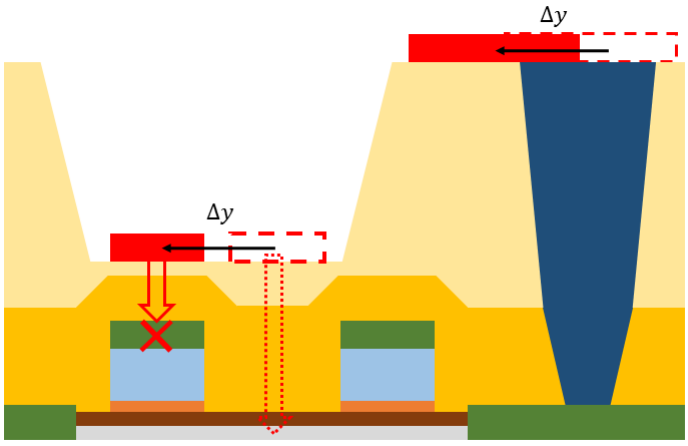


Figure 25: Impact of the gate misalignment. The Δy shift causes the thin exchange gates to be screened by the plunging gates

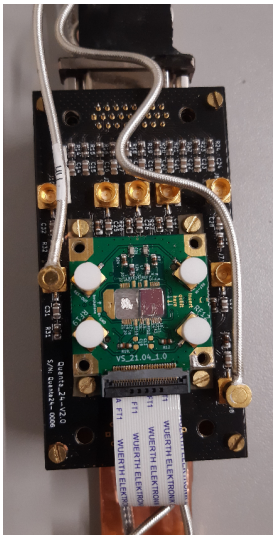
Overall, only part of the device could be expected to work properly due to the misalignment. The sample was then electrically characterized.

6.1.2 Sample preparation

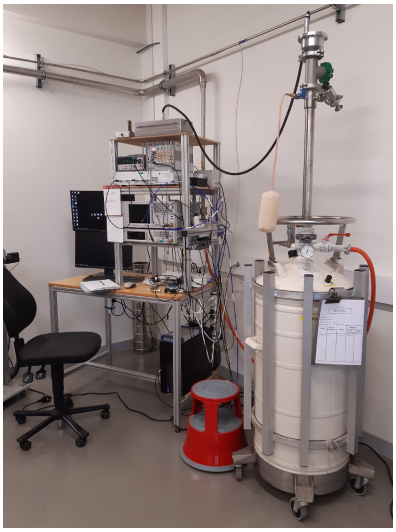
To be measured, the samples need first to be prepared. The die is cleaved into several parts and glued on a daughter board PCB a using conductive silver glue. The sample is then wedge bonded using a semi automatic HB10 Wire bonder by TPT that applies a force and a ultrasonic energy to solder $25um$ thick aluminum wires onto the bonding pads. This operation is delicate and time consuming, the wire can easily break and the sample contact pads be destroyed if the force or the ultrasonic power applied is not adapted.

The daughter board can then be placed on one of the standard motherboard PCB developed by the group that remains in each cryostats or 4K sticks, allowing to swap samples. This daughter board also contains the resonator tank circuit used for reflectometry measurements (not used here).

6.1.3 Measurement setup



(a)



(b)

Figure 26: **a)** Motherboard with a daughterboard and the device to be tested in the 4K stick. The ribbon is used to ground the device when handled **b)** Picture of the measurement setup. The 4K stick is placed on top of the Helium vase just before plunging it into the liquid He

The quantum dots effects discussed in the first section requires low temperature to be observed. Most of the experiments at PHELIQS are performed at $100mK$ or lower in dilution cryostats. Those can take several days to cool down. For fast measurements, 4K sticks are employed. Those are made of a $1.5m$ long stick with a motherboard placed at one end and connected with wires to the connectors placed at the other end of the stick. The whole apparatus is placed in a sealed tube, filled with Helium ($1mBar$) that acts as exchange gas, and plunged slowly into a vase of liquid Helium. The liquid Helium being at 4K, the stick is cooled down to almost 4K. The heat brought by the stick initially at 300K causes the evaporation o some liquid Helium (recovered with a dedicated system to limit the Helium

costs).

The 4K stick used was under repair at the beginning of the internship. Some time was spent to assist Estelle Vincent to fix it, by helping to solder the RF cables and their connectors (needed in other experiments using the 4K stick) as well as the 24 pins DC connectors.

The measurement setup is as following: the 4K stick (with the motherboard, daughter board and sample) is connected to a matrix box. This matrix box gives access to each of the 24 DC lines connected to the daughter board (and sample). Low pass filters are present on the mother board and before the I/V converter to remove high frequency noise. A Bilt Itest BN103 Digital to Analog converter (DAC) is employed to bias the device and control the gate voltages. A Femto DLPCA-200 I/V converter combined with an Agilent 34410A Digital MultiMeter (DMM) allow to measure the current I_d from the drain. A representation of the setup is given in figure 27. All the instruments are controlled from a computer using python scripts based on the QCoDeS library, an open source data acquisition framework developed by Copenhagen / Delft / Sydney / Microsoft quantum computing consortium [16].

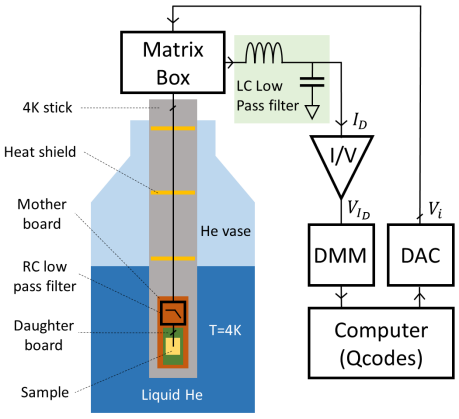
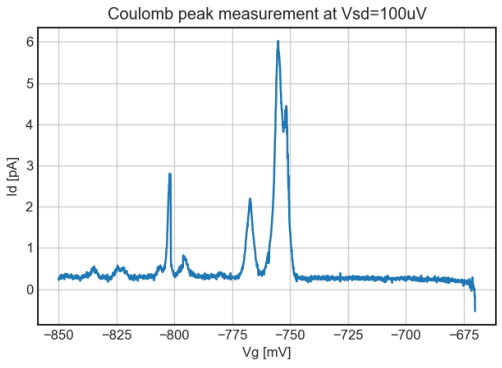


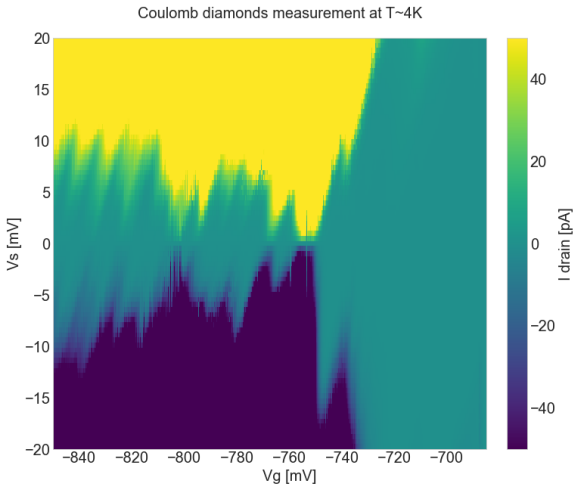
Figure 27: 4K measurement setup

6.1.4 Transport measurement

The measurement setup needed to be tested before measuring the actual sample to characterize. To this end, several test samples with devices similar to the one used in post process were measured. The results of one device (with $W = 60nm$, $L = 40nm$), measured at 4K are presented here. The first Coulomb peaks caused by the Coulomb blockade (as explained previously with figure 2b) are reported in figure 28a. Coulomb diamonds were also measured and are provided in figure 28b.



(a)



(b)

Figure 28: **a)** Coulomb peaks measured on the test sample **b)** Coulomb diamonds measured on the test sample

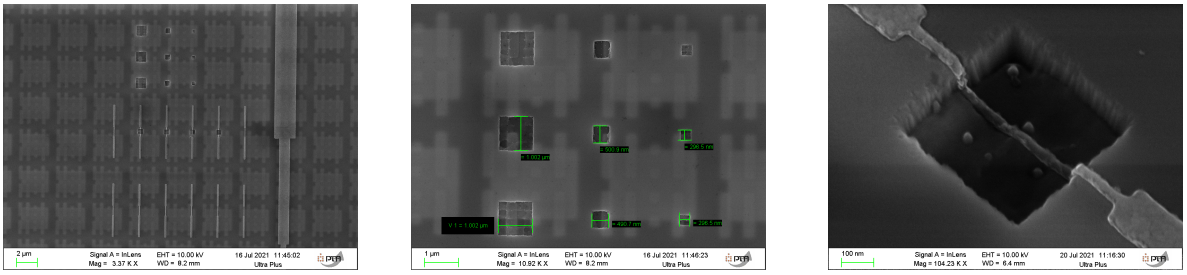
A period of approximately $11mV$ seems to be observed between the Coulomb peaks. Coulomb diamonds are observed but with fluctuating sizes. The huge first diamond is due to the blocking regime of the transistor. The large diamonds on right measure approximately $\Delta V_S/2 = 11.7mV$ over $\Delta V_G = 20mV$, giving $E_{add} \approx 11.7meV$ and $\alpha \approx 0.58$. The smaller one measure $\Delta V_S/2 = 5.2mV$ over $\Delta V_G = 11.5mV$, giving $E_{add} \approx 5meV$ and $\alpha \approx 0.45$. Such energy seems plausible compared to the electrons thermal energy at this temperature: $E_{th} = 3/2k_BT = 0.5meV$ at $T = 4K$, the difference is large enough to prevent electrons from jumping between the energy levels.

The sample fabricated was then measured but unfortunately, did not yield any results. The bonding pads on the sample proved to be more fragile and difficult to bond than expected. Some devices were sacrificed in order to find bonding parameters compatible with the pad employed (slightly different from the ones used previously). Two devices were successfully bonded, but did not react to the gate voltages applied, save for leakage effects at higher voltages. The bonding process having been difficult, it is possible that the devices were damaged during this final step.

6.2 Device with gates at pit level

A second sample was made from a non electrically functional "deep UV die" and aims to test the full process. Since no electrical characterization of the exchange gates were possible on this sample, only profilometer and SEM analysis were performed.

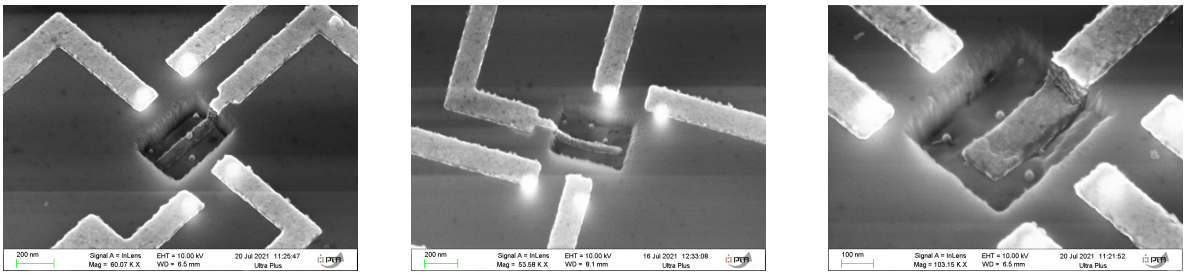
The transverse test cell, made of large etched strips, was use to measure the depth etched with the profilometer. An average depth of $138nm$ was measured, slightly less that the $150nm$ expected. The lateral dimensions of the etched area were measured with SEM (figure 29b) and are within the expected range . The slope of the pit spans over $20nm$ corresponding to sidewalls inclined of $8°$ with respect to the vertical. Pictures of the test cells are provided in figure 29. Small dots are visible at the bottom of the pit, those are likely to be a byproduct of the etching process. The pit floor appears to be slightly wavy as shown in figure31a.



(a) (b) (c)

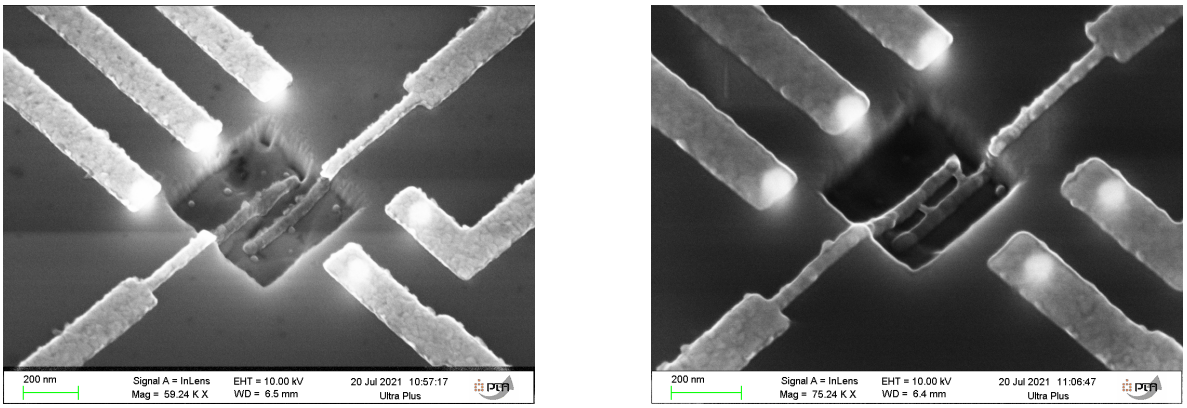
Figure 29: A selection of SEM pictures of the test cells of the version with gates at CMP level **a)** Test features on the test cell **b)** Zoom on the etch **c)** Pit connection test, $W_{pit} = 500nm$, $t_{etched} = 138nm$

In most of the test structures (such as in figure 29c) and devices observed (figures 30 and 31b), the gates are continuous over the pit edges. Over the 10 devices observed, only one presented merged gates which proves the possibility to pattern accurately at the bottom of the pit, despite the slightly wavy floor and the extra resist thickness induced by the pit.



(a) (b) (c)

Figure 30: A selection of SEM pictures of one exchange gate devices from the version with gates at pit level **a)** 2G12 device, $W_{target} = 68nm$ **b)** 2G23 device, $W_{target} = 40nm$ **c)** 3G12 device, $W_{target} = Xnm$



(a) (b)

Figure 31: A selection of SEM pictures of two exchange gates devices from the version with gates at pit level **a)** 3G22 device, $W_{target} = 50nm$ **b)** 3G23 device, $W_{target} = 40nm$

The etched areas and the gates are reasonably well aligned (within $10nm$) with each others proving the alignment to be reproducible, but surprisingly both the exchange gates and pit are misaligned with the vias. This could be caused by the presence of a small offset in the EBL tool or to a small error in the alignment crosses coordinates. This offset shifts the thin exchanges gates which cause them to be screened by the plunging gates at the active channel level. Only large exchange gates (as in figure 30 would have a chance of having an effect.

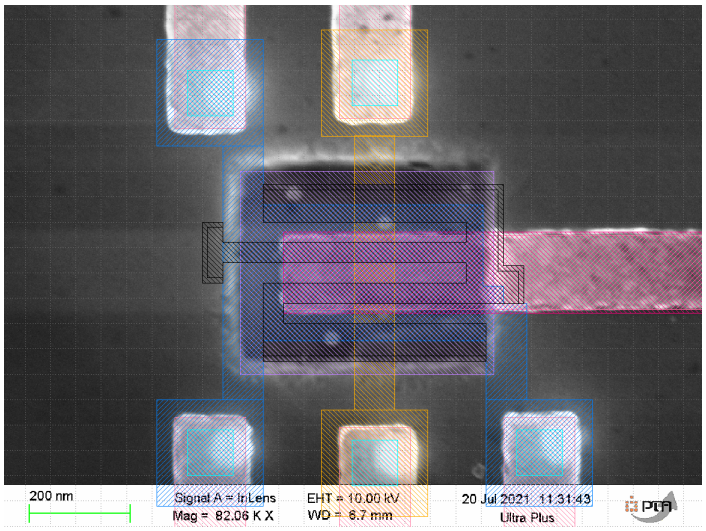


Figure 32: Design superposed over SEM picture of 3G12. The exchange gate/wiring are in pink, the area etched is in purple, the plunging gates in blue and black, the active channel is in orange and the vias are in light blue. The gate, wiring and etched area are aligned with eatch others but shifted with respect to the active device underneath

This device prove the feasibility of the whole process flow and its capability to produce thin additional continuous gates close to the device, but the alignment remains problematic.

6.3 Next steps

Those two samples prove the feasibility of the process initially envisioned, but many improvements are still possible. The two samples studied here show that a better alignment is required, the presence of an offset in the EBL tool or a small error in the alignment crosses coordinates must be investigated. The last test was limited to a shallow etch (the target was only $150nm$ while the devices are $220nm$ deep), the next test should try to get much closer to the devices. An etching recipe with a high selectivity between SiO_2 and Si_xN_y would be of precious assistance, making possible to place the exchanges gates right on top of the devices, using the SiN layer as an etch stop layer. The deposition of thin oxide layer (for instance with Atomic Layer Deposition technique) could be required to ensure that no short is formed between the exchanges gates and the existing stack. The etching step could be split into several sub-processes in order to achieve smooth edges, and ensure that the gates remain continuous over the pit edge, even for a $200nm$ deep pit.

7 Conclusion and perspectives

This report introduced the impact of control coupling in quantum dots and its effects. A post-process flow enabling the fabrication exchanges gates was presented and implemented on custom Si-MOS devices provided by the CEA Leti. The process flow delivered non functional devices, but most of the challenges initially anticipated were proven to be practicable, and no other issue was found. Exchange gates of the desired size were made, and remained continuous. The alignment crosses enabled to contact the active devices vias, but misalignment remains slightly larger than the tolerance level. Different improvements have been envisioned and should be implemented during a PhD which also includes a noise study, and how such structure can be used to perform two qubits gates operations.

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8 Appendix

8.1 Cleanroom recipes

This section summarizes the different cleanroom recipes employed.

Process	Usage	Recipe
Simple cleaning	Cleaning performed after a process and before EBL	• Bath of acetone (3 min) • Bath of IPA (3 min, do not let dry during transfer) • Blow dry
Improved cleaning	Used on the last samples to remove resist leftovers	• Simple cleaning • Diener stripper (Pico MW-PCCE 7): Standard etch: $P = 1mb$, O_2/Ar: [$55sccm$:$10sccm$], T¡116°C, from 2min to 10min • Simple cleaning
Resist stripping (PMMA)	To strip PMMA after a EBL	Same as simple cleaning but with steps of 5 min
Resist stripping (ZEP)	To strip PMMA after a EBL	• Expose with UVO-Cleaner for 4min • bath of MIBK:IPA [1:1], 1min30 • Bath of IPA (2 min, do not let dry during transfer)
Evaporation (Aluminium)	With a MEB550 from Plassy. To deposit $30nm$ for liftoff with	Al, 1nm/s, $30nm$, 20 min pumping steps
Lift-off (PMMA)	After Aluminium evaporation, to pattern the exchange gates	• Bath of acetone, ultrasounds (25 min) • Move the beaker to the 40°C bath (20 min) • Bath of IPA, ultrasounds (5 min, do not let dry during transfer) • Bath of IPA, ultrasounds (5 min, do not let dry during transfer) • Blow dry
Etching (SiO^2)	With an ICP Etcher Plasmalab 100. Used to dig the pit above the active devices	Cleaning with $SF_6/0_2$ (5min) with clean Si wafer before and after. CF_4/CH_2F_2 [$45sccm$:$5sccm$] RF power: $500W$, Bias power: $50W_B$, $P = 5mTorr$, T=20°C

Crosses patterning of the die provided by the CEA Leti (already patterned with TARF-P9000 LA, 1um and BARC AR19 still present at the bottom of the pattern):

- BARC removal with ICP SI-500-324 from Sentech (O_2, 10s) by Cécile Yu
- Evaporation (same as the one mentioned before but with Cr/Pt, 5/50nm)
- Lift-off
  - Clean bekers with acetone then IPA
  - Bath of ethyl lactate, ultrasounds (10min)
  - Bath of ethyl lactate, ultrasounds (10min)
  - Bath of ethyl lactate, at 40°C (10min)
  - Bath of IPA (5min)
- Improved cleaning, 10min

8.2 Cost estimate

Only direct costs of the internship can be estimated since the environment (offices, equipment, supervision, cleanroom running, administrative work etc.) is shared in between different actors and its costs cannot be easily calculated.

Type	Cost	Units	Comments	Total (€)
Salary	1300€/H	6 months	-	7800
EBeam Lithography (PTA)	100€/H	12 jobs	2H/job	2400
Evaporation machine (PTA)	50€/H	5.5H	-	275
RIE machine (PTA)	50€/H	6.5H	-	325
SEM (PTA)	50€/H	16H	-	800
Chemistry station (PTA)	20€/H	10H	-	200
Cleanroom work (PTA)	10€/H	36H	-	360
He (4K measures)	5€/L	3 cooldown	10L/cooldown	150

Table 2: Direct costs of this internship

The final cost of the internship is estimated at 12310€.

8.3 Gantt chart of the internship

Some of the work done in background has not be included on this Gantt chart. This includes tasks such as helping with the cryostats maintenance, git software assistance and sample preparation.

Victor Millory Internship Gantt chart

		15/03	22/03	29/03	05/04	12/04	19/04	26/04	03/05	10/05	17/05	24/05	31/05	07/06	14/06	21/06	28/06	05/07	12/07	19/07	26/07	02/08	09/08	16/08	23/08	30/08	06/09
Tasks	**Details**	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
Bibliography																											
Cleanroom training																											
Tests	1st design																										
	Etch test																										
	Dose test																										
	Thickness check																										
Device at CMP level																											
Device at pit level																											
Ebeam GUI																											
4K stick repair																											
Measurement																											
Master Thesis & defense																											
PTA tools availability	Orange=only some tools																										

Coupling control in Si-MOS quantum dots

Victor Millory

Nanotech track
Academic year: 2020-2021
From 15/03/2021 to 14/09/2021
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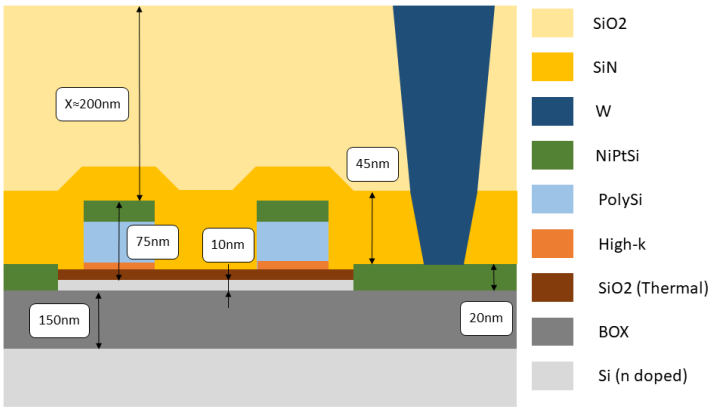

Fig. 1 - Stack composition of the devices provided by the CEA Leti

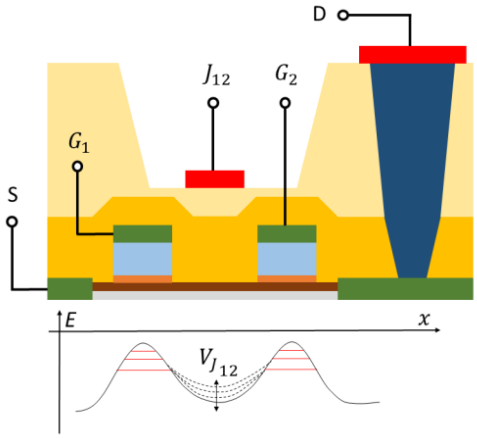

Fig. 2 - Device to fabricate and gate impact on the electrostatic landscape felt by holes

The demanding requirements of a practicable qubit implementation, summarized by the DiVicenzo criteria[1], illustrate the difficulty of qubit development. Amid the competing architectures, the recent Si-MOS spin qubit implementation[2] promises high integration by taking advantage of years of process development. Nevertheless, the higher integration sees the loss of coupling control between neighboring dots, which is yet needed to ensure that the qubits operate in an optimal regime and enable accurate readout [3,4]. This Master Thesis project reports the fabrication of exchanges gates enabling to control this coupling. Although no fully functional device has yet been produced, the process flow experimented here was found to be promising, since none of the fabrication challenges were proven to be intractable.

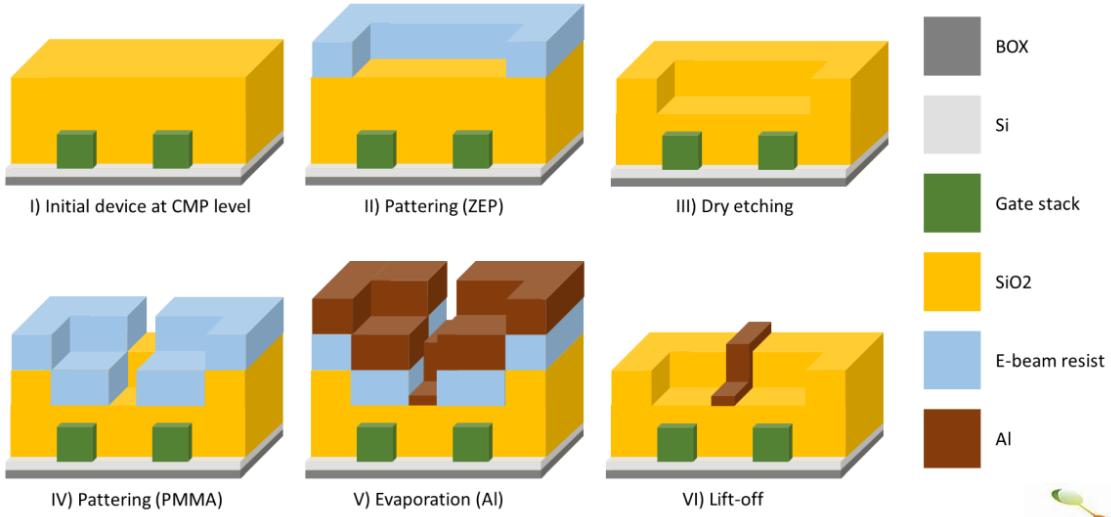

Fig. 3 – Process implemented

Fig. 4 – Layout of the devices

We successfully fabricated exchange gates on top of industrial-grade Si-MOS devices by overcoming the different process challenges (size, obtain continuous gates along the pit step, and –partially- alignment issues). Fully functional devices are yet to be made but the process is promising.

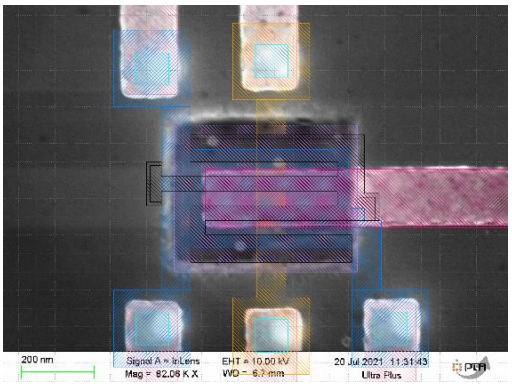

Fig. 6 – Layout and SEM picture superimposed. Alignment improvement is the next step

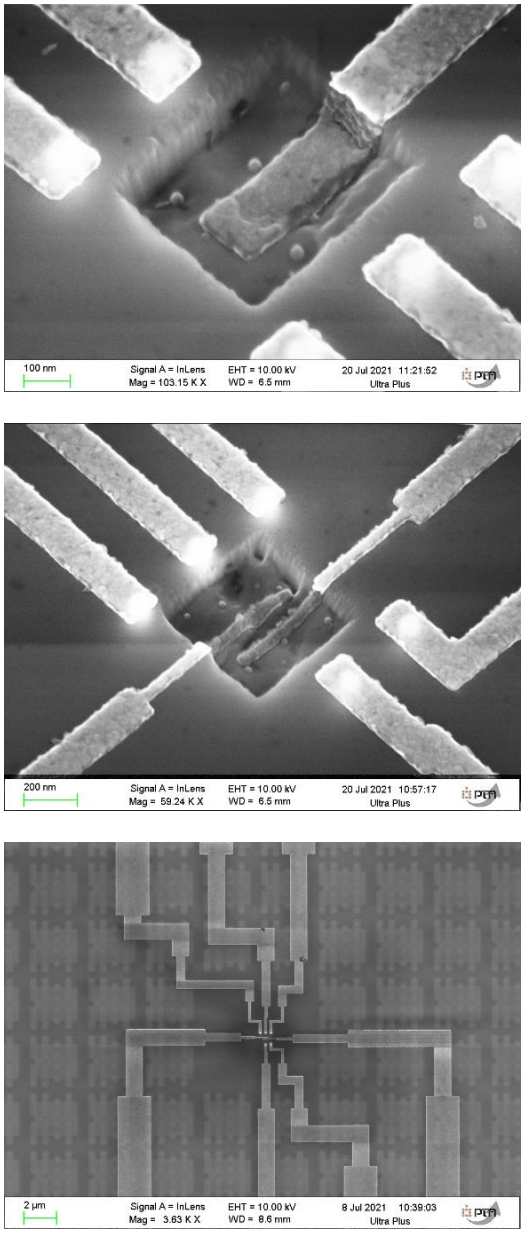

Fig. 5 - SEM pictures of the devices fabricated

With the guidance and help of:
S. De Franceschi, V. Schmitt, E. Vincent, M. Bassi, C. Yu, J.L. Thomassin, R. Maurand, F. Gustavo, S. Zihlmann, and the other members of the PHELIQS team and PTA staff

Cleanroom fabrication at the Plateforme Technologique Amont (PTA)

Equipment:

- Metal Evaporator (MEB550, Plassys)
- ICP Etcher (Plasmanlab100, Oxford Instrument)
- Stripper (Pico PCCE7, Diener)
- SEM (Zeiss Ultra+)
- Profilometer (Dektak DXT E)
- HB10 Wire bonder (TPT)
- 4K measurement station (4K stick)

References:

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