Politecnico di Torino

MASTER DEGREE THESIS

Broadband High Efficiency Class-F RF Power Amplifier

Author:
YUCHEN XIE

Supervisor:
Prof. VITTORIO CAMARCHIA
Dr. ANNA PIACIBELLO

October 13, 2021

Abstract

Broadband High Efficiency Class-F RF Power Amplifier

by YUCHEN XIE

The RF power amplifier is a crucial component in the modern telecommunication system, and it is also the component which consumes the largest portion of energy in the system. With the rapid development of wireless telecommunication techniques, the power consumption of the RF power amplifier has become more and more significant. Therefore, to reduce the power budget and improve the efficiency of the amplifier is an important topic in the future.

This thesis aims to focus on the whole family of Class-F RF power amplifiers and present the best performance of the Class-F topology. The family of Class-F amplifiers includes the Conventional mode RF power amplifier and Conventional mode RF inverse power amplifier, the Continuous mode RF power amplifier, and the Continuous mode RF inverse power amplifier. The main concern performance index is the efficiency of the amplifier. Therefore, the other performance will not be considered too much during the amplifier design.

The first step of the methodology is to review the whole family of Class-F theory to clear the difference between the inverse and the non-inverse amplifier and the difference between the conventional mode and continuous mode. Second step, we did plenty of investigation and research to figure out the proper topologies of the amplifier and set a desired objective for the final amplifier design. The third step, build the ideal amplifiers with the ADS software and indicate the highest efficiency while maintaining the smooth efficiency within the bandwidth. Finally, transfer the best ideal amplifier mode to the real amplifier, and fabricate this amplifier mode to evaluate with the real test environment.

The result of the thesis show that the best amplifier mode is the Continuous mode RF inverse power amplifier. This amplifier mode can maintain maximum efficiency and smooth within the bandwidth. Therefore, this amplifier mode is selected to fabricated and evaluated. This amplifier mode has 68%-78% efficiency with the ideal topology, and it has 65%-72% efficiency in the real amplifier. The bandwidth is from 1.5GHz to 2.0GHz. The fundamental frequency is 1.75GHz. The transducer gain is larger than 10dB within the entire bandwidth. The output power is around 40dBm. These results are satisfied the desired objective.

Acknowledgements

This project is a summary of my work in the last semester year. It is changing but very interesting. There are a lot of professional knowledge and experience was learned during this period. It is no doubt that this would not have been possible without the support of numerous people. First of all, I would like to thank my supervisor, **Prof. Vittorio Camarchia**, for his expert guidance. He led me into the world of analog telecommunication circuits in my first-year master's course. At that moment, I have been decided on my thesis topic and my future career plan. During my thesis period. He provides me continuous support, valuable discussion, constant encouragement and never-ending patience throughout my master thesis project. I deeply admire his professionalism. It is fortunate for me to get stat in this field with such an experienced guild.

I also would like to thank **Dr. Anna Piacibello**, who is my following supervisor, for the technical support and project detail guild. She has rich experience in RF power amplifier design. In addition, she taught me a lot of experience in circuit design and evaluation in CAD software. Therefore, I can really understand the process of the entire design process eventually. Moreover, when I encounter difficulties, she can always give me clear guidance and make me see the light.

Shuoyuan Qiao. He is my best friend. All the years we have known each other, from The Netherlands to Italy, you always gave me help and advice when I was in trouble and supported me without reservation. **Jianxing Wu** and **Chen Xie**. You are both my best friend, and thanks to your support during in my master study career, I will never forget our friendship.

Finally, I would like to thank my parents, thank you for giving me life. I cannot achieve my dream without your patience, understanding and support. I hope that in the future. I will make you proud of me again.

Contents

List of Figures

List of Tables

List of Abbreviations

RF	**R**adio **F**requency
BPF	**B**and **P**ass **F**ilter
OFDM	**O**rthogonal **F**requency **D**ivision **M**ultiplexing
WLAN	**W**ireless **L**ocal **A**rea **N**etwork
DC	**D**irect **C**urrent
AC	**A**lternating **C**urrent
PAs	**P**ower **A**mplifiers
CIMR	**C**arrier-to **I**ntermodulation **R**atio
IMP	**I**intermodulation **P**onducts
IIP	**I**nput **I**ntercept **P**oint
OIP	**O**utput **I**ntercept **P**oint
ACPR	**A**djacent **C**hannel **P**ower **R**atio
CCA	**C**urrent **C**onduct **A**ngle
Q-point	**Q**uiescent **P**oint
SiGe	**S**ilicon **G**ermanium
InP	**I**ndium **P**hosphide
GaN	**G**allium **N**itride
GaAs	**G**allium **A**rsenide
CMOS	**C**omplementary **M**etal **O**xide **S** emiconductor
FET	**F**ield **E**ffect **T**ransistor
BJT	**B**ipolar **J**unction **T**ransistor
HBT	**H**eterojunction **B**ipolar **T**ransistor
LDMOS	**L**aterally **D**iffiused **M**etal **O**xide **S**emiconductor
pHEMT	**P**seudomorphic **H**igh **E**lectron **M**obility **T**ransistor
SMD	**S**urface **M**ount **D**evices
TL	**T**ransimission **L**ine

List of Symbols

d	Distance	m
P	Power	W or dBm
ω	Angular frequency	rad
R	Electrical resistance	Ω
I	Electric current	A
V	Electric potential	V
Hz	Frequency	Hz
F	Capacitance	F
H	Inductance	H
G	Gain dB	
θ	Phase	°

Chapter 1

Introduction

1.1 Background

In the modern communication system, the RF power amplifier is a crucial part where the amplifier is located at the front of the TX path and is one significant consumer of power for the whole system. Therefore, higher consumption produces more heat, which is a critical situation that affects the performance of the power amplifier, such as efficiency. This issue increases the cost of communication system implementation, and the CO_2 emission due to wireless networking in our lives anywhere. Therefore, one of the objectives of the power amplifier is to reduce power consumption and increase efficiency. On the other hand, the 5G and OFDM technologies have been widely implemented in recent years. The bandwidth of the amplifier becomes wider on the frequency spectrum. How to keep the high efficiency with the wide bandwidth is an essential research topic in the future. Fig 1.1 illustrates a wireless base station block scheme of the communication system and indicates the role of the RF power amplifier.

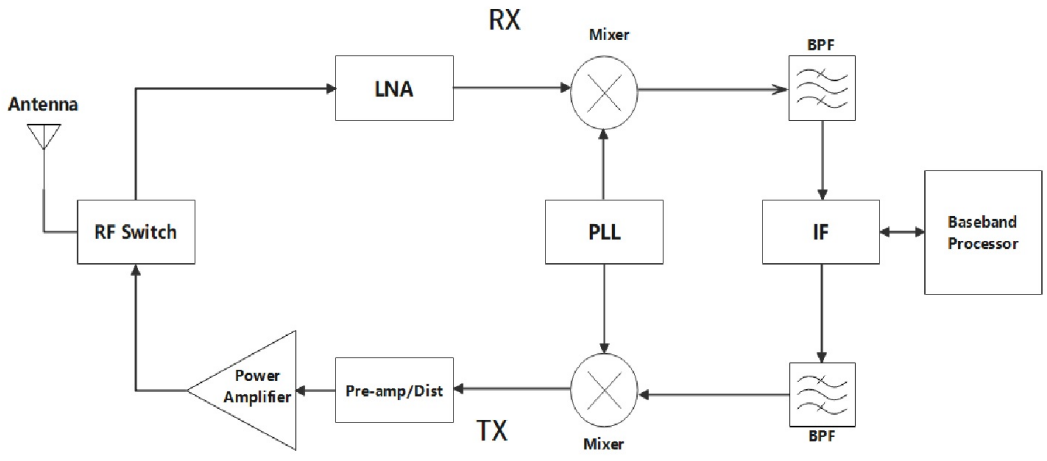


FIGURE 1.1: Wireless base station TX/RX block scheme

1.2 Project Overview

The main objective of this thesis is to research and develop the whole family Class-F RF power amplifier and find out the highest efficiency while maintaining the large bandwidth

amplifier topology. Then, employing the best performance amplifier topology to be fabricated and evaluated.

The high-efficiency RF power amplifier includes two types: The first type is switching mode amplifier. The switching mode efficiency can reach 100% in theory. The main class of the switch amplifier contains Class-E and Class-D amplifier. Another amplifier topology is the harmonic-loading amplifier, in which the tuned load is implemented for all order harmonics. The class of the amplifier is the Class-F amplifier. Compare two types of high-efficiency amplifier topologies. The Class-F amplifier has less influence from the active device. Therefore, the Class-F topology is a proper amplifier topology to implement for this thesis. Fig 1.2 is indicated the process of the thesis in each step. The thesis begins from the theory review, which contains Conventional mode Class-F/F^{-} and Continuous Model Class-F/F^{-} RF power amplifier. After the theory review, the ideal power amplifiers can be implemented with ADS software and analysis simulation results. The next step is to find out the best performance amplifier and realizing the ideal design and fabrication. Finally, measuring the performance of the power amplifier and give the conclusion.

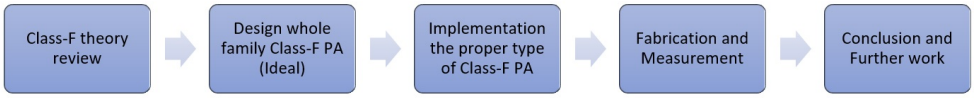


FIGURE 1.2: Main process for the thesis

The critical performance items of the power amplifier are high-efficiency while maintaining the bandwidth wider as much as possible in this thesis. Considering the property of the amplifier always trade-off each other when implementation, it is unrealistic to achieve all optimal properties. Thus, bandwidth and efficiency always have priority during the thesis research and implementation. Table 1.1 lists the requirements for the thesis. The operating frequency was defined at 1.75 GHz (L-Band IEEE). The output power is 10W, and the gain is the best effort. The bandwidth is 400 MHz at least and the efficiency within bandwidth should be grater than 60%. The last item within the table includes all series of Class-F amplifiers. The research step should consider and evaluate all series of the amplifier by ADS software with ideal conditions, then select the best performance amplifier to implement in the realistic design.

Operating Frequency	1.75 GHz
Output power in Bandwidth	10W (40dBm)
Gain	Best effort
Efficiency in Bandwidth (DCtoRF)	$\geq$ 60%
Power Amplifier Bandwidth	$\geq$ 400 MHz
Research PAs Items	1) Conventional Class-F 2) Inverse Conventional Class-F 3) Continuous-Mode Class-F 4) Inverse Continuous-Mode Class-F

TABLE 1.1: RF power amplifier design requirements

1.3 Thesis Outline

Chapter 2 will review the fundamental theory of the power amplifier, the first section is describe the critical parameters and characteristics in theory. Then, an introduction of the power amplifier operating class is given, the Class-F and Class-J will provide more discussion in order to understand the thesis clearly. Moreover. The active device is the core component of the amplifier, this chapter will give a short introduction to indicate each of the different active devices, and why the HEMT device was selected to design the power amplifier.

Chapter 3 is the initial design section. The main content of this chapter includes the active device study and the input/output section. Firstly, some parameters must be determined before the amplifier design, such as the bias point, DC voltage of the gate and the drain, stability, maximum gain, and the bias network. Secondly, input/output matching network theory should be reviewed and select some proper matching networks in order to realize the project requirements.

Chapter 4 and 5 are the design part of the thesis. The objective is to build the four types of ideal Class-F amplifiers by ADS software, including the Conventional Class-F/$F^{-}$and Continuous Mode Class-F/F^{-}.Then, select the highest efficiency PA topology, and meanwhile, conform to other project requirements. The content of chapter 5 is the implementation and evaluation of the best performance amplifier topology and gives the conclusion of this topology eventually.

Chapter 6 is the conclusion and gives the goals of further work in the future, such as the part of the power amplifier must be improved, and some works are not complete due to the schedule not catching up.

Chapter 2

Power Amplifier Fundamentals

2.1 Characteristics of Power Amplifier

At the transmitting terminal of the wireless system, the antenna (load) needs hundreds of power watts. However, the power only has a few tens of watts at the RF input port. Therefore, the power amplifier has to be used to increase the magnitude of the modulated wave to the high power level to match the antenna. The basic topology of the RF power amplifier is illustrated in Fig 2.1. The energy flow transfer from left to right, which is RF input power coming from RF input port, DC power coming from the DC source, and the output power signal is the RF signal. The output power signal transfer to the load(R_L), and the load transmitted to the receiver terminal eventually.

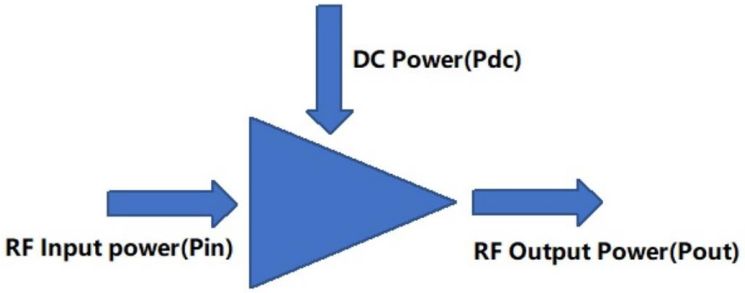


FIGURE 2.1: Basic operation of RF power amplifier

The basics operation, as shown in Fig 2.1, and the amplifiers relation between output and input can be formulated as follows:

Output power and input power relation with operational gain G_{op}:

$$P_{\text{out}}(f_0) = G_{op} * P_{\text{in}}(f_0) \tag{2.1}$$

Output power and input power relation with transducer gain G_t:

$$P_{\text{out}}(f_0) = G_t * P_{\text{av,in}}(f_0) \tag{2.2}$$

The power amplifier is a quasi-linear or nonlinear device. Therefore, the f_0 means the fundamental frequency at the center of the signal, if the signal includes high-order harmonics which can be represented $n \cdot f_0$. The main objective of the power amplifier is to transfer

the maximum power from the output to the load; as in the previous equations, the gain is a critical parameter when the input power is fixed. The P_{in} is the power transferred from the input power generator to the device. The $P_{av,in}$ is the power available (generated) by the input power generator.

On the other hand, the power amplifier consists of the active device. It depends on the maximum voltage and current swing limited of the active device. The saturation of the voltage and current at the drain (FET device) terminal must be attended for the amplifier design. This phenomenon is power saturation P_{sat}.

Efficiency and Power-Added Efficiency

The power amplifier's efficiency is the ratio of the RF output power and the DC bias power, as indicated in Equation 2.3. At the fundamental frequency, this power partly converter into the RF output power and in part dissipated into heat by the active device. This efficiency is also a representation of "Drain Efficiency" when the active device is FET structure.

$$\eta = \frac{P_{\text{out}}}{P_{DC}} \tag{2.3}$$

Another critical parameter is Power-Added Efficiency (PAE), which is similar to standard power efficiency, but it takes into account the RF power that is added to the device at its input and also the gain of the amplifier.

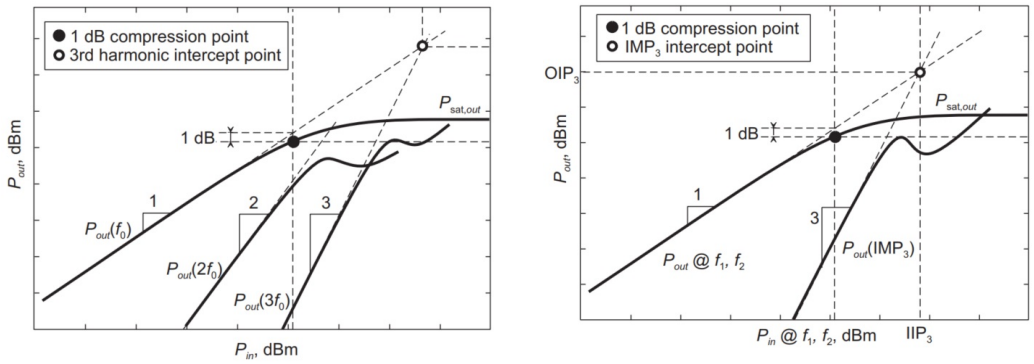
$$\text{PAE} = \frac{P_{\text{out}}\ (f_0) - P_{\text{in}}\ (f_0)}{P_{DC}} = \eta \left(1 - \frac{1}{G_{\text{op}}}\right) \tag{2.4}$$

P_{in} - P_{out} Characteristics

The characteristic of the power amplifier is a quasi-linear or nonlinear device as mentioned above. Therefore, the nonlinear power amplifier device exhibits complex behavior when input power is compared to output power, such as the harmonic generated, intermodulation products, and the power saturation[8]. Thus, the output signal level is different from the input signal level, and the behavior of the amplifier output signal depends on the input signal significantly. The output power of harmonics can be modeled by Equation 2.5, and the equation is represented to the harmonics with the single or two-tone test in the small-signal condition, where the K_n is the operation gain:

$$P_{\text{out}}\ (nf_0) = K_n \left[P_{\text{in}}\ (f_0)\right]^n \tag{2.5}$$

This relation is illustrated in Fig 2.2. Figure A is the single-tone test, and Figure B is the two-tone test. These graphs are in the log scale and the power defined in dBm. Among the critical specifications for the power amplifiers are their power output specification. At the fundamental frequency, the P_{sat} refers to the saturated output power, which is means the output power where the Pin-Pout curve slop goes to zero. The P_{1dB} refers to the output power at the 1dB compression point. It represented the input power that causes the gain to decrease by 1dB from the regular expected linear gain graph and where the amplifier goes to compression and nonlinear[8]. Another critical parameter is IP_3 (*Third-order Intercept Point*). This parameter represents a magnitude of linearity and harmonic distortion. Therefore, a higher IP_3 means the amplifier has better linearity and less harmonic distortion[8].



(A) P_{in} - P_{out} under single-tone test

(B) P_{in} - P_{out} under two-tonetest

FIGURE 2.2: P_{in} - P_{out} characteristics curve[8]

Intermodulation Products

The harmonics begin to be produced when the power amplifier becomes nonlinear. The second, third, and higher-order harmonics are outside the amplifier bandwidth, these harmonics signal are usually easy to filter out in this situation. However, if the signals are close together in frequency, some of the sum and difference frequencies called intermodulation products produced can occur within the band of the amplifier[17]. Some intermodulation products are of great concern as they are difficult to filter out. Considering two individual signals, f_1, f_2 occurring within the band of the amplifier. With the harmonic distortion, the new signals $f_2 - f_1$ and $f_2 + f_1$ are produced and can be filtered out easily. These signal products are called second-order intermodulation products. However, these products have not only the second-order products but also the higher harmonics to produce potentially interfering signals with amplifier passband. The third-order intermodulation products are the most troublesome, which are $2f_1 \pm f_2$ and $2f_2 \pm f_1$. The interfering signals usually occur in $2f_1 - f_2$ and $2f_2 - f_1$, as shown in Fig 2.3. The main products cause for harmonic distortion.[8]

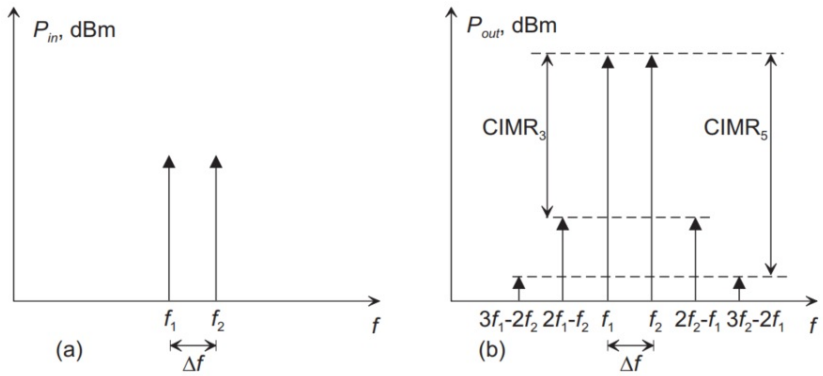


FIGURE 2.3: Input (a) and output (b) power spectrum under the two-tone test[8]

The above figure is indicated the third and fifth harmonic (IMP$_3$,IMP$_5$), these harmonic products fall close to the input band according to the previous relations function (f_1, f_2), back to the Fig 2.2, which can be defined as the slop of the IMP$_n$ output power is n, and

from the power at fundamentals and the IMP_n (with n odd), the n-the order carrier-to-intermodulation ratio $CIMR_n$ defines as[8]:

$$\mathrm{CIMR}_n = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}}\ (\mathrm{IMP}_n)} \tag{2.6}$$

In dB unit:

$$\mathrm{CIMR}_n|_{\mathrm{dB}} = P_{\mathrm{out}}\ |_{\mathrm{dBm}} - P_{\mathrm{out}}\ (\mathrm{IMP}_n)|_{\mathrm{dBm}} \tag{2.7}$$

The P_{out} is the output power at the fundamental frequency, and the $P_{out}(IMP_n)$ is the output power at the n-th intermodulation products, which can be defined by Equation 2.5 (replace the fundamental frequency condition to n-th harmonic), and the $CIMR_n$ can be figured out eventually.

Adjacent Channel Power Ration ACPR

The output spectrum generates the odd-order intermodulation products during the modulated signal test. Fig 2.4 illustrates the input modulated signal and after the amplified output signal. The noise around the IMP3 on the spectrum left and right. This noise is named the spectrum regrowth, and the spectrum regrowth channel is named the adjacent channel, which the ACPR parameter can derive. The ACPR is the important performance metric to account for the spectrum regrowth within the band.

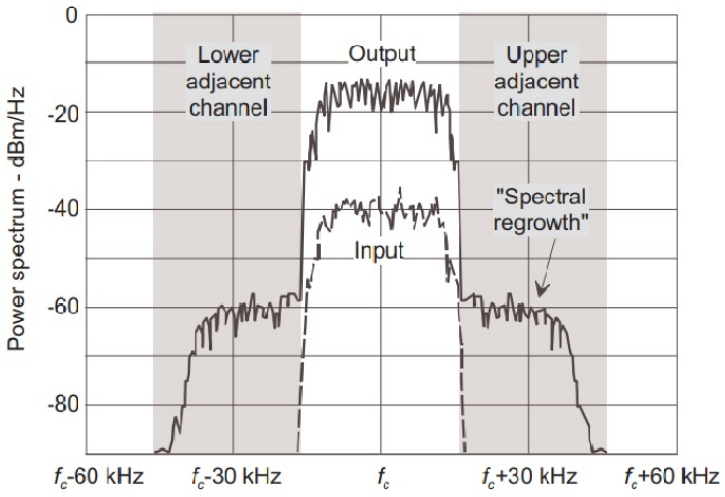


FIGURE 2.4: Spectrum Regrowth[8]

Gain offset and Phase Distortion(AM/AM and AM/PM)

Gain offset(AM/AM) and Phase distortion(AM/PM) are two significantly distortion to effects in power amplifiers. The spectral regrowth and a bit errors are being produced in the transmitted and the received signal. For the nonlinear behavior. The output differs from the input signal, and the distortion causes it. When the power amplifier employs a third-order power series approximation, the power amplifier's output voltage can be formulated as the function of input voltage

$$V_{out} = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3 \tag{2.8}$$

The a_1, a_2, a_3 are the factors of amplifications, and the V_o, V_{in} are the output/input voltage. This is an instantaneous model, which means the input/output of the power amplifier is memory-less description. However, in the real world, the power amplifier is the dynamic system with memory. The output signal and the phase are affected by the nonlinear behavior [5]. The input signal can be assumed to:

$$V_{in} = A(t) \cdot \cos[2\pi f t + \varphi(t)] \tag{2.9}$$

For the output signal, both the amplitude and phase may exhibit nonlinear phenomena. The output model can be written as:

$$V_{out} = G[A(t)] \cdot \cos\{2\pi f t + \varphi(t) + \theta[A(t)]\} \tag{2.10}$$

Where the $G[A(t)]$ is the gain, and the $\theta[A(t)]$ is the phase change. The nonlinear behavior in gain is the AM/AM compression, while in phase change is AM/PM conversion effects, and the $\theta[A(t)]$ is not the constant. The AM/ AM and AM/PM curve are plotted in Fig. 2.4[5]

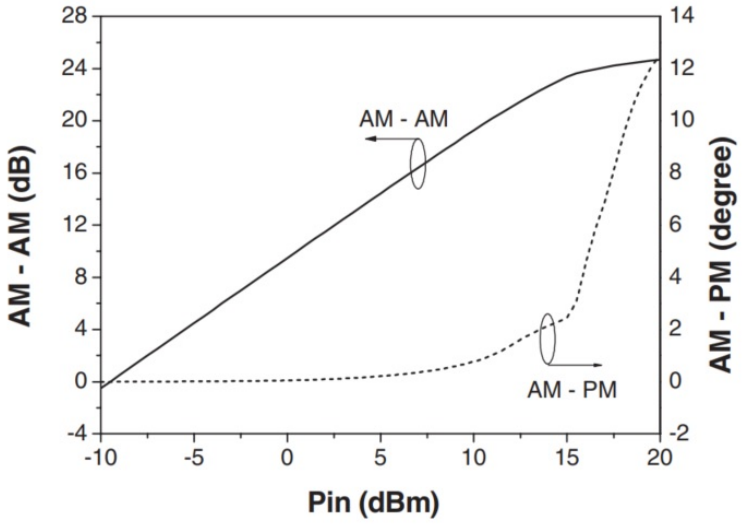


FIGURE 2.5: AM/AM compression and AM/PM conversion curves for a power amplifier[8]

This phenomenon (AM/AM, AM/PM) can happen because of the transistor model's nonlinear behavior, such as the conductance and the internal capacitor and inductor. The AM/AM and AM/PM can be found depending on the input drive level, as illustrated in Fig 2.5. This phenomenon can cause constellation distortion and affect the antenna's beamforming capacity lead to performance reduction (phase array application.[5])

2.2 Power Amplifier Class

The Power Amplifier (PAs) are classified into two main topologies, the linear (quasi-linear) and the non-linear. The output power of linear PAs is directly proportional to input power

and without excessive power of harmonics. Whereas in non-linear PAs, input and output power are not proportional, and the harmonic power is created with the main signal. The amplifiers can also fall into one of three classifications (class), namely the biasing, switching model, and harmonic-loading amplifier[6]. The Biasing PAs are classified as such due to their inherent quiescent point and/or our output Current Conduct Angle (CCA) θ. The θ can be defined as "the fraction of RF input drive signal where the non-zero current is flowing through the device."[5]. and the class of biasing PAs, namely Class A, AB, C. Another type of PAs is switching model (Class-D, Class-E) and harmonic-loading (Class-F) PAs, which have a network configuration attached to an active element, though not at the bias level. Therefore, switch transistors are switches that turn off and on in accordance with the input drive signal[5]. The switching amplifiers have high efficiency and PAE and can reach the 100% in theory. Fig 2.6 illustrates the family tree of the power amplifier.

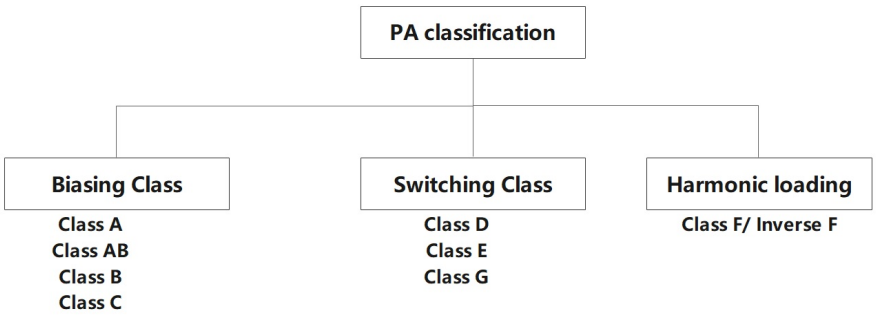


FIGURE 2.6: Family tree of power amplifier classification

2.2.1 Class A

Class-A is a quasi-linear amplifier and the conduction angle is 360°. This single output transistor is biased around the Q-point within the middle of its load-line and not goes into the saturation regions, which means the Class-A amplifier is never "off". Thus, the output voltage waveform and current waveform are both whole sinusoids and overlapping each other. Therefore, the Class-A amplifiers have outstanding linearity, but the maximum efficiency is only 50%. Fig 2.7 illustrates the Class-A characteristics.

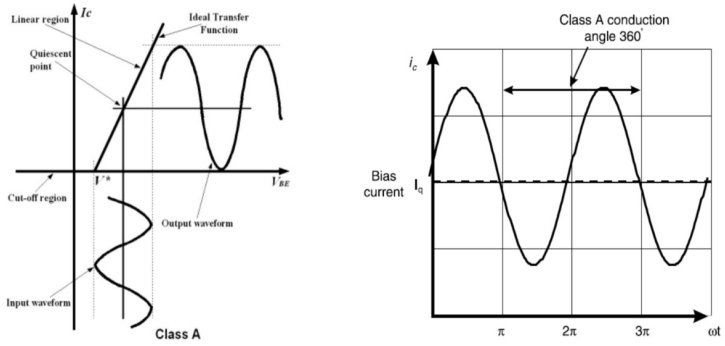


FIGURE 2.7: Class-A amplifier transfer characteristic and current/voltage waveform[13]

2.2.2 Class B

The Class-B PAs are also determined via the bias level, same as the Class-A power amplifier. The Q-point is lower than Class-A, where locate at the cutoff region. The input drive signal only has a half-cycle for the transistor conducts, as illustrated in Fig 2.8. Therefore, the Class-B PAs define approximately 180°, and the efficiency is better than Class-A PAs. However, the linearity performance decreases due to the higher-order harmonics generate. The resonator block is applied at the output terminal of the Class-B amplifier for the circuit design. The resonator block consists of the LC parallel circuit, which purpose is to give open conditions at the fundamental frequency and short-condition all frequency of above/low fundamental frequency. The other amplifier topology is the push-pull topology, which is usually applied to the Class-B amplifier. The circuit of the push-pull amplifier consists of two identical transistors T1 and T2[14]. The push-pull Class-B amplifier can provide the positive half cycle by T1 and the negative half cycle by T2. Therefore, compared to the single-ended Class-B amplifier, which only has a positive half cycle. The push-pull amplifier can decrease the distortion signal. Thus, the power dissipation will be lower. Therefore, the efficiency and output power are higher than the single-ended amplifier.

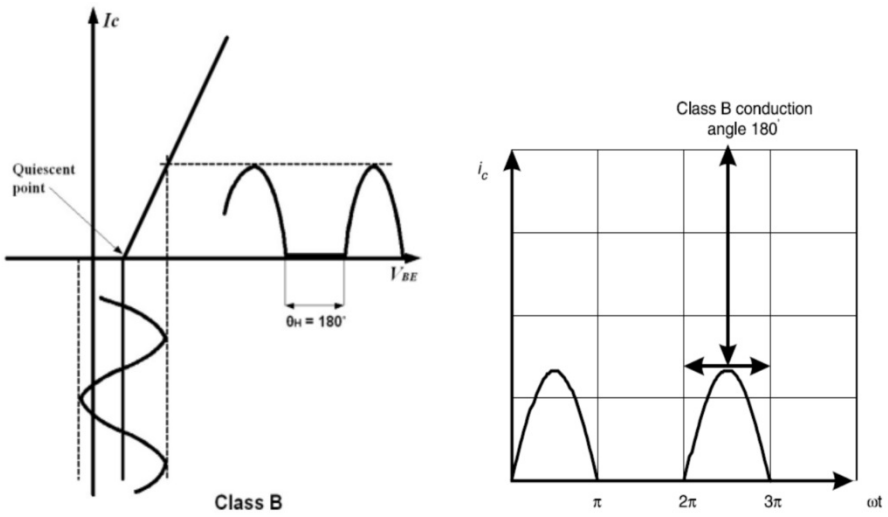


FIGURE 2.8: Class-B amplifier transfer characteristic and current/voltage waveform[13]

2.2.3 Class AB

The Class AB PAs are considered between Class-A and Class-B PAs in terms of efficiency and linearity. Fig.2.9 illustrates that the Q-point is between Class-A and Class-B, and the efficiency is lower than Class-B and better than Class-A PAs. The CCA is >180° and $\ll$ 360°, and the efficiency is between 50% and 78.5%. Actually, the Class-AB PAs is not a linear amplifier.

2.2.4 Class C

Fig 2.10 shows the Class-C PAs characteristics. It can be seen that the CCA is <180°, and the Q-point at the cut-off region is under ideal conditions. Thus, the linearity performance is poorest compared with other biasing PAs (A, B, AB). The distortion of the Class-C is high,

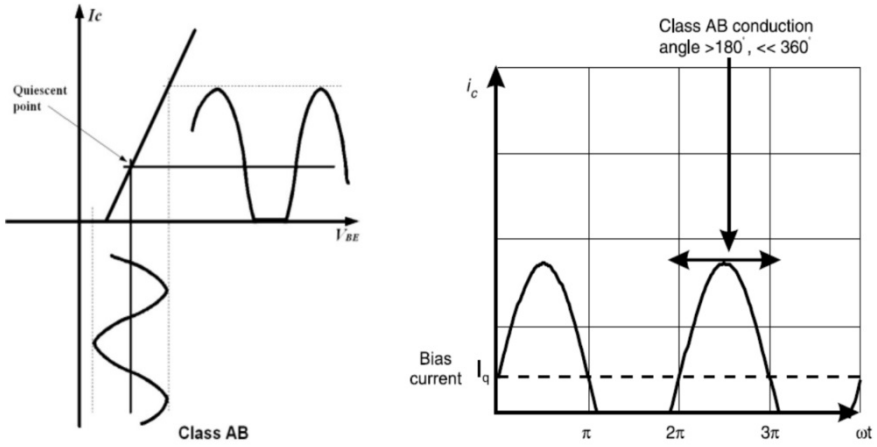


FIGURE 2.9: Class-AB amplifier transfer characteristic and current/voltage waveform[13]

and the tuned circuit is required as load in practice, the efficiency can reach 80% in RF application. However, the Class-C PAs has a large negative swing of the input drive, which coincides with the collector/drain output voltage peaks. Therefore, the worst condition of reverse breakdown will happen, and the leakage current has an important effect on the efficiency. For this reason. The Class- C PAs are not often considered in solid-state applications at higher RF and microwave frequencies[13].

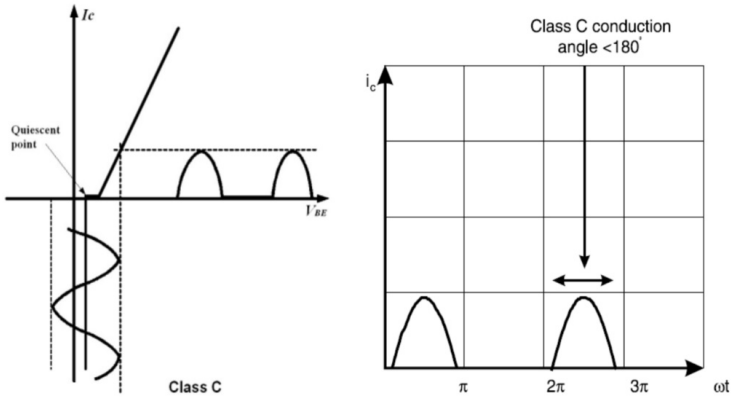


FIGURE 2.10: Class-C amplifier transfer characteristic and current/voltage waveforms[13]

A summary for the trans-characteristic of biasing PAs, which include the CCA, current/voltage waveform, Q-point of Class-A, B, AB, C, as illustrated all together in Fig 2.11 and made all comparison. The Q-point of Class-A is in the middle of the characteristic curve; it represents the Q-point as the center between saturation and cut-off region; the PAs are ON all-time with the output signal follow as the input signal. In Class-B, the Q-point is reaching the cut-off region, and the output signal only has a half-sine wave, and it contains even harmonics. The Q-point of Class-AB is between that of Class-A and Class-B, and the output signal is more than 50%. In Class-C, the Q-point is deeply located at the cut-off region and less than 50% of the output signal[13].

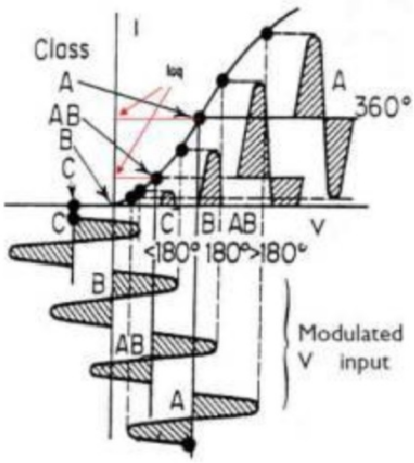


FIGURE 2.11: Biasing power amplifier trans-characteristics comparison[13]

2.2.5 Class F/Inverse Class F

The Class-F PAs is developed based on the Class-B topology. The basing of a quiescent point is close to Class-B PAs, and the CCA is 180°. The main difference between Class-F and Class-B is the open-condition is defined for the odd harmonic. The harmonics are generated since the switching characteristic of the active device. These harmonics are undesired for the biasing PAs. However, these harmonics are intentionally exploited to enhance the efficiency of PAs for Class-F amplifier. In theory, the efficiency of Class-F PAs can reach 100% under the ideal condition, which means the amplifier has no device power dissipation, and at the load port has no harmonics power is delivered. However, to realize the 100% efficiency of the amplifier, an infinite number of harmonics must be controlled perfectly. It is impractical during the actual design, because the parasitic influence cannot be totally eliminated.

Fig 2.12 shows the ideal drain voltage and current waveform of Class-F and Inverse Class-F PAs. The efficiency is 100% under the ideal condition, the waveform shape of voltage and current are perfect and the overlapping area is zero, which means the power has no dissipation during the switching. The drain side voltage and current waveform of the Inverse Class-F PAs are similar to the conventional Class-F, in which only the voltage and current shape exchange in Fig 2.12. The other details will be discussed later step by step. Because the Inverse Class-F is similar to Class-F PAs theory (only results or conditions exchange, such as waveform ect.), this section only focuses on introducing the Class-F topology. The Class-F voltage and current waveform are described by the general Equations 2.11 and 2.12, where the θ is the phase difference fundamental signal and harmonics.[5]

Voltage Waveforms:

$$V(t) = V_{dd} + V_1 \cos(\omega_0 t + \theta_1) + V_2 \cos(2\omega_0 t + \theta_2) + V_3 \cos(3\omega_0 t + \theta_3) + \cdots \tag{2.11}$$

Current Waveforms:

$$I(t) = I_{dd} + I_1 \cos(\omega_0 t + \theta_1) + I_2 \cos(2\omega_0 t + \theta_2) + I_3 \cos(3\omega_0 t + \theta_3) + \cdots \tag{2.12}$$

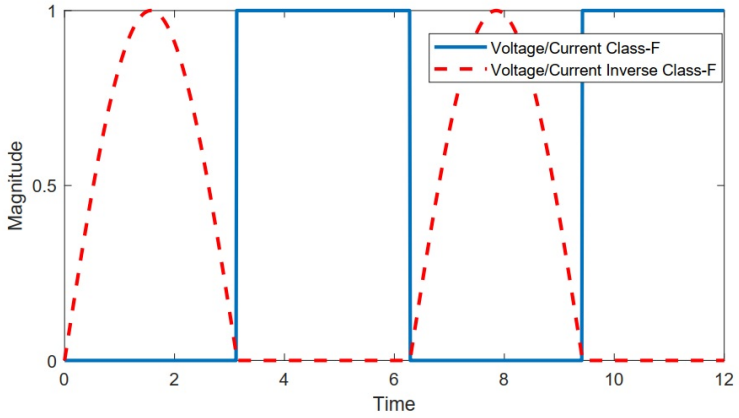


FIGURE 2.12: Ideal voltage waveform and current waveform

Fig 2.13 shows the drain current and voltage with the realistic parameters, which the purpose is to derive the relation current and voltage expression by mathematic approach. Fig 2.13 can easily be described through Equation 2.13 and Equation 2.14, and the knee voltage is assumed to be zero, $V_K = 0$.

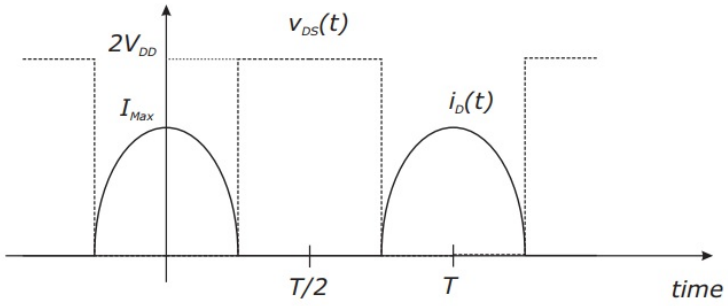


FIGURE 2.13: Ideal voltage waveform and current waveform assume for a Class-F power amplifier[5]

$$i_D(\theta) = \begin{cases} I_{max} \cdot \cos(\theta) & \text{if} -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 0 & \text{otherwise} \end{cases} \tag{2.13}$$

$$v_{DS}(\theta) = \begin{cases} 0 & \text{if} -\frac{\pi}{2} \leq \theta \leq \frac{\pi}{2} \\ 2 \cdot V_{DD} & \text{otherwise} \end{cases} \tag{2.14}$$

The results from Equation 2.13 and Equation 2.14 which the voltage and current waveform are not overlapping, which means the device dissipated power is approximately zero[5]. The purpose of this condition is to reach 100% efficiency. In the next step, to obtain the drain current and voltage with harmonics, the Fourier analysis can be exploited to get the coefficients of current and voltage, then substitution into the drain current and voltage ideal waveform equation.[5]

$$i_D(\theta) = \sum_{n=0}^{\infty} I_n \cdot \cos(n\theta) \tag{2.15}$$

$$I_n = \begin{cases} \frac{I_{max}}{\pi} & n = 0 \\ \frac{I_{max}}{2} & n = 1 \\ \frac{2 \cdot I_{max}}{\pi} \frac{(-1)^{\frac{n}{2}+1}}{n^2-1} & n, even \\ 0 & n, odd \end{cases} \tag{2.16}$$

$$v_{DS}(\theta) = \sum_{n=0}^{\infty} V_n \cdot \cos(n\theta) \tag{2.17}$$

$$V_n = \begin{cases} V_{DD} & n = 0 \\ -\frac{4 \cdot V_{DD}}{\pi} & n = 1 \\ 0 & n, even \\ \frac{4 \cdot V_{DD}}{\pi} \frac{(-1)^{\frac{n}{2}+1}}{n^2-1} & n, odd \end{cases} \tag{2.18}$$

As described in Equations 2.15 and 2.16, to shape a truncated half-sine current waveform at the drain, the odd harmonics must be eliminated and keep only even harmonics alive. Equation 2.17 and Equation 2.18 describe the voltage waveforms. In order to shape a perfect square waveform, the even harmonics must be eliminated and keep only odd harmonics alive. Theoretically, the above criteria must be met to eliminate the overlapping area between the current and voltage waveform, and the active device dissipated power is zero.[14]Fig 2.14 shows the effect of the odd and even harmonics on the voltage and current waveforms, which from $n = 1$ to $n = \infty$. According to these results, the waveforms are no overlapping between current and voltage until the number of harmonics is added to the infinity. The efficiency of the class-F power amplifier will reach 100%. Finally, Equation 2.19 is indicated the value of terminations, which can be derived as the ratio between the above Fourier components V_n and I_n.[5]

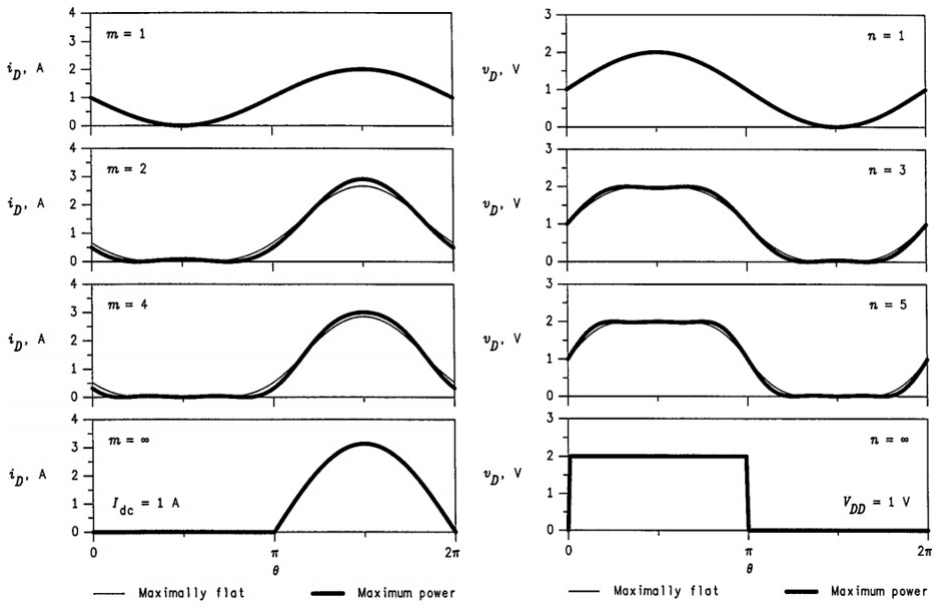


FIGURE 2.14: Current waveform(left) and Voltage waveform(right) with added difference number of harmonics in Class-F[12]

$$Z_n = \frac{V_n}{I_n} = \begin{cases} \frac{8}{\pi} \cdot \frac{V_{DD}}{I_{max}} & n = 1 \\ 0 & n, even \\ \infty & n, odd \end{cases} \tag{2.19}$$

Third-order Harmonic controlled architectures

Since the impedance matching network is difficult to control higher-order of harmonics(5th, 7th...), which means implemented infinity harmonics-controlled is impossible. Therefore, in order to implement the Class-F PAs in practice, the harmonics controlled architecture can be used, which be named third-order harmonic controlled (peaking) or third-order harmonic injection[14]. The topology of third-order harmonic controlled topology is presented in Fig 2.15 for the Class-F PAs. There are two resonators used between the drain output and the load. The purpose of the resonator L2||C2 gives the open condition at the third-order harmonic. Meanwhile, all other frequencies passing through the short circuit. Another resonator L1||C1 gives fundamental frequency passing to the load due to the resonator resonance at the fundamental frequency. Meanwhile, all other frequency signals are shorted to the ground. In the ideal conditions, this topology can be perfectly controlled harmonics power cannot reaching the load. Therefore, when the 50Ω is used at the load, the output voltage and current waveform after two resonators, which should be a purely sinusoidal waveform.

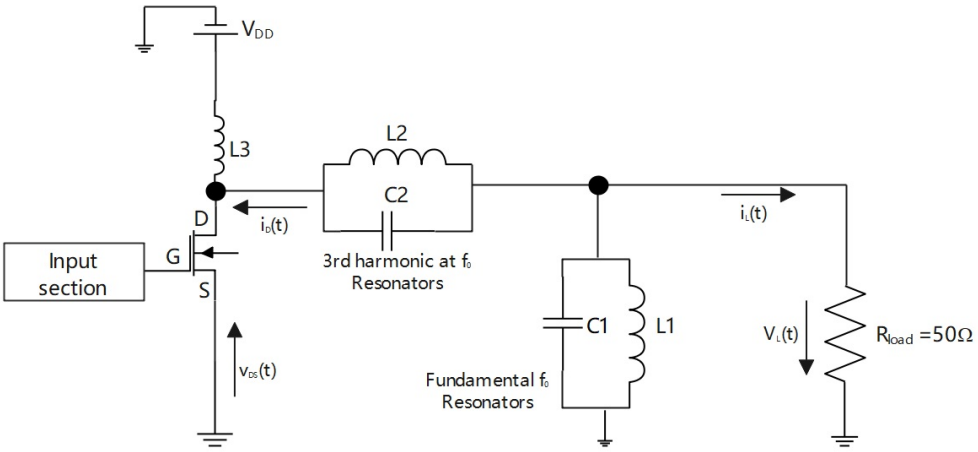


FIGURE 2.15: Third-harmonic controlled with lumped elements Class-F power amplifier

The advanced topology of the Class-F is presented in Fig 2.16, in which the quarter-wavelength transmission line at f_0 replaces the third-order harmonics controlled resonator. All odd harmonics have 180° phase shift in this topology, and all even harmonics phases will stay unchanged at the drain node (between the node of Drain and L3). Thus, the resonator L1||C1 is the same as before. However, this advanced topology is only available in theory. As the frequency increase, the quarter-wavelength transmission line becomes more inductive that the open-condition and short-condition cannot be executed perfectly. Therefore, the transmission line cannot be controlled with the harmonics of the infinity. Therefore, this thesis cannot use these two topologies to implement the Class-F/F^{-} output network directly. It should be more complex to obtain expect project goal.

The drain voltage and current waveforms at the third-order harmonic-controlled architecture for Class-F power amplifier is illustrated Fig 2.17, and the top figure illustrates the drain voltage square waveform which it is n1+n3. The below figure is half-sinusoids drain current waveform which it is n1+n2. The drain voltage and current waveforms shape are one of an approach to verify the performance of the class-F/F^{-} power amplifier.

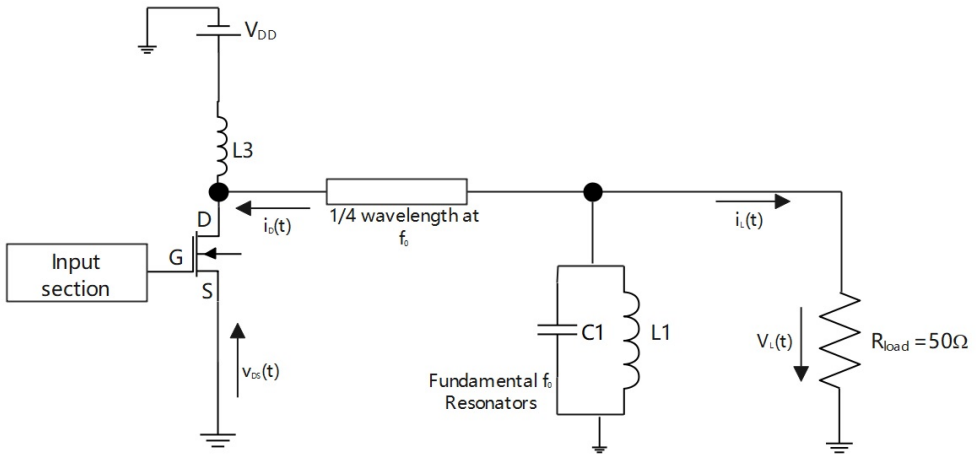


FIGURE 2.16: Third-harmonic controlled architecture with lumped elements and distributed elements Class-F power amplifier

2.2.6 Switching Mode Power Amplifiers

Class-D and Class-E are two types of non-linear amplifiers in the switching class. This section gives a brief description to introduce the switching PAs. Start from the Class-D PAs. Due to the active device working on the linear area will have many power consumption, so Class-D has better efficiency than linear amplifiers (Class A, B, AB) because the active device only works as a switch in Class-D topology. Class-D power amplifier mainly used for the audio system, and the active device (CMOS) cannot support the high-frequency application. Therefore, Mostly the Class-D topology is not considered to implement RF application in practice. Fig 2.18 shows the block diagram of a basic Class-D power amplifier.

Another switching amplifier is Class-E PAs. The basic working principle employs a single transistor as a switch. It gives an ON and OFF state for the circuit. In the FET structure active device. The drain voltage waveform results from the sum of the DC and RF currents charging the drain-shunt capacitance C_p parallel with transistor internal capacitance c_o[13]. When the transistor is ON state, the drain voltage from upper drop to zero and slop should also be zero in the ideal Class-E amplifier. The result of efficiency is 100%. Fig 2.19 gives the basic topology and the waveforms. The Class-E amplifier upper limit is decided the output capacitance required for the matching network at the output section, and the waveforms are presented in Fig 2.19. In order to obtain the optimum efficiency, the upper limit of the capacitance C_s should be required.

Compare Class-E and Class-F power amplifiers. The topologies of the amplifier are both non-linear types in the switching class. However, the Class-E amplifier has some disadvantages that should be concerned. Firstly, the Class-E is difficult to design in the high-frequency application since the C_p has a large output capacitance. Therefore, the operating frequency and the capability of output power at high frequency are limited. On the other hand, the

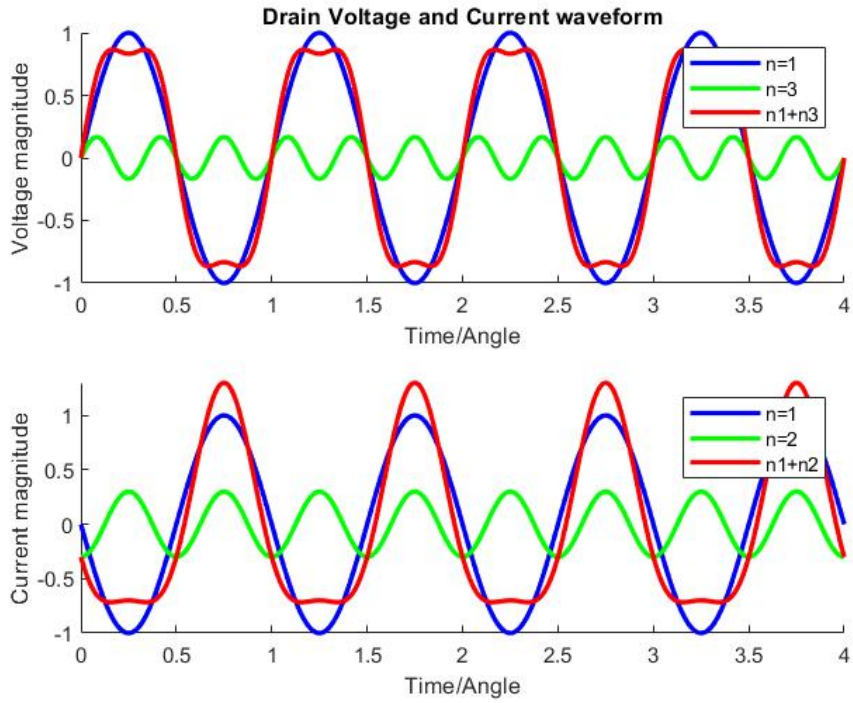


FIGURE 2.17: Third-order harmonic controlled architecture drain voltage and current waveforms for Class-F power amplifier

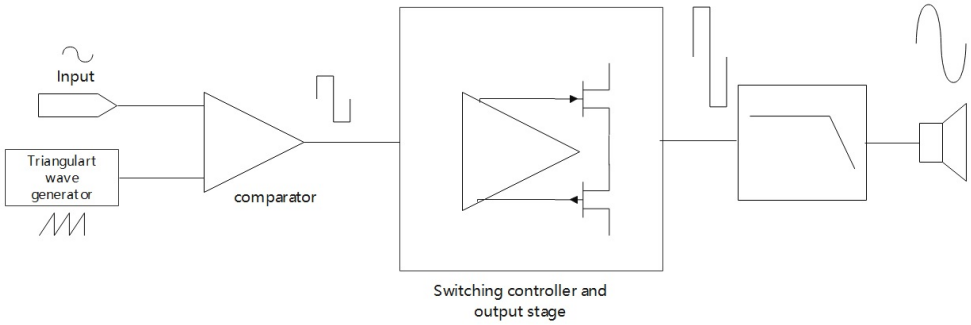


FIGURE 2.18: Block diagram of Class-D power amplifier

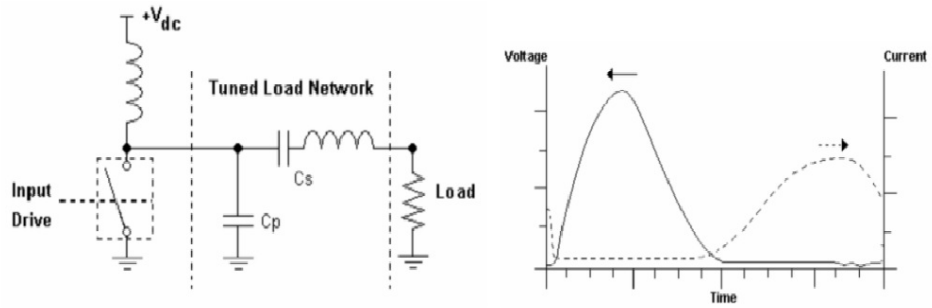


FIGURE 2.19: Circuit diagram of Class-E power amplifier and the general waveform[13]

general MOS/CMOS active device cannot support the high-frequency application. Therefore, the GaN should be used instead of MOS/CMOS device for implementation. However, the knee voltage of the GaN device is relatively high to turn on the device channel. Thus, the ON state required voltage is also high, which approximately 5V for the general GaN transistor. Because of the above disadvantage, the high-efficiency Class-E amplifier is implantation at the high frequency is difficult.

2.2.7 Class J Power Amplifier

Since the bandwidth is required at least 400MHz. Therefore, the power amplifier must be broadband while maintaining high efficiency, which means the type of the amplifier must be the broadband amplifier. To achieved the broadband amplifier, The continuous mode is an excellent topology to do the amplifier design. Therefore, the "father" of the continuous mode, the Class-J amplifier must be introduced in order to understanding the continuous mode easily.

Class-J amplifier was the first new model using to the combination of fundamental and harmonic impedance to support a wider bandwidth in wireless communication, and presented by Prof. Steven Cripps[3]. The Class-J amplifier theory can be discussed starting from the Class-B amplifier condition. In the conventional Class-B mode, the second-order harmonic provides a perfect short-circuit condition at the generator plane (I_{gen})[1]. The purpose is to reach the maximum efficiency while presenting the optimum fundamental impedance.[3] However, in the package plane (I_{pack}), the second-order harmonic and the fundamental impedance are often to be away from the ideal position on the Smith Chart due to the parasitic elements, resulting in the performance of the power amplifier is significantly decreased. In the Class-J mode. The intrinsic parasitic capacitor C_{ds} can provides the short-circuit condition for the high order harmonics. Once the Class-B amplifier is achieved, the Class-J mode is presented by introducing second harmonic reactance while also presenting reactance at the fundamental impedance.[3]. Due to the relation between the fundamental impedance and the second-order harmonic reactance is inverse, which means the negative second-order harmonic accompanies the positive fundamental impedance. The fundamental impedance and second harmonic are presented as Equation 2.20. R_L is the load, and the third harmonic is considered the short-circuit(equal zero)[3].

$$Z_n = \begin{cases} Z_{fund} = R_L + j \cdot R_L \\ Z_{2fund} = 0 - j \cdot \frac{3\pi}{8} \cdot R_L \\ Z_{3fund} = short - circuit \end{cases} \tag{2.20}$$

Fig 2.20 shows the results of voltage and current waveforms. The current waveform is the half-wave sinusoidal, it is the same as with Class-B amplifier. However, there are approximately half-wave sinusoidal voltage waveforms with 90° phase overlaps between the two and high peak voltage due to the fundamental and second reactive components[3]. Fig 2.21 is illustrated the locus of fundamental impedance and second-order harmonic on the Smith Chart, the locus from Class-B transform to Class-J. According to Equation 2.20, Due to the imaginary part is inserted in the impedance equations that the impedance is not constant anymore.

[1] The details of generator and package plane will be discussed in next chapter.

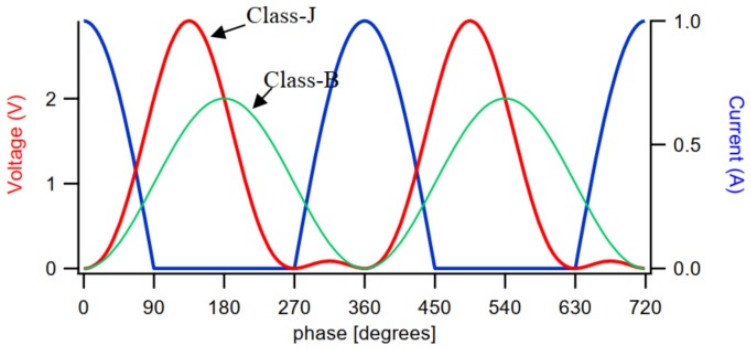


FIGURE 2.20: Class-B and Class-J voltage and current waveforms[3]

Moreover, if the locus of coefficients is inserted to the impedance Equation 2.20, the impedances (fundamental and harmonics) are no longer a single "point" on the Smith Chart. In other words, the fundamental impedance Z_{fund}, and second-order harmonic Z_{2fund} become variable value, it is the critical property to distinguish between Conventional mode and Continuous mode amplifier. This variable impedances mode is called the Continuous Mode Power Amplifier. This amplifier mode can maintain high-efficiency while the wider bandwidth, which is means the power amplifier can be designed broadband. the broadband amplifier is an important topic in the modern wireless communication system. In the following chapters, the continuous mode will be discussed in detail because this technology is the core content of this thesis.

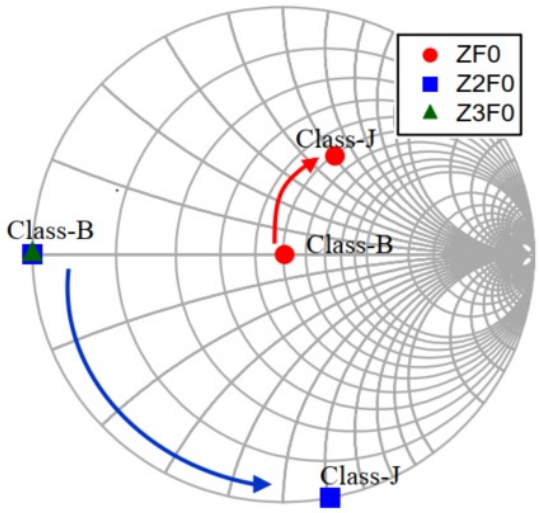


FIGURE 2.21: Class-B and Class-J first two impedances[3]

2.3 Active Device for High-Frequency Power Application

Fig 2.22 illustrates the family tree of the active device in the current market. Due to the power amplifier operating frequency working at L-band, the standard active device is not considered for implementation in this thesis. Therefore. There are three choices of the active devices: LDMOS, HBT, and HEMT. These power transistors are mainly used in RF/Microwave

applications

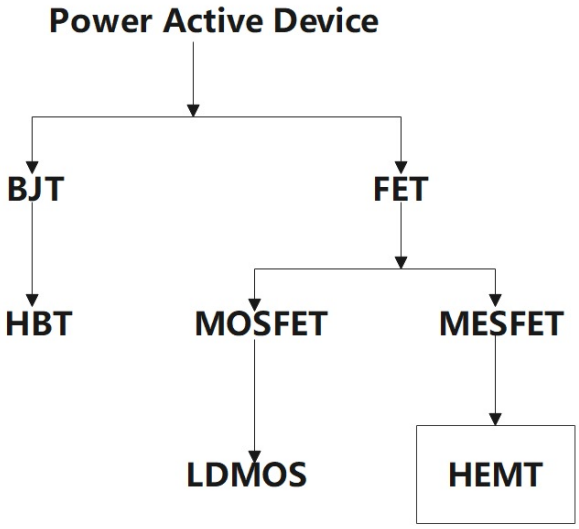


FIGURE 2.22: Family tree of active device

LDMOS (Laterally-Diffused Metal-Oxide Semiconductor)

LDMOS is an enhanced conventional MOSFET structure. It is fabricated on an epitaxial layer with a highly doped silicon substrate. The behaviour of LDMOS is similar to the standard MOS structure, and it has excellent compatibility with the CMOS structure, which means it is easier to build an integrated system for the application. In a linear amplifier, the LDMOS can provide the higher gain and better efficiency[16]. Due to it is base on the MOSFET technology, the thermal influence and the noise are low and have better power consumption. However, as the wireless system rapidly increases, especially 5G technology, the LDMOS cannot provide higher operating frequency and wider bandwidth in future wireless communication.

HBT (Heterojunction Bipolar Transistor)

The HBT represents the improvement of the conventional BJT structure due to the exploitation of heterostructure junction. The materials of heterostructure are compound semiconductor, such as GaAs, SiGe, and InP. Compared with conventional BJT, the bandgap between the emitter and base result in the common-emitter gain is higher[5]. The sheet resistance at the base is lower than conventional BJT, that the operating frequency is higher, from tens of Hertz to hundreds of Giga Hertz. Moreover, the parasitic influence will be reduced because of the semi-insulating substrate and the high electron mobility.[5]

Due to the HBT is base on the BJT structure, the main disadvantage is similar to the conventional BJT structure. The threshold voltage is higher and exists the base current, which means the power consumption is higher. On the other hand, the current density is larger result in the thermal influence that leads to the device performance will decrease, even device disable totally.

HEMT (High Electron Mobility Transistor)

The HEMT structure, which belongs to the FET class, compared with the conventional FET, the HEMT channel is used as a dope region between the drain and the source, and

the bandgaps are different due to the two materials are used. Therefore, the HEMT is the heterostructure FET. The HEMT is selected as the active device to design power amplifiers for this thesis, as indicated in Fig 2.22.

In recent years. The third generation GaN material has been widely implemented for HEMT devices. The previous generation GaAs material is slowly replaced in the future. The GaN is a binary III/V direct bandgap semiconductor, and the substrate is Si/SiC. Compared with the GaAs material, the advantages of GaN/SiC, which have a wider bandgap, higher breakdown voltage, higher power density, higher operating frequency, and higher thermal conductivity. For the RF power amplifier application, the operating frequency of GaN/SiC HEMT can reach tens of Giga Hertz or even higher. The efficiency and bandwidth will have significant improvement when using GaN/SiC HEMT. It is the best choice for the broadband RF power amplifier and working at ultra-high frequency area. Fig 2.23 shows the output power and operating frequency in different compounds.

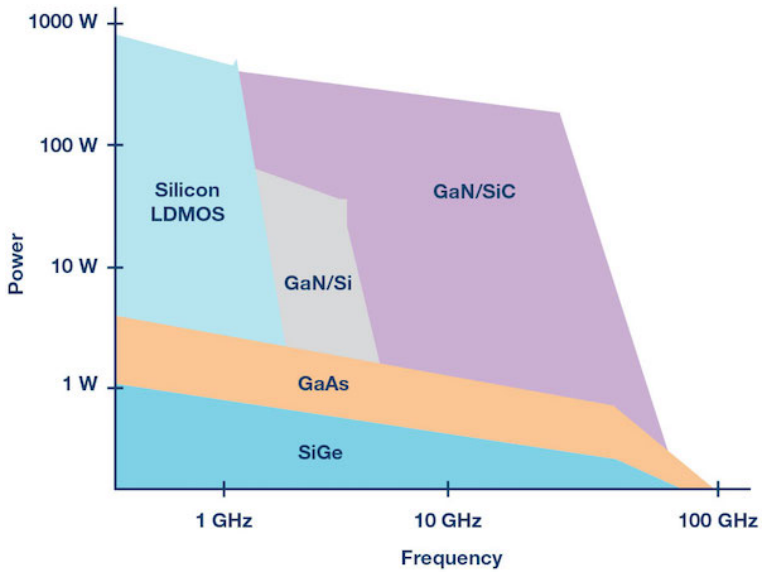


FIGURE 2.23: The output power and frequency property comparison in different compounds[2]

2.4 Power Back-off and Efficiency Enhancement

Today's communication systems use very complicated modulation methods to fully utilize the spectrum, such as the 64-QAM digital modulation. The messages are contained in both the phase and envelop amplitude of the modulation signal. Therefore, the linearity performance becomes significant of the power amplifier. Otherwise, the message binary codes position will shift on the output constellation, which means the output power signal is distortion, and the original input messages (power signal) cannot be identified at the output terminal. Therefore, the power amplifier must work in the saturation output power of several dB back to avoid nonlinear signal loss[8]. For example: A Class-A power amplifier backed off with respect to the 1dB compression point to increase linearity, which reduces IMPs. Another example is when the amplifier is backed off with respect to the optimum efficiency condition due to the slowly varying average input power being decreased. Typically,

the power amplifier operates with a given back-off concerning the reference condition when the input power is reduced by 3dB to 10dB for the reference input power.

However, the relation between linearity and efficiency is a trade-off. The back-off efficiency is certainly lower than the original efficiency of the amplifier. The conventional power amplifier leads to a good solution only near the maximum rated power. Thus, the efficiency will drop sharply if the power back-off. Therefore, the power amplifier must optimize efficiency after power back-off, which is called the efficiency enhancement method. The current method includes Envelop Elimination and Restoration (EER) method, Linear Amplification through Nonlinear Components (LINC) method, and the Doherty Amplifier. The Doherty Amplifier is the most useful approach to increase efficiency, which the two-path amplifier's topology can increase efficiency and low cost.

Doherty Amplifier

As we previously discussed. The excellent power amplifier must be taken into account both efficiency and linearity, even this condition is trade-off. Therefore, there are several methods to optimize this condition for the amplifier. The Doherty amplifier is an excellent topology to satisfied this condition. Fig 2.24 shows the fundamental Doherty amplifier structure, as can be seen. The amplifier contains two parts: One part is the Main amplifier. Another part is the Peak amplifier. The Main amplifier bias at Class-AB and the Peak amplifier bias at Class-C in general design. The working principle is: The Main amplifier works all the time, and the Peak amplifier does not work until it reaches the set peak value. The quarter-wavelength line after the Main amplifier is impedance transform, which aims to reduce the apparent impedance of the Main amplifier when the Peak amplifier is working. Therefore. The active load will be lower when the Peak amplifier is working and the current of the Main amplifier will be larger. Moreover, the quarter-wavelength line also should be inserted before the Peak amplifier to maintain the two paths are balanced.

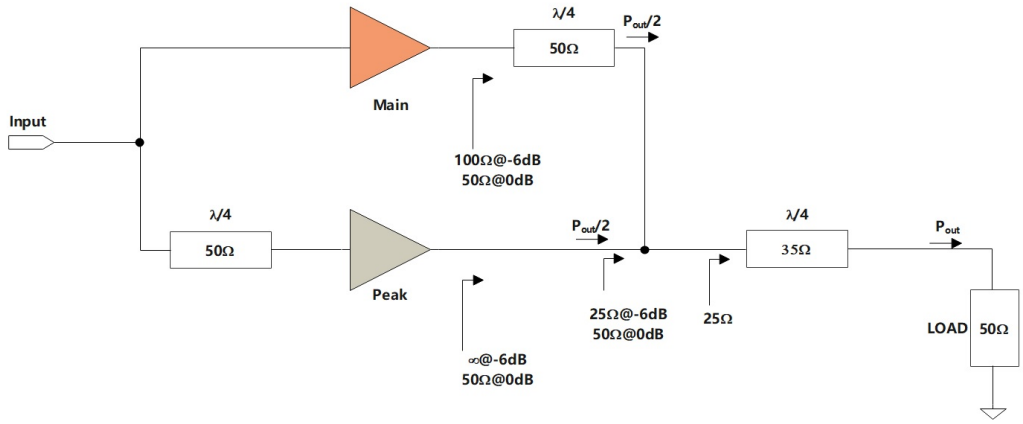


FIGURE 2.24: Doherty amplifier structure

The working principle of the Doherty amplifier contains three-phase, as shown in Fig 2.24. Assume the back-off power is minus 6dB. **Phase one:** The bias point at Class-C or Class-B of the Peak amplifier. The input voltage signal is low that it does not enough to turn on the Peak amplifier. Thus the Peak amplifier path is open. The Main amplifier equivalent load is 100Ω due to the quarter-wavelength line. The load voltage will increase that the Main amplifier enters the pre-saturation state. As a result, the efficiency of the amplifier is an improvement.

Phase two: When the input voltage signal is increasing, the Peak amplifier will be turned on. The **Active Load Modulation** behavior is activated. The equivalent load impedance starts to reduce from 100Ω to 50Ω of the Main amplifier. The voltage of the Main amplifier is maintained pre-saturated by the Peak amplifier. Meanwhile, the load of the Peak amplifier changes from the open state to 50Ω.

Phase three: As the input voltage continues increasing. The current of the Main amplifier and the Peak amplifier are both rising. The voltage of the Main amplifier will not change and maintain the high efficiency in the ideal condition. Meanwhile, the load of the Main amplifier continues decreasing, and output power continues increasing. When the Peak amplifier reaches saturation state, the Main and Peak amplifier current reaches the maximum. Finally, the equivalent loads of the Main and the Peak amplifiers are both 50Ω, and the output power is maximum.

Chapter 3

Initial Design for Power Amplifier

3.1 Active Device Study

The GaN HEMT active device was selected in this thesis due to its excellent operating frequency and wide bandwidth. Prior to designing the power amplifier, there are some properties of the active device should be determined under the Class-F/Inverse Class-F condition, such as the DC biasing, Stability, Gain, Optimum load and the Equivalent circuit model. These properties form the basic knowledge that should be made clear before beginning the amplifier design. Therefore, these properties are discussed in this chapter, detailing how they are determined during the amplifier design step by step.

3.1.1 Device DC Analysis

The active device CGH40010F non-linear model transistor was selected to design the circuit and fabricate the power amplifier. This transistor is manufactured by the Cree Company. It is an unmatched, GaN high electron mobility transistor (HEMT). Moreover, it offers a general-purpose, broadband solution to a variety of RF/Microwave applications. The physical model and ADS symbols are presented in Fig 3.1. The pin numbers (Pin number 1,2, and 3) of the ADS symbol represent the Gate, Drain, and Source, respectively. Moreover "t" and "rth" represent the device temperature and thermal resistance, respectively.

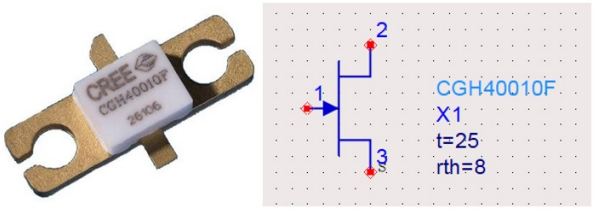


FIGURE 3.1: CGH40010F physical model and ADS symbol

First, it is necessary to determine the Q-point (Quiescent point) under the Class-F/F^{-} amplifier working condition. The previous chapters discuss the Q-points with different amplifiers classes. Therefore, the Q-point of the Class-F/F^{-} working condition can be applied here to design the power amplifier. The Q-points with device output characteristics are presented in Fig 3.2. Class-F/F^{-} can generate significant harmonics because the Q-point is close to the cut-off region, and the Q-point position is slightly higher than it is in Class-B, in a shallow Class-AB. Therefore, the drain current waveform is akin to that of Class-B that is a rectified half-sinusoid waveform. Moreover, the drain voltage waveform is a square

wave resulting from the $3f_0$ harmonic tuning, unlike a Class-B amplifier. This is the third-order harmonic-controlled architecture for Class-F/F^{-}, the theory of harmonics-controlled architecture is discussed in the previous chapter.

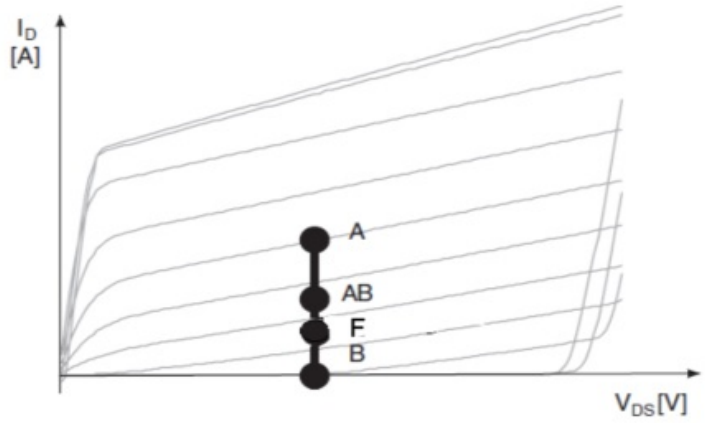


FIGURE 3.2: Q-points with output characteristics[5]

Fig.3.3 illustrates the I-V characteristics of CGH40010F with different gate bias voltage. This figure was plotted using ADS software. The drain voltage is 28V according to the device data-sheet suggestion (saturation region). The gate voltages are illustrated from 1V to -3V. Since the transistor pinch-off voltage is approximately -3V, the gate voltages can be selected from -2.5V to -3V. Therefore, a gate voltage of -2.8V for the desired class of operation is the proper biasing point to design the amplifiers.

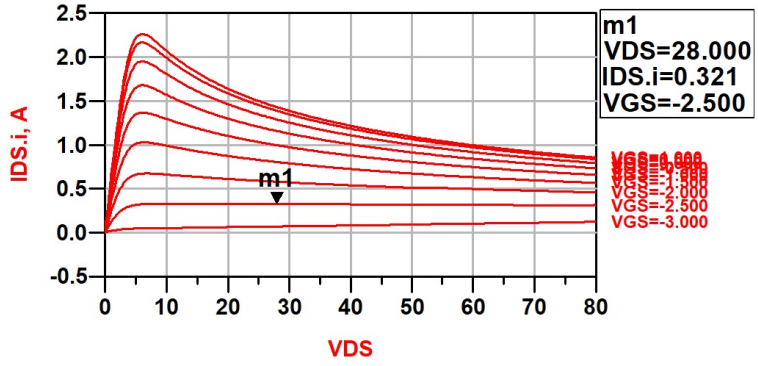


FIGURE 3.3: I-V characteristics of CGH40010F with different gate and drain bias voltages

Optimum load impedance

Since the load-pull technique was not applied to determine the optimum impedance (Z_{in} ,Z_{out}) of the device, this thesis uses the optimum load-line technique instead of load-pull to design the amplifiers. Therefore, the optimum resistance of Class-F/F^{-} should be calculated using the optimum load-line equation. The optimum load-line equation is based on Equation 2.19 with the first-harmonic impedance condition, and this equation is transformed into the new model. The new model of Equation 3.1 is as follow:

$$R_{opt} = Z_{n=1} = \frac{8}{\pi} \cdot \frac{V_{DD} - V_{sat}}{I_{max}} \tag{3.1}$$

R_{opt} is the optimum resistance, equals to first harmonic impedance. $I_{max} = I_{dss} = 1.5A$ was obtained from the transistor device specification(data-sheet). Furthermore, V_{sat} is the knee voltage which is approximately 3V, as shown in Fig 3.3. The purpose of subtracting V_{sat} from V_{DD} is to express the drain voltage swing precisely. In fact, to avoid distorting the drain current pulse, the drain voltage should not swing below the knee or saturation voltage[1]. Finally, the optimum resistance is 42Ω, which can be rounded to $R_{opt} = 40\Omega$ in designing the amplifiers.

3.1.2 Small-Signal Characteristics

The small-signal equivalent circuit represent the device behaviour under the small-signal condition. It is described by0 its frequency-dependent small-signal parameters, such as scattering, admittance, or impedance parameters[8]. The example of the HEMT small-signal circuit, as presented in Fig 3.4, is a general MESFET small-signal model, but it can also represent all FET families. The small-signal equivalent circuit can de-embedded the intrinsic from the extrinsic parameters. The color of the gray region indicates the intrinsic part, which contains C_{GS}, C_{GD}, C_{DS}, τ, R_I, R_{DS}, and g_m, while the extrinsic parameters are shown in the figure, and are L_G, R_G, L_D, R_D, L_S, and R_S. Finally, port G, D, and S are connected to the device package.

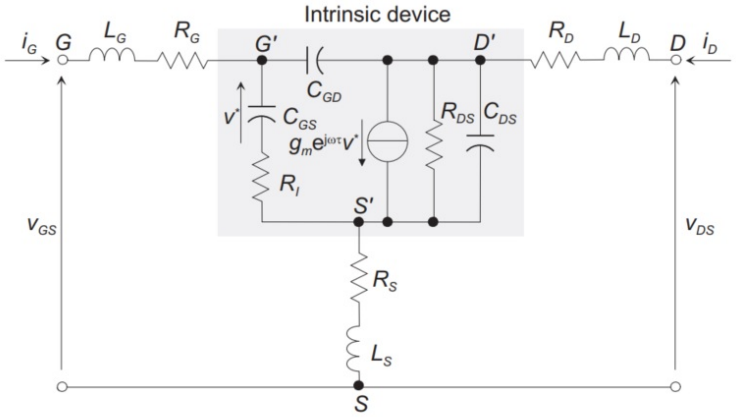


FIGURE 3.4: Small-signal equivalent circuit[8]

The general method used to determine these parameters is to exploit the “cold” and the “hot” FET measurements for the extraction of the parasitic. The "cold" measurement can directly obtain the extrinsic parameters, while the "hot" measurement can obtain the intrinsic parameters. However, for the aim of this thesis it was not necessary to determine all these parameters. Focusing on the design of a power amplifier, particularly one based on a Class of operations defined at the current generator (intrinsic) plane, the key aspect is to extract a linear model for the output (drain) parasitic, which has been achieved using ADS software to simplify the calculation procedure. This is discussed in the following section. Two important figures of merit for the device are: the cut-off frequency f_T and the maximum frequency of oscillations f_{max}.

The following frequency parameter is the maximum oscillation frequency f_{max}, which represents the frequency when the maximum available power gain (MAG) is the unity(MAG = 1)[8]. If $f > f_{max}$, the active device becomes a passive component and cannot provide gain. Therefore, f_{max} is an important parameter that influence the gain of the amplifier and its frequency operating range.

The consequence is that at frequencies beyond f_{max} ($f > f_{max}$), the device cannot operate, the reason for this is discussed in the above paragraph. Therefore, the operating frequency should be lower or much lower than cut-off frequency f_T [8].

3.1.3 Stability Circuit and Gain

Since the power amplifier operates at a high frequency, during the power transfer, significant parasitic effects are cause load and source impedance to not match perfectly. Moreover, due to the feedback mechanisms in the transistor, the output signals can be rerouted at the input side, and if the input and feedback signals have a specific phase relation, the oscillation phenomenon may occur. Therefore, stability analysis for the transistor must be performed before designing the input matching network. A typical requirement, though not strictly necessary, but still useful to ensure safe operation even in the case of unexpected conditions (e.g. source/load terminations that differ from the expected ones), is that the amplifier should be stable across all frequencies as well as all source and load impedances[6].

The source and load impedances are represented in the Γ_S and the Γ_L ($0 < \Gamma < 1$) planes, where they are mapped by conformal mappings. A few different approaches can be used to determine whether a transistor is unconditionally stable, such as the Rollet factor K, μ_1 and μ_2, B_1. One of the most straightforward methods is to observe the factor K and the determinant of the S matrix[8]. The stability factor K is defined as Equation 3.7. Equation 3.8 is the supplementary equation for Δ_s:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta_s|^2}{2\,|S_{12}S_{21}|} \tag{3.2}$$

$$\Delta_s = S_{11}S_{22} - S_{12}S_{21} \tag{3.3}$$

The K-factor is based on the S-parameters to design the stability circuit, and this equation contains two parameters as criteria. The following is presented to provide a better understanding of the equations that the S-matrix:

- S_{11} : Input port voltage reflection coefficient.
- S_{21} : Reverse voltage gain.
- S_{12} : Forward voltage gain.
- S_{22} : Output port voltage reflection coefficient.

To maintain the unconditionally stable of the system, the following condition should be satisfied: **K >1 and** $|\Delta_s|$ **<1**. With the amplifier stability circuit design, the K-factor should be considered at a sufficiently low frequency, well below the operating bandwidth, and in general around the frequencies at which the off-chip circuit elements begin to have an influence, up to sufficiently high frequencies, typically where the device is unable to provide significant gain. The K-factor can likewise be related to the maximum available gain(MAG). Equation

3.4 represents the MAG as it relates to the K-factor. The MAG is defined for only two-port networks and must be greater than one. Otherwise, the square root becomes negative, or $(K^2 - 1)$ is imaginary.

$$MAG = (\frac{|S_{21}|}{|S_{12}|}) \cdot (K - \sqrt{K^2 - 1}) \tag{3.4}$$

Fig 3.5 reveals that the transistor is unconditionally stable from around 4.5GHz to 9GHz in Class-F gate biasing(-2.8V), and the transistor is again unconditionally stable after 18GHz. However, as a requirement of this thesis, the operating frequency of interest is around 1.75GHz. Therefore, a stability circuit is needed to provide stability across the low-frequency region. The same results can likewise be indicated by the stable circle with the Smith Chart as presented in Fig 3.6. Here, the figure displays the source and load stability circles of the active device, which is potentially unstable at the frequencies for which the circle partially or completely includes the inside of the Smith chart (in which case, the intersection between the Smith chart and the stability circle identifies the unstable terminations).

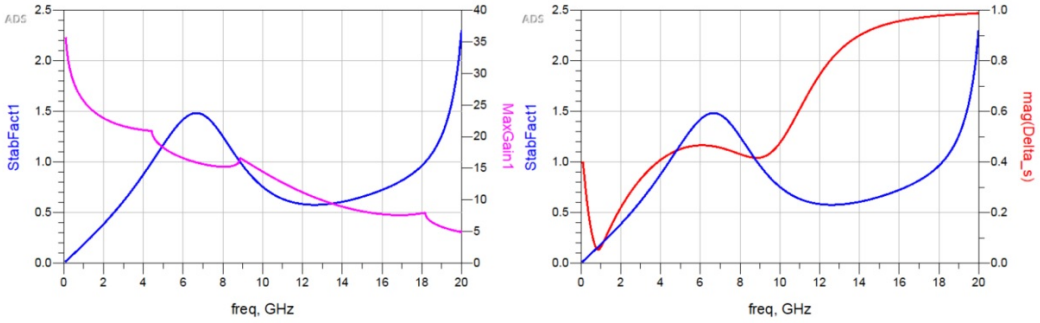


FIGURE 3.5: Stability/Δ_s and MAG with Class-F gate biasing

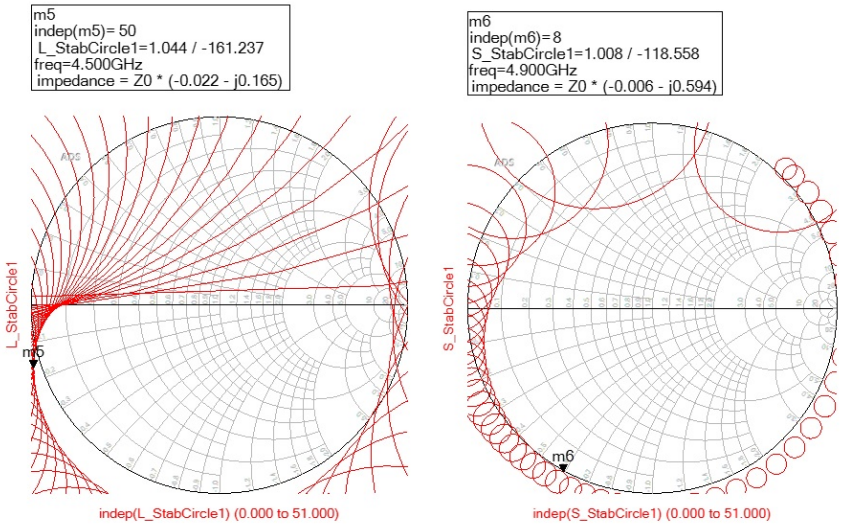


FIGURE 3.6: Stability circle with source and load

To ensure the active device is unconditionally stable at low-frequencies, a stabilization circuit is inserted before the gate of the device. Fig 3.7 displays the stability circuit with the ideal components and is inserted before the gate of the device. This circuit is based on

the frequency-dependent approach that uses resistors, inductors, and capacitors to provide stabilization. The resistor (R_{in}) is incorporated into a gate bias network, while the capacitor (C_{in}) is placed across the series stabilization resistor(R_{in}). The values of the capacitor and resistor can be tuned to increase the stable factor while decreasing the available gain at the low-frequencies. The tradeoff between the stability and the maximum available gain in the operating frequency range, the series inductor(L_2) and the resistor (R_1) are inserted before the parallel stability circuit. The purpose of the inductor(L_2) and resistor (R_1) is to increase the maximum available gain (MAG) without the stable factor decreasing proportionally, and to keep the MAG smooth and at its maximum. The results of the simulation are provide in Fig 3.8. Since the operating frequency is 1.75GHz and the bandwidth is $\geq$ 400MHz, the bandwidth of interest is around 1.5GHz to 2GHz. Therefore, enforcing unconditional stability from DC to 8GHz is sufficient, and the MAG is smooth around 22dB within the bandwidth(1.5GHz – 2GHz).

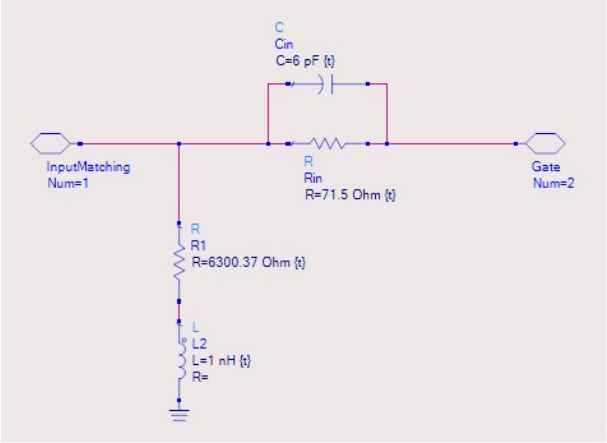


FIGURE 3.7: Schematic of the stability circuit with ideal components

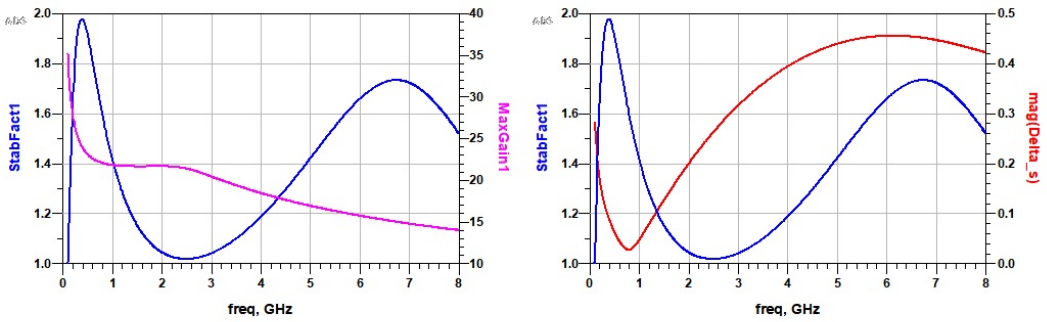


FIGURE 3.8: Stability/Δ_s and MAG with ideal components at Class-F gate biasing

The subsequent is to transfer the ideal components to the microstrip and the real passive components. The capacitor (R_{in}) was selected as an SMD component from the MuRata manufacturer. The resistors were likewise SMD components and have no other special requirements. The inductor is sufficiently small to be implemented by means of a piece of narrow microstrip line, which is more easily incorporated into the gate biasing networks. The circuit is presented in the Fig 3.9. This network is discussed with the bias network in the Section 3.3.

The final results of the stability circuit, which used microstrip lines and components are illustrated in Fig 3.10. The stability factor (stabFact1) decreases before 2GHz, but it is still greater than one from DC to 8GHz. Meanwhile, the MAG decreases to around 18dB within the bandwidth(1.5GHz - 2GHz). The attenuation of the MAG cannot be completely compensated due to the influence of the parasitic elements when the lossy microstrip lines are used in the network. The only approach to reduce this influence is to tune the parameters of the components and the microstrip lines for the stability circuit by ADS, and optimize the input section(input matching and stability circuit) during the input matching design to compensate for this influence. In other words, it is necessary to ensure the reflection coefficient(S_{11}) is as low as possible in the operating band. Therefore, these results are acceptable for the amplifier design.

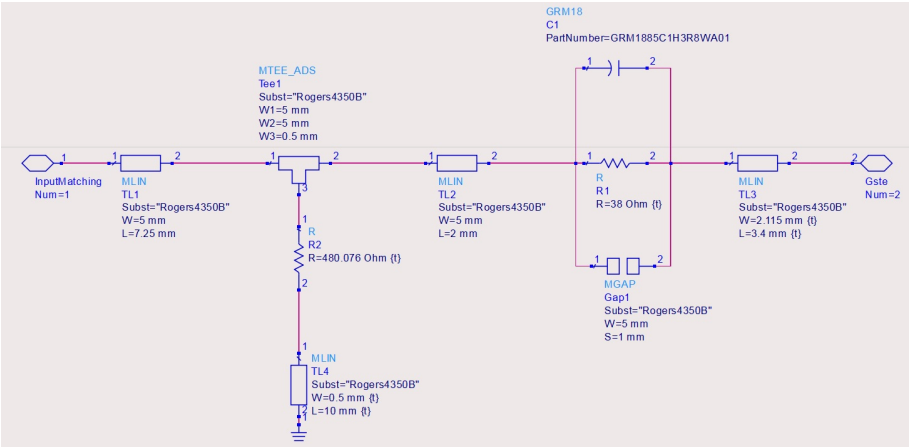


FIGURE 3.9: Schematic circuit of the stability in practice

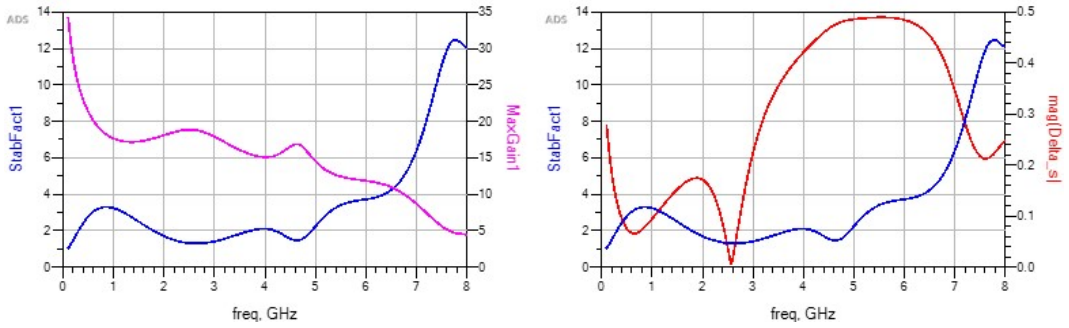


FIGURE 3.10: Stability/Δ_s and MAG in practice at Class-F gate biasing

3.1.4 Output Equivalent Model

Section 3.1.2 briefly introduces the intrinsic and extrinsic elements of the small signal equivalent circuit of the transistor. However, as anticipated, for the aim of this work, the extraction of the full model was not necessary and has not been entirely performed. For the design of the power amplifier, and particularly, the output matching network (OMN), it is often useful to extract a simplified (linear) output LC model, made of a shunt C_{out} and a series L_{out}, as depicted in Fig 3.4. These should represent the behaviour of the output of the device in the operating bandwidth, in order to allow for an easier design and optimization of the OMN, and they are extracted in a "cold" FET condition.

Suppose the device being applied the lower gate voltage causes the channel of the HEMT device to not be formed, such as the gate voltage beings lower than the threshold voltage, at this moment, the capacitance of C_{gd} does not influence the input and output of the device, and g_m does not exist in the current generator. Therefore, the major parasitic elements include only C_{ds}, R_{ds}, and L_D for the output(drain) side, and the input and output of the device can be analyzed separately. This is an easier approach to designing the output matching circuit without the input and other intrinsic and extrinsic parasitic elements having an influence. Fig 3.11 illustrates output equivalent model with the above condition, This model does not contain g_m and C_{gd} as indicated in the figure, and the model can be used to design the output matching network independently.

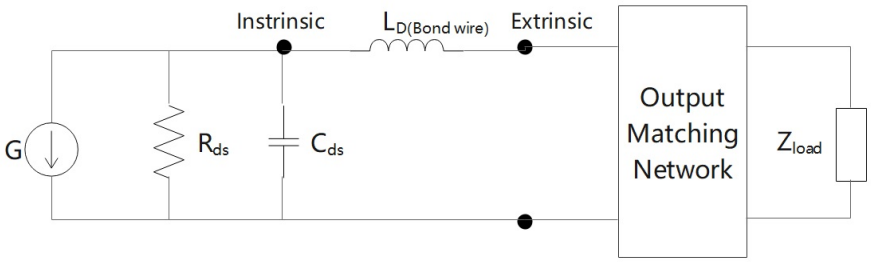


FIGURE 3.11: Output equivalent model

For the input matching network (IMN) design, the extraction of an equivalent input circuit is not so useful, since the stabilization circuit already transforms the input impedance of the device. The IMN will simply be designed by enforcing power matching in the operating bandwidth, thus maximizing the gain and consequently the power-added efficiency.

The approach for determining the parasitic elements for the output section is presented in Fig 3.12. The main idea is to let $S_{22} = S_{33}$ via ADS tuning. S_{22} and S_{33} are both the output port voltage reflection coefficient, the S_{22} is simulated by general small-signal analysis with CGH40010F, and port two is 50Ω. To ensure the intrinsic parasitic elements are the same as in Fig 3.12, the gate biasing is equal to -4V, which means it is below the threshold voltage and the channel cannot be formed as discussed previously. Therefore, the parasitic elements at the output side, which survival only R_{ds}, C_{ds}, and L_D (the names of the components are L_{out}, C_{out}, and R_{out} in ADS), can be built with port three, which is likewise 50Ω. This approach appears to extract the intrinsic parasitic elements from the active device and determine the value of these intrinsic parasitic elements via tuning.

Fig 3.13 is the simulation result of S_{33} and S_{22}. The impedance of S_{22} is close to that of S_{33}, and the bandwidth ranges from 1.5GHz to 2GHz as the requirement. These parasitic elements are extracted from the active device and build the output part to be analyzed and designed for the output matching network. At this point, the parasitic elements can be determined:

- $L_{out} = L_D = 1.2\text{nH}$
- $C_{out} = C_{ds} = 1.382\text{pF}$
- $R_{out} = R_{ds} = 8800.012\Omega$

Initially, the values of C_{out} and L_{out} can be tuned manually. To obtain more precise result, one can define a quantity as the difference between S_{22} and S_{33} and provide it as a goal for

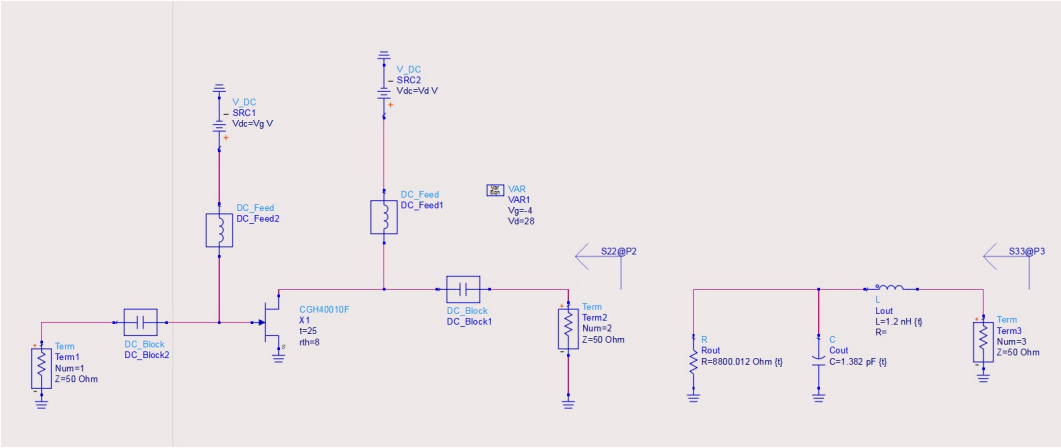


FIGURE 3.12: Schematic circuit to determine the output parasitic elements

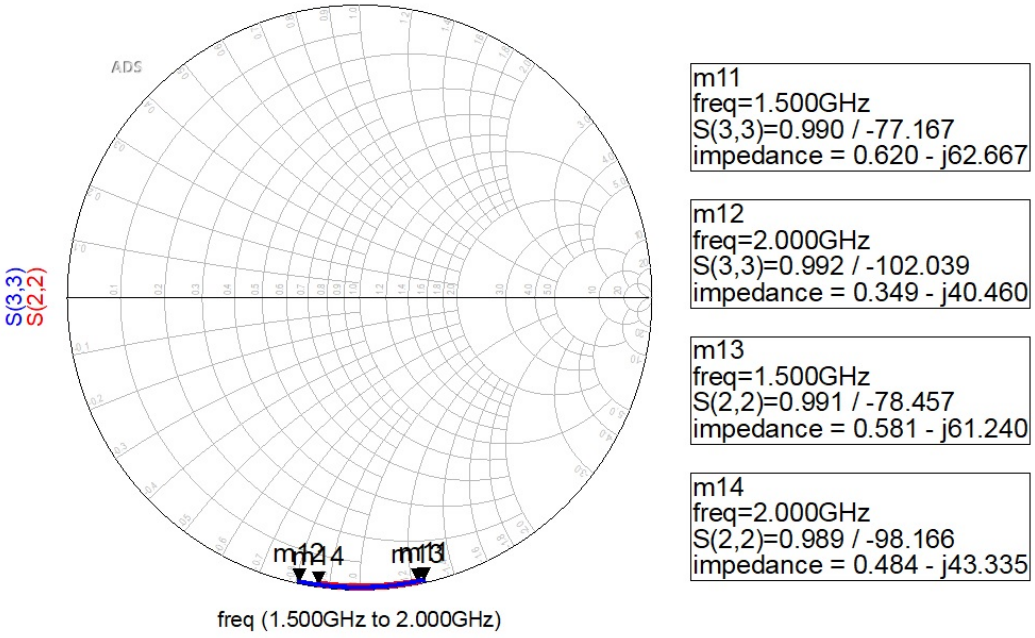


FIGURE 3.13: S_{22} and S_{33} results on the Smith Chart

the optimization tool, which should minimize it. The Difference Quantity can be derived by Equation 3.5. The simulation results are illustrated in Fig 3.14. This quantity result should ideally go to $-\infty$, and the quantity should be $\leq$-30dB, at least in practice. However, the bandwidth ranges from 1.5GHz to 2GHz, which cannot maintain the entire bandwidth due to it being too wide. Therefore, this result is acceptable.

$$\text{Difference} - \text{Quantity}(\text{dB}) = |S_{22} - S_{33}| \tag{3.5}$$

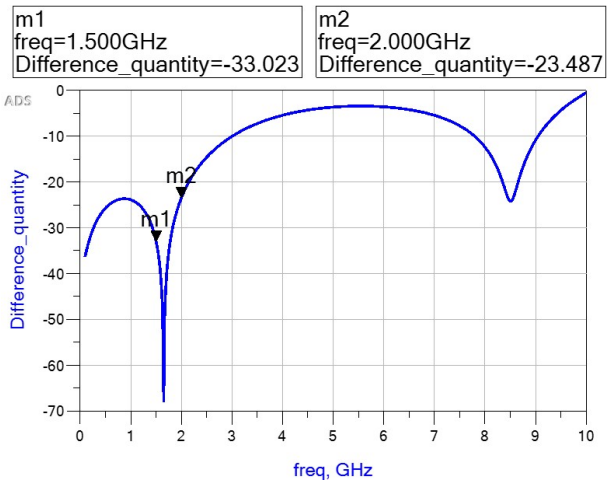


FIGURE 3.14: The result of difference quantity

3.2 Output Section Design

The output section contains the drain biasing network, wave-shaping circuit, and the sub-matching circuit. The block diagram is depicted in Fig 3.15. The bias network of the drain is similar to the bias network of the gate, the only difference is not considered, namely the stability circuit, as discussed in Section 3.1.3. Therefore, The drain basing network is not discussed in this section, and the details of the biasing network only discusses the gate biasing network, which is in the next section. As such, this section discuss only the output matching network, which contains the wave-shaping and sub-matching circuit. The purpose of the wave-shaping circuit is to shape the rectified half-sinusoidal wave and rectangle wave at the drain side (Class-F). Moreover, the wave-shaping circuit causes the intrinsic impedance of the second and third harmonics to be located at the correct location on the Smith Chart. Another component of the output matching network is a sub-matching circuit that ensures fundamental frequency impedance matching, which can be applied with a simple L, Pi or T matching circuit. However, the sub-matching circuit is sometimes unnecessary, depending on the wave-shaping circuit types and amplifier class. The reason is that some types of wave-shaping circuits can match the fundamental frequency impedance even though the impedance of the second and third harmonics controlled simultaneously. Furthermore, there are two types of the intrinsic impedance of the fundamental, second, and third-order harmonic on the Smith Chart. If the intrinsic impedance is a single node, the amplifier is the conventional Class-F/F^{-}, and if the Intrinsic impedance is the locus, the amplifier is the continuous mode F/F^{-}.

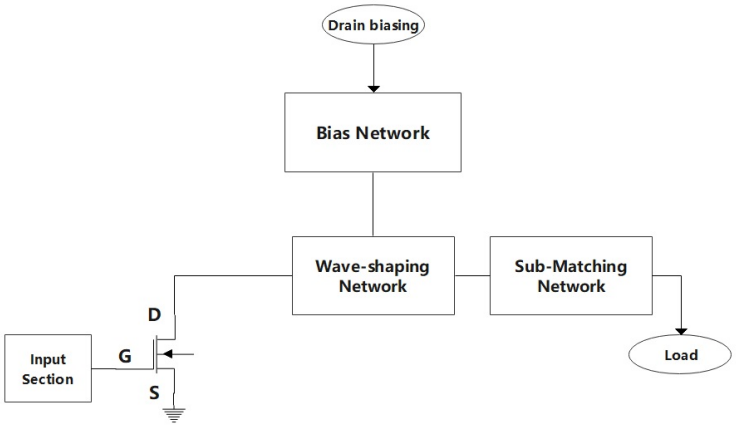


FIGURE 3.15: Output section of the power amplifier

3.2.1 Conventional Class-F Output Section

Fig 3.16 depicts the output matching network of the Class-F amplifiers. For the input port at plane Γ_{out}, its the value is the optimum loadline result (R_{opt} = 40Ω) , achieved as in Section 3.1.1. The output port at the load has value 50Ω. L_{out}, R_{out}, and C_{out} are the parasitic components. The output equivalent model is applied instead of the transistor to obtain the output matching network. The theory behind this method is discussed in Section 3.1.4. TL_4 is the open-circuit stub selected to be a quarter-wavelength at the third harmonic, a choice that can realise the short-circuit condition at the right-hand side of the series transmission line TL_3[11]. Therefore, the series transmission line section and open circuit stub can provide an open-circuit model at the third harmonic. On the other hand, TL_2 is a quarter-wave transmission line placed between the DC source and extrinsic drain terminal[9]. Therefore, it provides short-circuit termination for even voltage harmonics. The open stub TL_1 can improvement the efficiency, and the TL_5 and TL_6 transmission line tank is the L-section for building the fundamental output matching circuit.

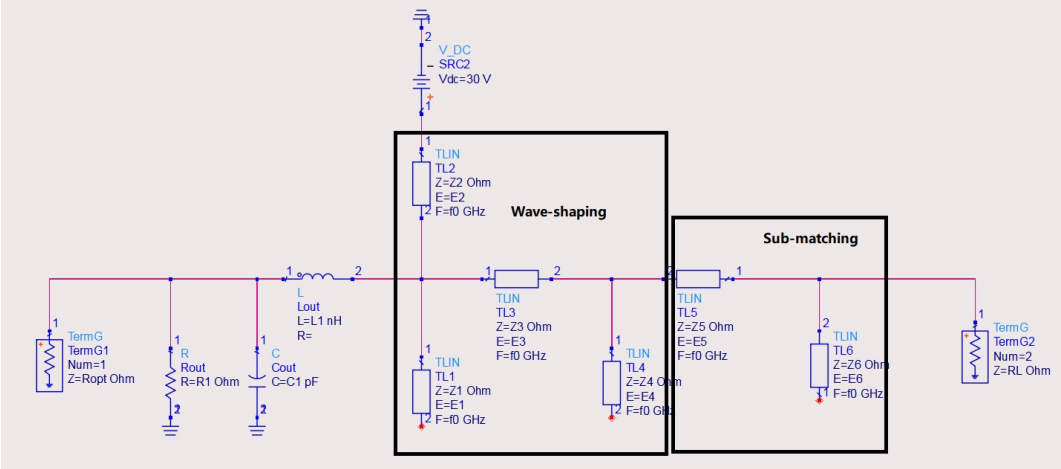


FIGURE 3.16: Class-F output matching network

As the above condition, the parameters of the electrical length E_3 can be determined by Equation 3.6 at the operating frequency. The other parameters of the electrical length can be set to approximate values: $E_2 = \lambda/4$ and $E_4 = \lambda/12$. The impedances Z_1, Z_3, and Z_4

can have any value[9], and the Z_2 is 50Ω. Then, the sub-matching circuit can be added to the output matching network. However, the second-order harmonic cannot be met perfectly due to the influence of the bond wire (L_D). Therefore, the optimization and tuning function can be applied using the ADS software to achieve more accurate results. In particular, the final result after optimization is illustrated in Fig 3.17 and Fig 3.18.

$$E_3 = \theta_3 = \frac{1}{3}\tan^{-1}\left(\frac{1}{3Z_0\omega_0 C_{out}} - \frac{3\omega_0 L_{out}}{Z_0}\right) \tag{3.6}$$

Fig 3.17 presents the reflection coefficient S_{11} and reverse voltage gain S_{21}. As can be seen, S_{11} at the fundamental frequency has no power reflection, and the bandwidth is quite narrow, while the S_{21} reaches the maximum value of 0dB. The second and third-order harmonics are the short and open conditions. Therefore, S_{11} should be 0dB, and the S_{21} cannot reach the maximum value. The intrinsic impedances of the network can also provide the condition of the class-F amplifier, as displayed in Fig 3.18. The intrinsic impedance of the fundamental frequency is close to 50Ω (the centering on the Smith Chart), the second-order harmonic intrinsic impedance is close to zero, and the third-order harmonic intrinsic impedance is large enough to approach the infinity, here, the harmonic intrinsic impedance nodes are located on the left and right side of the Smith Chart. The intrinsic impedance of the fundamental and high-order harmonics satisfy the specification of the Class-F power amplifier.

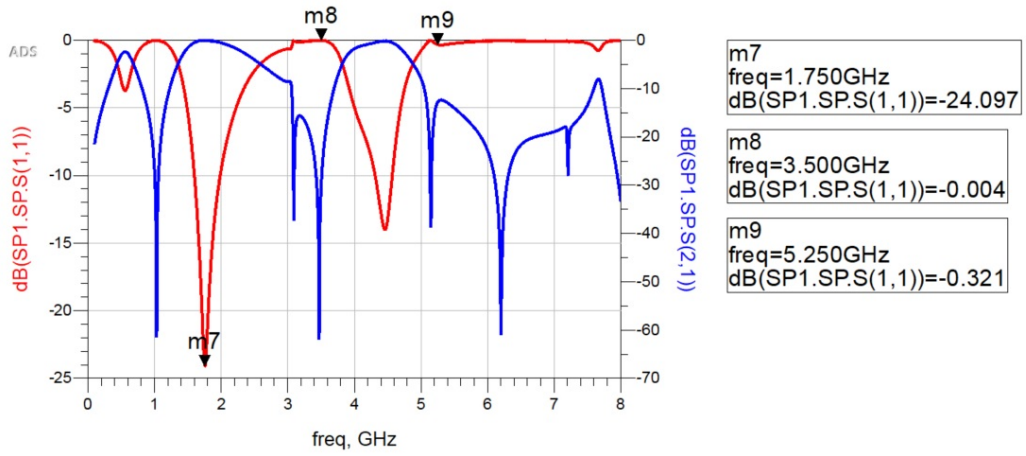


FIGURE 3.17: S_{11} and S_{21} results of the Class-F output matching network

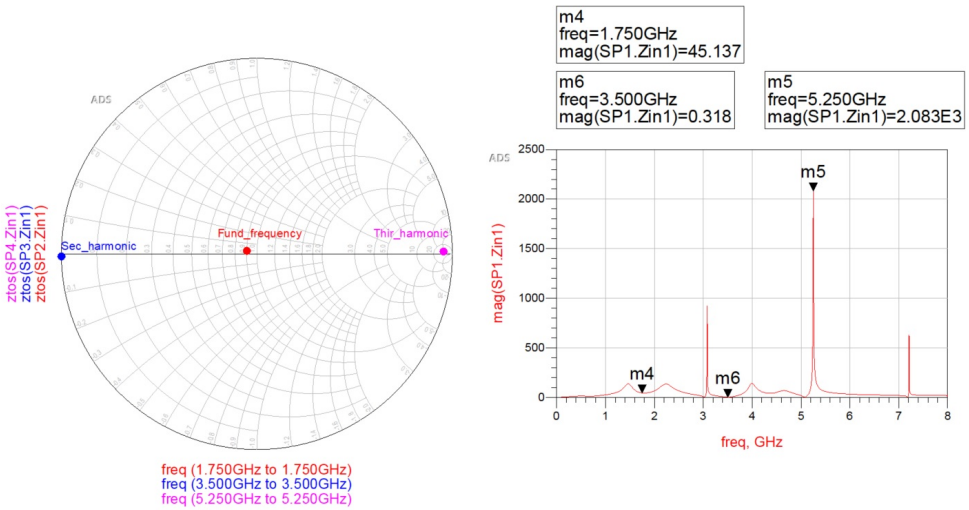


FIGURE 3.18: Intrinsic impedances of the Class-F output matching network

3.2.2 Conventional Inverse Class-F Output Section

The inverse Class-F output matching topology is illustrated in Fig 3.19. The parasitic elements replace the real transistor to be simulated by the ADS software, a procedure the same as with the Class-F amplifier. The series transmission line TL_1 is placed between the extrinsic drain terminal and shunt short-circuited quarter-wavelength transmission line TL_3; it provides an open-circuit condition for the second harmonic at the device output by forming a second-order harmonic tank together with C_{out} and L_{out}. The combined TL_1+TL_2 series transmission line short-circuited provides a short-circuit condition (together with L_{out}) for the third harmonic at the device output shorted on its right-hand side[10]. The open-circuit stub TL_4 provides a shorting effect at the third harmonic. On the other hand, when applying this topology to the conventional Class-F amplifier, the series transmission lines TL_1+TL_2 becomes very long, and the sub-matching circuit should be added. However, this topology is proper for the inverse class-F amplifier and does not require the addition sub-matching circuit to match the fundamental frequency. Therefore, this topology is more suited for the inverse Class-F amplifier.

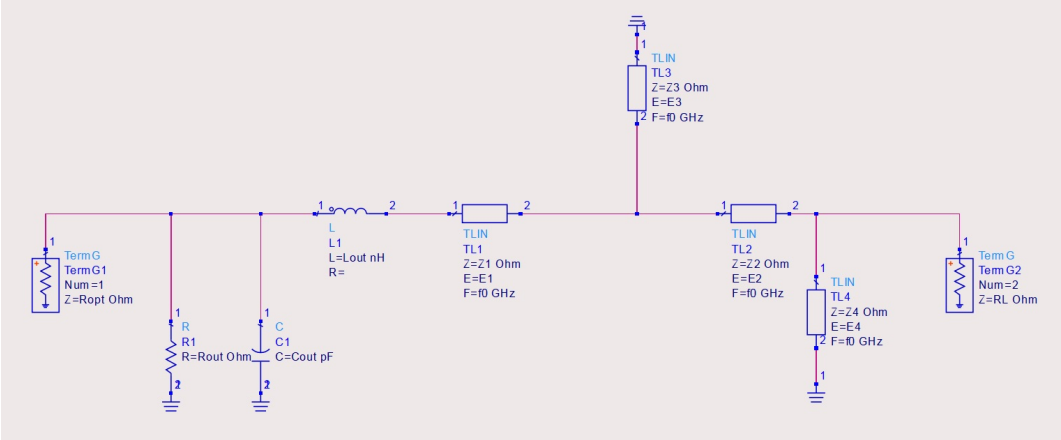


FIGURE 3.19: Inverse Class-F output matching network

The inverse output matching network can achieve the approximate values of each component via an analytical method, which can reduce the amount of work for tuning by the ADS software. As discussed above, this matching network seen by the device multi-harmonics current source at the second and third harmonic gives infinity and zero reactance. However, to derive the values of each component, the current source and parasitic elements should be considered at the fundamental frequency. TL_1+TL_2, L_{out}, and TL_4 can build the low-pass *Pi*-type matching network for the fundamental frequency, as depicted in the Fig 3.20.

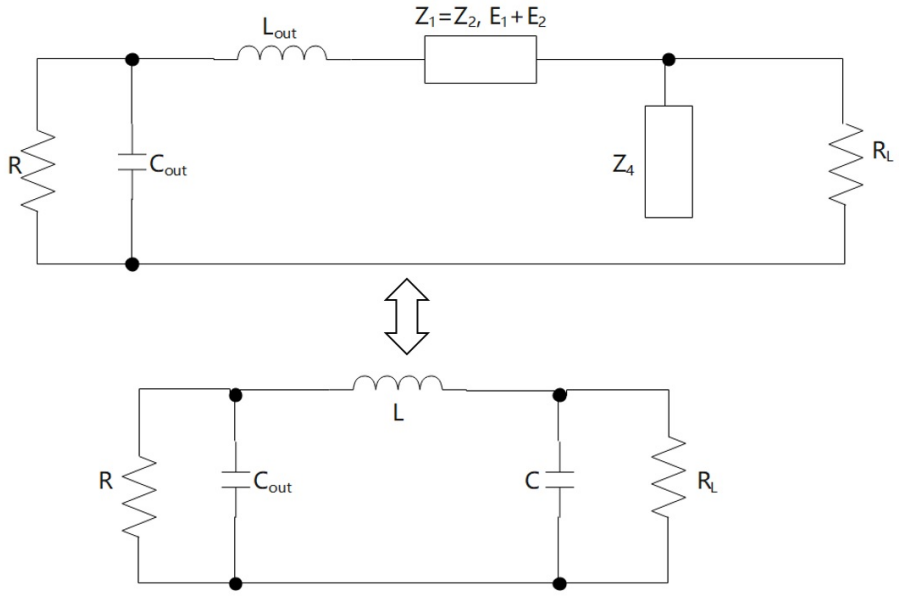


FIGURE 3.20: Equivalent representations of matching network at fundamental frequency

L_{out} and TL_1+TL_2 can be represented by the inductor L, for which $Z_1 = Z_2$. The value of θ_1+θ_2 (E_1 + E_2 in Fig 3.20) is less than $\frac{\pi}{3}$ at the fundamental frequency. The open-circuit can be represented as the capacitor due to their being equivalent each other. Then, the relevant equations of the Pi-network can be applied from Equation 3.7 to Equation 3.10. The values of L and C can be determined eventually. These equations are applicable only when $R_L > R_{opt}$ and $R = R_{opt}$. TL_3 is connected to the drain biasing rather than the RF choke inductor in practice.

$$Q = \omega_0 C_{out} R_{opt} \tag{3.7}$$

$$Q_L = \sqrt{\frac{R_L}{R_{opt}}(1+Q^2) - 1} \tag{3.8}$$

$$C = \frac{Q_L}{\omega_0 R_L} \tag{3.9}$$

$$L = \frac{Q + Q_L}{1 + Q_L^2} \cdot \frac{R_L}{\omega_0} \tag{3.10}$$

The value of Z_4 can be derived from Equation 3.12, and the electrical length of $\theta_4 = \frac{\pi}{6}$. Equations 3.11, 3.13, and 3.14 can then be put into MATLAB to yield the approximate values

θ_1, θ_2, and Z_1. TL_1 and TL_2 can be assumed to have the same characteristic impedance Z_1, and $\theta_1 + \theta_2$ should be smaller than $\frac{\pi}{3}$. TL_3 can be set to $\theta_3 = \frac{\pi}{2}$ and $Z_3 = 50\Omega$.

$$Z_1 = \frac{\omega_0(L - L_{out})}{\sin(\theta_1 + \theta_2)} \tag{3.11}$$

$$Z_4 = \frac{1}{\omega_0 C\sqrt{3}} \tag{3.12}$$

$$2\omega_0 C_{out} - \frac{1}{2\omega_0 L_{out} + Z_1 \tan 2\theta_1} = 0 \tag{3.13}$$

$$3\omega_0 L_{out} + Z_1 tan3(\theta_1 + \theta_2) = 0 \tag{3.14}$$

Fig 3.21 and Fig 3.22 display the simulation results of the S-parameters and the impedance positions for the inverse Class-F output matching network. These simulation results have been optimized by ADS software. The reflection coefficient S_{11} matches the fundamental frequency, which has no power reflection. Compared with Class-F, the bandwidth is larger and has less noise at the second and third harmonics. The correct impedance position and value of the inverse Class-F are shown in Fig 3.22, here, the second-order harmonic is infinity, while the third-order harmonic is zero.

The performance of the inverse Class-F output network has improved significantly compared with Class-F. As such. The inverse Class-F is more accessible to designing the output matching network, which does not require the addition fundamental sub-matching circuit. Moreover, the analytics method can be applied to easily calculate each component's approximate values and reduce the amount of work needed for tuning by ADS software. As a result, the simulation results of the inverse Class-F output matching network are more accurate, particularly the harmonics-controlled. The bonding wire (L_D) influence is limited due to L_D having been incorporated with the short transmission line(TL_1 + TL_2) perfectly.

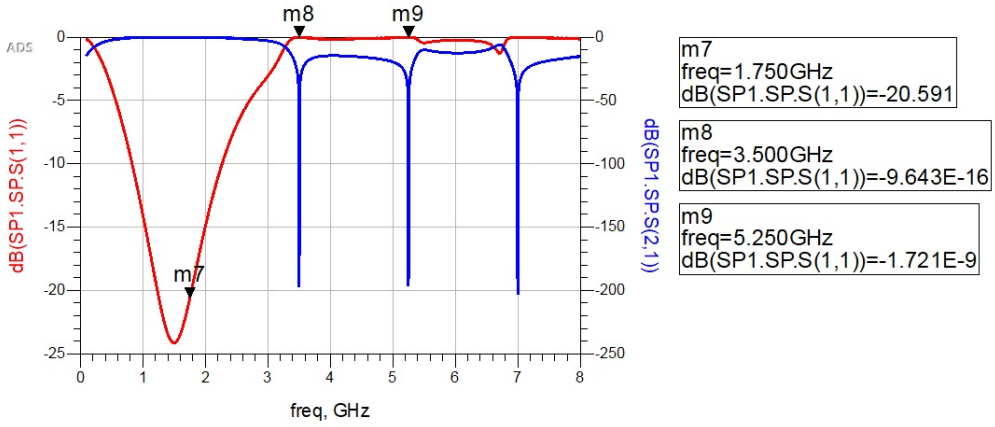


FIGURE 3.21: The S_{11} and S_{21} results of the inverse Class-F output matching network

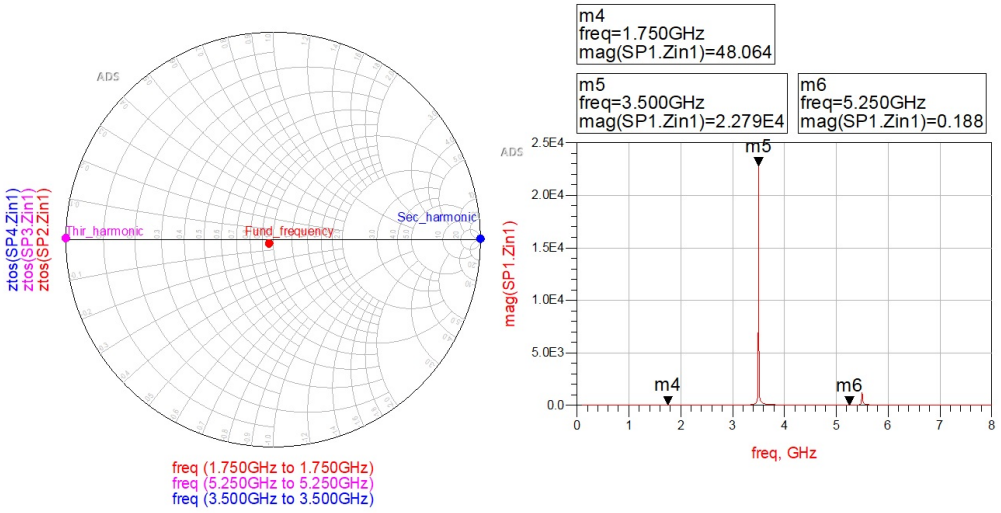


FIGURE 3.22: The intrinsic impedances of the inverse Class-F output matching network

3.2.3 Continuous Mode Class-F Output Section

For this thesis, the essential requirement is to design a larger bandwidth amplifier, at least 400MHz. Therefore, the conventional Class-F/F^{-} amplifier is difficult to reach, even though the input matching network is broadband. Thus, the continuous mode amplifiers can be applied to the broadband requirement, as discussed in Chapter 2. The impedance of the continuous mode is no longer a single node on the Smith Chart, so the impedance can be constrained to a certain frequency range, which can be applied to the bandwidth of the amplifier. The general continuous mode amplifier can be represented by Equation 3.15 and Equation 3.16. As observable, the new operators $[1 - \delta \sin\theta]$ on the voltage and $[1 - \xi \sin\theta]$ on the current are added, as opposed to in the conventional amplifier. These operators result in new voltage and current waveforms, and α/a , β/b and γ/c are the coefficients that define the amplifier class.

$$v(\theta) = (1 - \alpha\cos\theta - \beta\cos 2\theta - \gamma\cos 3\theta) \cdot [1 - \delta\sin\theta] \tag{3.15}$$

$$i(\theta) = (1 + a\cos\theta + b\cos 2\theta + c\cos 3\theta) \cdot [1 - \xi\sin\theta] \tag{3.16}$$

The conventional Class-F amplifier requires an open-circuit condition at the odd harmonic frequency and a short-circuit condition at the even harmonic frequency. This will generate the square voltage waveform and a half-rectified current waveform at the output current-generator plane. These waveforms are represented by Equation 2.11 and Equation 2.12 in Chapter 2. However, for the continuous mode Class-F amplifier, the output voltage and current waveform are illustrated in Fig 3.23. Here, the current waveform is still half-rectified, but the voltage waveform depends on the coefficient δ causing the waveform to be variable. Only when the coefficient is zero that the voltage waveform is the same as the conventional Class-F amplifier. Therefore, the waveforms can be represented by Equation 3.17 and Equation 3.18. In general, the range of the coefficient δ is from -1 to 1[3].

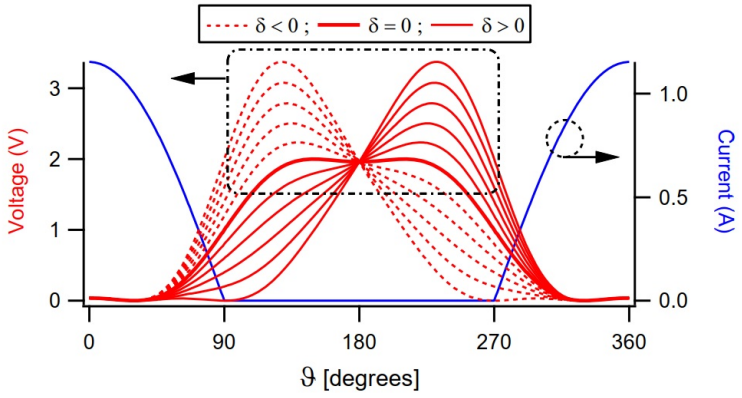


FIGURE 3.23: Theoretical Continuous Class-FV voltage and current waveforms for δ[3]

$$i_{CFV_\theta} = \begin{cases} I_{peak}\cos\theta & 0 < \theta < \frac{\pi}{2}, \frac{3}{2}\pi < \theta < 2\pi \\ 0 & \frac{\pi}{2} < \theta < \frac{3}{2}\pi \end{cases} \tag{3.17}$$

$$v_{CFV}(\theta) = (1 - \frac{2}{\sqrt{3}}\cos\theta + \frac{1}{3\sqrt{3}}\cos 3\theta) \cdot [1 - \delta\sin\theta] \tag{3.18}$$

In order to obtain the continuous mode Class-F output matching network. First, the impedance equations must be derived. The impedance equations can be derived according to the previous amplifier's voltage and current equations(3.17 and 3.18), and the equation results are obtained in Equation 3.19. Since the theory of the continuous mode amplifier is based on the conventional model amplifier, the impedances are likewise constrained at the fundamental impedances of the second and third harmonics. The difference is that the impedances can be tuned by coefficient x_i. The range of the coefficient x_i is from -1 to 1. Therefore, the locus of the fundamental impedance is variable around the center (50Ω). The second-order harmonic being on the short-circuit point and variable on the edge of the Smith Chart. Since the third-order harmonic is difficult to control, it is not considered when to realizing the output matching network. The coefficient σ is used to optimize the fundamental impedance, which causes the locus to be as close to the center of the Smith Chart as possible.

$$Z_n = \begin{cases} Z_{fund} = \sigma \cdot R_{opt} + j \cdot \frac{\sqrt{3}}{2} \cdot x_i \cdot R_{opt} \\ Z_{2fund} = 0 + j \cdot x_i \cdot 1.375 \cdot R_{opt} \\ Z_{3fund} = open - circuit \end{cases} \tag{3.19}$$

The bandwidth is 500MHz (bandwidth requirement $\geq 400MHz$), and the fundamental frequency is 1.75GHz. Therefore, the coefficient x_i from -1 to 1 corresponds to the frequency from 1.25GHz to 2.25GHz, as illustrated in Fig 3.24. This range is only for the output matching network to ensure better optimization through the ADS software. Therefore, the bandwidth range from 1.5GHz to 2GHz in the real amplifier.

Fig 3.25 present the output matching network for the continuous mode Class-F power amplifier. The main method is to control the harmonic separately to ensure that the frequency range is as wide as possible within the coefficient x_i. Thus, the first black block is controlled by the third-order harmonic, and the subsequent is controlled by the second-order

xi	SP1.SP.freq[0]	SP2.SP.freq[0]
-1.000	1.250 GHz	2.500 GHz
-0.900	1.300 GHz	2.600 GHz
-0.800	1.350 GHz	2.700 GHz
-0.700	1.400 GHz	2.800 GHz
-0.600	1.450 GHz	2.900 GHz
-0.500	1.500 GHz	3.000 GHz
-0.400	1.550 GHz	3.100 GHz
-0.300	1.600 GHz	3.200 GHz
-0.200	1.650 GHz	3.300 GHz
-0.100	1.700 GHz	3.400 GHz
-1.388E-16	1.750 GHz	3.500 GHz
0.100	1.800 GHz	3.600 GHz
0.200	1.850 GHz	3.700 GHz
0.300	1.900 GHz	3.800 GHz
0.400	1.950 GHz	3.900 GHz
0.500	2.000 GHz	4.000 GHz
0.600	2.050 GHz	4.100 GHz
0.700	2.100 GHz	4.200 GHz
0.800	2.150 GHz	4.300 GHz
0.900	2.200 GHz	4.400 GHz
1.000	2.250 GHz	4.500 GHz

FIGURE 3.24: The frequencies corresponding to the coefficient x_i

harmonic. Finally, the last one is the fundamental frequency matching. Since the fundamental frequency is difficult to match for the Class-F network, a sub-matching circuit is added, with TL_{11}, TL_{12} and TL_{13}. A *Pi*-matching circuit is used to here to ensure the fundamental frequency matching. This output matching section can follow the analytical method to determine the approximate value of each component. However, the analytics method is rather complicated, which must be taken an amount of work for the iterate analysis by Matlab. Thus, the value of each component can be achieved directly through the ADS software, and the ADS software can tuning the component's values to get the correct simulation results.

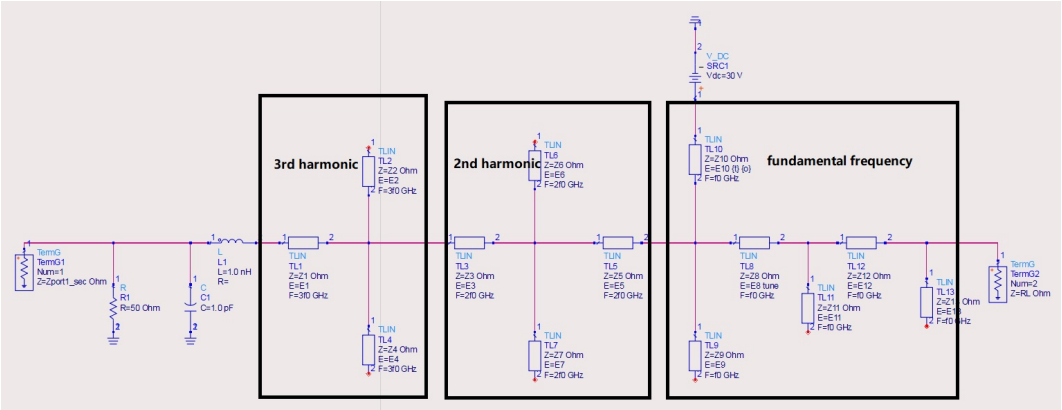


FIGURE 3.25: Continuous mode Class-F output matching network

Fig 3.26 present the fundamental and second-order harmonic impedance for continuous mode class-F; here, the left side displays the ideal locus in accordance with Equation 3.19. The frequency ranges from 1.25GHz to 2.25GHz. The right side is the simulation results compared with ideal equation locus. The pink and green nodes(locus) are represent the simulation results of the output matching network and are close to the ideal locus. Fig 3.27 displays the S-parameters of the output matching network. Here, the x-axis is the coefficient x_i from -1 to 1. Meanwhile, S_{11} is the reflection coefficient at a fundamental frequency larger than a conventional mode amplifier within bandwidth. while S_{33} is the reflection coefficient at the second-order harmonic.

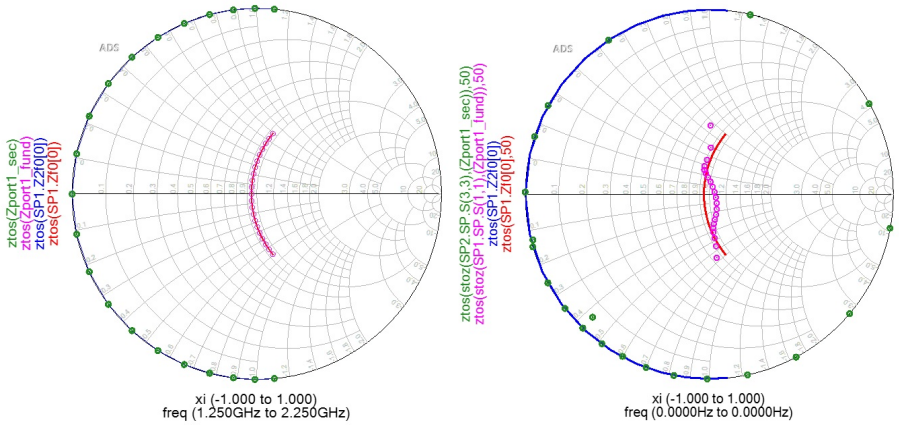


FIGURE 3.26: The intrinsic impedance locus at fundamental frequency and second-order harmonic

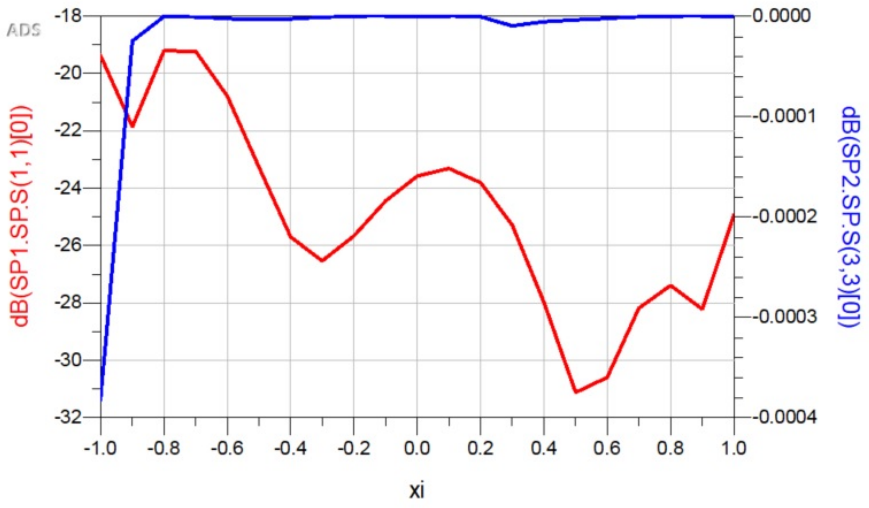


FIGURE 3.27: The S_{11} and S_{33} results of the continuous mode Class-F output matching network

3.2.4 Continuous Mode Inverse Class-F Output Section

The continuous mode inverse Class-F amplifier is based on the conventional mode inverse class-F amplifier. However, the second-order harmonic varies on the edge of the open-circuit condition, and the third-order harmonic is located on the short-circuit condition. Therefore, as with the continuous mode Class-F amplifier, the third-order harmonic was not considered in realizing the output matching network. Fig 3.28 presents the output voltage and current waveforms. The voltage waveform is the same as in the continuous mode Class-F when $\delta = 0$, as illustrated in Fig 3.23. However, the current waveform is no longer the half-rectified sinusoids as the conventional inverse Class-F, which depends only on the coefficient$[1 - \xi \sin\theta]$, with the range of ξ from -1 to 1. when $\xi = 0$, the current waveform is the conventional mode. The voltage and current waveforms can be represented by Equation 3.20 and Equation 3.21, respectively.

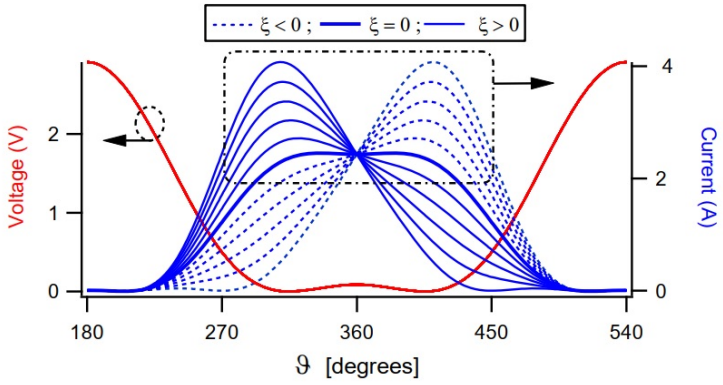


FIGURE 3.28: Theoretical Continuous Class-FI^{-} voltage and current waveforms for ξ[3]

$$v_{CFI^-}(\theta) = 1 - \frac{2}{\sqrt{2}}\cos\theta + \frac{1}{2}\cos 2\theta \tag{3.20}$$

$$i_{CFI^-}(\theta) = (i_{DC} + i_1\cos\theta + i_2\cos 2\theta - i_3\cos 3\theta)\cdot[1 - \xi\sin\theta] \tag{3.21}$$

Where $i_{DC} = 1.22$, $i_1 = \sqrt{2}$, $i_2 = 0$ and $i_3 = 0.203$. The coefficients i_1, i_2 and i_3 represent the fundamental(i_1), second-order harmonic(i_2) and third-order harmonic(i_3) current components and the load resistance is maintained at 50Ω. The fundamental frequency, second-order harmonic and third-order harmonic load admittances are represented by Equation 3.22. G_{opt} is the optimum admittance corresponding to the optimum resistance $1/R_{opt}(40_\Omega)$. σ is used to optimize the fundamental impedance locus, as as the case the continuous mode Class-F. The range of the tuning coefficient x_i is from -1 to 1 and corresponds to the frequency from 1.25GHz to 2.25GHz, as shown in Fig 3.24[3].

$$Y_n = \begin{cases} Y_{fund} = \sigma\cdot G_{opt} + j\cdot\frac{\sqrt{3}}{2}\cdot x_i\cdot G_{opt} \\ Y_{2fund} = 0 + j\cdot x_i\cdot 1.615\cdot G_{opt} \\ Y_{3fund} = short - circuit \end{cases} \tag{3.22}$$

To obtain the continuous mode inverse Class-F amplifier, the output section must be designed to control the fundamental frequency and harmonics. Fig 3.29 illustrates the wave-shaping circuit, containing the third-order harmonic, second-order harmonic and fundamental frequency blocks. However, with the inverse Class-F, the addition sub-matching circuit is unnecessary to match the fundamental frequency. The approach to obtain each component's values is the same as the continuous mode Class-F amplifier.

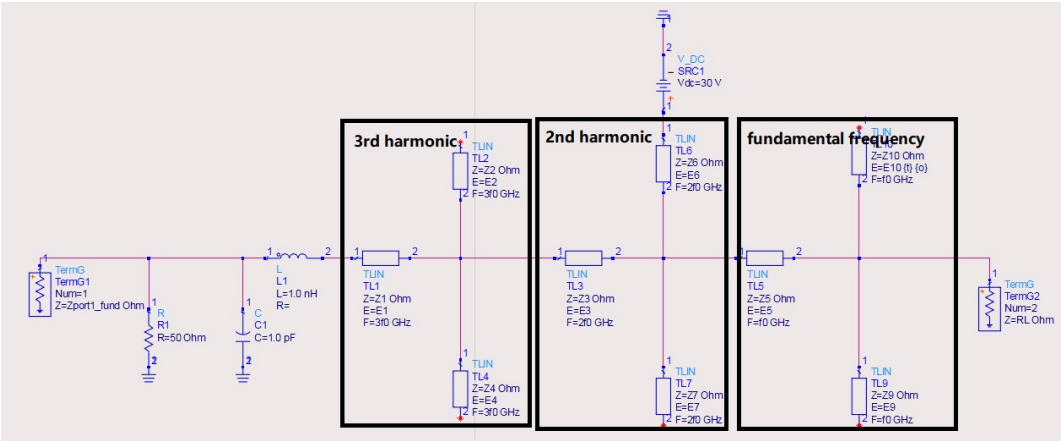


FIGURE 3.29: Continuous mode inverse Class-F output matching network

Fig 3.30 provides the impedances of the continuous mode inverse Class-F output section networks. The left-side displays the ideal fundamental frequency and second-order harmonic impedance locus, which is rolling-over compared with in the continuous mode Class-F. The fundamental frequency impedance is still near the center, and the second-order harmonic is varied on the edge of the open-circuit condition on the Smith Chart. Meanwhile, the right-side figure displays the real impedances locus with the output section. The pink-coloured locus is the fundamental frequency, and the green-coloured locus is the second order harmonic impedance. Fig 3.31 presents the reflection coefficient S_{11} for the fundamental frequency and the reflection coefficient S_{33} for the second-order harmonic impedance. Compared with the continuous mode Class-F, the bandwidth of S_{11} is narrower.

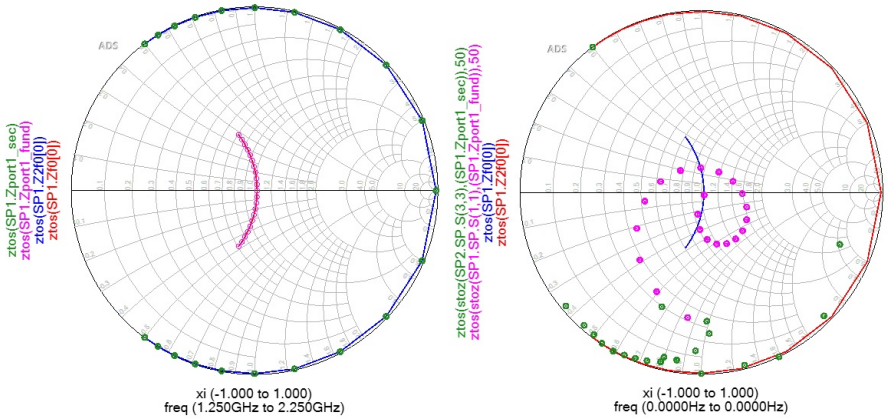


FIGURE 3.30: The intrinsic impedance locus at fundamental frequency and second-order harmonic

Given the above results, the continuous mode Class-F output section network is superior to the inverse type, since the bandwidth of the S-parameter is larger. However, the network

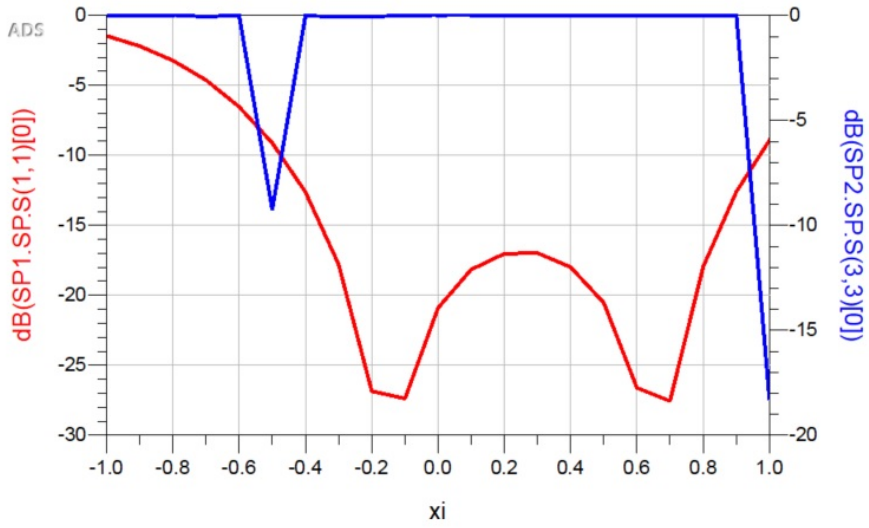


FIGURE 3.31: The S_{11} and S_{33} results of the continuous mode inverse Class-F output matching network

is more complex due to the addition sub-matching circuit that must be added to match the fundamental frequency impedance. Therefore, a conclusion of the best amplifier topology cannot be provided at the moment. Both networks should be further analysed regarding the input section network and the real active device(also conventional Class-F/F^{-}). Therefore, the complete RF power amplifiers under the ideal condition are discussed in the next chapter.

3.3 Input Section Design

The main RF power amplifier's input section includes the input matching network, stability circuit and bias network, as depicted in Fig 3.32. The stability circuit is discussed in a Section 3.1.3. Meanwhile, the bias network and input matching network are discussed separately; the performance of the entire input section is summarized. The bias network topologies of the gate are similar to those of the drain. Therefore, the design of the bias network is primarily discussed in the input section part.

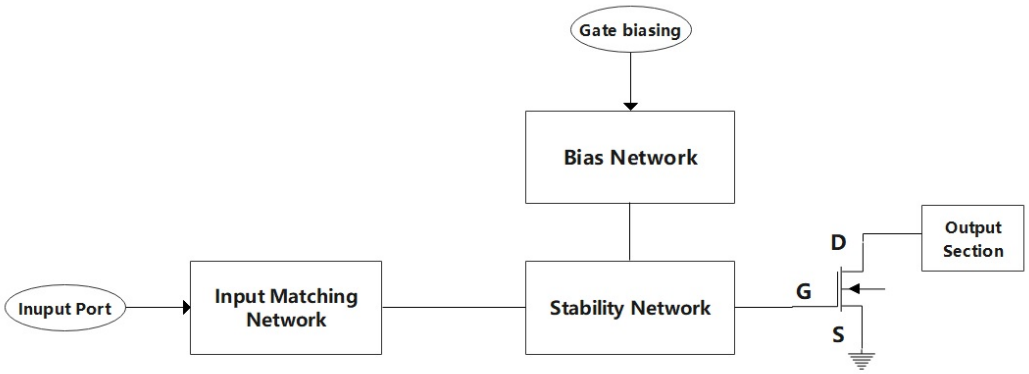


FIGURE 3.32: Input section of the power amplifier

3.3.1 Bias Network

The scheme of an ideal power amplifier includes, at both its input and output, a Bias Tee component; (i.e. a three-port element whose task is to feed the power amplifier with the RF signal and the DC supply, which come from separate paths and should not interfere with each other in an unwanted way). The scheme of a Bias Tee is illustrated in Fig 3.33. In particular, it contains an inductor and a capacitor of infinite value, called the RF block and DC block, respectively. Both of these components are ideal. The purpose of the RF block inductor is to block the RF signal, so that only the DC component can pass. On the other hand, the DC block capacitor has a large capacitance that blocks the DC component and allows the RF signal to pass. Therefore, both the DC and RF components can reach the transistor, without interacting with each other.

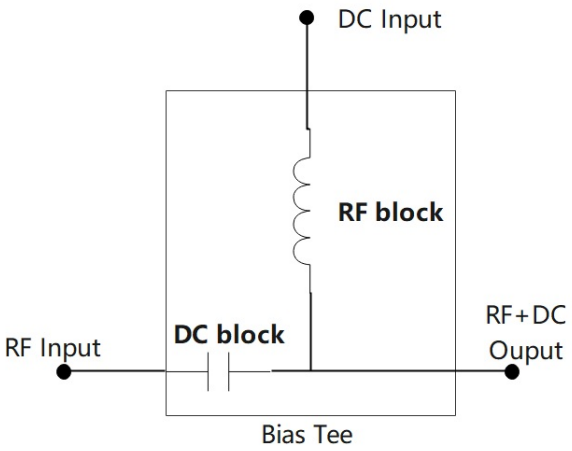


FIGURE 3.33: Bias-Tee model and the component

A real Bias-Tee is composed of non-infinite components, which should be implemented as close as possible to the functions just described. The DC block capacitor is easier to design than the RF block, as it is simply an SMD component; if the capacitance value is large enough, it behaves as a short circuit in the operating frequency; (i.e. it does not affect the input matching). Otherwise, if the value is smaller, it will affect matching in the band, but this effect is not necessarily unwanted or detrimental. The RF block inductor is more complex to design than the DC block because it has an effect during low-frequency as well, which means that stability circuit must be incorporated into the gate biasing network and designed together.

Fig 3.34 displays the bias network incorporated with the stability circuit. The series resistor (R_2) in the gate biasing circuitry is a vital component for achieving low-frequency stability[4]. The RF choke (inductor) between the shunt capacitor and series resistor is replaced by a microstrip line, which is around $\lambda/4$ wavelength. Since the wavelength at the DC is infinite, the microstrip line/transmission line is essentially transparent to the power supply. At the radio frequency, the line transforms the low impedance to an impedance that is very large relative to the impedance of the desired RF path[7]. Furthermore, the microstrip line is much cheaper and easier to tune than the discrete inductor coil on the printed circuit board.

The capacitors between the DC source and microstrip line are by-pass capacitors that short the RF signal to the ground, as such, the RF signal that may be present alone on a DC

path is removed, causing the DC signal to be cleaner and purer. Three capacitors connected in parallel are used here. With the following values:

- 100uF for the high frequencies.
- 100pF for the medium frequencies.
- 10pF for the low frequencies.

Each capacitor has its highest admissible frequency limit due to the Equivalent Series Resistance (ESR), which causes power loss for the amplifier. Therefore, a few capacitors topologies can cover the entire frequency band. Moreover, these capacitors' values are not fixed, and thus can be changed for the real design. As such, the above values only merely serve as an example to introduce the theory of the by-pass capacitors.

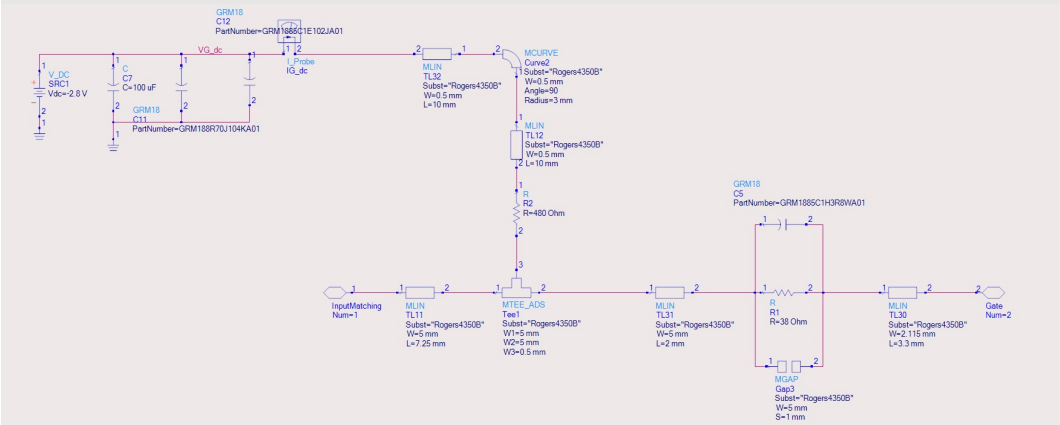


FIGURE 3.34: Bias network and stability schematic circuit at the input section

3.3.2 Input Matching Analysis

To achieve the maximum power and efficiency of the amplifier, the input and the output impedance of the device must be matched via the matching circuit. For the maximum power transfer, the source and load impedance must be a conjugate match. The resistive parts should be the same. while, the imaginary parts should be of the same magnitude, but with opposite polarity[15]. The main types of matching circuit contain LC matching, Transmission line matching and Transformer matching. The LC matching, which used the capacitor and inductor to build the circuit, resulted in a relatively narrow bandwidth match, with an operating frequency from 30MHz to 300MHz normally. The Transmission line method is matching by using the length and characteristic impedance of the transmission line, which is applied to the broader frequency range greater than 150MHz. The transformer matching can provide wide-band impedance matching, but the frequency and available impedance range are limited.

The purpose of the input matching circuit is to maintain the smooth efficiency and gain within the bandwidth. Therefore, the standard L, Pi, and T-matching circuit can no longer be used, as these simple circuits provide only the narrowband amplifier, which means the operating frequency is a single node. For a broadband amplifier, the input matching circuit must provide a larger bandwidth for the amplifier.

Before beginning the input matching circuit design, a critical parameter Q must be introduced. Q is a constant value that defines the bandwidth as being narrow or wide. If the matching circuit has a small Q value, a larger frequency bandwidth can be achieved, but the out-of-band suppression is poor. However, if the value of Q is large, the frequency bandwidth is substantially decreased[9]. The value of the Q can be derived using Equation 3.23.

$$Q = \frac{f_0}{BW} \tag{3.23}$$

Where f_0 is the operating frequency and BW is the bandwidth required. For example: the operating frequency is 1.75GHz, and the bandwidth is 400MHz. Therefore, the value of Q is 3.4, so the value of Q must be $\leq$ 3.4, or else, the bandwidth will be narrow. There are two approaches to obtain the input matching circuit: the analytics method and the graphical method. The analytics method can use the closed formulas to calculate the value of each component, but this method is complicated. Therefore, in this thesis, the graphical method was applied to achieve the input matching circuit to reduce the design procedure. Fig 3.35 provide an example with the conjugate matching range from 10Ω to 50Ω, and the Q value is 1.5. As observable, the matching circuit cannot cross the Q-circle. Therefore, the input matching circuit must be built with multistage shorted and open transmission lines, series inductors and shunt capacitors, or a mixed circuit(distributed combined with lumped components).

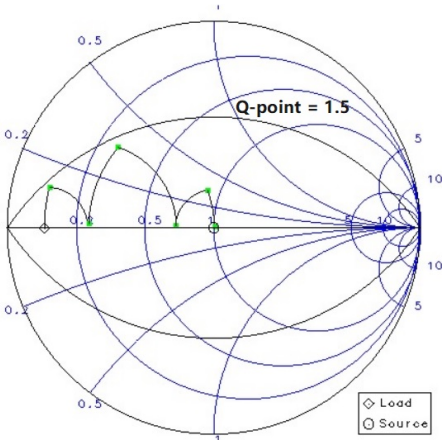


FIGURE 3.35: The Q circle on the Smith Chart

Fig 3.36 provides an example to introduce the multistage matching circuit matched from 50Ω(source) to 1.5Ω(load) with mixed transmission lines and capacitors. The frequency range is from 1.6GHz to 1.9GHz, and the bandwidth is around 300MHz. Fig 3.37 and Fig 3.38 display the simulation results of the S-parameters, as can be seen, the reflection coefficient S_{11} is less than -15dB within the bandwidth, and the reverse voltage gain is 0dB, the maximum value. The same results can be indicated on the Smith Chart, as illustrated in Fig 3.38. Here, S_{11} and S_{21} are no longer single nodes but are the locus. The S_{11} locus surrounds the matching node within the bandwidth, while the S_{21} locus is located at the edge of the Smith Chart. This result is expected, indicating that this circuit is a broadband matching circuit within the bandwidth.

The input section has been introduced completely. Moreover, the design part of the bias

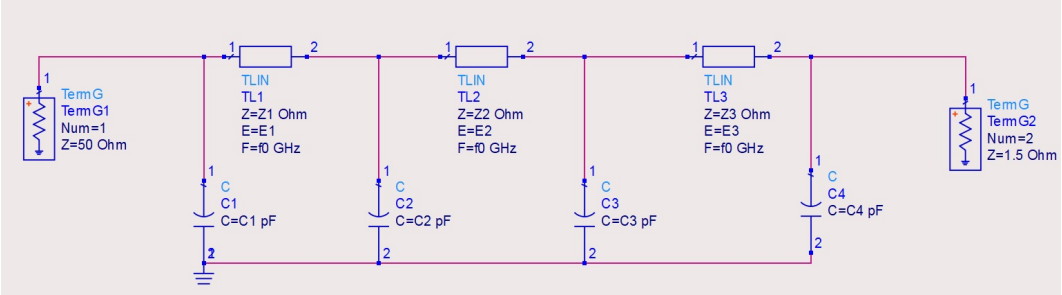


FIGURE 3.36: The schematic circuit of the broadband matching

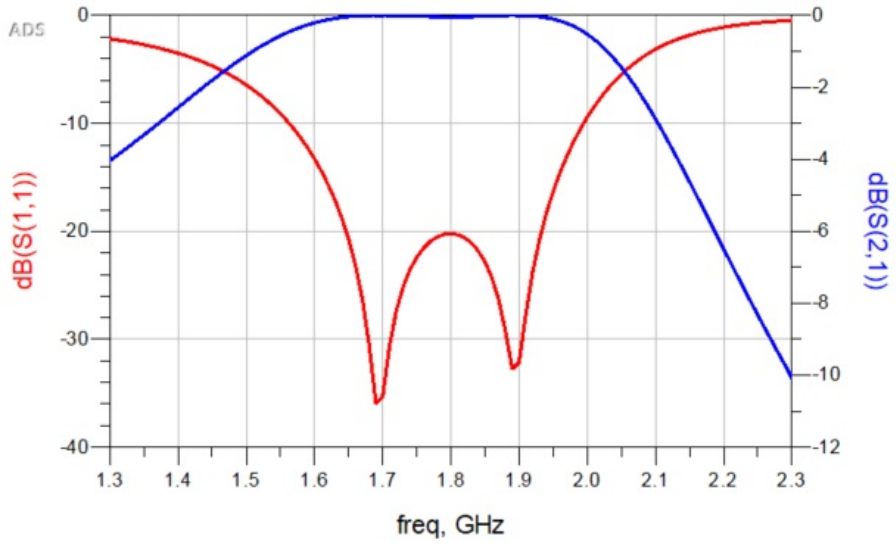


FIGURE 3.37: S_{11} and S_{21} broadband matching

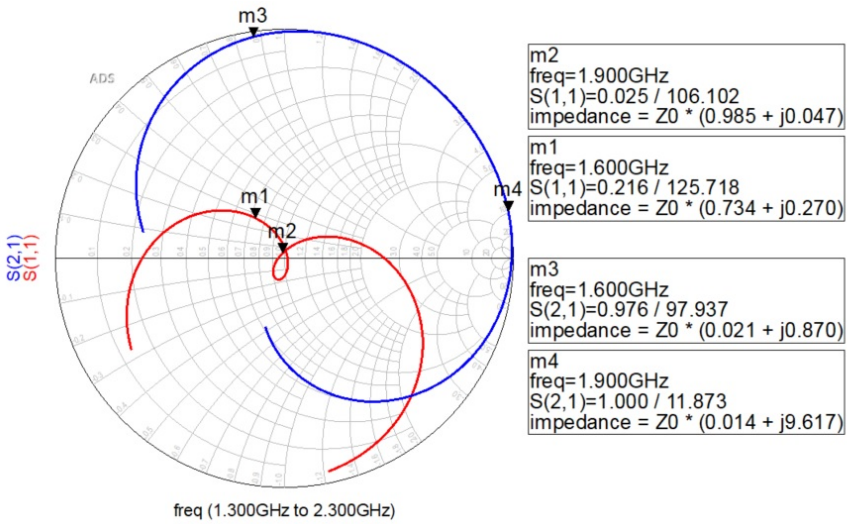


FIGURE 3.38: S_{11} and S_{21} broadband matching on Smith Chart

network and stability circuit has been completed, representing the final design for the amplifiers (not for fabricating the design). However, the input matching circuit offers only a short discussion to review the broadband matching network for the input. It merely only an example to introduce how the broadband matching circuit is realized in practice, so this example is not the final design for the simulation. Since the input matching circuit has many features that must be introduced, the details of the final design are discussed in the following chapter.

Chapter 4

Ideal Power Amplifiers Comparison

4.1 Input Matching Network

As described in Section 3.1.4 in Chapter 3, the main purpose of the input matching network is to enhance the power matching within the operating bandwidth to maximize amplifier gain and power-added efficiency. In addition, for this thesis. The input matching network does not need to consider the third-order harmonic controlled. Therefore, to design the broadband power amplifier, the bandwidth of the input matching network must be larger than in the conventional input matching network. An understanding of the broadband matching network is discussed in the previous chapter. Therefore, this section will gives the design procedure for the input matching network. Moreover, the input matching network is suitable for all types of Class-F amplifiers as it does not consider the harmonic control, means that the four types of amplifiers use the same input matching network.

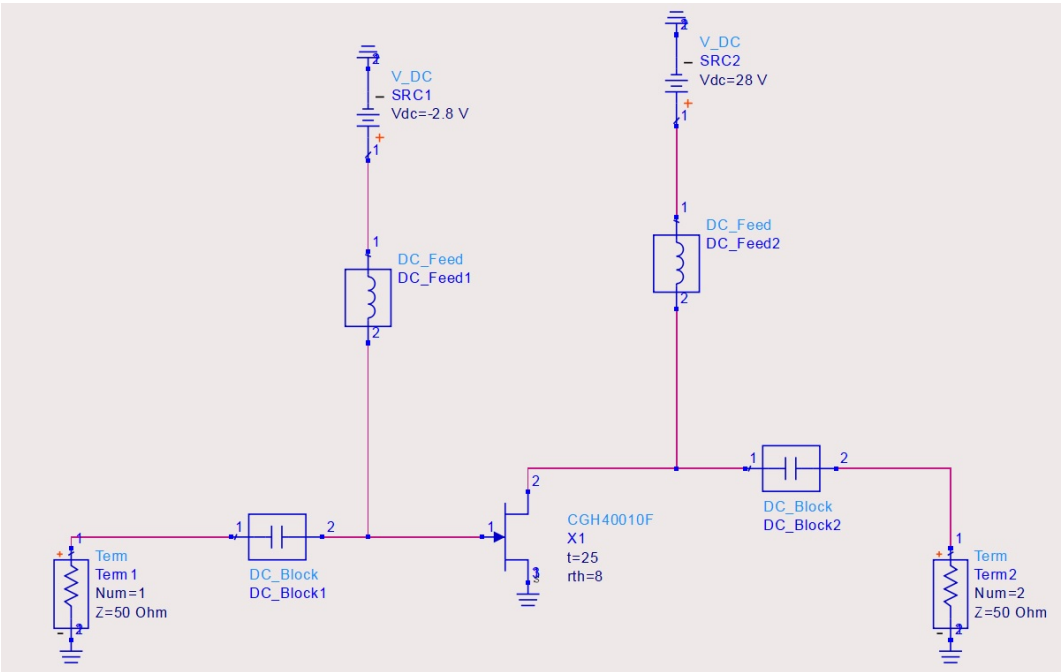


FIGURE 4.1: Small-signal analysis for CGH40010F HEMT device

The first step is to determine the input impedance at the gate side of the device. Fig 4.1 presents a small-signal analysis for the CGH40010F HEMT device to obtain the S-parameters

at 1.75GHz. Here, DC-Feed and DC-Block are the ideal lumped components for building the Bias-Tee model. The gate biasing is -2.8V, and the drain biasing is 28V at the Class-F amplifier's Q-point. Moreover, the impedance of port one and port two impedance is to 50Ω. The input impedance can be derived by Equations 4.1 and 4.2, with a relationship between the reflection coefficient and input impedance. The characteristic impedance(Z_o) can be assumed to be 50Ω. Fig 4.2 indicates that the real and imaginary values of the input impedance(Z_{in}) are at 1.75GHz. Therefore, the input impedance(Z_{in}) is equal to $2.542 + j * 0.909\Omega$.

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{4.1}$$

$$Z_{in} = Z_0 \cdot (\frac{1 + S_{11}}{1 - S_{11}}) \tag{4.2}$$

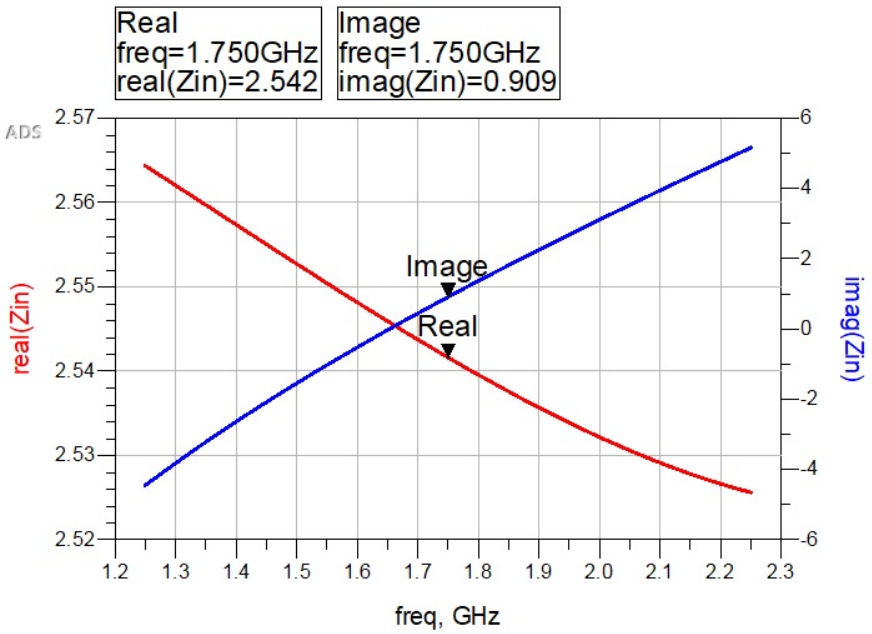


FIGURE 4.2: Simulated input impedance versus frequency

However, for broadband amplifiers, the input impedance displayed in Fig 4.2 cannot be used directly to design the input matching network of the power amplifier, as only the fundamental frequency (1.75GHz) corresponds to this impedance value. Still, the broadband power amplifier must consider the input impedance of the entire bandwidth, not just the fundamental frequency. Therefore, the input impedance corresponding to the entire bandwidth must be simulated by the ADS software again to obtain the appropriate input impedance value, the simulation results of which are present in Fig 4.3. The figure displays an input impedance ranging from 1.25GHz to 2.25GHz. As observable, the real part of the input impedance remains almost constant, while the imaginary parts of the input impedances changes significantly. Thus, the single input impedance cannot be used for the broadband matching network, which must be evaluated in a range of values within the entire bandwidth.

Fig 4.4 presents the broadband input section schematic. The port on the left-side is the source port, which is 50Ω. while, the port on the right-side is Z_{in}, which varies from 1.25GHz

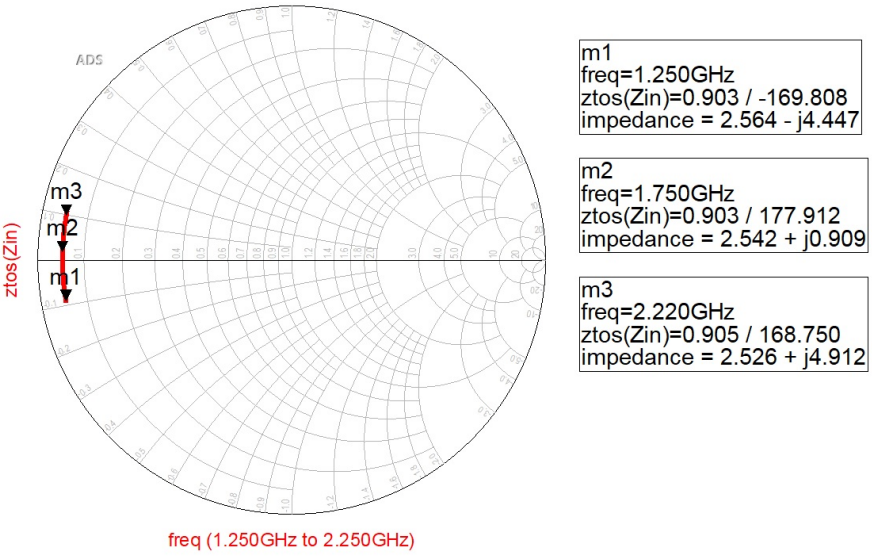


FIGURE 4.3: The input impedances from 1.25GHz to 2.25GHz on Smith Chart

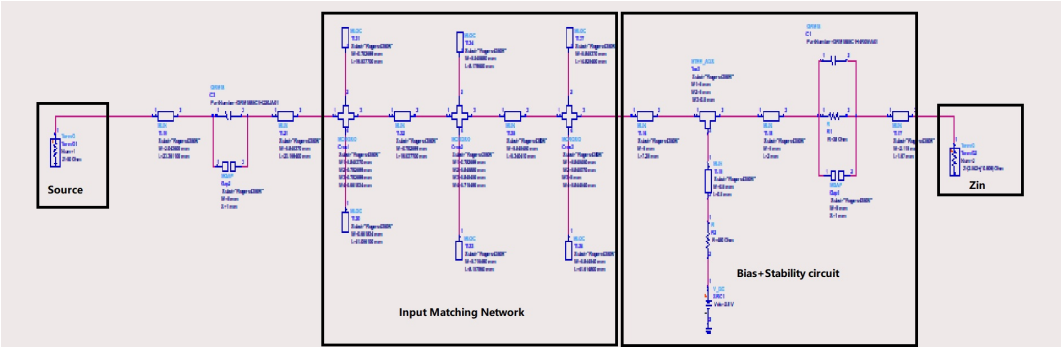


FIGURE 4.4: Broadband Input section schematic circuit

to 2.25GHz in the simulation. The main concept of the input matching network is to adapt the standard reference impedance of 50Ω to the optimum input impedance to minimize the mismatch and preserve the gain of the stage. Thus, the bandwidth can be as large as possible. An understanding of the multistage matching networks is provided in Section 3.2.2. Furthermore, the microstrip line is more accessible for tuning by ADS, and can be placed on the PCB easily. Therefore, only the distributed elements are applied to the matching circuit design. Other aspects include the gate biasing and stability circuit, which are discussed in Sections 3.3.1 and 3.1.2, respectively. Moreover, this network is not the final network to be fabricated, the size of the real amplifier topology should be further optimized. Therefore, this network only for ideal amplifier simulation. The Following chapter introduces the fabrication topic.

Fig 4.5 illustrates the simulation result of S_{11} and S_{21}. S_{11}, which ranges from 1.5GHz to 2GHz is lower than -10dB, and the majority region is lower than -15dB. Thus, the reflection coefficient S_{11} can be optimized on a smaller bandwidth. For example, by reducing the simulation bandwidth from 1.3GHz to 2.20GHz, the reflection coefficient S_{11} can be improved and made lower than -15 dB in the full range. However, this result is enough to be used for broadband amplifier design. On the other hand, S_{21} is nearly smooth, and the difference is smaller than -3dB from 1.5GHz to 2GHz. Therefore, this result is acceptable.

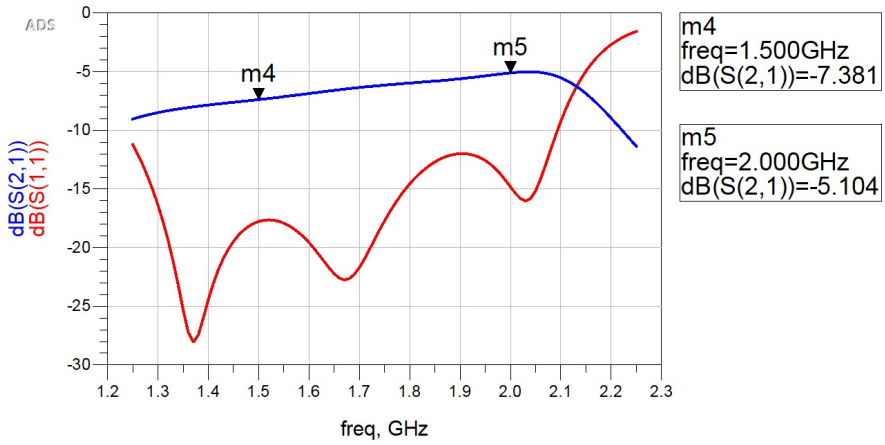


FIGURE 4.5: S_{11} and S_{21} for the final broadband input section schematic

4.2 Conventional Class-F/Inverse-F Power Amplifier

The input section has been completely introduced. The above topology represents the final design for all amplifier types. This section compares all types of Class-F power amplifiers with the ideal output section. The input section must be the same for all types of amplifiers. In fact, the final comparison results are mildly influenced by the input section and strongly depend on the output matching network, as better highlighted in the following, output section for the power amplifier. The four Class-F design topologies are introduced with ideal elements and then compared. The best topology is selected to realize the final power amplifier to be fabricated.

4.2.1 Conventional Class-F power amplifier

Fig 4.6 presents the large-signal analysis for the conventional Class-F power amplifier, whose the analysis theory is based on the harmonic balance method. The output section is an ideal network as introduce in Section 3.2.1, and the output section is the same as Fig 3.16, and the realistic network (non-ideal) is used to build the input section, as illustrated in Fig 4.4. The gate biasing is -2.8V. The drain basing is 28V. While, the load is 50Ω, the available power is 28dBm from the input port, and the fundamental frequency is 1.75GHz. These test conditions are the same as the following amplifiers type. The only difference is the output section used to indicate which is the best.

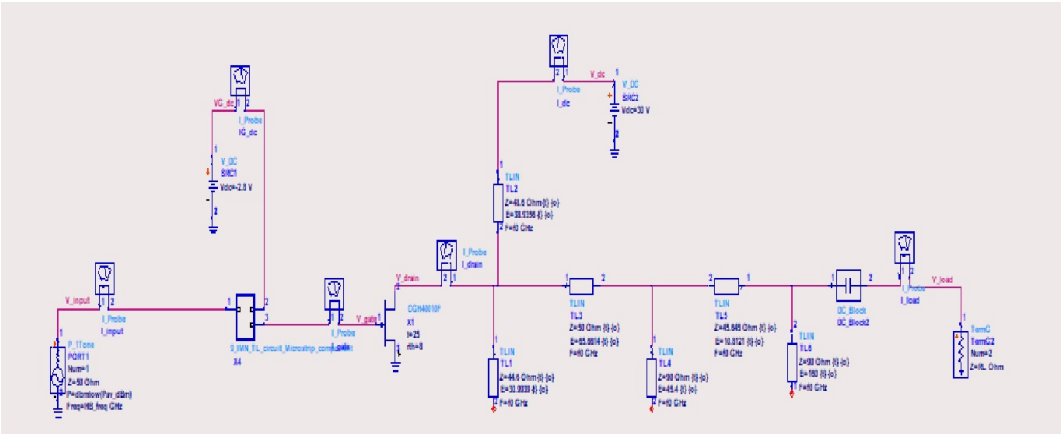


FIGURE 4.6: Large-signal analysis for ideal conventional Class-F amplifier

Fig 4.7 to Fig 4.10 present the simulation results of the amplifier. Fig 4.7 presents the fundamental, second, and third-order harmonic intrinsic impedance on the Smith Chart. Due to the simulated frequency from 1.5GHz to 2GHz as the required bandwidth, the intrinsic impedances are no longer a single node, and the position at 1.75GHz is shifted because of the parasitic elements. Fig 4.8 provides the efficiency, PAE, and output power versus the available input power. As observable, the simulated results reach the maximum value when the available power is around 30dBm within the bandwidth.

Fig 4.9 display the efficiency, PAE, gain, and output power at 30dBm available power (parameter ipow = 30 dBm) within the bandwidth, the amplifier reaches its maximum performance when the available power is around 30dBm as illustrated in Fig 4.8. The efficiency and PAE are the critical performance of the amplifier. As can be seen, the maximum efficiency and PAE are registered at the center frequency from 1.6GHz to 1.75GHz. Then, the results being to drop to 50% even though the input section is broadband. The output power is 40dBm, and the transducer gain (GainT) is around 14dB and likewise slowly decrease after 1.75GHz. Finally. Fig 4.10 provides the S-parameters for the amplifier.

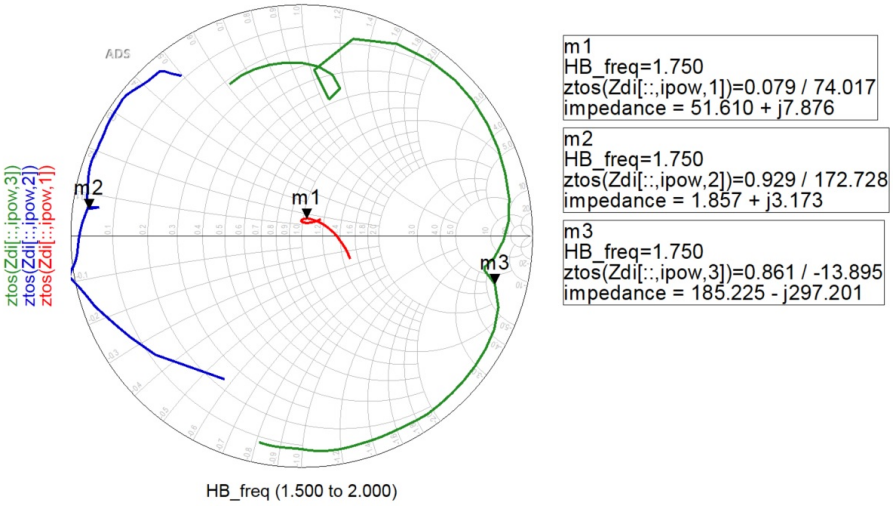


FIGURE 4.7: Fundamental and harmonics drain intrinsic impedance for ideal conventional Class-F amplifier

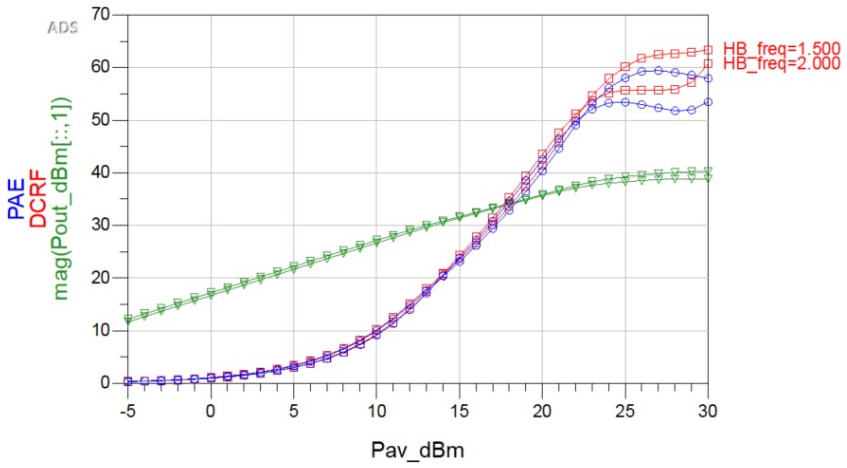


FIGURE 4.8: Efficiency, PAE, and output power for ideal conventional Class-F amplifier VS available power

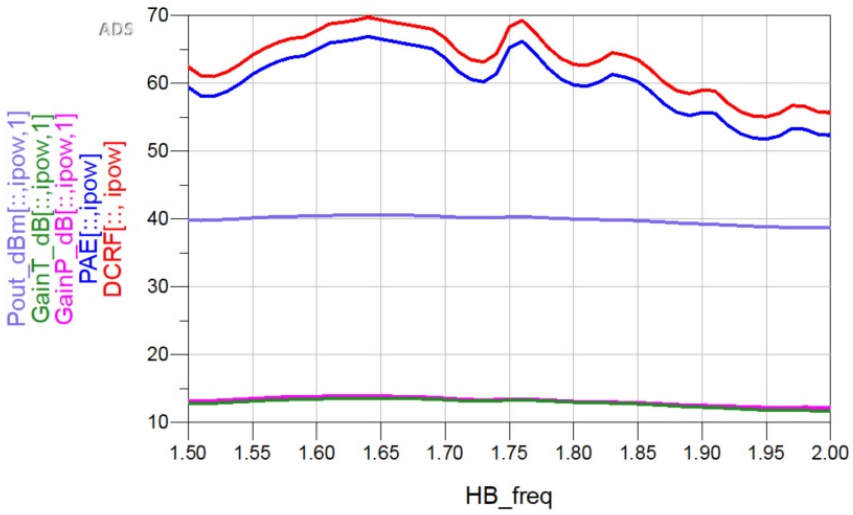


FIGURE 4.9: Efficiency, PAE gain, and output power from 1.5GHz to 2GHz for ideal conventional Class-F amplifier VS frequency

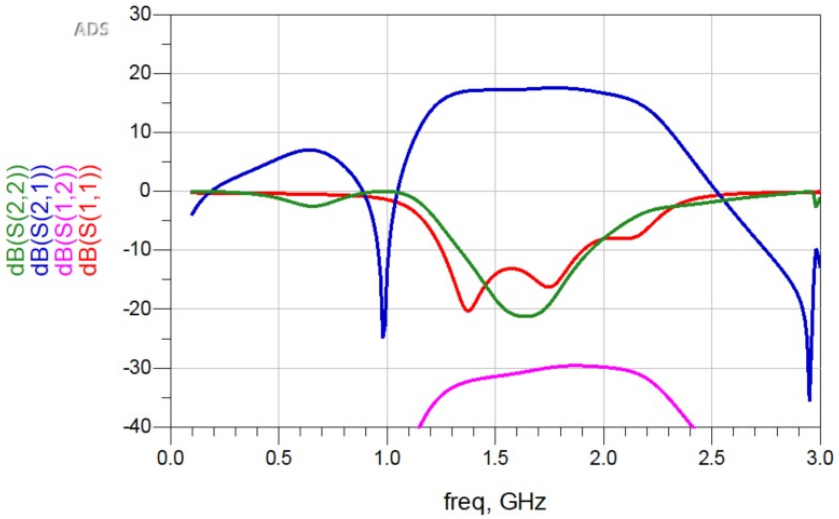


FIGURE 4.10: S-parameters for ideal conventional Class-F amplifier VS frequency

4.2.2 Conventional inverse Class-F power amplifier

The ideal conventional inverse Class-F power amplifier is depicted in Fig 4.11. The input section is a realistic network, while the output section is an ideal network with transmission lines, and the output section has introduced in Section 3.2.2, and it is the same as Fig 3.19. The test condition for the large-signal analysis is the same as in Conventional mode Class-F. Fig 4.12 presents the fundamental and harmonics intrinsic impedances locus on the Smith Chart, for which the simulated frequency range is from 1.5GHz to 2GHz. The fundamental frequency intrinsic impedance is similar to the Class-F amplifier. However, the second harmonic intrinsic impedance locus is switched to the open-circuit condition, and the third harmonic intrinsic impedance locus is located in the short-circuit condition. Therefore, this result reveals that the amplifier is the inverse type.

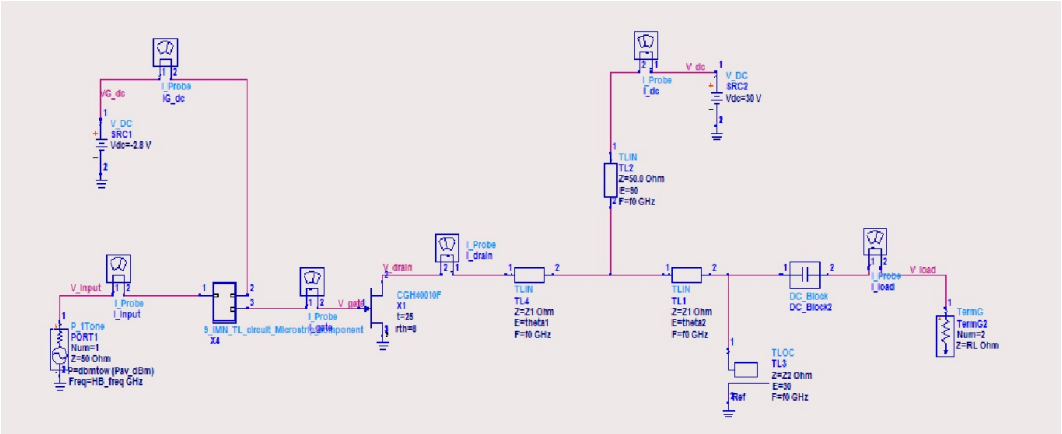


FIGURE 4.11: Large signal analysis for ideal conventional inverse Class-F amplifier

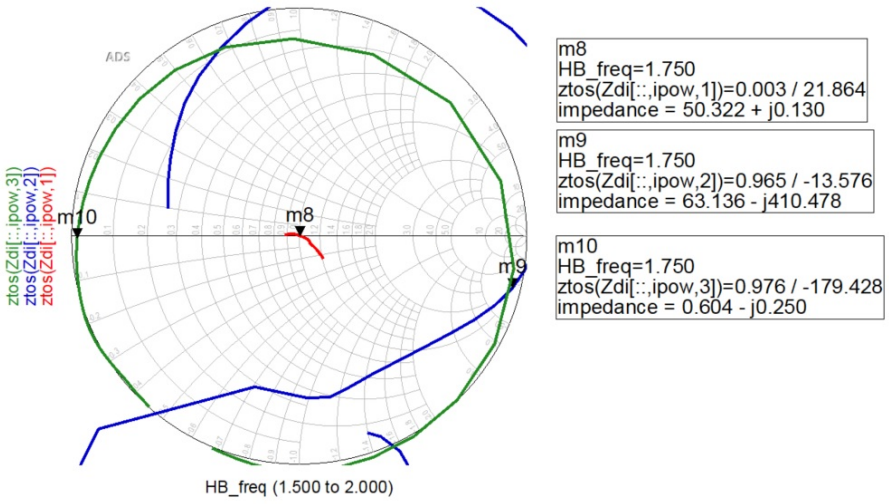


FIGURE 4.12: Fundamental and harmonics drain intrinsic impedance for ideal conventional inverse Class-F amplifier

Fig 4.13 presents the efficiency, PAE and output power. As observable, the efficiency and PAE nearly reach the maximum at around 30dBm input available power. The output power level begins to saturate after 25dBm, which is similar to the conventional Class-F amplifier. Fig 4.14 provides the above performance within the bandwidth. The efficiency and PAE are

lower prior to 1.70GHz, and from 1.70GHz to 1.80GHz, the efficiency and PAE as smooth and at 70%. However, after 1.80GHz, the efficiency and PAE become more unstable. The output power is around 40dBm, and the transducer gain is about 14dB within the bandwidth. Fig 4.15 presents the S-parameters for the inverse power amplifier.

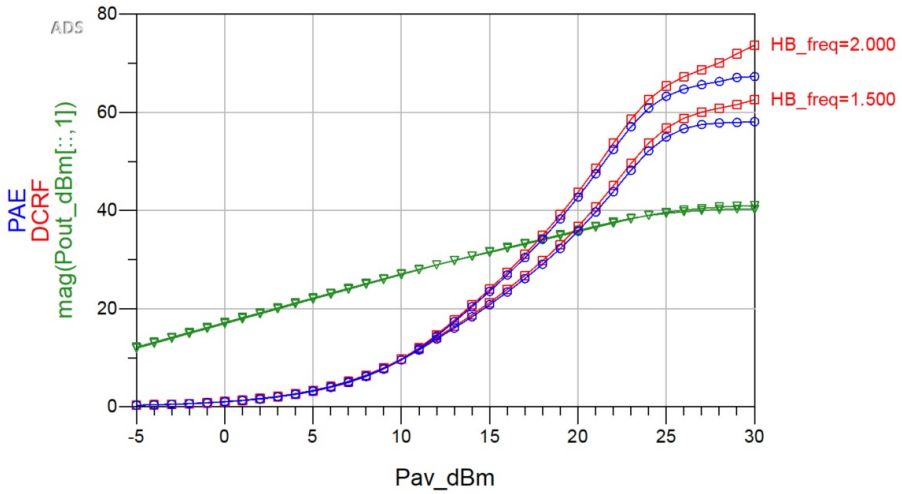


FIGURE 4.13: Efficiency, PAE, and output power for ideal conventional inverse Class-F amplifier VS available power

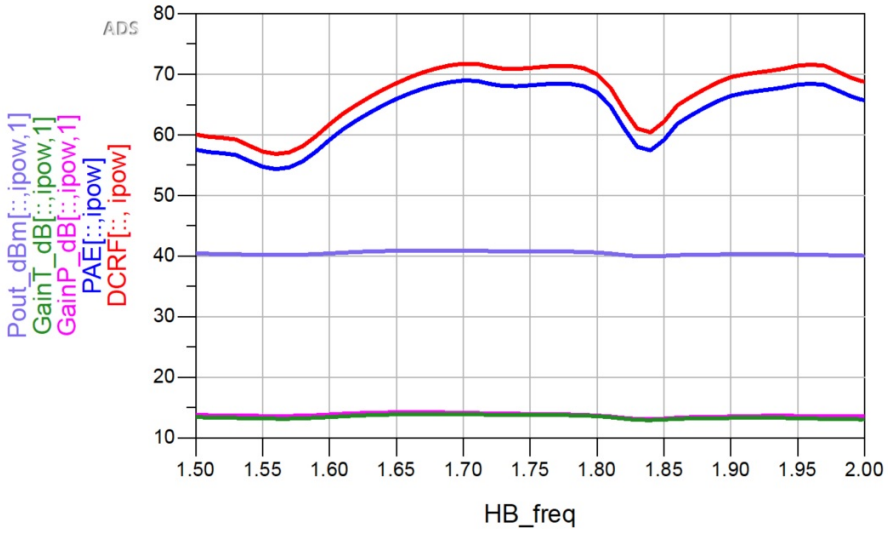


FIGURE 4.14: Efficiency, PAE, gain, and output power from 1.5GHz to 2GHz for ideal conventional inverse Class-F amplifier VS frequency

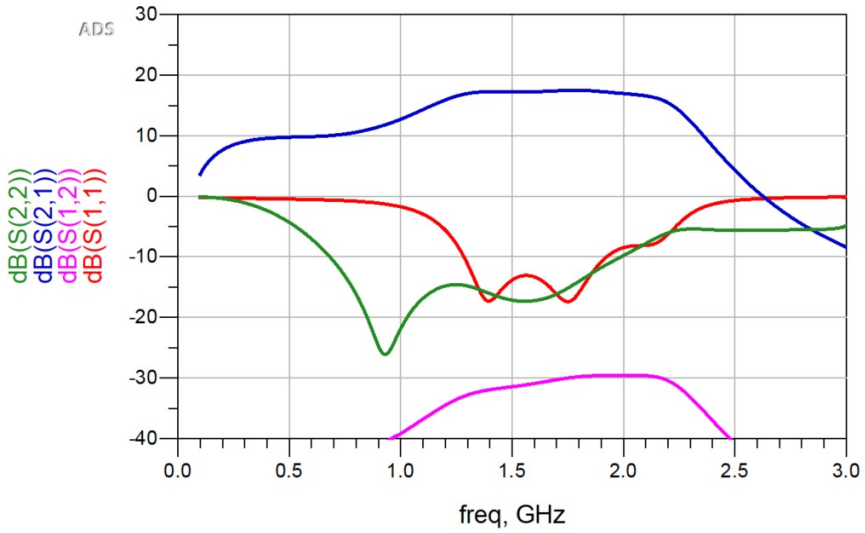


FIGURE 4.15: S-parameters for ideal conventional inverse Class-F amplifier vs frequency

4.3 Continuous Mode Class-F/Inverse-F Power Amplifier

The continuous mode analysis procedure is the same as the conventional mode: The input section can use the final network from Section 4.1 and executes the large-signal simulation with the ideal output section. The ideal output section can be taken from Section 3.2.3 and Section 3.2.4 in Chapter 3, which used the transmission lines to create the output matching network.

4.3.1 Continuous mode Class-F power amplifier

Fig 4.16 illustrates the large-signal analysis for the continuous mode Class-F power amplifier. The output section includes third-order and second-order harmonic networks to improve bandwidth and an additional fundamental network to match the fundamental frequency, and output section network is the same as Fig 3.25 and is discussed in Section 3.2.3. The continuous mode output section is more complicated compared with conventional amplifiers for obtaining better and more constant efficiency across the band. Fig 4.17 illustrates the drain intrinsic impedance locus for the amplifier. The pink and indigo colour represent the ideal impedance locus for the fundamental and the second-order harmonic impedances, respectively. The other locus is the real intrinsic impedance for the amplifier. However, because the output matching circuit is complex, there exists no precise analytic method to calculate the parameters of each transmission line. Therefore, the real impedance differs from the ideal case, especially the second-order harmonic impedance. It shifts from the ideal locus, causing the efficiency to decrease.

Fig 4.18 presents the efficiency, PAE, and output power. The efficiency and PAE abruptly decrease-upon reaching the maximum value at 30dBm, and the output power level likewise decreases has after 30dBm. Fig 4.19 displays the performance within the bandwidth. Here, the efficiency and PAE are more stable than conventional amplifiers. However, the results decrease by about 10% within the overall bandwidth because the second-order harmonic is not controlled correctly. The S-parameters are presented in Fig 4.20.

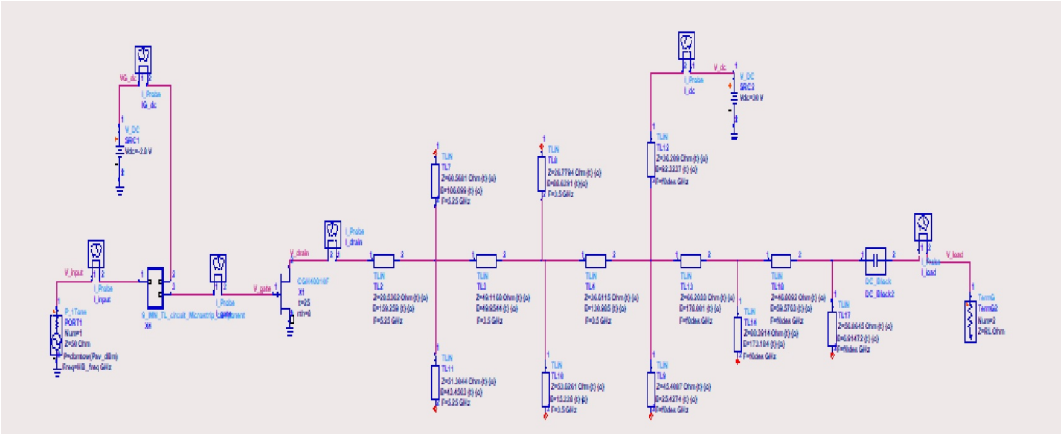


FIGURE 4.16: Large signal analysis for ideal continuous mode Class-F amplifier

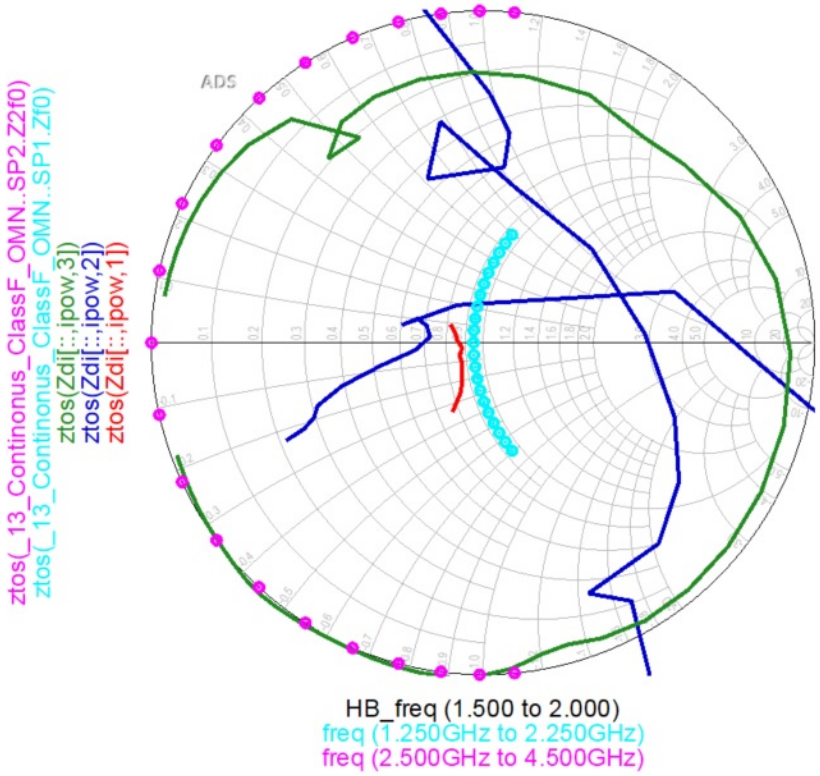


FIGURE 4.17: Fundamental and harmonics drain intrinsic impedance for ideal continuous mode Class-F amplifier

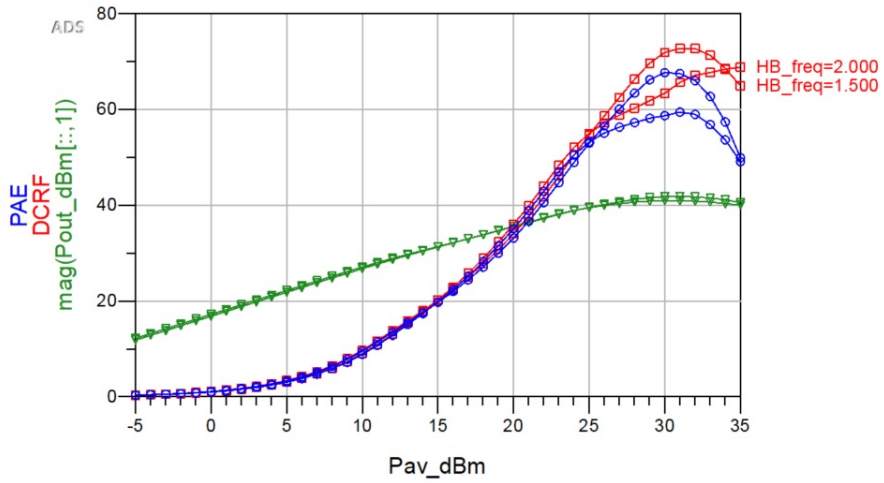


FIGURE 4.18: Efficiency, PAE, and output power for ideal continuous mode Class-F amplifier VS available power

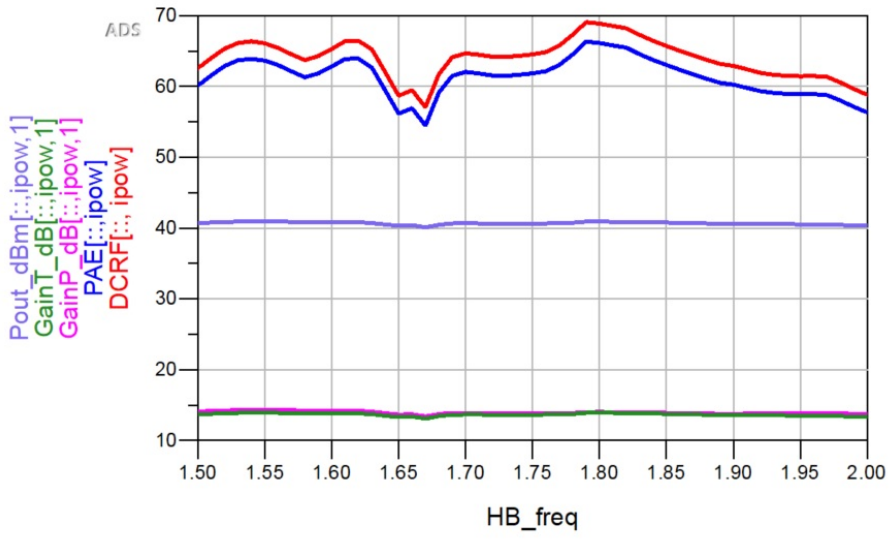


FIGURE 4.19: Efficiency, PAE, gain, and output power from 1.5GHz to 2GHz for ideal continuous mode Class-F amplifier VS frequency

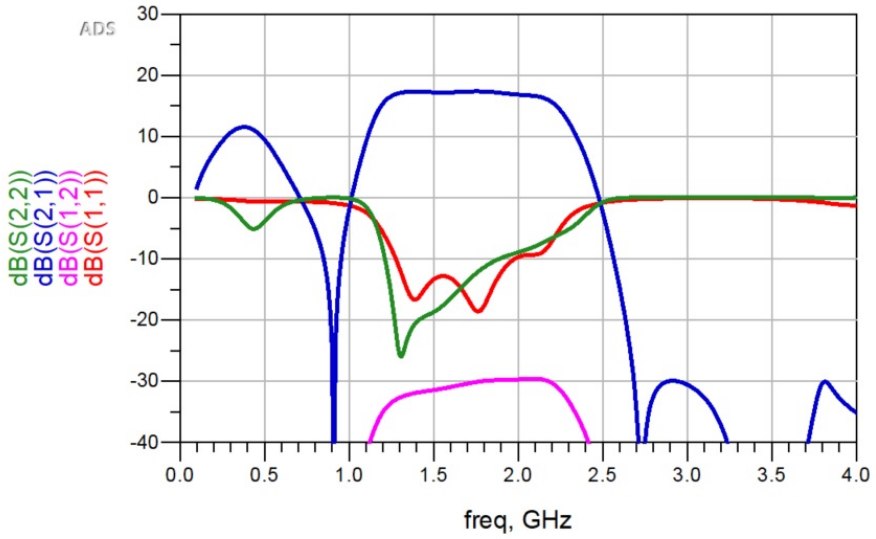


FIGURE 4.20: S-parameters for ideal continuous mode Class-F amplifier VS frequency

4.3.2 Continuous mode inverse Class-F power amplifier

The ideal continuous mode inverse Class-F power amplifier is similar to the continuous mode Class-F, whose the output section is the same in Fig 3.29 and discussed in Section 3.2.4. The large-signal analysis is presented in Fig 4.21 for the same test condition as before. Fig 4.22 provides the impedance locus for the continuous mode inverse Class-F amplifier. The fundamental frequency impedance locus is around the center (50Ω), and the second-order harmonic impedance controlled following the ideal intrinsic impedance locus. Therefore, the efficiency and PAE are better than in the continuous mode Class-F.

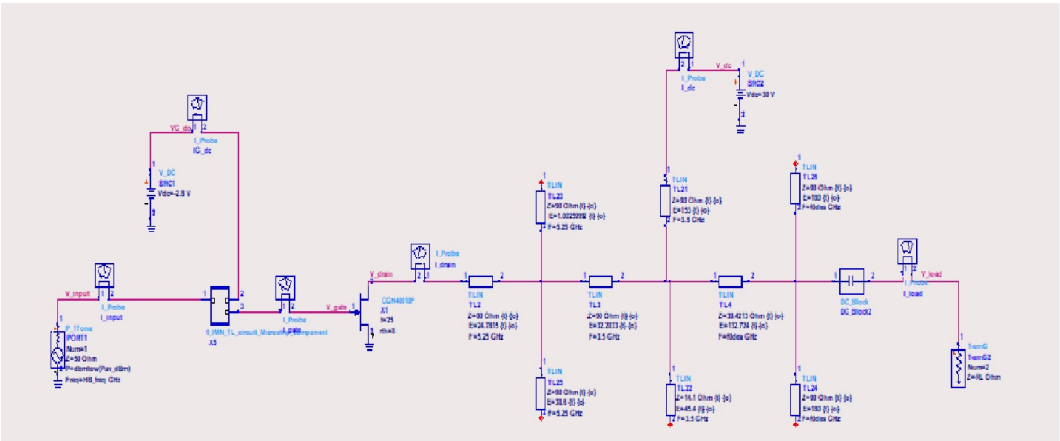


FIGURE 4.21: Large signal analysis for ideal continuous mode inverse Class-F amplifier

Fig 4.23 reveals that the efficiency and PAE are maximum for input power grater than 30 dBm. Meanwhile, Fig.4.24 displays the performance of the amplifier within the overall bandwidth. Here, the efficiency and PAE are nearly smooth while remaining high. The output power and transducer gain drop slowly from 1.95GHz to 2GHz, but this small drop can be ignored for the entire bandwidth due to the drop at the edge of the band.

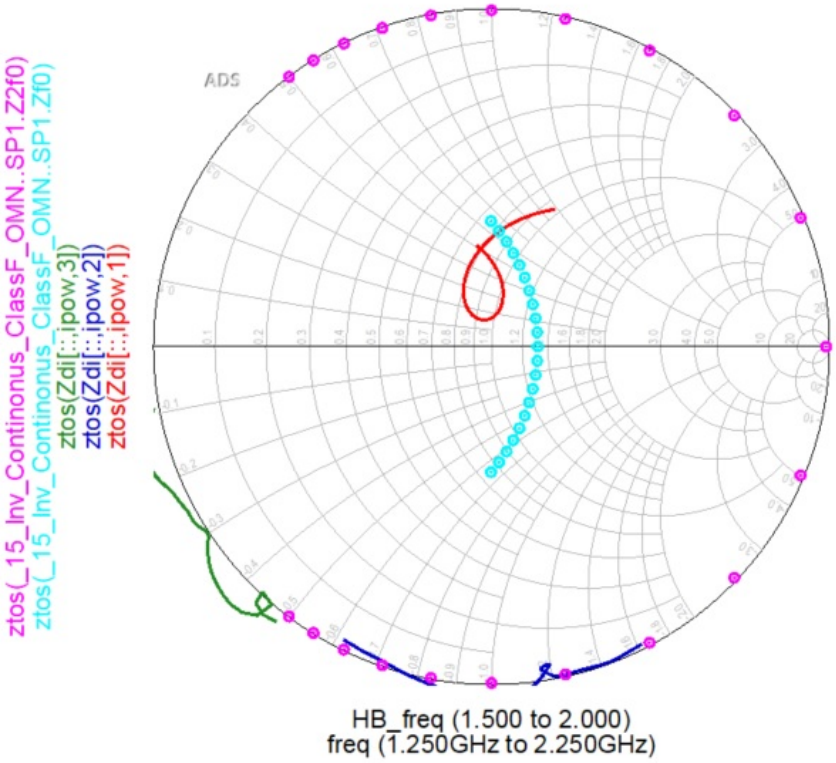


FIGURE 4.22: Fundamental and harmonics drain intrinsic impedance for ideal continuous mode inverse Class-F amplifier

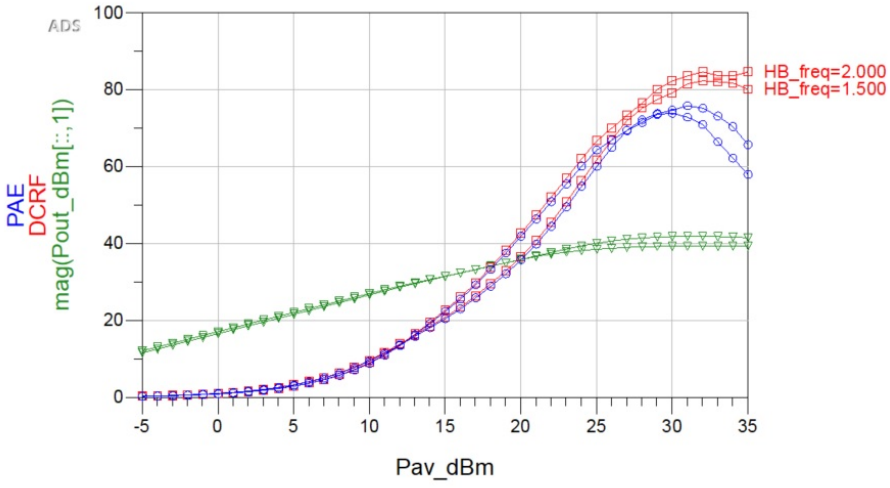


FIGURE 4.23: Efficiency, PAE, and output power for ideal continuous mode inverse Class-F amplifier VS available power

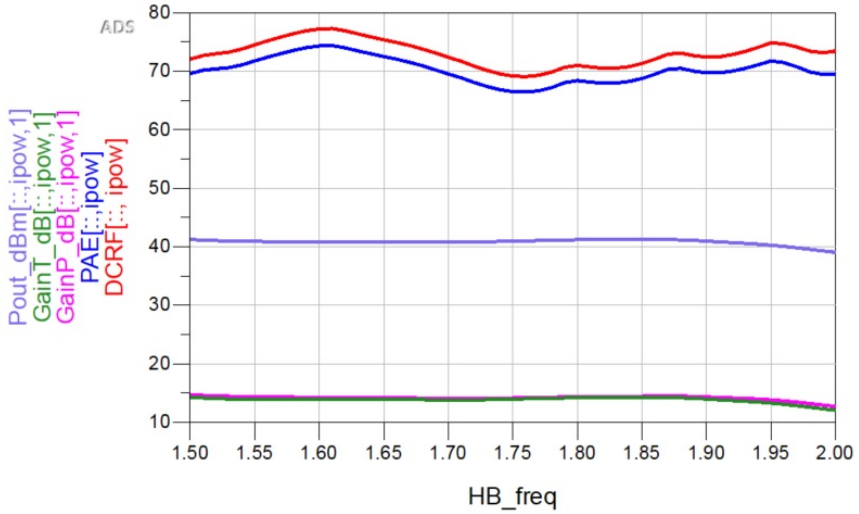


FIGURE 4.24: Efficiency, PAE, gain, and output power from 1.5GHz to 2GHz for ideal continuous mode inverse Class-F amplifier VS frequency

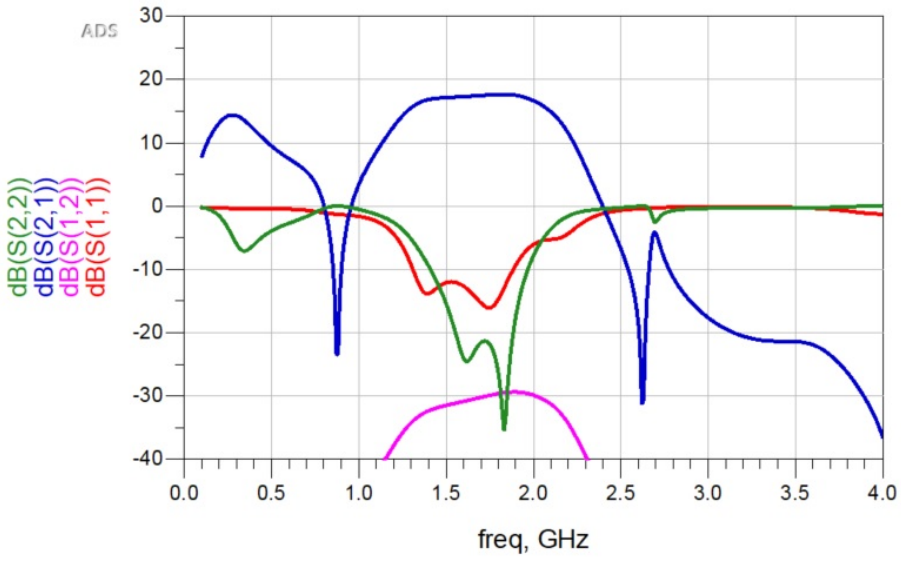


FIGURE 4.25: S-parameters for ideal continuous mode inverse Class-F amplifier VS frequency

4.4 Results Discussion

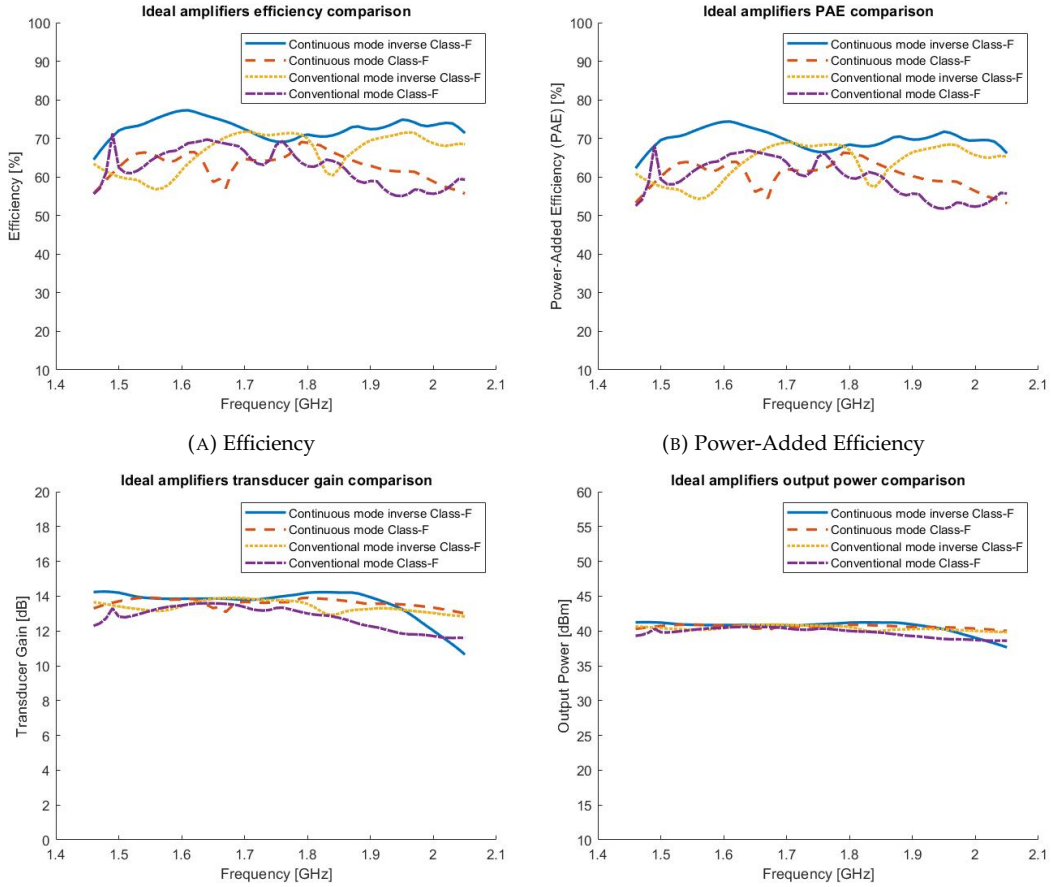
This chapter describes the simulation results for all types of ideal Class-F/F^{-} power amplifiers. An ideal amplifier means the output section is the ideal network, but the input section is not. Fig 4.26 illustrates the simulation results of the whole type of the power amplifiers, some conclusions can be summarized to indicate the best performance amplifier. The conventional class-F/F^{-} topology has a simpler output matching network for the amplifier. Thus, most output matching networks can be applied using the analytical method to determine each component's approximate value. The analytical method can reduce many tuning procedures during the output matching network build. As a result, the circuits are more accurate, that the performance of the amplifier is excellent. However, the conventional mode power amplifiers are difficult to support the broadband application, as illustrated in Fig 4.26, the conventional mode amplifiers maintain high efficiency/PAE at only a part of the bandwidth, which around 200MHz, and the efficiency/PAE decreases when outside of this bandwidth. As such, this result does not meet the design requirements. Therefore, so the conventional Class-F power amplifiers cannot be applied (fabricated) to this thesis.

The continuous mode Class-F/F^{-} topology can be applied to design the broadband amplifier through the multi-harmonics-controlled circuits. The idea here is to build a separate output matching network to match each frequency band. As illustrated in Fig 4.26, the efficiency and PAE are smooth within the entire bandwidth, with only a small drops during a short part of the bandwidth, after which it returns to the original position immediately. Therefore, the efficiency and PAE results can be approximated as smooth while maintaining the high results. As a consequence, the continuous mode amplifiers satisfy our design requirements. Moreover, the continuous mode inverse Class-F amplifier has higher efficiency and PAE within the entire bandwidth than continuous mode Class-F. In addition, the continuous mode inverse amplifier has a simpler output section network compared with continuous mode class-F. Therefore, the tuning procedure is more accurate and accessible during the amplifier design.

Fig 4.26(C) and Fig 4.26(D) illustrate the transducer gain and the output power. The results are similar for all types of amplifiers, with only 1-2dB/dBm difference in the bandwidth. Therefore, the transducer gain and the output power results are not important to evaluate the ideal amplifiers. Instead, the efficiency/PAE result is the essential parameter to evaluate the best performance amplifier. Thus, the final decision is to use a continuous mode inverse Class-F amplifier to perform the layout design and fabrication. Table 4.1 provides the specific performance parameters of all power amplifier types, and this table can observe each amplifier's simulation results clearly.

Items	Efficiency[%]	PAE[%]	Transducer Gain[dB]	Output Power[dBm]
Conventional Mode Class-F	58-70	53-65	11-14	39-40
Conventional Mode Class-F^{-}	58-72	53-70	13-14	40-41
Continuos Mode Class-F	63-70	58-68	13-14	40-41
Continuos Mode Class-F^{-}	71-80	69-78	12-14	39-42

TABLE 4.1: Comparison results of the ideal power amplifiers from 1.5GHz to 2GHz



(A) Efficiency

(B) Power-Added Efficiency

(C) Transducer Gain

(D) Output Power

FIGURE 4.26: Comparison results of the ideal power amplifiers

Chapter 5

Fabrication and Evaluation

5.1 Microstrip Circuit Design

The ideal continuous mode inverse Class-F amplifier was considered to be realistic because it demonstrated the best performance. Therefore, this chapter provides the details of the fabrication and evaluation of the amplifier. The amplifier circuit should be implemented using hybrid technology. The device and lumped components should be placed on the PCB, and the ideal transmission line must be transformed into the real microstrip line. The previous chapters demonstrate the real input section with the microstrip lines. Thus, the next step is to further optimize the size of the input section network and transfer the output section to the real microstrip line for the real amplifier structure. The series number of the PCB is **Roger4350b**. This material is suitable for broadband application thanks to its the stable dielectric over a broad frequency range. The main parameters of the PCB as listed in Table 5.1.

Substrate thickness (H)	0.762 mm
Relative dielectric constant (Er)	3.66
Relative permeability (Mur)	1
Conductor conductivity in Siemens/meter (Cond)	5.88e+7
Cover height (Hu)	1.0e+036
Conductor thickness (T)	35 um
Dielectric loss tangent (TanD)	0.0031

TABLE 5.1: Main parameters of Rogers4350b PCB

Fig 5.1 and Fig 5.2 display the complete topology of the continuous mode inverse Class-F amplifier with microstrips. In particular, Fig 5.1 presents the input section, and Fig 5.2 presents the output section. Due to the size of the amplifier that must be considered for the fabrication, the topology of the input matching network is changed to satisfy the design rules. The output matching network likewise simplifies the network for easier tuning and PCB design.

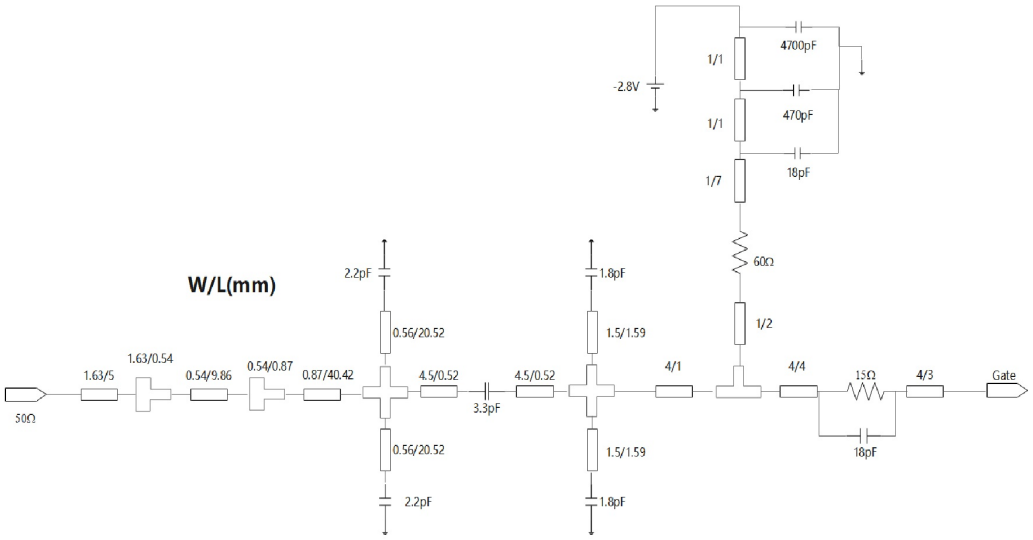


FIGURE 5.1: Completely continuous mode inverse Class-F RF power amplifier input section

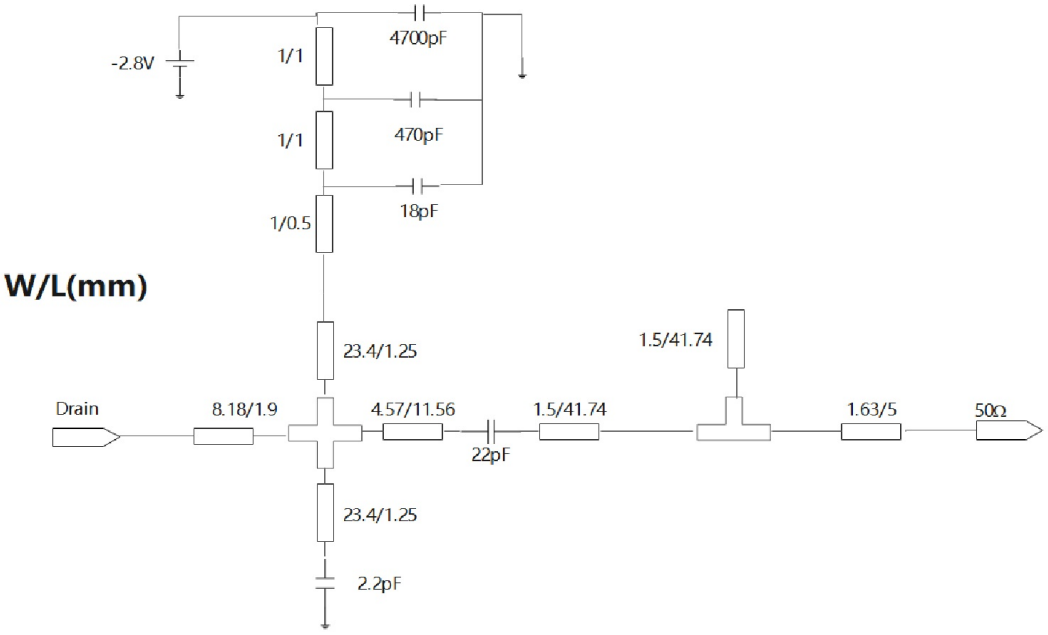


FIGURE 5.2: Completely continuous mode inverse Class-F RF power amplifier output section

5.2 Power Amplifier Simulation Results

Fig 5.3 presents the intrinsic impedance for the fundamental and high-order harmonics after tuning and optimization. Fig 5.4 displays the results of the efficiency/PAE and the output power. The amplifier can reach its maximum performance after 30dBm. The efficiency is larger than 70% with the microstrip topology, an acceptable result because the efficiency of the real amplifier is undoubtedly larger than 60%, thereby fulfilling the design requirement. Meanwhile, the output power reaches the maximum at 40dBm, while likewise meets the necessary requirement.

Fig 5.5 illustrates the final simulation results within the bandwidth. The bandwidth range of the simulation is from 1.45GHz to 2.05GHz to observe the results more precisely. The final simulation results of the efficiency/PAE can maintain high efficiency within the bandwidth, and the output power is around 40dBm in the entire bandwidth. Moreover, the transducer gain is around 14dB within the bandwidth. Fig 5.6 presents the S-parameter. S_{11} cannot be lower than -10dB, since the input section is changed to satisfy the design rules. However, this parameter is not essential for the conclusion. Thus, it can be accepted at the moment and further optimized in the future. Thus, the final result of the real amplifier is acceptable and satisfies all the requirements.

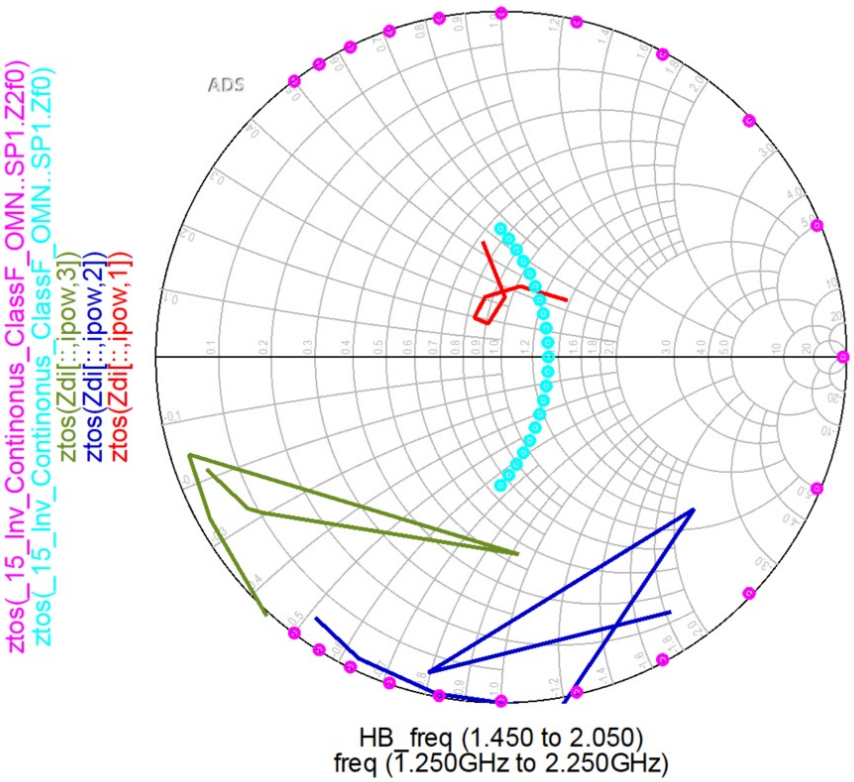


FIGURE 5.3: Fundamental and harmonics drain intrinsic impedance for completely continuous mode inverse Class-F amplifier

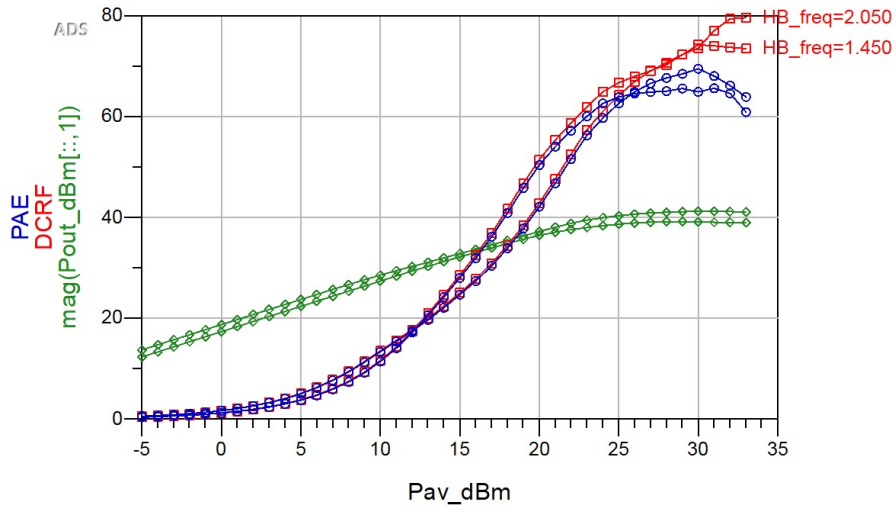


FIGURE 5.4: Efficiency and output power for completely continuous mode inverse Class-F amplifier

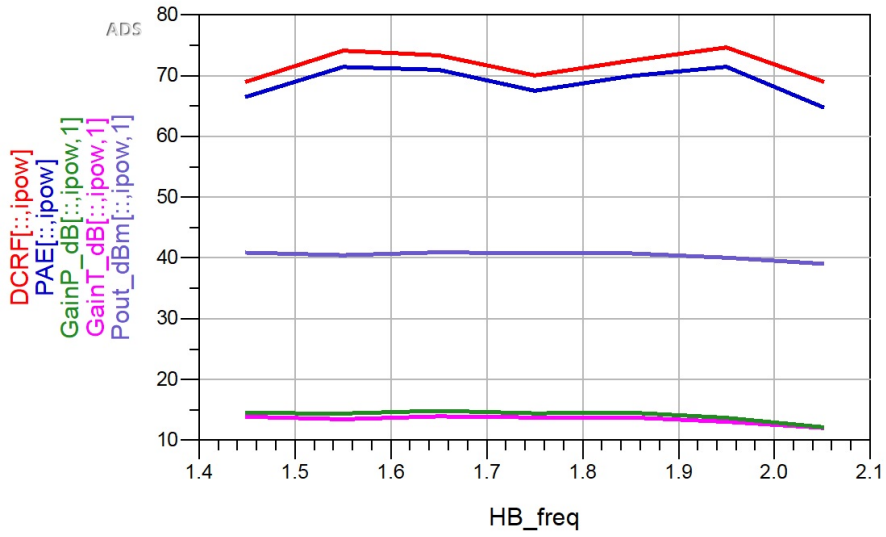


FIGURE 5.5: Efficiency, gain and output power from 1.45GHz to 2.05GHz for completely continuous mode inverse Class-F amplifier

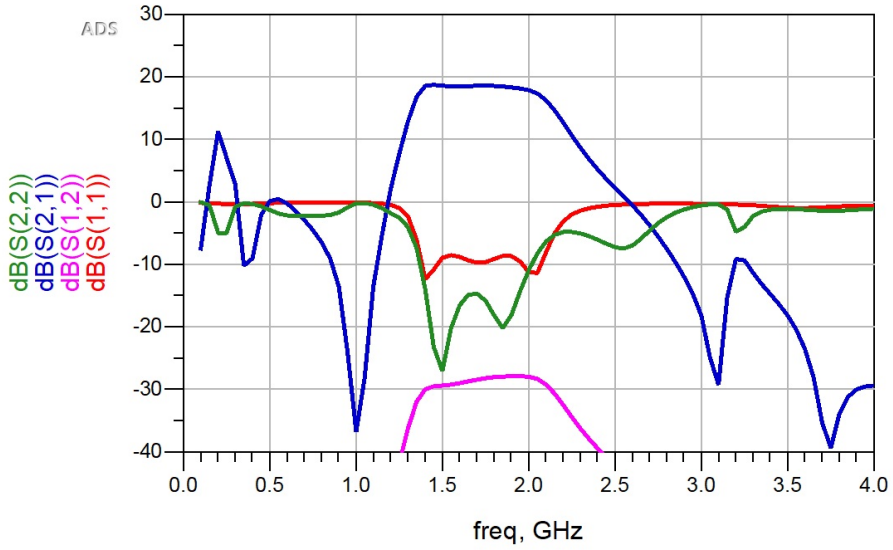


FIGURE 5.6: S-parameters for completely continuous mode inverse Class-F amplifier

5.3 Layout Design

Fig 5.7 illustrates the layout of the power amplifier. The capacitors and resistors used the SMD components to be implemented on the PCB board. However, this layout is not complete. The ground plane should be added and connected to each capacitor, and the open circuit on the right side is too long. Therefore, the circuit should be curve to create a bend. Then, this layout can perform the EM simulation with further work.

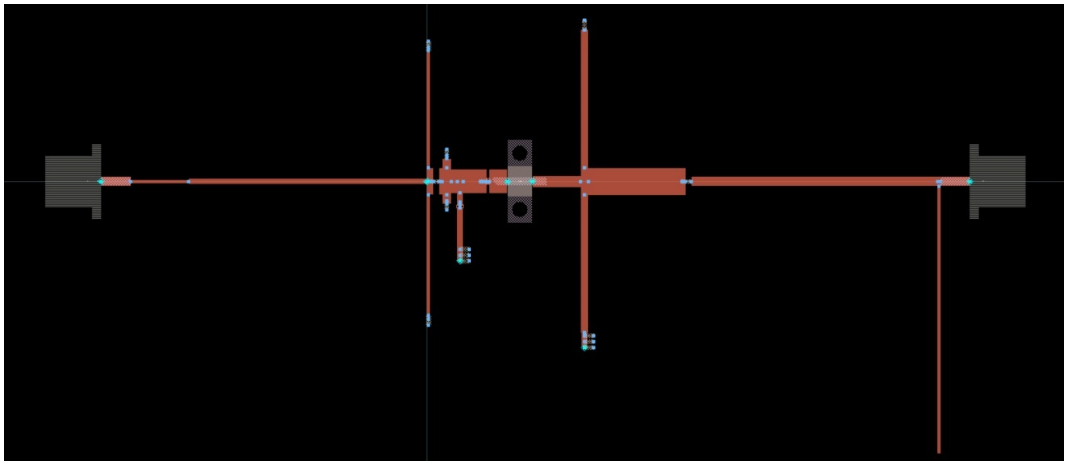


FIGURE 5.7: Completely layout for the final design

Chapter 6

Final Conclusion

6.1 Thesis Conclusion

This thesis aimed to identify the performance of a high-efficiency RF power amplifier. The topology of the amplifier is based on the entire family of Class-F because the efficiency can reach 100% in theory and there is a low influence of the active device self-property. Furthermore, the bandwidth of the amplifier is broadband, meaning the efficiency must be as large as possible with res;ect to the required bandwidth. The best Class-F amplifier type is the continuous mode inverse power amplifier with the ideal topology and transferring the ideal topology to the real network. Based on the above research and evaluated results, the continuous mode inverse power amplifier has maximum efficiency within the entire bandwidth and does not vary as much as the frequency changes. Moreover, the output section of this amplifier does not need to provide the an addition network to match the fundamental frequency, so the network can focus solely on the second-order harmonic tuning. Therefore, the fundamental frequency does not need to do much more work when performing the tuning procedure, which can easily increase the efficiency at the high frequency band (after 1.75GHz) to maintain the maximum efficiency.

6.2 Further Work of This Project

This thesis provides complete understanding to research and develop the high-efficiency RF power amplifier. It can help a beginner to comprehend understanding the entire process for amplifier design in practice. However, some further works still must be completed. First, the amplifier must perform the EM simulation by ADS to evaluate the layout performance and PCB product. In the subsequent step, the PCB board must be evaluated with the real test environment. Then, the results of the amplifier can be provided. Moreover, the test signal is the QAM/OFDM in the current telecommunication system with a transmission signal in binary code, it that can be plotted on the constellation. Therefore, linearity is important for the amplifier as well. Otherwise, the signal (binary code coordinate) at the output will shift on the constellation resulting in the output waveform distortion. Thus, if the continuous mode inverse Class-F amplifier has poor linearity, requiring more optimization to increaser the linearity, the power back-off and efficiency will drop significantly. As such. the efficiency enhancement must be applied to the amplifier, such as building a Doherty topology to the applied auxiliary amplifier to increase the efficiency.

Bibliography

[1] Firas Mohammed Ali. "Class-F RF Power Amplifier with a New Load Network Configuration". In: *High Frequency Electronic* (2017), pp. 22–38.

[2] Keith Benson. *GaN Breaks Barriers—RF Power Amplifiers Go Wide and High*. Tech. rep. Analog Devices, 20.17. URL: https://www.allaboutcircuits.com/industry-articles/gan-breaks-barriersrf-power-amplifiers-go-wide-and-high/.

[3] Vincenzo Carrubba. "Novel Highly EfficientBroadband ContinuousPower Amplifier Modes". PhD thesis. 2012, pp. 63–66.

[4] Osman Ceylan, Lazaro Marco, and Sergio Pires. "Refine biasing networks for high PA low-frequency stability". In: *Microwaves and RF* 57 (Apr. 2018), pp. 52–56.

[5] Paolo Colantonio, Franco Giannini, and Ernesto Limiti. *High efficiency RF and microwave solid state power amplifiers*. Wiley Online Library, 2009.

[6] Mustafa M Elarbi. "Electrothermal design and realization of high efficiency class F power amplifier". MA thesis. École De Technologie SUPÉRIEURE, 2018.

[7] Steven W. Ellingson. *Quarter-Wavelength Transmission Line*. [Online; accessed 2021-08-03]. Apr. 2, 2020. URL: https://phys.libretexts.org/@go/page/24231.

[8] Giovanni Ghione and Marco Pirola. *Microwave electronics*. Cambridge University Press, 2017.

[9] Andrei Grebennikov. *RF and microwave power amplifier design*. McGraw-Hill Education, 2015.

[10] Andrei Grebennikov, Nathan Sokal, and Marc Franco. *Switchmode RF and Microwave Power Amplifiers*. July 2012. DOI: 10.1016/C2011-0-04475-7.

[11] Andrei Grebennikov et al. "Load network design technique for class F and inverse class F PAs". In: *High Frequency Electronics* 10.5 (2011), pp. 58–72.

[12] F.H. Raab. "Maximum efficiency and output of class-F power amplifiers". In: *IEEE Transactions on Microwave Theory and Techniques* 49.6 (2001), pp. 1162–1166. DOI: 10.1109/22.925511.

[13] Iulian Rosu. *RF Power Amplifiers*. Tech. rep. YO3DAC.

[14] K. Tsang. "Class-F Power Amplifier with Maximized PAE". MA thesis. 2010.

[15] uniroma1. *RF Electronics Chapter 9: Impedance Matching of Power Amplifiers*. Tech. rep. 2009. URL: http://mwl.diet.uniroma1.it/people/pisa/SISTEMI_RF/MATERIALEINTEGRATIVO/Kikkert_RF_Electronics_Course/12-RF_Electronics_Kikkert_Ch9_MatchingPowerAmplifiers.pdf.

[16] Korne Vennema. *LDMOS transistors rise to occasion*. Tech. rep. Philips Discrete Semiconductors, 5.18.1999. URL: https://www.eetimes.com/ldmos-transistors-rise-to-occasion/.

[17] Ardit Veshaj. “Doherty Power Amplifier”. MA thesis. Politecnico di Torino, 2019.