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INSTITUT POLYTECHNIQUE DE GRENOBLE
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

MASTER OF SCIENCE THESIS

Design of Radiation Hardened Linear Regulator for GaN based DC-DC Converters

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Author:
Nicolas GALANTE

Supervisor:
Dr. Giacomo RIPAMONTI
Prof. Marco VACCA
Prof. Adil KOUKAB
Dr. Stefano Michelis
Prof. Carlo RICCIARDI

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Abstract

Power distribution to the High-Luminosity Large Hadron Collider (HL-LHC) detectors at CERN is a challenging task, due to the limited amount of material that can be used, to the limited cooling capability and to the presence of high levels of radiation. In this context, the use of step-down radiation tolerant DC-DC converters is of paramount importance to guarantee that the targets of power efficiency and minimization of the used material are met. A new generation of Gallium Nitride (GaN) based converters is now in development at CERN.

During recent years, the employment of GaN devices has become more and more widespread due their increased switching capabilities and power losses reduction. Nevertheless, even though GaN devices are superior to Silicon ones by many different metrics and parameters, they come with their own set of challenges in terms of circuit design.

The absence of a built-in body diode (unlike Silicon MOSFETs) eliminates reverse recovery losses in GaN transistors, since there are no minority carriers involved in the conduction. Nevertheless, the absence of such body diode leads to large negative voltages (about -2.5V, much lower than the -0.7V when using Silicon devices) on the switched node of a buck DC-DC converter during the dead times. When using a conventional bootstrapping technique to power the high-side gate drivers, this issue can lead to an overcharging of the power supply of the gate drivers, which in turn can damage irreversibly the gate driver or even the GaN transistor itself.

In this project, a linear regulator that supplies the gate drivers of a GaN device has been developed using a commercial 0.35 μm CMOS technology. Such regulator guarantees that a steady 3.3 V voltage is obtained as the power supply of the gate driver regardless of the large negative voltages reached by the switched node. The development has included the choice of the topology, its small-signal analysis, the transistor sizing, the validation of the schematic through simulations and the layout. In order to reach the targeted ultra-high levels of radiation tolerance (e.g. a Total Ionizing Dose of 100 Mrad), radiation hardening design techniques have been extensively adopted in this work, both in the schematic and in the layout phase.

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Chapter 1

Introduction

1.1 CERN

The acronym CERN stands for Conseil européen pour la recherche nucléaire (Organization for Nuclear Research) and its origins date back to the late 1940s, after the end of World War II [10]. A small number of visionary scientists from Europe and North America realised that there was the need to create a research center with a global character, both to stop the haemorrhage of minds fleeing from Europe to the United States and to provide an additional reason for unity and cohesion within a war-torn Europe. In December 1951, at a formal intergovernmental meeting of UNESCO in Paris, the creation of a "European Council for Nuclear Research" was agreed upon for the first time; two months later, a formal agreement was signed by 11 countries, a provisional council was organized, and the famous acronym CERN was born. Although our current understanding of physics goes far beyond core physics, the name has remained so for historical reasons, and a more current name we can refer to when talking about this organization is that of "European Laboratory for Particle Physics." One of the most important questions that emerged in the various meetings organized by the provisional council concerned a conceptually simple but not easy to solve question: where to build CERN? There were nominations from the Danish, Dutch, French and Swiss governments, but in the end Geneva, a Swiss city near the French border, was selected: the city's central position in the European context, the nation's neutrality during the war and its proven track record as the headquarters of several other international organizations made it prevail over the other candidates. The final convention was ratified in 1953 by the 11 original signatory countries plus the United Kingdom and in 1954 excavations began in the town of Meyrin. The importance and attractiveness of CERN over the years

grew exponentially in the world of elementary physics research; during the Cold War, CERN was one of the only places in the world where Western and Soviet scientists worked side by side and exchanged ideas. The history of CERN's accelerators is a complex and technologically rich one: In 1957, the first accelerator in CERN's history, a 600 MeV Synchrocyclotron (SC) dedicated to research in nuclear and particle physics, was turned on for the first time and began a period of honored service that would last for a full 33 years. In 1959 began to operate the Proton Synchrotron (PS), a much more advanced accelerator with a beam energy of 28 GeV that for a short period held the record for the highest energy accelerator in the world. The accelerator is still active, over the years it has been greatly enhanced and its main purpose since the 70's (when it was replaced by more advanced machines) until today is to accelerate particles to be supplied to other accelerators. The Super Proton Synchrotron (SPS) was, with its 7 km circumference, the first underground accelerator at CERN and the first to cross the French-Swiss border. Its construction was approved in 1971 and in 1976 it was turned on for the first time, quickly becoming the main workhorse of CERN; its high energy, currently equal to 450 GeV, has allowed to produce important discoveries in the field of antimatter, exotic matter and the first instants of life of the universe. Its most important achievement was the discovery of the W and Z particles of the weak interaction.

In 1989 one of the most impressive accelerators in the history of CERN started up, the so-called LEP (Large Electron-Positron Collider), a mammoth machine with its 27 km circumference. Reaching 209 GeV shortly before its dismantling in the year 2000, it allowed the consolidation of the electroweak theory and the discovery that there are three and only three twin generations of matter particles. In the year 2000 LEP was turned off and dismantled to leave room for the current flagship in the history of CERN, the famous LHC (operation started in 2008), a circular accelerator built inside the cavity in which LEP was contained that allowed to reach energy levels never seen before by man and still hold today this world record, equal to 6.5 TeV per single beam. Born to shed light on several unresolved issues in the world of physics, such as the nature of dark matter, one of the most important results obtained thanks to it was the discovery of the Higgs Boson in 2012. Since the '80s, dozens of nations from all over the globe began to be interested in collaborating and participating in the research carried out at CERN. Today CERN is a global and cosmopolitan research center, with more than 10,000 researchers

of more than 100 different nationalities. CERN has enabled scientists from all over the world to communicate through the language of science.

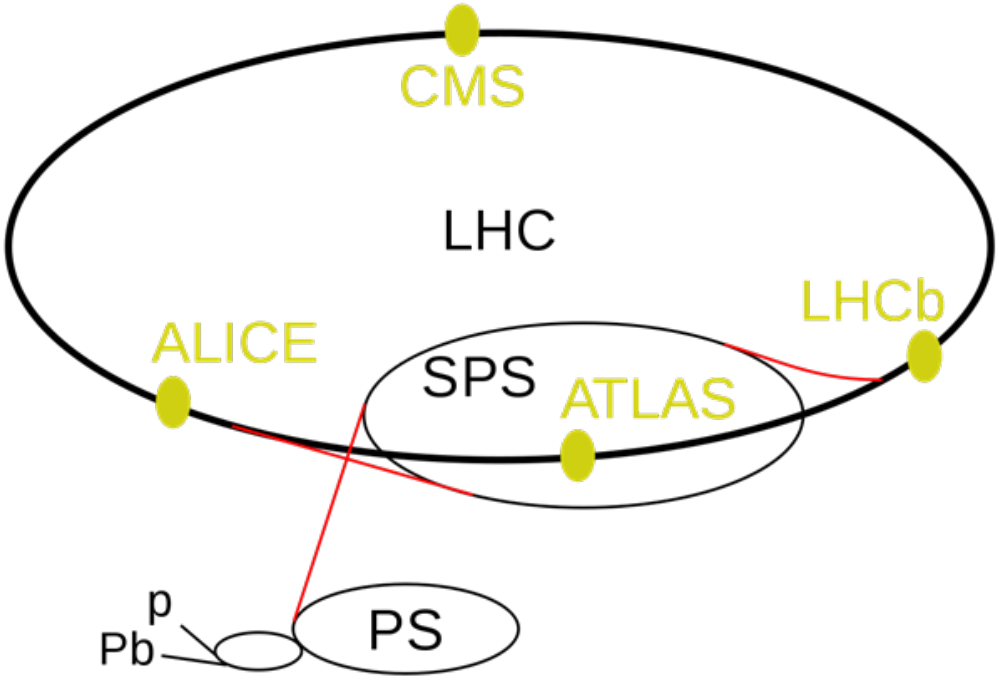

FIGURE 1.1: Accelerators and detectors at CERN.

The current system of accelerators at CERN involves a succession of different machines that accelerate particles to higher and higher energy levels until they reach the LHC, which is the last element of the chain. The smaller accelerators, in addition to this progressive system, have their own specific experimental sections to conduct experiments directly at lower energies. Starting from a simple hydrogen gas, by means of an electric field protons are stripped from electrons and accelerated in Linac 2, the first accelerator of the chain (linear), which allows the beam to reach energies equal to 50 MeV; after that, the beam is injected in succession in the Proton Synchotron Booster (PSB) to reach energies equal to 1.4 GeV, followed by the Proton Synchrotron (PS), with energies equal to 25 GeV; the protons are then accelerated up to 450 GeV in the Super Proton Synchrotron (SPS), before reaching the final accelerator, LHC, where they reach energies equal to 6.5 TeV per single beam. The beams are spun for several hours inside the LHC while the four detectors scattered around its circumference (ALICE,ATLAS,CMS and LHCb) analyze the collisions and study their nature.

The detectors are located at collision sites in order to analyze the collisions determining energy, position, velocity, angle of scattering and mass of the particles involved. Detectors are actually a complex array of circuits and sensors that can be divided into:

- Calorimeters that stop the particles and measure the energy released in the process
- Tracker detectors that track the position and velocity of the particles
- Strong electromagnets to bend the trajectory of charged particles (to distinguish them from neutral particles)

In addition to that there is the backend circuitry and converters to power all the above components.

The environment which the detector's components must endure is, as can be expected, extremely harsh, having to sustain levels of radiation of hundreds of Mrad and magnetic field that reach values up to 4 T.

The High Luminosity LHC upgrade is an upgrade set to be operational at the end of 2027 that aims to increase the luminosity of LHC by a factor of 10 [11]. An accelerator with colliding beams of particles has two main parameters:

- The beam energy, i.e. the mean energy of each particle in the beam
- Luminosity, i.e. a parameter related to the average numbers of particles in each collision

Even though the energy of the accelerator will remain the same (13 TeV), the increase in luminosity is going to raise drastically the number of particles involved in collision and subsequently the collision data magnitude. As can be expected, this upgrade is going to increase the power consumption of the detectors and this is a challenge itself. The power dissipation through Joule heating in the long cables that supply the detectors is equal to IR^2, thus in order to lower it either the resistance or the current must decrease. The resistance change would require thicker cables that would not be feasible due to the increase in cost and size; employing instead a lower current - higher voltage supply, stepping down locally the required voltages for the sensor circuits is a better strategy and it is the one that has been chosen and implemented at CERN. An example of the power distribution scheme can be observed in Figure 1.2, where each circuit domain has its own DC-DC converter that delivers the required voltage. Given that these converters must

operate in extreme conditions of radiation and magnetic fields, commercial converters available on the market could fail or get damaged; therefore the development of ASICs (Application Specific Integrated Circuits) that can sustain these conditions is required. A new generation of 48 V-input radiation-hard converters based on commercial GaN FETs is currently in development at CERN, in order to allow the power to be distributed to the detectors at a higher voltage compared to existing solutions (48V instead of 12V) [9].

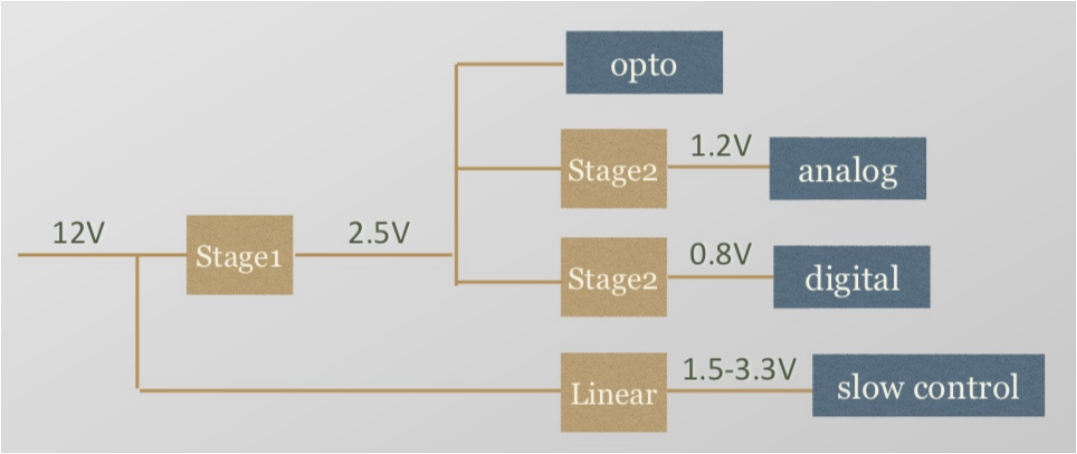

FIGURE 1.2: Power distribution at CERN.

1.2 Radiation Induced Damage and Radiation Hardening Techniques

Of all types of stress a circuit can experience, radiation is certainly one of the most dangerous ones. In typical environments where electronics circuit operate radiation is practically negligible and its effects can be neglected; in other environments, e.g. in the aerospace field, nuclear detectors or particle accelerators, its intensity is much stronger and it becomes a, if not the, major factor to take into consideration during the choice, design and layout of the circuit. [2]

1.2.1 Radiation Induced Damage

Radiation can be described as the emission or transmission of energy by particles through a medium. Particles can be either charged or neutral and cause damage to devices. Charged particles interact with the medium they are penetrating in the following ways:

- Protons through Coulomb interaction to induce ionization or atomic excitation, nuclear collisions to cause nuclear excitation or displacement, or nuclear reactions.
- Heavy ions have a behaviour very similar to protons.
- Electrons through Coulomb interaction (same as protons), nuclear scattering if they can transfer enough energy to the nucleus and x-rays Bremsstrahlung emission.

Neutral particles instead interact with the medium they are penetrating in the following way:

- Neutrons are similar to protons without the Coulomb interaction, i.e. through nuclear reaction and nuclear collision, either elastic or inelastic.
- Photons through the photoelectric effect, the Compton effect and the electron-positron pair creation.

A more effective way to categorize radiation is to do it by its effects on the sample; they can be divided into ionization effects and nuclear displacement.

In CMOS devices, ionization is mainly caused by charged particles that interact with the charged nuclei and the electrons in the material or by photons that excite electrons. The most important factor is the total energy absorbed by the device because different particles cause similar effects; the nature of the particles can be thus neglected and this effect is described by the so-called TID (Total Ionization Dose).

Nuclear displacement instead is typically caused by neutral particles, such as neutrons, that collide with the crystalline structure of the material and form traps or vacancies in the reticle. For the MOS transistors used in this work the ionization effects are the most detrimental, since nuclear displacement does not alter significantly their behaviour.

The main effect of ionization is the generation of electron-hole pairs (activation energy of around 17 eV). If the ionization happens within the gate or the substrate/channel, the charges recombine almost immediately and do not have visible effects. If the pair generation happens instead in the gate oxide, the situation becomes more problematic: in Silicon oxide electrons have a mobility many orders of magnitudes larger than holes and due to this an important fraction of the pairs does not recombine or get reabsorbed. In this case, the electrons and holes start to travel attracted respectively (if the gate

is positively biased) by the gate and the substrate. In Silicon oxide electrons have a mobility of $20\frac{cm^2}{Vs}$, while holes have a mobility of 10^{-4} to $10^{-11}\frac{cm^2}{Vs}$. This means that electrons reach rapidly the gate where they get absorbed but holes travel much slower and, due to their specific transport characteristics, can get trapped and accumulate at close to or at the SiO2-Si interfaces. The main consequence of this accumulated positive charge is a negative shift of the threshold voltage for both NMOS and PMOS, this means that in NMOS devices the absolute value of V_{th} is decreased (it becomes "easier" to turn it on), while in PMOS devices the absolute vale of V_{th} is increased (it becomes "more difficult" to turn it off). This effect does not cumulate with time indefinitely but it reaches a point of diminishing returns where the larger the shift the larger the absorption of trapped holes until it reaches a shifting saturation value.

Another possible effect is that radiation can cause a slowly generation of new traps at the Si/SiO2 interface, increasing their density by several orders of magnitude. This phenomenon is significantly slower than the positive charge accumulation. The observed effect on the transistor's energy levels is the creation of new both donor and acceptor levels between the conduction and the valence band, with the acceptor traps typically found above the Fermi level and the donor traps below it. When the bands start bending due to the presence of a bias, e.g. downwards in an NMOS transistor with a positive gate bias, if the acceptor level goes below the Fermi level then the corresponding trap captures an electron and it becomes negatively charged, repelling charges of the same sign, i.e. electrons; in the case of a negatived biased PMOS transistor with upwards bending, if the donor level goes above the Fermi Level, its trap loses an electron and becomes positively charged, repelling charges of the same sign, i.e. holes.

The described effects have the following consequences on the transistor electrical parameters:

- Threshold voltage: as stated before, both oxide hole generation and interface trap generation have a direct effect on Voltage threshold of both NMOS and PMOS devices. Given that the former is faster acting but tends to saturate with time and the latter is slower acting, the former dominates in the initial part of the IC lifecycle while the latter adds its effect after a certain amount of time. Oxide hole trapping lowers both the NMOS and PMOS thresholds, i.e. the PMOS |Vth| increase and

the NMOS |Vth| decreases, the effect is asymmetrical. Interface traps generation instead acts in a symmetrical way, increasing the absolute value of both NMOS and PMOS. The result is that in NMOS the two effects compensate at least partially, while in PMOS devices the cumulate causing a larger shifting.

- Leakage and parasitic currents: if positive charges start to accumulate in the STI oxide (Shallow Trench Isolation, which isolates different devices), a lateral parasitic path can form at the edges of an NMOS device. The result is the creation of two additional parasitic transistors connected in parallel to the original one, which can significantly increase the leakage current of the device.
- Mobility and transconductance are also degraded by interface traps at the Si/SiO2 interface.

On the other end of the spectrum of ionization effects, opposed to the cumulative effects (that depend on TID) there are the so called SEE, i.e Single Event Effects. As the name implies, they are caused by single particles that interact with one or more transistors and cause their malfunctioning. They can be either Soft Errors, i.e. they cause only a temporary failure, and Hard Errors, i.e. they cause a permanent failure.

Considering the characteristics of the design circuit and of the used 0.35 μm CMOS technology, the most relevant kinds of SEE for this work are Single Event Transients (SETs), which are soft errors consisting in the propagation of a voltage pulse generated by an incoming particle in either analog or digital circuits.

1.2.2 Radiation Hardening Techniques

Radiation hardening techniques stands for techniques employed in order to either reduce as much as possible the damage caused by radiation or to render the damage ineffective in changing the behaviour of the designed devices. They can be of three types, i.e. Radiation Hardening by process, Radiation Hardening by Layout and Radiation Hardening by design.

Radiation Hardening by Process

Radiation Hardening by process encompasses all the particular measures that can be taken to minimize the radiation induced damage by modifying

the chip manufacturing process itself. This usually means that some technological parameters could be tweaked or the process steps itself modified to reduce the radiation sensitivity. The most sensitive parts to TID are the gate oxide and the isolation oxide. Fortunately, employing a commercial deep submicron technological node increases massively the device's radiation tolerance due to its ultra thin gate oxide. The remaining radiation-induced problems can be faced with specific process changes. Among others:

- Increased gate oxide quality, e.g. employing nitrided oxides, to reduce TID induced problems.
- Reduction of the epitaxial layer thickness or increase in substrate doping to reduce SEE.
- Reduction of minority carriers lifetime, improvement in doping density profile density and increase in n+ and p+ diffusion distance to reduce SEE.
- SOI technologies due to their lower sensitivity and/or immunity to SEE or leakage between devices.

The main problem with these changes is that the potential market interest for this radiation tolerant devices is small and therefore there is no interest from the VLSI manufacturers to make them; in addition to this, most of these processes have typically a lower yield than standard commercial ones. The final result is an increase in cost that makes these techniques too expensive to be employed. This is the reason why they are not going to employed in this work.

Radiation Hardening by Design

In this work, Hardening by Design techniques have been extensively used to obtain the required radiation tolerance of the circuit.

First, models that include the TID-induced degradation of the devices have been used to simulate the circuit behavior after irradiation. This has allowed to devise the proper strategies to overcome TID-induced issues.

In addition, the significant increase of the leakage current due to TID has been addressed by means of a layout technique: an Enclosed Layout (see Fig. 1.3) has been used for all NMOS devices. In an Enclosed Layout Transistor (ELT), the STI is not in contact with the channel, and the TID-induced

leakage is therefore suppressed. Using ELTs has nevertheless several downsides, such as increased capacitance, increased area, lack of symmetry and strong limitations in the choice of the W/L ratio.

Concerning SEE, charge injections corresponding to the Single Events have been simulated to check for dangerous Single Event Transients and to consequently find solutions to minimize them.

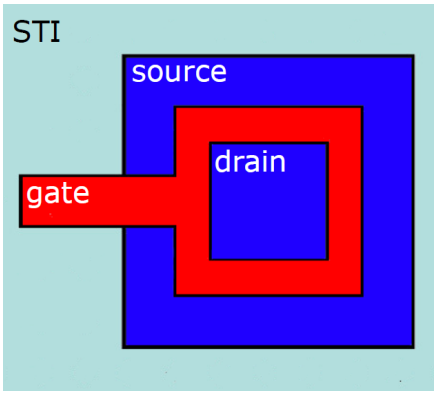

FIGURE 1.3: Representation of an Enclosed Layout Transistor.

Chapter 2

Converters and GaN devices

2.1 Converters

2.1.1 Buck

DC-DC converters are switching converters, in which switching devices (usually MOSFETs) are employed to deliver an output voltage smaller or larger than the input voltage with a low level of power losses (zero in the case of ideal components). The buck converter is one of the most common topologies for step-down DC DC converters due to its low complexity and high efficiency. The architecture of a typical Buck converter is presented in Figure 2.1.

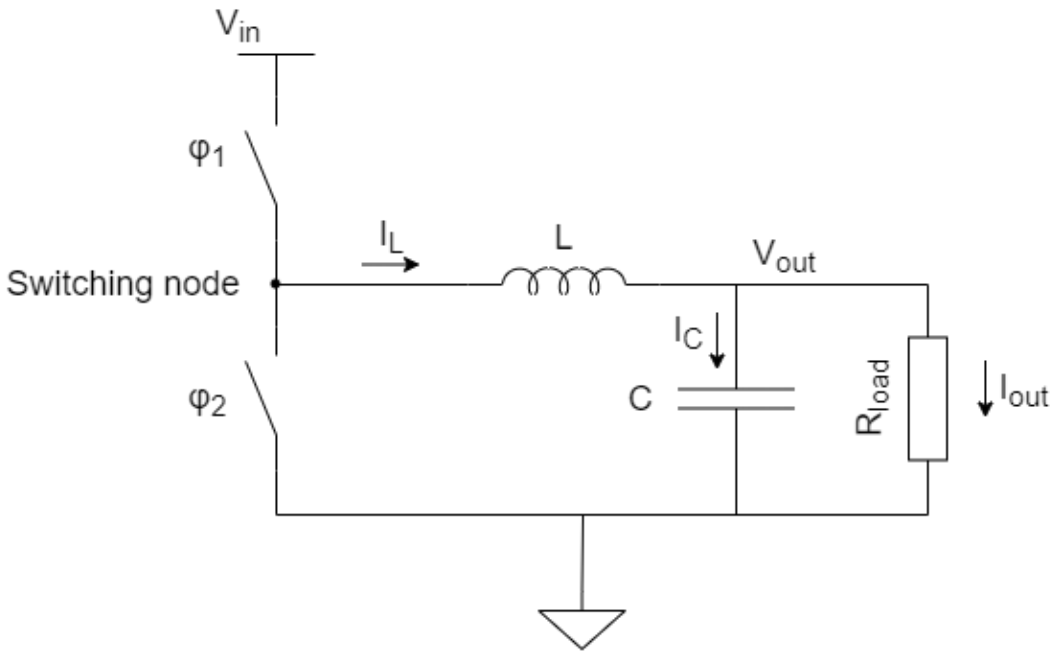

FIGURE 2.1: Architecture of a Buck converter.

There are two switches that act in an opposite way, i.e. when one is open the other one is closed and vice versa: when φ_1 is closed and φ_2 is open, the switched node SW is equal to the input voltage; when instead φ_1 is open and φ_2 is closed SW is connected to ground. Thanks to the action of the LC filter, the output voltage Vout is approximately DC (if the switching frequency is significantly larger than the cut-off frequency of the filter). Changing the relative time between the open and closed phase of each switch, the output voltage Vout can be tuned. In this case, given that we are talking about square waveforms, Vout can be expressed like this:

$$V_{out} = \frac{1}{T}\int_0^T SW\,dt = DV_{in} \tag{2.1}$$

where D is the duty cycle of the converter, i.e. the fraction of the switching period T where the switch φ_1 remains closed [5]. D corresponds therefore to Vout/Vin, i.e. to the conversation ratio of the buck converter. An example of a typical switching cycle is shown in Figure 2.2 (where D'=1-D).

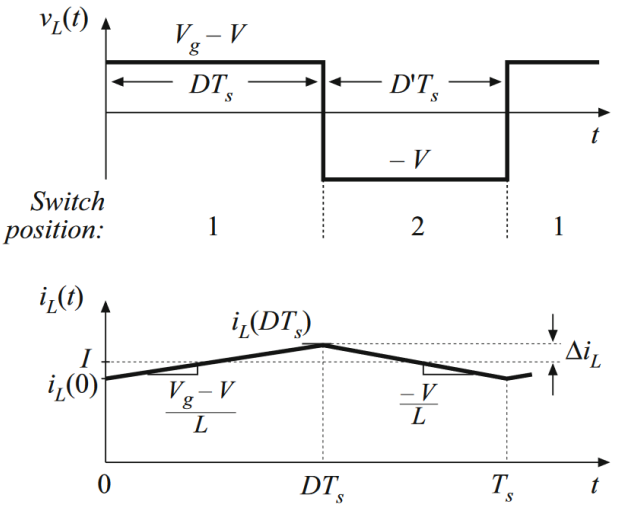

FIGURE 2.2: Voltage and current waveform of the inductor in a Buck converter.

Considering the *small ripple* approximation of the output voltage, i.e. the change in its value is so small that in can be neglected in calculations, during phase 1 of the switching cycle φ_1 is closed and φ_2 is open, thus the voltage across the inductor is approximately equal to:

$$V_L = V_{in} - V_{out} \tag{2.2}$$

the slope of the inductor current waveform during phase 1 is therefore:

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{V_{in} - V_{out}}{L} \tag{2.3}$$

, while during phase 2 of the switching cycle φ_1 is open and φ_2 is closed, therefore the voltage across the inductor becomes:

$$V_L = -V_{out} \tag{2.4}$$

the slope of the inductor current waveform during phase 2 is therefore:

$$\frac{di_L}{dt} = \frac{V_L}{L} = -\frac{V_{out}}{L} \tag{2.5}$$

During phase 1 the change in inductor current is:

$$\Delta I_{L,1} = \frac{V_L}{L} = \frac{V_{in} - V_{out}}{L} \cdot DT \tag{2.6}$$

During phase 2 the change in inductor current is:

$$\Delta I_{L,2} = \frac{V_L}{L} = \frac{-V_{out}}{L} \cdot (1 - D)T \tag{2.7}$$

In stationary conditions, $\Delta I_{L,1} = -\Delta I_{L,2}$. Using 2.1, the inductor current ripple can be expressed as:

$$\Delta I_L = Vin\frac{D(1 - D)T}{L} \tag{2.8}$$

In order to reduce ΔI_L, thus reducing the circulating RMS current and the conduction losses in the switches and in the inductor, either the inductance value L or the frequency $f = \frac{1}{T}$ should increase. In the former case, given that inductors are one of the most difficult circuit components to integrate, there will be a large increase in the converter volume and density; in the latter case, in real applications, such as employing Silicon MOSFETs as switches, an increase in frequency means an increase in switching and/or driving losses, negatively affecting the efficiency of the system. A trade-off between inductance and frequency means a trade-off between volume and efficiency.

GaN HEMTs (or GaN FETs) during recent years have shown their capability to outperform Power Silcion MOSFETs in switching converters due to their improved switching capabilities and lower losses at larger frequncies, leading to an increase in efficiency using the same inductance values.

2.2 GaN HEMT devices

GaN devices are a particular type of heterostructure based devices, more specifically they are HEMTs, i.e. High Electron Mobility Transistors [4]. Many different materials could be employed to make HEMTs (e.g. GaAs), among which GaN (and AlGaN) is certainly the most widespread and used thanks to its superior performance for high frequency and high power applications compared to typical Silicon MOSFETs. GaN is used in the production of power semiconductor devices, as well as RF components and light-emitting diodes (LEDs). GaN has demonstrated the ability to be the displacement technology for silicon semiconductors in power conversion, RF, and analog applications. In fact, Gallium Nitride is a III-V semiconductor with a direct wide bandgap of 3.4 eV, which it is one of its most significant advantages over its silicon (1.12 eV bandgap) counterparts. Having a bandgap almost three times that of silicon means that it requires much more energy to excite a valence electron in the conduction band of the semiconductor. This allows GaN to have larger breakdown voltages and greater thermal stability at higher temperatures. This characteristic, coupled with other critical advantages that are going to be presented in next sections (such as capacitance and on resistance of GaN HEMTs) make these devices the main candidate for a revolution in power electronics devices and performances that is already happening. The high resilience of the GaN devices in withstanding harsh environments i.e. ones with extreme levels of radiation represent a further advantage, making them one of the fittest options for spacecraft, particle accelerators / nuclear detectors applications.

2.2.1 HEMT Theory

GaN transistors are a specific type of HEMTs, High Electron Mobility Transistors, sometimes also called MODFET (Modulation Doped Field Effect Transistor). HEMTs typically have a structure like the one presented in Figure 2.3, where the junction materials can be either GaAs and AlGaAs or GaN and AlGaN.

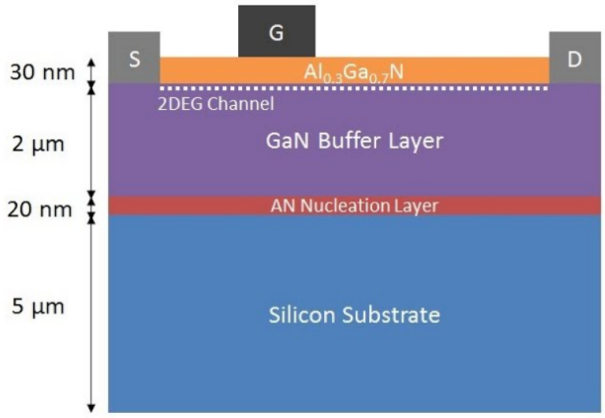

FIGURE 2.3: GaN HEMT structure.

It is made of a thick silicon substrate, an AlN buffer layer,the AlGaN/GaN heterostructure that represents the heart of the device, a Schottky metal/semiconductor junction for the gate contact and two additional electrodes for Source and Drain that pierce through AlGaN to form ohmic contacts with the electron channel. Their working principle is based on the particular way band diagrams of semiconductor heterostructures behave. Let us consider a vertical section of the junction: it can be divided in two parts, SCI i.e. an intrinsic semiconductor and SCII, a highly n-doped semiconductor with different electron affinity to the one of SCI. When the two parts are separated, each one has its own conduction and valence band level. When the two semiconductors are connected to form a junction, their Fermi Levels get aligned, the electrons that come mainly from donor impurities in SCII start moving to the conduction band in SCI until the charge difference between the two regions creates an electric field strong enough to stop the flow of electrons; a state of equilibrium is reached. In this case, the final band diagram, shown in Figure 2.4 is similar to the diagram of a pn junction in equilibrium (with the bands bending related to the local charge) but with an important difference that is crucial for the functioning of this new type of device. Given that the junction is made of two different semiconductors, a discontinuity in the band diagram is formed at the interface between the two materials, effectively trapping the electrons inside a triangular potential well. The electrons trapped inside are confined in a very thin layer close to the interface forming a 2-DEG electron gas, i.e. a "gas" of electrons with two degrees of freedom in the x and y direction but confined in the z direction. The separation of these electrons from the doping atoms lowers their scattering with the dopant sites that is

one of the one of the main reasons for the reduction of mobility in highly doped devices. This characteristic is what gives these devices their name. A passivation layer is typically employed on top of the AlGaN layer in order to prevent the formation of surface states or traps that could trap electrons and disrupt the device. Similarly, sometimes a refinement to the junction is added, inserting an undoped AlGaN layer in the junction between n+ AlGaN and GaN in order to separate even more the electrons from the donor sites and the scattering, at the cost of a lower electron density in the 2DEG gas channel.

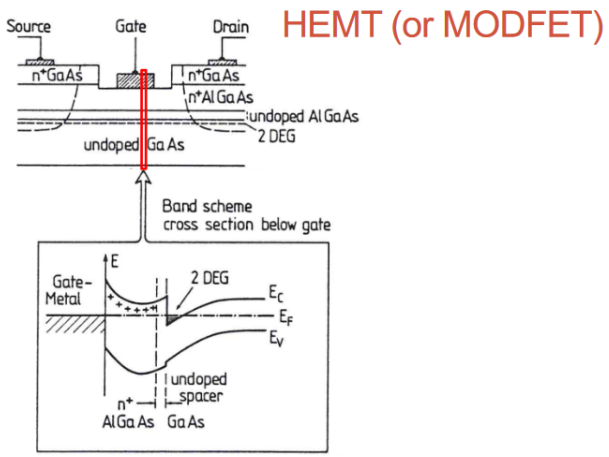

FIGURE 2.4: Example of band diagram of a HEMT [4].

The intensity of the voltage applied on the gate contact of the device modulates the conducting channel of the device, increasing the number of electrons in the 2DEG gas and therefore the current flowing.

This type of transistor is also called d-mode (depletion mode) transistor and is a type of "normally on" device. This means that without applying any voltage bias to the gate, there is already an electron 2DEG channel that can conduct electricity [1]. In power conversion, d-mode devices are problematic because during the startup they would require a negative voltage base on their gate in order to keep them off and prevent any possibility of short circuits. The solution is to build e-mode (enhancement mode) devices, i.e. "typically off" devices that at zero voltage bias do not conduct and only when a positive voltage bias is applied the 2DEG channel is formed. They are much more suitable for power conversion applications because in this way they work just like typical n-channel Silicon POWER MOSFETs.

2.2.2 Advantages compared to Power Silicon MOSFETs

Apart from the aforementioned wide bandgap, that allows GaN devices to sustain larger temperatures than GaAs or Silicon devices (400-300 °C compared to 150 °C) because it lessens the effects of thermal generation of charge carriers that are inherent to any semiconductor, they are many more advantages that granted them an ever-increasing interest regarding high power fast switching applications:

- Higher mobility thanks to the separation of the carriers from the scattering sites (donor sites). This confinement increases the electron mobility from about 1000 cm2/V-s in unfiltered GaN to between 1500 and 2000 cm2/V-s in the 2DEG region [8].
- Due to having a superior relationship between on-resistance and breakdown voltage, they are both smaller and with lower on-resistance for a specific breakdown voltage requirement, or have a much larger breakdown voltage for the same on-resistance[1].
- Faster switching times.
- GaN FET have very low capacitance C_{gs}, C_{gd} and C_{gs} due to the lower capacitance of the Schottky gate junction, to the device's lateral structure and to the reduced electron permittivity of GaN compared to Silicon [1, 14].
- Larger saturation velocity of $3.4 \cdot 10^7 \frac{cm}{s}$ vs $1 \cdot 10^7 \frac{cm}{s}$ in Silicon [18, 20].
- Gan FET have the ability to conduct in reverse direction but their working principle is fundamentally different from Silicon MOSFETS. In Silicon MOSFETs, reverse conduction is typically achieved through conduction across a pn-junction that effectively behaves as a Silicon diode with a typical voltage drop of 0.7 V. Gan FETs instead conduct through the very same channel of electrons during reverse conduction and do not have a diode in their structure, therefore their forward conduction voltage is larger, 2 to 2.5 V, that gets larger as the temperature increases (resistance increases). It is though still easy to manage and GaN FET have a great advantage thanks to it, i.e. they have no reverse recovery. In switching converters, reverse conduction occurs during the dead times (i.e. when both complementary power switches are off). After the end of a dead time (and in particular when turning on the complementary switch of the one where the reverse conduction occurs), in

silicon MOSFETs there is a charge recovery due to the fact that minority charges in the pn junction have to be reabsorbed. This causes increased switching losses and, in case there is a significant parasitic inductance in series with the diode, large voltage overshoots that can damage the devices. GaN FETs do not have such issues, since they do not have any bulk diode and do not have any reverse recovery because they work with majority carriers.

- Extreme resistance to long term exposition to heavy ion bombardment and gamma irradiation [15].

The main downside of GaN compared to Silicon MOSFETs is its thermal conductivity that is lower than silicon. Gallium Nitride has a thermal conductivity of 1.3 $\frac{W}{cmK}$, while silicon has a thermal conductivity of only 1.5 $\frac{W}{cmK}$ [14]. This should mean that in equal conditions heat accumulates more in GaN devices than Silicon devices, causing increases in temperature and power dissipation. This situation though does not happen in real applications, where GaN devices achieve almost always better power performances than Silicon ones. This happens because GaN devices' advantages overcompensate its downside, allowing them to achieve the same or even better performances than Silicon consuming significantly less power. Their efficiency at similar voltages reduce the thermal load of the circuit allowing them to stay at lower temperatures than silicon devices.

Another potential problem of Gallium Nitride is its manufacturing process compared to the state of the art of Silicon manufacturing process [13]. With Silicon the crystalline quality is extremely high with few hundreds defects per square centimeter of material, whereas Gallium Nitride currently has at least six more orders of magnitude defects (billions of defects per squared centimeters).

Obviously, this large amount of defects/area is inefficient given most of the design requirements of semiconductor manufacturing. Defects have also limited GaN semiconductor substrates by their physical size alone. While new manufacturing techniques have lowered the number of defects to more efficient numbers, the cost to produce the same amount of GaN wafers is still not comparable to silicon.

2.2.3 Bootstrap

A buck regulator can either employ two n-channel or one p-channel and one n-channel MOSFETs. The former case is usually preferred due to the low on resistance of NMOS compared to PMOS; the problem in this case is that it is harder to drive this type of regulator due to the differences among the High Side and Low Side MOSFETs. In Figure 2.5 a typical switching configuration with two NMOS transistors can be observed, each device having its own driver for switching. The lower transistor is referenced to as LS (Low Side) and the upper one is called HS (High Side). Low Side driving is straightforward, because the source of the LS transistor is connected to ground, therefore every voltage used for driving is referenced to ground. High Side driving is instead more complex because in this case the source of the HS transistor is not connected to ground but to the switching node; in order to make everything work, a way to refer the driver to that node must be found.

The technique employed to solve this problem is called bootstrapping [3]. A bootstrap circuit is a step up charge pump made of a switch, one diode and one capacitor called respectively bootstrap diode and bootstrap capacitor. Schottky diodes are preferred due to their low value forward voltage and their larger switching speed (compared to typical pn diodes). Since they are uniplanar devices made with a metal-semiconductor junction, they work with majority carriers (compared to minority carriers in pn-junction diodes); this means that they are only affected by junction capacitance and not diffusion capacitance (caused by the random recombination of carriers), allowing them to have a lower value of both capacitance and reverse recovery time.

2.2.4 Dead times

A dead time is defined as the time duration between the turning off of one transistor and the turning on of the other. Dead times have to be introduced to prevent the turning on of both transistors at the same, because that would provide a direct path from Vin to Ground with low resistance (short circuit path) that would drain a large amount of current, negatively affecting the power consumption of the converter and potentially damaging the devices. Dead times play a major role in converters switching losses. During the dead times, the inductor current I_L is typically not zero and tries to find a path to flow and discharge the energy accumulated in it. With silicon MOSFETs, the

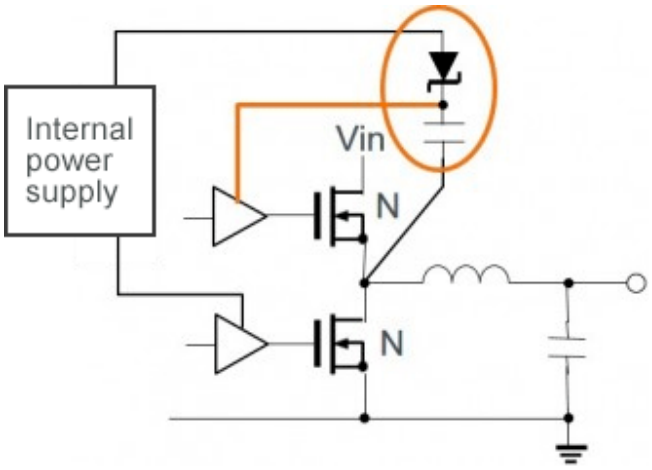

FIGURE 2.5: Example of bootstrap technique applied to a circuit [12]

intrinsic body diode present in their structure provides a path for the inductor current; the voltage of the switching node changes until the voltage drop across the diode reaches its forward voltage V_f (0.6-0.7 V): the bulk diode starts to conduct because it is forward biased and a large current can flow, dissipating a power equal to $P = I_L V_f$. The longer the dead time, the larger the energy dissipated, until after a certain point where the energy in the inductor and the capacitor are completely discharged and the current stops. As can be imagined, the main objective is to reduce the dead time value up to a minimal amount where it still work as intended, i.e. both transistors are never on at the same time.

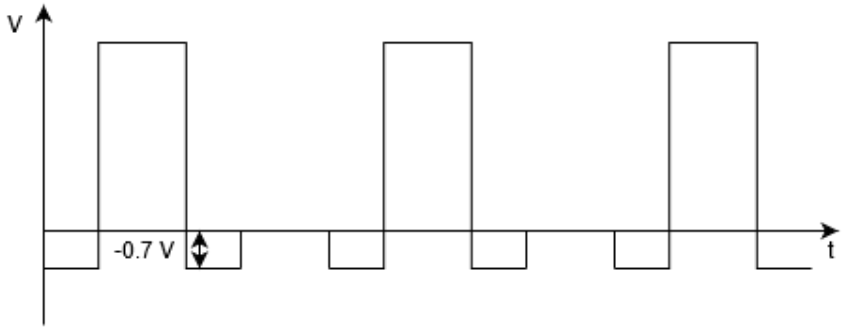

FIGURE 2.6: Voltage waveform of the switching node in a Buck converter that employs Silicon Mosfets as switches.

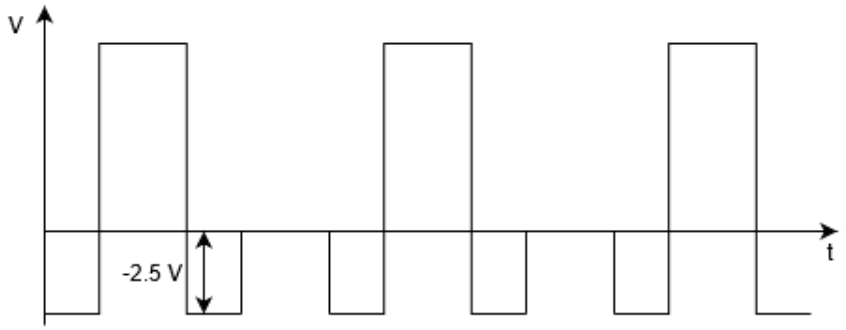

FIGURE 2.7: Voltage waveform of the switching node in a Buck converter that employs GaN FETs as switches.

2.3 Necessity of a linear regulator for GaN drivers

GaN FETs do not have a built in body diode and their reverse conduction profile is the same as their direct conduction (they are majority carriers devices), therefore they do not have any minority carrier to reabsorb and they do not experience the losses due to the reverse recovery charge. On the other hand, the reverse voltage during the dead times is larger than in Silicon MOSFETs, and managing it is a challenge itself. In particular, the reverse conduction of a GaN device occurs for a V_{ds} around -2.0/2.5 V (with $V_{gs} = 0V$, V_{ds} must be $< -V_{th}$ to turn on the device). It is thus very important to minimize the duration of the dead times to avoid significant losses ($P = I_L|V_{ds}|$). In addition, due to this large negative V_{ds} a conventional bootstrapping technique like the one depicted in 2.5 can be potentially dangerous for the reliability of the GaN devices: naming V_{dd} the internal power supply voltage, the voltage across the bootstrap capacitor can increase to $V_{dd} + 2.5V$ due to the reverse conduction (since the switched node can decrease to $-2.5V$). This results in turn to a large power supply voltage for the HS driver, which can possibly set the V_{gs} of the GaN FET to a value above its safe operating area. Finding a solution to this problem means finding a way to make the power supply voltage of the HS driver insensitive to the large negative values that the switched node can have during the dead times.

In this context, a linear regulator becomes certainly a viable solution. In order to protect the drivers from the voltage spike, two identical linear regulators are introduced in the design, one for the LS part and one for the HS part. They step down the voltage from 12V to 3.3V, which is a viable value to drive the GaN devices.

In the LS regulator, its Vdd, Vss and output terminal are connected respectively to a 12 V, to Ground and to the Vdd input of the driver of LS. In the HS regulator, its Vdd, Vss and output terminals are connected respectively to the Vboot node (12V + SW - Vdiode), to the switching node SW and to the Vdd input of the driver of HS. During the dead times, the increase in Vdd - Vss of the regulator does not affect its output that maintains a steady 3.3 V across the GaN driver. The final configuration of the circuit is shown in Figure 2.8.

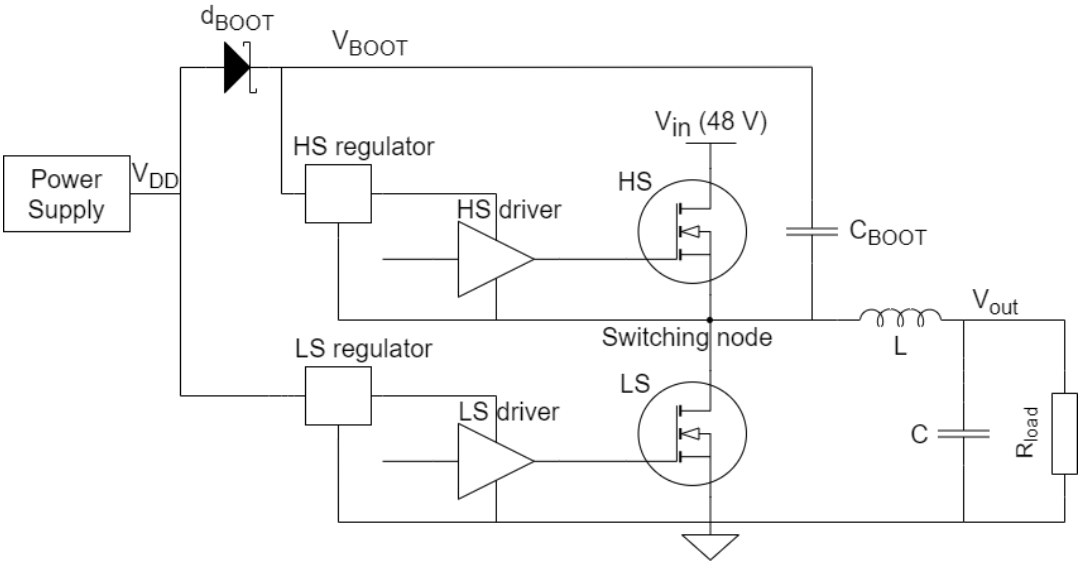

FIGURE 2.8: Schematic of the circuit with the implemented regulators.

Chapter 3

Linear Regulator

Considering the superior performance of GaN devices over Silicon devices and their tolerance to radiation, a new generation of 48 V-input radiation-hard converters based on commercial GaN FETs is in development at CERN. Such converters would allow a further decrease in the power dissipation in the cables, allowing the power to be distributed to the detectors at a higher voltage compared to the existing solutions. Developing such converters requires the design of radiation-hard Silicon gate drivers for the GaN devices, which must be powered by a dedicated linear regulator (as presented in Chapter 2). In this work, such linear regulator has been designed using a commercial 0.35 μm HV-CMOS technology, whose radiation response had been previously qualified.

3.1 Purpose and requirements of the circuit

A linear regulator is a step-down voltage regulation circuit whose objective is to provide a regulated fixed output voltage, regardless of variations in its input voltage and load. In this case, the circuit nominal working conditions are

- Input Voltage of 12 V
- Temperature of 27 °C
- Current load of approximately 7-10 mA (this is the average current drained by the load, while the real load will require large current spikes to drive the GaN FET)

The circuit however must effectively deliver an output voltage of 3.3 V in all possible conditions in terms of input voltage, load, temperature, process

Temperature	Load	Vin	TID
-30 °C to 120 °C	0 to 30 mA	5 – 15 V	0 to 100 MRad

TABLE 3.1: All possible conditions/specifications of the circuit.

variations and radiation. All the possible combinations of operation are described in Table 3.1.

Moreover, the circuit must be tolerant to Single Event Effects up to a Linear Energy Transfer of 40 $\frac{MeV \cdot cm^2}{mg}$. The core MOSFETs of the selected CMOS technology are rated 3.3 V, while it is also possible to use high-voltage DMOS devices (which can sustain a larger V_{ds} thanks to a low-doped drift region introduced at the drain side) whose V_{ds} is rated up to $25V$. Since the core devices exhibit a significantly better radiation tolerance compared to DMOS devices, the proposed design uses mostly 3.3 V-rated FETs. Given that the input voltage can reach values up until 15 V, it is nevertheless necessary to use also a limited number of DMOS transistors.

3.2 Analysis and Design

Figure 3.1 presents the schematic of a linear regulator. Compared to switching topologies, it is characterised by lower efficiency, but in this case the power consumption is not an important issue due to the fact that is going to be only a fraction of the power delivered by the entire converter; apart from that, it benefits from a simpler design, lower noise and continuous operation [16].

It is characterised by an error amplifier, a pass transistor that acts as variable resistor, two resistors for the feedback loop, a bandgap voltage reference, the output capacitance and the load. The bandgap voltage reference in this work is equal to 619.5 mV in nominal conditions: the values of the feedback resistors are chosen in order to feed back a fraction of the output voltage approximately equal to the voltage reference to the loop inverting input of the Amplifier. If the pass transistor is an inverting stage it will be fed to the non-inverting input of the amplifier (in order to maintain the inverting characteristic of the feedback loop), otherwise if the pass transistor was non inverting it would be fed to the inverting input of the Error Amplifier. As will

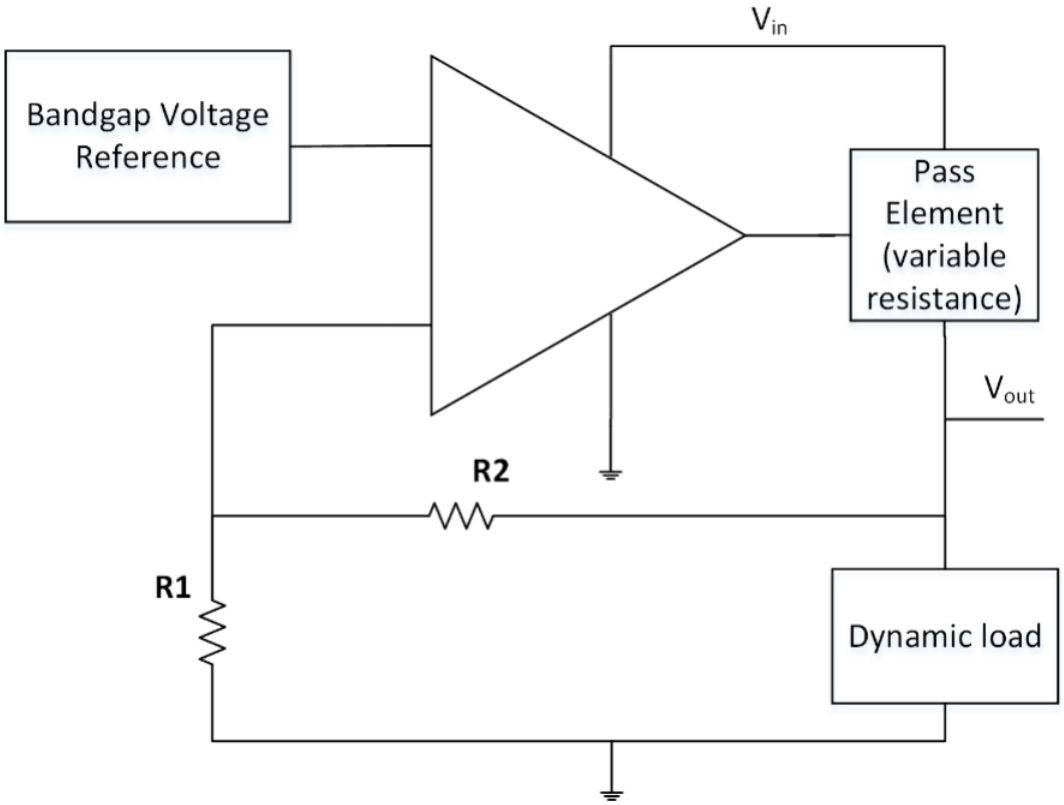

FIGURE 3.1: Schematic of a series linear regulator [17].

be seen, the former case will be the one happening in this work. Considering the Error Amplifier and the Pass transistor as a single amplifier, the circuit can be described in the following way:

$$V_{out} = A_0(V_{bandgap} - \beta V_{out}) \tag{3.1}$$

$$\frac{V_{out}}{V_{bandgap}} = \frac{A_0}{1 + \beta A_0} \tag{3.2}$$

$$\text{if } A_0 \to +\infty, V_{out} = \frac{1}{\beta} V_{bandgap} \tag{3.3}$$

where $\beta = \frac{R_1}{R_1+R_2}$, R_1 and R_2 are the feedback resistors, A_0 is the open-loop gain of the amplifier. The design choices have been the following:

- As Pass transistor, both NMOS and PMOS could be used; In this case, a PMOS device has been chosen due to its better PSRR and better performance with low dropout values (Vin-Vout): indeed, NMOS Vg - Vs can go only up to Vin-Vout (Vs=Vout and Vg obviously cannot go higher than Vin), meanwhile PMOS do not have this problem and their Vgs

can extend from 0 to Vin [19].

- The topology of the amplifier is chosen to be a two stage amplifier, cascading a source follower stage to a folded cascode topology. The folded cascode is chosen for its high output swing, large output resistance and high PSRR, meanwhile the p-type source follower stage is added to reduce the voltage value at the output of the folded cascode. In this way, there is a larger voltage drop across the cascode transistors to maintain them more easily in saturation in all working conditions; even if the pass transistor was off they could still have some headroom. Without the source follower sometimes the cascode transitors could enter triode region in some corners decreasing the gain of the amplifier.
- The output capacitance is a fixed external commercial capacitance equal to 2 uF.
- Bandgap voltage reference circuit employs an already exisiting circuit with a voltage value of 619.5 mV at nominal conditions (T=27 °C, Vin = 12 V).

3.2.1 Schematics

The schematic drawing of the circuit is presented in Figure 3.2.

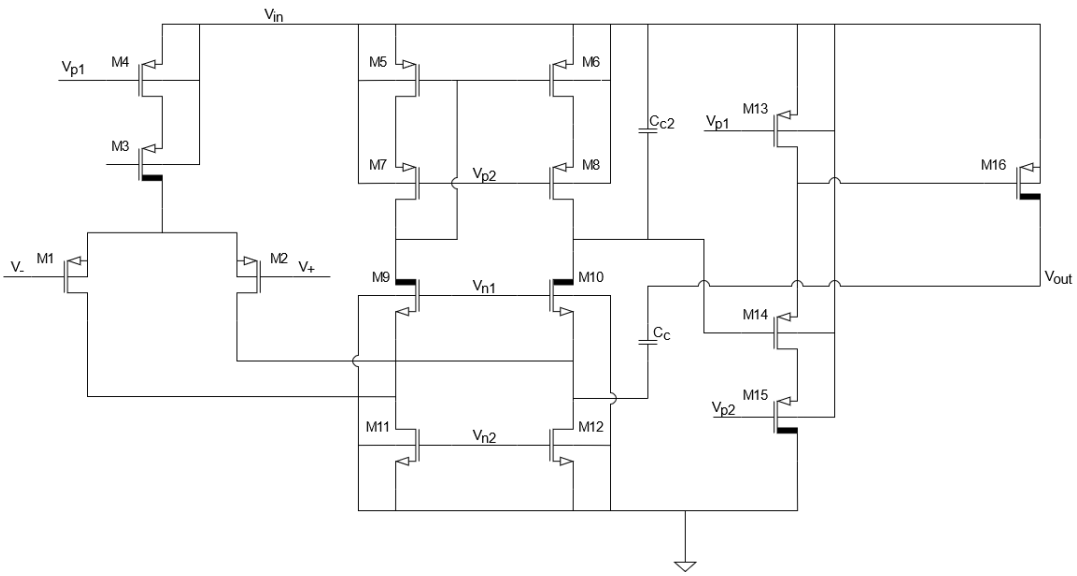

FIGURE 3.2: Amplifier drawing.

Regarding the folded cascode topology:

- M1 and M2 represent the differential pair.
- M5 M6 M7 and M8 represent the cascode current mirror.
- M9 and M10 are DMOS High Voltage transistors (to sustain the high input voltages) that act also as an additional cascode gain stage (common gate).
- M11 and M12 are the active load.
- M4 is the transistor that biases the differential pair.
- M3 is a High voltage Dmos to sustain the voltage.

Regarding the source follower stage:

- M13 represents the bias source.
- M14 is the source follower transistor stage itself.
- M15 is a DMOS to sustain the high input voltage and limit the V_{ds} of M14.

Finally, M16 is the last gain stage, the pass transistor that corresponds to a DMOS transistor, necessary due to the large voltage difference between its drain and source (12-3.3 V), in common source configuration.

There are two additional capacitors:

- Cc is employed as a compensation capacitance through the indirect feedback technique. It must be connected to a high PSRR node in order not to worsen the PSRR at the output.
- Cc2 is to convert the gate of M14 from a high PSRR node to a low PSRR node; in this way, its node and the gate of M16 follow more closely the behaviour/ripple of V_{in} and if V_g and V_s of M16 change in a similar way, V_{out} remains almost unaffected by it, improving the PSRR of the circuit.

The indirect feedback technique is similar to the Miller compensation but improves its flaws.

With the Miller capacitance compensation, a capacitor is introduced in the circuit. One of its ends is typically connected to the input node and the other end to the output node of one (or more) cascaded stage. It allows to both lower the frequency of the dominant pole ω_1 and increase the frequency of

the non-dominant pole ω_2; its size can also be quite low due to the Miller effect that boosts its capacitance value by the gain of the encompassed stages. Its major flow is that it introduces an additional positive zero to the transfer function that actually decreases the phase by 90 degrees and negatively affects the phase margin and stability of the circuit. A diagram example of Miller compensation is shown in Figure 3.3.

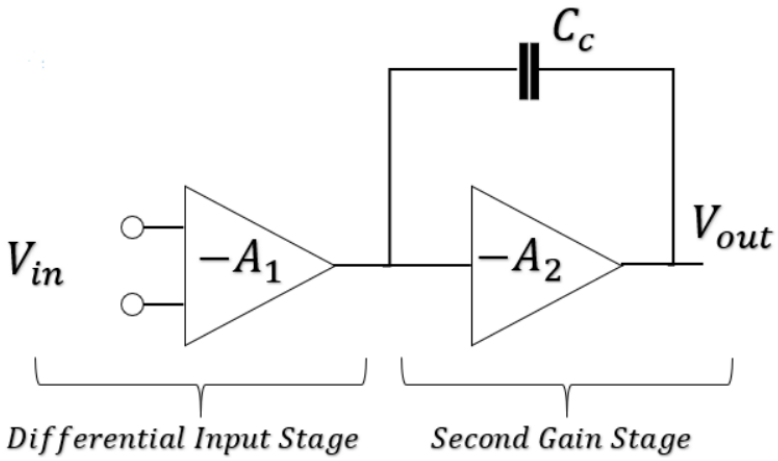

FIGURE 3.3: Diagram that shows an example of Miller compensation [6].

In order to solve this issue, keeping at the same time the positive sides of the Miller compensation, the so-called Indirect Feedback compensation is introduced. Simple but effective, its main difference is that instead of connecting one end of the capacitor to the input node of one (or more) cascaded stage (and therefore to the output node of the previous stage), it is connected to an internal Low Impedance node of the previous stage. The main reason Miller compensation caused problems was that it allows for both feecback (Miller effect) and feedforward (positive zero) greatly affecting its stability. With the Indirect Feedback technique, the compensation is now asymmetrical and one direction (the feedback) is favored compared to the other (the feedforward). Calling A the first end of the capacitor (the internal low-Z node i.e. a source) and B its second end (the high-Z output node of the encompassed stage, i.e. a drain), feedback corresponds to direction from B to A and feedforward to direction from A to B; feedback sees a low-Z, therefore a large current and signal can pass through without any problem; feedforward sees a high-Z, therefore only a small current passes through and the signal is effectively blocked. A diagram example of Indirect Feedback compensation is shown in Figure 3.4.

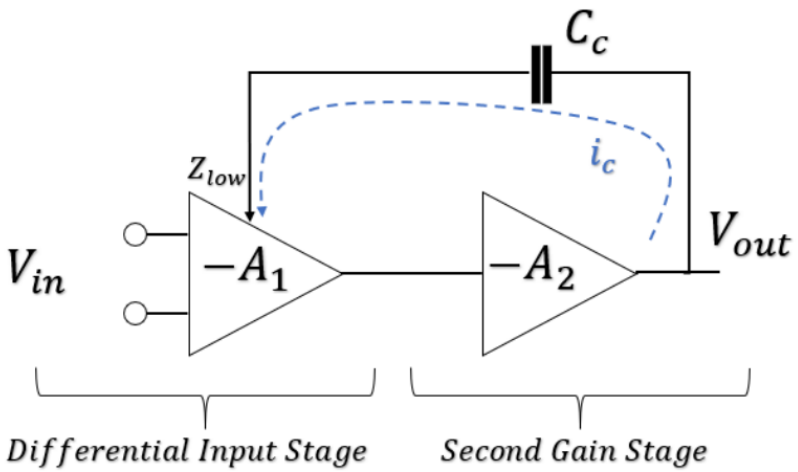

FIGURE 3.4: Diagram that shows an example of Indirect Feedback compensation [6].

The transistor sizing is shown in Figure 3.5.

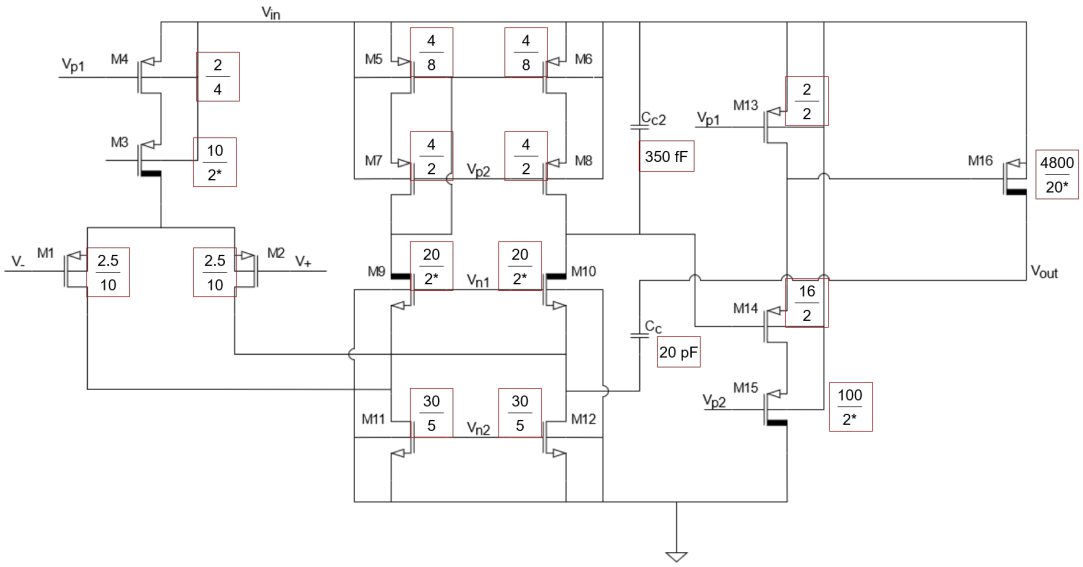

FIGURE 3.5: Transistor sizing of the linear regulator.

For each fraction, the numerator and denominator represent respectively the width and the length of each transistor expressed in μm. The only exception are the DMOS transistors because they have a fixed channel length; in this case, the denominator, written followed by an asterisk, stands for the number of channels of the transistor. Sizing the pass transistor means finding the best tradeoff among different parameters. Employing a pass transistor with a larger $\frac{W}{L}$ ratio means increasing the current it can conduct given a certain

V_{gs}; at the same time, the parasitic capacitance of the device increases, affecting negatively both the PSRR and the stability of the circuit (phase margin reduced). The chosen size correspond to a width a equalt to 4800 μm an a number of channels equal to 20. This size represents the best compromise that was found, employing the minimum size at which the transistor conducts and remains in saturation in every condition.

Final image of the Cadence schematic is presented in Figure 3.6.

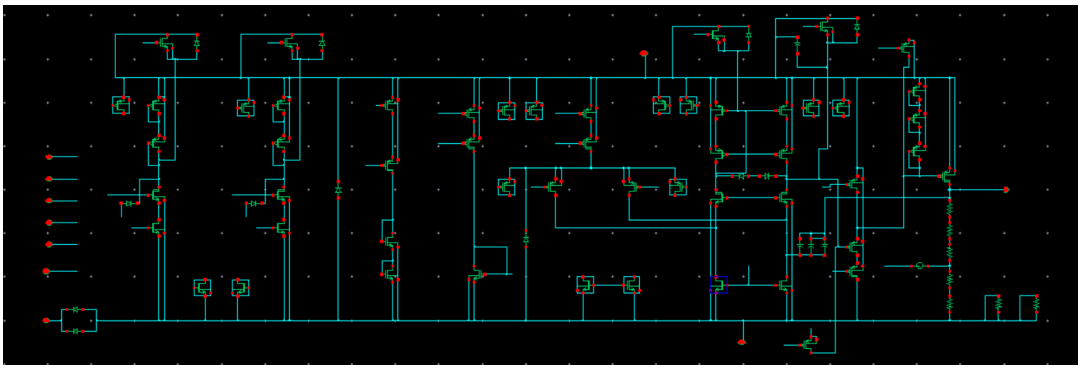

FIGURE 3.6: Final Cadence schematic.

3.2.2 Small signal analysis

The small signal equivalent circuit is shown in Figure 3.7.

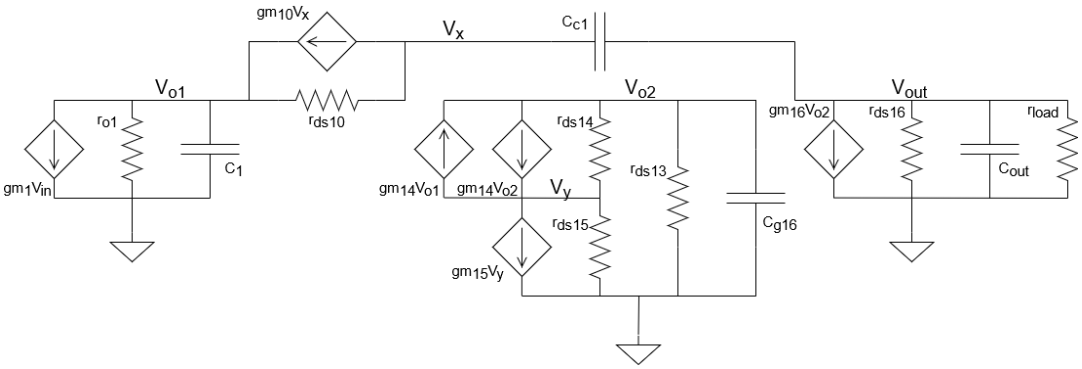

FIGURE 3.7: Small signal representation of the indirect feedback compensated circuit (implemented topology).

Where C_1 already includes the C_{c2} capacitor. Its simplified version is shown in Figure 3.8.

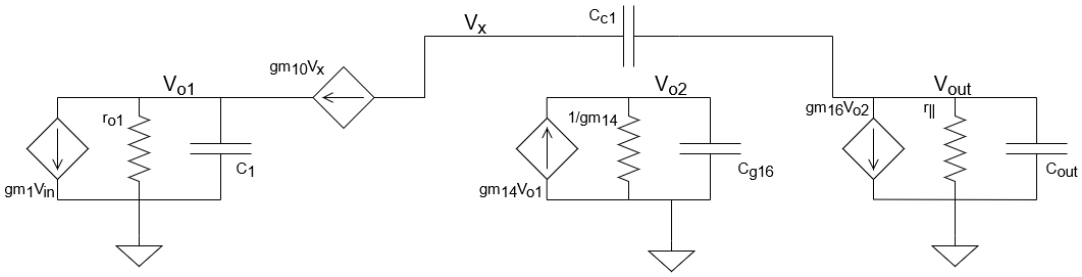

FIGURE 3.8: Small signal simplified representation of the indirect feedback compensated circuit (implemented topology).

The source follower stage was atypical due to the presence of M15, but after calculating its equation it can be approximated with the typical source follower stage small signal equivalent. At the output node there is now only one resistor $r_{||} = \frac{r_{ds16} r_{load}}{r_{ds16} + r_{load}}$. Additionally, r_{ds10} has been neglected while keeping the current source $gm_{10} V_x$. This choice can be justified by showing the complete derivation of the open-loop transfer function, which is beyond the scope of this work, and it allows to simplify the transfer function keeping at the same time the asymmetry between feedback and feedforward paths(the former being greatly favoured compared to the latter).

For the sake of comparison, the hypothetical Miller compensated circuit is shown in Figure 3.9 and its simplified version in Figure 3.10.

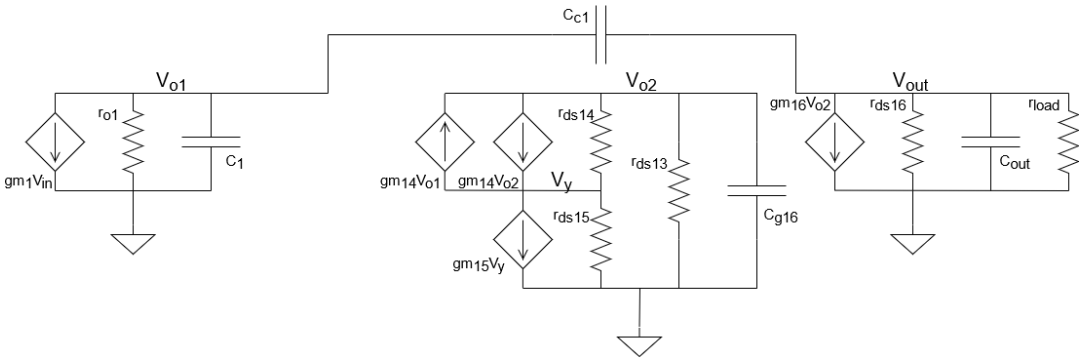

FIGURE 3.9: Small signal representation of the Miller compensated circuit (not implemented).

Both circuits will be analysed to determine their transfer functions and compared to show analytically the difference and the improvement of the Indirect Feedback technique.

The nodal equations of the Miller compensated circuit are:

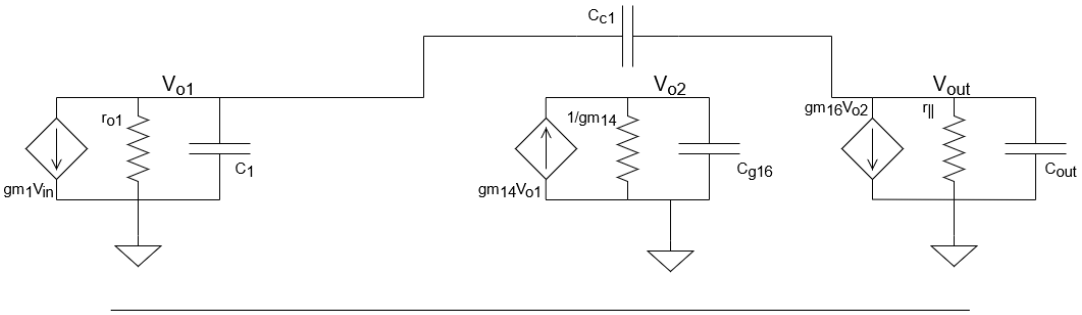

FIGURE 3.10: Small signal simplified representation of the Miller compensated circuit (not implemented).

$$\begin{cases} sC_c(V_{out} - V_{o1}) = g_{m1}V_{in} + \dfrac{V_{o1}}{r_{o1}} + sC1_{V_{o1}} \\ gm_{14}V_{o1} = gm_{14}V_{o2} + sC_{g16}V_{o2} \\ -sC_c(V_{out} - V_{o1}) = g_{m16}V_{o2} + \dfrac{V_{out}}{r_{\|}} + sC_{out}V_{out} \end{cases} \tag{3.4}$$

The transfer function of the Miller compensated circuit is the following:

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= gm_1 gm_{16} r_{o1} r_{\|} \cdot \frac{1 - s\frac{C_c}{gm_{16}} - s^2 \frac{C_c}{gm_{16}} \frac{C_{g16}}{gm_{14}}}{1 + \alpha_1 s + \beta_1 s^2 + \gamma_1 s^3} \\ \alpha_1 &= (C_1 + C_c) r_{o1} + \frac{C_{g16}}{gm_{14}} + \frac{C_c}{gm_{10}} + (C_{out} + C_c) r_{\|} + gm_{16} C_c r_{o1} r_{\|} \\ \beta_1 &= \frac{(C_1 + C_c) C_{g16} r_{o1}}{gm_{14}} + C_{out} r_{\|} + (C_1 C_{out} + C_c C_{out} + C_1 C_c) r_{o1} r_{\|} + \frac{(C_{out} + C_c) C_{g16} r_{\|}}{gm_{14}} \\ \gamma_1 &= (C_1 C_c C_{g16} + C_1 C_{g16} C_{out} + C_c C_{g16} C_{out}) r_{o1} r_{\|} \end{aligned} \tag{3.5}$$

It can be observed the presence of a second degree numerator in the transfer function. Performing algebraic calculations, it is found that the zeros of the transfer function are one positive and one negative, with the former being at a lower frequency than the latter. This can cause problem of stability due to 90 degrees reduction in phase brought by the positive zero.

The nodal equations of the implemented Indirect Feedback compensated circuit are :

$$\begin{cases} g_{m10}V_x = g_{m1}V_{in} + \dfrac{V_{o1}}{r_{o1}} + sC_1V_{o1} \\ gm_{10}V_x = sC_c(V_{out} - V_x) \\ gm_{14}V_{o1} = gm_{14}V_{o2} + sC_{g16}V_{o2} \\ -sC_c(V_{out} - V_x) = g_{m16}V_{o2} + \dfrac{V_{out}}{r_{\|}} + sC_{out}V_{out} \end{cases} \tag{3.6}$$

The transfer function of the implemented Indirect Feedback compensated circuit is:

$$\begin{aligned} \frac{V_{out}}{V_{in}} &= gm_1gm_{16}r_{o1}r_{\|} \cdot \frac{1 + s\frac{C_c}{gm_{10}}}{1 + \alpha_2 s + \beta_2 s^2 + \gamma_2 s^3 + \delta_2 s^4} \\ \alpha_2 &= C_1r_{o1} + \frac{C_{g16}}{gm_{14}} + \frac{C_c}{gm_{10}} + (C_{out} + C_c)r_{\|} + gm_{16}C_cr_{o1}r_{\|} \\ \beta_2 &= \frac{C_1C_cr_{o1}}{gm_{10}} + \frac{C_1C_{g16}r_{o1}}{gm_{14}} + \frac{C_cC_{g16}}{gm_{10}gm_{14}} + C_1(C_{out} + C_c)r_{o1}r_{\|} + \frac{C_cC_{out}r_{\|}}{gm_{10}} + \frac{C_{g16}(C_{out} + C_c)r_{\|}}{gm_{14}} \\ \gamma_2 &= \frac{C_1C_cC_{g16}r_{o1}}{gm_{10}gm_{14}} + \frac{C_1C_cC_{out}r_{o1}r_{\|}}{gm_{10}} + \frac{C_1C_{g16}(C_{out} + C_c)r_{o1}r_{\|}}{gm_{14}} + \frac{C_cC_{g16}C_{out}r_{\|}}{gm_{10}gm_{14}} \\ \delta_2 &= \frac{C_1C_cC_{g16}C_{Cout}r_{o1}r_{\|}}{gm_{10}gm_{14}} \end{aligned} \tag{3.7}$$

There are in this case four negative poles and one negative zero. Unlike the Miller compensation, there are no more positive zeros, therefore there is no more the stability problem caused by it.

The negative zero frequency is equal to:

$$f_{z1} = -\frac{gm_{10}}{2\pi C_c} \tag{3.8}$$

In order to find the poles, the following approximation can be made to simplify it:

$$
\begin{aligned}
&(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})(1+\frac{s}{\omega_{p4}}) = \\
&1+s(\frac{1}{\omega_{p1}}+\frac{1}{\omega_{p2}}+\frac{1}{\omega_{p3}}+\frac{1}{\omega_{p4}}) \\
&+s^2(\frac{1}{\omega_{p1}\omega_{p2}}+\frac{1}{\omega_{p1}\omega_{p3}}+\frac{1}{\omega_{p1}\omega_{p4}}+\frac{1}{\omega_{p2}\omega_{p3}}+\frac{1}{\omega_{p2}\omega_{p4}}+\frac{1}{\omega_{p3}\omega_{p4}}) \\
&+s^3(\frac{1}{\omega_{p1}\omega_{p2}\omega_{p3}}+\frac{1}{\omega_{p1}\omega_{p2}\omega_{p4}}+\frac{1}{\omega_{p1}\omega_{p3}\omega_{p4}}+\frac{1}{\omega_{p2}\omega_{p3}\omega_{p4}}) \\
&+s^4(\frac{1}{\omega_{p1}\omega_{p2}\omega_{p3}\omega_{p4}})
\end{aligned}
\tag{3.9}
$$

Considering that:

$$
\begin{aligned}
\frac{1}{\omega_{p1}} &>> \frac{1}{\omega_{p2}}, \frac{1}{\omega_{p3}} \\
\frac{1}{\omega_{p4}} &<< \frac{1}{\omega_{p2}}, \frac{1}{\omega_{p3}}
\end{aligned}
$$

the equation becomes:

$$
\begin{aligned}
&(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})(1+\frac{s}{\omega_{p3}})(1+\frac{s}{\omega_{p4}}) \approx \\
&1+s(\frac{1}{\omega_{p1}}) \\
&+s^2(\frac{1}{\omega_{p1}\omega_{p2}}+\frac{1}{\omega_{p1}\omega_{p3}}) \\
&+s^3(\frac{1}{\omega_{p1}\omega_{p2}\omega_{p3}}) \\
&+s^4(\frac{1}{\omega_{p1}\omega_{p2}\omega_{p3}\omega_{p4}})
\end{aligned}
\tag{3.10}
$$

The DC loop gain of the transfer function is:

$$A_0 = gm_1 gm_{16} r_{o1} r_{\|} \tag{3.11}$$

The first coefficient of the denominator of the transfer can be approximated as

$$\alpha = gm_{16} C_c r_{o1} r_{\|} \tag{3.12}$$

therefore the frequency of the first dominant pole is

Temperature	Load	Vin
-30 °C, 27 °C, 120 °C	0, 50 uA, 10 mA, 30 mA	5 V, 12 V, 15 V

TABLE 3.2: Specific values used for simulation parametric sweep.

$$f_{p1} = \frac{1}{2\pi g m_{16} C_c r_{o1} r_{\|}} \tag{3.13}$$

The other two dominant poles are close to each other, as will be shown in the simulation section, thus they cannot be found analytically.

The obtain the unity gain frequency GBW (gain bandwidth) one has to set $\frac{V_{out}}{V_{in}}$ and solve to find the corresponding frequency:

$$\frac{V_{out}}{V_{in}} = g m_1 g m_{16} r_{o1} r_{\|} \cdot \frac{1 + s\frac{C_c}{g m_{10}}}{1 + \alpha s + \beta s^2 + \gamma s^3 + \delta s^4} = 1 \tag{3.14}$$

$$g m_1 g m_{16} r_{o1} r_{\|} \approx 1 + \alpha s \approx \frac{s}{\omega_p 1} \tag{3.15}$$

$$f_{GBW} = \frac{A_0 \cdot \omega_{p1}}{2\pi} = \frac{g m_1 g m_{16} r_{o1} r_{\|}}{2\pi g m_{16} C_c r_{o1} r_{\|}} \tag{3.16}$$

$$f_{GBW} = \frac{g m_1}{2\pi C_c} \tag{3.17}$$

The values just found (GBW, $\omega_p 1$ and A_0) are the same as the Miller compensated circuit, meaning that its advantages are kept with this technique.

3.3 Simulation and results

In order to be validated, the circuit had to work effectively for every possible combination of temperature, input voltage, TID and current load as presented in Table 3.1. Employing Cadence Virtuoso, a test-bench circuit has been created. Both stability and DC simulations have been performed to determine phase margin, gain, PSRR and V_{out} of the circuit. The chosen points for the parametric sweep are shown in Table 3.2.

To simulate the load, a DC current source has been employed. In order to take into account the effects of both radiation and possible differences in transistors' technological parameters, 30 corners (including the nominal case) are

also employed to run the simulation, reaching a total of 1080 different simulation points: 30 corners, 3 different temperatures, 3 different input voltages, 4 different loads.

Let us start first with the nominal case, i.e.:

- $V_{in} = 12V$
- $T = 27^oC$
- $I_{LOAD} = 10mA$

In Figure 3.11, 3.12 and 3.12 are respectively shown the Loop gain,the phase and the PSRR plot of the circuit.

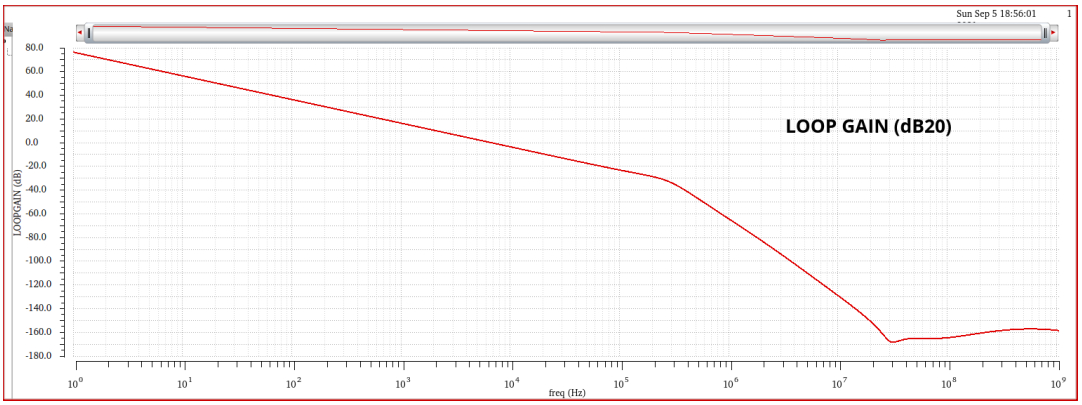

FIGURE 3.11: Loop Gain (dB20) of the circuit with the real bandgap in the nominal case.

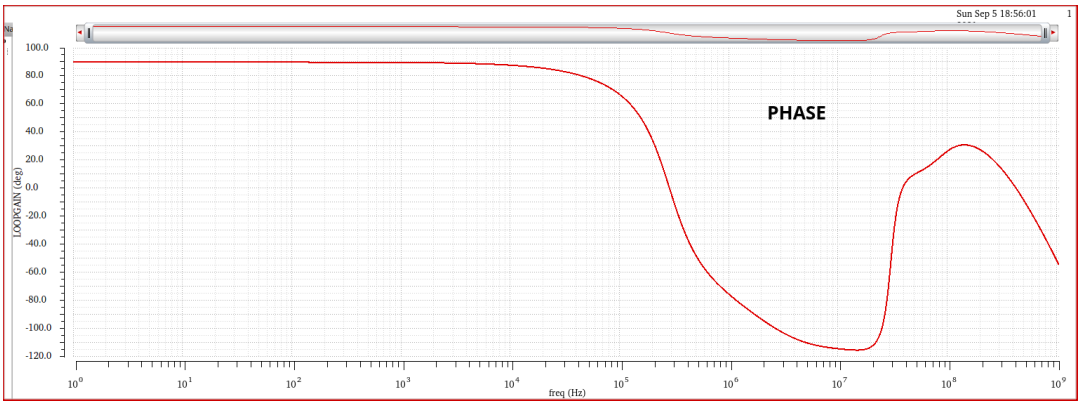

FIGURE 3.12: Phase vs frequency of the circuit with the real bandgap in the nominal case.

From the plots, it can be deduced that the dominant pole (fixed by the compensation) that is at such low frequencies that even at 1 Hz the slope of the

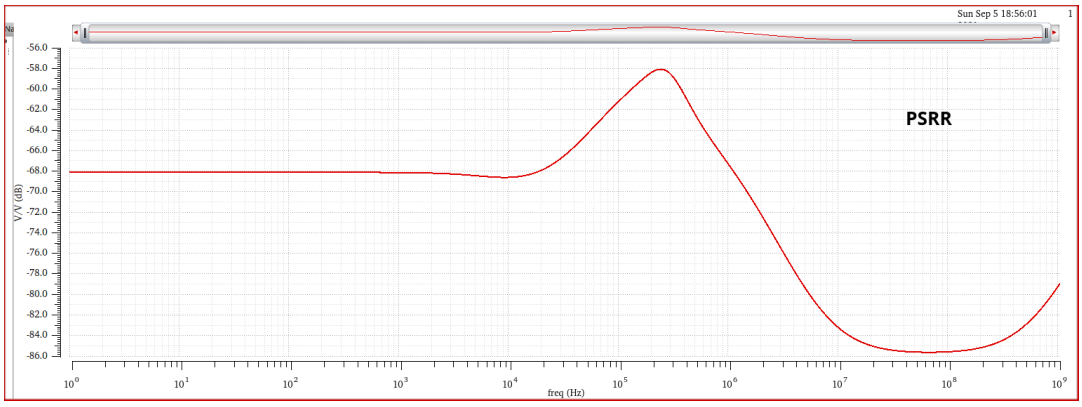

FIGURE 3.13: PSRR vs frequency of the circuit with the real bandgap in the nominal case.

gain is already equal to -20 dB/dec. At this load value, the second and third pole are at similar frequencies, therefore at around 250 kHz the slope changes from -20 dB/dec to -60 dB/dec. Other parameters found are:

- Gain (at 1 Hz) = 76.59 dB
- GBW=6.756 kHz
- Phase margin = 88.52 °
- DC PSRR = 68.1 dB
- Peak PSRR = 58.06 dB (at 240 kHz)

The PSRR value of the frequency of interest for the circuit, i.e. 1 MHz, is equal to 67.46 dB, which meets the design targets.

In order to obtain the distribution of the output voltage with process variations, two different MonteCarlo simulation of the output voltage with 200 points(in nominal condition) have been also performed, one simulating wafer-to-wafer (Process) variations and one for mismatch. The results are shown as Histograms respectively in Figure 3.14 and 3.15.

Process simulation has an average $V_{out} = 3.32V$ with a standard deviation of $\sigma = 37.6mV$. Mismatch simulation has an average $V_{out} = 3.32V$ with a standard deviation of $\sigma = 55.3mV$. As can be expected, the mismatch simulation has a larger impact on the output voltage, since it unbalances the matched pairs, leading to an input offset. Still, even considering a 2σ interval (confidence value of 95%) the resulting change in V_{out} stays within $\pm 3.3\%$.

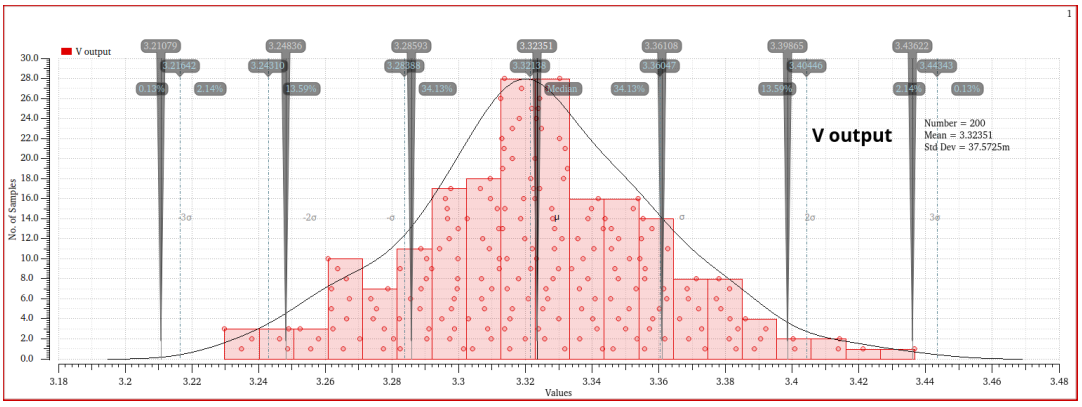

FIGURE 3.14: Histogram of the output voltage following a 200 points MonteCarlo Process simulation.

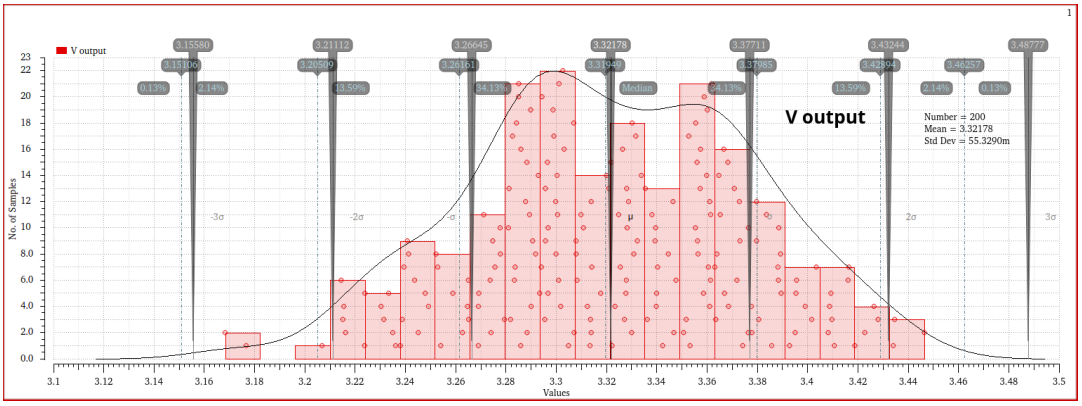

FIGURE 3.15: Histogram of the output voltage following a 200 points MonteCarlo Mismatch simulation.

Let us now proceed with a parametric simulation for all combinations of the sweep points presented in Table 3.2 and the radiation corners. Results are presented in Figure 3.16 (Gain), 3.17 (Phase) and 3.18 (PSRR). Moreover, two Histograms showing the values of the phase margin and the V output across all simulation points are presented in Figure 3.19 and 3.20.

The behaviour of the circuit meets the required targets in every condition, even extreme ones.

In the gain plot it can be observed how the gain changes with different loads. Both the dominant pole and the open loop gain depend on the load in an inverse way, i.e. if the frequency of the pole gets lower then the DC gain gets larger. The lower the load current, the larger the resistance load, the lower the frequency of the dominant pole and the larger the DC gain (as found in the small signal analysis circuit); this means that the observed gain

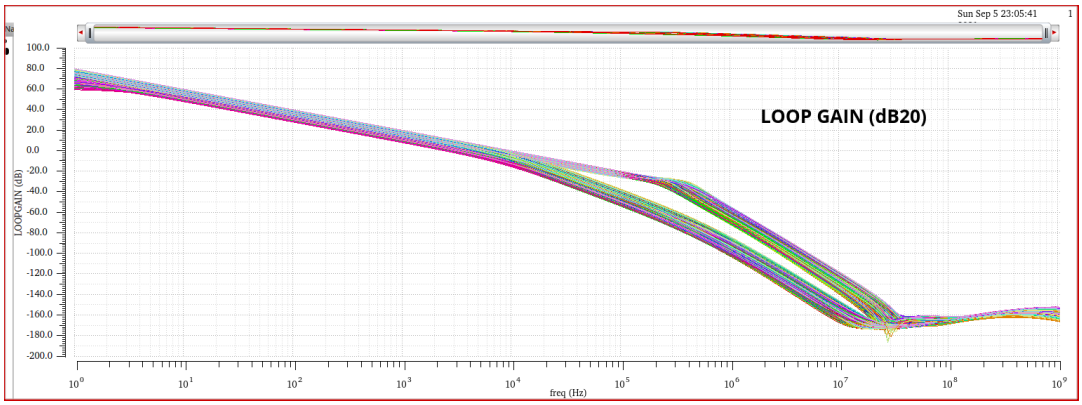

FIGURE 3.16: Loop Gain (dB20) of the circuit with the real bandgap across all design points.

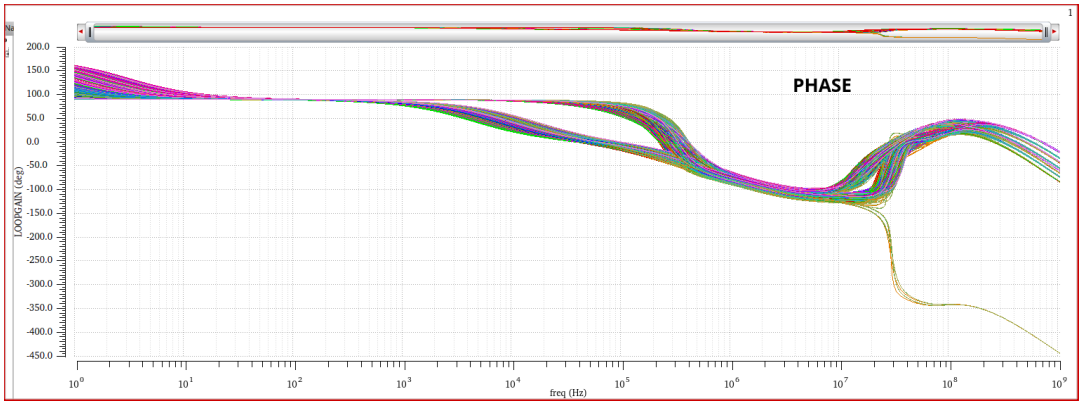

FIGURE 3.17: Phase vs frequency of the circuit with the real bandgap across all design points.

at 1 Hz (the minimum frequency shown in the plot) for zero current will remain approximately the same because the two effects tend to compensate. This is consistent with the plot because comparing nominal conditions with different loads, the 1 HZ gain varies from 76.60 dB (30 mA) to 76.59 dB (10 mA) to 76.36 dB to 76.25 dB. The largest gain value at 1 Hz across all the simulation points is equal 79.98 dB, while the lowest is equal to 59.40 dB.

From the PSRR plot, it can be observed that there is a handful of curves that behaves quite differently from the others, i.e. the ones on the left side of the graph with the wide peaks. These curves represent 10 different corners that are all characterised by the same input voltage $V_{in} = 5V$ and temperature $T = 120C$. It is clear that these are extreme conditions that don't reflect the real behaviour of the circuit, but even in these cases, the overall PSRR peak reaches a value of 30.47 dB at 14 kHz. Neglecting these curves, the peak

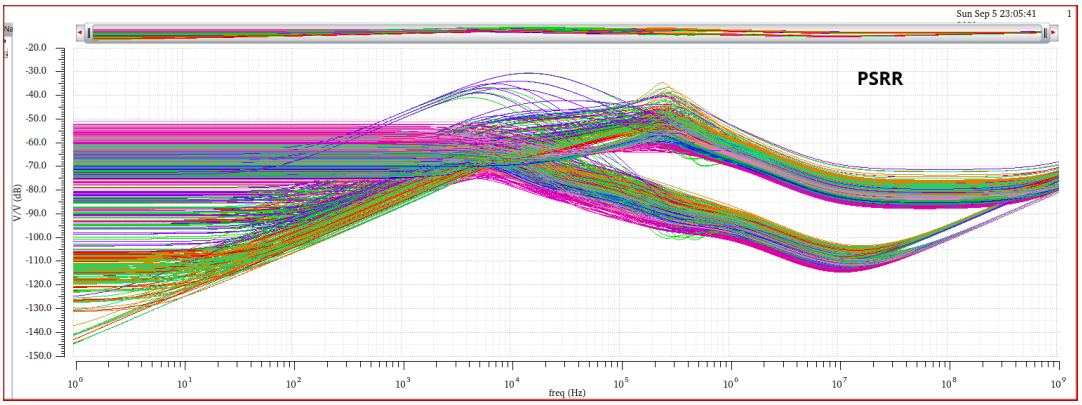

FIGURE 3.18: PSRR vs frequency of the circuit with the real bandgap across all design points.

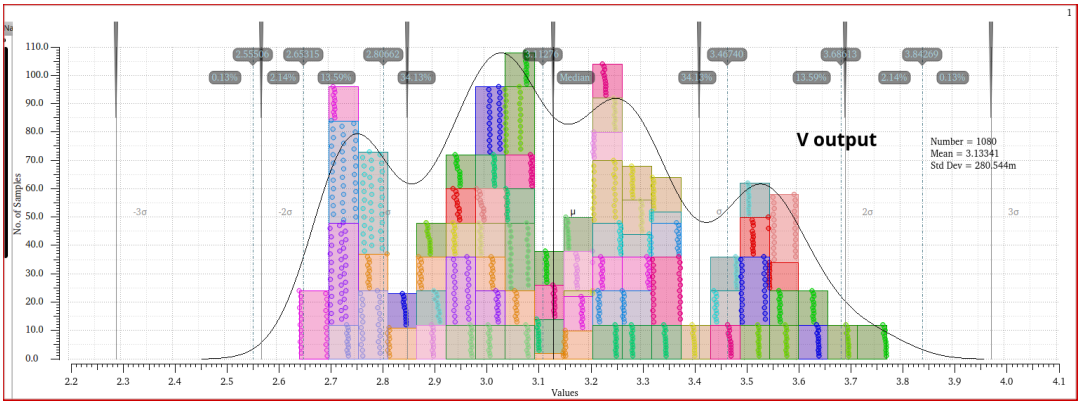

FIGURE 3.19: Histogram of the output voltage across all design points.

across all simulation points is the one equal to 34.58 dB at 240 kHz, while the peak at 1 MHz is equal to 52.15 dB. The PSRR required target is met for all conditions.

Another interesting consideration is that the two poles that were at the same frequency in the nominal case now are split, i.e. one stays at the same frequency while the other moves; this means that only one of the poles depends on the load, in the same way as the dominant pole, i.e. the lower the current load, the larger the resistance load, the lower its frequency, while the other remains at a fixed frequency. The load-dependent frequency pole changes depending on the load approximately from 330 KHz (30 mA), to 240 Hz (10 mA), to 11 kHz (50 uA) to 9 kHz (0 A).

The histograms of the DC output voltage and the phase margin show a different picture. There are some extreme cases where the phase margin falls

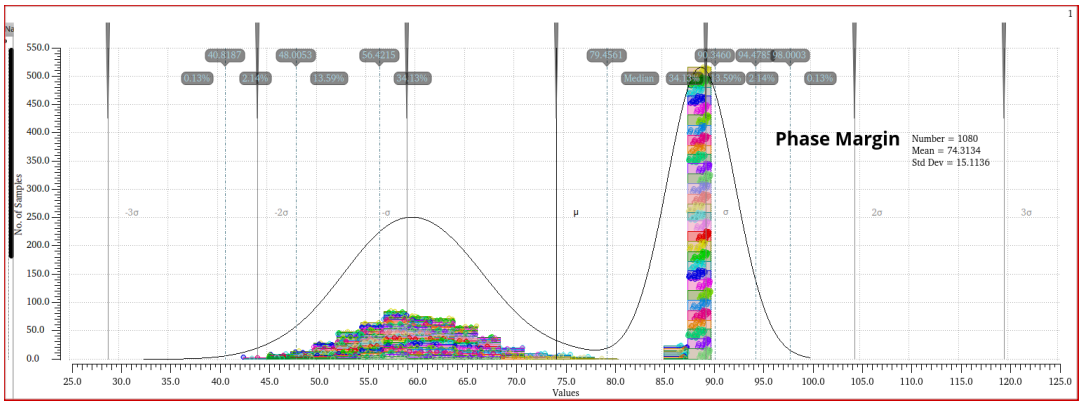

FIGURE 3.20: Histogram of the phase margin with the real bandgap across all design points.

below 50°, but these are specific corners at 5 V input voltage and 0 A current load, i.e. they do not reflect realistic conditions the circuit will encounter. Zero current load can be considered as an impossible situation, given that the drivers will always consume a little bit of power. At 50 uA of current load, that is still much less than the minimum expected current consumption, the phase margin already improves by a significant amount (55°). Moreover, 5 V input voltage can be considered an extremely unlikely case, given that the regulator will typically turn on only for input voltage larger than 6 V because at a voltage as low as 5 V the circuit struggles to keep all the transistors in saturation. Still, the behaviour of the circuit in this condition is acceptable and therefore it is a sign of its reliability.

The DC output voltage histogram is the plot that at first glance can seem disappointing, showing an average output voltage $V_{out} = 3.13V$ and standard deviation $\sigma = 280.5mV$, but there is a simple explanation. DC output voltages have a larger degree of variability, especially taking into account the radiation corners. This is due to the fact that a change in the bandgap voltage reference value affects deeply the feedback resistor ratio; nevertheless, the considered bandgap voltage circuit has already been tested over the years here at CERN in many different real situations and applications, showing on silicon much smaller chip-to-chip variations compared to the simulations. This means that the real behaviour of the regulator is going to be much more similar to a regulator simulated employing a bandgap voltage reference with small variations in its DC voltage value.

In order to consider this situation, a second simulation sweep is performed

with the same sweep points and corners, but now employing a DC ideal voltage source of 619.5 mV as voltage reference instead of the employed bandgap voltage circuit.

Its results can be found in Figure 3.21 (Gain), 3.22 (Phase) and 3.23 (PSRR), while the histograms of Vout and the Phase margin are respectively in Figure 3.24 and 3.25.

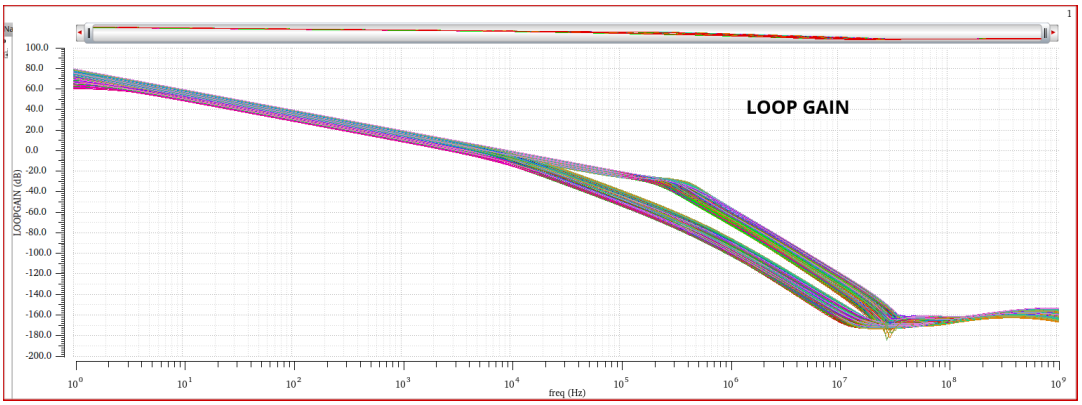

FIGURE 3.21: Loop Gain (dB20) of the circuit with the ideal bandgap across all design points.

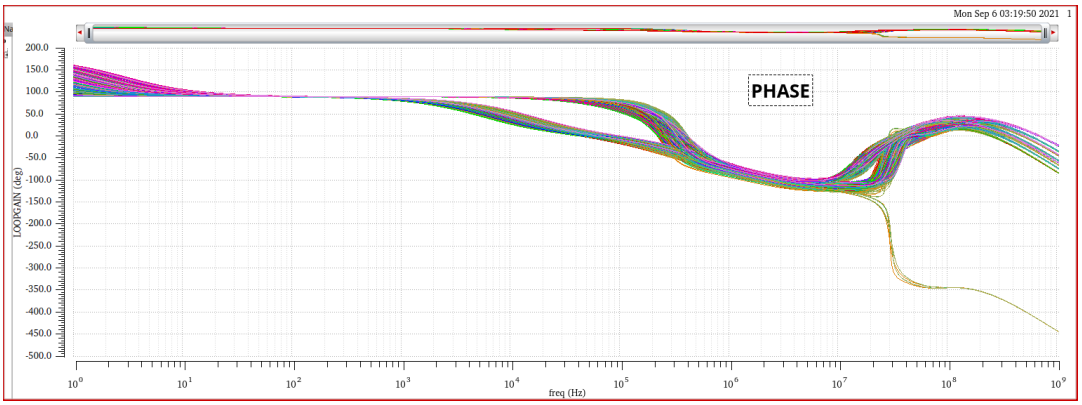

FIGURE 3.22: Phase vs frequency of the circuit with the ideal bandgap across all design points.

In this case, the gain, phase and PSRR plots remain excellent and very similar to the previous ones. Regarding the PSRR plot, the critical corners mentioned priorly in the real bandgap simulation don't represent an anomaly anymore and follow the behaviour of the other curves. The PSRR peak is now a little bit lower, reaching a value of 31.66 dB at 234 kHz. The PSRR value at 1 MHz is now 50.01 dB.

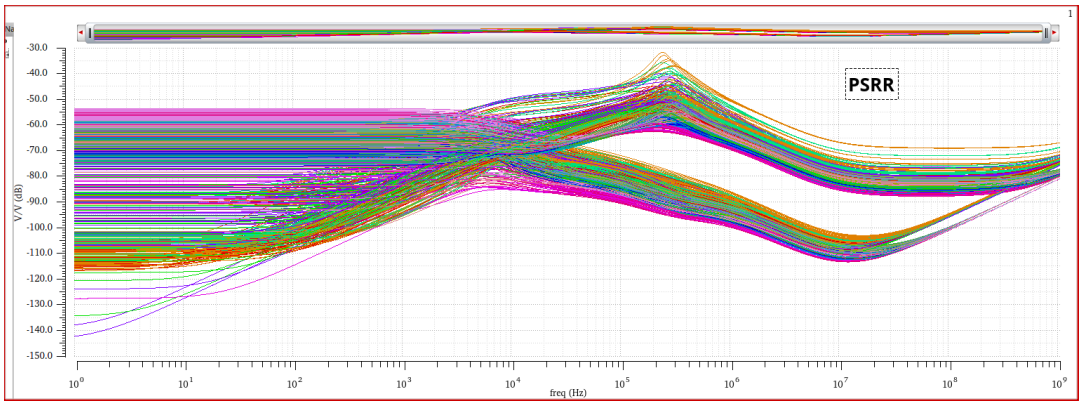

FIGURE 3.23: PSRR vs frequency of the circuit with the ideal bandgap across all design points.

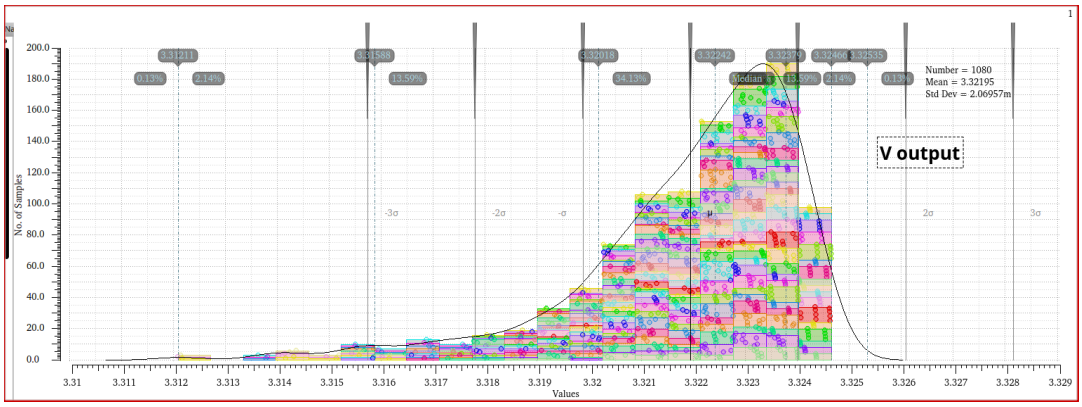

FIGURE 3.24: Histogram of the output voltage with the ideal bandgap across all design points.

The histograms of the phase margin is similar to the real bandgap case. The DC output voltage histogram is where the largest difference from the real bandgap case lies. The average V_{out} and its standard deviation are $V_{out} = 3.32V$ and $\sigma = 2.07mV$ compared to $V_{out} = 3.13V$ and $\sigma = 280.5mV$ in the real bandgap case, showing a significantly consistent V_{out} value.

Let us now consider transient simulations where either the load current or the input voltage changing rapidly over time.

The input voltage change is achieved through a Piece-Wise Linear voltage source employed in the testbench, with the parameters shown in Figure 3.26.

The total simulation time is equal to 600 μs. The result is shown in Figure 3.27.

Similarly, the abrupt change in current load is achieved through a Piece-Wise

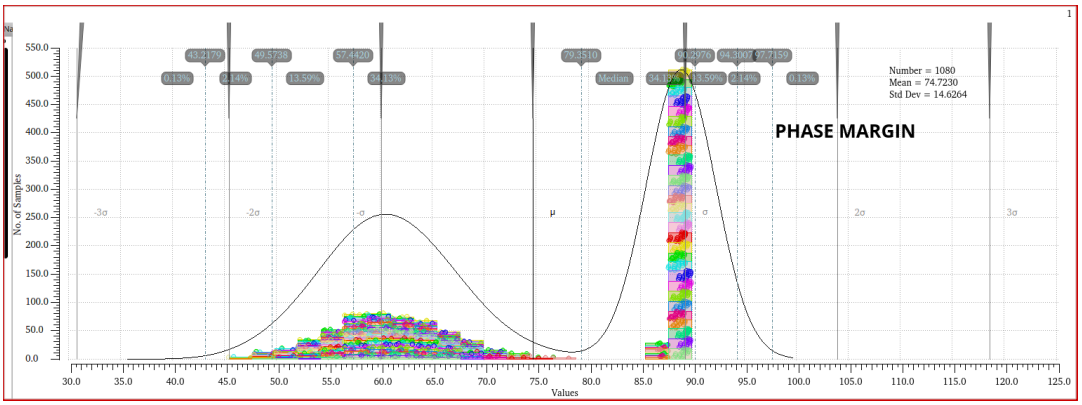

FIGURE 3.25: Histogram of the phase margin with the ideal bandgap across all design points.

Linear voltage source employed in the testbench, with its parameters shown in Figure 3.28.

The total simulation time is now equal to 1000 μs. The result is shown in Figure 3.29

As can be observed from the plots, the circuit responds well to abrupt changes in its input voltage or voltage conditions, reaching a peak of $\Delta V_{out} = 2.5mV$ in the former case and $\Delta V_{out} = 18mV$ in the latter case. It is important to remark that these abrupt changes employed for the simulation are extreme case and in real applications the increase over time will be less sudden.

Moreover, from these plots two parameters very important for the characterization of a linear regulator can be calculated. They are [7]:

- Line regulation, defined as $L_R = \frac{\Delta v_{out}}{\Delta v_{in}}$
- Load regulation, defined as $L_{DR} = \frac{\Delta v_{out}}{\Delta I_{out}}$

From Figure 3.27, V_{in} changes from 5 V to 12 V and V_{out} from 3.3233 V to 3.3226 V :

$$L_R = \frac{\Delta V_{out}}{\Delta V_{in}} = \frac{0.7\ mV}{7\ V} = \frac{-0.1\ mV}{V} \tag{3.18}$$

From Figure 3.29, I_{load} changes from 0 to 30 mA and V_{out} from 3.3229 V to 3.3225 V :

$$L_{DR} = \frac{\Delta V_{out}}{\Delta I_{in}} = \frac{0.4\ mV}{30\ mA} = \frac{-0.013\ mV}{mA} \tag{3.19}$$

Frequency name for 1/period	
Number of pairs of points	5
Time 1	0 s
Voltage 1	5 V
Time 2	50u s
Voltage 2	5 V
Time 3	60u s
Voltage 3	12 V
Time 4	350u s
Voltage 4	12 V
Time 5	360u s
Voltage 5	5 V
Noise file name	
Number of noise/freq pairs	0

FIGURE 3.26: Parameters of the vpwl voltage source employed for the transient simulation.

Their low values confirm that the circuit is able to mantain a stable output value with little variation depending on the V_in or I_{load} value.

Finally, Single Events simulation are performed. In order to simulate the effect of a particular type of single event effect, i.e. SET, the strategy employed is the following.

Two identical current sources with the parameters described in Figure 3.30 are added at each node of the circuit, connecting the other terminal of the current source to either V_{in} or GND.

Each current source has a different delay value added to its waveform in order to observe the effect of each single source separately. The delay value must be large enough to allow the circuit to reach again the equilibrium before the starting of the subsequent current source waveform. A transient simulation, whose runtime must obviously be larger than the maximum current source delay, is then performed and the variation to the output voltages is observed.In this case, the large majority of current sources don't produce any significant effects on the circuit or its output voltage; nevertheless, there are still some voltage spikes at certain critical nodes. These nodes are the ones highlighted in Figure 3.31, called "Vg_p", "Vg_{p2}", "net054"and "net0151". Among these, "Vg_p" and "Vg_{p2}" are nodes where large voltage spikes happen without any visible effect on the voltage output; whereas "net054"and "net0151", being internal to the amplifier, are nodes where large

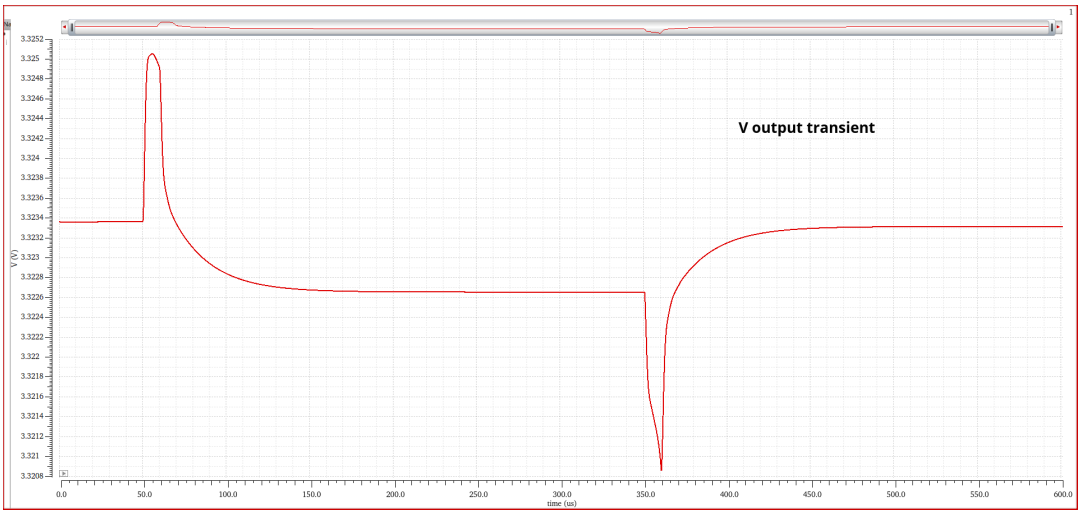

FIGURE 3.27: Transient simulation of abrupt changes in the input voltage over time.

voltage spikes happen with a visible effect on the voltage output. Even though it is highly unlikely that a SEE would cause any damage to the circuit, it would be good to mitigate at least partially this problem in a simple manner.

In Figure 3.32 it can be observed transient value of V_{out} as the SEE happen at the critical nodes. The simulation employed was a transient simulation of 2500 us with the SEE happening at 500 us, 1000 us, 1500 us and 2000 us at respectively . As stated before, the largest effect on the output are caused by the cascode nodes, whereas the other two are unnoticeable.

The proposed solution is to add NMOS transistors to these nodes, with respectively their drain connected to the Vdd of the circuit, their source connected to the node and their gate connected to a fixed bias that is typically at a lower voltage than the source node, but not too much lower than Vdd in order not to break the transistor. Vg_p2 is a biasing node created specifically for this purpose, with a value of $Vg_{p2} = 9.2V$ in nominal conditions. In this way, it becomes an optimal bias for the gate voltage of these transistors, given that in nominal conditions its voltage is always lower than all the source nodes considered. Hence, Vgs is negative and the transistors remain always off, until a SEE happens at one of the critical nodes lowering drastically its voltage value: in this case V_gs becomes positive and the transistor sinks the excess current limiting the voltage spike. Practically speaking, during normal operation conditions they remain off without affecting

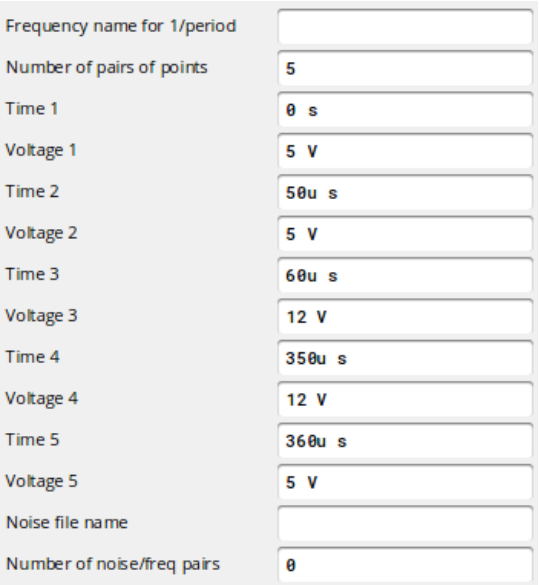

FIGURE 3.28: Parameters of the ipwl current source employed for the transient simulation.

the behaviour of the circuit, but when there are current spikes caused by single events they turn on to absorb the excess current and mitigate the voltage spike. A comparison between absence and implementation of this solution has been simulated, finding the results shown in Figure 3.33 for "Vg_p'", in Figure 3.34 for "net054"node and Figure 3.35 for "net0151"node.

It can be noticed the drastic reduction in the spikes.

Finally, a comparison of the output voltage transient simulation with and without these sink NMOS is presented in Figure 3.36.

The first peak, corresponding to SEE on net054 node, behaves similarly to the previous case, but its voltage spike on the output was already quite limited. In the second peak, i.e. SEE on net0151, the mitigation effect of the NMOS is much larger, with peak voltage value that goes respectively from 3.495 V to 3.365 V.

An overall summary of the performance of the circuit in nominal condition is shown in Table 3.3.

3.4 Layout and techniques

In order to make the circuit more resistant to radiation, ELT (enclosed layout transistor) technique has been employed, creating custom layout of each

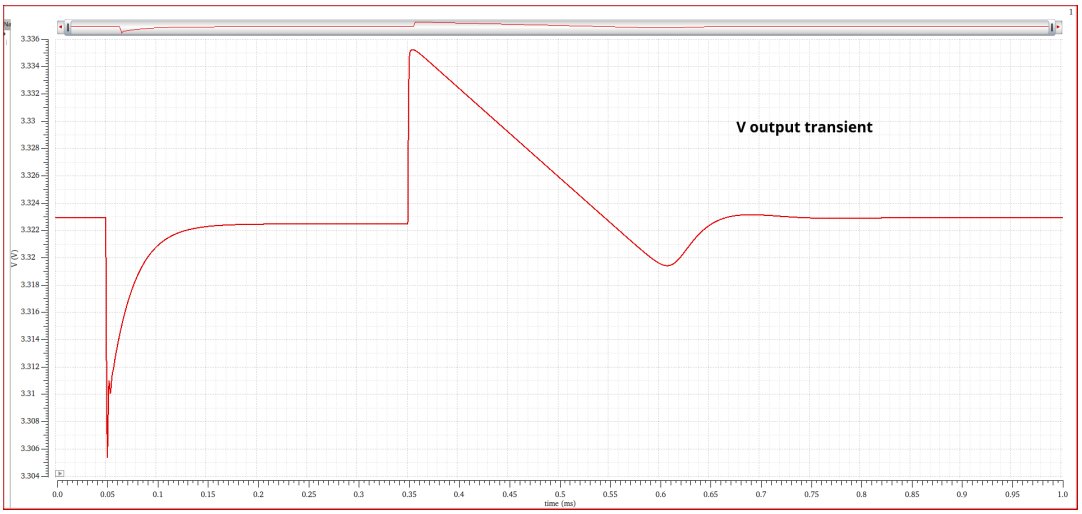

FIGURE 3.29: Transient simulation of abrupt changes in the current load over time.

NMOS in order to match the Width and Length values. Due to the technological process of the manufacturer, transistors are grouped in pockets electrically isolated from the others. Total area of the circuit must be contained in a rectangular area of 200 μm x 500 μum. In order to simplify the connection among transistors, vertical and horizontal lines employing two different metals (metal 3 for vertical lines and metal 2 for horizontal lines) have been traced in order not to create any unwanted intersection and to reduce parasitic contributions. The final layout is shown in Figure 3.37.

The final size of the circuit is equal to 192.25 μm (height) $\cdot$ 471.7 μm (width) $=$ 90684.325 μm^2(total area).

In Figure 3.38 the same layout is presented with the internal structure highlighted for a better comprehension.

The numbers are respectively:

1. DMOS of the source follower stage.
2. Feedback resistors.
3. NMOS sink transistors (SEE).
4. Pocket containing PMOS transistors of the circuit.
5. DMOS transistors (p-type).
6. DMOS transistors (both n and p-type).

Frequency name for 1/period	
Number of pairs of points	7
Time 1	0 s
Current 1	0 A
Time 2	1n s
Current 2	1.16m A
Time 3	3n s
Current 3	440u A
Time 4	5n s
Current 4	280u A
Time 5	7n s
Current 5	200u A
Time 6	33n s
Current 6	120u A
Time 7	100n s
Current 7	0 A
Noise file name	
Number of noise/freq pairs	0
DC current	
AC magnitude	
AC phase	
XF magnitude	
PAC magnitude	
PAC phase	
Multiplier	
Delay time	delay s

FIGURE 3.30: Parameters of the ipwl current source employed for the transient SEE simulation.

7. Capacitor Cc2.
8. Differential pair.
9. NMOS sink transistors (SEE).
10. Pocket containing NMOS transistors of the circuit.
11. Pass transistor.
12. Compensation capacitance C_c.

In can be observed the overall layout structure:

- The circuit is enclosed in a ground contact rectangular border made of metal 2 and metal 3.

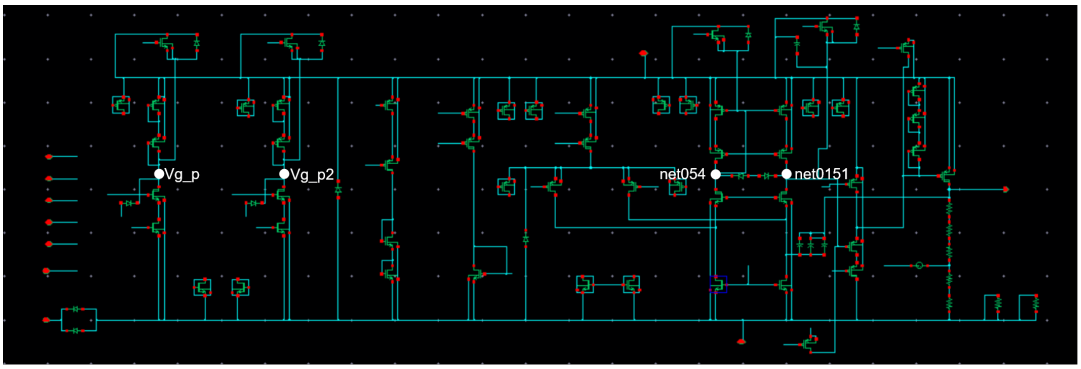

FIGURE 3.31: Critical nodes for SEE highlighted in the schematic.

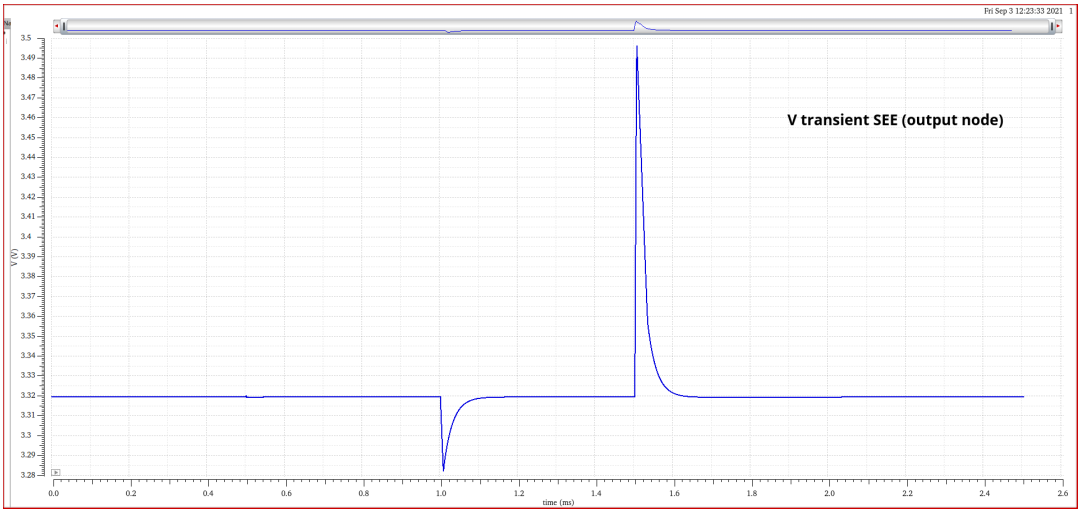

FIGURE 3.32: SEE affecting the output voltage value.

- The VDD track is the large vertical one that can be observed at the center of the circuit.

Finally, in Figure 3.39 the regulator is shown inside the final driver circuit. It has been validated and sent for tapeout, and its behaviour will be tested at CERN.

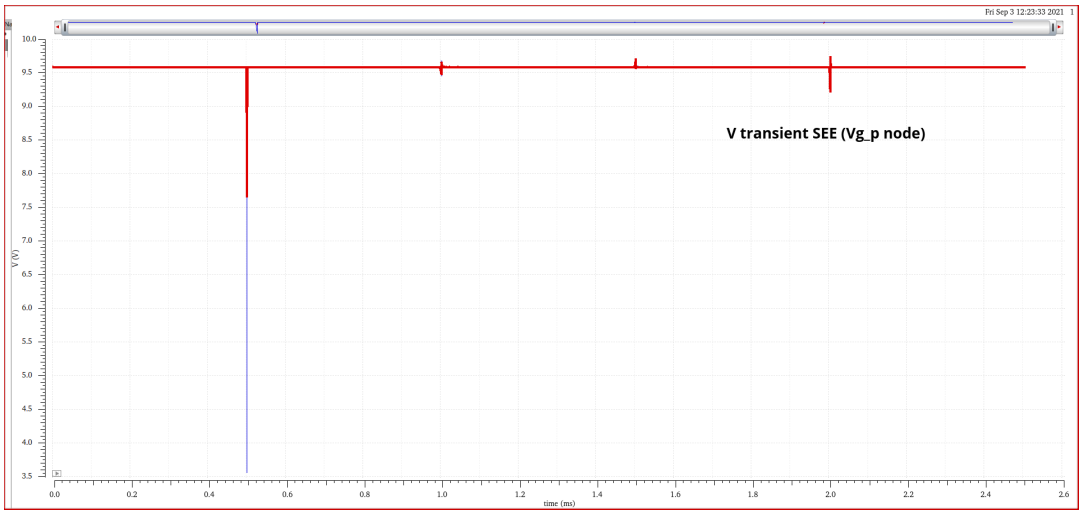

FIGURE 3.33: Comparison of SEE on Vg_p node with and without the sink NMOS transistor.

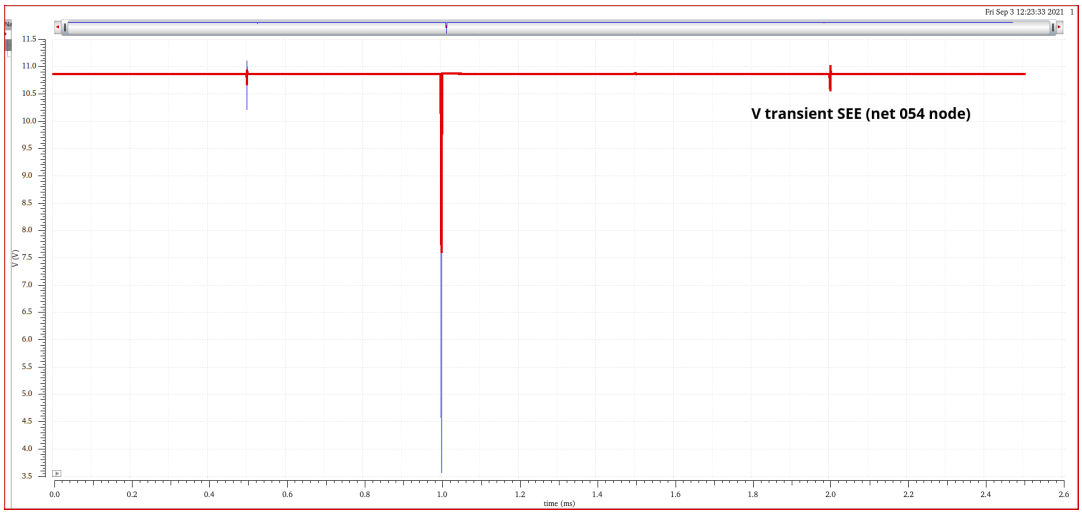

FIGURE 3.34: Comparison of SEE on *net*054 node with and without the sink NMOS transistor.

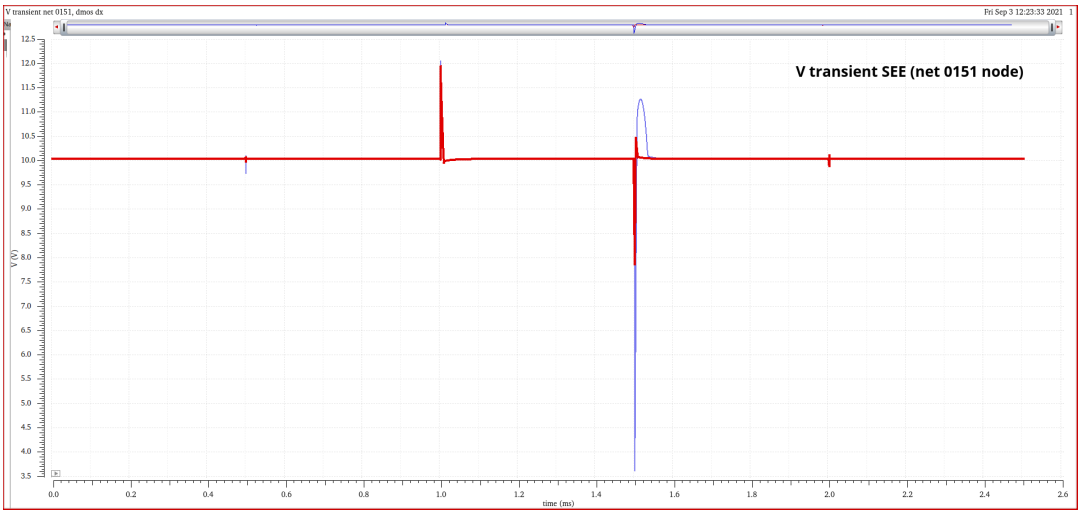

FIGURE 3.35: Comparison of SEE on *net*0151 node with and without the sink NMOS transistor.

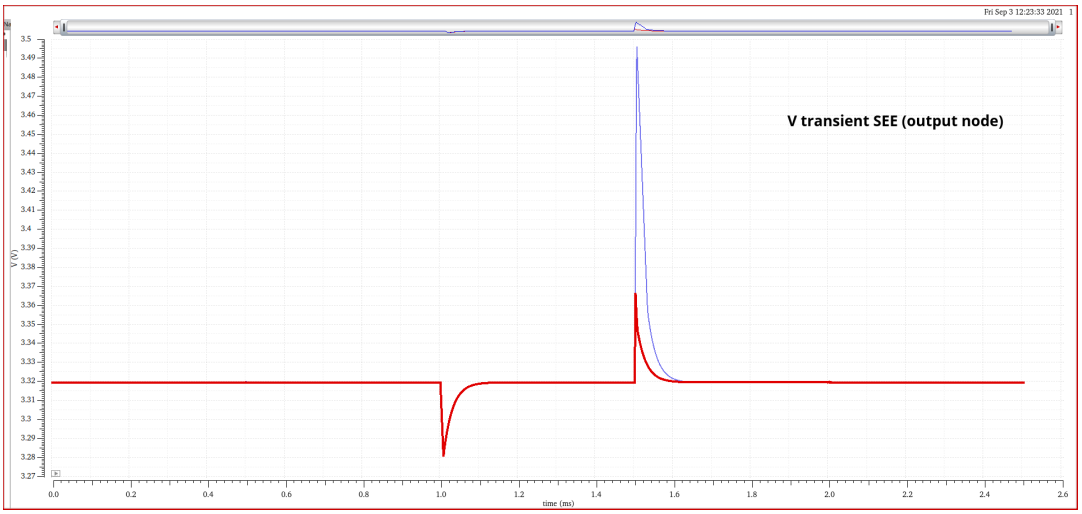

FIGURE 3.36: Comparison of SEE affecting the output voltage value with and without the sink NMOS transistors.

Parameter	Value
Gain (at 1 Hz)	76.59 dB
GBW	6.756 kHz
Phase margin	88.52°
DC PSRR	68.1 dB
Peak PSRR	58.06 dB (at 240 kHz)
L_D (line regulation)	$\frac{-0.1\ mV}{V}$
L_{DR} (load regulation)	$\frac{-0.013\ mV}{mA}$

TABLE 3.3: Overall summary of the performance of the circuit in nominal condition.

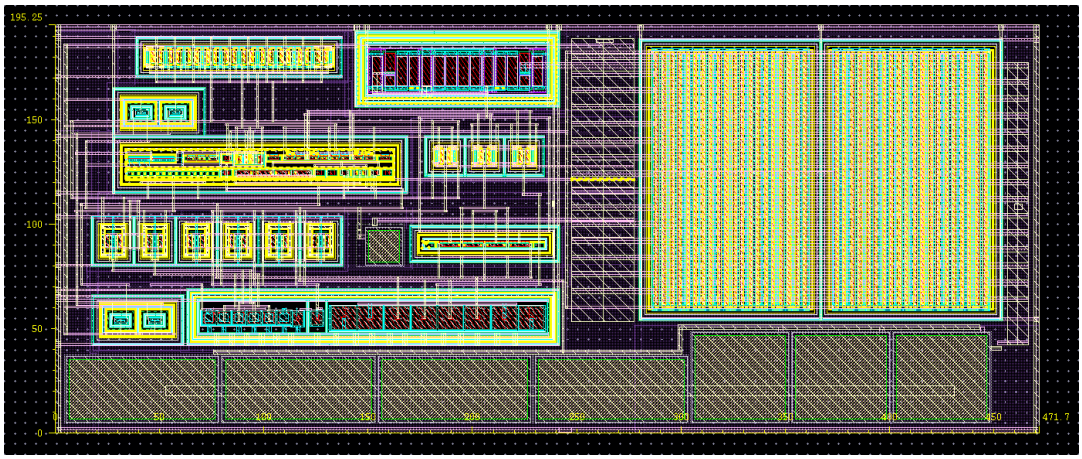

FIGURE 3.37: Screenshot of the final layout of the circuit.

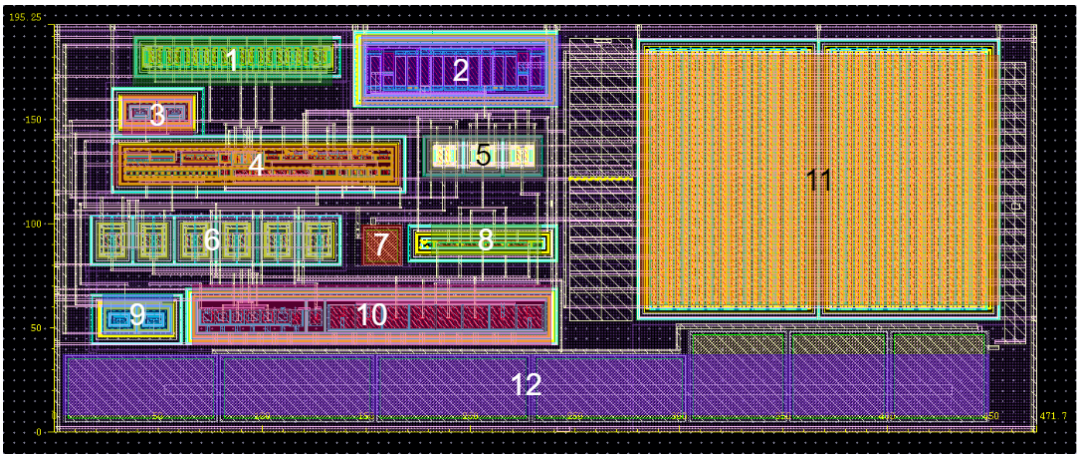

FIGURE 3.38: Screenshot of the final layout of the circuit with its components highlighted.

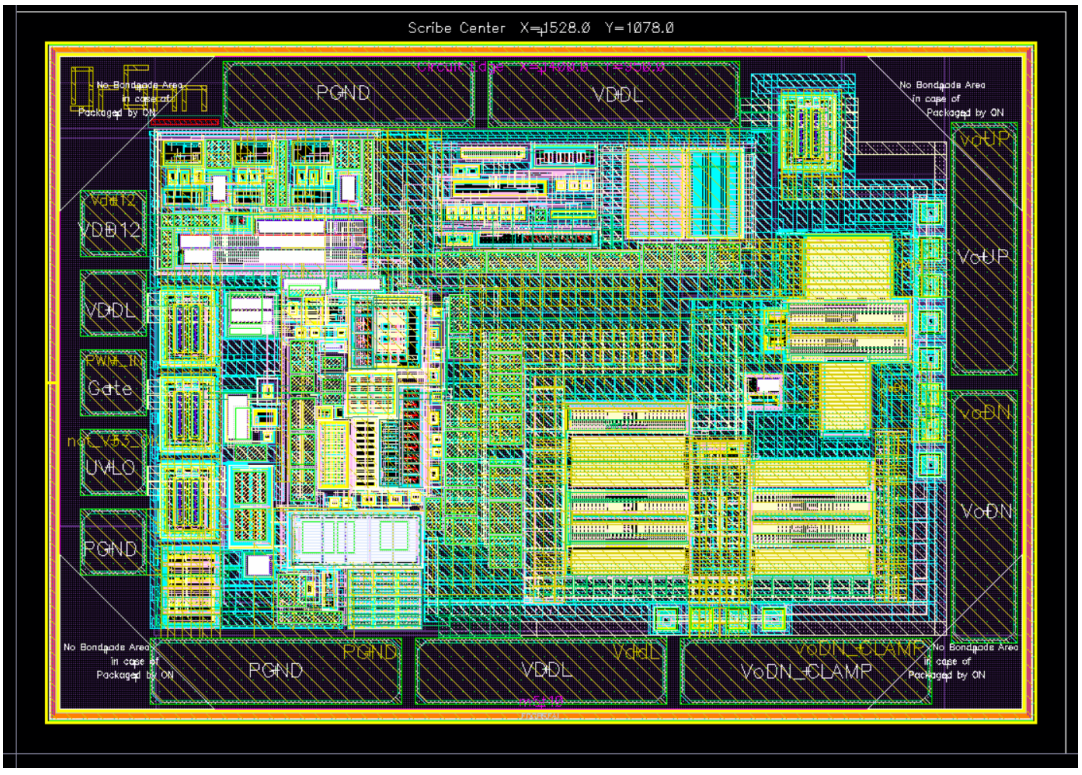

FIGURE 3.39: Screenshot of the final layout of the converter driving circuit.

Chapter 4

Conclusion

In this work, a radiation-hard linear regulator has been developed using a $0.35\mu m$ CMOS technology. It steps down the voltage from a 12V input to provide a 3.3V output voltage and power the gate drivers of Gallium Nitride power FETs. In a GaN-based buck converter using a conventional bootstrapping technique, the use of such regulator guarantees that the power supply of the high-side driver is not overcharged due to the large negative voltages reached by the switched node during the dead times.

This project has involved the choice of the topology for the linear regulator, the device sizing, the small-signal analysis (which highlighted the benefits of using the indirect feedback technique for the frequency compensation), the validation of the circuit through simulations and the design of the full-custom layout.

The linear regulator has been designed for high-radiation environments, such as the one found inside the High-Luminosity Large Hadron Collider experiments at CERN. To take into account the effect of radiation during the design phase, dedicated corner simulations to consider the TID-induced degradation (up to a 100 MRad) were employed, while the effect of charge injection due to Single Event Effects has been also simulated. Moreover, the full-custom layout has been developed employing radiation hardening techniques, such as the use of Enclosed Layout Transistors for nmos devices to suppress their radiation-induced leakage current.

The simulation results show a stable output voltage of 3.3 V, with a mean value and standard deviation of respectively $V_{out} = 3.32V$ and $\sigma = 2.07mV$ across all simulation points, i.e. taking into account temperature ranges from -30 ^oC to 120 ^oC, input voltage ranges from 5 V to 15 V, load value ranges from 0 up to 30 mA and a TID to 100 MRad. In addition, the PSRR, gain and

phase characteristics of the circuit meet the design targets in every simulated condition.

The final converter driving circuit, which includes the design linear regulator, has been validated and released for fabrication, and it will be soon tested at CERN.

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