POLITECNICO DI TORINO

Master of Science Degree in
Electronic Engineering

Analysis, design and efficiency optimization of a capacitively isolated AC-DC adapter

Master's thesis

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Abstract

Over the past century, the transfer of electrical energy without wires has become a very active research topic, due to its convenience and safety over wired methods. Wireless Power Transfer (WPT) is applied in numerous applications, such as cellphone charging, static and dynamic electric vehicles charging and bio-medical implants (powering life-critical devices).

There are several techniques to implement WPT, which differ in the type of electromagnetic energy they use for power transmission: magnetic fields, electric fields or electromagnetic radiation, like microwave or laser beams. Among these, inductive coupling between coils of wire, generating alternating magnetic fields, is the most widely used wireless power technology. This method is known as Inductive Power Transfer (IPT).

Capacitive Power Transfer (CPT) is the counterpart of IPT, in which power is transferred by means of electric fields. This technology is being actively studied nowadays, since CPT does not require the use of ferromagnetic material (e.g. ferrites) to improve coupling or provide field shaping. In the capacitive interface, the field is confined between low cost metallic plates, thus alleviating the necessity for magnetic flux guiding and shielding components that increase bulk and cost to the system. The simplicity and lower cost of capacitive interfaces make them a potential method for wireless charging stations and galvanically isolated power supplies.

In this thesis, a capacitively isolated power supply is studied in detail, both by circuit analysis and simulations. The system is designed to provide 40 W of power at nominal load, starting from the electric grid. A key aspect of this analysis is the system efficiency. This important parameter is deeply studied and optimized to have a high value not just at nominal load, but for the entire working range.

Acknowledgments

I would like, first of all, to thank my thesis supervisors: Prof. Paolo Crovetti, Prof. Francesco Musolino and Ing. Mario Pavone. Their dedication and predisposition, reflected in weekly meetings of up to 2 hours in duration, have been invaluable in the development of this thesis. I would also like to thank my colleague, Alberto Pili, who worked alongside me on a similar project.

Grateful to my family, starting with my parents, Marina and Héctor, who gave me the opportunity to start studying and finish my career abroad. To my older sister, Carla, whose personal support made my time in Italy as enjoyable as possible, and my younger sister, Laura, who accompanied me daily despite the distance. Also to my older brothers, Claudio and Mauro, to my grandparents, uncles and cousins, who are always there.

Even though I spent a year and a half abroad, my lifelong friends from Argentina were always present to accompany me. To them, and to the friends I made along the way, thank you very much for all your support.

Rounding out, I would like to thank all the people who, in one way or another, helped in my motivation, inspiration and perseverance to achieve my goals.

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Chapter 1

Introduction

In this chapter, the topic of the thesis is briefly introduced. The motivation, main objectives and a short description of the general structure of the thesis are presented, to serve as an overview.

1.1 Motivation

The transfer of electrical energy has traditionally needed the use of physical connections, that is, wires that connect a transmitter device to a receiver device. Recently, research on wireless power transfer (WPT) has become increasingly important, mainly due to the enormously growing number of portable devices, whose wired chargers limit their portability [1].

WPT is an extremely useful technology that has many applications and benefits. It can eliminate the use of wires and batteries, thus increasing the mobility, convenience, and safety of cell phones, laptops and other mobile devices. Also, this technology is useful to power electrical devices where interconnecting wires are inconvenient, hazardous, or are not possible.

A generic block diagram of a WPT system is reported in Figure 1.1. In a WPT system, a transmitter generates a time-varying electromagnetic field. This energy-contained field is transmitted across the space to a receiver, that converts the fields back into electric power and supplies it to an electrical load.

The WPT technologies differ in the type of electromagnetic energy they use: time-varying electric fields, magnetic fields, radio waves [3] or microwaves [4], among others. The most common implementation of WPT is through the use of alternating magnetic fields, producing inductive coupling between coils. This technology is called Inductive Power Transfer (IPT) [5].

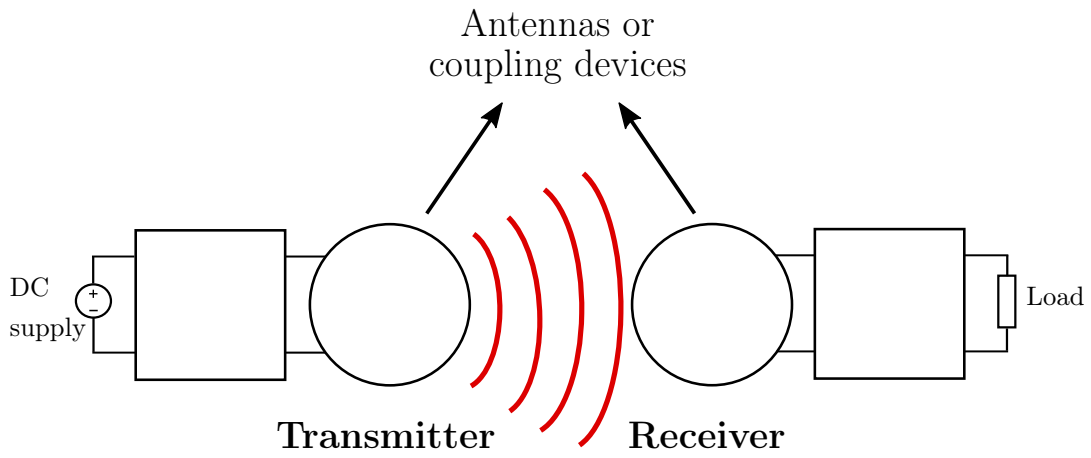

Figure 1.1: Typical structure of a Wireless Power Transfer system

Capacitive power transfer (CPT) technology is an alternative to the conventional IPT, that uses time-varying electric fields to transfer power between two metallic plates forming a capacitance [6]. The main advantage of CPT versus IPT is the use of a simpler, lighter and cheaper interface between transmitter and receiver.

There are many applications of the CPT technology. Electric vehicle charging is one that benefits from the use of CPT, since the electric fields can pass through the metal materials of the vehicle without generating significant power losses. For this application, a high power is needed, and it is shown in [7] that the CPT technology is able to achieve several kW power transfer, with an efficiency higher than 90%. Therefore, it is proven that CPT technology is suitable for this kind of applications.

Another interesting application for this technology is in isolated converters, where in this case the capacitive interface is used to provide galvanic isolation between the primary and the secondary. Usually, this is achieved by using a transformer, which adds complexity and cost to the power converter. Therefore, a transformerless power supply, that provides insulation by means of a pair of capacitors, is an attractive solution for AC-DC adapters.

1.2 Objective of the thesis

The objective of this thesis is to analize and design a capacitively isolated AC-DC adapter. In this power supply, discrete capacitors are used as galvanic isolation between the primary and secondary side. The analysis focuses on the study and optimization of the system efficiency.

1.3 Structure

In Chapter 2, the circuit topology to design the capacitively isolated power supply will be presented and analized. The analysis of this system will begin using some simplifications, and the necessary working conditions to obtain high efficiency will be established. Later, the equations that rule the behavior of the circuit will be provided, which will be verified by simulations later on.

Once the equations of the system have been obtained, the circuit will be designed to meet a series of requirements. Through simulations, these equations will be verified, and it will also be possible to perform a frequency analysis. This is the topic of Chapter 3.

In Chapter 4, the efficiency of the system will be studied. It will begin with a detailed analysis of the losses on each of the circuit components, according to which the efficiency at nominal load can be calculated. As the system is expected to work for a range of loads, it is interesting to observe efficiency curves. To develop these curves, a few simplifications are considered.

Finally, the limitations of the system will be studied in Chapter 5. It will be observed that the main limitations are due to problems related to inductors, and solutions to solve them will be proposed. Through this analysis, an optimal design is proposed, in which it is intended to obtain a balance between the different limitations and performances of the circuit.

Chapter 2

System analysis

In this chapter, capacitive power transfer (CPT) technology will be introduced. Different implementations using various compensation networks topologies will be briefly discussed, and one of them will be studied in detail. Since the CPT system contains non-linear elements such as diodes and transistors, a precise analysis is complicated and this is why linear simplifications will be considered. Then, this simplified linear circuit will be studied using standard AC analysis, to conclude with the analysis of the non linear circuit.

2.1 Capacitive power transfer

As mentioned in Chapter 1, capacitive power transfer (CPT) technology is an alternative to the conventional IPT, that uses time-varying electric fields to transfer power between two metal electrodes forming a capacitance. Even though IPT systems offer higher power transfer and efficiency than CPT systems, the latter can offer equally good galvanic isolation while providing some advantages [8]:

- A CPT system interface consists of just some metal plates, making it cheaper and lighter than the IPT interface (that includes a magnetic core).
- Since CPT technology uses electric fields to transfer power, there is no concern about the eddy-current loss in nearby metals. On the other hand, due to the magnetic fields used in IPT systems, significant eddy-current losses can be generated using the inductive technology.
- Experimental results show that CPT systems have much better misalignment performance than IPT systems.

Due to these features, research on CPT technology is becoming popular in recent years.

The typical structure of a CPT system is shown on Figure 2.1. It is a DC-DC converter, implemented using an inverter, compensation networks and a rectifier. The inverter is used to provide a high frequency excitation to the compensation network, in order to achieve effective power transfer through the capacitive interface. At the output, a rectifier serves to supply DC current to the load.

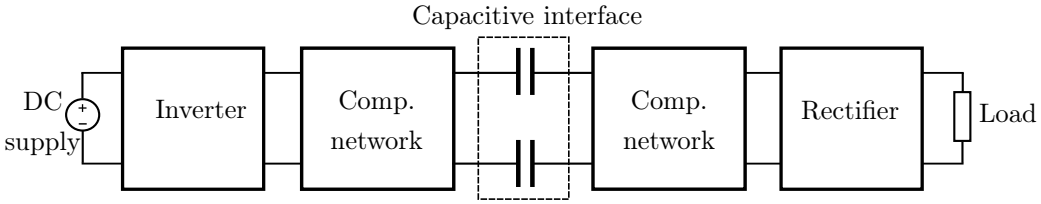

Figure 2.1: Typical structure of a Capacitive Power Transfer system

2.1.1 Compensation network

A compensation network (also called tank) is needed to cancel the reactance of the capacitive interface, which is achieved by designing the compensator to form a resonant circuit with the capacitive interface. The compensator being a resonant circuit is a necessary condition to achieve soft switching on the inverter, which is critical for good system performance, as will be explained in Section 2.3.

Different CPT systems can be distinguished by their compensation circuit topologies, which determine the system power capability, efficiency, and frequency properties [9]. The compensator is usually an inductor, or a combination of inductors and capacitors in series or parallel configuration.

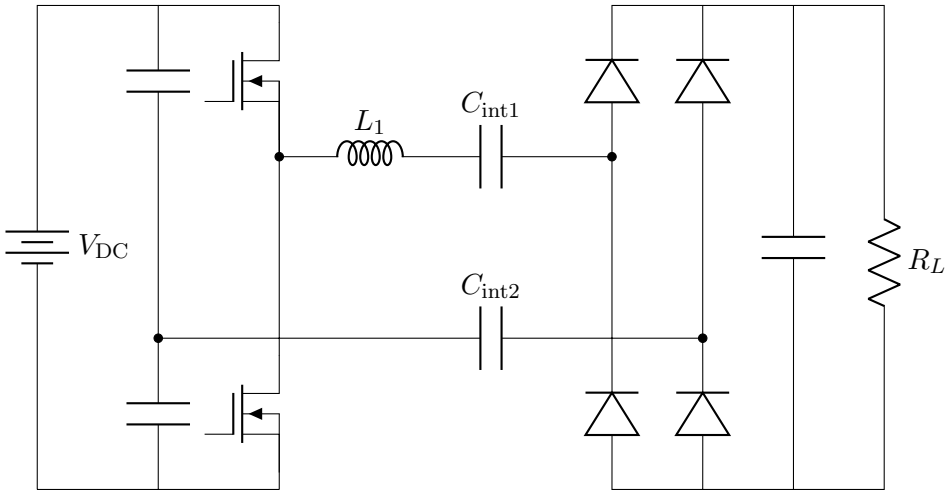

Figure 2.2: CPT system with series L compensator

The most simple compensation circuit is the series L compensator, in which an inductor is connected in series to the capacitive interface, as shown in Figure 2.2 [10].

The series inductor L_1 is designed to resonate with the capacitive interface at the working frequency, cancelling its reactance. Even though this network is simple and cheap, it has the drawback of needing a large inductor to compensate the tipically low capacitance of the capacitive interface. This capacitance is usually around 100 pF, so for a working frequency of 1 MHz, an inductance in the order of 250 µH is needed.

By adding more components to the compensation network, design flexibility is increased but at the expense of increasing complexity, weight, and cost. Adding an LC network at the transmitter and receiver side of the circuit of Figure 2.2, the LCL-LC compensator shown on Figure 2.3 is developed. This topology provides high power factor and achieves multiplication of the load current with respect to the interface current, therefore reducing the voltage stress of the interface and the losses of the compensation inductor L_2 [11]. It also provides flexibility of tuning the system power according to component values.

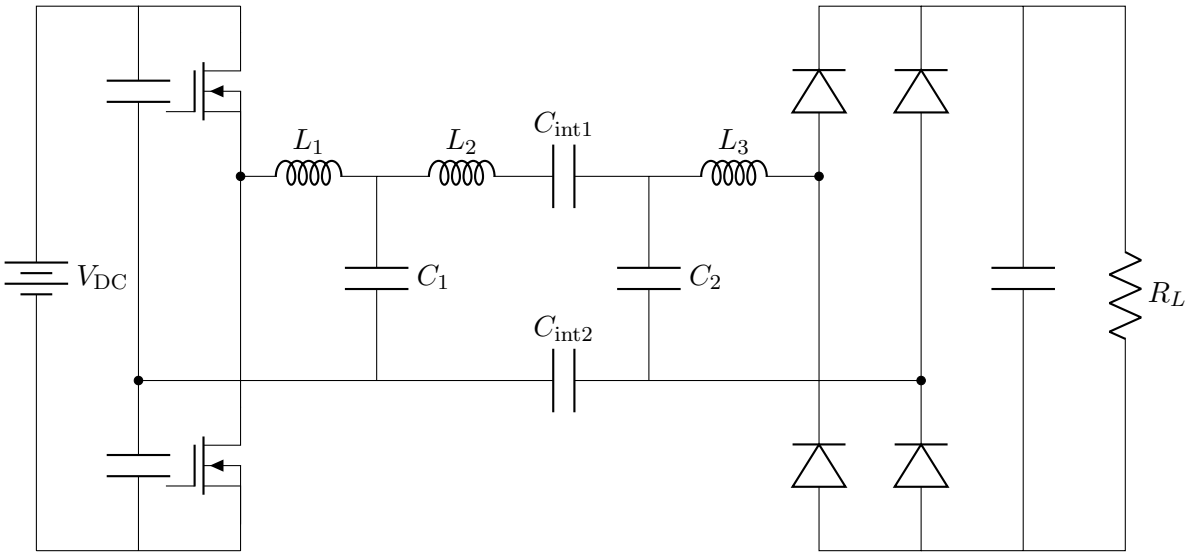

Figure 2.3: CPT system with LCL-LC compensator

The objective of this thesis is to design a power adapter starting from the rectified voltage of the electric grid, so V_{DC} is in the order of 300 V. Since the $L_1 - C_1$ network is used to increase the voltage levels of the circuit in order to achieve higher power transfer, for this design it will not be needed.

Therefore, the CPT system analyzed in this thesis is the LCL compensator, shown in Figure 2.4. Since this system contains non linear blocks (inverter and rectifier), linear simplifications on them will be studied before starting the circuit analysis.

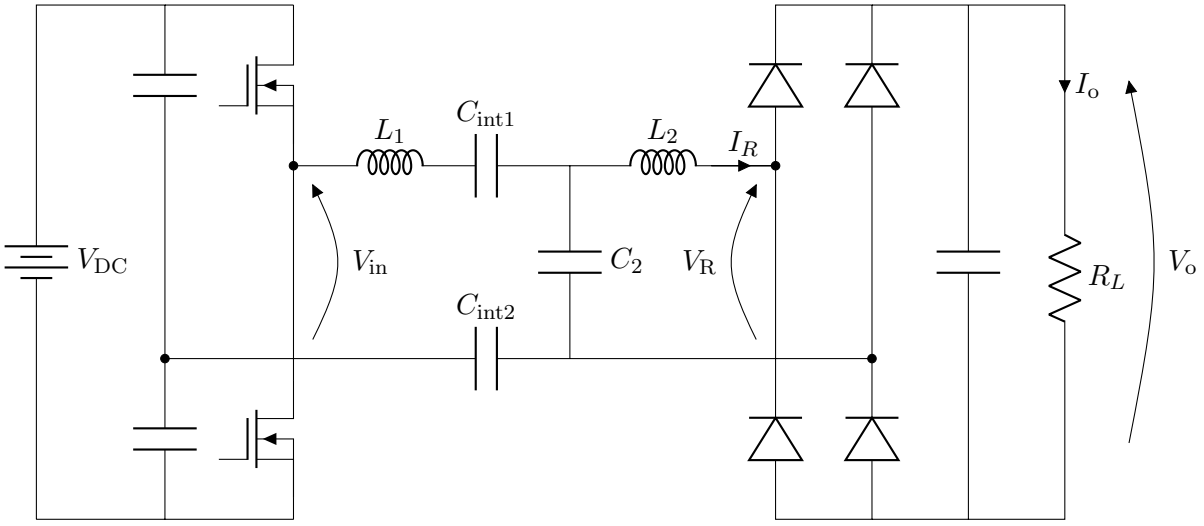

Figure 2.4: CPT system with LCL compensator

2.2 System simplifications

As mentioned, the system to be analized is the CPT with LCL compensator of Figure 2.4, which contains three main blocks:

- A half bridge inverter,
- A compensation network, and
- A diode bridge rectifier.

The inverter converts the supplied DC power into AC, in the form of a square wave voltage with a frequency equal to the compensation circuit resonant frequency. This resonant network rings with approximately sinusoidal waveforms, and its output is rectified by the diode bridge rectifier to supply DC current to the load.

Exact analysis of this resonant system would lead to a complex model that could not be easily used to derive a handy design procedure. In this thesis, a simplified method for resonant topologies will be used, which is based on the assumption that input to output power transfer is essentially due to the fundamental Fourier series components of currents and voltages [12]. This is what is commonly known as the "first harmonic approximation" (FHA) technique, which enables the analysis of resonant converters by means of classical complex AC circuit analysis.

The non linear blocks, i.e. the inverter and rectifier, will be linearized using the simplifications explained in the following subsections, and with more details on [13].

2.2.1 Inverter simplification

The proposed topology uses a half-brigde inverter, which is made by two power MOSFETs. These devices are driven on and off symmetrically with 50% duty cycle. Therefore, the input voltage of the resonant network, V_{in}, is a square wave of amplitude V_{DC}. Due to the capacitive voltage divider at the input, this voltage ranges from $-\frac{V_{\text{DC}}}{2}$ to $\frac{V_{\text{DC}}}{2}$, with an average value of 0 V.

This square wave voltage can be expressed in Fourier series as follows:

$$V_{\text{in}}(t) = \frac{2V_{\text{DC}}}{\pi} \sum_{n=1,3,5,..} \frac{1}{n} \sin(2\pi n f t) \tag{2.1}$$

Equation (2.1) means that the square wave can be decomposed into the sum of infinite sine waves, of different frequencies and amplitudes. In particular, it contains a component at the fundamental frequency and at all odd harmonics. In Figure 2.5, it is seen the original square wave in blue, with its fundamental component and the 3rd and 5th harmonics, for a particular case of $V_{\text{DC}} = 20\,\text{V}$.

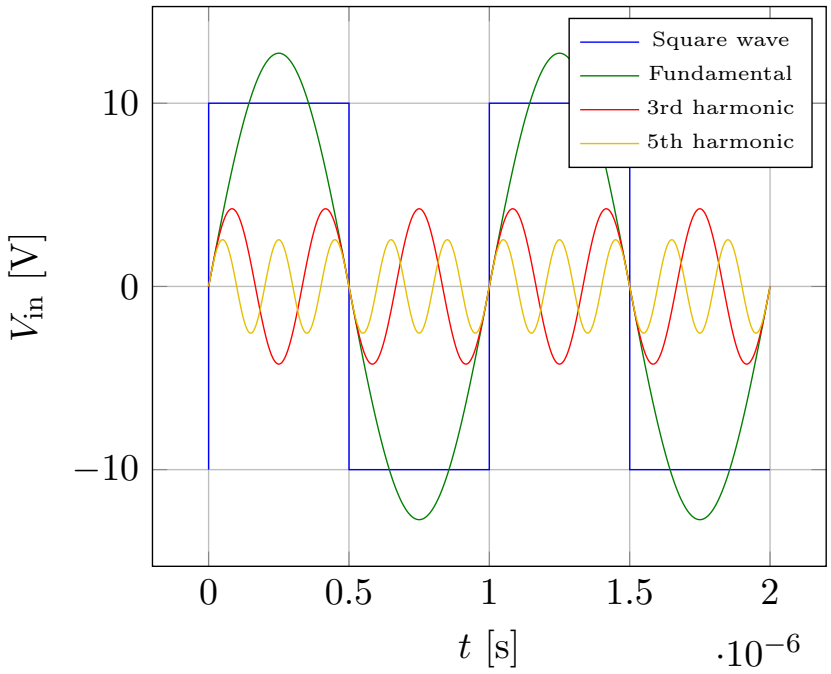

Figure 2.5: Inverter output voltage with its harmonic decomposition

Due to the selective nature of resonant circuits, all components besides the fundamental can be assumed to be filtered out. Therefore, all higher harmonics are neglected and the circuit waveforms are consequently assumed to be purely sinusoidal at the fundamental frequency. This is the FHA approach.

The inverter output terminal (the square wave voltage V_{in}), is then modeled as a sinusoidal voltage generator, with a peak value equal to the one of its fundamental component. This generator is expressed in phasor domain as follows:

$$V_{\text{in}} = \frac{2V_{\text{DC}}}{\pi} \tag{2.2}$$

2.2.2 Rectifier simplification

At the output of the CPT system there is a diode bridge rectifier, made using four diodes. This block is driven by the sinusoidal current I_R. Its input voltage, V_{R}, reverses when the current becomes zero. Therefore, the input voltage of the rectifier is a square wave in phase with its input current.

Making a Fourier analysis similar to Section 2.2.1, the fundamental component of V_R can be expressed in phasor domain as follows:

$$V_{\text{R}_{\text{fund}}} = \frac{4V_{\text{R}}}{\pi} \tag{2.3}$$

The input voltage of the rectifier, V_R, is approximately equal to the output voltage of the system, V_{o}. There is a slight difference between these two quantities due to the forward voltage drop on the diodes. In this analysis, the forward voltage drop is neglected and therefore V_R and V_{o} are considered to be equal:

$$V_{\text{R}} = V_{\text{o}} \tag{2.4}$$

The input current of the rectifer, I_R, is rectified and then filtered by the output capacitor. This produces a DC output current equal to:

$$I_{\text{o}} = \frac{2}{\pi} I_R \tag{2.5}$$

As previously stated, the rectifier input current I_R is in phase with the fundamental component of the rectifier input voltage V_R. Therefore, the rectifier presents an equivalent resistive load R_e to the compensation circuit. This resistance is obtained by the division of (2.3) by (2.5), and considering the approximation expressed in (2.4):

$$R_e = \frac{V_{\text{R}_{\text{fund}}}}{I_R} \tag{2.6}$$

$$R_e = \frac{8}{\pi^2} \frac{V_{\text{o}}}{I_{\text{o}}} \tag{2.7}$$

$$R_e = \frac{8}{\pi^2} R_L \tag{2.8}$$

Thus, the compensation circuit is loaded by an effective resistance R_e, approximately equal to 81% of the actual load R_L.

2.2.3 Equivalent circuit

Applying the simplifications on the inverter and rectifier, the non linear circuit of Figure 2.4, can be transformed into the linear circuit of Figure 2.6. In this approximation, a sinusoidal input source excites the resonant tank, which then drives a resistive load. This transformation allows the use of standard linear analysis to study the system.

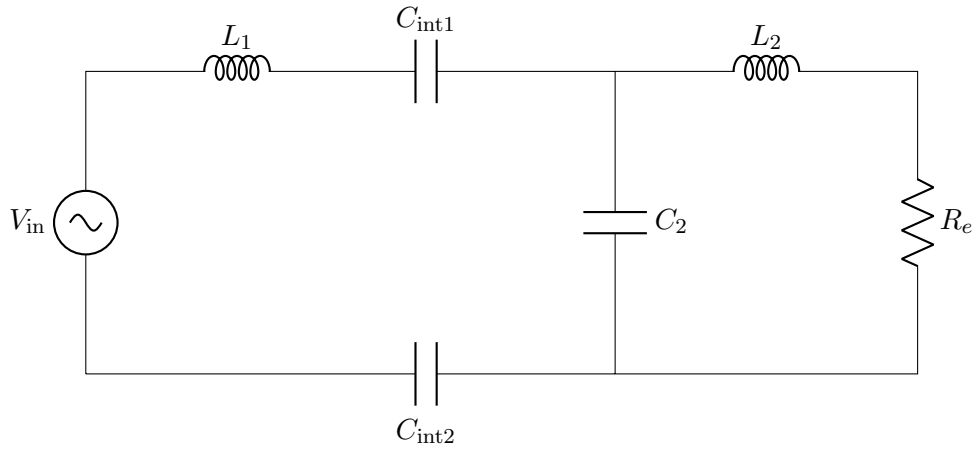

Figure 2.6: Equivalent linear circuit

It can be observed that the two capacitors of the capacitive interface, C_{int1} and C_{int2}, are in series. Therefore, they can be replaced by a single equivalent capacitor:

$$C_1 = \frac{C_{\text{int1}} C_{\text{int2}}}{C_{\text{int1}} + C_{\text{int2}}} \tag{2.9}$$

Making this replacement, the circuit of Figure 2.7 is obtained. This is the linear circuit that will be analyzed and studied.

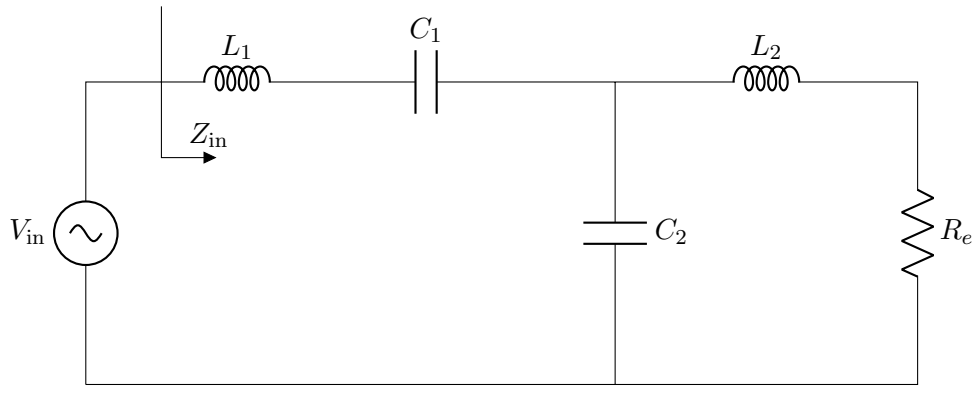

Figure 2.7: Simplified linear circuit with equivalent capacitive interface

2.3 Zero phase angle

Before starting the circuit analysis of Figure 2.7, the concept of zero phase angle (ZPA) must be introduced.

Zero phase angle is a condition in which the phase of the compensation network input impedance, Z_{in}, is zero, which means that this impedance is purely resistive. Therefore, the inverter output current and voltage lie in phase. ZPA operation is very important to reduce the volt-amp (VA) rating, thus enabling lower stress on the inverter at a given load.

Another important reason to work under ZPA condition, is to realize soft switching at the inverter [14]. This is a method of switching in which during the switching time, there is no simultaneous presence of voltage across the transistor and current through it. To achieve this, the transistors are turned on and off at zero voltage (zero voltage switching) or current (zero current switching) [15], [23]. This technique greatly reduces the power dissipated by the transistors during the switching time, while at the same time eliminating much of the generated high frequency noise.

Figure 2.8 shows the current and voltage waveforms of a hard switched transistor. The red curve is the voltage across the device and the blue one is the current through it. It is observed that during transitions, there is an overlap of the current and voltage waveforms, which will cause power loss due to the non immediate commutation between the on and off states.

In contrast, Figure 2.9 shows a soft switched device, in which the current is zero during on-off transitions (zero current switching). This behaviour provides the elimination of the switching power loss, therefore increasing system efficiency.

There are several methods to achieve ZPA operation. These include proper selection of the compensation network passive components, and dynamic tuning of circuit parameters, either by varying the switching frequency [16] or tank components [17]. However, it is preferred to obtain ZPA through appropriate selection of passive components, in order to avoid complexities involved with dynamic tuning, such as frequency bifurcation where more than one primary ZPA frequency exists [19].

Conventional approach of deriving required compensation components leads to load dependent ZPA [15]. However, it is shown in [18] that with appropriate design of the tank network, ZPA operation can be independent on the load.

In this thesis, a method for obtaining load independent ZPA through proper selection of passive components will be proposed. It will begin with the cancellation of the input reactance at fixed load, and will then proceed with the establishment of a condition to obtain ZPA at any given load.

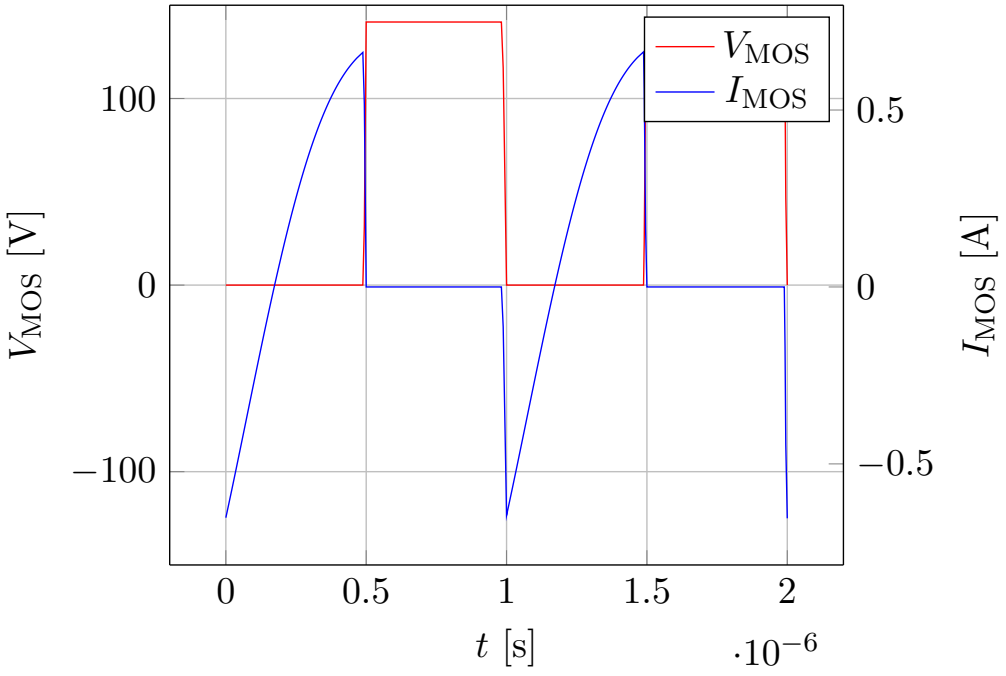

Figure 2.8: Hard switching current and voltage waveforms

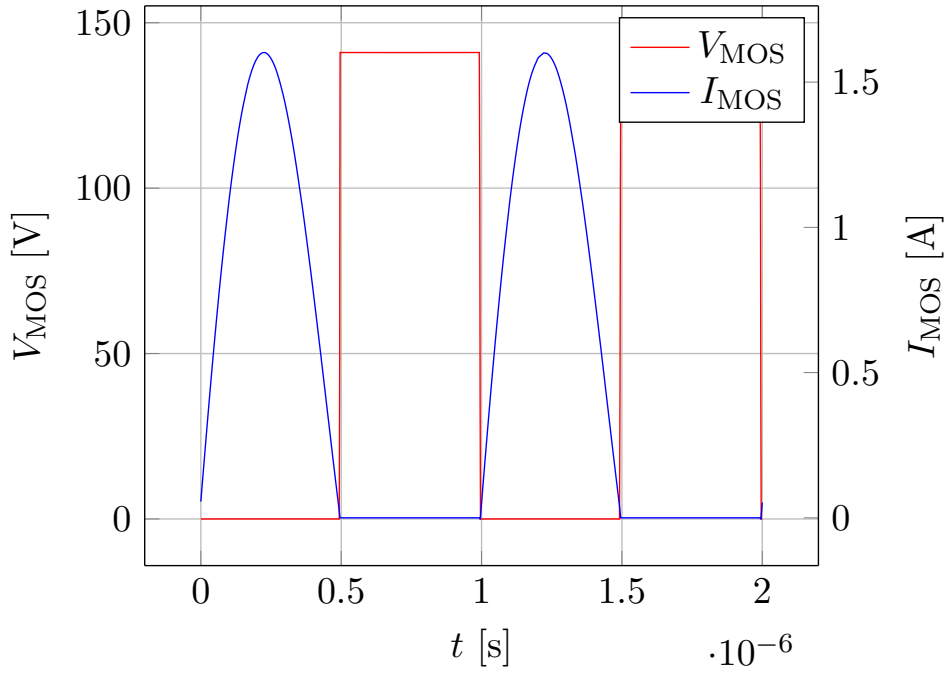

Figure 2.9: Soft switching current and voltage waveforms

2.3.1 Resonance condition

Before starting the ZPA analysis, the resonance condition must be introduced. It has been stated that the compensation network of Figure 2.7 is a resonant circuit, but the resonance condition has not yet been explained. For this analysis, the same condition as in [11] will be considered, which establishes that there is resonance between C_2 and the parallel combination of the L_1 and L_2 inductors, at the working frequency. This can be expressed mathematically as follows:

$$\omega = \frac{1}{\sqrt{C_2 L_{\text{comb}}}} \tag{2.10}$$

where ω is the angular working frequency and L_{comb} is the parallel combination of the inductors:

$$\omega = 2\pi f \tag{2.11}$$

$$L_{\text{comb}} = \frac{L_1 L_2}{L_1 + L_2} \tag{2.12}$$

2.3.2 Input reactance cancellation

As explained in Section 2.3, a necessary condition to achieve ZPA operation is that the compensation network input impedance, Z_{in}, is purely resistive. Therefore, its imaginary part (or reactance) must be zero. By doing a standard AC analysis on the linear circuit of Figure 2.7 (presented in Appendix A), its input reactance is found to be:

$$X_{\text{in}} = \frac{R_e^2 \dfrac{\omega L_1^2}{L_1 + L_2}}{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1 + L_2}\right)^2} - \frac{1}{\omega C_1} \tag{2.13}$$

This expression is formulated to make it evident that the capacitance of the capacitive interface, C_1, can be used to cancel the input reactance. Forcing $X_{\text{in}} = 0$, and solving for C_1, this compensation capacitor is calculated as:

$$C_1 = \frac{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1 + L_2}\right)^2}{R_e^2 \dfrac{(\omega L_1)^2}{L_1 + L_2}} \tag{2.14}$$

This equation shows that with proper inductor and capacitor selection, the LCL CPT system can achieve ZPA operation at a certain load condition R_e. It has to be noted that C_2 does not appear in equation (2.14) because it is not a degree of freedom. In fact, it is designed to make the system resonant at the working frequency, according to (2.10).

2.3.3 Load dependent ZPA

As can be seen from (2.14), the necessary C_1 to make X_{in} equal to zero is dependent on R_e. This means that the proposed design only provides input reactance cancellation for a specific load condition, i.e. ZPA operation is load dependent. The effect caused by this load dependence is shown in Figure 2.10, where the current through a transistor of the inverter is plotted under four different load conditions.

It is seen that only for a specific load (in this particular example the blue curve, for $R_e = 8\,\Omega$), ZPA condition is achieved. This means that for any load different than the calculated one, there will not be zero current during commutations, which will cause high power loss at the inverter, and consequently reduction on the system efficiency.

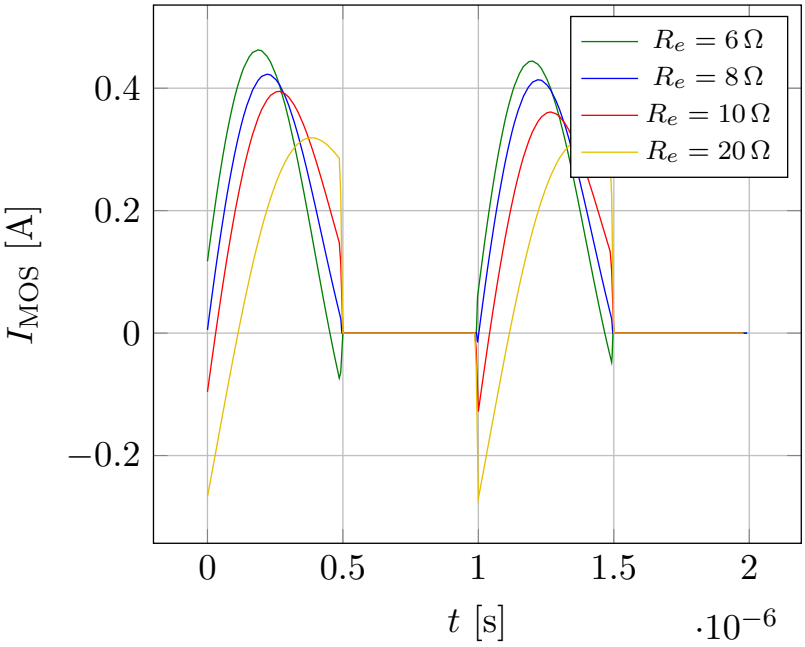

Figure 2.10: Transistor current under load dependent ZPA condition

This undesirable effect is caused by the load dependence of the input reactance. Figure 2.11 shows the phase of the input impedance as a function of frequency for different load conditions. It is observed that at the working frequency (in this case $f = 1\,\text{MHz}$), only the blue curve has zero input reactance and consequently only for that load ($R_e = 8\,\Omega$), ZPA operation is achieved.

To obtain ZPA at any given load, either the switching frequency or the compensation capacitor C_1 would need to be dynamically modified. Since it is desired to avoid the dynamic tuning complexity, a design methodology is proposed in which ZPA operation is maintained irrespective of load variation, just by proper design of the passive components.

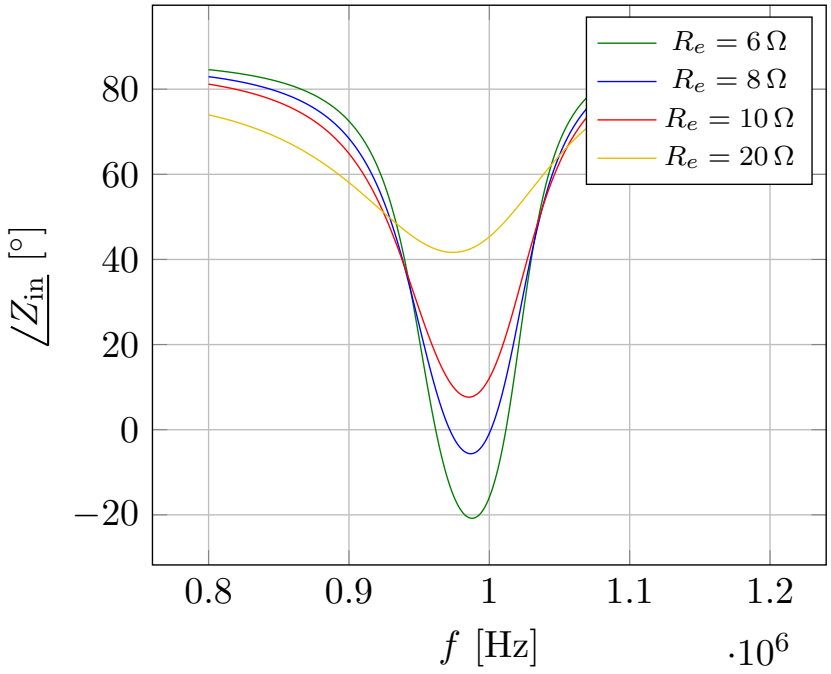

Figure 2.11: Phase angle under load dependent ZPA condition

2.3.4 Load independent ZPA

To obtain ZPA operation for all loads, a design methodology is proposed. The goal of this design is to make the compensation capacitor C_1, calculated by (2.14), independent on the equivalent load R_e. If this is accomplished, then load independent ZPA is obtained. Carefully looking at that equation, it is possible to realize that if the following condition holds:

$$R_e^2 >> \left(\frac{\omega L_2^2}{L_1 + L_2}\right)^2 \tag{2.15}$$

then, neglecting the much lower term in the numerator of (2.14), the R_e^2 factor can be simplified from the numerator and the denominator. Applying this simplification, the compensation capacitor can now be calculated as:

$$C_1 = \frac{L_1 + L_2}{(\omega L_1)^2} \tag{2.16}$$

which **is independent on the load.**

In this thesis, a term will be considered to be "much greater" than another if it is at least ten times higher. Therefore, condition (2.15) is assumed to be satisfied if:

$$R_e^2 \geq 10 \left(\frac{\omega L_2^2}{L_1 + L_2}\right)^2 \tag{2.17}$$

If this condition holds, then ZPA operation will be insensitive to load variations.

Figure 2.12 shows the current through a transistor under load independent ZPA condition, for different loads. It is seen that in this case, soft switching is achieved for all loads, which guarantees minimization of the switching losses for all working conditions. Taking a look at the phase of the input impedance as a function of frequency, shown in Figure 2.13, it is verified that at the working frequency of $f = 1\,\text{MHz}$, the reactance is zero for all loads.

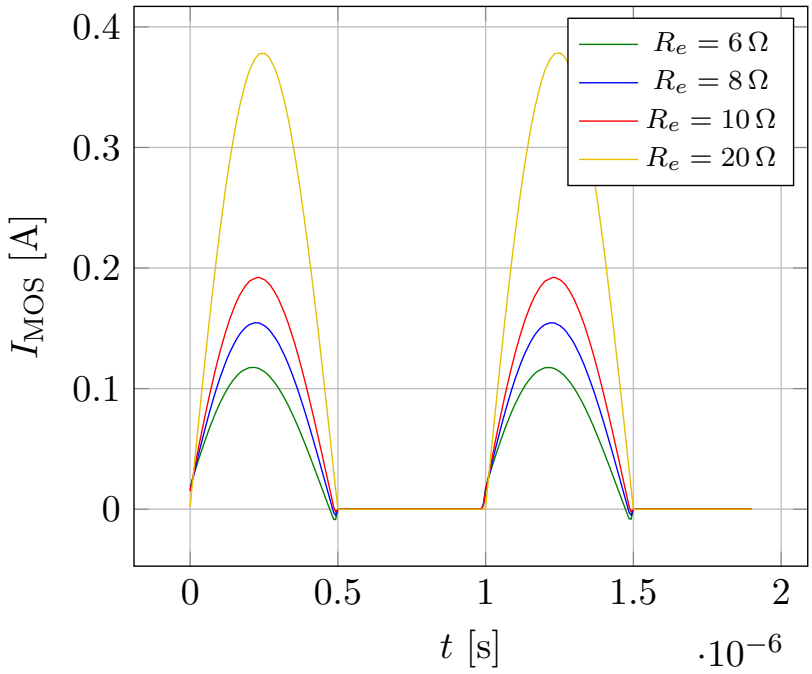

Figure 2.12: Transistor current under load independent ZPA condition

2.3.5 Minimum load

Analizing condition (2.17), it is observed it is more easily satisfied for larger loads. On the other hand, for lower loads the opposite happens. In fact, for a given L_1 and L_2, there exists a minimum load for which that condition is no longer satisfied. The minimum load for which the condition is still valid, is when the term on the left is exactly ten times higher than the term on the right:

$$R_{\text{e,min}}^2 = 10 \left(\frac{\omega L_2^2}{L_1 + L_2} \right)^2 \tag{2.18}$$

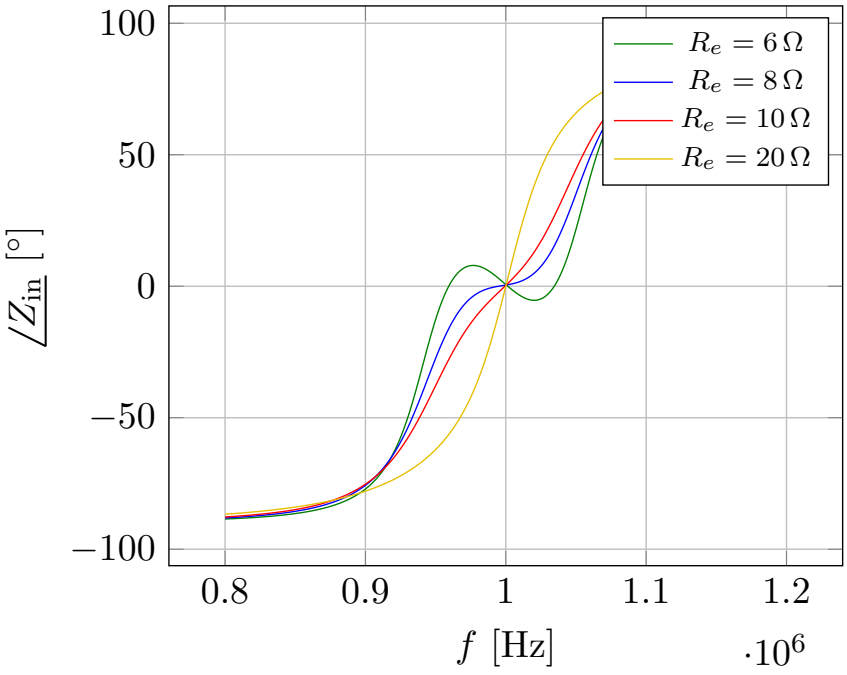

Figure 2.13: Phase angle under load independent ZPA condition

Solving for $R_{\text{e,min}}$, the minimum equivalent load for which load independent ZPA is guaranteed is calculated to be:

$$R_{\text{e,min}} = \sqrt{10}\frac{\omega L_2^2}{L_1 + L_2} \tag{2.19}$$

Using equation (2.8), the equivalent load R_e can be replaced by the output load R_L, giving the minimum load expressed below.

$$R_{\text{L,min}} = \frac{\pi^2\sqrt{10}}{8}\frac{\omega L_2^2}{L_1 + L_2} \tag{2.20}$$

The design procedure will take into account this detail, and will guarantee independent load ZPA operation for loads as low as $R_{\text{L,min}}$. In order to design the system, the minimum expected load is provided in the specifications (Section 3.1).

Now that ZPA operation has been studied in detail, the circuit of Figure 2.7 can be analyzed. This analysis will be made taking into consideration the resonance condition of (2.10) and the load independent ZPA condition, expressed in (2.17).

2.4 Circuit analysis

In this section, the equations that rule the CPT system with LCL compensator will be presented. The analysis will begin with the simplified linear circuit of Figure 2.7, and will then proceed with the complete system that includes the inverter and rectifier of Figure 2.4. The results obtained based on these equations will be validated in Section 3.3, where simulations results using software LTspice are presented.

2.4.1 Simplified circuit analysis

The simplified equivalent circuit of Figure 2.7 is, for clarity, shown again below. This is a simple linear circuit, which can be studied using standard AC analysis. The mathematical derivations are made in Appendix B, and here only the general procedure and final results are shown.

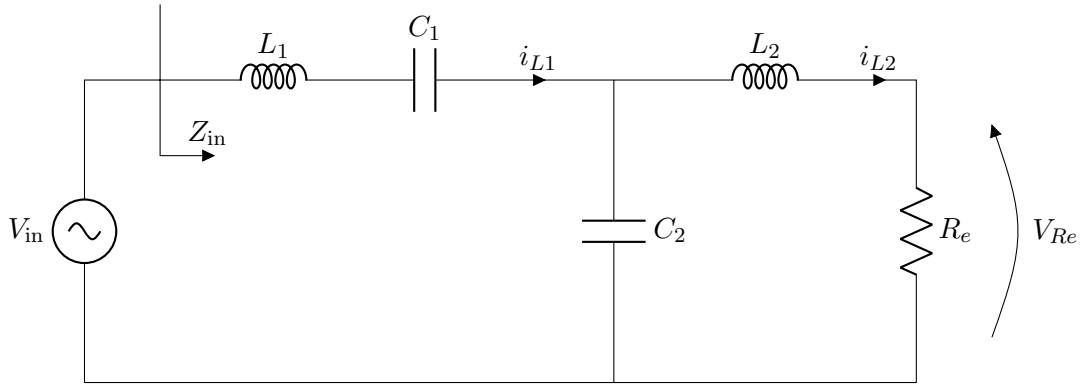

Figure 2.14: Simplified LCL compensation circuit

In order to obtain quantities such as currents and voltages, first the input impedance must be calculated. This impedance, Z_{in}, is expressed in cartesian form as follows:

$$Z_{\text{in}} = R_{\text{in}} + jX_{\text{in}} \tag{2.21}$$

According to what was explained in Section 2.3.2, if the compensation capacitor C_1 is calculated to achieve ZPA (as expressed in (2.14)), then the input reactance is zero. Consequently, the input impedance is purely resistive and can be calculated as follows (according to Appendix B):

$$Z_{\text{in}} = \frac{(\omega L_{\text{comb}})^2}{R_e} \tag{2.22}$$

Since this system is studied under the first harmonic approximation, all current and voltage waveforms are considered to be sinusoids ringing at the resonant frequency. Therefore, the circuit analysis can be done using current and voltage phasors. These quantities,

shown below, are verified by simulations in Section 3.3.

$$I_{L1} = V_{\text{in}} \frac{R_e}{(\omega L_{\text{comb}})^2} \tag{2.23}$$

$$I_{L2} = V_{\text{in}} \frac{1}{\omega L_{\text{comb}}} \tag{2.24}$$

$$V_{Re} = V_{\text{in}} \frac{R_e}{\omega L_{\text{comb}}} \tag{2.25}$$

As can be seen in (2.24), the current through L_2, which is the unrectified output current, is **independent of the load**. This means that under the ZPA and resonance conditions considered, this CPT system behaves as an **ideal current source.** This fact will be studied with more details when analyzing the frequency behaviour on Section 3.4.

Equations (2.23) to (2.25) are useful to understand the circuit operation, but do not provide a complete picture since they are not expressed as a function of the output parameters V_{DC} and R_L. To get rid of the intermediate quantities V_{in} and R_e, the complete circuit has to be analized.

2.4.2 Complete circuit analysis

To study the system including the inverter and rectifier, the circuit of Figure 2.4 is shown below for clarity. This non linear system will be studied starting from its simplified analysis (made on the previous section), and considering the simplifications on the non linear blocks explained in Section 2.2.

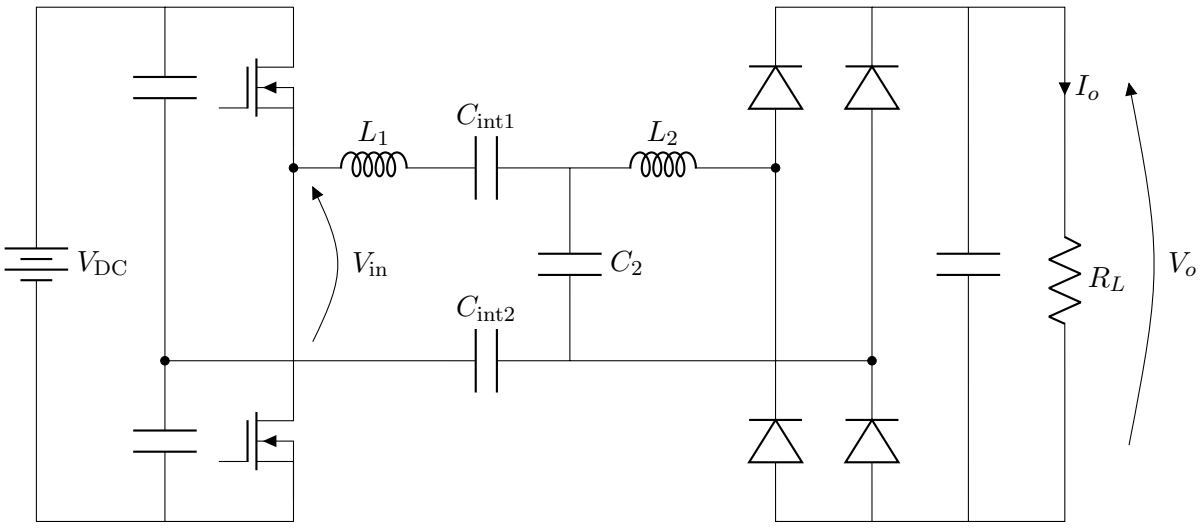

Figure 2.15: Complete circuit

To obtain equations (2.23) to (2.25) as a function of V_{DC} and R_L, instead of V_{in} and R_e, the following relationships (developed in Section 2.2) are considered:

$$V_{\text{in}} = \frac{2}{\pi} V_{\text{DC}} \tag{2.26}$$

$$R_e = \frac{8}{\pi^2} R_L \tag{2.27}$$

Using these relationships, now the circuit quantities can be expressed as shown below.

$$I_{L1} = \frac{16 V_{\text{DC}}}{\pi^3} \frac{R_L}{(\omega L_{\text{comb}})^2} \tag{2.28}$$

$$I_{L2} = \frac{2 V_{\text{DC}}}{\pi} \frac{1}{\omega L_{\text{comb}}} \tag{2.29}$$

Since the system under study is an ideal current source, it is important to express the output current as a function of circuit parameters. Applying (2.5) to (2.29), the rectified output current is expressed below.

$$I_o = \frac{4 V_{\text{DC}}}{\pi^2} \frac{1}{\omega L_{\text{comb}}} \tag{2.30}$$

The output voltage V_o is obtained by multiplying this current with the load:

$$V_o = \frac{4 V_{\text{DC}}}{\pi^2} \frac{R_L}{\omega L_{\text{comb}}} \tag{2.31}$$

Finally, the output power is calculated as the product between I_o and V_o:

$$P_o = \frac{16 V_{\text{DC}}^2}{\pi^4} \frac{R_L}{(\omega L_{\text{comb}})^2} \tag{2.32}$$

2.4.3 Equation summary

To conclude this chapter, a table that summarizes the most important results is presented. These equations will be used when designing the system, which will be the topic of Chapter 3.

Quantity	**Equation**	**Description**
$R_{\mathrm{L,min}}$	$\frac{\pi^2\sqrt{10}}{8}\frac{\omega L_2^2}{L_1+L_2}$	minimum load for ZPA operation
C_1	$\frac{L_1+L_2}{(\omega L_1)^2}$	compensation capacitor
C_2	$\frac{1}{\omega^2 L_{\mathrm{comb}}}$	resonance capacitor
I_{L1}	$\frac{16V_{\mathrm{DC}}}{\pi^3}\frac{R_L}{(\omega L_{\mathrm{comb}})^2}$	current through L_1
I_{L2}	$\frac{2V_{\mathrm{DC}}}{\pi}\frac{1}{\omega L_{\mathrm{comb}}}$	current through L_2
I_o	$\frac{4V_{\mathrm{DC}}}{\pi^2}\frac{1}{\omega L_{\mathrm{comb}}}$	load independent output current
V_o	$\frac{4V_{\mathrm{DC}}}{\pi^2}\frac{R_L}{\omega L_{\mathrm{comb}}}$	output voltage
P_o	$\frac{16V_{\mathrm{DC}}^2}{\pi^4}\frac{R_L}{(\omega L_{\mathrm{comb}})^2}$	output power

Table 2.1: Equation summary

Chapter 3

System design

The objective of this chapter is to establish a design procedure to calculate the passive components of the CPT system, according to some specifications. Then, circuit simulations using software LTspice will be performed. These simulations will allow to verify the theoretical analysis of Chapter 2 and to study the frequency behaviour of the system.

3.1 Input specifications

To be able to design the system, a list of specifications must be provided. These specifications often consist on input data (like input voltage and working frequency) and output requirements (like output power/voltage).

For the present design, the specifications proposed in Table 3.1 will be considered. The rectified voltage of the electric grid is taken as the input voltage, and the system is expected to deliver 40 W of power at a nominal load of 10 Ω.

Since the CPT system with LCL compensator is a current source, it makes sense to express the output requirements in terms of current rather than power. To do this, the relationship between power delivered to a resistive load and its current is exploited:

$$I_o = \sqrt{\frac{P_o}{R_L}} \tag{3.1}$$

Applying this equation, the required output current is found to be:

$$I_o = 2\,\mathrm{A} \tag{3.2}$$

As mentioned in Section 2.3.5, it is necessary to provide information about the minimum expected load, since the system will only guarantee ZPA operation up to this $R_{\mathrm{L,min}}$.

Parameter	Value	Description
V_{DC}	310 V	the input voltage is the rectified voltage of the electric grid
f	1 MHz	working frequency
P_o	40 W	output power
R_L	10 Ω	nominal load
$R_{\mathrm{L,min}}$	5 Ω	minimum load

Table 3.1: Specifications

3.2 Design procedure

The objective of this section is to develop a design procedure in order to easily calculate the values of the inductors and capacitors of the compensation network. These components will be calculated according to the specifications proposed in Table 3.1, and the goal is to make the CPT system of Figure 2.4 achieve the following:

- Deliver the expected output current I_o,
- Provide ZPA operation for loads as low as the minimum expected $R_{\mathrm{L,min}}$, and
- Resonate at the working frequency f.

The LCL CPT system is shown on Figure 3.1, where in this case C_1 is the equivalent capacitance of the capacitive interface, expressed in (2.9).

The design procedure will be developed considering a simplified version of the equations that rule the system behaviour, grouped together on Table 2.1. From that table, it can be observed that once the L_1 and L_2 inductors are fixed, the two capacitors are also fixed. This means that neither of the two capacitors is a degree of freedom. In fact, they are used to accomplish the following tasks:

- C_1: Used to cancel the input reactance, providing ZPA operation.
- C_2: Used to make the system resonate at the working frequency.

Therefore, L_1 and L_2 remain as the only degrees of freedom of the system. The equations to find their values will be developed next.

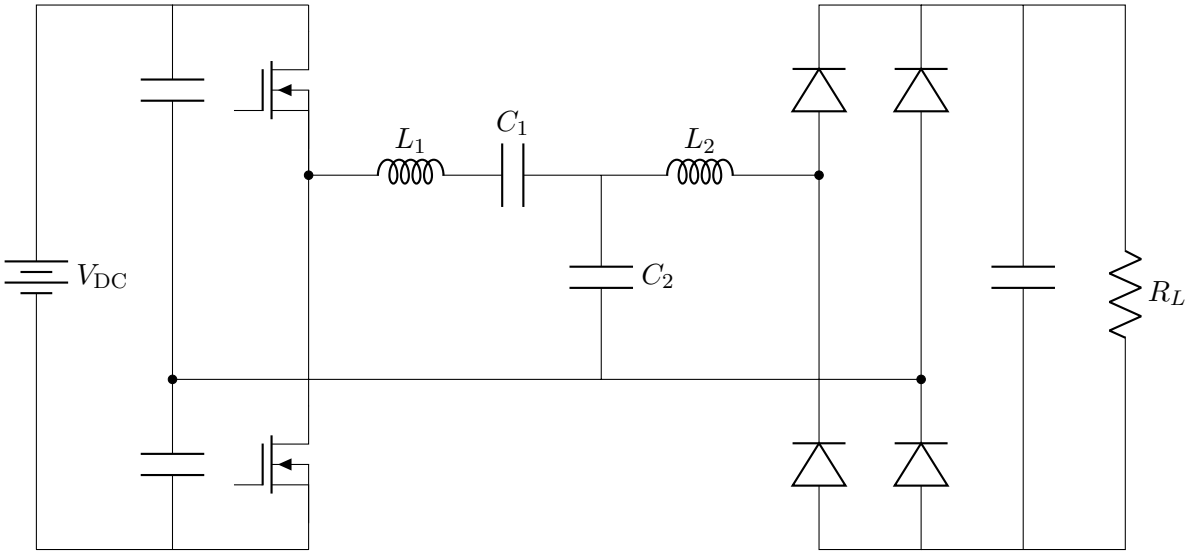

Figure 3.1: CPT system with LCL compensator

3.2.1 Simplification of circuit equations

In order to obtain simple equations for the inductor calculations, the following approximation is considered: L_1 *is assumed to be much bigger than* L_2. According to Section 2.3.4, this condition will be considered to be true if L_1 is at least ten times bigger than L_2:

$$L_1 >> L_2 \tag{3.3}$$

$$L_1 \geq 10L_2 \tag{3.4}$$

If this condition holds, then the parallel combination of these two inductors (which clearly depends on the value of both components), can be approximated to be just the smaller one. This is deduced by neglecting the much smaller term in the denominator of the parallel inductor configuration, as shown below.

$$L_{\mathrm{comb}} = \frac{L_1 L_2}{L_1 + L_2} \tag{3.5}$$

$$L_{\mathrm{comb}} \approx L_2 \tag{3.6}$$

Equation (2.30) is used to calculate the output current. It can be seen that it depends on the parallel combination of the inductors L_{comb}, which under the (3.6) approximation is assumed to be just L_2. This allows the output current to be just dependent on that inductor, obtaining the following approximated expression:

$$I_o = \frac{4}{\pi^2}\frac{V_{\mathrm{DC}}}{\omega L_2} \tag{3.7}$$

Another equation that will be simplified is Equation (2.20), which expresses the minimum load for which ZPA operation is guaranteed. Neglecting the much smaller L_2 in its denominator, the following expression for calculating the minimum load is obtained:

$$R_{\mathrm{L,min}} = \frac{\pi^2\sqrt{10}}{8}\frac{\omega L_2^2}{L_1} \tag{3.8}$$

It should be emphasized that these simplified equations are only valid if L_1 is at least ten times bigger than L_2. In the case that the calculated values of L_1 and L_2 do not meet this condition, then L_1 will be increased until a point where it is satisfied (in other words, until $L_1 = 10L_2$). This will be explained in detail in Chapter 5.

3.2.2 Design steps

All the equations necessary to calculate the passive components have been developed. Next, a design procedure is presented in which these equations have been ordered, to be able to design the compensation circuit in a series of simple steps.

1. *Calculate L_2 to obtain the required output current*:

   Solving (3.7) for L_2, the necessary inductance to provide the expected output current is shown below.

   $$L_2 = \frac{4}{\pi^2}\frac{V_{\mathrm{DC}}}{\omega I_o} \tag{3.9}$$

2. *Calculate L_1 to guarantee ZPA condition until $R_{\mathrm{L,min}}$*:

   Solving (3.8) for L_1, the following is obtained:

   $$L_1 = \frac{\pi^2\sqrt{10}}{8}\frac{\omega L_2^2}{R_{\mathrm{L,min}}} \tag{3.10}$$

3. *Calculate C_1 to compensate the input reactance*:

   The compensation capacitor is calculated by equation (2.16):

   $$C_1 = \frac{L_1 + L_2}{(\omega L_1)^2} \tag{3.11}$$

4. *Calculate C_2 to make the system resonate at the working frequency*:

   Applying the resonance condition (2.10),

   $$C_2 = \frac{1}{\omega^2 L_{\mathrm{comb}}} \tag{3.12}$$

3.2.3 Component calculation

Applying these design steps to the specifications proposed in Table 3.1, the passive components of Figure 3.1 can be calculated. Their values are shown in Table 3.2.

Component	Value
L_1	490 µH
L_2	10 µH
C_1	53 pF
C_2	2.54 nF

Table 3.2: Passive component values

Since C_1 is not an actual component but the equivalent capacitance of two series capacitors C_{int1} and C_{int2}, the values of the actual interface capacitors must be calculated. Assuming that these two components are equal, and applying (2.9), it is found that:

$$C_{\text{int1}} = C_{\text{int2}} = 106\,\text{pF} \tag{3.13}$$

To verify the theoretical results, simulations using software LTspice will be performed. The results of these simulations are presented in the following section.

3.3 Simulations

The circuit to be simulated is shown in Figure 3.2. All components (inductors, capacitors, transistors and diodes) are assumed to be ideal.

To verify the theoretical analysis of Chapter 2, the circuit quantities (such as currents and voltages) calculated using equations of Table 2.1, will be compared with the simulated ones. This comparison is shown on Table 3.3, and it is observed that the calculated values match the simulated ones with good accuracy. In fact, the calculated quantities are within less than 4% of the simulated ones. This verifies the theoretical derivations, even with the approximation considered on Section 3.2.1.

For the approximated equations developed in Section 3.2.1 to be valid, L_1 needs to be at least ten times greater than L_2. With the calculated components this condition is met. In fact, for this design:

$$L_1 = 49L_2 \tag{3.14}$$

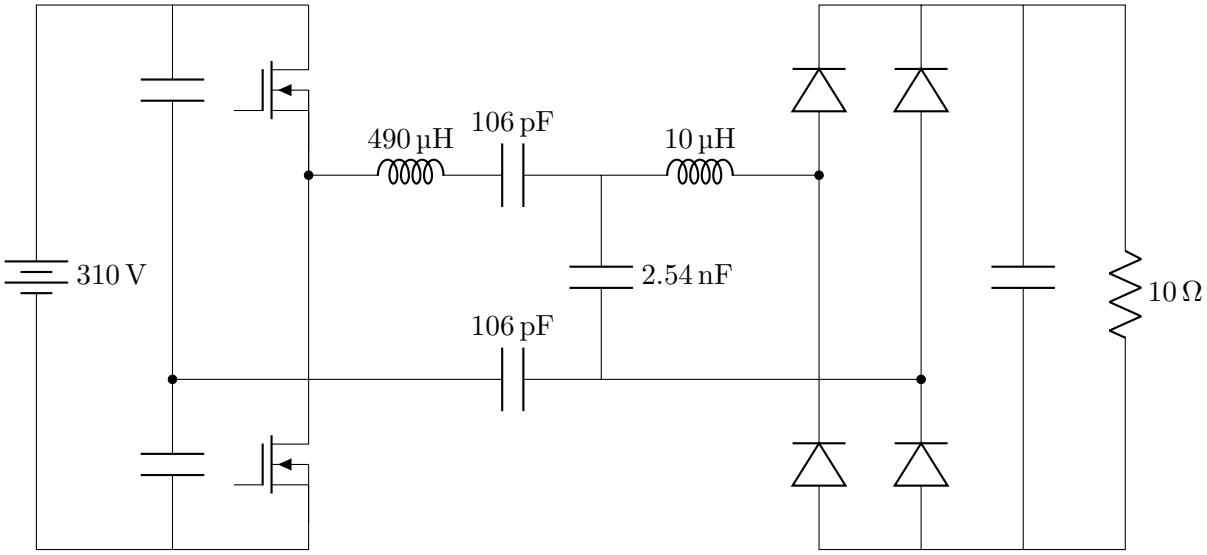

Figure 3.2: CPT system with component values

Quantity	Calculated	Simulated
I_o	2.04 A	2 A
I_{L1}	0.42 A	0.44 A
I_{L2}	3.2 A	3.19 A
V_o	20.4 V	20 V
P_o	41.6 W	40 W

Table 3.3: Calculation vs Simulation at nominal load

3.3.1 ZPA operation

As explained in Section 2.3, ZPA operation is a very important condition that allows, among other things, to improve the system efficiency. Since the design procedure was developed to guarantee ZPA operation for loads as low as $R_{\mathrm{L,min}}$, it is important to check whether this condition is met or not.

To verify this operation, the current through a MOSFET under different load conditions is shown on Figure 3.3. For large loads (red and yellow curves), almost zero current is present during commutations, which means that the system works under ZPA operation for those loads. On the other hand, for lower loads (green and blue curves) there is a somewhat significant current at commutations. This is not surprising, since it was demonstrated mathematically that ZPA operation is more easily satisfied for larger loads in Section 2.3.5.

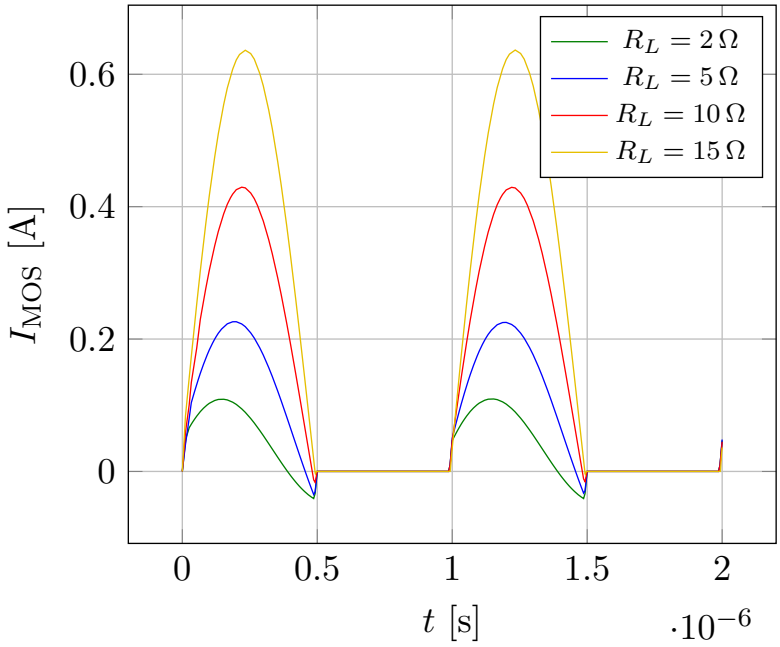

Figure 3.3: Transistor current under different loads

By looking at Figure 3.3, it can be seen that the peak current during the conduction state increases with load increments. This rise, along with the reduction in the instantaneous current during commutations, causes the relative effect of switching losses to be negligible for large loads.

To understand this last statement, it is necessary to introduce the various causes of dissipation in power MOSFETs. This topic will be discussed in detail in Section 4.2.3, when analyzing MOSFET losses. At this point, the two main causes of power loss in these transistors are briefly explained:

- Conduction loss: It is caused by the power dissipation on the intrinsic parasitic resistance of the device. It depends on the RMS current flowing through it, and therefore on the peak current during the conduction period.

- Switching loss: It is caused by the non-immediate commutation between on and off states, which produces a simultaneous presence of current and voltage across the device, and consequently power dissipation. It depends on the instantaneous current (and voltage) at commutations.

To obtain a more clear visualization of the instantaneous current at the switching time, a zoomed-in plot of Figure 3.3 is provided on Figure 3.4. From this graph, the exact values of the current at the on-off transition, for different load conditions, can be extracted. These values are used to quantitatively analyze the system behaviour.

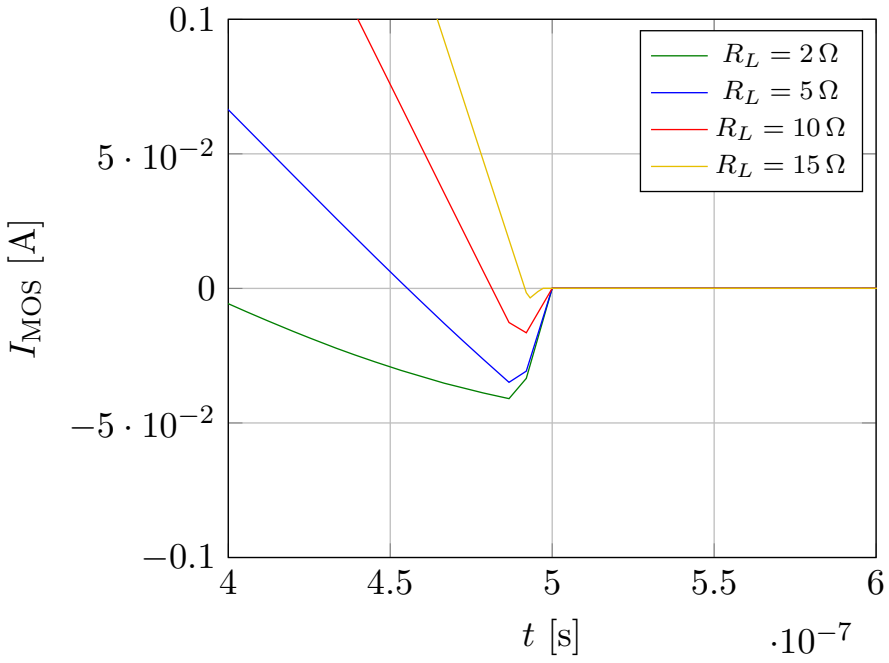

Figure 3.4: Zoomed-in current during on-off transition

In Table 3.4, a quantitave analysis of this discussion is presented. It shows the peak current during the on state, I_{peak}, the instantaneous current at commutations, I_{comm}, and the ratio between these two values; for different load conditions.

According to this table, for increasing loads there is a reduction in the ratio of I_{comm} vs I_{peak}, which means that the relative importance of the switching loss decreases, until a point where it is negligible. For the minimum expected load of $5\,\Omega$ the ratio is around 13%, while for $10\,\Omega$ load, this value goes down to 3%.

This analysis verifies that the system can be assumed to work under ZPA operation for loads greater than $5\,\Omega$. Therefore, switching loss is almost zero and the system efficiency is significantly improved.

R_L	I_{peak}	I_{comm}	**Ratio**
$2\,\Omega$	113 mA	42 mA	37%
$5\,\Omega$	223 mA	29 mA	13%
$10\,\Omega$	430 mA	13 mA	3%
$15\,\Omega$	635 mA	5 mA	<1%

Table 3.4: Current comparison for different loads

3.3.2 Considerations

- According to Equation (3.10), it can be observed that the current through the L_1 inductor increases linearly with load increments. This behaviour will produce a practical limitation on the maximum allowable load, since only up to a certain maximum current can flow through a real inductor. This limitation and its consequences will be studied in Chapter 5.

- Another important detail is related to the voltage stress of the components. Due to the high input voltage ($V_{\mathrm{DC}} = 310\,\mathrm{V}$), very high voltages appear across the passive components of the compensation circuit, which are reported in Table 3.5. In order to reduce these very high voltage stresses, the input voltage has to be reduced. The results of this modification will also be analyzed in Chapter 5.

Component	**Voltage stress**
L_1	1.3 kV
L_2	200 V
$C_{\mathrm{int1}}, C_{\mathrm{int2}}$	650 V
C_2	200 V

Table 3.5: Voltage stresses of passive components

3.4 Frequency behaviour

In this section, the frequency characteristics of the system will be analized, using software LTspice. To perform this analysis, the designed circuit of Figure 3.2 will be considered. Since this network has many reactive components, it has many resonances, i.e. it is a multiresonant circuit. The objective of this analysis is to study the output characteristics of each resonance point [20], [21].

In battery charging applications, load independent Constant Current (CC) and Constant Voltage (CV) output characteristics are necessary. This is because over the full range of the battery charge, the battery pack equivalent resistance varies in a wide range, and CC/CV charging profiles are desirable to ensure safety, durability, and performance of the battery [22].

On the other hand, as explained in Section 2.3, ZPA operation can minimize the apparent power required and enhance the power transfer capability. Besides, it makes it possible to achieve ZCS on the MOSFETs of the inverter, improving the system efficiency. Therefore, both CC and CV output characteristics with input ZPA are desirable for battery charging applications.

Since the resonances only depend on the passive components of the compensation circuit, instead of the complete circuit of Figure 3.2, a simplified version will be considered for the simulations. This equivalent circuit is made considering the simplifications explained in Section 2.2 and summarized below.

- Inverter: Approximated as a sine wave generator.
- Rectifier: Represented with its equivalent resitance R_e.
- Capacitive interface: Just considering its equivalent capacitance C_1.

Using these simplifications, the circuit of Figure 3.2 is transformed into the one of Figure 3.5. The following analysis will consist on the study of the resonance points of this circuit, to learn at which frequencies it works under CC or CV modes of operation. Besides, the simulation will allow to verify if ZPA condition is achieved at these resonance frequencies.

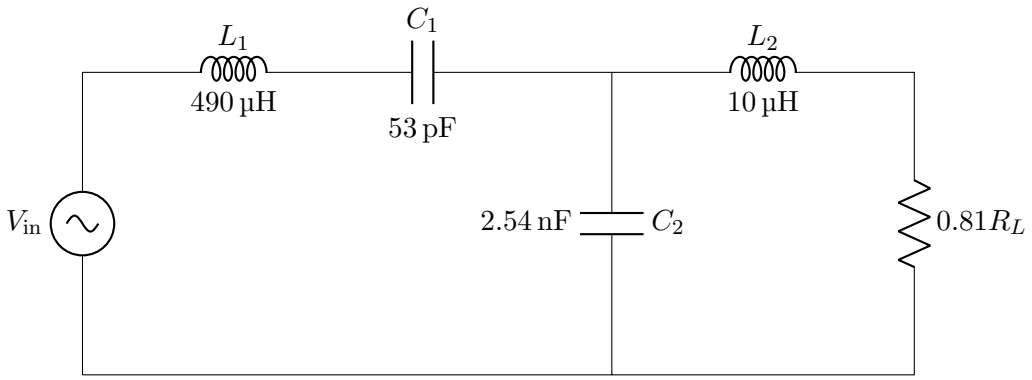

Figure 3.5: Equivalent circuit with component values

3.4.1 Constant current

To analize the output characteristics of the circuit of Figure 3.5 in terms of current, the output current is plotted as a function of frequency, for different load conditions. The simulation results of the output current are shown on Figure 3.6.

It is observed that there is a point in which all the curves have the same value. This is the constant current frequency, since the output current is always at the same value, independent on the load. This point is found to be at $f = 1\,\text{MHz}$ which, according to Table 3.1, is the working frequency. This means that the designed system works as a current source, a conclusion already drawn in Section 2.4.1.

The resonance condition under which the system works under CC mode of operation, is consequently the same as the one explained in Section 2.3.1. To recall, this behaviour

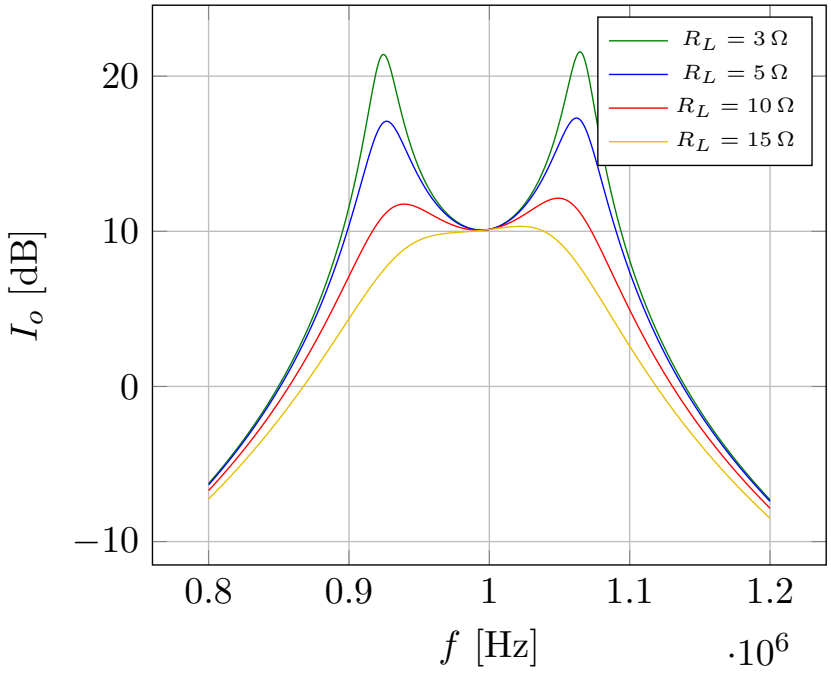

Figure 3.6: Output current as a function of frequency for different loads

occurs at the frequency in which the C_2 capacitor resonates with the parallel combination of the L_1 and L_2 inductors. This condition is expressed mathematically as follows:

$$\omega = \frac{1}{\sqrt{L_{\text{comb}} C_2}} \tag{3.15}$$

where L_{comb} is the parallel combination of the inductors:

$$L_{\text{comb}} = \frac{L_1 L_2}{L_1 + L_2} \tag{3.16}$$

3.4.2 Constant voltage

To analize the output characteristics in terms of voltage, now the output voltage of Figure 3.5 is plotted as a function of frequency, for different load conditions. These results are shown on Figure 3.7.

In this case, it can be seen that there are two points at which all the curves have the same value. This means that there are two frequencies where the output voltage is independent on the load, i.e, there are two frequency points at which the system behaves as an ideal voltage source. These frequencies, according to Figure 3.7, are approximately $f_{CV,1} = 0.92\,\text{MHz}$ and $f_{CV,2} = 1.07\,\text{MHz}$.

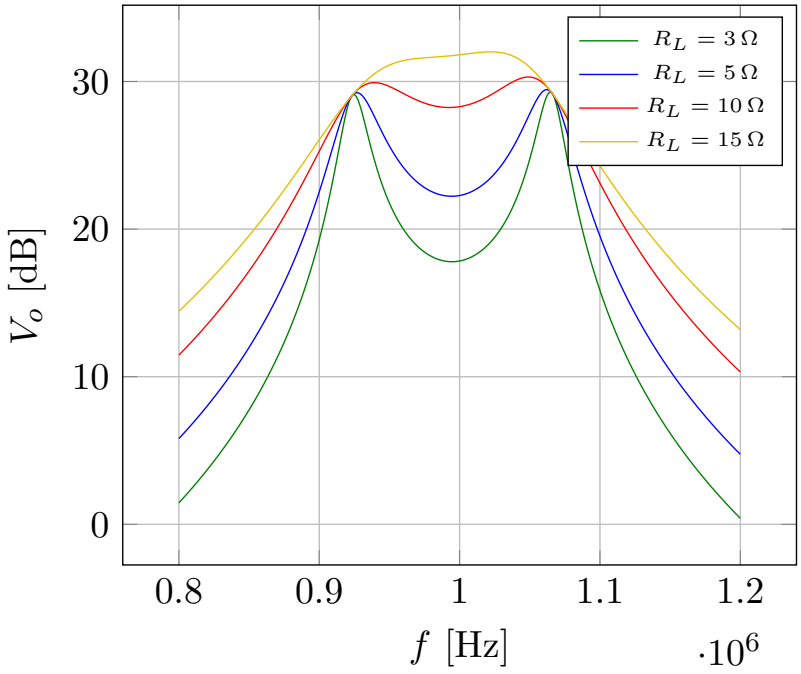

Figure 3.7: Output voltage as a function of frequency for different loads

To explain the resonance condition under which the system behaves as a voltage source, the L_1 inductor is divided into two series inductors, as shown in Figure 3.8. This is done to graphically indicate that a "part" of L_1 (indicated as L_{1a}) resonates with C_1, and the rest of it (L_{1b}) resonates with L_2 and C_2. In fact, CV mode of operation occurs when there is a simultaneous resonance between:

- L_{1a} and C_1, expressed mathematically as:

$$\omega_1 = \frac{1}{\sqrt{L_{1a}C_1}} \tag{3.17}$$

- and C_2 with the parallel combination of L_{1b} and L_2, expressed as:

$$\omega_2 = \frac{1}{\sqrt{(L_{1b} \parallel L_2)C_2}} \tag{3.18}$$

These two resonances coincide if ω_1 is equal to ω_2:

$$\omega_1 = \omega_2 \tag{3.19}$$

$$\frac{1}{\sqrt{L_{1a}C_1}} = \frac{1}{\sqrt{(L_{1b} \parallel L_2)C_2}} \tag{3.20}$$

Knowing that $L_1 = L_{1a} + L_{1b}$, and solving the previous expression for L_{1a}, the following equation can be found:

$$L_{1a}^2 - L_{1a}\left(L_1 + L_2\left(1 + \frac{C_2}{C_1}\right)\right) + L_1 L_2 \frac{C_2}{C_1} = 0 \tag{3.21}$$

This quadratic equation means that there are two values of L_{1a} for which (3.20) is satisfied. Therefore, there must be two constant voltage frequencies, which is consistent with what is observed in Figure 3.7.

Solving the quadratic equation by classical means, the two values of L_{1a} that make the resonances (3.17) and (3.18) happen simultaneously are found:

$$\begin{cases} L_{1a_1} = 420\,\mu\text{H} \\ L_{1a_2} = 560\,\mu\text{H} \end{cases} \tag{3.22}$$

Replacing these values in (3.17), the constant voltage frequencies are calculated to be:

$$\begin{cases} f_{CV,1} = 1.066\,\text{MHz} \\ f_{CV,2} = 0.923\,\text{MHz} \end{cases} \tag{3.23}$$

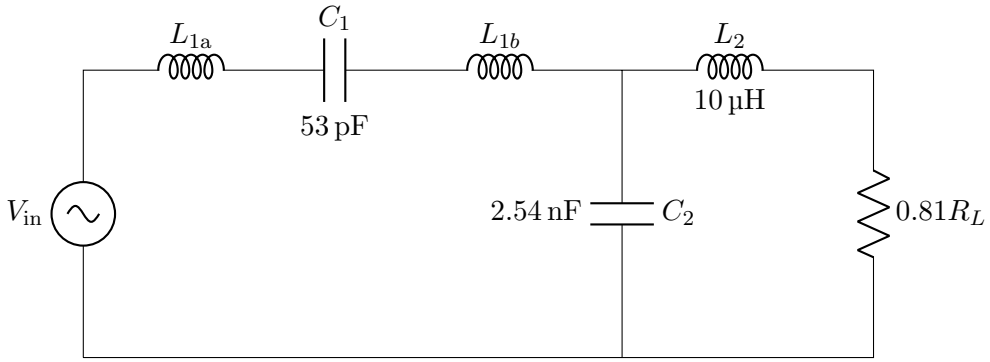

Figure 3.8: Equivalent circuit to illustrate CV points

3.4.3 ZPA

Finally, the phase of the input impedance is plotted in Figure 3.9. The goal is to observe at which points it is zero and consequently ZPA operation is achieved.

It is seen that only at the CC frequency (f =1 MHz), the phase of the input impedance is zero for all load conditions. This means that this topology can only be used as a current source, since the CV outputs do not provide ZPA operation. To obtain a CV output characteristic with ZPA operation, a variable frequency control can be applied [23].

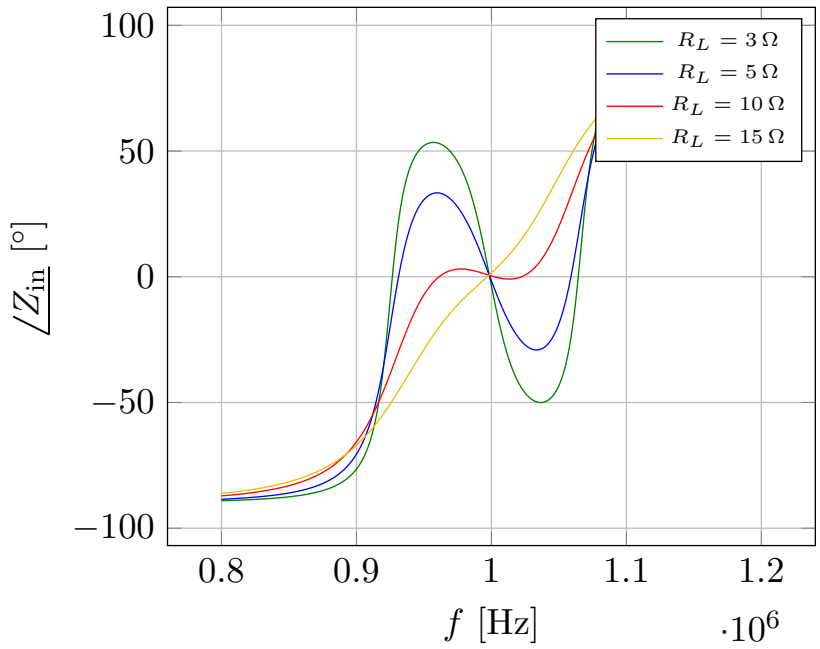

Figure 3.9: Phase of the input impedance as a function of frequency for different loads

Chapter 4

System efficiency

This chapter is devoted to analyzing the system efficiency. To calculate this important measure, first actual components from manufacturers are selected. Then, losses on each one of them are analyzed and the efficiency at nominal load is calculated. Finally, the relationship between efficiency and output quantities (load and output voltage) is expressed mathematically and graphically in the form of efficiency curves.

4.1 Component selection

In order to calculate the system efficiency, losses on every component must be studied and quantified. This means that real inductors, capacitors, MOSFETs and diodes must be selected. Identifying components that meet the requirements of this application is a critical step in the designing of this CPT system, whose overall performance is greatly determined by these choices. The performance characteristics of these components are provided by manufacturers in product datasheets, which will be the most useful resource to predict the component behaviour.

4.1.1 Normalization of passive components

The first step in selecting actual components is to normalize the values of Table 3.2. This is done by repeating the design steps presented in Section 3.2.2, but now normalizing these components at each step:

1. L_2 was calculated to be 10 µH, which is already a normalized value.

2. L_1 needs to be at least 490 µH, which is not a normalized value. In this design, this inductor is normalized to $L_1 = 680\,\mu H$. This increment does not modify system performance; it just provides ZPA operation for lower loads.

3. With this different value of L_1, now C_1 is calculted to be 37.8 pF. According to Section 2.2.3, this capacitor is not an actual component but the series combination of two capacitors:

$$C_{\text{int1}} = C_{\text{int2}} = 75.6\,\text{pF} \tag{4.1}$$

   which are normalized to 75 pF.

4. Again due to the variation of L_1, C_2 is now calculated to be 2.57 nF. Its closest normalized value is 2.7 nF, which due to the narrow band operation of resonant circuits, is way too far. To make this capacitance as close to the calculated one as possible, the proposed solution is to use two series capacitors of 5.1 nF each. In this way, the equivalent capacitance is 2.55 nF, a pretty accurate value.

Component	**Value**
L_1	680 µH
L_2	10 µH
$C_{\text{int1}-2}$	75 pF
C_{2a-b}	5.1 nF

Table 4.1: Normalized passive components

The normalized component values are shown in Table 4.1. Using these components, circuit quantities will be sligthly different than before (reported on Table 3.3). These new quantities, obtained by LTspice simulations of Figure 4.1, are shown on Table 4.2.

Quantity	**Simulated**
I_o	2 A
I_{L1}	0.41 A
I_{L2}	3.15 A
V_o	20 V
P_o	40 W

Table 4.2: Simulation results with normalized components

Now that all passive components are normalized and their working operation in terms of voltage and current are obtained by simulations, it is possible to select real components from manufacturers. For all cases, it is important to remember the following:

- All current and voltage waveforms are sinusoidal (FHA).
- All sinusoids ring at the resonance frequency $f = 1\,\text{MHz}$.

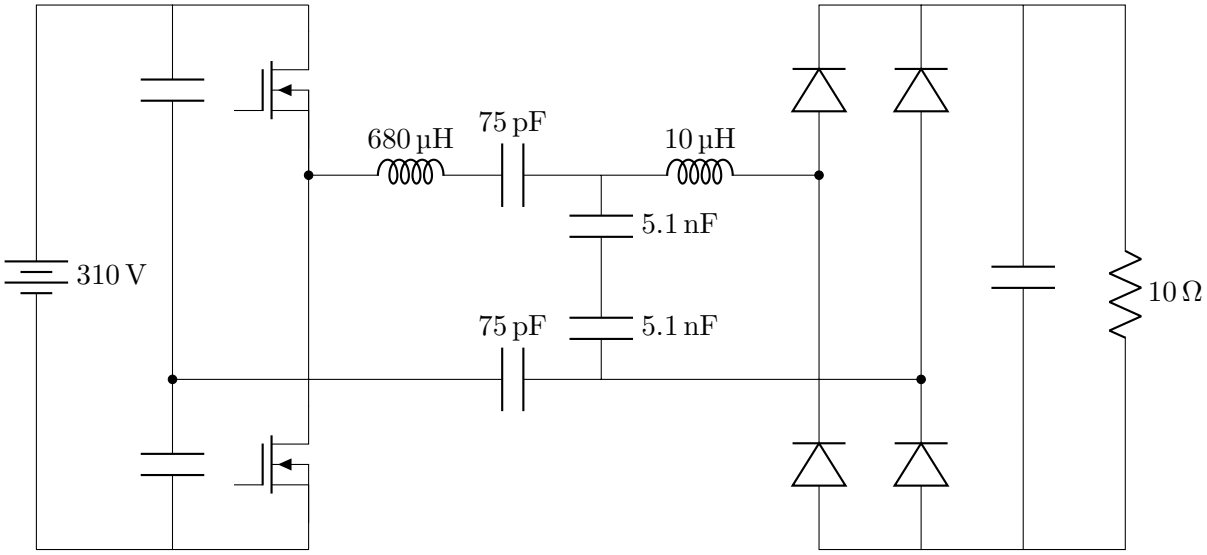

Figure 4.1: CPT system with normalized passive components

4.1.2 Inductor selection

In this thesis, all inductors used are from Coilcraft, specifically from the DO5040H series. This family of inductors is characterized by its high saturation current ratings and low DCR.

Inductor L_1

In Table 4.3, the working condition of L_1 is reported, where I_{L1} and V_{L1} are peak values of sinusoidal waves ringing at the working frequency f. According to these current, voltage and frequency requirements, an appropriate component is selected, whose main characteristics are presented in its datasheet and summarized in Table 4.4.

As can be seen, the component characteristics regarding current ratings and working frequency make the selected part a feasible solution. However, the voltage stress might be too high and damage this inductor. Even though this limitation is not specified in the datasheet, this high voltage might be critical and make the complete system fail. Nevertheless, since the purpose of the present chapter is to study the efficiency, this problem is neglected for now. In chapter 5 this limitation is studied and a way to reduce the voltage stress is proposed.

Parameter	Value
L_1	680 µH
I_{L1}	0.41 A
V_{L1}	1.75 kV
f	1 MHz

Table 4.3: Working conditions of L_1

Parameter	Value
P/N	D05040H-684
I_{sat}	2 A
I_{rms}	1.1 A
SRF	1.6 MHz

Table 4.4: Part characteristics

Inductor L_2

The current and voltage working conditions of L_2 and the selected part characteristics are shown on Table 4.5 and Table 4.6 respectively. In this case, both current and voltage stress are well handled by the selected part.

Parameter	Value
L_2	10 µH
I_{L2}	3.15 A
V_{L2}	200 V
f	1 MHz

Table 4.5: Working conditions of L_2

Parameter	Value
P/N	D05040H-103
I_{sat}	17.8 A
I_{rms}	8.6 A
SRF	22 MHz

Table 4.6: Part characteristics

4.1.3 Capacitor selection

Due to the frequency and voltage requirements of this application, the selected capacitors are multilayer ceramic capacitors (MLCC). This technology provides very low equivalent series resistance (ESR) and ultra high self-resonance.

Capacitor C_1

On Table 4.7 is reported the working condition of a single capacitor of the capacitive interface ($C_{\text{int1}} - C_{\text{int2}}$). According to these requirements, a capacitor from Vishay is selected, whose main characteristics are shown on Table 4.8, according to its datasheet.

Parameter	Value
$C_{\text{int1}-2}$	75 pF
$I_{C\text{int1}-2}$	0.41 A
$V_{C\text{int1}-2}$	1.1 kV
f	1 MHz

Table 4.7: Working conditions of $C_{\text{int1}-2}$

Parameter	Value
P/N	VJ1111D750JXRAJ
V_{max}	1.5 kV
DF	0.05%

Table 4.8: Part characteristics

Capacitor C_2

Similarly, the working condition of the series capacitors $C_{2\text{a}} - C_{2\text{b}}$ is shown on Table 4.9. The selected part (from Kemet) main characteristics are obtained from its datasheet, and reported on Table 4.10.

Parameter	Value
$C_{2\text{a}-\text{b}}$	5.1 nF
$I_{C2\text{a}-\text{b}}$	3.2 A
$V_{C2\text{a}-\text{b}}$	100 V
f	1 MHz

Table 4.9: Working conditions of $C_{2\text{a}-\text{b}}$

Parameter	Value
P/N	C0805C512MAGACAUTO
V_{max}	250 V
DF	0.1%

Table 4.10: Part characteristics

4.1.4 Power MOSFET selection

Due to the high switching frequency and voltage ratings of the inverter, the switches are made with Power MOSFETs. The working conditions of these transistors are shown in Table 4.11. According to these requirements, the selected device is from STmicroelectronics, and its main characteristics (presented in its datasheet) are reported in Table 4.12.

4.1.5 Diode selection

Lastly, the diodes of the rectifier must be selected. Since the working frequency is 1 MHz, these will be Schottky diodes. The working conditions on a single diode are reported in Table 4.13, according to which a component of STmicroelectronics is selected, whose main characteristics are reported in Table 4.14.

Parameter	Value
V_{max}	310 V
I_{max}	0.41 A
f	1 MHz

Table 4.11: Working conditions of the MOSFETs

Parameter	Value
P/N	STD5NK40Z-1
$V_{ds,max}$	400 V
$I_{ds,max}$	2 A
$R_{ds,hot}$	4 Ω
t_{rise}	6 ns
t_{fall}	11 ns
V_{sd}	1.6 V
Q_g	11.7 nC

Table 4.12: Part characteristics

Parameter	Value
$I_{D,av}$	1 A
$I_{D,max}$	3.15 A
$V_{inv,max}$	20 V
f	1 MHz

Table 4.13: Working conditions of the diodes

Parameter	Value
P/N	STPS2H100ZFY
$I_{av,max}$	2 A
$V_{inv,max}$	100 V
V_F	0.65 V

Table 4.14: Part characteristics

4.1.6 Component summary

To conclude this section, a summary of the selected components is presented in Table 4.15.

Component	Part number	Manufacturer
L_1	D05040H-684	Coilcraft
L_2	D05040H-103	Coilcraft
C_{int1-2}	VJ1111D750JXRAJ	Vishay
C_{2a-b}	C0805C512MAGACAUTO	Kemet
MOSFETs	STD5NK40Z-1	STmicroelectronics
Diodes	STPS2H100ZFY	STmicroelectronics

Table 4.15: Component summary

4.2 Loss calculation

Now that all components have been selected, the next step to obtain the system efficiency is to calculate the power dissipated by each one of them. Each component dissipates power in a different way, and the goal of this section is to study and quantify all of them.

4.2.1 Inductor loss

Power inductors are passive components made by an insulated wire wound into a coil, with a magnetic core made of iron or ferrite inside. Power dissipation of these components come in a few ways [24]:

- DC winding loss: Power dissipation on the DC resistance of the winding (DCR).
- AC winding loss: Power dissipation due to the increased winding resistance at higher frequency, caused by skin effect and proximity effect.
- Core loss: Power loss on the magnetic core. This contribution, difficult to predict, depends on several factors, such as peak-peak ripple current, ripple current frequency, core material, core size, and turn count.

DC winding loss is simple to calculate:

$$P_{\mathrm{DC}} = I_{\mathrm{L,rms}}^2 \mathrm{DCR} \tag{4.2}$$

By contrast, accurate AC winding and core loss are complicated to estimate, since they depend on proprietary design information, such as core material and number of turns.

Therefore, to predict the total loss in the inductors and not just the DC loss, an online tool will be used [25]. This Power Inductor Finder and Analizer tool, from Coilcraft website, is based on actual device measurements under different working conditions. Entering the information of required inductance, frequency and current ratings for a certain application, the tool provides the total inductor loss at these conditions.

To obtain the losses of the selected inductors for this application, the data of Table 4.3 (for L_1) and Table 4.5 (for L_2) is entered into the online tool. The results are shown in Figure 4.2, where at the top there is the L_1 loss, and at the bottom the one of L_2.

It has to be mentioned that these predicted losses are estimated under the assumption that the current waveform is triangular. This is not the case of the present design, in which the currents are sinusoidal. Due to the higher harmonic content and rms value of the sinusoidal waveform with respect to the triangular one, higher power loss is expected for the former. However, since there is no easy way to calculate this difference, and the objective of this analysis is simply to obtain an estimate, this fact will be neglected.

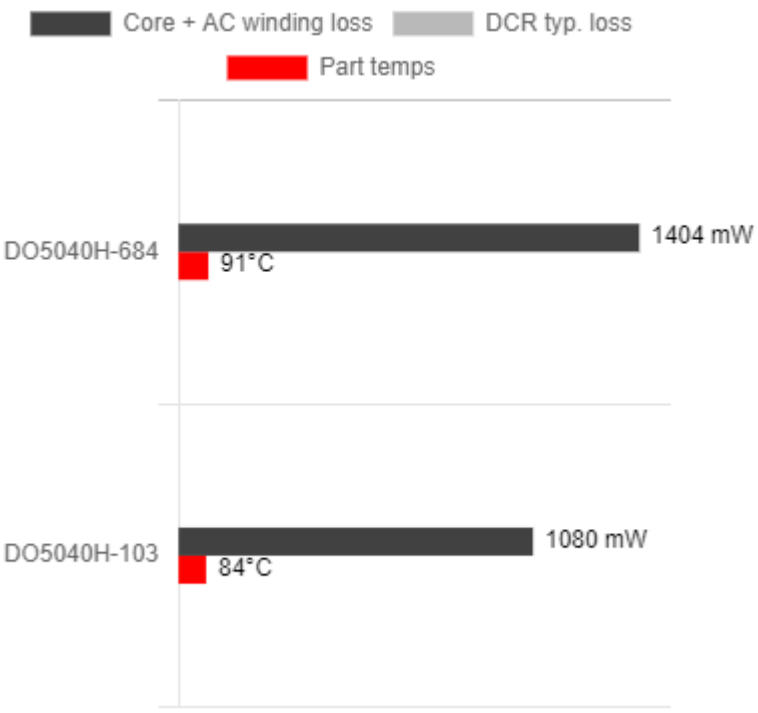

Figure 4.2: Total power loss of L_1 and L_2

4.2.2 Capacitor loss

Power loss of ceramic capacitors can be modelled simply using a single parameter, the ESR (Equivalent Series Resistance), which is the sum of the ohmic losses of the dielectric and the materials used in the construction of the capacitor [26]. Then, the power dissipated by a capacitor is calculated by multiplying the ESR with the square of the rms current flowing through it:

$$P_{\text{loss,C}} = I^2_{\text{C,rms}}\text{ESR} \tag{4.3}$$

Usually, datasheets do not provide directly the ESR. Instead, a similar parameter is provided: the dissipation factor, DF (also called loss angle). This parameter is defined as the ratio of the ESR and the capacitive reactance, which is expressed as follows:

$$\text{DF} = \frac{\text{ESR}}{X_c} \tag{4.4}$$

where X_c is the capacitive reactance, whose magnitude is:

$$X_c = \frac{1}{\omega C} \tag{4.5}$$

According to this, losses in the capacitors of the system are reported in Table 4.16. The rms currents are obtained by mathematical circuit analysis and verified by simulations.

	$C_{\text{int1}-2}$	$C_{2\text{a}-\text{b}}$
Capacitance	75 pF	5.1 nF
DF	0.05%	0.1%
ESR	1.06 Ω	31 mΩ
$I_{\text{C,rms}}$	0.29 A	2.25 A
P_c	90 mW	150 mW

Table 4.16: Capacitor loss

4.2.3 MOSFET loss

Power MOSFETs are semiconductor devices designed to handle significant power levels while working at high switching frequency. These devices dissipate power in the form of many different factors [27]:

- Conduction loss.
- Switching loss.
- Dead time loss.
- Gate charge loss.

All these contributions will be explained and quantified in the following subsections. To calculate them, it is necessary to observe both the current and voltage waveforms across the transistor, shown in Figure 4.3.

Some power loss contributions depend on rms current, while others depend on the instantaneous current and voltage at turn-on and turn-off transitions. If ZCS is achieved, the latter contributions (which are switching loss and dead time loss) are zero. However, as can be seen in Figure 4.3, ZCS is not completlely achieved since a small amount of current is present at the instant of commutations. Due to this current, which is estimated to be 20 mA, these two power loss contributions are greater than zero.

Conduction loss

Conduction loss is caused by the on-state drain to source resistance, which produces power dissipation due to the flow of current through it. This loss contribution is calculated as follows:

$$P_{\text{cond}} = I_{\text{rms}}^2 R_{\text{ds,on}} \tag{4.6}$$

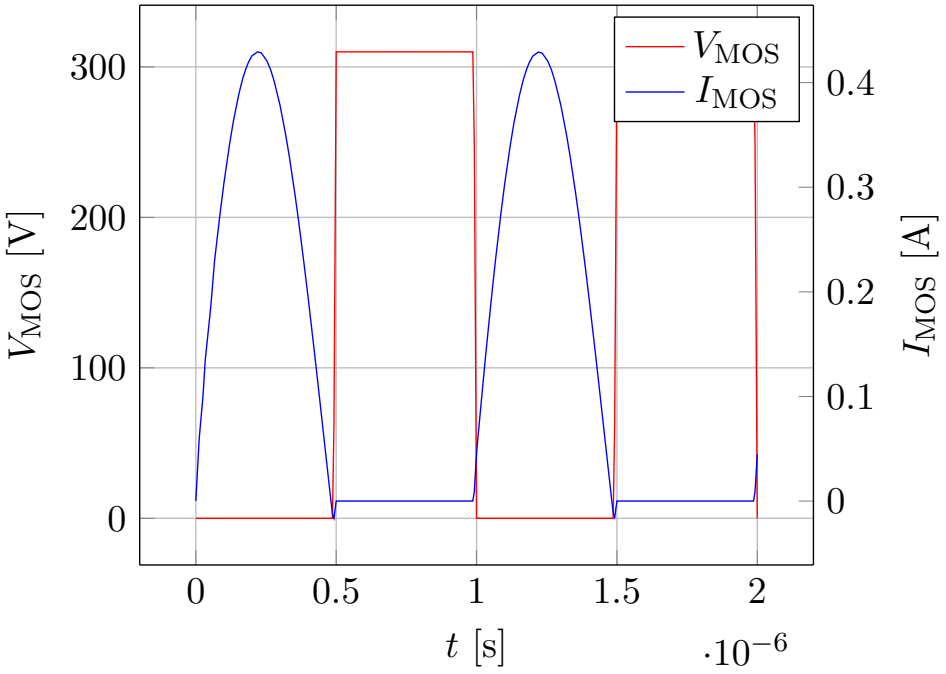

Figure 4.3: Current and voltage waveforms of MOSFETs

where I_{rms} is the rms current flowing through the transistor and $R_{\text{ds,on}}$ is the on-resistance, provided in datasheets. This parasitic resistance is dependent on the junction temperature, that depends in the flow of current. At zero current, the on-resistance is at its minimum, known as "cold" resistance. But if there is some current flow, this resistance increases its value, and under this condition it is known as "hot" resistance. This last value is the one that must be considered for calculating the conduction loss, which can be obtained by curves provided in datasheets and shown in Table 4.12.

Calculating the rms value of the half sinusoidal current through the transistor, shown in Figure 4.3, the conduction loss is found to be:

$$P_{\text{cond}} = 160\,\text{mW} \tag{4.7}$$

Switching loss

Switching losses occur due to simultaneous presence of drain-source voltage and drain current during each transient from turn-off state into turn-on state and viceversa. This loss depends on the instantaneous current and voltage at the moment of the commutations, and on the time that takes the device to turn-on and turn-off. These times depend on parasitics of each device, and estimated values are reported in datasheets, and shown in Table 4.12.

To calculate this power loss, the following formula is used:

$$P_{\text{sw}} = \frac{1}{2} V_{\text{DC}} I_{\text{comm}} (t_{\text{rise}} + t_{\text{fall}}) f \tag{4.8}$$

where I_{comm} is the instantaneous current at the instant of commutations, which according to Figure 4.3, is approximately 20 mA. Applying the previous equation, this loss contribution is approximately:

$$P_{\text{sw}} = 50\,\text{mW} \tag{4.9}$$

Dead time loss

If both the high-side MOSFET and low-side MOSFET are in conduction mode simultaneously, a short-circuit occurs between the voltage source and ground, and a very large current spike is generated. To prevent this, the dead time is set to turn OFF both MOSFETs. During this time, there is a flow of current due to the L_1 series inductor, which flows to the low-side MOSFET body diode, causing power dissipation in this diode. This power loss can be calculated as follows:

$$P_{\text{dt}} = V_{\text{sd}} I_{\text{comm}} t_{\text{dead}} f \tag{4.10}$$

where V_{sd} is the forward voltage drop across the body diode, which is provided in datasheets and shown in Table 4.12. The dead time is a value selected by the designer, in this case 30 ns. With these values, the dead time power loss is calculated to be:

$$P_{\text{dt}} < 1\,\text{mW} \tag{4.11}$$

Since this contribution is so small, it will be neglected.

Gate charge loss

Gate charge power loss is caused by the energy required to charge the parasitic input capacitances present in the device. It depends on the total gate charge needed to rise the V_{gs} voltage up to a certain threshold, in this analysis set to 10 V. The total charge, Q_{g}, is a parameter specified in datasheets and shown in Table 4.12.

This power loss contribution is calculated according to the following equation:

$$P_{\text{gc}} = V_{\text{gs}} Q_{\text{g}} f \tag{4.12}$$

$$P_{\text{gc}} = 120\,\text{mW} \tag{4.13}$$

Total MOSFET loss

The total power dissipated by a MOSFET is calculated by summing all its contributions. This is reported in Table 4.17.

Contribution	Value
P_{cond}	160 mW
P_{sw}	50 mW
P_{dt}	>1 mW
P_{gc}	120 mW
$P_{\text{tot,MOS}}$	330 mW

Table 4.17: Total loss of a MOSFET

4.2.4 Diode loss

Power loss on Schottky power diodes comes in the form of two factors:

- Conduction loss.
- Reverse loss.

These two contributions will be explained and quantified in the following subsections. In order to calculate them, the voltage and current waveforms across a diode are shown in Figure 4.4.

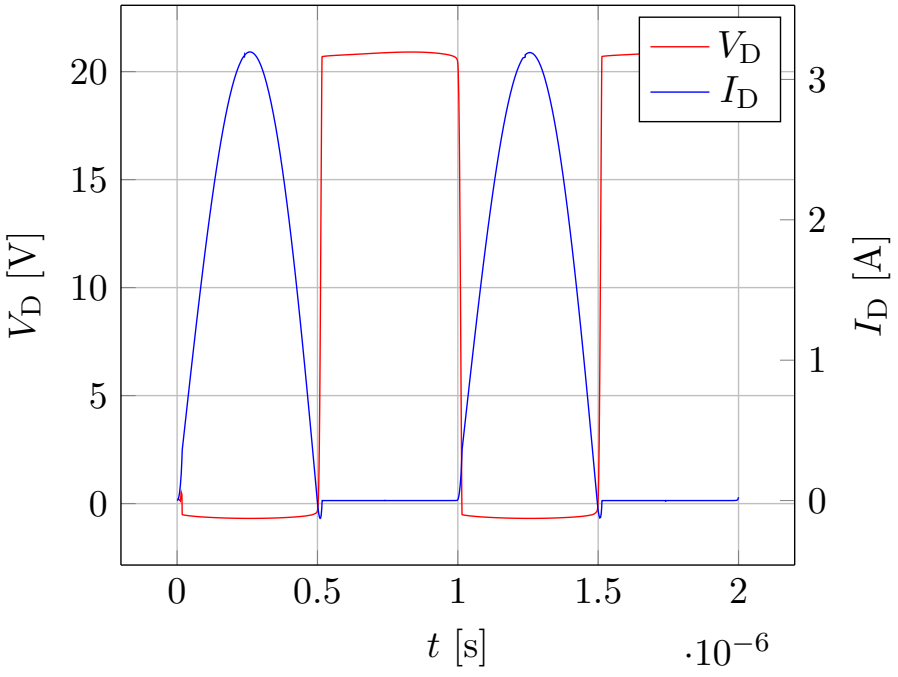

Figure 4.4: Current and voltage waveforms of a diode

Conduction loss

Conduction loss in a diode appears when it is in forward conduction mode, due to the on-state forward voltage drop (V_F). This loss is the average dissipated power in the diode during the conduction phase. To perform a precise analysis of these losses, considering diode parameters as a function of the junction temperature, one can refer to [28]. In this analysis, a simplified formula provided in the selected part datasheet is used:

$$P_{\text{cond}} = 0.57 I_{\text{D,av}} + 0.065 I_{\text{D,rms}}^2 \tag{4.14}$$

where $I_{\text{D,av}}$ and $I_{\text{D,rms}}$ are the average and rms currents through the diode respectively, which can be obtained by Figure 4.4:

$$I_{\text{D,av}} = 1\,\text{A} \tag{4.15}$$
$$I_{\text{D,rms}} = 1.58\,\text{A} \tag{4.16}$$

Applying these values to (4.14), the conduction loss is calculated to be:

$$P_{\text{cond}} = 730\,\text{mW} \tag{4.17}$$

Reverse losses

Reverse losses in a diode are the result of a reverse bias applied on the diode, which produces a leakage current I_{rev} [29]. The leakage current is an intrinsic parameter of the diode, which is provided in datasheets as a curve versus the reverse voltage and the junction temperature. This power loss contribution is calculated using the following equation:

$$P_{\text{rev}} = V_{\text{rev}} I_{\text{rev}} \tag{4.18}$$

According to the datasheet, the reverse leakage current at 20 V reverse voltage is around 3 mA. With these values, the reverse loss is calculated as:

$$P_{\text{rev}} = 60\,\text{mW} \tag{4.19}$$

Total diode loss

The total loss in each diode is given by the sum of the conduction and reverse losses:

$$P_{\text{tot,D}} = P_{\text{cond}} + P_{\text{rev}} \tag{4.20}$$
$$P_{\text{tot,D}} = 790\,\text{mW} \tag{4.21}$$

4.2.5 Total system loss

To conclude this section, the total system loss will be calculated by summing the losses on each device. This calculation is shown on Table 4.18.

Component	**Unit loss**	**Quantity**	**Total**
L_1	1404 mW	1	1404 mW
L_2	1080 mW	1	1080 mW
$C_{\text{int1}-2}$	90 mW	2	180 mW
$C_{2\text{a}-\text{b}}$	150 mW	2	300 mW
MOSFET	330 mW	2	660 mW
Diode	790 mW	4	3160 mW
		Total	6784 mW

Table 4.18: Total loss

4.3 Efficiency calculation

Now that all losses have been studied and quantified, the system efficiency can be calculated. First, it will be calculated at nominal load condition, so considering the losses of Table 4.18. Then, by making some approximations, the efficiency will be expressed as a function of the load and the output voltage.

4.3.1 Efficiency at nominal load

The efficiency of a system is defined as useful output power divided by total power consumed:

$$\eta = \frac{P_{\text{o}}}{P_{\text{in}}} \tag{4.22}$$

In an ideal lossless system, this ratio is 1 and the efficiency is consequently 100%. However, since real components have losses, the efficiency in practical applications is always lower.

A fraction of the power consumed is transformed into useful output power, and the rest of it is dissipated as heat. Therefore, equation (4.22) can be expressed as:

$$\eta = \frac{P_{\text{o}}}{P_{\text{o}} + P_{\text{L,tot}}} \tag{4.23}$$

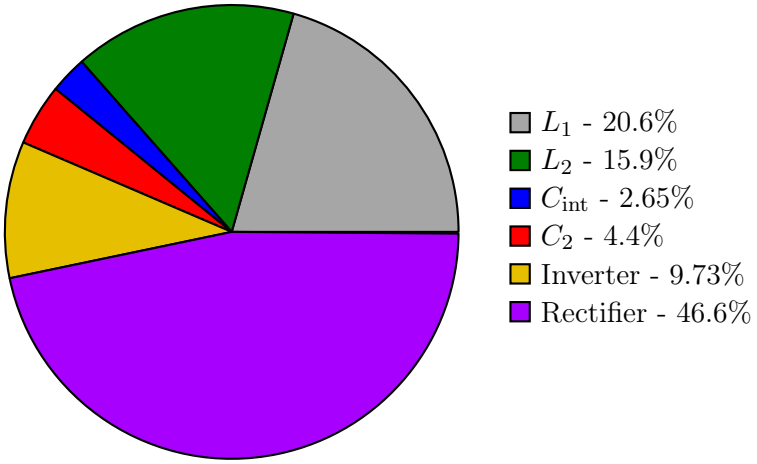

Figure 4.5: Power loss distribution among circuit components

where $P_{\text{L,tot}}$ is the total loss of the system, shown in Table 4.18. According to this result and the output power shown in Table 4.2, the efficiency is calculated as:

$$\eta = \frac{40\,\text{W}}{40\,\text{W} + 6.78\,\text{W}} \tag{4.24}$$

$$\eta = 0.855 \tag{4.25}$$

The CPT system of Figure 4.1 is expected to have an 85.5% efficiency when working at nominal load. To visualize the relative importance of the many loss contributions, a pie chart is presented in Figure 4.5. It can be seen that the most relevant factor is the rectifier, which constitutes almost 47% of the total loss.

4.3.2 Efficiency as a function of the load

Since in battery charging applications the load is expected to vary, it is useful to study the behaviour of the efficiency for different load conditions. This is why curves of efficiency versus output load will be developed, considering losses on all blocks, but with some simplifications. These simplifications are necessary in order to make hand-calculation analysis. The analysis presented here is an extension of [30], where just the losses of the passive components (inductors and capacitors) were considered.

The goal is to mathematically express the efficiency as a function of the load. In order to do this, an assumption is considered: *Power losses on all componentes can be represented simply with an equivalent resistor*. Of course, in general terms this is incorrect, since non linear devices such as power inductors, power MOSFETs and Schottky diodes produce losses that cannot be modeled in this way. However, under the approximations explained next, this assumption can be considered to be true.

If losses in all components can be modeled simply using a series resistor, then all of them can be calculated using the following equation:

$$P_{\text{Loss}} = I_{\text{rms}}^2 R_{\text{eq}} \tag{4.26}$$

Under this approximation, losses in all components can be calculated in a simple way, and so can the system efficiency. The problem is that this way of calculating losses is only valid for linear devices, which is not the case for this CPT system. Therefore, to express the losses in this way, the following approximations on the various components are considered.

- Inductors: As previously explained, power inductor loss comes in the form of different contributions. Some of them are linear (DC winding loss) and some not (AC and core losses). A power inductor of Coilcraft can be modeled with the equivalent circuit of Figure 4.6, in which the frequency dependent behaviour of the component is represented by frequency dependent resistors. Since the present analysis does not account for frequency variations, this model can be simplified into a single equivalent resistance. This series resistance is calculated to dissipate the same power than the complete model under the same working conditions:

  $$R_{\text{eq,L}} = \frac{P_{\text{L}}}{I_{\text{rms,L}}^2} \tag{4.27}$$

  Where the rms current is known by calculations, and the dissipated power is obtained using the online tool.

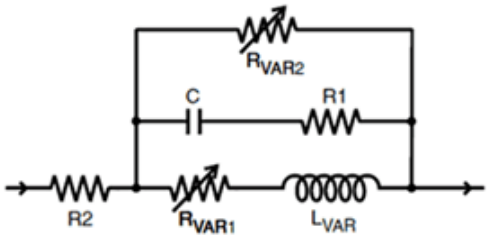

Figure 4.6: Coilcraft inductor model

- Capacitors: Power loss in capacitors is calculated using an equivalent series resistance, the ESR. Therefore, no simplifications are needed for this loss contribution.

- MOSFETs: Power loss in these devices comes in the form of four contributions, and the only one that can be modeled simply by means of a series resistor is the conduction loss. Therefore, for this simplified analysis this is the only factor that will be considered, and the equivalent resistance of the transistors is consequently assumed to be $R_{\text{ds,hot}}$:

  $$R_{\text{eq,MOS}} = R_{\text{ds,hot}} \tag{4.28}$$

As can be seen from Table 4.17, the conduction loss constitutes around 50% of the total MOSFET loss. This means that under this approximation, only this percentage of the inverter loss will be taken into consideration, and consequently the obtained efficiency will be higher than the real one.

- Diodes: Power loss in diodes comes in two different factors: conduction loss and reverse loss. To facilitate the analysis in order to make hand-calculations, only the conduction loss will be considered, which constitutes more than 90% of the total diode loss. This power loss will be calculated taking into account the average forward current trough the diode and the forward voltage drop V_{F}:

$$P_{\mathrm{L,diode}} = I_{\mathrm{D,av}} V_{\mathrm{F}} \tag{4.29}$$

Applying these simplifications, equation (4.23) can be expressed as follows, where to simplify the notation, all currents (with the exception of the output and diode current) are rms currents.

$$\eta = \frac{I_{\mathrm{o}}^2 R_{\mathrm{L}}}{I_{\mathrm{o}}^2 R_{\mathrm{L}} + I_{\mathrm{L1}}^2 R_{\mathrm{eq,L1}} + I_{\mathrm{L2}}^2 R_{\mathrm{eq,L2}} + 2I_{\mathrm{Cint}}^2 R_{\mathrm{eq,Cint}} + 2I_{\mathrm{C2}}^2 R_{\mathrm{eq,C2}} + 2I_{\mathrm{MOS}}^2 R_{\mathrm{eq,MOS}} + 4I_{\mathrm{D,av}} V_{\mathrm{F}}} \tag{4.30}$$

At the numerator there is the output power, while the denominator is made by the sum of the output power with the the power dissipated by every circuit component. These power losses are calculated according to the simplifications explained, in which losses on all components (except the diodes) are assumed to be represented simply with an equivalent series resistor.

To express the efficiency explicitely as a function of the load, both numerator and denominator are divided by I_{o}^2:

$$\eta = \frac{R_{\mathrm{L}}}{R_{\mathrm{L}} + \frac{I_{\mathrm{L1}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,L1}} + \frac{I_{\mathrm{L2}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,L2}} + 2\frac{I_{\mathrm{Cint}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,Cint}} + 2\frac{I_{\mathrm{C2}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,C2}} + 2\frac{I_{\mathrm{MOS}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,MOS}} + 4\frac{I_{\mathrm{D,av}}}{I_{\mathrm{o}}^2} V_{\mathrm{F}}} \tag{4.31}$$

This expression depends on the ratios between the current through the many components and the output current. These current ratios are calculated by circuit analysis on Appendix C. Once these factors are expressed as a function of circuit quantities, the efficiency can be calculated as follows:

$$\eta = \frac{R_{\mathrm{L}}}{\alpha + R_{\mathrm{L}} + \beta R_{\mathrm{L}}^2} \tag{4.32}$$

where α and β are parameters that depend on component values and equivalent resis-

tances, and are calculated as follows:

$$\alpha = \frac{\pi^2}{8}\left(R_{\text{eq,L2}} + 2R_{\text{eq,C2}} + 4V_{\text{F}}\frac{\omega L_{\text{comb}}}{V_{\text{DC}}}\right) \tag{4.33}$$

$$\beta = \frac{8}{(\pi\omega L_{\text{comb}})^2}\left(R_{\text{eq,L1}} + 2R_{\text{eq,Cint}} + R_{\text{eq,MOS}}\right) \tag{4.34}$$

As can be seen, these parameters depend on input specifications (input voltage and frequency), component values (L_{comb}), and the losses on every component, which are represented by equivalent resistances and the forward voltage drop on the diodes.

By deriving (4.32) and making it equal to zero, the load that maximizes the efficiency is found to be:

$$R_{\text{L,opt}} = \sqrt{\frac{\alpha}{\beta}} \tag{4.35}$$

With this optimum load, the maximum efficiency is obtained:

$$\eta_{\text{max}} = \frac{1}{1 + 2\sqrt{\alpha\beta}} \tag{4.36}$$

At this point, the efficiency can be plotted as a function of the load. To do so, the necessary circuit quantities and the equivalent resistances are shown in 4.19 and Table 4.20 respectively.

Parameter	**Value**
V_{DC}	310 V
L_{comb}	9.8 µH
f	1 MHz

Table 4.19: Circuit quantities

Parameter	**Value**
$R_{\text{eq,L1}}$	16.6 Ω
$R_{\text{eq,L2}}$	0.22 Ω
$R_{\text{eq,Cint}}$	1.06 Ω
$R_{\text{eq,C2}}$	31 mΩ
$R_{\text{eq,MOS}}$	4 Ω
V_{F}	0.65 V

Table 4.20: Equivalent resistances

With these values, α and β are calculated to be:

$$\begin{cases} \alpha = 0.9886 \\ \beta = 0.0048 \end{cases} \tag{4.37}$$

which makes (4.32) the following:

$$\eta = \frac{R_{\text{L}}}{0.9886 + R_{\text{L}} + 0.0048R_{\text{L}}^2} \tag{4.38}$$

According to (4.35) and (4.36), the optimum load and maximum efficiency are shown next.

$$\begin{cases} R_{\mathrm{L,opt}} = 14.3\,\Omega \\ \eta_{\max} = 0.88 \end{cases} \tag{4.39}$$

The efficiency curve, generated using Matlab, is shown in blue in Figure 4.7. It is observed that for loads higher than $8\,\Omega$, efficiency is mantained at a high value. On the contrary, for lower loads the efficiency presents a sharp decline. Even though this curve is not very precise due to the simplifications considered, it is helpful to understand the load conditions for which the system performs best.

In addition, Figure 4.7 shows in red the efficiency as a function of the load according to LTspice simulations. This curve was obtained by simulating circuit Figure 4.8, for loads that range from $1\,\Omega$ to $20\,\Omega$. It is observed that the simplified second order equation (4.38) is approximately in agreement with the simulated results, although there are some differences due to the simplifications considered.

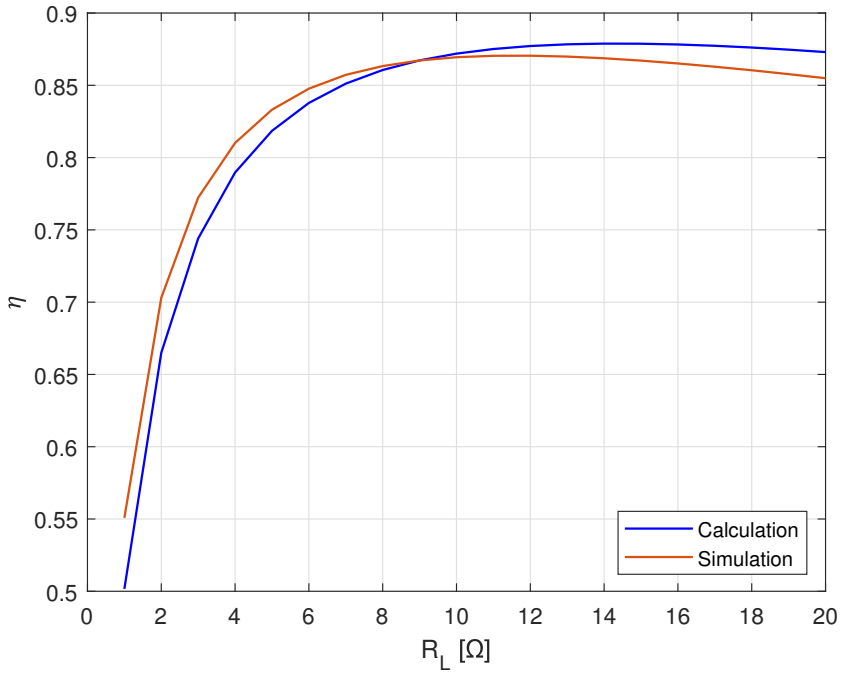

Figure 4.7: Efficiency versus load, Calculation vs Simulation

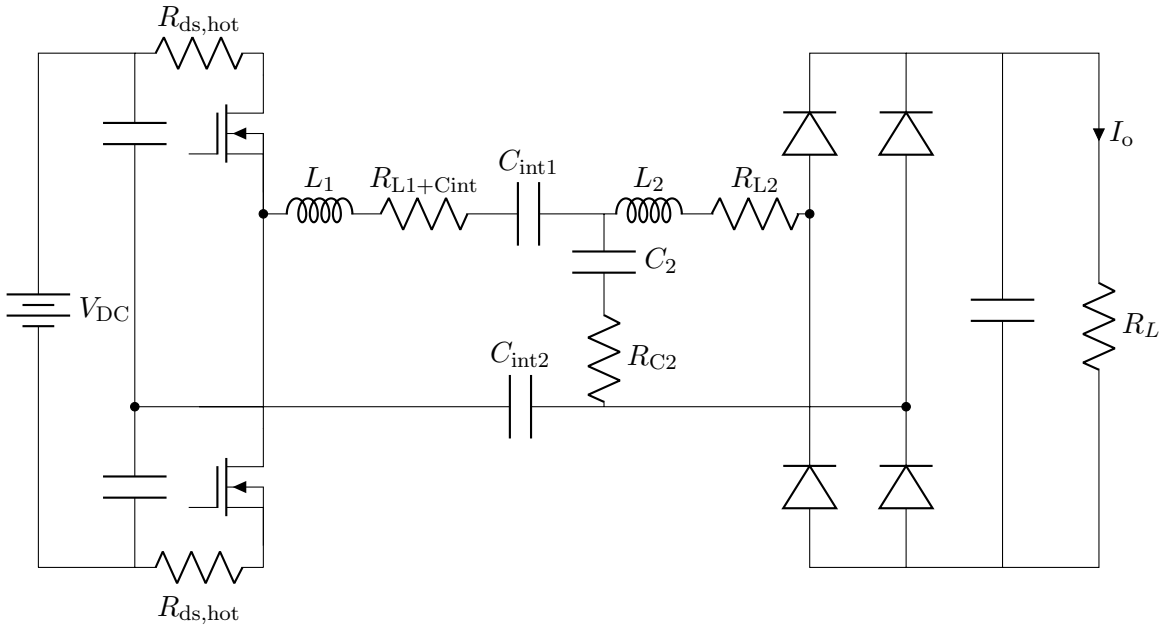

Figure 4.8: Circuit simulated on LTspice to obtain efficiency curves

4.3.3 Efficiency as a function of the output voltage

To conclude this chapter, the efficiency is now plotted as a function of the output voltage. To obtain an expression that shows the relationship between these two quantities, the load is expressed as follows:

$$R_L = \frac{V_o}{I_o} \tag{4.40}$$

Replacing R_L in (4.32) with the previous equation and making some manipulations, efficiency can be expressed as a function of the voltage as shown below.

$$\eta = \frac{V_{\text{o}}}{\alpha I_{\text{o}} + V_{\text{o}} + \dfrac{\beta}{I_{\text{o}}} V_{\text{o}}^2} \tag{4.41}$$

Remembering that for this design $I_o = 2\,\text{A}$, this curve can be generated using Matlab, and is shown in blue in Figure 4.9. In the same graph, it is shown in red the simulated efficiency versus the output voltage. This is obtained by simulating circuit of Figure 4.8 using LTspice.

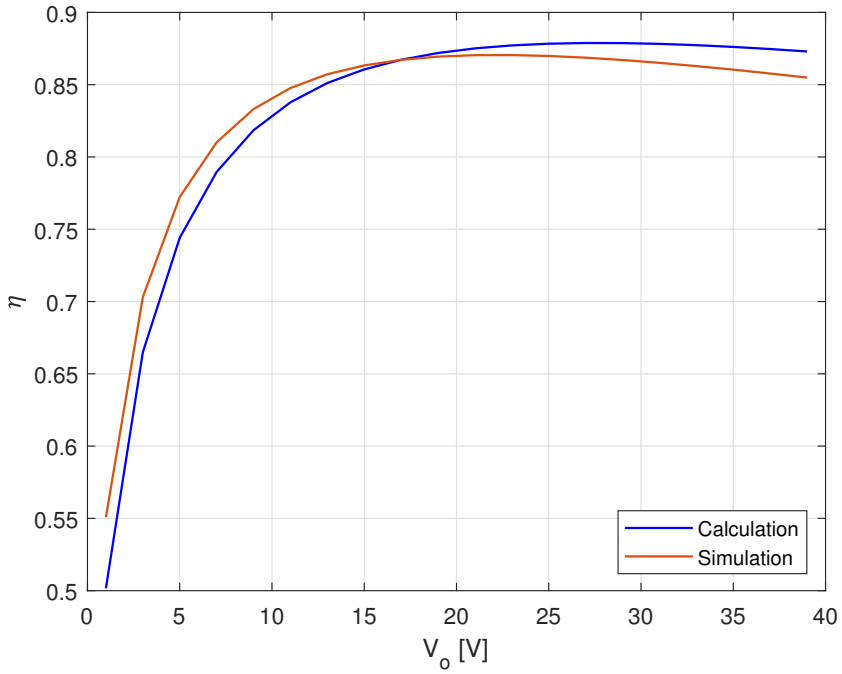

Figure 4.9: Efficiency versus output voltage, Calculation vs Simulation

Chapter 5

Practical limitations and optimal working conditions

In this chapter, the limitations of the CPT system will be studied. These limitations are given by the maximum voltage and current ratings of the devices, in particular of the big inductor L_1. A solution to relax this component is proposed, and its advantages and disadvantages are analized. Finally, the optimal working condition is presented, which is intended to provide a balanced design in terms of efficiency and component stresses.

5.1 Circuit limitations

In previous chapters, the CPT system of Figure 2.4 was studied in detail. From this analysis, it was possible to design a capacitively isolated current supply, that is able to meet the requirements specified in Table 3.1. Furthermore, the establishment of the independent load ZPA condition guarantees high efficiency over a wide range of loads, as shown in Figure 4.7.

However, there are practical limitations that make the designed system unusable. These limitations are given by the large required L_1 inductor, and its stressful working conditions. In fact, being a large inductor of 680 µH working at 1 MHz frequency, only a tiny amount of current would produce a high voltage drop across it. For example, if through this device there is a 1 A peak current, a voltage drop of over 4 kV across it would be generated.

Therefore, this inductor size should be reduced, in order to limit the voltage drop. In what follows, expressions to calculate the L_1 inductor size and its voltage drop, as a function of circuit parameters, will be presented. From this equations, it will be possible to find out how these quantities can be reduced. Besides, since real devices have both voltage and current ratings, also the current through L_1 must be controlled.

5.1.1 Voltage across L_1

According to Table 4.3, the voltage drop across L_1 at nominal load is 1.75 kV. This is a very high voltage that needs to be reduced. However, considering the system specifications and requirements of Table 3.1, this voltage stress cannot be reduced. This is because, according to the design procedure of Section 3.2.2, all the passive components are calculated to fulfill a specific task, which means that there are no degrees of freedom that could be used to reduce the voltage stress of L_1.

But since it is necessary to reduce this voltage stress, two solutions are proposed:

1. Relax input specifications:
    - Input voltage.
    - Working frequency.
2. Modify circuit topology.

Even though both solutions are feasible, the second one will not be considered since the goal of the thesis is to investigate the LCL topology. Then, the voltage stress will be reduced by relaxing the specifications, either on input voltage or working frequency.

To understand how these specifications can be used to relax the L_1 inductor, equations to calculate its size, current and voltage according to the specifications, are presented in Table 5.1. L_1 is obtained by the replacement of (3.9) into (3.10), while I_{L1} is obtained by the replacement of (3.9) into (2.28), considering the approximation of (3.6). Then, V_{L1} is calculated using the following equation:

$$V_{L1} = \omega L_1 I_{L1} \tag{5.1}$$

Quantity	**Equation**
L_1	$\frac{2\sqrt{10}}{\pi^2 R_{\mathrm{L,min}}} \frac{V_{\mathrm{DC}}^2}{\omega I_o^2}$
I_{L1}	$\frac{\pi R_L I_o^2}{V_{\mathrm{DC}}}$
V_{L1}	$\frac{2\sqrt{10}}{\pi} \frac{V_{\mathrm{DC}} R_L}{R_{\mathrm{L,min}}}$

Table 5.1: L_1 equations

Table 5.1 shows how the input specifications (of V_{DC} and ω) can be used to modify the conditions of L_1. Since the compensation circuit contains many reactive components, frequency variations would lead to a complex analysis due to the many resonances present in the system. Therefore, to simplify this analysis, only the input voltage will be considered as a degree of freedom to relax the L_1 inductor.

The goal is to reduce the voltage drop across L_1. By analyzing the equations of Table 5.1, it is observed that V_{L1} is linearly dependent on V_{DC}. Therefore, the voltage stress across this inductor can be reduced simply by reducing the input voltage. However, a reduction on V_{DC} not only produces a reduction on V_{L1}: it also modifies other circuit quantities, like I_{L1}. The consequences of the input voltage reduction will be studied later.

5.1.2 Current through L_1

Another quantity that must be controlled is the current that flows through the L_1 inductor. According to Table 4.3 , the peak current at nominal load is 0.41 A, which is lower than the current ratings of the selected inductor, shown in Table 4.4. However, it is shown in Table 5.1 that I_{L1} is linearly dependent on the load, which could cause excesive current through L_1 under light loads.

In order to analize the maximum current that can flow through an inductor, it should be mentioned that power inductor datasheets usually specify two current ratings:

- I_{sat}: defined as the current at which the nominal inductance drops 10% from its value without current.
- I_{rms}: defined as the current that causes a 40°C temperature rise from 25°C ambient.

The current that flows through the device should not exceed neither of the two ratings, so the maximum current that an inductor can handle is the minimum of these ratings. The selected part (DO5040H-683 from Coilcraft) maximum current, according to its datasheet, is then:

$$I_{\mathrm{L1,max}} = 1.1\,\mathrm{A} \tag{5.2}$$

Since this rating is higher than the current that flows at nominal load, no problems are expected in this case. However, due to the load dependence of I_{L1}, it is important to calculate the load for which the maximum current through L_1 (which is 1.1 A) is obtained. This will be the maximum load, and can be calculated by solving I_{L1} for R_L:

$$R_{\mathrm{L,max}} = \frac{I_{\mathrm{L1,max}} V_{\mathrm{DC}}}{\pi I_o^2} \tag{5.3}$$

The previous expression gives the maximum load that can be applied to the system. This limitation can be expressed in a more useful way by means of the output voltage

rather than the load. By multiplying (5.3) with I_o, the maximum voltage that this power supply can provide is obtained as:

$$V_{\mathrm{o,max}} = \frac{I_{\mathrm{L1,max}} V_{\mathrm{DC}}}{\pi I_o} \tag{5.4}$$

Since the maximum voltage is dependent on $I_{\mathrm{L1,max}}$, it is dependent on real device limitations. This makes the analysis complicated, since for every different inductor it would be necessary to look for their ratings on datasheets, which would difficult the design process if many different solutions want to be analyzed. Therefore, it would be useful to parametrize the maximum current as a function of the inductor size. If this is achieved, then the maximum output voltage can be calculated simply by knowing the inductor size, and it will not be necessary to normalize components and look for these limitations on datasheets.

5.1.3 Maximum current parametrization

Different inductors have different current ratings, which causes that the maximum voltage that the system can provide, expressed with (5.4), is dependent on the real device limitations. Since it is desired to perform a parametric analysis varying the input voltage, it would be benefitial to parametrize the maximum current through the inductors, as a function of their size. If this is achieved, then circuit limitations could be calculated mathematically, without needing to look for device limitations on datasheets, since this information would be already put into equations.

This parametrization is possible by selecting inductors of a single family, in this case the DO5040H from Coilcraft. Therefore, this analysis is valid only for inductors that belong to this series. To parametrize the maximum inductor current as a function of size, the maximum current for every inductor of the DO5040H series (extracted from datasheet) is plotted in Figure 5.1. In this graph, both axes are represented in a logarithmic scale, due to the wide ranges of both inductor size and maximum current.

The objective of this analysis is to develop a mathematical model that fits these data points. Analyzing this graph, it is observed that the $(L - I_{\mathrm{L,max}})$ points can be approximated with the following equation:

$$I_{\mathrm{L,max}} = \frac{k_1}{\sqrt{L}} \tag{5.5}$$

where k_1 is a constant that depends on the inductor family, in this case equal to 25.8e−3. Therefore, the maximum current through the inductors of the DO5040H family is calculated as a function of their size as follows:

$$I_{\mathrm{L,max}} = \frac{25.8\mathrm{e}{-3}}{\sqrt{L}} \tag{5.6}$$

The curve generated by this mathematical expression is plotted in the same graph than the data points on Figure 5.2. It can be seen that the curve fits the data reasonably well, and from this point on, the maximum inductor current will be calculated according to this model.

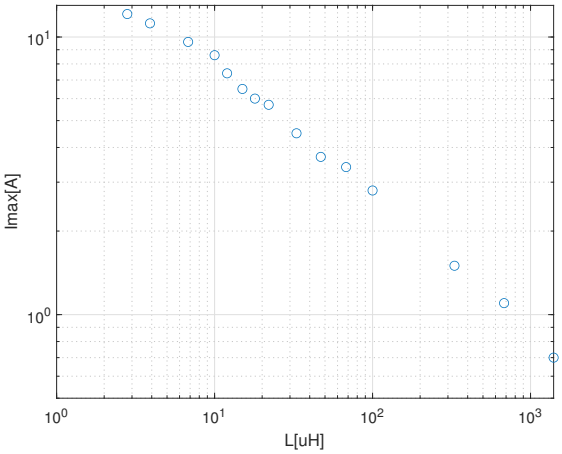

Figure 5.1: $I_{\mathrm{L,max}}$ data points

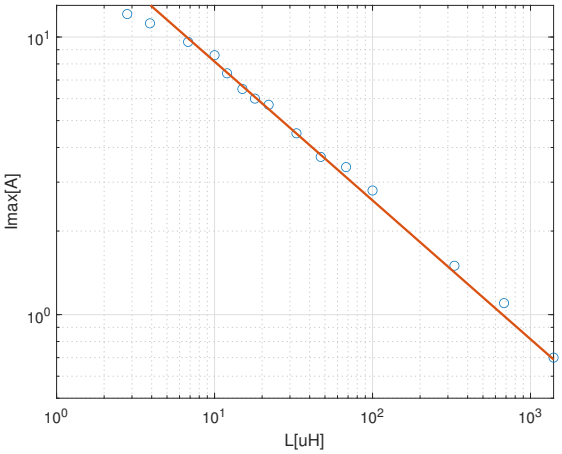

Figure 5.2: $I_{\mathrm{L,max}}$ curve fitting

5.1.4 Maximum output voltage

The maximum output voltage provided by the CPT system is expressed in (5.4). Replacing the maximum inductor current with the parametrization of (5.5), the maximum voltage is expressed as:

$$V_{\mathrm{o,max}} = \frac{k_1 V_{DC}}{\pi I_o \sqrt{L_1}} \tag{5.7}$$

Then, replacing L_1 with the equation of Table 5.1, the previous expression can be represented as follows.

$$V_{\mathrm{o,max}} = k_1 \sqrt{\frac{\omega R_{\mathrm{L,min}}}{2\sqrt{10}}} \tag{5.8}$$

It is observed that the maximum output voltage does not depend on either the input voltage or the output current. It only depends on the working frequency, the minimum load, and the L_1 inductor current limitation, modeled by k_1. Replacing values, the maximum voltage that this power supply can provide is calculated to be:

$$V_{\mathrm{o,max}} = 57.5\,\mathrm{V} \tag{5.9}$$

5.2 Input voltage variation analysis

According to Section 5.1.1, under the specifications of Table 3.1, a very high voltage drop across L_1 is present, which needs to be reduced. It was observed that a reduction in this voltage stress can be achieved by a reduction of the input voltage. Therefore, the system behaviour under different V_{DC} needs to be studied.

To analyze and compare the system performance under different input voltages, a tool presented in Section 4.3.3 will be used: efficiency curves as a function of the output voltage. These curves, in addition to showing the behaviour of the efficiency for different loads, will make it possible to compare different designs based on the following figures of merit:

- Maximum efficiency.
- Efficiency at nominal load.
- Output voltage range.

Besides these figures of merit, also the size and voltage stress of L_1 will be compared among the different designs. All these parameters will be used to select the ideal working condition as objectively as possible, in which it is expected to obtain a balanced design. This optimal design should provide good system efficiency, while at the same time relaxing the L_1 inductor.

To develop efficiency curves for various input voltages, in order to later compare them, the following steps are proposed:

1. Design a few systems according to different input voltages: [50 V, 100 V, 200 V, 300 V]. For each input voltage, the passive components are calculated according to the design procedure of Section 3.2.2.
2. Calculate system losses according to Section 4.2.
3. Develop the curves of efficiency versus output voltage, as explained in Section 4.3.3.

If for every design the passive component values were equal, then their equivalent resistances would also be equal, which would facilitate the analysis. However, passive component values are dependent on the input voltage, as can be seen in Section 3.2.2. This means that for every different design, the inductor and capacitor loss has to be obtained by looking into real device datasheets, which complicates the analysis process.

Therefore, it would be useful to parametrize these losses as a function of component sizes. Since Figure 4.5 shows that inductor losses are far more relevant than capacitor losses, only inductor losses will be considered, while the latter will be neglected.

5.2.1 Parametrization of inductor loss

Power loss on the inductors will be parametrized as a function of their size, in order to make it possible to calculate them for many input voltages without the need of looking for information in datasheets.

According to Section 4.3.2, the power dissipated by the inductors is assumed to be produced simply by an equivalent series resistance. This can be done because the inductor works at a single frequency point, and therefore its model of Figure 4.6 can be approximated to be an ideal inductor plus a series resistor. Therefore, the power dissipation on the inductors can be calculated as:

$$P_{\mathrm{L}} = I_{\mathrm{L,rms}}^2 R_{\mathrm{eq,L}} \tag{5.10}$$

where P_{L} is the inductor loss, provided by the online tool of [25], and I_{Lrms} is the rms current flowing through the inductor, calculated by circuit analysis. The equivalent resistance is then calculated as:

$$R_{\mathrm{eq,L}} = \frac{P_{\mathrm{L}}}{I_{\mathrm{Lrms}}^2} \tag{5.11}$$

The goal is to mathematically express $R_{\mathrm{eq,L}}$ as a function of the inductor size. To do this, the equivalent resistance of every inductor of the DO5040H series is calculated according to the previous expression, and then plotted as a function of its size. This is shown in Figure 5.3, in which again both axes are represented in a logarithmic scale.

By analyzing Figure 5.3, it can be observed that the $(L - R_{\mathrm{eq,L}})$ data points can be approximated by the equation of a straight line, as shown below.

$$R_{\mathrm{eq,L}} = k_2 L \tag{5.12}$$

where k_2 is a constant that depends on the inductor family, in this case equal to 22.8e3. Therefore, the equation of the line is expressed as:

$$R_{\mathrm{eq,L}} = 22.8\mathrm{e}3 \; L \tag{5.13}$$

This line is plotted in the same graph as the data points in Figure 5.4, where it is seen that it fits the data points fairly well. Therefore, the power dissipated by the inductors can be calculated with the following equation:

$$P_{\mathrm{L}} = I_{\mathrm{L,rms}}^2 k_2 L \tag{5.14}$$

where the dependence on real device models is represented by the constant k_2. This parametrization eliminates the need of calculating every inductor loss according to the online tool, therefore speeding up the analysis process.

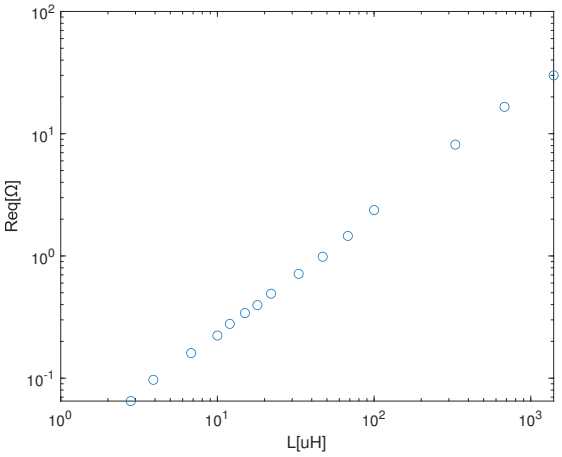

Figure 5.3: $R_{\mathrm{eq,L}}$ data points

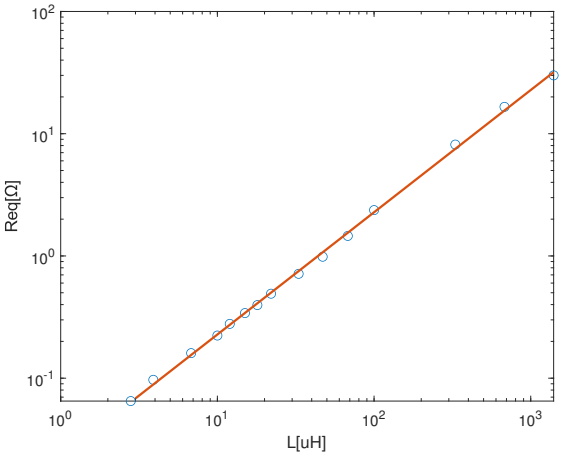

Figure 5.4: $R_{\mathrm{eq,L}}$ curve fitting

5.2.2 Efficiency curves for different input voltages

At this point, efficiency curves for different input voltages will be developed, in which losses on every component will be calculated as a function of both the input and output voltage.

To simplify the analysis, the selected MOSFETs and diodes are invariant according to the input voltage. This means that the parameters to calculate their power dissipations (shown in Table 4.20) are the same for every design, which makes it possible to calculate their losses simply by a mathematical model that considers both the input and output voltage.

On the other hand, the selected passive components cannot be the same for every design, simply because their values are dependent on the input voltage. Therefore, the inductor losses are parametrized according to Section 5.2.1, and the capacitors losses are neglected.

According to Section 4.3.3, the relationship between the efficiency and the output voltage is modeled by the following mathematical expression:

$$\eta = \frac{V_{\mathrm{o}}}{\alpha I_{\mathrm{o}} + V_{\mathrm{o}} + \dfrac{\beta}{I_{\mathrm{o}}} V_{\mathrm{o}}^2} \tag{5.15}$$

where α and β are parameters shown in (4.33) and (4.34) respectively, that model the loss contributions on the different devices, as a function of circuit quantities:

$$\alpha = \frac{\pi^2}{8}\left(R_{\mathrm{eq,L2}} + 4V_{\mathrm{F}}\frac{\omega L_{\mathrm{comb}}}{V_{\mathrm{DC}}}\right) \tag{5.16}$$

$$\beta = \frac{8}{(\pi\omega L_{\mathrm{comb}})^2}\left(R_{\mathrm{eq,L1}} + R_{\mathrm{eq,MOS}}\right) \tag{5.17}$$

These expressions do not consider the power loss on the capacitors, since they are neglected. The objective is to make these parameters take into account different input voltages. Then, the equivalent resistances of the inductors are replaced with the parametric model of (5.12). Also, the approximation of (3.6) is applied, which states that L_{comb} is approximately equal to L_2. With these considerations, now α and β are expressed as:

$$\alpha = \frac{\pi^2}{8}\left(k_2 L_2 + 4V_{\text{F}}\frac{\omega L_2}{V_{\text{DC}}}\right) \tag{5.18}$$

$$\beta = \frac{8}{(\pi\omega L_2)^2}\left(k_2 L_1 + R_{\text{eq,MOS}}\right) \tag{5.19}$$

Finally, L_1 and L_2 are expressed according to Table 5.1 and (3.9) respectively, which are shown below:

$$L_1 = \frac{2\sqrt{10}}{\pi^2 R_{\text{L,min}}}\,\frac{V_{\text{DC}}^2}{\omega I_o^2} \tag{5.20}$$

$$L_2 = \frac{4}{\pi^2}\frac{V_{\text{DC}}}{\omega I_o} \tag{5.21}$$

Replacing these expressions into α and β, now these parameters are expressed as:

$$\alpha = \frac{V_{\text{DC}}}{2\omega I_o}k_2 + \frac{2}{I_o}V_{\text{F}} \tag{5.22}$$

$$\beta = \frac{\sqrt{10}}{\omega R_{\text{L,min}}}k_2 + \frac{\pi^2 I_o^2}{2V_{\text{DC}}^2}R_{\text{ds,hot}} \tag{5.23}$$

These final expressions can be used to perform a parametric efficiency analysis while varying the input voltage, since all terms are expressed as combinations of specifications ($V_{\text{DC}}, I_o, R_{\text{L,min}}$, ω) and losses of components (k_2: inductors, V_{F}: diodes, $R_{\text{ds,hot}}$: MOSFETs).

Now the efficiency can be plotted according to (5.15), where α and β are calculated with (5.22) and (5.23) respectively. As input voltages, [50 V, 100 V, 200 V, 300 V] are considered, and the other parameters are summarized in Table 5.2. The efficiency curves are then plotted using Matlab, and shown in Figure 5.5. The curve for 300 V should be almost the same as the one shown in Figure 4.9, in which the input voltage was 310 V. In this case the efficiency is slightly higher due to the neglected capacitor loss.

It is observed in Figure 5.5 that there is an efficiency increase for input voltage increments, until a point in which it stabilizes, which is around 200 V. This tends to indicate that input voltage increments are benefitial for the system performance. However, it is known that for higher input voltages, the voltage stress of L_1 increases. Therefore, these curves show a tradeoff between system efficiency and inductor voltage stress for input voltage variations.

Parameter	Value
I_o	2 A
f	1 MHz
$R_{L,min}$	5 Ω
k_2	22.8e3
$R_{eq,MOS}$	4 Ω
V_F	0.65 V

Table 5.2: Specifications

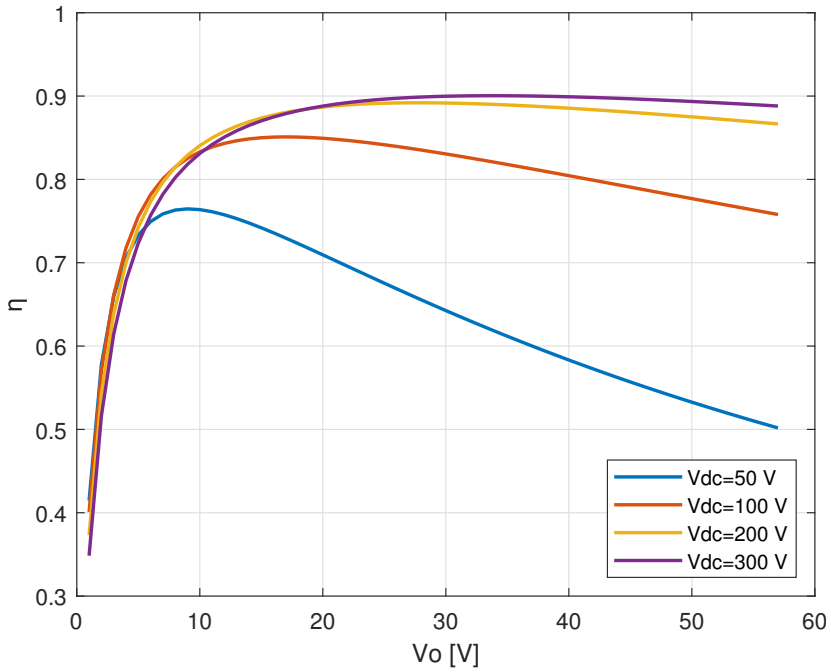

Figure 5.5: Efficiency for different input voltages

These curves are generated with equations (5.15), (5.22) and (5.23), that are developed under the approximation stated in Section 3.2.1, which states than L_1 is much bigger than L_2, expressed as:

$$L_1 \geq 10L_2 \tag{5.24}$$

However, this condition was not taken into account for the designs, which means that for some cases, the condition may not be satisfied and consequently the circuit equations would not be valid. This detail is analyzed in the following section, where a solution to guarantee the verification of condition (5.24) for all designs, is proposed.

5.2.3 Magnification factor

As mentioned, the system analysis and design is made under the assumption that L_1 is much higher than L_2, which is considered to be true if the former is at least ten times higher than the latter (Section 3.2.1). However, since the inductor values depend on the input voltage, there may be some voltages for which the previous condition does not hold.

The proposed solution to make the condition valid regardless of the input voltage, is to manually increase the L_1 inductor until it is exactly ten times greater than L_2, if (5.24) is not satisfied. This L_1 increment, according to (2.20), guarantees ZPA operation for lower loads than $R_{\mathrm{L,min}}$. However, it has two drawbacks:

- Since larger inductors have lower current ratings than smaller inductors (as shown in Figure 5.1), the maximum current through the augmented L_1 will be smaller, causing a reduction in the maximum output voltage (5.4).
- Since larger inductors have higher equivalent resistances than smaller inductors (as shown in Figure 5.3), the power dissipated by the larger L_1 will be higher (5.10), causing an efficiency reduction.

Therefore, an L_1 increment will cause reductions in both output voltage range and system efficiency, worsening system performance. However, this increment is necessary in order to make the system equations accurate, in the cases that condition (5.24) is not valid.

In the cases that L_1 must be increased, it is important to quantify the inductor increment, since this magnitude will determine how much the output voltage range and efficiency are reduced. Therefore, a new parameter m (magnification factor) is introduced, which serves to quantify the inductor increment:

$$m = \frac{L_{1,\mathrm{new}}}{L_{1,\mathrm{old}}} \geq 1 \tag{5.25}$$

where $L_{1,\mathrm{new}}$ is the value of L_1 necessary to satisfy (5.24) (i.e. $10L_2$), and $L_{1,\mathrm{old}}$ is the value of this inductor calculated according to the design procedure, so before the increment. If for a certain design, condition (5.24) is satisfied directly by calculting L_1 according to the design procedure, then this inductor does not need to be increased and m is equal to one. On the other hand, if L_1 needs to be increased, m is larger than one.

In what follows, a quantitative analysis of how the output voltage range and efficiency are reduced by m is presented.

Output voltage range reduction

The magnitude of the output voltage reduction due to the magnification can be obtained according to (5.7):

$$V_{\mathrm{o,max}} = \frac{k_1 V_{DC}}{\pi I_o \sqrt{L_1}} \tag{5.26}$$

It can be seen that the output voltage is inversely proportional to the square root of L_1. If this indutor must be increased, then its new value is obtained using (5.25) as follows:

$$L_1 = mL_{1,\mathrm{old}} \tag{5.27}$$

Replacing this new value on (5.26), now the maximum voltage can be expressed as:

$$V_{\mathrm{o,max}} = \frac{k_1 V_{DC}}{\pi I_o \sqrt{mL_{1,\mathrm{old}}}} \tag{5.28}$$

where $L_{1,\mathrm{old}}$ is the inductance calculated according to the desing procedure and shown in Table 5.1. Replacing this inductor value, the maximum output voltage is calculated to be:

$$V_{\mathrm{o,max}} = \frac{57.5\,\mathrm{V}}{\sqrt{m}} \tag{5.29}$$

It is verified that the presence of the magnification factor produces an output voltage range reduction. Therefore, in order to obtain the maximum achievable output voltage of 57.5 V, m should be one. This means that (5.24) should be satisfied directly by calculating L_1 with the expression shown on Table 5.1.

Efficiency reduction

According to (5.12), the equivalent resistance of the inductors is linearly dependent on the inductor size, as shown below.

$$R_{\mathrm{eq,L1}} = k_2 L_1 \tag{5.30}$$

If L_1 has to be increased to satisfy (5.24), then using (5.25), the equivalent resistance can be expressed as:

$$R_{\mathrm{eq,L1}} = k_2 m L_1 \tag{5.31}$$

Since m is equal or greater than one, the equivalent resistance will be increased. This increment will produce more power dissipation on L_1, which will cause an efficiency reduction. This reduction is quantified by replacing the previous expression on (5.17), and now the β term is expressed as follows.

$$\beta = \frac{\sqrt{10}}{\omega R_{\mathrm{L,min}}} m k_2 + \frac{\pi^2 I_o^2}{2V_{\mathrm{DC}}^2} R_{\mathrm{ds,hot}} \tag{5.32}$$

Efficiency curves considering the magnification factor

At this point, efficiency curves considering these two magnification factor effects are plotted in Figure 5.6. The input voltage range goes from 10 V to 200 V, in order to clearly see the maximum output voltage reduction effect. All these curves are made considering $I_o = 2\,\text{A}$.

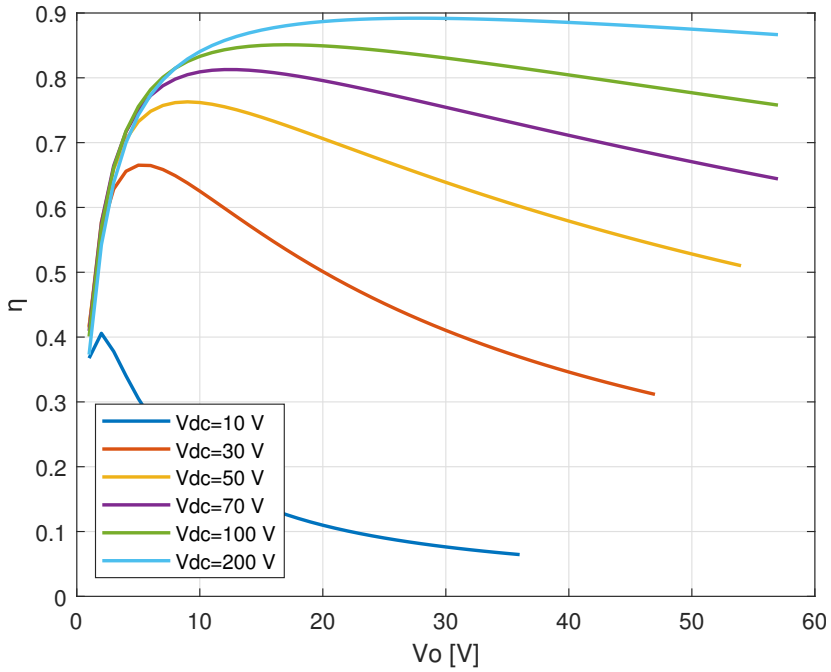

Figure 5.6: Efficiency for different input voltages considering the magnification factor

It is observed that for low input voltages, the maximum voltage and efficiency are lower than for high voltages. This is indicative that, for this voltage range, the magnification factor is higher than one. From the violet curve of 70 V up, the voltage range is at its maximum, which means that the magnification factor is one for these cases.

The condition for which m goes from being larger than one, to being exactly one, is between $V_{\text{DC}} = 50\,\text{V}$ (yellow curve) and $V_{\text{DC}} = 70\,\text{V}$ (violet curve). This happens when L_1 is exactly ten times L_2:

$$L_1 = 10L_2 \tag{5.33}$$

Replacing L_1 and L_2 with (5.20) and (5.21) respectively, the previous equation is expressed as:

$$\frac{2\sqrt{10}}{\pi^2 R_{\text{L,min}}}\,\frac{V_{\text{DC}}^2}{\omega I_o^2} = 10\frac{4}{\pi^2}\frac{V_{\text{DC}}}{\omega I_o} \tag{5.34}$$

Solving this expression for V_{DC}, the voltage for which L_1 is exactly ten times L_2 (defined as critical input voltage $V_{\mathrm{DC,crit}}$), is found to be:

$$V_{\mathrm{DC,crit}} = 2\sqrt{10} R_{\mathrm{L,min}} I_o \tag{5.35}$$

This critical voltage is dependent on the output current, and for $I_o = 2\,\mathrm{A}$ is calculated to be:

$$V_{\mathrm{DC,crit}} = 63.2\,\mathrm{V} \tag{5.36}$$

which is consistent with the appreciation that it should be between 50 V and 70 V.

5.2.4 Working conditions comparison

To find the best working condition as objectively as possible, the different designs of Figure 5.6 are compared in Table 5.3, according to the following figures of merit:

- Efficiency at nominal load, η_{nom}.
- Maximum efficiency, η_{max}.
- L_1 inductor size.
- Voltage stress across L_1 at nominal load, V_{L1}.
- Maximum output voltage, $V_{\mathrm{o,max}}$

V_{DC} [V]	η_{nom}	η_{max}	L_1 [µH]	V_{L1} [V]	$V_{\mathrm{o,max}}$ [V]
10	0.11	0.41	3.2	255	36.3
30	0.5	0.67	9.7	255	47.7
50	0.71	0.76	16.1	255	54.2
70	0.8	0.81	25	282	57.5
100	0.85	0.85	51	403	57.5
200	0.89	0.89	204	805	57.5

Table 5.3: Different solutions comparison

Table 5.3 shows that there are both advantages and disadvantages for designs using high input voltage, which are summarized in Table 5.4. In the following section, an optimal design according to this analysis is proposed.

Pros	Cons
Higher efficiency at nominal load	Larger inductors
Higher maximum efficiency	More stressed inductors
Higher output voltage range	

Table 5.4: Pros and cons of increasing voltages

5.3 Optimal design

In this thesis, a design will be considered to be optimal, if the input voltage is the critical voltage, calculated as (5.35). This choice is based on the intention of reducing the voltage stress across the L_1 inductor, even at the cost of efficiency reduction.

To design an optimal system, all the specifications of Table 3.1 will be kept the same, with the exception of the input voltage. This input voltage is calculated according to (5.35) as 63.2 V. However, due to the need of normalizing passive components, in order to provide 2 A of current, a larger voltage of 80 V is required. Then, the specifications for the optimal design are shown in Table 5.5.

With these specifications, the passive components are calculated according to Section 3.2.2 and shown in Table 5.6. The necessary capacitance to provide ZPA operation is calculated according to (2.14) as 832 pF. To synthesize it, two series capacitors of 1.5 nF and 1.8 nF are selected, whose equivalent capacitance is 819 pF.

Parameter	Value
V_{DC}	80 V
f	1 MHz
P_o	40 W
R_L	10 Ω
$R_{\mathrm{L,min}}$	5 Ω

Table 5.5: Optimal specifications

Component	Value
L_1	33 µH
L_2	2.8 µH
C_{int1}	1.5 nF
C_{int2}	1.8 nF
C_2	10 nF

Table 5.6: Optimal normalized components

The optimal design circuit, with its normalized passive components, is shown on Figure 5.7. The circuit quantities are calculated according to the equations of Table 2.1, and then simulated using LTspice to verify its behaviour. The comparison between calculations and simulations, at nominal load, is shown on Table 5.7.

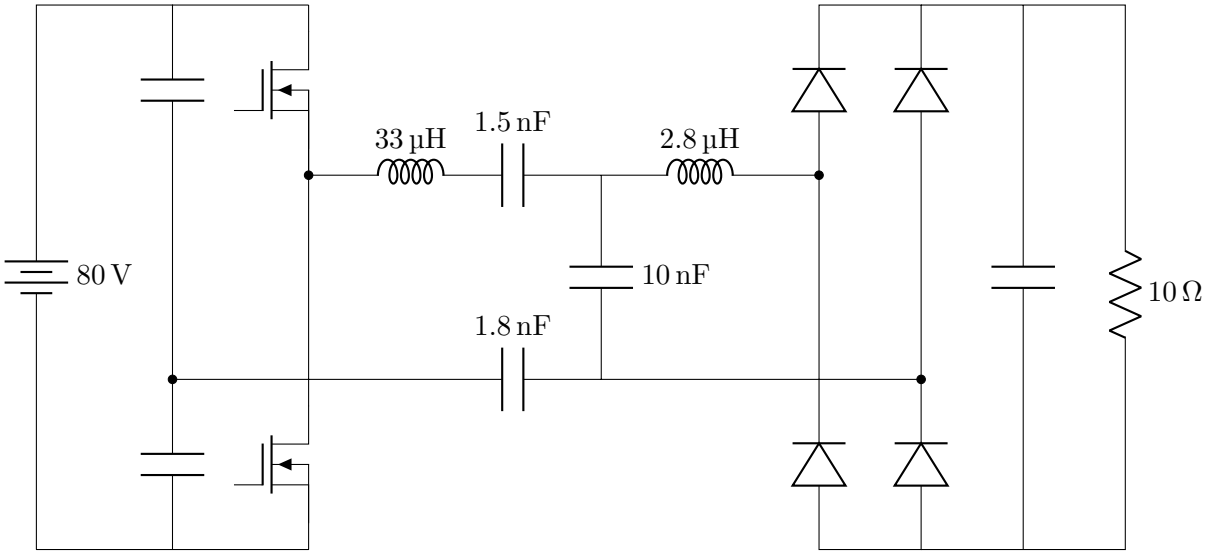

Figure 5.7: Optimal design with normalized passive components

Quantity	Calculated	Simulated
I_o	2 A	1.98 A
I_{L1}	1.57 A	1.64 A
I_{L2}	3.14 A	3.12 A
V_o	20 V	19.8 V
P_o	40 W	39.3 W

Table 5.7: Optimal design circuit quantities

5.3.1 Component selection

To conclude this analysis, the efficiency of the optimal design is calculated. To study the system efficiency, first actual components are selected according to Section 3.2.3. These devices are reported in Table 5.8, where it is seen that both the MOSFETs and the diodes are the same as the previous case (shown in Table 4.15). The inductors belong to the same family than before, but now have different values. Finally, since the capacitors also have different values than before, the devices are different.

Component	**Part number**	**Manufacturer**
L_1	D05040H-332	Coilcraft
L_2	D05040H-282	Coilcraft
C_{int1}	C1206C152JAGAC7867	Kemet
C_{int2}	C1206C182GCGAC7800	Kemet
C_2	C1206C103J1GACAUTO	Kemet
MOSFETs	STD5NK40Z-1	STmicroelectronics
Diodes	STPS2H100ZFY	STmicroelectronics

Table 5.8: Optimal component selection

5.3.2 Efficiency at nominal load

According to what was explained in Section 4.2 the losses on every device is calculated and reported in Table 5.9. Then, the efficiency at nominal load is calculated according to equation (4.22):

$$\eta = \frac{40\,\text{W}}{40\,\text{W} + 10.14\,\text{W}} \tag{5.37}$$

$$\eta = 0.798 \tag{5.38}$$

The CPT system with optimal design is expected to have a 79.8% efficiency when working at nominal load. This value is slightly lower than the 80% predicted in Table 5.3, due to the extra contributions of the losses in capacitors.

Component	**Unit loss**	**Quantity**	**Total**
L_1	970 mW	1	970 mW
L_2	330 mW	1	330 mW
C_{int1}	130 mW	2	130 mW
C_{int2}	110 mW	2	110 mW
C_2	80 mW	2	80 mW
MOSFET	2680 mW	2	5360 mW
Diode	790 mW	4	3160 mW
		Total	**10.14 W**

Table 5.9: Total loss

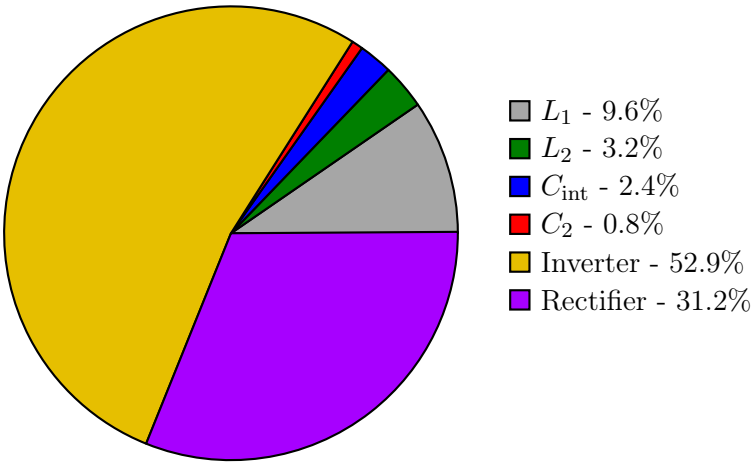

Figure 5.8: Power loss distribution among circuit components

To visualize the relative importance of the many loss contributions, a pie chart is presented in Figure 5.8. It can be seen that in this case, the predominant contribution is the power dissipated in the inverter. This is due to the increment of the conduction loss in the MOSFETs, since now the current through L_1 is increased. On the other hand, the losses on the inductors is reduced, due to a reduction in their sizes.

Therefore, by reducing the input voltage, the stress is moved from the inductors to the MOSFETs. Since the main problem is the stress on the inductors, it makes sense to do this, even if it means an efficiency reduction of around 5% with respect to the previous design.

5.3.3 Efficiency as a function of the output voltage

To conclude, the efficiency as a function of the output voltage is plotted for the optimal design. To do this, equations (5.15), (5.22) and (5.23), are used. The necessary circuit quantities are summarized in Table 5.7, while the parameters to calculate real devices losses are presented in Table 5.11.

The resulting curve is generated using Matlab, and shown in red in Figure 5.9. In blue, there is the efficiency curve of the previous design, the one of Figure 4.9. It is seen that the previous design achieves an efficiency of more than 5% than the optimal design over the entire working range. However, this efficiency reduction is compensated with the relaxation of the inductors, as is shown in the following section when comparing both designs.

Parameter	**Value**
V_{DC}	80 V
L_{comb}	2.58 µH
f	1 MHz

Table 5.10: Circuit quantities

Parameter	**Value**
$R_{\mathrm{eq,L1}}$	790 mΩ
$R_{\mathrm{eq,L2}}$	67 mΩ
$R_{\mathrm{eq,Cint1}}$	106 mΩ
$R_{\mathrm{eq,Cint2}}$	88 mΩ
$R_{\mathrm{eq,C2}}$	16 mΩ
$R_{\mathrm{eq,MOS}}$	4 Ω
V_{F}	0.65 V

Table 5.11: Equivalent resistances

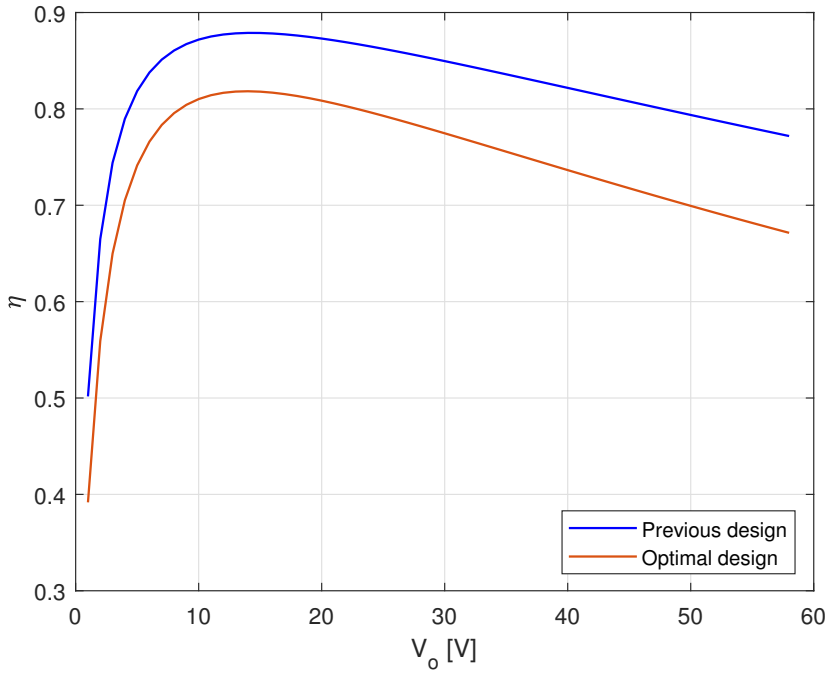

Figure 5.9: Efficiency vs output voltage for previous and optimal design

5.3.4 Design comparison

As a last step, the two designs are compared in Table 5.12. It is seen that the optimal design provides lower efficiency than the previous design, but it also has lower inductor size and voltage stress.

Design	η_{nom}	η_{max}	L_1 [µH]	V_{L1} [V]	$V_{\text{o,max}}$ [V]
Previous	0.87	0.88	680	1750	57.5
Optimal	0.81	0.82	33	330	57.5

Table 5.12: Optimal and previous design comparison

Chapter 6

Conclusion

6.1 Summary

Throughout the thesis, the operation of a system that implements CPT technology is studied in detail. Through this analysis, it is possible to design a capacitively isolated current source, that is, a power supply that has two distinctive features: galvanic isolation by means of a capacitive interface, and constant current output regardless of the load condition. The first characteristic is interesting since a capacitive interface, which consists on two metallic plates separated by a dielectric, is cheaper, lighter and simpler than the traditional inductive interface. Besides, a current source operation is useful for many applications, such as battery chargers and led drivers, to name a few.

This power supply is implemented using a topology that contains several components, some linear (such as capacitors and inductors) and some non-linear (diodes and transistors). As a precise analysis of this system is very complex, approximations are considered to simplify it, from which it is possible to understand, analyze and design the system to meet the proposed requirements. This analysis is then verified by simulations, using the electronic circuit simulator LTspice.

The design of the system consists on the calculation and selection of all the components that make up the circuit. The device selection is made by comparing products from many manufacturers, trying to choose those that are expected to work best under the expected working conditions in terms of voltage, current and frequency. An important criterion for the component selection, is to choose those devices that produce the least losses, in order to obtain a system that works with good efficiency.

Once all the components are selected, the power losses produced by each of them are calculated. This is possible through a detailed analysis of each component, since the physical reason for power dissipation is particular to each one of them. To calculate these losses, several parameters, provided by product datasheets, are used. Then, knowing the

total loss of the system, it is possible to calculate the efficiency, both for nominal load and for a wide range of loads.

Through all this analysis, it is possible to design a power supply, which, in addition to meeting the requirements, works with good efficiency. However, analyzing the working conditions of each component it is found that the series inductor has a very large voltage stress, which would destroy the component. The reason for this high voltage is the high input voltage proposed in the specifications. Then, to solve this problem, the system is analyzed for different input voltage conditions. Through this analysis, it is possible to find an optimal design point, which is expected to provide a balanced design in terms of system efficiency and voltage stresses.

6.2 Future work

All the conclusions established on the analyzed system are based on theoretical analysis and simulations. Even though in theory the system meets the requirements and has good efficiency, in practice there may be limitations in the components that would cause the system to not behave as expected. Therefore, a prototype should be built in order to verify the analyzes presented in this thesis.

In addition to building a prototype to verify the theoretical analysis and simulations, there are several arguments that would be interesting to study, in order to improve system performance. The first of these is to study the possibility of designing a constant voltage power supply with independent load ZPA operation. So far, the designed system only provides constant current with independent load ZPA operation, since the constant voltage mode of operation do not provide this characteristic. Therefore, this system can only be used as a current source, due to the large losses produced by the hard switching in the inverter if the constant voltage mode of operation is used.

Another interesting argument to study is the use of the working frequency as a degree of freedom, to obtain improvements such as the reduction of the voltage stress on the inductors. Although the frequency response of the system was studied through simulations, a complete analysis was not carried out due to the complex nature of multiresonance systems. Therefore, a detailed study of the frequency analysis remains as a future work argument.

Finally, the CPT implementation could be studied using another topology. The idea would be to slightly modify the topology used, in order to achieve better performances. Through the use of a different topology, problems such as the lack of an efficient constant voltage mode of operation or the very high stressed components could be solved.

Appendices

Appendix A

Input reactance calculation

In this appendix, the input reactance of the linear circuit of Figure 2.7 is calculated. This is done by calculating its input impedance and expressing it in cartesian form.

A.1 Input impedance calculation

The circuit of Figure 2.7 is shown again in Figure A.1, but exchanging the position between the L_1 inductor and the C_1 capacitor. This is done to calculate the impedance of the LCL network (Z_{LCL}), to then compensate its reactance using the C_1 capacitor.

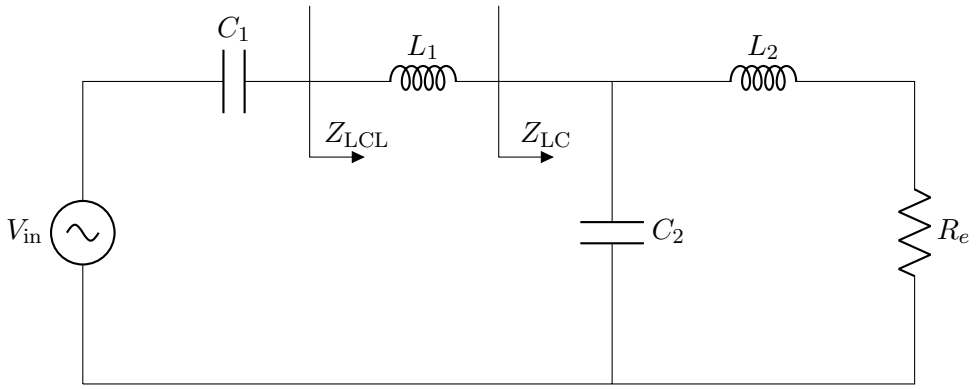

Figure A.1: Simplified linear circuit

As a first step, the impedance of the network formed by C_2, L_2 and R_e (expressed as Z_{LC}) is calculated. To recall, the complex impedance of inductors and capacitors is shown below:

$$Z_{\mathrm{L}} = j\omega L \tag{A.1}$$

$$Z_{\mathrm{C}} = -\frac{j}{\omega C} \tag{A.2}$$

The LC network is made by the parallel combination of C_2 with the series combination of L_2 and R_e:

$$Z_{\mathrm{LC}} = (L_2 + R_e) \parallel C_2 \tag{A.3}$$

Using (A.1) and (A.2), and applying the general rule for parallel impedance calculation, the previous expression can be calculated as:

$$Z_{\mathrm{LC}} = \frac{(j\omega L_2 + R_e)\left(-\frac{j}{\omega C_2}\right)}{R_e + j\omega L_2 - \frac{j}{\omega C_2}} \tag{A.4}$$

Making some manipulations on this expression, it can be transfomed into:

$$Z_{\mathrm{LC}} = \frac{\frac{L_2}{C_2} - j\frac{R_e}{\omega C_2}}{R_e + j\left(\omega L_2 - \frac{1}{\omega C_2}\right)} \tag{A.5}$$

According to Section 2.3.1, C_2 is not a degree of freedom. In fact, this component is calculated to resonate with the parallel combination of L_1 and L_2 at the working frequency. Therefore, C_2 can be expressed as:

$$C_2 = \frac{1}{\omega^2 L_{\mathrm{comb}}} \tag{A.6}$$

where L_{comb} is the parallel combination of L_1 and L_2:

$$L_{\mathrm{comb}} = \frac{L_1 L_2}{L_1 + L_2} \tag{A.7}$$

Replacing (A.6) into (A.5):

$$Z_{\mathrm{LC}} = \frac{\omega^2 L_2 L_{\mathrm{comb}} - jR_e\omega L_{\mathrm{comb}}}{R_e + j(\omega L_2 - \omega L_{\mathrm{comb}})} \tag{A.8}$$

Replacing L_{comb} with (A.7), this expression can be expressed as:

$$Z_{\mathrm{LC}} = \frac{\omega^2 L_2 \frac{L_1 L_2}{L_1 + L_2} - jR_e\omega \frac{L_1 L_2}{L_1 + L_2}}{R_e + j(\omega L_2 - \omega \frac{L_1 L_2}{L_1 + L_2})} \tag{A.9}$$

Making some manipulations, this equation is obtained to be:

$$Z_{\mathrm{LC}} = \frac{\dfrac{(\omega L_2)^2 L_1}{L_1+L_2} - jR_e\dfrac{\omega L_1 L_2}{L_1+L_2}}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} \tag{A.10}$$

At this point, the impedance of the LCL network is calculated by adding the impedance of L_1 to the previous expression:

$$Z_{\mathrm{LCL}} = Z_{\mathrm{LC}} + Z_{\mathrm{L1}} \tag{A.11}$$

$$Z_{\mathrm{LCL}} = \frac{\dfrac{(\omega L_2)^2 L_1}{L_1+L_2} - jR_e\dfrac{\omega L_1 L_2}{L_1+L_2}}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} + j\omega L_1 \tag{A.12}$$

To express this equation using a single denominator, the following is done:

$$Z_{\mathrm{LCL}} = \frac{\dfrac{(\omega L_2)^2 L_1}{L_1+L_2} - jR_e\dfrac{\omega L_1 L_2}{L_1+L_2}}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} + j\omega L_1\frac{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} \tag{A.13}$$

Making some manipulations on the second fraction, this equation is expressed as:

$$Z_{\mathrm{LCL}} = \frac{\dfrac{(\omega L_2)^2 L_1}{L_1+L_2} - jR_e\dfrac{\omega L_1 L_2}{L_1+L_2}}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} + \frac{j\omega L_1 R_e - \dfrac{(\omega L_2)^2 L_1}{L_1+L_2}}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} \tag{A.14}$$

These two fractions can now be summed, since the denominators are equal:

$$Z_{\mathrm{LCL}} = \frac{\dfrac{(\omega L_2)^2 L_1}{L_1+L_2} - \dfrac{(\omega L_2)^2 L_1}{L_1+L_2} + j\omega R_e\left(L_1 - \dfrac{L_1 L_2}{L_1+L_2}\right)}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} \tag{A.15}$$

It can be seen that the real part of the numerator is equal to zero. Making some manipulations on the imaginary part of the numerator, the impedance of the LCL network is expressed as follows:

$$Z_{\mathrm{LCL}} = \frac{jR_e\left(\dfrac{\omega L_1^2}{L_1+L_2}\right)}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} \tag{A.16}$$

To obtain this complex impedance is rectangular form, the denominator must be purely real. To achieve this, the denominator (and numerator) is multiplied by its complex conjugate, as shown below.

$$Z_{\text{LCL}} = \frac{jR_e\left(\dfrac{\omega L_1^2}{L_1+L_2}\right)}{R_e + j\dfrac{\omega L_2^2}{L_1+L_2}} \left(\frac{R_e - j\dfrac{\omega L_2^2}{L_1+L_2}}{R_e - j\dfrac{\omega L_2^2}{L_1+L_2}}\right) \tag{A.17}$$

Multiplying both numerators and denominators and ordering the numerator in real and imaginary part, the impedance can be expressed in cartesian form as follows:

$$Z_{\text{LCL}} = \frac{R_e\left(\dfrac{\omega L_1 L_2}{L_1+L_2}\right)^2 + jR_e^2\dfrac{\omega L_1^2}{L_1+L_2}}{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1+L_2}\right)^2} \tag{A.18}$$

Now that the impedance of the LCL network is expressed in this form, its imaginary part can be obtained simply by inspection as:

$$\text{Im}(Z_{\text{LCL}}) = \frac{R_e^2\dfrac{\omega L_1^2}{L_1+L_2}}{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1+L_2}\right)^2} \tag{A.19}$$

The input reactance of the circuit of Figure A.1, X_{in}, is the series combination of the reactance of C_1 and the one of Z_{LCL}:

$$X_{\text{in}} = \frac{R_e^2\dfrac{\omega L_1^2}{L_1+L_2}}{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1+L_2}\right)^2} - \frac{1}{\omega C_1} \tag{A.20}$$

Which is the equation presented in (2.13).

Appendix B

Circuit quantities calculation

In this appendix, the currents and voltages of the linear circuit of Figure 2.7 are calculated. This is achieved by using the results obtained in Appendix A.

B.1 Current through L_1

The first quantity that needs to be calculated is the current through the L_1 inductor of Figure B.1. This current is dependent on the input impedance, Z_{in}, which was calculated in Appendix A.

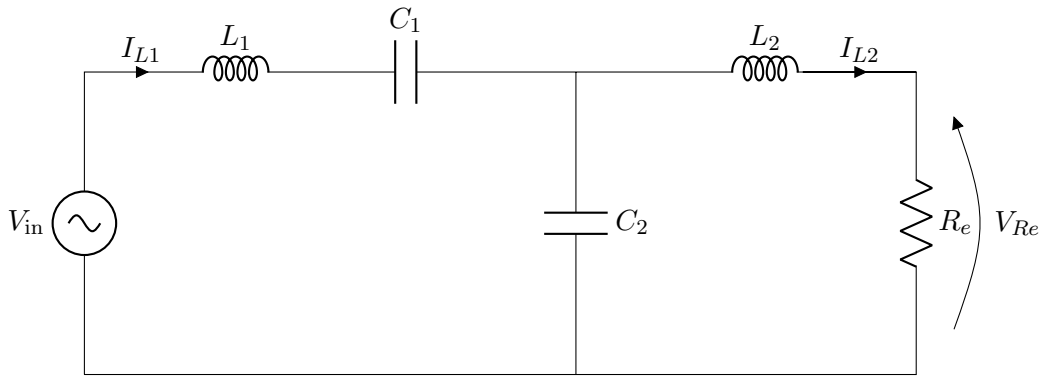

Figure B.1: Simplified linear circuit

In Appendix A, the impedance of the LCL network is calculated and presented in rectangular form in (A.18):

$$Z_{\text{LCL}} = \frac{R_e \left(\frac{\omega L_1 L_2}{L_1 + L_2} \right)^2 + j R_e^2 \frac{\omega L_1^2}{L_1 + L_2}}{R_e^2 + \left(\frac{\omega L_2^2}{L_1 + L_2} \right)^2} \tag{B.1}$$

However, as explained in Section 2.3.2, the reactance is compensated using the C_1 capacitor. Therefore, the input impedance is just the real part of the previous expression:

$$Z_{\text{in}} = \frac{R_e \left(\frac{\omega L_1 L_2}{L_1 + L_2} \right)^2}{R_e^2 + \left(\frac{\omega L_2^2}{L_1 + L_2} \right)^2} \tag{B.2}$$

This expression can be simplified considering the load independent ZPA condition, which is explained in Section 2.3.4. According to this section, in order to obtain load independent ZPA operation, the condition (A.18) needs to be met:

$$R_e^2 >> \left(\frac{\omega L_2^2}{L_1 + L_2} \right)^2 \tag{B.3}$$

Applying this condition, the input impedance can be simplified to:

$$Z_{\text{in}} = \frac{\left(\frac{\omega L_1 L_2}{L_1 + L_2} \right)^2}{R_e} \tag{B.4}$$

The numerator can be expressed in a more synthetic form using the parallel inductor combination equation of (2.12):

$$Z_{\text{in}} = \frac{(\omega L_{\text{comb}})^2}{R_e} \tag{B.5}$$

This input impedance expression is the one shown in (2.22). With this impedance, the input current I_{L1} is calculated as a function of the input voltage simply by means of Ohm's Law:

$$I_{\text{L1}} = \frac{V_{\text{in}}}{Z_{\text{in}}} \tag{B.6}$$

$$I_{\text{L1}} = V_{\text{in}} \frac{R_e}{(\omega L_{\text{comb}})^2} \tag{B.7}$$

This equation is the one reported in (2.23).

B.2 Current through L_2

The current through the L_2 inductor is dependent on the current through L_1 and the current divider formed by C_2 and $(L_2 + R_e)$. To visualize this current divider, the circuit of Figure B.2 is presented, in which L_1 and C_1 are neglected to focus on the last part of the circuit.

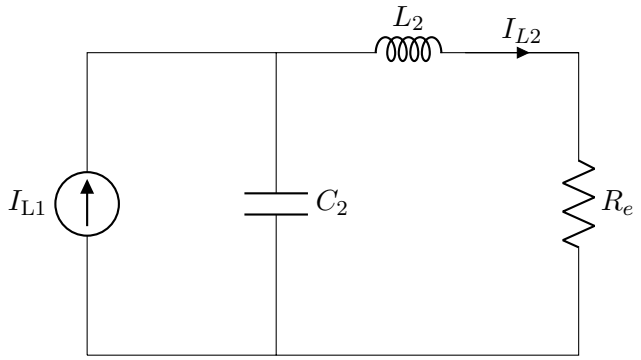

Figure B.2: Circuit to illustrate the current divider

The current through L_2 can be calculated as a function of I_{L1}, applying the current divider formula:

$$I_{\mathrm{L2}} = I_{\mathrm{L1}} \frac{Z_{C2}}{Z_{C2} + Z_{L2} + R_e} \tag{B.8}$$

Let us name the current divider factor as F:

$$F = \frac{Z_{C2}}{Z_{C2} + Z_{L2} + R_e} \tag{B.9}$$

$$F = \frac{-\dfrac{j}{\omega C_2}}{-\dfrac{j}{\omega C_2} + j\omega L_2 + R_e} \tag{B.10}$$

Replacing C_2 with its equivalent expression shown in (A.6), the previous expression is now:

$$F = \frac{-j\omega L_{\mathrm{comb}}}{-j\omega L_{\mathrm{comb}} + j\omega L_2 + R_e} \tag{B.11}$$

$$\tag{B.12}$$

$$F = \frac{-j\omega L_{\mathrm{comb}}}{R_e + j\omega (L_2 - L_{\mathrm{comb}})} \tag{B.13}$$

Replacing the parallel combination of the inductors with (2.12):

$$F = \frac{-j\omega \dfrac{L_1 L_2}{L_1 + L_2}}{R_e + j\dfrac{\omega L_2^2}{L_1 + L_2}} \tag{B.14}$$

This equation is now multiplied and divided by the complex conjugate of the denominator, to get rid of the complex denominator:

$$F = \frac{-j\omega \dfrac{L_1 L_2}{L_1 + L_2}}{R_e + j\dfrac{\omega L_2^2}{L_1 + L_2}} \left(\frac{R_e - j\dfrac{\omega L_2^2}{L_1 + L_2}}{R_e - j\dfrac{\omega L_2^2}{L_1 + L_2}} \right) \tag{B.15}$$

Applying the corresponding multiplications, the following is obtained:

$$F = \frac{-\omega^2 \dfrac{L_1 L_2^3}{L_1 + L_2} - jR_e \left(\omega \dfrac{L_1 L_2}{L_1 + L_2} \right)}{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1 + L_2} \right)^2} \tag{B.16}$$

This complex equation is expressed in cartesian form. However, to calculate the current through L_2 it is necessary to obtain its magnitude. This is calculated by obtaining the real and imaginary part, and then applying the Pythagorean theorem:

$$|F|^2 = \mathrm{Re}(F)^2 + \mathrm{Im}(F)^2 \tag{B.17}$$

where $\mathrm{Re}(F)$ and $\mathrm{Im}(F)$ are obtained by inspection from (B.16):

$$\mathrm{Re}(F) = \frac{-\omega^2 \dfrac{L_1 L_2^3}{L_1 + L_2}}{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1 + L_2} \right)^2} \tag{B.18}$$

$$\mathrm{Im}(F) = \frac{-R_e \left(\omega \dfrac{L_1 L_2}{L_1 + L_2} \right)}{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1 + L_2} \right)^2} \tag{B.19}$$

Applying (B.17), the magnitude of the current divider factor can be expressed as:

$$|F| = \frac{1}{R_e^2 + \left(\dfrac{\omega L_2^2}{L_1 + L_2} \right)^2} \sqrt{\left(\frac{\omega L_1 L_2}{L_1 + L_2} \right)^2 \left(R_e^2 + \left(\frac{\omega L_2^2}{L_1 + L_2} \right)^2 \right)} \tag{B.20}$$

This expression can be simplified by applying the load independent ZPA condition:

$$R_e^2 >> \left(\frac{\omega L_2^2}{L_1 + L_2} \right)^2 \tag{B.21}$$

Using this simplification, the current divider factor is simplified as follows:

$$|F| = \frac{1}{R_e^2}\sqrt{\left(\frac{\omega L_1 L_2}{L_1 + L_2}\right)^2 R_e^2} \tag{B.22}$$

$$|F| = \frac{\frac{\omega L_1 L_2}{L_1 + L_2}}{R_e} \tag{B.23}$$

$$|F| = \frac{\omega L_{\text{comb}}}{R_e} \tag{B.24}$$

At this point, the current that flows through L_2 is calculated using (B.8), with I_{L1} calculated as in (B.7):

$$I_{\text{L2}} = I_{\text{L1}}\,|F| \tag{B.25}$$

$$I_{\text{L2}} = V_{\text{in}}\frac{R_e}{(\omega L_{\text{comb}})^2}\frac{\omega L_{\text{comb}}}{R_e} \tag{B.26}$$

$$I_{\text{L2}} = V_{\text{in}}\frac{1}{\omega L_{\text{comb}}} \tag{B.27}$$

which is the expression reported in (2.24). Finally, to calculate the voltage across the equivalent resistance R_e, the I_{L2} current must be multiplied by the resistance:

$$V_{Re} = V_{\text{in}}\frac{R_e}{\omega L_{\text{comb}}} \tag{B.28}$$

This is the expression shown in (2.25).

Appendix C

Efficiency calculation

In this appendix, the expression to calculate the efficiency as a function of the load shown in (4.31) will be developed. It will start with the calculation of the different current ratios and then proceed with the efficiency equation derivation.

C.1 Current ratios calculation

In this appendix, the efficiency of the circuit of Figure 2.4 (shown below), will be calculated.

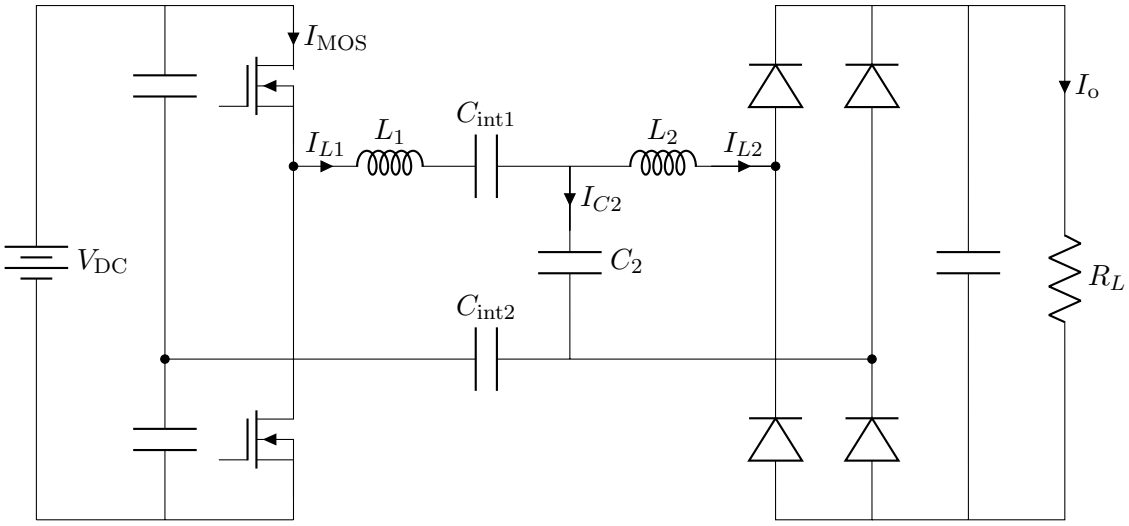

Figure C.1: CPT system with LCL compensator

As discussed in Section 4.3.2, the efficiency of the circuit of Figure 2.4 can be calculated using equation (4.31):

$$\eta = \frac{R_{\mathrm{L}}}{R_{\mathrm{L}} + \frac{I_{\mathrm{L1}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,L1}} + \frac{I_{\mathrm{L2}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,L2}} + 2\frac{I_{\mathrm{Cint}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,Cint}} + 2\frac{I_{\mathrm{C2}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,C2}} + 2\frac{I_{\mathrm{MOS}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,MOS}} + 4\frac{I_{\mathrm{D,av}}}{I_{\mathrm{o}}^2} V_{\mathrm{F}}} \tag{C.1}$$

In this equation, all currents (besides I_{o} and $I_{\mathrm{av,D}}$) are RMS currents. Next, the relationships of the current through the many components and the output current will be calculated.

I_{L1}^2 over I_{o}^2

The peak current through L_1 can be calculated as a function of I_{L2} according to (B.25) as shown below.

$$I_{\mathrm{L1,pk}} = \frac{I_{\mathrm{L2,pk}}}{|F|} \tag{C.2}$$

$$I_{\mathrm{L1,pk}} = I_{\mathrm{L2,pk}} \frac{R_e}{\omega L_{\mathrm{comb}}} \tag{C.3}$$

Since it is necessary to obtain the ratio between $I_{\mathrm{L1,pk}}$ and I_{o}, rather than $I_{\mathrm{L2,pk}}$, the current through L_2 is expressed as a function of I_{o} using (2.5) as:

$$I_{\mathrm{L2,pk}} = \frac{\pi}{2} I_{\mathrm{o}} \tag{C.4}$$

Also, the equivalent load R_e is replaced with the output load R_L using (2.8) as follows:

$$R_e = \frac{8}{\pi^2} R_L \tag{C.5}$$

Applying these replacements, (C.3) can be expressed as:

$$I_{\mathrm{L1,pk}} = \frac{4R_L}{\pi\omega L_{\mathrm{comb}}} I_{\mathrm{o}} \tag{C.6}$$

And the ratio between the two currents is then:

$$\frac{I_{\mathrm{L1,pk}}}{I_{\mathrm{o}}} = \frac{4R_L}{\pi\omega L_{\mathrm{comb}}} \tag{C.7}$$

This expression provides the relationship between $I_{\mathrm{L2,pk}}$ and I_{o}. However, the current through L_2 must be RMS rather than peak. Since I_{L1} is a sinusoidal current, the relation between these two quantities is well known:

$$I_{\mathrm{L1,RMS}} = \frac{I_{\mathrm{L1,pk}}}{\sqrt{2}} \tag{C.8}$$

Using this RMS value, now the ratio between I_{L1} and I_{o} is expressed as:

$$\frac{I_{\mathrm{L1,RMS}}}{I_{\mathrm{o}}} = \frac{4R_L}{\sqrt{2}\pi\omega L_{\mathrm{comb}}} \tag{C.9}$$

Squaring both sides to be consistent with the way the terms are expressed in (C.1), the final expression for this current ratio is shown below.

$$\left(\frac{I_{\mathrm{L1,RMS}}}{I_{\mathrm{o}}}\right)^2 = \frac{8}{\pi^2}\left(\frac{R_L}{\omega L_{\mathrm{comb}}}\right)^2 \tag{C.10}$$

I^2_{Cint} over I^2_{o}

Since the capacitive interface is in series with the L_1 inductor, the current that flows through these components is the same. Therefore, the ratio between I^2_{Cint} and I^2_{o}, and between I^2_{L1} and I^2_{o}, are also equal:

$$\left(\frac{I_{\mathrm{Cint,RMS}}}{I_{\mathrm{o}}}\right)^2 = \frac{8}{\pi^2}\left(\frac{R_L}{\omega L_{\mathrm{comb}}}\right)^2 \tag{C.11}$$

I^2_{L2} over I^2_{o}

The current through the L_2 inductor is the unrectified output current, which is calculated using (2.5) as:

$$I_{\mathrm{L2,pk}} = \frac{\pi}{2} I_{\mathrm{o}} \tag{C.12}$$

The ratio between these two currents is therefore:

$$\frac{I_{\mathrm{L2,pk}}}{I_{\mathrm{o}}} = \frac{\pi}{2} \tag{C.13}$$

To use RMS current rather than peak current, equation (C.8) is applied:

$$\frac{I_{\mathrm{L2,RMS}}}{I_{\mathrm{o}}} = \frac{\pi}{2\sqrt{2}} \tag{C.14}$$

Squaring both sides to be consistent with how the terms are expressed in (C.1), this ratio is shown below.

$$\left(\frac{I_{\mathrm{L2,RMS}}}{I_{\mathrm{o}}}\right)^2 = \frac{\pi^2}{8} \tag{C.15}$$

I_{C2}^2 over I_o^2

Performing an analysis similar to the one in Section B.2, the current through C_2 is found to be equal than the current through L_2. Therefore, the ratio between I_{C2} and I_o is the same than the ratio between I_{L2} and I_o:

$$\left(\frac{I_{C2,RMS}}{I_o}\right)^2 = \frac{\pi^2}{8} \tag{C.16}$$

I_{MOS}^2 over I_o^2

The current through a MOSFET of the inverter is a half sinusoid, with magnitude equal to that of I_{L1}:

$$I_{MOS,pk} = I_{L1,pk} \tag{C.17}$$

The RMS value of a half sinusoidal waveform is known to be half the peak value:

$$I_{MOS,RMS} = \frac{I_{L1,pk}}{2} \tag{C.18}$$

Performing a similar analysis to that of the I_{L1}^2 over I_o^2 subsection, the ratio between the current of the MOSFETs and the output current is found to be:

$$\left(\frac{I_{L1,RMS}}{I_o}\right)^2 = \frac{4}{\pi^2}\left(\frac{R_L}{\omega L_{comb}}\right)^2 \tag{C.19}$$

$I_{D,av}$ over I_o^2

The average current flowing through each diode of the bridge rectifier is half the output current:

$$I_{D,av} = \frac{I_o}{2} \tag{C.20}$$

$$\frac{I_{D,av}}{I_o} = \frac{1}{2} \tag{C.21}$$

Since (C.1) requests to have the ratio between $I_{D,av}$ and I_o^2, the previous expression must be divided by I_o:

$$\frac{I_{D,av}}{I_o^2} = \frac{1}{2I_o} \tag{C.22}$$

Replacing I_o with (2.30), this ratio is found to be:

$$\frac{I_{D,av}}{I_o^2} = \frac{\pi^2}{8}\frac{L_{comb}}{V_{DC}} \tag{C.23}$$

C.2 Efficiency calculation

At this point, the efficiency equation of (C.1), can be calculated by replacing the current ratios with the results obtained in the previous section.

$$\eta = \frac{R_{\mathrm{L}}}{R_{\mathrm{L}} + \frac{I_{\mathrm{L1}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,L1}} + \frac{I_{\mathrm{L2}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,L2}} + 2\frac{I_{\mathrm{Cint}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,Cint}} + 2\frac{I_{\mathrm{C2}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,C2}} + 2\frac{I_{\mathrm{MOS}}^2}{I_{\mathrm{o}}^2} R_{\mathrm{eq,MOS}} + 4\frac{I_{\mathrm{D,av}}}{I_{\mathrm{o}}^2} V_{\mathrm{F}}} \tag{C.24}$$

All results are summarized below.

$$\frac{I_{\mathrm{L1}}^2}{I_{\mathrm{o}}^2} = \frac{8}{\pi^2} \left(\frac{R_L}{\omega L_{\mathrm{comb}}} \right)^2 \tag{C.25}$$

$$\frac{I_{\mathrm{L2}}^2}{I_{\mathrm{o}}^2} = \frac{\pi^2}{8} \tag{C.26}$$

$$\frac{I_{\mathrm{Cint}}^2}{I_{\mathrm{o}}^2} = \frac{8}{\pi^2} \left(\frac{R_L}{\omega L_{\mathrm{comb}}} \right)^2 \tag{C.27}$$

$$\frac{I_{\mathrm{C2}}^2}{I_{\mathrm{o}}^2} = \frac{\pi^2}{8} \tag{C.28}$$

$$\frac{I_{\mathrm{MOS}}^2}{I_{\mathrm{o}}^2} = \frac{4}{\pi^2} \left(\frac{R_L}{\omega L_{\mathrm{comb}}} \right)^2 \tag{C.29}$$

$$\frac{I_{\mathrm{D,av}}}{I_{\mathrm{o}}^2} = \frac{\pi^2}{8} \frac{L_{\mathrm{comb}}}{V_{\mathrm{DC}}} \tag{C.30}$$

Replacing equations (C.25) - (C.30) into (C.24), the following expression can be obtained:

$$\eta = \frac{R_{\mathrm{L}}}{\frac{\pi^2}{8} \left(R_{\mathrm{eq,L2}} + 2R_{\mathrm{eq,C2}} + 4V_{\mathrm{F}} \frac{L_{\mathrm{comb}}}{V_{\mathrm{DC}}} \right) + R_{\mathrm{L}} + \frac{8}{(\pi\omega L_{\mathrm{comb}})^2} \left(R_{\mathrm{eq,L1}} + 2R_{\mathrm{eq,Cint}} + R_{\mathrm{eq,MOS}} \right) R_{\mathrm{L}}^2} \tag{C.31}$$

Naming as α all the terms independent of R_{L}, and β all the terms dependent on R_{L}^2, a more synthetic efficiency equation can be obtained:

$$\eta = \frac{R_{\mathrm{L}}}{\alpha + R_{\mathrm{L}} + \beta R_{\mathrm{L}}^2} \tag{C.32}$$

This is the expression reported in (4.32). In this equation, α and β are the following:

$$\alpha = \frac{\pi^2}{8} \left(R_{\mathrm{eq,L2}} + 2R_{\mathrm{eq,C2}} + 4V_{\mathrm{F}} \frac{\omega L_{\mathrm{comb}}}{V_{\mathrm{DC}}} \right) \tag{C.33}$$

$$\beta = \frac{8}{(\pi\omega L_{\mathrm{comb}})^2} \left(R_{\mathrm{eq,L1}} + 2R_{\mathrm{eq,Cint}} + R_{\mathrm{eq,MOS}} \right) \tag{C.34}$$

which are the expressions presented in (4.33) and (4.34), respectively.

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