Master thesis

Fabrication and Analysis of a Planar Junctionless Transistor

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Alla mia famiglia, per avermi sempre sostenuto e motivato, senza la quale non sarei la perona che sono oggi.

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Chapter 1

Motivation

Modern technology requires smaller transistors every year, the pursuit of miniaturization on the current devices has shown several difficulties such as leakage current and short channel effects, mostly due to the necessary formation of abrupt source/drain junctions in the channel. Among the possible candidates, junctionless transistors offer an interesting solution for these issues.

This project aims to analyze the working principles of a junctionless transistor and to provide a fabrication procedure that allows to obtain a similar device in the USN's MEMS laboratory.
This work is part of a broader project, which aims to define and analyze how the junctionless transistor could become in the future the driving technology in electronics. Last year, the project focused mainly on the definition of theoretical tools for the analysis and simulation of these devices (definition of the working properties). This project is focused on the fabrication and optimization of a possible device. These improvements have allowed to obtain a fabrication procedure that significantly reduced the cost of fabrication in terms of necessary resources and machinery for production.

Chapter 2

State of the Art

The junctionless transistor (JLT) was invented by J.E. Lilienfeld in 1925, it's a voltage controlled nonlinear resistor where the mobile carrier density can be modulated by the gate (also called gated resistor) and is characterized by a lack of junctions and doping concentration gradients [1]. The key to fabricating a junctionless gated resistor is the deposition of a semiconductor layer thin and narrow enough to allow for full depletion of carriers when the device is turned off [2]. The semiconductor must be heavily doped to allow current flow when the device is turned on [1]. Due to the technological limitations of that era, it took over 80 years for this device to be produced and tested.

JLT categories can be then classified based on the geometrical shape, material composition of the channel, as well as the gate structure [2].

The electrical characteristics are similar to those of a MOSFET, although the physics are quite different.

The advantages of a junction-free structure are numerous, such as the absence of doping concentration gradients [3], and the absence of junction leakage [4]. In addition, the required junction fabrication technology is less demanding, hence cheaper to produce.

Jean-Pierre Colinge and colleagues at the Tyndall National Institute University College of Cork were the first team that in 2010 was able to realize the first JLT. Their belief in the potential future development of this device is what motivated their work.

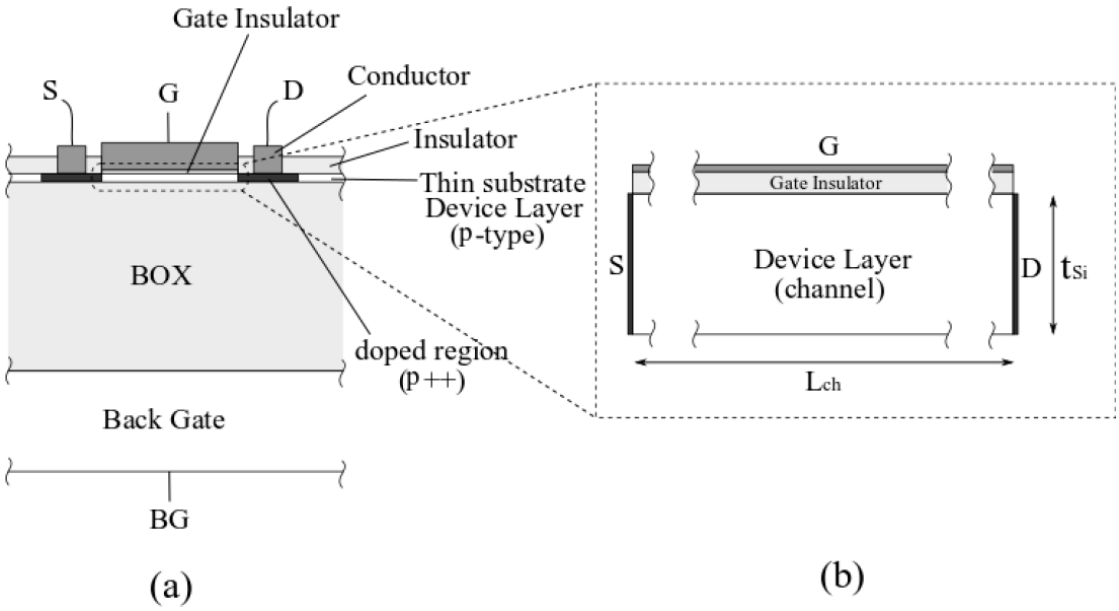

Figure 2.1: Junctionless transistor physical structure [5]

Fig 2.1, which has been extracted from [5] shows a theoretical overview of a planar junctionless transistor.

As can be observed in figure 2.1 the actual device is built on top of an SOI wafer (Silicon on insulator). These wafers are quite expensive (from 500 $ up), and since most of the university laboratories do not possess the machinery necessary for the fabrication of this silicon support, they have to be ordered from external companies.
SOI wafers are obtained from a silicon substrate where a silicon dioxide layer (insulating layer) is obtained from SIMOX, an oxidation technique that uses an oxygen ion beam implantation process followed by high-temperature annealing to create a buried silicon dioxide layer. A secondary Si layer is bonded on top of the oxygen rich layer employing either Smart cut or Nanocleave, which are wafer bonding techniques. SIMOX, Smart cut and Nanocleave require application specific tools, which are quite expensive and aren't normally found in common laboratories, making the price of this type of wafers higher compared to others.

Both the incapability of producing these wafers autonomously and the cost of the commercial ones are limitations for a fabrication procedure.
A possible solution could be to define a device that works as a junctionless transistor but does not require an SOI wafer. A good candidate, which can solve these fabrication challenges is the thin-film transistors.

A Thin film Transistor (TFT), fig. 2.2, operates similarly to a MOSFET as well as a JLT, it is obtained by depositing thin films of semiconductors, dielectrics, and ultimately the electrodes on top of a non conductive substrate (fig. 2.2). The first TFT was successfully produced in 1962 at RCA by Paul K. Weimer, the device was a follow up of the first ever MOSFET, which was developed in 1959 by Mohamed M. Atalla and Dawon Kahng at Bell Labs [6].

TFT can be built either on a silicon substrate or on top of a transparent non conductive layer such as glass. TFTs built on top of glass substrates are employed for the realization of LED TVs where they operate as the controllers for the pixels, which is the reason why they are usually referred to as "active matrix TFTs" [7]. The first commercial TFT-based AM LCD product was the 2.1-inch Epson ET-10 (Epson Elf), the first color LCD pocket TV, released in 1984.

Unlike the JLT, this model does not necessarily require the use of an FD-SOI wafer (full depletion silicon on insulator wafer) for the realization of the device. Hence, it is possible to obtain the thin film active layer using a deposition technique (sputtering, spin coating...) on a substrate, simplifying the production of the device. This characteristic makes the TFT particularly interesting for the means of this project.

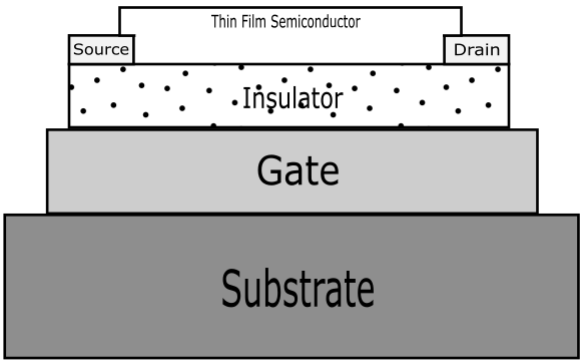

Figure 2.2: Generic Thin film transistor structure. The substrate material depends on the purpose of the device and could be either made of an insulating layer or a transparent conductive oxide (TCO)

Among other materials, Tin Dioxide is employed for the fabrication of the conductive layer in TFTs, and in recent years several papers have been written reporting on its characteristics and behaviour. These papers regard depletion-mode devices (devices which require the application of a gate voltage to turn them off),

and enhancement-mode operation devices (where a gate voltage must be applied to drive the transistor into operation [8]) [3], [9], [10] . These Tin Dioxide layers are obtained through sputtering or spin coating of solutions obtained by sol-gel procedures. Some devices examples are present in fig.2.3a and 2.3b

(a) **(b)**

Figure 2.3: SnO_2 thin film transistors [3],[9]

The transistor plotted in fig. 2.3a is very interesting because the obtained Tin Dioxide active layer is $20nm$ thick (similar dimensions to the ones employed in this project). The deposition procedure was conducted by the same researchers who wrote the article, removing the necessity to order it from an external company (clearly the right machinery must be available).
Regarding the electrical behavior of the device fig. 2.4 shows the output characteristic curve of a TFT (I_d vs V_{ds}). The I_d output resembles the one of a MOSFET device.

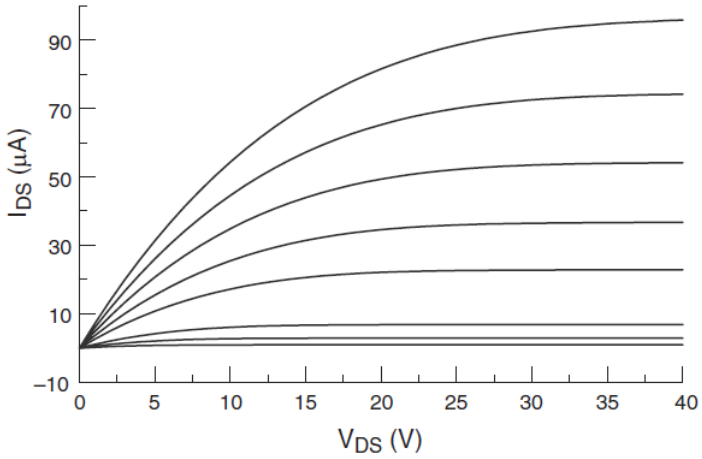

Figure 2.4: Drain current in the TFT reviewed in [3] (fig. 2.3a). V_{GS} is decreased from 40 (top curve, showing maximum current) to 0V in 5V steps.

The main idea of the project is to combine the characteristics of JLTs and TFTs to obtain a junction free device, with the advantages that have been explained. A review of the available literature regarding TFTs, and specifically the use of SnO2 in TFTs, highlighted that this technology is among the most promising to fulfill the requirements of this project. In the next chapter the working principle of the device is introduced. An explanation of how tin dioxide behaves when employed as a semiconductor, and some feasible deposition techniques that could be employed are also presented.

Chapter 3

Background

3.1 Planar Junctionless transistor working principle

A junctionless transistor works differently with respect to inversion mode devices [3]. Figure 3.1 shows the structure of a JLT built on a Silicon on insulator wafer (SOI):

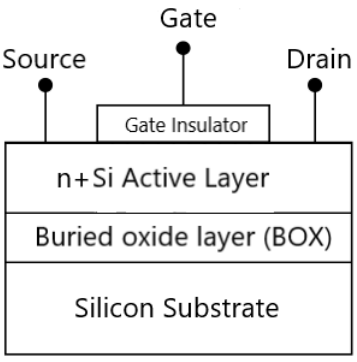

Figure 3.1: Junctionless transistor built using a silicon on insulator wafer

figure 3.2 instead shows the working principle of the n-type junctionless transistor presented in fig. 3.1. As can be observed, the gate voltage defines the different operating regions for the device.
Whenever $|V_g| < V_{th}$ (V_{th} is the threshold voltage), the depletion layer extends throughout the device active layer, blocking any conductive path between source and drain. This is known as the "OFF state" 3.2.(a).

By changing the gate voltage toward more positive values, the depletion layer will start to reduce due to the attraction of the majority carriers toward the gate contact, creating a path between the source and drain electrodes to allow a current flow 3.2.(b).

When $|V_g| > V_{FB}$ (V_{FB} is the flat band voltage) attraction of the electrons underneath the gate forms an "accumulation layer", extinguishing the depletion layer and allowing the maximum flow of current in the device 3.2.(c).

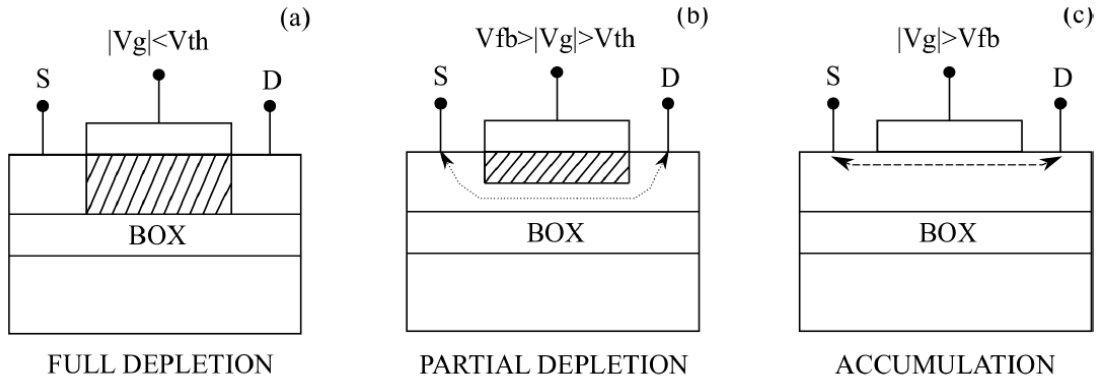

Figure 3.2: n doped channel junctionless transistor working principle: (a) Full Depletion; (b) partial depletion(bulk conduction); (c) Accumulation (surface conduction) [5]

Figure 3.3 shows an n-channel JLT giving an even better understanding of how the electron concentration is modulated in a PJLT by controlling the gate voltage [1].

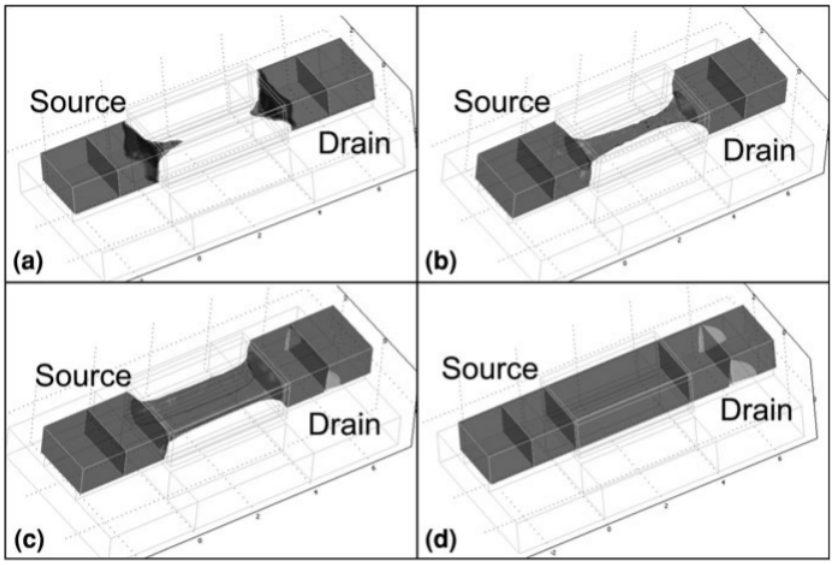

Figure 3.3: Electron concentration in a n-type JLT. The dark areas represent regions with high electron concentration: (a) $V_g < V_{th}$; (b)$V_g = V_{th}$; (c)$V_g > V_{th}$; (d)$V_g = V_{FB} >> V_{th}$; [1] as the gate voltage is increased toward the flat band voltage the electrons are attracted toward the gate area, creating an accumulation layer and allowing a current to flow through
;

3.2 Thin Film Transistors working principle

The operation of the SnO_2 TFT is based upon the control of majority carriers in a wide-band-gap semiconductor by means of an insulated control gate. [6]
Conduction is possible only when the applied gate voltage is greater than the threshold voltage. When the transistor is working in the saturation region ($V_{gs} > V_{th}$) the drain current is equal to [11]:

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{3.1}$$

Where:

- μ = carrier mobility $[cm^2/(V \cdot s))$;
- W = gate width;
- C_{ox} = gate oxide capacitance per unit area;

- L = gate length;
- V_{GS} = gate-source voltage;
- V_{th} = threshold voltage;

Figure 3.4 shows the voltage-current plot of the TFT that Paul K. Weimer used to present the electrical properties of this technology to the scientific community. A TFT fabricated with a microcrystalline layer of cadmium sulfide as active layer, gold for the source-drain and gate electrodes and silicon monoxide for the insulating layer.

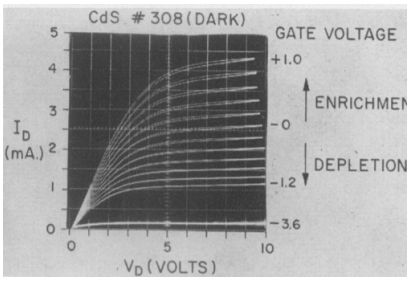

Figure 3.4: I-V curve of Weimer TFT, [6].

In the past 10 years, thin-film transistors have been improved drastically performance-wise, although they still aren't able to compare with normal MOSFETs in terms of mobility and current output [12]. Figure 3.5 shows the structural differences between a Mosfet and a TFT.

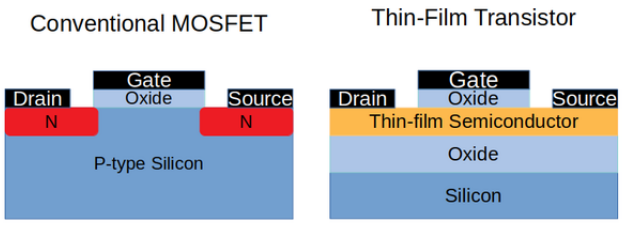

Figure 3.5: Comparison between the structures of a MOSFET and a TFT [13].

3.3 Depletion region

To correctly command a PJLT it is very important to be able to switch it on and off using the gate electric potential. Switching the gate voltage above and beneath the threshold voltage allows to 'open' or 'close' a conductive path between the source and drain, defining the ON and OFF states. This is because for $|V_g| < V_{th}$ the active layer will be completely depleted, meaning that no free carriers will be able to partake in any conduction. On the other hand, when $|V_g| > V_{FB}$ the channel of the transistor becomes fully conductive. It is very important to determine the values of these voltages to correctly control the transistor behavior.

To evaluate these voltages the most significant parameters are the layer thickness, the doping concentration, and the dielectric constant of the material.

By definition, total depletion is achieved when the depletion region width X_{dep} (which can be obtained using equation 3.2) is wider than the actual channel thickness.

$$X_{dep} = \sqrt{\frac{4\varepsilon\phi_{n,p}}{qN_{D,A}}} \tag{3.2}$$

where:

- $q = 1.602 \cdot 10^{19}\ (C)$ is the elementary electric charge;
- $\varepsilon = (F/cm)$ dielectric constant ;
- $\varepsilon_0 = 8.854 \cdot 10^{-14}\ (F/cm)$ vacuum permittivity;
- $N_{D,A}\,(atoms/cm^3)$ is the device layer donor/acceptor concentration;
- $q\phi_{n,p} = k_B T \cdot ln(N_{d,a}/n_i))$ (eV) is the n-type/p-type Fermi potential;
- $k_B = 8.6173303 \cdot 10^{-5}$(eV/K) is the Boltzmann constant;
- T = 293.15 (K) is the temperature;
- $n_i = 5.29 \cdot 10^{19}(atoms/cm^3)$ is the intrinsic carrier concentration for Silicon ;

This equation can be used in Matlab to obtain a theoretical evaluation of the recommended active layer thickness, as a function of the device layer material. Fig. 3.6 shows the relation between the layer doping concentration and the maximum obtainable depletion region. To ensure full control over the device, the active layer thickness must be thinner than the maximum depletion region width. For instance, for a doping concentration $N_D = 4.8 \cdot 10^{18}\ cm^{-3}$ the X_{dep} is evaluated to be $27nm$,

hence the active layer thickness should be thinner than this value to ensure full depletion.

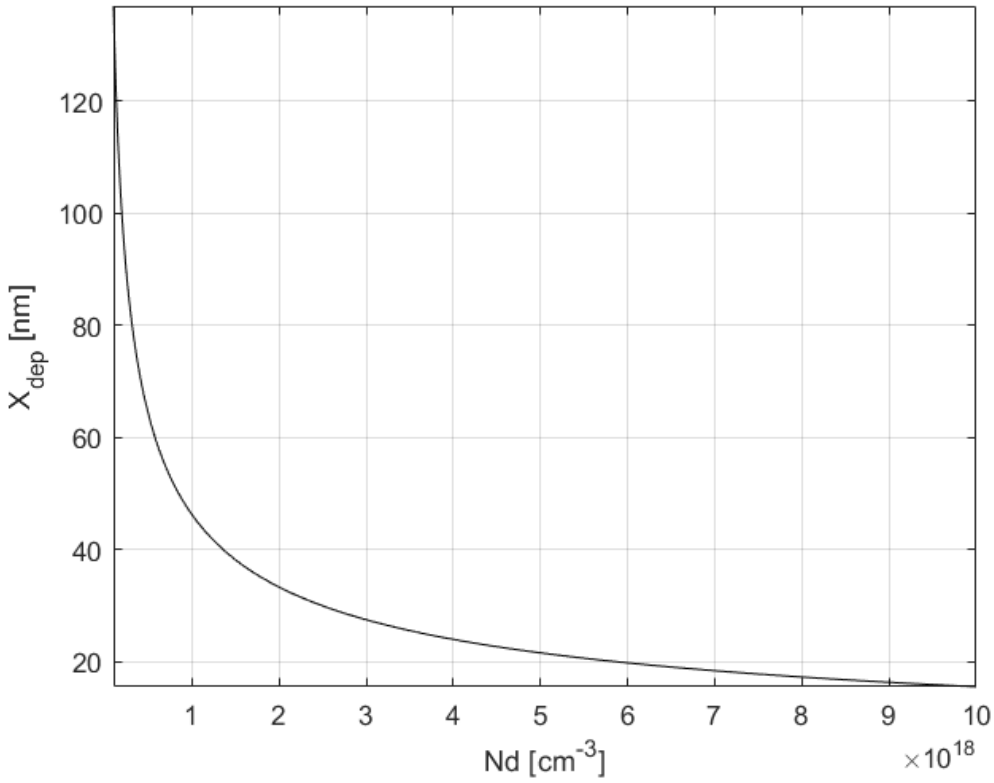

Figure 3.6: plot of the equation 3.2, depletion region vs. dopant concentration.

The choice of the material that will be used for the conductive layer therefore is very important, as well as the type and the amount of doping that will be implanted.

3.4 Gate voltage

The use of different materials for the gate electrode will directly influence the driving voltages, since both the flatband and threshold voltage are directly dependent on the gate material's workfunction [14]. The following equations are used for the evaluation of the flatband voltage when the semiconductor is n-doped (3.3) or p-doped (3.4).

$$V_{FB,n} = q\phi_M - q\phi_{s,n} = q\phi_M - (q\chi + E_g/2 - q\phi_n) \tag{3.3}$$

$$V_{FB,p} = q\phi_M - q\phi_{s,p} = q\phi_M - (q\chi + E_g/2 + q\phi_p) \tag{3.4}$$

The flat band voltage is also dependent on the type of doping of the active layer. The same goes for the threshold voltage, V_{th} is computed through equations 3.5 and 3.6 (once again based on the doping type), by forcing the depletion region to be as wide as the channel thickness $X_{dep} = T_{SnO_2}$:

$$V_{th,n} = V_{FB} + \frac{|q|N_d}{2\varepsilon_{SnO_2}}[\frac{\varepsilon_{SnO_2}^2}{C_{OX}^2} - (t_{SnO_2} + \frac{\varepsilon_{SnO_2}}{C_{OX}})^2] \tag{3.5}$$

$$V_{th,p} = V_{FB} - \frac{|q|N_a}{2\varepsilon_{SnO_2}}[\frac{\varepsilon_{SnO_2}^2}{C_{OX}^2} - (t_{SnO_2} + \frac{\varepsilon_{SnO_2}}{C_{OX}})^2] \tag{3.6}$$

As will be better explained in the next section, the active layer used in this project (SnO_2) behaves like an n-type semiconductor. The set of equations for this device are the ones in eq. 3.7.

$$\begin{cases} V_{G_{ON}} = V_{FB} \\ \\ V_{G_{OFF}} = V_{th} = V_{FB} + \frac{|q|N_d}{2\varepsilon_{SnO_2}}[\frac{\varepsilon_{SnO_2}^2}{C_{OX}^2} - (t_{SnO_2} + \frac{\varepsilon_{SnO_2}}{C_{OX}})^2] \end{cases} \tag{3.7}$$

the equations are influenced by the gate material, the active layer material and the insulating layer as well.

3.5 Tin Dioxide

Tin dioxide (SnO_2) is characterized by intrinsic transparency and wide bandgap, which averages between 3.6 to 4.3 eV [15]. It exhibits a tetragonal rutile form in his bulk form (Cassiterite), although when deposited through sputtering it can become either amorphous or polycrystalline. The reason behind its intrinsic doped behavior, is due to the impossibility of depositing perfectly stoichiometric SnO_2. As a result, the obtained layer shows high carrier concentration ($10^{18} - 10^{21} \quad cm^{-3}$) [16] [17] and high conductivity, as a doped semiconductor would. This behavior can be the effect of oxygen vacancies, or tin interstitial atoms in SnO_2, that produce shallow donor or impurity states located close to the conduction band [18].

Among other properties SnO_2 is a TCO, a transparent conductive oxide such as TiO_2. Their high optical transmission in the visible range, the infrared reflection, transparent thermal barrier component, and good chemical stability [19] have made these materials widely used in solar cells and thin-film transistors.
The electrical properties of TCO materials vary from isolating behavior to a metallic conductivity. Stoichiometric oxides are usually insulators. Under oxygen-deficient conditions the oxides obtain free electrons, each oxygen vacancy results in two free electrons in the conduction band. A further increase in conductivity is accomplished by doping [20].

3.5.1 Crystallography

Tin dioxide (SnO_2), also known as as stannic oxide, has a tetragonal rutile structure (fig. 3.7), which takes its name from Cassiterite. The unit cell possesses a space-group symmetry of $P4_2/mnm$ and the lattice constants a = b = 4.7374 Å and c = 3.1864 Å [15] [21]. For stoichiometric SnO2 a unit cell consists of six atoms: two six-fold coordinated tin and four three-fold coordinated oxygen ions with the oxidation states +4 (Sn^{4+}) and -2 ($O2^{-}$), respectively [15] [22]. The cations (Sn^{4+}) are located at the corners (0,0,0) and the centre $(1/2, 1/2, 1/2)$ of the unit cell, the anions (O^{2-}) at $(x, x,0)$ and ś$(1/2 + x, 1/2 - x,1/2)$ with $x = 0.307$ [23].

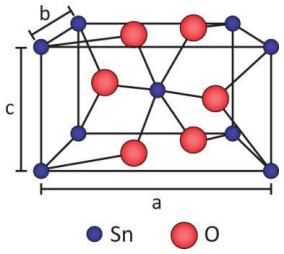

Figure 3.7: SnO2 rutile structure, [21] . Each tin atom (blue) is coordinated by six oxygen atoms (red). Each oxygen atom is coordinated by three tin atoms [22].

When SnO_2 is deposited through evaporation or sputtering ('reconstruction' processes) commonly, a non-stoichiometric structure will be obtained. Normally surfaced with Sn^{+4} will end up reduced to Sn^{+2} [24]. This particular variation is associated with a workfunction lowering, and an increase in the free charge carriers. Several studies have pointed out how the energetic reconstruction of the SnO_2 on the (110) and (101) phases results in the formation of surface oxygen vacancies [24]. Missing oxygen atoms in a compound are called oxygen vacancies. Normally an oxygen atom would require two electrons to complete its octet, but when an oxygen atom is missing from the structure, those two electrons are 'free', resulting in a higher density of electrons as free charge carriers (eq. 3.8). This is the same effect obtained with doping in conventional semiconductors.

$$O_O^X \rightarrow V_O^{**} + 2e^{'} + \frac{1}{2}O_{2(g)} \tag{3.8}$$

XPS analysis shows a correlation between the calcination temperature (calcination is the action of heating a material with high temperatures in high oxygen condition) on the SnO_2 and the presence of oxygen vacancies in the final structure.

The change with calcination temperature and correspondingly particle size, in the Oxygen 1s peak, has been investigated in [24]. By increasing the calcination temperature the material nano-particles tend growing, reducing the number of oxygen vacancies in the lattice, and hence reducing the number of free carriers in the deposited layer, the material shows a more stoichiometric behavior [24].

This dependency can be used to modulate the 'doping' of the SnO_2 layer when used as an active layer in thin-film transistors, for instance.

3.5.2 Electrical Properties

The electrical properties of Tin dioxide layers depend on the stoichiometric deviation (SnO_{2-x}) and on the crystalline structure (polycrystalline, amorphous) [25]. These parameters are dependent on the deposition technique (chemical vapor deposition (CVD), sputtering, sol-gel process or spray pyrolysis), and the deposition parameters. For this device, RF magnetron sputtering was chosen to deposit the SnO_2, allowing to obtain good control over the deposition parameters, high deposition rate, good reproducibility, and the possibility of using commercially available large-area sputtering systems[16] [18]. This procedure allows to control the free carrier concentration of the deposited layer by switching the Argon and Oxygen partial pressures during the deposition, as well as modulating the material's mobility and resistivity.

3.6 Magnetron sputtering deposition

Sputtering describes the physical phenomenon of bombarding a solid material target with particles of plasma or gas, allowing the ejection of particles from the material. This phenomenon is employed in the deposition of material layers, which allows the creation of electronic devices such as semiconductor devices and nanotechnologies. The sputtering deposition is acknowledged as a physical vapor deposition technique (PVD) and was first developed in 1920 from Langmuir.

The process requires the formation of plasma using an electric field, which results in the formation of ionized charges, usually from Argon. The ionized charges are then drove and accelerated with the same electric field to the negatively charged target (cathode). If said ions yield enough energy on impact, microparticles of the target material will detach and deposit on a chosen substrate (anode). The impact of the ions on the target will also release electrons, which will help to keep the plasma in the chamber. The chamber must have been evacuated prior to the sputtering process to an ultra-high vacuum condition to grant a pure coating process.

Figure 3.8: AJA Sputtering machine [26]

Fig.3.8 shows a Sputtering machine. The machine is mainly composed of three parts. The 'main' chamber, whose insides are shown in figure 3.9, where the sputtering takes place. The secondary chamber, used to insert and remove the wafer without negatively influencing the atmosphere inside the main. And then the control panel where the entire process and parameters are controlled.

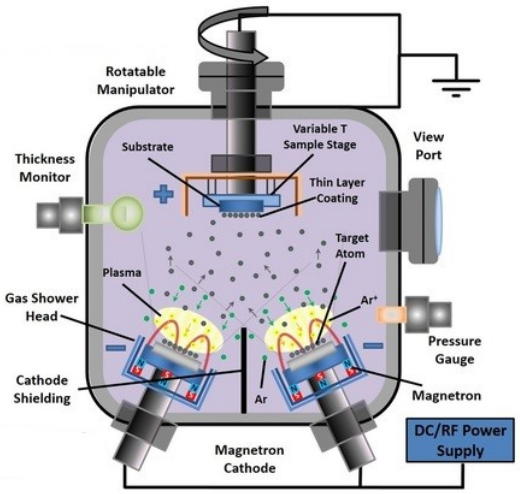

Figure 3.9: Schematic of the main chamber during operation [27]

The properties of the deposited material depend on the energy that the particles have when they reach the substrate along with other parameters. The quality of the deposited layer is controlled through five main parameters, which are:

- Working pressure in the chamber;
- Temperature on the substrate crucible;
- Argon flow in the chamber;
- Target to substrate distance;
- Sputtering power and type (radiofrequency or direct current powered);

Magnetron sputtering deposition uses a closed magnetic field to trap electrons. This allows to enhance the efficiency of the initial ionization process and allows

plasma to be generated at lower pressures. As a consequence, background gas incorporation in the growing film is reduced, as well as energy losses in the sputtered atom through gas collisions. Moreover, it allows through the magnetic field to focus the secondary freed electrons in a region close to the target (cathode), increasing the rate of ions that partake in the bombardment.

There are two different types of magnetron sputtering:

- **DC magnetron sputtering**, as the name suggests DC power is employed, it is used mainly for the deposition of metals or conductive materials in general, this procedure is ineffective with dielectric materials.
- **RF magnetron sputtering** alternates the electrical potential of the current in the vacuum environment at RF. Differently than for DC, in RF sputtering magnets are used behind the cathode (on top of which the target is positioned) to attract electrons, in order to speed up the procedure. The problem is that positive ions will be attracted toward the target, and this charge build up could at some point stop the sputtering of the target atoms. By alternating the electrical potential with RF Sputtering, the target material can be cleaned of said charges [28].

Dc magnetron sputtering is generally preferred for the deposition of the metals, whilst RF is more broadly used for the deposition of semiconductors and insulating layers.

A possible procedure for RF magnetron sputtering is presented in table 5.4 where the deposition parameters used for the deposition of the Tin Dioxide in this project are presented.

3.7 Sol-Gel synthesis

As pointed out in the previous section RF Magnetron sputtering allows to obtain thin films of tin dioxide and control the deposition technique using simple input parameters. None the less, sputtering machines are very expensive and not every laboratory has one, and even when they do the cost of targets can be prohibitive. A possible solution could be the use of different synthesis procedures to obtain the wanted material, followed by a deposition technique that does not require the use of a sputtering machine. A possible process for the production of tin dioxide is the sol-gel procedure, which especially nowadays is gaining more and more attention. The sol-gel procedure allows to obtain high purity and homogeneous films, based on the hydrolysis and polycondensation of metal-organic precursors, such as metal alkoxides [29]. Sol-gel requires low temperature of processing and simple and cheap technological equipment, which still ensure a good homogeneity at the molecular level in the solution, which results in good control over the coating of large substrates.
The sol-gel process also offers a versatile method for the preparation of optical quality films with controlled refractive indices and small thicknesses, allowing a nanoscale control of the film structure [29].
Generally speaking, the deposition of the gel is obtained using either:

- **Spin coating** deposition of a thin film on a flat surface, the solution is positioned on top of the sample, which is then spun with a spinner in order to uniformly spread the solution across the substrate.
- **Dip coating** immersing of a substrate into a tank containing coating material allowing for the formation of a layer on top of the substrate.

To better understand how the production through sol-gel and the deposition using spin coating work, a fabrication procedure for a tin dioxide thin film is presented [30]:

- Tin (II) chloride dihydrate ($SnCl_2 2H_2O$), the precursor, is dissolved in ethanol.
- stirring for 10 minutes.
- spin-coating at 3000 rpm for 50 s.
- drying for 10 minutes at 150 °C in air using a hot plate.
- (optional) annealing to tune the electrical properties of the obtained SnO_2 thin film.

The procedure is very easy and cheap, especially when compared to sputtering. On the other hand the deposition rate of the tin dioxide is less controllable when using spin coating, and its even worse when considering dip coating (spin coating is still preferable to dip coating since it allows to have more control over the layer's thickness).

Chapter 4

Proposed Device

4.1 Proposed Structure

In this chapter, an optimized structure for the planar junctionless transistor is presented, explaining how the device structure has been simplified allowing for an easier fabrication procedure. The initial structure presented in fig. 2.1 shows the design of the planar junctionless transistor developed in [5]. Being this project a follow up of the work developed by Arian Nowbahari in [5] the proposed device has been taken as a reference for the design of the PJLT.

The most significant difference is the decision not to build the device using a FDSOI wafer. Instead, the active layer will be deposited on top of a insulation layer obtained on a regular Si wafer. This choice allows to lower production costs and to obtain more freedom in the tuning of the device performances.
Other optimizations that have been implemented regard:

- Use of a Semiconductor material sufficiently doped to avoid the formation of rectifying junctions.
- Definition of the best process for the deposition of the active layer without using an FDSOI wafer.
- Use of the same metal for the deposition of all three electrodes to further simplify the fabrication procedure and the required masks.

Fig. 4.1 portrays the proposed structure for this project.

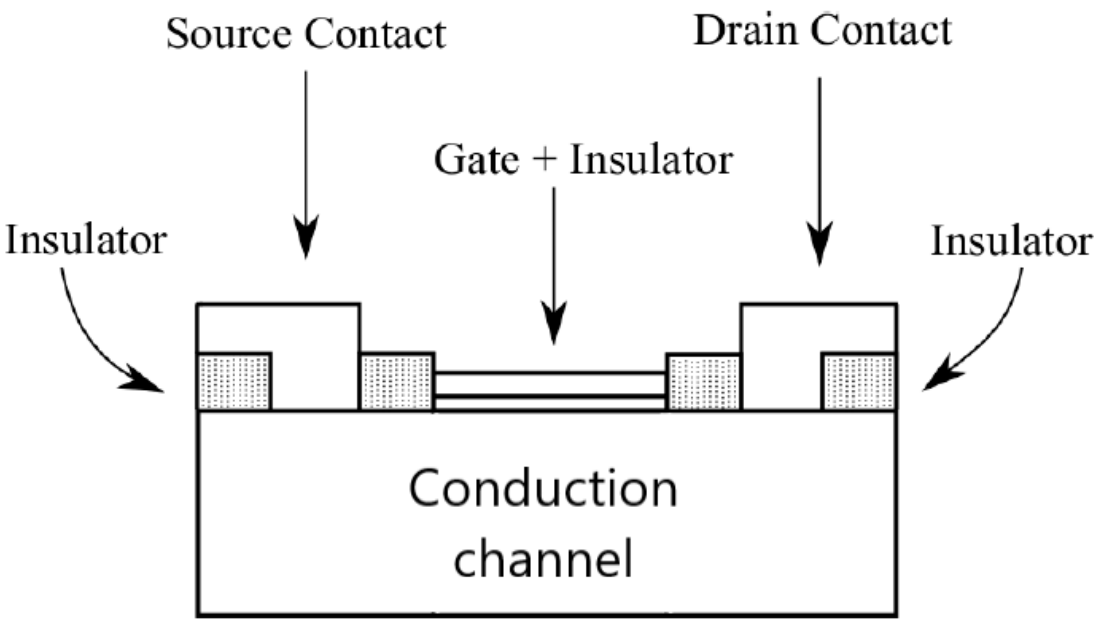

Figure 4.1: Generic structural overview of the proposed Planar Junctionless Transistor

This structure allows to simplify the entire process to a minimum. In the next paragraph, the fabrication process is showed to understand in detail how the transistor is built from the ground up, allowing the reader to better navigate the following paragraphs where the various procedures are explained.

4.2 Fabrication process flow

The substrate is a Silicon wafer with a $600nm$ thick Silicon Dioxide layer deposited using magnetron sputtering (the drawings are not in scale).

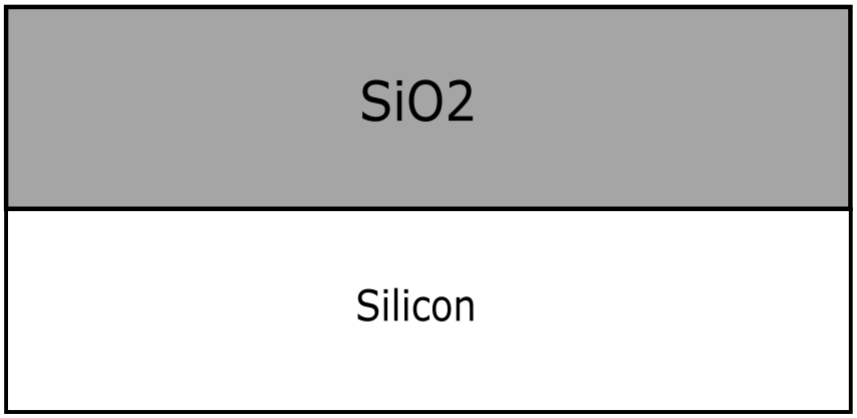

Figure 4.2: substrate

The first step requires the deposition of the Tin dioxide active layer on top of the SiO_2 substrate (the Silicon substrate from now on is being omitted from the figures for a matter of practicality)

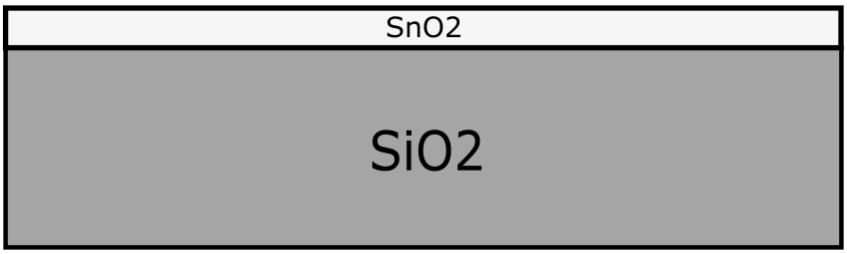

Figure 4.3: Step 1: Tin Dioxide deposition

The second step is the spinning of the photoresist (PR).

Figure 4.4: Step 2: Photoresist deposition

Mask 0 (fig.4.15) is positioned over the PR, which is then exposed to a UV light to define the patterning areas.

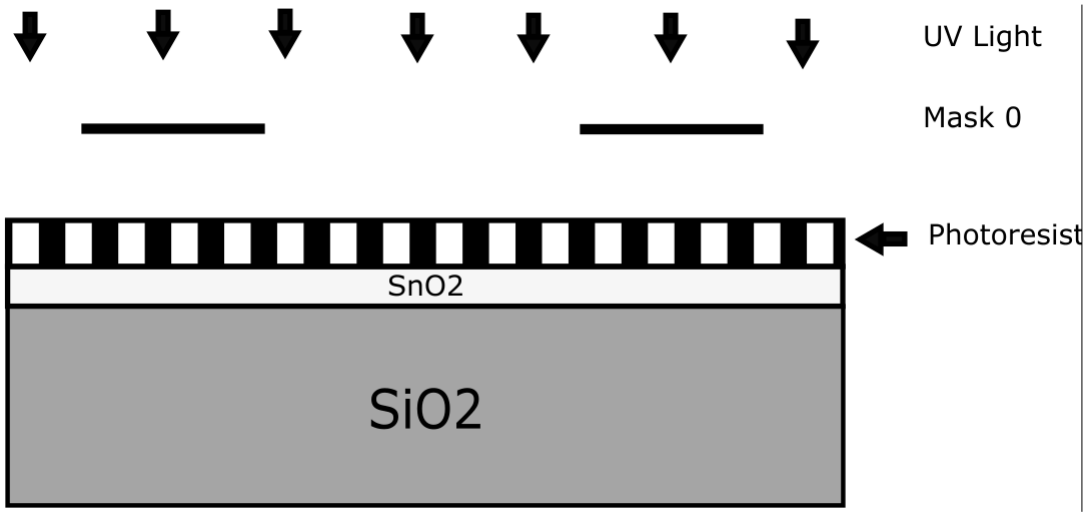

Figure 4.5: Step 3: Photoresist exposure to UV light through mask 0

Now the unnecessary photoresist can be removed leaving the correct patterning.
.

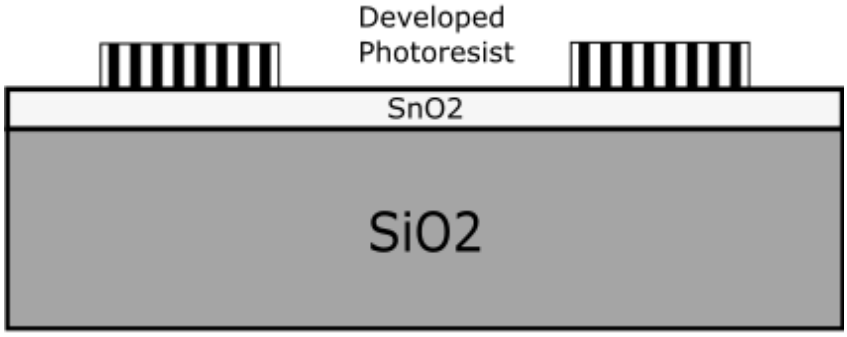

Figure 4.6: Step 4: Photoresist development, mask 0

Silicon Dioxide is then deposited on top of the Tin Dioxide and developed photoresist.

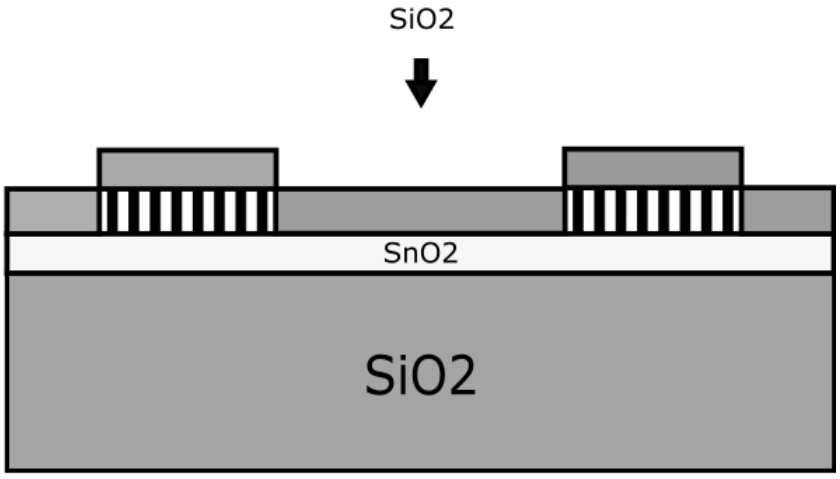

Figure 4.7: Step 5: Silicon Dioxide deposition

The sacrificial layer (developed PR) is removed to leave the wanted SiO_2 patterning.

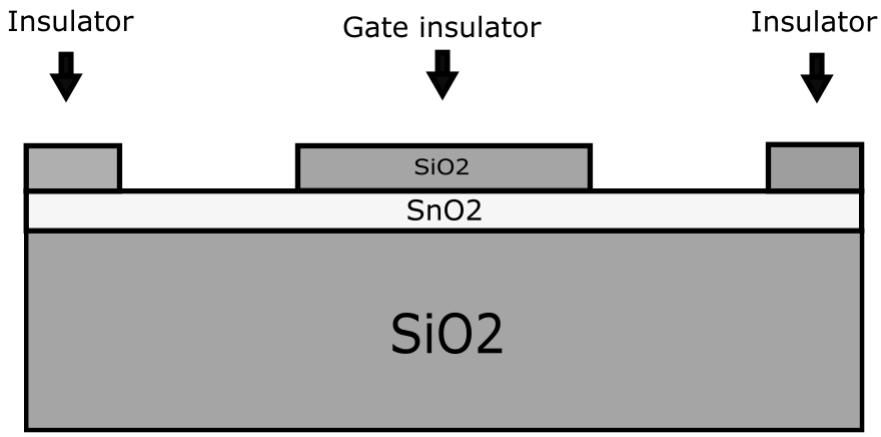

Figure 4.8: Step 6: Sacrificial layer etching

The photoresist is spun again on top of the structure.

Figure 4.9: Step 7: Photoresist deposition

Exposure of the photoresist using mask 1 (fig. 4.17).

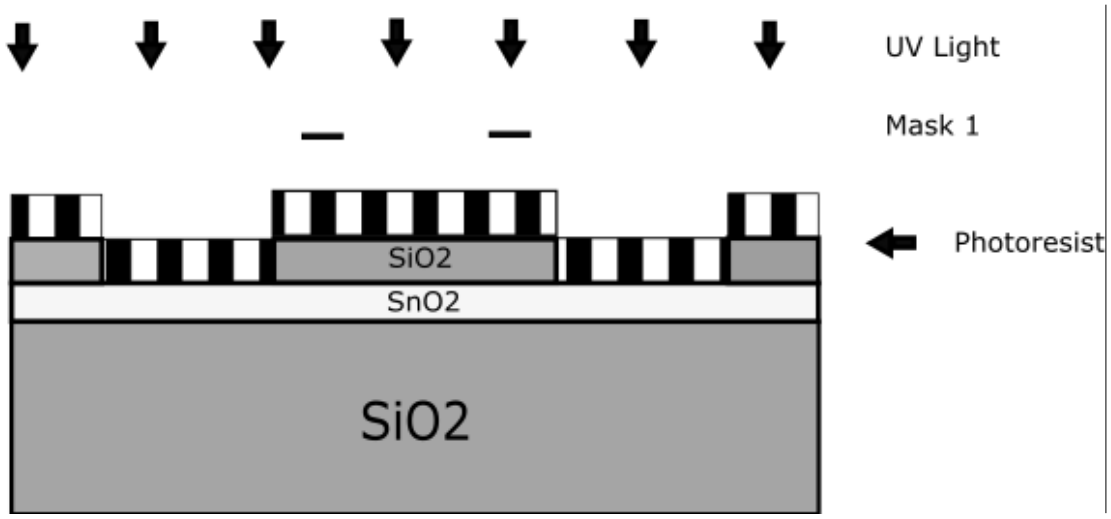

Figure 4.10: Step 8: Photoresist development, mask 1

Photoresist development, the photoresist is now positioned in the only spots where Aluminum is not needed.

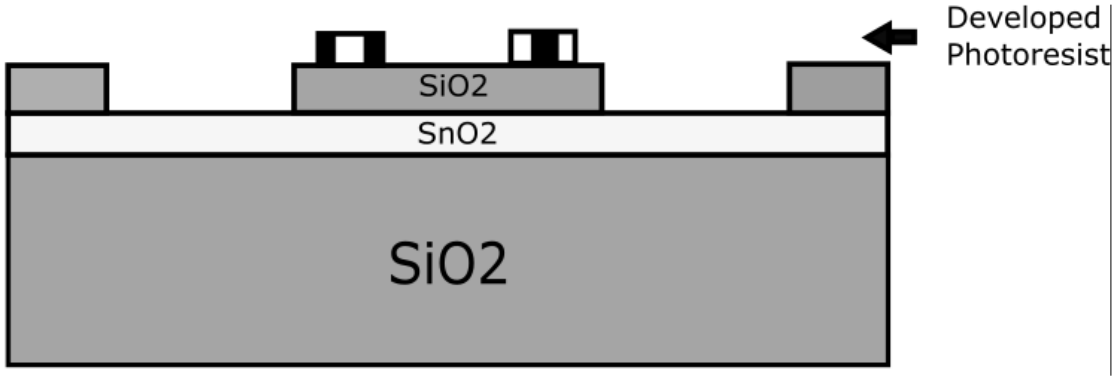

Figure 4.11: Step 9: Developed photoresist, sacrificial layer

Aluminum is sputtered on top of the wafer.

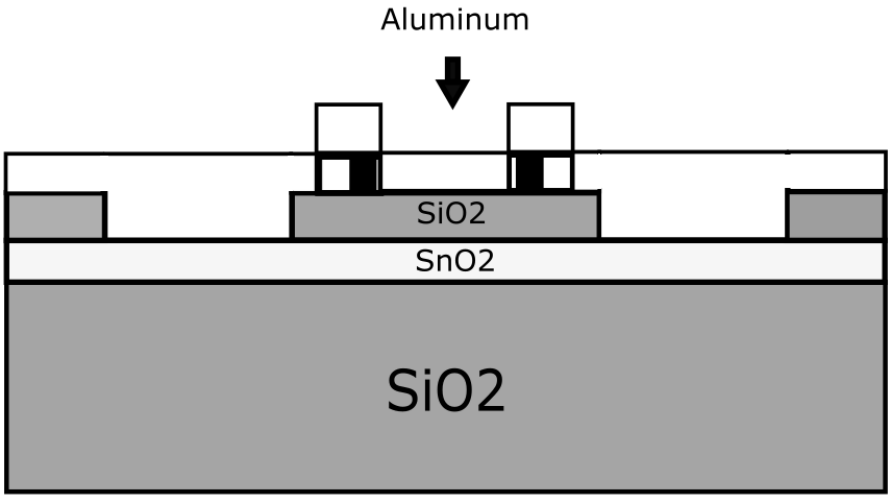

Figure 4.12: Step 10: Aluminum deposition

Photoresist lift off.

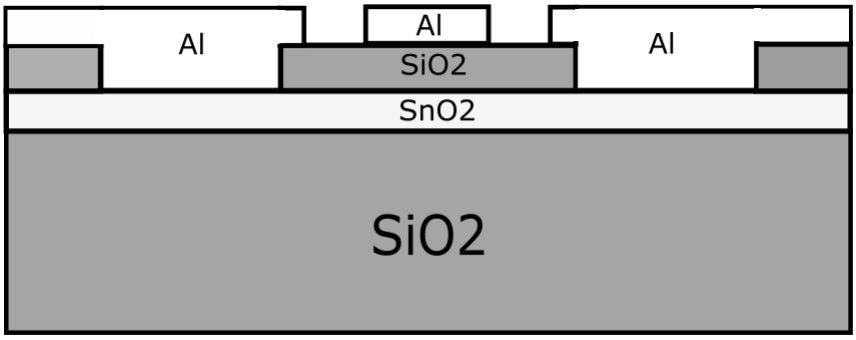

Figure 4.13: Step 11: Lift off

Fig. 4.13 shows the two-dimensional final structure of the PJLT, in total eleven steps are necessary for the fabrications of the entire structure (twelve, counting the deposition of the oxide layer on top of the Si wafer).

4.3 Masks

The patterning of the photoresist is obtained by exposing the sensitive layer to a strong UV light through a mask so that only certain areas are exposed.
A positive photoresist will be used for the fabrication. This implies that the masks should cover the photoresist from the UV light during exposure in the areas where the PR has to remain.

The number of masks necessary for the realization of the device have been reduced to a minimum, making only two masks necessary throughout the entire fabrication procedure.

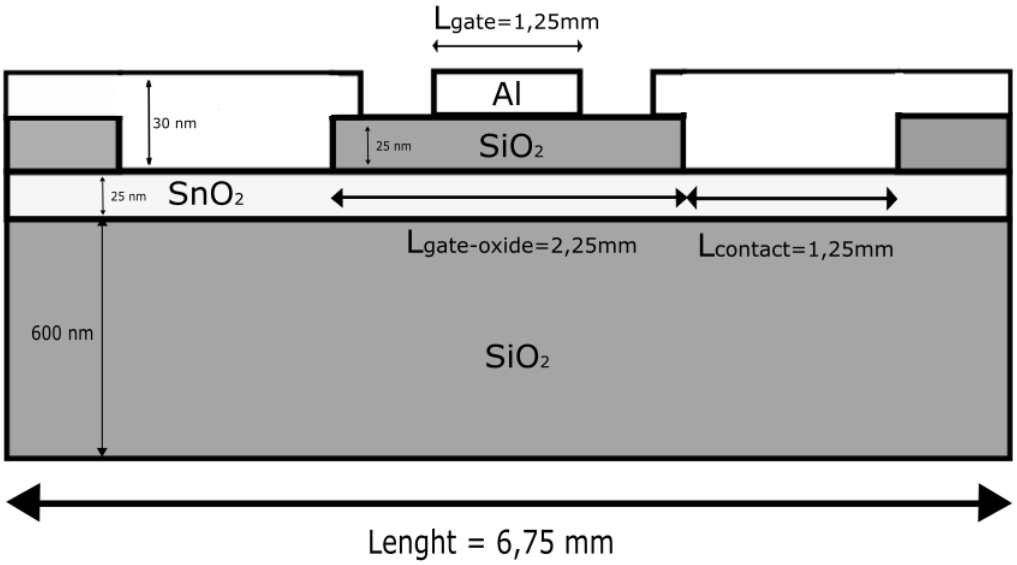

Figure 4.14: Physical dimensions for the device

Fig. 4.14 shows the physical dimensions of the final device, the only parameter missing in the image is the transistor width W = 2,65 mm . The width does not include the surrounding insulating layer necessary to isolate the transistors from one another.

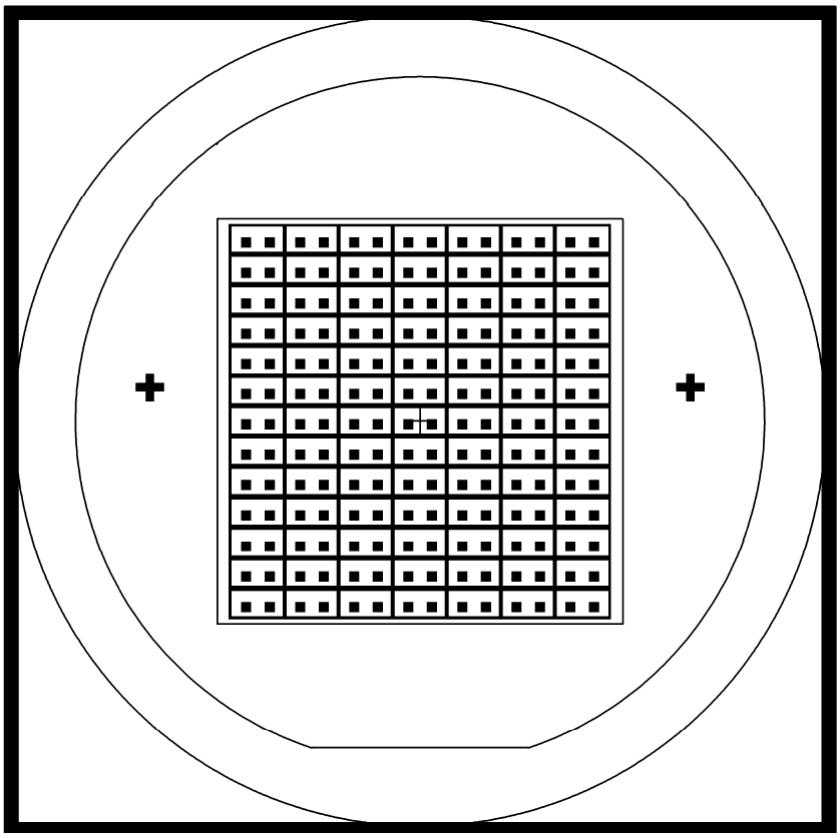

Figure 4.15: Mask 0 for SiO_2 patterning

Fig. 4.15 portraits mask 0, which is used for the patterning of the Silicon Dioxide, to obtain the openings in the insulating layer and to define the area of each transistor.

In this design 91 transistors are being defined for each wafer, the unit cell is showed in fig. 4.16 along with the chosen dimensions for the device structure.

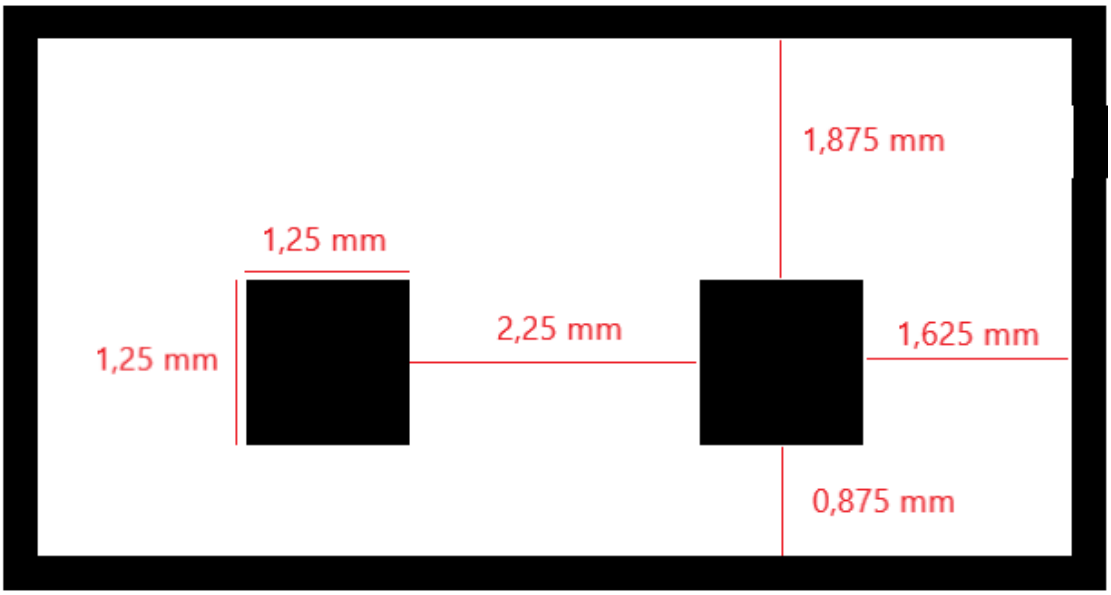

Figure 4.16: Basic cell on mask 0 for SiO_2 patterning

The black squares and blacked out perimeter will protect the photoresist from the UV light during the exposure so that it won't be etched afterward during the development.

The reason behind such a big structure is because these masks were printed on transparent paper using an ink printer to realize the final physical masks. Due to the high tolerances of the ink printer (0.5 mm) dimensions in the order of the millimeters were chosen. Theoretically the dimensions should have been as small as possible , yet it wouldn't have been wise to use dimensions too close to the printer limit.

The reported dimensions in the images are precise to the micro meter, clearly they could have been rounded up since the tolerance of the printer does not allow to accurately represent dimensions beneath 0.5 mm. Normally the designs would have been sent to a company for the development of glass masks with details of the nanometric size. Unfortunately due to the closing of the laboratories as a consequence of the corona virus pandemic, the project was developed especially on the theoretical side, leaving very few time for the actual realization of the device and the masks as well. This solution negatively influenced the final result, but under these circumstances, it was preferable rather than not being able to completely fabricate the device. Normally the width and length of the device are designed to ensure the best possible current output 3.1, due to the circumstances the dimensions have been chosen to grant the best fabrication procedure instead.

The second mask is necessary for the patterning of the photoresist before the deposition of the Aluminum to define the various electrodes. Fig. 4.17 shows the design.

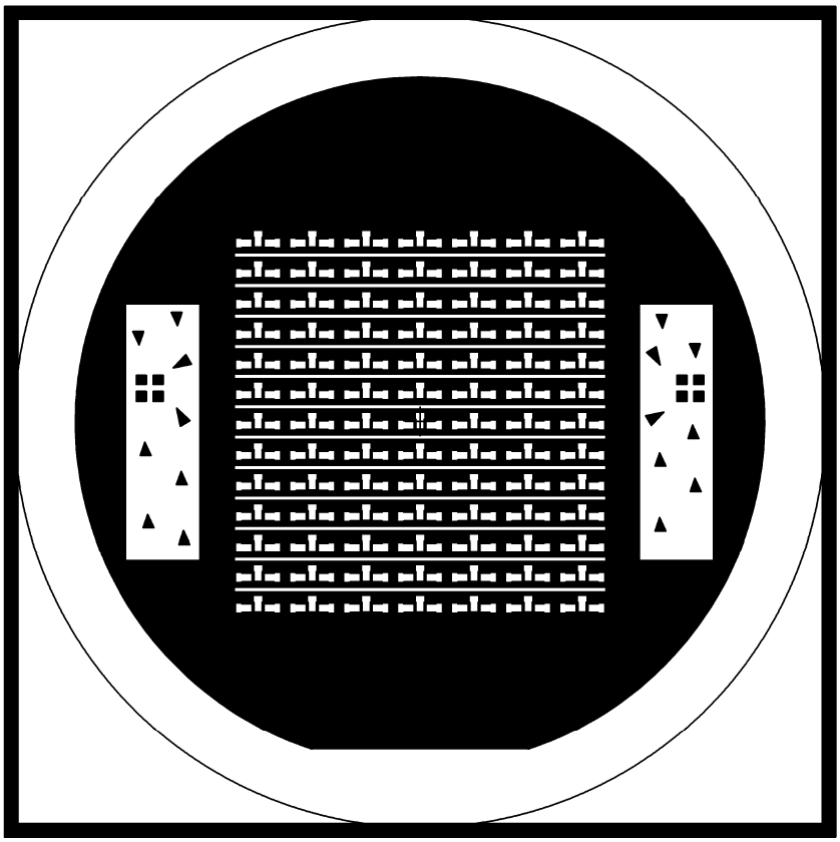

Figure 4.17: Mask 1 for *Al* patterning

Both masks show on the sides the presence of various alignment marks to facilitate the alignment process with the maskless machine. As for the previous mask the chosen dimensions for the unit cell are given in fig. 4.18

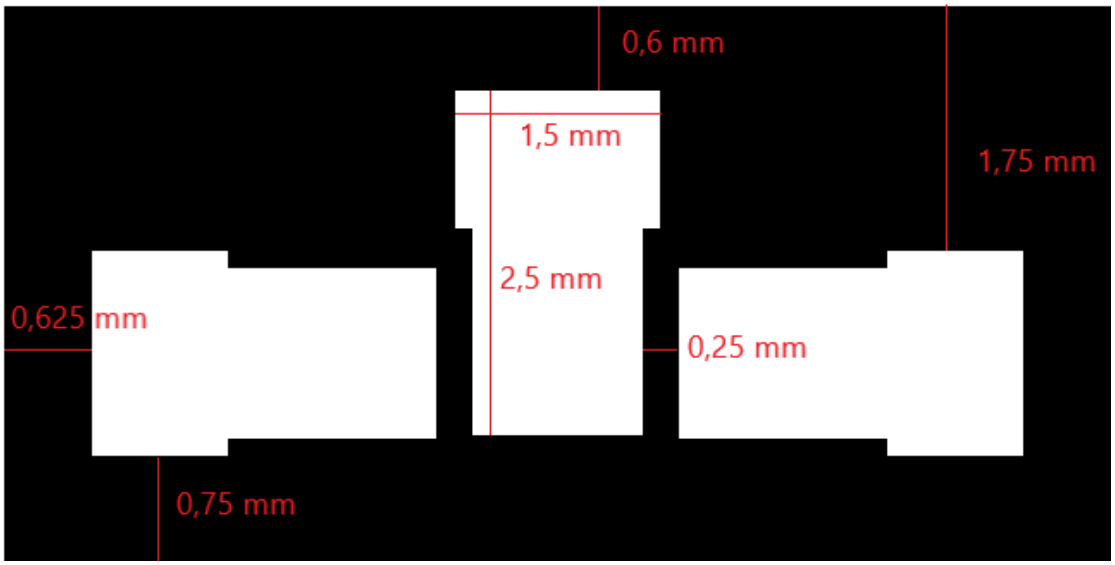

Figure 4.18: Basic cell on mask 1 for Al patterning

As for the previous case, the mask was designed for the development of a positive photoresist. The white openings will allow the deposition of Aluminum in the openings and on top of the insulating layer, so that the source and drain electrodes will be in contact with the SnO_2. The central opening is for the realization of the gate contact, which will be positioned on top of the silicon dioxide working as the gate dielectric. The black outline represents where the photoresist will be preserved during the development, so that after the lift off procedure the Aluminum will remain only in the area of the electrodes, leaving the rest of the cell insulated.

Chapter 5

Simulation measurements and results

To define the physical parameters of the device structure, a series of simulations have been implemented to determine the most suitable settings. The most important analysis regards the definition of the active layer thickness that guarantees full depletion of the transistor's channel for a reasonable gate voltage. Once a thickness has been chosen for both the active layer and the insulating layer, the flat band and the threshold voltage are computed to define the operating range of the gate voltage. These analyses are implemented both in Matlab, and in Comsol as well, to further verify the accuracy of the results obtained in Matlab.
The influence of the gate electrode metal is also investigated, proving how the variation of the gate work function "switches" the operating region toward either more positive or negative gate voltage values, influencing both the V_{FB} and the V_{th}.

5.1 Matlab Simulations

This section is devoted to illustrating the expected device behaviour, these analyses have been produced using Matlab.

5.1.1 Depletion region in Tin Dioxide

Equation 3.2 provides a theoretical evaluation of the maximum depletion region width. Unfortunately, Tin Dioxide is very sensitive to the deposition techniques, and as a consequence, its properties are quite variable. The following parameters have been extracted from [31], [32],[33], [34] it must be pointed out that different

values for the same parameters can be found, these values have been chosen because they appeared to be the most consistent ones throughout different papers.

- $q = 1.602 \cdot 10^{19}\ (C)$ is the elementary electric charge;
- $\varepsilon_{SnO2} = 9.86\ (F/cm)$ is the dielectric constant of Tin Dioxide;
- $\varepsilon_0 = 8.854 \cdot 10^{-14}\ (F = cm)$ vacuum permittivity;
- $N_{D,A}(atoms/cm^3)$ is the device layer donor/acceptor concentration;
- $q\phi_{n,p} = k_B T \cdot ln(N_{d,a}/n_i))$ (eV) is the n-type/p-type Fermi potential;
- $k_B = 8.6173303 \cdot 10^{-5}$(eV/K) is the Boltzmann constant;
- T = 293.15 (K) is the temperature;
- $n_i = 5 \cdot 10^{14}(atoms/cm^3)$ Tin Dioxide intrinsic carrier concentration for purely stoichiometric structures.

Fig. 3.6 shows the maximum depletion layer for Tin Dioxide as a function of the doping concentration (Although the origin of the free charge carriers is related to the oxygen vacancies it is still common referring to them as doping concentration).

Assuming a doping concentration around $4.8 \cdot 10^{18} \cdot cm^{-3}$ the maximum active layer thickness should be 26 nm or less. Starting from this first assumption it is then important to evaluate the voltages that allow to obtain the device V_{FB} and V_{th}.

5.1.2 Flat Band Voltage

To evaluate the flat band voltage of the device, it is necessary to define the physical parameters for the proposed structure. As equation 3.3 explains, the voltage is a direct function of the gate workfunction ϕ_M and Tin Dioxide workfunction ϕ_{SnO_2}. This implies that by changing the gate material it is possible to 'tune' the device, allowing it to work with different voltages. This is an important aspect since it allows to change a transistor purpose by simply changing the gate material.
In this design to comply with the task of simplifying the fabrication procedure Aluminum has been chosen for the realization of all three electrodes, to reduce the number of fabrication steps and necessary masks for the patterning. Table 5.2 shows how different gate materials would have influenced the flat band voltage.

The physical parameters used for the evaluation of the flat band voltage are depicted in table 5.1:

Material	Workfunction	Dielectric constant	Thickness
Aluminum	$\phi_{Al} = 4.11 \quad eV$	$\varepsilon_{Al} = 1.6 - 1.8$	$30 \quad nm$
Silicon Dioxide	$\phi_{SiO_2} = 5 \quad eV$	$\varepsilon_{SiO_2} = 3.7 - 3.9$	$25 \quad nm$
Tin Dioxide	$\phi_{SnO_2} = 3.7 - 4.2 \quad eV$	$\varepsilon_{SnO_2} = 9.86$	$25 \quad nm$

Table 5.1: Physical parameters for the active layer, insulating layer and gate electrode

Taking into consideration these parameters and the proposed structure the flat band voltage can be defined as a function of the free charge carriers in the active layer.

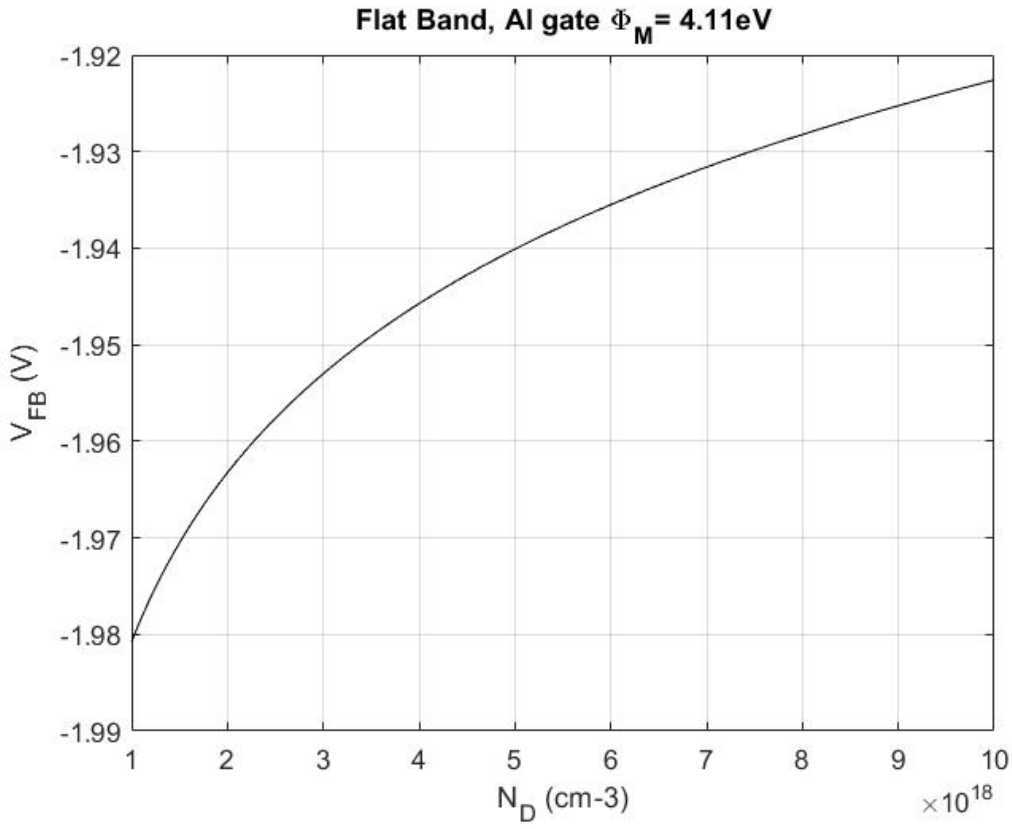

Figure 5.1: Flat band evaluation as a function of dopant concentration.

The flat band voltage isn't very sensible to the doping concentration in the current design, approximately for voltages of about -2 Volts or greater the transistor allows to obtain full conduction.

5.1.3 Threshold Voltage

Taking into consideration equation 3.5 it is possible to plot using Matlab the threshold voltage as a function of the doping concentration, fig. 5.2

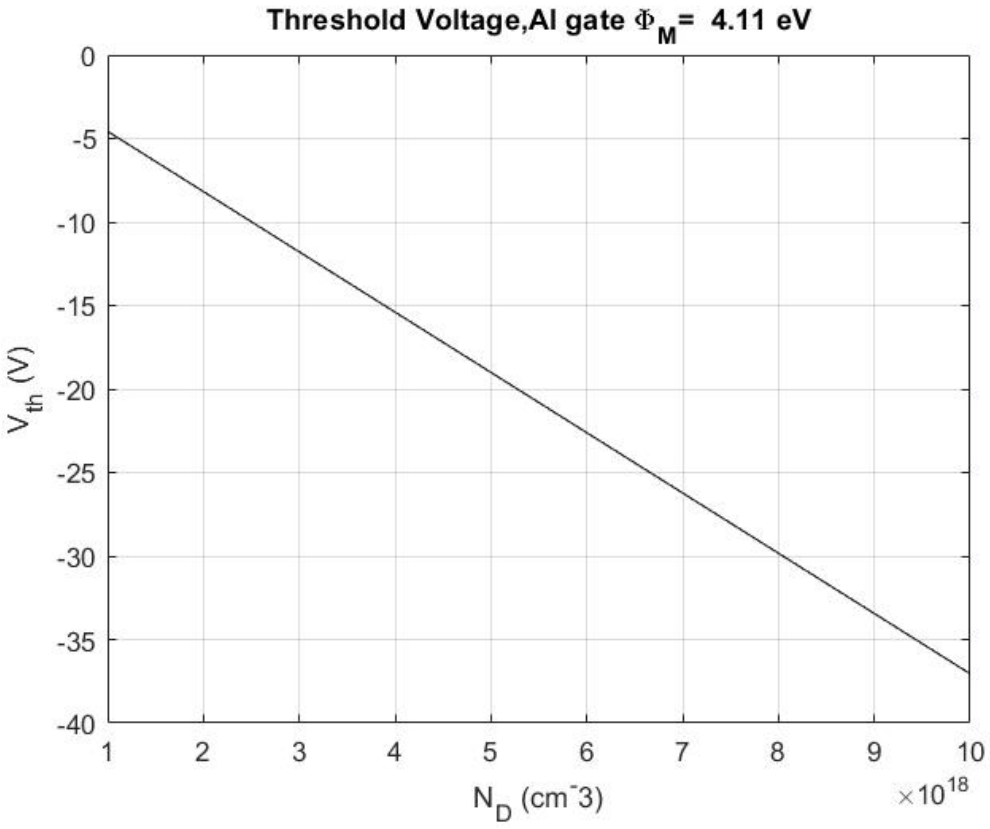

Figure 5.2: Threshold voltage evaluation as a function of dopant concentration.

The threshold voltage appears to be significantly more influenced by the doping concentration than the flat band voltage. Looking at equation 3.5 it is evident that contrarily to eq. 3.3 the threshold voltage has a direct dependency on the doping concentration. In the flatband voltage equation the doping accounts only for a logarithmic term in the Fermi potential : $q\phi_n = k_B T \cdot ln(N_d/n_i)$).

It should be pointed out that these plots are useful as a reference on the possible working behavior of the transistors, the equations that are being used have been developed for the study of doping in silicon rather than for the study of tin dioxide. None the less, since SnO_2 TFTs show the same I_d output curve as MOSFETs, these formulas can be employed for this case as well. Moreover, the band structure of tin dioxide can have very broad changes so it is very hard to identify specific parameters to develop the equations, hence some approximations and estimations have been made to obtain a finite model.

Both figs. 5.1 and 5.2 are useful in getting a sense of the device working parameters, to better understand the working principle some more detailed analysis have been implemented. In the following paragraph, more detailed simulations using Comsol Multiphysics are presented, showing the influence that the gate potential has on the depletion region.

The presented results have been obtained considering Aluminum as the gate electrode. By changing the gate material, and consequently the workfunction, the flat band and threshold voltage are influenced as well, fig, 5.2 shows the voltages for different gate materials. These values have been obtained employing eq. 3.3 and 3.5

Metal Φ_M	V_{th}	V_{FB}
Poly-Si(n)(4.05eV)	-15.78 V	-1.65 V
Al(4.1eV)	-15.5 V	-1.59 V
Ta(4.25eV)	-15.2 V	-1.49 V
Ti(4.33eV)	-15 V	-1.36 V
Cr(4.5eV)	-14.8 V	-1.19 V
Mo(4.6eV)	-14.73 V	-1.099 V
Au(5.1eV)	-14.23 V	-0.599 V
Ni/Poly-Si(p)(5.15eV)	-14.18 V	-0.55 V
Ir(5.25eV)	-14 V	-0.449 V
Pt(5.65eV)	-13.68 V	-0.049 V

Table 5.2: Flat band and threshold voltages for a SnO_2 based transistors as a function of different gate materials

As the gate material's bandgap increases both the V_{th} and V_{FB} are shifted toward more positive values. By choosing the right material it is possible to tune the threshold and flatband voltage accordingly with the use that will be done of the transistor.

5.2 Comsol Simulation

To analyze the behavior of the proposed structure, a two-dimensional version of the device has been created on Comsol. Fig. 5.3 shows the design illustrating the physical parameters as well. The gate insulator is not shown in the image, none the less a 30 nm layer of silicon dioxide is interposed between the aluminum gate electrode and the SnO_2 active layer.

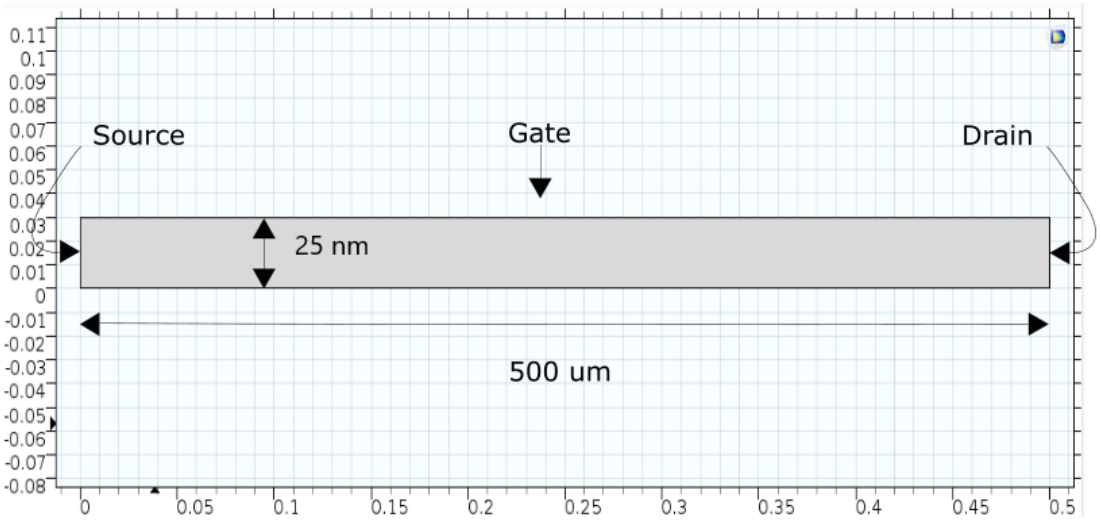

Figure 5.3: Two dimensional design of the Planar Junctionless Transistor on Comsol Multiphysics

Generally speaking, Comsol allows selecting a variety of materials for the study of devices. Tin dioxide is present among said materials, unfortunately the parameters necessary for the analysis of the charge carrier concentration and the study of the material as a semiconductor are absent. These missing parameters have been extrapolated from [31], [32],[33], and their values are shown in fig. 5.3 :

To study the effects of the gate voltage and verify the Matlab plots, the source and drain electrodes are forced to a zero potential, so that the device works as a MOS capacitor. More precisely, a MOS with an aluminum gate, a silicon dioxide

Relative permittivity	ε_r	9.86
Band gap	E_g	$3.72[V]$
Electron affinity	χ_0	$4.32[V]$
Effective density of states, VB	N_V	$2.4 \cdot 10^{18}[cm^{-3}]$
Effective density of states, CB	N_C	$1.8 \cdot 10^{19}[cm^{-3}]$
Electron mobility	μ_n	$100[cm^2/(V \cdot s)]$
Hole mobility	μ_p	$5[cm^2/(V \cdot s)]$
Electron lifetime	τ_n	$12.89[ns]$
Hole lifetime	τ_p	$12.89[ns]$

Table 5.3: Physical parameters used on Comsol Multiphysics for the simulations

insulating layer and tin dioxide as active layer.

Fig. 5.4 shows the electron carrier concentration in SnO_2 when $V_g = 0V$, the average concentration chosen for the device analysis is $N_D = 4.8 \cdot 10^{18} \quad cm^{-1}$, the plot shows that the electrons are distributed uniformly along the entire layer, showing a small peak close to the insulating layer. This peak can be attributed to the fact that the gate voltage is greater than the estimated flatband voltage ($V_{FB} = -2V$), creating an accumulation layer underneath the gate electrode. Reducing the gate voltage attracts positive carrier toward the gate electrode, ionizing them, and creating a depletion layer.

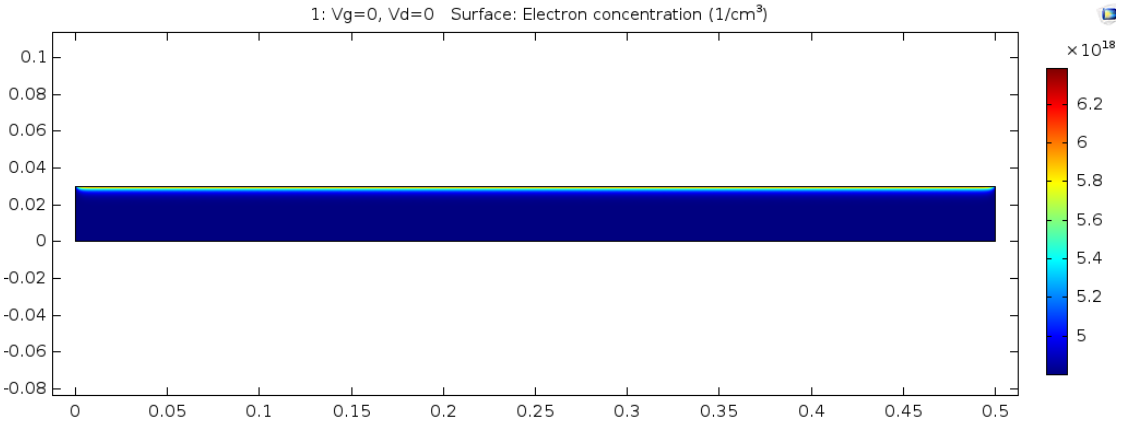

Figure 5.4: Electron concentration in the JLT for $V_g = 0V$

Figure 5.5 portrays the device when $V_g = -15.5 \quad V$. [5] provides a detailed analysis of how to theoretically extrapolate the position of the depletion layer barrier,allowing to define whether the channel is fully depleted or not. According to this paper, the depletion region confinement is associated with the position in the layer where the majority charge carrier concentration is half of the original doping concentration.

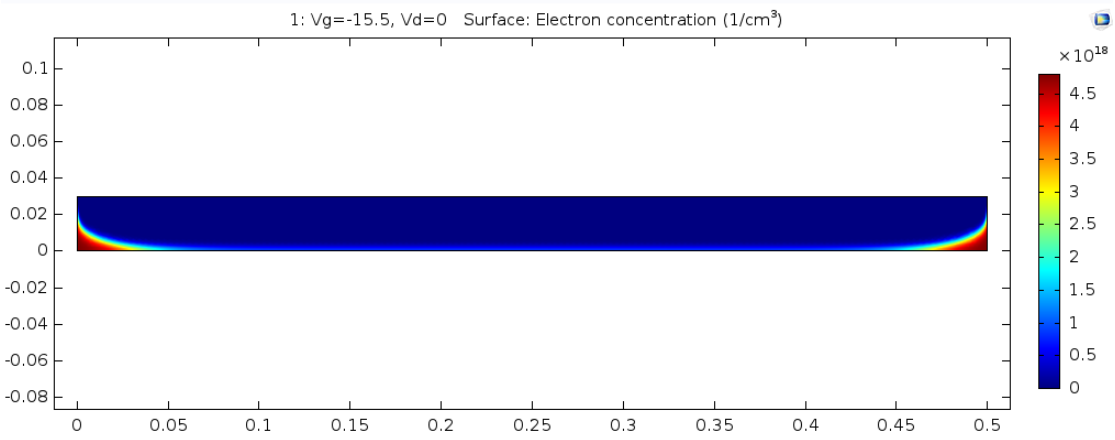

Figure 5.5: Electron concentration in the JLT for $V_g = -15.5V$

When $V_g = -15.5 \quad V$ the electron concentration at the bottom of the active layer (in this case for x: 0) is $N_D = 2 \cdot 10^{18} \quad cm^{-1}$, hence for this voltage the channel is fully depleted, the "OFF state" has been reached. $V_g = -15.5 \quad V$ is the first value for which the depletion region has fully expanded throughout the active layer, hence it's associated with the threshold voltage V_{th}. This proves that the Matlab plot 5.2 was was able to provide an accurate estimation of the device working parameters.

Arguably -15.5 volts isn't quite a common voltage for piloting nanotechnologies. On the other hand, the doping concentration taken into account is very heavy and the Tin dioxide band gap is quite wide, these factors influence the ability of the gate potential to ionize the charges and consequently creating the depletion layer. All these consideration could explain why such a low gate voltage is necessary to control the device. A possible solution could be reducing the doping concentration by changing the deposition parameter in the tin dioxide procedure, obtaining a more stoichiometric structure. Another possible solution could be to reduce the gate insulation oxide thickness. As stated in eq. 3.5 the thickness of the insulating

layer influences the threshold voltage, if the layer thickness is reduced, the threshold voltage is reduced as well (as well as the flatband voltage).
Both options must be taken into account carefully. An high doping concentration is necessary to ensure that the electrode to semiconductor contacts have an ohmic behaviour.

Assuming that a Schottky-diode contact for a chosen metal- n-type semiconductor interface ($\phi_m > \phi_{s,n}$) is created (rectifying contact), if the doping concentration in the semiconductor is high enough ($> 10^{18}[cm^{-3}]$) then the rectifying contact will be ohmic. This is because when a rectifying contact is realized, a depletion region on the semiconductor side is formed [35] as presented in 3.2:

$$X_{dep} = \sqrt{\frac{2\epsilon_{SnO_2(V_{bi}-V_a)}}{qN_d}} \tag{5.1}$$

in equation 5.1 V_{bi} is the built in potential, whilst V_a is the gate potential.

Raising the doping concentration will result in a thinning of the depletion layer, which would cause tunneling, making the contact ohmic. Hence reducing the doping concentration of the active layer could result in a rectifying behaviour for the source and drain contacts. A possible solution could be to reduce the doping in the active layer while keeping an high doping concentration underneath the source and drain. To do so, two $n++$ wells could be implanted underneath the source and drain contacts. This procedure of course would result in a longer fabrication procedure.

Reducing the gate insulation layer could also reduce the threshold and flatband voltage. But reducing too much the oxide thickness is dangerous, since this could lead to improper isolation between the gate and the active layer, resulting in leakage currents.

Plot 5.6 shows the current output I_d when the flat band voltage is applied at the gate:

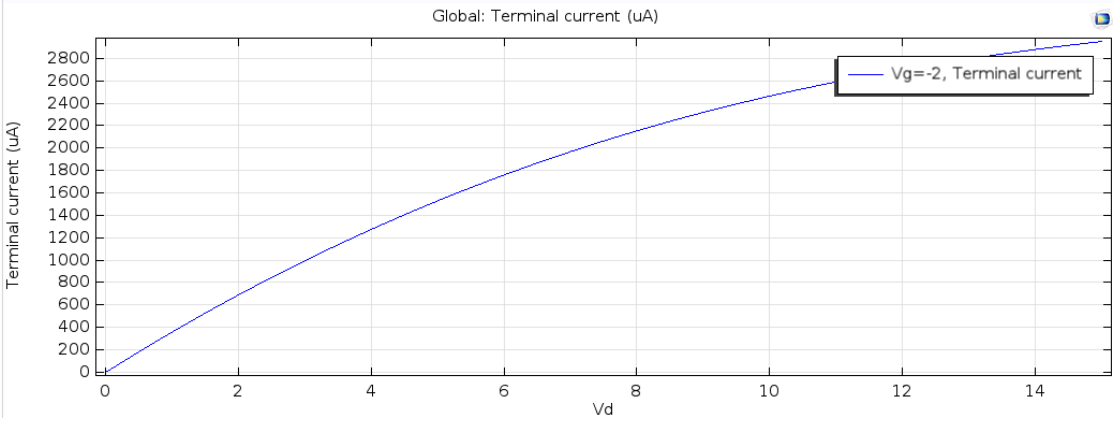

Figure 5.6: I-V curve of the JLT for $V_g = -2V$

As expected, when $V_g \geq V_{FB}$ the output current is maximised. The I_d output shows a very strong resemblance to the curvature of a MOSFET current output. The plot focuses mainly on the linear region of the device, although the current tends to saturate as the drain voltage increases (as for a MOSFET device upon saturation).

fig. 5.7 shows in more detail how the current output changes as a function of both the drain and gate voltage.

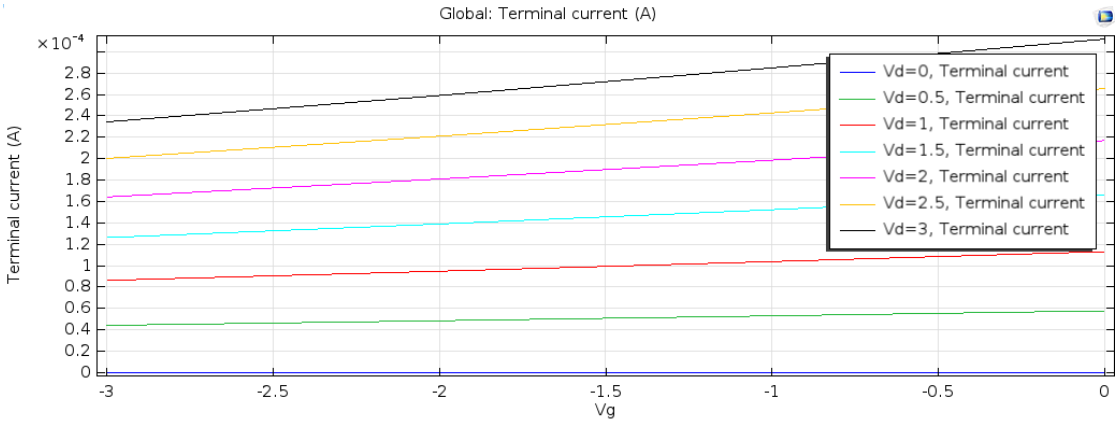

Figure 5.7: I-V curve of the JLT as a function of the drain and gate voltage

Fig. 5.8 shows the current flow for $V_G = V_{th}$, proving that for $V \leq V_{th}$ the depletion region significantly reduces the current output, allowing to define the ON and OFF states:

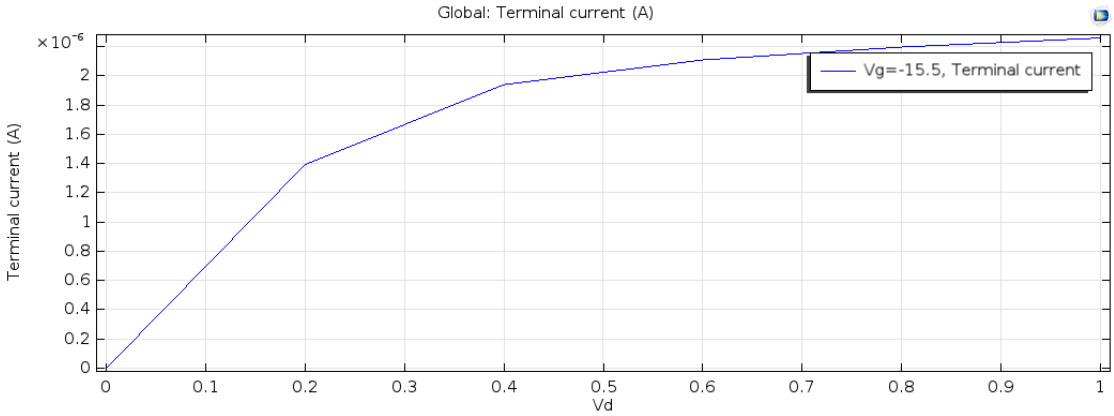

Figure 5.8: I-V curve of the JLT for $V_g = -15.5V$

The plot shows only values of the current until $V_D = 1V$ simply because afterward the current saturates. Unfortunately, the Comsol algorithm is not capable of computing the current output for values of $V_G < V_{th}$, this might be further proof that the values of current for voltages lower than the threshold voltage are so low that cannot be correctly computed by the software. None the less the results showed in 5.8 are still interesting. Comparing the current output of 5.6 with 5.8 the I_{on}/I_{off} rate is approximately $10^2 - 10^3$ for $V_D = [3 \div 10]$.

5.3 Fabrication procedure

In this section, a more in-depth description of the procedures and parameters for the fabrication is discussed.

5.3.1 Tin Dioxide Deposition

The starting substrate is a Silicon wafer with a diameter of 100 mm, on top of which a silicon dioxide has been grown using oxidation.

Tin dioxide is sputtered on top, the deposition parameters for the RF magnetron sputtering are presented in the table 5.4.

Target	**Target purity**	**Substrate**	**Target distance**	**Rotating spd**
SnO_2	99.6	SiO_2	18 $[cm]$	10 $[rpm]$
Power	**Base Pressure**	**Working Pressure**	**Temperature**	**Deposition rate**
150 W	40 $[mTorr]$	8.2 $[mTorr]$	250$[C]$	0,86 [Å/s]

Table 5.4: Deposition parameter RF Sputtering for Tin Dioxide.

The target distance is very difficult to set in the AJA sputter machine at the USN laboratory, hence it is fixed at 18 cm for most of the procedures. The target to substrate distance influences the deposition rate, the closer the target is to the substrate, the faster the deposition rate. On the other hand, if the target is too close, the particles released from it could reach the substrate with too much energy causing damage and compromising its stoichiometry. The rotating speed was set to 10 rpm as the lab engineer at USN suggested, in his opinion this rotating speed was sufficient to obtain good uniformity for the deposited material on the wafer. The deposited layer thickness accordingly to the sputter machine deposition controller is approximately 25 nm, further testing through SEM analysis proved that the actual deposited layer is 24 nm, fig. 5.15.

5.3.2 Silicon Dioxide deposition and lift off

Once the active layer has been deposited the next step is the deposition and patterning of the insulating layer. As previously explained, tin dioxide is highly sensible to the SiO_2 etchants, so a lift off procedure has been deemed more adequate under these circumstances for patterning.

- Wafer cleansing with Isopropanol.
- Drying with nitrogen gun followed by 5 minutes of heating on a hot plate at 100 °C.
- Spin coating, through Spinner 2 AB Plast Spin 150, of positive PR s1813.
  - Time: 30 seconds.
  - Speed : 2800 rpm.
- Bake 1min at 110°C.
- Photoresist exposure (Mask Aligner EVG 620) in order to imprint 4.17 on the substrate.
- Photoresist development through MF3189.
- Deposition of tin dioxide, the deposition parameters are presented in tab 5.5.

Target	**Target purity**	**Target distance**	**Rotating spd**	**Power**
SiO_2	99.6	18 $[cm]$	10 $[rpm]$	300 W
Ar flow	**Base Pressure**	**Working Pressure**	**Temperature**	**Deposition rate**
100 $sccm$	40 $[mTorr]$	13 $[mTorr]$	RT	0,04 [Å/s]

Table 5.5: Deposition parameter RF Sputtering for Silicon Dioxide.

The Argon flow in the chamber defines the amount of ionized Ar ions for target bombarding, hence the generation rate of sputtered SiO_2 particles. An high argon flow in the chamber would theoretically increase the deposition speed. But too high of and argon flow has been noticed to increase the number of scattering events between the ions and the sputtered silicon dioxide particles. These scattering events would cause loss of energy for the silicon dioxide particles, reducing their mean free path and ultimately the deposition rate.

Hence raising the Ar flow rate in the chamber over a certain limit would be counter productive.

fig. 5.9 shows the obtained layer:

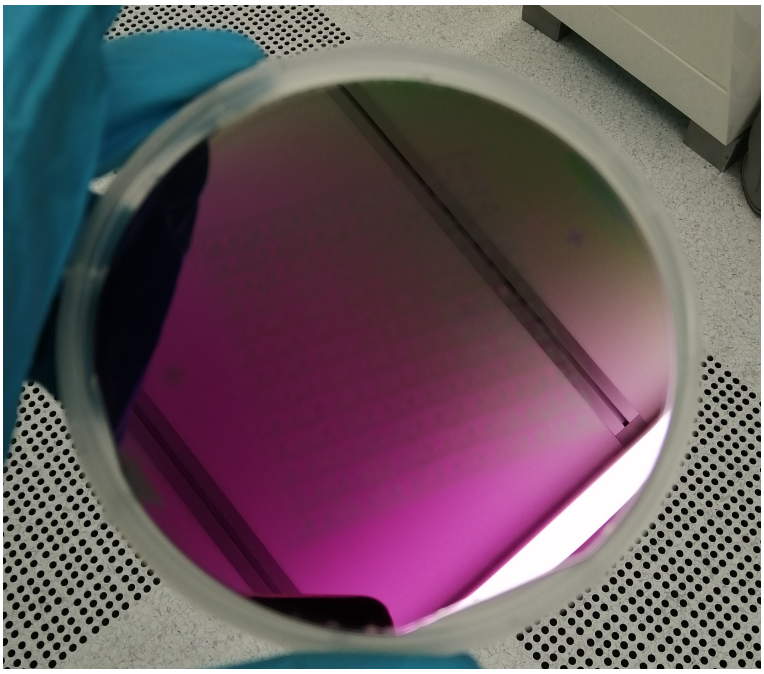

Figure 5.9: Wafer surface after the silicon dioxide deposition

- Lift off of the photoresist, the following procedure is repeated until the photoresist isn't completely removed:
  - Rinsing in acetone on a spinner for 4 minutes.
  - Rinsing in acetone and isopropanol for 4 minutes.
  - Deionized water cleansing.
  - Drying with nitrogen gun.

The final result after three lift off procedures is shown in fig. 5.10

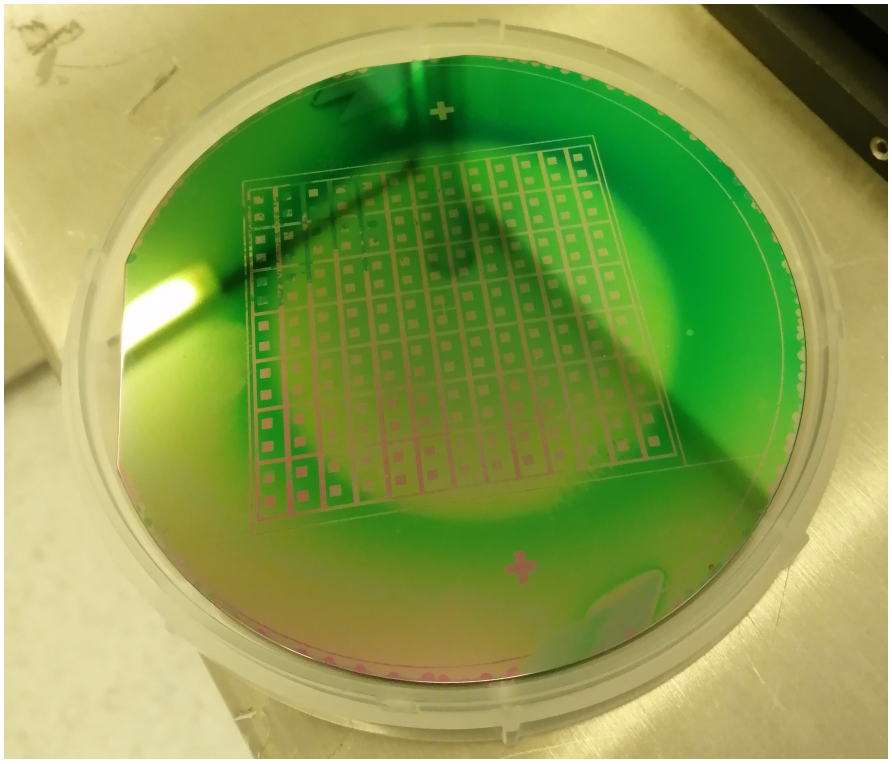

Figure 5.10: Wafer surface after the lift off of the photoresist for the creation of the openings and definition of the transistor patterning

5.3.3 Aluminum deposition and lift off

Aluminum is used for the realization of the source, drain, and gate electrodes. Since the project aims to reduce the fabrication steps, the use of the lift off technique for the patterning of Al has been chosen. To avoid the baking of the photoresist during the deposition of the Aluminum in the sputtering machine, it was necessary to find a procedure that allowed for the deposition of the Al at room temperature (RT). The deposition of Aluminum at RT also reduces its oxidation, sputtering causes the release of oxygen from the silicon dioxide and tin dioxide, which would result in oxidation of Al and the formation of Al_2O_3 for high deposition temperatures. Moreover lower deposition temperatures reduce the overall roughness of the Aluminum layer, creating smoother electrodes [36].
The chosen procedure has been defined as follows:

- Spin coating, through Spinner 2 AB Plast Spin 150, of positive PR s1813.
  - Time: 30 seconds.
  - Speed: 2800 rpm.
- Bake 1 min at 110°C.
- Alignment of mask 1 with respect to the alignment marks left purposely on the wafer with mask 0. Unfortunately the poor quality of the mask did not allow to use the Maskless aligner electron microscope, hence the alignment was done manually.
- Photoresist exposure (Mask Aligner EVG 620) in order to imprint mask 1 (fig. 4.17) on the wafer.
- Photoresist development through MF3189. Fig. 5.11 shows an image of the obtained patterning after the lift off procedure. The white area is the tin dioxide, which has been left exposed to create the electrodes, the bright green areas are silicon dioxide, whilst the brownish areas are where the photoresist has been deposited and developed. It can be observed how the tin dioxide area shows various dark spots, these spots are traces of photoresist, which wasn't correctly removed after the lift off procedure.

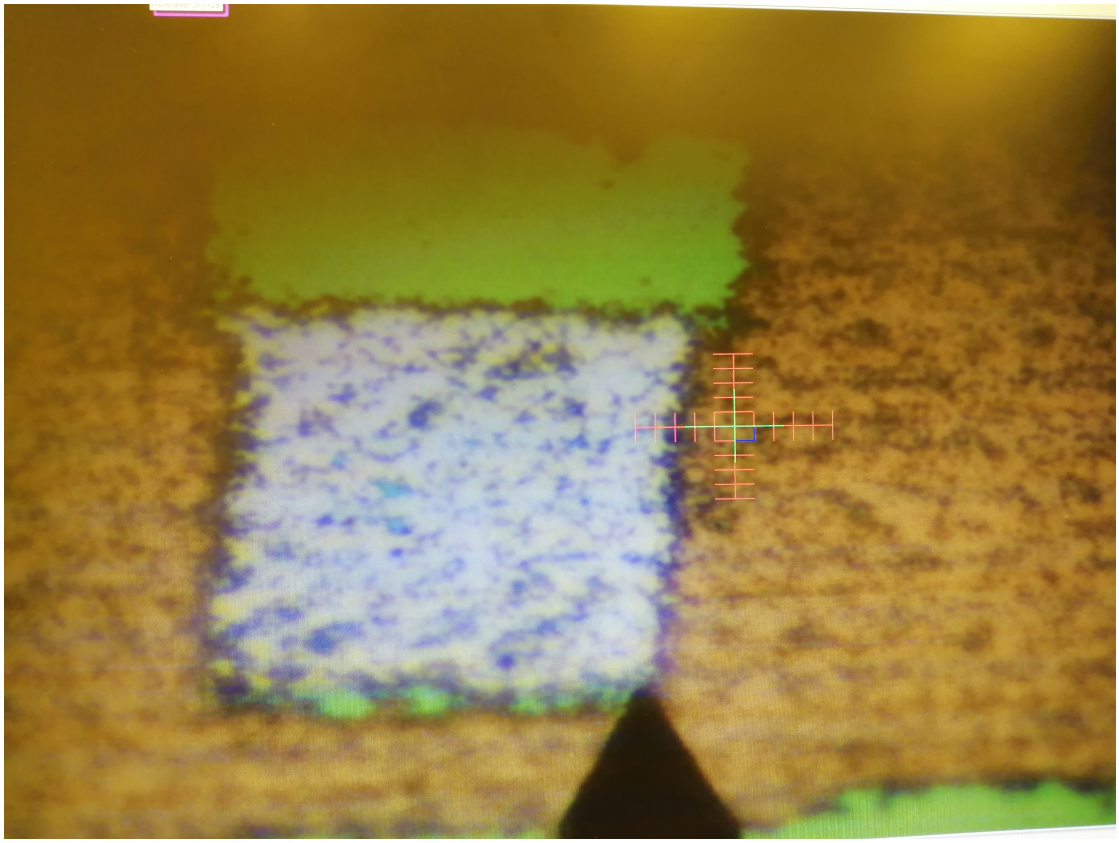

Figure 5.11: profile of the Surface after the lift off. The white square shows the tin dioxide opening, the dark spots in it are residue from the photoresist removal. The bright green areas are silicon dioxide, whilst the brown/yellow areas are where the photoresist lies after the development, hence where aluminum will be removed after the lift off procedure. .

- Deposition of Aluminum in the AJA sputter machine, tab 5.6 shows the deposition parameters.

Target	**Target purity**	**Target distance**	**Rotating spd**	**Power**
Al	99.6	18 $[cm]$	10 $[rpm]$	150 W
Ar flow	**Base Pressure**	**Working Pressure**	**Temperature**	**Deposition rate**
100 $sccm$	40 $[mTorr]$	13 $[mTorr]$	RT	0,6 [Å/s]

Table 5.6: Deposition parameters for DC Sputtering of Aluminum.

Fig. 5.12 shows the wafer after the Aluminum deposition:

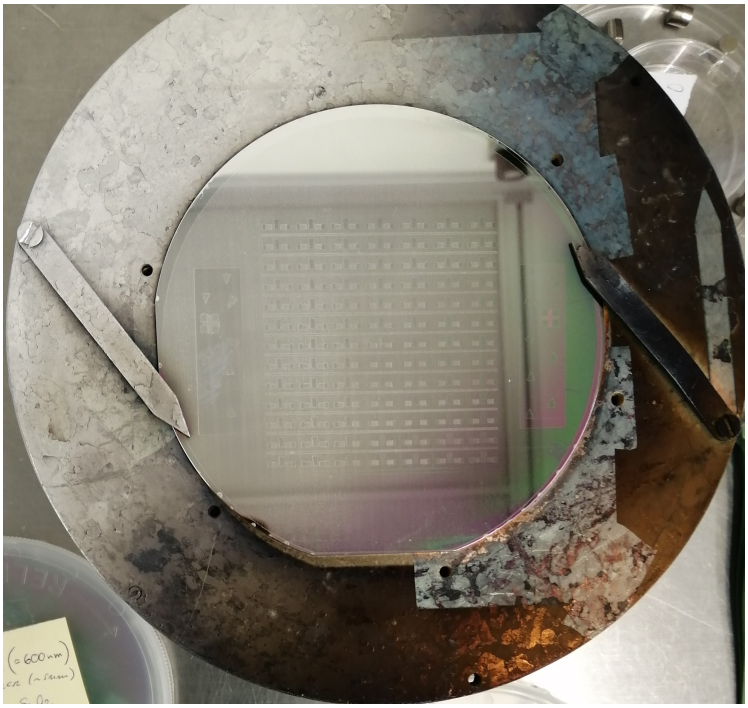

Figure 5.12: profile of the Surface after the Al deposition

- Lift off of the photoresist, the following procedure has been repeated until the photoresist was completely removed:
  - Rinsing in acetone on a spinner for 4 minutes.
  - Rinsing in acetone and isopropanol for 4 minutes.
  - Deionized water cleansing.
  - Drying with nitrogen gun.

  Some issues were encountered during the lift off procedure, after the fifth iteration of the process, it became clear that the photoresist wasn't being correctly removed.

5.4 Measurements results

5.4.1 Resistance measurements

The deposited SnO_2 is tested through a PWS Probe II system (4 probe measuring system), fig. 5.13, to evaluate the resistance of the deposited layer. A 5 point measurement procedure is used, which implies that the value of the resistance is measured in the four corners and in the middle of the wafer to verify if the deposited layer is uniform, the measurements are reported in table 5.7.

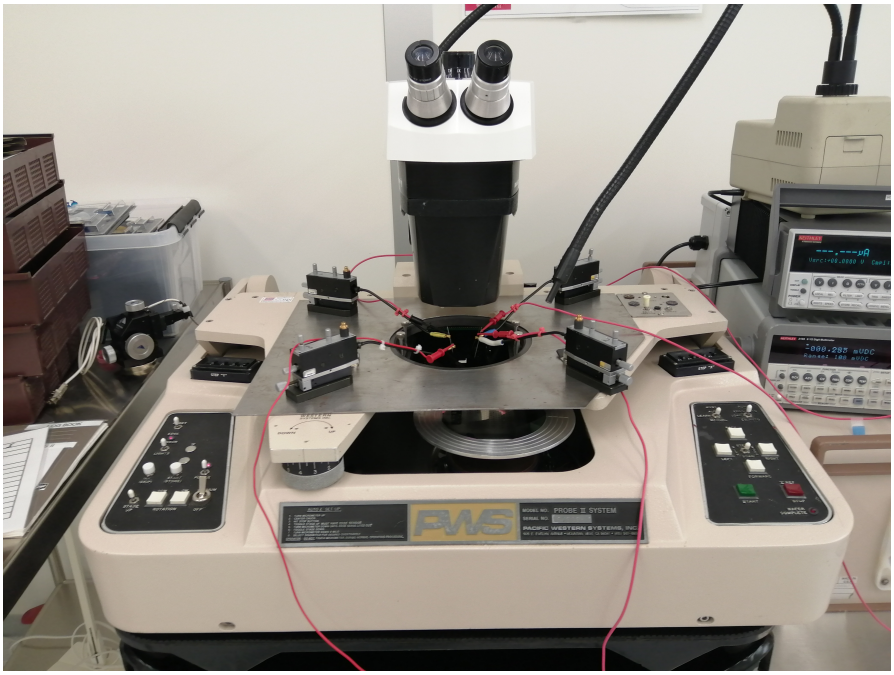

Figure 5.13: PWS Probe II four probe measurement system

The obtained resistance averages around $50k\Omega$ aside for the middle where the resistance is slightly lower, but overall the wafer has good uniformity.

Top Left	Bottom Left	Center	Top Right	Bottom Right
$52k\Omega$	$49k\Omega$	$43k\Omega$	$48k\Omega$	$51k\Omega$

Table 5.7: Measured resistance values on the SnO_2 wafer using the 5 point measurement procedure

5.4.2 SEM analysis

To verify the actual thickness of the deposited SnO_2 the SEM machine requires squares with sides of 5 mm. The wafer is diced using an Ion Milling IM4000 following the pattern showed in fig. 5.14

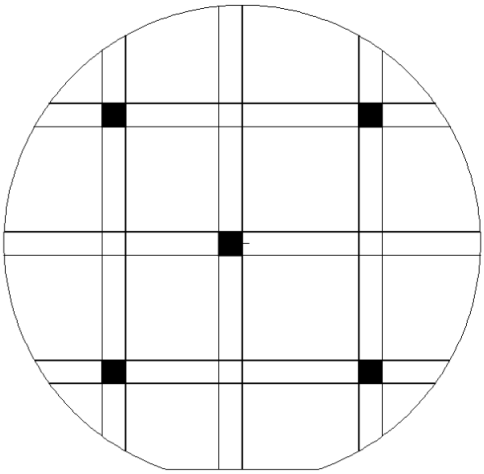

Figure 5.14: Schematic for the dicing of the wafer, the blacked out squares are the ones that can be used for the analysis

The samples are polished using a Struers DP10 on one side to allow the SEM analysis. Since the deposited layer is very thin and due to the transparent properties of tin dioxide the obtained pictures are quite blurry, none the less they can be used to measure the deposited $SnO2$, fig. 5.15

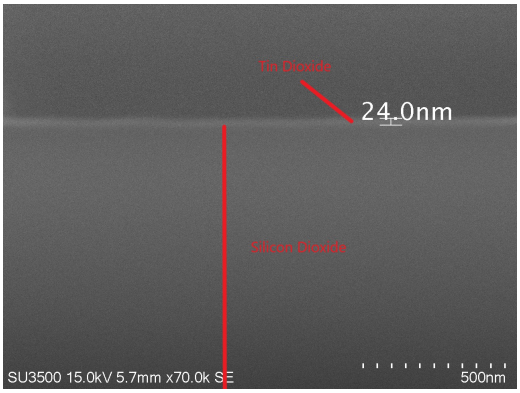

Figure 5.15: SEM Image of the deposited Tin Dioxide layer on top of the silicon dioxide

The SEM analysis was performed using an SEM Hitachi SU 3500, the obtained image shows that the deposited layer has a thickness of approximately 24 nm so the mismatch with the readings on the sputtering machine is approximately $[+1; -1]nm$.

SEM analysis was also employed on the final device cross-section, with the intent of verifying whether the obtained structure corresponded to the modeling. Unfortunately, this analysis was inconclusive, either by an incorrect dicing of the wafer, which lead to a damaging of the cross-section or some unknown factor. After an analysis of the image, it became clear that the backscatter detector could not find any material contrast to conform to the layer structure, not allowing to identify the different layered materials.

5.4.3 Characterization

A series of tests were conducted to determine whether the fabrication procedure was able to produce a working device and to test if its performances were similar to the results obtained in the theoretical evaluation.
To test the device a Micromanipulator 6000 probe station was employed along with a Keithley 2602 source meter.
Three probes were connected directly to the source, drain, and gate respectively as shown in fig. 5.16 . The Source meter in question is a dual-channel device, which implies that it is possible to modulate both the gate voltage and V_{ds} voltage at the same time through the same machine. Channel one was used to control the gate voltage, whilst channel two was used to define the voltage between the source and the drain.

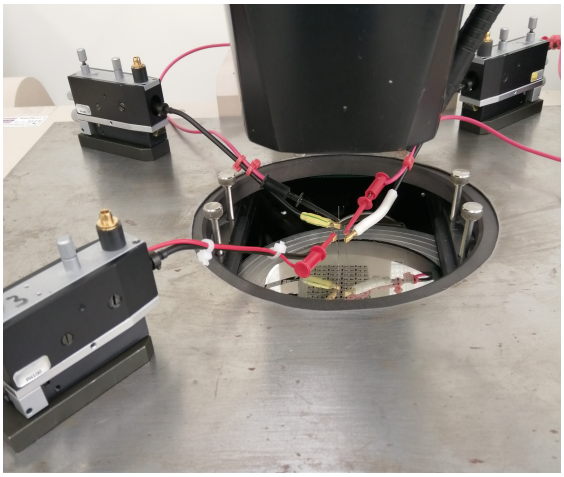

Figure 5.16: Positioning of the probes for the transistor characterization in the Micromanipulator 6000 probe station

The first test aimed to verify whether it was possible to conduct a current from source to drain when the gate voltage was zero, the obtained results are presented in the plot 5.17

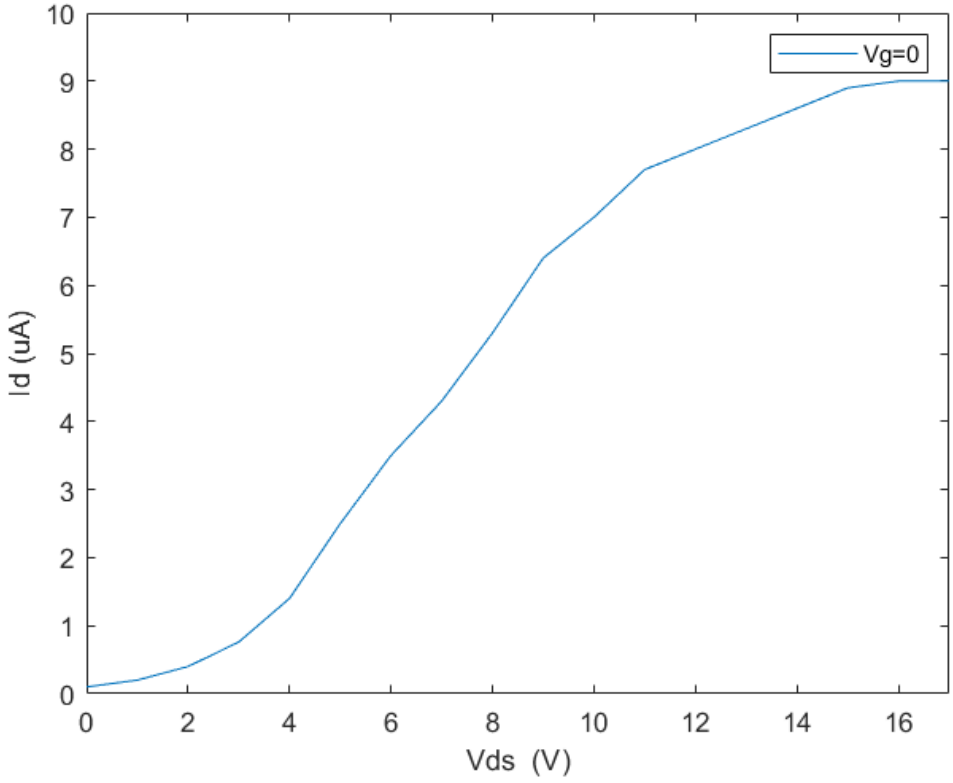

Figure 5.17: Current-Voltage plot $I_d - V_{ds}$ for $V_g = 0$

The current output in 5.17 is in the order of the micro amperes, hence lower than expected considering the $I - V_d$ output plot 5.6. This could be attributed to several reasons, such as a lower doping concentration in the tin dioxide layer, the presence of other crystallographic phases other than SnO_2, an higher scattering rate than expected due to the size of the nanograins, all factors which would result in a lower conductivity.

None the less the obtained curve resembles the curvatures that have been obtained in other papers for other junctionless transistors. The curvature resembles significantly the current output of a MOSFET as the one presented in fig.3.4. The MOSFET like I_d output obtained gives further proof that the equations used for the evaluation of V_{th} (3.5) and V_{FB} (3.3), can be used for the study of the SnO_2 PJLT, although developed for the study of silicon based TFTs.

Unfortunately, any further tests changing the gate voltage were inconclusive. It

was not possible to actively modulate the depletion layer inside of the tin dioxide layer through the gate voltage. The main assumption is that some of the fabrication step probably didn't go as planned.
A I_g leakage current was found by the source meter when applying a voltage at the gate electrode, suggesting that the insulation of the gate wasn't working as it should. Another possible explanation would be the presence of short-circuits between the electrodes. This could be the result of a faulty aluminum removal process during the lift off, which left some contact areas between the electrodes.

Chapter 6

Conclusions

In this project, a planar junctionless transistor was developed by analyzing the properties of junctionless transistors and thin-film transistors to combine the two and obtain a "hybrid" device. The aim was to obtain a device that would combine the advantages of a junction free structure and the possibility of fabricating the device using deposition techniques rather than FDSOI wafers.
The use of tin dioxide as the active layer of the proposed PJLT was studied, defining its physical properties and how they could be controlled by a chosen deposition technique.
As a result of these studies a theoretical model was defined, this model was then modified to simplify the fabrication procedure to a minimum number of steps.
The final device physical parameters are the result of several software simulations through Matlab and Comsol. These simulations were employed to define the most suiting dimensions for the proposed structure. These simulations also aimed to define the device working rage, characterizing its "ON" and "OFF" states as a function of the gate voltage V_g.
The fabrication procedure was established, selecting the most fitting procedures that granted a cheaper and faster procedure, without compromising the quality of the final product. The device was then built and tested entirely at the USN clean room. Resistance measurement and SEM analysis were conducted on the wafer throughout the procedure to identify the most important parameters, all the obtained results were reported in the thesis. The device was then characterized to define its working range. The current output was measured, proving that the device reaches full conduction when the flat band voltage is applied to the gate electrode. The current-voltage plot showed a very strong resemblance to the typical curvature that FET devices normally have, defining the linear and saturation regions.
Unfortunately, the gate insulation was somehow compromised, possibly due to some issues during the fabrication procedure (mask misalignment, faulty gate oxide), which led to the formation of a gate current when changing the gate

voltage. Some improvements are necessary for the fabrication procedure of the gate insulating layer. This could be achieved by employing glass masks for the fabrication procedure and thicker layers to facilitate the lift-off procedure.
The lack of time due to the circumstances (impossibility to access the clean room due to the Covid 19 pandemic) did not allow to repeat the fabrication procedure and repeat the testing of the device.

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