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Master Thesis

Test on charging systems for V2G application with Power Hardware-In-the-Loop methodology

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Abstract

The document is the result of an ongoing and wider collaboration between the Politecnico di Torino and Edison S.p.A., main player in the energy sector. The project aims to study the economic and technical feasibility of a specific V2G application. This thesis covers the beginning of the experimental part of the project, focusing on the charging station testing and the laboratory setup.
The test laboratory has been set up at the Energy Center Lab with the purpose of performing the Power-Hardware-In-The-Loop methodology using the charging station, capable of V2G application, as the device under test.

In order to correctly carry out the PHIL experiments on the charging station, all the instruments have been previously tested: Real-Time Simulator, Power Amplifier, Electronic Load (which replaced the charging station in the preliminary phase of the project).
While the components were added in the PHIL configuration, the simulation environment has been implemented as a Simulink model.

Afterwards, the measurement systems were implemented as a means to record and then process the measured data. For this purpose, sensors, current probes and a data acquisition system have been used.

Finally, the V2G charging station has been tested with an open loop chain. Firstly, its basic characteristics and firmware functions were evaluated. Then some regulated test have been performed to verify the compliance of the charging station for connection to the grid and V2G feasibility.

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Acronyms

API	Application Programming Interface
BEV	Battery Electric Vehicle
CHIL	Controller Hardware-In-The-Loop
DAQ	Data Acquisition system
DSO	Distribution System Operator
DUT	Device Under Test
EL	Emulated Load
EUT	Equipment Under Test
EV	Electric Vehicle
EVSE	Electric Vehicle Supply Equipment
FCEV	Fuel Cell Electric Vehicle
FPGA	Field-Programmable Gate Array
G2V	Grid to Vehicle
GUI	Graphical User Interface
HIL	Hardware-In-The-Loop
HV	High Voltage

I/O	Input / Output
IA	Interface Algorithm
IP	Internet Protocol
ITM	Ideal Transformer Metod
LV	Low Voltage
MV	Medium Voltage
PA	Power Amplifier
PHEV	Plug-In Hybrid Electric Vehicle
PHIL	Power-Hardware-In-The-Loop
RCD	Residual Current Device
RMS	Root Mean Square
ROS	Rest Of the System
RTS	Real-Time Simulator
SoC	State of Charge
SoH	State of Health
TCP	Transmission Control Protocol
THD	Total Harmonic Distorsion
TSO	Transmission System Operator
V2G	Vehicle to Grid
WB	WallBox

Chapter 1

Introduction

In the last years, the issue of greenhouse gases emission led to a greater deployment of electric vehicles.
Contextually, the Vehicle-to-Grid technology was taking hold, offering itself as a profitable market opportunity for both the electricity grid and the EV owner.
In fact, V2G technology can make use of the innovative bidirectional charging stations to take part in the ancillary services market.
Edison S.p.A. and Politecnico di Torino joined forces to both deepen research into the topic and to experimentally test the profitability of the technology, in interesting market scenarios for the company.

In this thesis the first part of the project is illustrated, focusing on the experimental side.
A bidirectional charging station was provided by Edison S.p.A. in order to test its validity for a wider V2G employment.

1.1 The rise of the electric vehicle

At this time the global warming is one of the major issues faced by the current society.
The traditional vehicles are powered by fossil fuels, which emit large emissions of carbon dioxide when are burned inside the internal combustion engines.
Apart from the increase of the Greenhouse gases in the atmosphere, the traditional vehicles are also responsible for air pollution due to secondary emissions (particulate matter, nitrogen oxides, etc..).
Many national and international governments are starting to stand against

this problem and are proposing many incentives to start adopting the electric vehicles [40].
Along with the environmental issues, another reason to deploy EVs is given by the increase trend of the oil prices during this decade and the need to terminate the dependency on oil [47].
V2G refers to a technology system in which the different types of EVs available on the market (BEV, PHEV, FCEV) supply power back to the grid.

1.2 Vehicle-To-Grid technology

The EV demand, pushed by the authorities, has undergone an outstanding growth in the past few years. So, as the light vehicle fleet moves towards the powertrain electrification, an opportunity opens for the Vehicle-to-Grid.
The V2G operation is able to smooth the load curve providing peak power, afford backup capacity for the future, improve reliability of the power system, while offering a revenue to the EV owner which effectively sell power to the grid [47].
For the V2G implementation three elements are required [47]:

- a power connection to enable the power flow from the EV battery to the electrical grid;
- control connection through which the grid operator requests ancillary services or power from the vehicle;
- precise and certified metering on board.

The V2G application has benefits for all the subjects involved.
Environmentally the V2G trend could imply a greater deployment of electric vehicles, resulting in decrease of air pollutants.
Economical benefits are assured to the vehicle owner as well. The electrical energy can be stored into the vehicle during the night, when the price is low. While it is withdrawn during peak-time, at higher prices. Revenues are given from the difference of prices.
Finally the major benefits are for the grid operator. The energy stored in the EV battery can be used to contribute to supply a local feeder, thus executing peak-shaving. This in turn translates to a reduction of line losses, a reduction transmission congestions and decreases the stress operation of the power system.

The V2G peak shaving application reduces the cost of the electricity during peak periods. Moreover, the EVs offer the power system with a flexible controllable load [47].

1.3 V2G & ancillary services

Ancillary services aim at assuring the reliability of the power system, enhancing the power quality.
In [14] is explained how, although the ancillary services are the same all over the world, in some nations the same service could have different names.
Generally these services are grouped into energy services, where the time represents an important variable, and into power services, in which the service performed is quicker with negligible energy exchanges.
Because of the limited energy capacity of the EV battery, it is clear that V2G can compete mostly in power services market. More valuable services for the V2G application appear to be the frequency control and reserve which match V2G feature as for instance the quick response. Other more energy sided services can be profitable, it is the case of load leveling, peak shaving and valley filling [14].

The V2G technology is already being deployed all around Europe with many operational pilot projects, for instance the SEEV4-City project [34] and the eVolution2G project [17]. More and more the spotlights are focused on this technology that can become profitable for many subjects involved.

1.4 Charging Infrastructure

The charging infrastructure supplies electric energy for the recharging of the electric vehicles. So far, most of the charging stations installed and available on the market allow the unidirectional flow. This traditional operation is defined as grid-to-vehicle (G2V).
When, instead, the electric energy flows in the opposite direction, thus from the vehicle to the grid (V2G), it is necessary to have a bidirectional charging station.

There are four modes of electric vehicle charging as described by International Electro-technical Commission (IEC) standard 61851-1:2018 [4]. The

first three modes relate to AC charging while the fourth mode sets the conditions for fast paced DC charging.
In this thesis, a DC charging station capable of V2G is tested (mode 4).
Differently from the AC charging station, a DC charging station contains a AC/DC converter.

Since the EV which will be connected to the charging station is a Nissan Leaf (Japanese manufacturer), the charger type is the CHAdeMO charger. This connector, at the moment, is the only standardized connector capable of feeding energy back to the electric grid with the V2G operation [26].
Deeper details about the types (connectors) are given in the standard IEC 62196 [**62**]

1.5 State of the art in V2G testing

Some test bed implementations can be found in literature.

A first case is given by the National Renewable Energy Lab (NREL, [10]) which made available a complete list of tests to be performed to evaluate the performance of a charging station.
As there is still no standard aimed at the requirements of V2G, the NREL collected many performance tests from different standards and adjust them for the V2G operation.
The paper results to be an useful guideline for V2G testing, and in chapter 9 many tests were performed following the NREL indications.

The University of Delaware [30] focused primarly on the response of regulation signals using two charging points with rated power of 16.6 kW and 12 kW.
The vehicle under test was modified, by adding controls and logic, to make it respond to the DSO real-time signal for regulation.
Still in USA, the University of California [43] the Demand Response of a V2G application in a distribution network was tested.
Their results showed that the system was able to support critical islanded DC/AC load and to respond quickly to the remote Demand Response signal for V2G, within 1.5 kW of power range.

The Universidade de Lisboa [9] used the same vehicle that we will be employ for our tests: the Nissan Leaf.
The DC charging station used has 10 kW of V2G rated power.

The work proposes a characterization procedure for V2G systems providing ancillary services. It focuses in acquiring data as communication and ramping times and to elaborate others as inaccuracy and variability of response.

Similarly to the primary attempt of this document, the University of Tokyo [42] used the HIL methodology to implement two control scheme for the EV frequency control.

1.6 Project overview and objectives of the thesis

Edison S.p.A. is a main player of the Italian energy sector. The company aims to extend its operation range involving the market opportunities offered by the V2G application.
For this purpose, a V2G charging station was purchased and made available to the Politecnico di Torino research group for the testing.
The firmware of the charging station has been edited, by a second company, in order to enhance the communication with the wallbox. In this way it is possible to make advanced requests to the wallbox, with a view of V2G operation.
For confidentiality reasons, the wallbox manufacturer and the company which modified the firmware are not cited in the thesis.

Another side of the joint project (not covered in this document) is represented by the study of the economical feasibility of the business scenario.
As the simulation would take into account the social aspect, the agent-based model will be applied.
Furthermore, the coexistence of the EVs with the power grid through V2G application involves many nonlinear variables. In the engineering field different methods are available to solve optimization problems. These are metaheuristic methods, analytical methods and an hybrid of the previous [40].
The scenario simulation will be carried out with one of these approaches.

This thesis focuses on the experimental side of the joint project.
In order to perform tests on the bidirectional charging station, a laboratory had to be set up in the Energy Center (EC-Lab) of Turin.
The instruments included in the setup are necessary to implement the innovative Power-Hardware-In-The-Loop (PHIL) methodology, through which it

is possible to evaluate the influence of the wallbox in a simulated scenario.
The simulated environment consists in a model of the real electrical grid in which the wallbox will be virtually placed with the purpose of evaluating its performance.
The use of the PHIL method has been increasing during the last years and it is considered already the state-of-the-art for testing devices which operate interfacing the electrical grid [29].
For the PHIL implementation, among the others, essential instruments are the workstation, the real-time simulator and the power amplifier. Each instrument must be tested and the communication with the other ones should be evaluated.

Contextually to the PHIL setup, also a measurement setup must be equipped in the laboratory. For this purpose a data acquisition system must be used to visualize, monitor, record and save the electrical parameters measured by the current probes and by the voltage sensors.
The software data acquisition system should be studied deeply in order to comprehend how to best execute the measurement acquisition during the different tests.

Part of the work developed during the thesis regards the installation of the charging station in the EC-Lab and the relative protection devices commissioning in order to operate safely.

Finally, after all the setup preparation, the V2G charging station will be ready to be tested.
The characterization of the wallbox logic behaviour shall be evaluated through preliminary tests.
Afterwards, some standardized tests to check the compliance with the grid interconnection requisites must be performed.
Tests to evaluate the V2G performance of the charging station should be executed as well.

The final part of the project consists in evaluating the wallbox performance in a business case scenario emulated through the PHIL simulation.

In chapters 2 and 3 are respectively introduced the real-time simulation concepts and the Power-Hardware-In-The-Loop methodology. The charging station, in the form of a wallbox, is going to be tested with these methods.
The wallbox operation will be tested simulating an high fidelity electrical grid. Its Simulink modeling and all the related issues are given in chapters 4

and 5.
To experimentally test the V2G charging station, a laboratory was setup (chapter 6) from the scratch. Its progress is illustreted in chapter 7.
Finally, after some characterization tests to understand the operating logic of the wallbox (chapter 8), some standardized test are performed (chapter 9) in order to evaluate the performances of the charging station.

Chapter 2

Real-Time Simulation

2.1 The what and why of the Real-Time Simulation

As the name suggests, the principle of the real-time simulation is that the simulation lasts as much as the phenomenon would last in the real world. Thus if one second in the simulation has passed, also one second in the real world (wall-clock time) has passed [27].
In this thesis a real-time simulation with discrete-time and constant step duration is performed.
With this type of setting, the simulation time moves forward in steps of equal duration. Alternatively, variable time-step techniques also exist, but are unsuitable for real-time purposes.
At a given time step, mathematical functions and equations are solved. At the end of the proceeding time-step, each variable or system state has been solved.

Another distinction is made between offline and online simulation. The connotation online refers to accomplish the tasks of a certain step, including the interaction with sub-processes and I/O exchange. While term offline does not include interaction with sub-processes because the whole process is simulated, or because the interaction is integrated artificially [27].
In a offline discrete-time simulation, as it is not in real-time, the time required to solve all the system mathematical functions and equations during a specific time-step can be longer or shorter than the time-step duration.
In both situations, an *offline simulation* takes place, as the moment at which the result becomes available is not relevant. Generally, the aim of offline simulation is to obtain the results as fast as possible or to test the model without

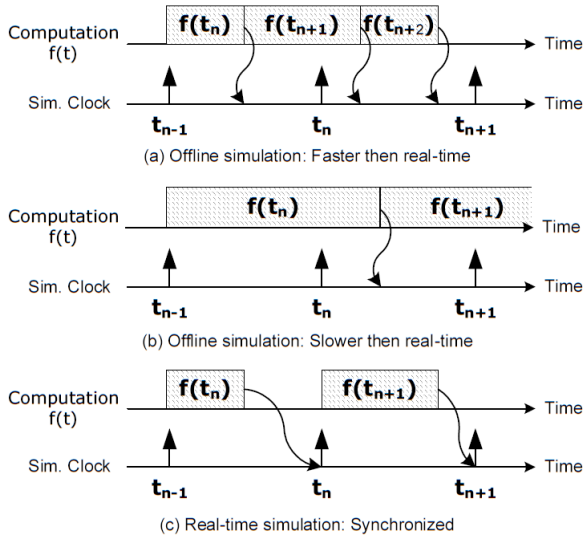

Figure 2.1: Computation comparison between real-time and different techniques [8].

the RTS. Available computation power and mathematical model complexity influence the system solving speed.
However, in real-time simulation, computation accuracy also depends on the time step used to produce results [8].
A real-time simulation is valid if, at a given time step, the time required to compute a solution is shorter than the time-step duration. This allows the simulator to perform its tasks, such as driving I/O to and from external devices.
As the solution is calculated for a given time-step, the time left before the next time-step is called idle-time. In offline simulation, if such situation occurs, the idle time is used to compute already the solution for the next step. In a real-time simulation, it is necessary to wait for the next time-step to begin, to let the computation restart (Figure 2.1 [8]).

Conversely, when the simulator operations are not concluded within the required fixed time-step, an *overrun* occurs, meaning the simulation is considered erroneous.
Therefore can be stated that a real-time simulator performs correctly if the mathematical functions and equations are accurately solved within the time step, thus without the occurrence of overruns [8].

In every time-step, the simulator [8]:

1. reads input and generates outputs;

2. solves model functions and equations;

3. exchanges results with other simulation nodes if any;

4. waits for the next step to begin.

This means that the state of an external device connected to the RTS is sampled just once at the beginning of the simulation time-step. As a consequence, the state of the simulated system is communicated to such external devices also just once per time-step.
For this reason is necessary to meet all the real-time simulation timing conditions, otherwise there could occur discrepancies between the simulator results and the physical counterpart [8].
The size of the time step acquires then importance. It must be chosen accordingly with the model requirement and hardware capability [35].

2.2 Introduction to RT-Lab

The Digital Real-Time Simulator used in this project is the OP5700 from OPAL-RT company. More details about analog I/O connections are given in section 6.3.

The software platform of OPAL-RT's simulators is named RT-LAB.
The RT-LAB interface, where a new model can be created, is shown in Figure 2.2.

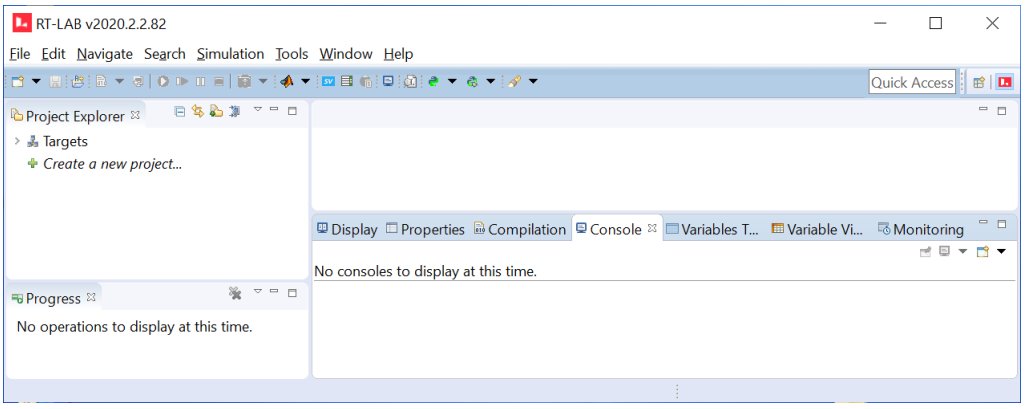

Figure 2.2: RT-LAB main user interface

RT-LAB is fully integrated with MATLAB/Simulink, which act as user designing front-end application.

After developing the model in Simulink, RT-LAB converts the model itself into C-code and loads it to the RTS, assigning the appropriate cores [35].

2.3 Subsystems Assignment

Before executing the real-time simulation online (on the RTS), precise steps are needed [13].
As anticipated, the virtual environment is firstly designed as a model on Simulink.
Then the model must be run correctly in the Simulink environment (offline).
Subsequently the Simulink model has to be be grouped into three types of subsystems in order to run correctly:

- Master Subsystem (SM)
- Slave Subsystem (SS)
- Console Subsystem (SC)

At the Simulink top-level, only these subsystems are allowed.
The two letter initials (SM, SS, SC) are important because must be inserted as prefix of the subsystem block name to be recognized by RT-LAB respectively as master, slave and console subsystem.
SM Master subsystem and SS Slave subsystem contain the computational elements of the model. Each of these subsystem runs in a different core of the simulator.
SC Console subsystem, instead, contains interface blocks to let the user analyze the behavior of the system. Hence it acts as Graphical User Interface (GUI). The console subsystem is the only accessible part of the model while it is running on the simulator, thus here are placed scopes, output displays, switches, etc. [35]
There could be only one master subsystem and one console subsystem, while multiple slave subsystems are possible if needed, according to the cores available on the simulator. The most simple case could be a model where only a master and a console are interacting, thus requiring the computation of only one core. The top-level of this elementary example is shown in Figure 2.3.

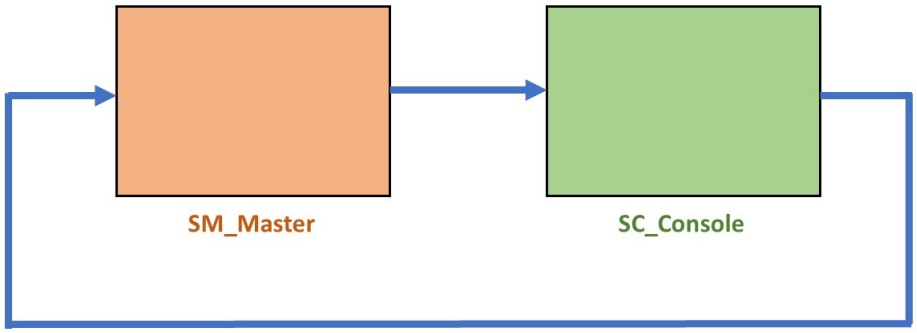

Figure 2.3: Elementary example of top-level Simulink model

As cited before, if the model requires higher computational capacity, it is possible to implement a parallel computation (as done in section 4.2) by using multiple cores of the simulator [12].
In Figure 2.3 is shown an example of a Simulink's top level in which more simulator's cores are employed. It can be noticed that to use multiple cores, multiple computational subsystems must be implemented. Indeed, in comparison with Figure 2.3 a slave subsystem was added. Thus in the example (Figure 2.4) two cores are assigned, one for SM and one for SS.

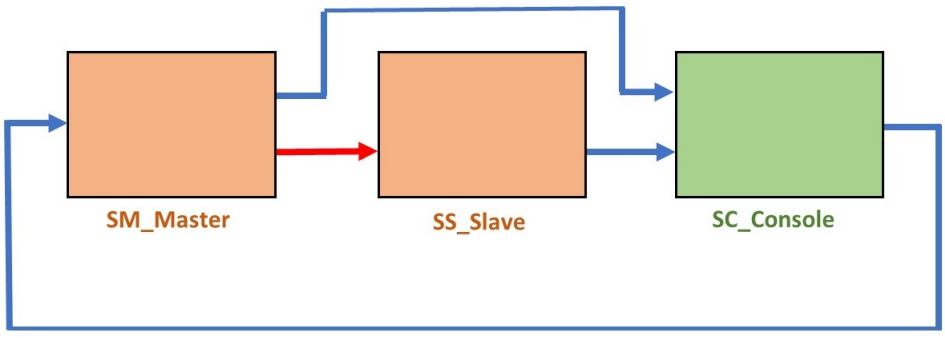

Figure 2.4: Parallel computation example in a top-level Simulink model

2.4 Subsystem communication

In Figure 2.4 it can be noticed two different colors in the communication between the top-level subsystems.
In red is shown the *synchronous communication* while the blue arrows represent the *asynchronous communication*.
The former is the communication type capable of real-time simulation as it is extremely fast. As matter of fact, it is the communication used among CPU cores, so among computation subsystems (SM - SS). The asynchronous type is a slower communication, not capable of real-time simulation. It is the communication between target and host computer, used for data logging and for feedback to user. As a result, the console subsystem communicates with the computation subsystems via asynchronous communication [13].
This happen because, while master and slaves subsystem run on the RTS, the console subsystem runs on the Host computer.

If a subsystem receives a signal from another subsystem, the signal must pass through an *OpComm* block before being processed. This feature is important to synchronize all the signals inside the simulation. The block simulates the behavior of the real-time communication link [23]
It is possible to adjust the number of input ports of the block (Figure 2.5), if multiple signals enter in a subsystem. In this way only an *OpComm* block per subsystem can be employed.
Actually an *OpComm* block cannot read both synchronous and asynchronous signals. Therefore when a computation subsystem receives both these type of signals, to guarantee a correct implementation, two *OpComm* blocks are required, one for each type of signal.
The *OpComm* block must be inserted only after the subsystem is created and properly named. As it is shown in Figure 2.5, both the block display and the mask change according to in which subsystem the *OpComm* is placed.

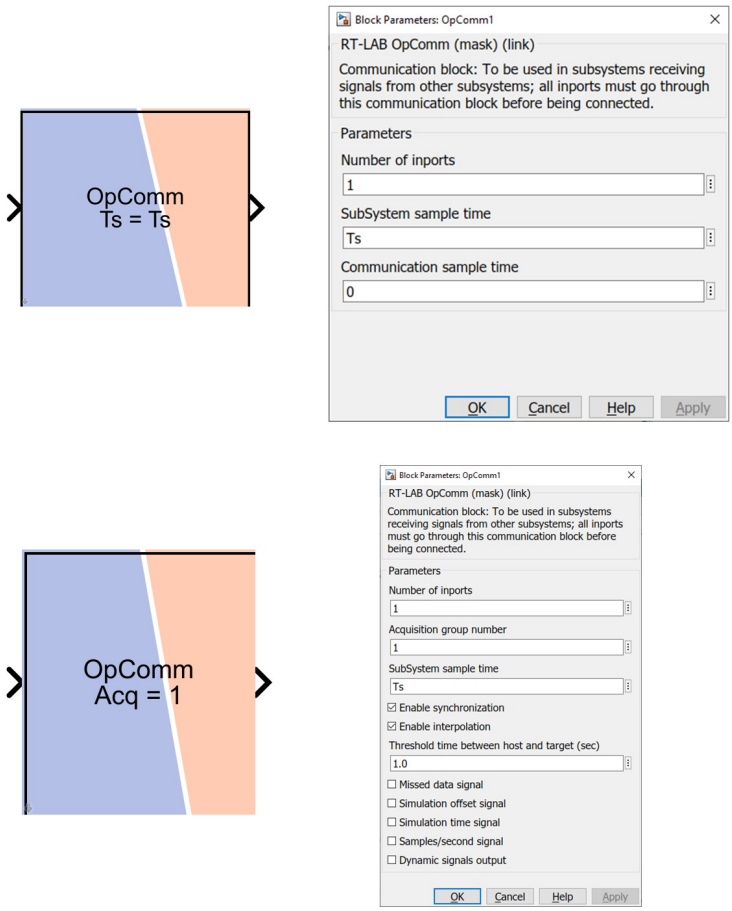

Figure 2.5: OpComm block in computation subsystem (top) and in console subsystem (bottom)

Chapter 3

Power Hardware In The Loop

3.1 What is the Hardware-In-The-Loop simulation?

Installing new grid-connected technologies poses risks as the hardware could act unpredictably when exposed to real-world grid operating conditions, leaving customers without power and potentially damaging components. Utilities and device manufacturers need to understand how new technology will perform under realistic operating conditions before the technology is connected to the grid.
HIL technique offers the ability to validate real hardware components using real-world conditions, simulated through a computer model. Hence, the real device is tested in a virtual environment. The connection is made via I/O interfaces.
Fault conditions and transient scenarios that would be hard to create in real world, are simulated and applied during a test without provoking any damage to the real power system [29]. The DUT interacts with the simulation in a closed-loop environment, creating an high-fidelity model. Signals are measured directly on the DUT and feeded back into the simulation to observe how the tested component influences the environment in which is introduced. In comparison to the traditional testing procedures, HIL simulation is more complex. For instance, it requires more circuitry, such as filtering and compensation components, in order to reduce the noise due to the sensors [29] [46].

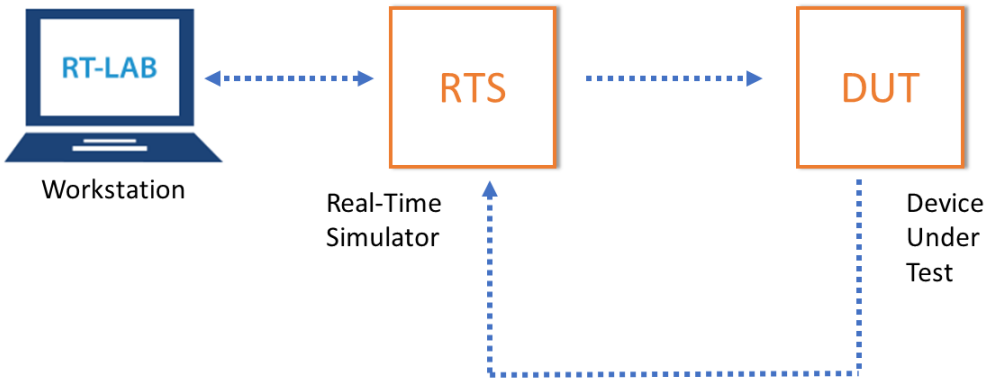

Figure 3.1: HIL principle scheme

In figure 3.1 the components of the HIL technique are showed:

- **Host Computer** : workstation where the virtual environment is implemented as a model. The model is built through a development environment (software) and sent to the RTS where a real-time simulation is held. The host computer represents the human-simulation interface as the user can only make changes on the simulation through this component. In fact, both the modeling and the monitoring are only possible through the software;

- **Real-Time Simulator (RTS)** : represents the center of HIL/PHIL simulation. It makes the real-time simulation possible and the model is executed on its cores.
  It is also called *Target Computer*. *Host* and *Target* Computer communicate with a specific communication protocol (UPD/IP or TCP/IP). In Figure 3.2 is shown the Host-Target connection using the devices employed in the project.
  The Real-Time Simulator also contains I/O interface cards to implement HIL/PHIL simulation. In fact, RTS acts as interface between the PC and the DUT: signals from the virtual environment are supplied to the hardware (output), while signals measured on the DUT are feeded back into the simulation (input).

- **Device Under Test (DUT)** : as explained before, it is the real component to be validated. Measurements are done to monitor the interesting parameters. The measured quantities are converted and then

sent back (feedback) to the workstation, in order to have an impact on the simulation.
Using the real hardware permits to have a more accurate model of the overall simulated system, in comparison to the case in which the DUT is modelized. This is due to the avoidance of approximation errors introduced by the DUT model itself.

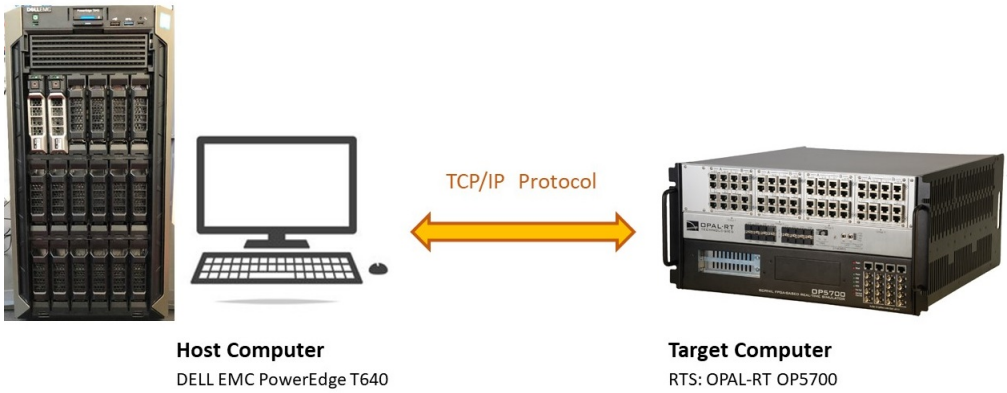

Figure 3.2: Qualitative scheme of the Host-Target connection

Two common variants of the HIL are Controller-Hardware-In-The-Loop (CHIL) and Power-Hardware-In-The-Loop (PHIL).
In the CHIL the element under study is a controller. The CHIL involves the exchange of waveforms between the simulator (virtual environment) and the controller platform (real word) at the signal level, with no real power exchange [33]. It is typically used to test control devices.
When, instead, the experiment requires a bidirectional power flow between the DUT and the virtual environment, a power interface is needed to generate the real voltage or current. In this case it is called PHIL and the power interface corresponds to the power amplifier and a set of sensors to monitor the DUT [36].
PHIL methodology is used in this project.

3.2 What is the Power-Hardware-In-The-Loop simulation?

The difference between the HIL and PHIL consists in the presence of a Power Amplifier (PA).

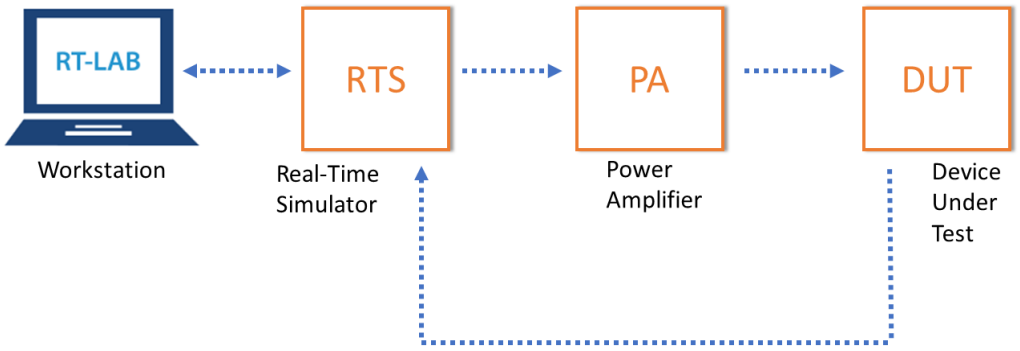

Figure 3.3: PHIL principle scheme

The PA act as an interface between the RTS and the DUT, amplifying the power needed to supply the physical device. In HIL, instead, the hardware device requires a power low enough to make possible a direct connection with the real-time simulator, thus PA is not needed [19].
In other words, aim of the amplifier is to convert in real power the low power signals received from the RTS and aimed to the DUT.

According to the capability of the PA to supply or absorb the active and reactive power to/from the DUT, a distinction is made between 2 and 4 quadrants amplifiers. As the purpose of the project is to evaluate the V2G application, a 4 quadrant PA must be used to either supply and sink power to and from the EV battery.

Another distinction is made between non-linear and linear amplifiers. The power amplifier used was linear, providing very clean waveforms. Linear amplifiers are characterised by high dynamic performance such as fast response time and high bandwidth, meaning shorter time delay in the closed-loop system, leading to less stability problems. Instead, non-linear amplifiers are generally used for MW range because are less expensive.
Other parameters to consider for a correct PA selection are the harmonic distortion level, the slew rate, the protection schemes and the I/O voltages

and currents ranges [29].

3.3 Stability and safety issues in a PHIL system

The Power-Hardware-In-The-Loop methodology requires interfacing between a virtual world and a real one.
The virtual environment can be renamed *Rest of the System* (ROS) and it is connected to the real *Device Under Test* (DUT) [25].

In order to supply power to the hardware under test during the PHIL experiments, a power interface is needed between the hardware and the virtual system.
The power interface mainly consists of two components: a power amplifier and the sensors, which measure the DUT electrical parameters and fed this information back to the ROS.
An ideal power interface is invisible to the system, because it introduces less errors if the overall system does not perceive the disjunction between the virtual and real systems.
In reality this cannot happen since it is not possible to have zero time delay, unity gain and infinite bandwidth.
The power interface creates an additional little closed loop system, which could injects errors, time delay and distortion. In turn, this would cause instability issues and loss of simulation fidelity (inaccurate results) [28].

Interface Algorithms (IAs) are used to counteract these instability problems. The correct choice of the IA increases PHIL stability and result accurateness.
Indeed it is possible to reach a stability region according to the right IA topology and parameters used [28].
The most common IA is the voltage type *Ideal Transformer Model* algorithm (ITM) illustrated in Figure 3.4. This is the IA in use in our PHIL setup.

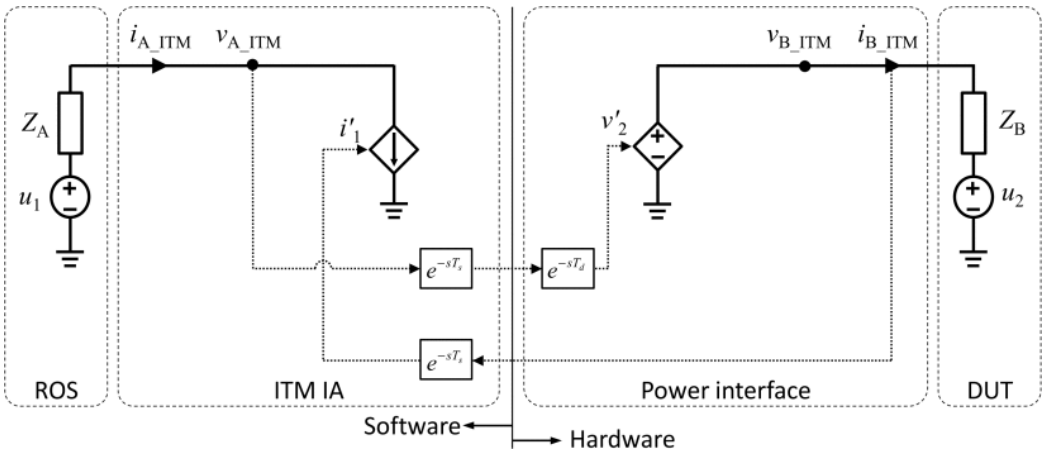

Figure 3.4: Ideal Transformer Metod (ITM) topology (voltage type) [25]

The voltage type ITM reflects our setup: the supply voltages, present at the node where the wallbox is placed, are sent to the RTS. The RTS passes the scaled signals of the voltages to the power amplifier which amplifies them and supplies the wallbox (DUT). In the previous figure can be seen that a controlled voltage source is placed in the power interface circuit.
Through the DAQ the currents flowing into the DUT are measured and then fed back into the simulation (ROS). Here are modeled as a controlled current source.

During the tuning of the PHIL setup, instability problems were faced. In section 5.3.2 is described the solution based on the ITM interface algorithm.

More details about the stability issues and interface algorithms are available in literature [25],[38],[15].

Verifying the safety of the system is also essential for PHIL implementation. First of all, the software safety depends on the system stability mentioned above. Therefore, before connecting the real DUT, the device must be simulated, represented in the model through a load.
In other words, as first thing it is necessary to simulate the PHIL experiment without real components in order to check the system response.
If the simulated PHIL experiment provides a negative response no components were damaged, and the user is able to make changes on the model.
Only when the response is positive, the simulation can include the real hardware.

A second form of safety is the hardware protection, intended as all the involved equipment: RTS, PA, DAQ, DUT, etc...
The user must verify that the electrical quantities under study are below certain limits declared by the instruments manufacturer.

Chapter 4

Modeling of the electrical network

The model of a real electrical network was elaborated in a previous Thesis by Dr. Stefano Frittoli [19], who worked in the same PoliTo research group as myself.
To be more precise, aim of the colleague was to execute remote Co-Simulations. Therefore, the model inherited was thought to be simulated on many different RTDS, while our target is to run the model in a single OPAL-RT simulator.

Keeping the model as it was originally meant a substantial computational burden, leading to overruns and a failed simulation. Since if the extension of the network reduces, the computational burden also reduces, we had to simplify the network to make it run without issues on the only three available cores of the simulator.

In this chapter the modifications respect the original Simulink model are commented.
Afterwards, a general recap of the model topology is given.
At the end of the chapter, particular interest is addressed to the explanation of the interaction with the wallbox in order to implement the Power-Hardware-In-The-Loop methodology.

4.1 Network topology

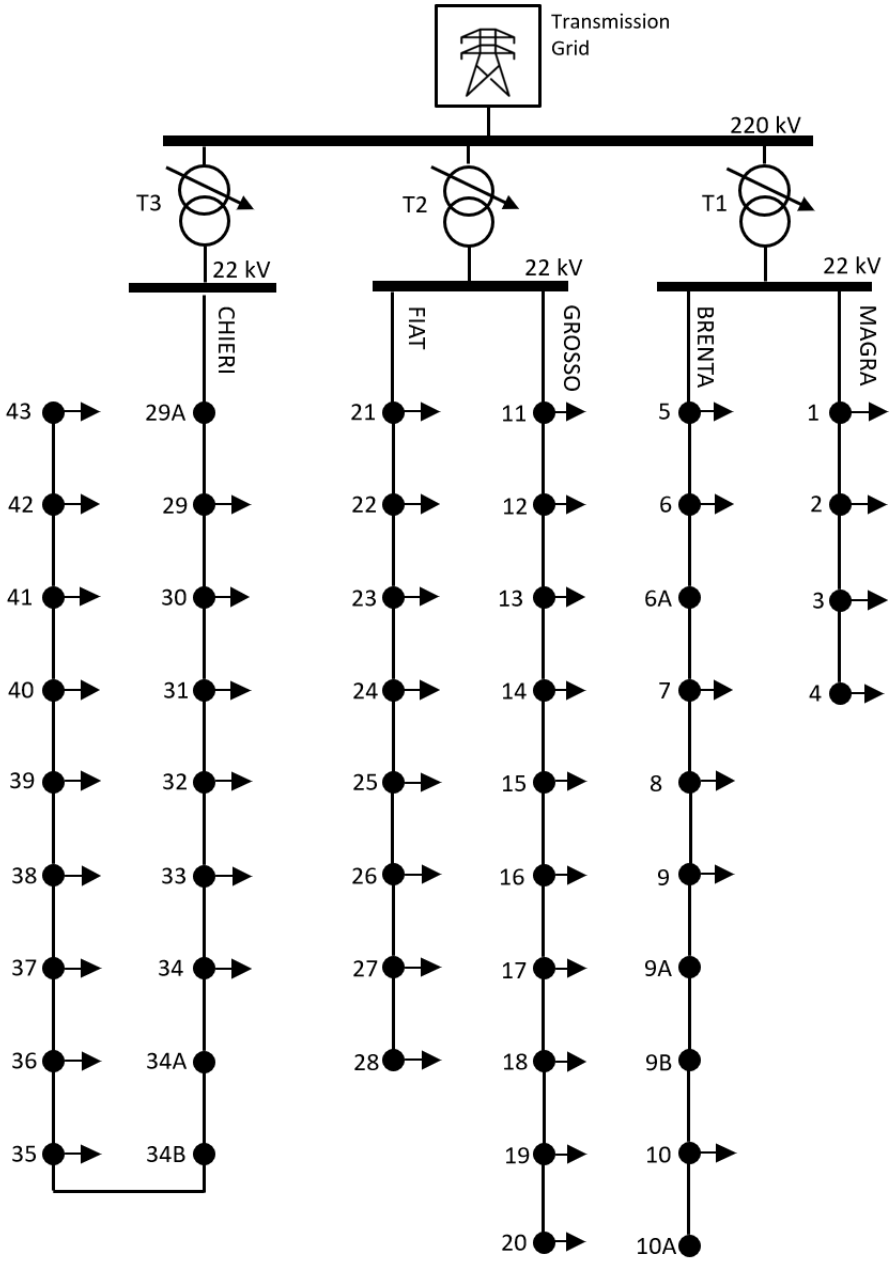

Figure 4.1: Qualitative representation of the original analysed electrical grid [19].

A qualitative representation of the electrical grid [19] is shown in Figure 4.1. The numbered dots represent the MV/LV substations.

The analysed electrical system is a portion of the electrical distribution grid departing after Stura HV/MV substation. Real data were provided by Turin DSO.
The HV network (220 kV) behind Stura primary substation is beyond the consideration of the project, thus is considered ideal and simply modeled with a Thevenin equivalent circuit.
The HV network model is then composed of two elements: a three-phase voltage generator with its internal impedance and an equivalent RLC impedance (RL series, C parallel) of the trasmission grid. The Simulink model of the HV network is shown in Figure 4.2 .

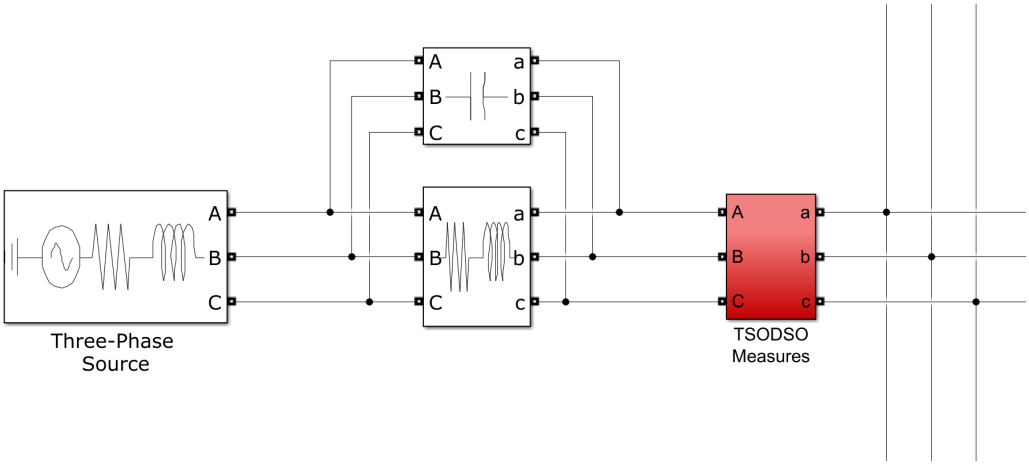

Figure 4.2: HV network equivalent model

Then, the electrical primary substation is composed of three HV/MV (220 kV - 22 kV) transformers. The first (T1) and third transformer (T3) have a nominal power of $S_N = 63\,\text{MVA}$, while the second one has $S_N = 55\,\text{MVA}$.
The parameters of the HV/MV transformers were also provided by Turin DSO [7] and are respectively listed in Table 4.1 and Table 4.2.

Table 4.1: Parameters of Magra-Brenta (T1) and Chieri (T3) transformers

Parameter	**Value**	**Meas. Unit**
Rated Power	63	MVA
Nominal frequency	50	Hz
Primary winding nominal voltage	220	kV
Secondary winding nominal voltage	22	kV
Primary winding resistance	0.5511	Ω
Primary winding inductance	0.1947	H
Secondary winding resistance	1.4627	Ω
Secondary winding inductance	0.1604	H
Magnetization resistance	$1.1607 \cdot 10^6$	Ω
Magnetization inductance	$1.0736 \cdot 10^4$	H
Leakage reactance	0.1593	p.u.
No load losses	$6.619 \cdot 10^{-4}$	p.u.
Copper losses	0.0022	p.u.

Table 4.2: Fiat-grosso (T2) transformer

Parameter	**Value**	**Meas. Unit**
Rated Power	55	MVA
Nominal frequency	50	Hz
Primary winding nominal voltage	220	kV
Secondary winding nominal voltage	22	kV
Primary winding resistance	0.0110	Ω
Primary winding inductance	0.0019	H
Secondary winding resistance	0.0146	Ω
Secondary winding inductance	0.0016	H
Magnetization resistance	$6.45936 \cdot 10^5$	Ω
Magnetization inductance	$4.56498 \cdot 10^2$	H
Leakage reactance	0.1146	p.u.
No load losses	$6.617 \cdot 10^{-4}$	p.u.
Copper losses	0.0033	p.u.

All three HV/MV transformers have a three-limb core and their winding connection is delta-wye. The neutral point of the secondary winding of the transformers is insulated.

From the Stura substation depart five MV distribution feeders. In particular, T1 supplies MAGRA e BRENTA feeders, T2 supplies FIAT and GROSSO feeders, while from T3 the feeder CHIERI departs (Fig. 4.1).

4.2 Subsystems and cores assignment

In order to implement correctly the realtime simulation, it becomes necessary to decouple the network taken into consideration in more subsystems. Every subsystem will be computed by a different core of the OPAL-RT simulator. The OPAL 5700 at our disposal has three cores available, thus the network can be split in three subsystems accordingly on what has been told in section 2.3.
That means there will be one Master Subsystem (SM) and two Slave Subsystems (SS). A recap is given in Table 4.3.
The console block is named "SC_Console" and, as said in section 2.3, it is useful for the visualization of parameters and waveforms, but also to maneuver switches. This block does not require computation, so is not related to a core.

Table 4.3: Core Partition

Core	*Subsystem Name*	*Subsystem Type*
Core n°1	SM_HV	Master
Core n°2	SS_MAGRA_BRENTA	Slave
Core n°3	SS_FIAT_GROSSO	Slave

The core partition represents the first difference with the model inherited. In fact, the starting model was divided in 4 different subsystems as can be seen in Figure 4.3 [19].
To reduce the number of subsystems from 4 to 3, the whole CHIERI feeder is now simplified in a electrical equivalent node and put into the Master Subsystem (Figure 4.4).

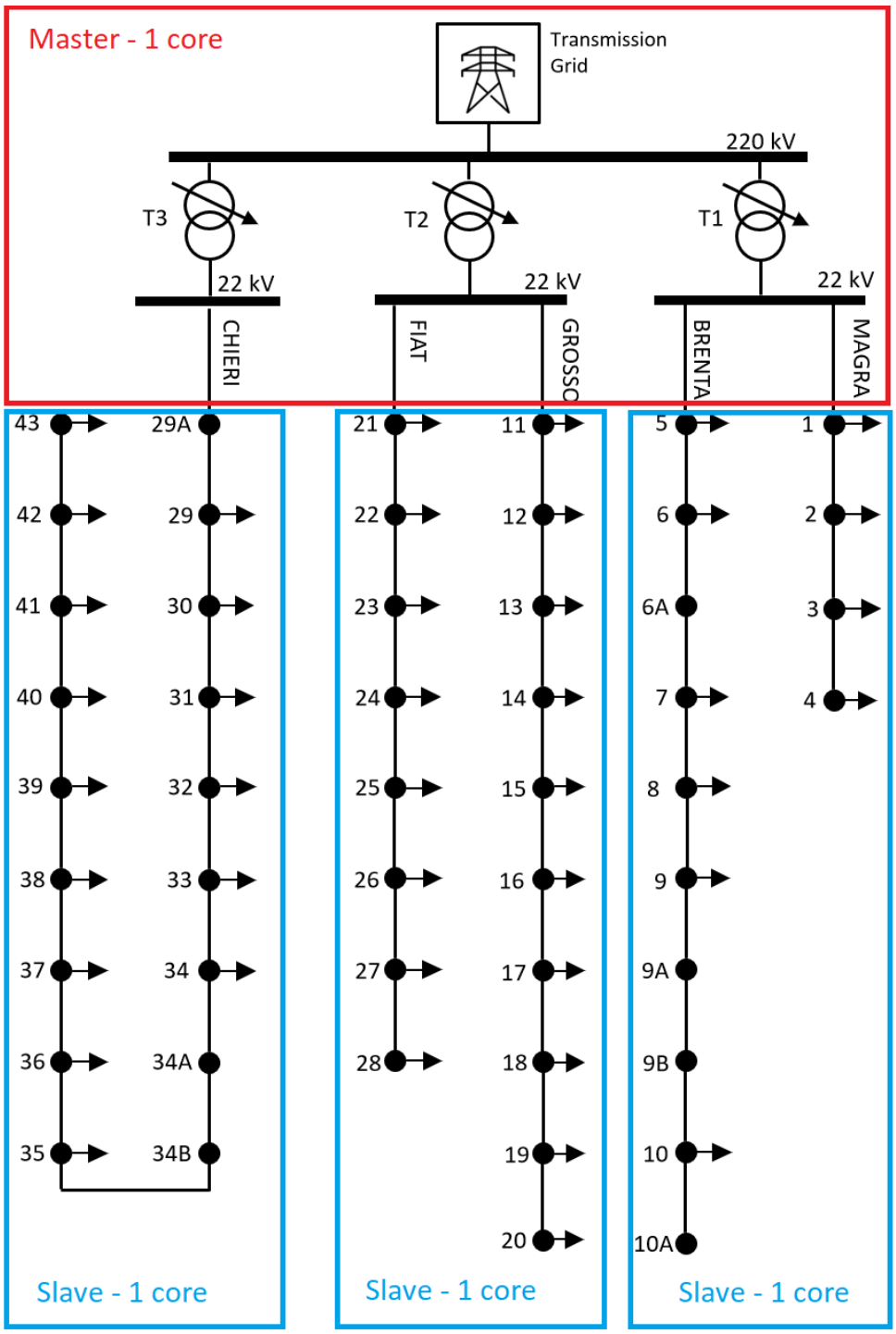

Figure 4.3: Qualitative representation of the original analysed electrical grid with the decoupling in subsystems.

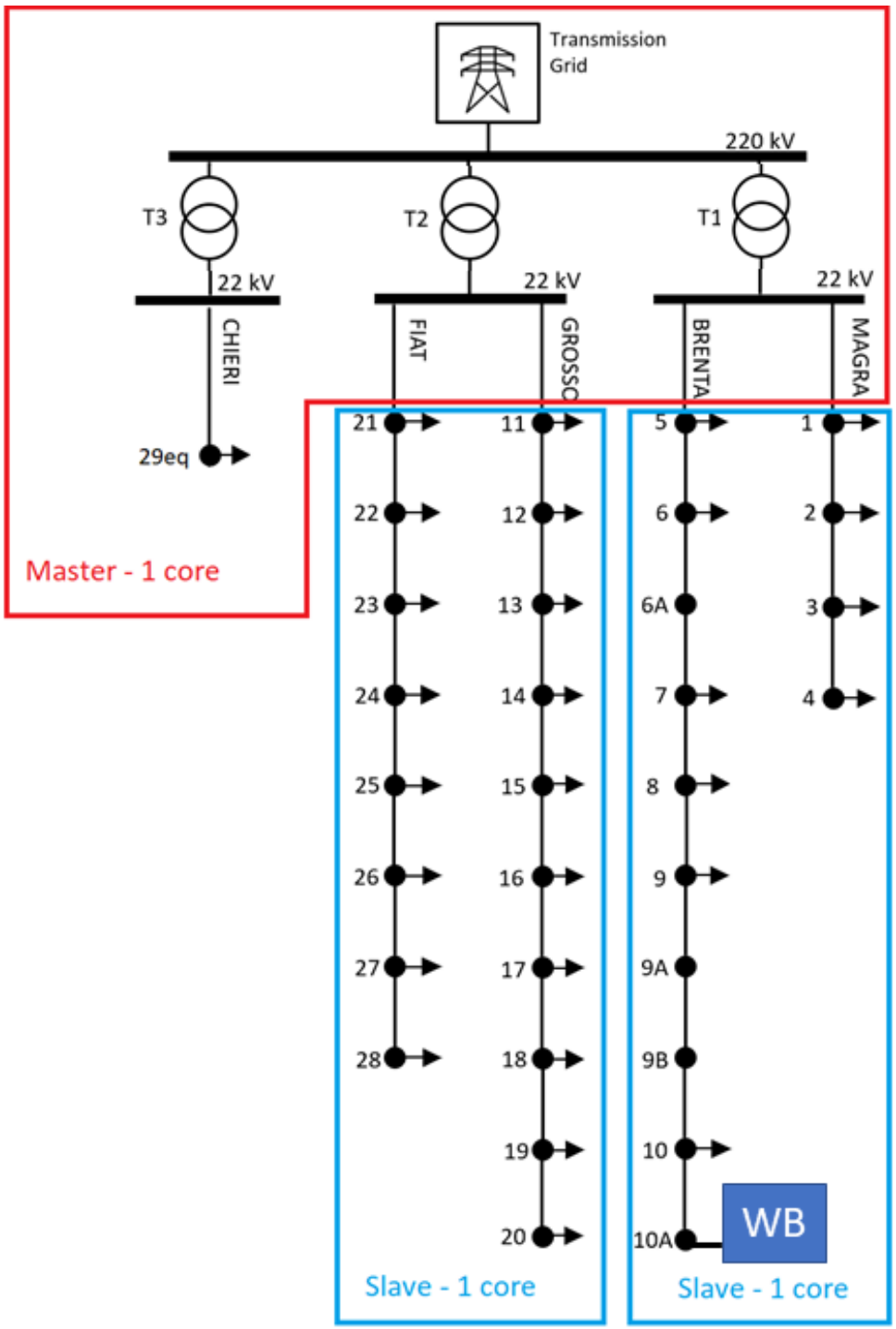

Figure 4.4: Qualitative representation of the new analysed electrical grid with the decoupling in subsystems.

The schematic representation illustrated above is clearly reflected into the Simulink model (Figure 4.5).
The Console subsystem, which does not require a core computation, it is also visible.

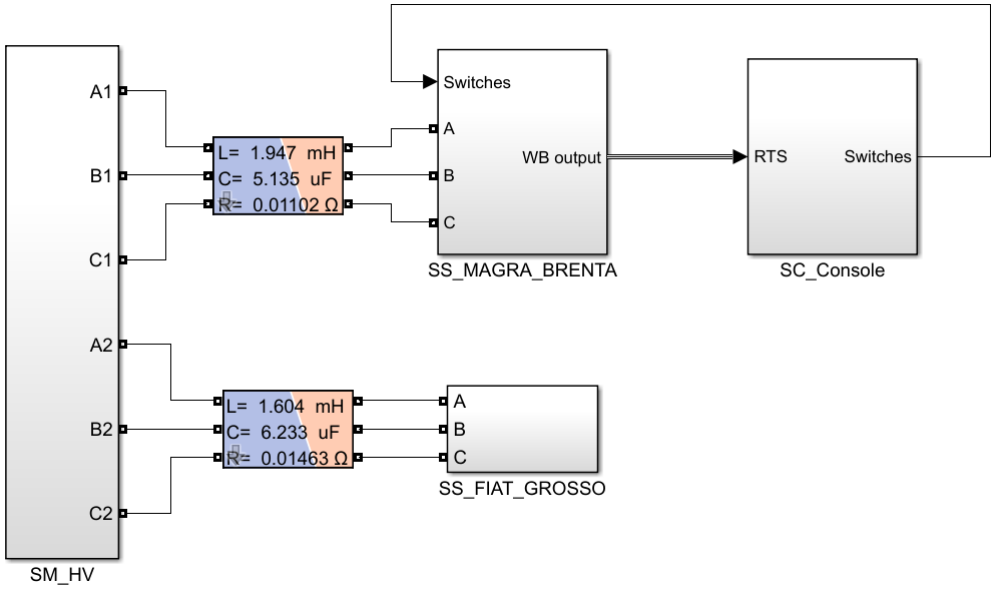

Figure 4.5: Subsystems overview.

As may be noted, the master is connected to each slave subsystems through a block named *Stubline* from Artemis library.
This block is the one responsible for decoupling and separating computational tasks on different cores.
It is located on the top-level of the Simulink model and indeed its outports are connected to subsystem blocks (which names begin with SS or SM).
Purpose of Stubline is to implement an N-phase distributed parameters transmission line model with exactly one-time step propagation delay.
This block is optimized for real-time simulation and is based on Bergeron's travelling wave method [21].

Stubline method has an acceptable accuracy and high effectiveness if, as in this case, is used next to a transformer.
A common usage, as we did considering the HV/MV transformers (T1, T2) in the Master subsystem, is to remove the secondary leakage inductance (and the secondary series resistance) from the Transformers block parameters. These values are then inserted into the Stubline block placed right

downstream, outside the Master subsystem. This move will introduce automatically, inside the Stubline block, a capacitance whose value is adjusted to obtain an exact one-time-step delay of propagation [12].
The calculations to obtain the capacitance of the Stubline block C_{stub} are explained in the equations 4.1 and 4.2, where T_s is the step time and L_{stub} is the inductance of the Stubline block, which corresponds to to the secondary leakage inductance of the transformer upstream.

$$C_{stub} = \frac{T_s^2}{L_{stub}} \tag{4.1}$$

from:

$$T_s = \sqrt{L_{stub} \cdot C_{stub}} \tag{4.2}$$

Then, it is required to compensate the capacitance contribution from the Stubline block, which is just a computational effect but not a real element.
This issue was solved introducing a three-phase shunt inductance in one of the two subsystems connected by the Stubline block.
In Figure 4.6 is shown the solution applied for the Stubline between the Master and the Magra-Brenta subsystem.
The solution is replicated also for the Stubline before Fiat-Grosso subsystem. Obviously there is no need to implement a shunt inductance downstream of T3 because the Stubline block was not placed. As a matter of fact, Chieri feeder is located inside the Master subsystem itself.

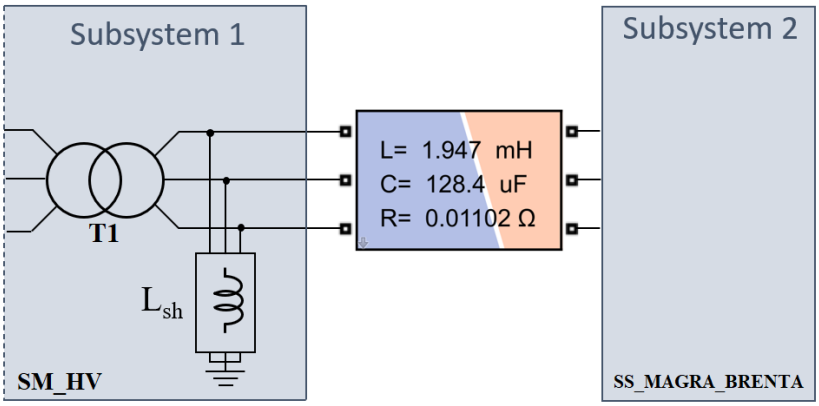

Figure 4.6: Reactive compensation of Stubline block from T1.

From the following equations (4.3 and 4.4), the value of the shunt inductance is finally deduced [19]. V is the voltage right downstream of the transformer. $X_{C_{stub}}$ is the capacitive reactance of the Stubline block and $X_{L_{sh}}$ is the inductive reactance of the shunt inductor. These two reactances have the same value, due to the equivalence of $Q_{L_{sh}}$ and $Q_{C_{stub}}$, which are the reactive powers of the shunt inductance and of the Stubline block (only capacitive side) respectively.
ω is the system's angular frequency.

$$Q_{L_{sh}} = 3 \cdot \frac{V^2}{X_{L_{sh}}} = Q_{C_{stub}} = 3 \cdot \frac{V^2}{X_{C_{stub}}} \tag{4.3}$$

$$L_{sh} = \frac{1}{\omega^2 \cdot C_{stub}} \tag{4.4}$$

The Master Subsystem is shown in Figure 4.7, where the transformers described in section 4.1 are also visible. It can be noticed the presence of the inductances downstream of T1 and T2 transformers. The four red boxes represent the measurement blocks to acquire the electrical parameters.

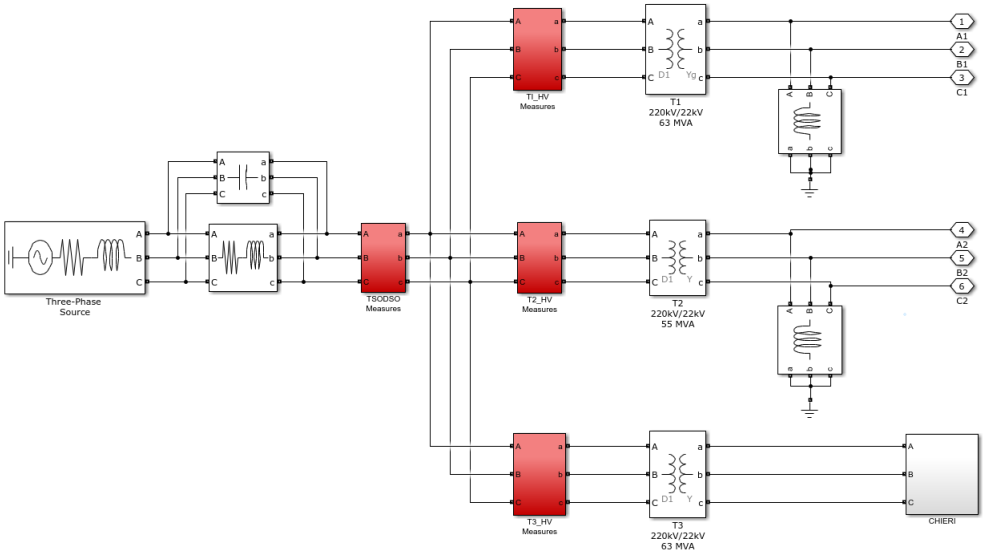

Figure 4.7: Master Subsystem

4.3 SSN Parallelization

Apart from Stublines, another decoupling method has been applied to enhance the realtime simulation. The method is the SSN (State-Space Nodal) Parallelization.
SSN uses internal threads to compute in parallel part of its algorithm, the group calculations, chosen by the user through some interface blocks. In other words, this method allows to break circuit equations in smaller parts to compute them in parallel, reducing the computation time.
Differently from the Stubline or other decoupling methods, which exchange data between two consecutive time steps, in the SSN method the parallelization occurs within the time step [12].
To apply SSN method, *SSN block* and *SSN interface block* from Artemis library need to be introduced inside the Simulink model (Figure 4.8).
The SSN Interface block is always followed by the *SSN group tag* which is the green rectangular box. This element is used to identify a specific SSN group in the prompt listing.

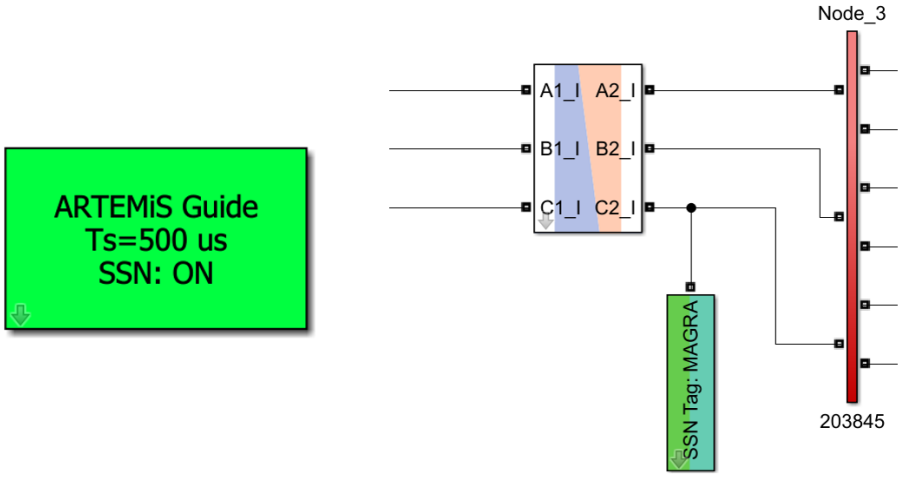

Figure 4.8: SSN block (left) and SSN Interface block (right). [19]

The SSN block is inserted at the top level of the model, while the SSN interface blocks are placed inside the two Slave subsystems.

In the following figure is shown the electrical grid highlighting the division in subsystems and groups (olive green boxes).

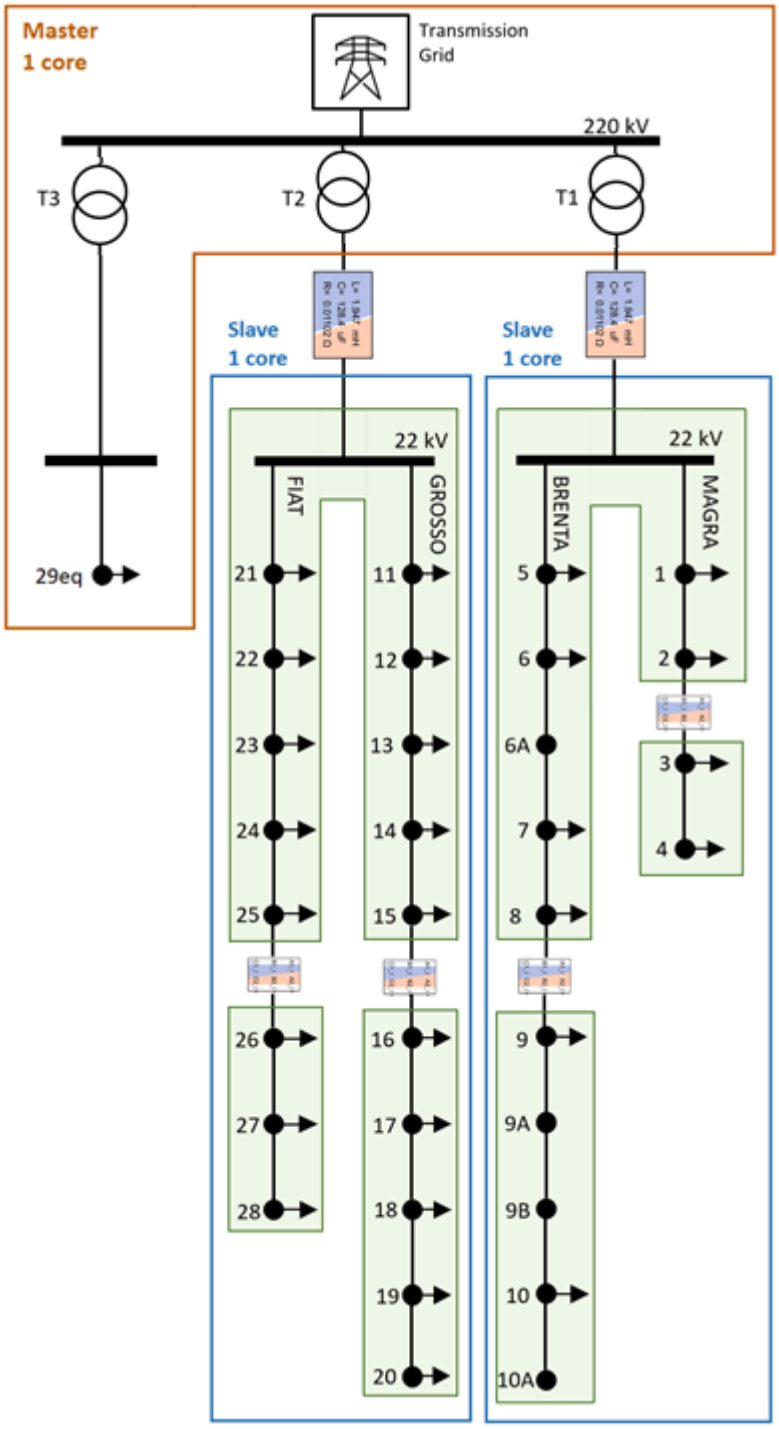

Figure 4.9: Qualitative representation of the new analysed electrical grid with the decoupling in subsystems and groups.

More details on the theory behind the SSN method can be found in [16].

4.4 Calculation monitoring and model simplification

After the reduction from 4 to 3 subsystems through the simplification of Chieri feeder, a second difference from the model inherited from [19] is the OLTP (On-Load Tap Changer) absence.
To be more detailed, originally the transformer T2 supplying Fiat and Grosso feeders was a variable ratio transformer. But this block required a huge computational effort.
In our model, since the usage of a OLTC is not useful for our purposes, we replaced this complex transformer with a simple fixed ratio transformer, keeping the nominal parameters of the previous one. Without this simplification, the model could not run correctly on the real-time simulator because the computational time was higher of the step time, causing overruns.

The block *OpMonitor* played a key role in solving this issue (Fig. 4.10). This block from the RT-LAB library provides information on the subsystem where it is placed. To our interest, the useful output are the computation time, the real step size and the number of overruns.

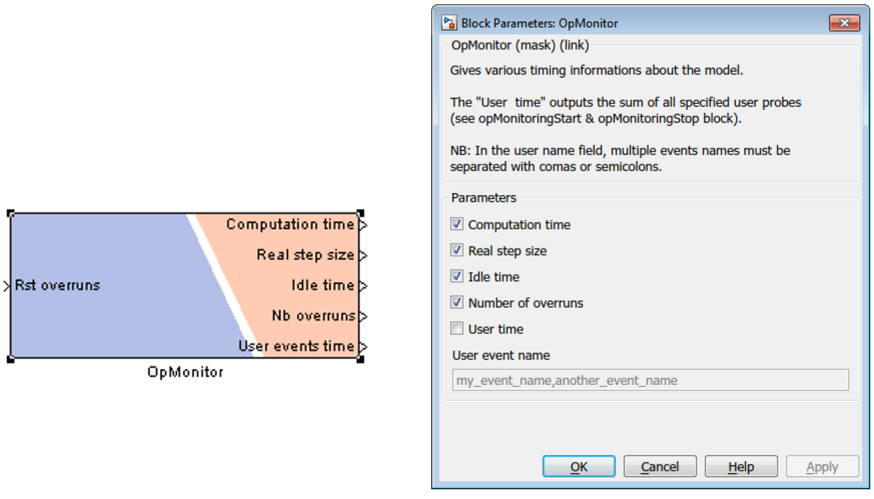

Figure 4.10: OpMonitor block (left) and its mask (right).

When the OLTC was still present in the SM_HV subsystem, an OpMonitor was inserted inside each subsystem (SM_HV, SS_MAGRA_BRENTA,

SS_FIAT_GROSSO) to evaluate the burden on each core. The output signals of each OpMonitor were transmitted to the Console where could be visible during the simulation. Result was a big number of overruns occurring only in the Master subsystem, where the OLTC was placed.
After the replacement with a fixed-ratio transformer, the overrun issue was completely solved. As matter of fact the computation time in SM_HV is now significantly lower. Actually in the all three subsystems the computation time is even lower than the idle time.

4.5 Loads

Every black dot in Figure 4.1 represents a MV/LV substation, modelled as a load. For each load, the values of active and reactive power installed were given by the Turin DSO. However, it is known that power absorption varies according to the node voltage. Hence, to implement a voltage-dependent load model, the ZIP load model has been chosen.
Equations describing ZIP load follow:

$$P(V) = P_0 \left[Z_p(\frac{V}{V_n})^2 + I_p(\frac{V}{V_n}) + P_p \right] \tag{4.5}$$

$$Q(V) = Q_0 \left[Z_q(\frac{V}{V_n})^2 + I_q(\frac{V}{V_n}) + P_q \right] \tag{4.6}$$

For a specific voltage:

- $P(V)$ and $Q(V)$ are the active power and reactive power values;
- P_0 and Q_0 represent the values at nominal voltage;
- Z_p and Z_q are the coefficients at constant impedance;
- I_p and I_q are the coefficients at constant current;
- P_p and P_q are the coefficients at constant power.

Generally, loads are distinguished between residential, commercial and industrial type.
In [19] each load has been assigned one type (Table 4.4).
Consequently, the ZIP model coefficients for each type of load (residential, commercial and industrial) have been chosen (Table 4.5).

Table 4.4: Type of load for each distribution node [19].

Type of load	Node number
Residential	5, 8, 10, 17, 19, 20, 26, 34, 35, 36, 37, 40 41, 42, 43
Commercial	4, 6, 7, 9, 13, 15, 16, 18, 23, 24, 27, 28, 31 32, 33, 38, 39
Industrial	1, 2, 3, 11, 12, 14, 21, 22, 25, 29, 30

Table 4.5: ZIP coefficient for each type of load [19].

Type of load	P_p	I_p	Z_p	P_q	I_q	Z_q
Residential	1.21	-1.61	1.41	4.35	-7.08	3.72
Commercial	0.76	-0.52	0.76	6.92	-11.75	5.83
Industrial	1.5	-2.31	1.81	7.41	-11.97	5.55

For demonstrative purposes, in Figure 4.11 is shown the Simulink representation of an entire feeder with its loads.
At each node is present a load with its active and reactive power measurements.
Between the nodes is visible a three-phase PI transmission line block.
The topology respects the scheme in Figure 4.9. In particular, between node 2 and node 3 is visibile the SSN Interface block.

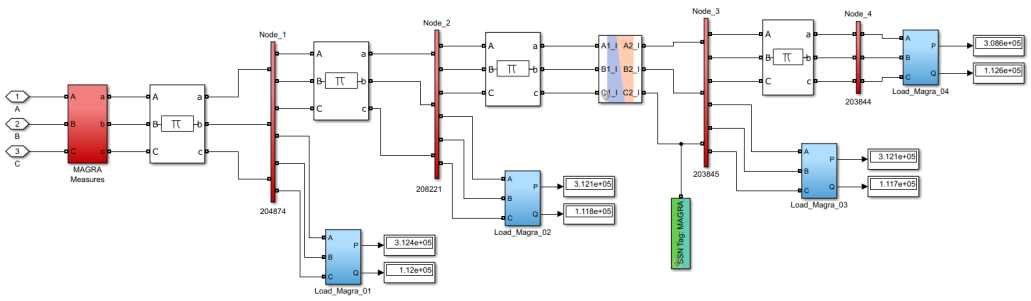

Figure 4.11: Magra feeder.

4.6 Network model overview

At this point it is necessary to recap the model topology from the Simulink perspective.

4.6.1 Top-Level and Master subsystem

In Figure 4.12 is proposed again the top-level of the Simulink model:

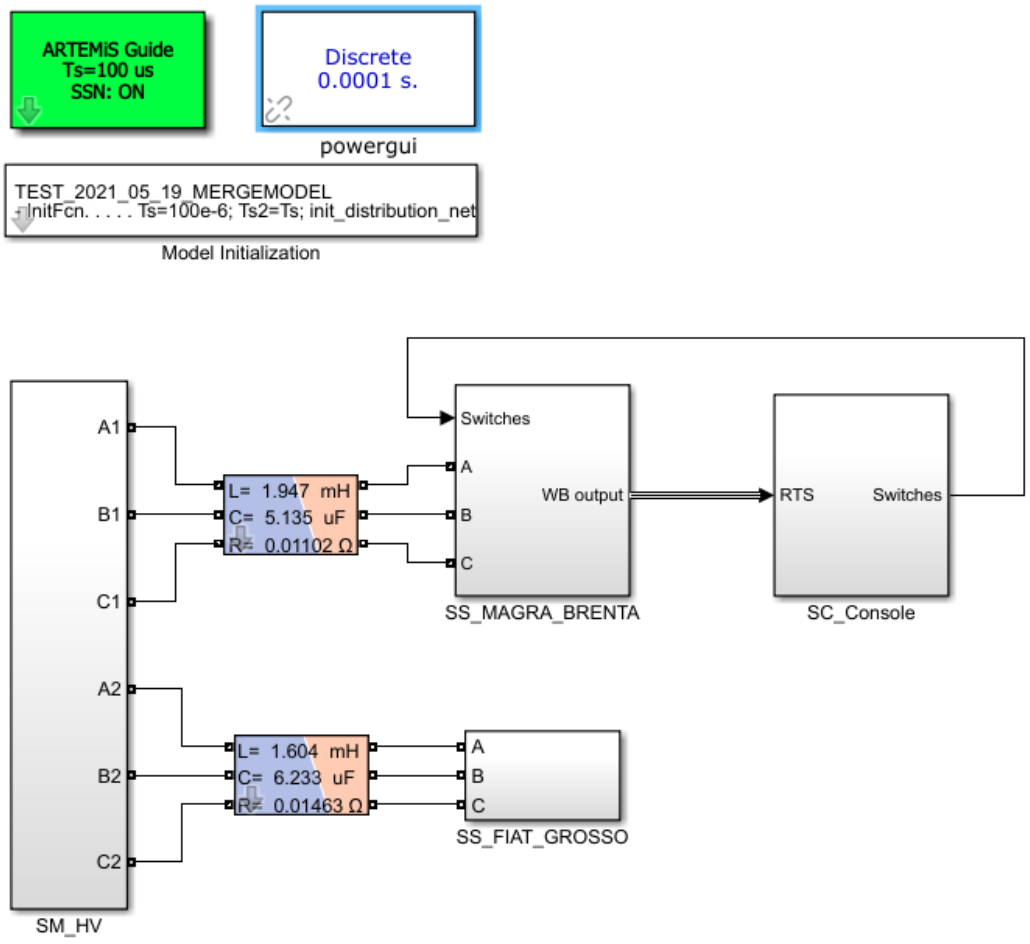

Figure 4.12: Top-level of the Simulink model.

In the upper part are visible:
- *Artemis* block, (introduced in 4.3);
- *Model Initialization* block, which initializes all the parameters written and

calculated in the relative matlab script;
- *Powergui* block, which sets the simulation type (discrete) and the simulation parameters (sample time: 0.0001 s). Other preferences are available.

Inside the Master subsystem it is implemented the equivalent HV network, the three HV/MV transformers and the equivalent block of the Chieri feeder (Fig. 4.14).

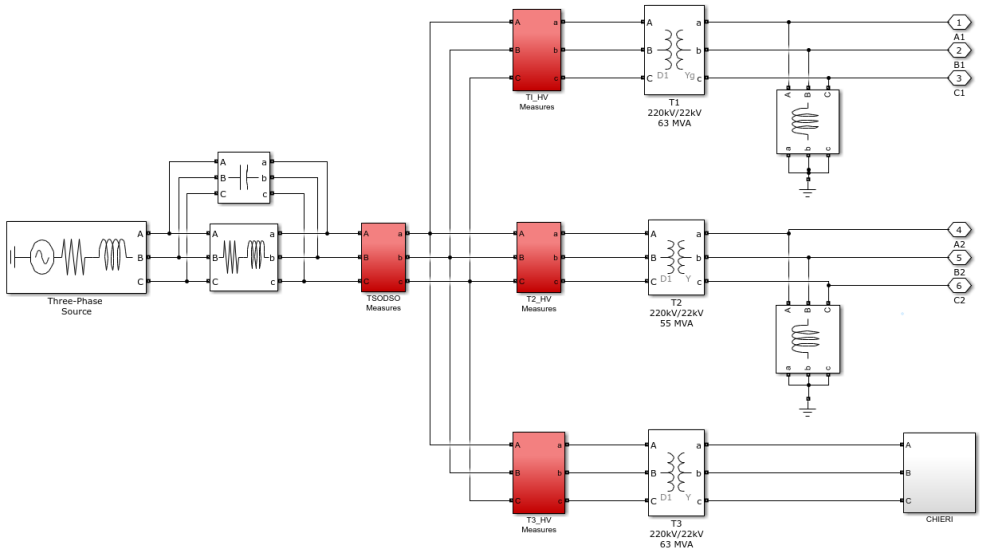

Figure 4.13: Master Subsystem.

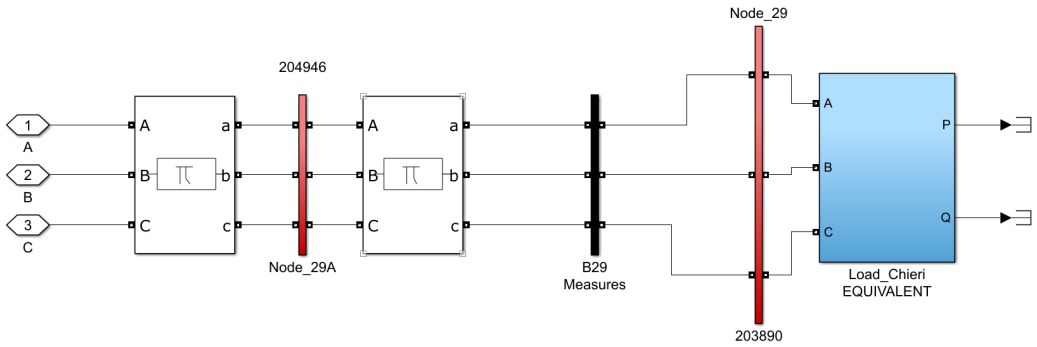

Figure 4.14: Chieri equivalent feeder.

4.6.2 Slave subsystem: Fiat_Grosso

Coming inside the Fiat_Grosso subsystem (Figure 4.15) it is possible to look into the Fiat feeder (4.16) and the Grosso feeder (Figure 4.17).

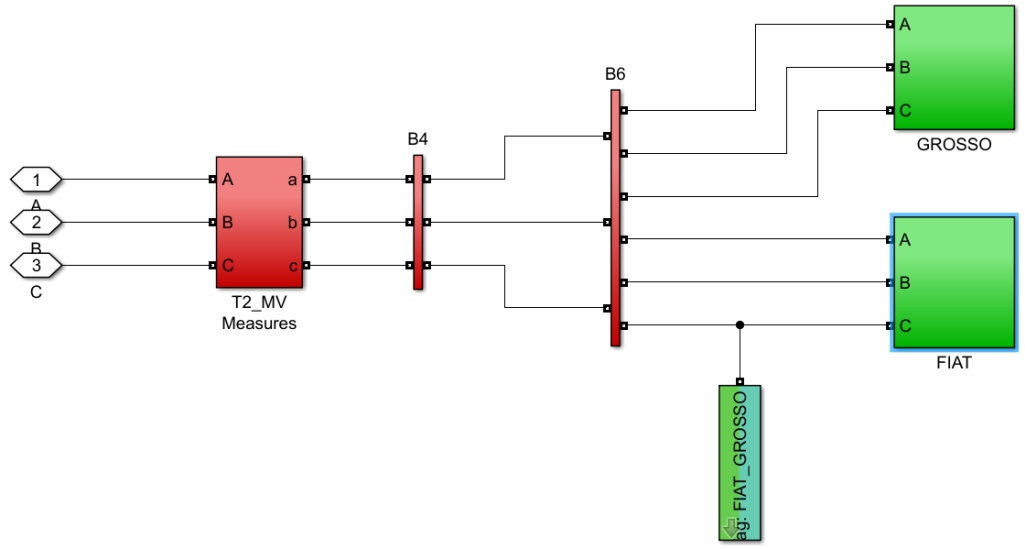

Figure 4.15: Fiat-Grosso Subsystem.

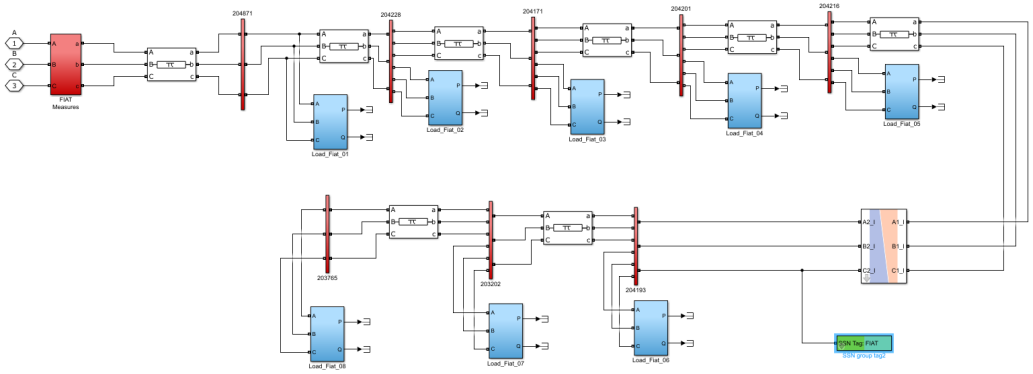

Figure 4.16: Fiat feeder.

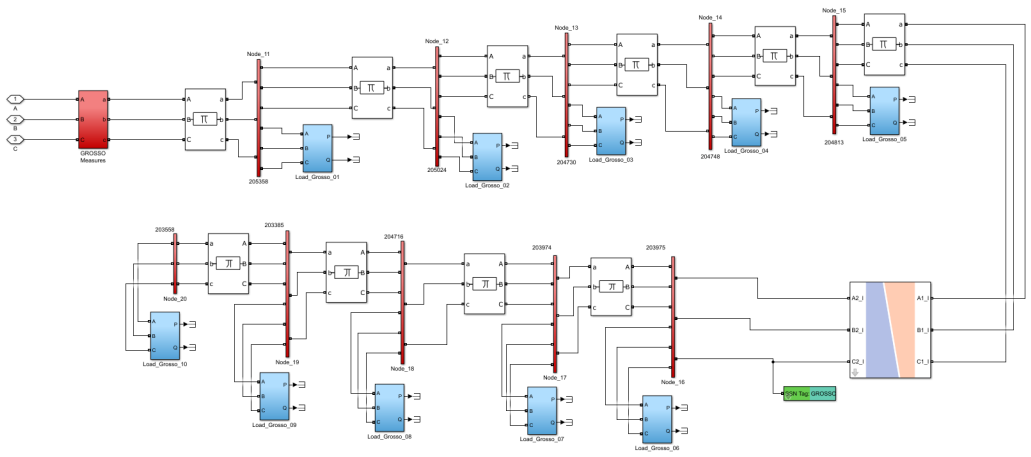

Figure 4.17: Grosso feeder.

4.6.3 Slave subsystem: Magra_Brenta

A similar perspective is offered by the Magra_Brenta subsystem (Figure 4.18). Differently from Fiat_Grosso subsystem, in this one the presence of the Opcomm block is relevant. The component is responsible for the acquisition of the switches signals coming from the Console subsystem.
Furthermore, it can also be noticed the *WB output* port, which is connected to the Console subsystem in the upper layer.
Both these differences are due to the fact that the V2G charging station to be tested is virtually placed into the Brenta feeder.
Therefore the signals passing through the Opcomm block are destined to the WB, and the output port exports parameters concerning the charging station.
More details about the wallbox connections are given in chapter 5.

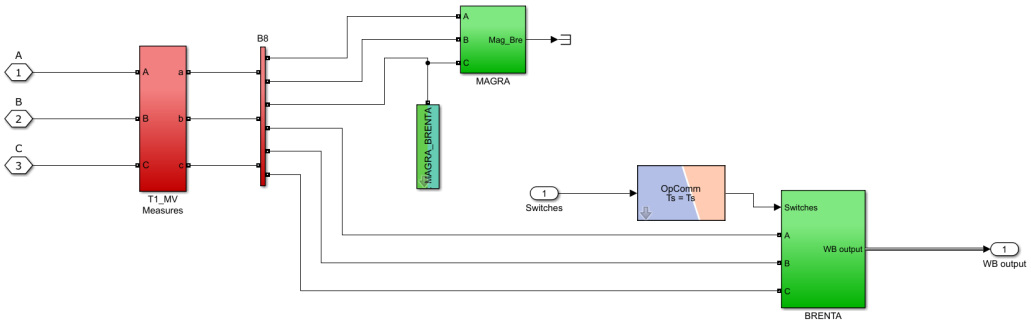

Figure 4.18: Magra-Brenta Subsystem.

From the Magra_Brenta level it is possible to view the Magra feeder (Figure 4.19) and Brenta feeder (Figure 4.20).
In the latter it can be noticed the wallbox subsystem at the end of the feeder, as if it was an additional load.

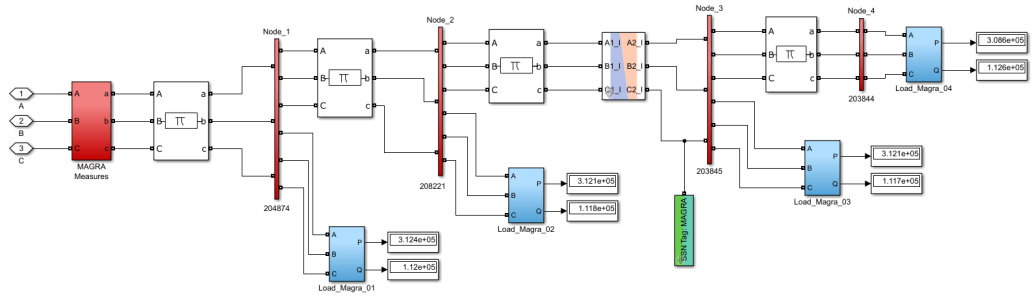

Figure 4.19: Magra feeder.

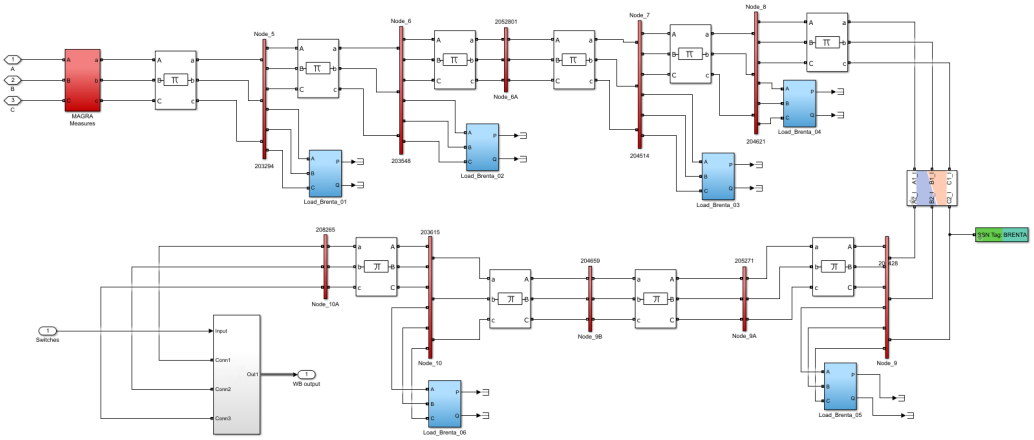

Figure 4.20: Brenta feeder.

4.6.4 Console Subsystem

The Console subsystems contains the *Scope* blocks in order to visualize the waveforms of the interesting parameters.
The Console subsystem communicates only with the Magra_Brenta slave subsystem (see previous Figure 4.12), that is the subsystem from which it receives the parameters to be visualized.

In the console subsystem are also available the logic switch that can be maneuvered by the user during the simulation.

These switches allow the user to choose the load, passing from a simulated load to the real one (DUT) or viceversa.

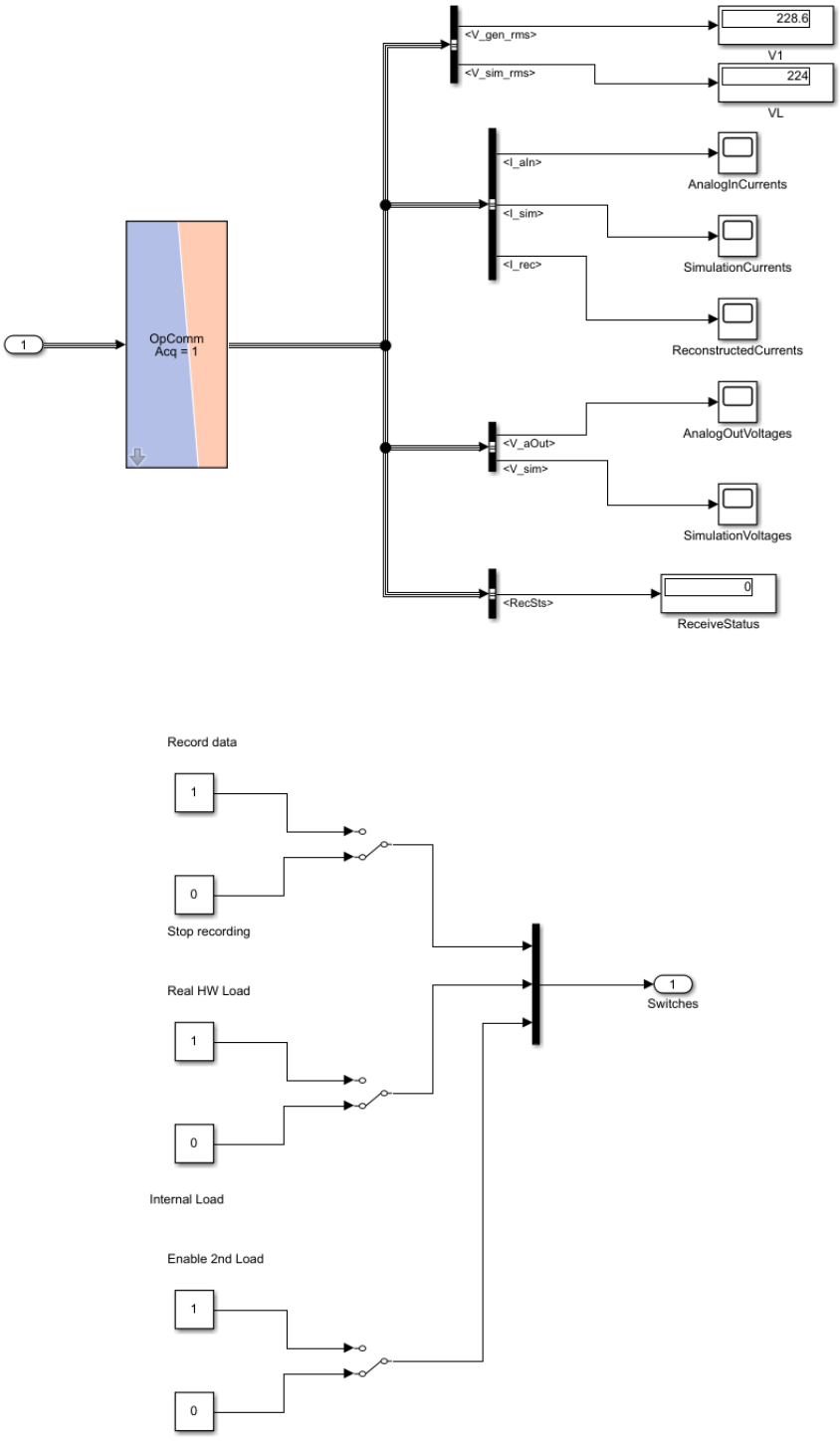

Figure 4.21: Console Subsystem

Chapter 5

Modeling of Power-Hardware-In-The-Loop and Wallbox representation

In the previous chapter the electrical grid side of the model has been explained
Aim of this chapter is to show how the charging station interaction has been modeled inside the Simulink model.
The input and output modeling of the Real-Time Simulator is illustrated in detail.

All the frequency-based components inside the model are set to 50 Hz, which is the nominal frequency of the italian grid.
The Simulink model solver is set to Fixed-Step type and discrete solver (no continuous states).

5.1 MV/LV Transformer

Every node in the model is supplied at 22 kV which is a Medium Voltage, while the charging station has a nominal voltage of 400 V 3-phase with neutral.
Inside the node where the wallbox is placed (Node 10A), a step-down transformer is needed to properly connect the wallbox. Hence, a three-phase MV/LV transformer has been introduced upstream of the wallbox itself.
To better represent the real conditions, values from an actual transformer nameplate are taken [37].

Table 5.1: MV/LV Transformer nameplate [37].

	Parameter	**Value**	**Unit**
S_n	Rated Power	160	kVA
f_n	Nominal frequency	50	Hz
V_{n1}	Primary winding nominal voltage	22	kV
V_{n2}	Secondary winding nominal voltage	400	V
R_{cc1}	Primary winding resistance	0.0110	Ω
P_0	No Load losses	0.46	kW
$P_{cu,FL}$	Full Load losses (75°C)	2.36	kW
$V_{cc\%}$	Shortcircuit Voltage (75°C)	4	%
$I_{0\%}$	No Load current	2.3	%

From the nameplate, further parameters are obtained (Table 5.2). These parameters must be inserted in the Simulink mask of the MV/LV transformer. The subscript **pu** stands for *"per unit"*.

Table 5.2: MV/LV Transformer mask parameters (per unit values).

Parameter	**Formula**	**Value [p.u.]**
$R_{1,pu}$	$\frac{P_{cu,FL}}{2 \cdot S_N}$	$7.3438 \cdot 10^{-3}$
$R_{2,pu}$	$\frac{P_{cu,FL}}{2 \cdot S_N}$	$7.3438 \cdot 10^{-3}$
$L_{1,pu}$	$\frac{S_n}{P_0}$	0.02
$L_{2,pu}$	$\frac{S_n}{P_0}$	0.02
$R_{m,pu}$	$\frac{100}{I_{0\%}}$	347.826
$L_{m,pu}$	$\frac{100}{I_{0\%}}$	43.4783
$L_{0,pu}$	$80\,\% \cdot (2 \cdot L_{1,pu})$	43.4783

To be more detailed, the MV/LV transformer introduced has a common delta-wye configuration and is a core-type transformer (three-limb core).

5.2 Wallbox virtual positioning

As introduced in the previous chapter, the V2G charging station is virtually positioned in *Node 10A* of the Brenta feeder (Figure 5.1).

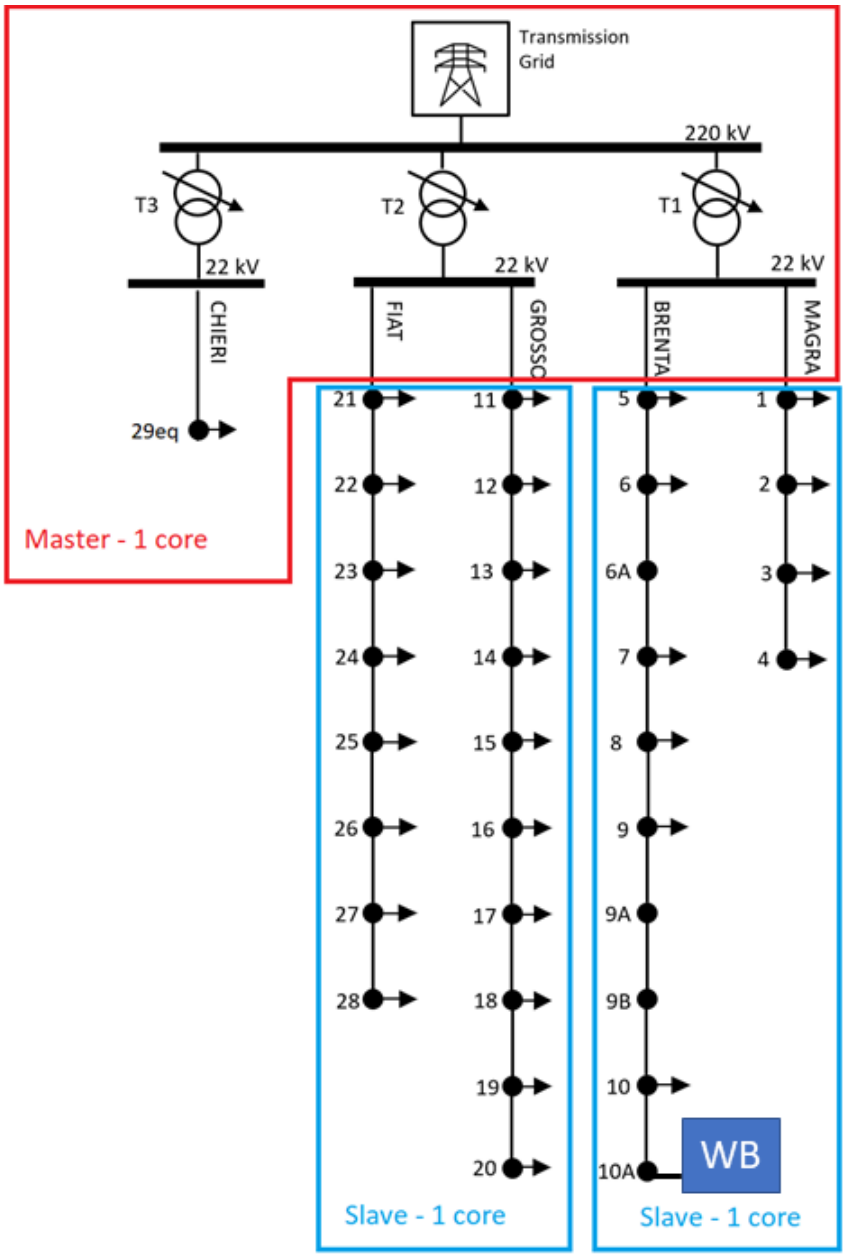

Figure 5.1: Qualitative scheme of the definitive network topology

5.3 Input signals from the Console Subsystem

Apart from the three inputs which stand for the voltage supply, another input which previously passed through an *OpComm* block (SS_Magra_Brenta), comes inside the WB subsystem (Figure 5.2).

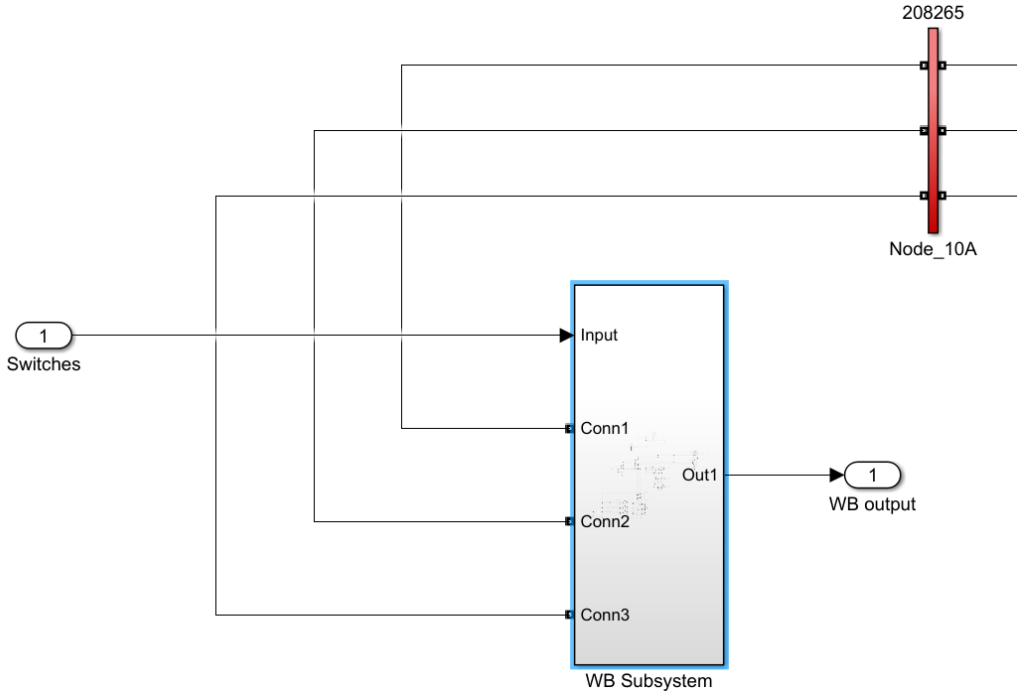

Figure 5.2: Zoom on Wallbox subsystem block

The input comes from the Console subsystem (Figure 4.21) and transports three different signals.
Inside the WB subsystem the input is split in the three binary signals.

The first signal could enable the recording of the data and their saving into a Matlab file (.mat).
The signal goes into an *OpTrigger* which triggers the acquisition when the input signal is greater than the 0.5 value (Figure 5.3).

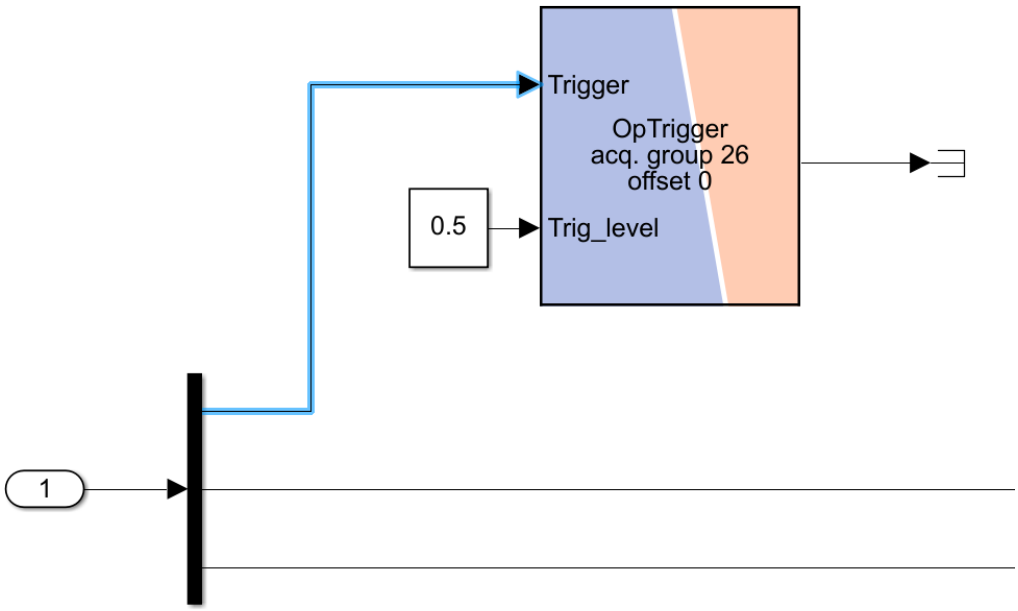

Figure 5.3: First input signal

Since the signal has a binary nature, it is the user to decide whether enabling the acquisition or not, in the console subsystem.
The data to be saved are specified as inputs of the *OpWrite* block, shown in Figure 5.4).
In our case, the saved data are the output of the WB subsystems, which are sent to the console subsystem to be monitored by the user in real-time. In particular they are the measured and reconstructed voltages and currents which will be explained in the following sections.
Data savings is necessary to analyze what has been happened during the simulation. The monitoring through the scopes cannot assure high fidelity. This is due to the fact that the signals from and to the RTS are sent through an ethernet network. That means that sometimes the data packages for the parameters visualization are not sent or not received.
Thus, the scopes inside the console give an idea of what is happening during the system, but it is essential to look to the recorded data.

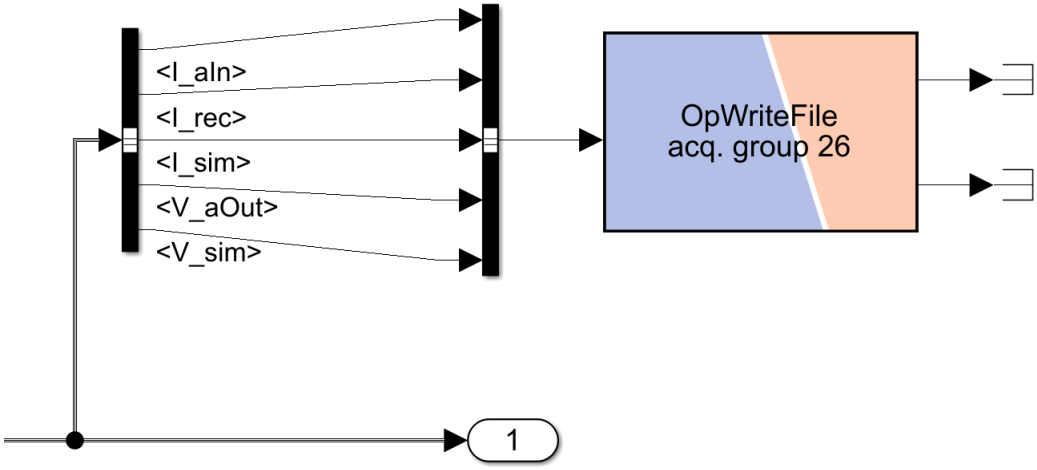

Figure 5.4: OpWrite block for data savings

The third signal simply commands a switch in order to eventually include an additional three-phase power load of 4 kW (Figure 5.5).

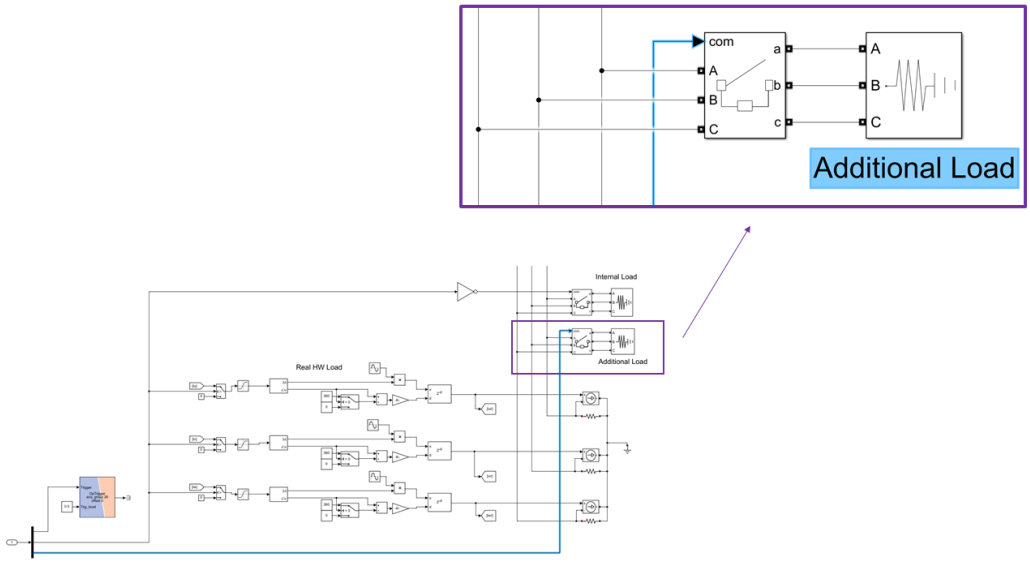

Figure 5.5: Third input signal

The second signal is responsible for the choice between a simulated internal load (0) and the real load (1).

5.3.1 Internal Load

In Figure 5.6 are shown the blocks involved when the user decides to use a simulated internal load.
The switch is set to zero, but passing through a *NOT port*, the zero signal becomes one and activate the switch, which in turn enables the internal load of 11 kW.

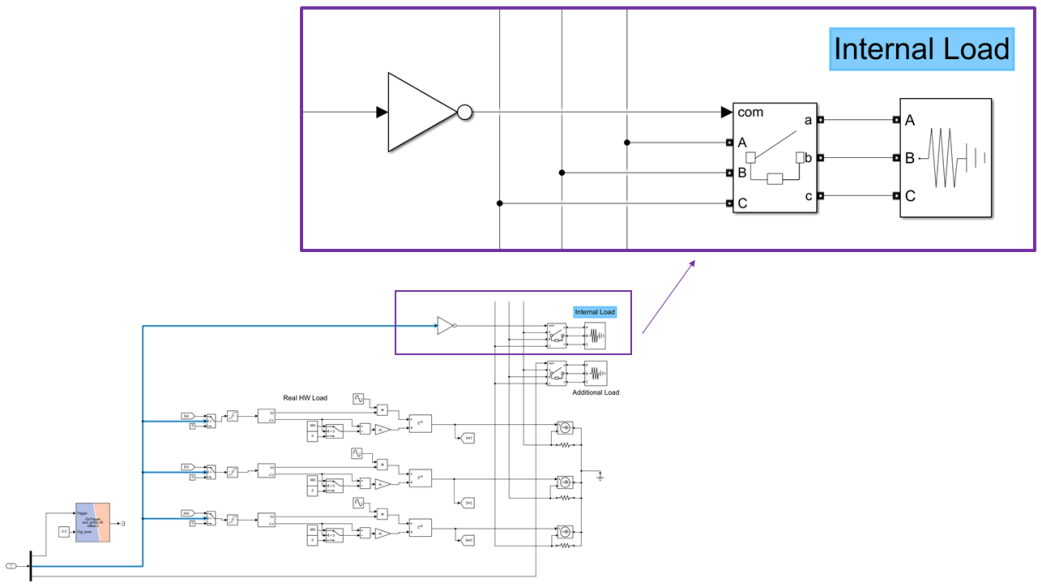

Figure 5.6: Second input signal, internal load.

The choice of the 11 kW is not random. It is the rated power of the V2G charging station.
In fact, as explained in section 3.3, before connecting the real hardware it is always advisable to emulate it in the software model.
This was done through the simulated internal load.

5.3.2 Real Load and Current Reconstruction

It's reminded that in the final configuration the real load is the V2G charging station, while in the tuning of the instruments the wallbox was replaced by an electronic load.

When the signal is 1, the output of the *NOT* port (Figure 5.6) is zero, thus excluding the internal load.

Conversely, the real hardware modeling side is activated if the signal has value 1.
The Simulink scheme in Figure 5.7 must be read from left to right (for a better understanding, only one phase is shown).
The switch on the left side is activated if the input signal (second input) is higher than zero.
The outcome of the switch is the value of the real current (I_u) measured with the current probe, sent to the RTS.
For major details on the I/O acquisition please read section 5.5.

The current value passes through a saturation value of

$$\pm 20 \cdot \sqrt{2}$$

The rms AC current limit of the charging station is indeed 20 A. To limit the peak values, $\sqrt{2}$ was added.

After the saturation starts a reconstruction procedure of the current waveform.
During the tuning of the instruments and the firsts trial of the PHIL methodology with the emulated electronic load (7.5) some instability problems occurred.
The emulated load is a switching load, thus the current increased its harmonic content. When the current was fed back to the simulation, creating a closed loop, its harmonic content negatively influenced the node voltages waveforms.
These voltages were the ones supplying the charging station. Hence, at every loop, the harmonics values amplified themselves, increasing indefinitely.
The solution to this instability problem has been to reconstruct the current waveforms.

In few words, the reconstruction consists in identifying the amplitude and the angle phase of the fundamental of the current waveform.
Then these two parameters, after some processing, are put together again to form the new current that will be send to the Console (I_{ur} *goto* block).

The procedure is explained.
The current amplitude is used again to be the magnitude of a new 50 Hz sinewave.
On the other side, the phase angle (in degrees) passes through a switch and a sum block in order to make sure the phase angle value is positive.

Right after a gain has the aim to change the phase value from degrees to "number of samples", trough the formula 5.1:

$$frac-\frac{1}{f_n}360 * T_S \tag{5.1}$$

Afterwards, both the perfect sinewave (with the correct amplitude and correct frequency) and the phase angle value (in samples number) are fed to a *delay* block. Purpose of this block is to shift the sinewave of the right angle, which is the phase angle of the original current waveform.

Through this procedure, the current waveform is cleaned from all the harmonics, thus cleaned from the distortion. The reconstructed current is now a perfect 50 Hz sinewave.
The procedure is repeated for all the three phase currents.

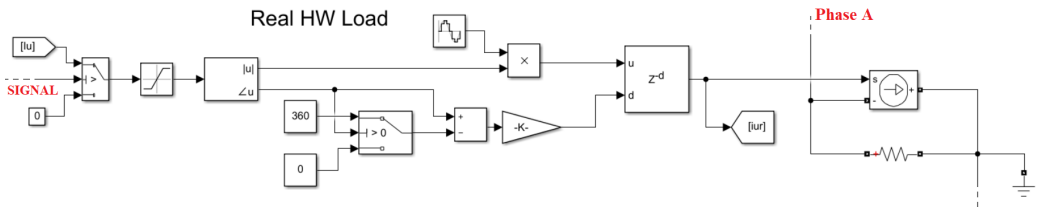

Figure 5.7: Second input signal, real load and current reconstruction in one phase.

In the right side of the Figure 5.7, after the I_{ur} flag is notable the interaction between the "Internal Load" and the "Real HW Load" procedures.
A current source, with the value of the real measured current, is placed in parallel to a 1 MΩ resistance.
The current source is hence a controlled source. This is congruent with the ITM algorithm interface explained in section 3.3 (Figure 3.4).

When the internal load is enabled (load switch set to 1), the 11 kW simulated load is in parallel with the 1 MΩ resistance. The resistance is electrically invisible as it absorbs a negligible current.
The current source branch is absent as the load switch is set to zero. Hence the current is not reconstructed.

Conversely, when the real load is enabled, the internal 11 kW load is not present.
This time is the current source to be in parallel with the resistance, which

again absorbs a very small current.

In Figure 5.8 is shown the electrical circuit representation of the two loads configurations.

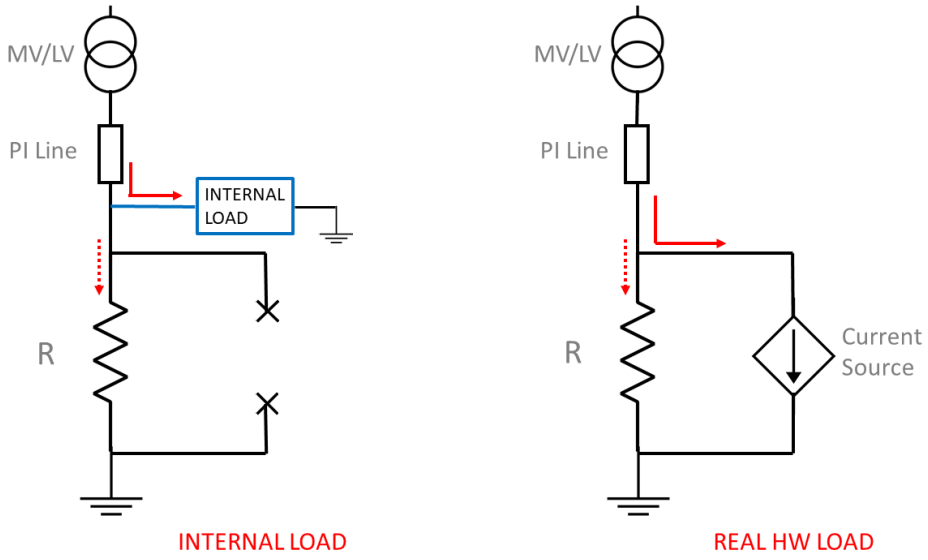

Figure 5.8: Load electrical representations. Internal (left), Real (right).

Parameter	Symbol	Value
Frequency	f_n	50 Hz
Positive-sequence resistance	r_1	0.529 Ohm/km
Zero-sequence resistance	r_0	0.529 Ohm/km
Positive-sequence inductance	l_1	24.8e-3 H/km
Zero-sequence inductance	l_0	6.1e-3 H/km
Positive-sequence capacitance	c_1	$5e^{-}9$ F/km
Zero-sequence capacitance	c_0	$5e^{-}9$ F/km
Line length	L	0.3 km

Table 5.3: Three-phase underground cable specifications

5.4 Network voltage supply and voltage reconstruction

The Simulink WB subsystem is supplied by the three voltages arriving at node 10A.
These voltages are in the order of 22 kV, hence is necessary a step-down transformer (described in section 5.1) to reduce the voltage level to 400 V, for the purpose to supply the wallbox at the nominal voltage.

Before arriving to the wallbox, the low level voltages pass through a *Three-Phase PI Section Line* block. The PI line block emulates a three-phase underground cable whose realistic specifications can be read in table 5.3.

Before and after the PI line block are visible two *Three-Phase V-I Measurement* blocks.
These blocks have two additional signal outputs for the visualization of voltages and currents.
If the current measured in *Measure1* is the same as the one measured by *Measure2*, the voltage is different because of the voltage drop on the PI line.
Eventually, both the voltage and current measurements of the two blocks are sent to the console subsystem to allow the monitoring of the system.

In Figure 5.9 are shown the blocks above described.

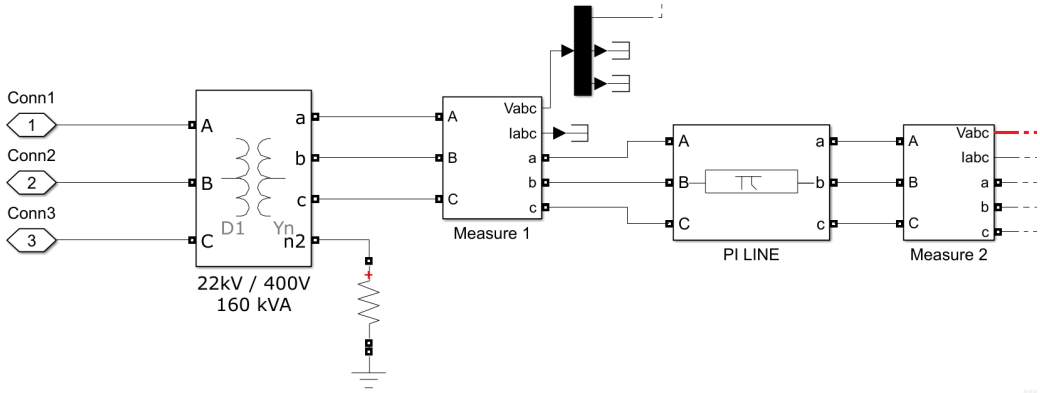

Figure 5.9: Network voltage supply

5.4.1 Voltage Reconstruction

As analyzed in subsection 5.3.2, some instability issues were provoked by the current distortion.
To enhance the result accurateness, it was decided to reconstruct also the voltages to be sent to the real-time simulator.

Therefore from the *Measure2* block the voltage signals were obtained and each signal was reconstructed.
The blocks used for the voltage reconstruction are the same used in the current reconstruction: to avoid excessive elongation, the procedure is not explained again.

Result of the voltage reconstruction procedure is the creation of a voltage waveform (one for each phase) which is going to be plotted in the console subsystem. But, more important, the *"v_u" goto* block sends the voltage to the RTS analog output (section 5.5), in order to be consequently sent to the amplifier.
Again, the procedure is repeated for each phase.

5.5 Input & Output connection with the real world

The blocks which enable the interfacing between the virtual environment (Simulink model) and the real world (Real-Time Simulator I/O) are illustrated in Figure 5.10.

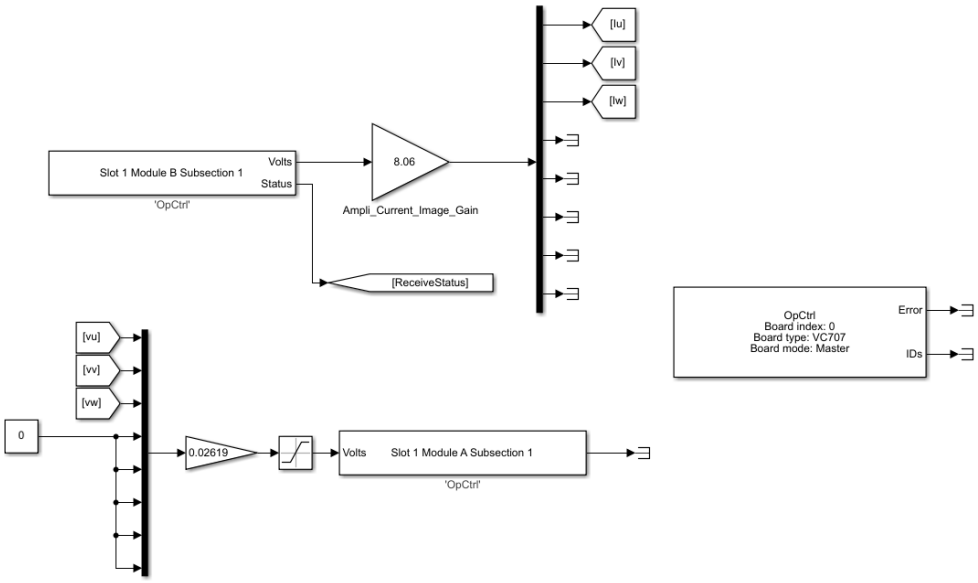

Figure 5.10: Opal-RT blocks for the communication with the RTS

In particular Opal-RT library makes available three important blocks: *OpCtrl*, *AnalogIn*, *AnalogOut*.

5.5.1 OpCtrl block

The *OpCtrl* block controls the programming of one OPAL-RT cards, its initialization and the selection of the hardware synchronization mode of the card.
It also binds the I/O blocks (*AnalogIn* and *AnalogOut*) to that specific card. For each card used in the model, only one *OpCtrl* block must be used.
At the parameters the controller name must be the same for the two I/O blocks (Figure 5.11).
Essential is to write the correct Primary Bitstream Filename (.bin). This file, together with the .conf file, is responsible for the FPGA configuration.

In fact, both files must be uploaded in the project folder of RT-LAB.

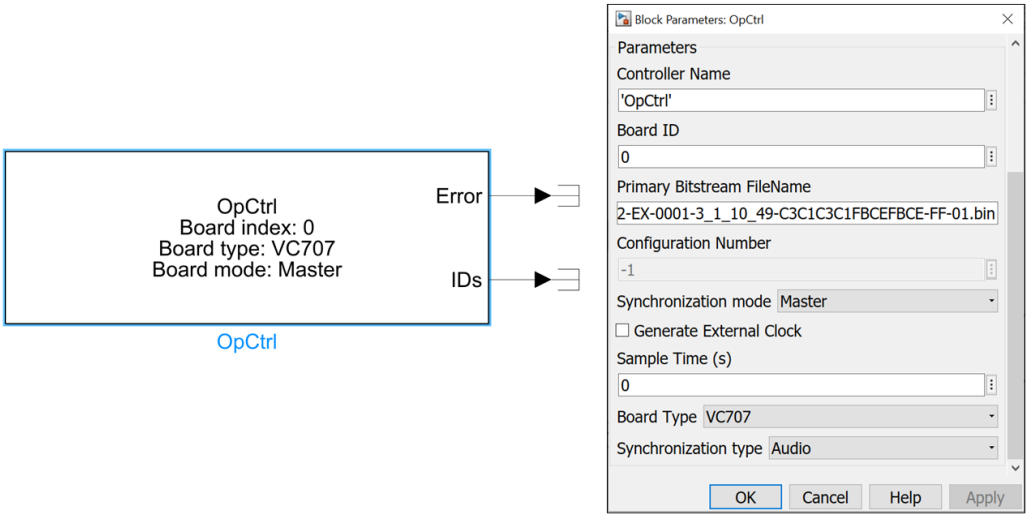

Figure 5.11: OpCtrl block (left) and its parameters (right).

5.5.2 AnalogIn block

For the input acquisition (Figure 5.12) is essential the use of *AnalogIn* block. The block returns as output the voltage values from Analog Input channels of a physical I/O card.
A second output is the status, that is a binary signal representing the status (1 if the input acquisition is occurring, 0 otherwise).
Inside the model, the output voltage values from the analog input channels are scaled up with a gain of 8.06.
The value is the image gain of the power amplifier: when the DUT currents are measured from the PA, the measurement is sent from the PA to the RTS via a BNC cable. The measurement is not a current value anymore, but a voltage signal, scaled down with gain of 8.06 (8.06 A of real current measured corresponds to 1 V of signal).
It is necessary to put the gain when the currents are measured through the power amplifier.
If the measurement is done through the AC current probes and then the DAQ, the gain must be deleted.

After the gain a demux splits the eight signals. Of the eigth channels avail-

able, only the first three are used.
The values of the measured current are then obtained and available to be sent to the current reconstruction area (subsection 5.3.2).

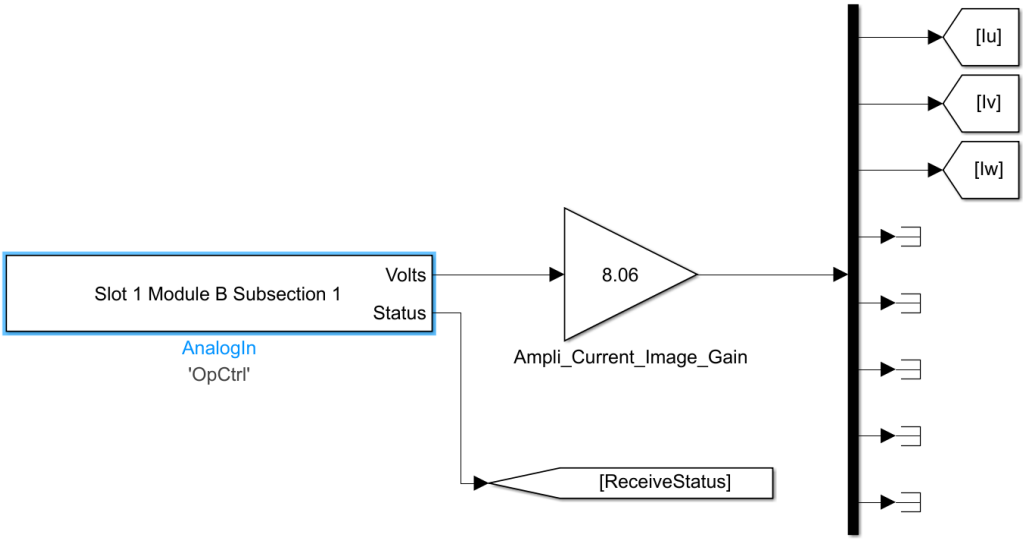

Figure 5.12: Analog Input Acquisition blocks.

In the parameters section of the *AnalogIn* block, among the others, must be specified the controller name ('OpCtrl'), the port number and the number of analog inputs (Figure 5.13).

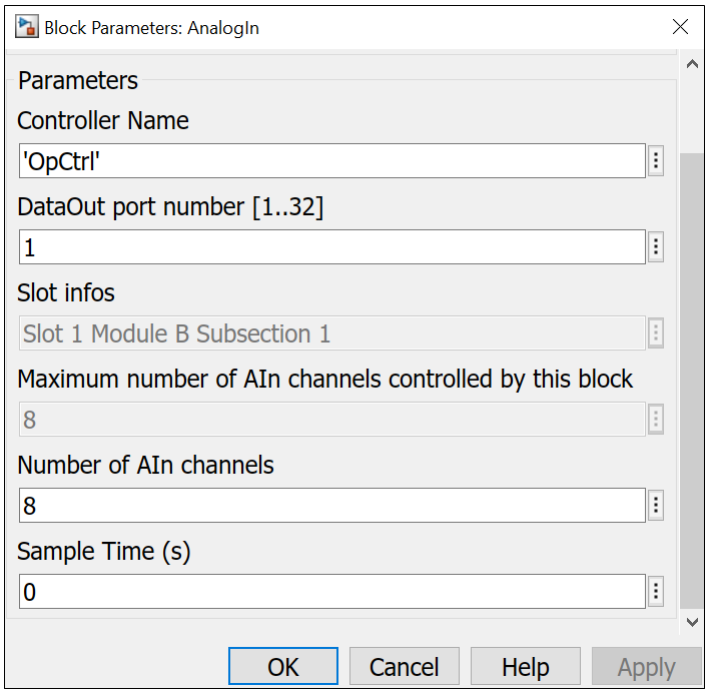

Figure 5.13: Parameters of AnalogIn block

5.5.3 AnalogOut block

The *AnalogOut* block carries out the opposite function of the *AnalogIn* block, that is transmitting to a physical I/O card the voltage values to be applied to Analog Output channels.

The simulated reconstructed voltages must supply the DUT, they are the RTS output to be sent to the PA (Figure 5.14).
After the mux block which merges the eight signals, a gain is inserted. This gain has the same function of the one described in the previous subsection: it is not possible to send the real signal (approximately 230 V) to the PA input ports. Thus the signals must be made smaller.
The gain of 0.02619 is not a random value. When a voltage signal is acquired at the input side of the PA, it is amplified and made available at the power output passing through a gain of 1/0.02619.
As the DUT is always supplied by the power amplifier during the PHIL experiments, this block is always present (differently from the gain after *AnalogIn* block.

A saturation block with values of ±12 V was put as safety measure. The

power amplifier accepts input signals of ±15 V as maximum voltage. Precautionary, a smaller value is put into the saturation block.

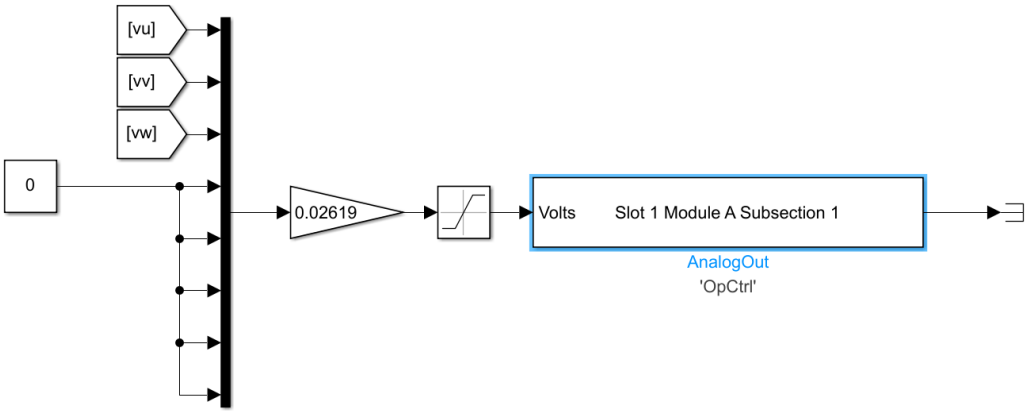

Figure 5.14: Analog Output Acquisition blocks.

5.6 Console Subsystem Monitoring

The output port of the WB subsystem contains many signals which are sent to the Console Subsystem.
The view of the signals monitored via the console subsystem is offered in Figure 5.15.

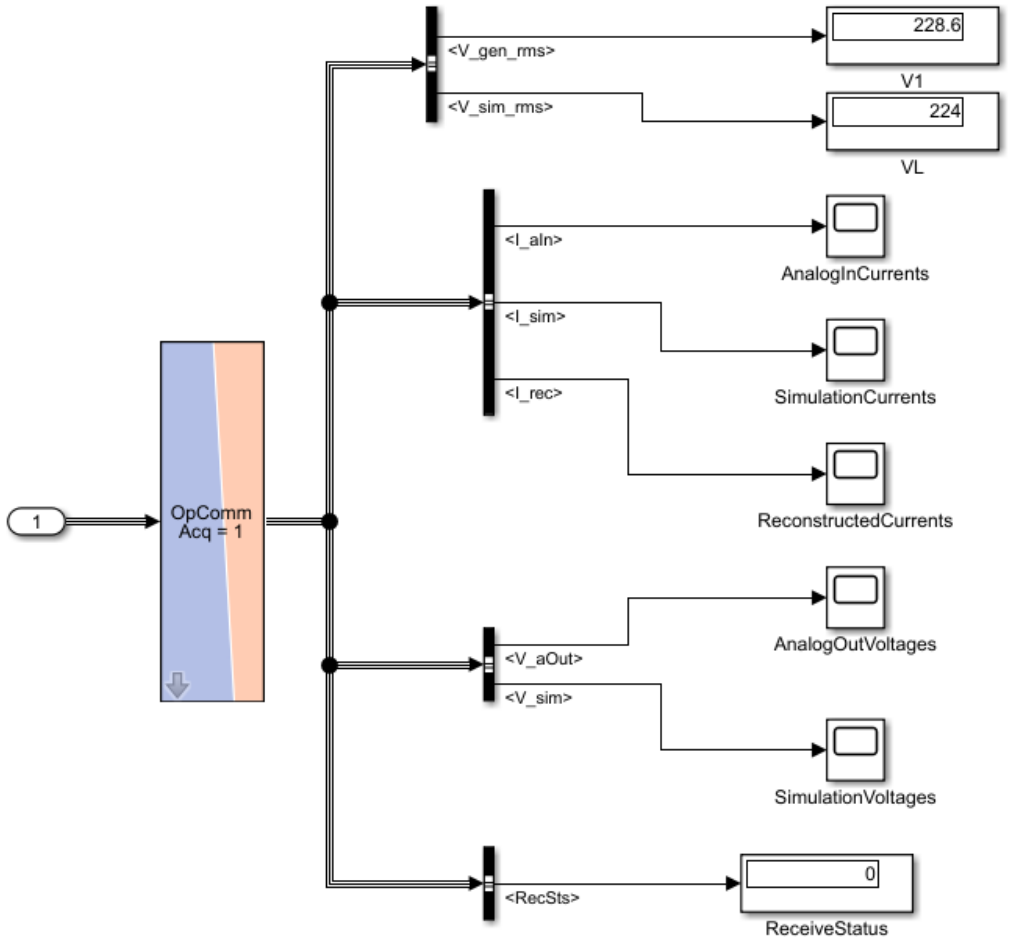

Figure 5.15: Console Subsystem - signals monitoring.

The first signal "V_gen_rms" is the simulated voltage value measured by *Measure1* block, just upstream of the MV/LV transformer (see section 5.4.
The second signal "V_sim_rms" is the simulated voltage measured by *Measure2* block, which is located just downstream of the MV/LV transformer.

The third signal is in turn split in three signals:
- The first one ("I_aIn") are the real measured currents (ex. I_u) and put into the simulation via *AnalogIn* block;
- The second one ("I_sim") are the simulation currents obtained by *Measure2* block;
- The third one ("I_rec") are the reconstructed currents (ex. I_{ur}), which are different from zero only when the real load is used. In such case, they would coincide with the simulation currents.

The fourth signal are the reconstructed voltages ("V_aOut") sent to the DUT, while the fifth signal are the simulation voltages ("V_sim"), measured by *Measure2* block.
It is reminded that the reconstructed voltages are just the simulation voltages without distortion.

Finally, the sixth signal is the ReceiveStatus binary value. When it is 1, it means that the input acquisition is correctly occurring.

5.7 RT-LAB Settings

After the Simulink model is properly built, the simulation is ready to be run. It is advisable to always proceed cautiously in order to avoid safety problems. Therefore, as first step the simulation must be run offline, that means without using RT-Lab.
If no problem occurs, then the simulation can be run online.

Once RT-Lab software is open, it is necessary to import the built Simulink model.
First, a project must be created. Then the model can be imported inside the project folder.
The model overview appears as in Figure 5.16

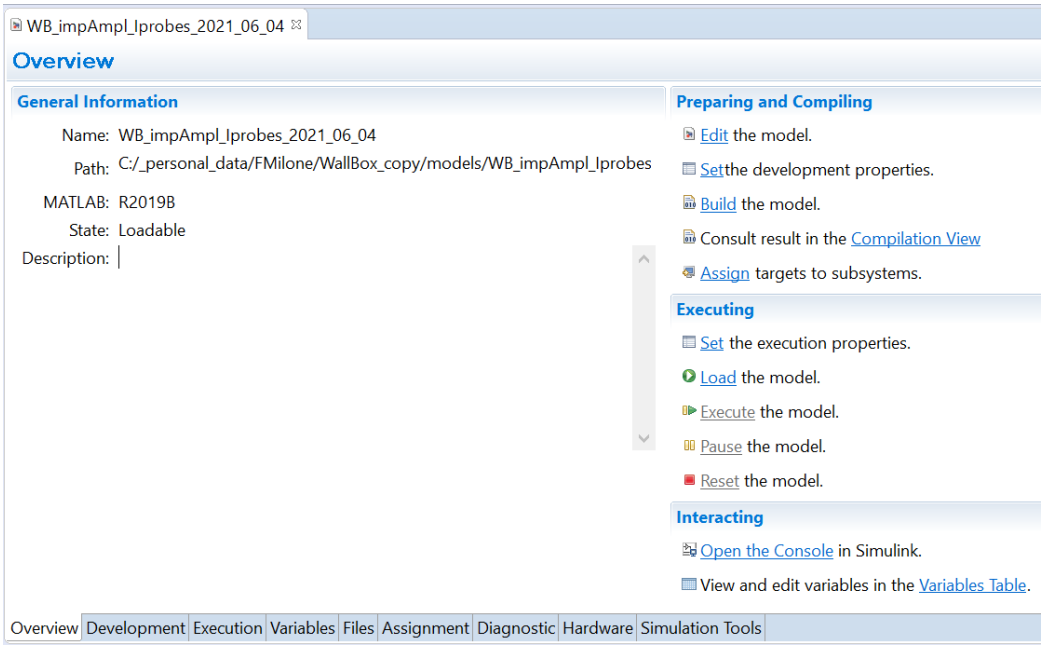

Figure 5.16: Model overview in RT-Lab environment

In the bottom of the Figure are visible the other setting windows.
Respect to the default RT-Lab settings, some changes are necessary to enable correctly the real-time simulation.
In the Execution window, the *real-time simulation mode* must be set to *Hardware Synchronized*.
Also, in the Files window must be added the FPGA configuration files (.bin and .conf).
In Figure 5.17 are shown the windows above mentioned.

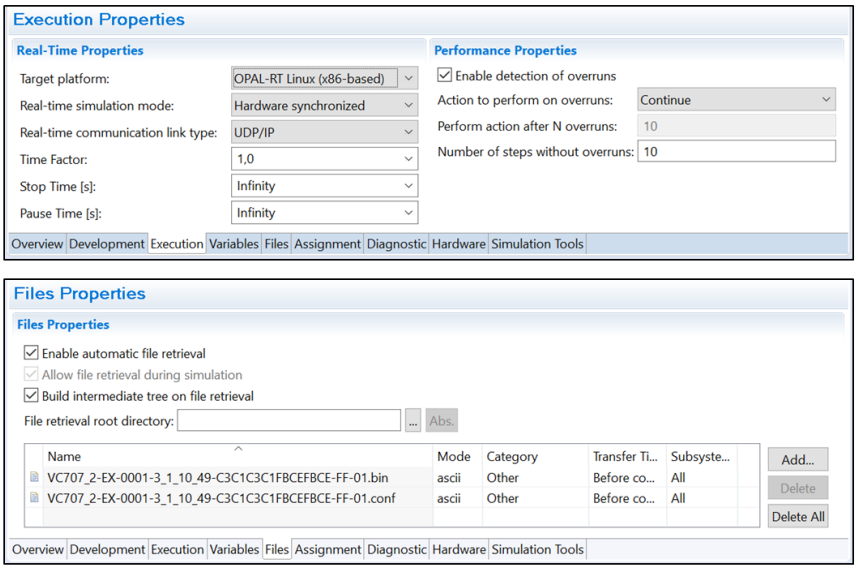

Figure 5.17: Execution (top) and Files (bottom) windows

The following step consists in loading the model through the *Load the Model* function in the model overview.
This function basically loads the Simulink model on the OPAL RTS. If the configuration is not properly set, some problem occurs. Otherwise the model is correctly loaded.
Afterwards, in the Assignment window, it is possible to observe the subsystem assignment to the cores (5.18). Also, the "Run in XHP mode" must be set for every subsystem. XHP stands for "eXtra High Performance" and allows very fast computation of the real-time model on the target system [22].

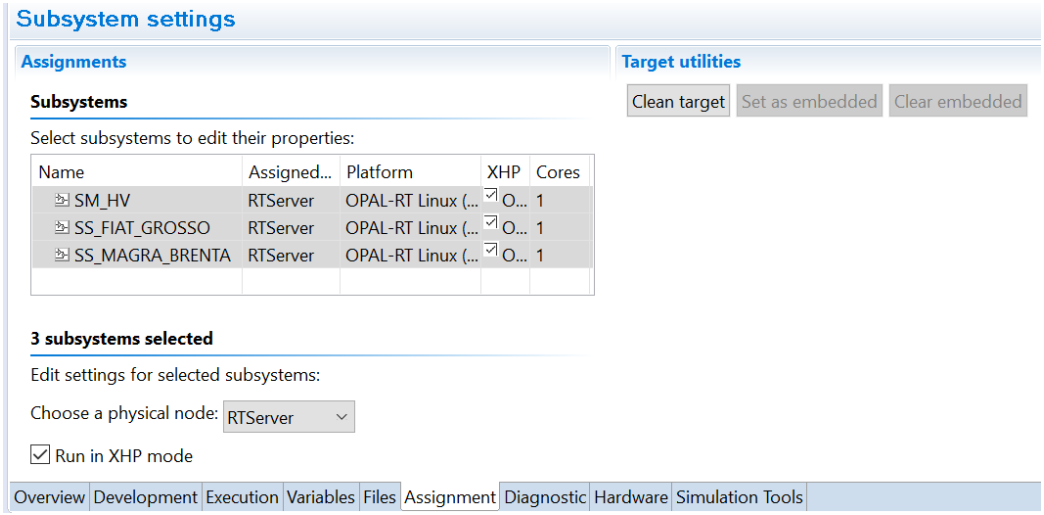

Figure 5.18: Assignment window

If no problem occurred in the loading, the simulation is ready to be run via "Run the Model".
Automatically the Simulink model will open showing the Console subsystem. This is the only accessible part to the user while the simulation is running.

To stop the real-time simulation, "Reset the Model" is the right function to select in the RT-Lab environment.

[30]

Chapter 6

Experimental Layout

6.1 Electrical Protection Box Design

For the first part of the joint project, the charging station is placed in the EC-Lab. The first of long series of validation tests have been executed in the EC-Lab.
To permit a safe supplying of the charging station, before starting the tests, an electrical protection box was designed and installed in the EC-Lab. The wallbox then is not directly connected to the AC grid, but through the protection box, where the adequate protections are placed.
The installation work of the electrical protection box was commissioned to an Edison supplier.

During the grid compliance tests (9.2, 9.3, 9.4), the wallbox is powered directly from the AC electrical network. But for complicated scenarios, in which for example an abnormal situation must be simulated, the wallbox is supposed to be supplied via power amplifier. In this way, through a Simulink model, the operators are able to choose in detail the characteristics of the AC voltage waveforms which power the wallbox. As a matter of fact, the interconnection grid tests are executed using the power amplifier.
Hence, in order to make possible a quick switch of the supply (between AC grid and power amplifier), the purchase of an additional socket was also commissioned to the Edison supplier.
To be more specific, a power cable is derived from the protection box. An electrical plug is put at the extremity of the power cable. To directly connect the protection box to the AC grid, the plug must be inserted into a wall socket already present in the EC-Lab.
To supply the wallbox, so the protection box, through the power amplifier,

the plug must be inserted to a socket which in turn is directly connected to the amplifier via another power cable.

In table 6.1 is listed the equipment needed for the electrical protection box installation.

Figure 6.1 shows a qualitative scheme of the connections with the components numbered as in Table 6.1.

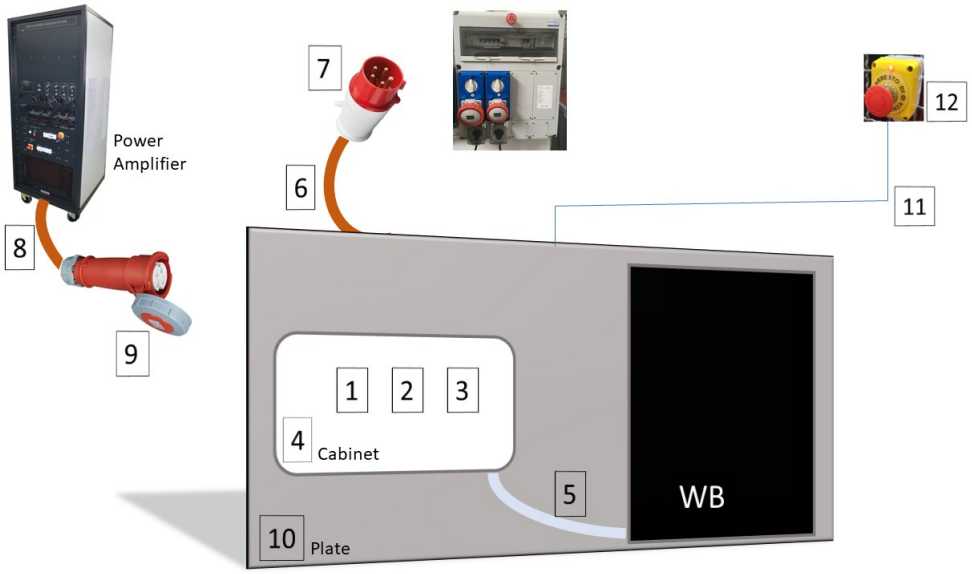

Figure 6.1: Qualitative scheme of electrical protection box connections

The plate was installed on the grid (Figure 6.2) in order to create a more stable surface on which to mount the wallbox.

Table 6.1: Equipment list

Number	**Device**	**Specifications**
1	Energy meter	
2	Residual current device (RCD)	B type 4P 230/400 V , In = 40 A AC: 30 mA, DC: 6 mA
3	Magneto-thermal breaker	C curve 4P 230/400 V , In = 32 A
4	Electrical protection box case	
5	WB supply power cable	3PH + N + PE ext. diameter = 13-18 mm S = 6 mm^2
6	Protection box supply cable	3PH + N + PE L = 5 m S = 6 mm^2
7	CEE Plug	3PH + N + PE In = 32 A 230/400 V
8	PA output power cable	3PH + N + PE L = 2 m S = 6 mm^2
9	CEE Socket	3PH + N + PE In = 32 A 230/400 V
10	Checkered steel plate	1350 mm x 650 mm
11	EPO signal cable	2P
12	EPO button	

Figure 6.2: Grid measures

As can be seen in Figure 6.3, in addition to the wallbox, the cable holder and the protection box are mounted on the plate too.

Figure 6.3: Protection box, wallbox and cable holder.

A zoom of the protection box is proposed in Figure 6.4 where the components are easily distinguishable.
From left to right: energy meter, magneto-thermal breaker, residual-current device.
The two protection devices are inserted to fulfill the CEI 64-8 technical standard [2].
In the Section 722 of the standard ("*EV power supply*") it is explicitly required to equip the charging station connection point of a protection device against overcurrents (magneto-thermal circuit breaker).
Also, it is mandatory to install a protection device against indirect contacts, capable of automatically interrupting the supply.
Two are the possible solutions:
- B type RCD
- A type RCD + Residual DC detecting device (6 mA)
In our case, the first choice has been made.

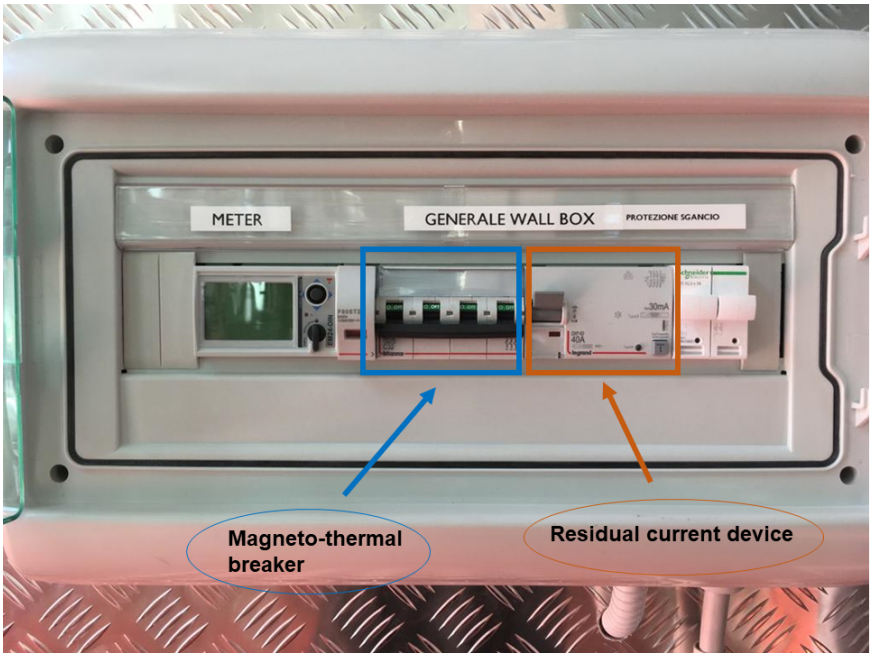

Figure 6.4: Zoom of the electrical protection box

Lastly, following the vision of the Italian fire brigade circular 2/2018 [1], an emergency power off (EPO) button was placed in the Lab (Figure 6.5). It has been installed at a distance of 3 meters from the charging station to be easily accessible in the event of a fire on the EV or on the charging station

itself.
The EPO button is electrically installed upstream of the protection box, and it is phisically connected to it through a bipolar signal cable.

Figure 6.5: Emergency push-off button

6.2 Measurement Setup

The charging station to be tested acts as an AC/DC converter.
For the G2V use, it absorbs AC power from the electrical grid (or from the PA), converts in DC acting as rectifier and supplies the EV battery.
For the V2G operation, the battery provides DC power that is converted in AC power by the wallbox, acting as inverter.

To comply with regulations, some parameters need to fulfill certain requirements.
To check whether these requisites are respected, it is essential to accurately measure voltages and currents in both sides of the wallbox.

To measure the three AC currents and the DC current, four current probes are then employed.
For the DC side one probe (Hioki 3274) is sufficient. Though, it is fundamental to clamp the instrument on only one of the two polarities of which a DC cable is composed.
For the AC side three instruments (Pico TA189) are enough as, expecting a symmetrical system, the current flowing through the neutral wire is negligible. In any case, it can be obtained simply summing the three phase currents.

Every measurement is transmitted through a coaxial cable to the DAQ where the waveforms are visualized and recorded.

6.2.1 DC Currents

The wallbox is connected to the EV through the DC CHAdeMO connector. The CHAdeMO cable contains two power supply wires (pin layout visible in Figure 6.6). Clamping the current probe on the DC cable is not useful: the value read by the instrument is zero as the effect of the two wires balance out.
Only clamping the probe on one of these two supply wires can be helpful, providing the real DC current value.
Since cutting the cable insulation does not comply with the safety instruction, it is more practical to clamp the probe below the bonnet. Here, the positive and negative polarity cables are distinguishable (Figure 6.7).

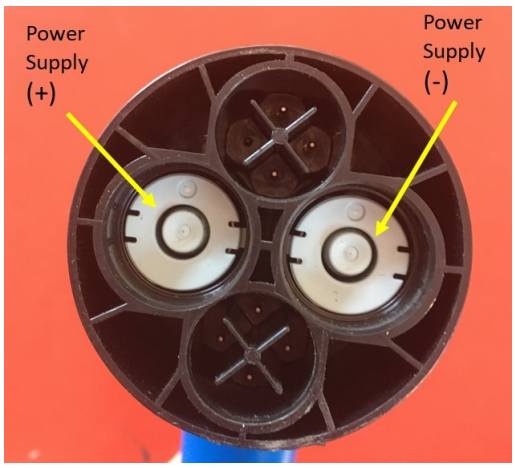

Figure 6.6: CHAdeMO polarities

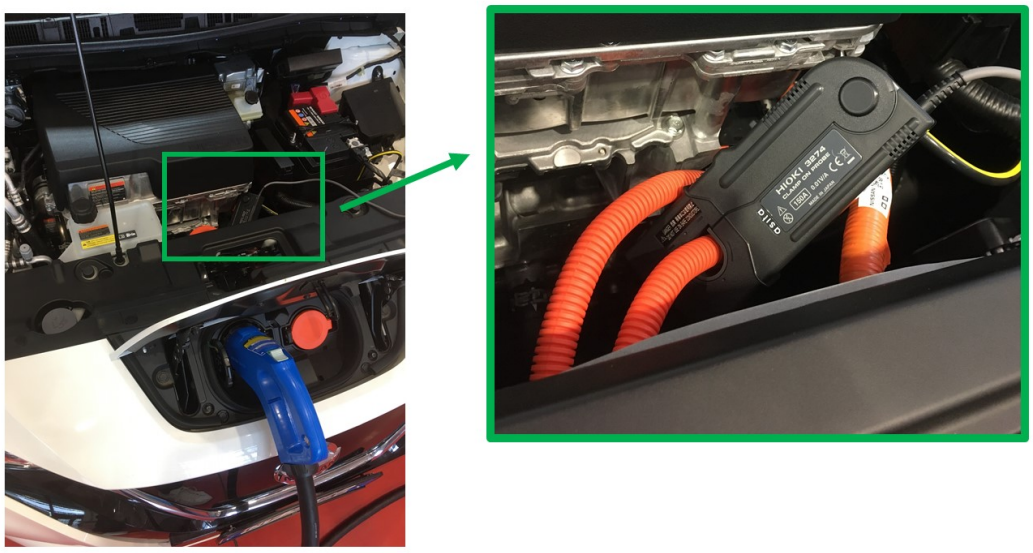

Figure 6.7: DC clamp outside the battery

As explained in the Hioki 3274 (section 6.7) introduction, the probe has a BNC derivation which makes possible the DC current waveform transfer to the data acquisition system.

6.2.2 AC Currents

The current measurements on the AC side of the wallbox are not carried out directly upstream of the charging station.
The protection box supply power cable (component number 6 of Figure 6.1) has been stripped for a short distance. In this way the three phase wires are exposed and the probes can be placed (Figure 6.8).
Therefore the measurement takes place right upstream of the protection box.

Figure 6.8: AC measurement

In this position, the AC currents are measured whether the protection box is powered by the mains, or if it is powered by the PA.
Each probe is furnished of a BNC terminal which is connected to the data acquisition systems in order to visualize, monitor, record and process the waveforms.

6.2.3 DC and AC Voltages

The voltage acquisitions are made with the assistance of two junction boxes provided of insulated bushings for banana plugs (Figure 6.9).

Figure 6.9: DC (left) and AC (right) voltage measurement boxes

In Figure 6.10 is illustrated a qualitative scheme of voltage measurements.

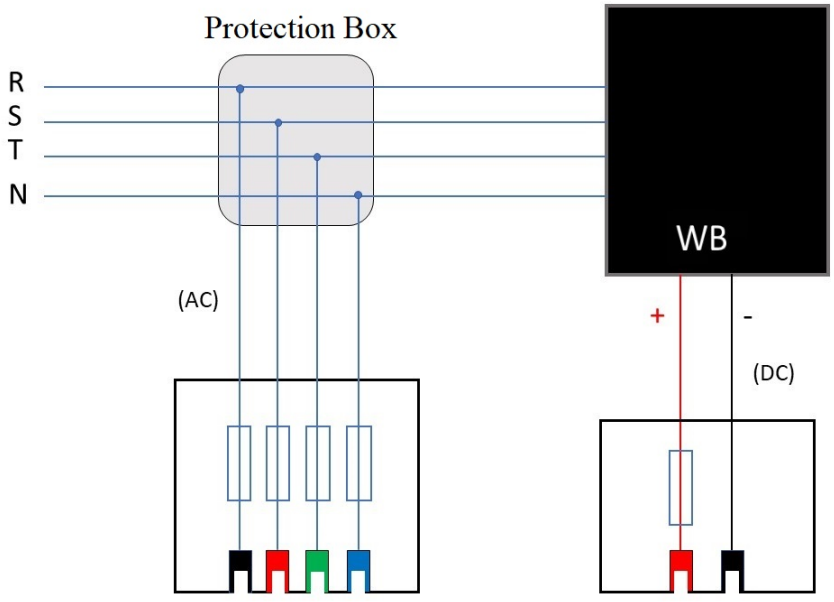

Figure 6.10: Qualitative scheme of voltage measurements

For the DC voltage measurements, the wallbox cover has been removed and both the DC power supply polarities have been derived into one of the two junction box.

Inside the DC junction box a 500 V 2 A fuse is present. Indeed, two fuses would have been redundant since the DC current value is the same on the positive and on the negative wire.
The DC junction box consists then of two insulated bushings for banana plugs. Through a banana cable, the signals are finally transmitted to the DAQ.

To obtain the AC voltages a similar procedure has been performed.
This time four 1.5 mm^2 wires (three phases and neutral) have been derived downstream of the RCD to terminate into the AC junction box. Inside the box, the wires pass through four 400 V 4 A fuses, before making their voltages available at the bushings.
In the figure 6.11 is shown the connection of the AC junction box to the DAQ.

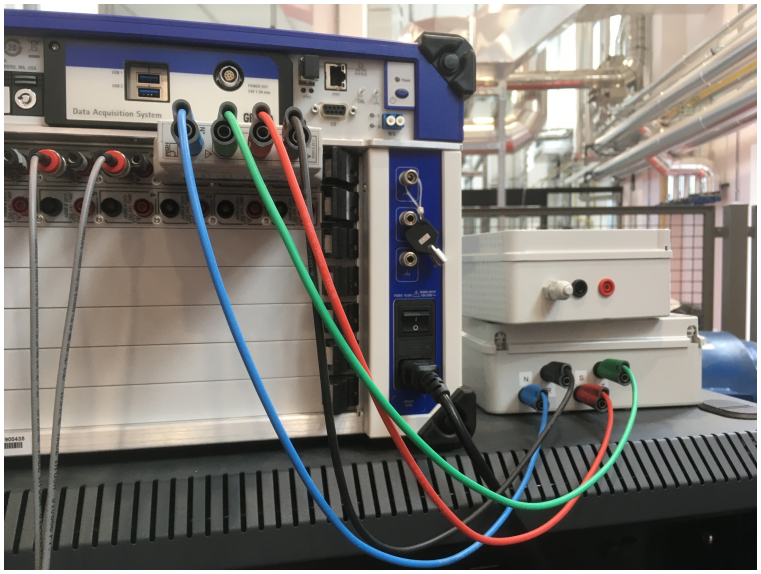

Figure 6.11: AC and DC voltage measurement. Box-DAQ connection.

6.3 Real-Time Simulator : OPAL-RT OP5700

The Real-Teal Simulator used for this project is the OP5700 from OPAL-RT technologies which uses RT-LAB as simulation software.
To edit and monitor the simulation, the OP5700 can be connected to a hosting computer through TPC/IP Ethernet.

Figure 6.12: OP5700 Real-Time Digital Simulator [22]

All the specifications provided in this section are obtained from [22].

CPU	Intel Xeon E5, 4 core 3GHz to 32 cores 2.3GHz
FPGA	Xilinx Virtex 7 FPGA on VC707 board
I/O lines	256 lines, routed to 8 analog or digital 16 or 32 channel, conditioning modules
High-speed communication ports	16 SFP sockets, up to 5GBps
I/O connectors	4 panels of 4 DB37F connectors
Monitoring connectors	4 panels of RJ45 connectors
PC interfaces	Standard PC connectors (monitor, keyboard, mouse, and network)
PCIe slots	6 onboard PCIe slots.
Hard disk	512 GB SSD
Power supply	Input: 100-240 VAC, 50-60 Hz, 8A-4A
Dimensions	22.27 x 47.7 x 49.3cm HxWxD
Weight	17kg

Table 6.2: OP5700 Technical Specifications

The main housing is divided into two sections.
The upper part contains the FPGA and the analog and digital I/O modules, while the lower section contains the multi-core processor target computer.

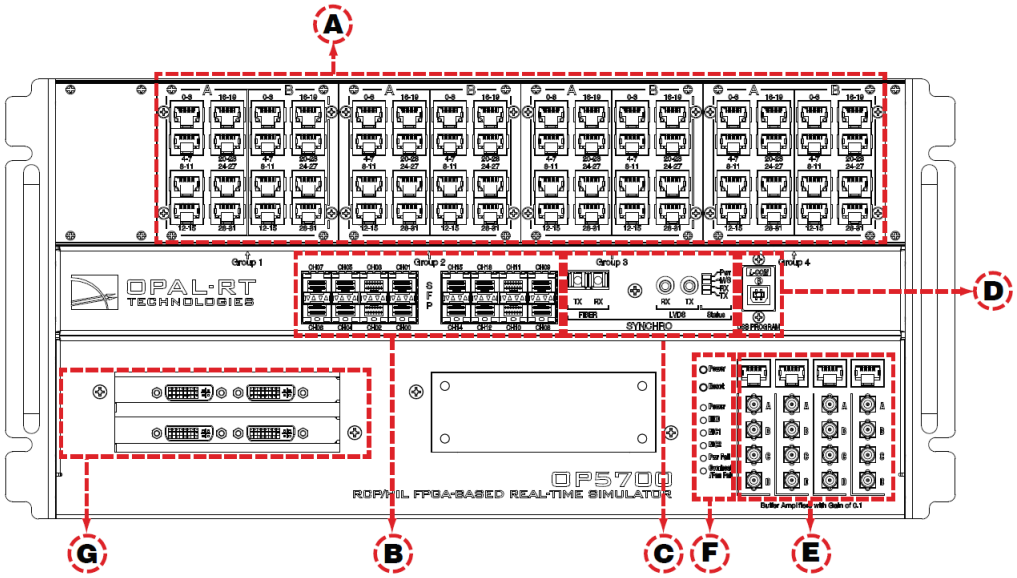

Figure 6.13: OP5700 front panel [22]

In Figure 6.13 only panels *A* and *E* are of our interest.
***A* – RJ45 Panel**: provides connections to monitor signals from mezzanine I/O boards. Analog mezzanines (channels 0-15) use only the first column of connectors, while digital ones require also the second column (channels 16-31).
***E* – mini-BNC Monitoring Panel**: an RJ45 cable coming from RJ45 panel, contains 4 channels. With this panel is possible to split these 4 channels (Figure 6.14 [22]). Mini-BNC connectors are present because usually allow quick connections to monitoring device.

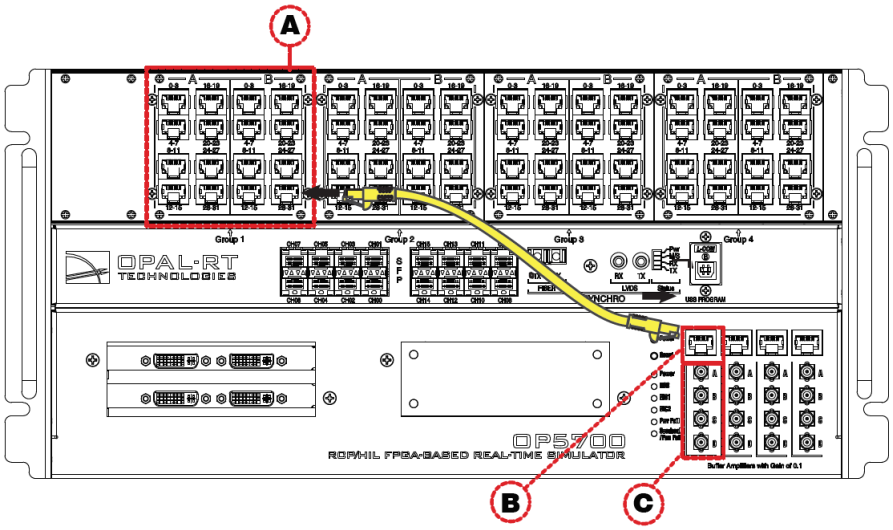

Figure 6.14: Channels splitting [22]

In Figure 6.15 are shown the rear connectors of the OP5700.
Inside the A-labeled box are visibile the DB37F I/O connectors.

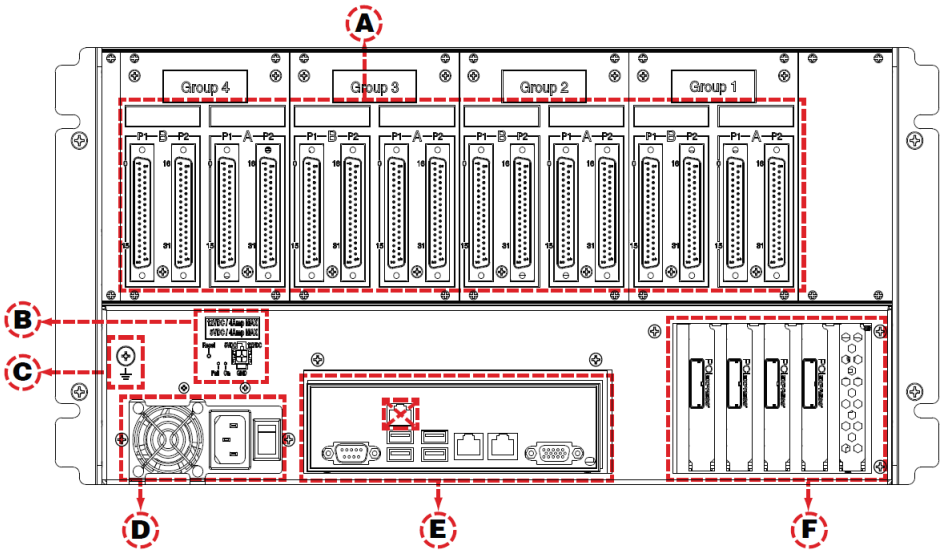

Figure 6.15: OP5700 back panel [22]

Four groups of mezzanines are visible, labeled from 1 to 4.
Each group (zoom in Figure 6.16) contains two subgroups (A and B) linked to four females DB37 connectors (I/O).

The first two connectors from the left represent channels from subgroup B, which are linked to the conditioned channels from the rear mezzanine. Instead, the last two connectors (subgroup A) are linked to conditioned channels from the front mezzanine.

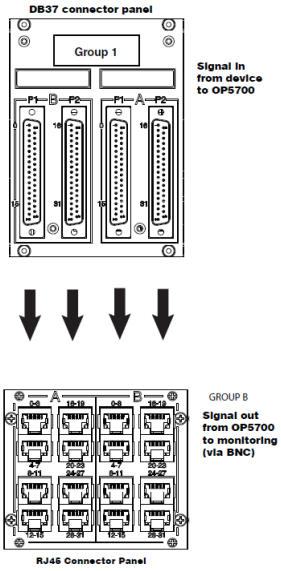

Figure 6.16: DB37 Connectors [22]

As can be seen, two connectors (P1 and P2) are available for each mezzanine: for analogue modules, as our case, one connector (P1) is sufficient because the module uses only 16 channels (P2 does not carry any signals). For digital modules, both connectors are needed [22].

6.4 Power Amplifier - Spherea Puissance Plus PA-3x7000-AC-DC-400V-54A-4G

The power amplifier used in this thesis has been manufactured by Spherea Puissance Plus.
It is a four quadrants 21 kVA (7 kVA per phase) amplifier that can be operated both in AC (three-phase) and DC.

Figure 6.17: Power Amplifier 3x7kVA [**PA**]

Manufacturer declares both rise time and fall time are less than 7 µs considering 10% - 90% depth. While for 20% - 80% interval, rise time and fall time are less than 7 µs [24].

Four coupling modes are available:

- LVAC - Low Voltage Alternate Current
- HVAC - High Voltage Alternate Current
- LVDC - Low Voltage Direct Current

- LVDC - High Voltage Direct Current

For this thesis, only LVAC mode has been used.

For each mode, four operating ranges are available. The ones for LVAC are (Figure 6.18):

- 135 V - 54 A
- 200 V - 36 A
- 270 V - 28 A
- 400 V - 18 A

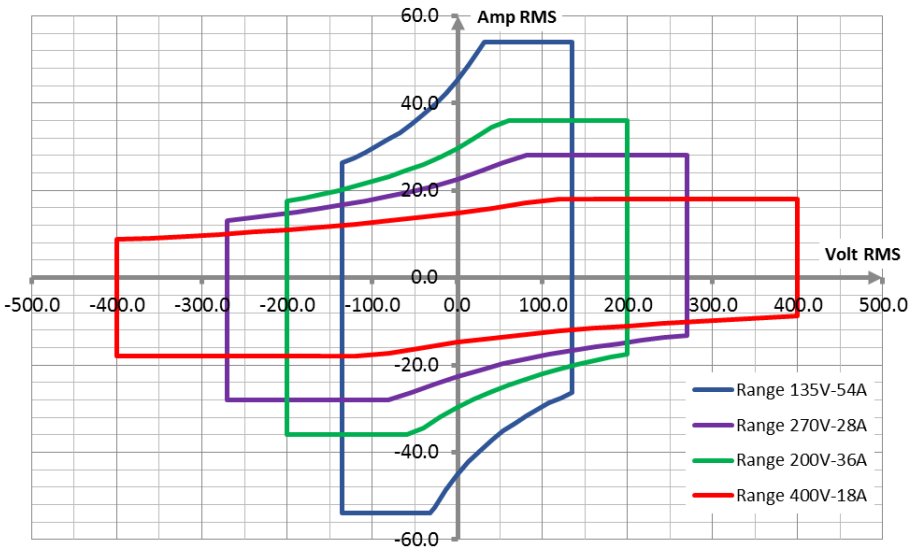

Figure 6.18: LVAC operating ranges [24]

A touch-screen display is integrated in the front panel for the local control. The PA can also be controlled remotely from a supervisor system via Ethernet or RS232.
Regarding the local control, a first screen is for the amplifier configuration (Figure 6.19).

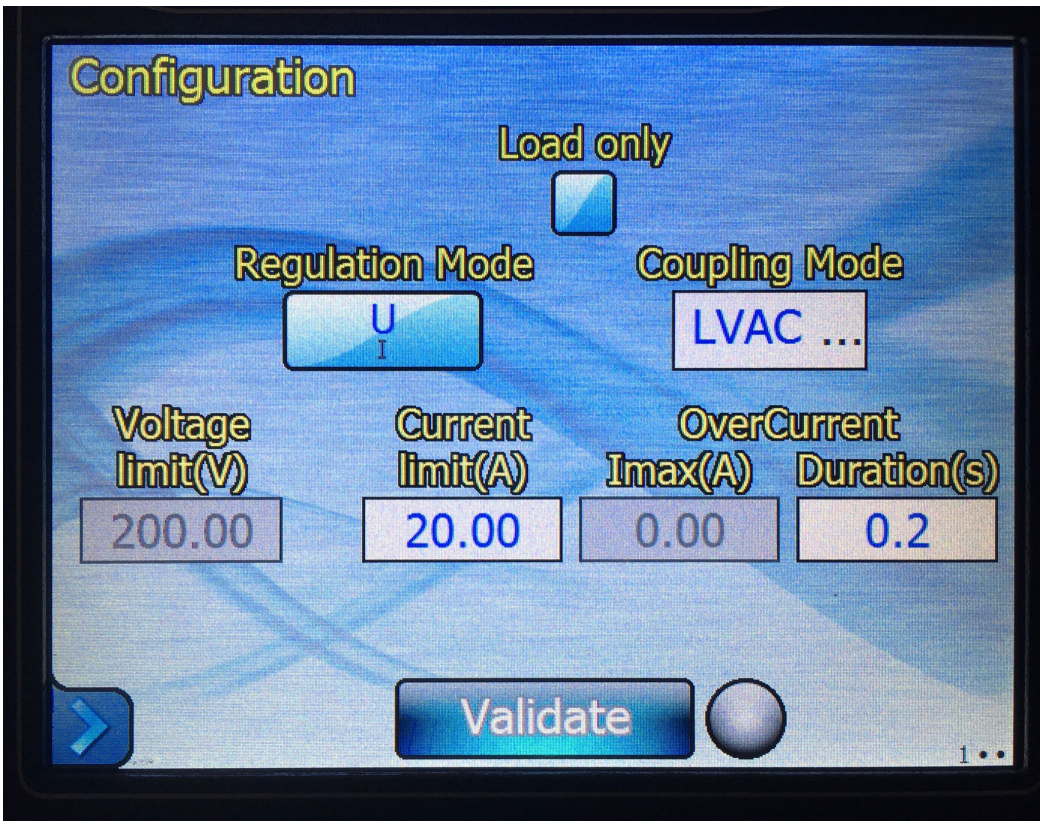

Figure 6.19: PA configuration settings

Here the coupling mode (LVAC, HVAC, LVDC, HVDC) can be chosen, such as the voltage and current regulation and limitation. For an overcurrent, it can also be specified the maximum amplitude and the duration allowed. All the values mentioned above are specified as effective values (rms).
For this thesis, LVAC is selected as coupling mode and 270 V as range (rms value). The regulation is the voltage type.
Finally maximum current is set to 20 A as it is the maximum AC current accepted by the charging station.

Another screen is for measurement (Figure 7.10) returning currents and voltages instantaneous values. On the right side, LEDs show the possible status of thermal fault, overcurrent, etc..

Figure 6.20: Measurement screen of the amplifier display

More screens are present, but they are outside the scope of the document.

In Table 6.3 are listed some PA characteristics from [24].
The analog input, for each phase, receives a "pilot" signal whose amplitude is $0 - \pm 10\,\text{Vpeak}$ (7.07 Vrms)
Images of voltage and current with amplitude $0 - \pm 10\,\text{Vpeak}$ are available from two analog outputs on the front panel (insulated from power output).

Some modifications are necessary when the amplifier supplies voltage to the wallbox and a long discharging process is desired.
In V2G operation, as the energy provided by the EV cannot be sent into the electrical grid, it is dissipated thermally in the power amplifier.
But in the standard PA configuration it is not possible to dissipate 10 kW in continuous operation.
Therefore it is necessary to change the amplifier settings and add an $8\,\Omega$ series resistor for each phase. This is done in order to avoid the device thermal breakdown and to provide V2G continuous operation.
In Figure 6.21 are shown the operation ranges with (green) and without the resistive load (red).

Table 6.3: Power Amplifier technical characteristics [24]

MAINS POWER SUPPLY	
Number of phases	Three-Phases + Neutral + Earth
Voltage	$400Vrms \pm 10\%$
Frequency	47-63 Hz
Max. Input current	55 Arms / Phase
Input current protection	Magneto-thermal breaker
OUTPUTS: POWER	
Rated power per phase	7000 VA
Rated power total	21 000 VA
Output type	Direct (without transformer)
TIME FEATURES	
Full scale output bandwidth	DC - 15 kHz
LOW VOLTAGE INPUTS: INPUT SIGNAL AMPLITUDE	
Voltage for full output scale	±10 Vpeak/7.07 Vrms
Max. Voltage	±15 Vrms
LOW VOLTAGE OUTPUTS: IMAGES	
Voltage Image accuracy	1 Vrms for 60.3 Vrms
Current Image accuracy	1 Vrms for 8.06 Arms
Connectors	BNC sockets
Accuracy of measurement displayed on touch screen	
Voltage measurement	0.3% of range + 0.3% of measure
Current measurement	0.3% of range + 0.3% of measure

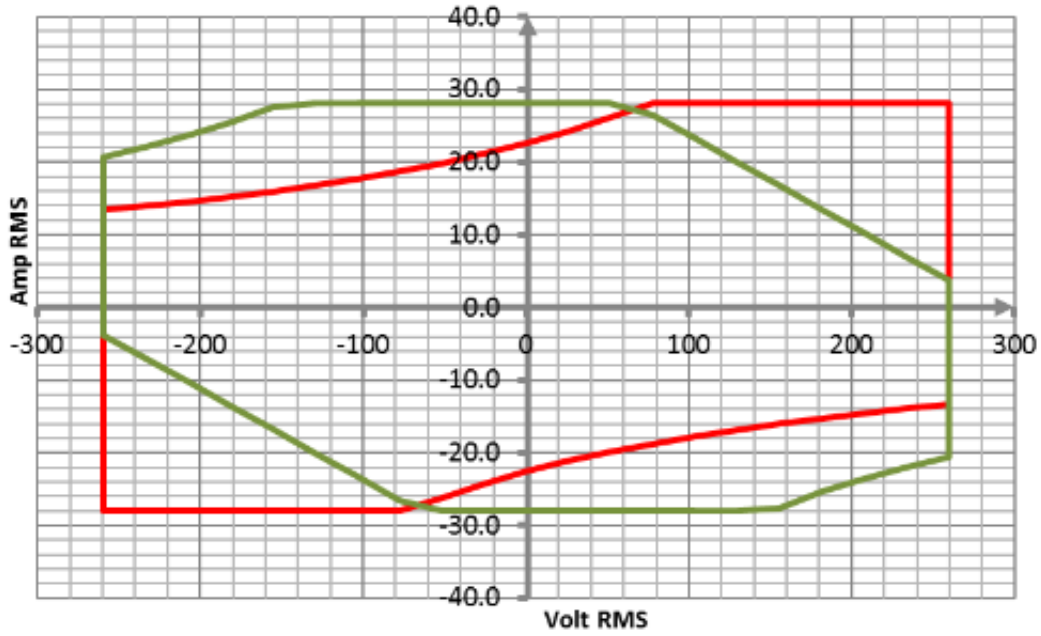

Figure 6.21: PA range with and without 8 Ω resistor load (LVAC, 270 V)

Assuming that the supply voltage is positive, the G2V mode corresponds to the first quadrant and the V2G mode to the second one.
It is visible how the second quadrant range increases its area after the resistor insertion.
As can be noticed, in G2V operation the resistors should not be inserted as they would reduce the amplifier operation range.

The following is the procedure to change the settings using the touchscreen display:
- menu "PCU-3x7000-AC-DC-400V-54A-4G"
- window "Program"
- impose settings as in Fig. 6.22.

The procedure shall be done whenever a long discharging session must take place to perform the tests in chapter 9.

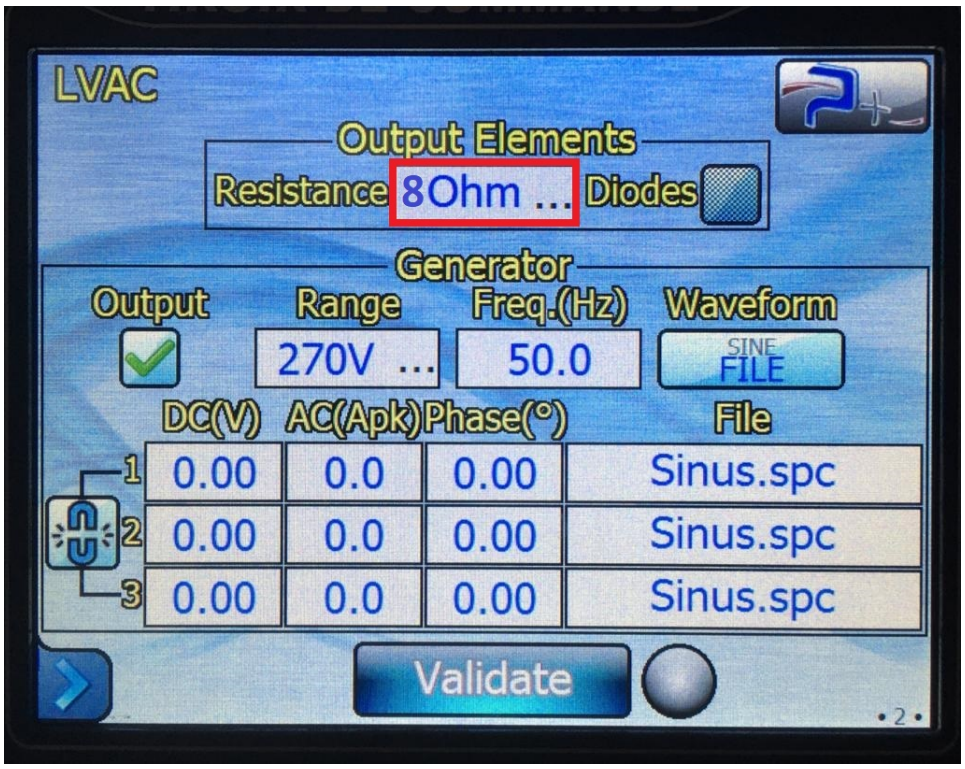

Figure 6.22: PA settings. 8 Ω resistor load insertion

6.5 Load Emulator CINERGIA EL+15 vACDC Full

The electronic emulated load is a programmable load which replaced the V2G charging station during the preliminary setup phase.
This was done for the purpose of avoiding unexpected damages on the wallbox.
The load emulator has a range of ± 15 kVA thus it is able to cover the whole operation range of the wallbox.

CINERGIA's EL+15 vAC/DC is a regenerative Current Source (Electronic Load Emulator) for energy testing in AC and DC applications. Its Bidirectional and Regenerative Hardware is based on a back-to-back power conversion topology.

Figure 6.23: Electronic Load Emulator

The device is capable of acting as load, absorbing energy from the grid, or as generator, injecting energy to the grid (Figure 6.24 [32]).

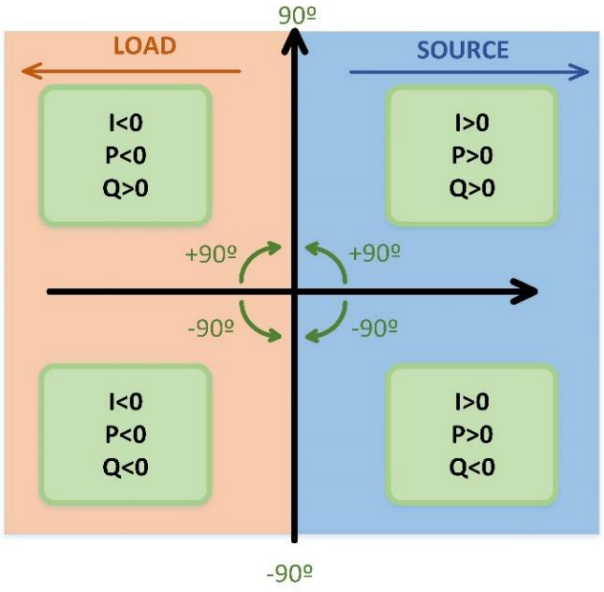

Figure 6.24: Load emulator operating range [32]

The active and reactive consumption is programmable.
It is possible an indipendent configuration of: rms current, phase angle, harmonics, interharmonics, generation of fast transients ("Current Dips").
It provides an intuitive user interface through a 4.3" touch-screen panel. A remote control port (LAN Ethernet with Open Modbus-TCP protocol) permits the user to control the load emulator via a proprietary software [20].

As anticipated, the EL+15 is capable of working both in AC and DC. In figure 6.25 are shown the switches to select the different connection modes.
From left to right:
- AC/DC switch;
- Output disconnector;
- Parallel connection switch;
- Bipolar/unipolar switch.

Figure 6.25: Load Emulator switches

The figure 6.25 already shows the three-phase connection mode, which was used in our experiments: AC Mode, Output EUT side enabled, Indipendent, Bipolar.

The Electronic Load distinguishes the input side and the output side. The input side represents the connection to the electrical grid (three-phase + neutral + ground). Instead, the output side (also called EUT side) represents the connection to the power amplifier.
Although for the experimental layout employed the power amplifier is not the device supposed to be tested, from the emulator point of view the PA is the EUT (Fig. 6.26).

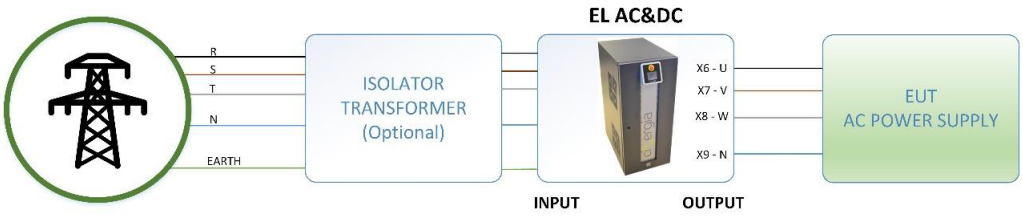

Figure 6.26: Three-phase mode [32]

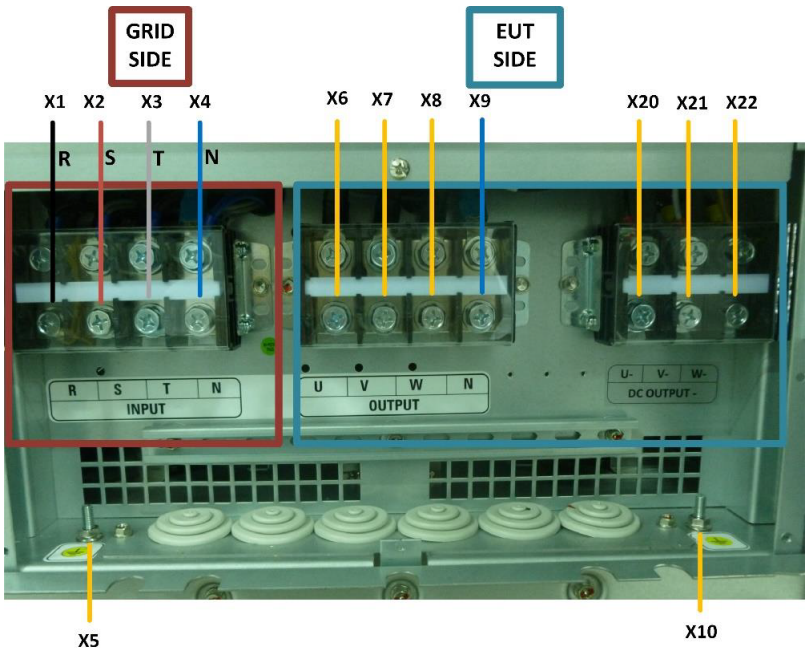

Figure 6.27: Wiring connection terminals of the Electronic Load [32]

In Fig. 6.27 the terminals for the wiring connection are illustrated.
X1, X2, X3 represent the phases terminals for the grid side connection, X4 and X5 are for the neutral and the ground respectively.
For the EUT side, the nomenclature is shifted: X6, X7, X8 for the three phases, X9 for the neutral and X10 for the ground.
X20, X21, X22 are not related to the AC mode.

Figure 6.28 shows the wiring connections used for the laboratory setup (section 7.4).
From the EUT side terminals depart two connections. The one leading to right goes to the rear part of the power amplifier (PA power output - Fig. 6.29). Instead, the cables leading to left (black, brown, grey, yellow-green) go to the DAQ, where the voltage and current waveforms feeding the load emulator are monitored and saved.

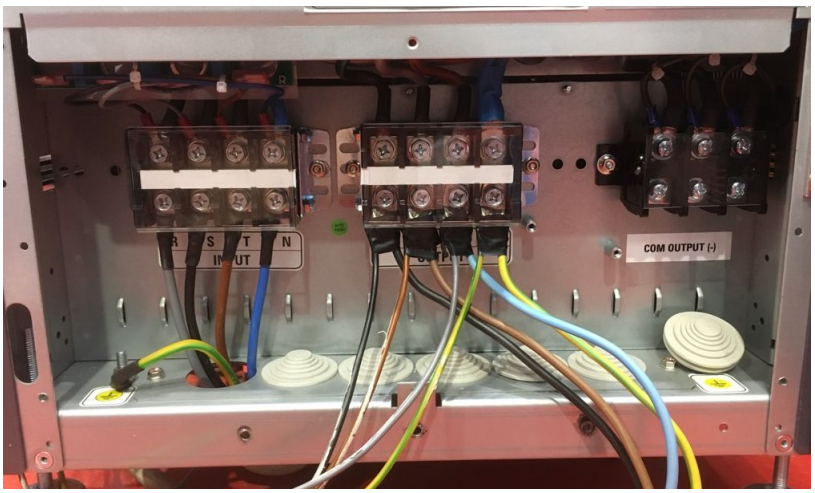

Figure 6.28: Wiring connection terminals of the Electronic Load for the setup

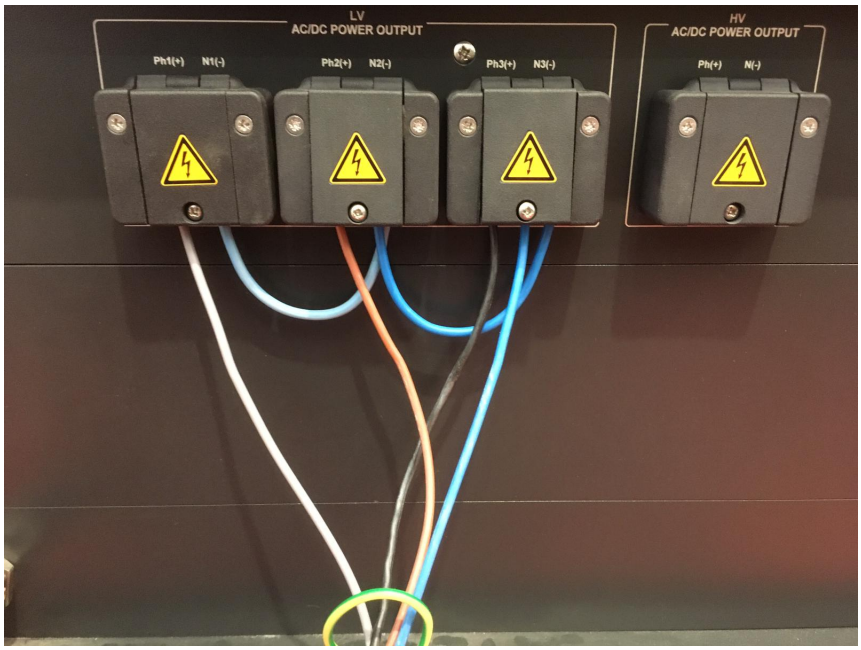

Figure 6.29: Power output connection of the power amplifier

Some of the specifications provided by the manufacturer ([20]) are listed in table 6.4.

Table 6.4: Electronic Load technical characteristics

GENERAL	
AC Rated Power	15 kW
AC rated current (3 channels)	22 Arms
INPUT SIDE (GRID SIDE)	
Number of phases	Three-Phases + Neutral + Earth
Voltage	400 Vrms +15%/−20%
Frequency	48-62 Hz
Current Harmonic Distortion	THDi $< 3\%$ at rated power
Current Power Factor	PF > 0.98 at rated power
Efficiency	$\geq 90\%$
OUTPUT SIDE in EL-AC	
Connection	1-phase, 3-phase star, 3-phase delta
Maximum Voltage	±400 Vpeak
Harmonics Range	up to 50th

6.6 Data Acquisition System : HBM Gen7TA

Figure 6.30: Data Acquisition System

The GEN7tA is a transient recorder and data acquisition system. In the project is used to visualize, monitor, record and post-process the electrical quantities.
An on-board display is not available, but through a RJ45 port, it is possible to remotely visualize all the measured quantities on a computer where the proprietary software *Perception* is installed.
The 1 Gbit Ethernet interface is capable of streaming recorded data to the PC at 100 MByte/s.

6.7 Clamp on Probe : HIOKI 3274

The Hioki 3274 clamp on probe is the measurement instrument that has been used for the DC current waveform visualization. It requires its own power supply.
The clamp has two connectors: one goes to the power supply, while the other (BNC cable) trasmits the signal to the DAQ.

Figure 6.31: Hioki 3274 clamp

Table 6.5: Hioki 3274 clamp on probe basic specifications [44]

Frequency bandwidth	DC to 10 MHz
Rated current	500 |Arms
Rise time	35 ns max.
Noise level	25 mA (rms) max.
Continuous allowable input	150 Arms
Max. allowable peak input	300 Apeak (non continuous) 500 Apeak (max. pulse width: 30 µs)
Output voltage rate	0.01 V/A
Output connector	BNC Connector
Power supply	±12 V ± 1 V, ±5.5 VA .

6.8 Clamp on Probe : PICO Technology TA189

Another current probe based on closed-loop hall effect technology is the Pico TA189.
A number of three of this instrument hav been employed to measure the AC currents. The maximum measurable current is 30 A (DC or AC peak). The wallbox, indeed, has a maximum bearable AC current of 20 Arms (28.28 Apeak). Unlike the Hioki clamp on probe, the PICO TA189 is supplied by an internal 9 V battery, thus is easily transportable [45].

Figure 6.32: Pico TA189 clamp

Table 6.6: Pico TA189 clamp on probe basic specifications [45]

Frequency bandwidth	DC to 100 kHz
Nominal Current	30 ApeakAC, 30 ADC
Measuring Range	30 A
Overload capacity	500 A (60 sec)
Output sensitivity	0.1 V/A
Accuracy	±1 % of reading ±2 mA
Resolution	±1 mA
Gain variation	±0.01 % of reading/°C
Power supply	9 V alkaline battery
Conductor size	25 mm diameter

6.9 V2G Charging Station

The traditional charging stations are intended for unidirectional use (G2V), while the wallbox to be tested is capable of V2G application.
It supplies DC power to the EV and it is equipped with the CHAdeMO connector (Figure 6.33).
Its specifications are given in table 6.7

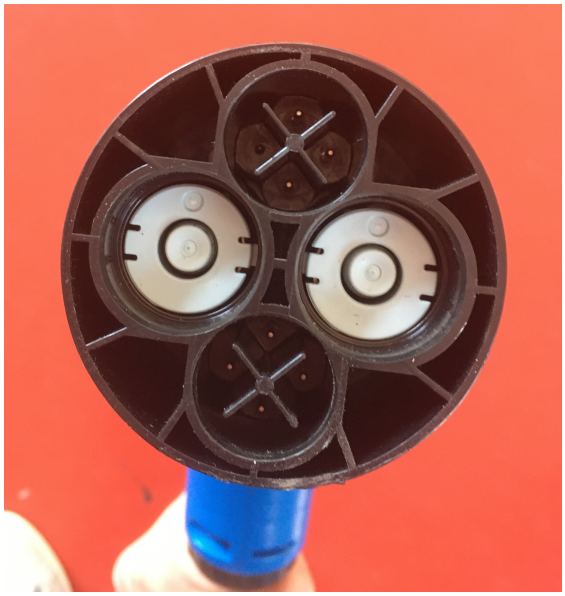

Figure 6.33: CHAdeMO connector

Table 6.7: Wallbox technical specifications

General specifications	
Frequency	45-65 Hz
Maximum AC current	20 A
Full power AC voltage	340-440 V
Standby power consumption	< 20 W
Peak efficiency	95.9 %
AC input specifications	
Input AC power connection	3phase + neutral + ground
Input voltage	340-440 V
DC output specifications	
DC output voltage range (G2V)	150-500 V
DC output voltage range (V2G)	150-450 V
Rated DC power (G2V)	11 kW
Rated AC power (V2G)	10 kW
Max. DC output charging current	36.7 A
Max. DC output discharging current	33.3 A
Connection standard	CHAdeMO

The vehicle used for the test is a Nissan Leaf e+ 2019 which comes with a 62 kWh lithium-ion battery (Figure 6.34).
The Nissan Leaf is capable of both DC and AC charging, as it is provided respectively of the CHAdeMO and Mennekes (Type 2) inlets. Only the CHAdeMO socket is of our interest.

Figure 6.34: Electric vehicle plugged

Chapter 7

Preliminary Laboratory Setup

This chapter wants to be a sort of brief logbook of the first experiences within the EC-Lab.
It is explained how the instruments were tuned and configured in order to be used in the PHIL methodology.
One by one each device involved in the simulation is gradually inserted inside the setup.
Furthermore, in the chapter is shown how the Simulink model was implemented step by step, using the components punctually described in chapter 5.

7.1 Virtual and Real world interface

A simple Simulink model was implemented: in the top level is visible the distinction between master and console subsystem.
Inside the master is placed the equivalent thevenin HV generator, the PI underground line, the *Measure1* and *Measure2* measurement blocks, the 11 kW internal load and the 4 kW additional load.
For each measurement block, the first voltage value is picked up and the effective value is calculated, in order to show it in the console subsystem.
A switch in the console subsystem permits the user to choose whether adding the additional load to the internal one or not.

Furthermore, the *OpCtrl* and the *AnalogOut* blocks are necessary to send the simulated load voltages to the RTS.
For each slot, 8 channels are available at the RTS, meaning that we can send to the RTS at maximum 8 signals. That is the reason why the mux block

has 8 inputs, but only the first three are used.
The RTS at its output ports makes available a voltage signal of ±16 Vpeak. For such reason, in the model a saturation block with this value is placed. Before the saturation block, a gain to resize the waveform is needed. The value is 16/350. The voltage waveform nominally is at 230 Vrms, that means its peaks are at around 325 V.
Precautionary, instead of 325 V, the value of 350 V was put.
In Figure 7.1 is shown the model just described.

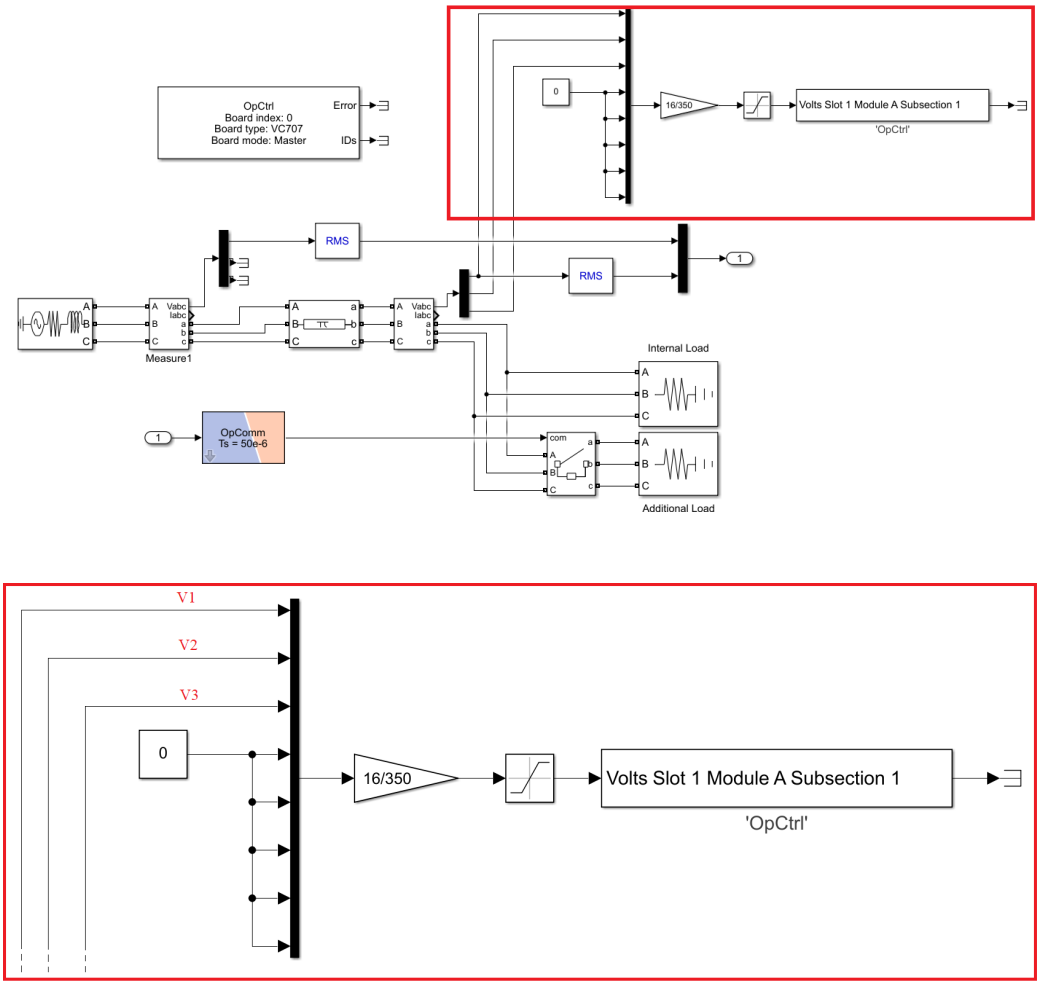

Figure 7.1: Output blocks inside the Master subsystem

In this section the connection with only the RTS is tested.
But first it is necessary to introduce the real-time simulator configuration (for preliminary details see section 6.3.

The RTS presents its I&O ports in the front panel (Figure 7.2).
Here are distinguishable a first series of BNC sockets on the left side, numbered from 00 to 15, which are the analog output ports.
At the right side the BNC channels are again numbered from 00 to 15, but this ports are related to the analog inputs.

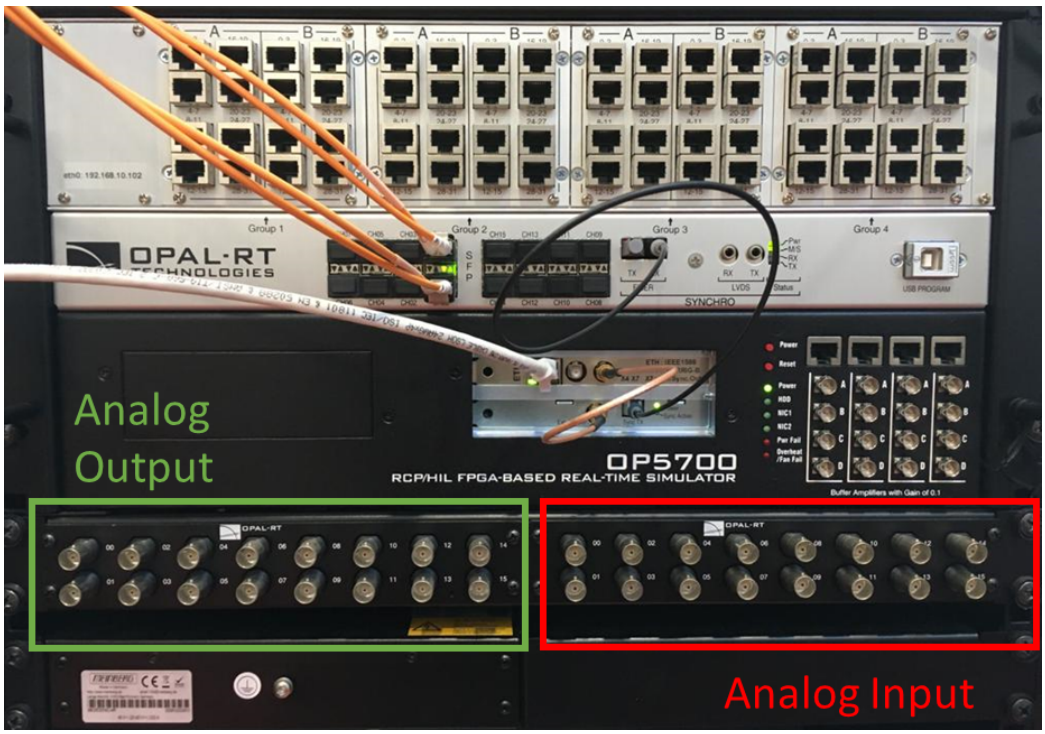

Figure 7.2: RTS front panel - BNC sockets

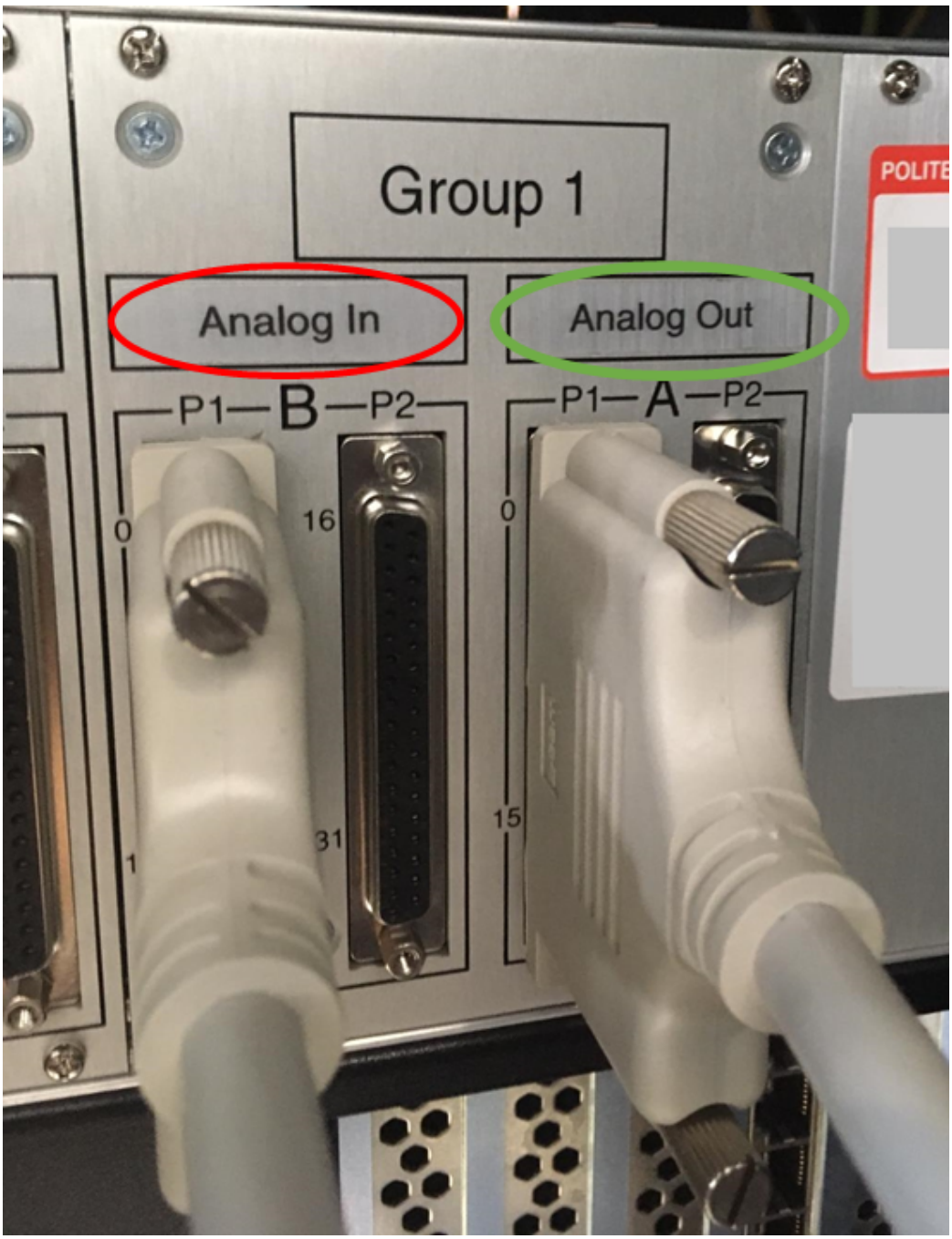

Figure 7.3: RTS rear side

As can be seen from Figure 7.3 which shows the rear part of the RTS, two DB37 connectors are plugged. The first one (left to right) is responsible to receive the input signals from the ports located at the front panel. The con-

nection is labeled as: Group 1, Module B, Slot P1. When the *AnalogIn* block is inserted into the Simulink model, it is important to identify from which card the inputs are taken, thus it is necessary to write that label (section 5.5. The second (left to right) DB37 connector enables the output BNC ports at the front panel. In this case as well, in the Simulink model must be specify to which card the outputs are sent, in order to have them available at the front BNC sockets.

As the three voltages were placed at the first three places in the mux block, automatically they should be sent respectively to 00, 01, 02 RTS output ports.
The data acquisition system was connected as well to verify that the output of the RTS made available the three voltage signals (Figure 7.4).
The RTS output ports are BNC type, thus a cable BNC-banana is necessary to transmit the simulation signal voltages to the DAQ. In fact, the DAQ channels present banana input sockets. In table 7.1 are shown the connections for this test.

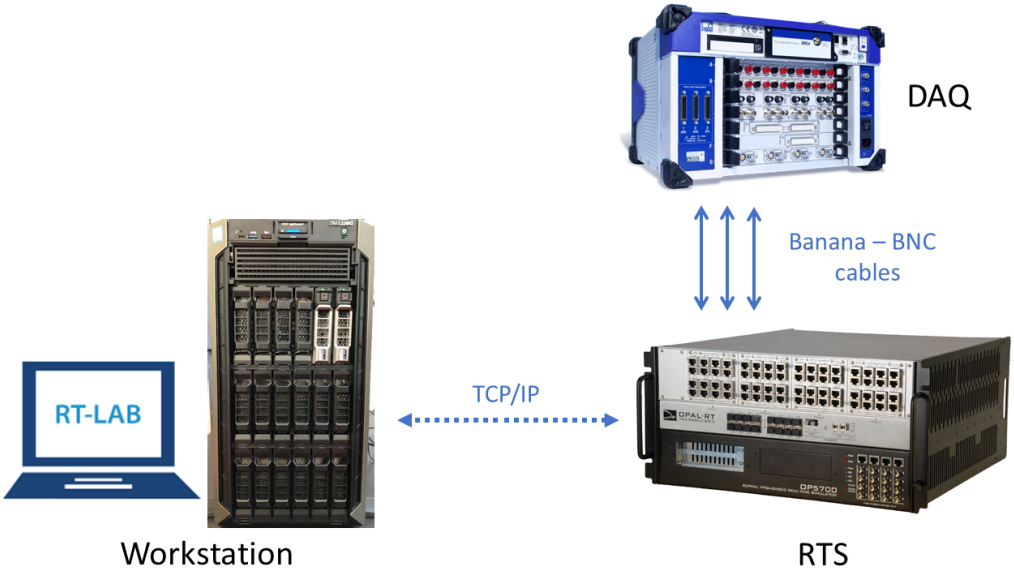

Figure 7.4: RTS-DAQ connection

RTS output port	DAQ channel
00	A1
01	A2
02	A3

Table 7.1: RTS-DAQ connections

Through Perception (DAQ software) the reduced voltage waveforms (max. $\pm 16\,\mathrm{V_{peak}}$) are correctly visualized.
The RTS communication works properly, thus it is possible to proceed to the next step: the addition of the power amplifier.

7.2 Power Amplifier addition

The voltage signals made available at the RTS output can be now sent to the power amplifier.
Its available connections are shown in Figure 7.5 and explained in table 7.2

Figure 7.5: BNC sockets of the power amplifier

Port	Function
J13	pilot input Phase 1
J14	voltage image output Phase 1
J15	current image output Phase 1
J23	pilot input Phase 2
J24	voltage image output Phase 2
J25	current image output Phase 2
J33	pilot input Phase 3
J34	voltage image output Phase 3
J35	current image output Phase 3

Table 7.2: Power amplifier signal connections [24]

With the addition of the PA, the new qualitative scheme is in Figure 7.6. As the voltage signals are transmitted from the RTS output to the PA input, the BNC sockets used are the input ones (see table 7.3 and Figure 7.7).

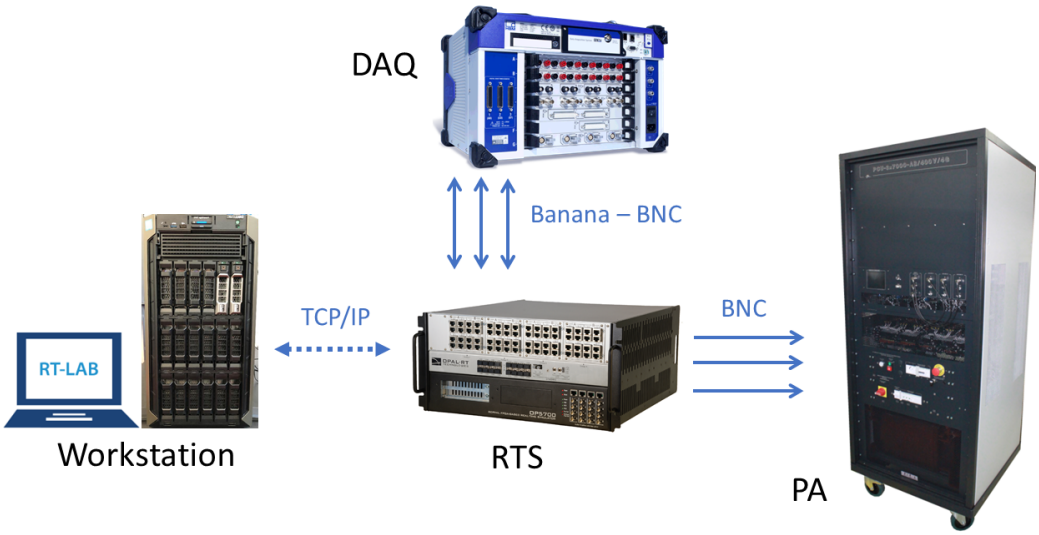

Figure 7.6: RTS-DAQ-PA connection

RTS output port	DAQ channel	PA port
00	A1	J13
01	A2	J23
02	A3	J33

Table 7.3: RTS-DAQ-PA connections

Figure 7.7: PA input connections

The input ports of the power amplifier accept at maximum ±15 Vpeak voltage signal.
Before we had to pay attention to the RTS output limit (±16 Vpeak), but now the PA introduced a smaller limit.
Therefore the gain block and the saturation block, described in the previous section, must be modified to reduce both of them: where it is set 16, it must be changed to 15.

So far, we just added the power amplifier instrument. The reduced voltage waveforms (max. ±15 Vpeak) are received by the PA via the input ports.

7.3 Power & Signal output of the Power Amplifier

The power amplifier presents its signal connections (Figure 7.5) at the front panel, while the power output is the backside.

The power output, which will be responsible for the wallbox supply, provides

the three voltage waveforms obtained as input (J13, J23, J33) but increased of a gain of 1/0.02619 (value determined by the range and the mode used) [24].

The voltage image output ports (J14, J24, J34) simply make available the image of the voltage at the amplifier power side.
The image, as the other signals, has a range of $\pm 15\,\mathrm{V}$peak.
This means that a gain is applied to pass from the real voltage value to the image: it is 60.2.

The figure 7.8 should help to comprehend the gain configuration.

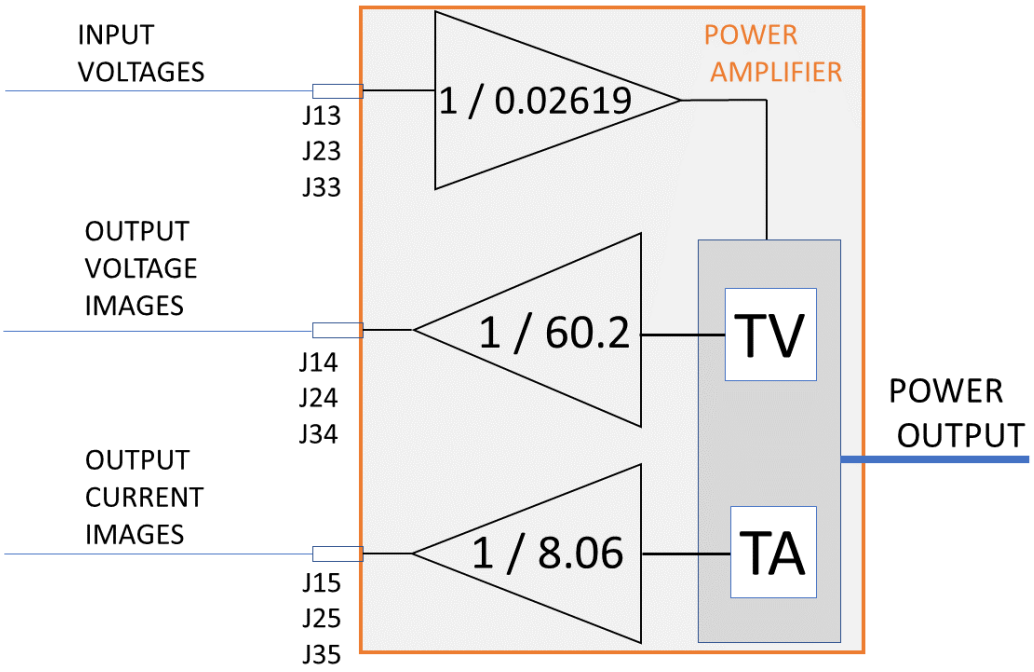

Figure 7.8: Power amplifier and gains representation

Inside the Simulink model a little modification is made: the gain block changed its value from 15/350 to 0.02619.
This way, at the PA power output are available voltages with the same value of the ones in the simulation 7.9.

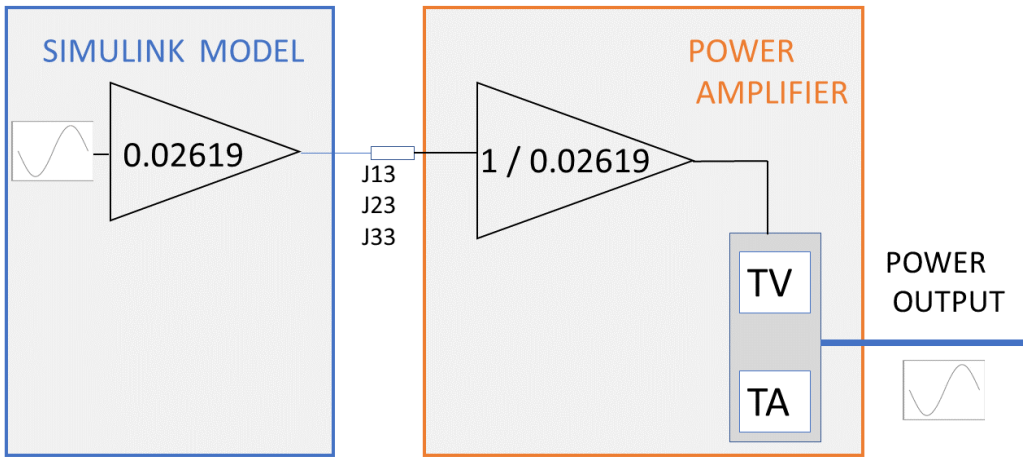

Figure 7.9: Reciprocal gains

The power amplifier itself has an internal measurement system which measure the voltage and current values on the power side. The measures are visible on the touchscreen display (Figure 7.10).

Figure 7.10: Measurement screen (random experiment)

The PA power side can now be involved in the experiment layout (Figure 7.11).

From the figure it can be seen that it is not necessary to connect the yellow-green cable for grounding. This is due to the presence of the isolation transformer inside the power amplifier.

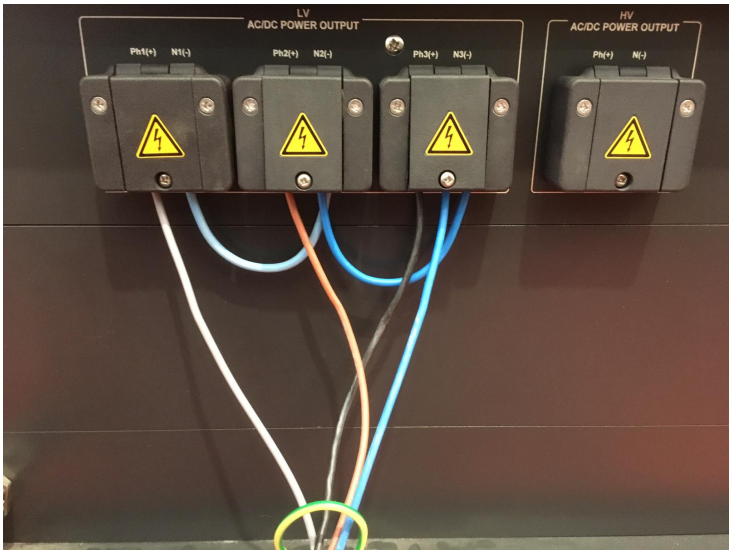

Figure 7.11: PA power output connections

For the moment, the power cables are sent directly to the DAQ (Figure 7.12) in order to verify the correct functioning of the power amplifier (Figure 7.13).

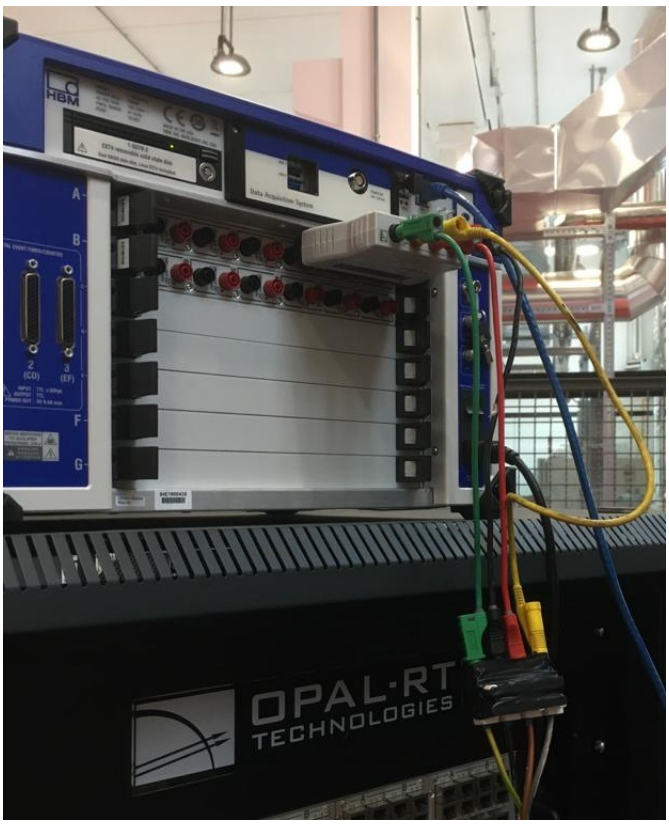

Figure 7.12: HBM and power cables from the power amplifier

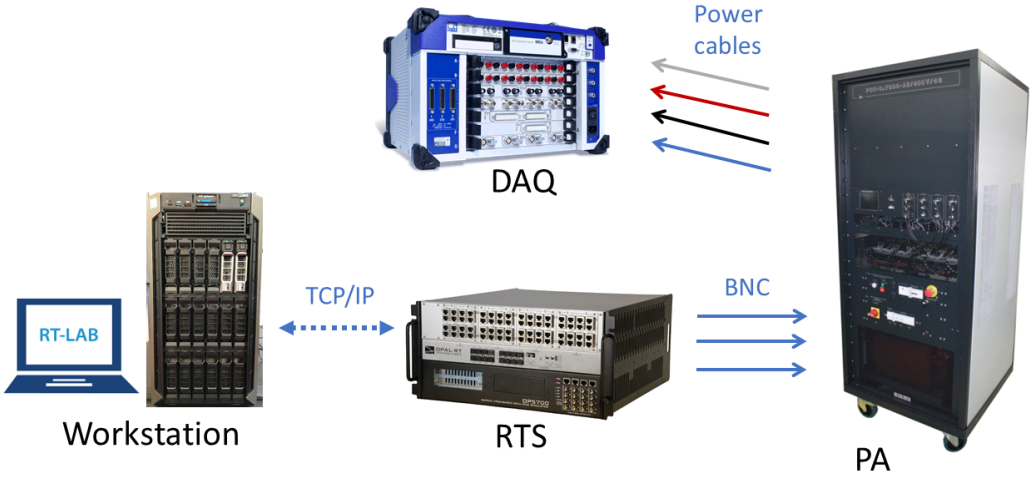

Figure 7.13: RTS-DAQ-PA connection (with power cables from PA)

7.4 Load Emulator

The following instrument to be added is the Load Emulator.
This device has the aim to replace the wallbox during the preliminary phase of the PHIL setup.
Firstly, the substitution is necessary as a safety measure, thus to avoid damages on the charging station itself, which is definitive hardware under test.
Furthermore, the wallbox was not phisically available in EC-Lab. Hence, it was exploited the opportunity to test the simulation running with an available device.

For our purposes, the emulator is set as shown in Figure 6.25.

The load emulator, even if acting as programmable load, is able to provide to the grid all the energy that receives from the power amplifier. The energy is not wasted since the thermal dissipation is avoided.

Before connecting the load emulator, another measurement is requested to the DAQ.
Also the PA output current images are sent to the DAQ through BNC cables (Figure 7.14).

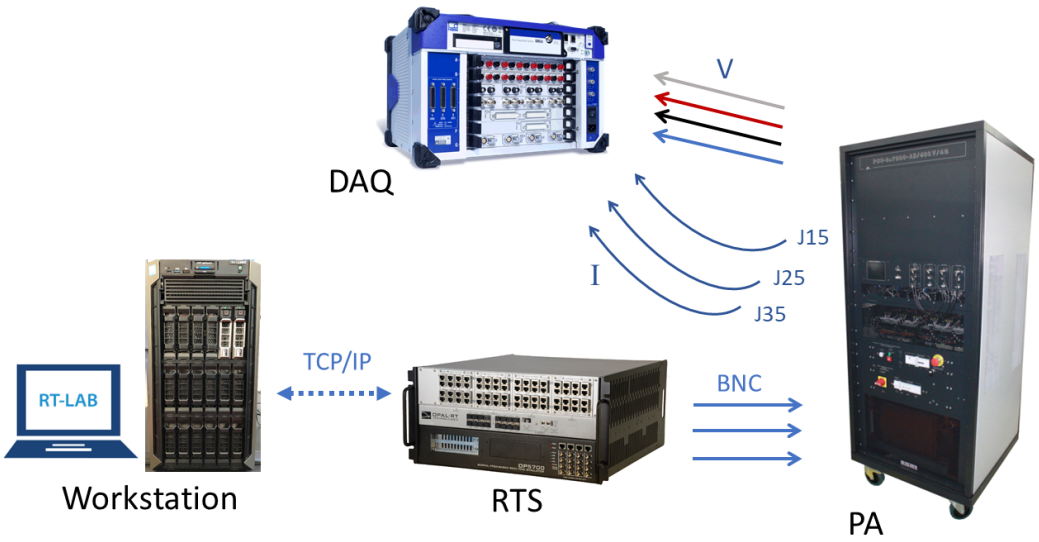

Figure 7.14: RTS-DAQ-PA connection scheme

As explained before, the BNC sockets for the current images are J15, J25, J35 which are connected directly to the HBM channels (respectively A4, A5,

A6). The DAQ channel configuration is exposed in table 7.4

DAQ channel	PA port
A1	J13
A2	J23
A3	J33
A4	J15
A5	J25
A6	J35

Table 7.4: DAQ-PA connections

It must be taken into account that the current image corresponds to a voltage signal which is 8.06 times smaller than the real current at the PA power output (see scheme in Figure 7.8) [24].

Finally, the emulated load can be inserted into the layout.
The new connections schematized in Figure 7.15 are then showed in Figure 7.16.
From the EL terminals, two three-phase cables depart: the one on the right is connected to the PA power side, the one on the left goes to the DAQ for the voltage visualization.
To recap, the PA receives from the RTS the voltage signals (J13, J23, J33) and sends as output the current images (J15, J25, J35).

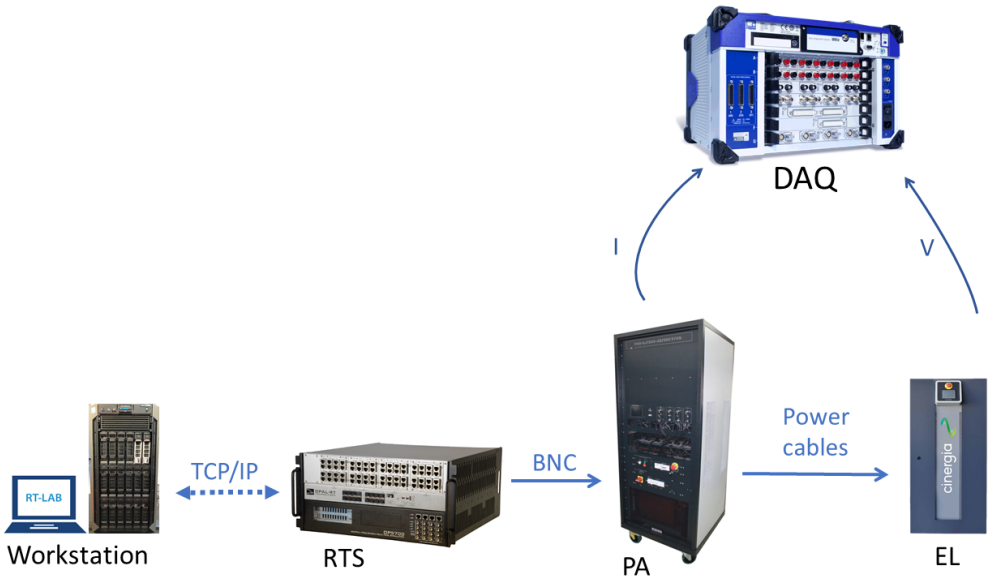

Figure 7.15: Complete connection scheme (open loop)

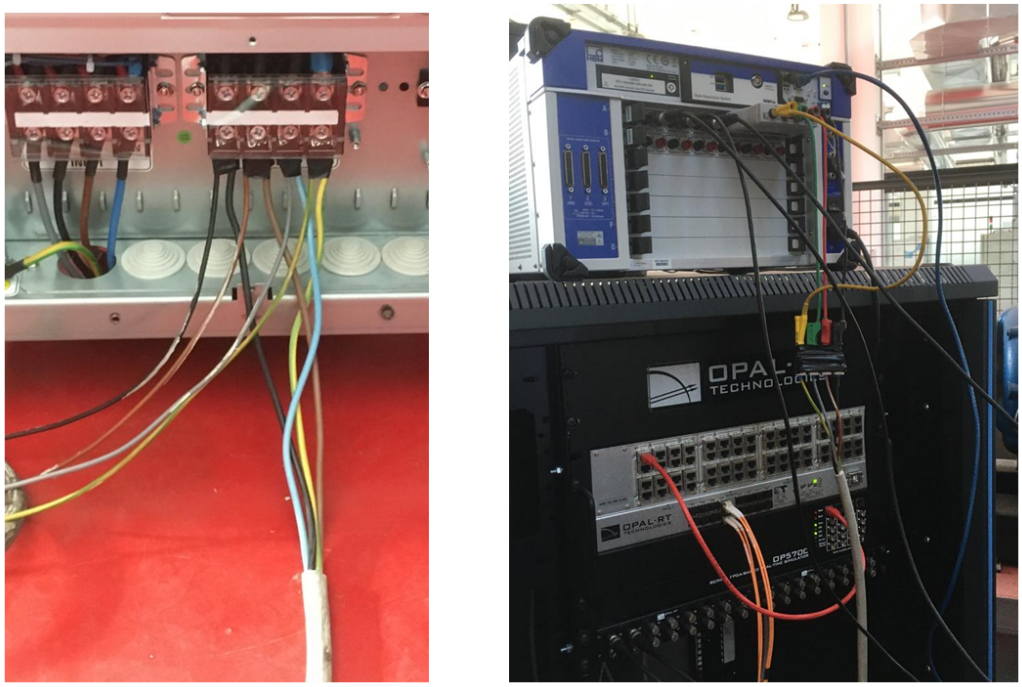

Figure 7.16: Emulated Load terminals (left), DAQ connections (right).

The HBM channels are now configured as in table 7.5.
Hence, since the emulated load is directly supplied by the amplifier, through

Perception is possible to visualize the voltages (A1-A3) and the currents (A4-A6) of emulated load.

DAQ channel	EL	PA port
A1	Phase 1 voltage	-
A2	Phase 2 voltage	-
A3	Phase 3 voltage	-
A4	-	J15
A5	-	J25
A6	-	J35

Table 7.5: DAQ connections (PA & EL)

Through the proprietary software of the emulated load it is possible to set its parameters.
Many trials were performed using the EL as a constant power or a constant current load. In particular, for the current load, it is even possible to set the harmonic content.

7.5 Closing the loop

At this point, every useful device has been tested and its correct functioning has been verified. Next aim is to close the loop to have the definitive PHIL configuration. Also, it is important to check that instability problem do not occur.

The PHIL layout with the use of the emulated load as DUT is shown in Figure 7.17.

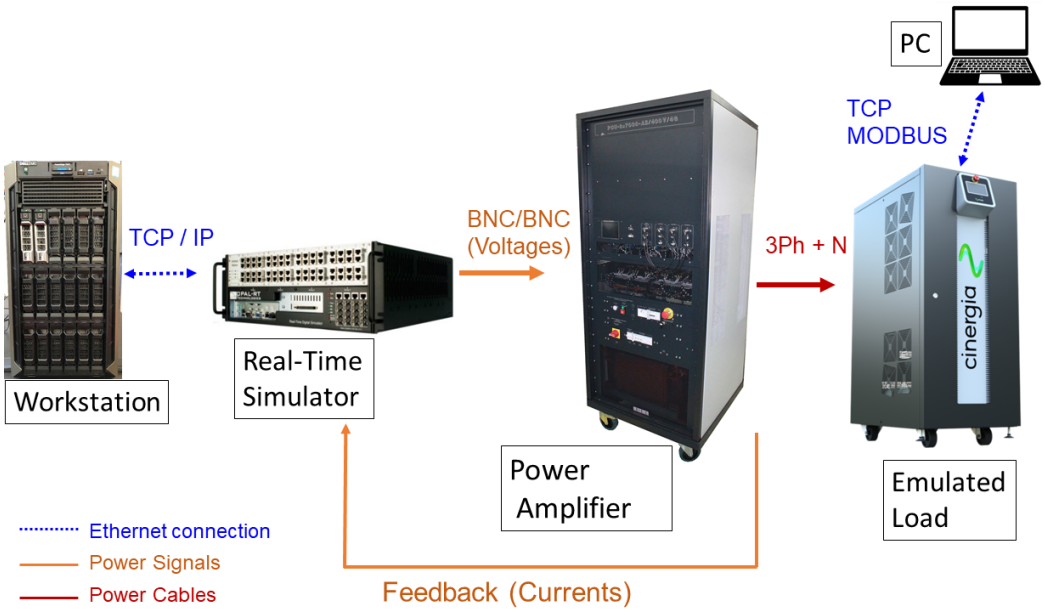

Figure 7.17: Closed loop qualitative scheme

To close the loop it is necessary to obtain as feedback the information the DUT current values. The current which flows inside the load emulator (DUT) is provided by the power amplifier. Thus the information on the currents values is given by the current images of the PA.
To close the loop, the current images available at the PA output ports (J15, J25, J35) must be sent to the RTS.
The front panel of the real-time simulator with the BNC sockets was shown in Figure 7.2.
Hence, it is reminded that the left side of the panel is connected with the analog output, while the right side is related to the analog input.

A coaxial cable transmits the current image from the power amplifier to the real-time-simulator (Figure 7.18). The connection are summarized in table 7.6

Figure 7.18: RTS input ports used

PA port	RTS bnc channel
J15	00
J25	01
J35	02

Table 7.6: Current images transmission (PA-RTS)

Apart from the physical connections, the Simulink model must be edited too. The *AnalogIn* block is finally added and the first three signals (which corresponds to the channels 00, 01, 02) are used inside the simulation as the three currents (Figure 7.19).
The gain is necessary to counteract the reduction gain inside the power amplifier.
The ReceiveStatus flag is a binary output of the *AnalogIn* block, which is 1

if the acquisition is occurring.

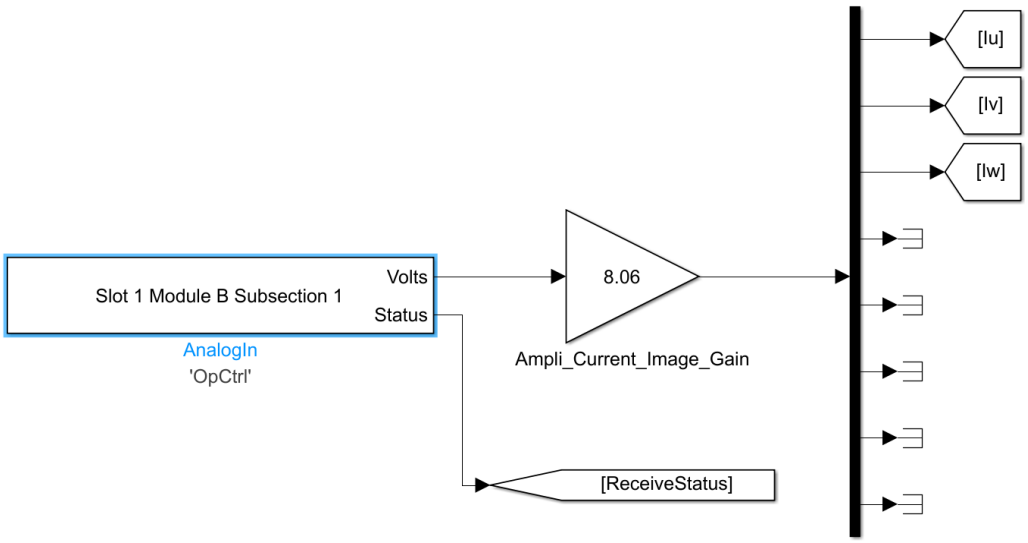

Figure 7.19: Input acquisition in Simulink

A second modification is the removal of the additional 4 kW load in order to replace it with the current source controlled generators.

A first attempt of modeling the real load is shown in Figure 7.20.
Here the model shows issues, since the circuit breaker and the current generator cannot be placed in series.

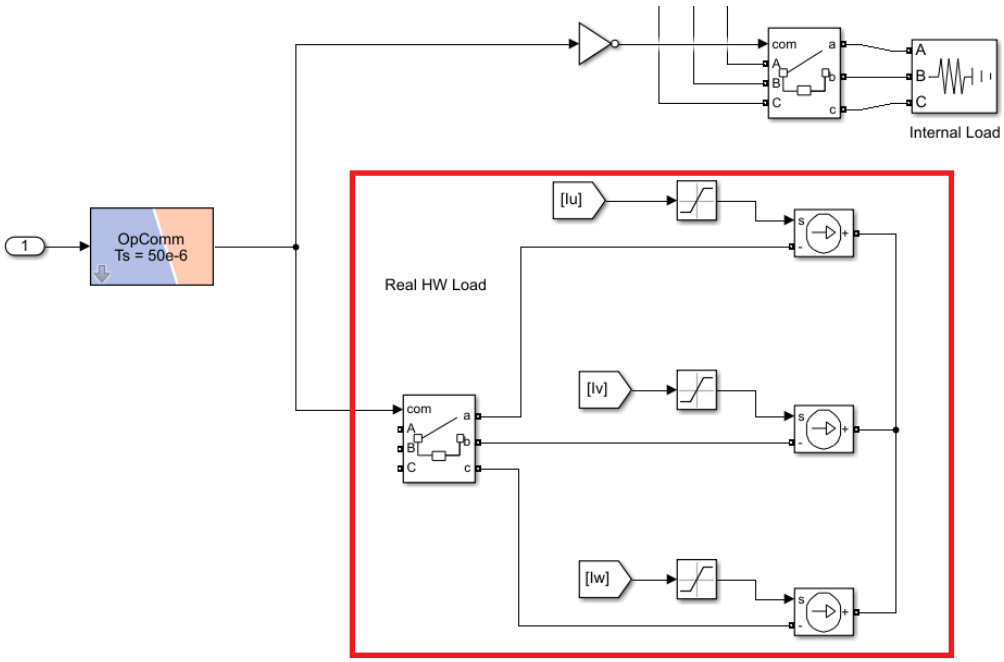

Figure 7.20: Current generators

To solve this issue, a 1 MΩ resistor per each phase was added in parallel to the source (Figure 7.21).

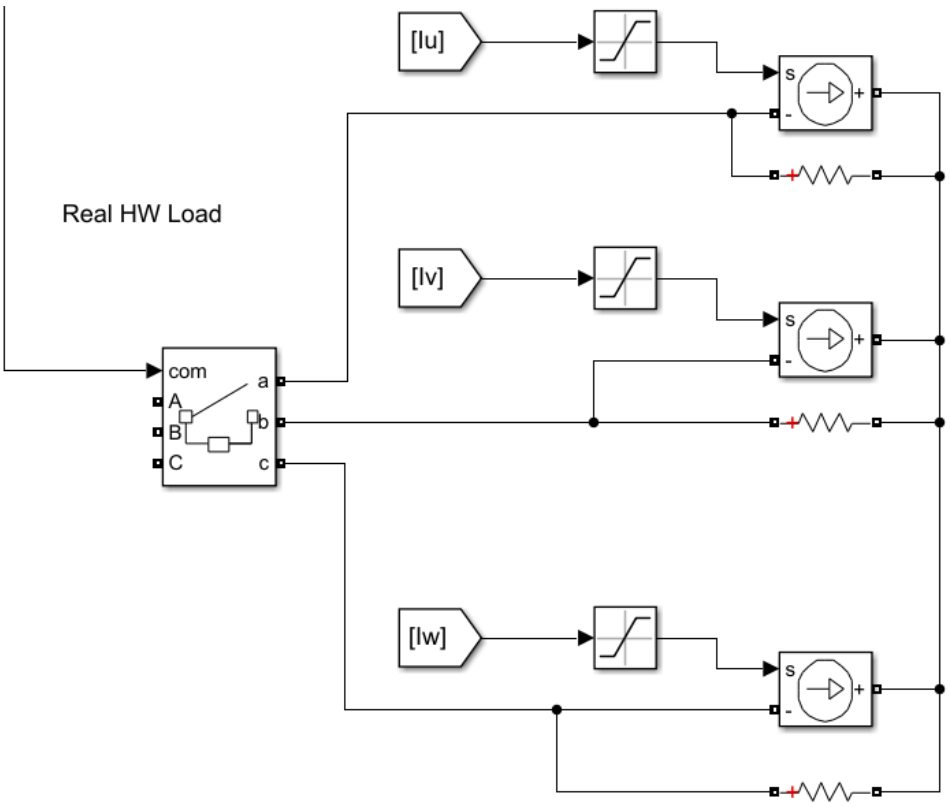

Figure 7.21: Current generators and resistances

Also with this configuration, the system shows instability: even if the switch is disconnected, the voltage value on the resistance is very high.
The value is so high that the circuit breaker was bypassed.

The ultimate configuration for the real load modeling, which is correctly functioning, is the one described in section 5.3.2.

Once verified that the closed loop is properly implemented, the emulated load can be replaced by the V2G charging station (Figure 7.22).

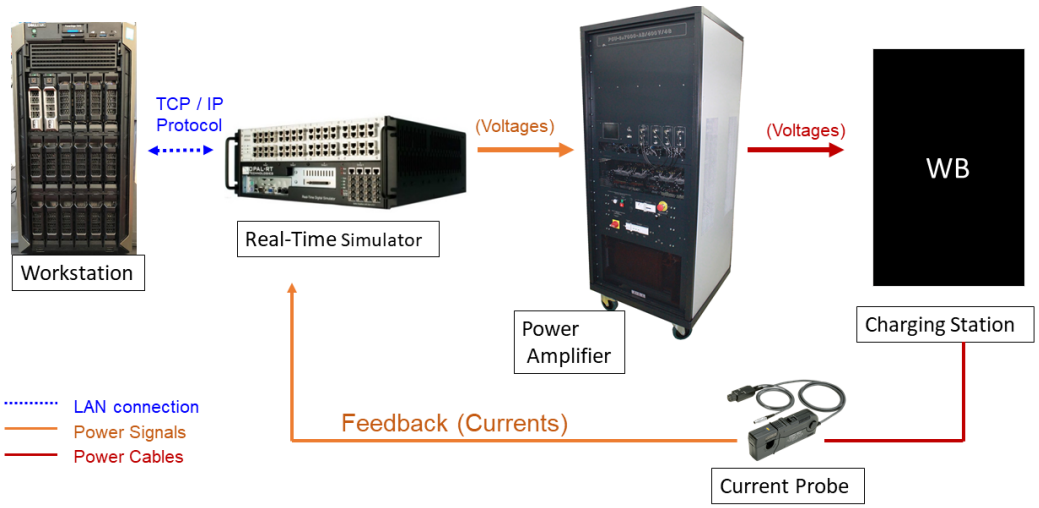

Figure 7.22: Definitive PHIL scheme

Chapter 8

Test Preparation

In this chapter is firstly given a brief description of the general procedure to execute a test.
Before explaining how the post processing was done, the laboratory configuration is illustrated.
Subsequently the test planning of the project is introduced.
Finally some characteristics of the V2G charging station are explained.

8.1 Procedure and Test Introduction

Thanks to the measurement setup, for every test to be performed it is possible to obtain many electrical parameters.
For both the AC and DC side are available all the currents, the voltages and the power values (active for DC; active, reactive and apparent for AC).
The acquisition varies according to the aim of each test. For some tests it is sufficient to acquire each real-time value every 10 minutes (such as the *Charging and Discharging Time Evaluation*). While for other tests, for example, it is necessary to record a whole acquisition window of 2 seconds.
The general initial procedure to conduct the test is described below.

```
INSTRUMENT SETTINGS

    - Switch on the RTS
    - Switch on the DAQ
    - Open DAQ software
    - Clamp the DC current probe
        (on one battery cable underneath the bonnet)
```

```
    - Clamp the three AC current probes
      (on the protection box supply power cable)


MODEL

    - Open RT-Lab
    - Project 'Project\_Name' -> Models 'Models\_Name'
    - Build the model
    - Load the model
    - Execute the model
    - Set the desired AC voltage value from the console block


START

    - Check open state of the switches (protection box)
    - Connect the plug of the protection box supply power
      cable with the socket of the amplifier power
      output (see Figure \schema).
    - Switch on the power amplifier
    - Set the PA. From the touchscreen display:
       menu "PCU-3x7000-AC-DC-400V-54A-4G"
       window "Configuration"
       impose settings as in Fig. \ref{fig:PAconfig}.
    - then:
       menu "PCU-3x7000-AC-DC-400V-54A-4G"
       window "Program "
       impose settings as in Fig. \ref{fig:PAconfig}.
    - Close the protection box switches
    - Wait until the WB led turns blue
    - Plug the CHAdeMO connector into the EV
    - Push the WB button
    - Verify that the WB led turns green
    - Verify that all the waveforms
      (AC and DC voltages and currents)
      are correctly visualized on Perception


COMMUNICATION SETTINGS
```

```
- Send the power setpoint request through the LabView
    project or the other function
    (Immediate Charge, SoC schedule) through the app.
- Check if the request has been received correctly.
```

Figure 8.1: Power amplifier settings. Configuration (left), Program (right)

Before executing any test, the thermal equilibrium was reached by simply powering the charging station for some minutes. This should reduce the temperature influence on the measurement, decreasing the potential errors.

On board the vehicle is present a battery diagnostic device.
Communicating with the battery management system, the diagnostic device is capable of measuring many battery parameters and sending the samples to a cloud where they are stored.
The parameters recorded are for example the cell voltages, cell temperatures, DC voltage, DC currents, DC power and so on.
Among these, two different SoC readings are available: *SoC Real* and *SoC Display*. Explaining the difference between the two parameters is crucial.
The SoC Real is intuitively the real battery capacity level, while the SoC display is the value readable from the user as it is displayed on the EV dashboard.
The wallbox has its own measurement system and, through API requests, it is possibile to ask the SoC and AC side power readings. The two parameters are sampled every 10 second if the wallbox is running. The SoC provided by the wallbox reading is the SoC Display read by the battery diagnostic device.

That is one of the reasons why the SoC Real was not taken into consideration.
Therefore, all the SoC values printed and provided in the chapter coincide with the SoC Display.

Another reason is that the SoC display is a more precautionary value respect to the SoC Display.
At lower battery capacity, the SoC Display is way lower of the SoC Real. Increasing the SoC, the display value approaches the real value up to slightly exceed it when the battery is almost definitively charged.
This difference is due to prevent the user to fully charge and discharge the battery, in turn safeguarding the battery health. Indeed, chemical and thermal stress occur at extreme SoC values.

The battery diagnostic device helps the measurement setup in the data acquisition. As a matter of fact, in some tests some figures obtained by the diagnostic device are shown.

8.2 Laboratory Configuration

As will be explained later, all the tests are performed without the Power-Hardware-In-The-Loop simulation.
The wallbox was evaluated as stand-alone device and not in a simulated environment.
This is due to the fact that, in this beginning phase of the project, only preliminary tests are performed on the charging station.

The charging station is supplied not from the electrical grid but from the power amplifier.
This choice comes from the need to impose different testing voltages to the wallbox.
With the traditional connection to the grid, it is not possible to change the voltage value. The AC mains should supply a phase-to-neutral voltage of 230 V, but in truth at the socket is not available a perfect sinewave of that amplitude.
Disturbs are always present and this is a factor able to falsify the result of the tests.

Conversely, if the wallbox is connected to the power amplifier, it receives a perfect sinusoidal waveform of the desired amplitude.
In Figure 8.2 is shown the equipment chain to supply the wallbox with the desired voltage.
Although the Real-Time Simulator was used, the loop was open and not closed. This means that the behaviour of the WB does not influence the applied voltage.
To explain better, in Simulink a simple model is built. In few words, the model consists of a 50 Hz sinusoidal waveform block and of a constant block through which the amplitude is decided time after time by the user.
The Simulink model is opened via RT-LAB, that is the RTS software. In fact, the desired voltage is sent to the RTS output, which in turn is passed as a signal to the power amplifier.
More details about the connection are given in the chapter 6.
Finally the output power of the PA supplies the wallbox.

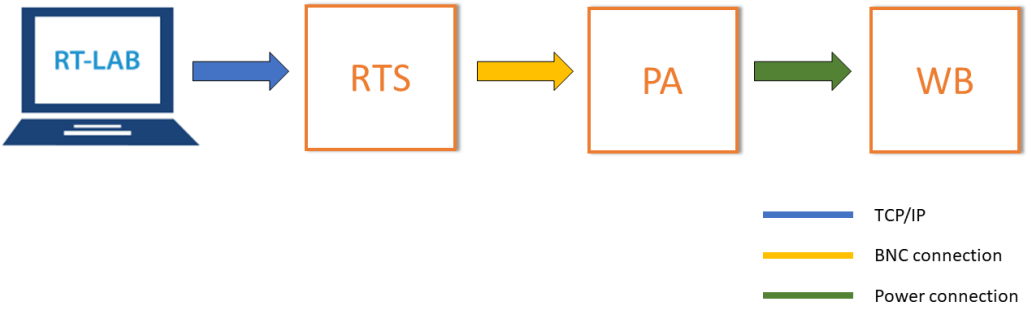

Figure 8.2: Qualitative chain of the wallbox supply

As showed in table 6.7, the charging station has an AC side phase-to-phase voltage operating range of 340 - 440 V, while the nominal value is 400 V.
In many tests the wallbox is fed with three different voltage conditions: nominal value, maximum allowable value and minimum allowable value. Respectively: 400 V, 440 V, 340 V.
In the Simulink model a phase-to-neutral value must be inserted.
According to the eq. 8.1, values showed in the second column of the table 8.1 should be inserted into the model.
For safety reason, these values have been moved towards the nominal value.
In conclusion, the phase-to-neutral voltage values to apply through the PA will be 200 V, 230 V and 250 V.

$$V_{pp} = \frac{V_{pn}}{\sqrt{3}} \tag{8.1}$$

	V_{pp}	V_{pn} calculated	V_{pn} test
Min. Voltage allowed	340 V	196.30 V	200 V
Nominal Voltage	400 V	230.94 V	230 V
Max. Voltage allowed	440 V	254.03 V	250 V

Table 8.1: Voltage values used in conversion efficiency test

In the tests performed in this document, the power amplifier is used to supply the wallbox.
It must be reminded that, in V2G operation, the energy supplied from the EV battery cannot be sent to the electrical distribution grid. As the power amplifier is not a reversible instrument, the energy must be dissipated thermally (always by the power amplifier).

In the basic configuration, the PA is not able to dissipate the rated V2G power (11 kW) in continuous operation.
In order to do so, a three-phase resistance load is added.
Therefore the PA settings must be changed before performing the V2G operation.
In truth, if the additional resistances are inserted, it is not possible to supply the wallbox in G2V mode at the rated power.
This means that actually every time the user wants to switch from G2V to V2G (and viceversa), he must take into account that some operations are limited. Otherwise the resistances can be easily added or removed.
In truth, if the V2G operation lasts a short time (3-5 minutes at the rated power), the amplifier is capable of dissipating the power without adding the resistors.
More details were given in section 6.4.

8.3 Data Acquisition and Post Processing

The DAQ has been used to measure, monitor, record and analyze the electrical quantities.
The experimental point of view, including the connections, has been analyzed in chapters 6 and 7.
In this section is illustrated the software point of view. The user interacts with the DAQ through the proprietary software *Perception*.
The software permits to visualize in real-time the measured waveforms (Figure 8.3).

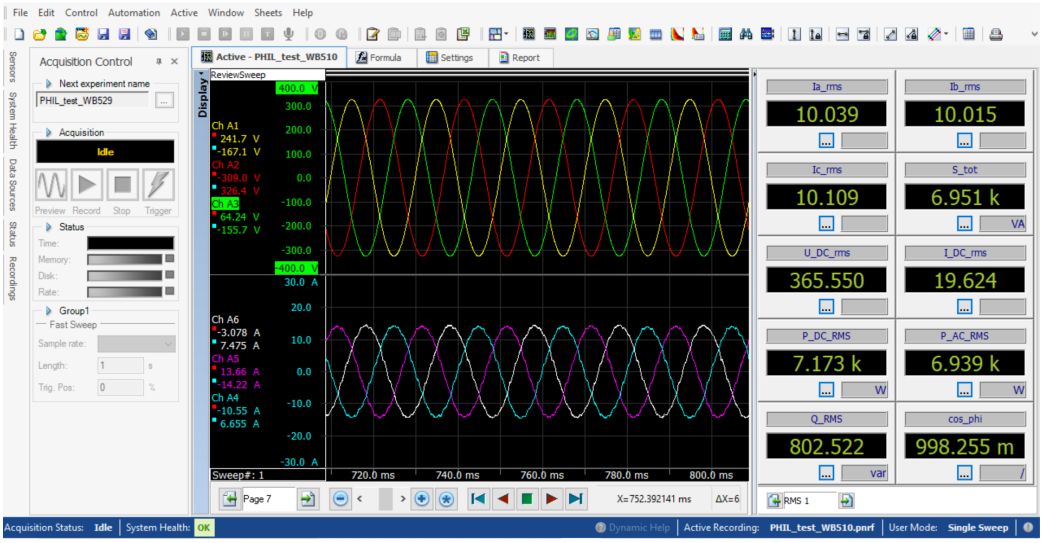

Figure 8.3: Perception interface

It is essential to deepen the knowledge of the software to be able of properly display the electrical quantities received at the channels specified in table 8.2.

	Parameter	Recorder	Channel
$v_{RN}(t)$	Voltage phase R	A	A1
$v_{SN}(t)$	Voltage phase S	A	A2
$v_{TN}(t)$	Voltage phase T	A	A3
$i_R(t)$	Current phase R	A	A4
$i_S(t)$	Current phase S	A	A5
$i_T(t)$	Current phase T	A	A6
$u_{DC}(t)$	DC Voltage	B	B1
$i_{DC}(t)$	DC Current	B	B2

Table 8.2: DAQ Channels

To each recording session corresponds a Perception experiment. The experiment is loaded into a workbench where all the settings are set accordingly to the purpose of the test.
The acquisition typology depends indeed on the recording time.

The first type is the Single Sweep and regards the recording of the waveforms for a limited amount of time, for instance 2 seconds.
To such acquisition window are applied the formulas previously saved in the workbench sheet named *Formula*.
Many tests, such as the *Wallbox Conversion Efficiency* and all the Interconnection Tests use this methodology.

A second typology (included in the Single Sweep mode) is the Real-Time acquisition, which is appropriate for long lasting test such as the *Continuous Output Power Evaluation* and the *Roundtrip Efficiency*.
This acquisition, since it is executed in Preview state, is enabled with the *Macro manager* setting.
The Macro function, in our case, is the automated recording at each step time (decided by the user) of the recorded parameters and of the real-time calculations.
The real-time formulas this time are implemented in the workbench settings, and are different formulas from the ones mentioned above.

8.3.1 Single Sweep formulas

The effective value (root mean square) is calculated for all the measured quantities (8.2) received at the input channels.
The rms calculation is extended also to the DC quantities in order to have

a parameter not related to the instantaneous time, but related to the whole measurement window.
In table 8.3 is shown the nomenclature of the effective parameters, which is useful for the formulas written in table 8.4.

$$X = \sqrt{\frac{1}{T_2 - T_1} \int_{T_1}^{T_2} x(t)^2 \quad dt} \tag{8.2}$$

V_{RN}	Voltage phase R
V_{SN}	Voltage phase S
V_{TN}	Voltage phase T
I_R	Current phase R
I_S	Current phase S
I_T	Current phase T
U_{DC}	DC Voltage
I_{DC}	DC Current

Table 8.3: RMS parameters in Single Sweep mode

The calculation of the AC active power (P_{AC}) is more complicated.
First of all, the instantaneous AC active power $p_{AC}(t)$ is obtained via eq. 8.3:

$$p_{AC}(t) = v_{RN}(t) \cdot i_R(t) + v_{SN}(t) \cdot i_S(t) + v_{TN}(t) \cdot i_T(t) \tag{8.3}$$

Afterwards, a Bessel digital low-pass filter is applied through the software function *FilterBesselLP*.
It is chosen a third order type with a cut-off frequency of 100 Hz.
Finally, the RMS value is applied in order to obtain a value not linked to the time instant.

Apparent Power	S	$v_{RN} \cdot I_R + V_{SN} \cdot I_S + V_{TN} \cdot I_T$
DC Active Power	P_{DC}	$U_{DC} \cdot I_{DC}$
Reactive Power	Q	$\sqrt{S^2 - P_{AC}^2}$
Power Factor	$cos\phi$	P_{AC}/S
G2V efficiency	η_{G2V}	P_{DC}/P_{AC}
V2G efficiency	η_{V2G}	P_{AC}/P_{DC}

Table 8.4: Perception Single Sweep formulas

8.3.2 Real-Time formulas

For our purposes, the Real-Time acquisition has been useful for the calculation of the energy.
In order to do so, it must be calculated the power first.
The instantaneous AC ($p_{AC_{RT}}(t)$) and DC power ($p_{DC_{RT}}(t)$) are obtained as in equations (8.4) (8.5).

$$p_{AC_{RT}}(t) = v_{RN}(t) \cdot i_R(t) + v_{SN}(t) \cdot i_S(t) + v_{TN}(t) \cdot i_T(t) \tag{8.4}$$

$$p_{DC_{RT}}(t) = u_{DC}(t) \cdot i_{DC}(t) \tag{8.5}$$

Then, for both AC and DC side, the energies ($E_{AC_{RT}}$, $E_{DC_{RT}}$) are calculated via *Integrate* function which indeed represents the mathematical integration (8.6) (8.7).

$$E_{AC_{RT}} = \int_{T_1}^{T_2} p_{AC_{RT}}(t) \quad dt \tag{8.6}$$

$$E_{DC_{RT}} = \int_{T_1}^{T_2} p_{DC_{RT}}(t) \quad dt \tag{8.7}$$

8.4 Planning of the Tests

In table 8.5 are listed the tests to carry out on the V2G charging station. The planning is not definitive. The bottom part must be detailed according to the project updated status and economy targets.
The tests which are already performed are described in the following sections of the chapter.

number	Test	Section
Characterization Tests		
1	"Power Setpoint" Setting	9.1.1
2	"Instant Charge" Setting	9.1.2
3	"SoC Requirement" Setting	9.1.4
4	Wallbox behavior	9.1.3, 9.1.5
5	Conflicts with the EV schedule	
Grid Interconnection Tests		
6	Power Factor Measurement	9.4
7	DC Current Injection Measurement	9.3
8	Harmonics Measurement	9.2
9	Response to Abnormal Frequencies	
10	Response to Abnormal Voltages	
11	Reconnect after Abnormal-Condition Disconnect	
12	Open Phase	
V2G Performance Tests		
13	Continuous Maximum Output Power	9.5
14	Conversion Efficiency Measurement	9.6
Reserve Services Tests		
15	Active Power Reserve Capacity	
16	Charging Time Measurement	9.7
17	Roundtrip Efficiency	9.8
Market Services Enabling Tests (Balancing, Congestion, FFR..)		
Business Case Scenario		

Table 8.5: Test list

- **Characterization Tests**: basic tests to be executed to better comprehend the wallbox logic and to get familiar with both APP and API requests.
  Setpoint, Instant Charge, SoC are the three settings available to the user.

- **Grid Interconnection Tests**: these are the tests required by IEEE Std 1547.1-2020 [18], IEC 62909-1:2017 [3] and CEI/IEC 61727-2004 [6].
  Purpose is to verify the compliance of the wallbox to be connected to the grid.
  These are pass/fail tests.

- **V2G Performance Tests**: the NREL (National Renewable Energy Laboratory) suggested a pair of tests in order to determine the vehicle's suitability for V2G applications [10].
  These are performance test, so there is no pass/fail criteria.

- **Reserve Services Tests**: ancillary services such as frequency regulation and spinning reserve are the most promising markets for V2G [10]. These test procedures (as well from NREL) are applicable to V2G vehicles that wish to provide reserve functions.

- **Market Service Enabling Tests**: these tests are again focused on the market application, but this time the charging station must comply with the requirements of the TSO for providing a specific service.

- **Business Case Scenarios**: This category represents the final chapter of the collaboration between Edison and Politecnico di Torino.
  Some market scenarios will be simulated to confirm that the wallbox is profitable and that it is able to provide the ancillary services requested by the network.
  These are the tests which require the Power-Hardware-In-The-Loop simulation.

In the next sections are evaluated only the tests which are referenced in the right column.
A future work for the continuation of the project consists in executing the tests which are not described and analysed in this thesis.

8.5 Wallbox Logic Overview

As explained in section 6.9, the charging station is capable of V2G mode. But if the rated power in G2V mode is 11 kW, the discharge nominal power is 10 kW. Both values are referred to the AC side, which means that in V2G mode the DC side of the wallbox could absorb more than 10 kW because of the internal WB losses.

The charging station presents a led in order to show its current status (Table 8.6).

Led color	Status
Red	OFF
Blue	Ready
Green	ON
Yellow	*Immediate Charge*

Table 8.6: WB status

8.5.1 Communication: API and APP Requests

The communication between user and wallbox is made possible through two different ways: API and APP requests.
Both ways are used for the preliminary tests (section 9.1, while for more complex tests the requests were made only via API as power setpoints cannot be imposed via APP.
To enable the requests, it is necessary to have the charging station connected to the internet. When the WB is not connected to the internet, only the charging process at 7 kW is enabled.

The API requests are sent through a LabView project.
In the project it is already implemented the whole recognition procedure.
It requires parameters such as the User ID, EV ID, the EVSE ID to first obtain the access token authorization and secondly to execute the commands.
The project permits the user to determine the operating power of the wallbox. Together with the desired power value, the schedule demands a time interval to which the setpoint is referred.
For the V2G operation the power setpoints are positive, while are negative if the G2V mode is desidered. Nevertheless this happen only in API request, as in the plot the signs are opposite: if the G2V operation is ongoing, a positive value is shown, and viceversa.

Must be told that all the setpoints are referred to the AC side of the wallbox, both in V2G and in G2V operation.

Other API requests are the visualization of the battery SoC (sampled every 10 seconds), the visualization of the AC power (sampled every 10 seconds), and the possibility to delete a scheduled power setpoint. Obviously the SoC is not measured by the charging station, but it is obtained by the wallbox through the communication with the EV via CHAdeMO CAN protocol [39].

The APP for mobile devices allows to monitor and command all the EVs connected to the charging station owned by the user.
It is possible to visualize the SoC of the vehicle and to send requests.
If via API it was possible only to set a power schedule, this time the functionalities are different. There is the *Immediate Charge* setting and the *SoC schedule*.
The SoC schedule is the analogous of the Power schedule that can be set via API.
Hence it must be set a time interval and a minimum expected SoC value: aim of the charging station is to provide to the user the SoC desired in the specified time window.
In theory if a desired SoC, higher than the actual SoC, is set for a close time interval, the wallbox automatically charges up the EV.
The Immediate Charge is a function which has priority on the previous requests. It disables every transaction in process on the wallbox and instantly charge the EV at nominal power (11 kW).
Moreover, without the Immediate Charge, the SoC requirement has priority on the power setpoint.

It is necessary to remind that the SoC readings available both from API and APP are referred to the *SoC Display* mentioned earlier in section 8.1.

8.5.2 Threesholds

The wallbox presents a minimum power threshold of 3 kW both in charge and discharge.
Every power setpoint lower than 3 kW (absolute value) is automatically raised up to such value.

Another threshold concerns the battery SoC. If during a discharge the percentage reaches the 35%, the discharging process is automatically stopped.

If a further discharge is requested via API at this point, the wallbox does not respond to the command.
Hence it is not possible to go below the 35% level through a discharging process.

The WB maximum power in G2V and V2G mode corresponds to the nominal values (respectively 11 kW and 10 kW) only when the WB is connected to the internet.
If the WB is not connected to the internet and it is turned on, a charge of 7 kW automatically starts regardless the battery SoC level.
The only exception is when the SoC is below the 35% and WB is connected to the internet: a charging process of 11 kW takes place to restore the 35% level, then it stops 8.7.

Internet	Charge/Discharge	SoC	Power
Yes	D	$\leq 35\%$	0 W
No	C	(any)	7 kW
Yes	C	$< 35\%$	11 kW

Table 8.7: Wallbox behaviors recap

Chapter 9

Test execution and results

In this chapter every test that has been performed is described, citing from which standard the test was taken, analysing the objective, detailing the procedure and finally observing the results.

9.1 Characterization Tests

9.1.1 Power setpoint and delay

Ideally, when a power setpoint is scheduled for a time window, the charging station is supposed to supply (or absorb) the desired power as soon the window starts.
In truth, a delay always occurs when fulfilling a command.
Aim of the test is to obtain information about the order of magnitude of the delay.
Some G2V power commands were made through API (table 9.1) and the delay respect to the expected start of the command was evaluated.
In Figure 9.1 there is the graphical representation.

Power value (AC side)	start time	end time	delay
3000 kW	200 sec	434 sec	38 sec
5000 kW	434 sec	666 sec	28 sec
7000 kW	666 sec	900 sec	10 sec
9000 kW	900 sec	1332 sec	1 sec
0 kW	1132 sec	1250 sec	9 sec

Table 9.1: Power setpoints and obtained delay

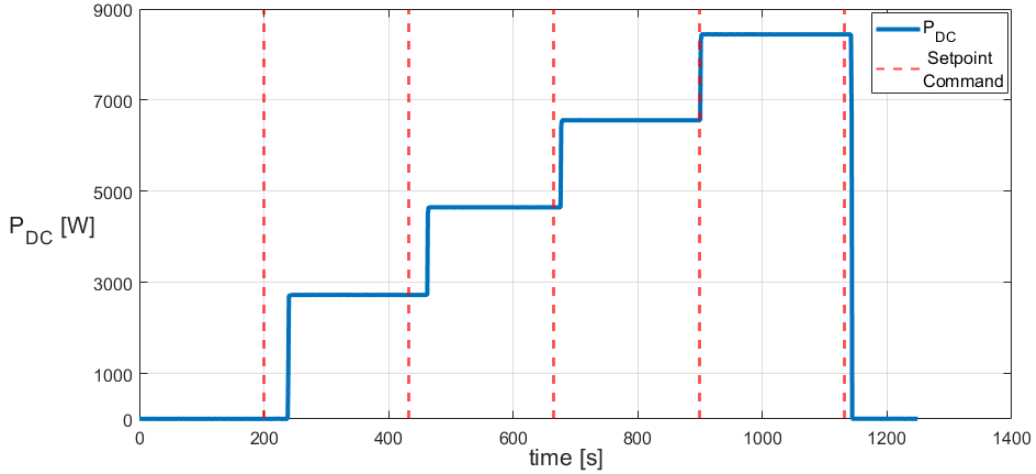

Figure 9.1: Power setpoint and delay

As may be noticed, the power values shown in table 9.1 are referred to the AC side, instead in the figure is plotted the DC power.
As matter of fact, being a charging process, the DC values are lower than the AC ones.

A trend line is the reduction of the delay time along the commands.
The response time delay might consists of different factors. Among them, the communication time between the charging station and the cloud plays a huge role.
It was not possible to measure it as it is not clear with which regularity the wallbox questions the cloud regarding the future commands, and with which frequency the cloud provides the commands to the wallbox.

Another trial was executed to further evaluate the delay when switching from the maximum G2V power condition to the maximum V2G power (and viceversa).
The intermittent graph is shown in Figure 9.2.
The delay between the expected start of the switching and the performed switching is below 20 seconds in most cases.
Furthermore, the change of power direction takes place rapidly without intermediate power steps: no power modulation occurs.

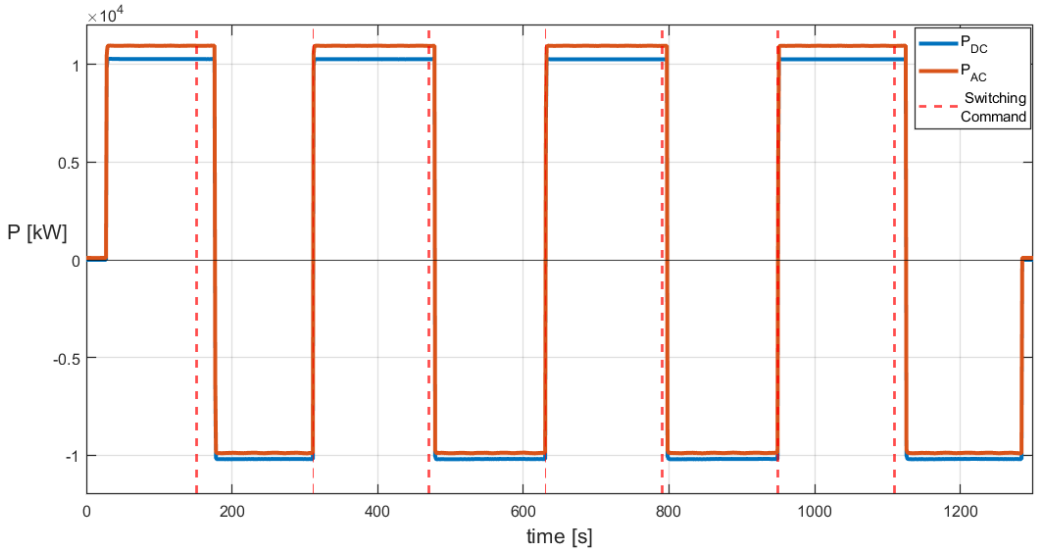

Figure 9.2: Switching between rated power values

Power value (AC side)	start time	end time	delay
−10 kW	152 sec	311 sec	26 sec
11 kW	311 sec	471 sec	1 sec
−10 kW	471 sec	631 sec	7 sec
11 kW	631 sec	790 sec	1 sec
−10 kW	790 sec	950 sec	8 sec
11 kW	950 sec	1109 sec	1 sec
−10 kW	1109 sec	1284 sec	17 sec

Table 9.2: Switching delays between rated power values

Here the difference between the DC and AC power values is more visible: in G2V mode (positive power values) the AC power is higher, while in V2G mode (negative values) the AC power absolute values are slightly lower.
Still, it can be appreciated how the difference between AC and DC power is not the same on both the operating modes. In the charging process, the power lost into the wallbox is higher.
Although the rated G2V power is 10% higher than the rated V2G power, this does not explain such huge difference.
In section 9.6 (Table 9.12) is observed how the efficiency for the V2G operation is higher respect to the G2V operation. Therefore the power difference aforementioned may be due to the distinct efficiency values.

In table 9.2 it can be appreciated how the delay to pass from a charging process to a discharging process is way bigger than the delay occurring when passing from V2G mode to G2V mode.

9.1.2 Immediate Charge setting

In this test the APP setting *Immediate Charge* is evaluated.
The functionality is supposed to ignore the previous and ongoing commands sent to the WB and instantly impose a maximum power charge.

To test it, a discharging power setpoint of 7 kW was imposed to the charging station.
Intermittently, the *Immediate Charge* request was applied through APP. The response is immediate: the WB within few seconds stops the discharging process to start the 11 kW charge (Figure 9.3).

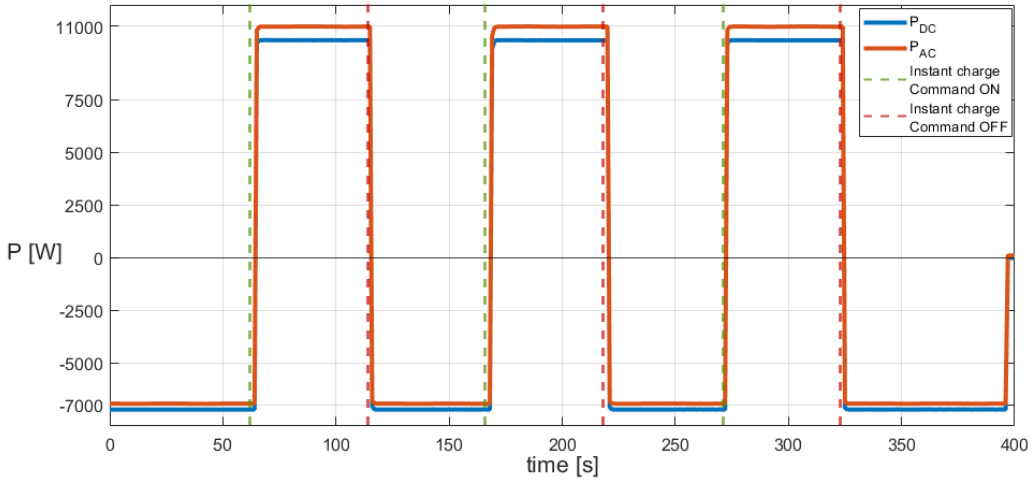

Figure 9.3: Immediate Charge function

As in the previous preliminary tests only power setpoints were scheduled, in this test it was also useful to evaluate the short delay between two different functions: the power setpoint imposed via API and the *Immediate Charge* via APP.
It was confirmed the priority status of the Immediate Charge in comparison to the power setpoint.

9.1.3 Power step resolution

When the user wishes for a precise power setpoint, it is not said that the charging station is able to provide the exact value desired.
It is possible that the charging station is able to comply the desired value by only reading the hundreds.
To be more precise, for example a setpoint of 7635 W could be automatically converted to 7600 W by the charging station.

The test aims to discover the sensibility of the wallbox.
Different setpoints have been tried, in Figure 9.4 are shown the most interesting ones.

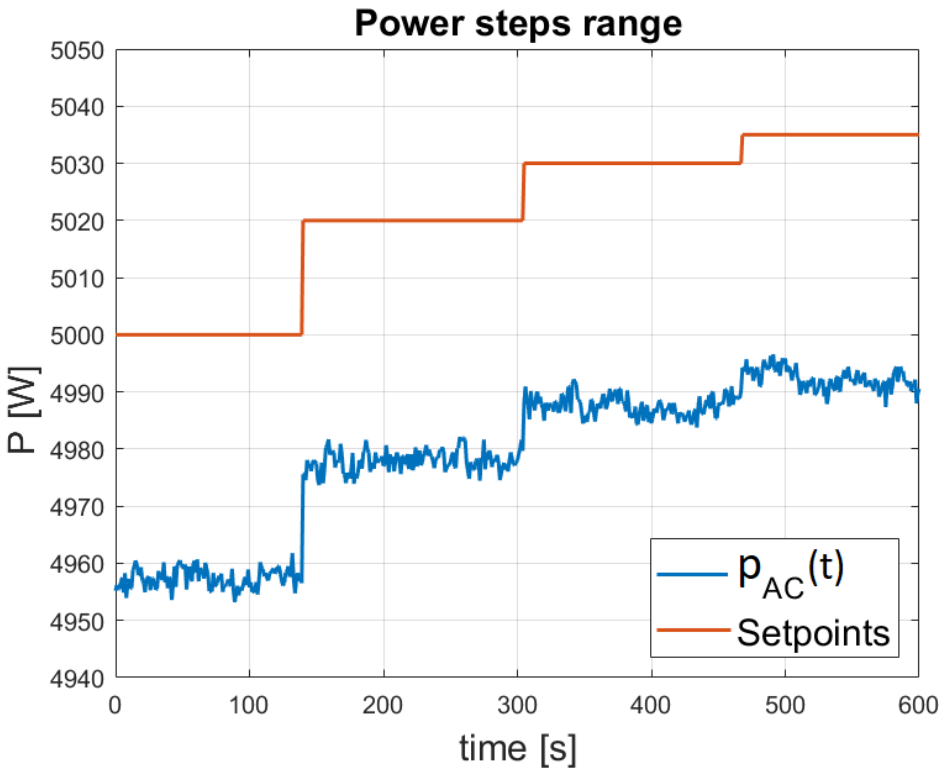

Figure 9.4: Power step resolution

Setpoint	Step
5000 W	-
5020 W	20 W
5030 W	10 W
5035 W	5 W

Table 9.3: Power step resolution

The y-axis depicting the AC power has a small range on purpose. In this way it can be appreciated the tiny and almost constant difference between the requested power and the effective measured value. The latter is slightly smaller.

The test result is surprising, as a resolution of 5 W is more than sufficient to comply to all the applications executable by the charging station.
Furthermore, smaller steps could not be appreciate in the plot, because of the noise affecting the power measurement (blue waveform).

9.1.4 SoC schedule

Apart from the Immediate Charge function, through the APP it is possible to set a SoC schedule. It consists of imposing a mininum expected SoC value for a defined time interval.

The basic functioning is shown in Figure 9.5.
A minimum SoC of 60% was scheduled for a time interval starting a few minutes after the request.

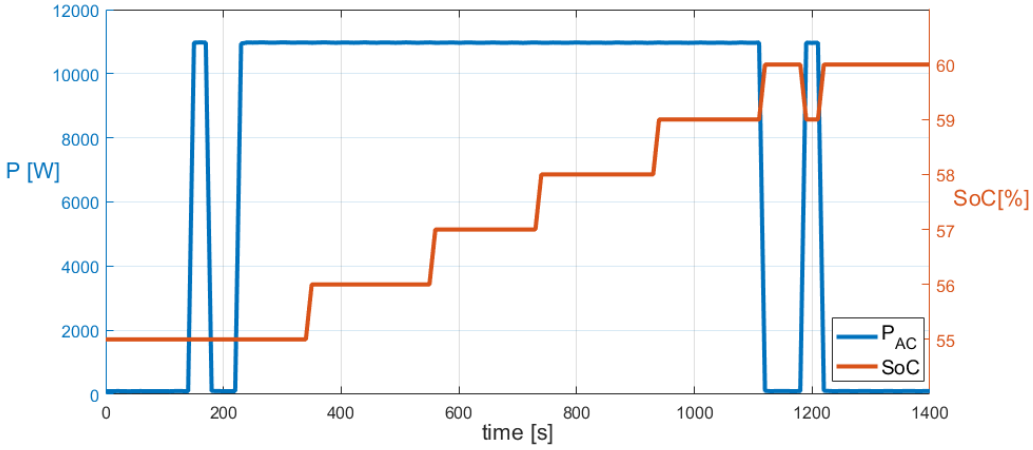

Figure 9.5: SoC schedule function

It may be seen how the charging station initially was not supplying any power and suddenly it started charging at maximum power.
There is a quick drop probably due to a communication loss.
Then the EV is constantly charged again at 11 kW until the 60% of SoC was reached.
Here the EV self-consumption decreased the SoC of a percentage value.
Instantly the WB supplied again with the maximum power in order to restore the 60% level.
Finally the charging power dropped to zero when the desired SoC was obtained.

Another trial was executed in order to test the priority status of the SoC requirement on the power setpoint schedule.
From the APP a minimum SoC of 75% is expected for a distant time interval.
Meanwhile a 3 kW V2G power setpoint was requested.

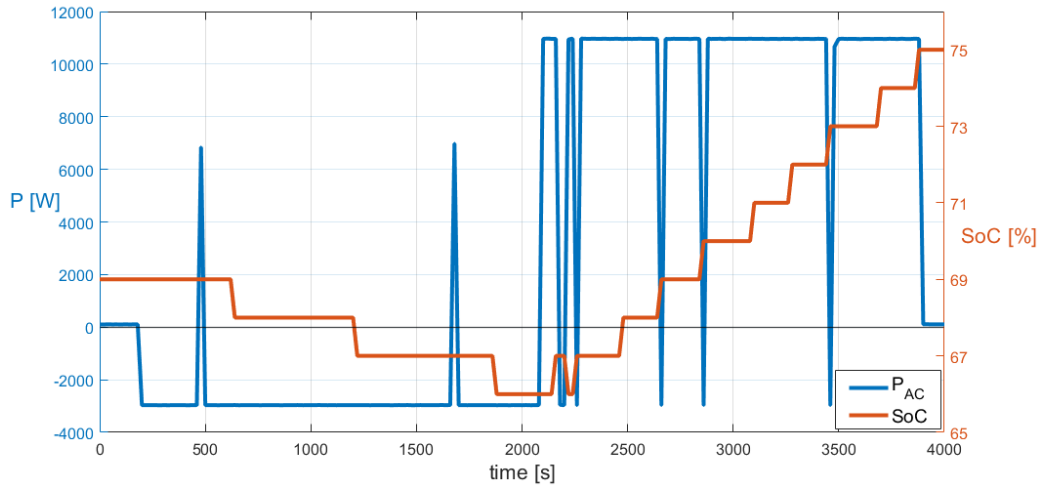

Figure 9.6: SoC schedule function 2

As depicted in Figure 9.6, the wallbox starts discharging the vehicle at the desired power, respecting the setpoint command.
From a certain point on, the wallbox tends to charge the EV at the maximum power in order to reach the 75%.
When the required SoC is reached, the charging power drop to zero.
The behavior of the charging station respected the priority of the SoC requirement on the power schedule.

Moreover, it is interesting to focus in the middle part of the plot. Here is visible the intermittent behavior of the WB, that might be generated by the conflict of having two active commands.
An hypothesis is that the charging station has a controller which calculates the time needed to reach the SoC required. If the WB would be able to reach the SoC value before the time interval in which it is required, it fulfills the power setpoint.
Drops and spikes present in the middle of the plot could be due to the controller calculations.

9.1.5 Power Derating

The Nissan Leaf battery uses the lithium-ion technology.
To extend the operational life of these kind of batteries, the derating (or depowering) process is applied from the battery management systems.
Derating consists in gradually decreasing the charging or discharging power when approaching a SoC limit (superior for the charge, inferior for the discharge) [41].

The full charging profile of the EV battery is shown in Figure 9.7.
It can be seen how two different behaviours occur. Initially the battery is charged at constant power. When the capacity is nearly full the power (and the current) decays exponentially, and the constant voltage phase starts.
It is speculated that the lithium ion battery adopts the CCCV strategy, which consist in performing a constant current phase (CC) first and then a constant voltage one (CV).
In our case it was not possible to obtain the CC phase as the power was controlled. In fact, to charge the battery, the nominal power setpoint (11 kW) was imposed. The wallbox took care of providing a constant power over time. But as the SoC increased, also the battery voltage increased. And to keep the power value constant, the current was forced to slightly decrease.
If the battery had been charged without a power setpoint (which means a power control), the full CCCV profile could have been appreciated, with a clear constant current phase.
It can be stated that the CV phase coincides with the derating process highlighted on the right.

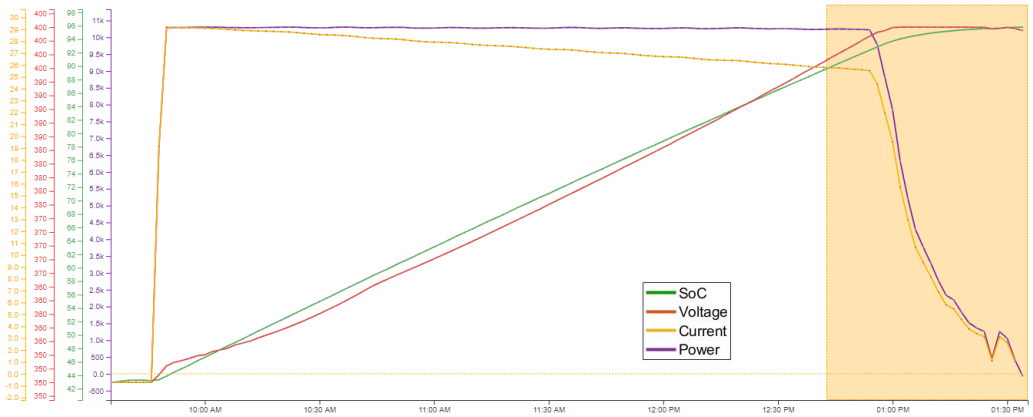

Figure 9.7: Charging profile - Derating

The derating during a charging process starts at a SoC right above 90%.
For completeness, also the discharging profile has been investigated (Figure 9.8). Here no inferior derating occurs.
For the whole discharging process the power supplied by the EV remained constant (10 kW for the V2G mode). Suddenly, at SoC=35% the power immediately dropped to zero.

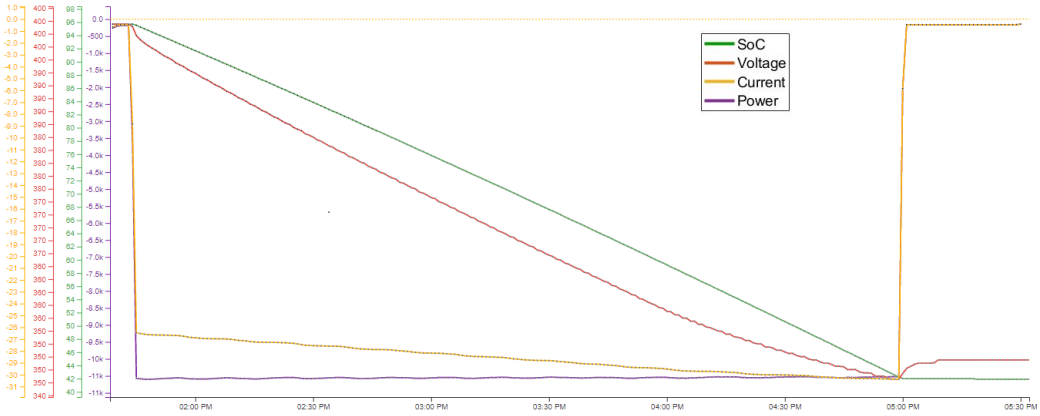

Figure 9.8: Discharging profile

9.2 Harmonics Measurement

Low levels of voltage and current harmonics depend upon distribution system characteristics, type of service and connected apparatus.
To ensure that no adverse effects are caused to the equipment connected to the utility system, the charging station output should have low current-distorsion levels.
Since the voltage waveform is imposed through the simulation, is supposed to be a quasi-perfect sinewave. Thus only the current harmonic content is measured.
The Harmonics Test aims to measure the individual current harmonics and the total-harmonic current distortion (THD) of the charging station under normal operating conditions.
Test procedure requirements are explained in [6] and [18].
This is a pass/fail test and the wallbox is considered in compliance if the individual current harmonics do not exceed the limits specified in table 9.4 when running at rated power.
Another requisite is that the THD shall be less than 5% at rated power [6].
Since the charging station is a multi-phase device, each phase must comply with the limits.

Odd harmonics	**Distorsion limit**
3^{rd} to 9^{th}	less than 4.0 %
11^{th} to 15^{th}	less than 2.0 %
17^{th} to 21^{th}	less than 1.5 %
23^{rd} to 33^{th}	less than 0.6 %
Even harmonics	**Distorsion limit**
2^{nd} to 8^{th}	less than 1.0 %
10^{th} to 32^{nd}	less than 0.5 %

Table 9.4: Current distorsion limits (respect to the fundamental) [6]

The suggested general procedure is exposed in IEEE Std. 1547.1 Section 5.11 [18].

To execute the test, both a charging and a discharging process (respectively at 11 kW and 10 kW) were imposed to the charging station.
Then, only the three AC currents were measured and saved by the DAQ.
To the six samples (three for G2V, three for V2G) a Fast Fourier Transform was performed.

The Fast Fourier Transform is an efficient method used to compute the discrete Fourier transform of a series of data samples, which are referred to as a time series). The result of the transform are the amplitude values but referred to as a frequency series [11].
In our case, the data samples are the AC currents and the result is a series of current rms values, each one referred to a specific frequency.
The length of the frequency series and its resolution depend on the measurement window length and the sample rate.
The measurements were done using a 2 s window length and a sample rate of 20 kS/s.
For our purposes, the maximum harmonic order to be measured was 33, which corresponds to 1650 Hz.
To avoid aliasing and information losses on the current signals, the Nyquist-Shannon sampling theorem claims that the minimum sampling rate shall be greater than the double of the maximum interested frequency [48].
Theoretically, a sample rate of 3.3 kS/s (sample frequency of 3.3 kHz) would have been sufficient.
The FFT was executed with a frequency resolution of 0.5 Hz, defined through the sampling rate f_s and the number of samples N:

$$\Delta_f = \frac{f_s}{N} = \frac{20\,000\,\mathrm{S/s}}{40\,000\,\mathrm{S}} = 0.5\,\mathrm{Hz} \tag{9.1}$$

The harmonic content is measured both in the G2V and in V2G mode for the three AC currents.
To avoid repetition, only the current spectrum of the phase B has been plotted in the following figures. The other phases have similar behaviour

In Figure 9.9 is shown the harmonic content in G2V mode. To better visualize all the orders until the 33th, the fundamental value has been cut.
All the harmonics are under the limit shown in red in the plot. Intuitively, the high values of the limit stair correspond to the odd orders, while the low values correspond to the even orders, as depicted in table 9.4.
Only one order seems to be approaching the limit, it is the 23rd (1150 Hz) and it is zoomed in Figure 9.10 to guarantee is still below the limit.

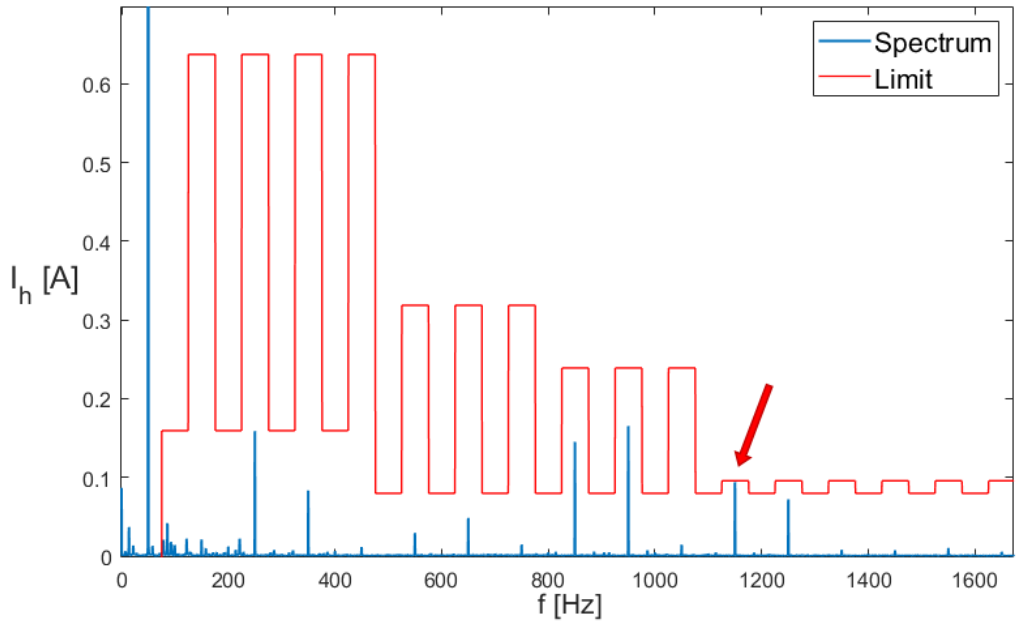

Figure 9.9: G2V harmonic content current I_B

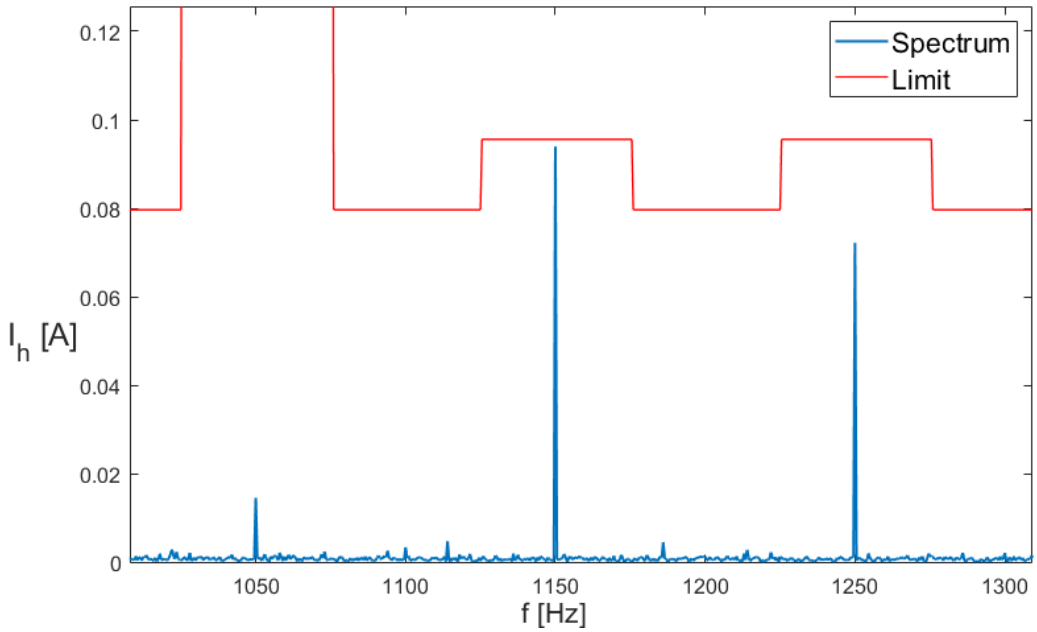

Figure 9.10: G2V harmonic content current I_B (zoom in)

The figures are repeated for the V2G mode in 9.11 and 9.12.
This time it can be stated that for the phase B, the 23rd order harmonic

exceeds the limit. This happens for phase A too.
It can be due eventually to measurement errors.
In table 9.6 are shown the values obtained for the 23rd harmonic and their exceeding percentage.
A possible future work consists in repeating the test increasing the number of samples, hence improving the frequency resolution (smaller frequency step).

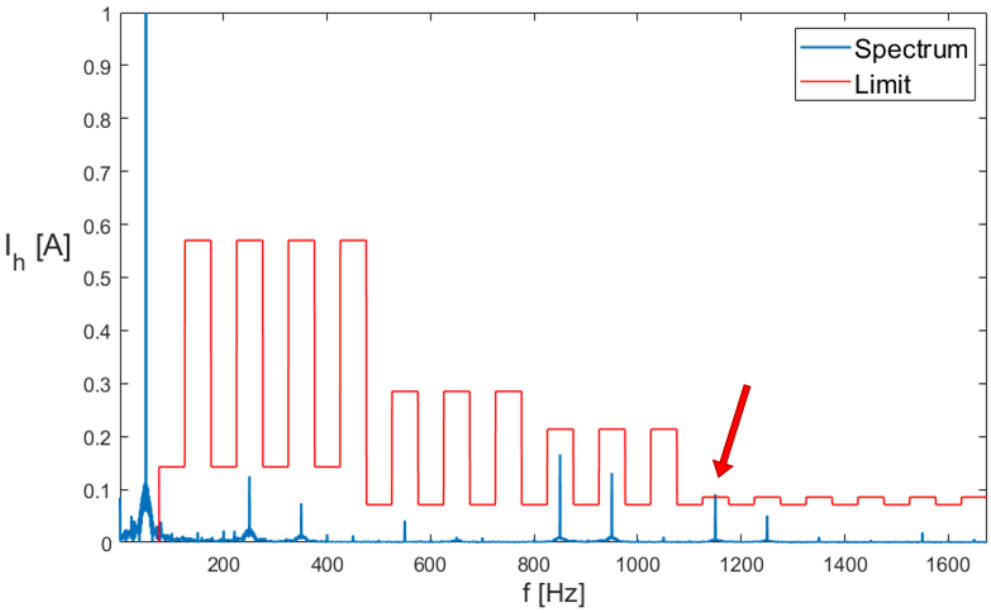

Figure 9.11: V2G harmonic content current I_B

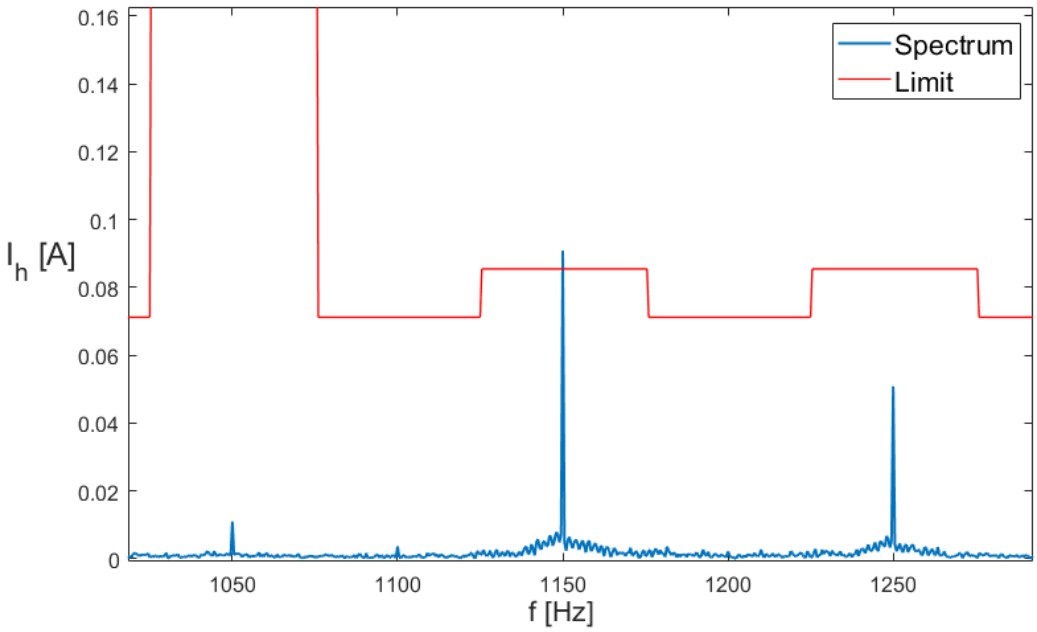

Figure 9.12: V2G harmonic content current I_B (zoom in)

Table 9.5: 23rd order harmonic - values for each phase

Phase	Limit [A]	Value [A]	Excess
A	0.0857	0.0892	4.13 %
B	0.0855	0.0909	6.29 %
C	0.0865	0.0834	-3.48 %

Table 9.6: 23rd order harmonic - values for each phase

Phase	Limit [A]	Value [A]	Excess
A	0.0857	0.0892	4.13 %
B	0.0855	0.0909	6.29 %
C	0.0865	0.0834	-3.48 %

In Figures 9.13 and 9.14 are shown again the G2V and V2G harmonic contents with the respective limits, but this time against the logarithmic scale. In this way is visible the whole spectrum, including the fundamental value.

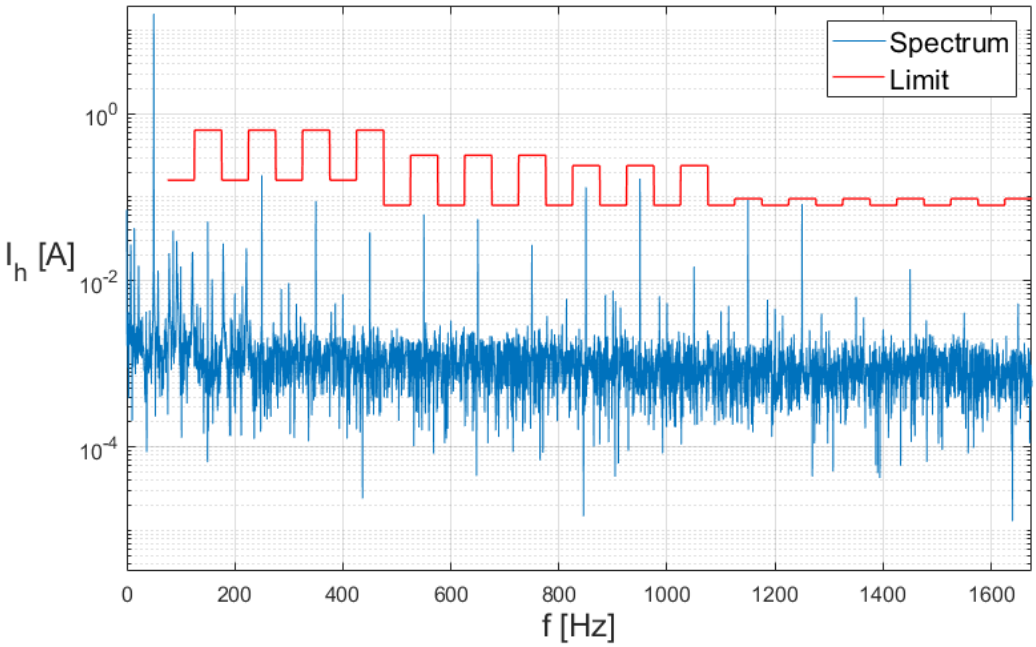

Figure 9.13: G2V harmonic content current I_B (logarithmic scale)

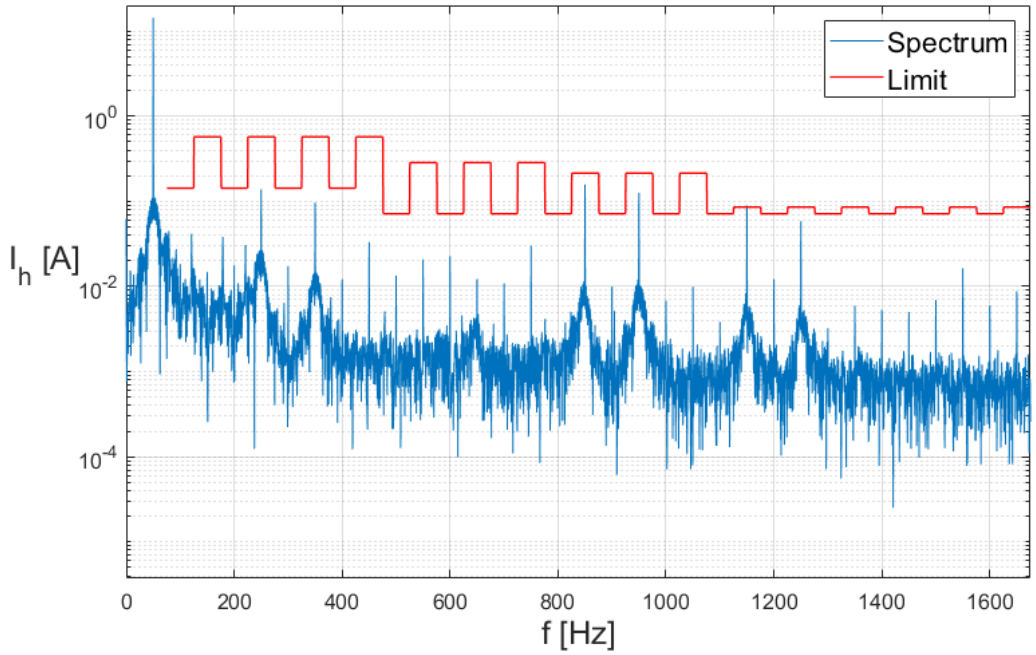

Figure 9.14: V2G harmonic content current I_B (logarithmic scale)

The THD is defined in eq. 9.2, but for our purposes is calculated as in eq.

9.3:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} \cdot 100 \tag{9.2}$$

$$THD = \frac{\sqrt{\sum_{h=2}^{33} I_h^2}}{I_1} \cdot 100 \tag{9.3}$$

All the harmonic values are listed in tables 9.7 and 9.8.
The harmonic orders exceeding the value are highlighted in red.
All the percentage values are referred to the fundamental value of the corresponding phase.

Order	**Ph. A [%]**	**Ph. B [%]**	**Ph. C [%]**	**Limit [%]**
2	0.092	0.088	0.114	1
3	0.320	0.132	0.278	4
4	0.044	0.076	0.086	1
5	1.150	0.997	1.205	4
6	0.058	0.018	0.086	1
7	0.561	0.523	0.535	4
8	0.043	0.040	0.043	1
9	0.235	0.072	0.158	4
10	0.017	0.017	0.006	0.5
11	0.389	0.185	0.295	2
12	0.021	0.009	0.016	0.5
13	0.340	0.305	0.427	2
14	0.006	0.020	0.025	0.5
15	0.168	0.093	0.145	2
16	0.014	0.030	0.036	0.5
17	0.823	0.911	0.876	1.5
18	0.047	0.006	0.043	0.5
19	1.048	1.037	1.187	1.5
20	0.034	0.029	0.047	0.5
21	0.092	0.091	0.086	1.5
22	0.027	0.021	0.030	0.5
23	0.581	0.590	0.565	0.6
24	0.029	0.008	0.032	0.5
25	0.517	0.453	0.556	0.6
26	0.016	0.013	0.019	0.5
27	0.040	0.051	0.018	0.6
28	0.016	0.015	0.019	0.5
29	0.086	0.047	0.037	0.6
30	0.008	0.006	0.011	0.5
31	0.026	0.064	0.078	0.6
32	0.003	0.008	0.014	0.5
33	0.033	0.035	0.029	0.6

Table 9.7: G2V Harmonic values

Order	**Ph. A [%]**	**Ph. B [%]**	**Ph. C [%]**	**Limit [%]**
2	0.128	0.126	0.075	1
3	0.103	0.139	0.029	4
4	0.124	0.156	0.180	1
5	0.966	0.876	0.994	4
6	0.122	0.018	0.113	1
7	0.679	0.516	0.540	4
8	0.085	0.107	0.133	1
9	0.233	0.093	0.195	4
10	0.094	0.035	0.064	0.5
11	0.145	0.291	0.209	2
12	0.159	0.037	0.137	0.5
13	0.086	0.073	0.161	2
14	0.076	0.067	0.074	0.5
15	0.211	0.014	0.179	2
16	0.010	0.043	0.056	0.5
17	1.103	1.165	1.118	1.5
18	0.070	0.023	0.082	0.5
19	0.883	0.919	0.995	1.5
20	0.048	0.038	0.038	0.5
21	0.069	0.077	0.121	1.5
22	0.027	0.026	0.027	0.5
23	0.625	0.638	0.579	0.6
24	0.085	0.015	0.091	0.5
25	0.410	0.357	0.425	0.6
26	0.023	0.012	0.022	0.5
27	0.042	0.074	0.018	0.6
28	0.037	0.023	0.015	0.5
29	0.035	0.030	0.023	0.6
30	0.048	0.005	0.044	0.5
31	0.114	0.135	0.143	0.6
32	0.042	0.027	0.051	0.5
33	0.062	0.046	0.061	0.6

Table 9.8: V2G Harmonic values

In table 9.9 are listed the THD values of each phase for both the operating conditions.
The THD compliance is respected as every value is below the 5% limit.

V2G		**G2V**	
THD_A	2.0559 %	THD_A	2.1240 %
THD_B	1.9963 %	THD_B	1.9802 %
THD_C	2.0828 %	THD_C	2.2336 %

Table 9.9: THD values

9.3 DC current injection

From the standard IEC 62909-1:2017 [3] for the bidirectional power converters (Section 4.4), the charging station shall not inject DC current greater than 1 % of the rated inverter output current, into the utility AC interface.

The test procedure is given in Section 5.9 of IEEE Std 1547.1-2020 [18], which specifies to set the device under test at 100% of the continuous rated current.
The wallbox is then supplied at the nominal voltage and it is tested under the rated power conditions.

For the V2G operation, the rated current of the wallbox is calculated as follows:

$$I_{V2G} = \frac{P_{V2G}}{sqrt(3) \cdot V_n} = \frac{10000}{sqrt(3) \cdot 400} = 14.4338\,\text{A} \tag{9.4}$$

For the G2V:

$$I_{G2V} = \frac{P_{G2V}}{sqrt(3) \cdot V_n} = \frac{11000}{sqrt(3) \cdot 400} = 15.8771\,\text{A} \tag{9.5}$$

The DC current is determined from the FTT performed in the previous section (Section 9.2) to obtain the harmonic content.
The DC current component corresponds to the 0 Hz component.

In Figure 9.15 are shown the harmonic contents of the three phase currents and the relative limit, which amount to 1% of the rated current.

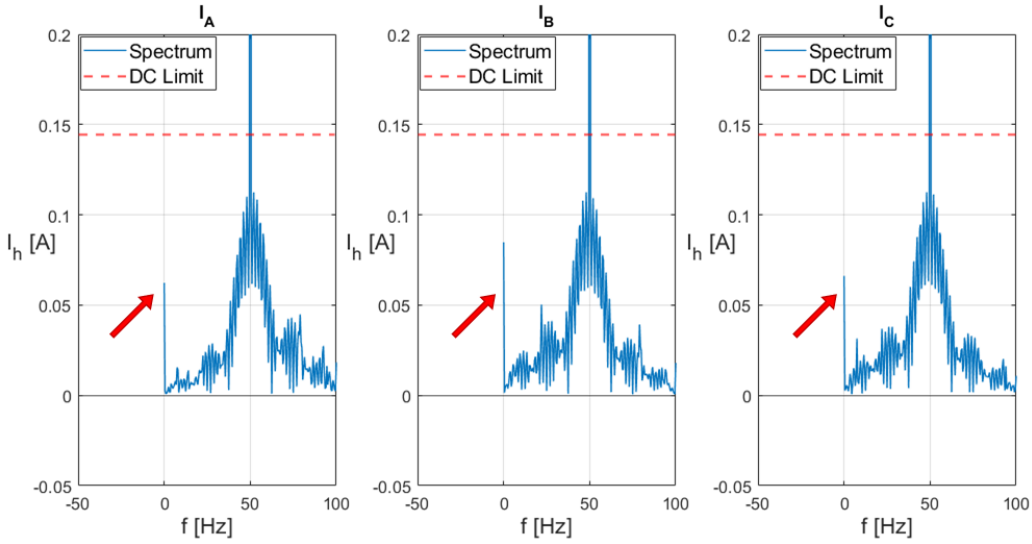

Figure 9.15: V2G harmonic spectrum (zoom in)

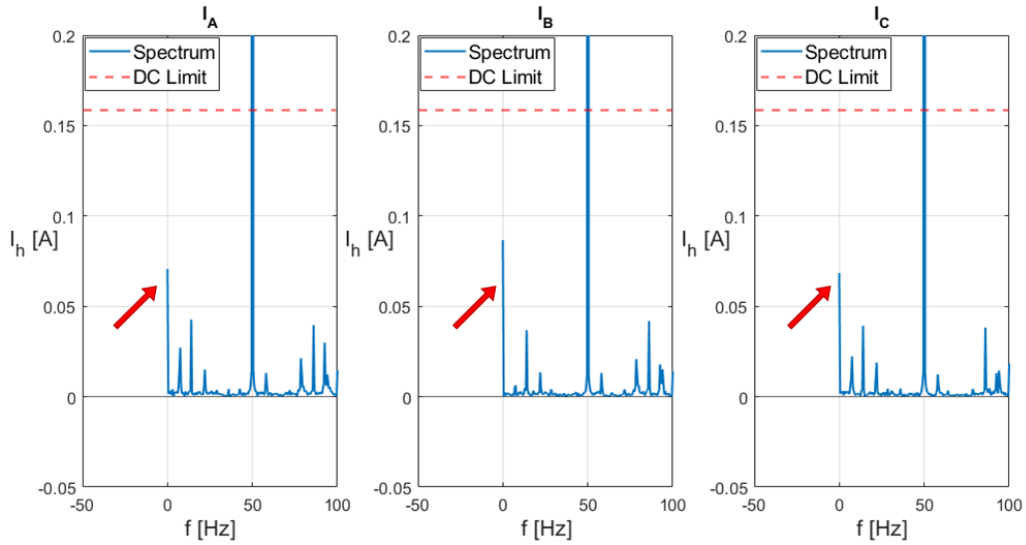

Figure 9.16: G2V harmonic spectrum (zoom in)

	Value [A]	$1\%I_{rated}$ **Limit [A]**	**% of the rated current**
V2G			
I_{DC_a}	0.0623	0.1443	0.4318
I_{DC_b}	0.0848	0.1443	0.5875
I_{DC_c}	0.0661	0.1443	0.4582
G2V			
I_{DC_a}	0.0707	0.1588	0.4454
I_{DC_b}	0.0867	0.1588	0.5460
I_{DC_c}	0.0685	0.1588	0.4312

Table 9.10: Overview on DC injection measurements

The zoomed in V2G harmonic content (Figure 9.15) shows a greater inter-harmonics presence in comparison to the G2V operation (Figure 9.16).

As visible in the previous figures and table, the DC component is way below the limit in all the phases and in both the operating modes.
This testifies the compliance with the standard for the DC injection.

9.4 Power Factor Measurement

As written in standard IEC 62909-1:2017 [3] (which in turn cites the standard CEI/IEC 61727-2004 [6]), the charging station shall provide a lagging power factor greater than 0.9 when the output is greater than 50 % of the rated inverter output power.
Such rated inverter output power is the V2G/discharging rated power which amounts to 10 kW.
The test is replicated for the G2V mode, where the rated power is 11 kW.
Also, the charging station is tested supplying three different voltages: the nominal value and both the maximum and the minimum allowable.

For the analysis are used the same data elaborated in section 9.6 for the wallbox conversion efficiency calculation.

In Figure 9.17 the power factors, obtained at the nominal voltage, are plotted against the power setpoints.
The overlapping lines represent the different SoC.
The only visible trend line is the increase of the power factor with the increase of the power.
There seems to have no relation between the wallbox efficiency and the battery SoC.

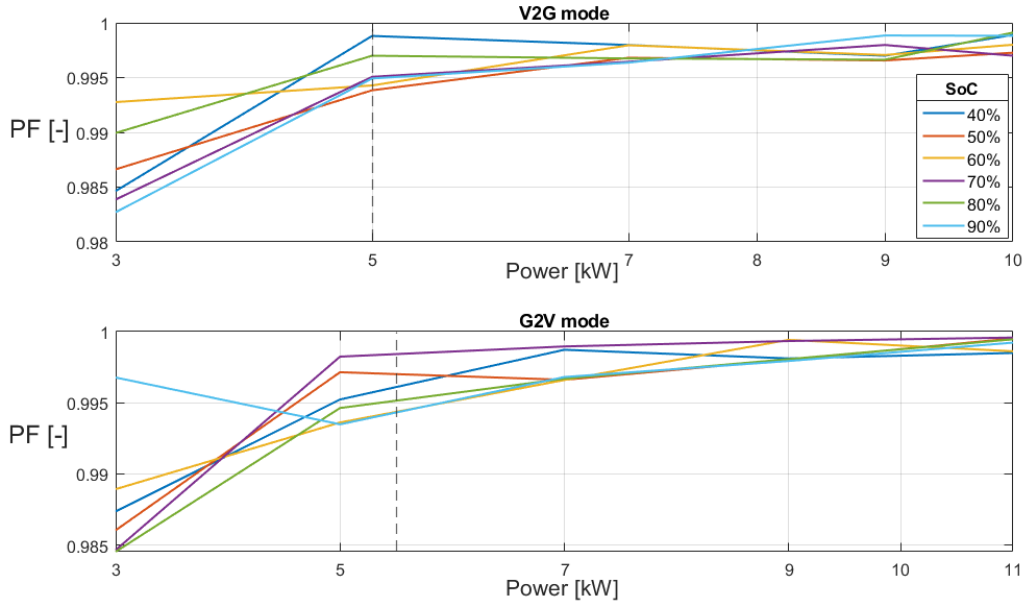

Figure 9.17: Power Factor - 230V

The plots for a supplying voltage different from the nominal value keep the same trend (Figure 9.18).

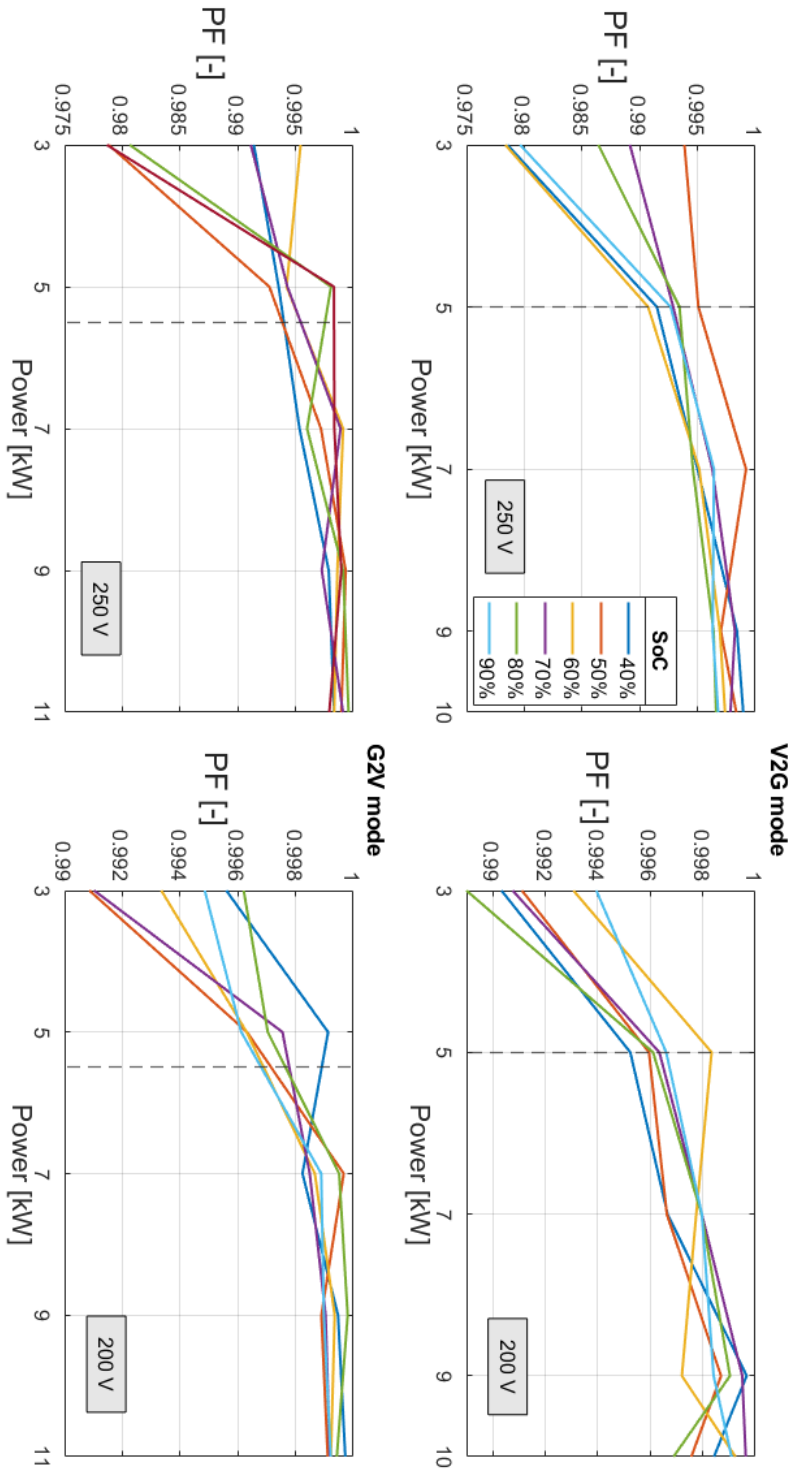

Figure 9.18: Power Factor - Power 200/250 V

In the figures are plotted, with a vertical black dashed line, the 50% nominal power threshold cited in the standard. This is done to highlight the observation area at the right of the threshold
As the rated power are 11 kW for the G2V operation and 10 kW for the V2G operation, the thresholds are respectively set to 5.5 kW and 5 kW,

It can be immediately noticed that in each graph the power factor is way above the 0.9 limit, even for power values lower than the 50% threshold.
As a matter of fact, the lowest recorded value in the observation area is 0.990728 .
The value was obtained during a 5 kW discharge, with the 250 V supply, at the 60% SoC.
The power factor test is successfully passed.

Both the previous figures have few sampling points and between them a linear interpolation was performed.
This is the reason why the lines appear jagged, but for our purposes is sufficient to analyze the trend line and to make overall observation. Thus a dense sampling was not necessary.
The reasoning is applied to the all following figures whose curves do not seem continuous.

9.5 Continuous Output Power Evaluation

The Continuous Output Power test belongs to the V2G Performance Test suggested by NREL [10].
Purpose of the test is to establish the continuous output level (V2G - discharging process) that the charging station can maintain. To obtain the continuous output level, in such scenario, it is necessary to make the wallbox work at the rated V2G power, which is 10 kW.
The test is performed without temperature control and must be repeated for the three voltages: nominal voltage (400 V phase-to-phase), minimum allowable voltage(340 V), maximum allowable voltage (440 V).

First step is to verify that the battery SoC is above 98%.
Otherwise it is necessary to charge the EV in order to reach such value.
Then a discharging process occurring at the nominal power is performed.

The test ends when one of the following cases occurs:

- *Foldback*: Output power curtailment by vehicle controls to protect the wallbox itself;
- *Shutdown*: The inverter inside the wallbox turns itself off to protect the charging station;
- *Low SoC*: Minimum SoC value is reached, in our case it is 35% level.

The AC power was measured almost every 5 minutes when the nominal voltage is applied, every 10 seconds when the WB was supplied at maximum and minimum voltage.
This is due to the fact that the tests at the limit voltages (340 V and 400 V) last a very short time in comparison to the normal voltage test.
In fact, if the test at nominal voltage takes the whole discharging process (nearly 3 hours) to be completed, supplying at limit voltages for a long time is demanding for the wallbox. The device was not supposed to work continuously at rated power with the limit voltages.
For this reason, at minimum and maximum voltages the test ends when the wallbox shuts itself down.
In table 9.11 are listed the results of the continuous output power test.
For *Continuous output power* is intended the minimum value recorded during the discharge at a given voltage.
The time of each test is reported as well.

Voltage (phase-to-phase)	Continuous Output Power	Test time	Ending
340 V	9665.90 W	6 min 38 sec	Shutdown
400 V	9884.52 W	194 min 12 sec	Low SoC
440 V	9903.12 W	7 min 46 sec	Shutdown

Table 9.11: Continuous Output Power test results

The continuous output power is defined as the minimum AC active power recorded.
It is obtained a value for each test.
As 10 kW is the rated V2G power, it is logical to obtain continuos output power levels smaller than 10 kW .

9.6 Wallbox Conversion Efficiency

The procedure for this test is suggested by the NREL (National Renewable Energy Laboratory) [10].
The purpose is the calculation of the charging station efficiency in different operating conditions.
As it is a performance test, there are no specific pass/fail criteria.

The operating conditions differ according to whether the vehicle is charging or discharging and according to various parameters:
- AC side voltage value;
- SoC;
- power setpoint.

The efficiency is calculated for every discrete variation of these three parameters.
For a given voltage value, at a certain SoC, a power setpoint is imposed to charge the vehicle.
Different setpoints are set. Then the SoC is changed and the same power setpoints are imposed again.
Finally, the voltage value is modified and the efficiency is calculated again with the same values of SoC and power.
All these calculations are replicated in the discharge mode.

The wallbox is supplied with the three voltage values specified in Table 8.1.
As already explained in chapter 8, the WB has a continuous range of 85%-110% of the rated voltage value (400 V phase-to-phase).
For the test, through the are imposed the corresponding phase-to-neutral voltages: 200 V, 230 V, 250 V.

The WB configuration has a 3 kW threeshold as minimum charging and discharging power.
Hence the power setpoint values, covering the whole power range, are set to 3-5-7-9-11 kW for the charge and 3-5-7-9-10 for the discharge (as 10kW is the maximum discharging rate).
To avoid data overload, a power step of 2 kW was chosen.
The test is performed without the ambient temperature control.

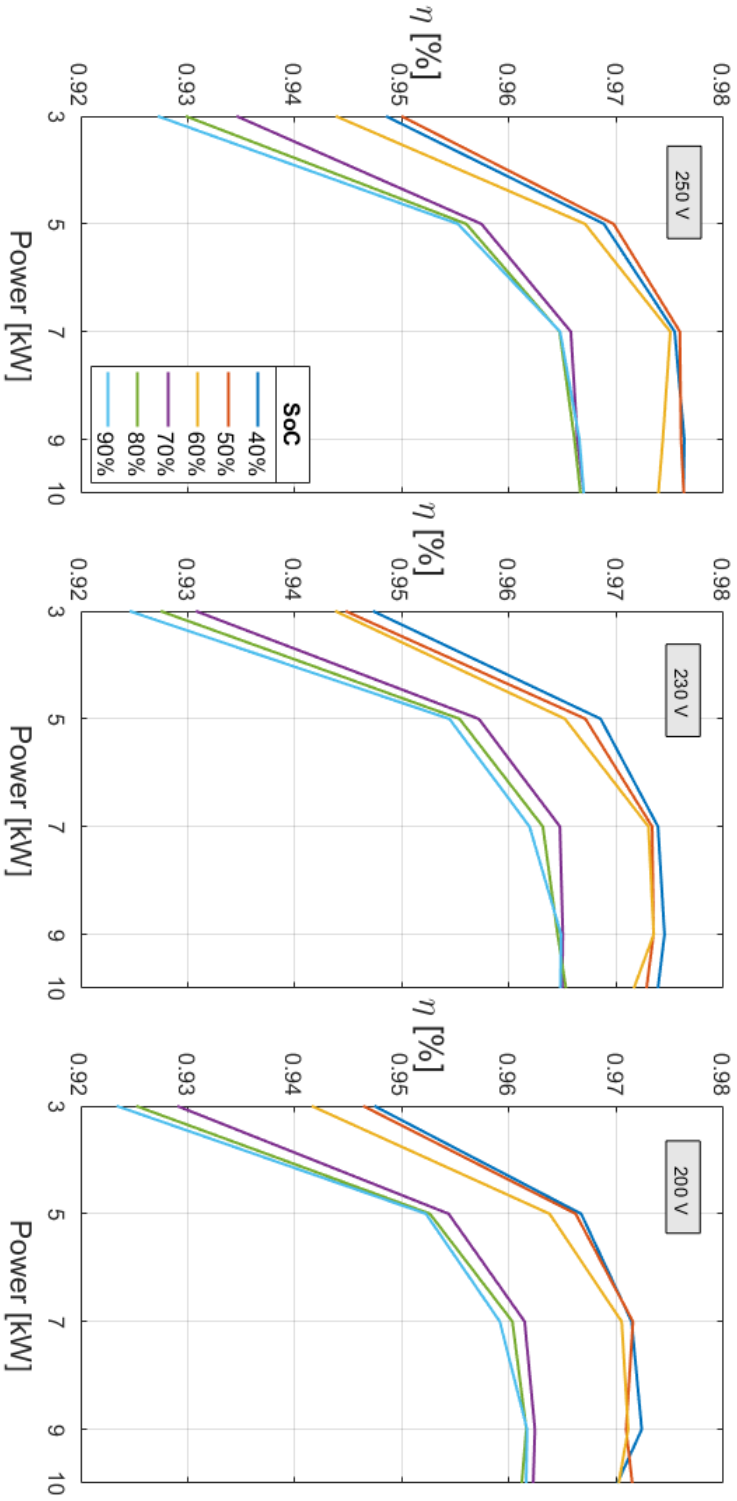

Figure 9.19: η-power (different SoC) V2G

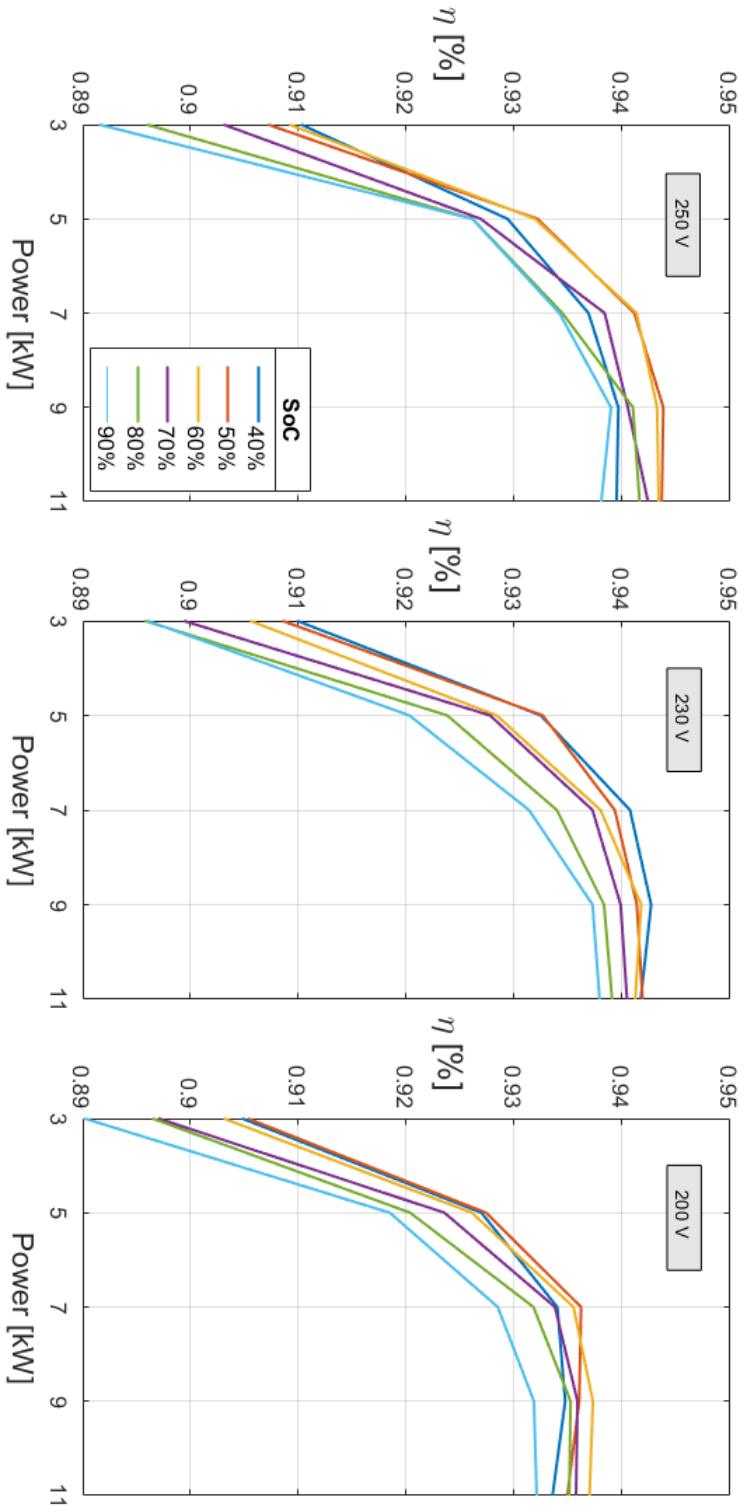

Figure 9.20: η-power (different SoC) G2V

Figure 9.19 and Figure 9.20 show respectively how the efficiency changes according to the discharging power and to the charging power.
For each figure three subplots are present because of three different voltages (maximum voltage, nominal voltage, minimum voltage).
In the same subplot are shown the different SoC analysed.

In both V2G and G2V figures it is easily recognisable the trend line: efficiency increases if the power increases too.
The dependency is not linear though, an higher slope is obtained at low power values, similarly to what happened in the power factor measurement (Section 9.4, Figure 9.17).
It seems that the charging station is optimized to work in a range in proximity of the rated power value. If the power value goes away from this range, the efficiency drops [31].

The second visible trend is that a better efficiency is obtained for lower SoC.
An explaination of this phenomena could be given by the voltage difference: the AC side of the wallbox has a constant voltage value determined by the PA, while the DC side voltage corresponds to the voltage across the EV battery.
Low SoCs are related to low voltage. It could make sense, from an energetic point of view, to assert that the charging station works in better conditions if the difference between the AC side voltage and DC side voltage is higher.

Another point of analysis is that the efficiency is higher if the voltage is higher. Hence, the wallbox is more efficient if supplied at 250 V respect to when supplied at nominal voltage (230 V).
This could be due to the fact that, to absorb (or supply) a fixed amount of power, if the voltage value increases, the current decreases its value. Consequently, less losses occur inside the charging station.

Only for V2G graphs (Figure 9.19 an observance is made: the efficiency shows a massive step of about 1% value between 60% and 70% of SoC.

The graphs showed in Figures 9.19 and 9.20 can be offered again from another point of view.
As a matter of fact, in Figures 9.21 (V2G up, G2V down) the efficiency is plotted respect to the SoC.
In the graph multiple lines are present, which represent the set power values. Values are referred to the nominal voltage.
For these two graphs the same consideration made for the previous eta-P

plots can be made.

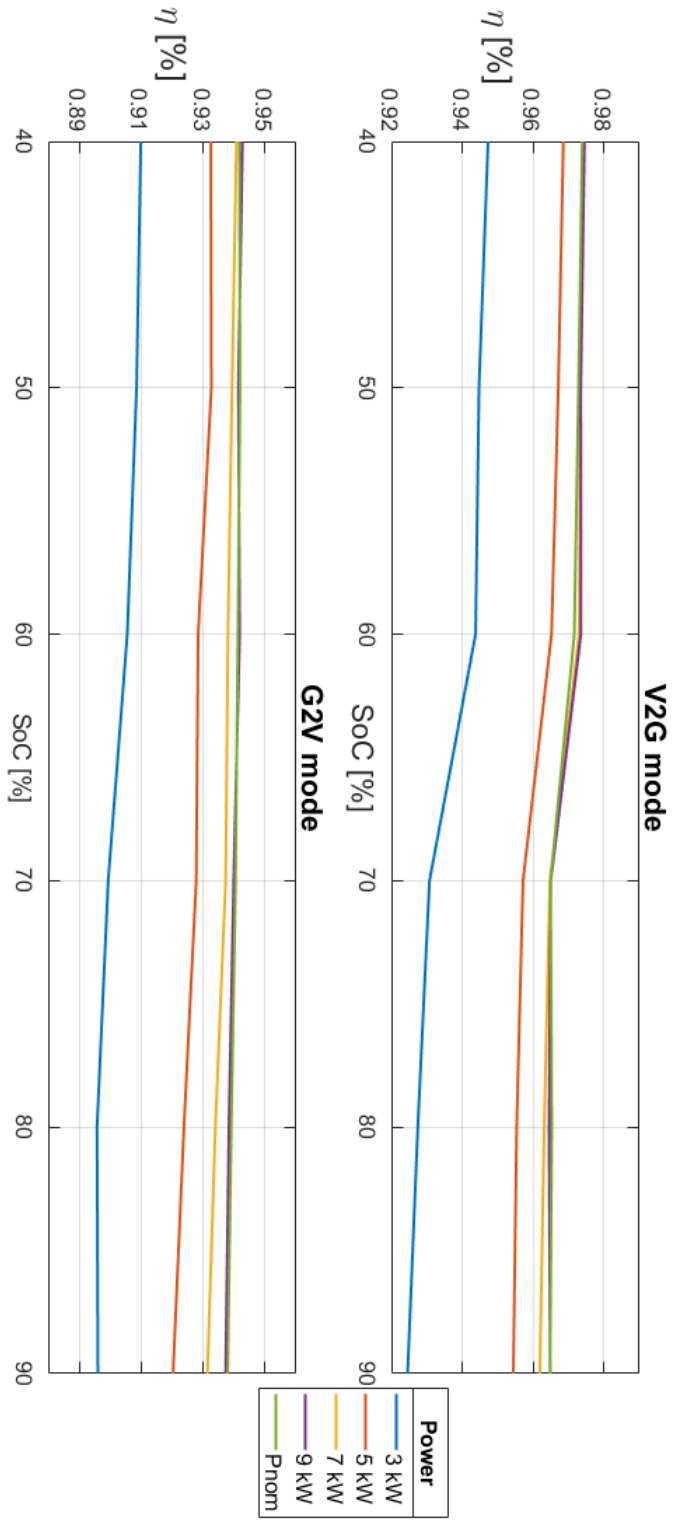

Figure 9.21: η - SoC at different voltages. V2G (above) and G2V (below).

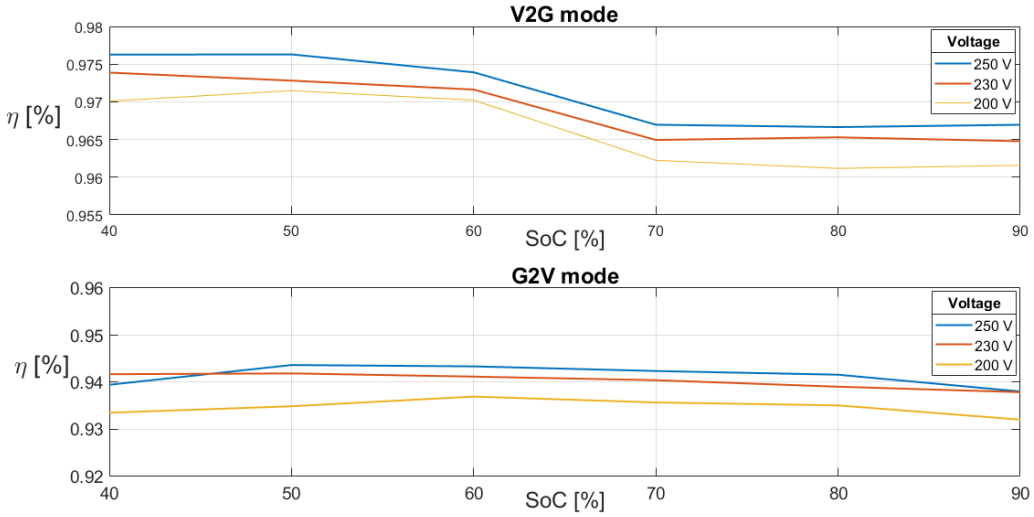

Figure 9.22: η - SoC (different Power)

In Figure 9.22 the efficiency is still plotted against the SoC but here the three lines represent the three supply voltages.
To avoid redundance, only the plots regarding the nominal power values are shown.
The observations about the conversion efficiency behavior are repeated.

The previous analysis can be summoned in a single graph.
A surface is plotted in a 3-D environment, where the x-axis represents the SoC, the y-axis represents the power and the z-axis is for the efficiency.
The surface is built for both V2G and G2V cases.
The colorbar next to each subplot helps to comprehend the dependency of the charging station efficiency with the battery SoC and with the power setpoint.

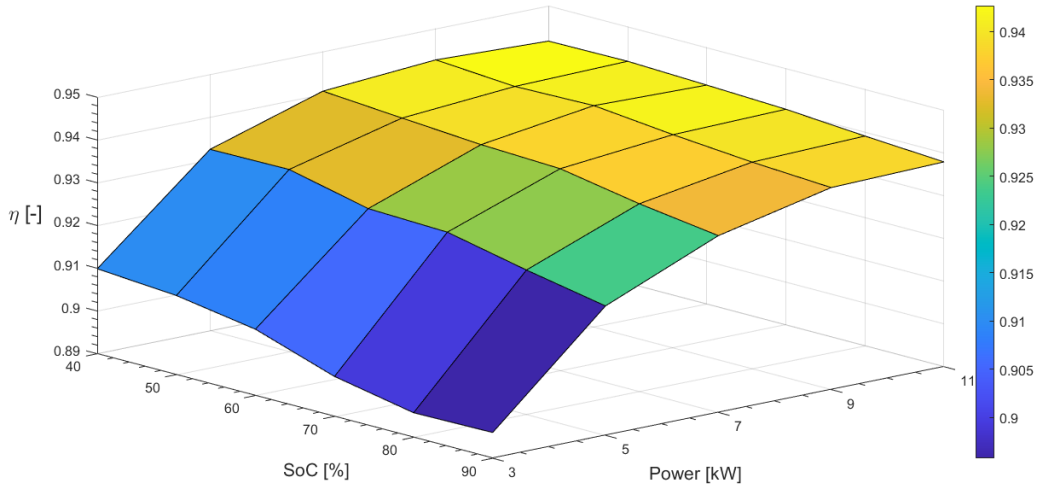

Figure 9.23: G2V efficiency colormap

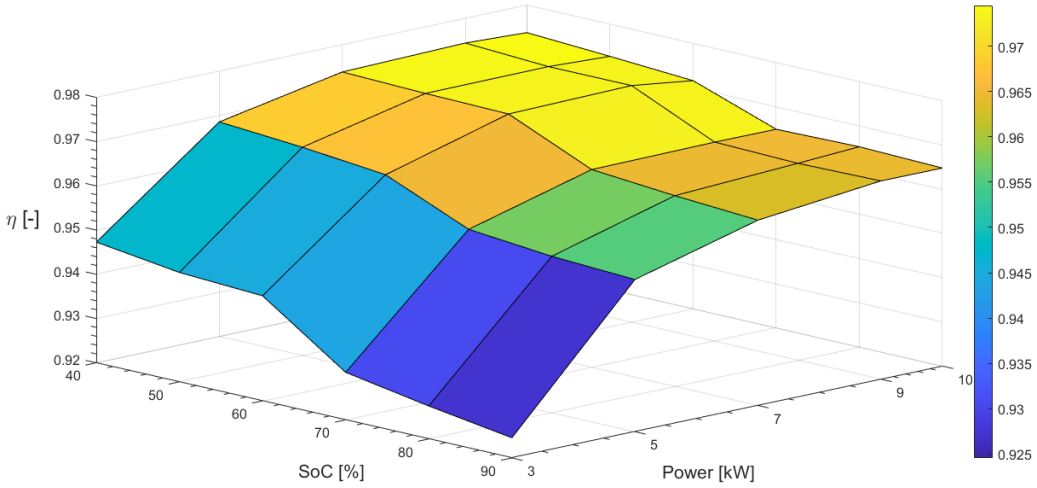

Figure 9.24: V2G efficiency colormap

Finally, among the results, the maximum value obtained (at nominal voltage) is stated as *Peak Efficiency*. The value is 0,9745, recorded at 40% SoC and 9 kW in V2G mode, and its position is easily identifiable in Figure 9.24. Another definition that could be given is the *Nominal Power Average efficiency*, stated as the average of the twelve efficiency values calculated when the wallbox was charging and discharging at the rated power and rated voltage.
Charging Average and *Discharging Average* comprehend all the samples at the different power, SoC and voltage.

These values, together with other more are listed in Table 9.12.

A last observation is made regarding the efficiency difference between V2G and G2V operation. This is visible in the average values *Nominal V2G Power Average* and *Nominal G2V Power Average* which consider only six values each, taken at nominal voltage.
The wallbox is more efficient converting the DC power to AC power. As a matter of fact, all the discharging efficiencies are higher than the charging counterparts.
A possible explanation could be found in the intrinsic operation of the AC/DC converter. It is thought that the power electronics components inside the charging station could perform better in inverter mode, rather than in rectifier operation.

Efficiency	**Value**	**Power [kW]**	**SoC [%]**	**Voltage [V]**
Peak Efficiency	0.9745	9 (V2G)	40	230
Nominal Power Average	0,9546	-	-	230
Nominal G2V Power Avg	0,9404	-	-	230
Nominal V2G Power Avg	0,9689	-	-	230
Charging Average	0.9284	-	-	
Discharging Average	0.9608	-	-	
Charging Peak	0,9438	9	50	250
Discharging Peak	0,9763	9	40	250
Lowest Charging	0,8902	3	90	200
Lowest Discharging	0,9234	3	90	200

Table 9.12: Relevant conversion efficiency values

A total of 180 operating points are analyzed (2 modes, 3 voltages, 6 SoC levels, 5 power setpoints).
Particular attention was paid to this test as the conversion efficiency becomes a relevant factor for an in-deep economic analisys.

9.7 Charging and Discharging Time Evaluation

9.7.1 Charging Time

This test too is provided by NREL guideline [10].
It aims to measure the time required to fully charge a V2G vehicle from a specified starting state-of-charge with the nominal power. The guideline suggests to repeat the test starting from different SoC: minimal allowable, 30%, 45%, 60%, 75%, 90%.
For our specific case, the test is performed with only one starting SoC: the minimal allowable SoC, which corresponds to 35%.
About the "fully charge" definition, the guideline precisely asks to reach the 100% level of SoC. Our charging station performs a gradual derating right above the 90%, then the charging power definitively drops to zero at 98%. Hence, is not possible to reach the 100% and therefore the test is ended at 98% of SoC.
Usually, when the battery reaches this capacity, two events could happen: the wallbox does not supply anymore the vehicle (hence supplying a power of 0 kW) or the wallbox shut itself down.
In this test, the wallbox remained turned on providing no power.

DC Current [A]	DC Voltage [V]	DC Power [W]	SoC [%]	Time
29,3	351,5	10298,95	35	09:49
29,1	354	10301,4	40	09:59
29	355,5	10309,5	42	10:09
38,8	357,5	13871	46	10:19
28,6	359,5	10281,7	49	10:29
28,5	362,5	10331,25	52	10:39
28,2	365	10293	55	10:49
28	367,5	10290	59	10:59
27,8	370	10286	62	11:09
27,6	373	10294,8	65	11:19
27,4	375,5	10288,7	68	11:29
27,2	378	10281,6	71	11:39
27	381	10287	74	11:49
26,7	384	10252,8	77	11:59
26,5	386,5	10242,25	80	12:09
26,4	389,5	10282,8	83	12:19
26,1	392,5	10244,25	86	12:29
25,9	395,5	10243,45	89	12:39
25,7	399	10254,3	92	12:49
21,5	401,5	8632,25	95	12:59
9,6	402	3859,2	96	13:09
4,6	402	1849,2	97	13:19
7,5	402	3015	97	13:29
-	402	-	98	13:33
				3h 44min

Figure 9.25: Charging time evaluation table

In Figure 9.25 the row highlighted shows the first sample in which the derating was visible.
It took nearly 3 hours and 44 minutes to fully charge the EV battery from the lowest available SoC to the fullest.

9.7.2 Discharging Time

The Discharging time evaluation test is the analogous of the previous one, but for the discharging process.

DC Current [A]	DC Voltage [V]	DC Power [W]	SoC [%]	Time
-26,4	400	-10560	98	13:45
-26,7	396	-10573,2	97	13:55
-27	392,5	-10597,5	94	14:05
-27,2	389	-10580,8	91	14:15
-27,4	385,5	-10562,7	88	14:25
-27,6	382,5	-10557	85	14:35
-27,9	379,5	-10588,05	82	14:45
-28	376,5	-10542	79	14:55
-28,3	373,5	-10570,05	76	15:05
-28,5	370,5	-10559,25	72	15:15
-28,8	367,5	-10584	69	15:25
-29	364,5	-10570,5	66	15:35
-29,2	361,5	-10555,8	62	15:45
-29,4	358,5	-10539,9	59	15:55
-29,7	356	-10573,2	56	16:05
-29,8	353,5	-10534,3	52	16:15
-30	351,5	-10545	49	16:25
-30,1	350	-10535	45	16:35
-30,3	348,5	-10559,55	41	16:45
-30,4	347	-10548,8	37	16:55
-	346.5	-	35	17:00
				3h 10min

Figure 9.26: Discharging time evaluation table

In comparison with the charging time evaluation, the discharging process took less time: almost 3 hours and 10 minutes. It means nearly the 15% less.

9.8 Roundtrip Efficiency

The test procedure is provided by the standard IEC 62933-2-1:2017 [5].
The roundtrip efficiency is given for an energy storage system. It is defined as the ratio between the total output energy divided by the total input energy over one charging/discharging cycle using the rated input and output power. In our case, the EV battery and the V2G charging station are the devices to be tested. Hence the input power is referred as charging power (G2V), while the output power is responsible for the discharge (V2G).

The test is executed starting a charging process from the minimum available energy level, which in our case, is represented by a SoC of 35%.
Then the full available energy level is reached. Teorically it should be SoC=100%, but when the SoC is right above 90% a derating process occurs. Sometimes, when the SoC level exceedes 95%, the charging power value intermittently drops to zero, and finally it stays to zero approaching the 98% level.
When this happen, the charging process is considered terminated. Hence, the SoC does not reach the 100%.
The discharging process at 10 kW is imposed as soon as the charging process ends. This is done to avoid self-consumption for a long period, that could falsify the test decreasing the overall efficiency.
The test is terminated when the SoC drops to the initial value of 35%.

The roundtrip efficiency is supposed to be performed at the standard test conditions which are [5] :
- ambient temperature < 25°C ;
- altitude < 1000 m;
- humidity < 95 %.
In our case the test was performed at a temperature of almost 29°C.

The standard IEC 62933-2-1:2017 [5] suggests to repeat the test twice using the rated power values, then to calculate the average of the two roundtrip efficiency values.
For time reasons, the test is performed just once instead.
The AC and DC energies for both the charge and the discharge are measured.
Through the following scheme (Figure 9.27) can be visualized the energy flows and to what are referred the energy values measured.

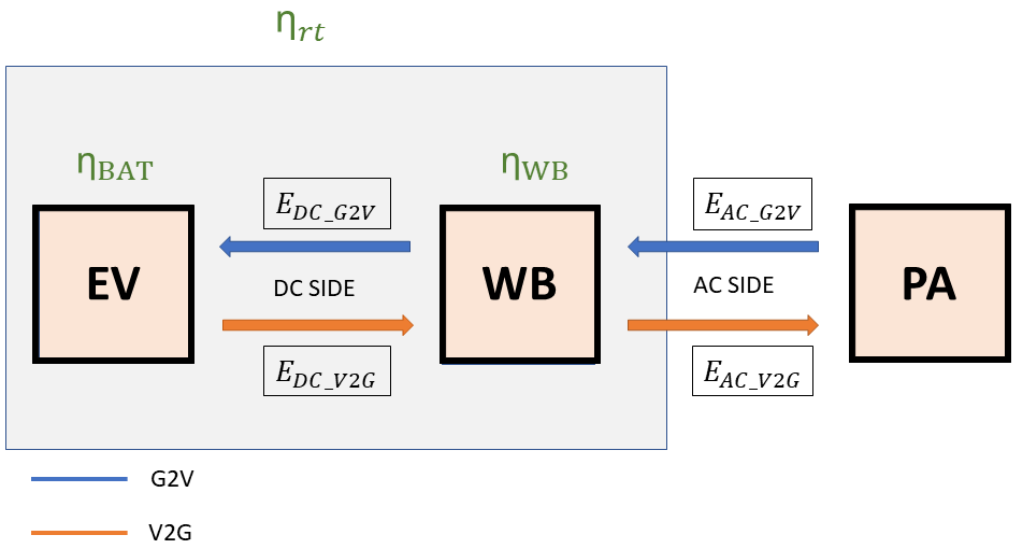

Figure 9.27: Energy flows

The *overall* or *AC roundtrip efficiency* is defined as [5]:

$$\eta_{rt} = \frac{E_{AC\_V2G}}{E_{AC\_G2V}} \tag{9.6}$$

where E_{AC_V2G} and E_{AC_G2V} are respectively the total output (V2G) energy and total input (G2V) energy measured at the AC side of the wallbox.
The calculation includes the conversion losses inside the charging station and the battery losses.

To obtain just the *battery* or *DC roundtrip efficiency*, the energies are measured on the DC side:

$$\eta_{rt\_BAT} = \frac{E_{DC\_V2G}}{E_{DC\_G2V}} \tag{9.7}$$

Indeed E_{DC_V2G} and E_{DC_G2V} are respectively the total output (V2G) energy and total input (G2V) energy measured at the DC side of the wallbox.

As can be understood from Figure 9.27, the overall roundtrip efficiency contains both the roundtrip efficiencies of the charging station and of the battery. If the battery roundtrip efficiency is obtained from eq.9.7, the wallbox roundtrip efficiency can be calculated:

$$\eta_{rt} = \eta_{rt\_WB} \cdot \eta_{rt\_BAT} \tag{9.8}$$

$$\eta_{rt\_WB} = \frac{\eta_{rt}}{\eta_{rt\_BAT}} \tag{9.9}$$

$$\eta_{rt\_WB} = \frac{E_{AC\_V2G}}{E_{AC\_G2V}} \cdot \frac{E_{DC\_G2V}}{E_{DC\_V2G}} \tag{9.10}$$

For completeness, the wallbox roundtrip efficiency has been splitted in the two components: wallbox G2V energy efficiency η_{G2V_WB} and wallbox V2G energy efficiency η_{V2G_WB}.
Equations follow:

$$\eta_{G2V\_WB} = \frac{E_{AC\_G2V}}{E_{DC\_G2V}} \tag{9.11}$$

$$\eta_{V2G\_WB} = \frac{E_{DC\_V2G}}{E_{AC\_V2G}} \tag{9.12}$$

Indeed:

$$\eta_{rt\_WB} = \eta_{G2V\_WB} \cdot \eta_{V2G\_WB} = \frac{E_{AC\_G2V}}{E_{DC\_G2V}} \cdot \frac{E_{DC\_V2G}}{E_{AC\_V2G}} \tag{9.13}$$

In the following table, the roundtrip efficiency values are finally listed:

Overall roundtrip efficiency	η_{rt}	86.62%
Wallbox roundtrip efficiency	η_{rt_BAT}	89.02%
Battery roundtrip efficiency	η_{rt_WB}	97.30%
Wallbox G2V efficiency	η_{G2V_WB}	93.63%
Wallbox V2G efficiency	η_{V2G_WB}	95.08%
AC output energy	E_{AC_V2G}	31.7485 kWh
AC input energy	E_{AC_G2V}	36.6527 kWh
DC output energy	E_{DC_V2G}	33.3903 kWh
DC input energy	E_{DC_G2V}	34.3174 kWh

Table 9.13: Roundtrip energies and efficiency values

Although the EV battery has a nominal energy capacity of 62 kWh, from table 9.13 is notable how the energy absorbed by the battery during the charging process is way less (34.32 kWh).
The difference is explained looking to the SoC used as limits of the charging part of the roundtrip. Indeed the charging process started at 35% and not from 0%, finishing at around 98%.
To be more precise, as explained in chapter 8 these values are referred to the SoC display which is a more conservative parameter respect to the real SoC. Thus the the charging process actually started at about 42-43% and concluded at around 95-97 %. This is the reason why the energy stored is about half of the declared battery energy capacity.

In Figure 9.28 a pie chart shows the energy losses, which are in turn shown in Table 9.14 .
The whole pie corresponds to the AC energy supplied to the wallbox in the charging process (E_{AC_G2V}).
Then are visible the losses on the wallbox due to the two processes (blue: ΔE_{WB_G2V} and orange: ΔE_{WB_V2G}). Other losses are due to the battery (grey: ΔE_{BAT}).
Finally, the last piece represents the energy fed back from the EV during the V2G mode (E_{AC_V2G})

G2V WB losses	ΔE_{WB_G2V}	E_{AC_G2V} - E_{DC_G2V}	2.3353 kWh	6%
V2G WB losses	ΔE_{WB_V2G}	E_{DC_V2G} - E_{AC_V2G}	1.6418 kWh	4%
Battery losses	ΔE_{BAT}	E_{DC_G2V} - E_{DC_V2G}	0.9271 kWh	3%

Table 9.14: Energy losses

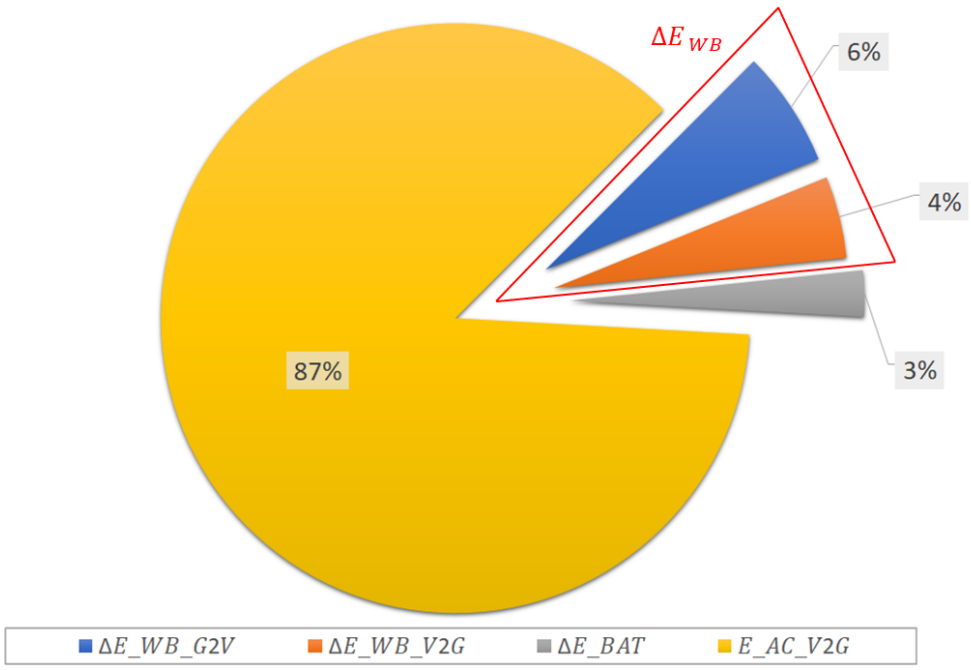

Figure 9.28: Energy losses percentages

It must be taken into account that, during the whole roundtrip test, some energy is sucked up from the battery by the EV auxiliary subsystems (battery diagnostic device, dashboard, communication electronics, etc..). These

losses are included in the battery energy losses.
Even if the battery rountrip efficiency is nearly the 97.30% (Table 9.13), the value could be higher without these continuous losses.

Chapter 10

Conclusion

We had set ourselves the goal of starting the experimental phase of the project. As a matter of fact, the laboratory in the Energy Center has been set up and the first preliminary tests on the wallbox have been performed.

The laboratory setup to test the V2G charging station was successfully implemented starting from the scratch.
Each device involved was individually tuned for the purpose of testing the WB with the Power-Hardware-In-The-Loop methodology.
The physical and virtual connection between all the instruments did not create any issue in particular, except for an obstacle found while closing the loop. In fact, particular attention must be paid when modeling the interface algorithm in order to avoid instability issues as we encountered.
As a matter of fact, since the PHIL is an innovative methodology, more efforts in the research literature could be done to standardize the modeling for closing the loop when electrical systems are simulated.
Our definitive method used for closing the loop has been developed after many trials in which instability problems kept to take place.
The method used is the currents reconstruction. It could be a valid proposal for the modeling standardization above mentioned, apart from the fact that, when the waveforms are reconstructed, only the fundamental is taken into account to generate the new reconstructed sinewave. Thus the disturbances present in the real world are neglected. An higher fidelity method could be found.

Overall, all the high performance instruments look to be valid for every complex scenario that could emulate the wallbox interaction with the electrical grid.

From the point of view of the simulated network, the computational effort of the RTS to run the electrical grid model has been heavily reduced in comparison to the starting grid model.
Plenty of free room on each core is still available for further additions inside the model.

The results of the characterization tests performed on the V2G charging station show some critical points.
In the first place, the communication between user and charging station is made possible by a server controlled by the company which is responsible of the wallbox firmware.
This intermediate step does not allow an immediate response from the charging station to the requests made by the user, either via APP or API.
The communication delay represents a red flag in perspective of the definitive use of the charging station. In order to participate in the ancillary services market or in the balancing market, the V2G charging station must comply with the response time requirements imposed by the transmission system operator.
For instance, to participate in the Fast Reserve service, the V2G system should eventually comply to the request within one second. At the moment, the wallbox is not capable of this service, as its delay most of the times are above 30 seconds.
In the following tests to be executed for the continuation of the project, the response time of the wallbox will be deeply analyzed and tested in order to verify this compliance.
The communication issues testifies how innovative this technology is, but in the future a bigger effort is expected by the firmware developer to adjust the wallbox configuration and make it suitable for V2G market operations.

Confirming what has been said so far, as soon as the V2G charging station was installed into the lab a problem occurred. Due to a software bug, all the requests from the server were ignored by the wallbox. Because of the problem, the charging station has been out of use for almost a month. The event highlights that this kind of devices are still a kind of prototypes and undoubtedly other similar hurdles could show up again during the project.

From a technical point of view, the grid interconnection tests and the V2G performance tests highlighted the excellent performance of the V2G charging station.
Every requirement from the standards was successfully fulfilled, apart from a doubtful behavior in the current harmonics test: the overall harmonic con-

tent is way below the limit, but just the 23rd harmonic is a little over the cap (excess of 4-5 %). This could be due to some random condition and to the resolution of the FFT method. Even if the overall harmonic behavior would be accepted by the standard, it is suggested to repeat the test under different conditions.
Regarding the disturbances, the DC current injection is almost negligible. A good tolerance to the extreme voltages (85% and 110% of the nominal voltage) is also shown during the tests.
The power factor value, measured under every condition, is way above the minimum limit of 0.9. Actually, in the worse condition it had the outstanding value of 0.98.
The same happens for the conversion efficiency. Great values are obtained in both V2G and G2V operation. In the majority of operating conditions, the efficiency is higher the 90%. The optimal condition seems to be the rated power discharge (V2G) at low SoC.
To be more detailed, an efficiency map was drawn (for both V2G and G2V). Important considerations can be made on the efficiency map for future economic evaluation. Indeed, the choice of the right ancillary service will depend on factors such this.
Finally, few words on the roundtrip efficiency are spent: almost the 90% of wallbox efficiency has been obtained during a complete cycle of charge-discharge.

Another possible future work consists in performing new tests and repeating the ones we made when the wallbox is placed in another location outside the EC-Lab. In fact, the charging station is supposed to be located in the company parking lot. Here it can start the real V2G operation with the electrical grid, replying to the simulated TSO requests.

To recap, the laboratory setup was developed starting from zero.
The Power-Hardware-In-The-Loop setting is ready for the following steps of the project, which involve the use of the charging station as DUT inside in the simulation.
The Simulink model is expected to be modified according to the business scenarios which will be chosen to verify the profitability of the V2G charging station employment.
Additionally, more tests to verify the grid interconnection compliance must be performed.

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