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Analysis of MMIC GaN technology oriented to Doherty Power Amplifier design

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Introduction

The radiofrequency transmitter is one of the most important building block of the entire wireless communication infrastructure, responsible of modulation, upconversion and power amplification while interfacing with the antenna. It poses many challenges to the designer. Many applications such as wireless communication, navigation and broadcasting rely on its performance.

The Power Amplifier is one of the most critical elements of the transmitter and typically the most power consuming block of the RF transceivers. The main purpose of the PA is to deliver an output signal of the transmitter chain with a significant power level without distortion. From an energy standpoint, it converts DC power from the power supply into RF power to the load with a given efficiency[3].

Originally the Doherty Power Amplifier (DPA) was introduced as a new form of linear power amplifier that would reduce the power consumption and increase noticeably the efficiency with respect to the limited conventional circuits of the times [4].
The DPA is a multidevice power amplifier enabling the possibility to work in such a way that the efficiency is high even when the amplifier is working in backoff region. This feature is necessary as the DPA works with digitally modulated signals with high *peak-to-average* power ratio [5].

The thesis is based on the stability and the re-design part of a DPA in the Ka-band, 17.3-20.3 GHz, Microwave Monolithic Integrated Circuit (MMIC) fabricated on a commercial Gallium nitride on Silicon (GaN on Si) technology[6].
The theoretical results that support the design of a DPA have been presented in the initial chapter. The rise of the task of the re-design is a result of the necessity to correct various drifts of the simulation results from the measurements on the actual device and last, but certainly not least for

its importance, the upgrade of the commercial Gallium nitride on Silicon technology from the foundry.
In the second chapter, the study and the comparison between the two different versions of the active devices used on the project has been reported, to be followed by the re-design of the DPA in the third chapter. The re-design stage consists on two parallel activities, the analysis of the behaviour of the existing design of the DPA with the new upgraded active device and the synthesis. The increase of the overall performance, the improving of the stability and the correction of frequency shifts have been the main focus of this thesis.

The *Keysight PathWave Advanced Design System*(ADS) software has been exploited in order to develop and support the work process.

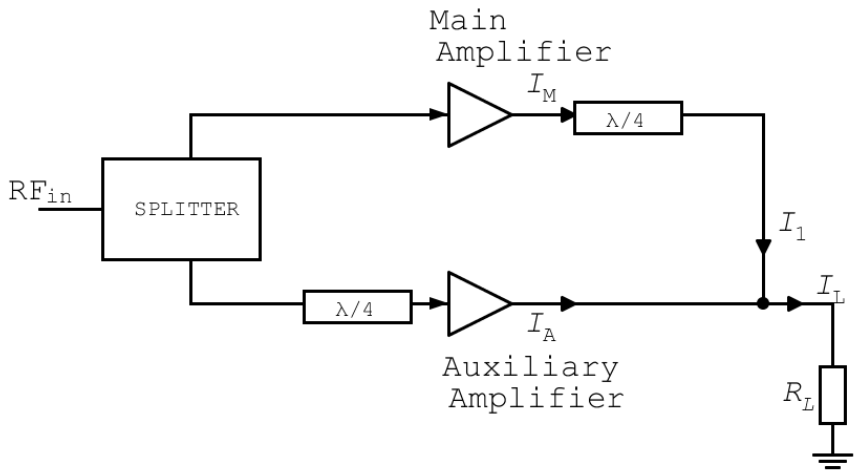

Figure 1: Basic scheme of a Doherty Power Amplifier.

Chapter 1

Basics

1.1 The Power Amplifier

The main task of the Power Amplifier (PA) is to provide maximum output power from a given active device with the maximum acceptable efficiency for the required level of linearity[3].

In order to be able to design and proceed with the analysis of the PA, it is necessary to define a set of PA parameters as follows.

The power delivered to the load at a given frequency f is defined as the **output power** P_{OUT} expressed as in (1.1).

$$P_{\mathrm{OUT}}(f) = \frac{1}{2} Re\left\{V_{\mathrm{OUT}} \cdot I^*_{\mathrm{OUT}}\right\} \tag{1.1}$$

The **input power** P_{IN}, is defined as the available input power at a given frequency expressed as in (1.2).

$$P_{\mathrm{IN}}(f) = \frac{1}{2} Re\left\{V_{\mathrm{IN}} \cdot I^*_{\mathrm{IN}}\right\} \tag{1.2}$$

Another important parameter to be considered for the PA is the power gain. More than a single power gain definition may be used for PAs. The **operational gain** G_{OP} is expressed as in (1.3), while the **transducer gain** G_{TR} as in (1.4). The P_{IN} is the actual transferred power from the generator to the amplifiers input while the transducer gain involves the $P_{\mathrm{av,IN}}$ that stands for the available input power of the generator. As a consequence, the transducer gain takes into account possible power mismatches between the generator and the amplifier.

$$G_{\mathrm{OP}}(f) = \frac{P_{\mathrm{OUT}}(f)}{P_{\mathrm{IN}}(f)} \tag{1.3}$$

$$G_{\mathrm{TR}}(f) = \frac{P_{\mathrm{OUT}}(f)}{P_{\mathrm{av,IN}}(f)} \tag{1.4}$$

Considering that a PA, from the energy standpoint, converts DC power P_{DC} (1.5), into microwave power P_{OUT}, parameters measuring the efficiency of this conversion have to be defined.

$$P_{\mathrm{DC}} = V_{\mathrm{BIAS}} \cdot \frac{1}{T} \cdot \int_0^T I_{\mathrm{BIAS}}(t)dt \tag{1.5}$$

The **efficiency** parameter η, is defined as in (1.6) and usually expressed as a percentage. It is straightforward to understand the importance of this parameter as not only it allows to evaluate the DC power transferred as microwave P_{OUT}, but also indicates the power dissipated by the active device.

$$\eta = \frac{P_{\mathrm{OUT}}(f_0)}{P_{\mathrm{DC}}} \tag{1.6}$$

Another parameter defined for the efficiency conversion of the PA is the **power added efficiency**, PAE as in (1.7), that as the name suggests, indicates the power added to the input signal centered at frequency f_0, taking into account the input power.

$$PAE = \frac{P_{\mathrm{OUT}}(f_0) - P_{\mathrm{IN}}(f_0)}{P_{\mathrm{DC}}} \tag{1.7}$$

In Fig. 1.1, a generic $P_{\mathrm{IN}} - P_{\mathrm{OUT}}$ graph including also the other parameters such as power gain and efficiency of a PA is shown. This power sweep indicates typical nonlinear behaviours of the amplifier such as the gain compression for the large signal regime. For small drive levels the amplifier behaves as almost linear but while the input drive is increased it passes to a highly non linear behaviour. The **-1 dB compression point** as depicted in the graph, is a figure of merit used to express this changing of behaviour. The corresponding drive level ($P_{IN,-1\mathrm{dB}}$) is the drive level where the gain compression is of 1 dB and as a consequence even the P_{OUT} deviates of 1 dB ($P_{OUT,-1\mathrm{dB}}$) with respect to the ideal linear approximation of the output power.
The nonlinearity behaviour of the amplifier is also mitigated in the drop of performance in terms of efficiency (both η and PAE).

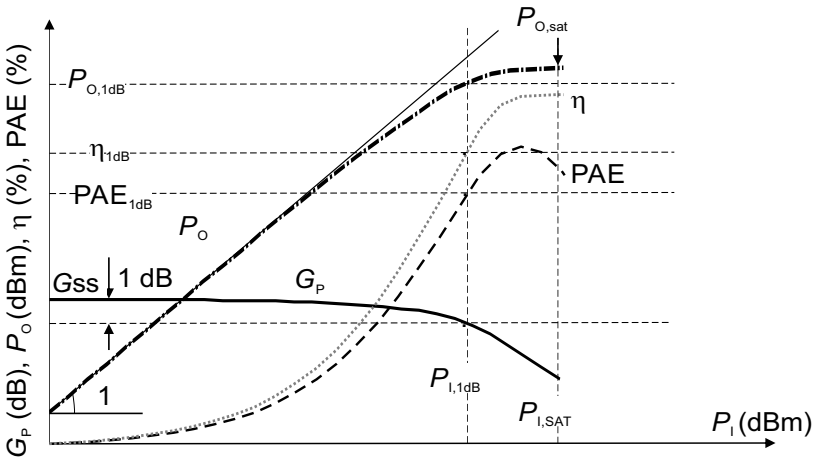

Figure 1.1: Generic PA, $P_{\mathrm{IN}} - P_{\mathrm{OUT}}$ including non linearities and various effects on different figure of merits, *Source*: *Telecommunication Electronics* [1]

The non linearities may be divided in two different groups, the *weak* non linearities and the *strong* non linearities [7] and much work has been done to characterized and model the actual device behaviour such as the *power series model*. The strong non linearities are introduced due to the physical limits of the FET, such as the pinchoff and power saturation. Either these models or behavioral models that come in form of libraries supported by the software are often used in the design of the power amplifiers and simulation of it and this is also valid for the work done in this chapter and throughout the other chapters of this thesis.

An important aspect of the presence of nonlinearities due to the behaviour of the amplifier is also the generation of intermodulation products. Considering two input signals centered at frequencies f_1 and f_2 (*two-tone test*), the intermodulation products are the results of their mutual interaction in the nonlinear PA [8]. Intermodulation products are generated tones at the output, centered at frequencies $\mathrm{m}f_1 + \mathrm{n}f_2$, with m and n nonzero positive or negative integers. The third-order intermodulation products generated (also higher odd orders), where $|\mathrm{m}| + |\mathrm{n}| = 3$, can become dangerous. The odd order intermodulation products centered at $|\mathrm{m}|f_1 - |\mathrm{n}|f_2$, with $\mathrm{m} > \mathrm{n}$ are the dangerous tones, as they are centered at frequencies close to f_1 and f_2, causing interference in the nearby channels.

In real case scenarios in communication, the input signals of a PA is usually neither single or two tone but signals with spectrum spread in a given band. For this reason another figure-of-merit has to be defined such as

the **adjacent channel power ratio**, (ACPR) (1.8), where MC stands for main channel and C_K stands for the k-th adjacent channel.
The APCR is a quantitative measure of the spectral regrowth and it is often regulated by standards regulatory bodies[9]. The standards are introduced by standardization bodies like the European Telecommunication Standards Institute (ETSI). As for the spectral regrowth, the regulations come in terms of *masks* that indicate the margin of the spectral regrowth between the main channel and the adjacent ones[10]. While designing a PA, the spectral regrowth has to be evaluated and then compared to these masks such as the ETSI mask, Fig. 1.2, in order to make sure that it complies to it.

$$ACPR_k = \frac{\int_{MC} p_{\text{out}}(f)df}{\int_{C_k} p_{\text{out}}(f)df} \tag{1.8}$$

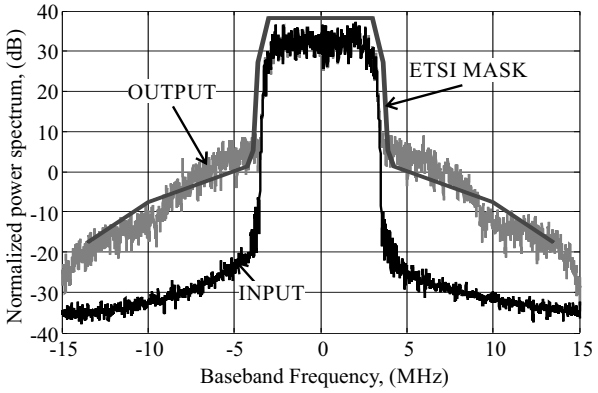

Figure 1.2: Example of an *ETSI* Mask as limit case for spectral regrowth, *Source*: *Electronics for Microwave Backhaul* [2]

PA Classes

There exist various classes of PAs, but in this chapter only the main classes such as Class A, B, AB and C have been chosen to be analysed as they are the most meaningful leading afterwards to the presentation of the DPA theory.

In Fig. 1.3 a general overview of the transcharacteristic (left) and of the output characteristic (right) of the different classes of PAs is shown. The design choice is done by properly setting the bias point of the active device. The choice of the various classes are mitigated even in terms of performance

as the results of a tradeoff between efficiency, gain and linearity go hand-to-hand with the choice of the bias.

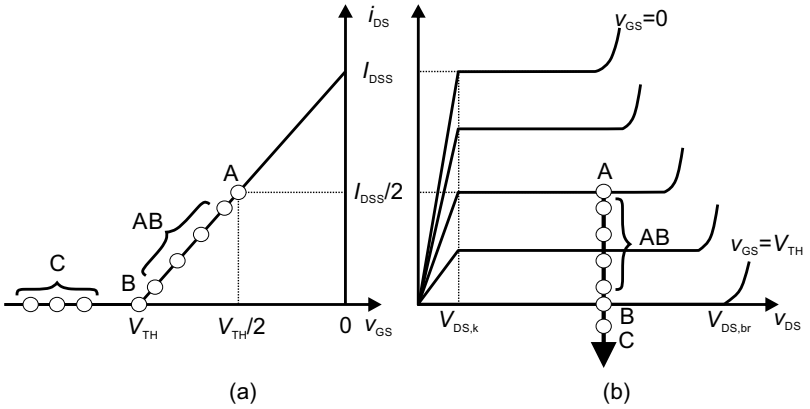

Figure 1.3: Transcharacteristic (left) and output characteristic (right) of generic FET and the bias setting for the different PA class, *Source*: *Telecommunication Electronics* [1]

The Class A amplifier, also known as the *quasi-linear* amplifier has the gate bias set at a greater value than the device threshold V_T, precisely at $V_T/2$. From the linearity standpoint the class A is known for it's optimum linearity whereas the relative distortion is minimum.

By proper selecting the optimum load and as a consequence the optimum load line as in Fig. 1.4 (left), the output waveform obtained is a sinusoidal as the input depicted also in Fig. 1.4 (right). The optimum load allows the output to have a maximum swing both in current and voltage limited only by the active device.
In terms of efficiency the performance of the class A is poor, with a maximum achievable efficiency of 50% (1.11) considering that the DC power consumption is given by (1.9) and the average RF power to load given by (1.10).

$$P_{\mathrm{DC}} = \frac{V_{\mathrm{DS,br}} \cdot I_{\mathrm{DSS}}}{4} \tag{1.9}$$

$$P_{\mathrm{RF,m}} = \frac{V_{\mathrm{DS,br}} \cdot I_{\mathrm{DSS}}}{8} \tag{1.10}$$

$$\eta = \frac{P_{\mathrm{OUT}}(f_0)}{P_{\mathrm{DC}}} = \frac{\frac{V_{\mathrm{DS,br}} \cdot I_{\mathrm{DSS}}}{8}}{\frac{V_{\mathrm{DS,br}} \cdot I_{\mathrm{DSS}}}{4}} = \frac{1}{2} \tag{1.11}$$

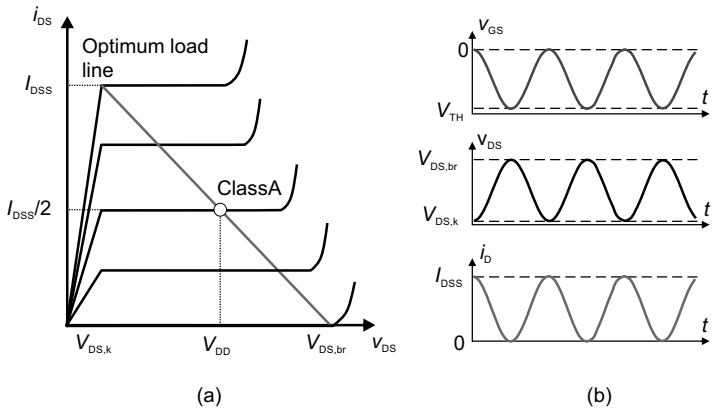

Figure 1.4: Class A output characteristic a) and terminals waveforms b), *Source*: *Telecommunication Electronics* [1]

A way to increase the efficiency exploited for the class B PA design is to reduce the DC power consumption.
The Class B has gate bias at threshold and as a consequence the output voltage does not overcome threshold for half of the period leading to a half wave rectified sinusoid drain current as in 1.6 (right). By doing this, the DC power consumption is lowered (1.12) with respect to Class A, meanwhile the average RF power to load remains unchanged, as in (1.10).

$$P_{\mathrm{DC}} = \frac{V_{\mathrm{DS,br}} \cdot I_{\mathrm{DSS}}}{2 \cdot \pi} \tag{1.12}$$

$$\eta = \frac{P_{\mathrm{OUT}}(f_0)}{P_{\mathrm{DC}}} = \frac{\frac{V_{\mathrm{DS,br}} \cdot I_{\mathrm{DSS}}}{8}}{\frac{V_{\mathrm{DS,br}} \cdot I_{\mathrm{DSS}}}{2 \cdot \pi}} = \frac{\pi}{4} \tag{1.13}$$

In order to have load current almost sinusoidal, a modification is done at system level, introducing a tuned load as in Fig. 1.5 in order to overcome the high nonlinearity of the amplifier.
The efficiency obtained in this way is a maximum of 78.5% (1.13) on the tuned load but this comes with a gain loss of 6 dB with respect to Class A considering the same optimum load is used.

Proceeding with the same concept as used for Class B, a Class AB and a class C have been developed in order to increase the efficiency.
The Class AB has input voltage that does not overcome the threshold for less than half a period. There is an increase in terms of efficiency with respect to class A but lower than the maximum of class B. The gain penalty is smaller.

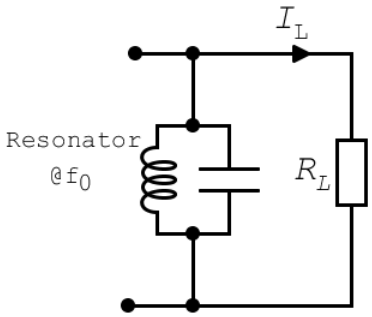

Figure 1.5: Tuned load necessary for employment of class B PA

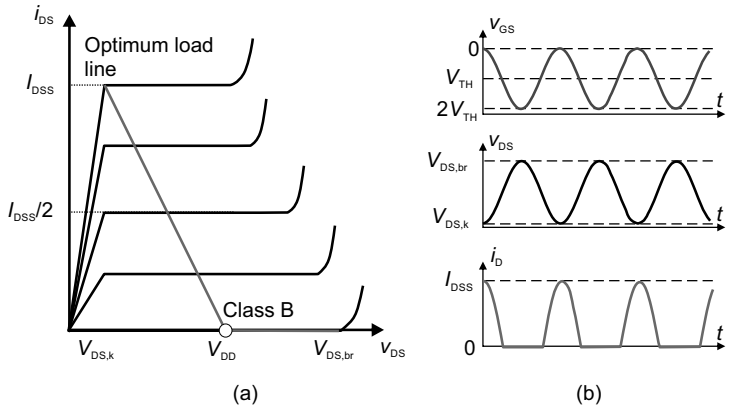

Figure 1.6: Class B output characteristic a) and terminals waveforms b), *Source*: *Telecommunication Electronics* [1]

The Class C the input voltage does not overcome the threshold for more than half of a period allowing the PA to reach 100% efficiency theoretically, with no practical utility as in this extreme case there would be no gain. While pushing the bias of the class C to lower values the efficiency can be increased but there is a linearity penalty to be considered, as it keeps decreasing. Usually in the Class C a compromise for a practical choice of bias leading to a certain level of efficiency has to be made. The efficiency chosen is reached when the amplifier is driven into saturation.

Other classes of PA exist and are used in a wide variety of applications. The most commonly designed except the Class A,AB and C are the Class D, E and F[11]. The Class D PA use at least two transistors as switches in order to generate square drain voltage or current waveforms. At the output of the Class D a tuned output filter has to be introduced in series that allows only the fundamental component to the load. For the ideal PA

a 100% efficiency is reachable. The practical class D PA performance is limited from switching speed and parasitic capacitance. The Class E is also based in switching operation but it employs a single transistor as a switch and has an additional drain shunt susceptance. The optimal Class E PA is assumed to have an ideal switch and can reach up to 100% efficiency but in practical cases it is limited by the non ideality of the switching capability of the transistor and variations in load impedance and shunt susceptance. The Class F instead, uses harmonic resonators at the output network to boost the efficiency by allowing to obtain square wave for the voltage waveforms and half sine wave current waveforms.

1.2 The Doherty Amplifier

Nowadays, the wireless communications systems employ high spectrum efficient access techniques and are in constant search to improve network capacity and reach higher data rate. Techniques such as Code Division Multiple Access (CDMA) or Orthogonal Frequency Division Multiplexing (OFDM) and others are included in the most common standards such as Wireless Local Area Network (WLAN) standards or either mobile communication networks as 3GPP LTE or 5G [12],[13],[14] and the trend for the future is clear.

Exploiting this techniques leads to good performance but it comes with a cost of having to use envelope varying signals, ruling out the usage of simple class PAs such as class AB or class C as they would dynamically change the PAs performance and not only but the Peak to Average Power Ratio (PAPR), (1.14), of this signals is also increased. Working with high PAPR signals means that the PAs have to be modified in order to be able to work in backoff without loosing efficiency.

$$PAPR_{[dB]} = 10 \cdot \log_{10}\left(\frac{P_{OUT,peak}}{P_{OUT,avg}}\right) \tag{1.14}$$

As mentioned even before in the introduction chapter, W.Doherty introduced the DPA and since then it has become one of the solutions for enhancing the efficiency of the PA whilst it is working in backoff.

The DPA is a multidevice power amplifier, based on the usage of two amplifiers, a main and an auxiliary amplifier, an input power splitter and a

common load as in Fig. 1.

The reason of the success of this configuration is the *Dynamic load modulation* that may be achieved. In order to understand this concept and for the sake of simplicity, a classic DPA with main amplifier an ideal class B amplifier case will be treated in the following. The maximum efficiency reachable by this class is 78.5% (1.13) at saturation of the device, where both drain current and output voltage reach their maximum swing having used as a load R_L the optimum load $R_{OPT} = \frac{V_{br}-V_{knee}}{0.5 I_{DSS}}$.

By defining the **Output back-off**, OBO as in (1.15), when operating at a certain OBO a class B would loose efficiency as the drain voltage swing would not be maximum.

$$OBO_{[dB]} = 10 \cdot \log_{10}\left(\frac{P_{OUT,sat}}{P_{OUT}}\right) \tag{1.15}$$

The *Load Modulation* is based on the idea that to reach the maximum efficiency at a given OBO, the R_L should be increased. As an example, if the amplifier is operating at half drive, by increasing the R_L from R_{OPT} to $2R_{OPT}$, maximum efficiency is achieved as in Fig. 1.7.

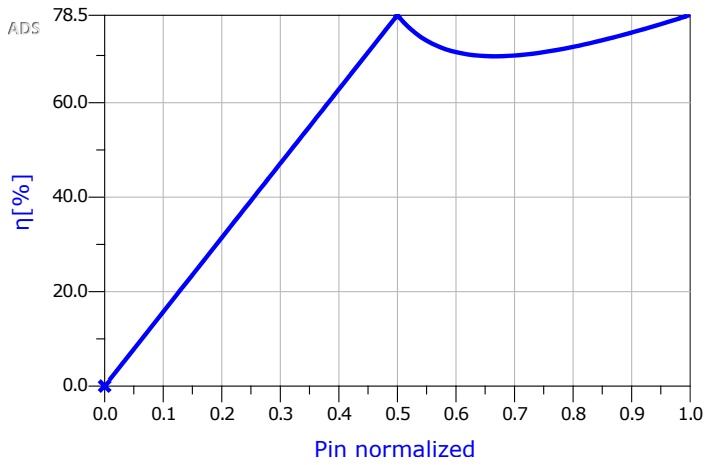

Figure 1.7: Efficiency of an ideal DPA

The working set of principles behind the dynamic load modulation, are the following three:

1. Load modulation

2. Active Load Pull

3. Impedance Inversion

The increasing input drive with a scheme containing only a simply modified load only ($2R_{\mathrm{OPT}}$), leads to the degradation of the efficiency. The *Active Load Pull* concept now becomes important, and so does the branch containing the auxiliary amplifier, ideally represented by the current generator I_2, see Fig. 1.8. Current generator I_1 represents the main amplifier. By using the active load pull, the impedance Z_1 may be modified by changing the current from the second generator I_2 , check equation (1.16).

$$Z_1 = \frac{V}{I_1} = R \cdot \left(\frac{I_1 + I_2}{I_1}\right) = R \cdot \left(1 + \frac{I_2}{I_1}\right) \tag{1.16}$$

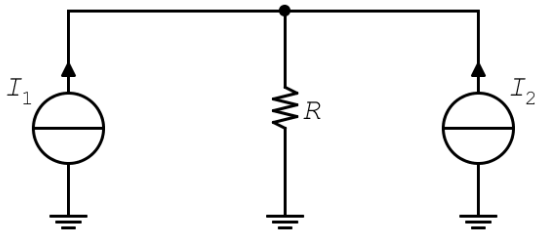

Figure 1.8: Basic scheme for the Active Load Pull concept

The problem at this point remains the fact that as both the input of the main and auxiliary amplifier increases the $\mathrm{R_L}$ has to be decreased up to reaching the $\mathrm{R_{OPT}}$ when the input goes full drive, in order to still have maximum class B efficiency, the active load pull concept alone is not able to achieve that.

In order to be able to have the right modulation of the load, the *Impedance inversion* is introduced, see Fig. 1.9. In this case by adding a quarter wavelength transformer line with characteristic impedance $Z_1 = \mathrm{R_{OPT}}$, the impedance of the common node is expressed as in (1.17). By choosing $\mathrm{R} = 2\mathrm{R_{OPT}}$, when $I_2 = I_0$ then $Z_{IN} = \frac{\mathrm{R}}{2} = \mathrm{R_{OPT}}$ (saturation) and when $I_2 = 0$ then $Z_{IN} = 2\mathrm{R_{OPT}}$ (breakpoint).

$$Z_{\mathrm{IN}} = \frac{R^2}{Z_1} = \frac{R^2}{R \cdot \left(\frac{I_0+I_2}{I_0}\right)} = \frac{R}{\left(\frac{I_0+I_2}{I_0}\right)} = R \cdot \left(1 - \frac{I_2}{I_0 + I_2}\right) \tag{1.17}$$

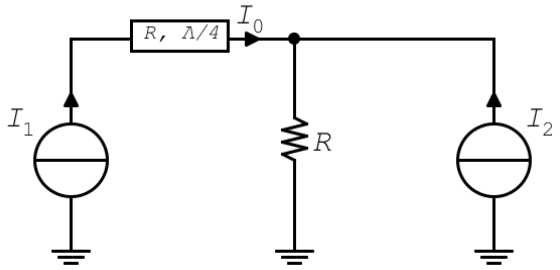

Figure 1.9: Basic scheme for the Impedance Inversion concept

By inserting a quarter wavelength transformer line, the branch containing the main amplifier has a phase delay with respect to the branch containing the auxiliary amplifier. As a consequence, another quarter wavelength transformer line must be introduced before the auxiliary amplifier to achieve the phase compensation.

Different OBO levels indicate the starting point of the choice of all the other parameters, and this work may be translated into resolving a set of equations in order to retrieve the main parameters (ideal case).

Small-signal equivalent circuit model of the GaN HEMT

Before proceeding with the analysis of the DPA, the *small-signal equivalent circuit model* of the active device (GaN on Si substrate, HEMT[15]) has to be presented, as in Fig. 1.10. In the extrinsic part of the model, the R_g (g-gate), R_s (s-source) and R_d (d-drain) represent the contact resistances, while L_g, L_s and L_d are the metallization inductances.
In the intrinsic part, the capacitance C_{gs} and C_{gd} together with the resistances R_i and R_{gd} describe the charge and discharge process for depletion region under the gate. The gate forward conduction is represented by G_{gsf} while the breakdown conduction by G_{gdf}, The G_{gsf} models the capacitance between drain and source electrodes separated by the depletion region in an electrostatic sense while R_{ds} is the channel resistance. The g_m represents the transconductance whilst the τ models the channel propagation delay.

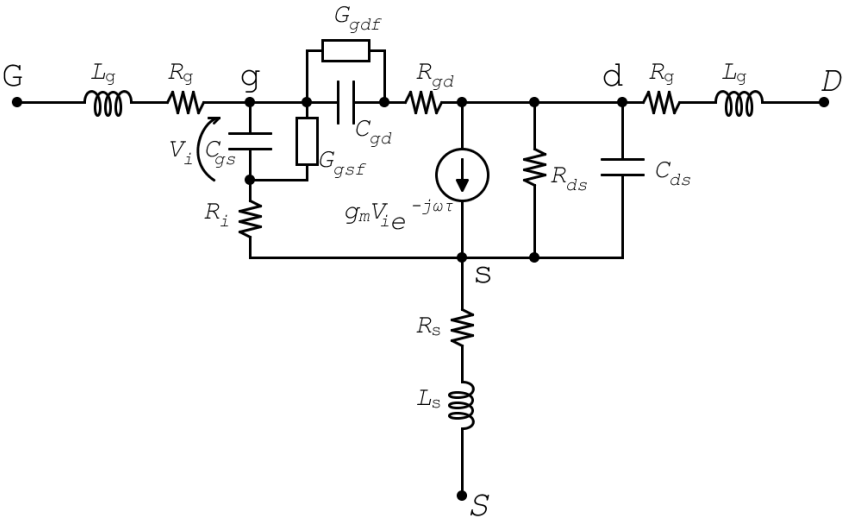

Figure 1.10: Small signal equivalent circuit model of a GaN on Si HEMT

The Ideal DPA

In this section, the results of the simulations of the ideal DPA operating at 6 dB backoff in the frequency range 17.3-20.3 GHz have been presented in addition to the efficiency η that has already been analysed (Fig. 1.7).

In the ideal simulation, both the main and auxiliary amplifier have been replaced by voltage controlled current generators, I_{MAIN} and I_{AUX} neglecting the *parasitic components* introduced in the small-signal equivalent circuit. As depicted in Fig. 1.11, the real active device (GaN HEMT in this project) are represented by the generators, where $I_{MAIN} = g_{m_{main}} \cdot V_i$ and $I_{AUX} = g_{m_{aux}} \cdot V_i$.

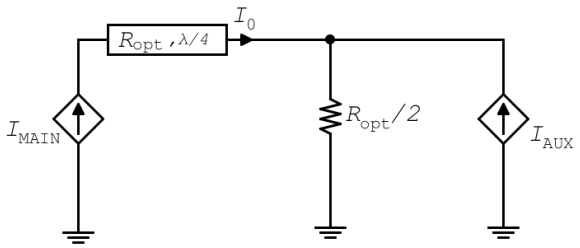

Figure 1.11: Ideal DPA scheme with voltage controlled current generators

By quickly analysing Fig. 1.12, it is immediately noticed that already at

half input drive the main drain voltage has saturated as expected, meanwhile the current generator of the auxiliary amplifier only starts at half drive.

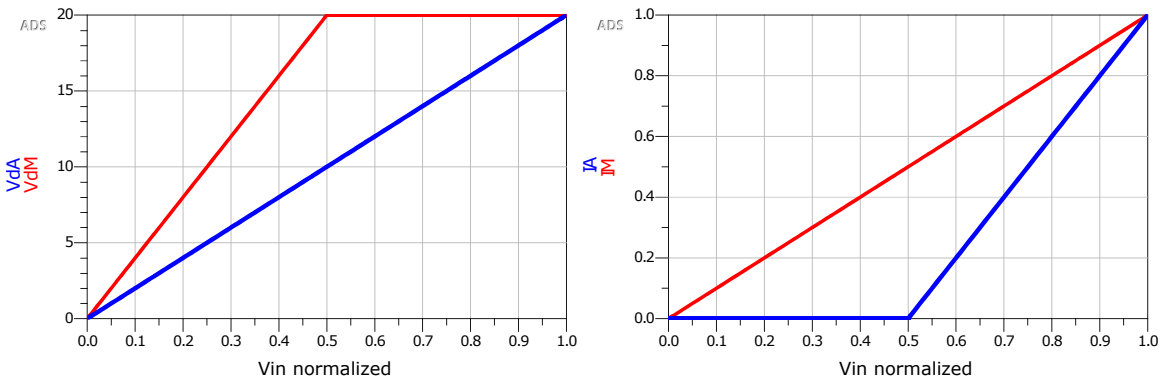

Figure 1.12: Main and auxiliary drain voltages (left) and drain currents (rights) in the ideal case

The Fig. 1.13 instead, represents the load modulation achieved in this ideal case. In this chart the reflection coefficients of the auxiliary and main generators, with respect to the optimum load R_{OPT} as in (1.18) have been presented. The main and auxiliary impedances are verified to reach R_{OPT} at saturation, where the reflection coefficient is unitary.

$$\Gamma = \frac{Z - R_{\mathrm{OPT}}}{Z + R_{\mathrm{OPT}}} \tag{1.18}$$

Bandwidth limitations

The bandwidth of the DPA is a well-known issue and considering that the space application of this project requires a large bandwidth[16], specific techniques for bandwidth extension have to be introduced.

Several factors, listed below, are contributing to the bandwidth limitations of the classic DPA[17].

1. Output Network

   The $\lambda/4$ impedance inverter at the output of the main amplifier is usually the main bandwidth limiting component. This limitation is

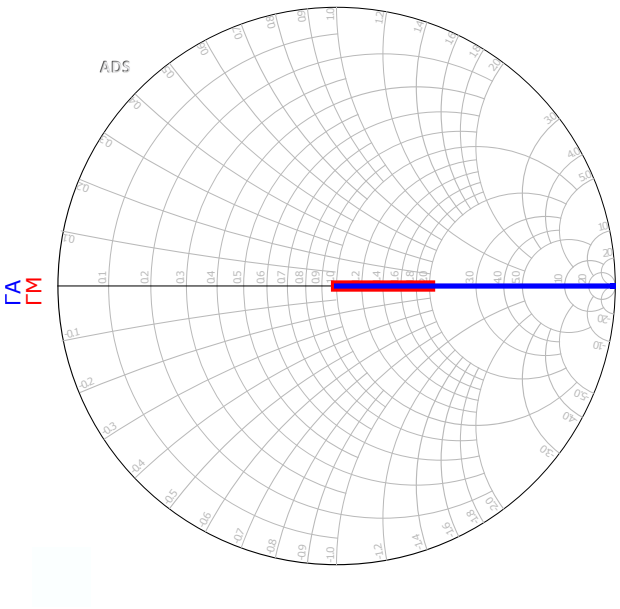

Figure 1.13: Main and auxiliary load modulations in the ideal DPA case

easily understood by analysing the impedance (or the reflection coefficient) of the main amplifier at peak output power and also at backoff. Considering the ideal DPA working at 6 dB backoff and assuming a symmetric transistor configuration, the characteristic impedance chosen is $Z = R_{OPT}$, while the load $R_L = 2R_{OPT}$. The load at the main amplifiers output is as described in (1.19) where k=1 at saturation and k=2 at backoff.

$$Z_M(f) = R_{\mathrm{OPT}} \cdot \frac{k + j \cdot tan(\frac{\pi \cdot f}{2 \cdot f_0})}{1 + j \cdot k \cdot tan(\frac{\pi \cdot f}{2 \cdot f_0})} \tag{1.19}$$

In Fig. 1.14 the results of the simulation of a quasi-ideal model of the transmission line used for the following steps has been introduced.

Since the load impedance is different from the value optimal load requested, an output matching network to match the two impedances has to be inserted. Assuming the output matching network an ideal $\lambda/4$ transmission line, it can be concluded in an analogous way that also the output matching network introduces a bandwidth limitation for the DPA.

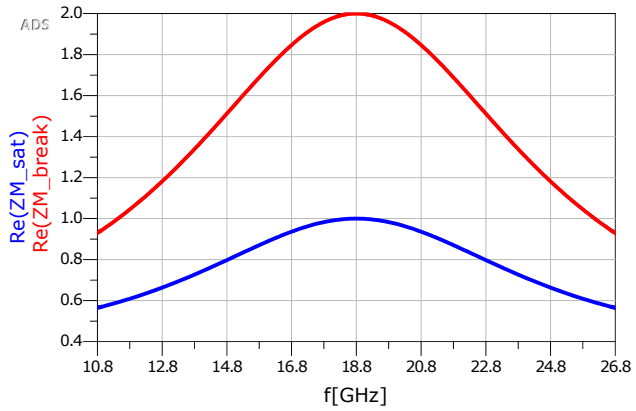

Figure 1.14: Main amplifier output impedance (normalized) at saturation (blue) and breakpoint (red), ideal case

2. Parasitic Capacitance

   The parasitic capacitances of the transistor are also limiting the bandwidth of the DPA. By considering the small-signal equivalent model examined, the parasitic capacitances of the amplifiers limit the bandwidth if not properly taken into account at design stage of the overall DPA. The gate-source capacitance C_{gs} limits the bandwidth of the input phase-alignment network (correcting the phase between the input of the main and auxiliary amplifier) and also of the input power splitter. The complexity of dealing with this input parasitic capacitance is increased due to its non linearity, making the input impedance sensitive to different input power levels used.
   The gate-drain capacitance C_{gd} is another nonlinear impedance at the input and as such it also limits the bandwidth.
   The least but not for importance of the parasitic capacitances introducing limits is the drain-source capacitance C_{ds}. The C_{ds} affects the output impedance seen by the amplifiers, leading to bandwidth limiting of the load-modulation network. Several techniques may be introduced in order to mitigate the bandwidth limitation effects of the parasitic capacitances such as offset lines[18] or compensation networks[19].

3. Input Network

   The phase-shift network and the input power splitter are introduc-

ing $\lambda/4$ transmission lines (i.e Wilkinson power splitter[20]). As a consequence, the components of the input network of the DPA are also limiting its bandwidth.

A solution used in order to limit the effects of the parasitic capacitance C_{ds} is its absorption into the impedance inverter network. An equivalent lumped element network of the $\lambda/4$ transmission line, as in Fig. 1.15 has been exploited. The equations used to evaluate the value of the components L and C of this equivalent network are listed below (1.20) and (1.21). This solution is not suitable to all cases as the C_{ds} has to be smaller than the value of the capacitor calculated via (1.21).

$$L = \frac{Z_0}{\omega_0} \tag{1.20}$$

$$C = \frac{1}{Z_0 \cdot \omega_0} \tag{1.21}$$

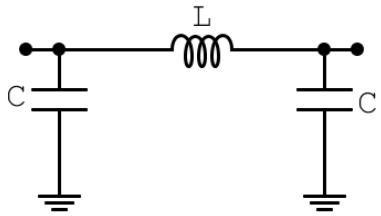

Figure 1.15: Lumped component equivalent of a generic transmission line

The introduced solution does not cancel the limitations of the bandwidth of the DPA. In order to enhance the bandwidth of the DPA in this project, another solution known as the *Two-Section Peaking Network*[21] is embedded at the output of the two amplifier branches as in Fig. 1.16. This whole network is given the name of output combiner stage.

The Two-Section Peaking network consists in adding two $\lambda/4$ at the output of the auxiliary amplifier with parameters calculated as in equations (1.22),(1.23) and (1.24). These considerations are valid assuming the DPA is symmetrical, so same transistor for both main and auxiliary amplifier are adopted. The C_{OUT} is the amplifiers output parasitic capacitance. By employing a semi-lumped or lumped element equivalent of the transmission lines, it is clear that this solution implements even the parasitic capacitance absorption in the combiner stage.

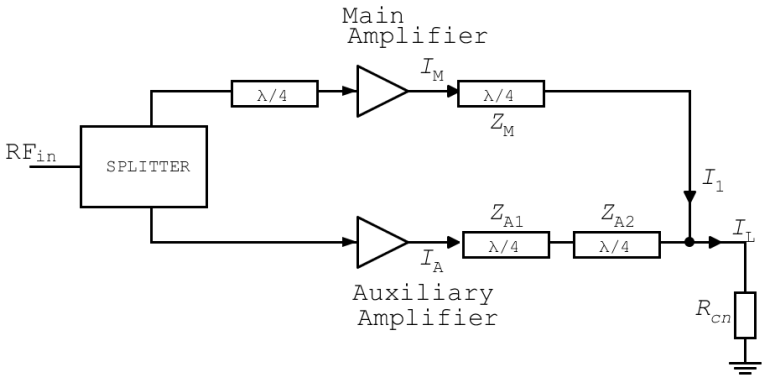

Figure 1.16: DPA with Two-Section Peaking Network for bandwidth enhancement

$$Z_M = Z_{A1} = \frac{1}{2\pi \cdot f_0 \cdot C_{\mathrm{OUT}}} \tag{1.22}$$

$$Z_{A2} = 2R_{cm} \tag{1.23}$$

$$R_{cm} = \frac{Z_M^2}{2R_{\mathrm{OPT}}} \tag{1.24}$$

The immediate effect that can be checked is the difference of the impedance at the amplifiers output in the working band at both saturation and breakpoint as in Fig. 1.17. The curve depicted in *RED* represents the impedance of the main amplifier at saturation while in *BLUE* the equivalent at breakpoint. The dashed curves represent the equivalent main amplifier output impedances in the initial basic DPA . In order to have better understanding of how the combiner stage has modified the bandwidth, in Fig. 1.18 the reflection coefficient of the output of the main amplifier has been evaluated in the different cases mentioned. As in the previous chart, the *RED* indicates the reflection coefficient of the output impedance of the main amplifier at saturation with respect to $2\mathrm{R}_{\mathrm{OPT}}$ and the *BLUE* the equivalent reflection coefficient with respect to $\mathrm{R}_{\mathrm{OPT}}$. Both this reflection are related to the bandwidth enhanced DPA with the proposed network. Analysing the difference in terms of band with respect to the basic DPA (represented by the reflection coefficient, dashed curves), an improve is noticed both at saturation and at breakpoint of the bandwidth enhanced DPA.

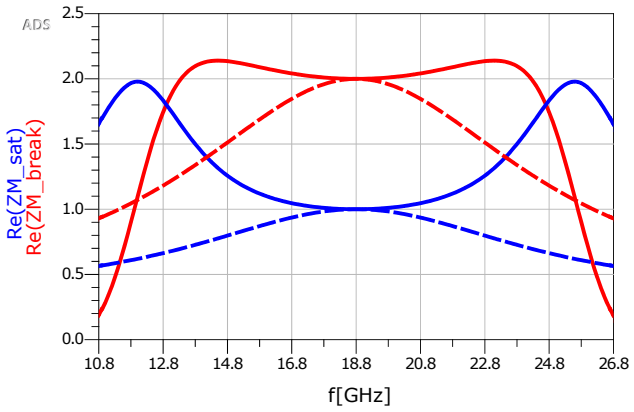

Figure 1.17: Main amplifier output impedance (normalized) at saturation (blue) and breakpoint (red) of the DPA with Two-Section Peaking Network(solid) and basic DPA (dashed)

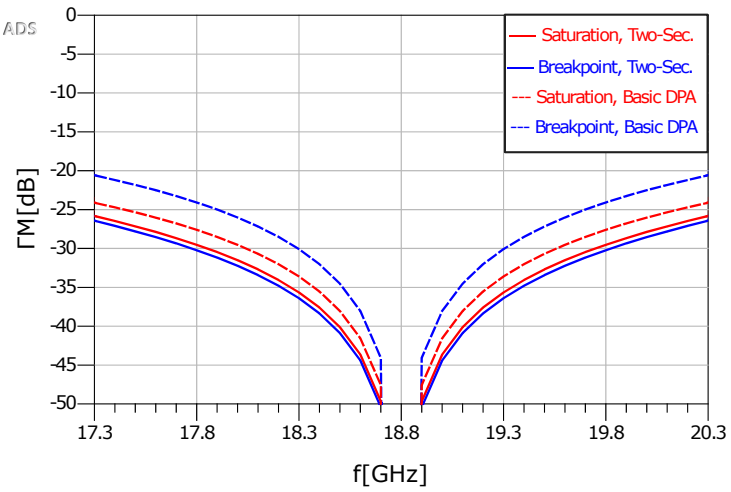

Figure 1.18: Reflection coefficient of the main output impedance at saturation (red) and breakpoint (blue) of the DPA with Two-Section Peaking Network (solid) and basic DPA (dashed)

The ideal DPA introduced may be also enhanced leading to improvements in terms of output power and larger OBO regions with high efficiency[22]. In order to increase the overall output power of the system, two individual DPA structures as seen before may be implemented in the same architecture where both are connected to the same load. Proper modifications in terms of matching networks have to be done in order to implement this architecture.
An architecture that introduces the possibility to extend the region of high efficiency over a wider range of output powers is the N-way DPA[23]. The N-way DPA architecture is composed of one main amplifier in parallel with (N-1) number of auxiliary amplifier. The complexity of the classic N-way DPA increases as it is composed of (N-1) auxiliary amplifiers with a much more complex overall output combiner N input and N output matching networks and a N-way power splitter. Another negative aspect of the N-way DPA is related to the significant drop in efficiency between the two peaking efficiency points, which is proportional to N.
Another architecture that allows to extend the region of high efficiency is the Multistage DPA[24]. Also this architecture employs more auxiliary amplifiers where each one of them is connected with different quarter wavelength transmission lines to combine the output powers. The characteristic impedances of the quarter wavelength depend on the levels of the backoff power requested to be achieved. The difference with respect to the N-way DPA is that in this architecture the efficiency peaking points are more than two, proportionate to the number of the auxiliary amplifiers allowing

to provide higher efficiencies at all the backoff levels.

1.3 Doherty on GaN technology

Nowadays, Gallium-nitride power transistor have matured and are well integrated in many different applications[25] due to their advantages with respect to the other power transistor technologies.
To begin with, the GaN HEMTs are characterized by a high breakdown voltage allowing to reach high output impedance per watt of RF power and as a consequence lower loss matching circuits. The reason for this is that the high breakdown allows to have much larger drain voltages to be used.

Other key advantages are the proper combination of the high output power density at high frequencies with larger bandwidth and increased linearity with respect to other technologies . All these advantages are results of the semiconductors physical properties, consisting in large band-gap generating the breakdown electrical field up to ten times larger than the one of Si. Another reason for the widespread is even the control of thermal degradation and the trap effects which give rise to frequency dispersion effects in Nitrides.[26]

This latter key feature is very interesting from the point of view of this project as the DPA targets an architecture handling the satellite downlink in the Ka-band (17.30-20.30)GHz. Not only it benefits this project, but the control of the thermal degradation is a key advantage on the widespread of the GaN technology on satellite communications.
The thermal stress at microwave power is a major issue as it immediately impacts the operating life time of MMICs on board satellites[27]. In the task of increasing reliability, leading to a major lifetime, electronic systems must comply with *derating* rules. What this means is that the major source of stress for the high-power active devices is self heating and the design should address carefully this aspect. The *non-heat conduction* in space complicates even more the overall DPA design. The high power efficiency reachable throughout the technology is also a key feature to be used in the PAs in space application as the power supply available is more limited.

The GaN epitaxy can be grown on both SiC and Si substrates. The SiC substrate is characterized by extremely good thermal behaviour as it better

mitigates heat dissipation issue whilst being much more expensive as it is not widely commercialized.
The Si substrate instead, is more limited in terms of thermal behaviour but it has a much lower cost with respect to SiC and much better integrated with other systems on the same chip. As a result, the thermal issue causing performance leaking has to be evaluated more carefully in the case when the derating must be applied.

Chapter 2

Analysis of the active device

In this second chapter the work has been focused on the characterization and analysis of the active devices used in this project. The used active devices are based on the III − V compound semiconductor Gallium nitride technology for the active layer on Silicon substrate technology by *OMMIC*.

This thesis work consists on the stability study and re-design of an already existing DPA. Following an update on the technology available from the foundry, in this chapter an analysis and comparison between the characteristics of the old version of the active devices included in the *Process Design Kit* (PDK) and the new PDK version is shown.
In the design kit of both PDK, the transistors available are of two types, one with 100nm of gate length used in the present work and the other with 60nm of gate length. Another aspect on the active devices geometry is that in order to obtain high DC current and output power from transistors the gate width has to be increased. An immediate result of this is the increase of the gate resistance (R_G), check equation (2.1), where R_{G0} is gate resistance per unit and W stands for the width of the gate.

$$R_G = R_{G0} \cdot W \tag{2.1}$$

A *parallel multifinger gate* approach, as in Fig. 2.1, is exploited by this technology, avoiding the usage of a single wide gate but introducing several (N) fingers. The adoption of this approach results in a decrease of the gate resistance, check equation (2.2). Negative aspects to be taken in account are that with the increase of the number of gate fingers above certain values, there are effects that may impact the gain become important such as the increase of the source inductance and increasing of phase shift between the gate fingers.

$$R_G = \frac{R_{G0} \cdot W}{N^2} \tag{2.2}$$

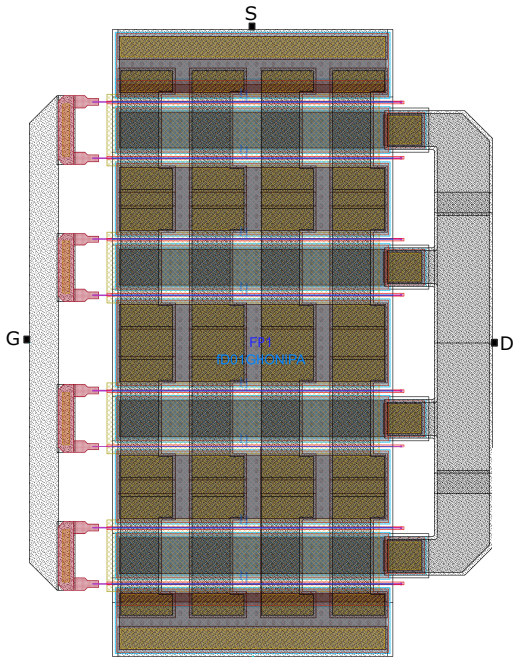

Figure 2.1: Example: Layout of the active device with N=8 gates, *parallel multifinger* approach

The actual devices used and compared in this chapter are the 8x100 μm, 6x50 μm and 4x50 μm, were the name format is (N *x Width of the gate in* μm) and will be used throughout their treatment in the following chapter.

2.1 DC characteristics

As a first step to be taken in the design of the PA and eventually the DPA, the devices DC characteristics has to be analysed. In this first section, in Fig. 2.2 the DC characteristic of the new PDK, 8x100 μm is shown.

The breakdown can be immediately confirmed to be at a high voltage of around 30V. The maximum of the drain voltage swing chosen is 22V in order to avoid the breakdown effect. The drain current slopes at higher constant V_{GS} with increasing V_{DS} are negative as an result of the increasing thermal effect.

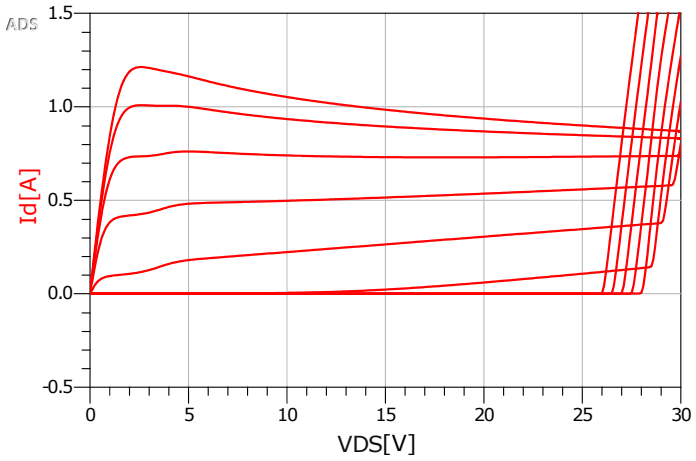

Figure 2.2: DC, output characteristic of the new PDK device 8x100 transistor

Having chosen the V_{DS}=11V the drain current with respect to the gate voltage of the 8x100 μm transistor is described in Fig. 2.3.
Another important aspect that had to be verified, useful for the following analysis and re-design stages is the analysis on the difference of the DC characteristics between the two different PDK and the effect on the bias chosen.

In the following Fig. 2.4, the devices output characteristic 8x100 μm, new PDK is shown in *RED* and in *BLUE* the output characteristic of the 8x100 μm, old PDK. In order to have a I_D=60mA/mm, so basically I_D=50mA for the 8x100 μm device, I_D=20mA for the 6x50 μm and I_D=12mA for the 4x50 μm it has been found that at V_{DS}=11V the V_{GS}=-1.35V with respect to the previous version of the technology that the V_{GS} necessary was -1.6V. The new bias voltage to be applied for the gate and the overall

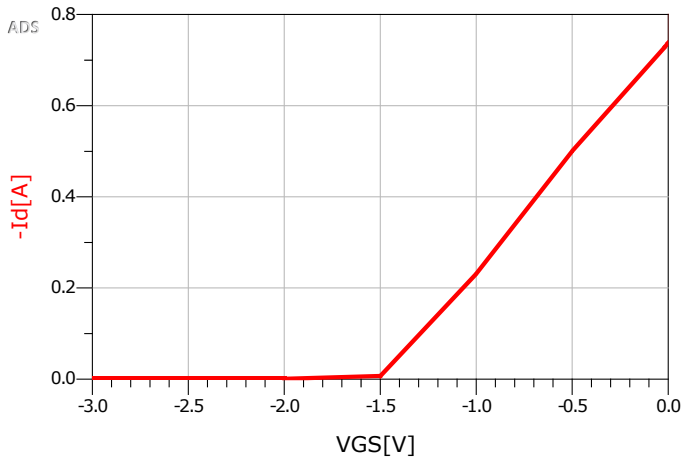

Figure 2.3: Drain current vs gate voltage of the new PDK 8x100 transistor , V_{DS}=11V

I_D=60mA/mm will be also used in the next stages. This is the first major difference between the two versions of the active devices. The dashed output highlight this difference as they are both correspondent to the same V_{GS}=-1.5V.

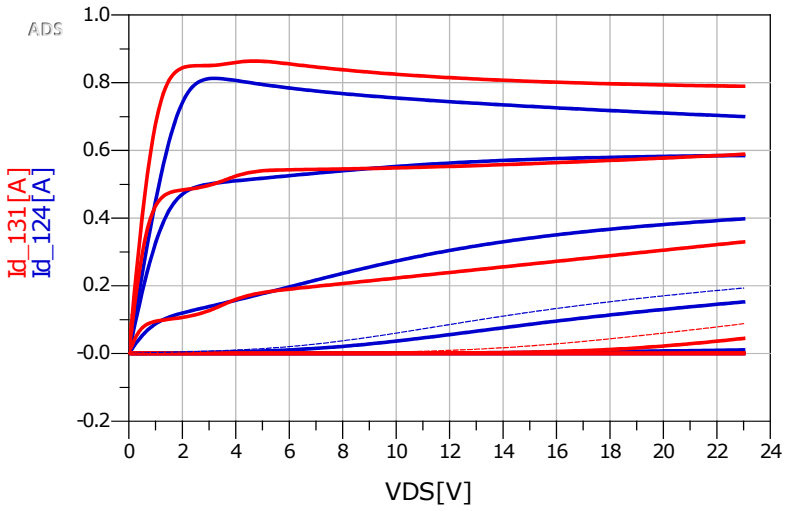

Figure 2.4: DC, output characteristic of the new PDK transistor 8x100, *RED* and of the old PDK 8x100, *BLUE*

Extrinsic Parasitic Parameters

An important step in the initial design stage of the PA and eventually the more complex DPA is the extraction of the extrinsic parasitic parameters. The eventual evaluation of these parameters allows to access the intrinsic drain node and obtain the intrinsic drain current and voltage behaviour. The most important aspect of the extraction of the parasitic components values is the necessity to properly include their values afterwards in the output combiner stage design. Once these parameters C_{OUT} and L_{OUT} are extracted, the intrinsic drain node is made available at simulation level by first cancelling the effect of this components and then by properly re-introducing them as in Fig. 2.5.

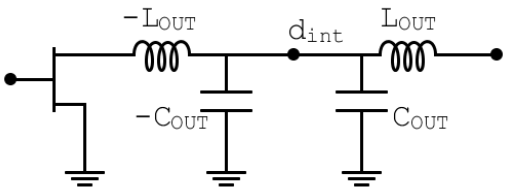

Figure 2.5: Schematic of the method to access the intrinsic drain node at simulation level

In order to complete the extraction, one possible way is to bias with the chosen V_{DS} and $V_{GS} < V_{po}$ and evaluate the S-parameters of the amplifier. Afterwards through the S-parameters de-embedding, the relative C_{OUT} and L_{OUT} are obtained.
For this given application, the models of the amplifiers include an option that allows to access immediately from it the intrinsic drain node. By using this option and the S-parameter de-embedding, a more accurate model is obtained. The latter method was the one chosen for the extraction and the values of the extrinsic parasitics at drain found for the 8x100 μm device are $C_{OUT} = 471$fF and $L_{OUT} = 25$nH.

2.2 Stability

2.2.1 Stability theory

Stability is a very important aspect to consider when designing a power amplifier and as consequence of a Doherty power amplifier. Unconditional

stability is the key word for the achieving of simultaneous power matching in an amplifier[3].
The out-of-band stabilization is always mandatory, especially at low frequency, as possible and spurious low frequency oscillations may occur leading to the saturation of the amplifier. The gain at low frequency for the amplifiers tend to be very high.

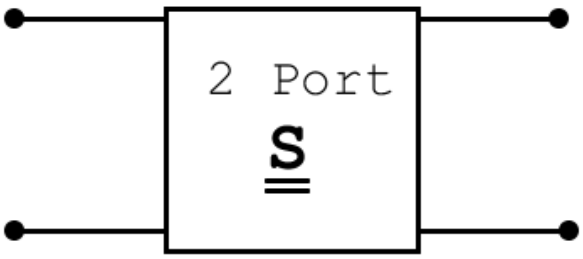

Figure 2.6: Two-port symbol ,unloaded

To actually study the stability, it is assumed a two-port as in Fig. 2.6 is loaded with real generator and load impedance, so a generator and load impedance with a real part which is positive. As described in the *Two-Port Stability* chapter in [3] this loaded two port is unconditionally stable if :

1. " The input impedance has positive real part for *any* value of the generator impedance.

2. The output impedance has positive real part for any value of the generator impedance."

Translated in terms of reflectance coefficients :

1. For every $|\Gamma_L| < 1$, the $|\Gamma_{\mathrm{IN}}| < 1$

2. For every $|\Gamma_G| < 1$, the $|\Gamma_{\mathrm{OUT}}| < 1$

Two different approaches may be followed in order to quickly evaluate the unconditional stability of the two port based upon two different parameter evaluation based criteria.

The first is the *Two Parameter Criteria* where in order to have unconditional stability the set of following two criteria (2.3) and (2.4), where K

stands for stability coefficient/ *Linville* coefficient and Δ_S for the determinant of the two port S-matrix.

$$K = \frac{1 - |S_{22}|^2 - |S_{11}|^2 + |\Delta_S|^2}{2 \cdot |S_{21} \cdot S_{12}|} > 1 \tag{2.3}$$

$$|\Delta_S| < 1 \tag{2.4}$$

The second approach is the *Single Parameter Criteria*. In this case it is necessary to check that only one of the two following parameter (2.5) or (2.6) is true. This parameters will be more extensively used in the stability analysis of the devices.

$$\mu_1 = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \cdot \Delta_S| + |S_{12} \cdot S_{21}|} > 1 \tag{2.5}$$

$$\mu_2 = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \cdot \Delta_S| + |S_{12} \cdot S_{21}|} > 1 \tag{2.6}$$

2.2.2 Ideal Stabilization Network

The stabilization of the active device is achieved by properly setting dissipative elements in the input/output or even in feedback as in Fig. 2.7 [3]. By adding a proper resistance in series or conductance in parallel as in the figure leads to unconditional stability as it is able to compensate for any negative input/output resistance of the device due to the possible output/input termination at a given frequency.

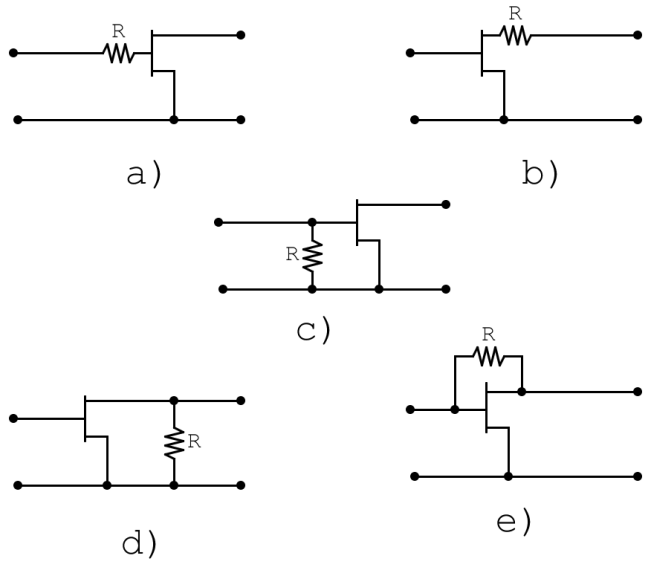

Figure 2.7: Ideal stabilization network with resistive elements in input a) and c) , feedback e) and in output b) and d)

The resistive elements as described before, that may be included in the stabilization network, have an immediate effect on the stability as it modifies the stability factor K. In order to understand the concept of stabilization throughout the use of dissipative elements, the stability factor is expressed in terms of admittance (or impedance) as in equation (2.7) (or (2.8)).

$$K = \frac{2Re[Y_{11}]Re[Y_{22}] - Re[Y_{12}Y_{21}]}{\mid Y_{12}Y_{21} \mid} \tag{2.7}$$

$$K = \frac{2Re[Z_{11}]Re[Z_{22}] - Re[Z_{12}Z_{21}]}{\mid Z_{12}Z_{21} \mid} \tag{2.8}$$

The introduction of the feedback resistive elements is avoided in the classic design of the PA because of the reduction of gain and other complications

such as the need to add DC block to keep the input and output bias separated. In order to make the stabilization effect frequency dependent, reactive elements are introduced to the stabilization network as in Fig. 2.8. By using either in series a R in parallel C (RC block) or in parallel a R in series with a L (RL block) stabilization in-band may be achieved. The impedance/admittance of the relative blocks are expressed on the equations (2.9) for the RC block and (2.10).

$$Z_{\text{IN}} = \frac{R}{1 + j\omega RC} \tag{2.9}$$

$$Y_{\text{IN}} = \frac{G}{1 + j\omega GL} \tag{2.10}$$

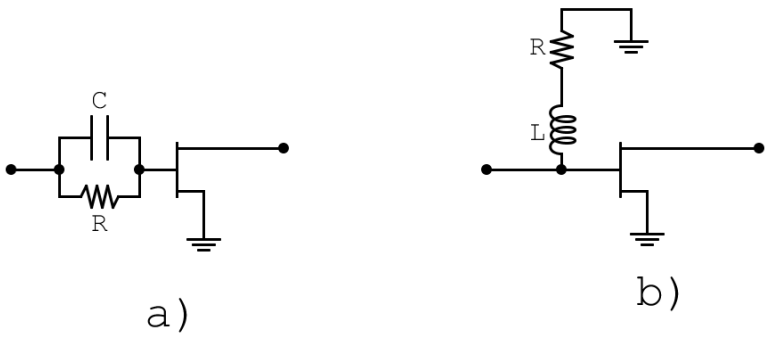

Figure 2.8: Ideal stabilization networks extended with reactive elements

In Fig. 2.9 the immediate effect on the K stability factor of the presented networks is shown. In *RED* the stability factor K_1 of the active device without a stabilization network followed by K_2 in *BLUE* represented the stability factor of the device and the series of the RC parallel block, K_3 in *PURPLE* of the active device and the parallel RL series block and finally in *GREEN* the K_4 of the active device and both the combination of the RC parallel block and the parallel RL series block as in Fig. 2.10. To be noticed that in this treatment I have considered only the modification on the Rollet stability factor but this does not lead to the stability of the device as even the condition on (2.4) must be verified. Moreover, the latter stabilization network introduced of both the combination of RC and RL blocks is used at least in the initial PA designing stage as it properly enforces the stability condition verification both in-band and out-of-band, as described in Fig. 2.10.

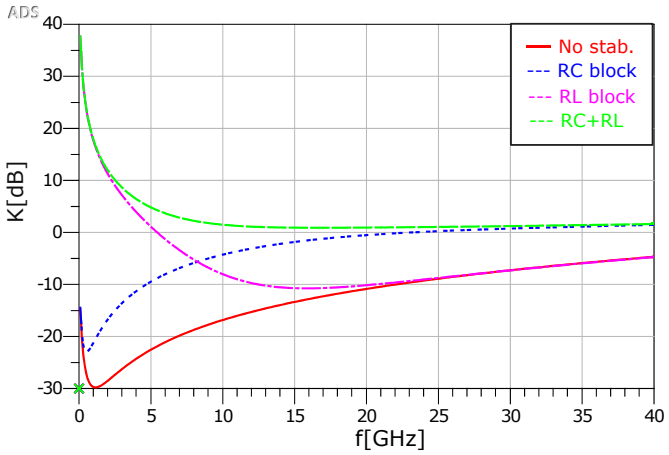

Figure 2.9: Modification of the Rollet stability factor throughout the various ideal stabilization networks, in red- no stabilization, in blue- RC, in purple- RL, in green- RC and RL combination

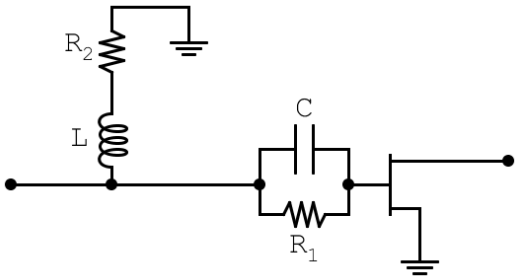

Figure 2.10: Final ideal stabilization network including both RC parallel block in series and RL series block in parallel at devices input.

In the following Fig. 2.11-2.12 the proposed final ideal stabilization network has been applied to the different devices. After a simulation activity the parameter values, described on Table 2.1, are the values used to generate the examined results.

It is important to notice that at this point, dealing only with idealized networks, values of μ_1 higher but very close to 1 are easily achievable in-band. This leads to very low difference of MAG and for that it is possible to have ΔMAG lower then 0.5 dB at center frequency 18.8 GHz as shown in the result table.
In all cases, the stability was achieved from DC to at least 40 GHz with a MAG reduction of the order of 1 dB at the lower frequencies in the operating band. Moreover, the decreasing with the frequency behaviour of the

MAG has been compensated through the stabilization network.

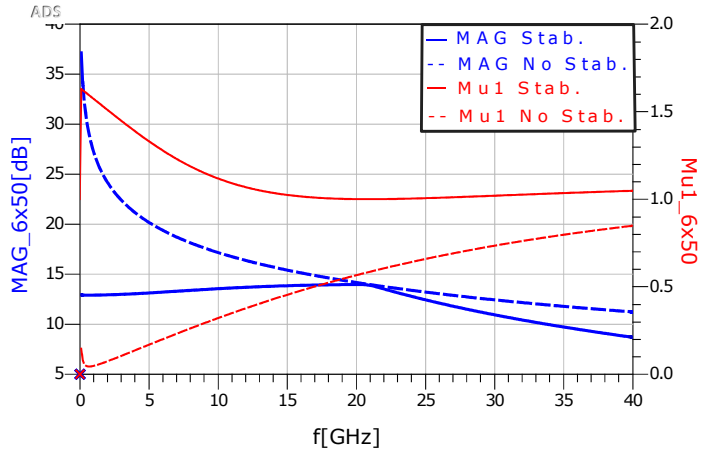

Figure 2.11: Device performance after applying the ideal stabilization network, 6x50 (right) at V_{DS}=11V , I_D=60mA/mm

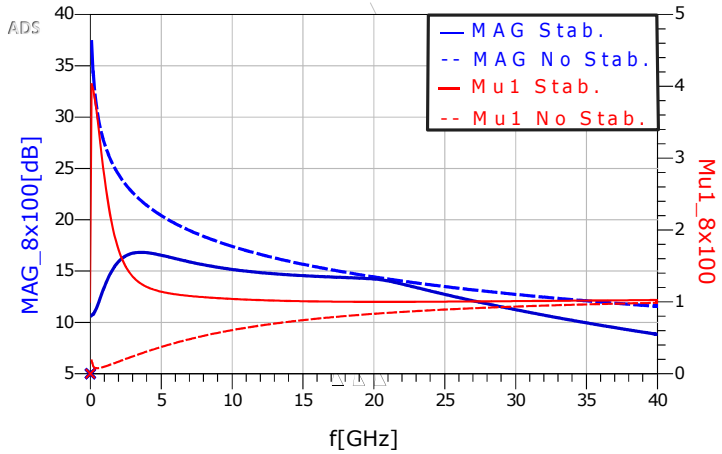

Figure 2.12: Device performance after applying the ideal stabilization network, 8x100 at V_{DS}=11V , I_D=60mA/mm

Before proceeding with the analysis of the active device and it's behaviour with respect to the existing stabilization network built on the old PDK in RUN1 of the project, a quick overview of the behaviour of the MAG and μ_1 at V_{DS}=11V and I_{DS}=60mA/mm bias, of the two version of active devices has been and shown as in Fig. 2.13 and in Table 2.2. It is fundamental to evaluate the difference in terms of MAG and μ_1, considering that normally maximum effort is put in the stabilization network to obtain μ_1 as close

Device	**R1 [Ω]**	**R2 [Ω]**	**C [pF]**	**L [nH]**	**ΔMag [dB]**
4x50	5.35	31.05	0.401	0.632	0.15
6x50	16.24	12.02	0.718	0.15	0.48
8x100	18.5	2.8	1.152	0.514	0.374

Table 2.1: Parameters of the various ideal stabilization network for the different devices able to satisfy the stability condition .

to 1 but always higher in order to guarantee both stability and no gain degradation in-band. By considering the results expressed, the difference for all the set of devices between the new and old PDK is noticeable. The differences are both in terms of MAG (ΔMAG $>$ 2 dB in-band) and μ_1.

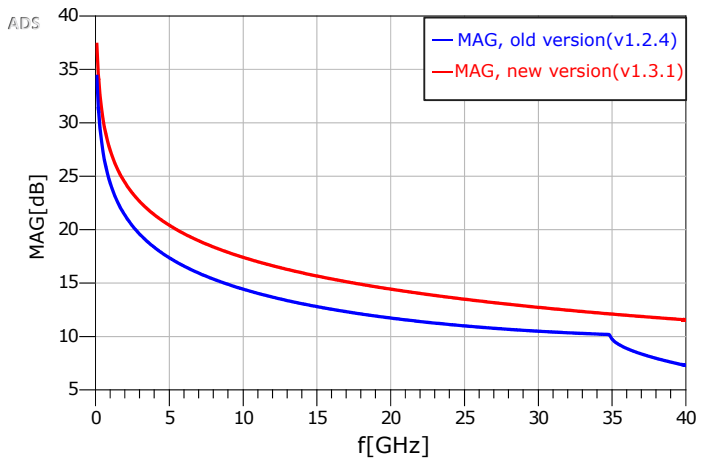

Figure 2.13: Devices MAG in the two versions, 8x100 at V_{DS}=11V , I_D=60mA/mm

Device		**17.3 GHz**		**18.8 GHz**		**20.3 GHz**	
		MAG [dB]	μ_1	**MAG [dB]**	μ_1	**MAG [dB]**	μ_1
4x50	v.1.2.4	11.75	0.449	11.4	0.482	11.1	0.513
	v.1.3.1	14.83	0.419	14.5	0.450	14.1	0.481
6x50	v.1.2.4	11.77	0.573	11.45	0.609	11.15	0.642
	v.1.3.1	14.8	0.508	14.4	0.541	14.1	0.572
8x100	v.1.2.4	12.25	0.814	11.95	0.840	11.67	0.863
	v.1.3.1	15	0.791	14.7	0.816	14.4	0.838

Table 2.2: Parameters of the MAG and μ_1 differences between the different devices, old and new PDK

2.3 Loadpull

2.3.1 Loadpull Theory

The *Loadpull* theory was introduced by S.C. Cripps in *1983* [28]. Since then it is been exploited mostly for RF and microwave power amplifier design as it indicates a proper impedance design target that is suitable to be used afterwards for the matching network design[7]. It is often used as an *a priori* design method before starting the PA design, so at first at simulation level to be then backed up by proper loadpull measurements. As for the theory in which the analysis is founded to be valid, the device should be operating in the limits of its linear region. Moreover, due to the theory supporting the loadpull operation, there should be considered that the operation is done at a single frequency and in order to have a better knowledge of the performances of the device and the matching network required over frequency more loadpull simulations/measurements sets may be required.

Assuming to be working with a Class A amplifier, the optimum output power $\mathrm{P_{OPT}}$, as in (2.11), is obtained by fixing the optimum load $\mathrm{R_{OPT}}$.

$$P_{\mathrm{OPT}} = \frac{1}{2} \cdot V_{DC} \cdot I_{DC} \tag{2.11}$$

It can be easily concluded that in order to have a certain fraction of this optimum power as P_{OPT}/p this can be obtained by either operating in backoff lowering the current swing and increasing the load to $\mathrm{R_{OPT}} \cdot p$ or by either operating with the same maximum current swing and lowering the resistive load to $\mathrm{R_{OPT}}/p$. In order to obtain the loadpull contours on the Smith Chart, then an extention has to be made. In analogy to what said before, to keep the same maximum voltage swing a shunt susceptance as in Fig. 2.14 has to be added to the load $\mathrm{R_{OPT}} \cdot p$ and (2.12) is valid, while for the other case of mantaining maximum current swing a series, introducing a series reactance to $\mathrm{R_{OPT}}/p$ as in Fig. 2.15 and checking that (2.13) is valid. In this way both upper and lower arcs have been depicted indicating the set of impedances for which the RF $P_{\mathrm{OUT}} = P_{\mathrm{OPT}}/p$. For various values of p different contours may be expressed.

$$P_{\mathrm{OPT}}/p \text{ for } -B_M < B_p < B_M \text{ where } B_M^2 = G_{\mathrm{OPT}}^2(1 - \frac{1}{p^2}) \tag{2.12}$$

$$P_{\mathrm{OPT}}/p \text{ for } -X_M < X_s < X_M \text{ where } X_M^2 = R_{\mathrm{OPT}}^2(1 - \frac{1}{p^2}) \tag{2.13}$$

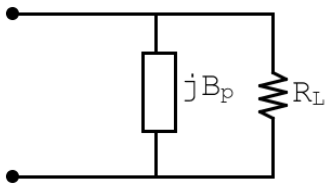

Figure 2.14: Load including shunt susceptance to obtain the extended arc of the contour for which the RF $P_{\mathrm{OUT}} = P_{\mathrm{OPT}}/p$

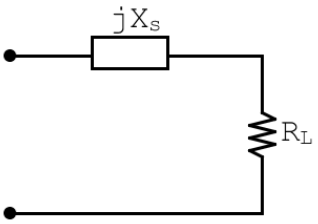

Figure 2.15: Load including series reactance to obtain the extended arc of the contour for which the RF $P_{\mathrm{OUT}} = P_{\mathrm{OPT}}/p$

2.3.2 Loadpull results

Loadpull activity results of the different amplifiers have been included in this section. The difference with respect to classical loadpull activity, in this case a comparison between the two versions of the technology, has been examined. Moreover, a further comparison with the actual measurements on the old version of the technology devices has been examined in order to have a more complete understanding of the modifications and better understand the implication on the whole DPA project.
The experimental setup schematic adopted is indicated in Fig. 2.16. The *source* of all the measurements are *courtesy* of the *Microwave Electronics Laboratory, DET Polito.*

The network analyzer is the actual core of the loadpull measurement system. The active loadpull is performed by using external amplifiers driven by the networks analyzer sources. Moreover, the active loadpull is controlled by a properly developed software.
The calibration of the whole system consists in two different phases. Initially the vector calibration is performed by actually using a onboard Thru Reflect Line (TRL) provided by the foundries standard as in Fig. 2.17 in order to automatically define the reference planes at the devices port. Following this, the second phase consists in the usage of an extended port at

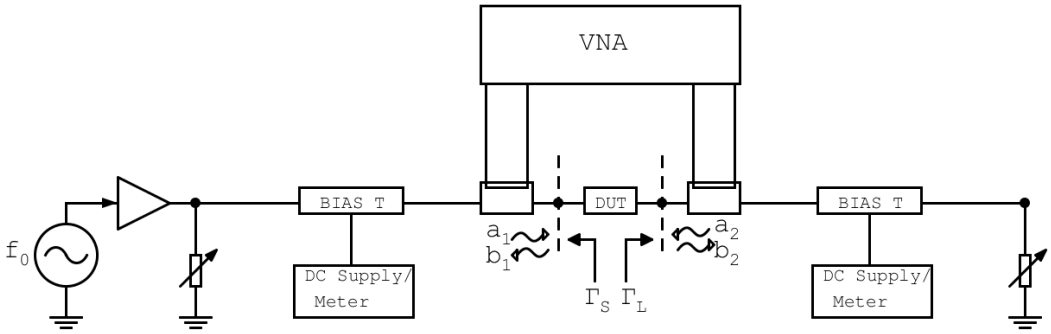

Figure 2.16: Experimental setup schematic employed

port two in order to calibrate the absolute power of the receivers and a power meter.

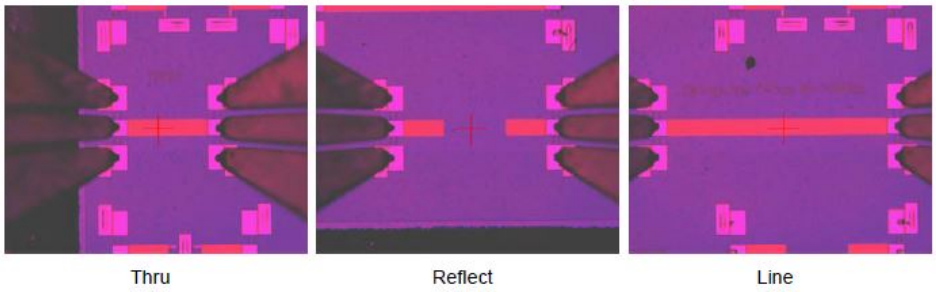

Figure 2.17: The onboard TRL standard used for the first phase of calibration

The measurements that are recalled in this section consists of measurements done on a chip sample and the characterization of the following devices : 8x100 μm, 6x50 μm, 4x50 μm. The comparison between measurements and simulation regard the characterization of a Class AB, linked to the main amplifier of the DPA with a bias set at $I_D = 60$mA/mm, $V_{DS} = 11$V and $V_{GS} = -1.6$V (related to the old bias for the chosen drain current) and $V_{GS} = -1.35$V (related to the new devices). The actual bias used in the experimental setup, differs from the wanted bias due to gate current leakage causing a voltage drop and for this the V_{GS} is set at -1.74V while V_{DS} remains unchanged.

New PDK and old PDK

The loadpull contours of the devices of the two different versions are analysed in this section. The bias is set as explained before at $V_{DS} = 11V$ and $I_D = 60mA/mm$ and the intrinsic temperature of the devices is set at 25°C. The following figures are set in two columns. On the left the loadpull contours in terms of output power have been listed, whereas in the right the loadpull contours in terms of maximum efficiency have been included. In the whole set of figures, the *GREEN* contours are product of the simulation and instead the *BLUE* are the contours derived from the measurements. The simulation results in terms of optimum load, PAE and/or η, output power are treated and expressed in the Table 2.3.

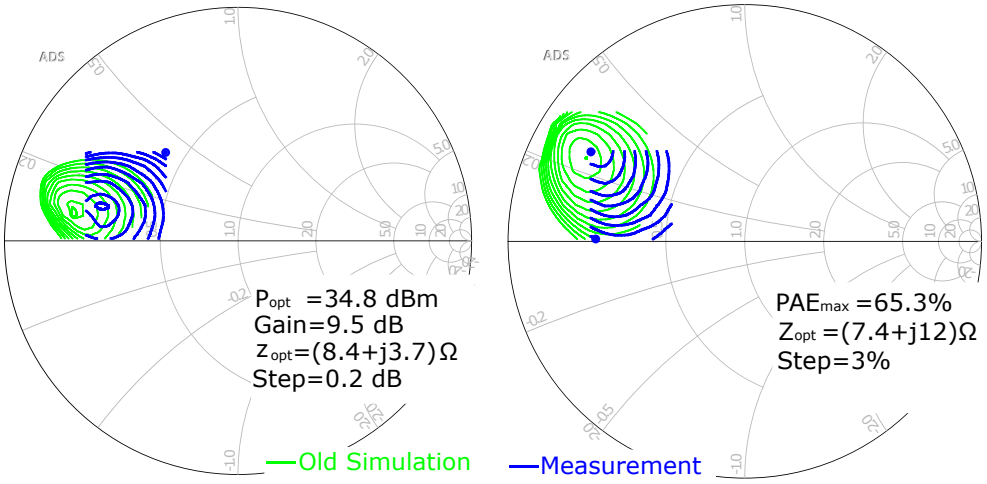

Figure 2.18: Loadpull contours of the device 8x100, old PDK, output power @0.2dB step (left) and efficiency (right) @3% step at temp. 25°C

In the following Table 2.3, a quick overview on the results obtained for the optimum output power case for both the devices of the new PDK and old PDK, as it is important to know the differences and how they may affect the next stages of the project.

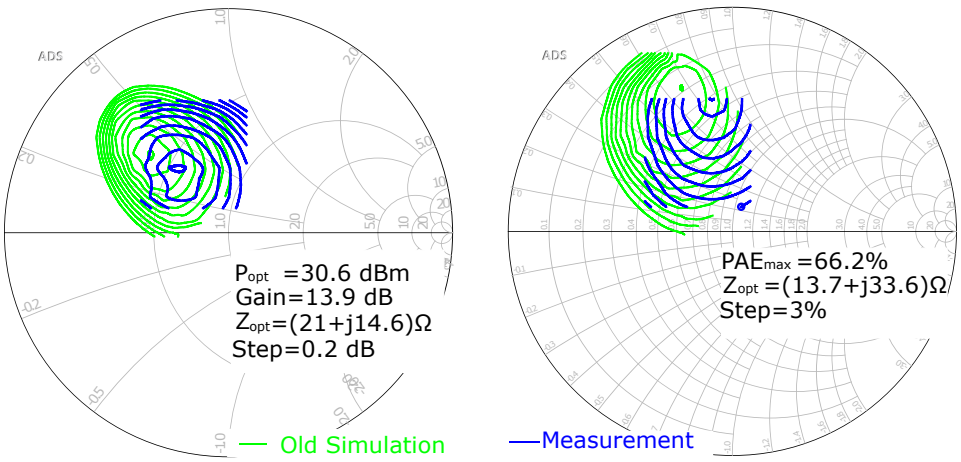

Figure 2.19: Loadpull contours of the device 6x50, old PDK, output power @0.2dB step (left) and efficiency (right) @3% step at temp. 25°C

Device		**Z_{LOAD}** [Ω]	**P_{OUT}** [dBm]	**Scaled Power** [W/mm]	**G_{OP}** [dB]	**PAE** [%]
4x50	New PDK	36+j*24	29.8	4.75	15	55.4
	Old PDK	33.8+j*24	29.0	3.975	14	54
6x50	New PDK	25+j*16.4	31.6	4.818	15.6	56.5
	Old PDK	21+j*14.6	30.6	3.833	13.9	53
8x100	New PDK	9.8+j*3.86	35.5	4.435	9.55	53
	Old PDK	8.4+j*3.7	34.8	3.775	9.5	48

Table 2.3: Loadpull results of the new PDK and old PDK devices at 25°C , VDS=11V, IDS=60mA/mm

New PDK and experimental data

In this section the simulation of the new PDK devices, are compared to the measurements done on the old devices as described in the previous section. On the left the loadpull contours in terms of output power have been listed, whereas in the right the loadpull contours in terms of maximum efficiency have been included. In the whole set of figures, the *RED* contours are product of the simulation and instead the *BLUE* are the contours derived from the measurements. The results and the comparison of the simulation and measurements, in terms of optimum load, PAE and/or η, output power are treated and expressed in the Table 2.4.

The following Fig. 2.20-2.21 regard the 8x100 μm, 6x50 μm results at temperature 25°C in the order described.

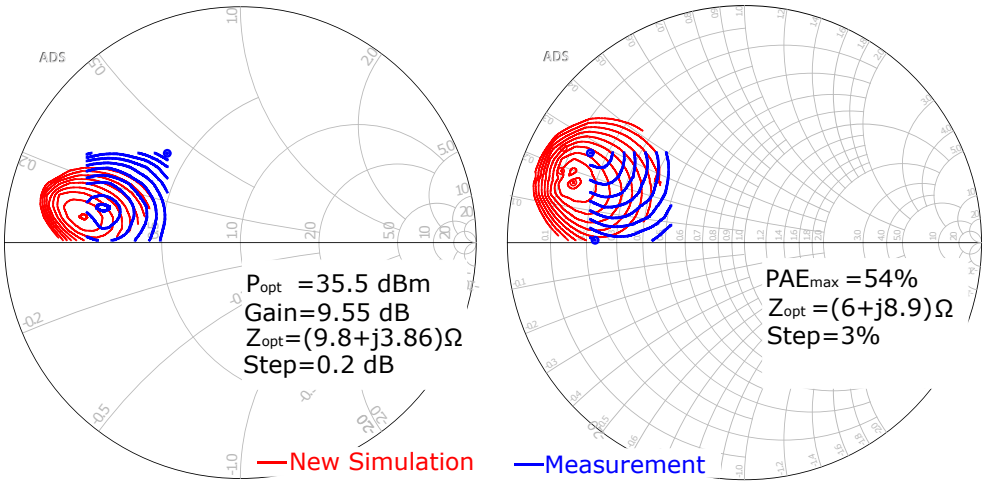

Figure 2.20: Loadpull contours of the device 8x100, output power @0.2dB step (left) and efficiency (right) @3% step at temp. 25°C

As expected, due to the already known fact that the measurements results already differ from the results of the simulation on the old PDK devices, major differences can be highlighted between the results of the devices of the new PDK in terms of output power load, the overall output power, gain and efficiency.
The trend of the decrease of the scaled output power with respect to dimensions of the devices is verified in both cases. Overall, it may be concluded that the measurements on the old devices may not be very accurate to be exploited in further stages of the project such as for example the re-design.

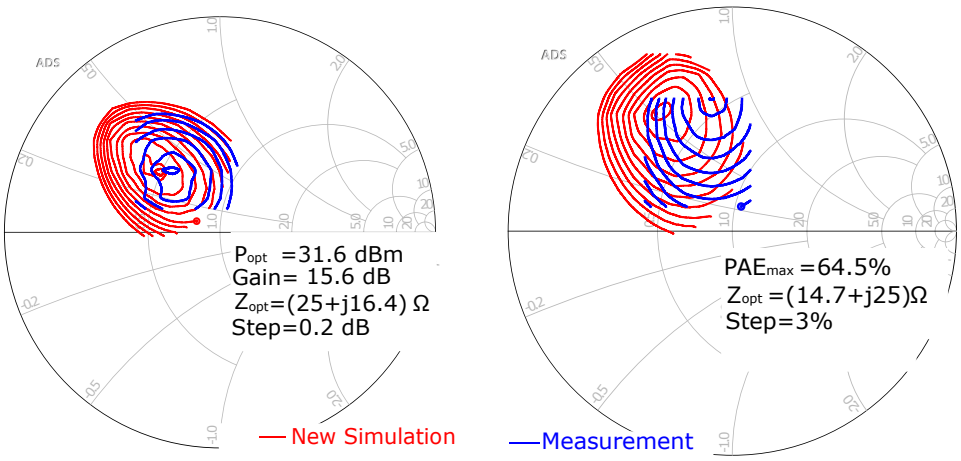

Figure 2.21: Loadpull contours of the device 6x50, output power @0.2dB step (left) and efficiency (right) @3% step at temp. 25°C

Device		**Z_{LOAD} [Ω]**	**P_{OUT} [dBm]**	**Scaled Power [W/mm]**	**G_{OP} [dB]**	**PAE [%]**
4x50	SIM	36+j*24	29.8	4.75	15	55.4
	MEAS	39+j*31	29.0	3.975	13.5	55
6x50	SIM	25+j*16.4	31.6	4.818	15.6	56.5
	MEAS	28+j*18	30.0	3.33	13.8	56
8x100	SIM	9.8+j*3.86	35.5	4.435	9.55	53
	MEAS	12+j*6	33.1	2.52	10.4	58

Table 2.4: Measured and simulated performance of the new PDK devices at 25°C

Thermal Effect

Following the same procedure, in the following Fig. 2.22 and 2.23, the loadpull contours of the 8x100 μm and 6x50 μm results at temperature 75°C in the order described are presented.
For the analysis of the degradation of the performance related to the increase of the temperature Table 2.5 has to be consulted. It is easily noticeable that there is a degradation in terms of efficiency as the temperature goes up. As for the other important parameters, there is no reported difference in terms of the optimum output load and a slight decrease in terms of output power and gain. This degradation of the efficiency may be considered negligible as long as the differences of the other parameters do not indicate that the DPA may suffer from potential performance issues or faults due to thermal effects.

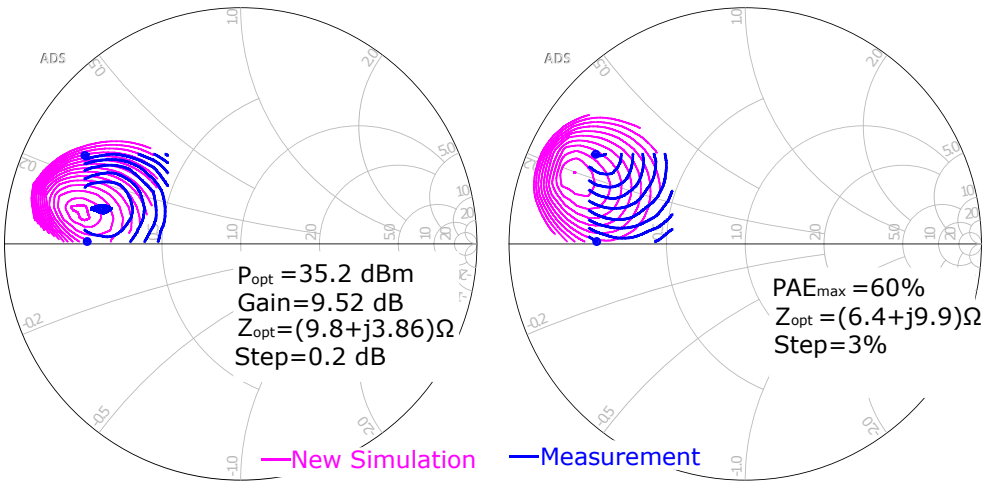

Figure 2.22: Loadpull contours of the device 8x100, output power @0.2dB step (left) and efficiency (right) @3% step at temp. 75°C

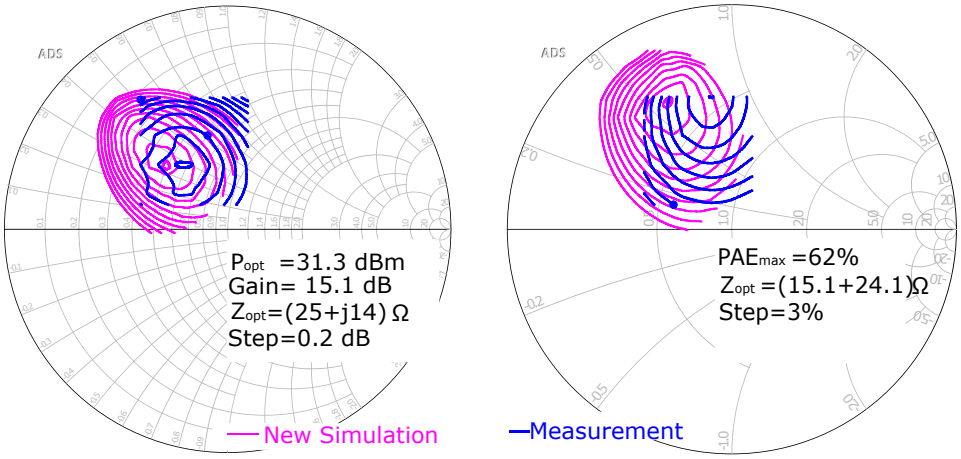

Figure 2.23: Loadpull contours of the device 6x50, output power @0.2dB step (left) and efficiency (right) @3% step at temp. 75°C

Device		**Z_{LOAD} [Ω]**	**P_{OUT} [dBm]**	**Scaled Power [W/mm]**	**G_{OP} [dB]**	**PAE [%]**
4x50	25°C	36+j*24	29.8	4.75	15	55.4
	75°C	30+j*29.7	29.3	3.975	14.5	57
6x50	25°C	25+j*16.4	31.6	4.818	15.6	56.5
	75°C	25+j*16.4	31.3	4.5	15.1	55
8x100	25°C	9.8+j*3.86	35.5	4.435	9.55	53.5
	75°C	9.8+j*3.86	35.2	4.14	9.52	51.6

Table 2.5: Simulation results and performance of the new PDK devices at 25°C and 75°C

Chapter 3

Re-design activity

The re-design activity starting by how the RUN1 project behaves including the new active devices has been presented and examined. A description of how some of the various DPA functional blocks had to be re-designed in order to comply to the requirements of the overall DPA's project is also presented.

The *electromagnetic* (EM) simulations of some of the circuits components (e.g. capacitors and via holes) of the project have been used in order to have a more realistic behaviour of the active devices and their performance when inserted in the bigger picture of the entire project layout. The EM simulator used is the Keysight ADS *Momentum* (simulation in microwave mode). The EM setup includes the foundry substrate used for the whole project (Si stack). This aspect is important when working with center band frequencies of the order of 18.8 GHz which are high enough. At those frequencies the behaviour of all the actual components included (even passive) are expected to be different with respect to the lumped elements that are usually used on the initial design stage of a power amplifier.

3.1 Stabilization network

As described in Chapter 2, the active devices of the two versions present different performance results in terms of MAG and $\mu 1$. In Fig. 3.1 and 3.8 are shown the layouts of the actual stabilization networks layout. One of the major differences with respect to the ideal stability network introduced is that now the stabilization network integrates both the classic stabilization network (the RL block's) behaviour with the gate bias network.

EM simulations require high computational effort and it has been decided to work on a more intermediate level by introducing the real component models (of the new PDK) that describe better then lumped elements the majority of the components of the networks. The most critical parts of the design such as the support of the RC parallel block in series at the input of the device have been EM simulated and the actual scattering parameters obtained from them are adopted to simulate the rest of the circuit such as in Fig. 3.3. Moreover, the first capacitor to ground, where the ground connection is implemented by the via hole, is critical to guarantee proper separation of the DC bias path from the RF path. Therefore it has been chosen to tune its value as a first step and to replace its circuit model with its scattering parameters obtained from EM simulation, which are more accurate, in all successive simulations. The results are presented in the following analysis.

3.1.1 Analysis of performance and synthesis

8x100 μm device

The layout of the existing stabilization and bias network for the 8x100 μm device is presented in Fig. 3.1
As a result of RUN1 this whole structure built on PDK v1.2.4 has been EM simulated and the actual results have been exploited in order to understand the active devices behaviour. As expected due to the already made considerations, in Fig. 3.2 it is presented the actual proof that the existing network is not able to stabilize the device in and out of band, more precisely not stable in the [17.6;34] GHz.

The present layout has been translated back into the circuit schematic level by using the new PDK components. In the following Fig. 3.3 the schematic of the stabilization network is presented, missing the RC parallel block and

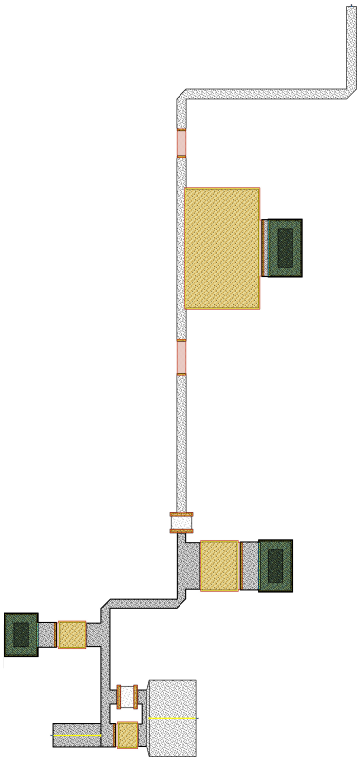

Figure 3.1: Layout of the actual stabilization network on the new PDK, 8x100

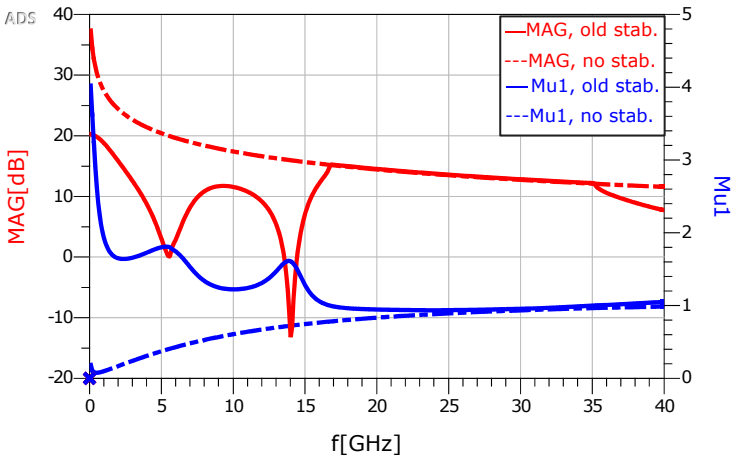

Figure 3.2: Results of the simulation of the active device new PDK, 8x100 and stabilization network on old PDK

it's interconnecting lines. No actual bending of the transmission lines has been inserted at this level. While dealing with the bias network, an eventual bending of a transmission line may be tolerated, although the same

reasoning cannot be accepted while designing a matching network.

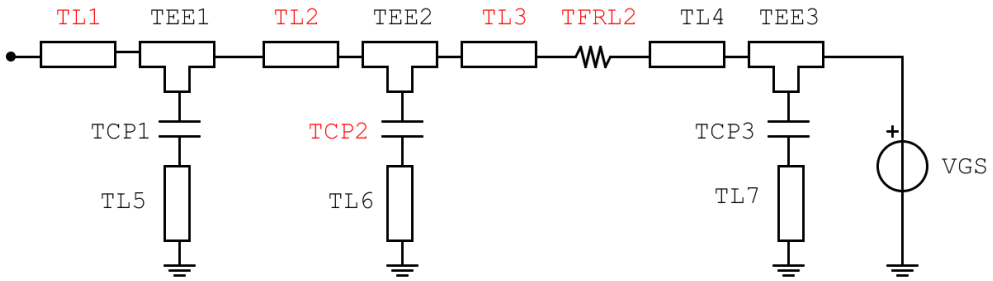

Figure 3.3: The schematic translation of the old PDK layout, 8x100, shunt part of the stabilization network

The first capacitor-via hole branch is built in the new PDK and afterwards replaced by its scattering parameter 2 port. Its behaviour on the new PDK results to be correct at simulation level (Z=0.015+j4.7 Ω) marked at 18.8GHz) as in Fig. 3.4. No major parameter tweaking has been done in the latter part described, since its function is to decouple DC and RF paths at frequencies lower than the operating band, and therefore the precise value of the components is not critical, as long as the various capacitors to ground provide a low impedance for the RF signal.

Another critical part which has been chosen to be inserted in terms of scattering impedance in this analysis and re-designing have been the interconnecting lines of the RC parallel block represented as in the relative layout, Fig. 3.5 (actual ports used in the following steps are shown).

The re-design stage in the case of the 8x100 μm has been done at a schematic layer, meaning that the full network could only be modified by tweaking the parameter values of the various components whose circuit model was present in the schematic, and leaving fixed the portions already replaced by their EM simulated scattering parameters, in order to reach the stabilization of both in-band and out-of-band of the device.
In Fig. 3.6 the MAG and μ1 of the device after the modifications has been presented. In this figure the trend of the change of the behaviour by tweaking of the most critical components is shown. The modified parameters are included in Table 3.1. The components in *RED* in Fig. 3.3 are tweaked parameters also shown in the Table 3.1. The transmission line TL1 is not presented in the figure, but is the line connecting the whole branch with the input while TFRL1 and TCP1 are the values of the RC parallel at the

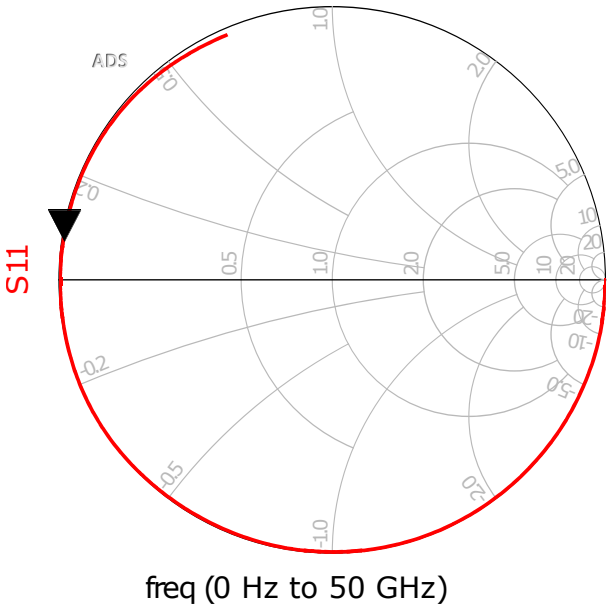

Figure 3.4: Scattering parameter S(1,1) of the C1-VIA HOLE simulation

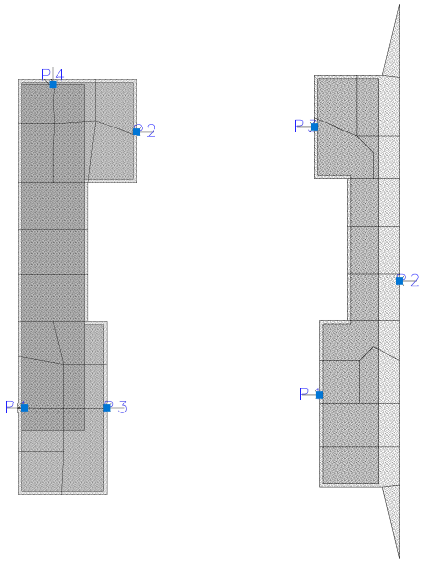

Figure 3.5: Layout of the interconnecting lines of RC parallel block, new PDK, 8x100

input of the device.

The resistance of the RC parallel block (TFRL1) in series at the input has an immediate effect at the third positive peak of the MAG (marker 1), increasing it by increasing the R parameter. The other important resistance that affects the positive peak at low frequencies (marker 2) is the

Component	**Parameter**	**Old PDK**	**New PDK**
TL1	Length[μm]	90	116
TL2	Length[μm]	80	144
TL3	Length[μm]	20	35
TCP1	C value[pF]	Not Available	0.576
TCP2	C value[pF]	2.1	3.84
TCP3	C value[pF]	15	15
TFRL1	R value[Ω]	Not Available	71
TFRL2	R value[Ω]	25	25.5

Table 3.1: Stabilization network components and their relative parameters modified after the re-design, 8x100

TFRL2, integrated in the bias network, even though its effect is inverse, meaning the peak is lowered by increasing this resistance value.

The length of the two transmission lines TL1 and TL2 modify the position of the second negative peak of MAG (marker 3), shifting it to lower frequencies by increasing the relative lengths.
As for the first negative peak (marker 4), it is shifted to higher frequencies by lowering the value of the capacitors value TCP2. The capacitor of the RC parallel block at the input instead shifts the whole band of interest and the nearby peaks to higher values by increasing its value.

In Fig. 3.7 a close look in-band of the final results is presented including even the results of the active devices without a stabilization network. The centerband MAG has a value of 14.3 dB corresponding to a μ1 of 1.002 followed by a MAG at 17.3 GHz of 14.2 dB and at 20.3 GHz of 13.96 dB.

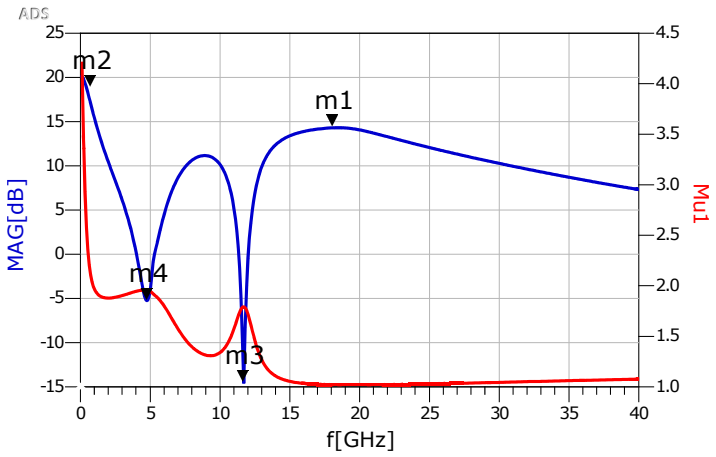

Figure 3.6: MAG and $\mu 1$ of the 8x100 after the re-design

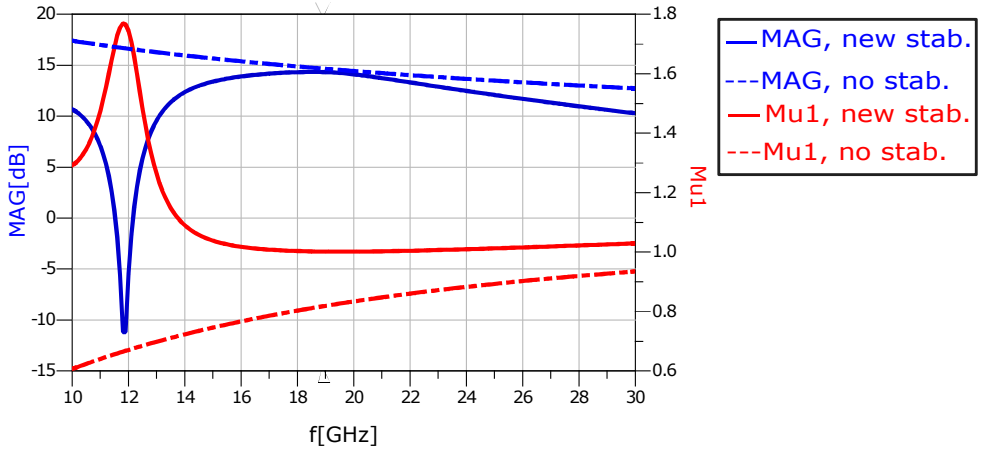

Figure 3.7: MAG and $\mu 1$ in-band of the 8x100 after (solid) and before (dashed) of the re-design

6x50 μm device

The same procedure adopted for the 8x100 μm device has been applied to the 6x50 μm. In Fig. 3.8 the layout of the actual stabilization network is presented and in the following Fig. the schematic 'translation' of it. As in the previous case some of the critical components of the whole schematic have been undergoing the EM simulations and their actual scattering parameters are used in order to stabilize and find the proper RC values.

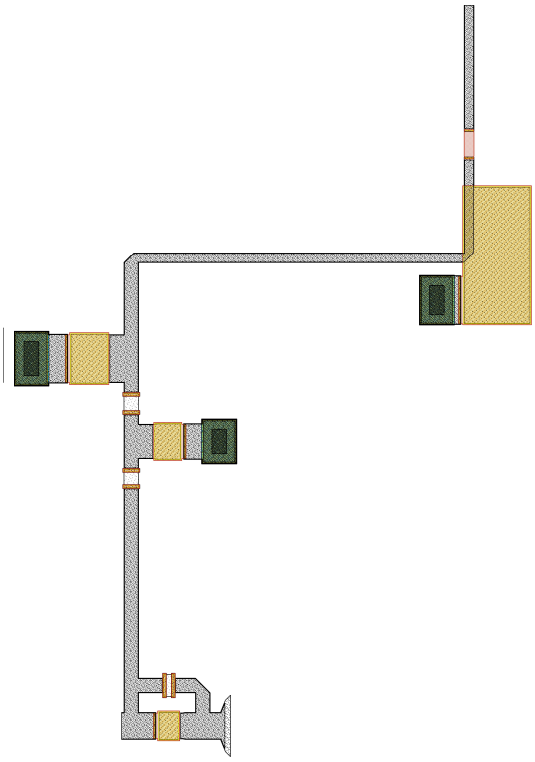

Figure 3.8: Layout of the actual stabilization network of the new PDK, 6x50

As for the first branch of capacitor-via hole, no tweaking with respect to the previous old PDK has been used as when translated in the new PDK, the performance did not require extra modifications.

The main difference with the previous case of this stabilization network is that, the μ1 of the device implemented with the imported network presents two negative peaks around the high positive peak as in Fig. 3.10. It becomes impossible to find a combination of the default given components parameters that is able to soften the difference between the peaks and si-

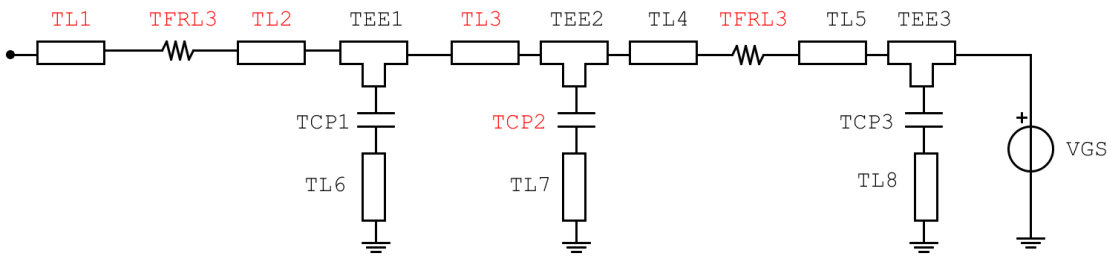

Figure 3.9: The schematic translation of the old PDK layout, 6x50, shunt part of the stabilization network

multaneously make $\mu 1$ greater than 0 dB. What this means is that it is impossible to make it stable both in-band and out-of-band with the stabilization network used.

As a consequence a modification of the RC parallel block is found to be the only way to reach stability both in and out of band. The modification is done as in Fig. 3.11, by actually adding a small resistance in series with the capacitor, and as verified it does not have a noticeable not wanted effect on the gain of the device.

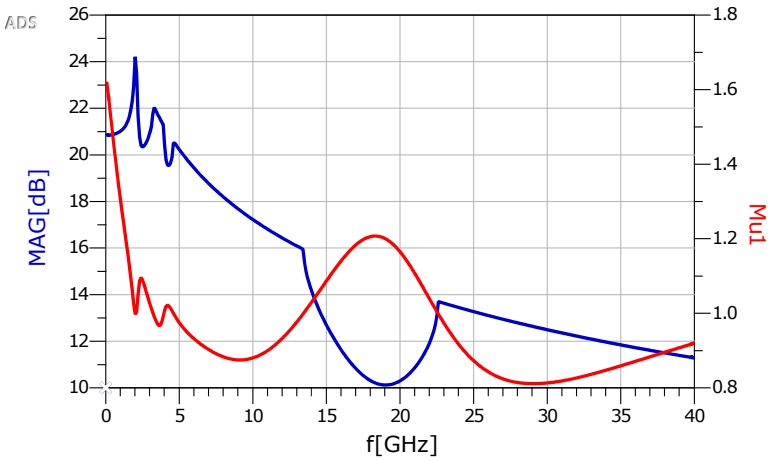

Figure 3.10: Starting MAG and $\mu 1$ of the 6x50 device implementing the stabilization network built on the old PDK

In Fig. 3.12 the final behaviour of the device with the re-designed stabilization network is shown. The added resistance in series with the capacitor increases the in-band and higher frequencies slope (marker 1) when decreasing. As for the other resistance in parallel it decreases mainly the

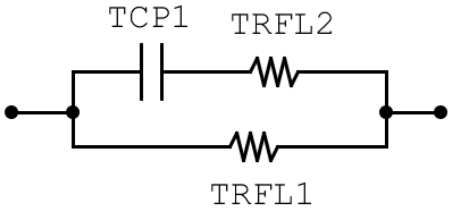

Figure 3.11: Modification of the RC block in the case of the 6x50 device's stabilization network

negative peak at marker 2 while increasing, but also it implies around this frequencies a vertical shift on the MAG.

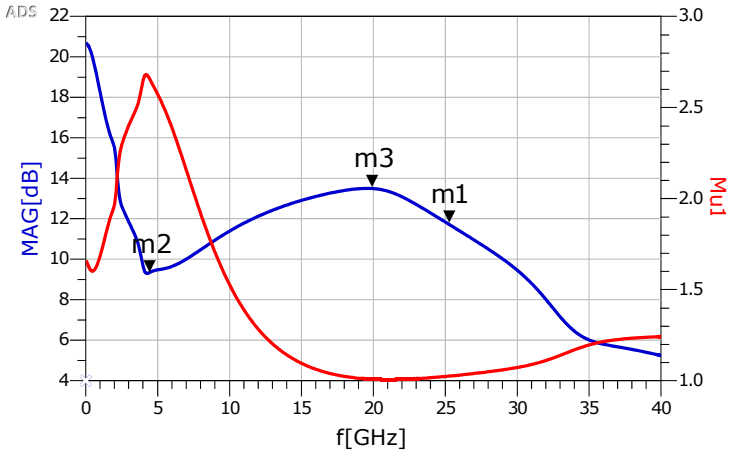

Figure 3.12: MAG and $\mu 1$ of the 6x50 of the re-design

The positive peak of interest of the MAG was managed to be centered in-band by tweaking the lengths of the first two transmission lines connected at the input of the bias/stabilization network and by properly setting the capacitor at the input. More specifically, by increasing both the lengths of the transmission lines we have a shift towards the lower frequencies of the peak (marker 3), whereas the effect of the length of the closest transmission line to the input is higher. The capacitor is mainly responsible for the vertical shifts of the peak.

A closer look of the MAG reached in-band is shown in Fig. 3.13. The MAG in centerband is equal to 13.47dB at $\mu 1$ at 1.015 followed by MAG at 20.30 GHz of 13.4 dB and 13.8 dB at 17.30 GHz. The behaviour is

close to compensating the f^{-1} behaviour of the MAG. The gain reduction is contained in the range 0.9 $\pm$ 0.5 dB with respect to the case without stabilization network (in *BLUE*).

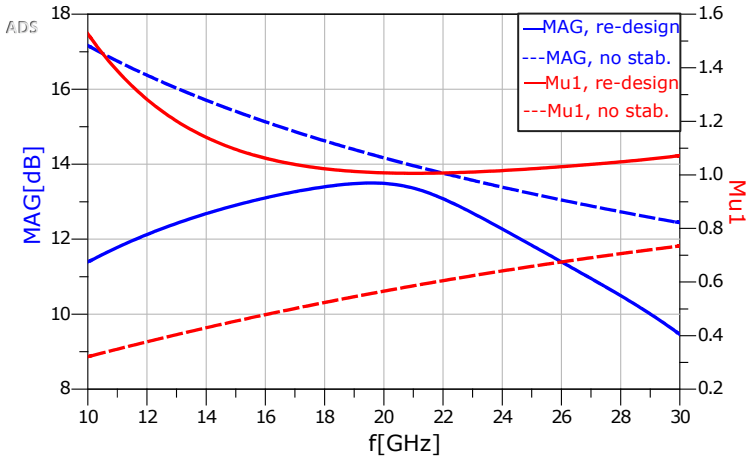

Figure 3.13: MAG and $\mu 1$ in-band of the 6x50 after (solid) and before (dashed) of the re-design

The critical components whose values have been modified are shown in *RED* in Fig. 3.3. The overall overview of how the components have changed is shown in Table 3.2. Although not indicated in the table, as the parameters are not shown in the schematics, the length of the transmission lines of the interconnection between the device's gate and the RC//C block has been increased for layout purposes, i.e. to accommodate the resistor that has been added in the CR//C block, whose value is very low and therefore its width is very high.

Component	**Parameter**	**Old PDK**	**New PDK**
TL1	Length[μm]	391	1230
TL2	Length[μm]	20	298
TL3	Length[μm]	35	20
TCP1	C value[pF]	Not Available	0.452
TCP2	C value[pF]	2.1	2
TCP3	C value[pF]	15	15
TFRL1	R value[Ω]	Not Available	85.5
TFRL2	R value[Ω]	-	4.16
TFRL3	R value[Ω]	33.75	30.77

Table 3.2: The update of the general components parameters after the re-design, stabilization network

The Via Hole Effect

In all the networks that have been introduced until now the via-hole model has been used. Ideally the actual via-hole behaves as a short circuit and an inductance as the model used in the previous stage. In Fig. 3.14 the actual EM simulations and the measurements of the via-holes of the technology is presented.

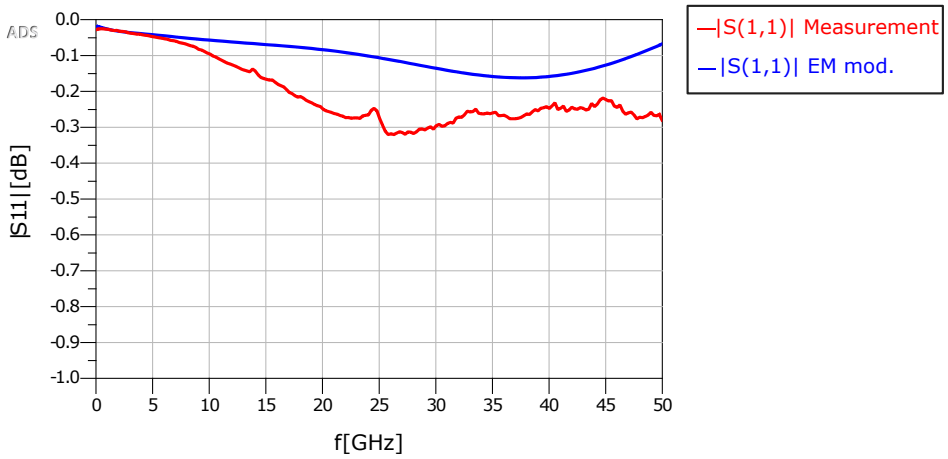

Figure 3.14: Scattering parameter S(1,1), of the EM model (red) and measured (blue) via-hole

The actual behaviour of the via holes makes the performances of the amplifiers degrade significantly due to this far from ideal behaviour. In Fig. 3.16 the MAG examined with the previous stabilization network, 8x100 μm, with the ideal via-holes is depicted in the *BLUE* curve while in *RED* the same stabilization network but with the via-holes replaced with the EM models. It is easily verified that the MAG drops by at least 5 dB in the bandwidth. These effects on the stabilization networks have to be controlled. In the following stages, a modified stabilization network, with the embedded EM models of the via holes, for the 8x100 μm amplifier has been exploited.

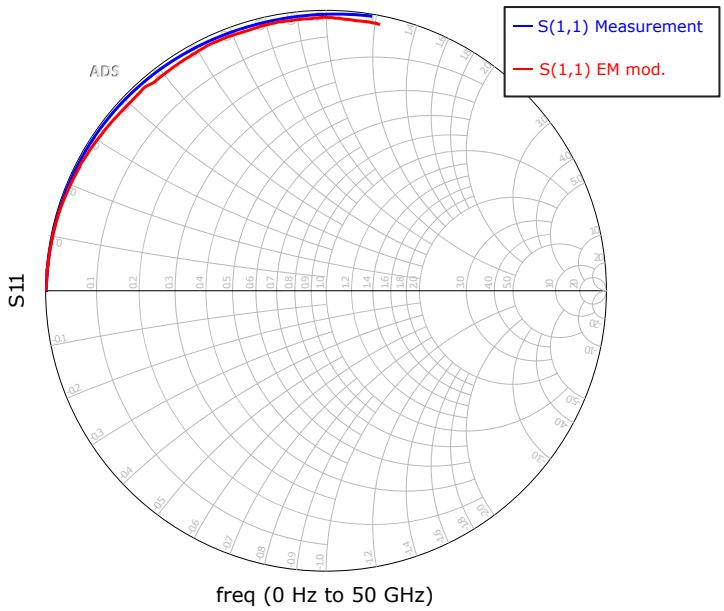

Figure 3.15: Scattering parameter S(1,1), of the EM model (red) and measured (blue) via-hole from 0 Hz to 50 GHz

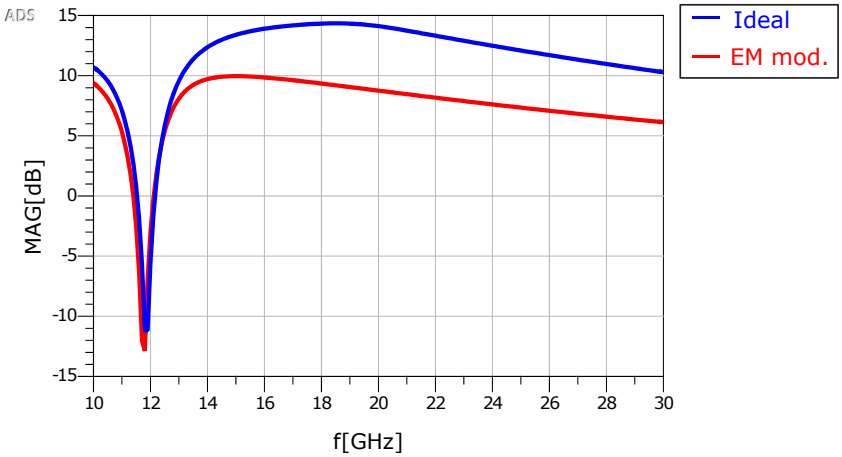

Figure 3.16: MAG and $\mu 1$ in-band of the amplifier, in *BLUE* stab. network with ideal via-hole, in *RED* stab. network with EM model parameters of the via-hole

3.2 Output Combiner

The output combiner introduced in the first chapter has been designed for the DPA where both the main and the auxiliary amplifiers chosen are the OMMIC 8x100 μm. In the design of the output combiner, the values of the output parasitics $C_{OUT} = 471fF$ and $L_{OUT} = 23nH$ extracted, are taken into account. The basic scheme has been slightly modified to the one in 3.17. The actual layout of the output combiner is presented in Fig. 3.18. It is common in practical implementations that the inductances present in the output combiner are replaced by short transmission lines. This technique is also known as the semi-lumped equivalent network. The is the first modification of the output combiner scheme with respect to the ideal network, where the inductances are replaced by the transmission lines TL1, Tl2 and TL5. A second modification with respect to the initial Two-Section Peaking network introduced consists in replacing the sets of two capacitors in parallel by the capacitors TCP1 and TCP2.

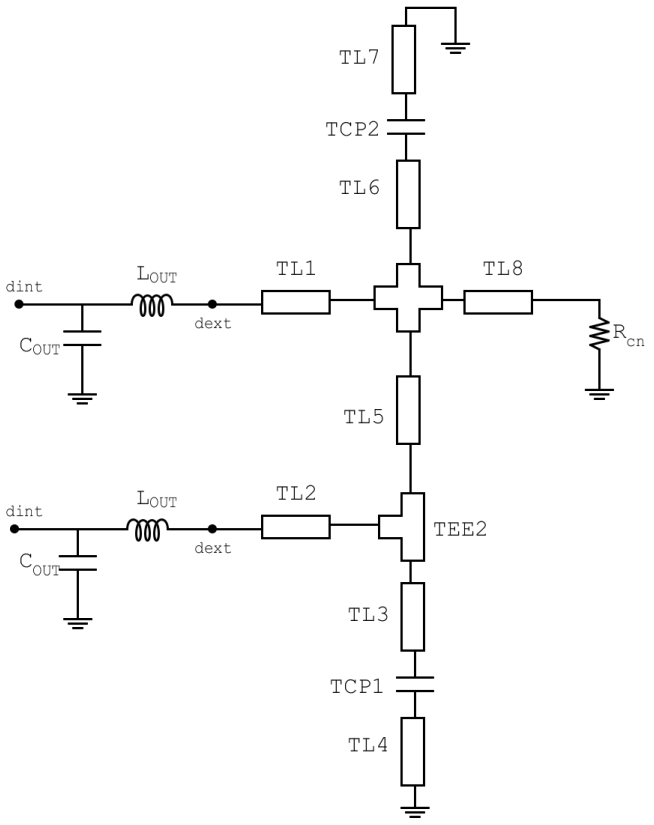

Figure 3.17: Schematic of the output combiner of the DPA

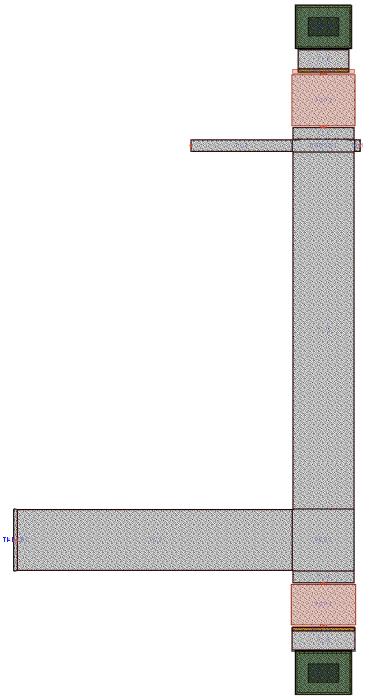

Figure 3.18: Layout of the output combiner network of the new PDK, 8x100

The values of the mentioned capacitors and also the lengths of the transmission lines have been tweaked with respect to the initial values. The parameters have been modified so that the network works as close as possible to the ideal behaviour in the entire band. The design goals of the network have been chosen so that the real part of the impedances of both the main and auxiliary amplifier at saturation (R_{OPT}) and backoff ($2R_{OPT}$) are satisfied. More precisely, the goals chosen for the design consist in the difference between the real parts of the impedances at main and auxiliary amplifier with the ideal values is less than -20 dB. The R_{cn} used in this stage is evaluated through equation (1.23) and it is equal to 11.2 Ω.

Considering the limitations in terms of number of tweakable parameters and the large bandwidth of 3 GHz, a relaxation in terms of the previous goal designs was decided to be done at the higher end of the band. This relaxation leads to non ideal values of the real part of the impedances in saturation and backoff at these frequencies that are afterwards translated in poor performance in terms of various figure of merits of the DPA. From the load modulation, shown in Fig. 3.19, it is verified that the real part

of the load impedance of the main amplifier starts at $2R_{OPT}$ and reach R_{OPT} at saturation. As for the auxiliary amplifier which is turned off initially (open circuit), starts working and afterwards the real part of the impedance at saturation reaches R_{OPT} at saturation as expected. The non ideal behaviour of the imaginary parts of the impedances have also been neglected due to the relaxation of the design goals.

As mentioned before, from checking the efficiency in Fig. 3.20, a drop from the expected values of the DPA is verified. The efficiency curve depicted in *RED* is the correspondent of the efficiency curve at center-band, while the efficiency at 17.3 GHz and 20.3 GHz are represented by the dashed curves in *BLUE* and *GREEN* respectively. At the upper frequencies the efficiency drops due to the motivated reasons above.

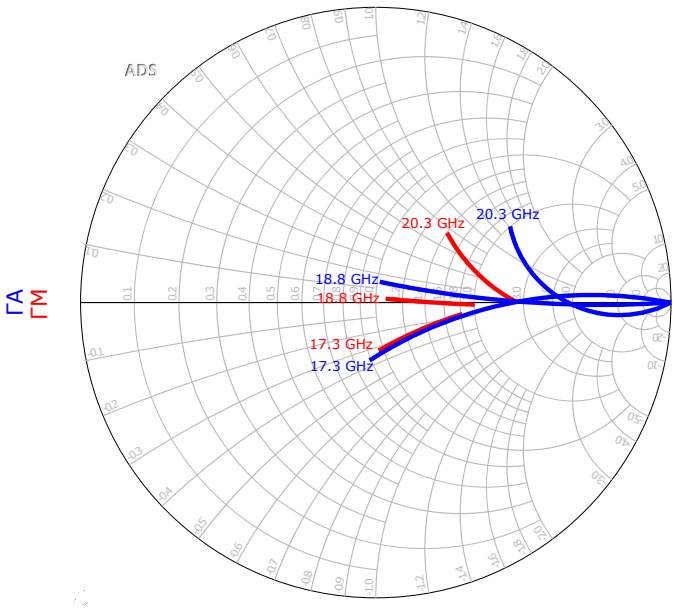

Figure 3.19: Main and auxiliary load modulations after applying the designed output combiner at 17.3 GHz, 18.8 GHz and 20.3 GHz

In the following table the update of the components parameters after the re-design has been shown.

Post Matching Network

The *Post Matching Network* (PMN) architecture implemented is a real to real impedance matching network at the output node that transforms the

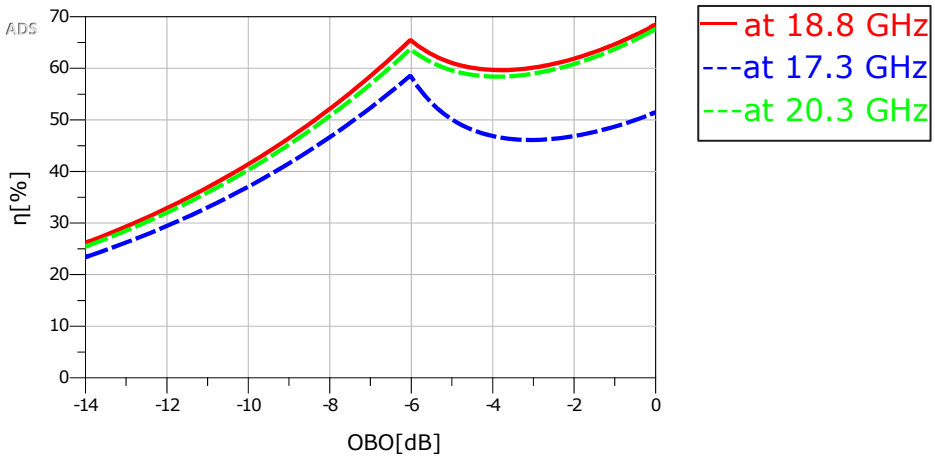

Figure 3.20: Efficiency of the DPA after applying the designed output combiner, RED η at 18.8 GHz, BLUE η at 17.3 GHz, GREEN η at 20.3 GHz

Component	**Parameter**	**Old PDK**	**New PDK**
TL1	Length[μm]	220	165
TL2	Length[μm]	429	450
TL5	Length[μm]	395	585
TCP1	C value[fF]	285	340
TCP2	C value[fF]	377	420

Table 3.3: The update of the general components parameters after the re-design, output combiner

output load to the conventional 50Ω load resistance. The schematic of the distributed matching network architecture is shown in Fig. 3.21 and its design is based on the technique described in [29]. The schematic includes the bias network at the output, for that reason there is a capacitor TCP3 at the output as the DC block and the TCP1-via hole shorting any signal preventing it from reaching the bias generator. The components values have been slightly modified with respect to the parameters of the PMN components built on PDK v1.2.4. The length of the TL4 is excessive and as can be checked in the actual layout generated (Fig. 3.22), additional bending of the transmission line have been introduced in order to reduce the overall space occupied from this section of the DPA.

The input reflection coefficient throughout the entire band is less then -23 dB with two negative peaks at the bands limits, as can be verified from Fig. 3.23. With this architecture the main limitations of the bandwidth

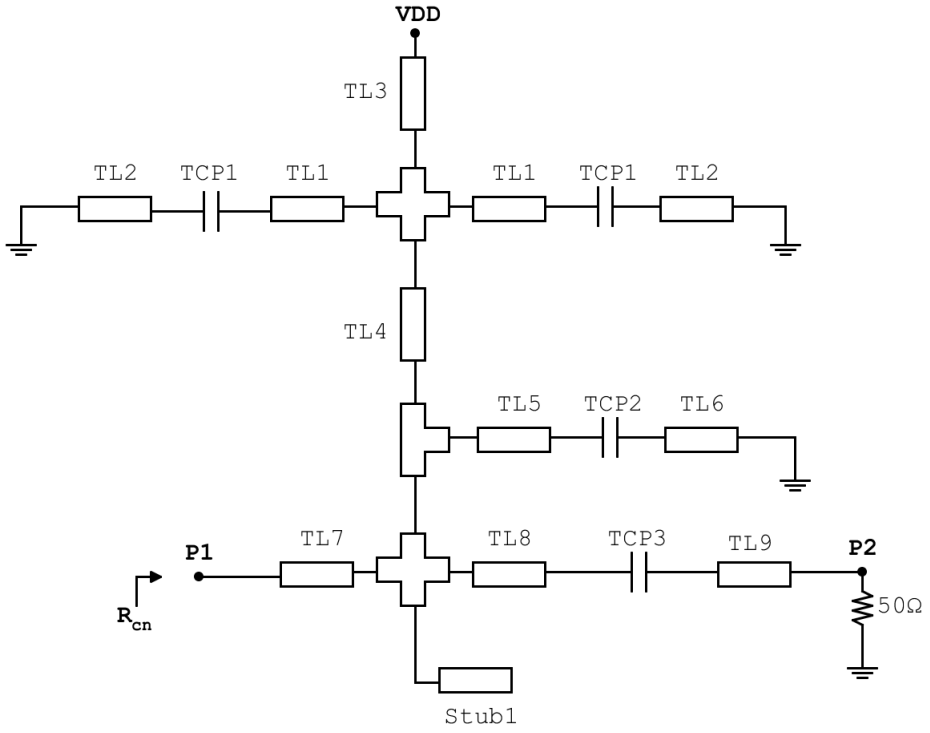

Figure 3.21: Schematic of the post matching network at the output of the DPA

of the output of the DPA have been covered. In addition to the matching requirements, the PMN components values have been affected even by design goals introduced for the limiting of the losses on the network. The results are translated into S(2,1) values of the PMN reasonably close to 0 dB, between -0.6 dB and -0.75 dB.

3.3 Complete DPA final stage

The last step involves putting together all the examined and designed components as in Fig. 3.24 to complete the DPA final stage. The schematic includes ideal *Input Matching Networks* (IMN). The ideal IMNs consisting in a transmission line and a stub have been used in this stage and more complex solutions have been avoided as in following developments of the project they are to be replaced by proper interstage matching networks. As already mentioned, for this DPA it was chosen to proceed with the 8x100 μm transistors for both the main amplifier and auxiliary amplifier.

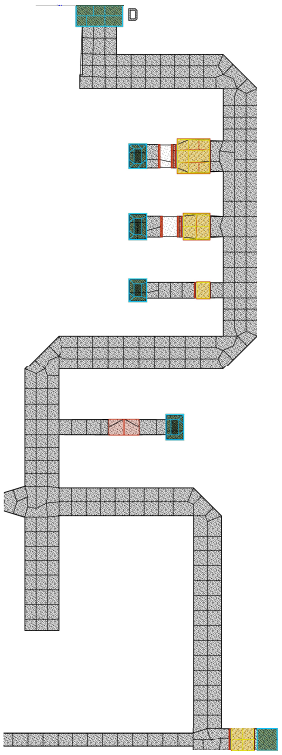

Figure 3.22: Layout of the PMN on the new PDK, 8x100

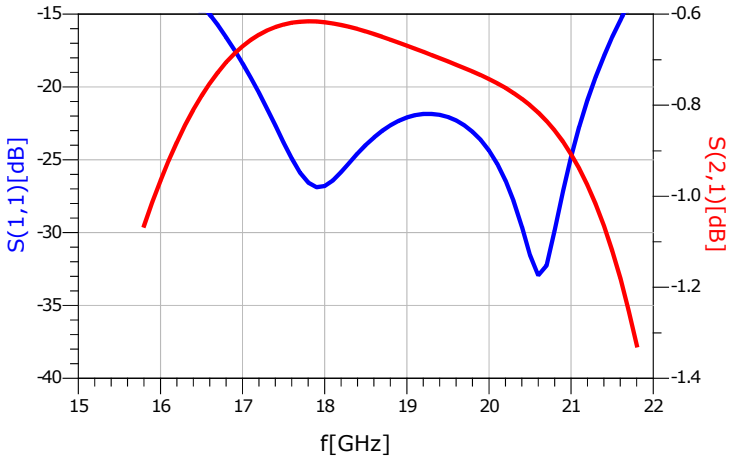

Figure 3.23: Main scattering parameters of the PMN network matching R_{cn} to 50Ω

The main amplifier is chosen to be in class AB, I_D=60mA/mm (V_{GS}=-1.35V) and V_{DS}=11V while the auxiliary amplifier in Class C, V_{GS}=-6.5V and V_{DS}=11V for the targeted 6 dB OBO DPA. The two transistors now

operate at different bias translating in different drain current profiles, gains and input/output impedances leading to additional performance issues. A technique chosen for the DPA in order to limit these issues and their mitigation was the *uneven input-power splitting*. An ideal two way power splitter has been used, dividing the power as below:

$$K = \frac{P_{MAIN}}{P_{AUX}} = 1.8 \tag{3.1}$$

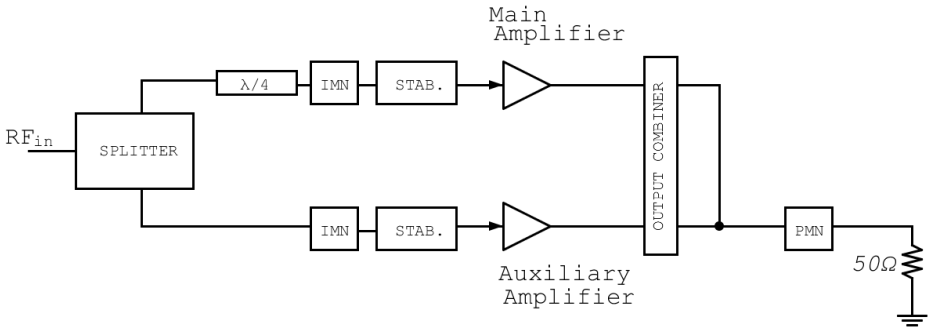

Figure 3.24: Final Single Stage DPA schematic with 8x100 for both main and auxiliary amplifiers

With the implementation of all the examined components to the DPA, non ideal conditions and not negligible losses within the components have been introduced. The performance of the final DPA simulated drops significantly with respect to the idealized performance of the ideal DPA initially introduced. In the graph in Fig. 3.25, the main figure of merits for the DPA, $P_{OUT} - P_{IN}$, G_{OP} and η at the centerband frequency of the design, 18.8 GHz, have been shown. An immediate feature of the final DPA designed to be noticed is the linearity achieved. The -1 dB compression point begins at circa input power 34 dBm. As expected the efficiency has a significant drop with respect to the ideal behaviour of the efficiency of the DPA and the η from breakpoint to saturation is at 45% ±1.5%. The operational gain instead is evaluated to be 4.5 dB ± 0.55 dB.

In the Fig. 3.26, the actual load modulation of the DPA at the centerband frequency has been shown. The difference with the ideal behaviour is noticeable as the real part of the load is properly modulated while the imaginary part is not. This is related also due to the nonlinear effects related also the introduction of the uneven input splitter and the fact that the auxiliary amplifier is in Class C, differently from the main amplifier.

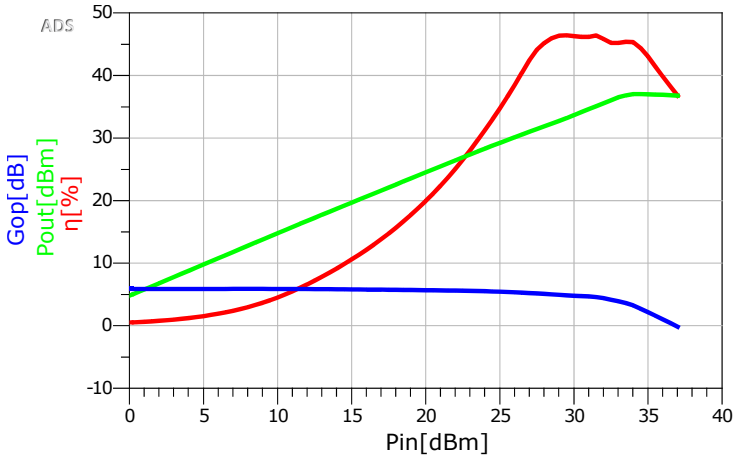

Figure 3.25: Final Single Stage DPA figures-of-merit at 18.8 GHz

The parasitic capacitance C_{GD} is sensitive to this modifications. Through Miller effect it is concluded that the C_{GD} modifies the C_{OUT} used in the design stage, meaning that the output combiner and the following parameters and components may be still be optimized.

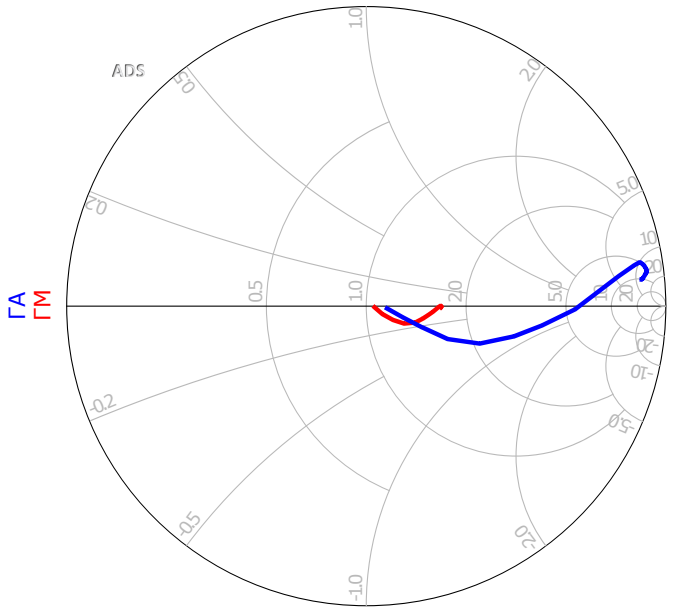

Figure 3.26: Main and auxiliary load modulations final DPA at 18.8 GHz

Another important aspect that has been verified is the behaviour of the DPA in the frequency band from 17.3 GHz to 20.3 GHz with a 0.5 GHz step. In Fig. 3.27 and 3.28, the efficiency and the operational gain have

been evaluated in various frequencies. The efficiency in the whole band is evaluated at 45% ±1.5% while the operational gain 4.5 dB ± 0.55 dB. It can be concluded that these parameters do not vary extensively in the whole band.

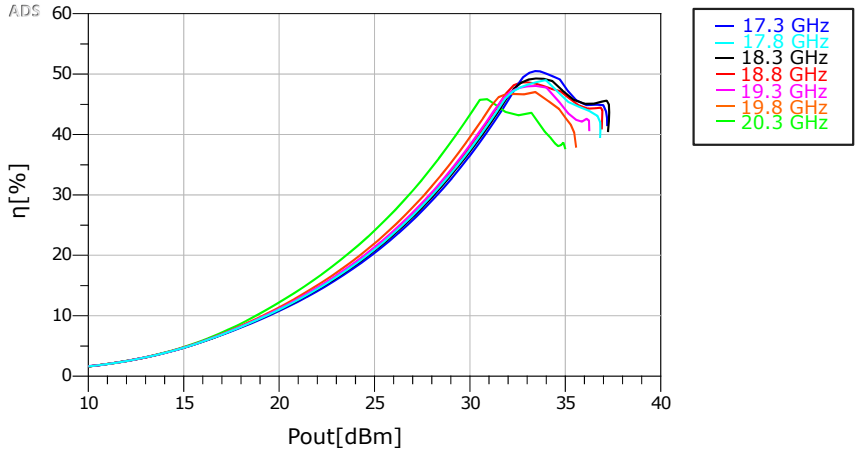

Figure 3.27: Final Single Stage DPA efficiency η in the frequency band

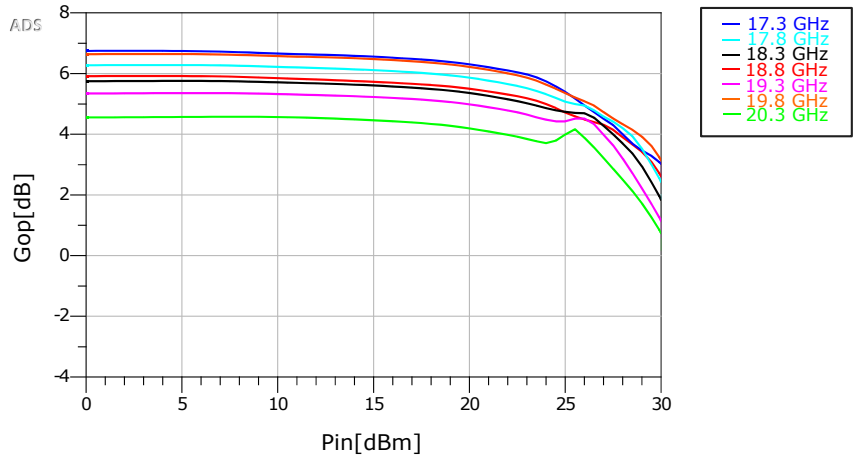

Figure 3.28: Final Single Stage DPA operational gain G_{OP} in the frequency band from 17.3 GHz to 20.3 GHz with a 0.5 GHz step.

Chapter 4

Conclusions

In this thesis, the re-design of the most critical components of a MMIC Doherty Power Amplifier in Ka-band has been presented.

The choice of the commercial GaN on Si HEMT process of OMMIC for the implementation of the MMIC results suitable for the application, as it combines a series of good features like the high output power density at high frequencies, the good thermal conductivity of the Si (in comparison to GaAs for example) and the favorable impedance levels, all factors concurring to successfully achieve with the amplifier the desired wideband operations.

In particular, the thesis has been focused on the assessment of the new process development kit of the OMMIC MMIC process, recently released. The redesign of some of the main building blocks of the amplifier, namely the stabilization networks of the power devices, the Doherty output combiner and the post-matching network has been carried out by detailed comparison one-by-one of the performance of the redesigned blocks simulated with the old and new PDKs.

Thanks to the feedback from the experimental characterization of the first run DPAs and to the updated PDK these key elements of the entire architecture have been readapted, correcting some issues related to stability and improper load modulation occurred in the first design due to shifts and model inaccuracy.

The thesis has permitted to the candidate to explore the different tools of the high frequency design, spanning from the circuit level equivalent circuit of nonlinear active devices to the electromagnetic simulations with

advances FEM-based CAD tools of complex passive structures.

A complete single DPA stage, useful as intermediate benchmark for the assessment of the performance of the redesigned DPA has completed the work giving to the candidate the picture of a complete DPA design in MMIC.

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