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Design and characterisation of a GC-eDRAM memory array with 22nm transistor

Telecommunications Circuits Lab (From 01/02/2020 to 31/07/2020)

Under the Supervision of

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Confidentiality : No

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Lausanne, August, 2020

Candidate's Declaration

I hereby declare that the work presented in the thesis entitled **"Thesis Title"** in partial fulfillment of the requirements for the award of the Degree of **Master in micro and nanotechnologies for integrated system** is an authentic record of my own work carried out during a period from February 2020 to August 2020 under the supervision of **Prof. BURG. Andreas.**, Department of Electrical Engineering, Telecommunications Circuits Lab.

The matter presented in this thesis has not been submitted by me for the award of any other degree of this or any other Institute/University.

(R. V.)
(Reg. no. .....)

This is to certify that the above statement made by the candidate is true to the best of our knowledge and belief.

(Dr. R. P.)
Professor, ECE Department
NIT Kurukshetra

Place: Kurukshetra
Date:

Thanks

In this thesis I would like to thanks all the people that help me during my internship. Especially Mr.Gitterman which thanks to his expertise have helped me a lot to understand the subject. With his pedagogy and patience he was a great help to overcome the different challenge that I had to deal with.

I would also like to thanks Mr.Burg which have offered me the opportunity to work in the prestigious lab of the EPFL. Thanks to this internship I know for sure that I want to specialize in nanoelectronics.

Thanks also to all the personnel of the lab for their support and warm welcome which has allowed me to enjoy the lab and the atmosphere of a research lab.

Finally, I also want to thanks the personnel of Phelma which helped me with the procedure and how to work with the pandemic crisis.

(R. V.)

Lab presentation

The Telecommunication Circuits Laboratory (TCL) is part of the Institute of Electrical Engineering at EPFL and concentrates on the development of circuits and systems for digital signal processing with a strong focus on telecommunications. Their work finds application in wireless and wireline communication systems, and in a variety of applications related to telecommunications.

Their main research topic are the development of low-complexity signal processing algorithms for communication technologies,

the design of technology demonstrators and prototypes for performance assessment,

the hardware-efficient, low-power implementation of digital integrated circuits for VLSI signal processing (in communications, but also other applications) and for embedded systems

the utilization of communication concepts for designing robust/reliable and energy efficient systems.

They focus on a system-level perspective and try to consider both algorithm and implementation aspects jointly. In particular,they are interested in new, spectrally efficient communication technologies such as multi-antenna wireless communication systems which serve a wide range of applications from cellular systems to local high speed wireless networks. Furthermore,they are interested in wireless and wireline communication links with very high throughput and processing requirements that challenge even the most advanced silicon process technologies. Finally,they are interested in linking concepts from communications (e.g., coding) to future deep submicron integrated circuit technologies which are likely to suffer from reliability issues.

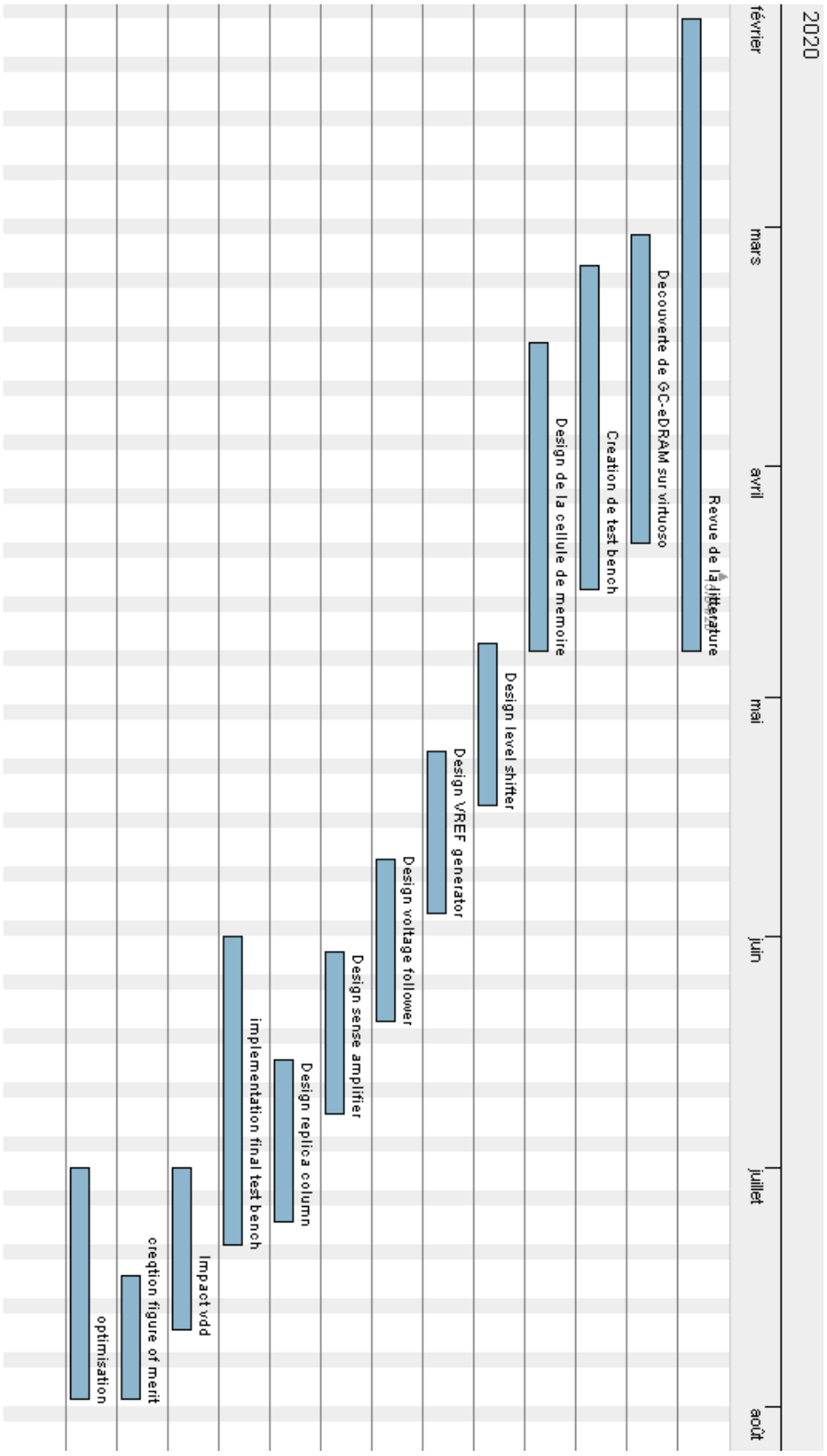

Figure 1: Gantt diagram

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List of Acronyms/Abbreviations

2D	Two Dimensional
3D	Three Dimensional
2T	Two transistor
3T	Three transistor
DRT	Data retention time
GC-eDRAM	Gain cell embedded DRAM
IDRT	Intensity data retention time
RWL	Read word line
RBL	Read bit line
SN	Storage node
VDRT	Voltage data retention time
vdd	Voltage drain to drain
vss	voltage source to source
Vth	Voltage threshold
WWL	Write word line
WBL	Write bit line

Chapter 1

Introduction

This Chapter provides a brief description of GC-eDRAM technologies and its goals. The motivation and objectives of the present research work are presented. It also highlights the organization of the thesis.

1.1 Background

In our world were the computing need is always growing we are facing a new challenge every day to follow this demand especially since we are at the end of the Moore law. The memory is an essential part of the computing system, especially in an embedded circuit. In fact, the memory currently takes half of the place in an embedded circuit and is responsible for most of the energy consumption of the chip. Consequently, recent research tends to provide always smaller and energy-saving memory. The scaling down allow to achieve always better performance in term of cost, size and energy consumption.

1.2 Motivation for the present research work

The two most common types of memory is the SRAM and the DRAM. The SRAM need at least 6 transistors to be functioning so it has a large energy consumption and size occupation with respect to DRAM. Consequently, we could consider the DRAM as the solution to scale down the memory but the DRAM need 1 transistor and 1 capacitor. The scaling down of the capacitor is very challenging and make this unsuitable to be integrated into the new technology node of the transistor.

Consequently there is an increasing need to develop a new type of memory cell to follow the Moore law and so follow the development of the other part of the computing system.

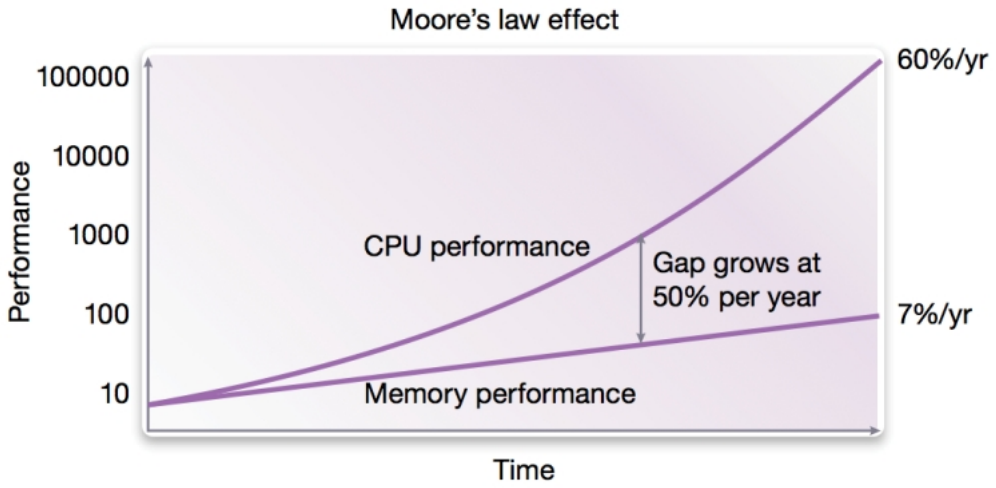

Figure 1.1: The end of Moore law for memory [5]

In this work, we will present the adaptation of the GC-eDRAM on 22nm technology. This memory cell presents many advantages that address the issue explain previously.

- The GC-eDRAM is compatible with the CMOS technology that allows to follow the innovation made on the transistor.
- On is smaller configuration the GC-eDRAM use only 2 transistors and consequently is much more compact than the SRAM which necessitates 6 transistors.
- The energy consumption of this memory cell is also improved.

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1.3 Problem statement

But this memory cell due to his recent development still exhibits challenge and issue that need to be deal with so it could consider as a functioning memory. This is especially true since we are working on the 22nm technology which causes some of the following issues to more significant.

i) The smaller we scale down the transistor the leakier they are. This creates some issue on the data retention time of the memory.

ii) To be considered as competitive the memory should be able to not have a functional error. And this error due to coupling effect or leakage should be minimized as a maximum under all corner process

iii) While maintaining the maximum data retention time we should be able to reduce the voltage supply of the cell

iv) The memory should be able to be resilient to temperature variation

1.4 Organization of the thesis

The research work presented in the thesis is organized and structured in the form of seven chapters, which are briefly described as follows:

i) **Chapter 1** Introduction

ii) **Chapter 2** Presentation of GC-eDRAM

iii) **Chapter 3** Literature review

iv) **Chapter 4** The choice of the memory cell

v) **Chapter 5** Peripheral

vi) **Chapter 6** Timing and yield result

vii) **Chapter 7** concludes the thesis with overall discoveries of the present research work. The scope for future work is also mentioned.

Chapter 2

Gain cell presentation

This Chapter presents the most commonly used GC-eDRAM

2.1 Gain-cell

2.1.1 Cell presentation

The basic principle of the GC-eDRAM is inspired by the DRAM the information goes through a transistor and are stocked in a capacitor. The main difference with the DRAM is that the capacitor in GC-eDRAM is made from the gate of a second transistor, the gate is called storage node and its here that the 1 and 0 voltage will be held.

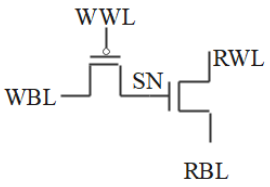


Figure 2.1: Two transistor GC-eDRAM

The Gain cell in his more simple form is made from two transistors. The first one is called write transistor because it is responsible for the write operation. You need two signals to pilot it. The WBL which will contain the information to write on the storage node and the WWL that will open the transistor during write and closed when the information on SN needs to be held.

The second transistor can be duplicated for a reason which will be explained after but they are always called read transistor. Like in the SRAM you need to signal to select the cell from the array. If the write operation is quite trivial the read of a 1 and a 0 will need more attention and will be explained in the next section.

2.1.2 Operating mechanism

The GC-eDRAM operation can be separated into two phase, the write and the read. During write you will open the write transistor with the WWL then you insert the voltage of ”1” and ”0” on the storage node. The waveform of the WWL, WBL and

SN are presented on the two first panel of the following picture but notice this is for a GC-eDRAM made from a n-transistor for read and write.

To read the voltage held on the storage node you need in this case to make the RWL go to 0V while the RBL was pre-charged to Vdd. Then if the storage node contains a 1 aka a high voltage the read transistor will be open and the RBL will be discharged in the RWL causing the RBL voltage to go down. On the contrary, if we had been written a 0 in the storage node the read transistor will be closed and the RBL will not discharge in the RWL and consequently, the voltage will stay high. The two operation waveform are presented int the tow last panel of the following picture[1].

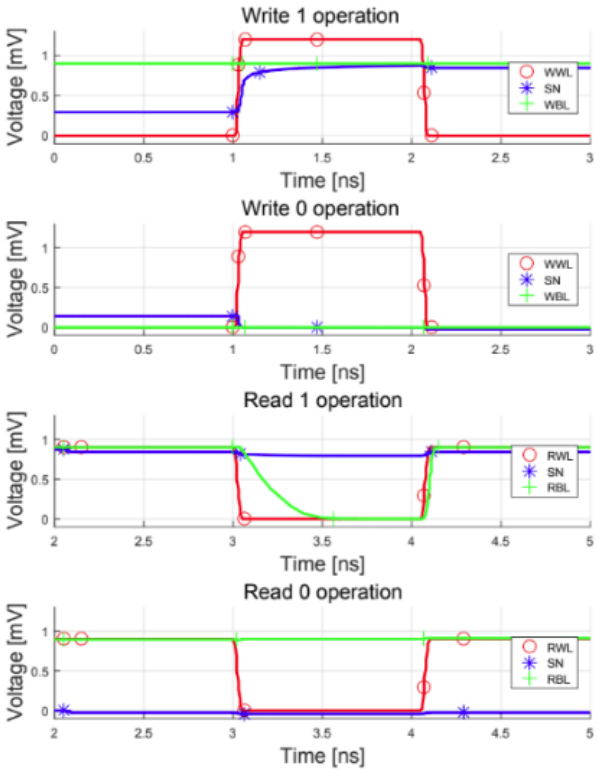


Figure 2.2: Operating mechanism GC-eDRAM [1]

One of the big advantages of the GC-eDRAM is that the read is non-destructive and can be done at the same time as the write. This simplifies the control of this memory and reduces the number of operation needed for a write and read. Consequently less operation you need less time and less power to operate the cell.

2.2 Different GC-eDRAM

The gain cell is an old concept and has been optimized throughout the year. Many scientists have created different configuration to optimize data retention time or energy consumption. On the following picture, it is represented the most commonly used configuration, To distinguish them they are referred by their number of transistor and the type of the read and write transistor

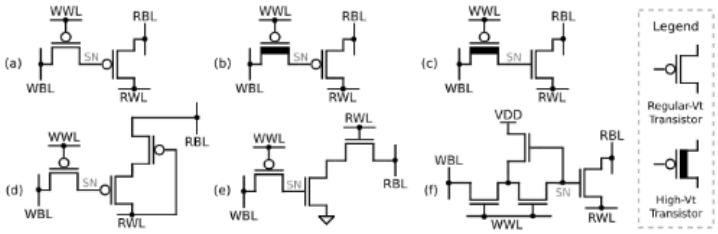


Figure 2.3: Potential GC-eDRAM choices[3]

Each of this configuration present advantages and drawback that need to be taken into account during the design to achieve higher performance. The first study conducted during the internship was to choose between the 2T, 3T and 4T configuration

2.2.1 2T Gain cell

The 2T configuration is the most compact way to design the cell with only 1 read transistor and 1 write transistor. This is sufficient in theory to accomplish the memory need but it suffers from big drawback when put in a whole array due to the negative impact of the cell can have with each other. Especially during the read of 1.

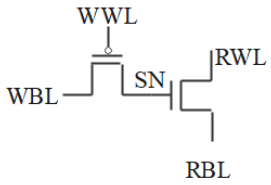


Figure 2.4: 2 Transistors GC-eDRAM

2.2.2 3T Gain cell

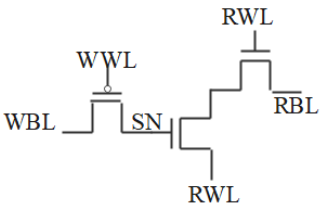


Figure 2.5: 3 Transistors GC-eDRAM

The 3T configuration consists of adding a transistor to the read circuit to isolate the RBL of each gain cell from the other. This is made to avoid the RBL saturation when we read a "1". In fact, without this second transistor on the RBL of the cell, the other cell creates a parasitic discharge on the studied cell. This can be observed while reading a "1" and it is observed saturation of the voltage to the value Vdd-Vth [1]

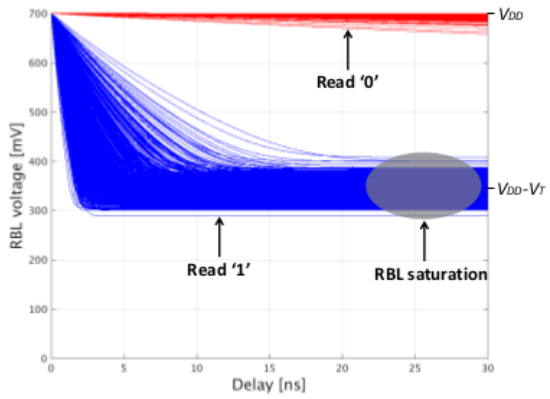


Figure 2.6: RBL saturation in 2T GC-eDRAM [1]

This a non-negligible effect that was chosen to be deal with because the 1 have a faster decay in our final configuration

2.2.3 4T Gain cell

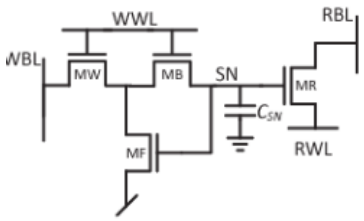


Figure 2.7: 4T GC-eDRAM [4]

In this configuration which was discovered by my internship advisor Mr Gitterman, we add a feedback mechanism to increase the data retention of a "1". This allows to greatly increase the final DRT with a reasonable increase of the size of the memory since many gate and drain of the transistor can be shared

2.3 Summary

From this section what need to be remembered is that the GC-eDRAM can be constructed in many different ways. The cell in most simple form is made of two transistors but it can go up too 5 transistors. The cell that was chosen in this study is the three transistors one because it allow to the RBL to discharge completely to 0V. This is really important because the read of a "1" and "0" is the most important factor to optimize.

An other important point that was tackled in this section is that the read is non destructive in GC-eDRAM in contrary to regular DRAM. Moreover the read and write can be done simultaneously.

To distinguish the discharge of RBL_1 and RBL_0 we will need a third signal which discharge is in between of the two RBL. Then we will be able to amplify the difference and read the value written on the storage node.

Chapter 3

Litterature review

The comprehension of the different physic effect that operates in the cell is essential to provide an optimisation of the parameter 2.

3.1 Leakage

The main issue that is facing the GC-eDRAM is the rapid degradation of the voltage present on the gate of the read transistor due to the leakage of the transistor. Here in the figure below is presented the leakage present in a 2T cell which is sufficient to understand the main issue that needs to be resolved.

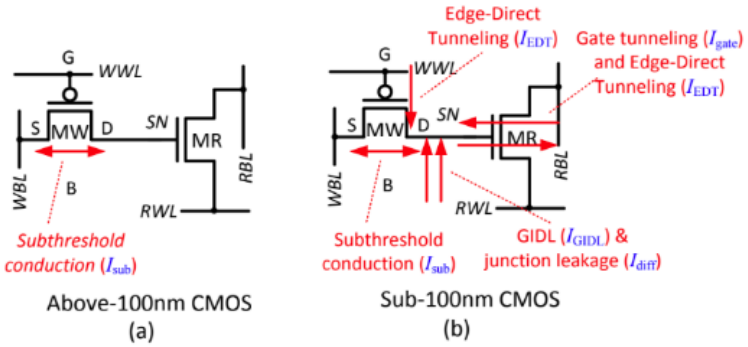


Figure 3.1: Leakage impact [3]

As presented on this figure we can observe that the leakage of the transistor is present between the gate and the drain, the gate and the source and finally between the source and the drain. Also, it is important to understand that the leakage was expected to increase when we reduce the size of the transistor.

3.1.1 Leakage analysis

The first part of my theoretical study of the cell was to identify which of this different leakage was predominant and needed to be reduced as possible. The literature explains that the subthreshold leakage (between drain and source of the write transistor) was expected to be predominant.

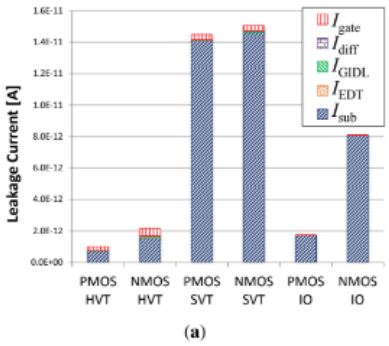


Figure 3.2: Leakage of GC-eDRAM [2]

Since then we were using transistor on the 22nm technology node which is smaller than every GC-eDRAM ever made so a study through simulation was made to verify this assessment

3.1.2 Voltage threshold

One of the essential factor to reduce the subthreshold leakage is to choose an adapted voltage threshold voltage. There is an exponential dependency of this leakage with respect to the value of V_T

$$I_{sub} = I_0 e^{\frac{V_{GS} - V_{THO} - \eta V_{DS} + \gamma V_{BS}}{nV_T}} (1 - e^{\frac{-V_{DS}}{V_T}})$$

But this is a trade-off with the speed of the transistor and the voltage supply that we will use to power the memory

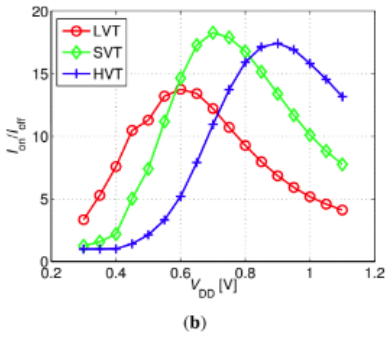


Figure 3.3: Voltage threshold versus speed [1]

A study presented in the next chapter will explain how we designed the cell concerning this parameter.

3.2 Summary

This section presented result from previous study on how to optimize the cell. From this the important point are that the leakage have an determinant impact on the data

retention time of the cell. In fact the DRT is directly related to the ability of the write transistor to not let the voltage value discharge in the WBL due to subthreshold leakage. In fact the most important leakage in the cell is the subthreshold leakage.

To reduce the subthreshold leakage the most effective way is to design the transistor with an adatapted voltage treshold. The higher the value the least will be the leakage but this come with some trade off. Increasing the voltage threshold have for effect to reduce the speed of the transistor and increase the difficulty to write a strong "0" on SN.

Chapter 4

Design choice of the memory cell

The gist of the memory is the cell in which the "1" and "0" will be retained so the first simulation was made to optimize the cell

4.1 Transistor choice

In the beginning, the study has begun with 28nm technology to understand the base of the GC-eDRAM. Then I used the 22nm technology this came with a whole library of transistor and the first design choice was to determine which transistor was the most suited to our application.

The test bench testing methodology it consists of all transistor possible. The simulation aimed to determine the leakage under different biasing. Having the lowest sub-threshold voltage is essential for the writing transistor. On the other hand, it was needed to quantify the gate leakage for the read transistor

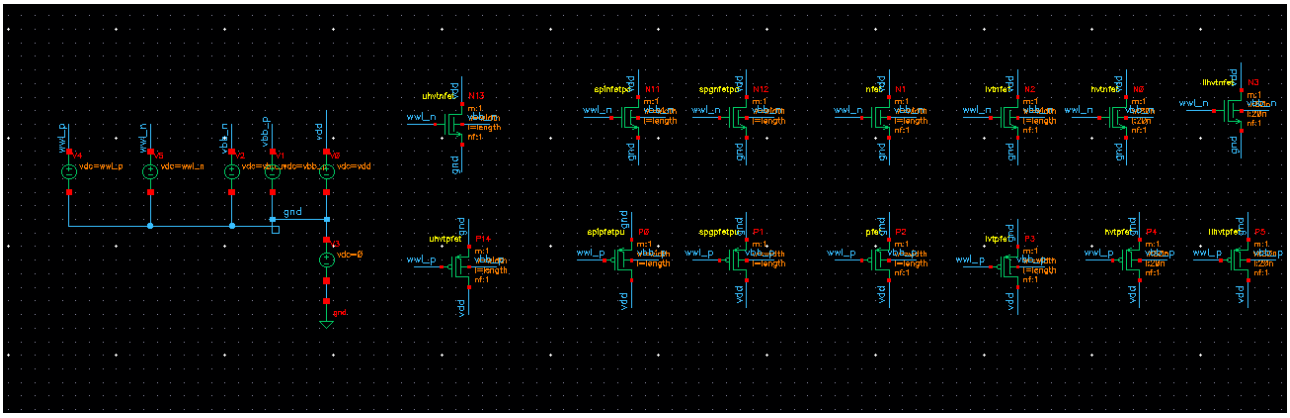


Figure 4.1: Transistor characteristic test bench

From this it was concluded that the best transistor for the write transistor is p one. Also this helped to determine first potential candidate for the write transistor:

i) **llhvt** Low leakage high voltage threshold

ii) **uhvt** Ultra high voltage threshold

iii) **rvt** Regular voltage threshold

iv) **hvt** high voltage threshold

furthermore, the gate leakage is always 2 order of magnitude lower than the sub-threshold leakage. The leakage for the write transistor is not a relevant factor consequently we will use the low voltage threshold one (lvtfet). This is done to improve the speed of the read which is directly correlated to the value of the voltage threshold.

The second step was to conclude on the best write transistor usable from the library. To do so a simulation of the DRT was done with different write transistor.

To do so it is important to first define the notion of Data Retention Time (DRT). This is the time after we consider that the voltage value written on the storage node is too deteriorated to be read correctly. This on a first approach will be the criterion that will allow us to do our design choice. There are many way to define the DRT and the test bench will be explained in detail in the section 6.

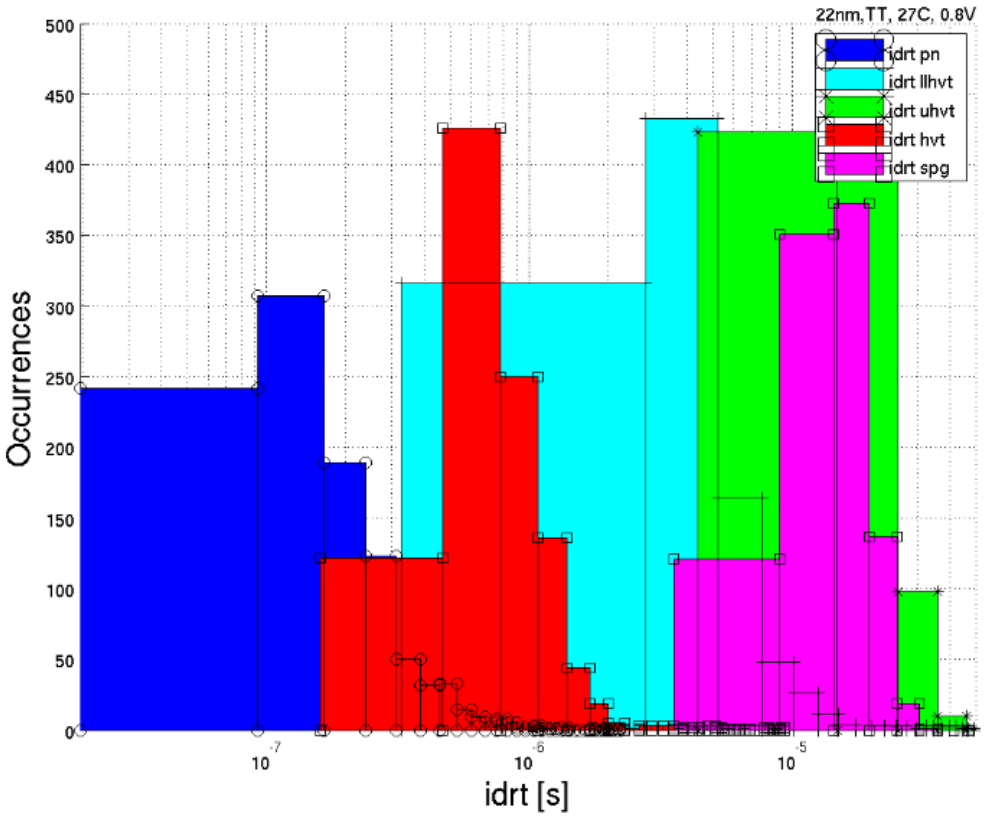


Figure 4.2: Idrt of uhvt llhvt hvt spg rvt in Monte Carlo simulation

The single-port pull-down (spg) is here for reference because it's not usable because its a transistor designed solely for the SRAM cell. The best transistor which was chosen then was the Uhvt because he got the highest DRT.

4.2 Transistor sizing

4.2.1 width of the transistor

After choosing the transistor the design of his parameter, width and length so on the leakage test bench presented earlier the impact of width on the gate leakage voltage

threshold and subthreshold leakage was plotted.

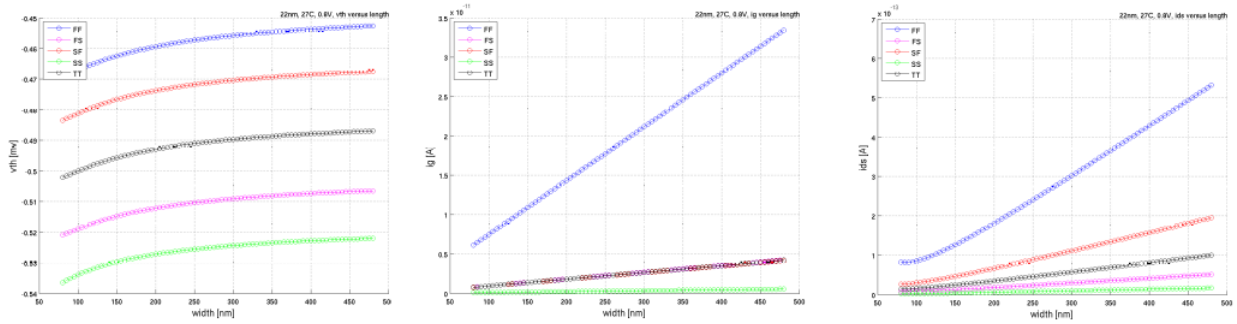


Figure 4.3: Impact of width

From this figure, we can conclude that the width has a linear dependence with all this parameter and it should not be worthy to increase the width of the transistor. The minimum size of 80n will be used for the write and read transistor

4.2.2 Length of the transistor

The length of the transistor has a non-negligible impact on the sub-threshold leakage which the biggest limiting factor of our application. It may be interesting to increase a bit the length even though its a trade-off with the total size of the memory array

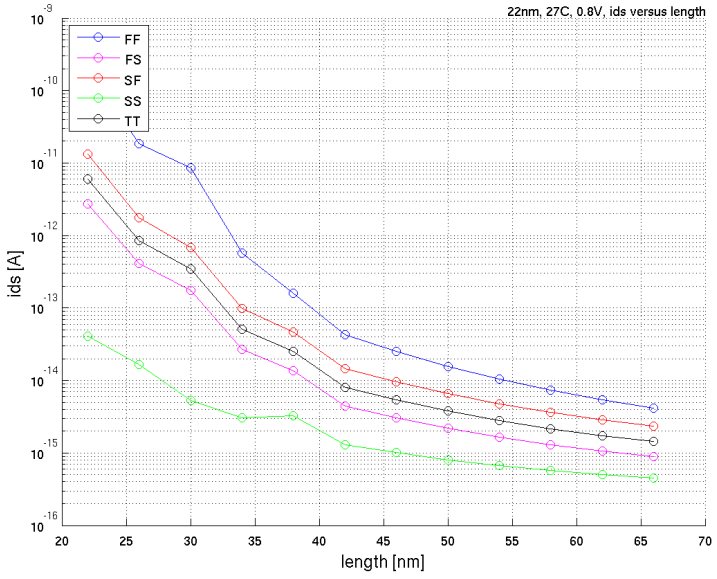


Figure 4.4: Subthreshold leakage versus length

So it was decided to use 35nm length for the write transistor because the exponential dependence on the length was too important to not be used. this comes with a small increase of the area of the cell so this trade-off was considered as worthy

4.3 Transistor biasing

The biasing of the cell is also very important because a good biasing should allow increasing greatly the data retention time and the yield of the cell.

4.3.1 Negative Voltage on WWL

The first thing to do is to use a negative voltage on the WWL during write. This allows overcoming the threshold loss due to the high voltage threshold of the transistor. this phenomenon can be observed by looking at the value of the storage node 0 versus the negative voltage applied to the WWL. It s important to notice due to circuit constraint (driving force) it is unrealistic to apply a negative voltage smaller than -0.3V.

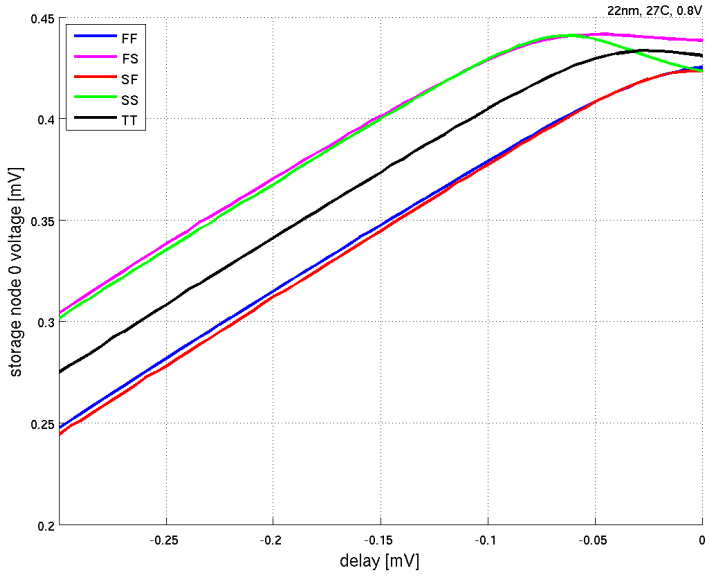
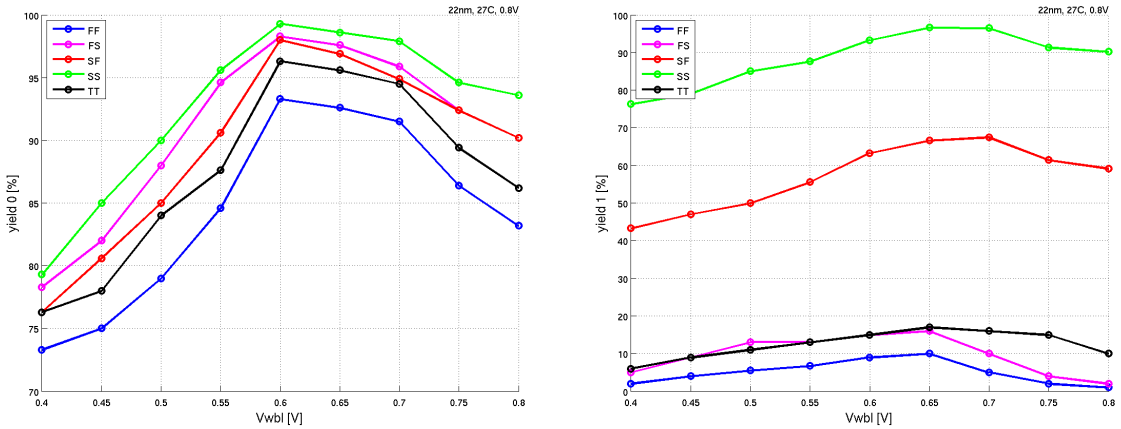


Figure 4.5: Storage node 0 voltage versus negative voltage on WWL

4.3.2 Voltage of the WBL

The value of the voltage of the WBL during write and during the idle state is important to increase the DRT of the memory. It has a direct impact on the subthreshold leakage of the transistor. Through simulation it was proven that it is best to have the WBL at high during idle state, this can be explained by the difficulty of the cell to retain the value "1".

The next simulation shows the yield of the cell, in other words, the number of time the good value of the cell was read over the number of simulation. The yield is plotted versus the voltage applied to the WBL when writing a "1". It is always better when writing a 0 to have the smallest value possible so 0V due to the positive threshold loss.



(a) Yield 0 versus Vwbl **(b)** Yield 1 versus Vwbl

Figure 4.6: Impact of Vwbl versus yield

From this result it was conclude that the best way to use the WBl is to have an idle voltage of 0,6V. Also the write of a 1 will be done with a voltage of 0.6V.

4.3.3 Coupling voltage

A technique to also improve the voltage written on the storage node 0 is to use a coupling voltage. This is necessary since the threshold loss that increases the value of sn0 during write. The coupling voltage consists of a voltage going from vdd to 0 after having written the value, this will reduce the value on the storage node 0.

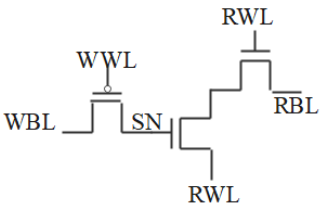
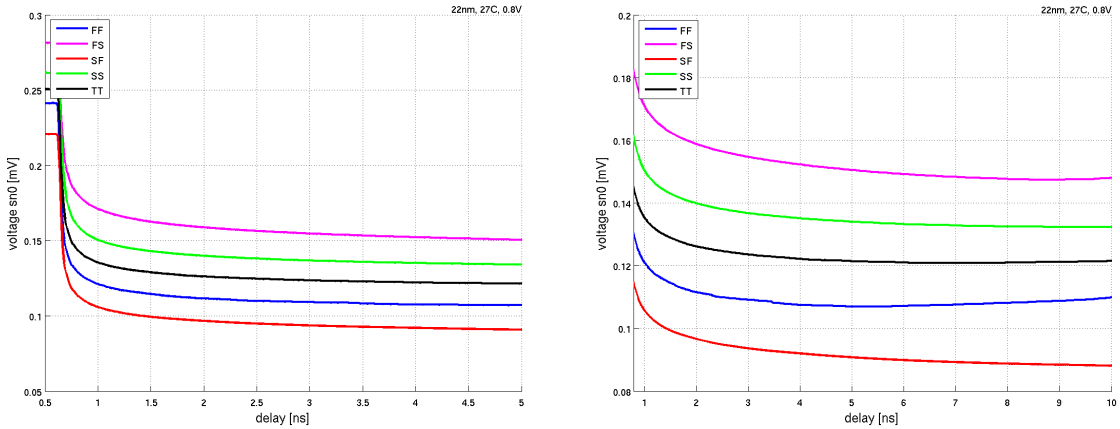


Figure 4.7: Schematic of 3T GC-eDRAM

then the second step is to know at which time the coupling voltage should go down after the write. To do so the value of the storage node 0 versus the delay between the WWL and coupling voltage was plotted.



(a) Configuration of delay for V coupling **(b)** Configuration of delay for V coupling

Figure 4.8: Configuration of delay for V coupling

From this result, the optimal value decided was 1ns

4.4 Summary

In this chapter, a focus on the memory cell design have been provided. From the result presented in this section it have been conclude that the best transistor for write was an UHVT and LVT for read. This have been mad to reduce at maximum the subthreshold leakage through the write transistor, but also to increase the speed of the read transistor. This design choice can be justified by the fact that the read is expected to be much more time consuming than the write.

Also on a second part it was shown that the exponential dependence of the subthreshold leakage to the length justify a increase of the length of the write transistor to 36nm. The width on the other hand will remain the same because the linear dependence of the capacitance to this factor is no sufficient to justify an increase of the width.

The last section shown the three techniques used to optimize the write which is necessary due to the high value of the voltage threshold of the write transistor. Applying an negative voltage have for effect to partially overcome the voltage loss during the write. Also using a coupling voltage is good solution to allow the write of a stong ”0” on the storage node. The best time to launch the coupling have determinded to be 1ns after the WWL open the write transitor. Also to optimize the DRT the idle voltage of the WBL should be 0.6V and the voltage of the write was choosen to be 0.6V too. This choice can be justified by simulation result that show an increase of the yield for this value.

Chapter 5

Peripheral design

The memory to considered as functional need peripheral to allow good writing and reading of a "1" and "0". In this chapter it will be presented the choice made for the different peripheral of the writing and reading circuit

5.1 Peripheral presentation

The peripheral of the memory cell can be separated in two parts. First the writing circuit which used to write a strong "1" and "0". The second part is the reading circuit which should be able to distinguish the discharge of "1" and a "0" and transform it a signal that can be interpreted by other components.

5.1.1 Writing circuit

The first operation that needs to be executed is to write the wanted voltage on the storage node. The constrain are to write a strong "1" and "0" which is difficult considering the coupling effect present at this scale. To do so efficiently it is needed the following peripheral:

- Level shifter to apply a negative voltage on the WWL and overcome the voltage loss due to V_T

- Voltage follower is needed because the DRT is increased with a "1" with 0.6V and an idle voltage of 0.6V. Furthermore, this should be done by a system with a good driving force and so a voltage follower is needed

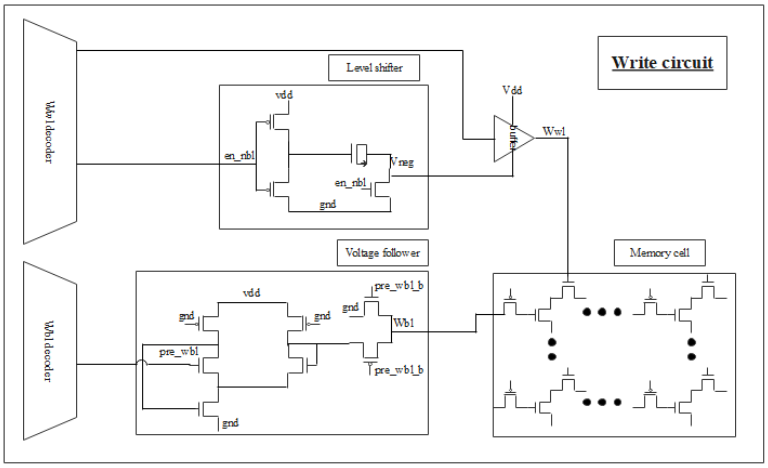


Figure 5.1: Write circuit schematic

5.1.2 Reading circuit

The memory beside retaining the "1" and "0" should be able to read this value on the storage node and transform in a square-like signal so it can be read by other components of the computing circuit. To do so the solution that was found was the use of:

- Voltage reference generator which is a circuit generating an electrical signal RBL_{ref} with a discharge faster than the one of RBL_0 and slower than RBL_1.
- The replica column is essential to create the impulsion that will enable the sense amplifier. This should be done when the difference between the RBL and RBL_{ref} is sufficient to be detected by the sense amplifier.
- The sense amplifier should be able to transform the difference between the RBL into a readable signal by all computing component.

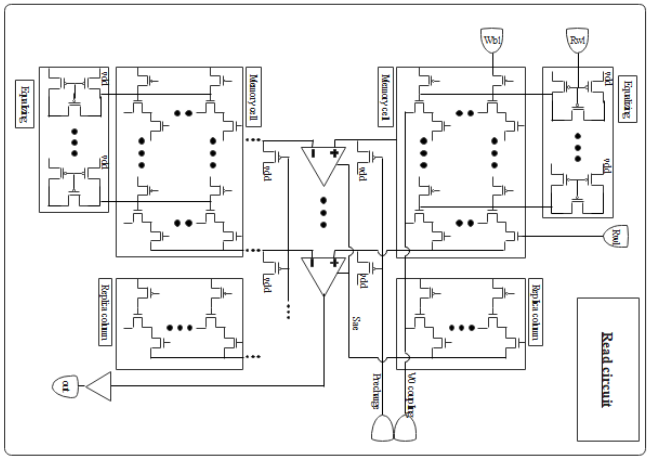


Figure 5.2: Read circuit schematic

5.2 Writing circuit

5.2.1 Level shifter

The level shifter is the component where the negative voltage that will go to the WWL is created. To do so we use a signal here call enable negative voltage but which is similar to WWL to charge a capacitor to vdd when the signal goes low. This cause a coupling phenomenon which creates a negative voltage on the other side of the capacitor. When the signal enable negative voltage goes highs the negative voltage is discharged to ground through the last transistor

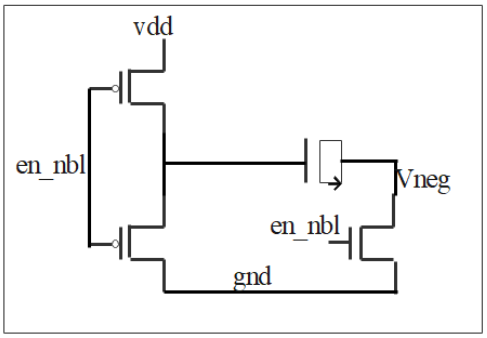


Figure 5.3: Level shifter schematic

To have a good capacitor adapted to our need in term of negative voltage the component ncap of the library was used. The n-cap is multiple n-transistor with their gate and drain connected to each other put in parallel. It is possible to change the width and the length of the transistor to obtain a negative voltage adapted to our need here -300mV. Consequently, a swipe on the width shown below have revealed that the optimum dimension is a length of 750nm for a width of 1.5um

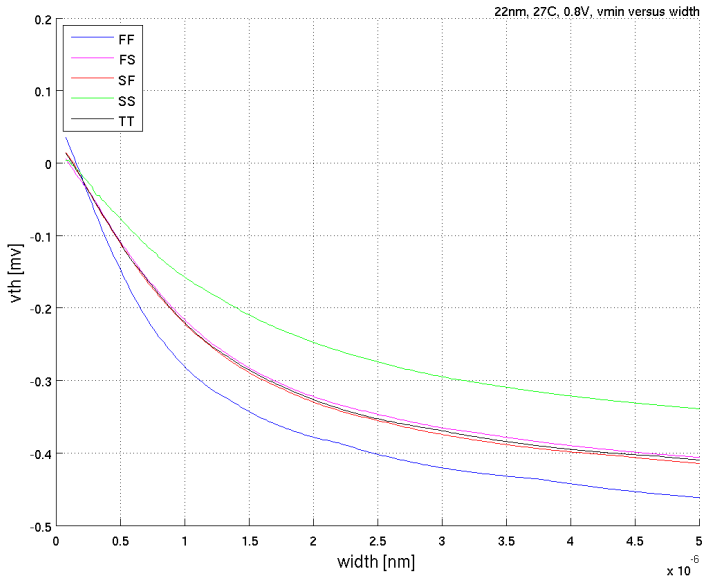


Figure 5.4: Negative voltage generation versus width of cap

5.2.2 Voltage follower

To write the good value on the storage node it was needed to have a system able to create a square waveform going from 0.6V to 0V. But to generate VREF with a circuit with a low driving strength a current amplifier is needed, that why we use a voltage follower. A trade-off between the speed and the dynamic range had to be effectuated. But even the best voltage follower could not go to 0V so a mux gate at the end of the voltage follower was added to allow the voltage follower to discharge to 0V when the pre WBL goes low. After research in the literature, the model that was selected is the following (fig 5.4)

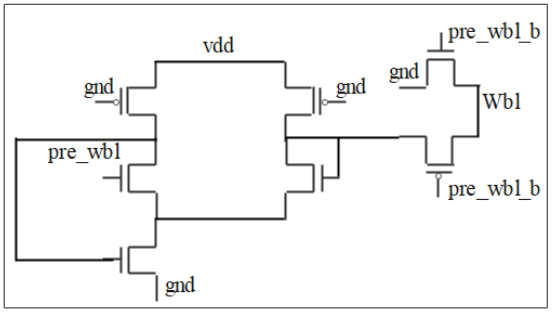


Figure 5.5: Voltage follower schematic

5.3 Reading circuit

5.3.1 Voltage reference generator

To create a signal that has a discharge that allows distinguishing the discharge of RBL_0 and RBL_1 we use two different circuits the equalizing circuit and an array of cell which create RBL_{ref}. The equalizing circuit that creates the desired voltage then it is conducted to the cell and the RBl will go down with a falling time which is faster than RBL0 and slower than RBL1. This will allow differentiating the two signals and the difference between the RBL will be amplified by the sense amplifier.

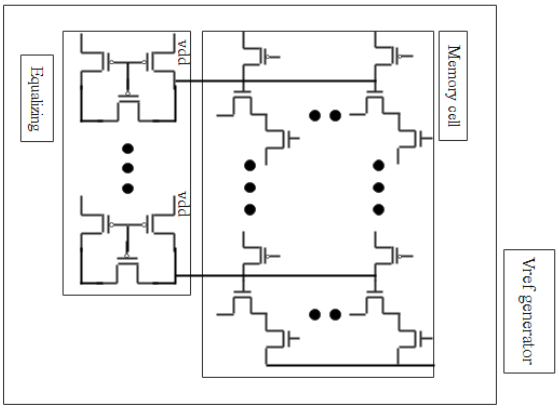


Figure 5.6: Voltage reference generator schematic

The equalizing circuit use two transistor one connected to vdd the other to gnd. When the RWL go up they open and they connect through a third transistor. By tuning the width of the two first transistor you can tune the value at which the voltage will stabilize. Finding the good parameter is for the transistor was a good part of my internship

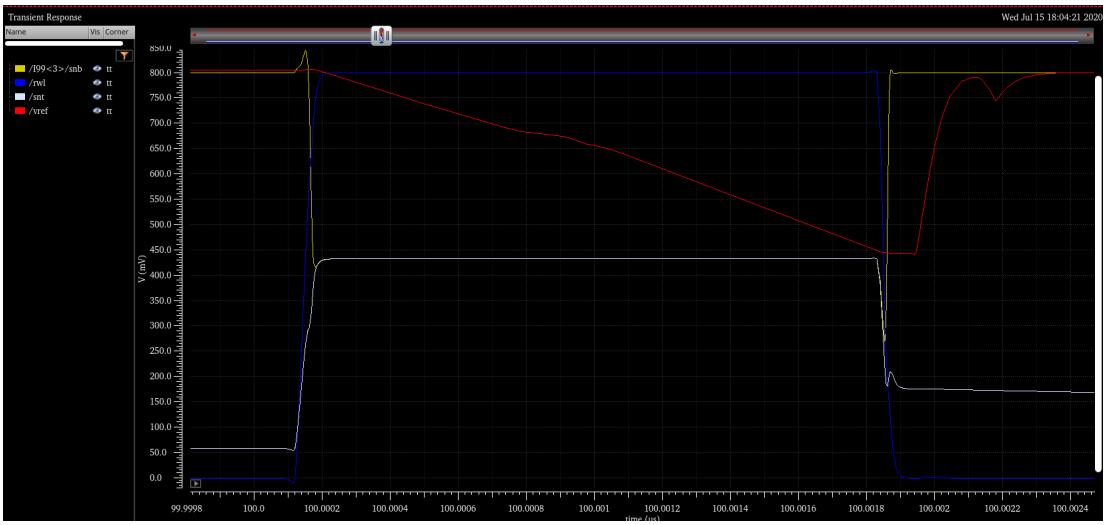
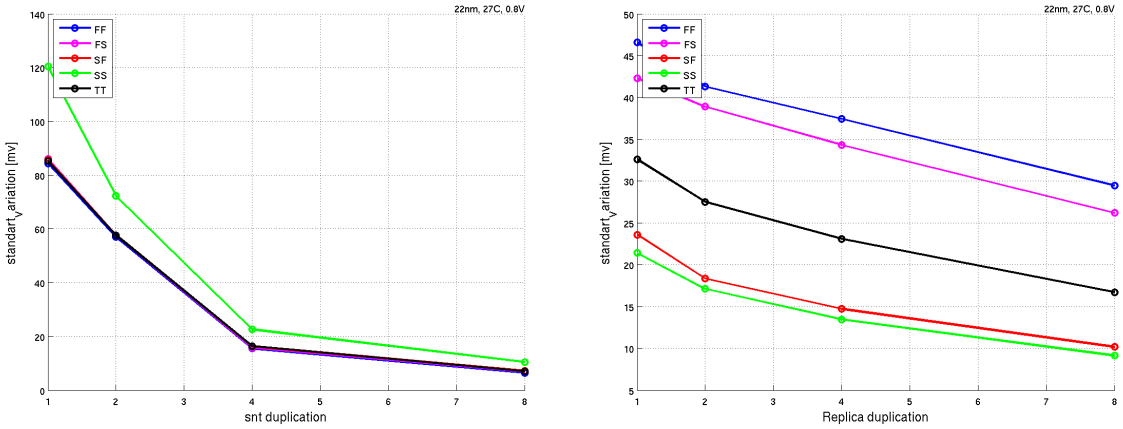


Figure 5.7: Waveform of voltage reference generator

It's important to not have too much variations both on SN_{ref} and RBL_{ref} because

it increases a lot the time after which we can still read a 1 and 0. To do so its possible to put many systems in parallel. To find the optimal number of duplication the variation versus the number of duplication was plotted.



(a) Sn_{ref} variation versus equalizing circuit duplication

(b) RBL_{ref} variation versus equalizing circuit duplication

Figure 5.8: Variation versus equalizing circuit duplication

From this, we can conclude that the best trade-off between space and variation is a duplication 4 time of the equalizing circuit

5.3.2 Replica column

The timing between the moment the RWL go down and the moment the sense amplifier should read the difference between the RBL is essential. In fact, the timing to be optimal the RBL should discharge enough to have a difference the RBL_1 and RBL_0 with RBL_{ref} readable (approximately 50mV). Also, the timing should depend on the process variation on the transistor to be truly effective. Consequently, the replica column was chosen because it can track global process variations (PVT) since it has similar read port as the array.

The solution which was chosen is to use a column of cell call replica column in which we write a voltage of Vdd. When the RWL go down the RBl of the replica column will go down and this is connected to an inverter which generates the sense amplifier enable signal

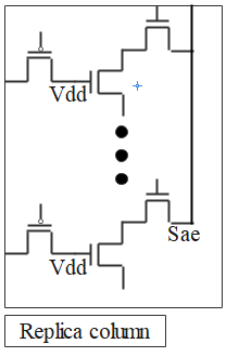


Figure 5.9: Replica column schematic

To be sure of the good functioning of the system the delay between the moment the RWL go down and the sense amplifier enable go up was calculated under Monte Carlo simulation.

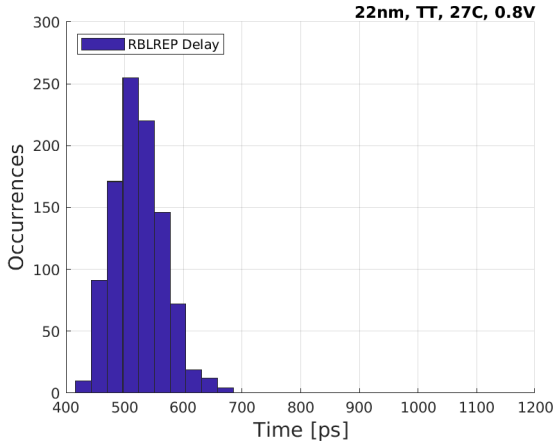
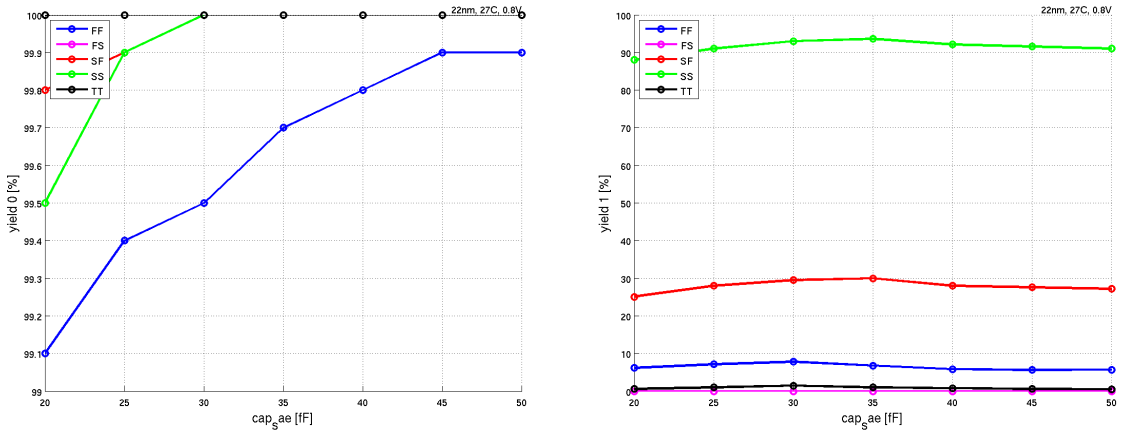


Figure 5.10: Delay replica column versus Vdd

From this figure, it was concluded that the distribution of the delay is not wide and the delay is not too long. We are targeting a 1ns read and write cycle and the reading time is expected to be responsible for most of the time consumption.

This delay can be optimised by adding a capacitor on the RBL of the replica column. This will allow having control over the delay to optimise the yield with respect to the delay between the read. Consequently, the yield at 600us was plotted versus the capacitance of the capacitor.



(a) yield 0 versus capacitance replica at 500u **(b)** yield 1 versus capacitance replica at 500u

Figure 5.11: yield evolution versus capacitance replica at 500u

From this study was concluded that the optimal capacitor was an n-cap of 35f. This is due to the importance to optimize the yield of reading 1 over to reading 0. Reading 0 yield does not decrease a lot when the read time is high and consequently is not a limiting factor.

5.3.3 Sense amplifier

The sense amplifier is essential to transform a small difference between the RBL into a readable signal by all computing systems. To do so we will use a design based on an SRAM cell but this time the transistor width will be 10 times increased. So the difference will be amplified by the feedback system of the two inverter

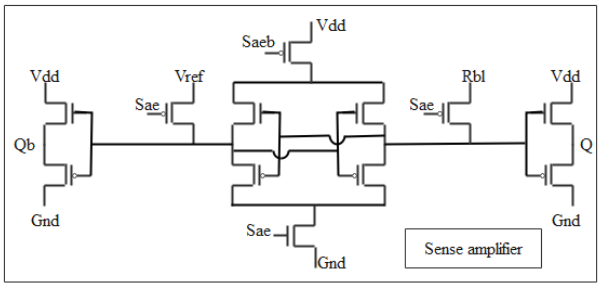
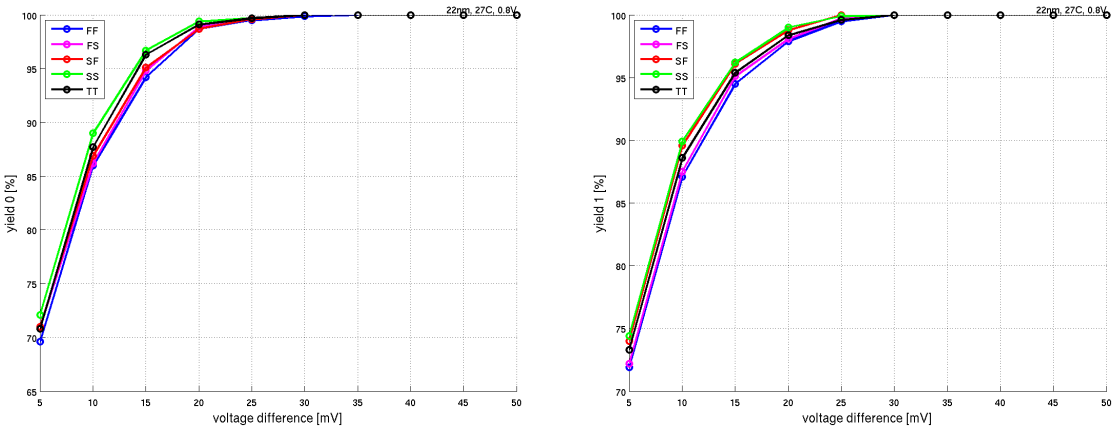


Figure 5.12: Sense amplifier schematic

To have an idea of the limits of the sense amplifier the yield versus the difference of the RBL was plotted in the next figure



(a) Read of 0 versus voltage difference **(b)** Read of 1 versus voltage difference

Figure 5.13: Sense amplifier performance

The limit of detection with our sizing is 40mV which of the order of what we are looking for

5.4 Summary

In this chapter a focus have been made on the peripheral that compose the memory array. First, the write circuit is composed of a level shifter and a voltage follower. Then the read circuit is composed of a voltage reference generator, a replica column and a sense amplifier.

The performance of each of this peripheral have been tested individually to conclude how to use them at the maximum of their potential. Due to system constraint the level shifter will not be used to create a negative voltage stronger than -0.3V. The voltage follower is adapted to our utilisation but needed a mux gate to go to 0V. The voltage reference generator is also performing as expected but to reduce the variation on RBL_{ref} the equalizing circuit have been duplicated 4 time. The delay generated the replica column for the sense amplifier enable signal have been optimized thank to a ncap present on his RBL. Finally the transistor of the sense amplifier have been up sized ten time to allow a detection of the order of 50mV.

Chapter 6

Timing and yield result

To evaluate the performance of our GC-eDRAM it was essential to create a test bench that evaluates with precision the limits and the impact of the different parameter.

6.1 Test Bench

6.1.1 VDRT

The first test bench that was used in our study was the Voltage Data Retention Time. As a first approximation, the VDRT is a good beginning to evaluate the capacity of the cell to retain a voltage on a storage node. The principle of the VDRT as said in his name is based on the study of the voltage present on the storage node.

To evaluate the retention time two cell is instantiated, the first one will be written a "1" and the second will be written a "0". From this point after writing their value the retention time is the time needed for the difference between the storage node of the "1" and "0" to be $Vdd/2$.

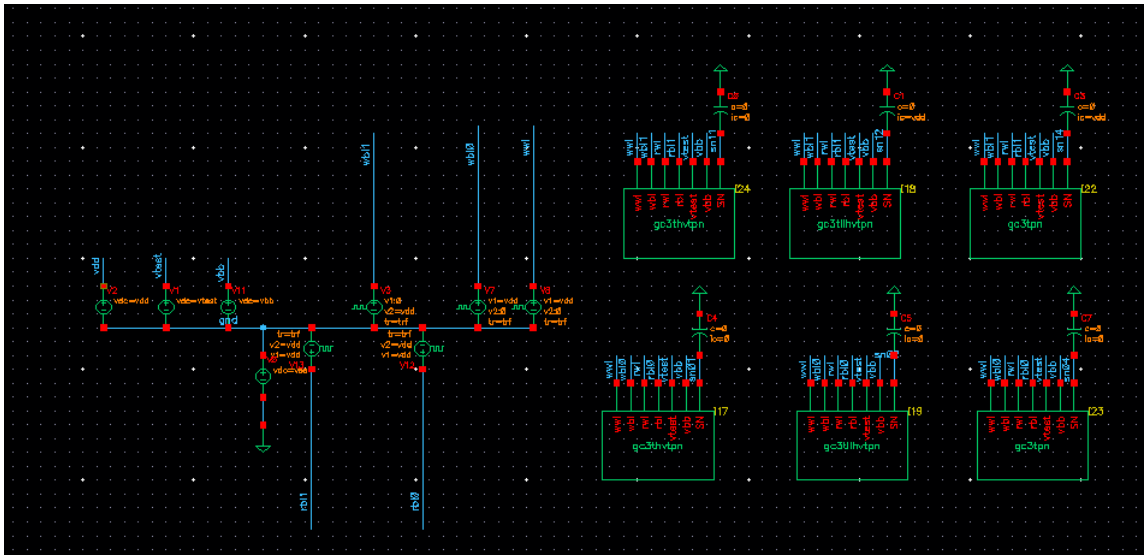


Figure 6.1: Vdrt test bench

This first Test bench is a good first approximation and was used during the first month to evaluate the impact of different biasing and different transistor. But on the other hand, it does not take in account the impact of the read on the storage node, this is a real issue since the coupling effect is not negligible for a transistor of this

scale. Consequently to make relevant design choice it was necessary to develop a more performing test bench the one based on the current

6.1.2 IDRT

The IDRT test bench as said in the name is based on the current evaluation in the cell. The working principle of this test bench is still really similar to the VDRT. Once again two cells are used one with a "1" and the other with "0". The retention time will be the time needed for the current difference in the two read transistor to be 0.

This is due to the decay of the value on the storage node that will cause read transistor of the "1" to close after a certain time causing decay of the current. On the other hand the voltage on the storage node "0" will increase which imply the opening of the read transistor after a long time. This will cause an increase in the current.

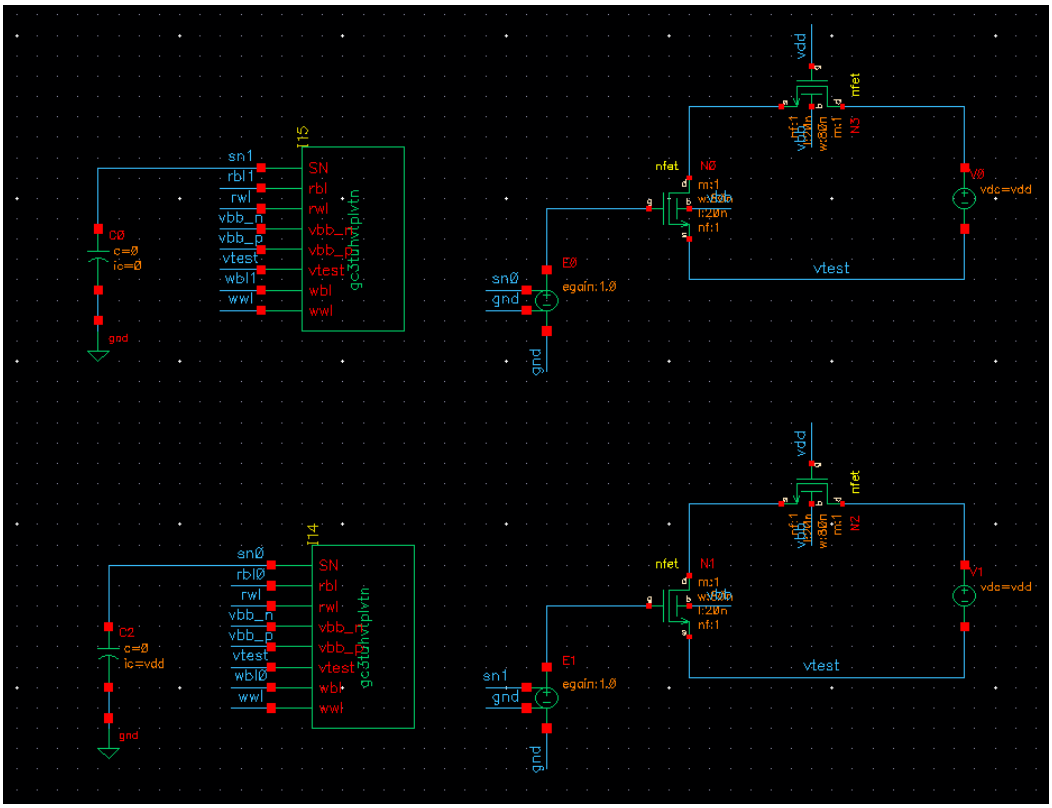


Figure 6.2: Idrt test bench

This test bench is interesting because it allows us to evaluate the performance of both the read transistor and write transistor. This test bench was used to choose between all transistor present in the library of 22nm. The result as explained in section 2 the write transistor be the Ultra High Voltage Threshold while for the read transistor the Low voltage Threshold was chosen due to the direct relationship between the voltage threshold and the speed of the circuit.

Even if this test bench is sufficient to choose and design the cell the next step is to evaluate the performance of the full memory cell. To do that it is impossible to

neglect the impact of the peripheral, consequently, the next step was to incorporate all peripheral on the next test bench.

6.1.3 Test bench final

As explained previously to have a real evaluation of the performance we need to incorporate the constraint generated by the peripheral. That why the last month of the master thesis was dedicated to creating a functioning model of the whole array. In the following picture, you can see the voltage follower, the Vref generator, sense amplifier enabler, the sense amplifier and the cell.

The major advantage of this test bench is that the evaluation of the performance can be done by reading the value at the output of the sense amplifier. This allows to make Monte Carlo simulation and have an estimation of the yield of the memory under all process corners. The Monte Carlo simulation was usually made with 1000 to 10000 design points. to perform this big simulation the laboratory lent me access to the dedicated computing system

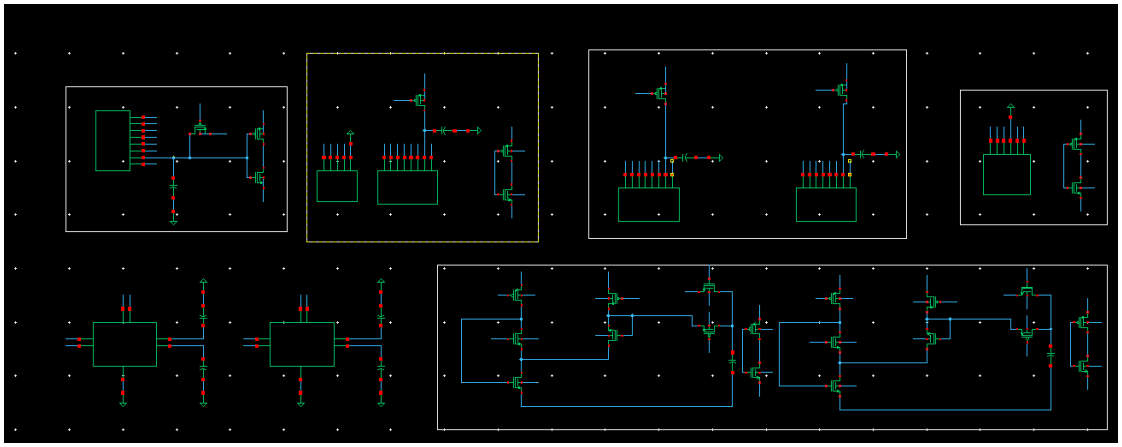


Figure 6.3: Test bench final

Most of the final results comes from this test bench, for instance, the impact of the power supply and the different biasing were performed on this schematic.

6.2 Results

6.2.1 Temperature impact

It s important to have an idea of how the memory cell will react to the temperature variation. The potential customer needs to know this parameter will impact the DRT because this has a direct impact on the application to which the GC-eDRAM. Consequently, a study was conducted on the Data Retention Time evolution versus the temperature on the IDRT test bench.

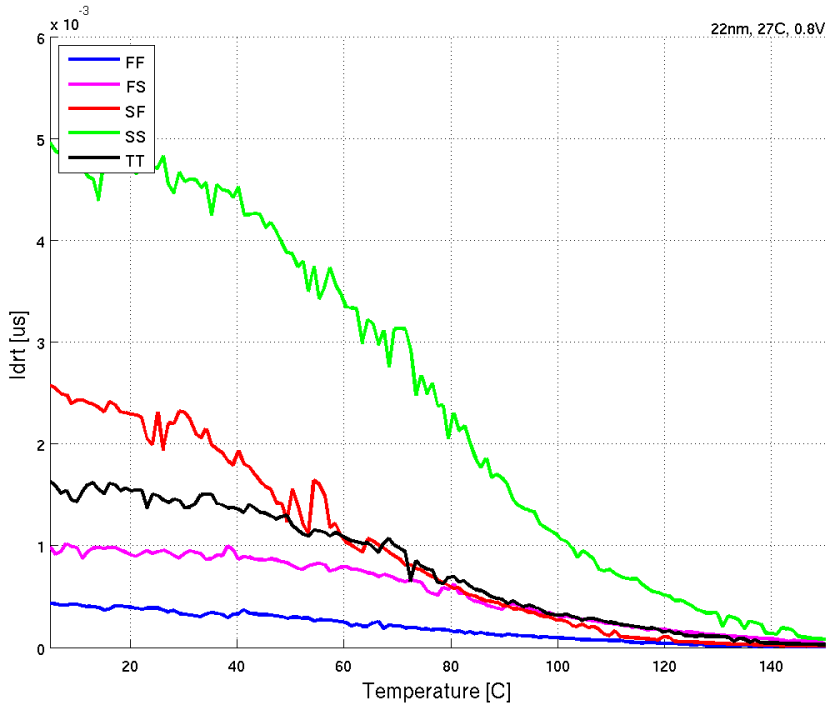


Figure 6.4: Evolution of Idrt versus temperature

From this, we can conclude that as expected the GC-eDRAM is sensitive to the temperature. It seems that the DRT is falling faster for a temperature superior to 40C. The least affected by this is the FF corner and the most affected one is SS.

6.2.2 Impact of Vdd

The study on the impact of the power supply is essential to the design of the memory. To perform this study all component have been studied individually to see where could come the issue. Finally, a study of yield at different retention time was conducted on the whole memory and so conclude on the performance of the memory under different voltage supply.

Level shifter

The first writing element of this study was the level shifter which is used to create a negative voltage on the WWL. The waveform plotted on the following figure represents the WWL after the level shifter for VDD = 0.8;0.6;0.4;0.4.

From this result, we can expect the level shifter to work well under all voltage supply. All the waveform show the expected waveform from the circuit: a square-like shape which goes to a negative voltage.

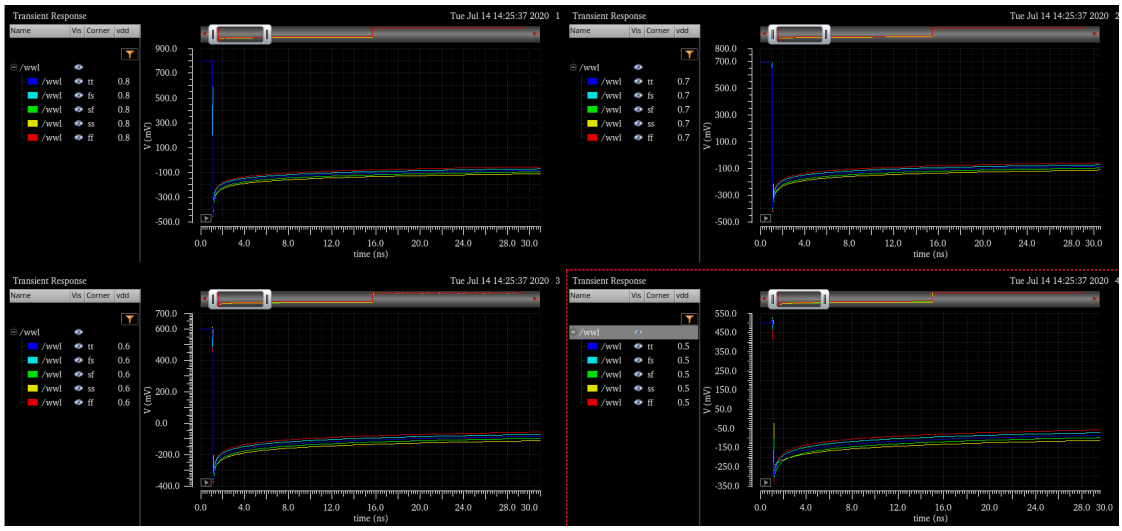


Figure 6.5: Waveform level shifter for vdd = 0.8,0.6,0.4,0.2V

But this is not sufficient to conclude on the performance of the level shifter. It is needed to look at the negative voltage created under all voltage supply to be sure that the circuit is still functioning under low voltage. Here it is plotted the negative voltage produced by the level shifter under all voltage supply possible.

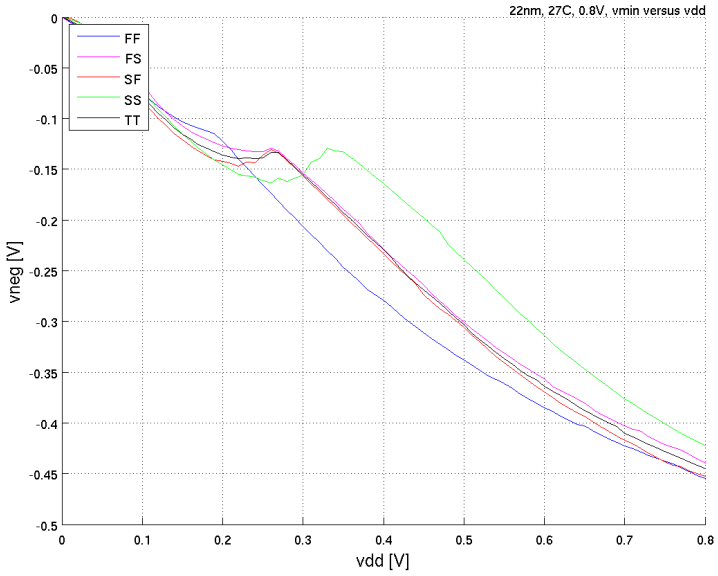


Figure 6.6: Negative voltage versus Vdd

From this result, we can conclude that the level shifter is functional under all voltage and is some error in the yield appear it does not come from this circuit

Voltage follower

The voltage follower is another essential component of the writing circuit. Once again the first thing that was studied is the waveform under different voltage. the input was a square-like wave and from this, it was observed that for a voltage lower than 0.3v the

voltage follower could not be considered as functioning. Here it is plotted the result for VDD = 0.8;0.6;0.4;0.4

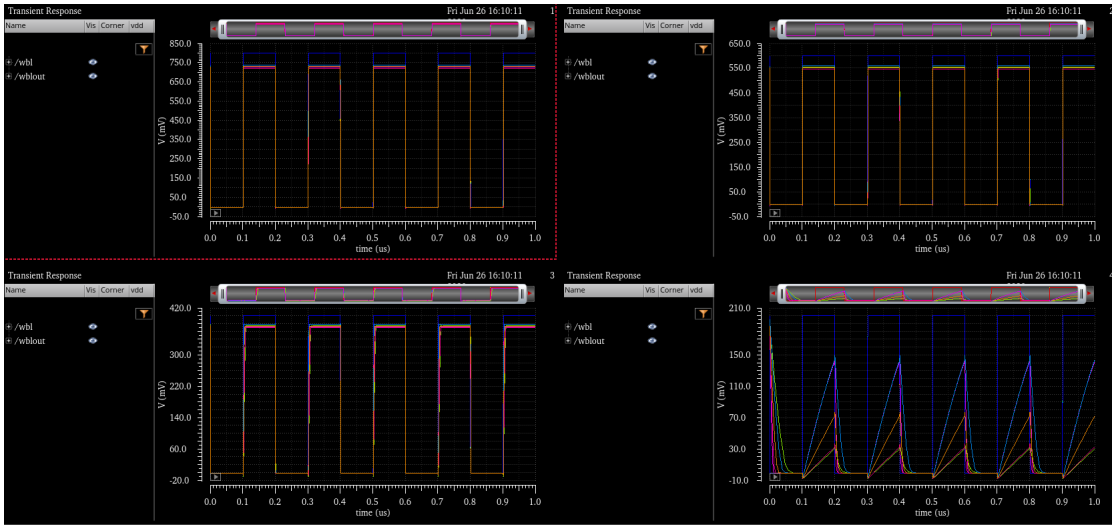


Figure 6.7: Voltage follower vdd waveform for Vdd = 0.8,0.6,0.4,0.2V

Thanks to the max gate added to the voltage follower it can always goe to 0v under all voltage. So to conclude on the performance the maximum value of the voltage follower versus the vdd was plotted

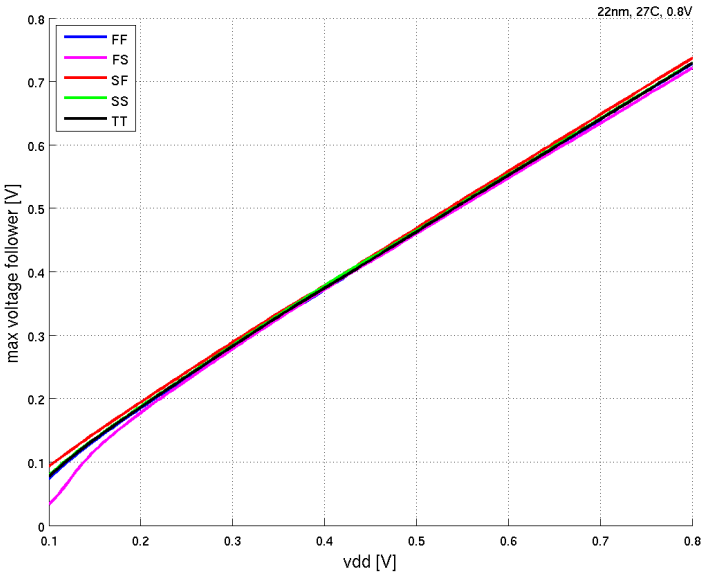
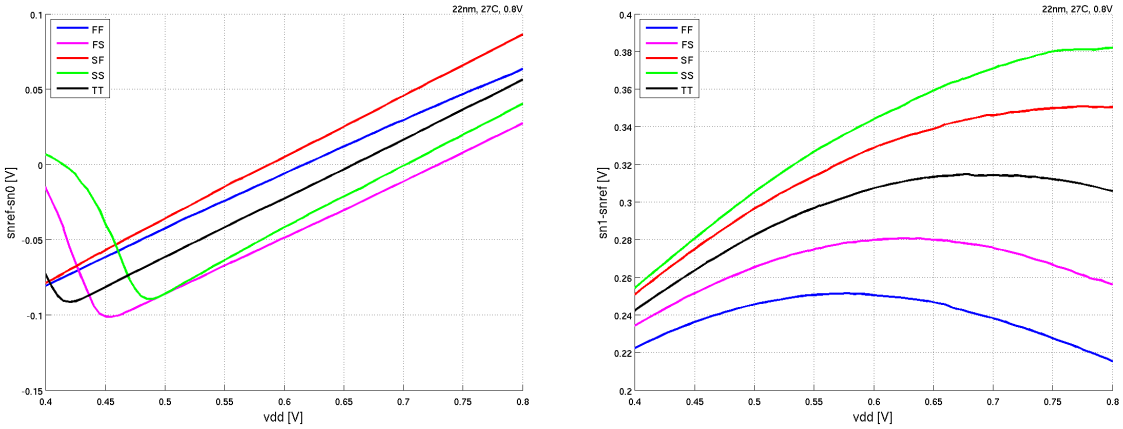


Figure 6.8: max of volatge follower vs vdd

This illustrates very well why it is needed to look both at the waveform and the characteristic of the circuit to conclude on its performance. If we look only at the maximum voltage we can conclude that the voltage follower is working under all supply voltage due to his linear dependence. But looking at waveform reveals that for lower voltage than 0.3V the waveform is erratic. This is not a major issue since our study is focusing on vdd going from 0.8V yo 0.4V.

Cell and Vref generator

The voltage dependence study of the cell and the voltage generator need to be separated in two-step to be relevant. First, we will look at the evolution of the difference of the storage node with the storage node of reference created by the equalizing circuit.

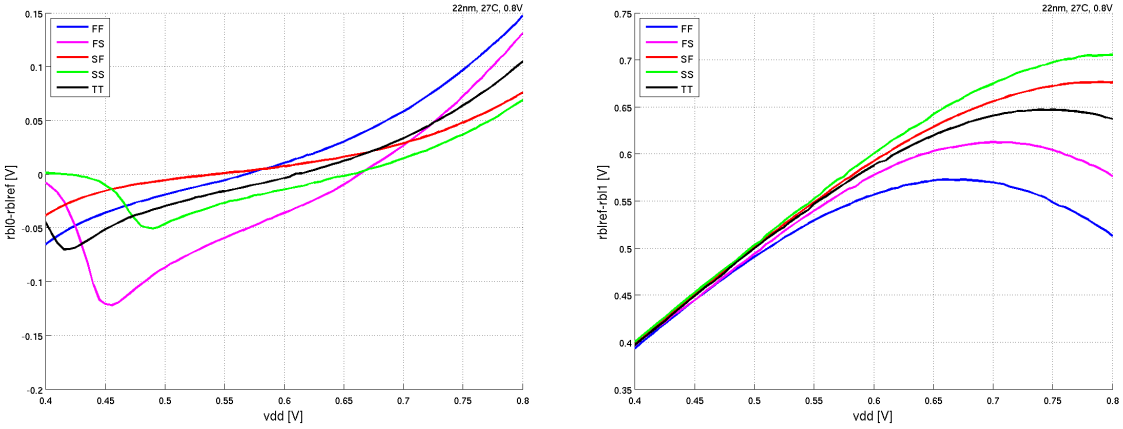


(a) snref-sn0 vs vdd **(b)** sn1-snref vs vdd

Figure 6.9: Storage node difference versus vdd at 5u

Surprisingly the difference between the storage node for the 1 is increasing when we decrease the voltage to then go to negative value when the supply voltage is 0.5V. On the other hand, the 0 is doing a lot worse it goes to a negative value for the voltage of 0.7V consequently it is expected to be the limiting factor. This issue is probably due to reference voltage generator which fails to generate a VDD/2 voltage at the reference cell.

But to be sure of the impact of Vdd we need to also look how does this impact the difference of RBL and it is done in the next plot.



(a) rbl0-rblref vs vdd **(b)** blref-rbl1 vs vdd

Figure 6.10: Rbl difference versus vdd at5u

It seems from this study that the limiting factor in voltage supply comes from the

cell since the difference of the RBL goes quickly under 0mV. This prevents the reading of 1 and 0 for the sense amplifier.

Replica column

The replica column should also adapt herself to the voltage supply, indeed when we reduce the voltage all the circuit become slower. Consequently, the delay between the RWL and the creation of the sense amplifier enable signal should also increase

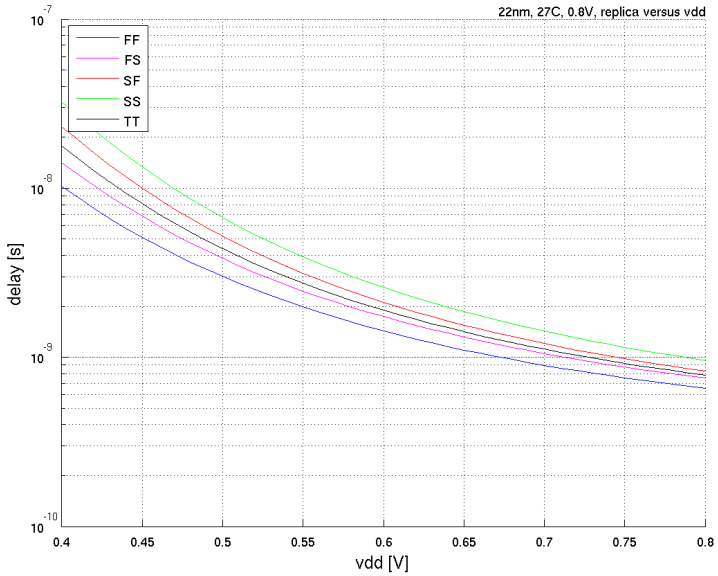


Figure 6.11: Replica column delay versus vdd

This is what we can observe in this plot. This concludes the study on the replica column which considered to be functional under all supply

Sense amplifier

To test the performance of the sense amplifier it was used two sense amplifier one in which it will be read a 1 and 0 on the other. This is done by using tow constant signal in with a difference of 50mv between each. This simulates the difference voltage that needs to be amplified through the sense amplifier. From the waveform, we can conclude that the sense amplifier is functional at all voltage. There is no deformation of the waveform and the 1 and 0 are always readable.

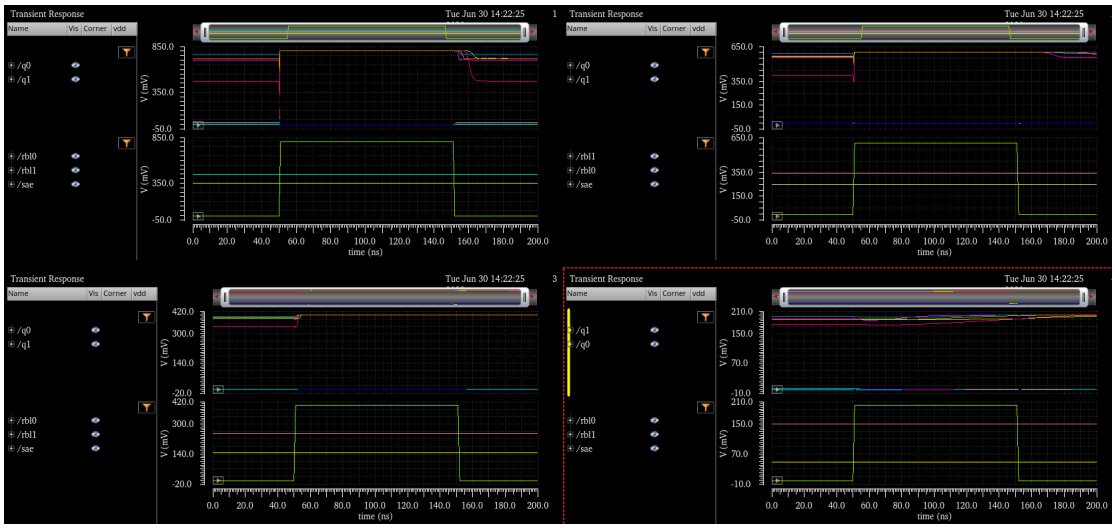


Figure 6.12: waveform sense amplifier 0.8,0.6,0.4,0.2V

To finalize the study Monte Carlo simulation were performed under different vdd and the yield is plotted in the next figure. It s important to notice that the yield of reading a 0 is always 100 so only the yield of reading a 1 is the constraint.

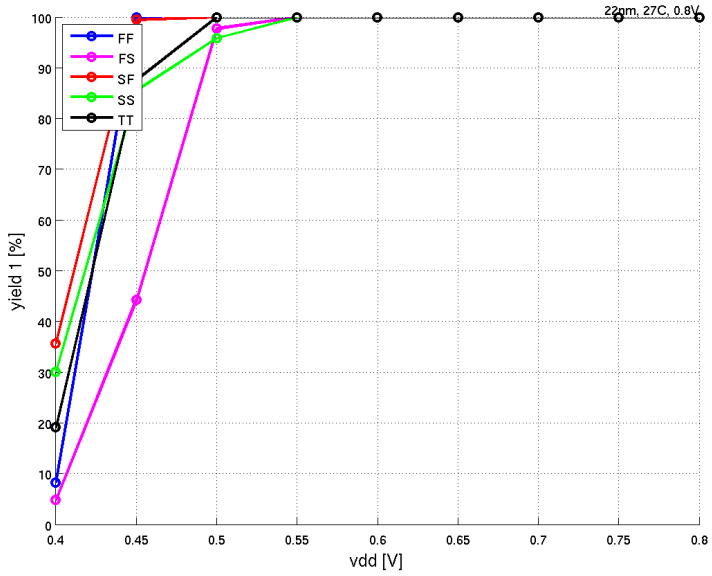
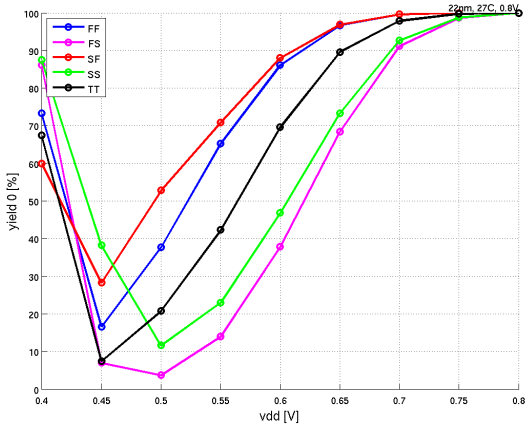


Figure 6.13: Impact vdd on sense amplifier yield

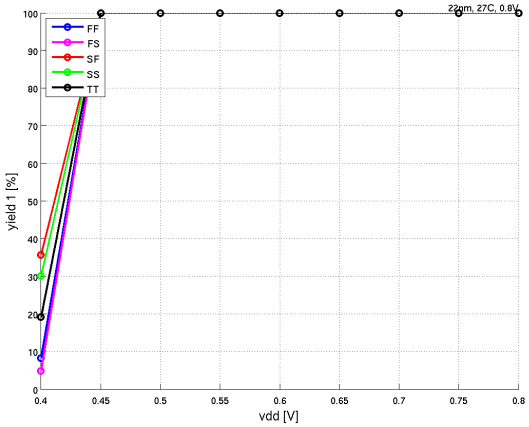
The yield is satisfying but it starts to decrease for a voltage lower than 0.55V. This will be the minimum for the sense amplifier in term of power supply.

Yield result

From this, we can now finish our study on the voltage supply with the yield of the whole array under different vdd and for the reading time of 5u,10u,25u.

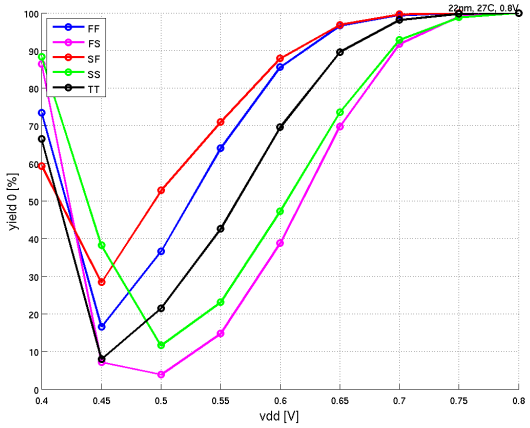


(a) Yield 0 evolution versus vdd at 5us

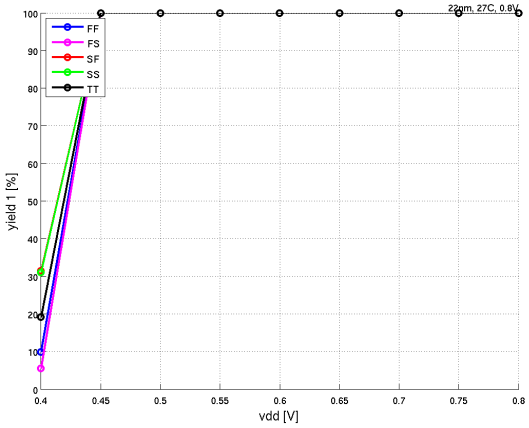


(b) Yield 1 evolution versus vdd at 5us

Figure 6.14: Yield evolution versus vdd at 5u

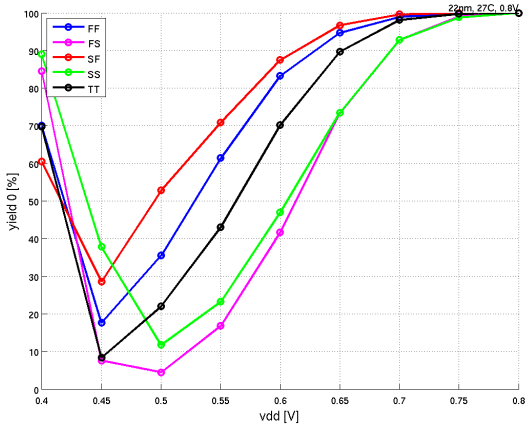


(a) Yield 0 evolution versus vdd at 10us

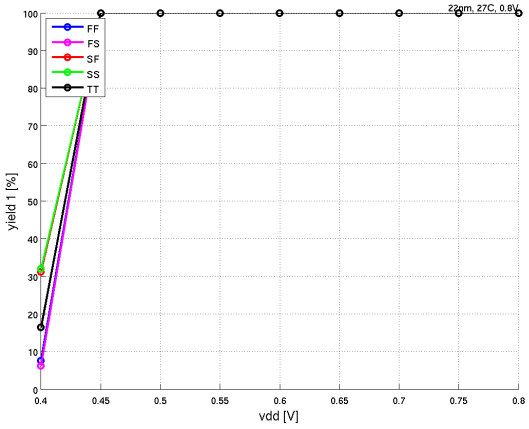


(b) Yield 1 evolution versus vdd at 10us

Figure 6.15: Yield evolution versus vdd at 10u



(a) Yield 0 evolution versus vdd at 25us



(b) Yield 1 evolution versus vdd at 25us

Figure 6.16: Yield evolution versus vdd at 25u

The yield is decreasing much faster for reading 0 than for reading a 0 this is due to the decrease in the difference of sn0-snref. From this, we can conclude that the voltage limit of the GC-eDRAM is 0.75V.

6.2.3 Timing simulation

The last characteristic that was evaluated was the minimum time needed to write and read with this memory. This will determine the maximum frequency at which the memory can operate, this an important characteristic of the memory. To do so the delay of the writing and reading cycle was estimated by a Monte Carlo simulation. Since much peripheral work in parallel the equation that allows determining the time is the following:

$$Writetime = t_{buffer} + t_{voltage_follower} + t_{memory_cell}$$

$$Readingtime = t_{equalizing} + t_{sae_generator} + t_{sense_amplifier}$$

The monte carlo simulation was performed with all the component of the array and for thousand point:

	Buffer	Voltage follower	Memory cell	Total
Writing time	48,7p	158,7p	87,0p	294,p

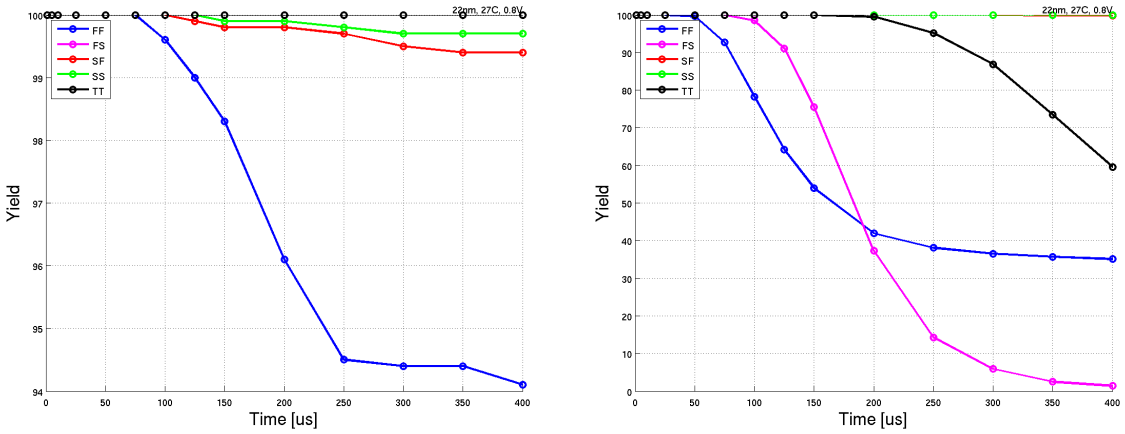
	Equalizing	Sae generator	Sense amplifier	Total
Reading time	43,51p	831,6p	151,3p	1026,41p

Figure 6.17: Timing simulation

We have a total writing time of 1.32041ns which gives us the maximum frequency of 757MHz which is a good result compare to the current state of the art in term of the operating frequency.

6.3 Yield versus time

The research work embodied in this thesis has addressed the problem of the optimisation of a memory cell GC-eDRAM and his peripheral. The final result of the yield degradation over time is the following



(a) Yield of 0 versus read time **(b)** Yield of 1 versus read time

Figure 6.18: Yield evolution over time

The maximum data retention time at which we can have both yields of 1 and 0 at maximum yield is 25us, this simulation was performed with a Monte Carlo simulation made of 1000 design points. This result concludes my thesis on the subject and it's the best result that was achieved through this semester of optimisation. It's a promising result due to the small place used for the memory and the low power supply used.

6.4 Summary

In this chapter, the limit of the memory cell in his final from have been tested. To do so the three test bench used during my master thesis: VDRT,IDRT and final test bench. From the result presented we can conclude that the memory is really sensible to the temperature. Especially when the temperature exceed 40 Celsius. So the cell can operate at room temperature but his not really fit too high temperature application.

The impact of the voltage supply was a big part of the study the peripheral and the cell have been tested individually and in group. The conclusion were that the limiting factor is the cell. In fact, this refrain the cell to be considered as functional for a voltage lower than 0.75V. But this is due to mainly to the degradation of the read of 0 in fact if we focus only the read of "1" the cell can operate up to a voltage of 0.45V. This issue is probably due to reference voltage generator which fails to generate a VDD/2 voltage at the reference cell.

The last study was the evolution of the yield versus the time of the read. This determine the data retention time maximal of the memory and in this case the best result that we obtained is 25us. This is mainly due to the quick deacrease of the yield on the FF process corner

Chapter 7

Conclusions and future directions

The research work presented in this thesis mainly results from simulation through virtuoso

7.1 Conclusions

to conclude on the work made in this master thesis I would say that it was a success. After the semester I was able to provide a working schematic of the memory cell and gain a considerable knowledge on the subject from the literature. From this it was possible to evaluate the yield, the DRT and the influence of temperature and power supply to the memory array. Moreover through different test bench that were also delivered, consequently it is possible to evaluate my design choice and maybe reuse them for further optimization. I was able to optimize both the peripheral and the cell, I proceeded down top approach from the memory cell to the peripheral. Consequently we can say that for this configuration the design is optimal.

The key result are that the memory was designed for the 22nm technology and the final data retention time was 25us. The best operation temperature is the room temperature. The memory cell and his peripheral can work from a voltage supply of 0.8V to 0.75V.

7.2 Scope for future studies

The GC-eDRAM technology is still far from being mature and lots of work could still be done to improve the performance. Moreover, my study on this technology node is not yet complete and other works on the subject can still be done.

- The nest step that need to be conducted in this study would be to add the layout to the schematic to have a precise value of the capacitance present on the gate. Morever it would give us more relevant result on the maximum operating frequency of the cell.

- The present research work can be extended to real-life implementation to verify the simulation result through experiment.

- The transistor technology is always changing and improving it surely would be interesting to try to develop this memory with other types of transistor.
- Currently the retention of 0 is a lot more efficient than the retention of a 1 it may be interesting to try a different approach to this phenomenon to improve the overall retention time o the memory.
- This application has a lot of potentials when it comes to a low voltage supply and I am sure that with more time and study it should be possible to increase the voltage range at which the memory can operate.

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ABSTRACT

The scaling down of the memory cell is goal push everyday further by the research. To achieve this goal the main alternatives are to use always smaller transistors or to innovate on the type of memory used. Among the different types dynamic random access memories (DRAMs), gain-cells embedded DRAM (GC-eDRAM) is a memory based on more compact cell than the conventional DRAM while being low power and CMOS compatible.

The main advantages of this type of memory cell is his small size, in fact it can be implemented with only two transistors. Being CMOS compatible allow this memory to scale down with the new innovation made on the transistors technology. In this work will be presented the implementation of this memory cell with the technologies node of the 22nm transistor. At a such small scale it will be presented the result of 6 month of simulation on the memory cell and of the peripheral that constitute the memory.

This work will show how we designed the memory cell and how the choice on the GC-eDRAM type cell was made. A study on the different transitors present on this technologies node was also conducted to find the best option while optimising the size and the power consummation of the memory

This cell imply a lot of challenges that need to be deal with due to the 22nm transistor, especially in term of leakage. Consequently this imply choice and compromise to overcome this difficulty. In this paper it will also be presented the techniques and choices made to optimise the memory cell and it's peripheral.

La réduction de la taille des cellule-mémoire est un objectif poussé chaque jour plus loin par la recherche. Pour atteindre cet objectif, les principales effort sont concentrer sur des transistors toujours plus petits ou d'innover sur le type de mémoire utilisée. Parmi les différents types de mémoires dynamiques à accès aléatoire (DRAM), la DRAM embarquée à cellules de gain (GC-eDRAM) est une mémoire basée sur une cellule plus compacte que la DRAM classique tout en étant de faible puissance et compatible CMOS.

Le principal avantage de ce type de cellule mémoire est sa petite taille, en fait elle peut être implémentée avec seulement deux transistors. Être compatible CMOS permet à cette mémoire de diminuer avec les nouvelles innovations faitent sur les technique de production des transistors. Dans ce travail sera présentée l'implémentation de cette cellule-mémoire avec la technologie transistor 22 nm. À une si petite échelle, il sera présenté le résultat de 6 mois de simulation sur la cellule-mémoire et des périphériques qui constituent la mémoire.

Ce travail montrera comment nous avons conçu la cellule-mémoire et comment le choix sur la cellule du type GC-eDRAM avons été faits. Une étude sur les différents transitors présents sur cette technologies a également été menée pour trouver la meilleure option tout en optimisant la taille et la consommation de puissance de la mémoire par cette cellule implique de nombreux défis à relever en raison du transistor 22 nm, notamment en matière de fuite de courant. Par conséquent, cela implique des choix et des compromis pour surmonter ces difficultés. Dans cet article, il sera également présenté les techniques et les choix effectués pour optimiser la cellule-mémoire et ces périphériques.