POLITECNICO DI TORINO

Master Thesis in Electrical Engineering

Single- and Three-phase on-board charger for Electric Vehicle

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Contents

Chapter 1

Aims and structure of the master degree thesis

This project is part of the FITGEN (Functionally Integrated e-axle ready for mass market Third GENeration electric vehicle), which is a project commissioned by the European commission. The Politecnico di Torino is in charge of developing the power electronics and the battery charger of the vehicle. So the aim of this master thesis is to develop a preliminary design that can be subsequently expanded and improved.

The structure of the considered solution is composed of a T-type converter as AC/DC stage and a LLC converter as DC/DC stage. In order to make the battery charger as adaptable as possible, both three- and single-phase supply system has been considered during the design, leading to a structure that can be used both in three- and single-phase configuration without changing in the internal components.

This master thesis is divided into the following chapters:

1. Aim of the thesis: to understand the motivation and the goal of the work
2. Introduction: analysis of the type of the battery charger and explanation of the proposed structure
3. Battery charger description: accurate analysis of the T-type and LLC conveter and of their control strategies

4. Preliminary design: it permits to choose the components of the two converters
5. Software simulation: it is used to check the parameters chosen during the design and to verify if the adopted control strategy are suitable for the application

Chapter 3

Analysis of the proposed structure

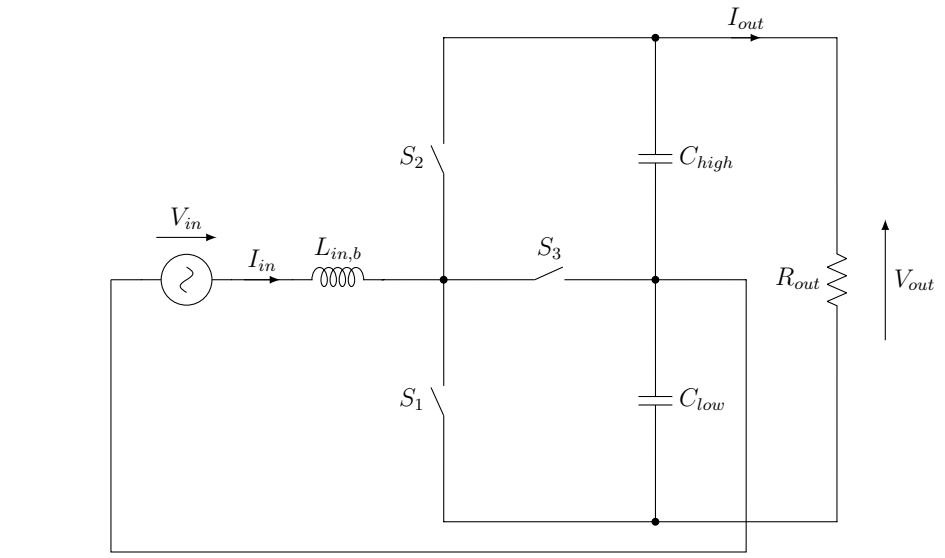
As the battery charger is composed of two cascaded power converters, in this chapter both of them are introduced and analyzed to illustrate their working principles and their control strategies. The goal here is to understand how the T-type converter and the LLC converter work individually and, finally, how they are working together forming the complete battery charger.

3.1 The unidirectional T-type converter

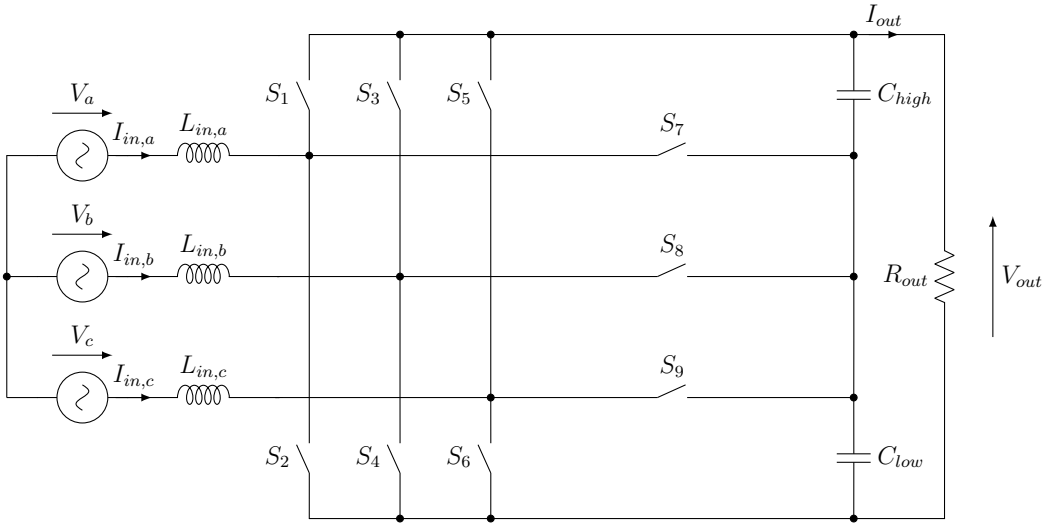
Analyzing the power flow from the grid to the battery pack, the first converter that is found is the T-type converter, which can assume both the single-phase and three-phase configurations (Figure 3.1).

Regardless of the configuration, the task of the T-type converter is to rectify the AC grid voltage to a DC form in the DC-link, while maintaining a unitary power factor seen from the grid. In this way it is possible to reduce harmonic distortion and its associated losses, improving the power quality at the battery charger input.

The proposed T-type structures are unidirectional in terms of power flow, so there are ideally just three active switches (S_1, S_8, S_9) in the three-phase configuration and one active switch (S_3) in the single-phase configuration. All the others switch are freewheeling diodes. simplifies the converter control strategy and



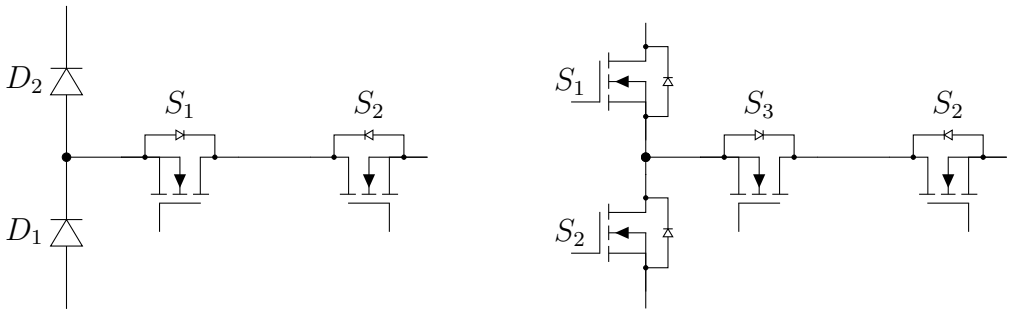
(a) Single-phase configuration



(b) Three-phase confuguration

Figure 3.1: T-type converter circuit scheme

reduces the number of components used for the control circuit. In fact, in bidirectional structures, diodes are replaced by active switches (Figure 3.2) giving a leg structure that requires more complicated control strategies, like 3-level Space Vector Modulation [3], and more driver circuit designed for high frequency. So, in the proposed structure, one leg of the rectifier presents two diodes and ideally one



(a) Unidirectional (b) Bidirectional

Figure 3.2: T-type leg structures

active switch, which in the real application is composed of two power MOSFETs driven by the same gate signal.

Besides the switches, there are also three input inductors (one per phase) that are used as current filters and two output capacitors used to filter the DC-link voltage V_{DC}. These two capacitors are identical, so the DC-link voltage is, in principle, divided into two equal parts on the two capacitors.

Depending on the configuration of the converter (single-phase or three-phase), two different control strategies are adopted that are described in the next paragraphs.

Finally, as in the control scheme the input voltage value is required, a Phase Locked Loop (PLL) must be implemented, both for single-phase and three-phase configurations.

3.1.1 Single-phase T-type converter

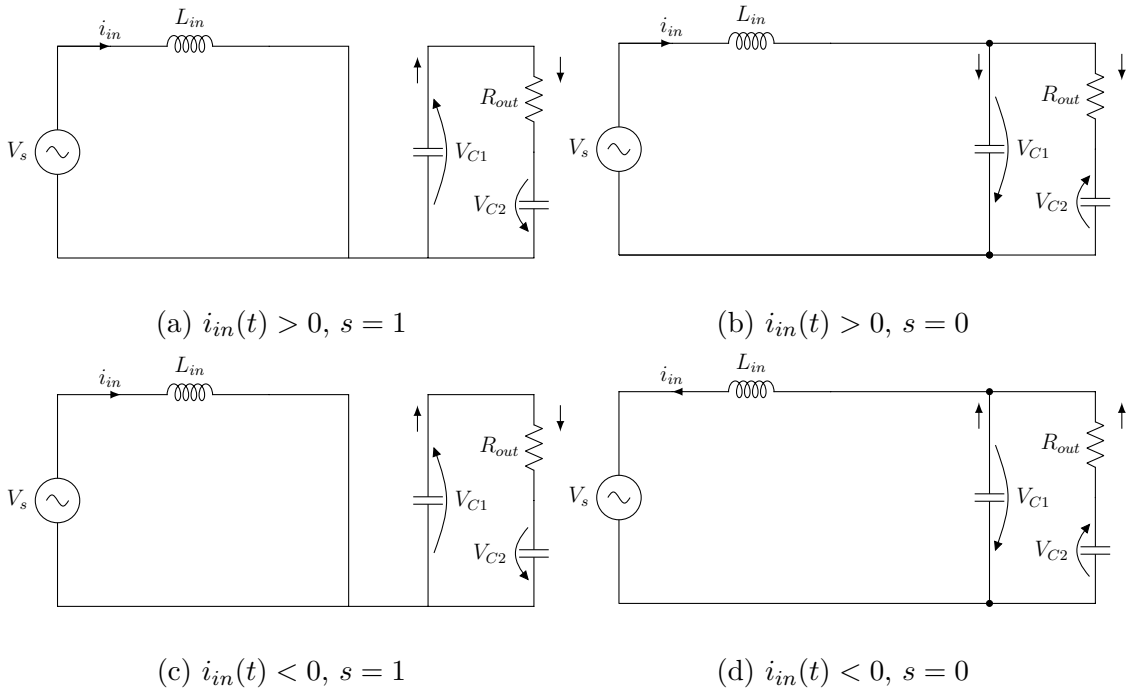
Driving the active switch (S_3) it is possible to regulate the voltage on the input inductor and consequently the current that flow through it. The voltage v_{Lx} applied to the input inductor of the phase x can assume different values depending on the input current direction and the gate signal $s_x(t)$ of the active switches ($s_x(t) = 1$

for closed active switches, $s_x(t) = 0$ for open active switches):

$$i_{in}(t) \geq 0 \Rightarrow v_{Lx}(t) = \begin{cases} v_{in} & \text{when } s_x(t) = 1 \\ v_{in} - \dfrac{V_{dc}}{2} & \text{when } s_x(t) = 0 \end{cases} \tag{3.1}$$

$$i_{in}(t) \leq 0 \Rightarrow v_{Lx}(t) = \begin{cases} v_{in} & \text{when } s_x(t) = 1 \\ v_{in} + \dfrac{V_{dc}}{2} & \text{when } s_x(t) = 0 \end{cases} \tag{3.2}$$

It is important to note that during one half of the current period just two voltage values of $v_{Lx}(t)$ are available so the complete structure behaves like two cascaded boost converters that work alternatively at each half waveform of the input current (Figure 3.3). This fact dictates an important restriction to be considered when designing the converter: the voltage applied to a single output capacitor must be higher than the input voltage peak value or, in other words, the DC-link voltage must be higher than the peak-to-peak input voltage.



(a) $i_{in}(t) > 0$, $s = 1$ (b) $i_{in}(t) > 0$, $s = 0$

(c) $i_{in}(t) < 0$, $s = 1$ (d) $i_{in}(t) < 0$, $s = 0$

Figure 3.3: T-type equivalent circuits depending on current direction and gate signal

Since the rectifier has to work as a PFC, guaranteeing a high power factor on the grid side, the grid voltage and current should always have the same sign. So, when the input voltage is positive the input current should be positive as well and if the active switch of the phase x is closed a positive voltage is applied to the input inductor and the current that flows through it tends to increase. Vice versa, if the active switch is closed a negative voltage is applied to the inductor and the current tends to decrease.
Analyzing the situation with a negative input voltage (so the input current is negative too), it could be found that the current behaves in a similar manner, with opposite sign. In both cases, when the active switch is closed the input current tends to increase in magnitude and when the active switch is open the current tends to decrease.

3.1.2 Cascaded current and voltage control loops

Normally, the T-type converter is controlled by two control loops (Figure 3.4). A inner current loop is used to drive the active switches in such a way that the input current results in phase with the input voltage, giving a unitary power factor (Figure 3.5) and the outer voltage loop impose the DC-link voltage value.

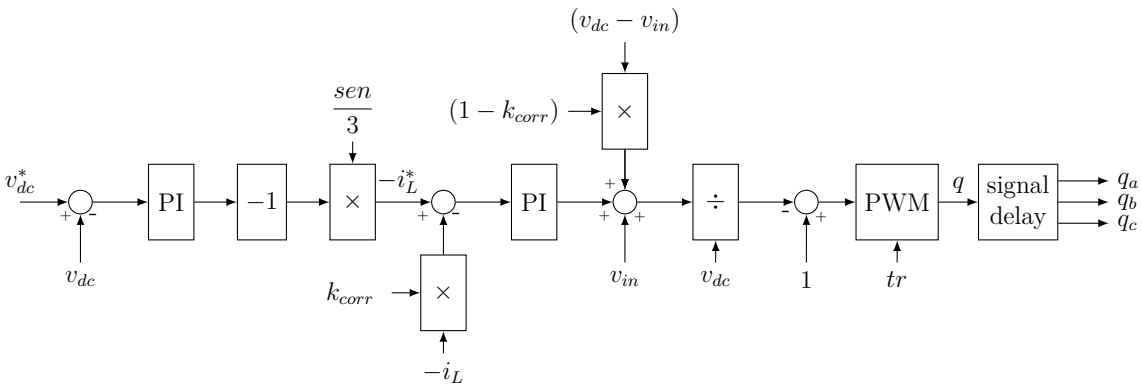


Figure 3.4: Complete control scheme of the single-phase T-type converter

The input of the control scheme is the desired DC-link voltage and the comparison with the measured value is sent to a PI regulator. Its output correspond to the desired input current value which represent the input of the current loop.

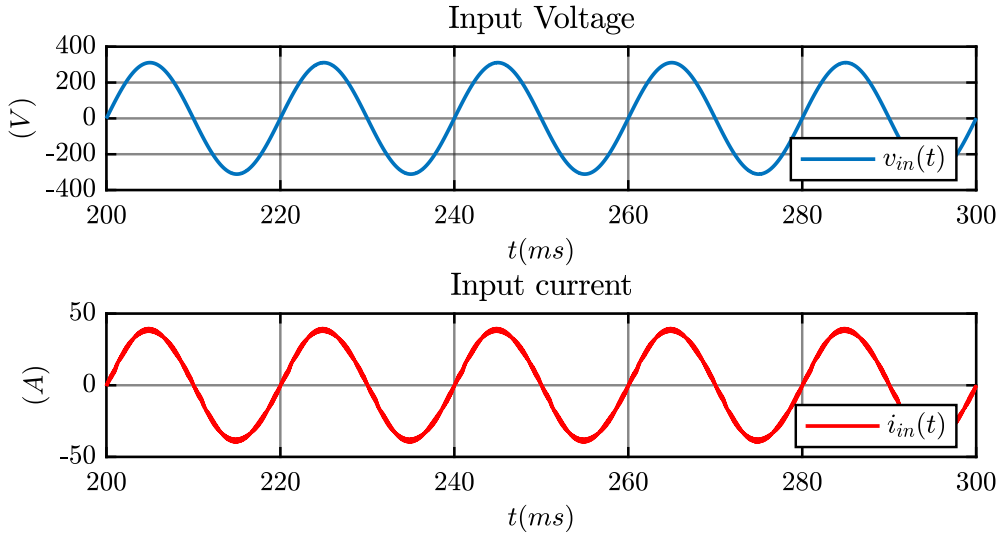


Figure 3.5: Typical input voltage and current waveforms for a PFC converter

A feed-forward signal, equal to the measured input voltage, is added to the output of the voltage regulator. The results is then divided by the voltage applied to the output capacitor and subtracted to 1, obtaining the required duty cycle. The gate signal q is generated using the PWM technique in which the duty cycle d is compared with a triangular wave that vary from 0 to 1. In order to use the same control scheme for both the situation with positive and negative input voltage, it is enough to change the construction of the signal v_x^* depending on the input voltage polarity:

$$v_{in}(t) \geq 0 \;\Rightarrow v_x^* = v_{Lin}^* + v_{in} \tag{3.3}$$

$$v_{in}(t) < 0 \;\Rightarrow v_x^* = -v_{Lin}^* - v_{in} \tag{3.4}$$

With this construction the duty cycle d can always be compared with the triangular wave in the right way. Furthermore, the signal v_{out} used to construct the duty cycle does not correspond to the output voltage of the T-type converter (the DC-link voltage) but it corresponds to the output voltage of the boost converter structures. Consequently, v_{out} is equal to $v_{c,high}$ when the input current is positive and to $v_{c,low}$ when the input current is negative.

The parameters $k_{p,i}$ and $k_{i,i}$ of the current PI can be set as following:

$$\omega_i = 2 \cdot \pi \cdot f_s \cdot 0.05 \tag{3.5}$$

$$k_{p,i} = \omega_i \cdot L_{in} \tag{3.6}$$

$$k_{i,i} = 0.1 \cdot \omega_i \cdot k_{p,i} \tag{3.7}$$

where:

- $fs[Hz]$: is the switching frequency
- $\omega_i[rad/s]$: is the current loop bandwidth, which is set to a value that corresponds to one tenth of the switching frequency
- $L_{in}[H]$: is the input inductance value

To complete the control scheme of the T-type converter, a outer voltage loop is added to the inner control loop. Its functions is to maintain the required DC-link voltage, which is the input of the voltage loop. The comparison with the actual DC-link voltage value is send to another PI regulator, which parameters are set as following:

$$\omega_v = 0.01 \cdot \omega_i \tag{3.8}$$

$$k_{p,v} = \omega_v \cdot C_{out} \tag{3.9}$$

$$k_{i,v} = 0.01 \cdot \omega_v \cdot k_{p,v} \tag{3.10}$$

where:

- $\omega_v[rad/s]$: is the voltage loop bandwidth, which is set to a value that corresponds to one tenth of the current loop bandwidth
- $C_{out}[F]$: is the capacitance value of the output capacitors

The voltage loop bandwidth is set to a value that is much less than the current loop bandwidth so the current reference signals can assume a more sinusoidal waveform. In fact, in this kind of application precision is more important than response time.

3.1.3 The Discontinuous Conduction Mode

As the current is controlled in order to assume a sinusoidal form, in the first and last instants of a half period of the fundamental frequency the Discontinuous Conduction Mode (DCM) may happen so the sampled current value does not correspond to the actual mean current value and could not be controlled in a right way. The DCM can occur when the current ripple is higher than the mean current. This can happen either for low average phase current or for high ripple systems (Figure 3.6).

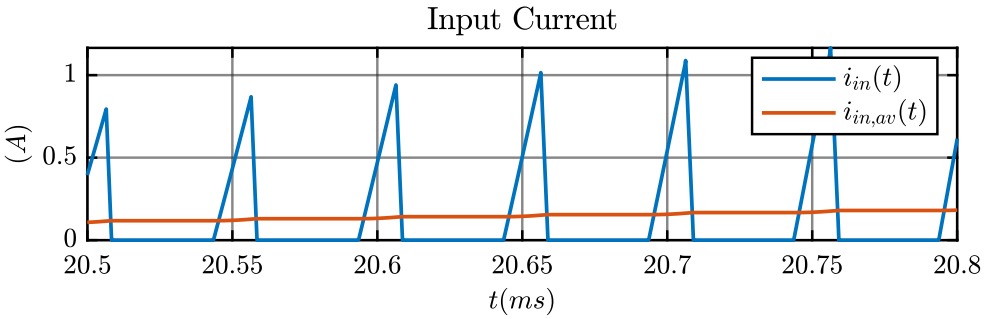


Figure 3.6: Current waveform in Discontinuous Conducting Mode (DCM)

During the DCM, the sampled current value must be corrected through the introduction of a corrective coefficient k_{corr} [6]:

$$k_{corr} = d \cdot \frac{v_{out}}{v_{out} - v_{in}} \tag{3.11}$$

The DCM must be taken into account also in the current control loop modifying the construction of the signal v_x^*:

$$v_{in}(t) \geq 0 \;\Rightarrow v_x^* = v_{Lin}^* + v_{in} + (1 - k_{corr}) \cdot (v_{out} - v_{in}) \tag{3.12}$$

$$v_{in}(t) < 0 \;\Rightarrow v_x^* = -v_{Lin}^* - v_{in} + (1 - k_{corr}) \cdot ((v_{out}) - v_{in}) \tag{3.13}$$

3.1.4 Interleaved single-phase T-type converter and current control with phase interleaving

Taking advantage of the three-phase input T-type power modules, the single-phase structure can become a single-phase inlet, three-leg interleaved T-type converter

(Figure 3.7). This structure introduces many advantages:

- adaptation of the converter to both single-phase and three-phase supply system
- lower current that flows through the inductors
- inductors of smaller size, dictated by the specs of the three-phase solution. A single leg single-phase inlet T-type converter would require an inductor of triple size, current wise

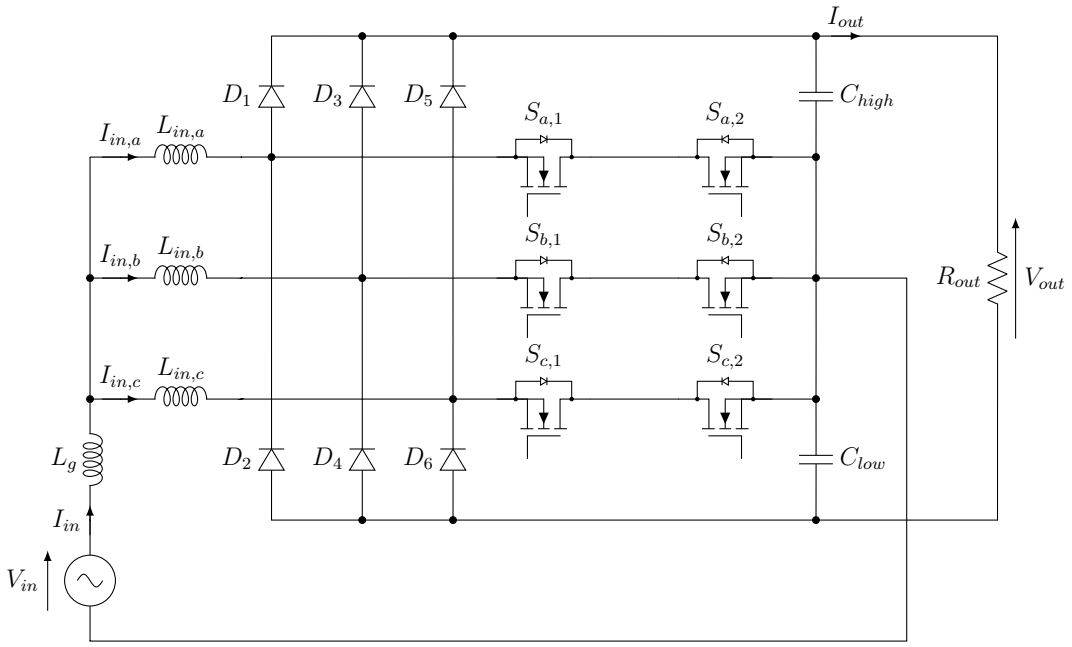


Figure 3.7: Proposed structure for the single-phase T-type converter

The easiest way to control this type of structure is to use the same gate signal for all the active switches, so the three phases behave like one single equivalent phase. However, it is possible to introduce an interleaving technique which consists in delaying in time the gate signals one from another by one third of the switching period (Figure 3.8). The instantaneous phase currents assume different values from each other, but the average value is the same for all of them.

For equal input inductance and switching frequency, the interleaving technique leads to a smaller ripple of the input current, so it is possible to satisfy the standards

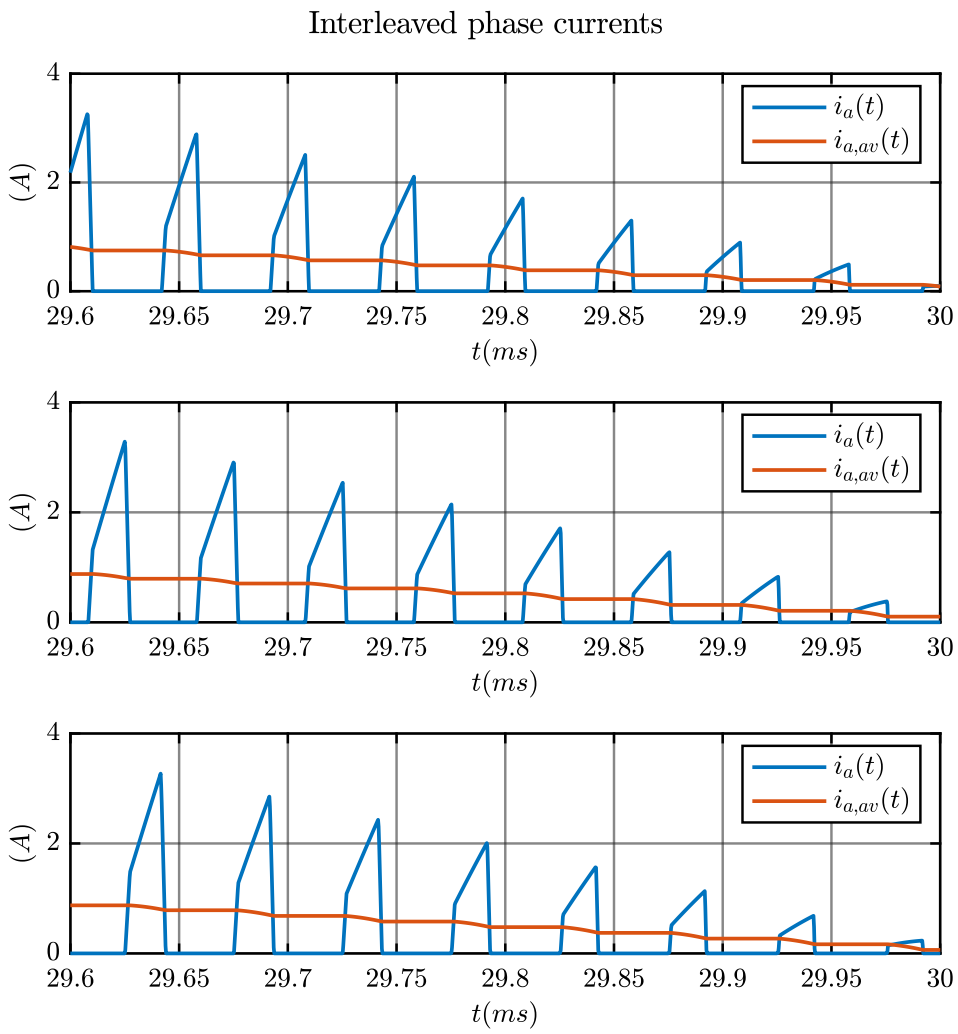


Figure 3.8: Phase currents waveforms with interleaved gate signals

requirements with smaller input inductors. The converter is also improved in terms of weight and volume. Due to this consideration, the interleaving technique is adopted for this work.

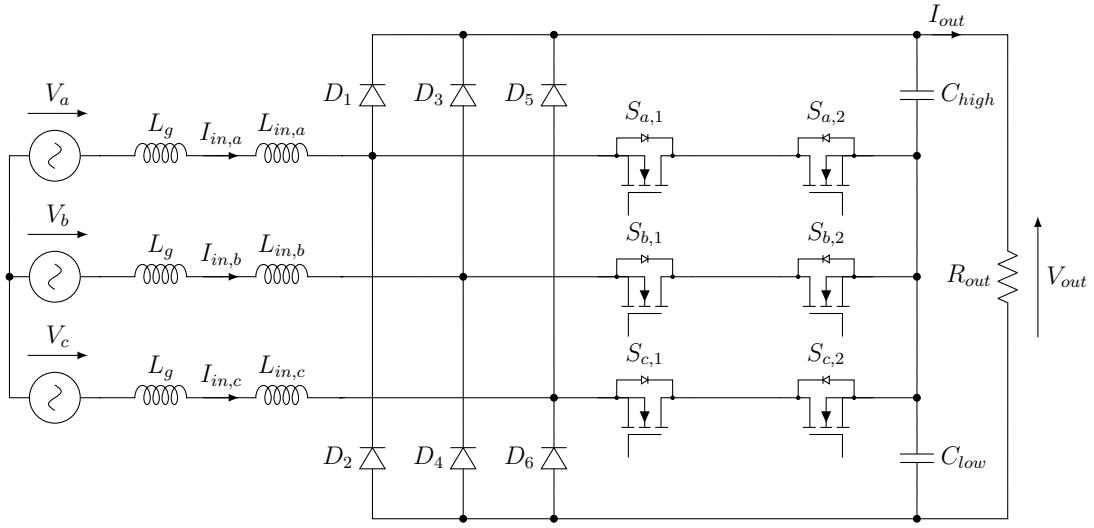


Figure 3.9: Proposed structure for the three-phase T-type converter

3.1.5 Control strategy for unidirectional three-phase T-type converter

Also for the three-phase T-type converter (Figure 3.9) the control is composed of a inner current loop and an outer voltage loop (Figure 3.10).

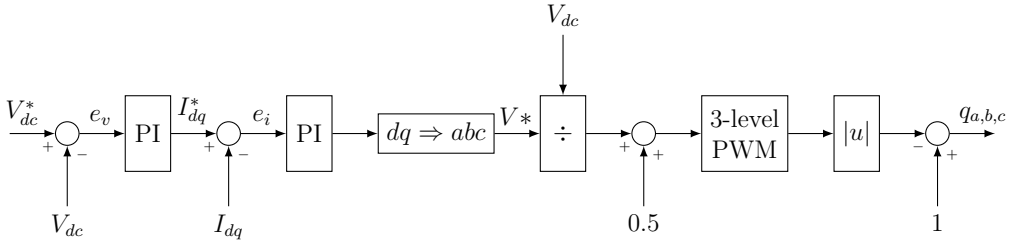


Figure 3.10: Control scheme for the three-phase T-type converter

First of all, the reference DC-link voltage value is compared with its actual value and the difference is set to the PI regulator of the voltage loop. The current control is implemented in dq coordinate, where the position of the d-axis is imposed by the phase of the grid voltage. The output of the voltage loop sets the reference id*, while iq* is set to zero for the sake of having grid current in phase with the grid voltage, and so obtaining unitary power factor.

The reference current values must be compared with the actual values, so the measured 3-phase currents are transformed into dq components by using Clarke and Park transformations:

$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{3.14}$$

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = \begin{bmatrix} cos(\omega t) & sin(\omega t) & 0 \\ -sin(\omega t) & cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} \tag{3.15}$$

Of course, the homopolar component is not used in the control scheme.

the difference between desired and measured dq current components is sent to the PI regulators of the current loop. Its output is composed of the required voltage in *dq* coordinates so, before to be compared with the triangular wave of the PWM modulation, they are reported in *abc* coordinates using the inverse transformations:

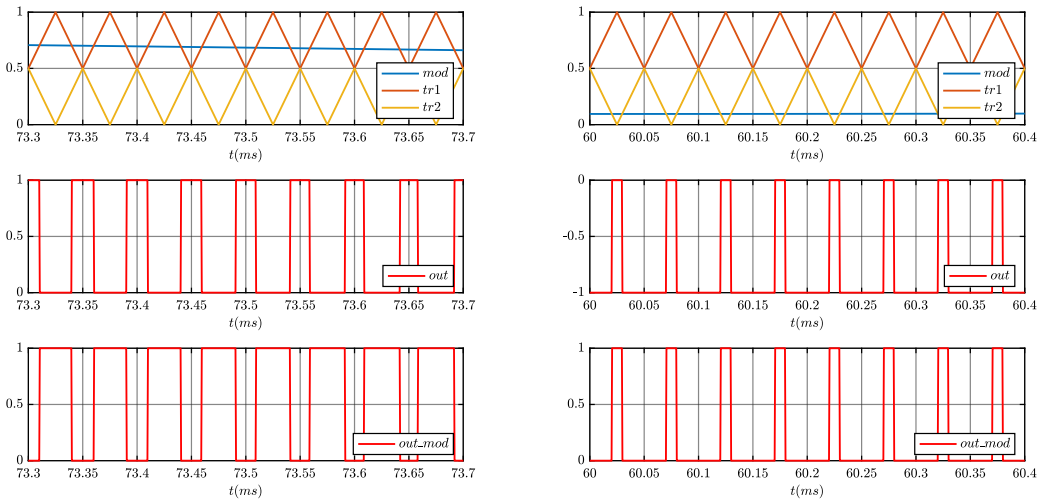
$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = \begin{bmatrix} cos(\omega t) & -sin(\omega t) & 0 \\ sin(\omega t) & cos(\omega t) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \tag{3.16}$$

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & 1 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & 1 \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} \tag{3.17}$$

The modulating signal is created dividing the output of the current regulator by the DC-link voltage value. The modulation uses a Three-level PWM, which output signals can be either -1, 0 or 1 and they normally correspond to three different voltage levels. However, the only active switches that can be driven are the middle ones so the gate signals must be modified.

In the proposed structure the modulating signals $v_{xm}*$ tend to increase in amplitude when the current error e_i tends to increase too. Consequently, if the output signals of the PWM were directly used to drive the active switches without being modified they would create a voltage value v_{xm} that decreases the phase current. Therefore, the control would try to increase the current amplitude, but the actuator tends to decrease it.

Due to the above consideration, the PWM output signals are modified in such a way that when the control want to increase the input current amplitude, the duty cycle of the middle active switch is increased (Figure 3.11).



(a) $v_x^*(t) > 0$ (b) $v_x^*(t) < 0$

Figure 3.11: Three-level PWM: triangular carriers, modulating signal, non-modified and modified outputs

The PI regulators are tuned in the same way as for the single-phase configuration ((3.5) to (3.7) and (3.8) to (3.10)).

3.1.6 PLL scheme for single-phase T-type converter

The control scheme of the T-type converter requires to retrive of the input voltage sine waveform in both single-phase and three-phase configurations. In the single-phase configuration the signal is used to form the current loop input and in the

three-phase configuration it is used for Clarke and Park transformations. The reconstruction of the input voltage signal is made by a Phase Locked Loop (PLL), which is composed of a closed loop system that keeps the time of some external periodical signal using the feedback loop. The scheme of the PLL is different depending on the system configuration.

The PLL scheme for single-phase systems (Figure 3.12) is composed of three fundamental blocks [14]:

- *Phase Detector (PD)*: this block generates an output ε_{PD} that is proportional to the phase difference between the input signal and the signal generated by an internal oscillator

- *Loop Filter (LF)*: this block is a low-pass filter used to reduce the high frequency components of the signal generated by the PD and in this work it is constituded by a PI controller

- *Voltage-Controlled Oscillator (VCO)*: this block generates a signal that is phase shifted with respect to a given central frequency ω_c and that depends on the signal v_{LF} provided by the LF block

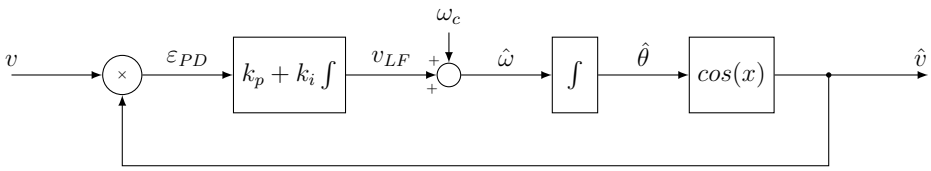


Figure 3.12: PLL scheme for single-phase T-type converter

The input signal applied to the PLL is the input measured voltage:

$$v = Vsin(\theta) = Vsin(\omega t + \phi) \tag{3.18}$$

and the output signal generated by the VCO block is given by:

$$v' = cos(\hat{\theta}) = cos(\hat{\omega} + \hat{\phi}) \tag{3.19}$$

The phase error at the PD block output can be calculated as follow:

$$\begin{aligned}\epsilon_{PD} &= V sin(\omega t + \phi) cos(\hat{\omega} t + \hat{\phi}) \\ &= \frac{V}{2}\Big[sin\big((\omega - \hat{\omega})t + (\phi - \hat{\phi})\big) + sin\big((\omega + \hat{\omega})t + (\phi + \hat{\phi})\big)\Big]\end{aligned} \tag{3.20}$$

The second term between parenthesis represents the high frequency component of the PD output signal and it is attenuate by the PI regulator so it is possible to consider just the low frequency term of the signal. In this way it is possible to consider the ε_{PD} signal as follow:

$$\bar{\varepsilon}_{PD} = \frac{V}{2} sin\big((\omega - \hat{\omega})t + (\phi - \hat{\phi})\big) \tag{3.21}$$

Assuming that the PLL is well tuned, the frequency at the output of the oscillator is very closed to the frequency of the input signal ($\hat{\omega} \approx \omega$) it is possible to further simplify the phase error signal:

$$\bar{\varepsilon}_{PD} = \frac{V}{2} sin(\phi - \hat{\phi}) \tag{3.22}$$

When the phase error is very small it is possible to linearize (3.22):

$$\bar{\varepsilon}_{PD} = \frac{V}{2}(\phi - \hat{\phi}) \tag{3.23}$$

The average frequency of is given by:

$$\hat{\bar{\omega}} = \omega_c + \bar{v}_{LF} \tag{3.24}$$

while the small signal variation is given by:

$$\tilde{\hat{\omega}} = \tilde{v}_{LF} \tag{3.25}$$

Finally, the variations in the phase-angle detected by the PLL can be calculated

by:

$$\tilde{\hat{\phi}}(t) = \int \tilde{\hat{\omega}} dt = \int \tilde{v}_{LF} dt \tag{3.26}$$

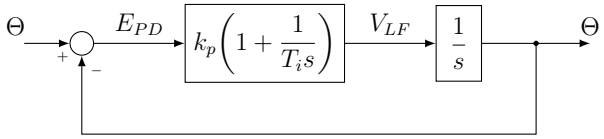


Figure 3.13: Small signal model of PLL for single-phase T-type converter

With these equations it is possible to construct the small signal model of PLL in Laplace domain (Figure 3.13). The closed loop transfer function in the normalized form is given by:

$$H_\phi(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.27}$$

where:

$$\omega_n = \sqrt{\frac{k_p}{T_i}} \qquad \zeta = \frac{\sqrt{k_p T_i}}{2}$$

As 3.27 represents a second order transfer function, the settling time t_s responding to a step input can be approximated by:

$$t_s = 4.6\tau \tag{3.28}$$

where:

$$\tau = \frac{1}{\zeta\omega_n} \tag{3.29}$$

These expressions can be used to tune the PI controller:

$$k_p = 2\zeta\omega_n = \frac{9.2}{t_s} \tag{3.30}$$

$$T_i = \frac{2\zeta}{\omega_n} = \frac{t_s\zeta^2}{2.3} \tag{3.31}$$

If the amplitude input voltage is different from 1, the parameters in 3.31 must be divided by the actual input voltage amplitude V. Furthermore, it is worth to remember that these expressions are just a guide to tune the PI controller and they can be modified in order to obtain better parameters values.

3.1.7 PLL scheme for three-phase T-type converter

The PLL scheme adopted for the three-phase configuration (Figure 3.14) is not so different from the previous one.

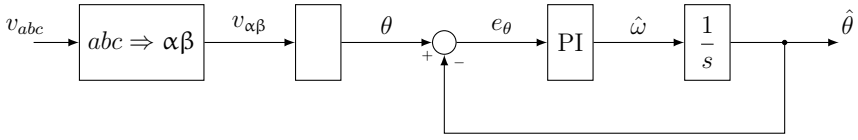


Figure 3.14: PLL scheme for three-phase T-type converter

In this configuration, the input of the PLL is composed of the measured input voltages v_{abc} which are transformed using Clarke transformation to obtain the components $v_{\alpha\beta}$. The components referred to the $\alpha\beta$ coordinate system are used to computed the phase angle θ (Figure 3.15).

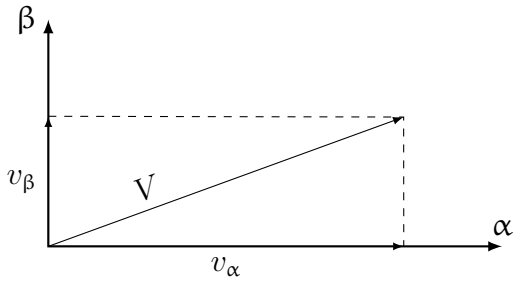


Figure 3.15: Representation of the voltage space vector in $\alpha\beta$ coordinates system

So, starting from $v_{\alpha\beta}$ it is possible to write:

$$V = \sqrt{v_\alpha^2 + v_\beta^2} \tag{3.32}$$

$$\cos\theta = \frac{v_\alpha}{V} \tag{3.33}$$

$$\sin\theta = \frac{v_\beta}{V} \tag{3.34}$$

Assuming that the PLL is well tuned, the difference between real and estimated voltage angle ($\theta - \hat{theta}$) is very small. So the phase angle error e_θ can be calculated by using:

$$e_\theta = \theta - \hat{\theta} \approx sin(\theta - \hat{\theta}) = sin\theta cos\hat{\theta} - cos\theta sin\hat{\theta} \tag{3.35}$$

(3.35) permit to avoid the discontinuities due tho the value of the voltage angle, which vary from 0 to 2π. The error e_θ is sent to a PI regulator which parameters are set as follow:

$$\omega_{PLL} = 2 \cdot \pi \cdot f_s \cdot 0.1 \tag{3.36}$$

$$k_{p,PLL} = \omega_{PLL} \tag{3.37}$$

$$k_{i,PLL} = k_{p,PLL} \cdot 0.1; \tag{3.38}$$

The output of the PI regulator is adopted as estimated pulsation $\hat{\omega}$. This signal is integrated to obtain the estimated phase angle $\hat{\theta}$ and its components $cos\hat{\theta}$ and $sin\hat{\theta}$, used as feedback. Once obtained $cos\theta'$ and $sin\theta'$, these components are used for the Park transformations in the three-phase T-type control scheme.

3.2 LLC converter

The LLC converter (Figure 3.16) is a DC/DC converter which functioning is based on the resonant interaction between the reactive components of the resonant tank.

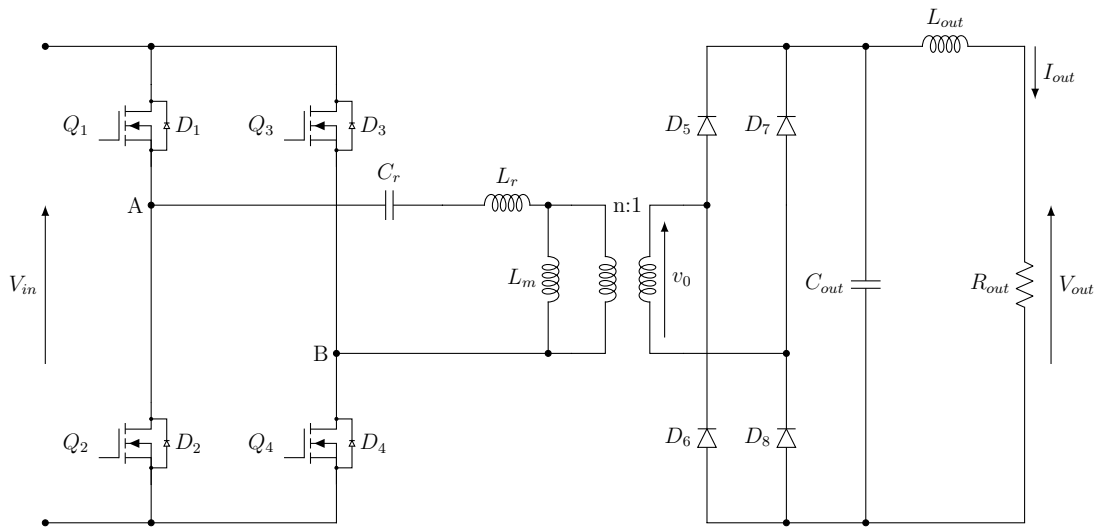


Figure 3.16: LLC converter

The bridge inverter is controlled with a constant duty cycle $d = 0.5$, so the voltage at the resonant tank terminals has a square waveform with magnitude equal to $V_{dc}/2$ and variable frequency.

3.2.1 First Harmonic Approximation

A good way to understand the working principle of the LLC converter is to use the First Harmonic Approximation (FHA) which gives a easy procedure and an easy model that represent the complete converter.

First of all, the FHA consider just the fundamental of the input square wave, so it is possible to assume that the resonant tank is supplied by an AC sinusoidal voltage source which amplitude is equal to:

$$V = \frac{2}{\pi} V_{DC} \tag{3.39}$$

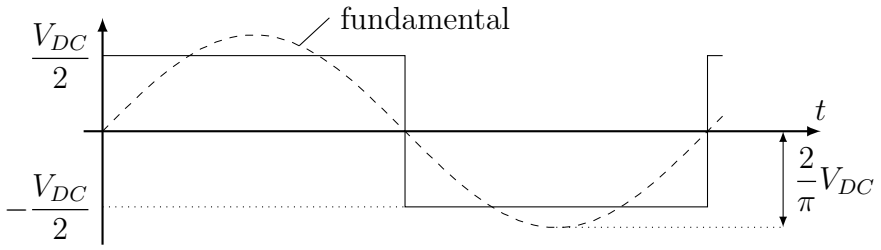


Figure 3.17: Representation of a square wave and its fundamental component

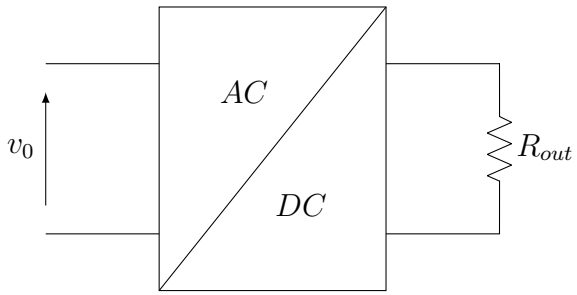


Figure 3.18: Load model

where V_{DC} is the value of the DC-link voltage. V represent the amplitude of the fundamental harmonic component of a square wave that vary from $-V_{DC}/2$ and $+V_{DC}/2$ (Figure 3.17). The rms value of the voltage source is then given by:

$$V_{in,rms} = \frac{\sqrt{2}}{\pi} V_{DC} \tag{3.40}$$

The load of the converter is composed of a single phase diode bridge and a battery pack, which can be modeled by a resistance (Figure 3.18). The output power can be expressed by:

$$P_{out} = V_{out} \cdot I_{out} \tag{3.41}$$

Using the FHA it is possible to write the voltage v_0 as a function of the amplitude of V_{out}:

$$v_0 = \frac{4}{\pi} V_{out} sin(2\pi f t - \phi) \tag{3.42}$$

where ϕ is the phase shift with respect to the input voltage. The rms value can be obtained by:

$$v_{0,rms} = \frac{2\sqrt{2}}{\pi} V_{out} \tag{3.43}$$

The value of the output current I_{out} corresponds to the mean value of the current rectified by the bridge rectifier:

$$I_{out} = \frac{2\sqrt{2}}{\pi} i_{0,rms} \tag{3.44}$$

at this stage the load will be modeled as a resistance, the output current is in phase with the output voltage so it is possible to calculate the equivalent resistance value at the bridge rectifier input:

$$R_{0,sec} = \frac{v_{0,rms}}{i_{0,rms}} = \frac{\frac{2\sqrt{2}}{\pi} V_{out}}{\frac{\pi}{2\sqrt{2}} I_{out}} = \frac{8}{\pi^2} R_{out} \tag{3.45}$$

To complete the model of the LLC converter, this analysis considers also the transformer ratio n to transport the value of the equivalent resistance to the primary side:

$$R_{0,eq} = n^2 \frac{8}{\pi^2} R_{out} \tag{3.46}$$

Based on (3.41), the equation 3.46 can be rewritten as:

$$R_{0,eq} = n^2 \frac{8}{\pi^2} \frac{V_{out}^2}{P_{out}} \tag{3.47}$$

Using the expression of the equivalent output resistance and the fundamental component of the input voltage it is finally possible to draw the equivalent circuit of the LLC converter (Figure 3.19).

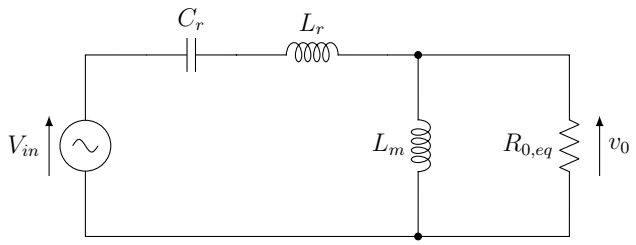


Figure 3.19: Equivalent circuit of the LLC converter using the FHA

3.2.2 Voltage transfer function of the LLC converter

Once the equivalent circuit of the LLC converter is retrived, the next step is to understand how the resonant tank affect the behavior of the transfer function between output voltage and input voltage.

The voltage gain $\bar{M}$ is given by the ratio of the output and input voltage, which are characterized by a magnitude and a phase. Consequently, also the voltage gain has its magnitude and phase and, as for the voltages, it can be represented by a complex number:

$$\bar{M} = n\frac{\bar{V}_0}{\bar{V}_{in}} \tag{3.48}$$

From now on, the analysis consider the a unitary turn ratio n. The results for different turn ratio value can be easily retrived accordingly. Considering the structure of the equivalent circuit, it is possible to write:

$$\bar{M} = \frac{1}{\frac{1}{s^2 C_r L_m} + \frac{1}{sC_r R_{0,eq}} + \frac{L_r}{L_m} + s\frac{L_r}{R_{0,eq}} + 1} \tag{3.49}$$

where s is the Laplace variable. The aim of the discussion is to find the Bode plot of $\bar{M}$, so s is replaced by$j\omega$:

$$\bar{M} = \frac{1}{-\frac{1}{\omega^2 C_r L_m} + \frac{1}{j\omega C_r R_{0,eq}} + \frac{L_r}{L_m} + j\omega\frac{L_r}{R_{0,eq}} + 1} \tag{3.50}$$

for better comprehension of the analysis, it is useful to define the following quantities:

- first resonance frequency:

$$f_{r,1} = \frac{1}{2\pi\sqrt{C_r}L_r} \tag{3.51}$$

- second resonance frequency:

$$f_{r,2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{3.52}$$

- characteristic impedance:

$$Z_0 = \sqrt{\frac{L_r}{C_r}} = \frac{1}{2\pi f_{r,1}C_r} = 2\pi f_{r,1}L_r \tag{3.53}$$

- quality factor:

$$Q = \frac{Z_0}{R_0} = \frac{\pi^2}{8}\frac{I_{out}}{n^2 V_{out}}Z_0 = \frac{\pi^2}{8}\frac{P_{out}}{n^2 V_{out}^2}Z_0 \tag{3.54}$$

- inductance ratio:

$$\ell = \frac{L_r}{L_m} \tag{3.55}$$

- normalized frequency:

$$f_n = \frac{f}{f_{r,1}} \tag{3.56}$$

With these definitions, in is possible to write 3.50 in the following way:

$$\bar{M} = \frac{1}{\left(1 + \ell - \frac{\ell}{f_n^2}\right) + jQ\left(f_n - \frac{1}{f_n}\right)} \tag{3.57}$$

The voltage gain $\bar{M}$ is functions of three variables:

$$\bar{M} = f(f_n, Q, \ell) \tag{3.58}$$

As the amplitude of $\bar{M}$ represent the voltage gain, it is important to find its expression and to understand how the parameters of the LLC converter affect its characteristic. The amplitude of $\bar{M}$ can be computed from 3.57:

$$M = \frac{1}{\sqrt{\left(1 + \ell - \frac{\ell}{f_n^2}\right)^2 + Q^2\left(f_n - \frac{1}{f_n}\right)^2}} \tag{3.59}$$

the inductance ratio depends on the selected hardware and can be considered constant during operation. The voltage gain M depends on the switching frequency and on the quality factor Q (Figure 3.20). For small value of Q the peak of voltage gain, which occur at the second resonance frequency, is bigger while the amplitude at the first resonance frequency does not depend on the quality factor and it is always equal to 1. Moreover, when Q is small the characteristic is more sensitive to frequency variations for low f_n, but if the frequency is higher than the first resonance frequency the characteristic is flatter and it needs higher frequency values to reach a lower M value with respect to a characteristic with higher Q. In other words, if the value of Q is high the peak of voltage gain is smaller, but the characteristic does not require high frequency values to reach lower voltage gain.

For the sake of sizing the hardware components it is useful to plot the M characteristic for a fixed Q and different ℓ (Figure 3.21). For higher values of inductance ratio, higher voltage gains can be reached. However, high values of ℓ mean lower values of the magnetizing inductance L_m which causes an increase of the magnetizing current and higher power losses. So, the choice of ℓ value is a trade off between

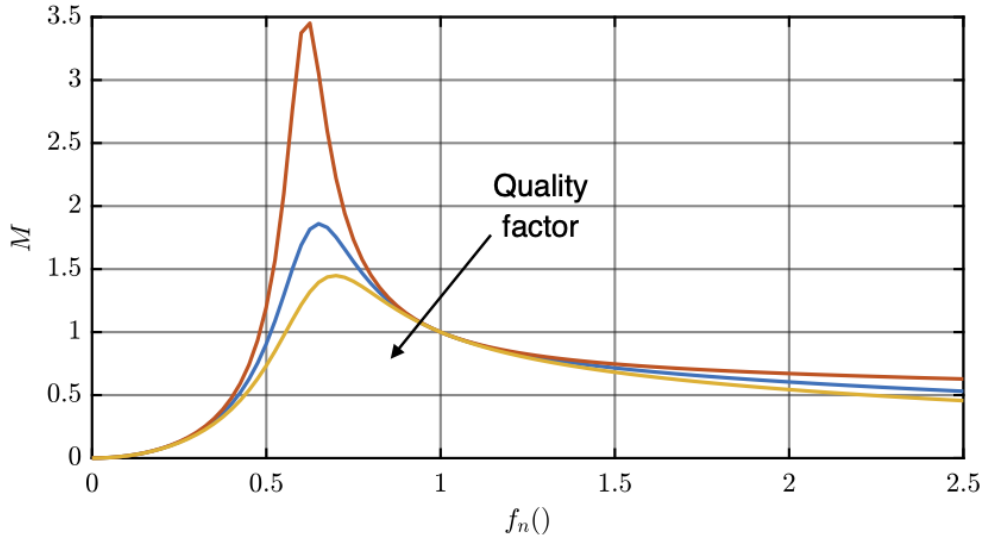


Figure 3.20: Different characteristics of voltage gain M depending on quality factor values

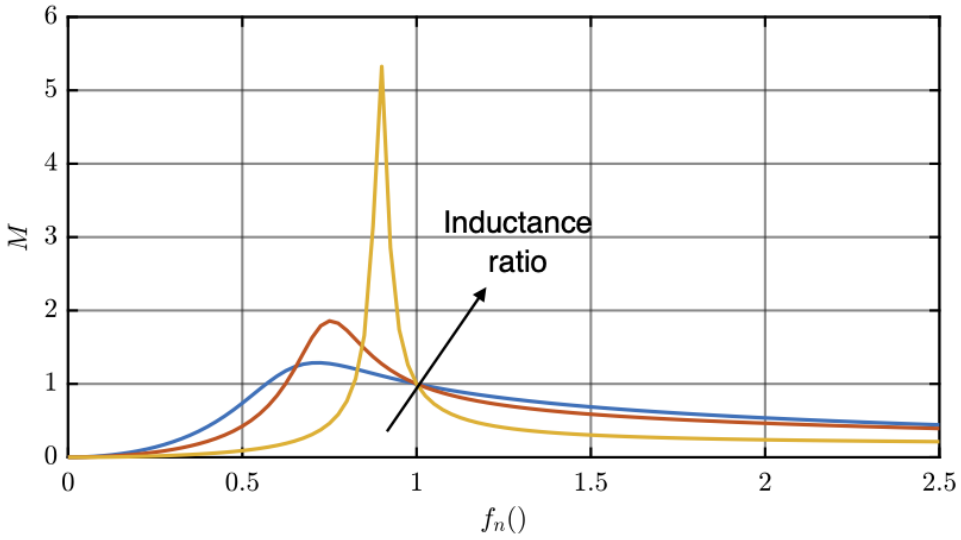


Figure 3.21: Different characteristics of voltage gain M depending on inductance ratio values

voltage range requirements and converter efficiency. Another aspect affected by the inductance ratio is the difference between the first and the second resonance frequency. With higher value of ℓ this difference is smaller and the characteristic is more sensitive to frequency variations.

Regardless the working point, which determine the value of Q, and the chosen value of ℓ it is possible to recognize two areas of the characteristic of the voltage gain, one for $M \geq 1$ and the other one for $M < 0$. This consideration means that the LLC converter can work both as step-up and step-down converter. It is worth at this point to notice that the previous voltage characteristic does take account of the voltage gain given by the transformer and its turns ratio can be designed to help the LLC converter to reach the required voltage gain.

3.2.3 Zero Voltage Switching

The LLC converter is used in applications requiring high efficiency. In fact, when the design of the LLC converter is well done the mosfets on the H-bridge converter are characterized by a Zero Voltage Switching, making the switching losses very small.

The ZVS operation [15] can be understood analyzing the waveform of current and voltage in the LLC converter during one switching period (Figure 3.22). The switching period can be divided into smaller time intervals:

- *Mode 1-2: Q_1,Q_4 ON and Q_2,Q_3 OFF.* The the input current flows through the resonant tank and becomes the primary side current of the transformer which is composed of the magnetizing current and the primary side load current. The current at the secondary side flows through D_5 and D_8 and the voltage applied to the output capacitor is applied also to the secondary side of the transformer, causing a voltage at the magnetizing inductance terminals equal to nV_{out}. As the output capacitance is assumed to be sufficiently high, the voltage applied to L_m result flat, causing a linear increasing of the magnetizing current. As the load current through the primary side is sinusoidal due to the resonant phenomena of the resonant tank, also the current through C_r and L_r has a form close to a sinusoidal wave. This mode finishes when the primary load current has reached the zero value.

- *Mode 2: Q_1,Q_4 ON and Q_2,Q_3 OFF.* The load current on the primary side has reached the zero value so only the magnetizing current is flowing through the circuit. It is important to note that for higher values of L_m, smaller values

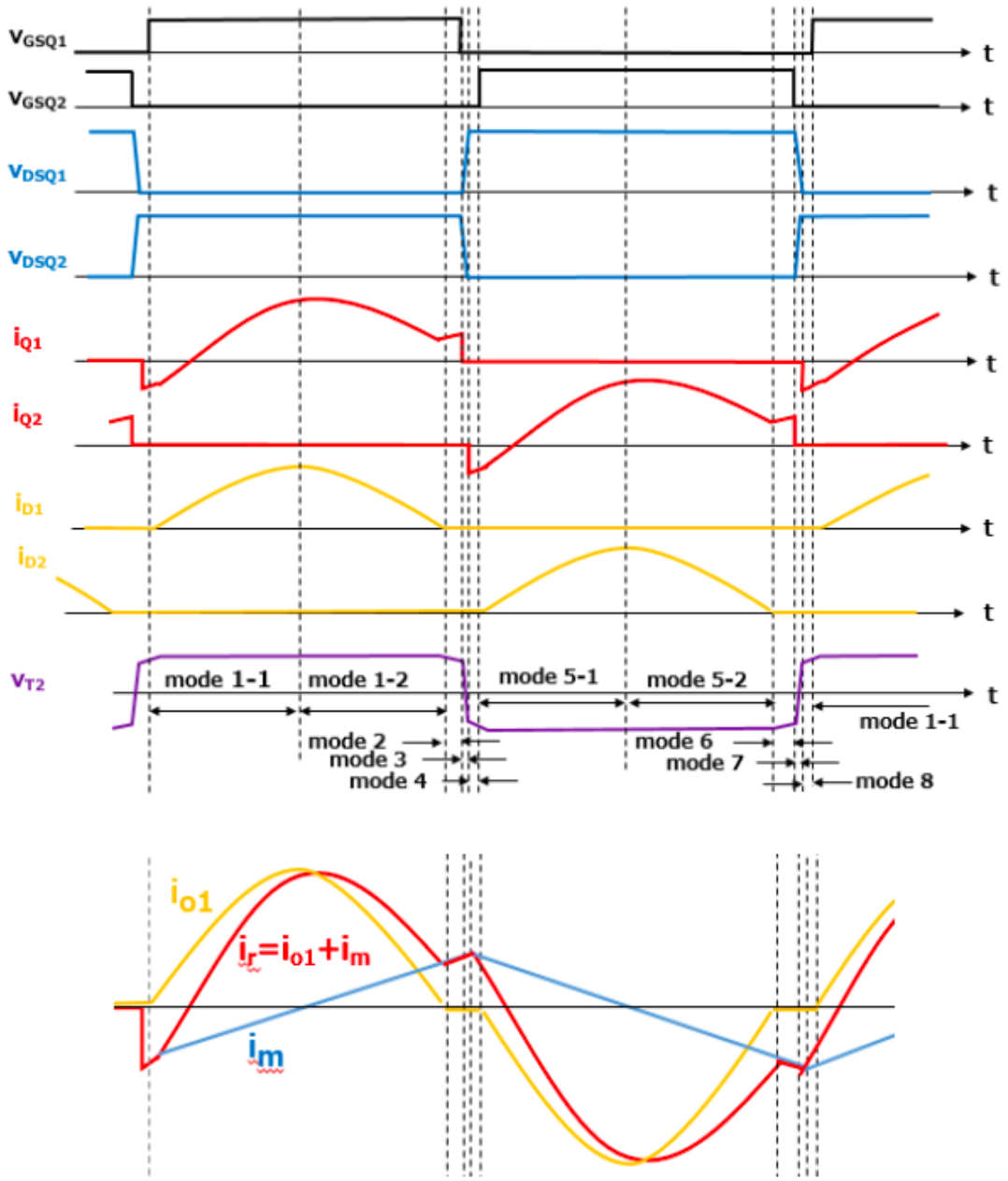


Figure 3.22: Waveforms of the electric quantities during a switching period in a LLC converter

of current flow through the circuit, improving the converter efficiency. Then, Q_1 and Q_4 turn OFF and the mode finishes when the current through them

reach the zero value

- *Mode 3: Q_1,Q_2,Q_3,Q_4 OFF.* In this interval of time the parasitic capacitance of the power switches play a key role. In fact, as Q_1 and Q_4 turn OFF the magnetizing current keep flowing through the transformer via the parasitic capacitance of the power switching, causing the voltages Q_1 and Q_4 to increase and Q_2 and Q_3 to decrease. This mode finishes when the charging and discharging of the capacitances is complete.

- *Mode 4: Q_1,Q_2,Q_3,Q_4 OFF.* When the charging operation of capacitance C_2 and C_3 is complete the diodes D_3 and D_4 result forward biased and they begin to conduct. This mode finishes when Q_2 and Q_3 turn ON.

- *Mode 5-1: Q_1,Q_4 OFF and Q_2,Q_3 ON.* At the beginning of this time interval diodes D_2 and D_3 are in a conductive state, so mosfet Q_2 and Q_3 are turned ON under ZVS condition. As Q_2 and Q_3 turn ON, C_r act as a voltage source due to the stored energy and it causes a current to flow in the opposite direction. In this way, the load current on the primary side of the transformer assume negative values causing D_6 and D_7 to conduct. As a consequence, a negative voltage is applied to L_m that decrease the value of the magnetizing current. This mode finish when the magnetizing current reach zero and revers its polarity.

- *Mode 5-2: Q_1,Q_4 OFF and Q_2,Q_3 ON.* The magnetizing current continues to increase in negative direction. This mode is the same as Mode 1-2, but with reversed polarity of the electric quantities.

After Mode 5-2, the trend of currents and voltages is the same as described in the previous Modes, the only difference is the polarity of their values. Also the behavior of the power switch is the same.

The ZVS can be identified in Mode 3 and in Mode 5-1. At the beginning of Mode 3 switches Q_1 and Q_4 turn OFF and this transition happen in a ZVS condition. In fact, before the turn OFF the voltage applied to the switch is very small and equal to the voltage drop of the conducting state. When the switches turn OFF, the value of the voltage is kept almost constant due to the parasitic capacitance. So,

if the value of parasitic capacitance is high enough, the current through the switch can reach zero while the voltage is still close to zero. When the current through the switch reach zero, the current of the resonant tank start to flow through the parasitic capacitance increasing the voltage at the terminals of the power switch. In this way, during the switching time interval, there are not contemporary values of current and voltage thus ensuring a very low switching loss.

Considering Mode 5-1 it is possible to note that when Q_2 and Q_3 turn ON, their body diodes D_2 and D_3 are already in a conducting condition so the voltage applied to their terminal was close to zero. Consequently, the current through the power switch can increase while the voltage at its terminals is close to zero.

It is important to note that the current of the resonant tank lags the voltage given by the bridge inverter. This is an essential requirement to make the ZVS happen.

3.2.4 The equivalent input impedance

As the ZVS require an inductive behavior, the next step is to analyze the equivalent input impedance and defining the border line between the capacitive and inductive behavior.

Considering the equivalent circuit of the LLC converter (Figure 3.19), the input impedance can be calculated using:

$$\bar{Z}_{in} = \frac{1}{sC_r} + sL_r + \frac{sR_{0,eq}L_m}{R_{0,eq} + L_m} \tag{3.60}$$

3.60 can be normalized with respect to the characteristic impedance Z_0:

$$\bar{Z}_n = \frac{\bar{Z}_{in}}{Z_0} \tag{3.61}$$

Using 3.51, 3.53, 3.54, 3.55 and 3.56, 3.61 can be written as follow:

$$\bar{Z}_n(f_n, Q, \ell) = \frac{Qf_n^2}{\ell^2 + Q^2 f_n^2} + j\left(\frac{f_n \ell}{\ell^2 + Q^2 f_n^2} - \frac{1 - f_n^2}{f_n}\right) \tag{3.62}$$

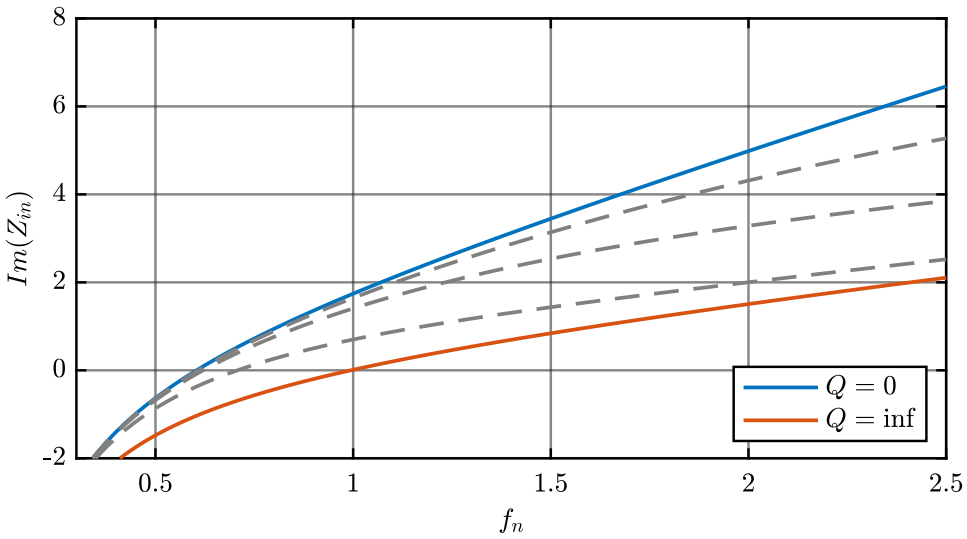


Figure 3.23: Trend lines of the imaginary part of the input impedance as function of the switching frequency

Equation 3.62 is very important because it shows the real and imaginary parts of the input impedance, which determines the behavior of the LLC converter.

If the components of the resonant tank are know, the imaginary part of 3.62 depends on Q and f_n (Figure 3.23). There are two border lines: one referred to the short circuit condition and the other one referred to the open circuit condition. Between these border lines there are all the possible values of the imaginary part of the input impedance. It is possible to see that the inductive behavior is always ensured when the switching frequency is higher than the first resonance frequency. Likewise, the LLC converter always assumes a capacitive behavior when the switching frequency is lower than the second resonance frequency.

The limit condition in which the ZVS is still ensured occurs when the imaginary part of 3.62 is equal to zero:

$$\frac{f_n \ell}{\ell^2 + Q^2 f_n^2} - \frac{1 - f_n^2}{f_n} = 0 \tag{3.63}$$

Assuming that the working point and the parameters of the LLC converter are

know, the only unknown variable in 3.63 is f_n, which can be evaluated using:

$$f_{n,lim} = \sqrt{\frac{Q^2 - \ell(1+\ell) + sqrt[\ell(\ell+1) - Q^2]^2 + 4Q^2\ell^2)]}{2Q^2}} \tag{3.64}$$

Likewise, if in 3.63 the frequency and the inductance ratio are know, it is possible to retrive the limit value of the quality factor:

$$Q_{lim} = \sqrt{\frac{\ell}{1 - f_n^2} - \left(\frac{\ell}{f_n}\right)^2} \tag{3.65}$$

which is valid for:

$$\sqrt{\frac{\ell}{\ell+1}} < f_n < 1 \tag{3.66}$$

The limit of the voltage gain is retrived by using (3.65) in (3.59):

$$M_{lim} = \frac{f_n}{\sqrt{f_n^2(1+\ell) - \ell}} \tag{3.67}$$

It should be remarked that expression (3.67) is valid for values of switching frequency between the first and the second resonance frequency. In fact, as mentioned before, for values of frequency higher than the first resonance frequency the behavior of the LLC converter is always inductive, so the ZVS is always possible.

3.2.5 Step-up and Step-down functioning

In previous subsections the voltage gain has been analyzed and it is possible to see that its trend line assumes values below and above the unitary value depending on the switching frequency. So it is interesting to understand how the LLC converter works for values of the switching frequency above, below and equal to the first resonance frequency.

For values below the resonance frequency the LLC converter works as a step-up (boost) converter (Figure 3.25). In this condition there are two freewheeling

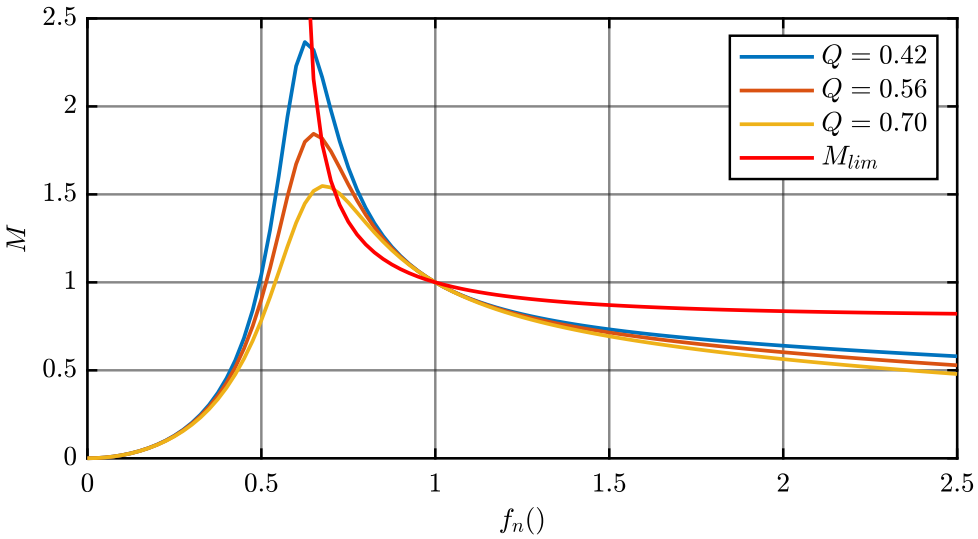


Figure 3.24: Representation of the limit value of the voltage gain

operations every switching period. In fact, as the resonance frequency is higher than the switching frequency, the current flowing through the L_r reaches the same value of the magnetizing current before that the half switching period ends. This leads to a zero current on the secondary side of the transformer and L_m starts to resonate with the other capacitor. As the second resonance frequency is lower than the first one, the current through the inductors remains almost constant. In boost condition, the diodes of the bridge rectifier works with Zero Current Switching (ZCS) as their current reaches zero before the next half switching period.

When the switching frequency is equal to the first resonance frequency the LLC converter works in the best condition (Figure 3.26). The current flowing through L_r reaches the same value of the magnetizing current exactly at the end of the half switching period and it has a perfect sinusoidal form. In this case there are no freewheeling operations, but still the diodes of the bridge rectifier work in a ZCS condition.

For values of switching frequency above the first renonant frequency the LLC converter works as a step-down (buck) converter (Figure 3.27). As the switching frequency is higher than the first resonance frequency, the current through the inductor L_r can not reach the same value of the magnetizing current before the end of the half switching period. When the polarity of the input voltage is reversed,

the current through L_r rapidly decrease to reach the magnetizing current. In this condition the diodes of the bridge rectifier are hard switched as the current does not reach zero before the end of the half switching period.

3.2.6 Control strategy for the LLC converter

Once the transfer function of the voltage gain M is understood it is possible to implement a control scheme in order to properly manage the battery charging. From the specifications of the project, the following characteristics of the battery pack are identified:

- $V_{batt,n}$: nominal battery voltage
- $V_{batt,f}$: voltage of at the battery terminals when fully recharged
- $I_{batt,n}$: nominal recharging current
- $P_{r,max}$: maximum recharging power

The charging profile (Figure 3.28) consists in two different time intervals. The first one is characterized by a constant recharging current, equal to the nominal value, and a low voltage which increase with time. The second time interval starts when the voltage reach $V_{batt,f}$ and it remains constant. The current starts to decrease with time and the battery recharge stops when the current reaches a threshold value close to zero.

The maximum power is reached when current and voltage assume their maximum values at the same time, which occur on the transition between the constant current interval and the constant voltage interval:

$$P_{r,max} = V_{batt,f} \cdot I_{batt,n} \tag{3.68}$$

As the converter is designed for a specific range of power and the battery voltage is given by its datasheet, it is possible to retrive the nominal current of the battery recharge:

$$I_{batt,n} = \frac{P_{r,max}}{V_{batt,f}} \tag{3.69}$$

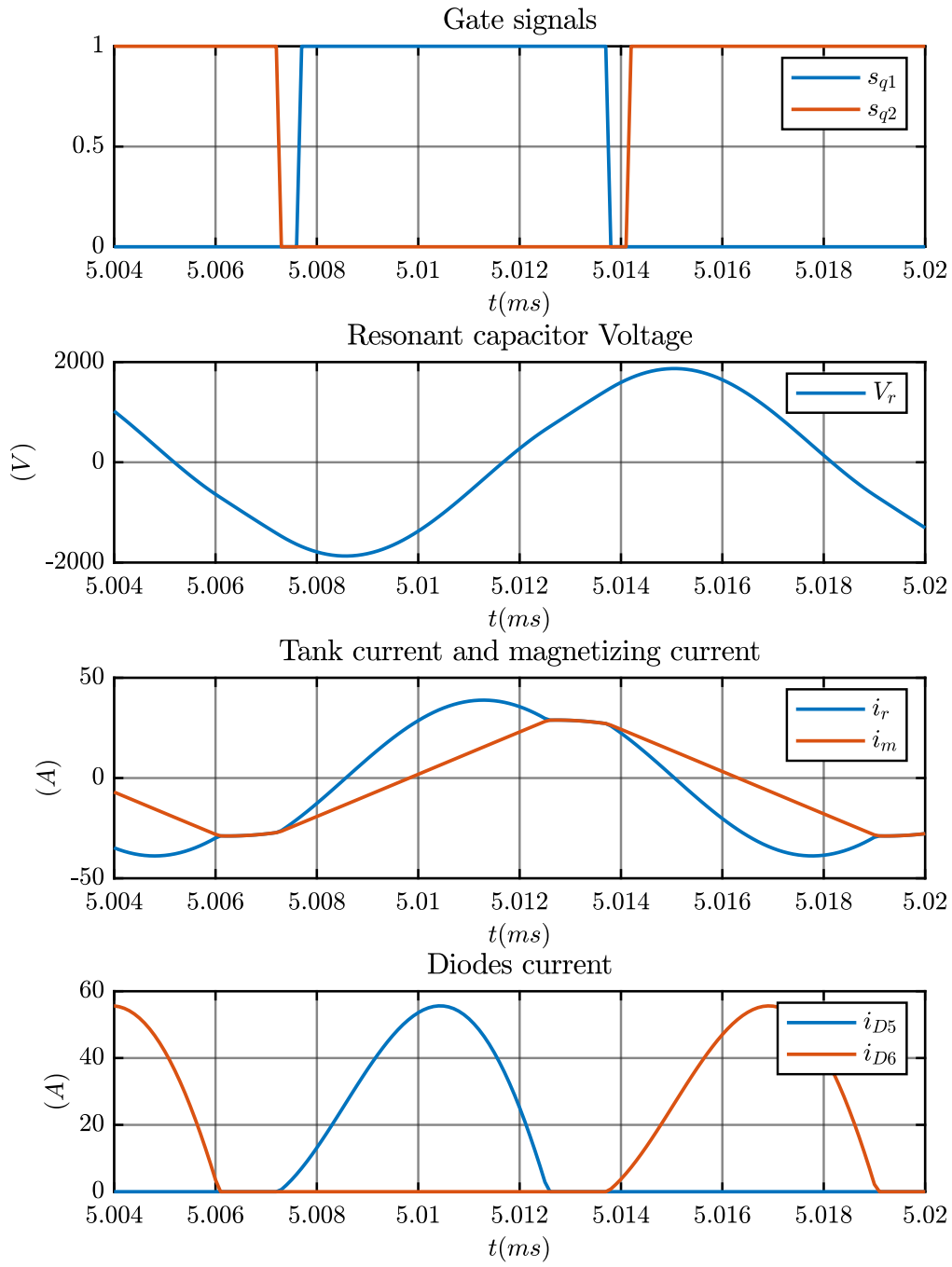


Figure 3.25: LLC waveforms in boost mode

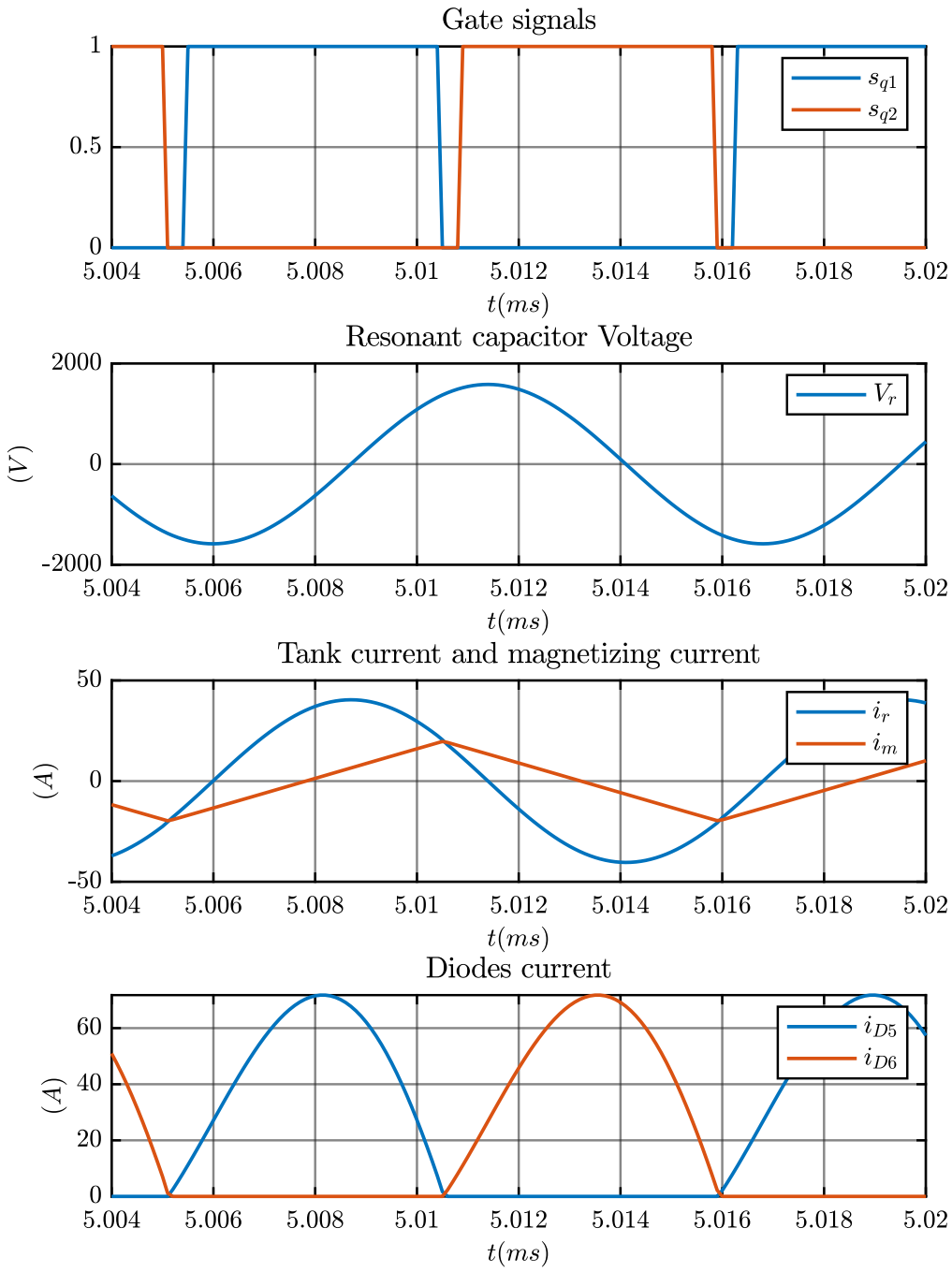


Figure 3.26: LLC waveforms in first resonant mode

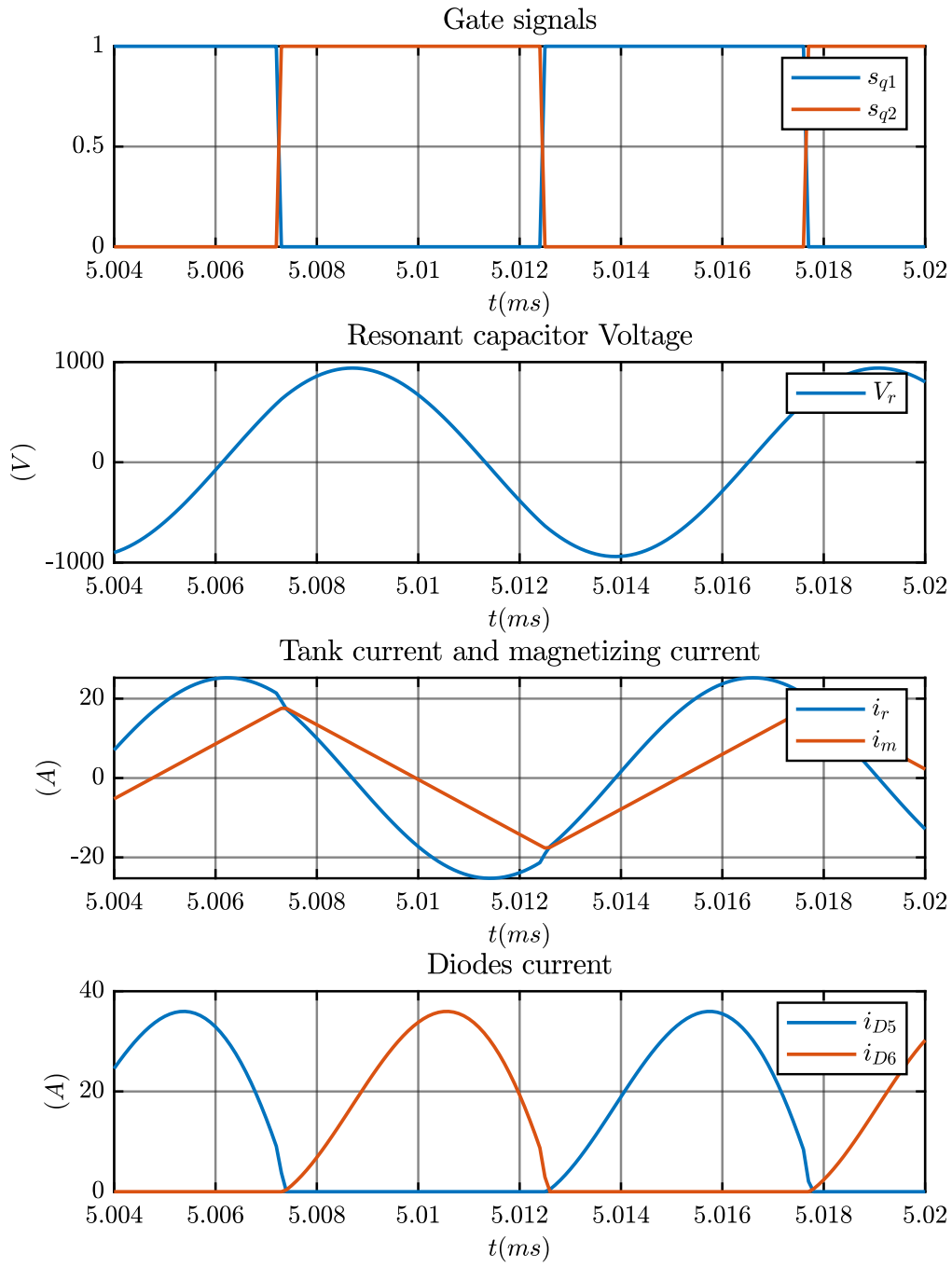


Figure 3.27: LLC waveforms in buck mode

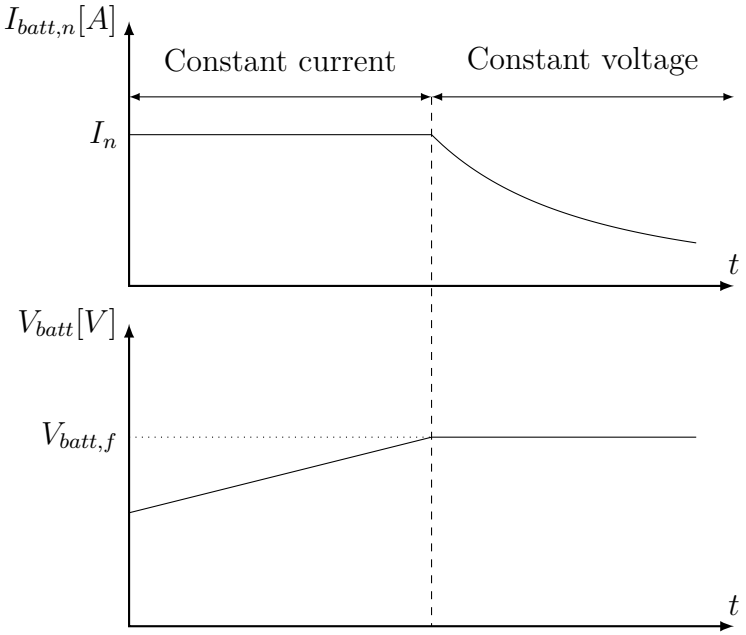


Figure 3.28: Recharge profile of the battery pack

A cascaded control is used to realize the recharging profile just described. An inner current loop is used to control the battery current while an outer voltage loop is dedicated to control the battery voltage and to determine the current reference value of the current loop (Figure 3.29).

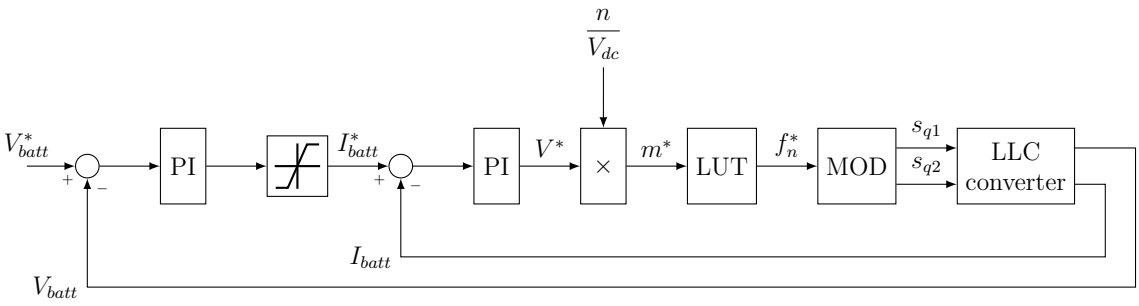


Figure 3.29: Control scheme of the LLC converter

The input of the control scheme is the desired battery voltage V^*_{batt} that is equal to the value of the battery voltage when it is fully charged. This value is compared with the actual value V_{batt} at the battery terminals and the difference is sent to

the PI regulator. The output of the PI is saturated to the nominal current value $I_{batt,n}$ and it represent the desired current I^*_{batt} through the battery. The difference between I^*_{batt} and the actual value I_{batt} is sent to another PI and its output represent the required voltage V^* at the LLC output terminals. This value is then multiplied for the turns ratio n of the transformer and divided by the measured nominal input voltage V_{dc}, which is the voltage on the DC link. At this point the required voltage gain m^* is found and it is sent to a Look-Up Table (LUT) giving at its output the required normalized switching frequency f^*_n. The last control block is the modulation block (MOD) which determines the gate signal of the bridge inverter depending on the value of f^*_n. Finally, the measured values of current I_{batt} and voltage V_{batt} are retrived from the output of the LLC converter, which is connected to the battery pack.

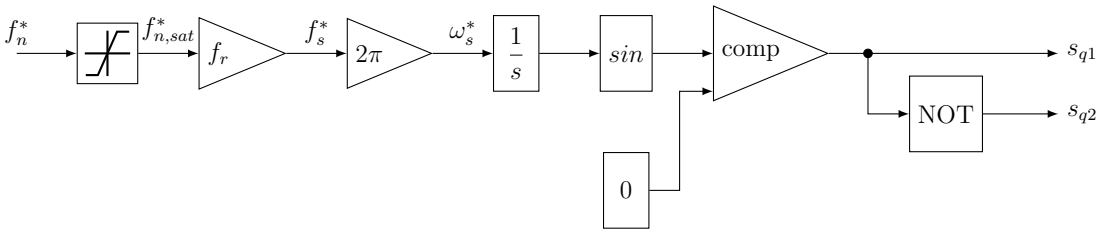


Figure 3.30: Modulation block of the LLC control scheme

The modulation block (Figure 3.30) takes as input the required switching frequency f^*_n and the first thing it does is to saturate this value between the maximum and the minimum normalized switching frequency in which the LLC converter works. The saturated switching frequency is then multiplied for $2\pi f_{r,1}$ to give the real value ω^* of the desired switching frequency. The reference frequency is integrated to obtain a fictitious position signal. The square wave gate signals s_{q1} and s_{q2} are obtained by comparing the sine of this fictitious angle with zero. As the duty cycle of the bridge inverter is always equal to 0.5, s_{q1} is ON during the first half period of the sinusoidal signal and s_{q2} is ON during the second half period. To complete the modulation block, the dead time are introduced for the turn ON of the gate signals.

As the output filter introduces an inductor in series with the battery pack, the

parameter of the current PI can be easily tuned as follow:

$$k_{p,i} = \omega_{b,i} \cdot L_{out} \tag{3.70}$$

$$k_{i,i} = \omega_{b,i} \cdot k_{p,i} \tag{3.71}$$

where:

- $\omega_{b,i}[rad/s]$ is the bandwidth of the current loop
- $L_{out}[H]$ is the output inductance given by the filter

In order to determine the parameters of the voltage PI two assumption are considered:

1. the output current ripple is very small
2. the battery is considered as a capacitor with a very high capacitance value

With this assumption it is possible to consider the transfer function between output current and output voltage as follow:

$$\frac{I_{batt}(s)}{V_{batt}(s)} = sL_{out} + \frac{K}{sC_{batt}} + R_b \approx R_b \tag{3.72}$$

where:

- $R_b[\Omega]$ is the equivalent series resistance of the battery pack
- K is a coefficient that depends on the battery characteristics
- $C_{tot}[F]$ is the equivalent capacitance of the battery pack

3.72 is justified by the fact that the ripple current is very small so the voltage drop due to L_{out} is very small and the equivalent battery capacitance C_{tot} is very high. Consequently, both of the voltage terms due to these parameters can be neglected.

The parameters of the voltage PI are then tuned as follow:

$$\omega_{b,v} = 0.1 \cdot \omega_{b_i} \tag{3.73}$$

$$k_{p,v} = 0 \tag{3.74}$$

$$k_{i,v} = \frac{\omega_{b,v}}{R_b} \tag{3.75}$$

Chapter 4

Preliminary design of the battery charger

At this point the working principles of the T-type and of the LLC converter are known so it is possible to design the battery charger in order to satisfy the specifications of the project. The first step is to design the components of the T-type converter because it establishes the grid connection and the voltage value on the DC-link. After the design of the T-type converter it is possible to design the components of the LLC converter.

The design made in this chapter is just preliminary and the results will be used for the first simulations via software. The simulations will successively help to find the final components of the two converters.

4.1 Design of the T-type converter

The first thing to do is to decide the DC-link voltage value and then it is possible to design all the T-type converter components:

- input inductors
- output capacitors
- power mosfets

- power diodes

As said in the previous chapter, the functioning of the T-type converter is similar to a boost converter so half of the DC-link voltage value V_{dc}must be higher than the peak of the input voltage V_{in}:

$$\frac{V_{dc}}{2} \geq \sqrt{2}V_{in,rms} = \sqrt{2} \cdot 220 = 311V \tag{4.1}$$

The chosen value of the DC-link voltage is $800V$.

4.1.1 Design of the output capacitors

Once the DC-link voltage value is established, it is easy to determine the nominal voltage $V_{c,n}$ of the output capacitors:

$$V_{c,n} \geq \frac{V_{dc}}{2} = 400V \tag{4.2}$$

The capacitance values are chosen with the aim to reduce the voltage ripple on the DC-link. Considering the boost functioning:

$$\frac{v_c}{v_{in}} = \frac{1}{1 - d(t)} \tag{4.3}$$

$$\frac{i_{dc}}{i_{in}} = 1 - d(t) \tag{4.4}$$

where the input voltage is given by:

$$v_{in} = \hat{V}_{in} sin(\omega t) \tag{4.5}$$

Recombining these equations it is possible to write:

$$i_{dc}(t) = \frac{\hat{V}_{in}}{V_c}\hat{I}_{in}(sin\omega t)^2 = \frac{1}{2}\frac{\hat{V}_{in}}{V_c}\hat{I}_{in}\frac{1}{2}\frac{\hat{V}_{in}}{V_c}\hat{I}_{in}cos(2\omega t) \tag{4.6}$$

4.6 shows that the current on the DC-link is composed of one mean term and one sinusoidal term which is characterized by the double of the input frequency. The sinusoidal term will introduce a voltage ripple on the output capacitor at the same frequency. Its peak value is given by:

$$\hat{V}_{dc,2nd} = \frac{1}{2\omega C_{out}} \hat{I}_{dc,2nd} = \frac{\hat{I}_{in}}{4\omega C_{out}} \frac{\hat{V}_{in}}{V_c} \tag{4.7}$$

Consequently, the capacitance value of each output capacitor can be calculated by assuming a maximum value of the voltage ripple:

$$C_{out} = \frac{\hat{I}_{in}}{4\omega \hat{V}_{dc,2nd}} \frac{\hat{V}_{in}}{V_c} \tag{4.8}$$

As a matter of fact, the LLC converter is very sensitive to voltage variations at its input terminals, so the ripple voltage at the DC-link should be very small. The chosen value of $V_{dc,2nd}$ is the equal to $8V$ which correspond to 1% of the nominal DC-link voltage. The other required values are equal to:

- $\hat{I}_{in} = \frac{P_{n,1ph}}{V_{in}}\sqrt{2} = \frac{6000}{220}\sqrt{2} = 38.7A$
- $V_c = 400V$
- $\hat{V}_{in} = \sqrt{2} \cdot 220 = 311.12V$
- $\omega = 2\pi f = 2\pi \cdot 50 = 314.16 rad/s$

Substituting these values in 4.8, it is possible to find the output capacitance value:

$$C_{out} = \frac{38.7 \cdot 311.12}{4 \cdot 314.16 \cdot 8 \cdot 400} = 3mF \tag{4.9}$$

4.1.2 Design of the input inductors

The standard requirements splits into two different approaches depending on the value of the input current: in the first case the input current is higher than $16Arms$ and the limit value of THD can not be exceed, in the second case the input current is lower than $16Arms$ and the peak of harmonics components can not exceed specific

limits. The most difficult part in satisfying the requirements is to have a THD not higher than the standard limit when its value is exactly $16Arms$.

The current THD is defined as:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{fund,rms}} \tag{4.10}$$

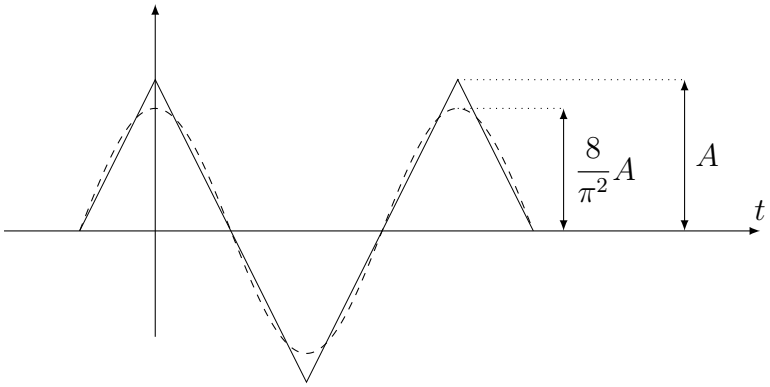


Figure 4.1: Triangular wave and its first harmonic component

A first try value for the input inductor is calculated considering the input current as a sine wave with a triangular ripple due to the switching process. The fourier series of a triangular wave is given by:

$$tr(t) = \sum_{n=1}^{\infty} a_n cos(n\omega_0 t) \tag{4.11}$$

where:

$$a_n = \begin{cases} 4A\dfrac{1-(-1)^n}{\pi^2 n^2}, & \text{n odd} \\ 0, & \text{n even} \end{cases} \tag{4.12}$$

The coefficient A is the magnitude of the triangular wave (Figure 4.1). The current

ripple assume a symmetric shape when the duty cycle is equal to 0.5 and the peak-to-peak value reach its maximum value which can be calculated using [14]:

$$\Delta_{i,pp} = \frac{V_{out}}{4 f_{sw} L_{in,eq}} \tag{4.13}$$

where:

- $L_{in,eq}[H]$ is the equivalent input inductance
- $f_{sw}[Hz]$ is the switching frequency
- $V_{out}[V]$ is the output voltage of the single converter structure and in this application corresponds to $\frac{V_{dc}}{2}$

As A is equal to half of the peak-to-peak value of the ripple current, it is possible to write:

$$A = \frac{\Delta_{i,pp}}{2} = \frac{V_{out}}{8 f_{sw} L_{in}} \tag{4.14}$$

Considering just the first harmonic component of the triangular wave it is possible to substitute 4.12 into 4.10:

$$THD = \frac{8A}{\sqrt{2}\pi^2 I_{fund,rms}} \tag{4.15}$$

Finally, substituting 4.14 into 4.15 it is possible to retrive the first try value of $L_{in,eq}$:

$$L_{in} = \frac{V_{out}}{\sqrt{2}\pi^2 I_{fund,rms} f_{sw} THD} \tag{4.16}$$

Considering the following values:

- $V_{out} = 400V$
- $I_{fund,rms} = 16Arms$

- $f_{sw} = 20kHz$
- $THD = 0.23$

4.16 will give:

$$L_{in,eq} = 390\mu H \tag{4.17}$$

The single-phase configuration of the T-type converter works with the three phases connected in parallel, so the inductance for each phase must be equal to:

$$L_{in} = 1.17mH \tag{4.18}$$

Obviously, this is a precautionary value as the interleaved control has not been taken into account to reach this result and the expectations is to reduce this value for the final design. This is just a starting point value and the simulations via software will help to improve the design.

Regarding the choice of the nominal current, it is possible to verify that in the three phase configuration the current that flow through the input inductors is higher than in the single-phase configuration:

$$I_{L,3ph} = \frac{P_{n,3ph}}{3V_{in}} = \frac{11000}{3 \cdot 220} = 16.7A \tag{4.19}$$

$$I_{L,1ph} = \frac{I_{in}}{3} = \frac{P_{n,1ph}}{3V_{in}} = 9.1A \tag{4.20}$$

So the nominal current of the inductors must be higher than $16.7A$.

4.1.3 Choice of the semiconductor devices

The last step of the preliminary design of the T-type converter is to choose the semiconductor devices. As mentioned before, the three-phase configuration is the one with higher current on each phase so it determines the reference value for the nominal current of diodes and mosfets. The diodes must withstand a reverse voltage equal to the entire DC-link voltage value. Conversely, the mosfet on the middle

legs must withstand just half of the DC-link voltage because they are connected in series. These considerations permit the choice of the diodes and mosfets.

	Diodes	Mosfet
$I_n[A]$	≥ 16.7	≥ 16.7
$V_r[V]$	≥ 800	≥ 400

Table 4.1: Values of nominal current and reverse voltage for the choice of diodes and mosfet in the T-type converter

4.2 Design of the LLC converter

The most important part of the LLC converter design is to determine parameters of the resonant tank and of the transformer, because they affect the voltage gain between input and output. Once they are determined it is possible to continue with the design of the resonant inductor and of the transformer. Finally, some considerations are made about the output filter.

4.2.1 Design of the resonant tank

The design of the resonant tank has been already treated in previous works ([16]) and can be divided into the following steps:

1. Define all the specifications of the LLC conveter:

Minimum battery voltage	$V_{batt,min}$	350	$[V]$
Maximum battery voltage	$V_{batt,max}$	420	$[V]$
Minimum DC-link voltage	$V_{dc,min}$	792	$[V]$
Maximum DC-link voltage	$V_{dc,max}$	808	$[V]$
Maximum recharging power	P_{max}	$11 \cdot 10^3$	$[W]$
First resonant freqeuncy	$f_{r,1}$	$100 \cdot 10^3$	$[Hz]$
Maximum switching frequency	f_{max}	$130 \cdot 10^3$	$[Hz]$
Maximum dead time	$t_{d,max}$	$50 \cdot 10^{-9}$	$[s]$
Output mosfet capacitance	C_{oss}	$56 \cdot 10^{-12}$	$[F]$
Efficiency	η	0.95	[]

Table 4.2: Specifications for the resonant tank design

2. Find the transformer turn ratio:

$$n = \frac{V_{dc,min}}{V_{batt,min}} \tag{4.21}$$

Using 4.21, the minimum voltage gain is required when the input voltage is at its maximum value and the desired battery voltage is at its minimum, while the maximum voltage gain is required when the battery voltage is at its maximum and the input voltage is at its minimum.

3. Define the maximum and the minimum voltage gains:

$$M_{max} = \frac{nV_{batt,max}}{V_{dc,min}} \tag{4.22}$$

$$M_{min} = \frac{nV_{batt,min}}{V_{dc,max}} \tag{4.23}$$

4. Define the inductance ratio ℓ:

$$\ell = \left(\frac{1}{M_{min}} - 1\right)\frac{8f_{max}^2}{8f_{max}^2 - \pi^2} \tag{4.24}$$

In order to be able to control the current down to zero it is necessary to verify:

$$M(1+\ell) \geq 1 \tag{4.25}$$

5. Determine the limit conditions for the ZVS in boost mode:

$$M_{crit} = \sqrt{1 + \sqrt{\frac{\ell}{\ell+1}}} \tag{4.26}$$

$$Z_{0,crit} = \frac{8V_{dc,min}^2}{\pi^2 P_{out,max}}\left(\sqrt{\ell(1+\ell)} + \ell\right) \tag{4.27}$$

The LLC converter works in the limit condition for the ZVS when the characteristic impedance is equal to $Z_{0,crit}$ and the battery voltage determine a voltage gain equal to M_{crit}. In this conditions the input and output currents are equal to:

$$I_{batt,crit} = \frac{nP_{out,max}}{M_{crit}V_{dc,min}} \tag{4.28}$$

$$I_{dc,crit} = \frac{P_{out,max}}{\eta V_{dc,min}} \tag{4.29}$$

6. The expressions in the previous step are related to the inductance ratio so it is possible to determine the magnetizing inductance:

$$L_m = \frac{n^2}{f_{r,1}}\frac{M_{crit}\frac{V_{dc,min}}{n}}{4nI_{dc,crit} + (\pi^2\ell M_{crit} - 4)I_{batt,crit}} \tag{4.30}$$

7. Verify if the value of the magnetizing inductance is not too high:

$$L_m \leq \frac{t_{d,max}}{8\pi f_{r,1} C_{oss}} \sqrt{\left(1 + \frac{1}{\ell}\right) M_{min}^2 - dfrac1\ell(1+\ell)} \tag{4.31}$$

   This check is done considering the maximum switching frequency and power equal to zero delivered to the battery. In this condition the current that flow through the resonant tank is equal to the smallest possible value. If L_m is too high, the current is not high enough to charge and discharge the parasitic capacitance of the mosfets, so the ZVS is not ensured.

8. Once the inductance ratio and the magnetizing inductance are determined, it is possible to retrive the other parameters of the resonant tank:

$$L_r = \ell L_m \tag{4.32}$$

$$C_r = \frac{1}{4\pi^2 f_r^2 L_r} \tag{4.33}$$

$$f_{r,2} = \frac{1}{2\pi\sqrt{(L_m + L_r)C_r}} \tag{4.34}$$

$$Z_0 = \frac{L_r}{C_r} \tag{4.35}$$

   The value of the characteristic impedance Z_0 must not exceed its critical value $Z_{0,crit}$:

$$Z_0 \leq Z_{0,crit} \tag{4.36}$$

9. The minimum switching frequency is the lower value in which the ZVS must be ensured. Once the maximum value of voltage gain is determined, it is possible to substitute it into 3.67 and to retrive the value of minimum switching

frequency:

$$f_{n,min} = \frac{1}{\sqrt{1 + \frac{1}{\ell}\left(1 - \frac{1}{M_{max}^2}\right)}} \tag{4.37}$$

10. Finally, it is necessary to check if the maximum value that the quality factor can assume during the converter functioning does not exceed the limit value for the ZVS Q_{lim}:

$$Q_{max} \leq Q_{lim} \tag{4.38}$$

The limit value can be retrived by substituting 4.37 into 3.65:

$$Q_{lim} = \frac{\ell}{M_{max}\sqrt{\frac{1}{\ell} + \frac{M_{max}^2}{M_{max}^2 - 1}}} \tag{4.39}$$

The maximum value that the quality factor can assume during the converter functioning is given by:

$$Q_{max} = \frac{\pi^2 n^2}{8} \frac{I_{batt,max}}{V_{in,min}} Z_0 \tag{4.40}$$

If the conditions given in steps 4, 7, 8, and 10 are not satisfied it is necessary to modify the value of the inductance ratio ℓ.

The results of this procedure havee been calculated by using a MATLAB Script and they are reported in Table 4.3.

4.2.2 Design of the resonant inductor

The procedure followed for the design of the resonant inductor is described in [5].

The selected shape of the core is the PQ shape as this topology is designed specially for switching mode power supply and they optimize the ratio of core

turns ratio	n	2	[ ]
maximum voltage gain	M_{max}	1.0606	[ ]
minimum voltage gain	M_{min}	0.8663	[ ]
inductance ratio	ℓ	0.5714	[ ]
magnetizing inductance	L_m	108	$[\mu H]$
resonant inductance	L_r	62	$[\mu H]$
resonant capacitance	C_r	41	[nF]
characteristic impedance	Z_0	38.74	$[\Omega]$
minimum switchin frequency	f_{min}	95.346	$[kHz]$

Table 4.3: Results of the LLC converter design

volume to winding and surface area. The material of the core is Ferrite T, which is suited for Automotive applications.

The design procedure is divided into the following steps:

1. Compute the LI^2 product:

$$LI^2 = L\left(\frac{1.5 \cdot P_{max}}{V_{dc}}\right)^2 = 62 \cdot 10^{-6}\left(\frac{1.5 \cdot 11000}{800})^2 = 20mJ \tag{4.41}$$

   Note that a precautionary margin for the value of current has been taken into account.

2. Select the core model using the Ferrite Core Selector chart (Figure 4.2) and read the nominal inductance A_L. The core model chosen for the resonant inductor is *PQ44040* ([4], Figure 4.3) and its nominal inductance is equal to $A_L = 150mH/1000turns$

3. Calculate the number of turns:

$$N = 10^3\sqrt{\frac{L}{A_L}} = 10^3\sqrt{\frac{62 \cdot 10^{-6}}{150 \cdot 10^{-3}}} = 20 \tag{4.42}$$

Once the core model is selected it is possible to design the winding of the inductor. Litz wire is used for this purpose because their are designed for high frequency

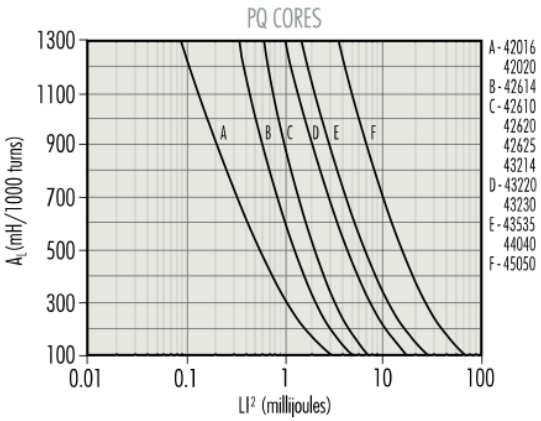
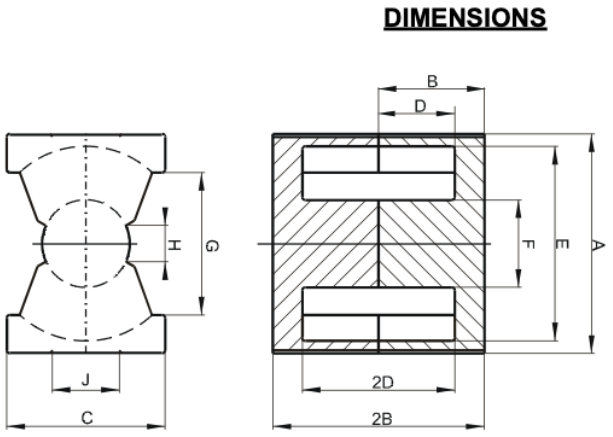


Figure 4.2: MAGNETICS Ferrite Core Selector chart for PQ shape



(mm)	Nominal:	Tol. min.:	Tol. max.:
A	41.5	-0.9	+ 0.9
B	19.9	-0.15	+ 0.15
2B	39.8	-0.30	+ 0.30
C	28.0	-0.6	+ 0.6
D	14.75	-0.20	+ 0.20
2D	29.5	-0.4	+ 0.4
E	37.0	-0.6	+ 0.6
F	14.9	-0.30	+ 0.30
G	28.0 Min.		
H	6.05 Min.		
J	15.0 Min.		
Eff. Parameters			
Ae mm ²	Amin mm ²	le mm	Ve mm ³
201	175	102	20500

Figure 4.3: MAGNETICS Core PQ44040

applications and they are able to minimize the skin effect.

Assuming a fill factor f_{Cu} equal to 0.4 it is possible to calculate the copper section of the inductor winding:

$$A_{Cu} = (E - F) \cdot 2D \cdot f_{Cu} = (37 - 14.9) \cdot 29.5 \cdot 0.4 = 260mm^2 \tag{4.43}$$

The section of the single wire is retrived dividing the last expression by the number

of turns:

$$S_{Cu} = \frac{A_{Cu}}{N} = 13mm^2 \tag{4.44}$$

The chosen value of the wire section is $10mm^2$ that is a bit smaller than the value in 4.44. This solution is better in term of weight and it permits to have a good value of current density anyway.

4.2.3 Transformer design

The procedure used to design the transformer refers to the document "Ferrite and accessories: application notes, TDK" [11].

First of all, the core model must be chosen depending on the power capacity. A suitable solution for a nominal power equal to $11kW$ is *E 100/60/28* ([12], Figure 4.4) and the selected core material is N97 [13], which is characterized by low core losses.

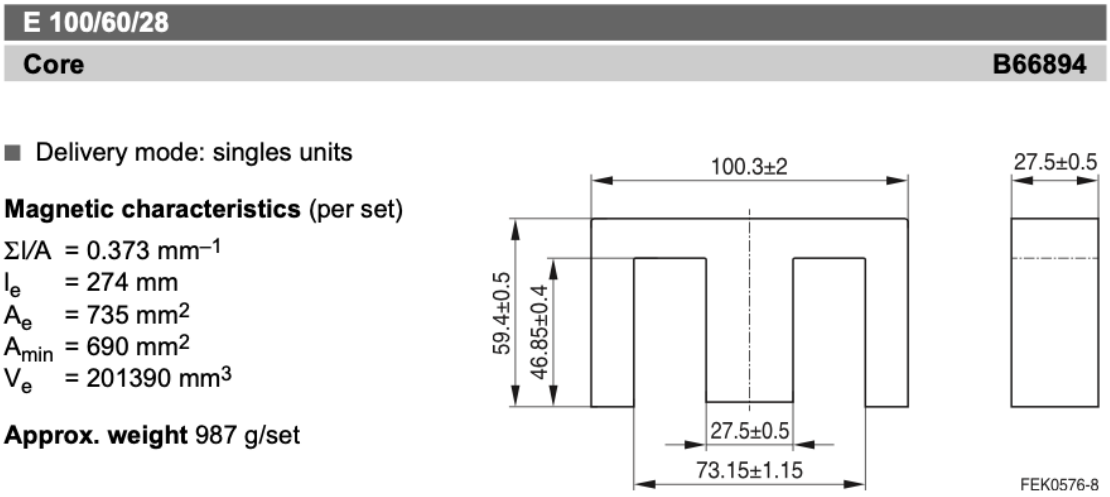


Figure 4.4: TDK Core E 100/60/28

The following relation is used for the calculation of the number of turns on the primary side :

$$V_1 = 4.44 \cdot f \cdot N_1 \cdot B \cdot S_{Fe} \tag{4.45}$$

where:

- $V_1[V]$ is the voltage at the primary side of the transformer
- $f[Hz]$ is the working frequency
- N_1 is the number of turns at the primary side
- $B[T]$ is the magnetic flux density
- $S_{Fe}[m^2]$ is the section of the magnetic path

The following assumptions are considered:

- $V_1 = V_{dc} \cdot M_{max} = 800 \cdot 1.06 = 848V$
- $f = f_{min} = 95346Hz$
- $B = 0.2T$

Moreover, reading the data sheet of the core, the section of the magnetic path is known and it is equal to $S_{Fe} = 690mm^2$. So the number of turns is equal to:

$$N_1 = \frac{V_1}{4.44 f_{min} B S_{Fe}} = 19.35 \Rightarrow 20turns \tag{4.46}$$

As the turn ratio of the transformer is equal to 2, the number of turns at the secondary side of the transformer is given by:

$$N_2 = \frac{N_1}{n} = \frac{20}{2} = 10turns \tag{4.47}$$

Also for the winding of the transformer, the litz wire is used and the procedure to calculate the sections is similar to the one used for the resonant inductor. From the data sheet of the transformer core, the geometry is know, so it is possible to retrive the total copper section considering a fill factor equal to 0.4:

$$A_{Cu} = \frac{(73.15 - 27.5)}{2} \cdot 2 \cdot 46.85 \cdot 0.4 = 824.4mm^2 \tag{4.48}$$

Assuming that at the secondary side the section of the wires are double with respect to the section at the primary side, the section of the wire at the primary side is given by:

$$S_1 = \frac{A_{Cu}}{N_1 + 2N_2} = \frac{824.4}{40} = 20.61mm^2 \tag{4.49}$$

Consequently, the section at the secondary side is equal to:

$$S_2 = 2S_1 = 41.22mm^2 \tag{4.50}$$

At this point its been decided to use litz wires with nominal section equal to $10mm^2$, so for the primary winding two wires are connected in parallel, while for the secondary side there are four wirese connected in parallel.

4.2.4 Output filter

In order to improve the current waveform at the battery side, an inductor is connected to the output of the LLC converter, forming a CL filter with the output capacitor. The resonance frequency of the output filter is set to $f_{filt} = 10kHz$ which is much less than the minimum switching frequency. A reasonable value of the output inductance in terms of ripple attenuation and size of the inductor is $L_{out} = 10\mu H$. Consequently, the output capacitance is given by:

$$C_{out} = \frac{1}{4\pi^2 f_{filt}^2 L_{out}} = 25\mu F \tag{4.51}$$

Chapter 5

Software simulation

In this chapter the results of the converters design are tested with PLECS simulations. The aim is to check if the parameters found in the last chapters are a good solution for the battery charger and, if not, to choose better values for the application. Moreover, the dynamic of the controlled quantities can be analyzed in order to verify if the parameters of the PI regulators are well tuned.

At first, the two converters are simulated individually to check their functioning and their parameters. During this operation the parameters of the converters have been modified, if required, in order to obtain an optimized design. Before to simulate the complete cascaded converter, the commercial solutions for the converters components are chosen. So the final simulation gives the result of the complete converter behavior with the final chosen parameters and components.

The last section of the chapter is dedicate to the ZVS of the LLC converter. As PLECS does not simulate the switching process, LTSpice will be used for this purpose.

5.1 Simulation of the T-type converter

For the simulation of the T-type converter, the LLC converter is modeled as a current source, which absorb the output power of the T-type converter. The reference value of the DC-link voltage is kept equal to $800V$.

During the simulations, also a grid inductance equal to $100\mu H$ has been taken

into account.

5.1.1 Three-phase configuration

The first simulation of the single-phase T-type converter has been run with the parameters reported in Table 5.1. The parameters of the control and of the PLL

Converter Parameters		
Input Voltage	220	[Vrms]
Switching frequency	20	[kHz]
Input inductance	1.2	[mH]
Output capacitance	3.0	[mF]
Initial capacitor voltage	390	[V]

Table 5.1: Parameters of the T-type converter for the fisrt simulation

are tuned as explained in chapter 3. In order to check the value of the input inductors, the value of the output current source has been set in such a way that the input current of the T-type converter is equal to $16Arms$:

$$I_{out} = \frac{3V_{in}I_{in}}{V_{dc}} = \frac{3 \cdot 220 \cdot 16}{800} = 13.2A \tag{5.1}$$

From this first simulation (Figure 5.1) it is possible to see the following results:

- the currents through in dq coordinates follow their reference values
- the voltage on the DC-link follow its reference value
- the input current has a sinusoidal waveform and it is in phase with the input voltage

Moreover, it is possible to measure the THD of the input current using the cursors inside the PLECS scope. In this case the THD is close to 5% so the value of the input inductance can be decreased. After some tries, the chosen inductance value is $L_{in} = 200\mu H$. Changing the value of the inductance, the new THD value of the input current is equal to 24%. One solution could be to increase the inductance value,

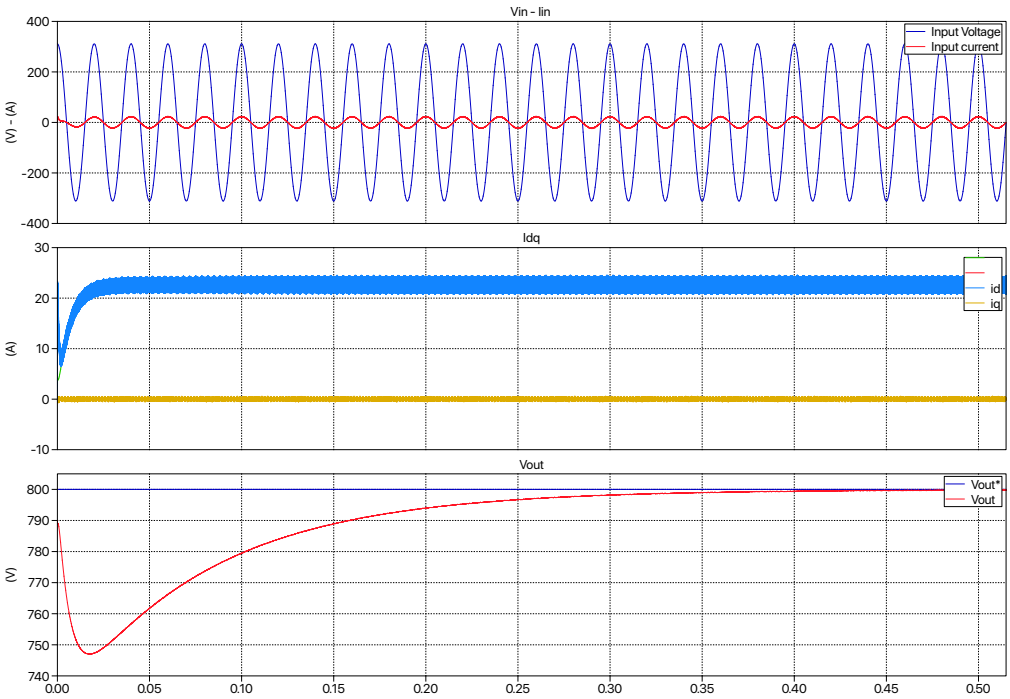


Figure 5.1: Results of the first simulation of the T-type converter

however this will negatively affect the weight and the volume of the converter. An alternative way to overcome the problem is to limit the input current to $16Arms$ so the standard requirements to be satisfied regard just the magnitude of the harmonic components. Limiting the input current does not affect the transferred power so much. The nominal current of the T-type converter should be:

$$I_n = \frac{P_n}{3V_{in}} = \frac{11000}{3 \cdot 220} = 16.67A \tag{5.2}$$

So, limiting the input current to $16A$ does not affect much on the recharging profile and it permits to save weight and volume of the converter.

During the simulation, also the current through the capacitors has been measured:

$$I_{c,rms} = 10.7A \tag{5.3}$$

One simulation has been run at the 10% of the rated power in order to check if the harmonics magnitude of the input currents satisfy the standard requirements. The results (Table 5.2) of the simulation say that the standards are satisfied.

n	f	magnitude	n	f	magnitude
1	50	2.64	21	1050	0.01
2	100	0.19	22	1100	0.01
3	150	0.07	23	1150	0.01
4	200	0.04	24	1200	0.01
5	250	0.33	25	1250	0.01
6	300	0.03	26	1300	0.01
7	350	0.26	27	1350	0.01
8	400	0.02	28	1400	0.01
9	450	0.02	29	1450	0.03
10	500	0.02	30	1500	0.01
11	550	0.10	31	1550	0.02
12	600	0.02	32	1600	0.01
13	650	0.06	33	1650	0.00
14	700	0.02	34	1700	0.01
15	750	0.01	35	1750	0.00
16	800	0.01	36	1800	0.00
17	850	0.02	37	1850	0.01
18	900	0.01	38	1900	0.00
19	950	0.02	39	1950	0.00
20	1000	0.01	40	2000	0.00

Table 5.2: Three-phase T-type converter: Harmonics magnitudes of the input current during a functioning at 10% of the rated power

5.1.2 Single-phase configuration

As the interleaved control reduces the ripple on the inductor currents, the value of inductance found for the three-phase configuration is good also for the single-phase configuration. A simulation at rated power has been run to verify all the components value (Table 5.3) and the tuning of the control parameters, which are

set as described in chapter 3. The results of the simulation (Figure 5.2) lead to the following observations:

Converter Parameters		
Input Voltage	220	[Vrms]
Switching frequency	20	[kHz]
Input inductance	200	$[\mu H]$
Output capacitance	3.0	[mF]
Initial capacitor voltage	390	[V]

Table 5.3: Parameters of the single-phase T-type simulation

- the current through the inductor follow their reference value
- the input current has a sinusoidal waveform and it is in phase with the input voltage
- the output voltage follow its reference voltage
- the output voltage is affected by a 100Hz ripple, which peak value is equal to 8V

During the simulations, also the current through the capacitors has been measured. The rms value is a bit higher than in the three-phase configuration and it is equal to:

$$I_{c,rms} = 13.6A \tag{5.4}$$

In order to check if the standard requirements are satisfied also for low values of input current, a simulation has been run at the 10% of the rated power. From the results (Table 5.4) it is possible to see that the standard requirements are satisfied.

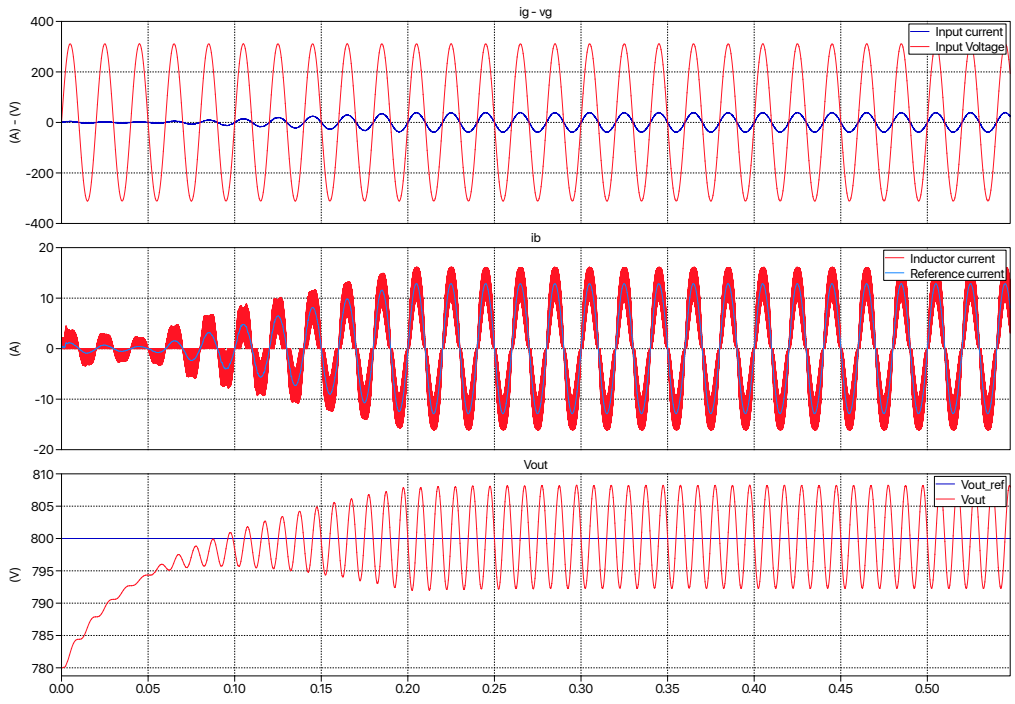


Figure 5.2: Results of the single-phase T-type simulation

5.2 Simulation of the LLC converter

The input of the LLC converter in the simulation is modeled as a constant voltage source, which value is equal to $800V$. In order to consider its dynamic behavior, the battery is modeled as a capacitor with a very high capacitance value. The parameters used for the simulations of the LLC converter are reported in Table 5.5. The regulators are tuned as reported in chapter 3.

As the recharging time is very long, two simulation has been run. The first one starts with an initial battery voltage equal to $350V$ which is the assumed value of the battery voltage when its state of charge is very low. From the first results (Figure 5.3) it is possible to note the following facts:

- at the beginning of the simulation the control does not respond because the LUT needs some moments to find the first frequency value that allow to control the current

n	f	magnitude	n	f	magnitude
1	50	3.86	21	1050	0.01
2	100	0.00	22	1100	0.00
3	150	0.10	23	1150	0.01
4	200	0.00	24	1200	0.00
5	250	0.04	25	1250	0.00
6	300	0.00	26	1300	0.00
7	350	0.07	27	1350	0.01
8	400	0.00	28	1400	0.00
9	450	0.05	29	1450	0.00
10	500	0.00	30	1500	0.00
11	550	0.03	31	1550	0.00
12	600	0.00	32	1600	0.00
13	650	0.02	33	1650	0.00
14	700	0.00	34	1700	0.00
15	750	0.04	35	1750	0.00
16	800	0.00	36	1800	0.00
17	850	0.02	37	1850	0.00
18	900	0.00	38	1900	0.00
19	950	0.01	39	1950	0.00
20	1000	0.00	40	2000	0.00

Table 5.4: Single-phase T-type converter: Harmonics magnitudes of the input current during a functioning at 10% of the rated power

- after the first moments of the simulation, the current follows the reference with a good response
- the reference value of current is saturated to the nominal value
- the voltage at the battery terminals is almost flat because of the the big capacitance value, and it increases very slowly

In order to see the transition from the constant current interval to the constant voltage interval of the charging profile, a second simulation has been run. This time, the initial battery voltage has been set to 415 which is very close to $420V$

Converter Parameters		
Input Voltage	800V	[Vrms]
Resonant inductance	62	$[\mu H]$
Resonant capacitance	40	$[nF]$
Magnetizing inductance	108	$[\mu H]$
Transformer turns ratio	2	[ ]
Filter capacitance	25	$[\mu F]$
Filter inductance	10	$[\mu H]$

Table 5.5: Parameters of the LLC converter used for the simulation

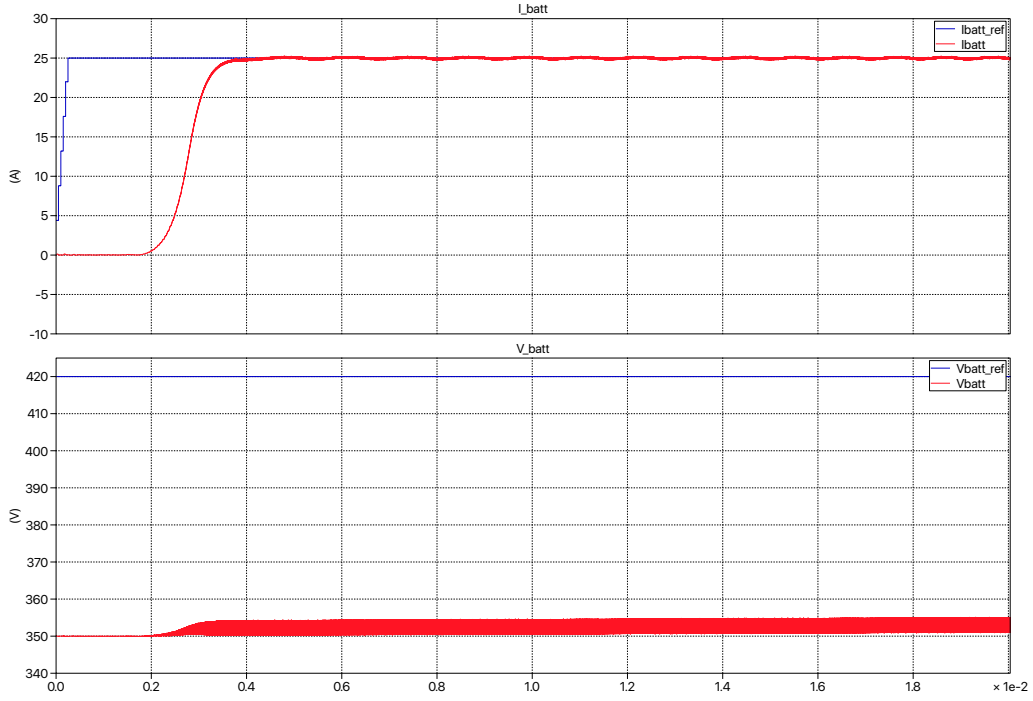


Figure 5.3: Results of the LLC converter simulation with a initial battery voltage equal to 350V

that corresponds to the value of the battery when it is completely recharged. From the results of this second simulation (Figure 5.4), it is possible to note that:

- during the first moments the battery current is equal to the nominal value and

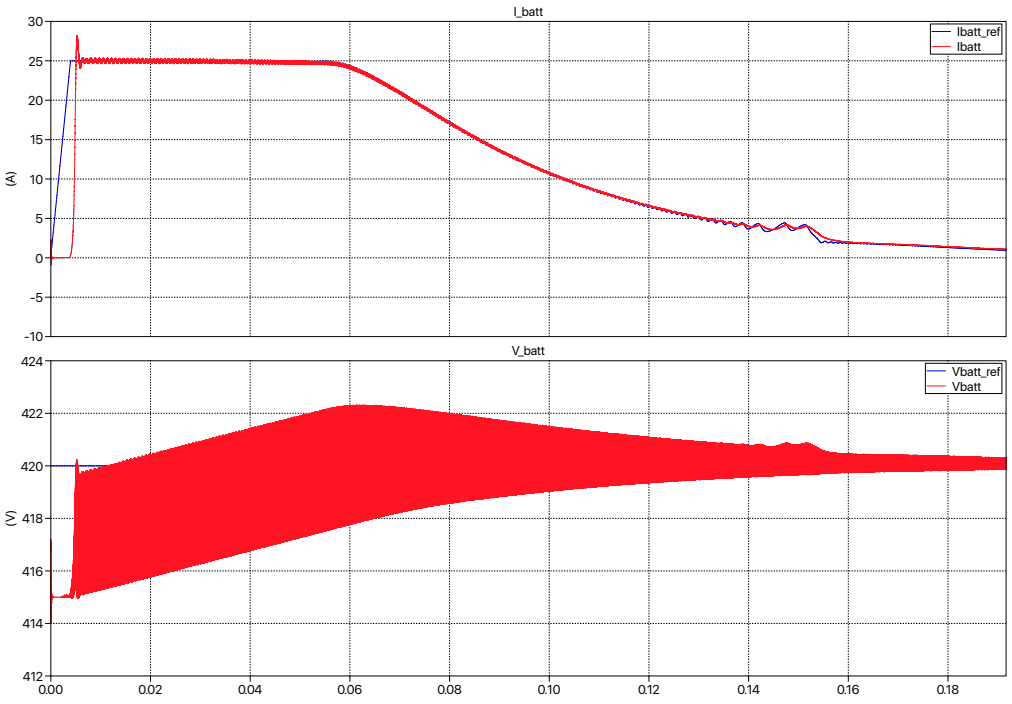


Figure 5.4: Results of the LLC converter simulation with a initial battery voltage equal to 415V

the battery voltage is increasing to reach the desired value

- when the battery voltage reaches the desired value, the current start to decrease and the voltage remain constant: this is the transition between the two intervals of the charging profile

- while the voltage remains constant, the current decreases with time reaching values that are close to zero

- the output voltage is affected by a high frequency ripple, but its magnitude is close to 1% of the nominal value so it is acceptable

Combining the results of the two simulation it is possible to note that the recharging profile correspond to the desired one (Figure 3.28), so the chosen parameters for the converter components and for the PI regulators are suitable for the application.

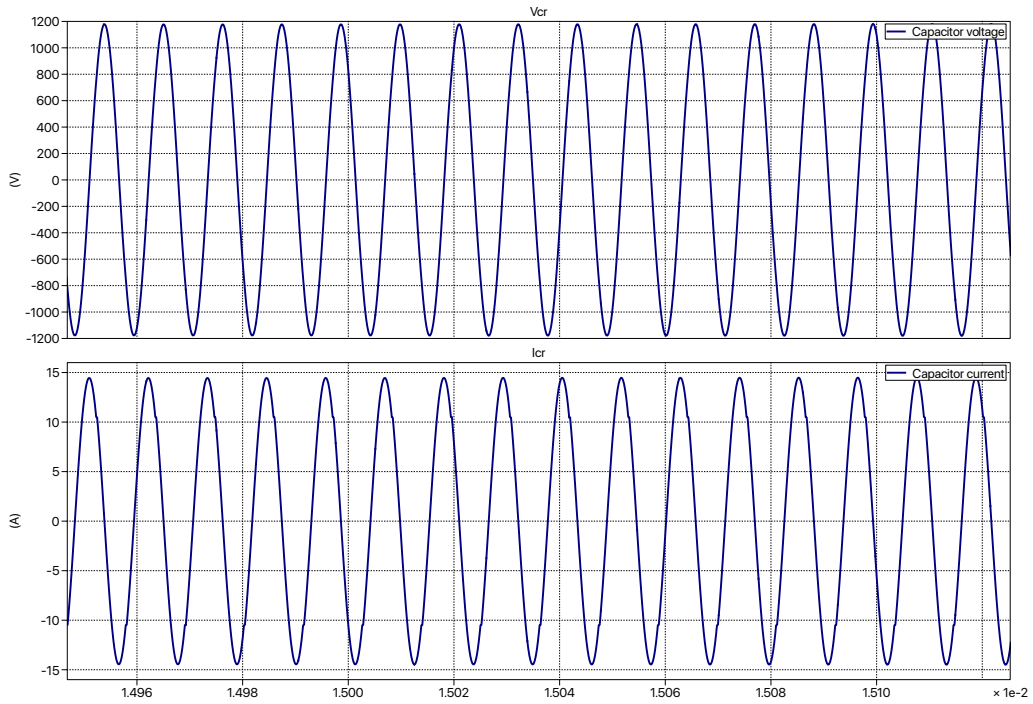


Figure 5.5: Voltage and current of the resonant capacitor during the simulation

During the simulations the value of current through the filter capacitor has been measured and it is equal to:

$$I_{C,filt} = 14.7Arms \tag{5.5}$$

Also the current and the voltage of the resonant capacitor has been measured (Figure 5.5):

$$V_{Cr} = 830Vrms \tag{5.6}$$

$$I_{Cr} = 10.3Arms \tag{5.7}$$

These value are useful in order to choose the commercial solutions for the capacitors.

5.3 Choice of the commercial components

The following list report the relevant values for choosing the commercial solutions of the components:

1. T-type converter

   - Input inductor:

   $$L_{in} = 200\mu H \qquad I_n \geq 16A$$

   - Output capacitor:

   $$C_{out} = 3mF \qquad I_n \geq 10A \qquad V_n \geq 400V$$

   - Diodes:

   $$I_F \geq 16.7A \qquad V_r \geq 800V$$

   - Mosfets:

   $$I_F \geq 16.7A \qquad V_r \geq 400V$$

2. LLC converter

   - Resonant capacitor:

   $$C_r = 40nF \qquad I_n \geq 10.3 \qquad V_n \geq 830V$$

   - Filter capacitor:

   $$C_{out} = 25\mu F \qquad I_n \geq 14.7 \qquad V_n \geq 420V$$

- Mosfets:

$$I_F \geq 7A \qquad V_r \geq 800V$$

- Diodes:

$$I_F \geq 13A \qquad V_r \geq 420V$$

Considering these results, the components has been chosen and the list is reported in Table 5.6. Note that in this section the data sheets of the resonant inductor and of the transformer are not reported because they have already been reported in the last chapter.

T-type converter

Component	Model name	Data sheet
Input inductor	VISHAY IHV	[18]
Output capacitor	259 PHM-SI	[17]
Diode	STPSC20H12-Y	[10]
Mosfet	ST Microelectronics SCTH40N120G2V7AG	[9]

LLC converter

Component	Model name	Data sheet
Resonant capacitor	CalRamic 10HS06N473JS	[1]
Output capacitor	MKP1848 DC-Link	[7]
Output inductor	IHDM-1008BC-30	[19]
Diode	STPSC20H12-Y	[10]
Mosfet	SCT30N120	[8]

Table 5.6: Chosen components for the LLC and T-type converters

The current capability and the rated current of the T-type output capacitor does not satisfy the specification. To overcome the problem it is been decided to

connect four VISHAY 259 PHM-SI in parallel to form one equivalent capacitor. So the T-type converter will have eight capacitors divided into two group. Each group form an equivalent capacitor with the following equivalent capacitance:

$$C_{out,eq} = 4 \cdot 0.68 = 2.72mF \tag{5.8}$$

The result is a bit less then the required value (3mF) so the expectation is an increased value of the ripple at the DC-link terminals.

The value of output capacitance on the LLC converter is a bit higher than $25\mu F$, so the ripple at the battery terminals will be reduced.

5.4 Simulation of the complete converter

The data sheet of the chosen components give all the necessary parameters for the last simulations in which the two converter are connected in order to form the complete battery charger.

Both single-phase and three-phase configurations have been simulated considering the parameters reported in Table 5.7. The initial voltage V_{C0} on the output capacitor of the T-type converter is lower than 400V so it is possible to see if the control of the DC-link voltage works or not. Moreover, the initial voltage of the battery is close to the maximum value because the aim of the simulation is to see the transition between the two recharging intervals.

The simulation with single-phase supply configuration (Figure 5.7) leaded to the following results:

- the input current has a sinusoidal waveform and it is in phase with the input voltage
- the current through the input inductors follow its reference value
- the value of the voltage on the DC-link is initially equal to $2V_{C0}$ and it increases with time until it reaches the reference value
- there is a ripple of 100Hz plus a high freqeuncy ripple on the DC-link voltage: the first one is due to the T-type structure and the second one is due to the

current absorbed by the LLC converter, which is affected by the switching frequency

- the battery current remain at first equal to zero until the LUT find the good value for its control
- after the first moments the battery current follows the reference value
- apart from the switching ripple, the battery current is affected by a 100Hz ripple due to the oscillation of the DC-link voltage
- the battery voltage slowly increases to reach the maximum value and then remain constant
- when the voltage reaches its maximum value, the battery current starts to decrease with time until it reaches values close to zero

The results of the simulation with the three-phase supply configuration (Figure 5.8) are very similar. Just some differences can be highlighted:

- the interval of the recharging profile with constant current is shorter because in this case the battery current is saturated to 25A (15A in the case of the single-phase configuration)
- when the current starts to decrease the voltage on the DC-link increases a little bit because the control bandwidth is not high enough to decrease the input current

The final increasing of the DC-link voltage is not a big problem because its value is very small (1% of the nominal value). Moreover, the time of the simulation is not realistic, in fact in real applications the recharging time take few hours. Consequently, in real situations, the control have time enough to respond to the changing of the battery current, so the DC-link voltage will not increase.

5.5 Simulation of the ZVS in the LLC converter

As mentioned in previous chapters, the LLC converter is employed in order to obtain the ZVS and increasing the global efficiency of the battery charger. The

design made in chapter 4 leaded to the choice of the resonant tank parameters and a simulation of the LLC converter using LTSpice is reported in this section. The result let to understand if the chosen parameters of the resonant tank will really permit the ZVS in the LLC converter. The parameters used in the simulation are reported in Table 5.8.

The aim is to analyze the switching process of the bridge inverter and the time interval of the simulation is very small. Consequently it is possible to consider the output capacitor of the LLC converter as a constant voltage source.

Looking at the turn-off transition (Figure 5.10) it is possible to see that the current through the mosfet decrease significantly before the voltage applied to its terminals reach the value of the input source. The commutation is not perfectly done with zero voltage, but it is a reasonable result and the turn off losses are very low if compared with hard switching converters.

To understand the turn-on transition (Figure 5.11) it is required to look also at the gate signal of the power switch. When the value of the current is negative and the gate signal is still equal to zero it means that the current is flowing through the body diode. When the gate signal switch to one, the voltage at the power switch is already zero, so the ZVS during the turn on is ensured.

T-type converter		
f_{sw}	20	$[kHz]$
V_{in}	220	[V]
L_g	100	$[\mu H]$
L_{in}	180	$[\mu H]$
C_{out}	2.70	[mF]
V_{C0}	390	[V]
V_{dc}^*	800	[V]
$\omega_{b,i}$	$2\pi f_{sw} \cdot 0.05$	[rad/s]
$k_{p,i}$	$\omega_{b,i}(L_g + L_{in})$	
$k_{i,i}$	$\omega_{b,i} k_{p,i} \cdot 0.1$	
$\omega_{b,v}$	$0.005\omega_{b,i}$	[rad/s]
$k_{p,v}$	$\omega_{b,i} C_{out}$	
$k_{i,v}$	$\omega_{b,v} k_{p,v} \cdot 0.005$	

LLC converter		
L_m	108	$[\mu H]$
L_r	62	$[\mu H$
C_r	47	$[nF]$
n	2	[ ]
C_{out}	40	$[\mu F]$
L_{out}	10	$[\mu H]$
$C_{batt,eq}$	0.5	F
$E_{batt,in}$	416	V
$\omega_{b,i}$	$2\pi f_{sw} \cdot 0.5$	[rad/s]
$k_{p,i}$	$\omega_{b,i} L_{out}$	
$k_{i,i}$	$\omega_{b,i} k_{p,i}$	
$\omega_{b,v}$	$\omega_{b,i} \cdot 0.01$	
$k_{p,v}$	0	
$k_{i,v}$	$\frac{\omega_{b,v}}{R_b}$	

Table 5.7: Parameters for the Simulation of the complete battery charger

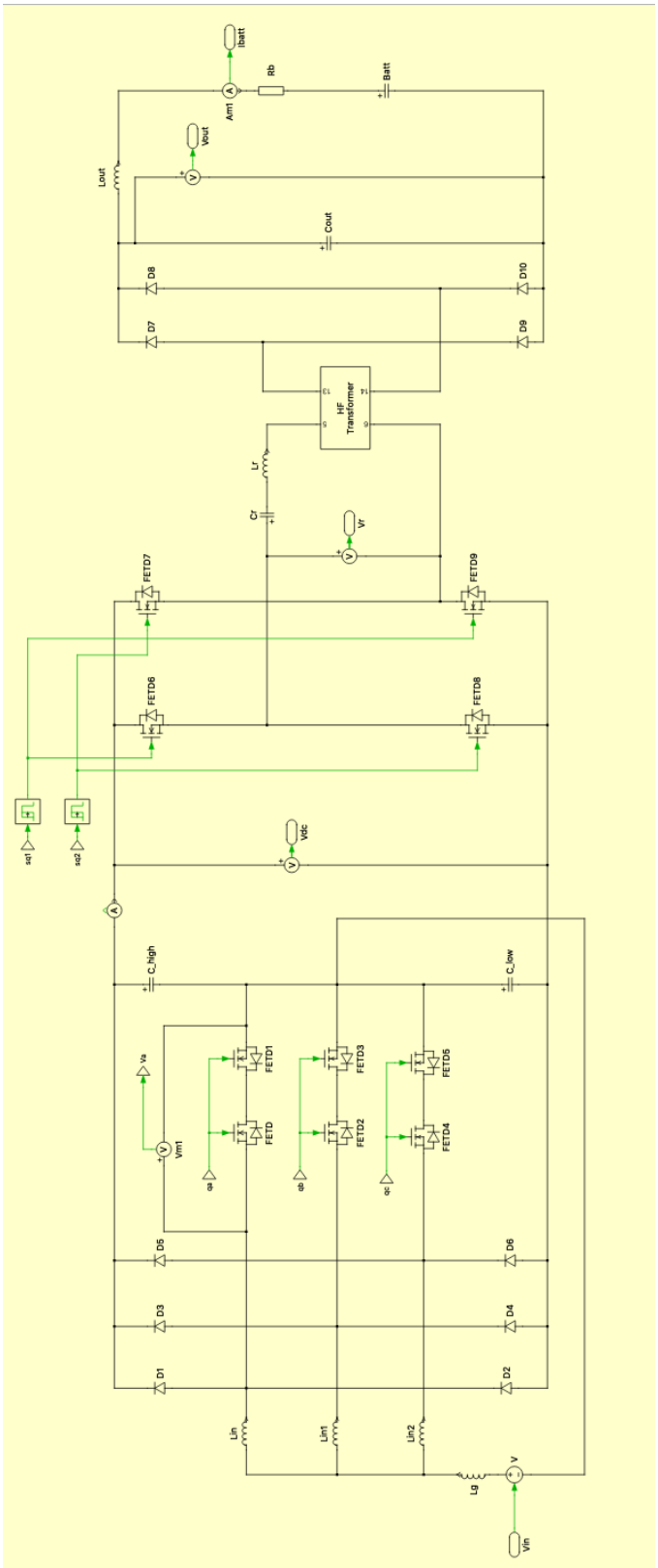


Figure 5.6: Schematic in PLECS of the complete converter with single-phase supply configuration

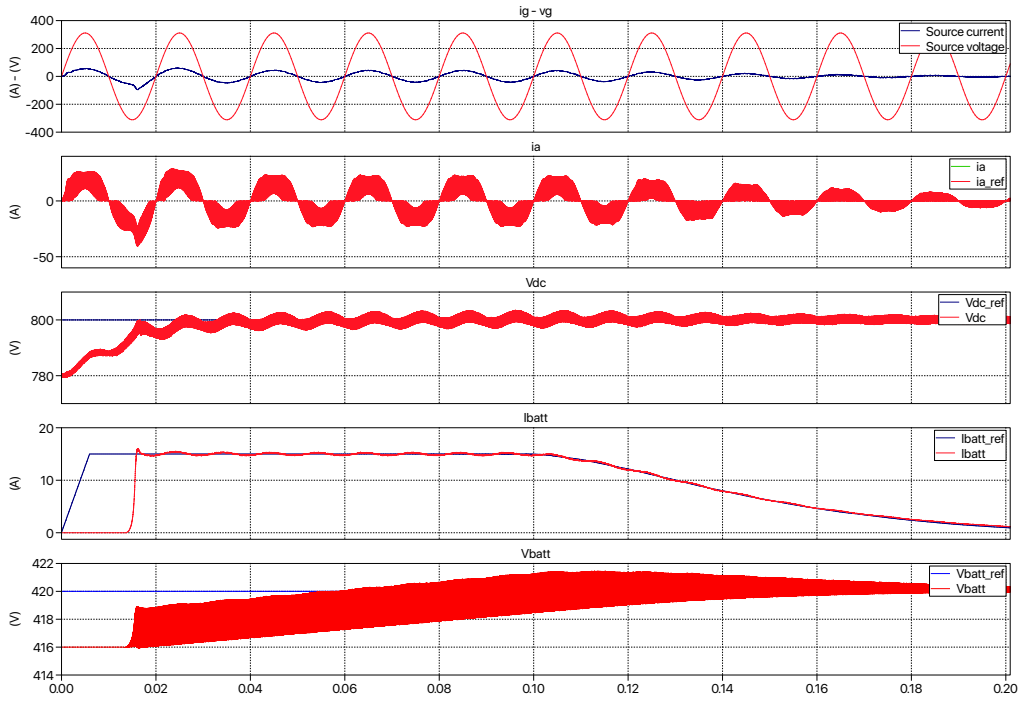


Figure 5.7: Results of the complete battery charger with single-phase supply configuration

V_{in}	800	V
V_{batt}	380	V
L_m	108	$[\mu H]$
L_r	62	$[\mu H$
C_r	47	$[nF]$
n	2	[]
t_{dt}	400	ns
C_{oss}	130	pF

Table 5.8: Parameters of the LLC converter for the simulation in LTSpice

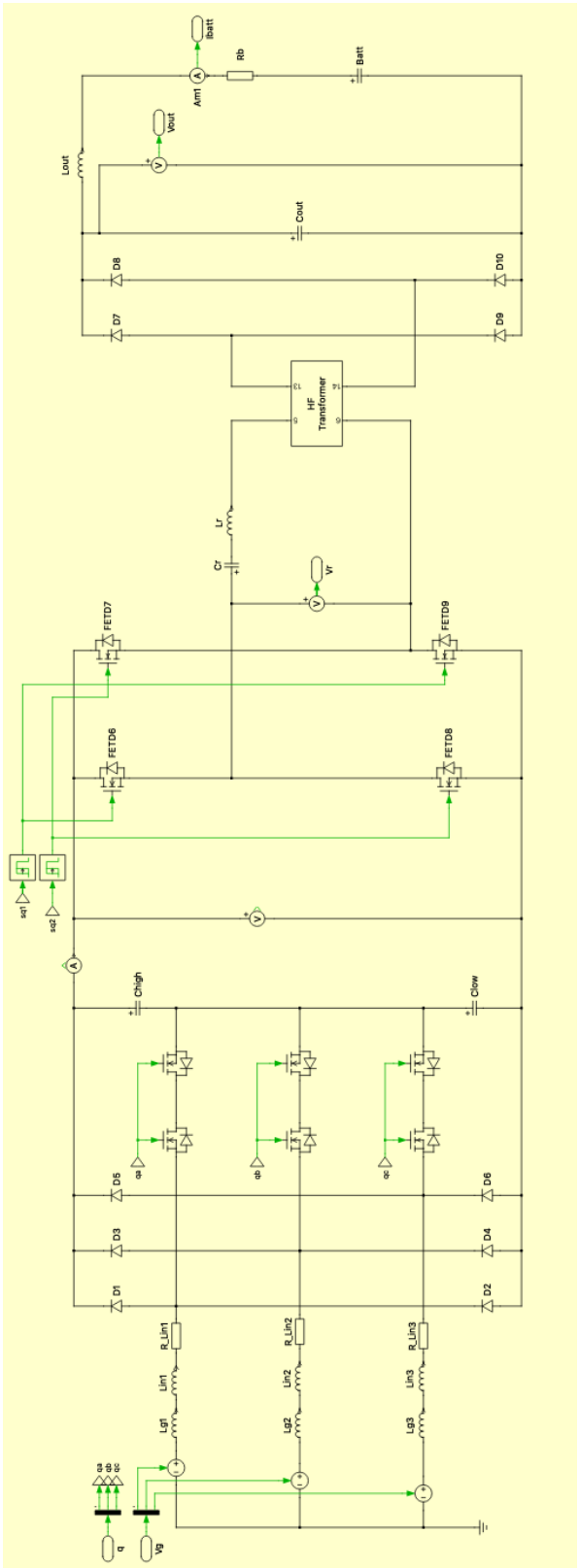


Figure 5.8: Schematic in PLECS of the complete converter with three-phase supply configuration

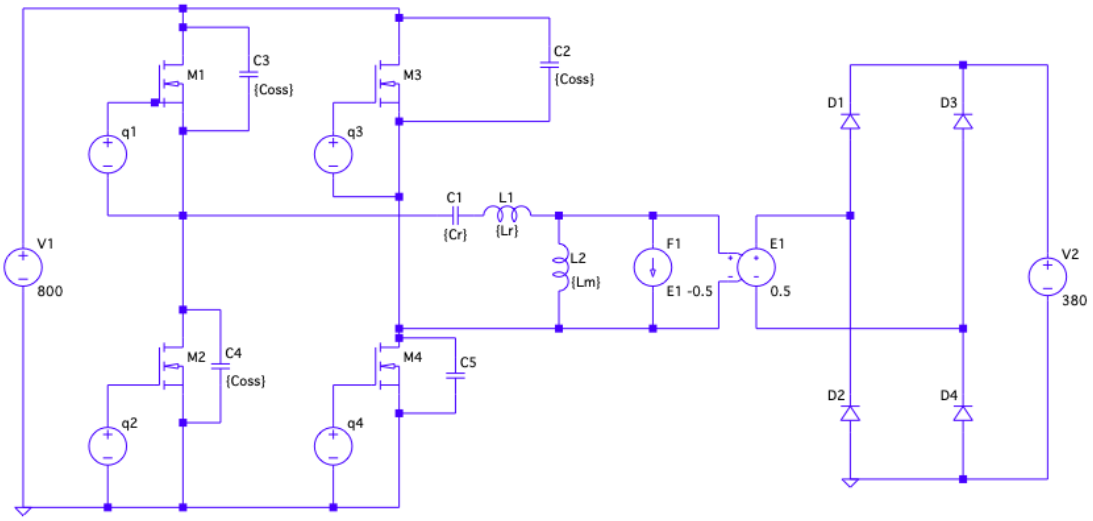


Figure 5.9: Schematic of the LLC converter for the simulation in LTSpice

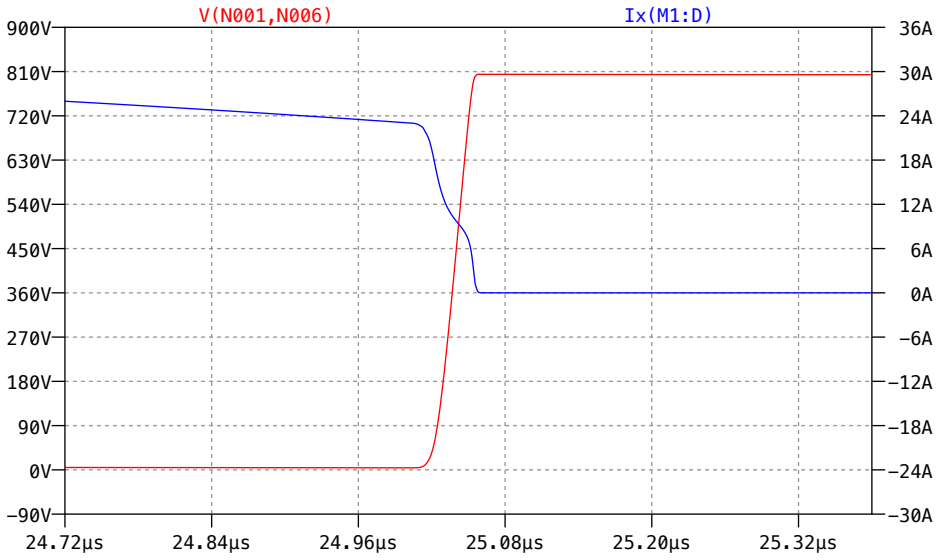


Figure 5.10: Turn-off transition of the power switch in the LLC converter

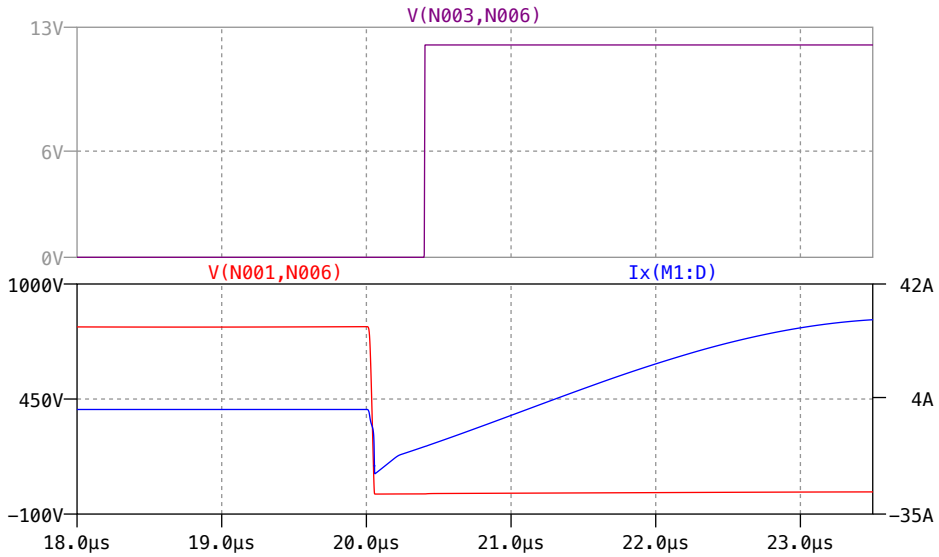
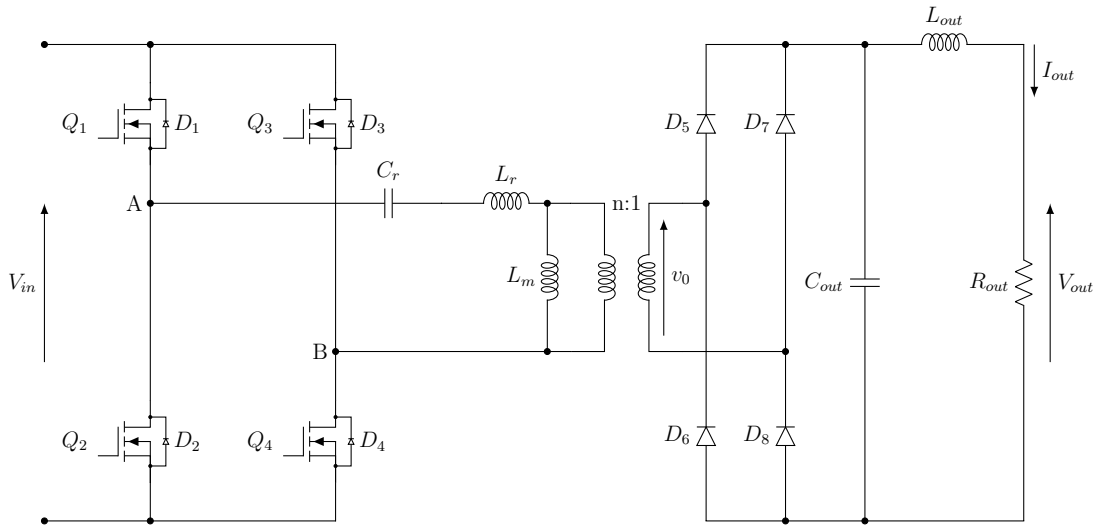


Figure 5.11: Turn-on transition of the power switch in the LLC converter


L_{out}
I_{out}
Q_1
D_1
Q_3
D_3
D_5
D_7
C_r
L_r
A
n:1
V_{in}
L_m
v_0
C_{out}
R_{out}
V_{out}
B
Q_2
D_2
Q_4
D_4
D_6
D_8

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