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Tesi di Laurea Magistrale

Versatile power electronics teaching setup



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The logo of the École Polytechnique Fédérale de Lausanne (EPFL) is displayed in a bold, red, sans-serif font. The letters are stylized, with the 'E' and 'F' having a distinctive geometric design.

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Abstract

The goal of this work is to design, size, simulate, realize, test, validate and investigate an open and customised power electronics teaching setup platform that will be used by the power electronics laboratory of the EPFL for teaching purposes.

The aforementioned system is made in order to be as modular as possible allowing to perform different converter topologies operations, exploiting the hardware and software potentialities of it and keeping all the safety requirements.

In particular, using two converters (3 phase rectifier+ 3 phase inverter) from Hyundai and replacing all the control boards with an open and completely custom system interface from Perun technologies, it is possible to give the possibility to the user of programming in real time the DSPs with PLECS or Simulink C code generation tools interfacing the system directly to a personal computer.

This way, there is the opportunity of running an initially wanted simulation in a physical environment, performing manoeuvres and experiments using the desired control technique in a real system for teaching or research objectives.

For what concerns the hardware potentiality of the system, the user through a reconfiguration physical panel can decide which physical connections enable inside the system giving rise to the desired converter topology operation.

Furthermore, in order to make the system more custom enabling several converter topologies, relevant electrical elements are added to the setup.

Indeed, using AC and DC power supplies, an AC grid emulator, a motor load, two braking resistors, an LC filter, boost inductors and a precharge circuit the system potentialities become remarkably.

It has to be underlined that the personal contribution of the candidate to this work is on the hardware and power components aforementioned above having the shrewdness of using a systematic and engineering approach covering all the design and prototyping steps.

Moreover, the focus is also on design and realization of some unique auxiliary measurements PCBs components such as a PCB safety light controller board and a GPIO collecting signals board.

Once the system will be fully complete and tested 20 other models will be realized by a professional company based on the prototype and put in the lab.

List of Acronyms

Acronyms

CCS	Code composer studio
DSP	Digital signal processor
EMC	Electromagnetic compatibility
EPFL	Ecole polytechnique fédérale de lausanne
FTDI	Future technology devices international
GCC	Grid control card
GPIO	General purpose input output
GUI	Graphical user interface
HMI	Human machine interface
IDE	Integrated development environment
IGBT	Insulated gate bipolar transistor
MCC	Motor control card
PCB	Printed circuit board
PETS	Power electronics teaching setup
PLL	Phase lock loop
PWM	Pulsed Width modulation
SMT	Surface mounted technology

Chapter 1

Introduction

1.1 Background

The main interest of this work is to design, size and choose the components in order to build a programmable and customised power electronics teaching setup (PETS) that allows reconfiguration and experimentation considering different topologies and applications.

This setup is going to be tested and validated and then used by the EPFL students in order to do maneuvers and experiments in the lab for having a better understanding of the theory seen during different lectures in courses at Bachelor and Master level where the goal is to design and control grid connected power converters.

This project is done following a precise path articulated according to the following main points:

- understanding of the theory principles behind the different converter topologies and related components
- design and sizing of relevant external components
- offline simulations through different softwares such as PLECS in order to verify the results of the sizing
- building and assembly of the hardware followed by tests and validations in order to match the results of the simulations
- Experimental testing and validation of different parts of the system

1.2 Configuration of the teaching setup

The strength of this setup is that the user through an existing physical panel, that will be shown and explained in detail later, can achieve different system topologies through reconfiguration and interconnections, acquiring a better understanding of the converter principle operations and keeping all the safety requirements.

The overall system, shown in the Figure 1.1, can operate with an AC or a DC source and manage the power efficiently in order to transfer power to an AC grid load or a motor drive load by means of two power electronics converters and related electrical external elements.

The flexibility of the system is achieved through replacement of the original control of the

industrial power converters that was changed with open and flexible DSP-based controller, that will be analyzed in detail in the next chapter, giving the user the possibility to program directly the converter interfacing the system to a personal computer and making the system customized.

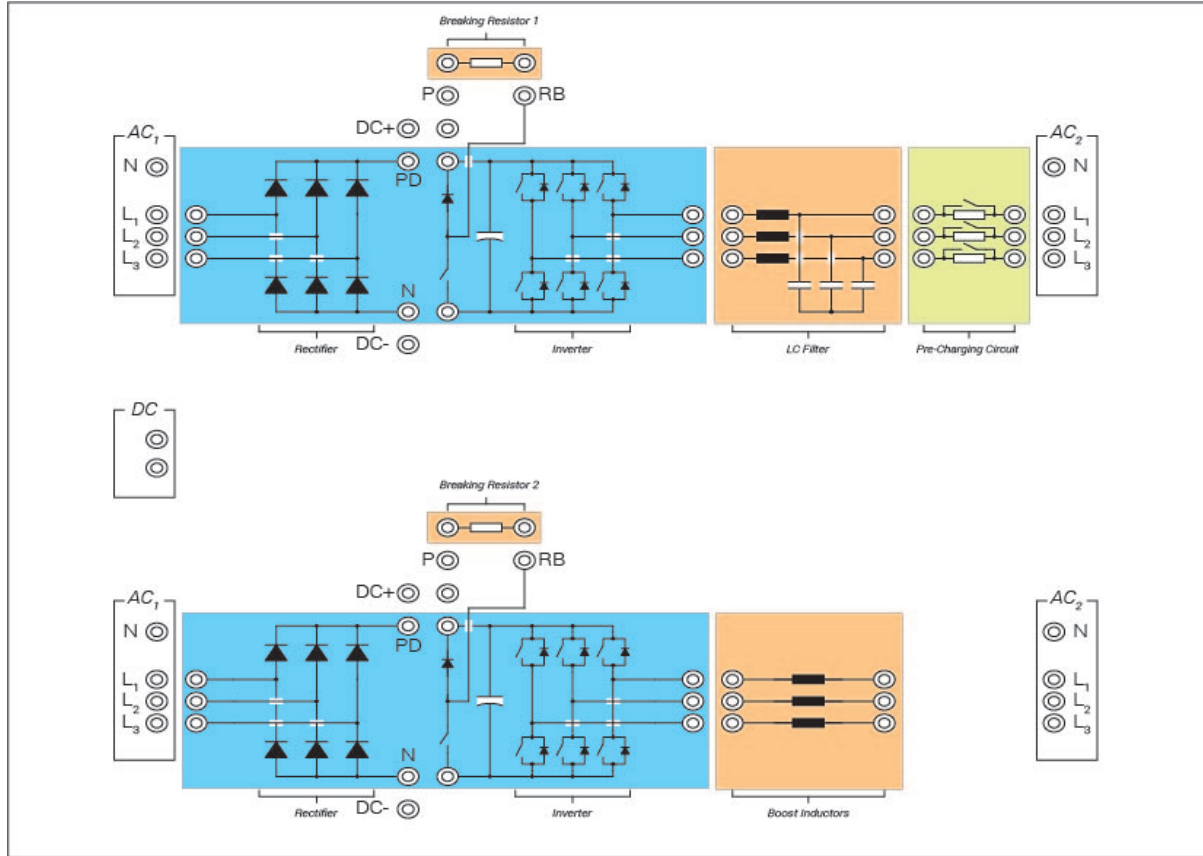


Figure 1.1: Schematic of the reconfiguration panel

The system as can be deduced from the previous schematic illustration is composed by the following main elements that will be described in detail in the next chapters:

- Power supply
 - AC1 power supply (3-phase, 400V, 5kVA)
 - DC power supply (600V, 3.5kW)
- power electronics
 - two power converters: rectifier+inverter (5.5kVA each one)
- power electronics related elements
 - LC filter
 - precharge circuit
 - boost inductors
 - two braking resistors one per converter
- external laboratory equipment
 - AC2 power supply
 - AC2 motor load

User interface

The reconfiguration panel allows the user to realize desired topology of the system, for different exercises, indeed the user has the possibility to operate on the power part connecting or not with some plugs the active and external passive components of the converters giving the possibility to operate with different power electronics topologies. About that, the Figure 1.1 shows the schematic of the reconfiguration control panel accessible by the user.

Using some isolated plugs shown in the Figure 1.2 and placing them inside the connectors present on the panel is possible to connect electrically the terminals exposed in the panel allowing the physical connection inside the setup.

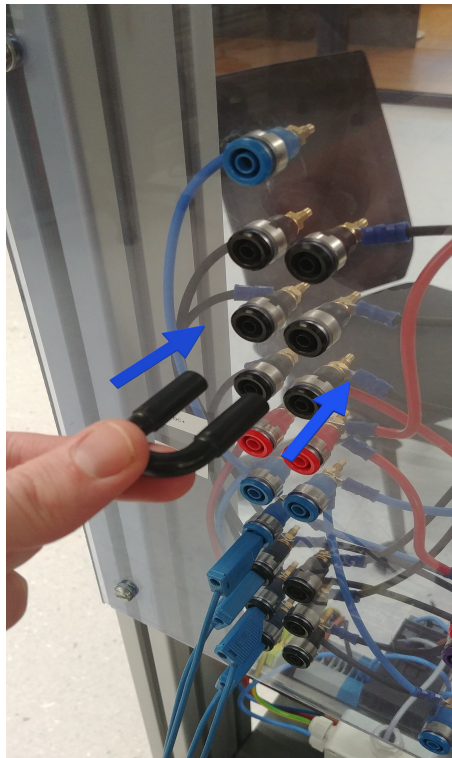


Figure 1.2: External plugs used by the user to electrically connect elements by the means of the reconfigurable panel

The modularity comes from the fact that using those plugs is possible to link the two drives to the following setup components:

- AC1 or DC source
- external braking resistors
- external LC filter
- external boost inductors
- external precharge circuit
- AC2
- connection between rectifier and inverter through the DC bus

Power converter topologies

The teaching setup is done in order to be as modular as possible so the user can set the power configuration, AC or DC by connecting relevant elements on the reconfiguration panel.

Furthermore, the flexibility of the system allows different converter topologies operations such as:

- three phase diode rectifier
- single phase diode rectifier
- interleaved boost converter
- 1,2 or 4 quadrant DC-DC converter
- three phase inverter
- back to back converter putting the two drives in parallel

About that, several examples are shown in the Figures below:

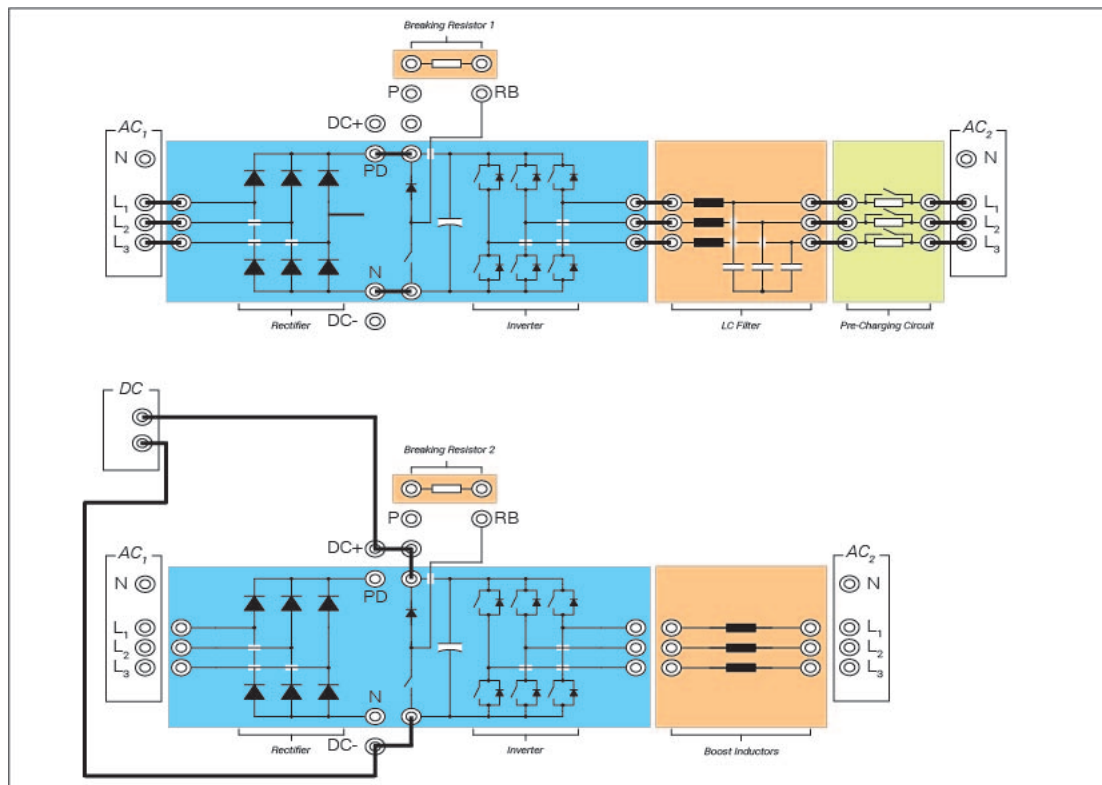


Figure 1.3: In this example configuration, the upper inverter is supplied from the AC1 source through a diode rectifier, while the bottom inverter is directly supplied from the DC source

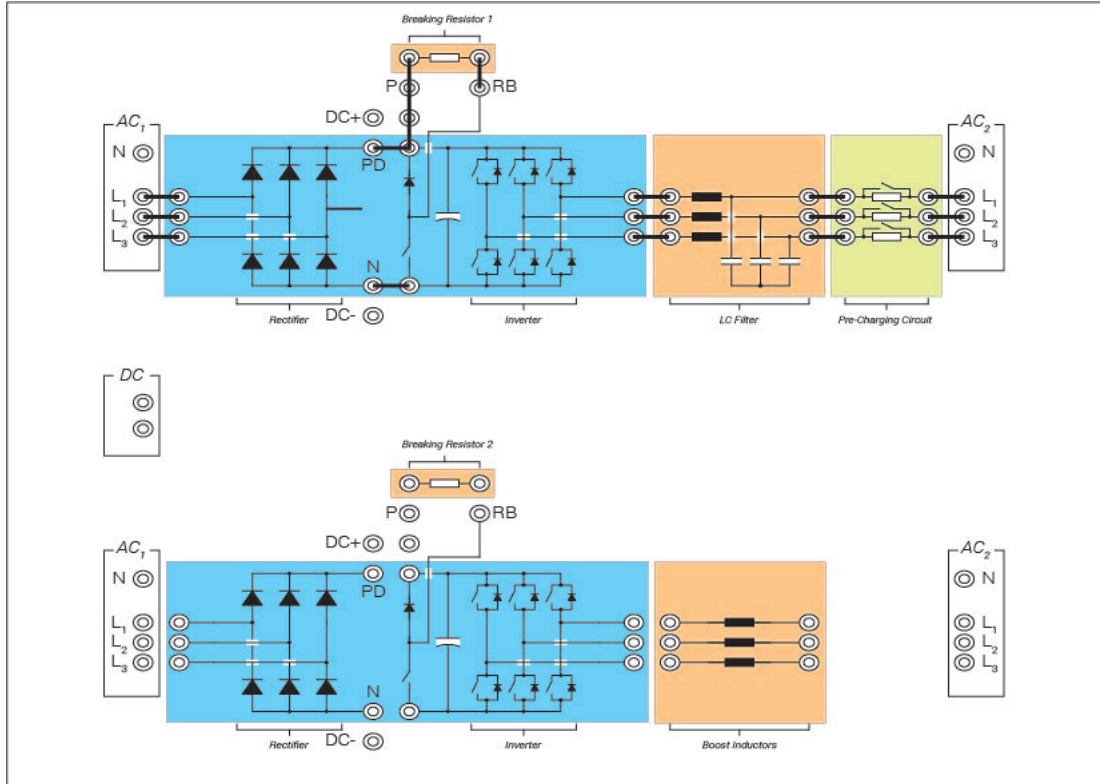


Figure 1.4: In this example configuration, the upper inverter is supplied from the AC1 source through a diode rectifier and the braking resistor is responsible of limiting the DC link voltage exceeding rated values

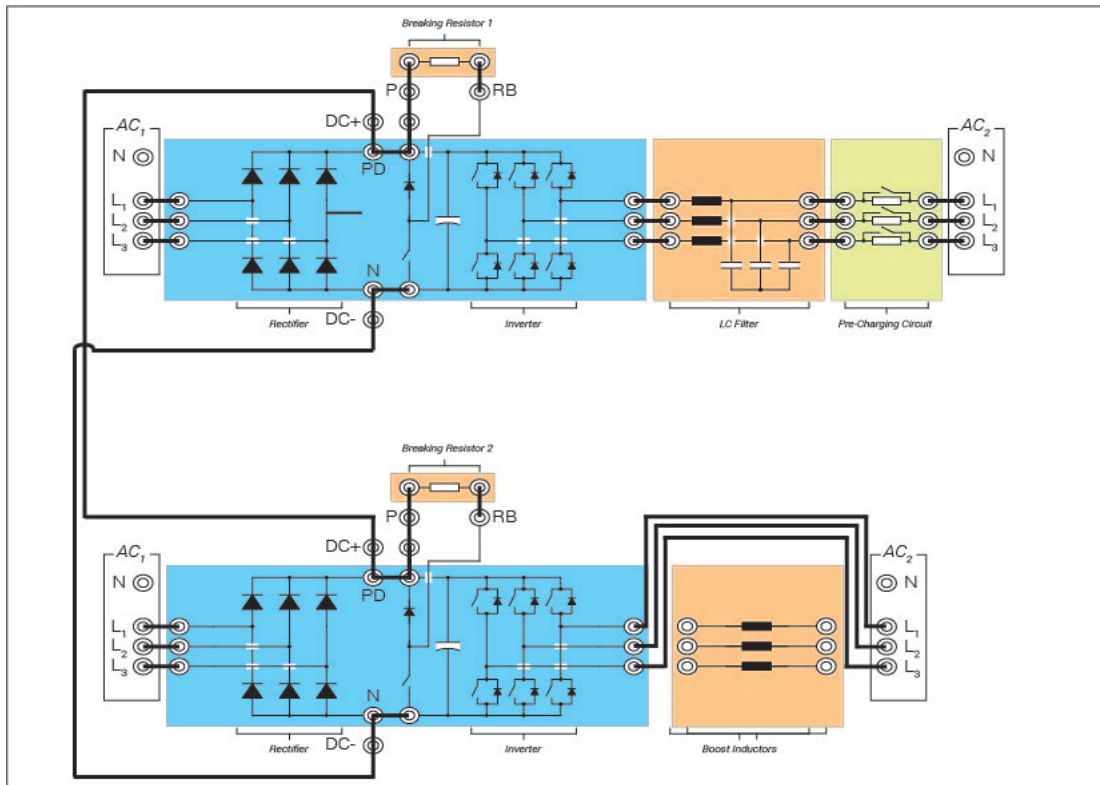


Figure 1.5: In this example configuration, the upper and bottom topology are connected in parallel giving rise to a back to back operation

1.3 Project objectives and limitations

The scope of this work is to design, realize, simulate, prototype, test and validate the aforementioned power electronics setup (PETS) in order to make as clear as possible for the user the exploitation of the power converters.

Furthermore, the building and prototyping process is complete including the installation, the cabling, the mounting, the soldering of new designed PCBs and so on, giving the possibility to understand all the processes of industrial prototyping and assembly.

Once the system will be successfully tested other 20 models will be realized by a professional company based on that prototype and put in the lab.

1.4 Structure

This master thesis is divided into 6 chapters according to the following structure:

1. Introduction and presentation of the system underlying the goals and objectives of this work
2. Description of the system and related hardware and software components explaining how is done the exploitation by the user and the potentialities of the setup
3. Design, sizing, prototyping, test and validation of some components composing the system in order to match the results from the simulation to the realization
4. Design and prototyping of some sensing and measurements PCB components
5. Final hardware version of the power electronics teaching setup
6. Conclusions and future works

Chapter 2

Description of the overall system

2.1 Power stage

The system is composed by the following electrical and power electronics components:

2.1.1 Power supply components

- AC1 power supply
 - the system is connected to the grid through a 3 phase (L1, L2, L3) + neutral(N) and ground (PE) industrial power connector for the 230 V phase AC grid connection



Figure 2.1: Three phase connector

- 4 poles circuit breaker: 3 phase + neutral and ground Schneider electric ic60h circuit breaker that protects the system from overloads and short-circuits interrupting the current flow when a fault occurs



Figure 2.2: 4 poles circuit breaker [3]

- 4 poles contactor: Siemens Sirius 230 V 3 phase contactor that is driven by a control circuit in order to energize the equipment on the setup

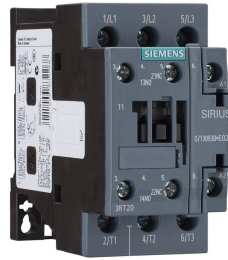


Figure 2.3: 4 poles contactor [4]

- transformer: Erea three phase delta-star 4 kVA transformer with a transformation ratio 1:1 used for isolation safety purposes

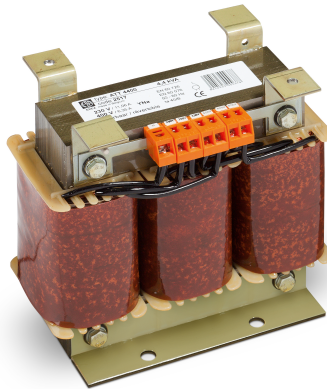


Figure 2.4: Transformer [5]

- three phase 5.5 kVA Ruhstrat toroidal variable Variac that is responsible for continuous transformation ratio variation giving the possibility to adjust the desired AC voltage at the reconfiguration panel where converters are connected



Figure 2.5: Variac

- DC power supply: Delta elektronika SM3300 ar11 DC power supply that is feed by the 3 phase AC supply and is responsible for emulating a 3,3 kW PV panel allowing an output voltage range of 0-330 V and an output current range of 0-11 A. This power supply can work up to 4 interface modules: Analog, Digital, Isolated and Ethernet interfaces.



Figure 2.6: Delta DC power supply [6]

2.1.2 Power converter related elements

- two braking choppers for the two respective drives, that convert the power into heat dissipating the regenerative power through a resistor, in order to limit the DC link voltage.

Indeed, they intervene in case the motor load feeds back power behaving like a generator during uncontrolled generation operation for the bottom drive or dissipating the power coming from the AC2 four quadrant power supply for the top drive



Figure 2.7: Braking resistor

- LC filter allowing the connection of the inverter and AC2 grid emulator

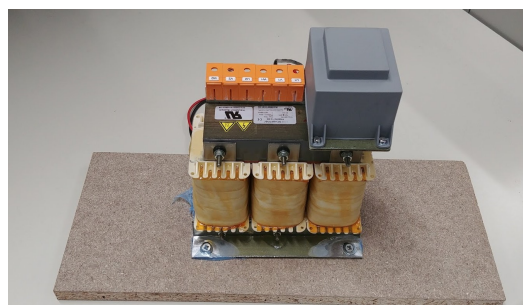


Figure 2.8: LC filter

- precharging circuit for limiting the starting inrush current in the capacitors, composed by three resistors, a 4 poles contactor and a timer that triggers the latter

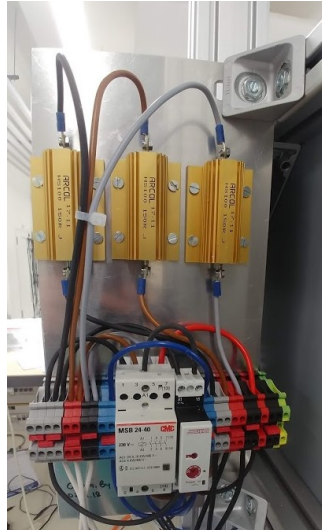


Figure 2.9: Precharge circuit

- boost inductors connected to the inverter that allow the system operating as a interleaved boost converter stepping up the voltage

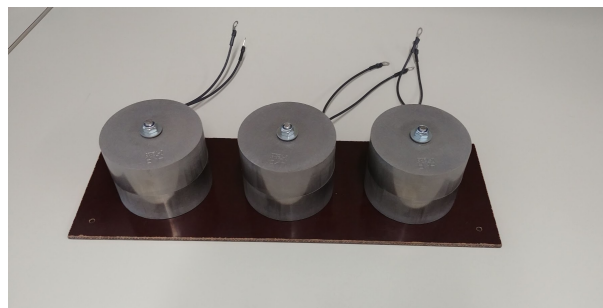


Figure 2.10: Boost inductors

2.1.3 External related laboratory equipment

- AC2 laboratory grid emulator four quadrant Regatron power supply that should simulate a grid "load" for the drive in the top



Figure 2.11: Regatron grid emulator

- AC2 motor load for the drive in the bottom

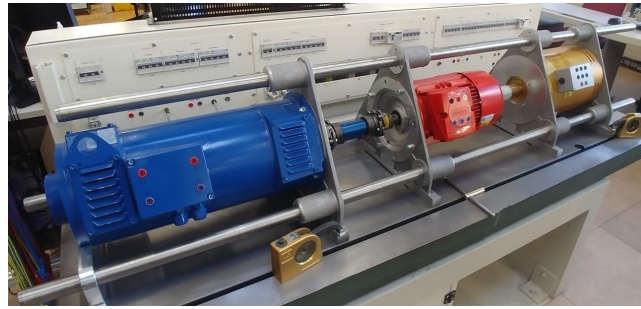


Figure 2.12: Motor load

2.1.4 Power converters drives

- two identical 5 kW Hyundai n700 power converter, for the two respective drives, composed by rectifier+inverter
 - rectifier: uncontrolled three-phase diode full-wave bridge rectifier
 - inverter: three-phase inverter composed by three legs each one with 2 IGBT and antiparallel diodes



Figure 2.13: Original Hyundai n700 hardware power converter [7]

It has to be underlined that as mentioned in the introduction, the original control of the Hyundai converters was changed and replaced with an open and configurable platform called Perun Lara 100 from the company Perun Technologies giving the possibility for the students to interface the system to the computer.

The only component not changed is the original plastic structure of the converters while the platform and all his related elements and control boards will be analyzed in the next sections.

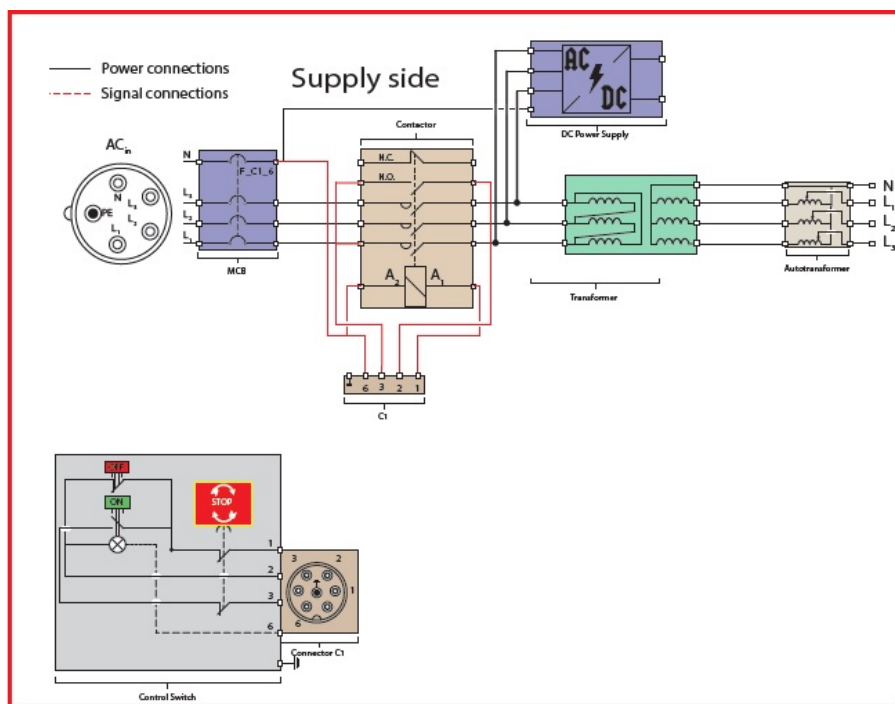
2.2 Control stage

The system is composed by the following control signals and control devices which make the whole system manageable and operating:

2.2.1 External related control devices

Safety equipment

- Emergency stop control setup:
 - the green button allows to turn on the system and is a normally open switch, this way when the user press the button green the system starts operating because the contactor and the normal open switch are closed
 - the red button allows to turn off the system and is a normally closed switch, this way when the user press the red button the system stops operating because the contactor and the normal close switch are open
 - the bigger red button allows the emergency stop of the system and is a double normally closed switch, this way when the user press the red big button the system stops operating for any emergency situation



(a) Contactor and emergency stop setup electrical scheme



(b)
Emergency
stop and
operation
control box

Figure 2.14: Emergency stop and input power control device

- Two lamps safety panels per converters: device that is responsible for the safety of the system operation allowing control signals turn on the lights in case of

- experiment on is when the motherboard, that will be covered and explained later, is sending a signal to the Relay output connector 1 connected to the safety lamp that turns on the Red light
- setup powered is when the motherboard is sending a signal to the Relay output connector 2 connected to the safety lamp that turns on the Green light
- DC link charged is when the DC link sensing circuit observes a voltage on the DC Link and send a signal to the Orange light that turns on
- setup grounded is when an external Relay is connected to a 24 V power supply and turns on the White light



Figure 2.15: Safety lamp

2.2.2 Customized control boards from Perun technologies

Motherboard, expansions boards and controllers

- Perun Lara 100 motherboard that behaves like a dock board for the DSP controller and is able to communicate with the power stage and other applications boards
- Perun UI application board Grid Control Card (GCC) board for measuring additional voltages or currents, in particular will be used for measuring the voltage of AC2 for grid synchronization using the Phase Locked Loop (PLL)
- Perun encoder application board "ENC INC SSI 5V" Motor Control Card (MCC) board for the motor drive encoder
- Perun communication board "COMM 01" that enables the system to communicate with standard communications protocols such as CAN, RS485 or Ethernet giving the possibility to connect the system with external equipment such as PLC, encoders, resolvers or even to connect the two Lara 100 motherboard in the back to back configuration
- Perun I/O board "GPIO 01" board that consists in analog and digital inputs and outputs where the pins will be available for the final user giving the possibility of interfacing switches, contactors, meters, buttons, leds and so on.

- Texas Instruments TMS320F28335 Digital Signal Processor (DSP) controller that is a floating point controller 150 MHz, 34K x 16-bits SRAM, 256K x 16-bits Flash and I/O peripherals high performance device for power electronics applications and is used in the setup for pin allocation in the Hyundai power converters

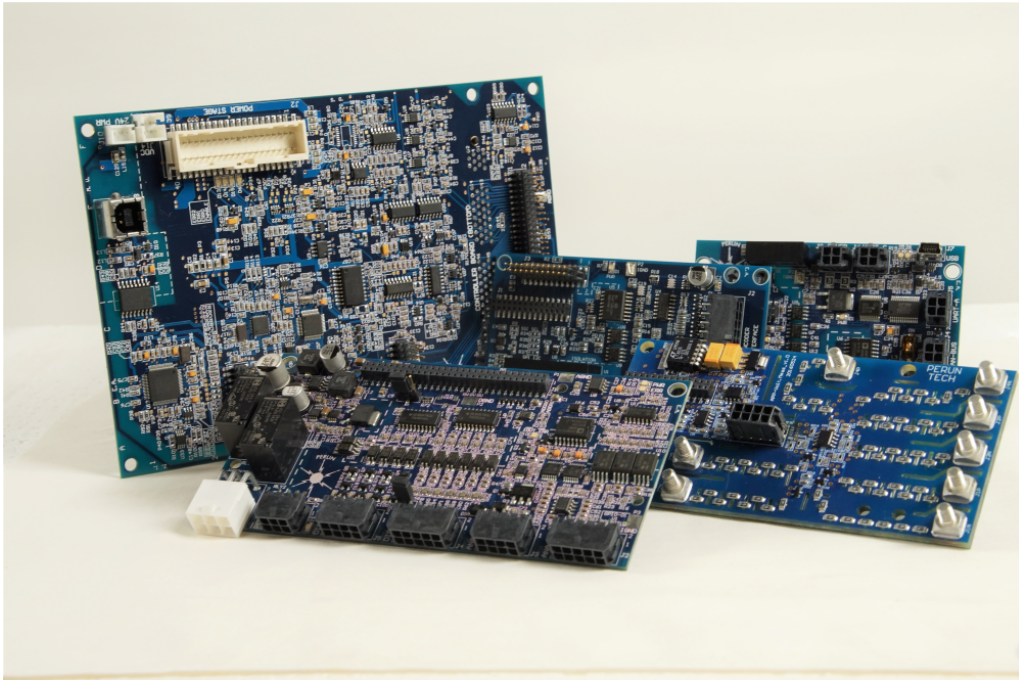


Figure 2.16: Lara 100 control board and expansion boards used from Perun Technologies [1]

Therefore, the aforementioned boards, illustrated in the picture 2.16, are used instead of the original Hyundai boards.

Furthermore, for understanding better the control components interaction, in the Figure 2.17, is possible to see the connection between the DSP, motherboard and the other boards with the complete pinout allocation.

Farther, in red arrows are underlined the protection and error signals, in yellow the communication signals, in green the measured and feedback signals and finally in blue the logic execution signals.

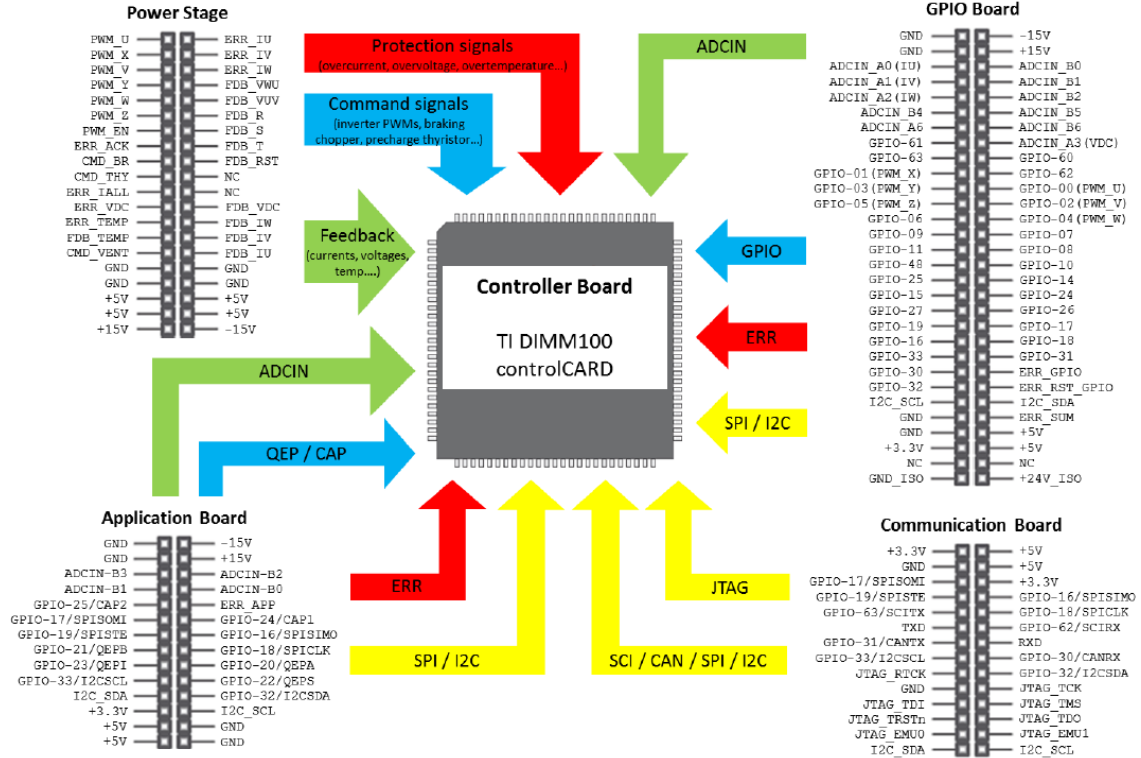


Figure 2.17: Connections between the DSP, the power stage and the other application boards through the Lara 100 Motherboard as docking board and pinout definition [2]

2.2.3 Power stage control signals

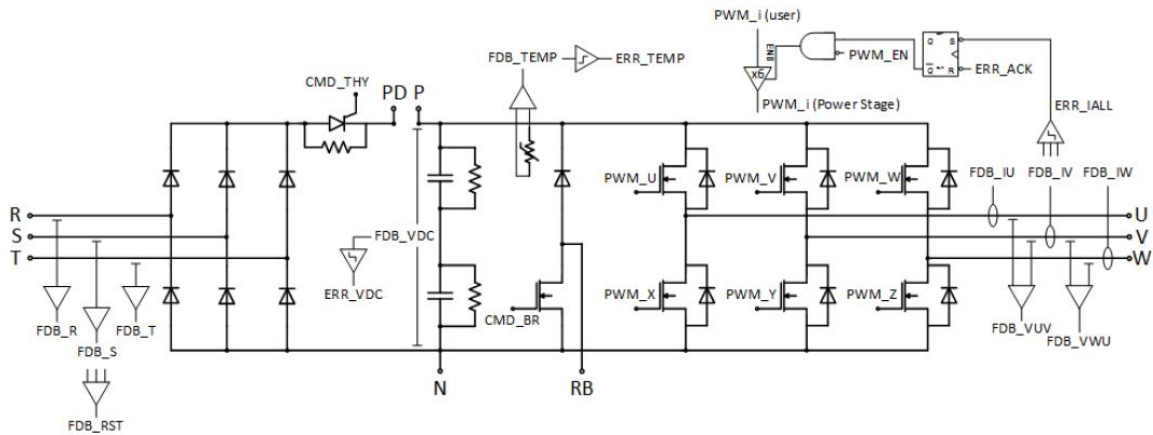


Figure 2.18: Power stage signals [1]

From the Figure 2.18 is possible to see all the command control signals for the power stage interface in order to exploit power electronics components acquiring all measuring and protection signals that are conditioned and given to the DSP.

Those signals are:

- DC link voltage measurement
- three phase power converter input voltages R,S,T
- three phase power converter output voltages and currents
- braking resistor IGBT command signal
- heatsink temperature and overtemperature protection signals
- 6 PWM signals
- thyristor command signal for the internal precharge circuit

2.3 Software platform interface

The user in order to interface to the system will use the commercial software from Perun Technologies called Perun Power Desk (PPD). This feature allows high level debugging of the converters enabling auto-coding generation and also some signal processing and analysis tools in real time.

In other words, it represents the Human Machine Interface (HMI) or Graphical User Interface (GUI) of the system that allows to declare some global variables.

Moreover, the code is not written in Perun Power Desk (PPD) but in the Texas Instrument IDE controller platform called Code Composer Studio (CCS) and load directly to the DSP, because the Perun software is just for manage data and acquire variables.

Indeed, the final user will be able to program directly the DSP using Simulink or PLECS coder that allow to generate the C code for the DSP.

About that, in the Figure 2.19 is shown the code generation in Simulink and loading on DSP interfaced through the Lara 100 motherboard to the computer using the Future Technology Devices International (FTDI) chip with Perun Power Desk software where is possible to store variables, doing plots and some data processing.

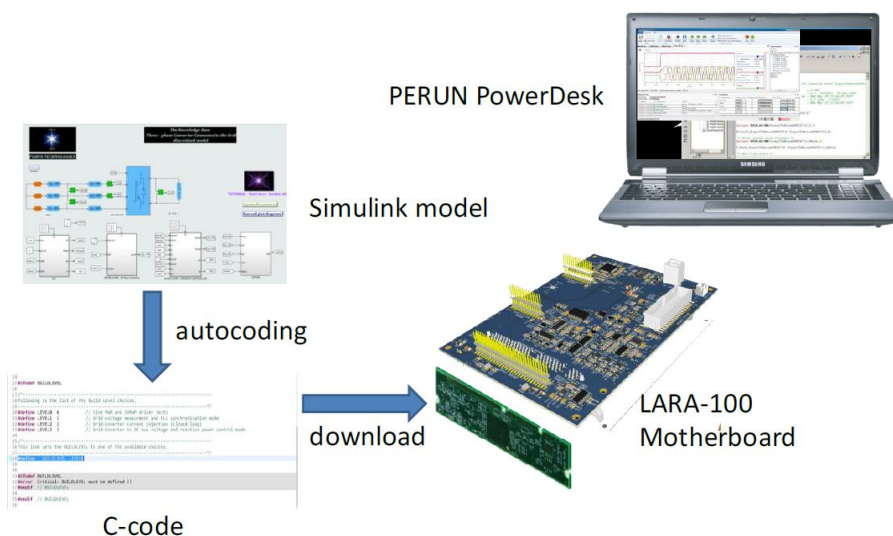


Figure 2.19: PPD, DSP and motherboard illustration [1]

2.4 Overall hardware and software operation

Furthermore, the Figure 2.20 gives a general overview working representation of the Lara 100 operation and underlines the link between the power electronics components, the signal boards components and the user software interface.

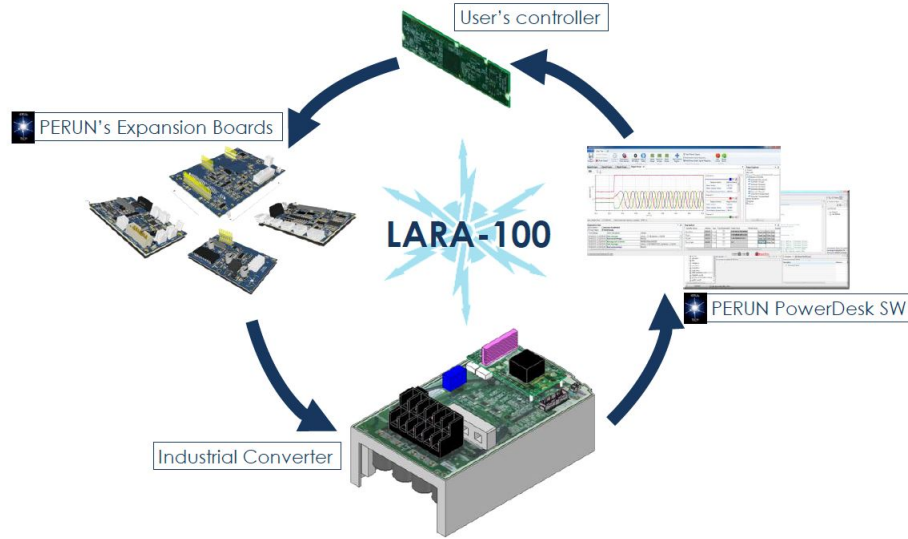


Figure 2.20: Perun Lara 100 overall principle operation [1]

2.5 Final user's dashboard external interface

The final user will have the possibility to use a system interfaced dashboard with: knobs, potentiometers, digital and analog ports that is connected to the GPIO board of the Perun system.

This way become easy acquiring measurements, set quantities values and so on reading all the variables from an outside system interface.

Chapter 3

Electrical design, sizing, test and validation

In this chapter, a precise systematic approach is followed by designing, sizing and testing some relevant components for the system.

In particular, the relevant elements that will be taken into account are:

- boost inductor
- braking resistor
- LC filter
- precharge circuit

3.1 Boost inductors

In this section the step process aforementioned is followed in order to find proper boost inductors available on the market and place the order for them.

3.1.1 Sizing of the boost inductors

About that, when the power supply is DC the model behave like a three phase interleaved boost converter [8] due to the presence of boost inductors, diodes and IGBTs of the inverter.

In particular, one converter can be used as PV boost DC-DC converter and the availability of 3 legs provide opportunity to implement interleaved DC-DC boost converter.

Moreover, the boost inductors of the interleaved converter require sizing and design, this way in the next sections theory, sizing, simulation, verification will be covered.

Before starting the sizing of the elements, in the Figure 3.1, is presented the three phase interleaved boost topology where are visible the aforementioned boost inductors.

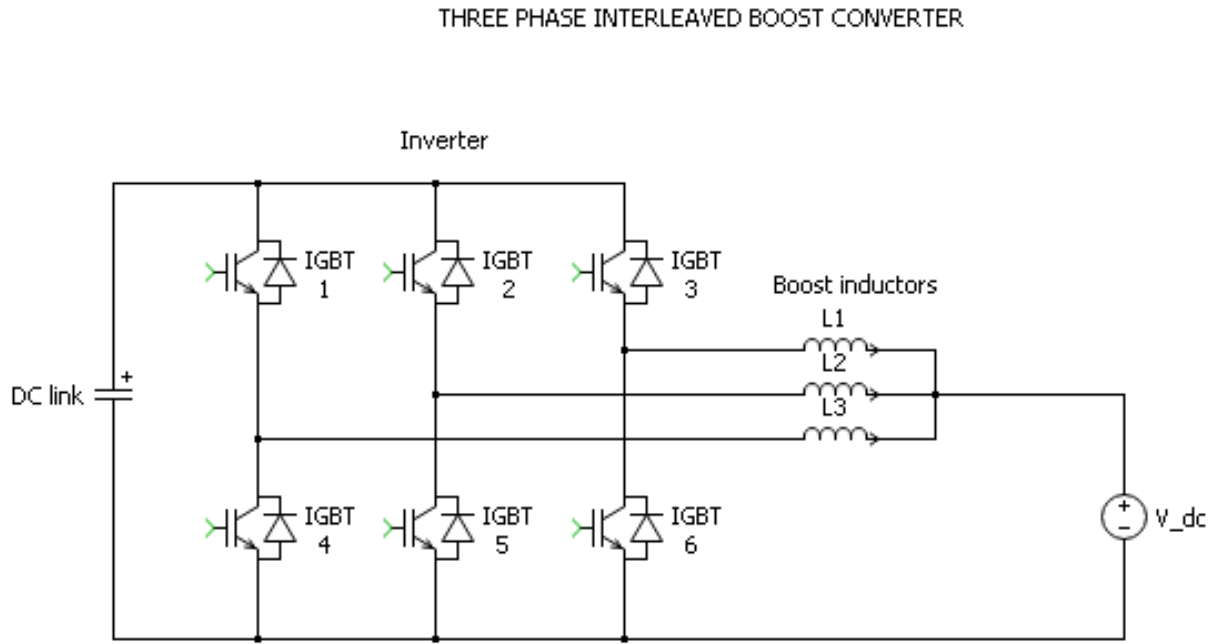


Figure 3.1: Interleaved boost converter topology

The purpose is to size the boost inductances in order to limit the current ripple. Starting from the duty cycle expression for a boost converter

$$d = 1 - \frac{V_{in}}{V_{out}} \quad (3.1)$$

where

- V_{in} is the boost DC input voltage, in other words the output of the PV system that has the following range $V_{in} = 200$ to $400V$
- V_{out} is the boost output voltage that we want to keep constant at the $600 V$ value because is the DC link voltage

Being in the worst case the power to handle $P_{in} = 1.5kW$ for each phase, so 4.5 kW total power, we need to calculate the phase current of the inductor:

$$I_{in,worstcase} = I_{L,dc} = \frac{P_{in}}{V_{in}} = \frac{1500}{200} = 7.5A \quad (3.2)$$

where $V_{in} = 200V$ in the worst case.

The request is to have a converter switching frequency $f_{sw} = 20kHz$ and a maximum tolerable ripple percentage current of 5%, this way the ripple current is $\Delta i_L = 0.375A$.

Finally inductor sizing value is found according to the following boost converter equation [9]:

$$L = \frac{V_{in} \cdot d \cdot T_{sw}}{\Delta i_L} = 0.01778H \quad (3.3)$$

3.1.2 PLECS simulation

In order to verify the inductors sizing, a PLECS simulation is done to see if the values match with the sizing.

From the Figure 3.2, can be seen the equivalent circuit of the interleaved open loop boost converter topology in PLECS corresponding to the bottom drive of the system powered from the DC power supply.

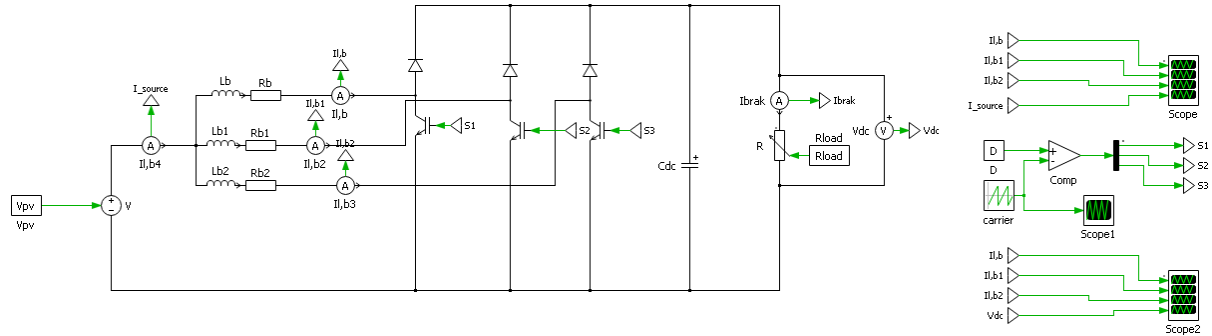


Figure 3.2: Interleaved boost converter topology in PLECS

It has to be underlined that the use of three legs interleaved boost converter topology leads to advantages for the converter efficiency and sizing, indeed the ripple has a three times higher frequency leading to smaller inductances and capacitors in the circuit. Moreover, in this case, the sizing of the inductor is done for having 3 times smaller ripple in one leg from the point of input power supply.

The strength of this topology is that the current of the DC source is divided into 3 paths, as can be seen in the picture 3.2, achieving that source sees much less current ripple at increased frequency.

Indeed, from the picture 3.3 can be done some considerations about the ripples and quantities values.

It can be seen that the ripple current on each inductor is nearby as calculated $\Delta i_L = 0.375A$ and the phase current $I_{in,worstcase} = 7.5A$ in each phase is as mentioned above. So from the DC source the total current is three times the current of each phase as shown in the Figure 3.4, not only, also the DC link voltage shape results better and with less ripple compared to a standard topology.

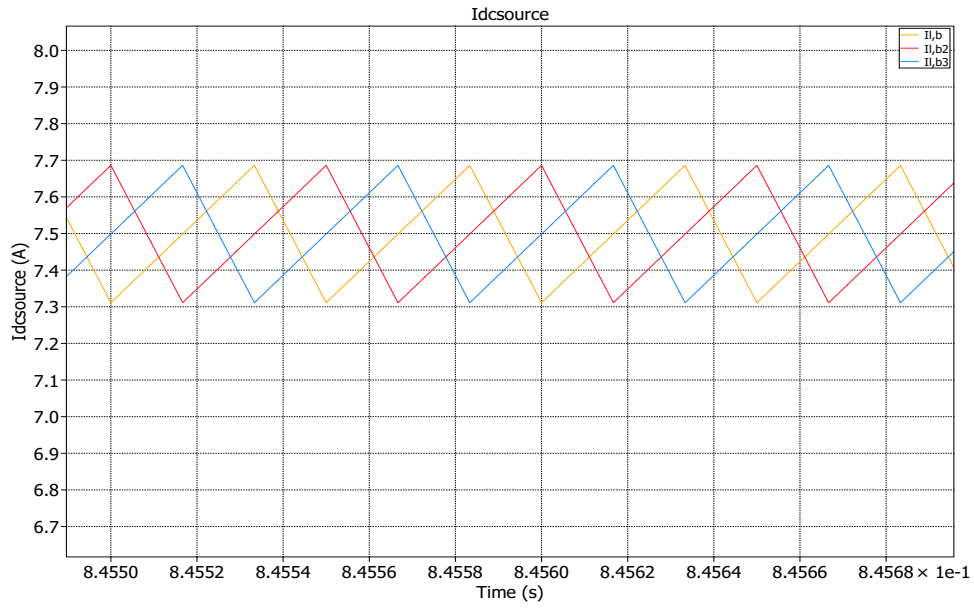


Figure 3.3: Interleaved boost converter current ripple on three phases

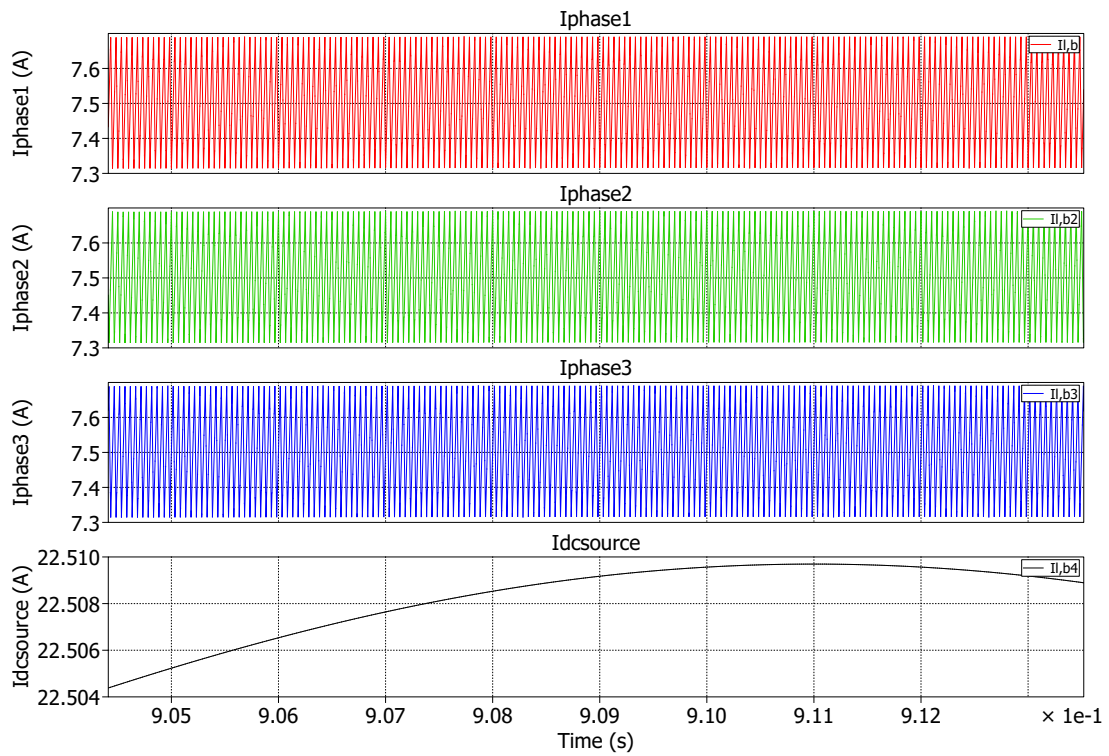


Figure 3.4: Interleaved boost converter currents

Therefore it can be deduced that the sizing of the inductors was done properly because the simulations results match the sizing values.

About that, 3 boost inductors of 18 mH present on the market were ordered from Rotima AG company because the simulation has verified the sizing in the worst case conditions.

3.1.3 Test and validation

The aforementioned boost inductors need to be tested and validated in order to understand the behaviour and main characteristics of the selected product. Indeed, the simulation is not enough because there is also the need of doing some real test on the hardware in order to be able to validate the components and matching the simulation and design results.

That's why, two tests were performed in the lab using two different equipment:

- inductance versus frequency (L-f) plot extrapolation using the vector network analyzer Bode 100 from Omicron Lab
- inductance versus current (L-I) plot extrapolation using the ed-k pulse inductance measurement device

Frequency response test of the boost inductors

Using the bode 100 device it was possible to test the boost inductors with a frequency range from 50 Hz to 1 MHz even if that device allows different tests such as sine generator, gain or phase meter, frequency response analyzer..., it was used to perform a test of Impedance analysis using the frequency sweep measurement mode.

The experiment is done firstly setting and configuring Bode 100 impedance calibration analyzer and then connecting it to the boost inductor, as illustrated in the Figure 3.5, where the boost inductor, the RLC meter, the bode 100 and the ed-k equipment are shown.

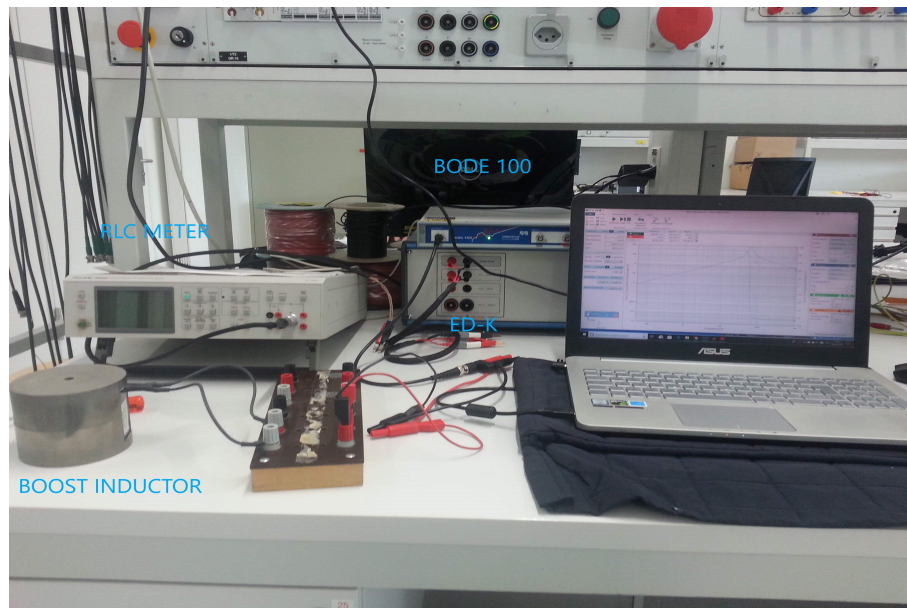


Figure 3.5: Test and validation setup of the boost inductor where are indicated the LRC meter, BODE 100 and ED-K devices

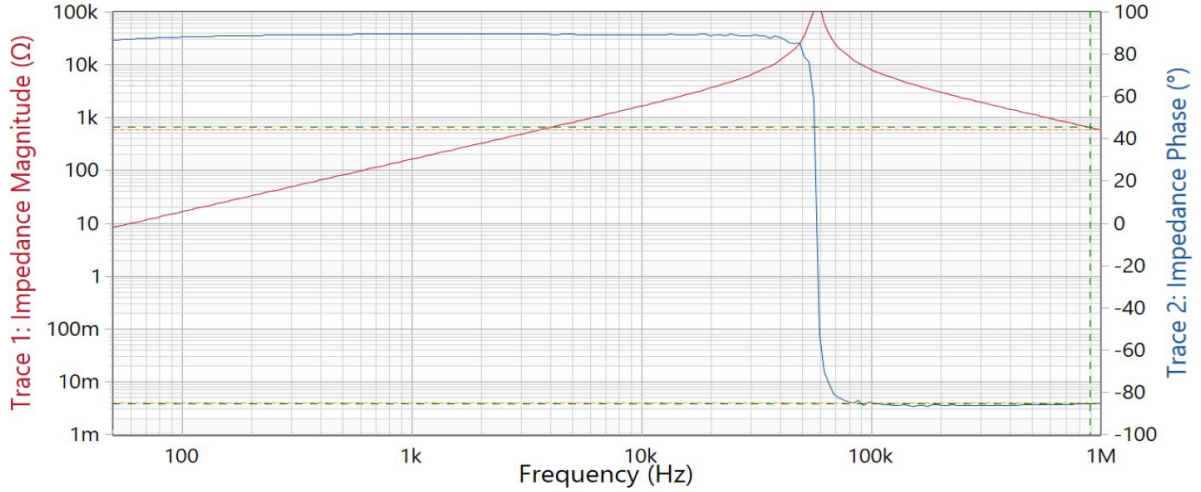


Figure 3.6: Impedance magnitude and phase versus frequency of the tested boost inductor

Carrying on the experiment is possible to extrapolate and manage on a personal computer some electrical quantities and plots. About that, from the Figure 3.6 is possible to see the frequency-impedance characteristic of the boost inductor, in particular it can be underlined the resonant frequency of the inductor, close to 70 kHz, that is the frequency where the parallel parasitic capacitance value of the inductor is resonant deriving a really high impedance value, the peak of impedance magnitude in the plot, behaving similarly to an open circuit.

The impedance of the inductor given by, $X_L = 2\pi f \cdot L$, rise up linearly with the frequency, but at certain frequency value a parallel parasitic capacitance enables a resonant phenomena and the impedance falls down with the increasing of the frequency behaving more like a capacitor rather than an inductor.

Moreover, in this type of application the inductor will not behave like a capacitor because the frequency working operation is not that high and the purpose of the boost inductor is to let pass DC current and filter the alternating component.

Furthermore, the inductance value at the switching frequency, $f_{sw} = 20kHz$, can be extrapolate from the plot taking the magnitude value cross with the red curve at the switching frequency.

So,

$$L = \frac{X_L}{2\pi f} = \frac{3800}{2\pi \cdot 20000} = 0.030H \quad (3.4)$$

this means that at the switching frequency the inductor value is higher than the one needed leading to a smaller ripple according to

$$\Delta i_L = \frac{V_{in} \cdot d \cdot T_{sw}}{L} \quad (3.5)$$

therefore, the maximum current ripple target is achieved during real system operation.

Saturation characteristic test of the boost inductors

Carrying on another test using the power choke tester DGP10 b series from ed-k it was possible to test the boost inductors and getting the saturation characteristics curve of inductors applying a large signal impulses method.

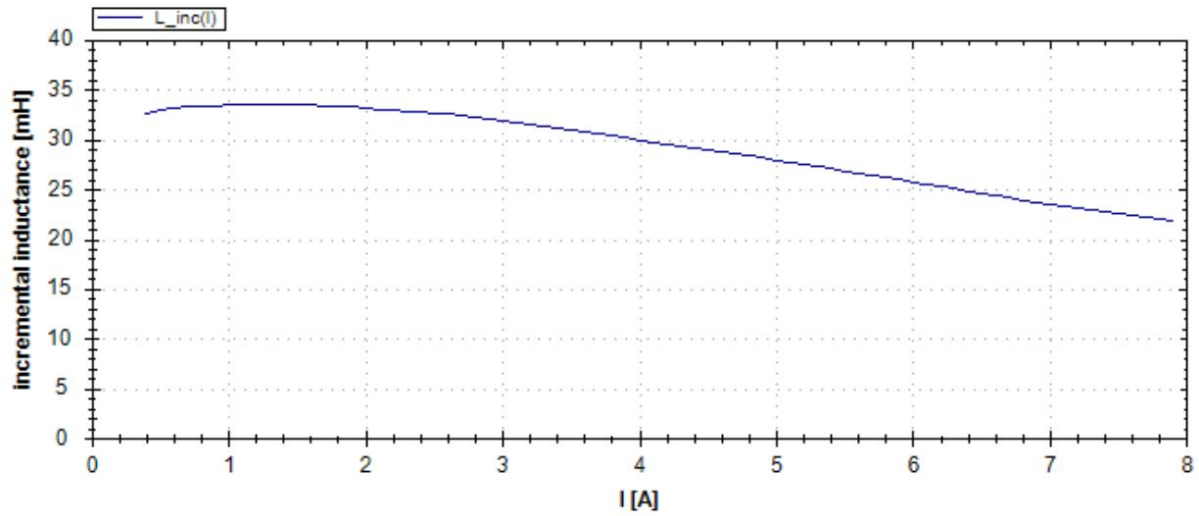


Figure 3.7: Saturation characteristic of the tested ferrite boost inductor

The test is done using the maximum current tolerable by the inductors from the datasheet, 8 A, for a really short time because the device delivers current pulses.

The test is performed realising a maximum current of 8 A, because in the worst case condition from the sizing process the phase current was 7.5 A, so we want to know the inductor characteristic below 8 A because the inductor saturation current zone in the worst working condition will never be reached.

It's possible to see from the characteristic, Figure 3.7, the typical shape of a ferrite inductor and that the real inductance is slightly higher, nearby 22 mH, than the one declared by the manufacturer 18 mH.

The possible motivation of this light difference can be due to different experiment conditions.

It can be deduced that this is not a problem because an higher inductance value leads to a smaller ripple, in reverse a smaller value would have been a problem as demonstrated in the previous section.

3.2 Braking resistor

In this section the step process is followed in order to find proper braking resistors available on the market and place the order for them.

3.2.1 Sizing of the braking resistor

As discussed in the Chapter 2, Hyundai converter has extra braking chopper legs that can be used.

This way the placement of two braking resistors can leads to two different functions on the PETS:

- it can operate as a chopper or Buck DC/DC converter with the possibility to connect an external resistor and changing the duty cycle of the IGBT in order to apply different voltages across the resistor and thus dissipate different power levels, behaving like a variable load
- it can ensure the voltage limiting function because this circuit with the resistor can be used to prevent DC link voltage going too high for various reasons when the motor load is not connected or like a braking energy dissipating device when the motor is connected to the drive

By the way , the aforementioned braking chopper resistor is responsible for the dissipation of the power generated by the load and should be able to handle a power of 1.5 kW continuously, this way the braking resistor is found according to the following equation:

$$R_{\text{braking}} = \frac{V_{\text{dc,bus}}^2}{P} = \frac{600^2}{1500} = 240\Omega \quad (3.6)$$

Note that this corresponds to the worst case when the braking switch is always close. Besides, it was decide to consider a load power of 1.5 kW because it's precautionary enough for considering the braking motor load behaviour in terms of stopping energy generated during the braking [10].

Furthermore, this will lead to a good compromise between heating generation, cooling needs and space allocation.

3.2.2 PLECS simulations

For verify the braking resistor sizing two PLECS simulations are done considering two converter topologies:

- DC/DC buck with braking resistor as variable load

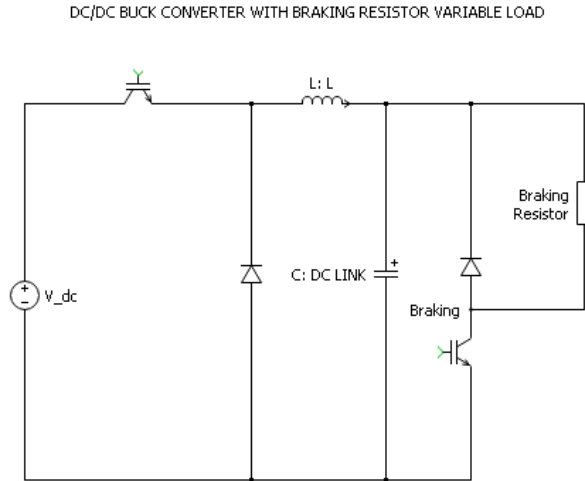


Figure 3.8: DC/DC buck with braking resistor as variable load

- rectifier+inverter with braking resistor as DC link limiting voltage function

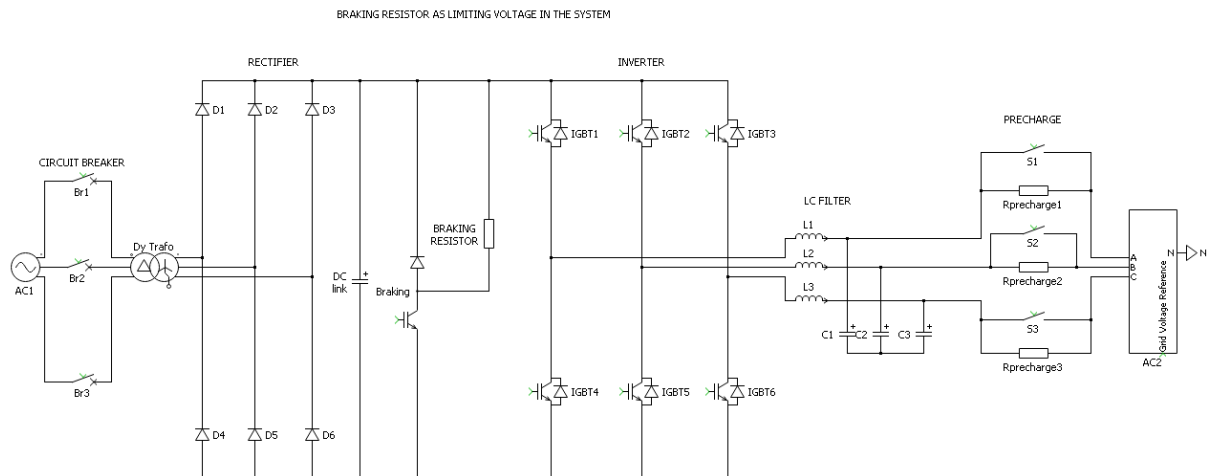


Figure 3.9: rectifier+inverter with braking resistor as DC link limiting voltage function

DC/DC buck with variable load braking resistor function

The setup can operate as a buck converter topology where the external resistor is responsible for dissipating the power into heat like a variable load. The modularity of the setup allows one quadrant, two quadrant and four quadrant DC/DC operation. In particular, in the Figure 3.10 is shown the PLECS simulation of a buck converter topology operation with the braking resistor as variable load.

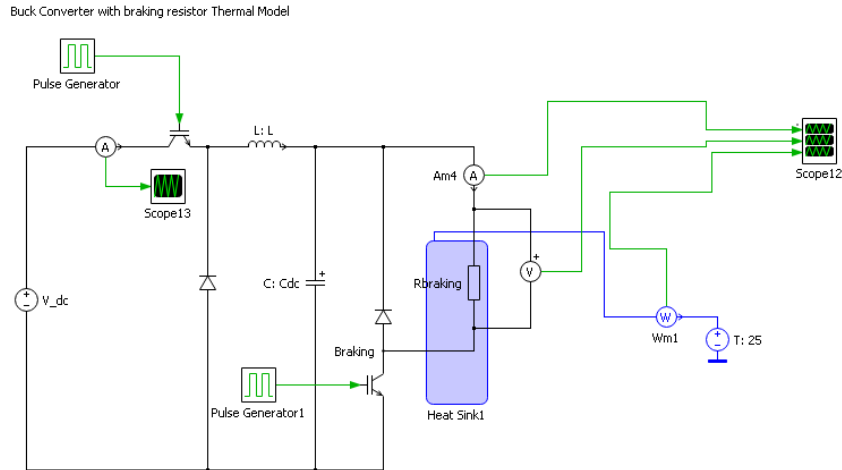


Figure 3.10: Buck converter topology in PLECS with braking resistor as variable load

Indeed, the word variable comes from the fact that changing the duty cycle of the IGBT chopper low side switch is possible to have different load values so different thermal stresses on the braking resistor at different duty cycle percentages.

This way, three simulations are run using respectively three different values of duty cycles

- $d=25\%$
- $d=75\%$
- $d=100\%$

and the patterns of braking resistor current, voltage and power dissipated are recorded.

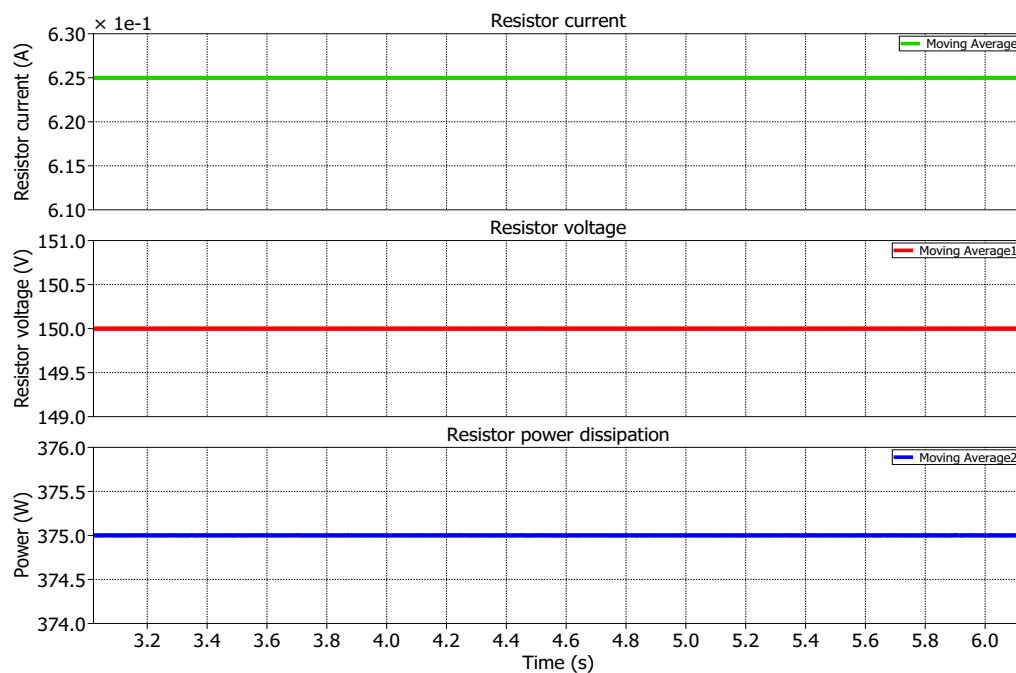


Figure 3.11: Resistor current, voltage and power for a duty cycle $d=25\%$

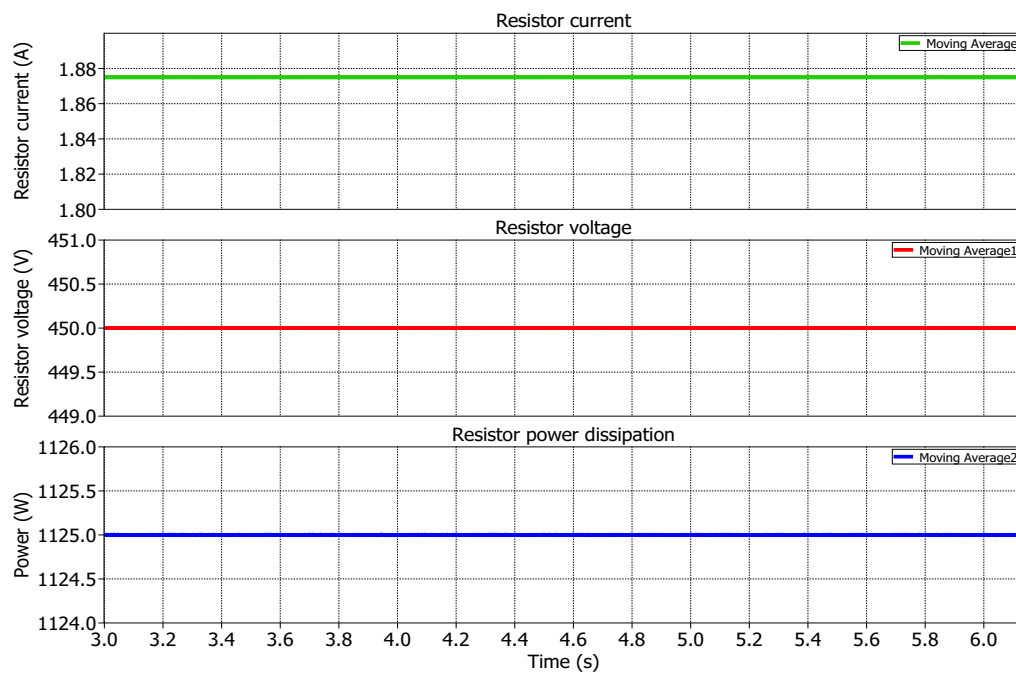


Figure 3.12: Resistor current, voltage and power for a duty cycle $d=75\%$

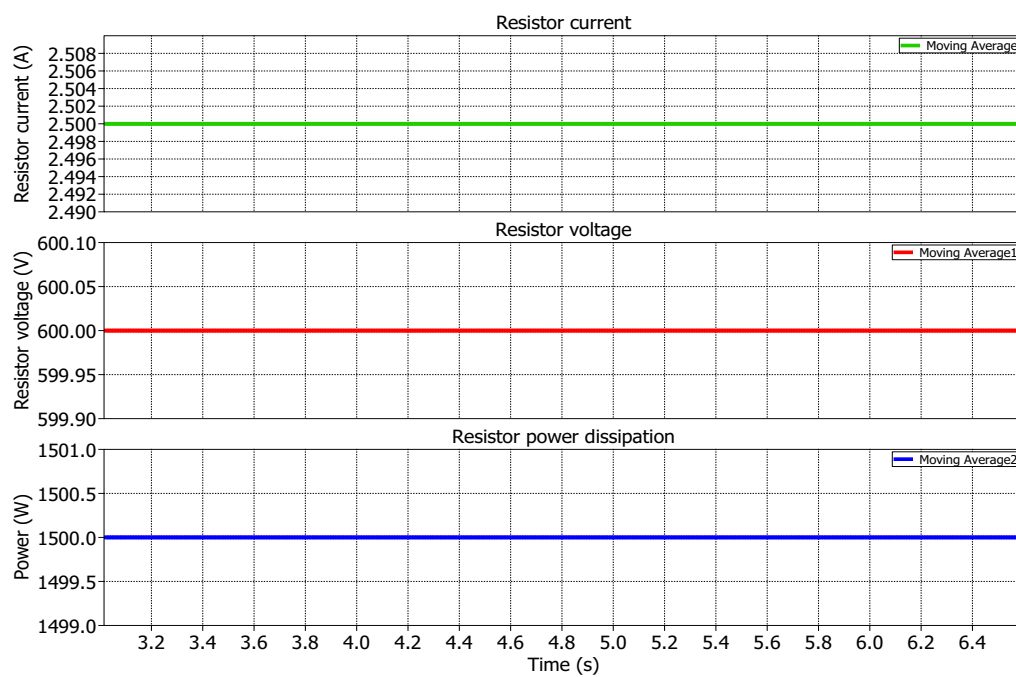


Figure 3.13: Resistor current, voltage and power for a duty cycle $d=100\%$

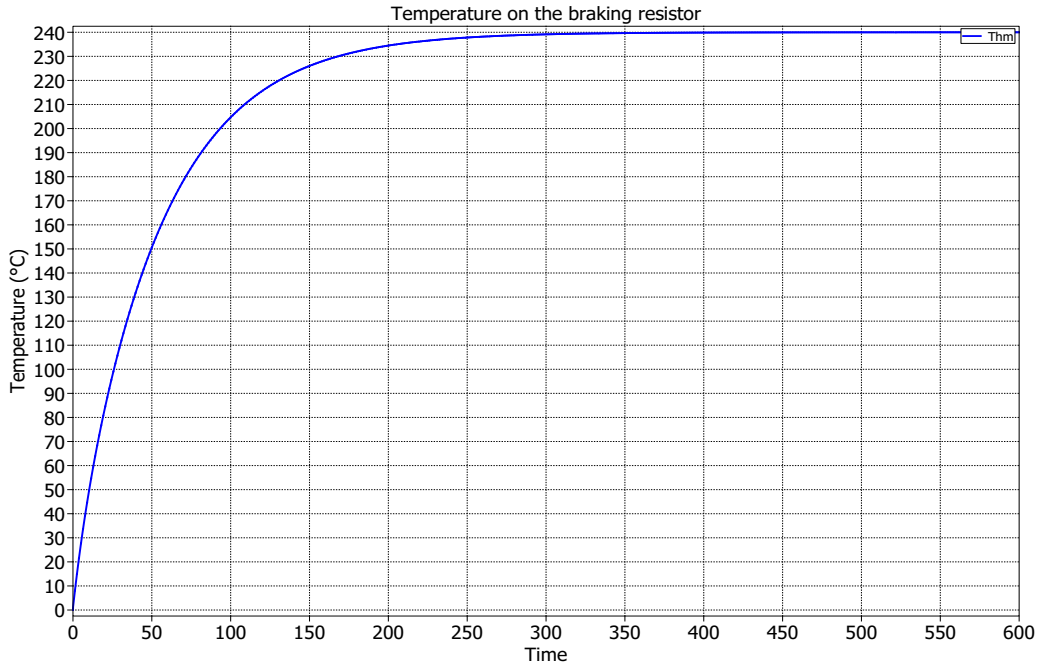


Figure 3.14: Simulation of the temperature reached on the resistor after 10 minutes in the worst case scenario of $d=100\%$

From the Figures 3.11, 3.12 and 3.13 is possible to see that increasing the duty cycle, the current on the resistor and the voltage across it increase leading to an increase of power to be dissipated.

Besides, in the worst case scenario where the duty cycle of the braking resistor leg IGBT is always close, $d = 100\%$, on the braking resistor there is the DC link voltage of 600 V so the power across the resistor is like the one designed in the previous sizing section, $P = 1.5kW$.

This means that the sizing was done properly and that the worst case is keep in consideration during the full process.

For what concerns the resistor temperature reached during the operation in the worst case condition, $d=100\%$, the pattern simulation is shown in the Figure 3.14.

Limiting voltage function of the braking resistor

The setup can operate with the braking resistor as a key element because it can ensure the limiting voltage function avoiding the rising of several problems.

In particular, in the Figure 3.15 is shown the PLECS simulation of the system rectifier+inverter and related elements where the DC link voltage is keep under certain value thanks to an hysteris comparator control on the braking resistor IGBT.

Indeed, controlling the braking resistor IGBT it can be ensured that the voltage in the DC link does not exceed remarkable values.

Furthermore, it was decided to use a simple hysteris control because is commonly used on those types of applications since uses the feedback for switching brutally between two positions.

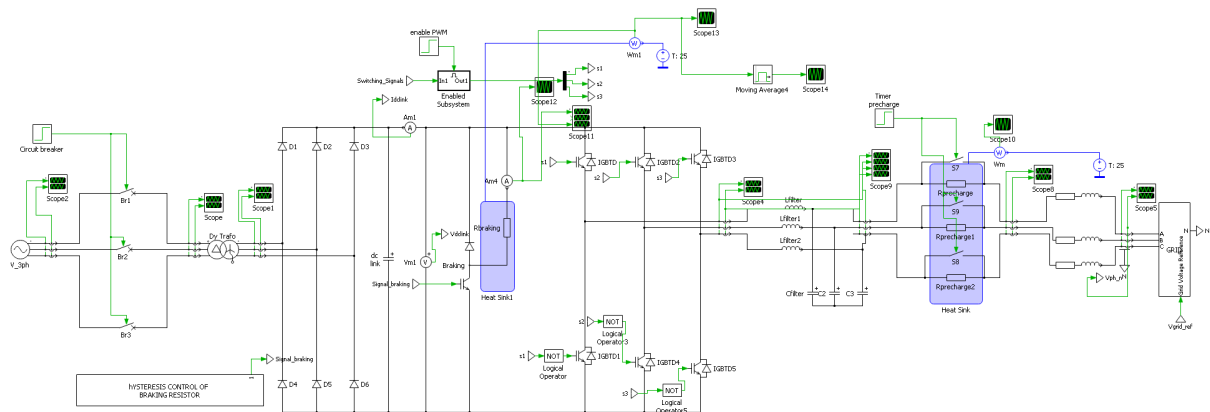


Figure 3.15: PLECS simulation of the PETS braking resistor limiting voltage function

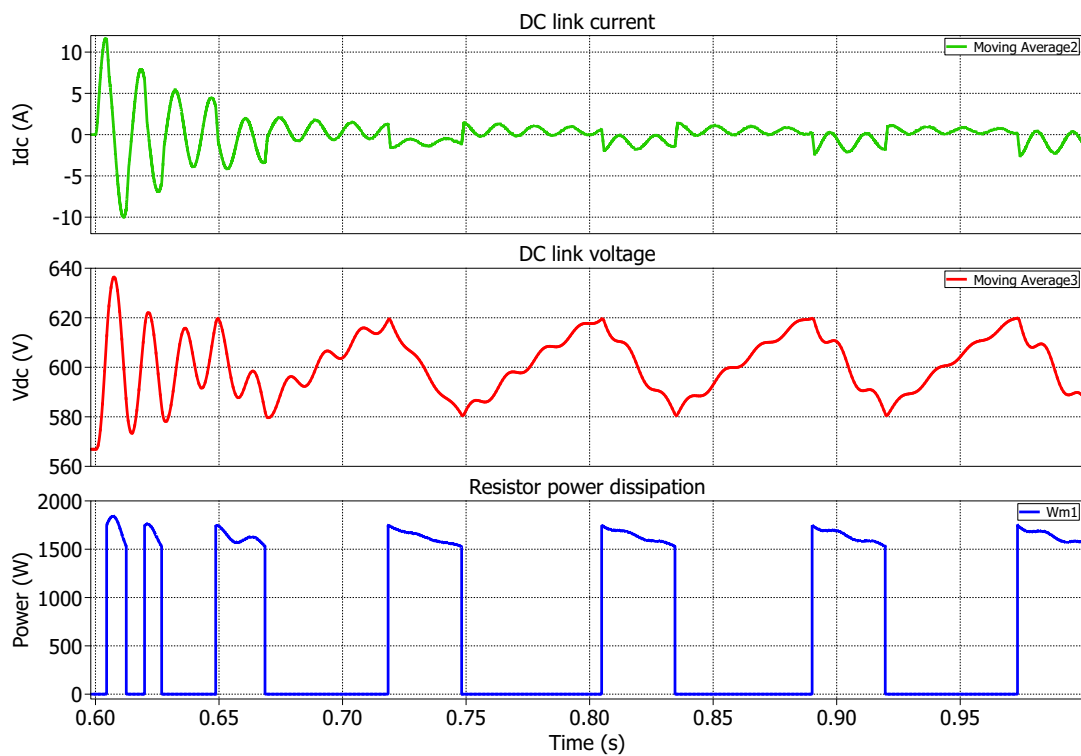


Figure 3.16: DC link current, DC link voltage and power dissipated by the resistor with an hysteresis controller

From the picture 3.16 is possible to see that the hysteresis controller intervenes because it is visible the opening and closing of the IGBT braking resistor switch, indeed the shape is that of a continuous rising and falling of the red and green curves. In particular, setting a DC link lower voltage and a DC link higher voltage value on the controller is possible to keep the DC link voltage inside those two limits. When the DC link voltage decreases from the upper limit to the bottom limit the braking resistor is dissipating the power, peak values of the blue curve, behaving like a braking resistor avoiding DC link value exceeding safety values for the DC link good operation.

This way, the DC link voltage doesn't rise upon or fall remarkably the rated values and the braking resistor does its job dissipating power accordingly to the hysteresis control. Therefore since the sizing and simulation results are comparable the system will be composed by two identical $240\ \Omega$ Widap wire wound tubular braking resistors each one for the two power converter drives.

3.2.3 Test and validation

For validating the sizing and simulation of the braking resistor a test was performed. Indeed, it was stressed with a DC power supply for see if it was able to handle for 10 minutes continuously the datasheet rated power without problems ($V = 550V, I = 2.5A$). Using a thermal camera from FLIR the values of the temperature and hotspots are detected and recorded.

About that, in the Figure 3.17 is shown the infrared image of the resistor stressed with the rated values while in Figure 3.18 is shown the infrared image of the resistor stressed with a 5% overload compared to the rated values ($V = 595V, I = 2.63A$).

Comparing the test result rated values of ($V = 550V, I = 2.5A$) with the ones of the simulation during the worst case condition of $d=100\%$, ($V = 600V, I = 2.5A$) it can be noticed that the final temperature reached after 10 minutes in the test is really close to the one simulated, Figure 3.14.

Indeed, in the simulation the reached temperature is around $240\ ^\circ C$ while for the test the final temperature is $228\ ^\circ C$. So following the test can be deduced that the resistor is properly chosen and is able to guarantee the continuously power dissipation for a discrete amount of time considering that the generation behaviour of the load is a relatively short time phenomena.

Therefore, the important thing for the installation and mounting of the braking resistor is that is placed in the top part of the PETS for a good heating cooling avoiding to damage or heat up other delicate components.

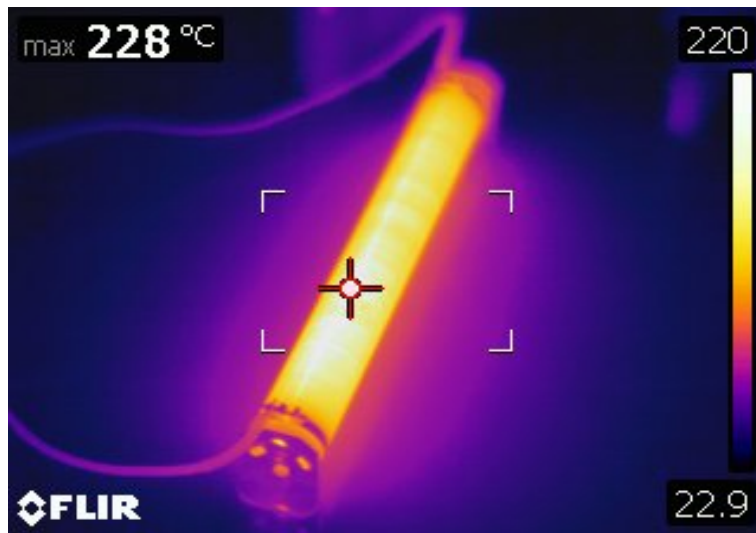


Figure 3.17: Thermal behavior of the braking resistor according to rated values

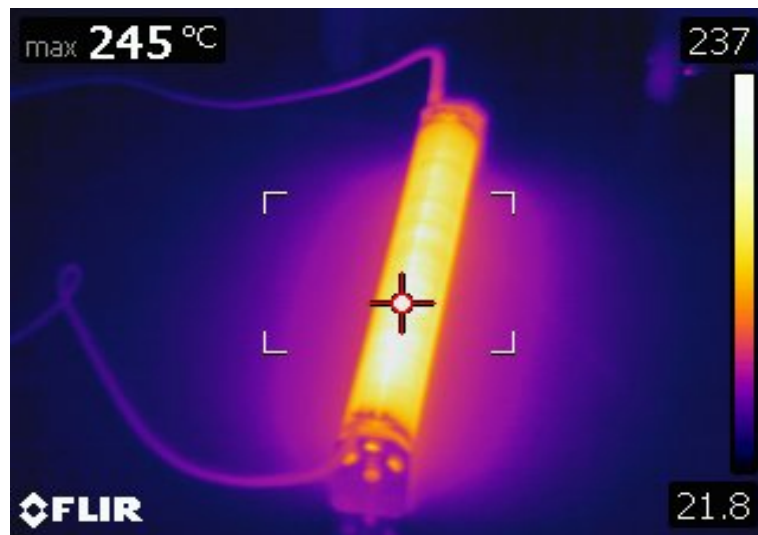


Figure 3.18: Thermal behavior of the braking resistor with a 5% overload of the rated values

3.3 LC filter

In this section the step process is followed in order to find proper LC filter available on the market and place the order for it.

3.3.1 Sizing of the LC filter

The purpose of the three phase LC passive filter is to connect the converter to the AC power supply filtering the high harmonics spectrum generated by the PWM and to have an inductive behaviour controlling the active and reactive power exchanged with the Regatron grid emulator load.

In order to size the LC filter it's important to select a cut off frequency f_o above which the signals are attenuated.

About that, for an LC filter configuration the cut off frequency is given by [11]:

$$f_o = \frac{1}{2 \cdot \pi \sqrt{L \cdot C}} \quad (3.7)$$

So we decide to select a resonant frequency of 850 Hz because it's a good compromise between the grid frequency of 50 Hz and the IGBT switching frequency of 20 kHz.

Indeed, the resonant frequency has to be included between ten times the grid frequency and $\frac{f_{sw}}{2}$, furthermore the L and C values should be selected according to:

- capacitors value should be selected avoiding to decrease too much the power factor since the capacitor provide negative reactive power and also according to maximum voltage ripple it can withstand
- inductor value should be selected avoiding significant voltage drops and also according to maximum current ripple it can withstand

This way, considering a cut off frequency of 850 Hz a couple of possible values of L and C with an easy and effective availability on the market are selected according to the aforementioned equation.

A possible combination of those values corresponding to market products is to have an LC filter with a capacity around

$$C = 7\mu F \quad (3.8)$$

and an inductance of around

$$L = 5mH \quad (3.9)$$

About that, an LC sine wave filter is selected from Schaffner company with a capacity of

$$C = 6.8 \cdot 10^{-6} F \quad (3.10)$$

and an inductance of

$$L = 5.2 \cdot 10^{-3} H \quad (3.11)$$

that are really close to supposed values and can satisfy the cut off frequency request.

3.3.2 Simulations

Using the software Matlab and analyzing the frequency response of an LC low pass filter some considerations are done.

Knowing the LC low pass filter configuration, it can be derived that the filter transfer function is:

$$G(s) = \frac{1}{s^2 LC + 1} \quad (3.12)$$

Setting the filter values of

$$C = 6.8 \cdot 10^{-6} F \quad (3.13)$$

$$L = 5.2 \cdot 10^{-3} H \quad (3.14)$$

and considering the resistance value negligible, the frequency response of the filter in dB is shown in the Figure 3.19.

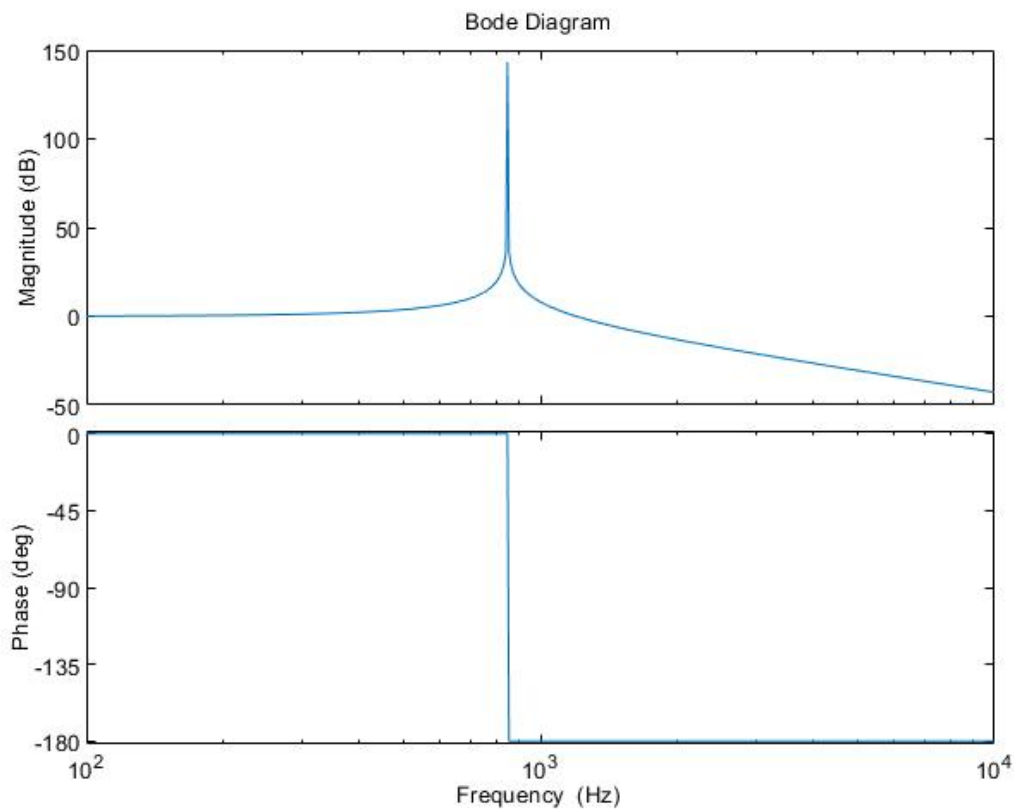


Figure 3.19: Filter frequency response from Matlab

It can be noticed that the resonance frequency from the Matlab simulation is close to the one calculated, 850 Hz, visible in the system as magnitude peak. Furthermore, the peak value is really high because it isn't consider the parasitic resistance of the filter in the simulation since it isn't provided by the manufacturer datasheet. The resulting damping ratio calculated in Matlab is $\zeta = 0.691$, where it was supposed a small resistance value, R_L , in order to avoid getting damping ratio zero and system completely underdamped.

This way, the damping ratio is

$$\zeta = \frac{1}{2Q} \quad (3.15)$$

and Q is the quality factor given by

$$Q = R_L \sqrt{\frac{C}{L}} \quad (3.16)$$

this means that the filter frequency response is quite underdamped being $\zeta = 0.691$.

Furthermore, using the software PLECS and running the simulation of the same converter topology presented in the previous chapter but focusing on the LC filter this time.

Indeed, the circuit topology taken into account for the PLECS simulation is shown in the Figure 3.20, where for the following simulation plots the inverter duty cycle is set $d = 0.5$.

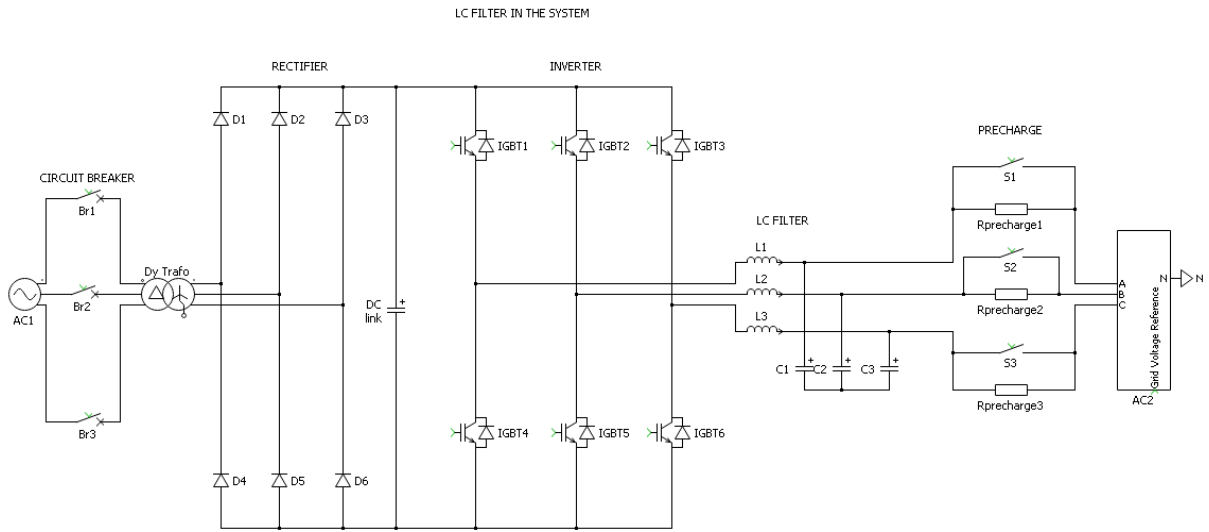


Figure 3.20: Converter topology with the LC filter in the system

It can be underlined that the shape of the voltage with and without the filter is quite different. Indeed, from the Figure 3.22 is possible to see the output voltage of the system without the presence of the filter that has some harmonics and it's not symmetrical. While, in the Figure 3.21 is possible to see the effects of the filter resulting in less harmonic and perfect sinusoidal shape of the voltage.

For having an idea of the harmonic spectrum, in the Figures 3.24 and 3.23, is possible to see the different harmonic Fourier spectrum of the two cases.

About that, with the filter the voltage output harmonics are remarkably reduced, in particular the high harmonics order components are close to zero and also the second, third and fourth component are drastically reduced.

This means that the LC filter is doing properly its job reaching better voltage shapes according to grid codes requirements.

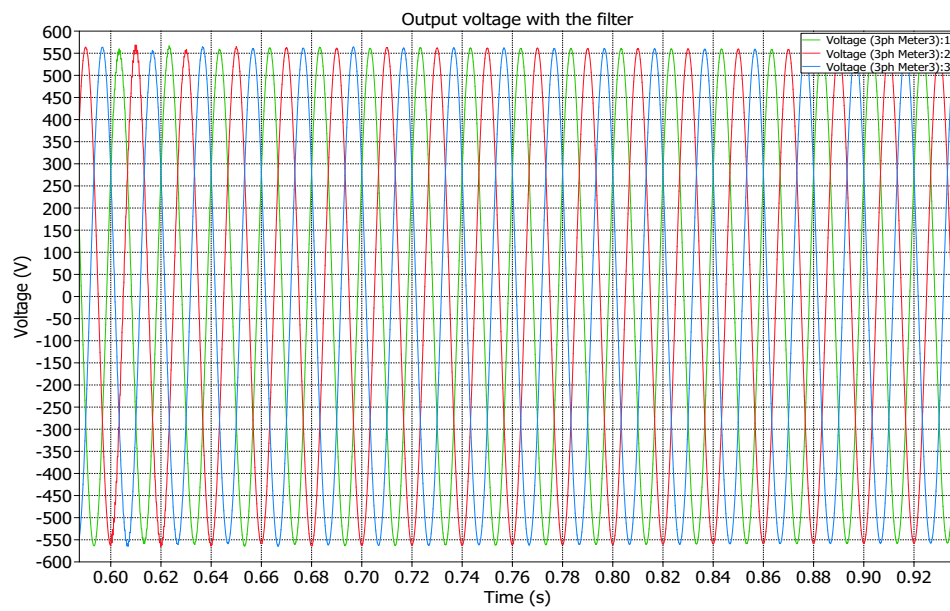


Figure 3.21: Output voltage with the LC filter

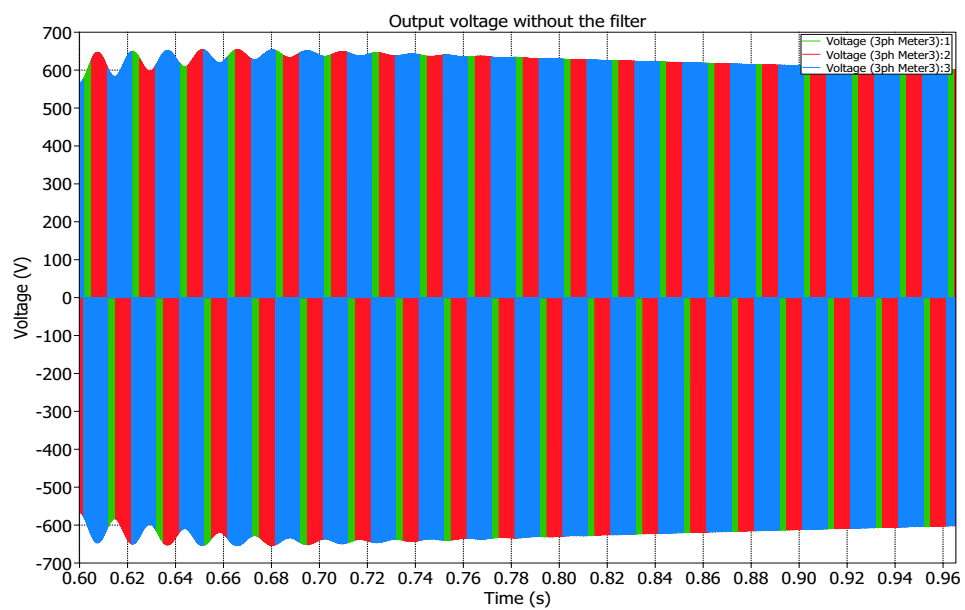


Figure 3.22: Output voltage without the LC filter

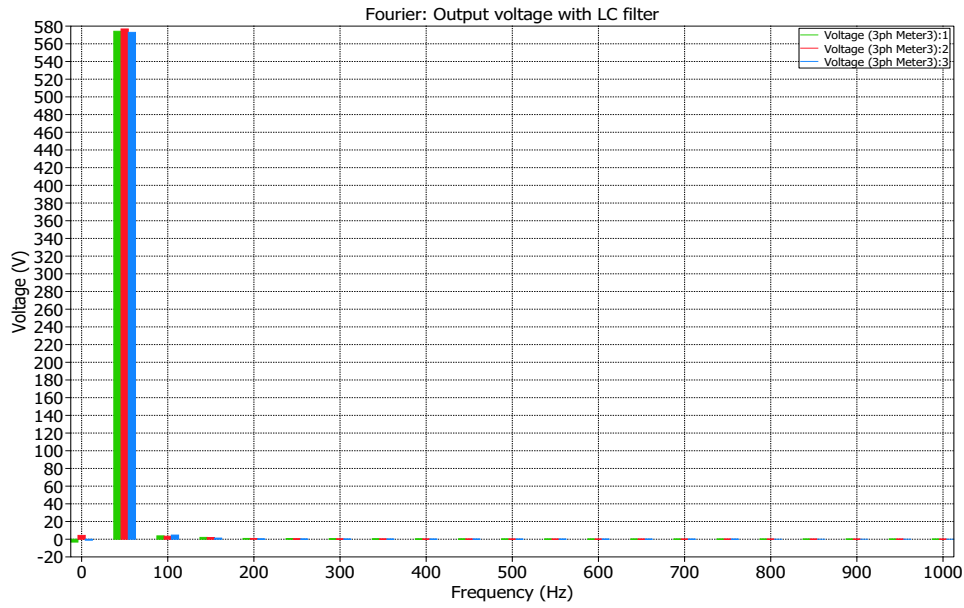


Figure 3.23: Fourier analyses of the voltage with the LC filter

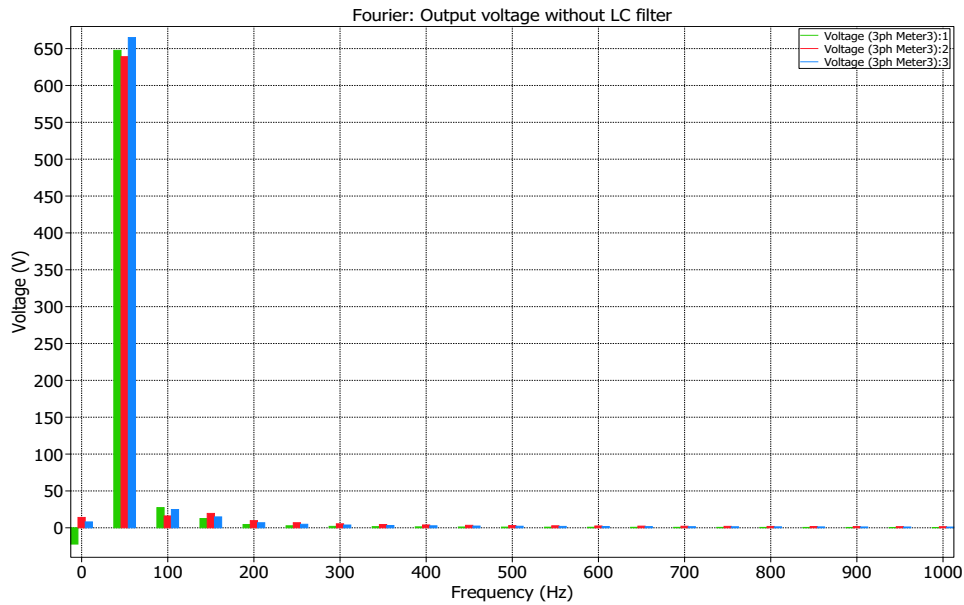


Figure 3.24: Fourier analyses of the voltage without the LC filter

3.3.3 Test and validation

Using the bode 100 device, Figure 3.25, it was possible to test also the LC filter with a frequency range from 10 Hz to 100 kHz performing the gain transfer function measurement mode.

This way it was obtained the LC filter transfer function plot extrapolation, as shown in the Figure 3.26.

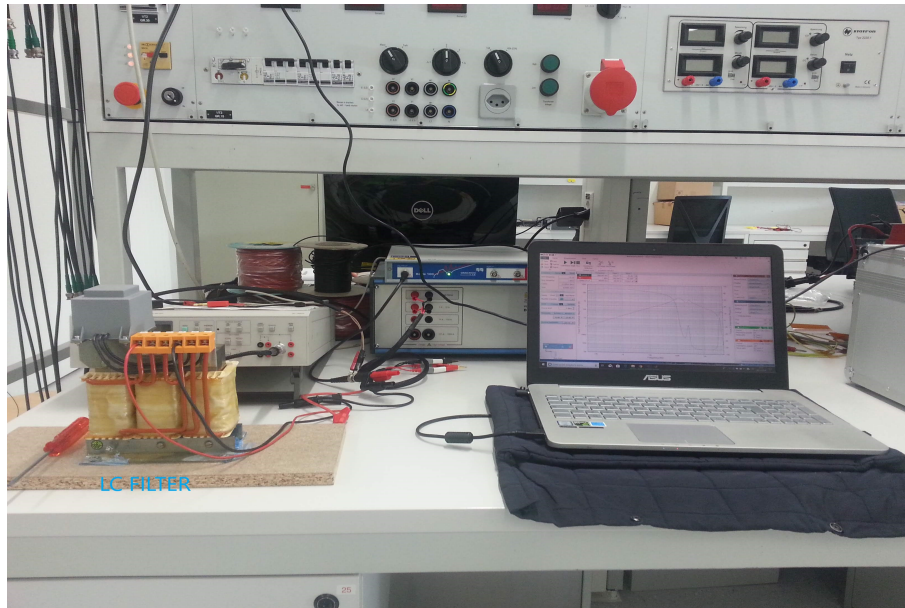


Figure 3.25: Test and validation setup of the LC filter

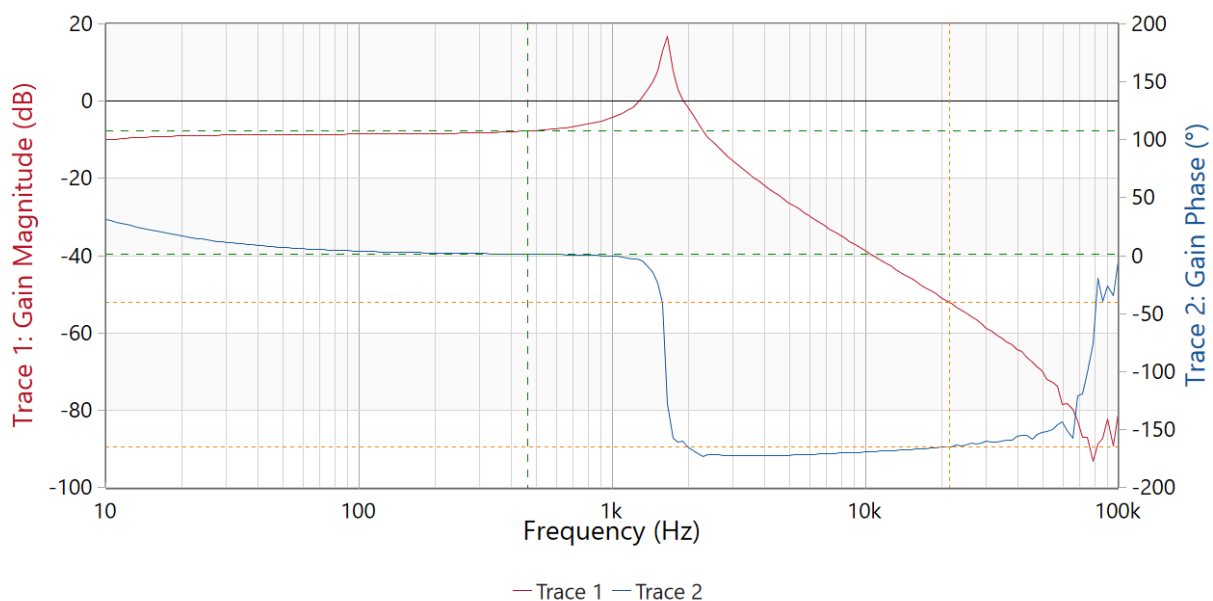


Figure 3.26: Transfer function measured of the tested LC filter

From the test it can be underlined that the resonant frequency selected in the design part, 850 Hz, is close to the cutoff frequency of the real filter wired by the manufacturer. Moreover, the real resonant frequency, around 1050 Hz, is slightly higher than the theoretical one, 850 Hz. This way the RLC meter is used for measuring the real LC filter parameters obtaining that the real inductance value of the phases is different from the one declared by the manufacturer.

Indeed, the measured inductance is 3.9 mH while the declared inductance is 5.2 mH, this leads to an increase of the resonant frequency as shown in the measurement test.

For what concerns the capacitor value there isn't the possibility of measuring the value since there is not access to the neutral point, so the only way of measuring it would be

destroying and opening the LC filter.

Not only, because the difference with the simulation is also due to the fact that in the measurement also the parasitic resistance of the filter intervenes resulting in a reduce peak and a different shape.

It has to be underlined that this doesn't imply remarkable differences in term of harmonics and power quality for the setup routine operations.

The possibility to use an LCL filter would have lead to a more compact and light filter, moreover the choice of an LC filter is effective due to its simplicity and working behavior.

3.4 Precharge circuit

In this section the step process is followed in order to find proper resistors, timers and contactors composing the precharge circuit available on the market and place the order for them.

3.4.1 Sizing of the precharge circuit

The role of the precharging circuit is to avoid the inrush current during the turn on of the system, on the diodes avoiding to damage them and on the capacitors of the DC link, indeed, the capacitors are able to tolerate a certain amount of inrush current that can not be exceeded.

The precharge circuit is needed due to the converter topology where there is a rectifier using the antiparallel diodes of the VSI due to a power flow coming from AC2 because only for this source there is the need of putting a precharge circuit.

Indeed, if the power comes from the AC1 source there is no need of limiting the inrush current due to the presence of the isolating transformer and the variac connected to the diode rectifier that allows changing manually with a knob the voltage giving the possibility to avoid a step full power variation of the voltage and also because in the Hyundai inverter drive is present an inrush limiting circuitry.

Moreover, in case the power flow comes from the AC2 Regatron power supply there is the need of limiting the inrush current because the power supply can furnish a 400 V phase to phase voltage supply when the system is turned on unleashing an inrush current to the DC link.

This way, in the Figure 3.27 is shown the precharge circuit place inside the system circuit topology.

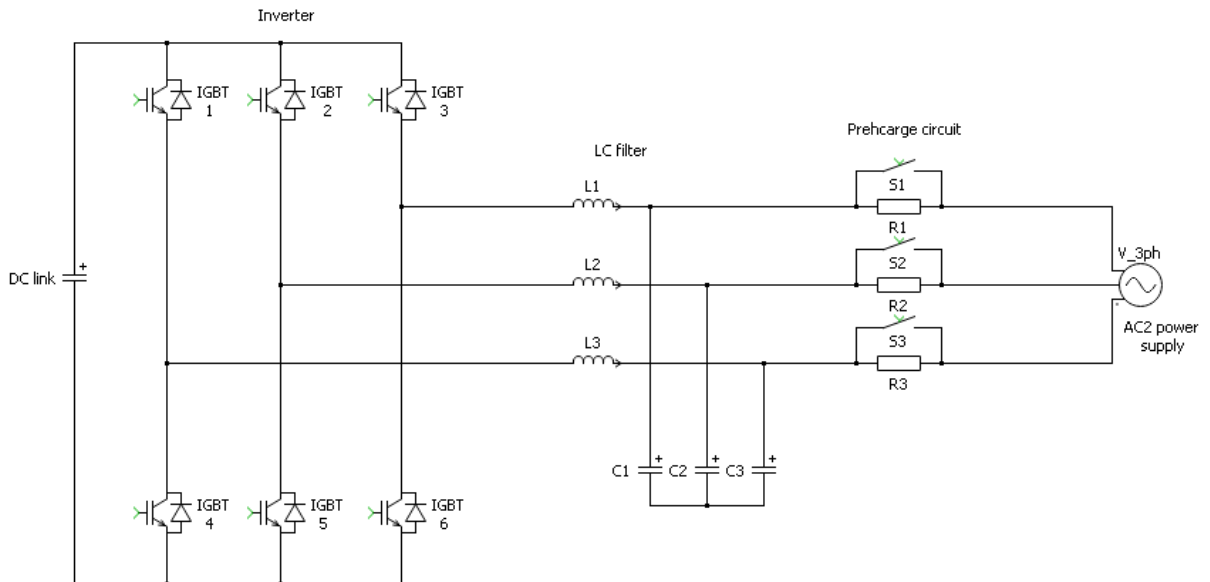


Figure 3.27: Precharge circuit allocation in the system

Besides, a precharge circuit needs to be sized for order and place all relative components [12].

For bounding the inrush currents in the DC link is important to add a resistance for

avoid step voltage variation on the capacitor, in this section will be done the sizing of the precharge resistors as follows:

Knowing the DC link inverter capacity that is $C = 700\mu F$ from the datasheet.

It is supposed a precharge time of 500 ms, so

$$R = \frac{T_{\text{precharging}}}{5 \cdot C} = 142.9\Omega \quad (3.17)$$

so, from the equation can be deduced that we need three 143 Ω resistors for each phase to put in the real system.

This way from the market are selected 3x150 Ω Alcom resistors.

Knowing the maximum grid voltage $V_{\text{max,grid,ph}} = 230\sqrt{2}$ and the resistance R we can calculate the maximum current on the capacitor C:

$$I_{\text{max}} = \frac{V_{\text{max,grid,ph}}}{R} = 2.3A \quad (3.18)$$

that is less of the maximum inrush current tolerable by the capacitor.

For having an idea of the worst case working condition the peak power losses $P_{\text{loss,max}}$ experienced by the resistors can be calculated as follows:

$$P_{\text{loss,max}} = \frac{V_{\text{max,grid,ph}}^2}{R} = 740W \quad (3.19)$$

It has to be underlined that this value is remarkable but it is for a very short time, 500 ms, so the amount of energy losses is negligible.

3.4.2 PLECS simulations

In order to verify the precharge circuit sizing, a PLECS simulation is done for checking if the values match with the sizing.

From the model shown in Figure 3.28 is possible to see the circuit topology in PLECS and with that two simulations are performed:

- Simulation of the precharge circuit
- Simulation of the precharge circuit in the back to back topology

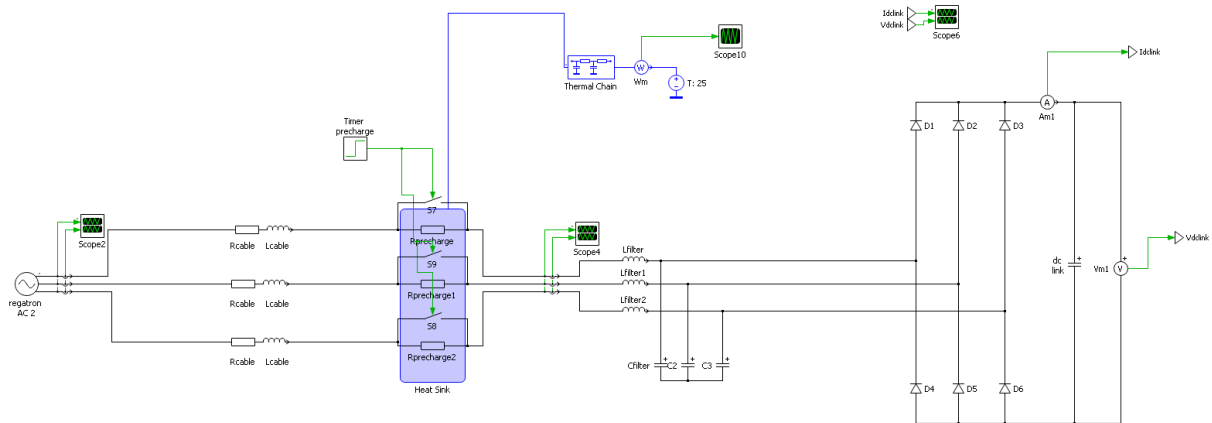


Figure 3.28: Precharge circuit composed by three 150 Ω resistors simulation in rectifier converter topology powered from AC 2

Simulation of the precharge circuit

The simulation was run with the real values of the setup, so the capacitor is $C = 700\mu F$ and the voltage from the source is 230 V phase. Running the simulation, the focus will be mainly on the DC link because it's the delicate element that the precharge needs to protect.

Therefore, the benefits of the precharging circuit can be seen on the DC link current and voltage patterns as shown in the Figure 3.29, the DC link voltage rises slowly allowing a correct charging of the capacitor and the inrush current is limited because when the full power goes to the converter without the presence of the precharge resistors at 0.5 s, the capacitor is already charged.

It has to be underlined that the peak current visible in the simulation at 0.5 s is for a really short period of time.

Furthermore, also the power and related energy that the precharge resistors have to carry on are analyzed in the simulation and plotted in the Figure 3.30.

The peak power shown in the aforementioned Figure is remarkable but since the amount of time is really short, just 0.5 s, the total energy dissipated is low and there are not problems of thermal nature imputable to the precharge system.

Also, the current flowing through every single resistor, Figure 3.32, is remarkable just for a really short amount of time, this implies that the thermal heating deriving from that on the resistors is not relevant as stated before.

For what concerns the filter sized in the previous section, in the Figure 3.31 is possible to see the resulting better voltage and current shape after the filter connected to the precharge system.

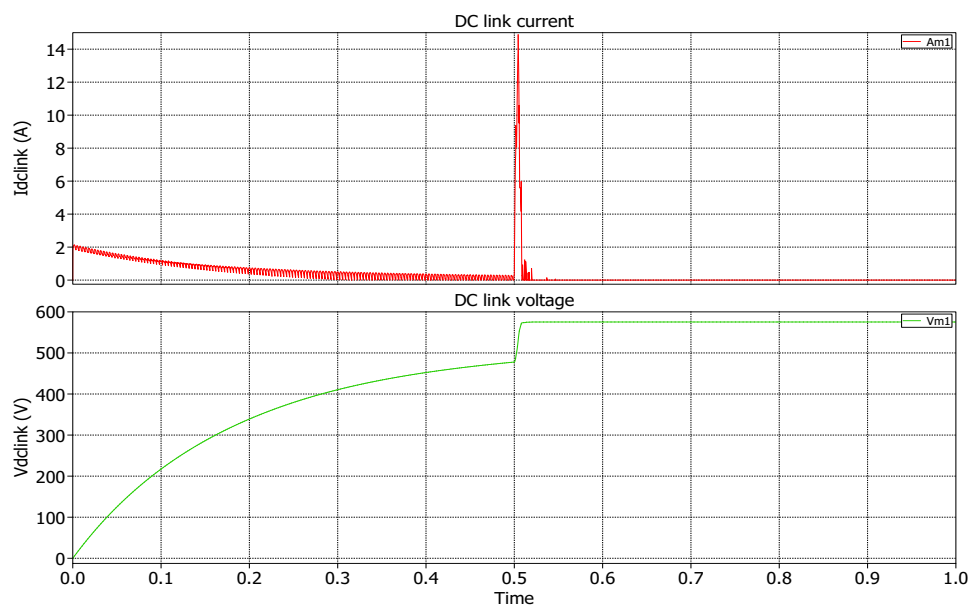


Figure 3.29: Simulation plots of DC link current and voltage with the precharge circuit active until 0.5 s

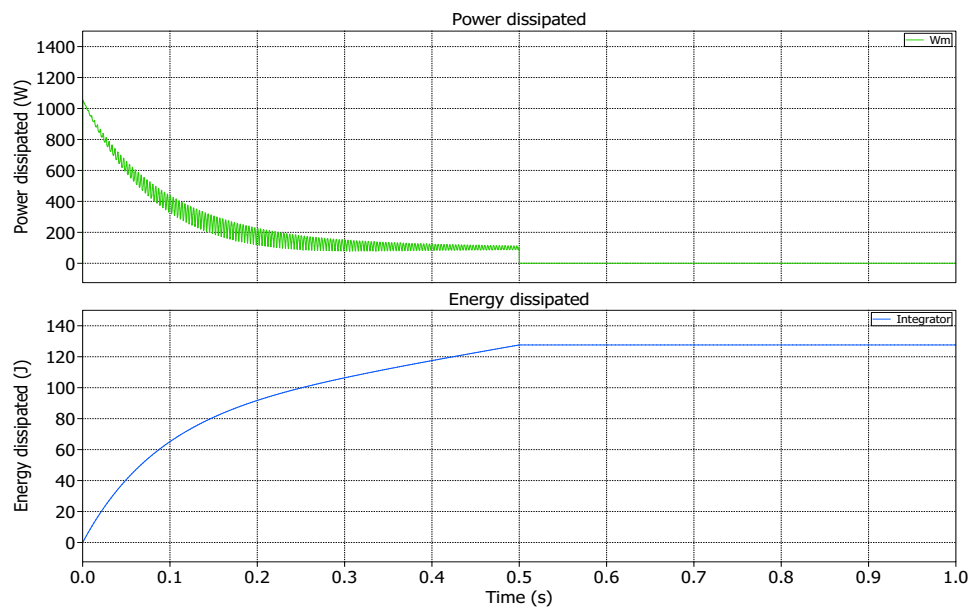


Figure 3.30: Simulation plots of energy and power dissipated through the precharge resistors

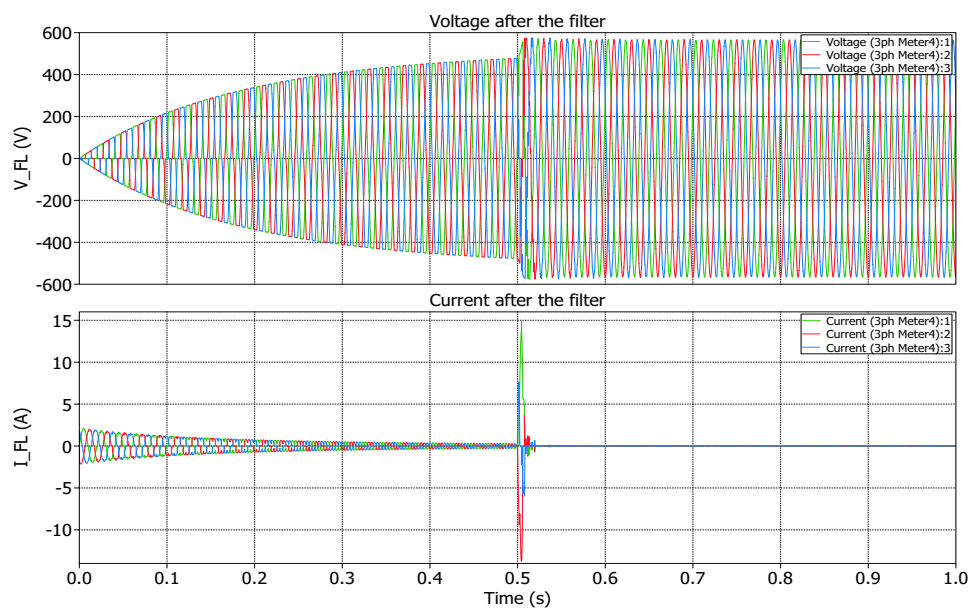


Figure 3.31: Simulation plots of current and voltage after the filter in the precharge circuit

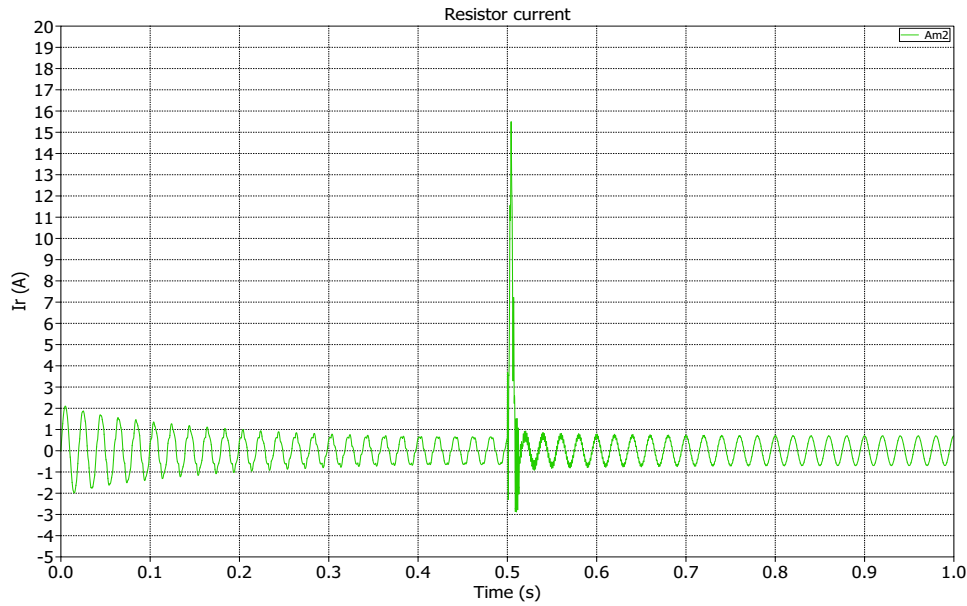


Figure 3.32: Simulation plots of the current flowing through the precharge resistor

Simulation of the precharge circuit in the back to back configuration

Furthermore, the precharge circuit is also responsible for the protection of both the drives in the case of the DC link connection in parallel of the two drives, giving the possibility of back to back converter operation. This way the DC link total capacity double, $C = 1400\mu F$, because the two drives are in parallel.

The simulation is repeated giving the focus and plotting the same electrical quantities as before.

Indeed, in the Figure 3.33 is shown the DC link current and voltage, in the Figure 3.34 the energy and power on the precharge, in the Figure 3.35 the voltage and current after the filter and in the Figure 3.36 the current on every resistor.

Therefore, this time the DC link current and voltage patterns are different because with a double capacitor value the DC link voltage rise with a bigger slope and the inrush current peak is higher compared to the previous case.

Also the power handled by the resistors is increased, nearby 200 J, but it has to be underlined that it's still negligible so there are not thermal problems on the precharge even in the back to back topology.

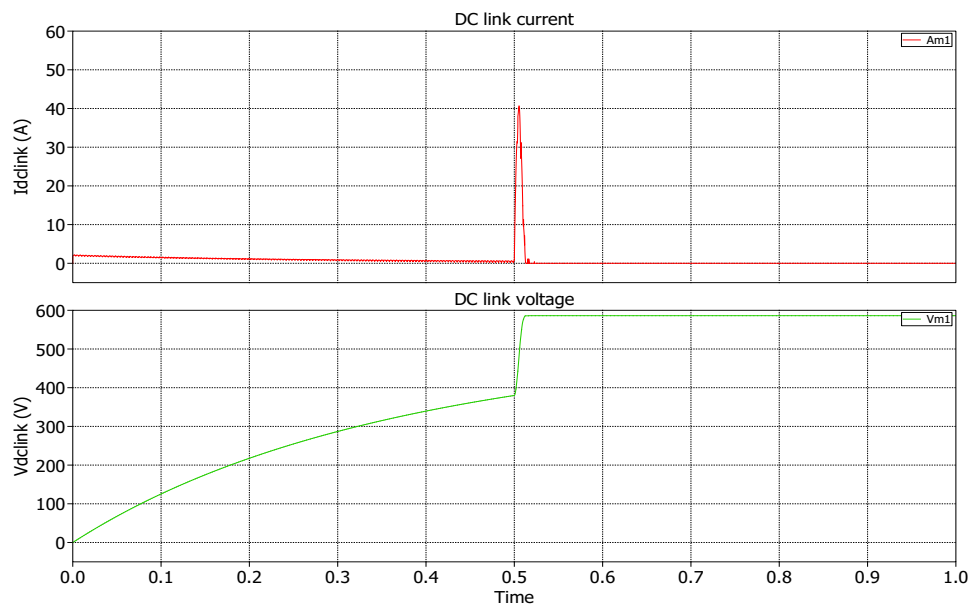


Figure 3.33: Simulation plots of DC link current and voltage with the precharge circuit active until 0.5 s

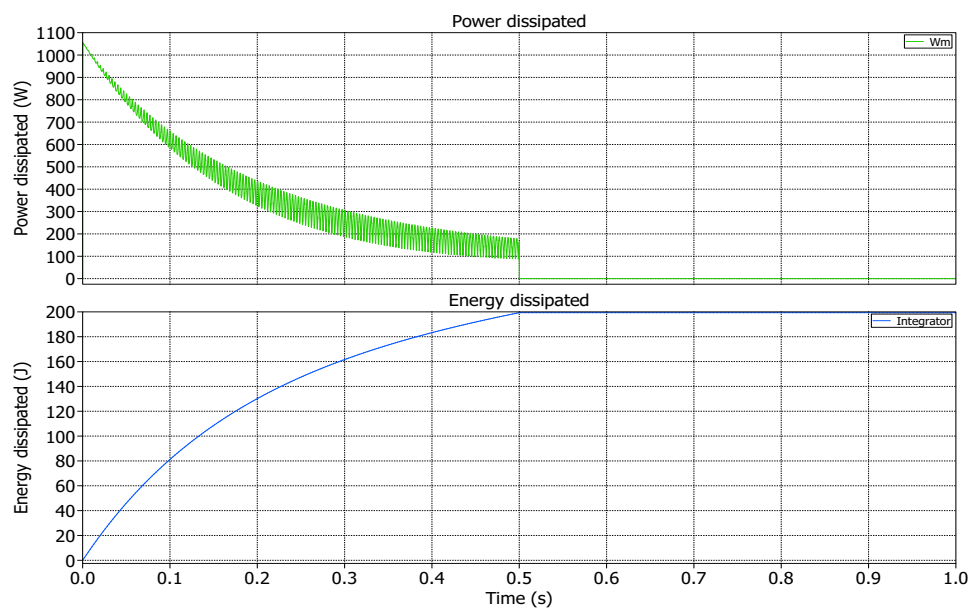


Figure 3.34: Simulation plots of energy and power dissipated through the precharge resistors

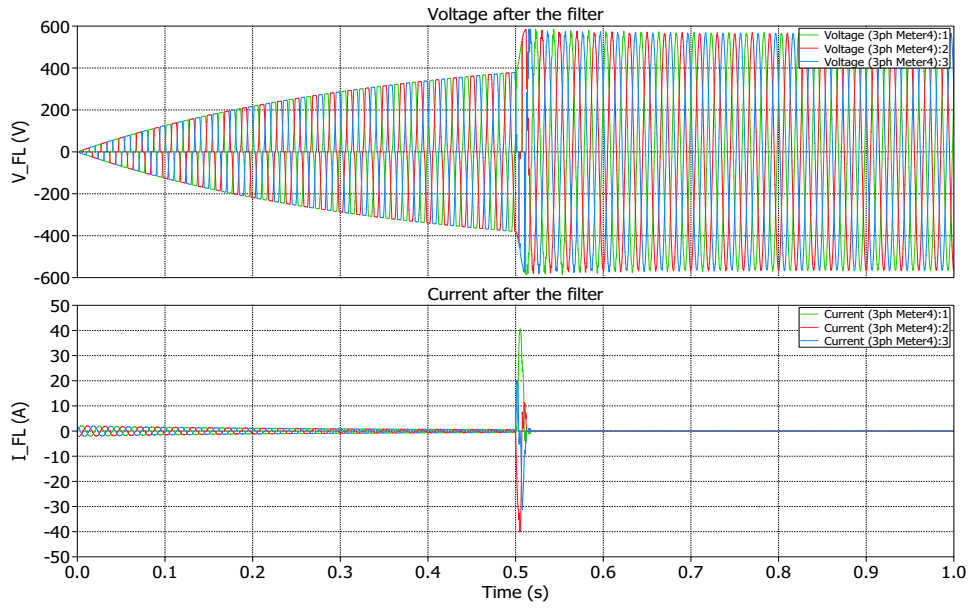


Figure 3.35: Simulation plots of current and voltage after the filter in the precharge circuit

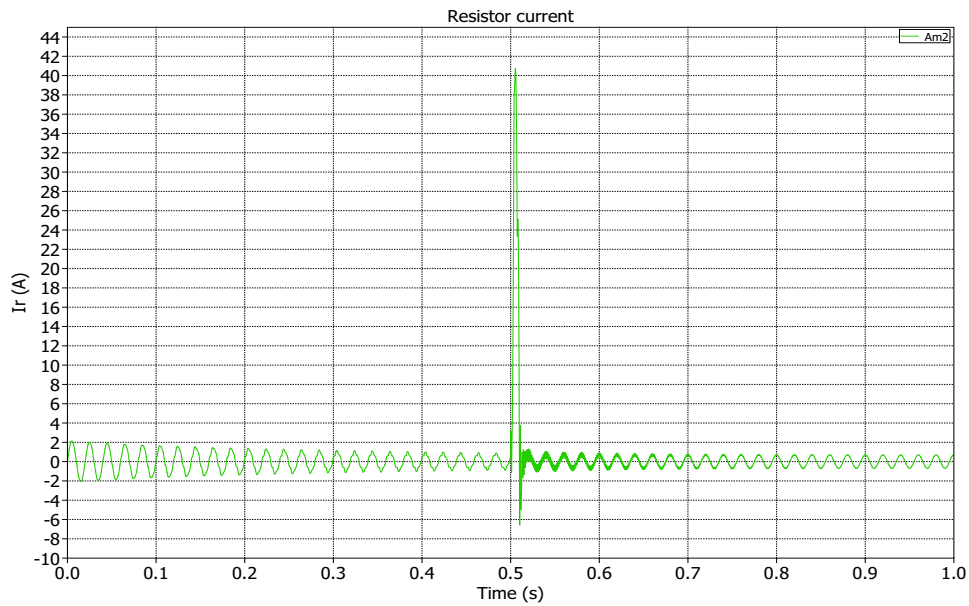


Figure 3.36: Simulation plots of the current flowing through the precharge resistor

3.4.3 Test and validation

During the start up when the current is too high, a contactor operates in order to flow the power in a precharge resistor dissipating the energy into heat and the contactor operation is determined by a timer that can be settled.

The precharge circuit assembled and used in the teaching setup is shown in Figure 3.37 where are visible the resistors, the contactor and the timer.

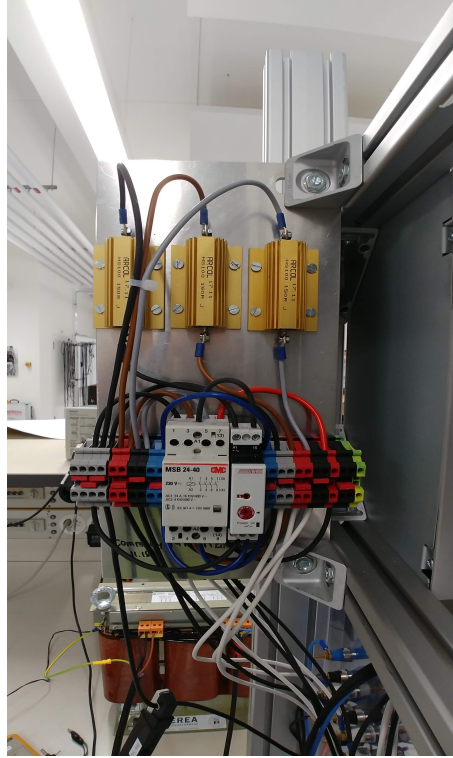


Figure 3.37: Precharge circuit in the teaching setup

Firstly, an experiment was built for test and validate the precharge circuit. Moreover, a backup detached similar capacitor is used for safety scopes because in the following test the goal is protecting the DC link of the real setup for precautions reasons, this way another external capacitor has the role of emulating the DC link of the setup. The capacitor used is a $1000\mu F$, instead of the setup nominal one of $700\mu F$ and the voltage used is less compared to the nominal value because this capacitor for the test can sustain 400 Vdc on it instead of 600 Vdc of the real DC link. This way the voltage used for feed the setup during the test was 200 V instead of 230 V for avoid to exceed rated values of the capacitor. About that, in the Figure 3.38 is possible to see the drawing of the experiment electrical scheme test using the external backup capacitor emulating the DC link.

The test was performed and the DC link current and voltage plot exported from a 4 channels Rigol oscilloscope and then manipulated in Matlab as plotted in Figure 3.39. As can be seen, the results are quite similar to the simulation plots with PLECS, indeed the capacitor initially is charging until 0.7 s where the timer triggers the precharge contactor and the precharge resistors are short-circuited giving rise to a short and small inrush current that disappears over a period of time really short as was in the simulation. The matching between the simulation and reality allows to say that the precharge circuit is well build and install inside the system.

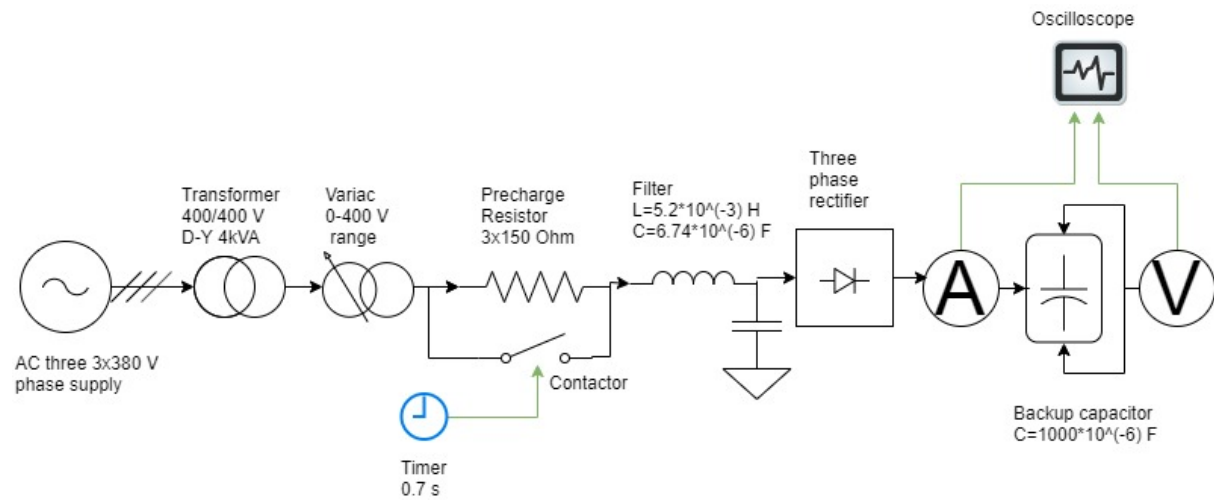


Figure 3.38: Test experiment components for the DC link backup capacitor

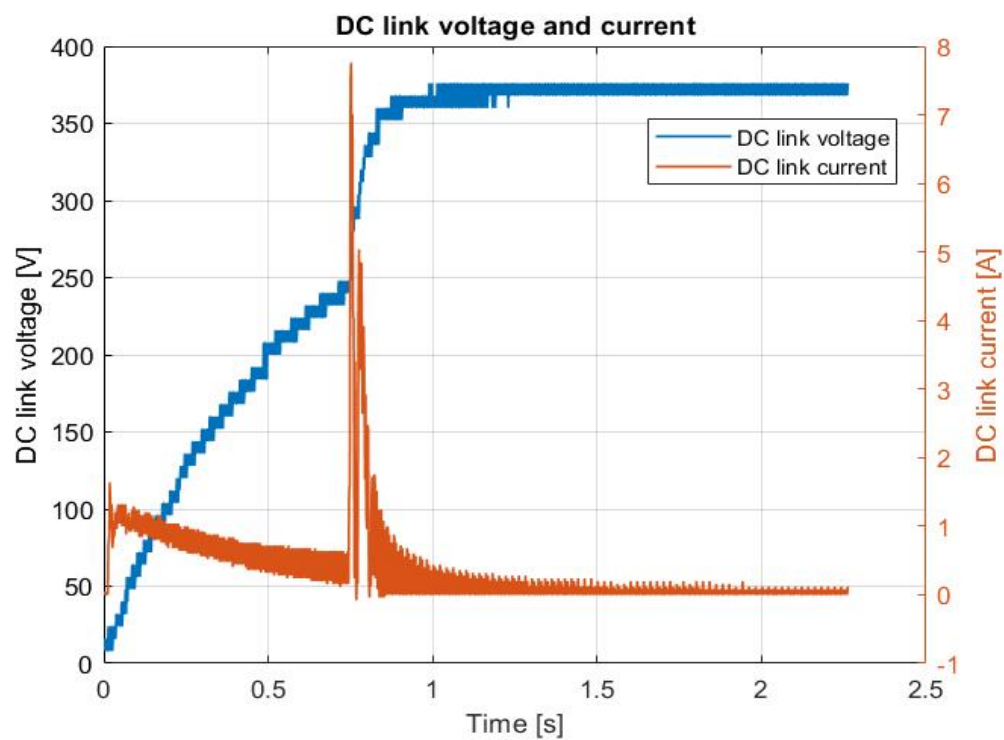


Figure 3.39: Test and validation oscilloscope plots of the DC link inrush current and the voltage with the precharge circuit

Chapter 4

Auxiliary measurements and PCB design

In this chapter a precise systematic approach is followed by designing, sizing and testing a light controller PCB for turning on the safety lamp, presented and described in the chapter 2, in case the DC link of the setup is charged.

Furthermore, the same process is followed by creating a PCB responsible for collecting signals and able to organize digital and analog signals coming from the Perun GPIO and connect them to the external user dashboard interface.

This way, the aforementioned components step realizations will be explained in detail in the following sections.

4.1 PCB safety light controller

In the next sections is presented the design, simulation, prototyping, test and validation of an electric sensing circuit connected to the DC link of each drive called PCB safety light controller [13].

Therefore, it will be organized as follows:

- sensing circuit design objectives and goals
- design of the circuit
- circuit simulation on LTspice
- creation of a PCB voltage sensing prototype with the simulated electronics components
- test of the PCB voltage sensing prototype
- proper PCB design in Altium in order to create a commercial PCB that can be replicate in 40 exemplars in the future for the setup
- test of the PCB designed in Altium

4.1.1 DC link voltage sensing circuit objectives

This circuit takes power from the DC link self supplying himself and it is responsible of the measurement of DC link voltage and comparison with a safety voltage lower value

of 50 V.

The sensing circuit as long as the voltage measured on DC link is above 50 V powers the orange light of the safety lamp indicating that the capacitor of DC link is charged, so it warns the user avoiding electric shock touching something in tension.

Once the DC link voltage goes below 50 V, the orange light goes off indicating that a safety level voltage is on DC link for the user that approach and manipulate something. Moreover, the strength of this sensing circuit is that if you disconnect the setup from the power supplies and inverters, the orange safety light has to stay on, as long as the DC link voltage is above 50 V, allowing an high reliability level on safety because the circuit is passive and doesn't need an external power supply for working.

4.1.2 Design and simulation of DC link sensing circuit

In the Figure 4.1 is shown the circuit simulation with the help of the LTspice software.

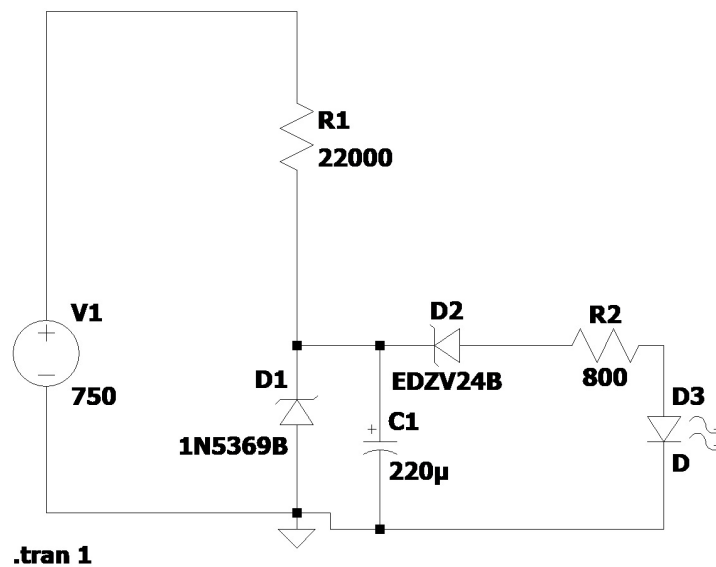


Figure 4.1: DC link voltage sensing circuit topology simulation on LTspice

Where

- V1 voltage source is the maximum DC link voltage
- R1 is a potential divider resistor to scale down the voltage
- D1 is a zener diode that has 50 V breakdown voltage and it is used in reverse polarization for stabilizing and limiting the voltage to 50 V
- C1 is a capacitor used for stabilize the voltage of the zener diode D1
- D2 is a zener diode with a breakdown voltage of 24 V used in reverse polarization that provide certain threshold, as voltage needs to be over 24V for this zener to break, and once D1 holds 50V, this zener will limit 24 volts on lamp
- R2 is the load lamp impedance
- D3 is the LED lamp that has to be powered

From the topology can be deduced that the zener diodes play a crucial role, in particular, the zener diodes are used because when the voltage on the zener or breakdown voltage is bigger than the rated value, the avalanche breakdown takes place and the current flows through the zener in order to avoid a voltage rise on it [14].

This way, when the reverse saturation is reached, the voltage across the zener diode becomes stable behaving like a constant voltage power supply.

Knowing the maximum DC link voltage

$$V_{dc,max} = 750V \quad (4.1)$$

and the maximum voltage and current tolerable by the lamp from the datasheet

$$V_{lamp,max} = 24V, I_{lamp,max} = 30mA \quad (4.2)$$

it was possible to calculate the potential divider resistor that represents a delicate component of the circuit, because it has to dissipate a remarkable amount of power losses considering the PCB thermal behaviors and patterns.

Therefore, the important thing is to have a dissipation power tolerable by the resistor in order to avoid to damage it and all the other electronics components.

Using a resistor $R1 = 22000\Omega$, the current flowing through it is $I_1 = 31.8mA$, this way the maximum power that it has to handle is

$$P_{1,max} = R1 \cdot I_1^2 = 22.25W \quad (4.3)$$

that is acceptable for a through hole PCB resistor.

Besides, using the two aforementioned zener diodes, the maximum voltage across the lamp and the current flowing through it in the worst DC link condition are acceptable because

$$V_{lamp,max} = 24.5V, I_{lamp,max} = 29.8mA \quad (4.4)$$

that are closed to the lamp datasheet values.

Therefore, in the Figure 4.2, is possible to see the Ltspice simulation plots exported in Matlab of the lamp turning on during the start of the system powering the DC link voltage.

Indeed, the DC link turning on, is represented by a voltage step rise from 0 to 750 V in blue and the output voltage across the lamp, in orange, it is an exponential voltage curve of the lamp turning on process.

It has to be underlined that the delay between the output voltage, lamp voltage in orange, and the input voltage, DC link voltage in blue, is really short, less than 0.2 s, but in the reality that time will be longer.

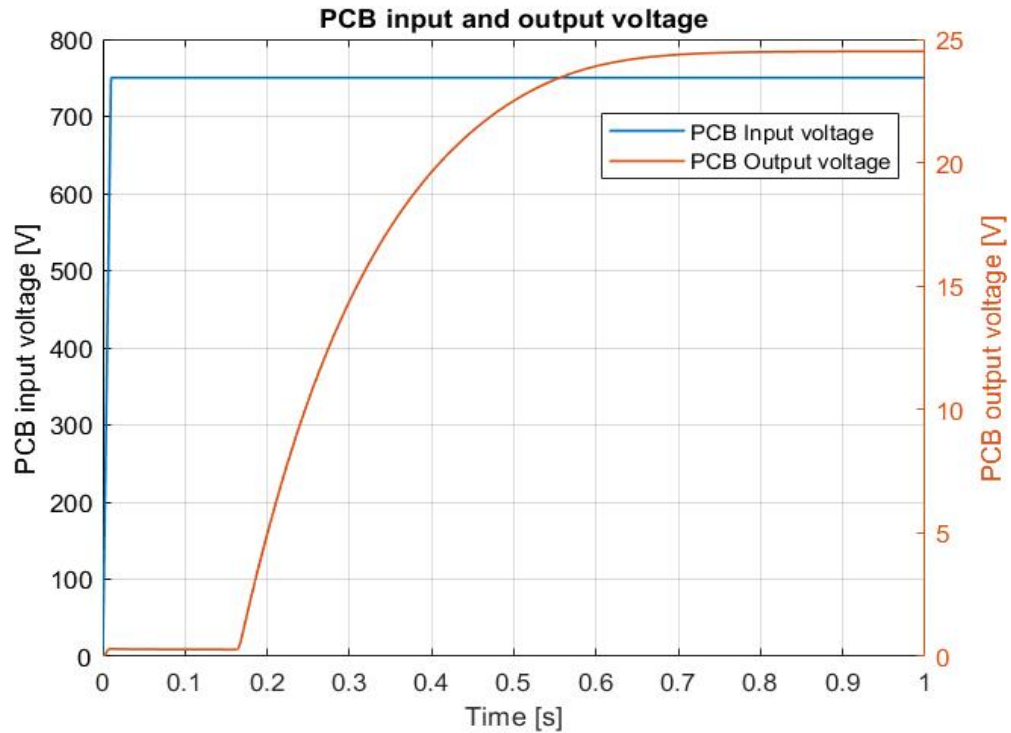


Figure 4.2: Ltspice simulation of the DC link voltage called PCB input voltage and lamp voltage called PCB output voltage

4.1.3 DC link PCB voltage sensing prototype

After selecting the available appropriate components and a breadboard, the soldering of the components is done in order to replicate the circuit topology shown in the Figure 4.1.

The PCB prototype with through hole components is illustrated in the Figure 4.3, where is possible to see the following components:

- two $10k\Omega$ resistors
- $1.5k\Omega$ resistor
- $220\mu F$ electrolyte capacitor
- 24 V and 51 V breakdown voltage zener diodes
- 2 DC link input connectors for + and - detached for isolation safety reasons
- output connector to lamp light

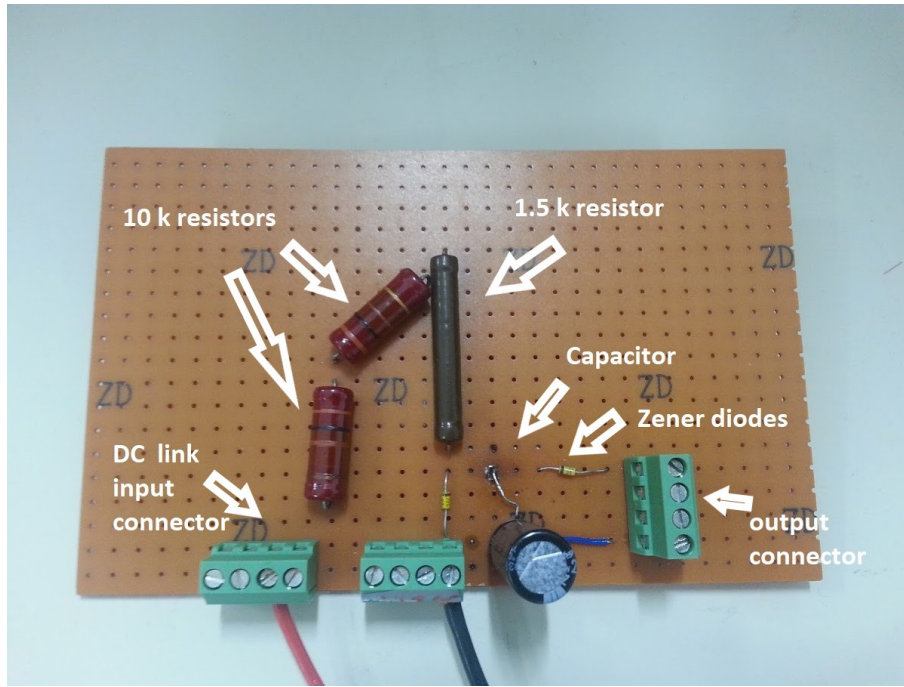


Figure 4.3: DC link voltage sensing circuit prototype

It can be noticed that there is a small difference with the topology shown in the LTspice simulation.

Indeed, on this prototype were used two $10\text{ k}\Omega$ resistors and a $1.5\text{ k}\Omega$ resistor in series for a total value of $21.5\text{ k}\Omega$ instead of $22\text{ k}\Omega$ because that was the immediate availability of resistor components value in the Lab, but this is not leading to relevant differences.

4.1.4 DC link PCB sensing voltage prototype test

For being able to validate the aforementioned PCB sensing voltage prototype it was tested on the teaching setup.

The lab test, illustrated in the picture 4.4, is performed with the goal of using the DC link voltage sensing circuit for turning on the orange light when the DC link voltage is above 50 V . Therefore, the experiment is done varying the DC link voltage from 0 to the nominal value using a DC power supply and recording the behaviour of some electrical quantities.

About that, the input and output voltage of the circuit are measured through voltage differential probes and plotted in the oscilloscope in order to see the DC link voltage and the voltage across the lamp variations.

The goal is to have the same results of the Ltspice simulation, this way a trigger is set when the Input voltage is above 50 V , in order to record the plots of Input voltage and Output voltage as soon as the light is on.

In the Figure 4.5, is possible to see the DC link voltage step variation from 0 to 600 V and the output lamp voltage pattern.

It has to be underlined that the plot of the output voltage is slightly different from the ideal simulation because as soon as the voltage zener reaches the breakdown voltage of 50 V , small rise of orange plot at 0.9 s , the capacitor charges and then at 1.3 s the output voltage rises starting turning on the lamp.

By the way, the simulation results and the prototype test results well matches meaning

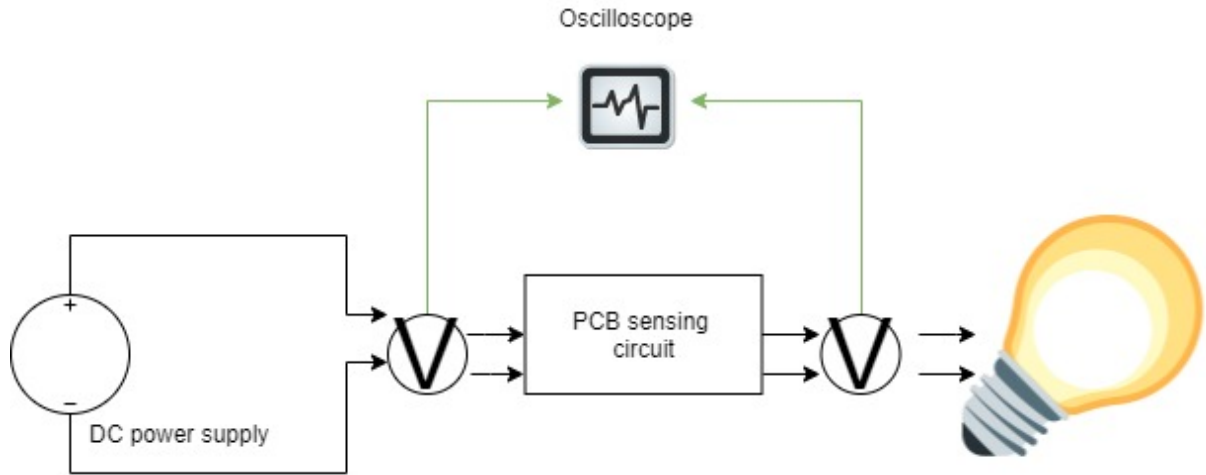


Figure 4.4: DC link PCB sensing prototype test

that the sizing and simulation are corrects.

Indeed, the goal of having the orange light turned on when the DC link is charged is reached.

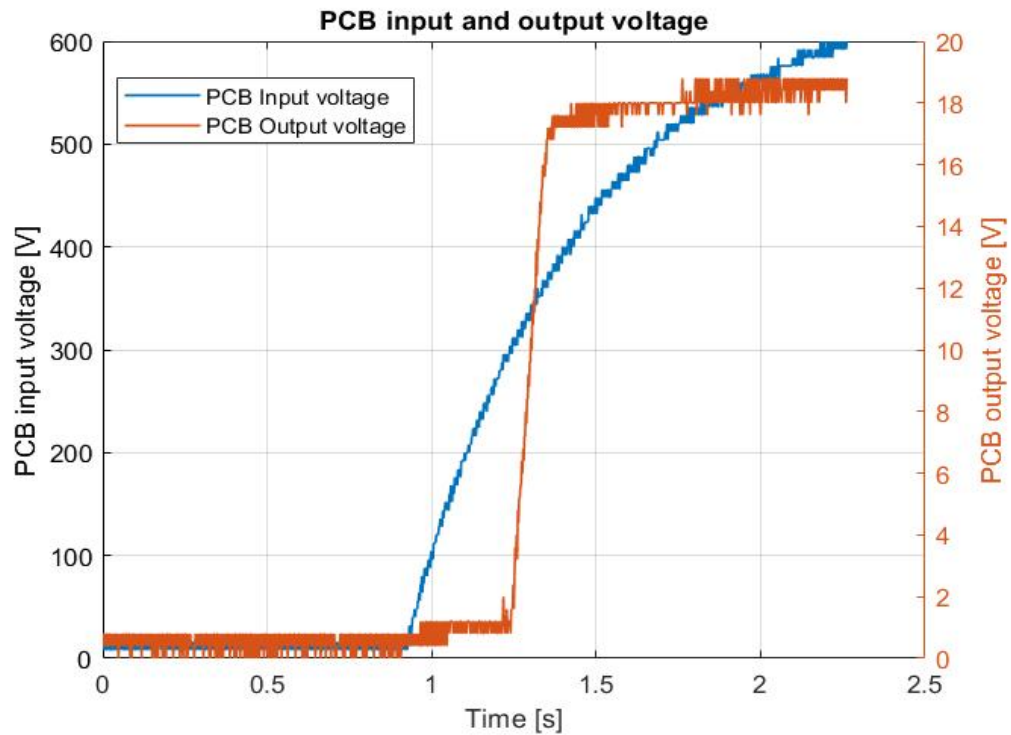


Figure 4.5: DC link voltage and lamp voltage oscilloscope test plots of the DC link PCB sensing prototype

4.1.5 Complete PCB safety light controller board design in Altium

After having successfully tested the voltage sensing prototype, a proper PCB design using surface mounted components and the software Altium is done.

Furthermore, from the initial PCB prototype are added also a fuse for protection reasons, some connectors for PCB pin assignments in order to exploit all the lights of the safety lamp, connectors for connect to Perun internal Relays, external Relays and an external power supply.

The PCB design process in Altium is composed by the following steps:

- creation of the schematic components library
- creation of the PCB components footprints according to datasheets
- creation of the schematic circuit with the schematic components, as shown in the Figure 4.6
- creation of the PCB according to design rules
- creation of 3D PCB components for having the idea of the space occupied inside the inverter box by the PCB
- order of components selected from online manufacturers databases

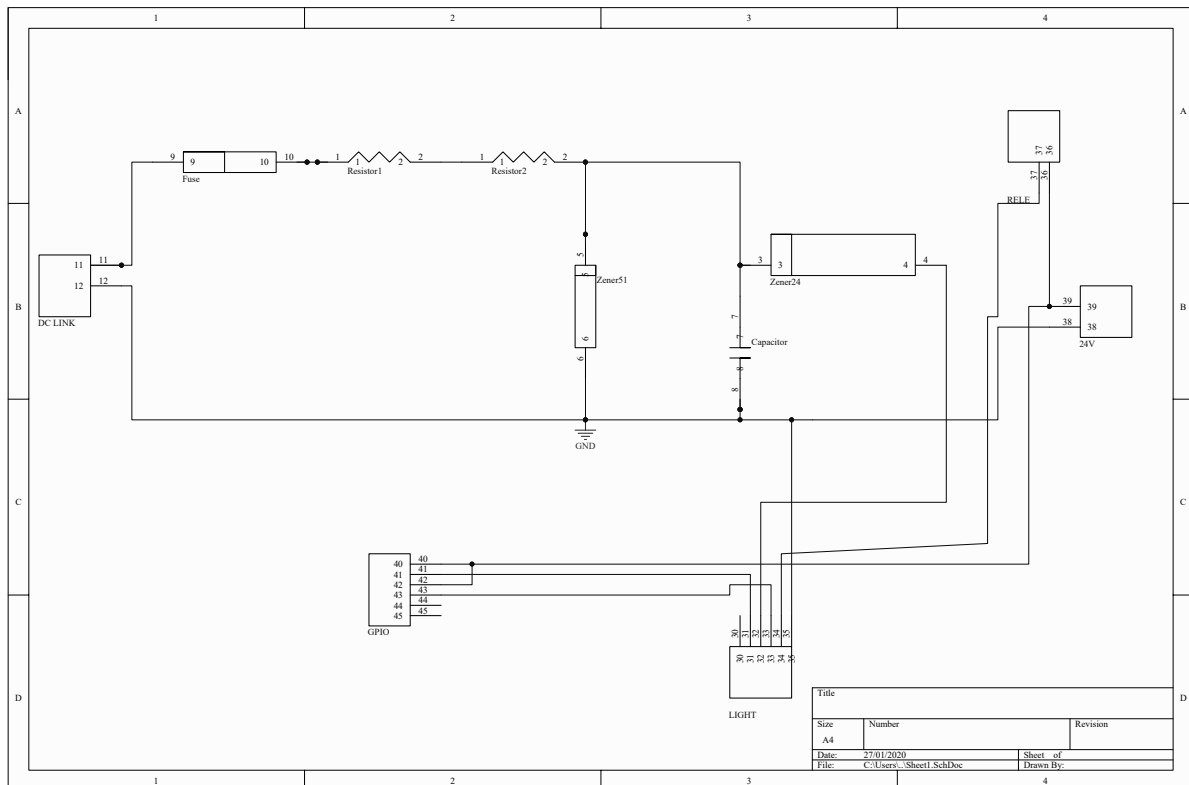


Figure 4.6: PCB schematic in Altium

Besides, the elements composing the PCB designed in Altium and ordered online are:

- two $11\text{ k}\Omega$ SMT resistors in series
- SMT electrolyte capacitor
- 24 V SMT zener
- 51 V SMT zener

- protection fuse
- fuse holders
- DC LINK 2 pin input high voltage connector using the following pins
 - +
 - GND
- 6 pin connector for the safety light pins:
 - PIN 30 Alarm
 - PIN 31 Red light
 - PIN 32 Orange light
 - PIN 33 Green light
 - PIN 34 White light
 - PIN 35 Ground
- 6 pin connector for Perun internal system Relay Outputs connector controlled by motherboard error signal ERR connecting the red light and green light pins using the following pins
 - PIN 40 Relay 1 COM
 - PIN 41 Relay 1 NC
 - PIN 42 Relay 2 COM
 - PIN 43 Relay 2 NC
 - PIN 44 Relay 1 NO
 - PIN 45 Relay 2 NO
- 2 pin connector for connecting to an external Relay the white light pin using the following pins
 - PIN 36 NC1
 - PIN 37 NC2
- 2 pin connector for connecting the external NC Relay to an external 24 V power supply using the following pins
 - PIN 38 GND
 - PIN 39 24 +

It has to be underlined that the design is done according to some mechanical constrains because the PCB place inside the inverter box can not be more than 6 cm x 6 cm with a limited 3D space.

Therefore, the design in Altium is done keeping in mind to reach the goal of having small and efficient components that allow to save space.

Indeed, in the Figure 4.7 is shown the 2D PCB layout in Altium, where in red are visible the solder paths and footprints, while in green can be seen the holes for the placing of

some through hole components.

Furthermore, in the Figure 4.8 are shown the 3D Altium picture from the top sight with all the components characterising the sensing circuit and the 3D Altium picture from the bottom sight with all the connectors linking the PCB to other systems.

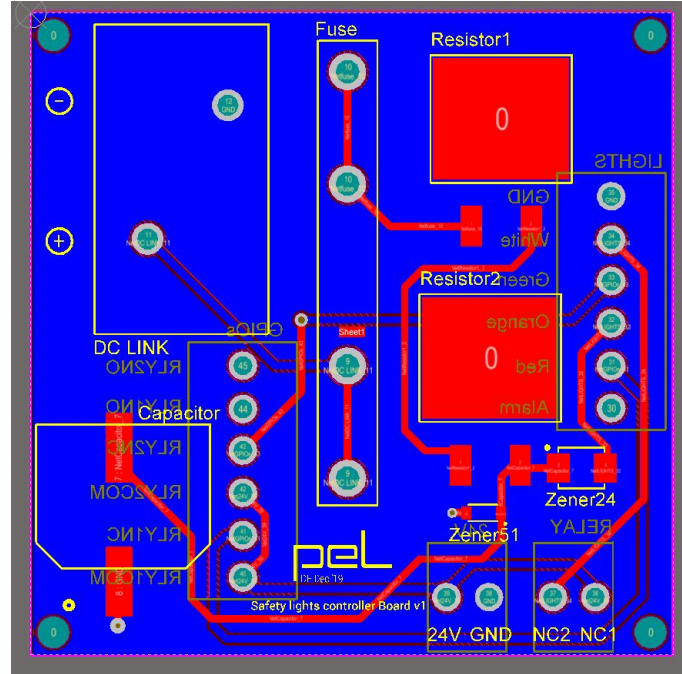
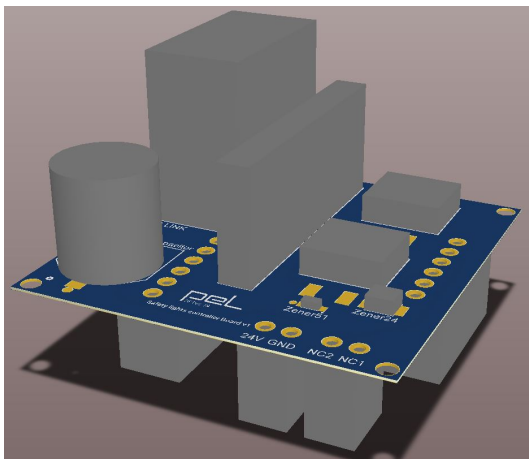
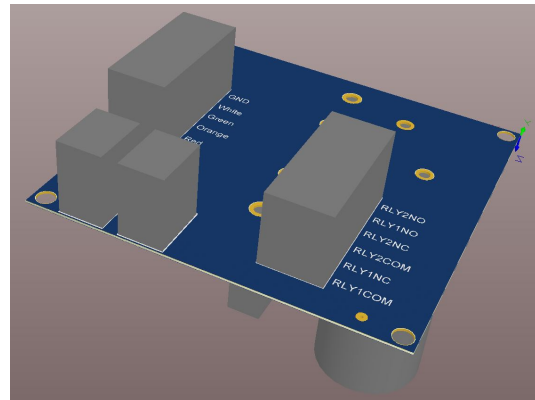


Figure 4.7: 2D PCB in Altium



(a) 3D PCB in Altium top sight



(b) 3D PCB in Altium bottom sight

Figure 4.8: 3D PCB in Altium

4.1.6 PCB safety light controller version 1 realization

Once the design is completed and the PCB with all the components is ready, the order of the PCB and related components is done.

After that, the soldering is realized and the final PCB for the teaching setup ready for being replicate in big numbers.

Therefore, the realized PCB version 1 is illustrated in the Figures 4.9 and 4.10.

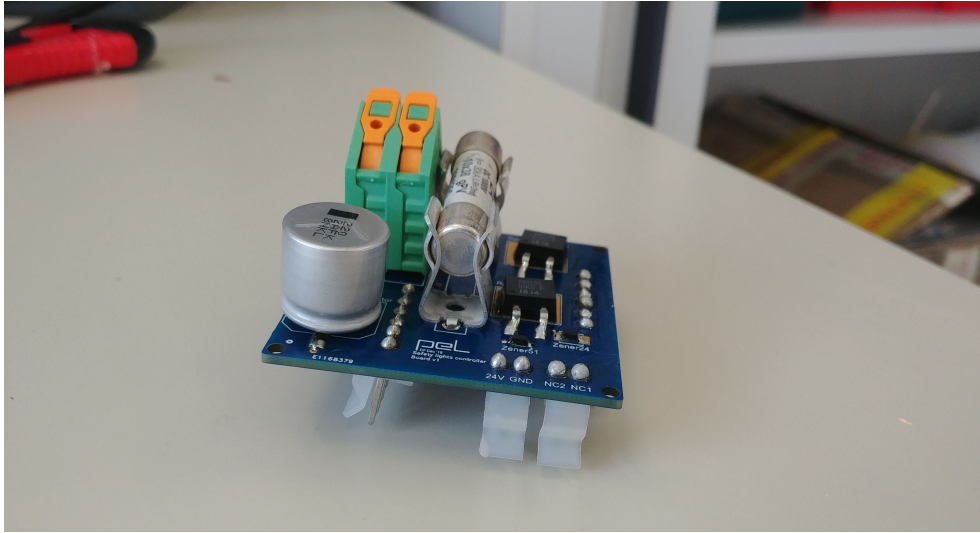


Figure 4.9: PCB version 1 front sight



Figure 4.10: PCB version 1 top sight

It has to be underlined that the version 1 of the PCB is working properly, according to the purpose for which is designed as explained in the previous part.

Moreover, for optimizing the design due to some physical constrains, the DC link connector and the fuse with the related fuse holders should be changed, using some smaller ones because the vertical space they occupied is too much for a perfect space allocation in the inverter box.

Also the resistors should be changed because the SMT components are heating too much during normal operating condition since it is detected from the thermal camera a temperature of 130°C .

Therefore all those constrains leads to a second design version that will be presented in the following sections.

4.1.7 Test and validation of the safety light controller PCB

The same test that was carried out for the PCB sensing prototype is repeated in this section with PCB version 1. Also in this case, the goal is that the DC link voltage sensing circuit is turning on the orange light when the DC link voltage is up to 50 V.

This way, a step voltage variation from 0 to 600 V, the nominal voltage value, is done with the DC power supply behaving like the DC link and the oscilloscope is used for recording some plots.

About that, in the Figure 4.11, is possible to see the DC link voltage and the voltage across the lamp that behave similarly to the PCB prototype test. Not only, it can be deduced that the safety light controller design and assembly is done properly and in a correct manner because the results shown in the Figure matches to ones of the PCB prototype test.

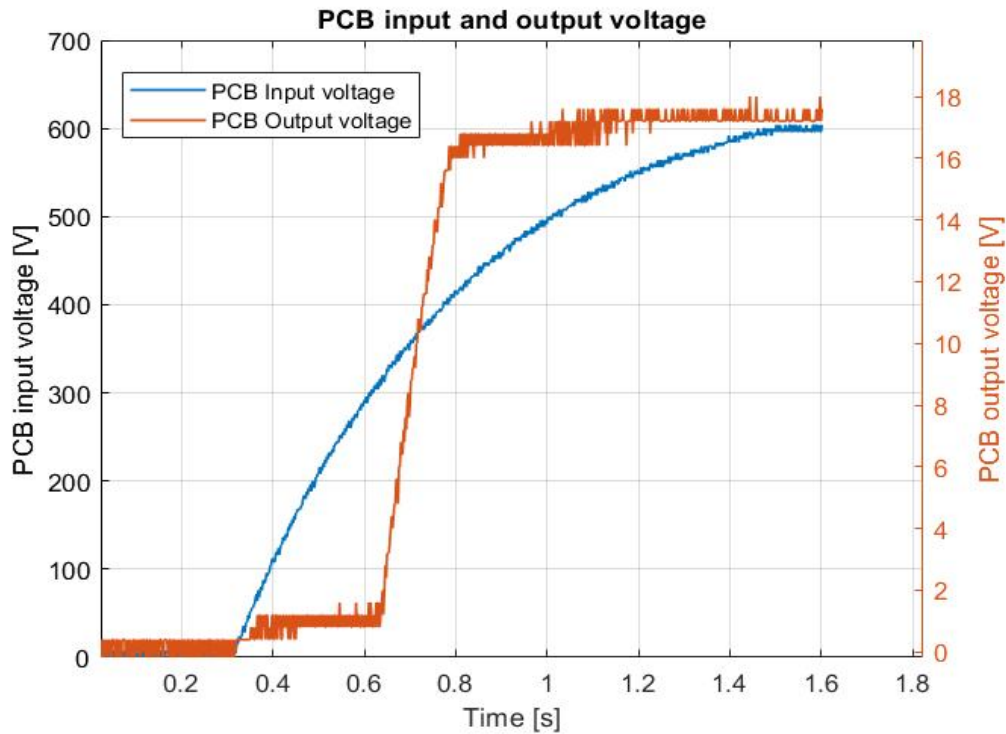


Figure 4.11: Safety light controller DC link voltage and lamp voltage oscilloscope test plots

4.1.8 PCB safety light controller version 2

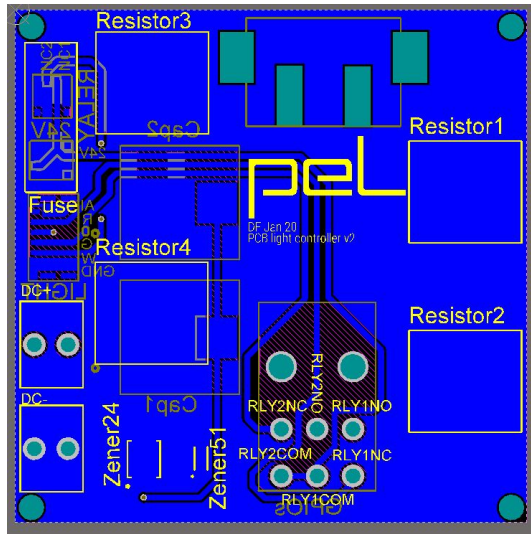
As mentioned previously, a new version of the PCB is done in order to optimize the space occupied by the components and avoiding excessive heating on the PCB during normal condition operation.

The new PCB done in Altium, called PCB version 2, is shown in the Figure 4.12 where is possible to see that new more compact components were selected, indeed the 3D space occupied is less compared to the previous version.

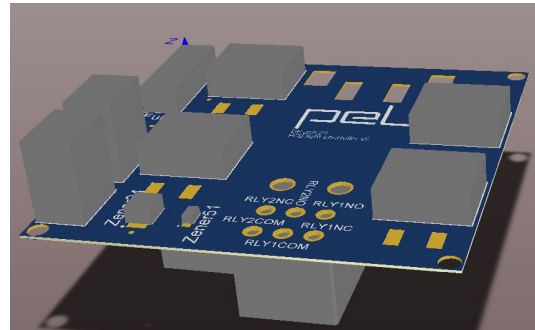
Those components are:

- new and more compact SMT fuse

- 4 resistors in series reaching the same previous resistance value, instead of 2, but each one able to handle 35 W so the thermal stress on those components is half
- more compact connectors



(a) 2D PCB version 2 in Altium



(b) 3D PCB version 2 in Altium

Figure 4.12: PCB version 2 in Altium

Moreover, the PCB version 2 will not be realized physically by me due to a leak of time during the project period.

4.2 GPIO collecting signals PCB

In the next sections is presented the design and prototyping of a PCB that collects the signals coming from the Perun GPIO and organize them properly in order to make them accessible to the external user dashboard interface.

This PCB is called GPIO collecting signals PCB that will be presented as follows:

- GPIO collecting signals objectives and goals
- GPIO collecting signals design in Altium
- GPIO collecting signals realization

4.2.1 GPIO collecting signals PCB objectives

The purpose of that PCB is to collect some of the signals coming from the Perun GPIO board, and through the use of a PCB connect them to a main LEMO connector grouping and sending them to the user dashboard interface where knobs, meters and other devices allow to manage those signals.

Furthermore, the total amount of signals coming out from the Perun GPIO system are 36 but the user dashboard interface needs just 30 of them respectively:

- 9 signals for the Analog Input
- 8 signals for the Analog Output
- 7 signals for the Digital Input
- 6 signals for the Digital Output

Furthermore, on the PCB there is also an output connector that is responsible of collecting and making easily accessible the GPIO signals that are used externally for:

- triggering of the precharge timer circuit
- analog interface feedback voltage of the Delta Elektronika DC power supply

This way, from the Figure 4.13, is possible to see the schematic of the collecting signals PCB where all the aforementioned connector and respective signals are shown in details. It has to be underlined that the Ground signals, GND, are all referred to the same ground but they need to be taken into account for each respective signals for EMC reasons keeping differential signals intact quality.

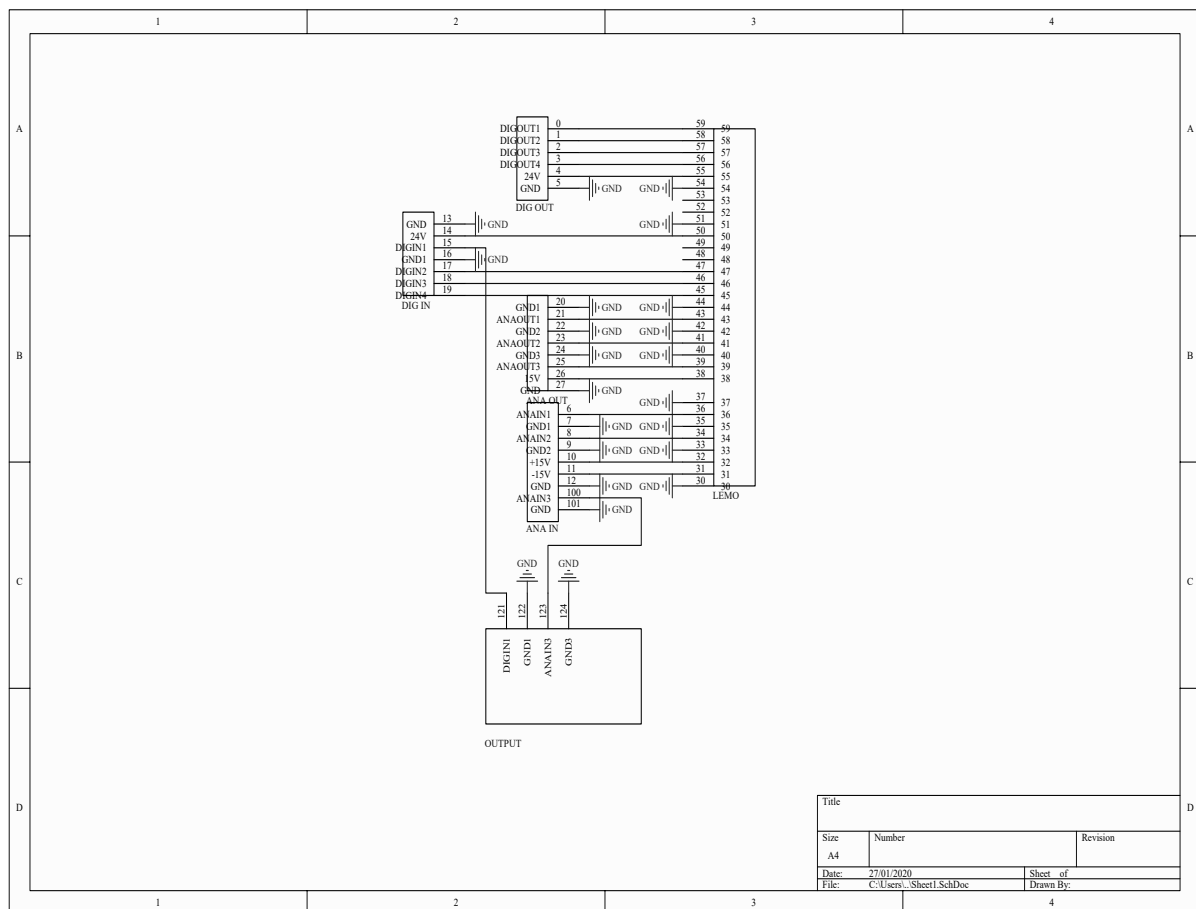


Figure 4.13: Schematic of the GPIO collecting signals PCB

4.2.2 GPIO collecting signals PCB design in Altium

The goal of this PCB is to collect and organise properly all the signals coming from GPIO board in order to avoid mess wiring inside the converter plastic and link them by the mean of copper traces to a main 30 pin LEMO connector.

Attached to this connector a wire can be plugged outside the converter box giving the possibility to access to all those signals from the final user dashboard interface.

The design process is done as the previous PCB, because also in this case, there is a restricted space allocated for the PCB, so the mechanical constrains are the main problems to be respected in the design.

About that, in the Figure 4.14 is possible to see the 2D Altium PCB layout having in the center the main communication connector from Lemo and around it all the other connectors linking the PCB to the GPIO boards.

While, the 3D Altium PCB design is shown from the top and from the bottom in the Figure 4.15.

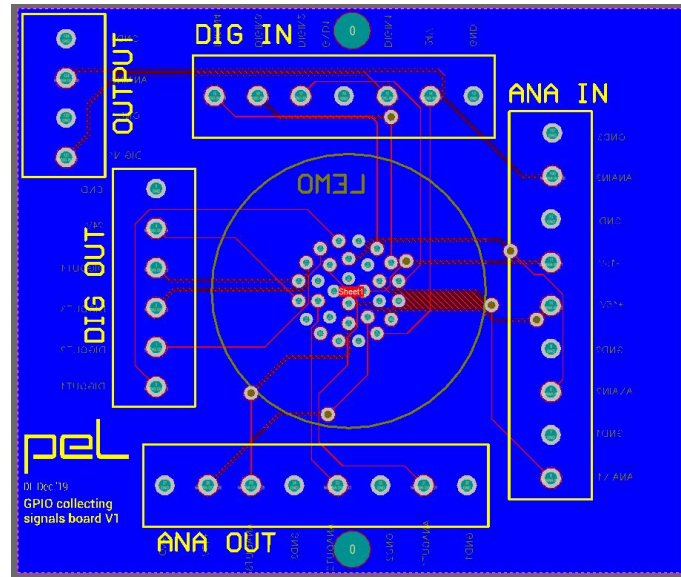
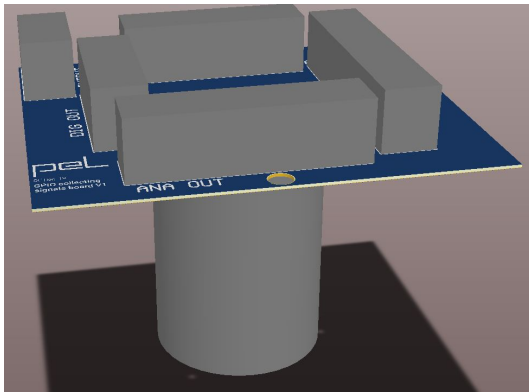
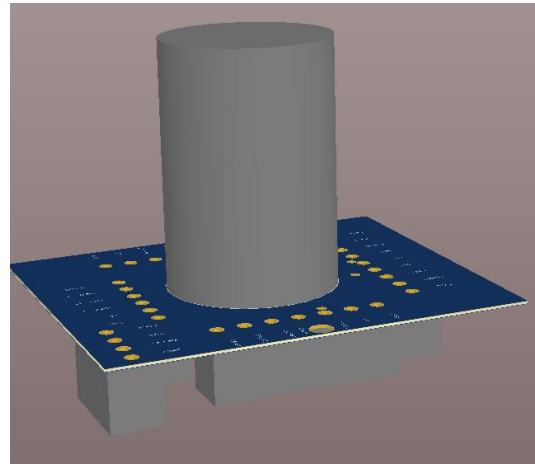


Figure 4.14: 2D GPIO PCB in Altium



(a) 3D GPIO PCB in Altium top sight



(b) 3D GPIO PCB in Altium bottom sight

Figure 4.15: 3D PCB in Altium

4.2.3 GPIO collecting signals PCB realization

In the Figure 4.16 is shown the GPIO collecting signals PCB soldered and realized ready for be operative.

Indeed, it's possible to see the Digital output connector, the Digital input connector, the Analog output connector, the Analog input connector, the output connector and the through holes footprints of the LEMO connector allocated on the back PCB layer.

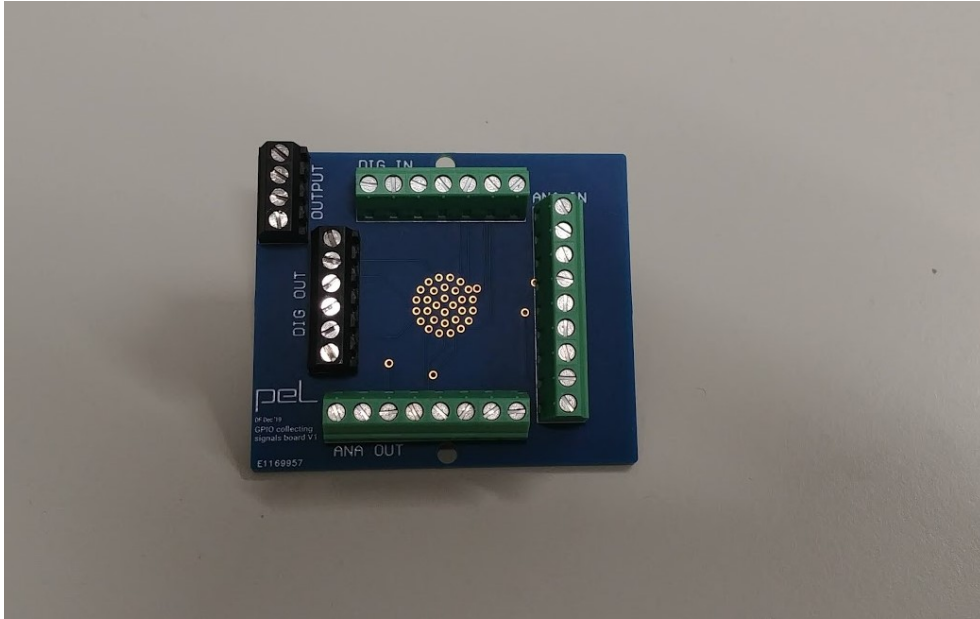


Figure 4.16: Top sight of the PCB realized

Chapter 5

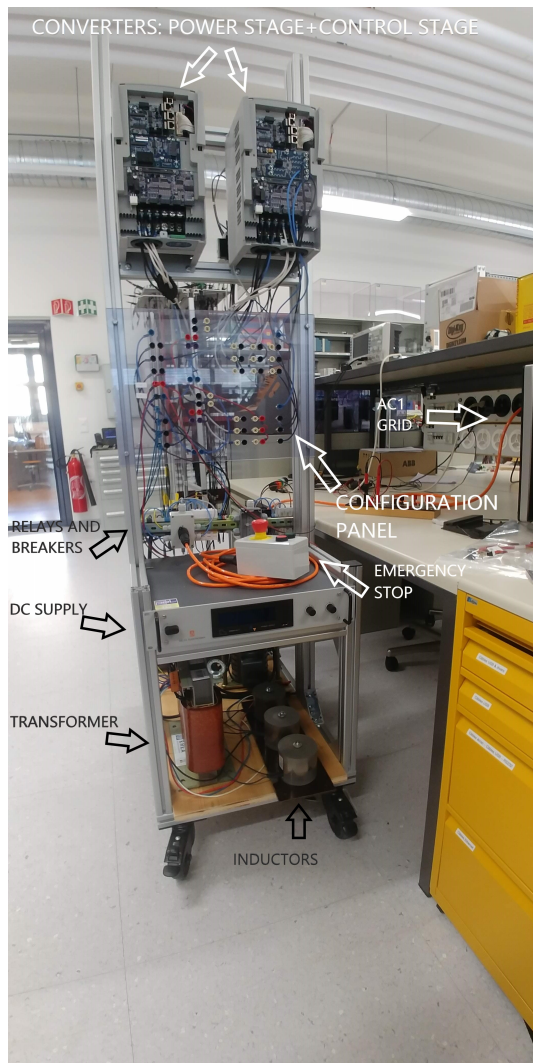
Final teaching setup prototype

In this section is presented the power electronics teaching setup state when I finished my project period. About that, from the Figure 5.1 is possible to see the real hardware setup with all its main related components indicated through arrows.

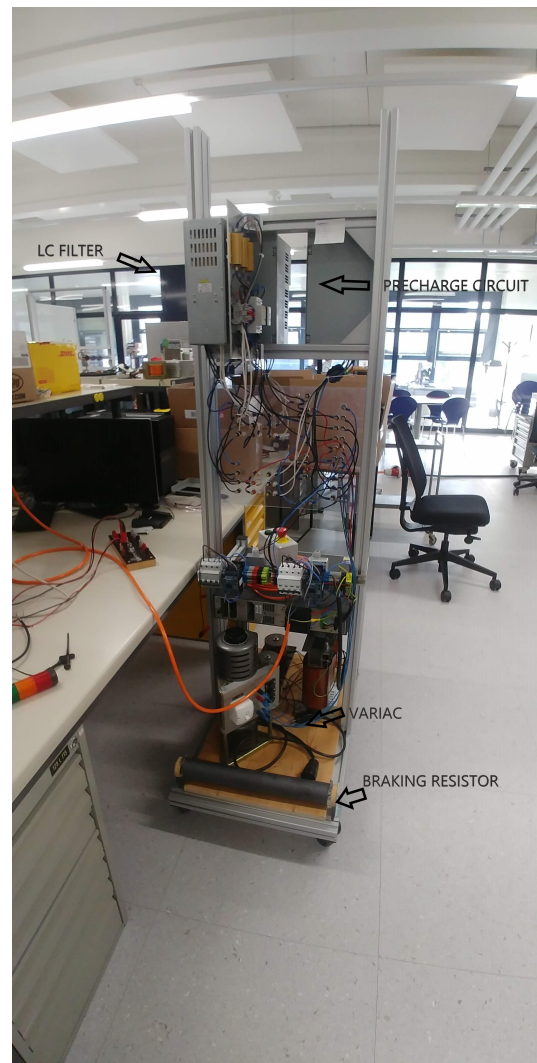
Moreover, it has to be underlined that it's not the final complete and working version due to lack of time carrying out the long project and unexpected problems encountered during the realization and assembly of the hardware components.

In particular, the order and delivery of some components was really long this way the systematic approach couldn't be fully covered.

Therefore, the completion of the setup realization will be committed to other persons and the future works and elements to improve or change will be presented in the next chapter.



(a) PETS front sight



(b) PETS rear sight

Figure 5.1: PETS hardware

Chapter 6

Conclusions and future works

At the conclusion of this project can be derived that even if the prototype is not fully complete and operational the results reached were satisfying. In particular, the approach followed has given the possibility to cover all the steps of the design and realization processes, indeed designing, sizing, test and validating allowed to understand multiple engineering fields and skill sets acquiring practical knowledge of what studied during the academic path.

Furthermore, all the designed relevant elements and PCBs outlined proper choices, since the matching between size, simulation and test were always reached and explained in this thesis.

Therefore, the potentialities of this setup seems to be promising ensuring a remarkable knowledge about power electronics to the future users.

For what concerns the future works the possible goals to be completed can be:

- program the DSP and interface the system with the Perun software
- design and prototype of the student dashboard interface
- preparation of DEMO exercises for the final user in order to exploit the PETS
- realization of the designed PCB version 2
- connection of the PETS with the Lab AC2 Regatron and motor load

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