POLITECNICO DI TORINO

College of Engineering

Master's Degree Course in Biomedical Engineering

MASTER'S DEGREE THESIS

Feasibility Study for sub-Hz oscillators in 180nm and 28nm CMOS technologies with area high-constrains

Supervisors:

Prof. Danilo DEMARCHI

Prof. Sandro CARRARA

Candidate:
Chiara BIELLI

March, 2020

ACKNOWLEDGMENT

Finalmente sono arrivata alla conclusione di questo importantissimo capitolo della mia vita e, nonostante l'immensa felicità, mille altre emozioni si fanno spazio nella mia mente. Questo lungo percorso è terminato, ma non devo i miei successi solo all'impegno e alla dedizione personale, quanto anche a tutti coloro che mi hanno sostenuta, consigliata e guidata fino al raggiungimento di questo importante traguardo.

Innanzitutto, con immensa stima e riconoscenza vorrei ringraziare i miei due relatori: il Professor Danilo Demarchi, per il contributo avuto nella mia formazione e l'aiuto fornitomi nel corso di questo progetto, e il Professor Sandro Carrara, che è stato il mio punto di riferimento all'EPFL di Losanna, per i suoi fondamentali suggerimenti e la grande disponibilità mostrata a supportarmi per arrivare alla conclusione di questa tesi.

Un ulteriore ringraziamento al Professor Danilo Demarchi per avermi anche dato la possibilità di partecipare ad un altro stimolante progetto, in collaborazione con MECA e l'Ing. Vladimir Stavrov, CEO all'AMG Technologies in Bulgaria, con il quale ho avuto la possibilità di mettermi alla prova con un primo studio di fattibilità su un vero progetto industriale.

A sincere thanks to Professor Catherine Dehollain, Professor at EPFL in Lausanne, whose support was extremely helpful during our multiple meetings, and her knowledge was fundamental for the conclusion of my project.

Un sentito ringraziamento anche ai miei colleghi, con cui ho condiviso le infinite ore di lezione, le lunghe giornate di studio e gli interminabili progetti. In particolare, a Rosa, mia compagna di banco il primo giorno di università e mia amica fino all'ultimo sui banchi del Politecnico e a Gian Luca, collega, amico e insostituibile compagno in tutti i giorni trascorsi in università, che hanno reso questo lungo viaggio un percorso ancora più memorabile.

Ringrazio dal profondo del cuore la mia migliore amica Carlotta, il cui sostegno è stato fondamentale per aiutarmi a superare i momenti di difficoltà e farmi sempre e comunque sorridere nonostante gli ostacoli che mi si opponevano.

Tutto questo non sarebbe però stato possibile senza il supporto della mia famiglia, che ha condiviso con me gioia e tristezza, senza mai farmi mancare l'aiuto di cui avevo bisogno. Quindi un grande grazie al mio grande "zione" Alberto e a mia nonna Luisa. Un particolare grazie a mio fratello Giulio, che è sempre stato per me un riferimento dal punto di vista scolastico e cinque anni fa mi ha proposto la "folle" idea di iscrivermi ad ingegneria.

Ed infine il ringraziamento più grande ai miei genitori. Mi hanno consigliata, aiutata sia finanziariamente che moralmente, non facendomi mai mancare l'appoggio di cui avevo bisogno in ogni aspetto della mia vita. Quindi un grazie a mio papà Davide, da cui ho ereditato una forte dedizione al lavoro e che mi ha insegnato che con il giusto impegno qualsiasi traguardo è raggiungibile. E a mia mamma Silvia, che con grande dolcezza mi ha sempre saputo sostenere e con infinita pazienza ha sopportato le lunghe ore passate a ripeterle lezioni interminabili.

Per ultimo un grazie anche a tutti coloro che non sono riuscita a citare direttamente in queste poche righe, professori, amici di corta e lunga data che hanno comunque avuto un contribuito nel mio percorso e mi hanno resa ciò che sono oggi.

CONTENTS

CHAPTER 1

INTRODUCTION

This master thesis takes part of a bigger project, the "Body Dust", that started in 2017 thank to the collaboration among professor Sandro Carrara from the EPFL in Lausanne, professor Georgiou Pantelis from the Imperial College of London and professor Danilo Demarchi from Politecnico di Torino.
The "Body Dust" concept is based on CMOS electronic sensing system and its realization could potentially completely change the medical diagnostic method used until now. In fact, the goal is to realize functionalized particles, with a total size in the "range of μm^3", which can target specific entities inside human body and measure their concentrations. The patient would be asked only to drink a cocktail, with millions of these nanoparticles that, after being ingested, would spread in human tissues, identifying specific molecules, blood proteins and whatever entities we are interested in, so that it would be immediate the identification of an unhealthy patient.
It is evident that in this way the traditional, medical methods used for diagnosing a disease, to observe the evolution of a tumor or the effect of a therapy, will be revolutionized: starting from TC to PET, from blood analysis to in vitro studies, everything could be done in real time, just by following the transfer of millions, or even billions of these nanoparticles inside human tissues, organs and cells.
So what the "Body Dust" really is it's a chip, made with integrated circuits (IT), less battery, that can enter in the metabolism of human body. We are not talking about a real molecular entity but about electronic components, which obviously need to respect biocompatibility boundaries, able to provide wireless information outside the body.
It's understandable that the project has well defined targets but at the same time it is very challenging: the possibility to have particles with almost the same size as red blood cells allows their spreading without problems inside the body and through gut-wall barriers and blood channels; the simultaneous functionalization with more than one molecule allows the multiple diagnosis of different components: from single entity to drugs concentrations but not only. The specifications of a project with such delicate application, as the medical environment is, are even more and this is the reason why we need a long and complex research work to accomplish the final aim. In particular one of the key components is the oscillator, responsible to fix the working frequency of the system and also one of the most difficult to design respecting the boundaries discussed before. This is exactly what this thesis wants to do: starting from the general concept of the "Body Dust" and the realization of its different components, travels the path that brings from the design of a proper analog oscillator to the research of the solution, its development and finally to its conclusion.

CHAPTER 2

TOWARDS BODY DUST DEVELOPMENT

From the previous introduction is understandable that the main goal of the "Body Dust" is to study the feasibility of a new diagnostic method using particles with a total size comparable to red blood cells (whose diameter is 7 μm), that can diffuse in human tissues, exploiting the mechanism of cells internalization. From the present state-of-the-art in CMOS design the size requirement seems to be unfeasible for now.
Therefore, as I already explained, this is not the only challenge because these particles also need to provide diagnostic information through specific molecular functionalization, using data-telemetry, with low power consumption and obviously observing biocompatibility.
The core idea is the design of a fully packaged CMOS cube as illustrated in Figure 2.1.

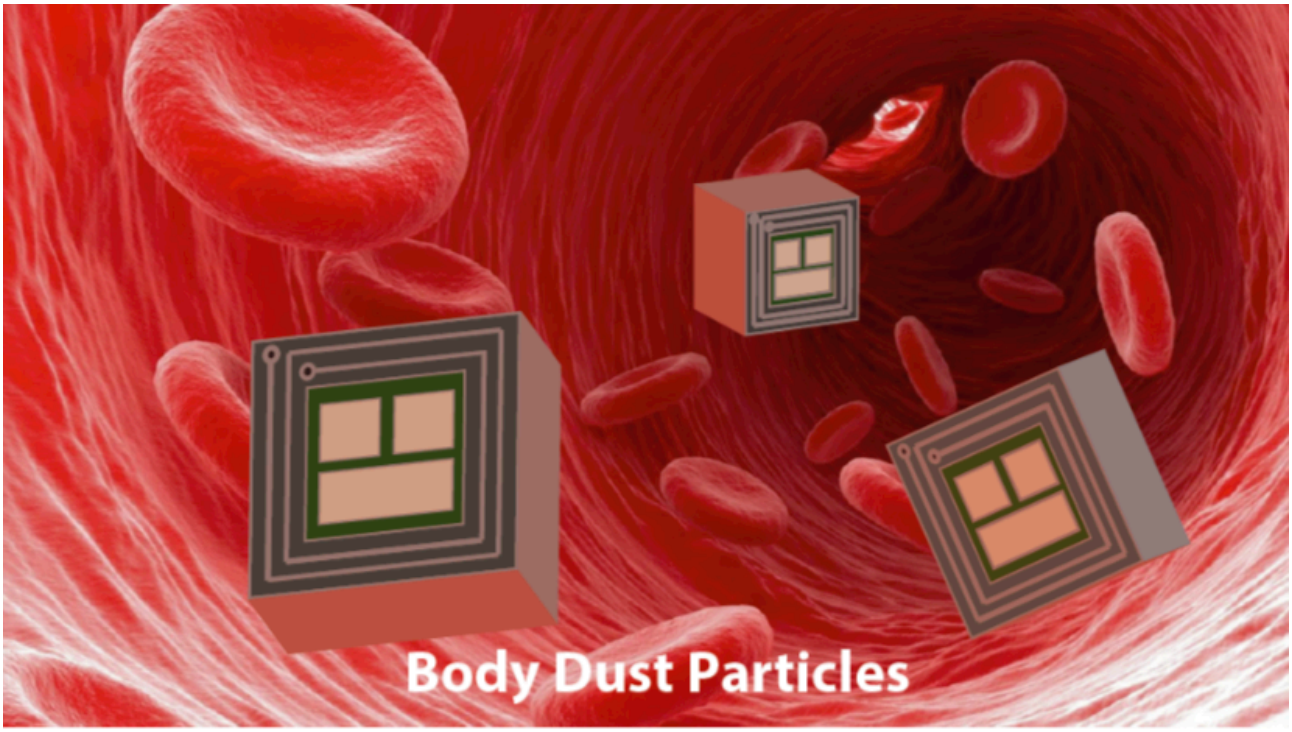


Figure 2.1 Illustration of the concept of Body Dust: diagnostic sensing cube with red blood cells comparable size; reprinted with permission from [2.1]

In 2012 a CMOS circuit for glucose sensing was successfully realized at size of 0.36 mm^2 [2.1], in 2014 biosensors with working electrodes radii of almost 2.5 μm have been published and successfully tested for glucose detection [2.2] and in 2016 micro-coils with lateral size from 200 μm to 50 μm to provide power in implantable micro-stimulators have been published [2.3], as well as a biocompatible packaging in epoxy-resin, to protect telemetric diagnostic devices, was discovered [2.4].
Thanks to all the mentioned researches the first model of CMOS Body Dust cube was proposed (Figure 2.2).

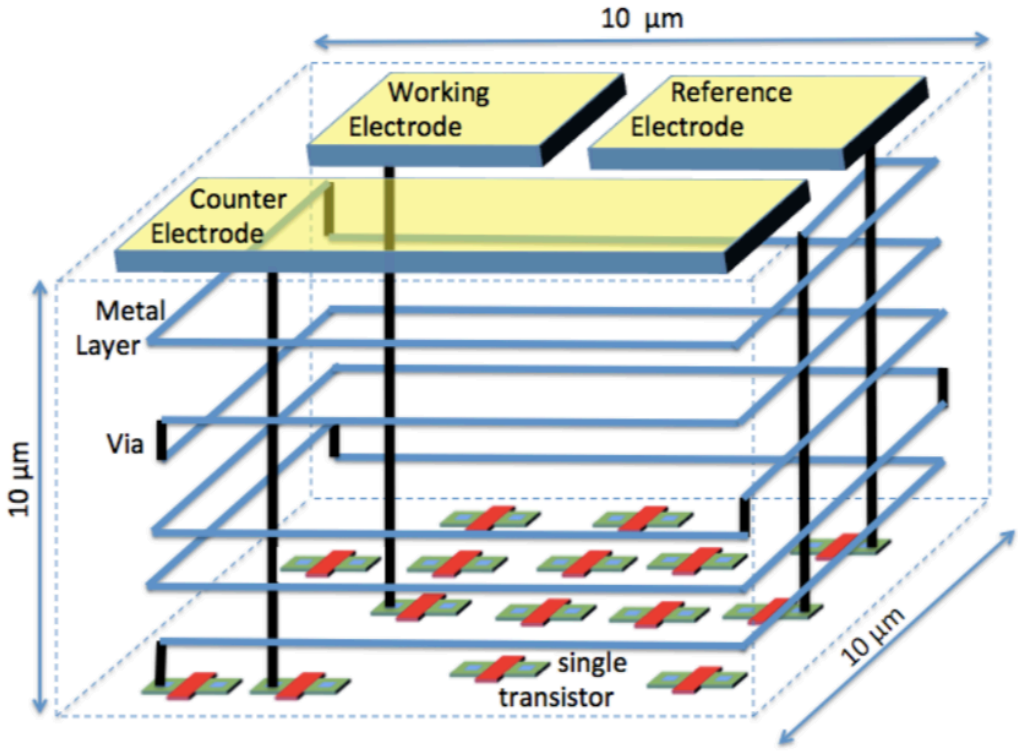


Figure 2.2 First prototype of Body Dust cube; reprinted with permission from [2.1]

2.1 STATE-OF-THE-ART

In this section I want to present the main work done in the development of the body dust design: from the first idea of a Bio/CMOS integrated circuit for biosensing, through the Drinkable Diagnostic till the layer architecture of the Budy Dust cube and the brief presentation of the communication system developed for transmitting signals outside the body.

2.1.1 STATE-OF-THE-ART: FIRST ARCHITECTURE

In literature the first step in the "Body Dust" project proposed an architecture that tried to accomplish a cube design with self-forming, self-localization, and diagnostics capability. In particular to constitute the system on-chip, in charge of the sensing, the following main blocks were identified: a transimpedance amplifier (TIA), a potentiostat, a rectifier, a ring oscillator and a three electrodes set (reference electrode, working electrode and counter electrode), as shown in the following Figure 2.3.

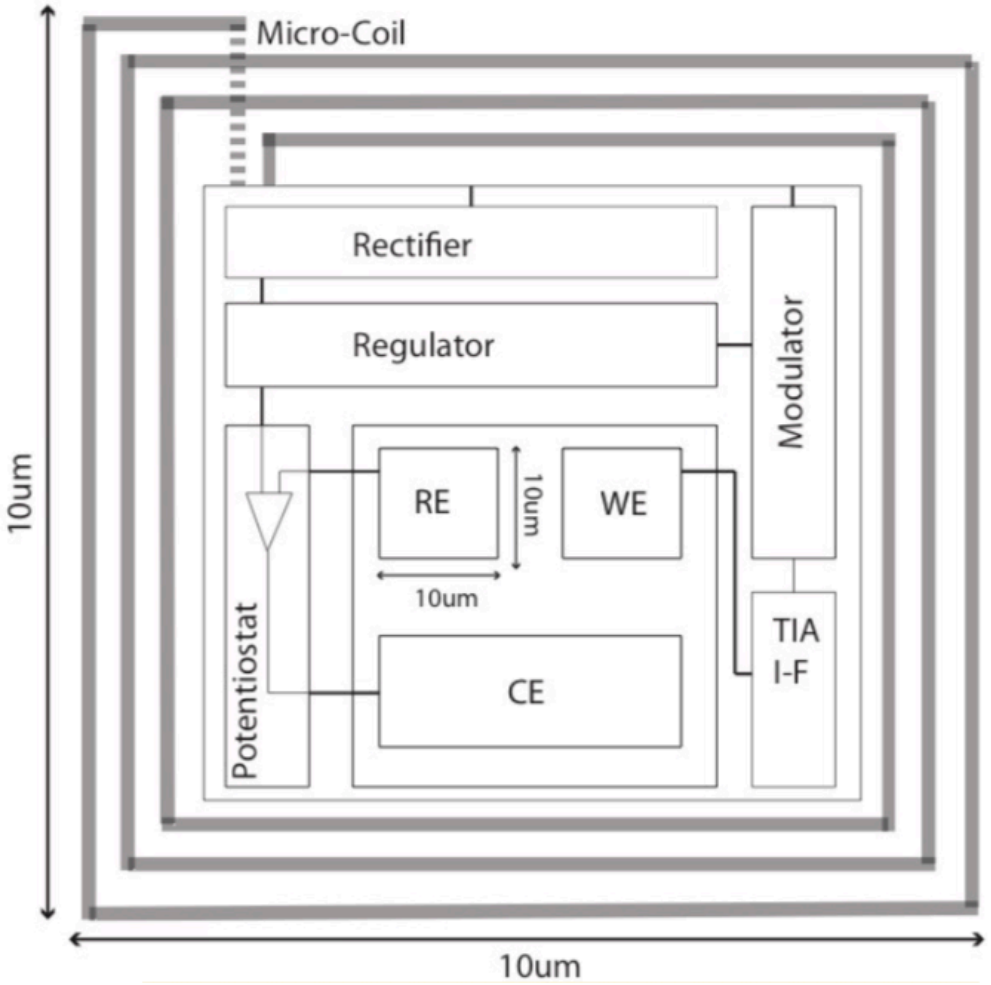


Figure 2.3 First architecture of the front-end for the "Body Dust"; reprinted with permission from [2.1]

One of the most used method for biosensing applications is the amperometric one which exploits a redox reaction to generate a current proportional to the concentration of a specific biological target. In the previous design a potentiostat, with sufficient bandwidth to perform cyclic voltammetry, is used to apply a stable voltage to a reference electrode (RE) in order to generate a current that can be measured through a working electrode (WE). For reading this measurement is used a transimpedance amplifier (with high gain, low noise, high dynamic range) which converts the current into a voltage. A controlled ring oscillator is then used to convert the sensed current from the TIA into a frequency-modulated signal, which drives the transmission coils through backscattering. In the end a power rectifier to extract power and generate a regulated supply from the signal received by the coils is used. On the top of such CMOS die, an array of aluminum electrodes is formed in order to realize the proper electrodes, which allows the platinum deposition.
Starting from what just explained [2.5] further studies were launched toward drinkable diagnostic, like the system that will be now briefly discussed.

2.1.2 STATE-OF-THE-ART: GLUCOSE SENSING

A compact architecture in CMOS, using a UMC 180 nm, to interface a glucose biosensor was proposed in [2.6]. It consists in: an AC to DC rectifier, a band-gap reference, a voltage regulator, a potentiostat, a I to f converter, a pulse generator and a back-scattering unit (Figure 2.4).

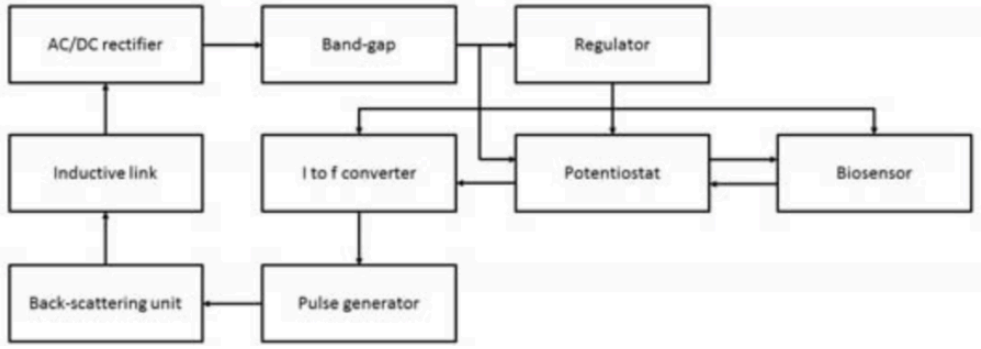


Figure 2.4 Glucose sensing system block diagram; reprinted with permission from [2.6]

The aim was to study the feasibility to realize a system with minimum area and low power consumption, so each block of the circuit was optimized by keeping into consideration these two boundaries. The most critical elements for the total size of the model are the current to frequency converter and the rectifier. The first one was implemented using a ring oscillator, whose frequency change according to the well-known equation:

$$f = \frac{I}{N * C_{tot} * V_{DD}} \tag{2.1}$$

Where N is the number of stages of the ring oscillator, C_{tot} the total capacitance of each stage and I the total current in each stage.
The rectifier was implemented using a four-diode bridge with an added capacitor at the input of the rectifier itself, representing the most critical part in term of area (10 fF of capacitance corresponds to 6.4 μm^2 while 25 fF, more suitable for this application, takes around 25 μm^2).
About the power consumption the voltage regulator is the costliest, even if it represents the right compromise between area and power consumption for this application: a high supply voltage can not be chosen because of the area occupied, while a too low value would impact on the gain of the transconductance amplifier.
All the information about the circuit's block are summarized in the following Figure 2.5 and Table 2.1.

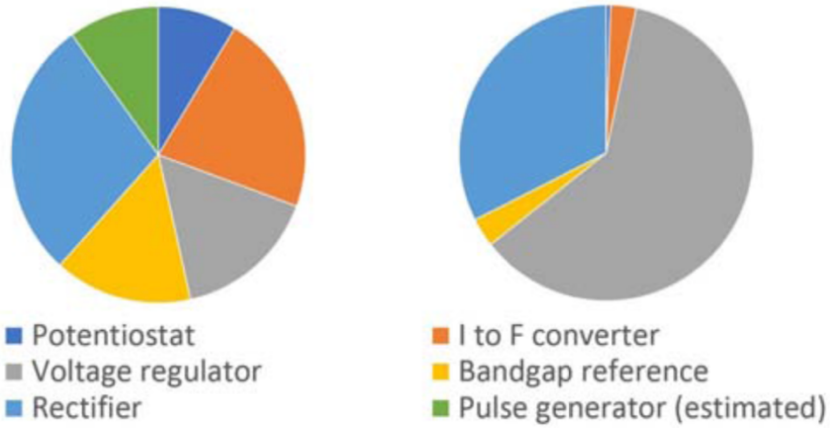


Figure 2.5 Best case of total area (left) and corresponding power consumption (right); reprinted with permission from [2.6]

	Area [μm^2] (best case)	Power [μW]	Power [μW] (best case)	Area [μm^2]
Potentiostat	8.7	0.141	0.124	12
I to f conv.	22	0.836	0.836	22
Rectifier	28.44	9.655	9.655	28.44
Voltage regulator	15.9	18.170	5.7	24
Band-gap ref.	15.2	0.939	0.939	15.2
Pulse generator	10	—	—	10
Total	100.24	29.741	17.254	111.64

Table 2.1 Total area and power consumption; reprinted with permission from [2.6]

The approach studied in this research considered the analysis of only one component, the glucose, so that after the measure of its concentration the corresponding signal would be sent outside the body through backscattering. A more complex architecture for the "Body Dust" implementation considers a 3D CMOS integration in order to have the third dimension of the cube and so dividing the work into different layers of integration. In this way it's possible to imagine this configuration as formed by different biosensors working together for a common goal. According to this idea instead of a single functionalization now we can have a multiplexing layer that can switch from one channel to another, allowing the measurement of different biomolecular concentrations. All the signal derived from the multiplexer are then sent outside the body through a communication circuit that, as well as the power management, will use a US wave to receive power and transmit data.
So the [2.6] was the first attempt to realize a micro-sensing system but also the starting point for future drinkable diagnostic, setting the two boundaries that will represent the main problem in the development of the disclosed 3D model of the "Body Dust".

2.1.3 STATE-OF-THE-ART: COMMUNICATION SYSTEM

Starting from the idea of an implementation with 3D CMOS integration a research for the design of the communication layer was conducted in [2.7]. In particular it was studied the feasibility of an UltraSound (US) communication circuit to wireless transmit information outside the body: the sensing-chip in connected wirelessly to an external base station through an US system and the in-body biochip needs to answer by reflecting back a portion of the incoming wave by backscattering modulation.
In the design of this circuit the two main boundaries were again the total lateral area (less than 100 μm^2) and the overall power consumption.
This communication circuit was design as in the following Figure 2.6.

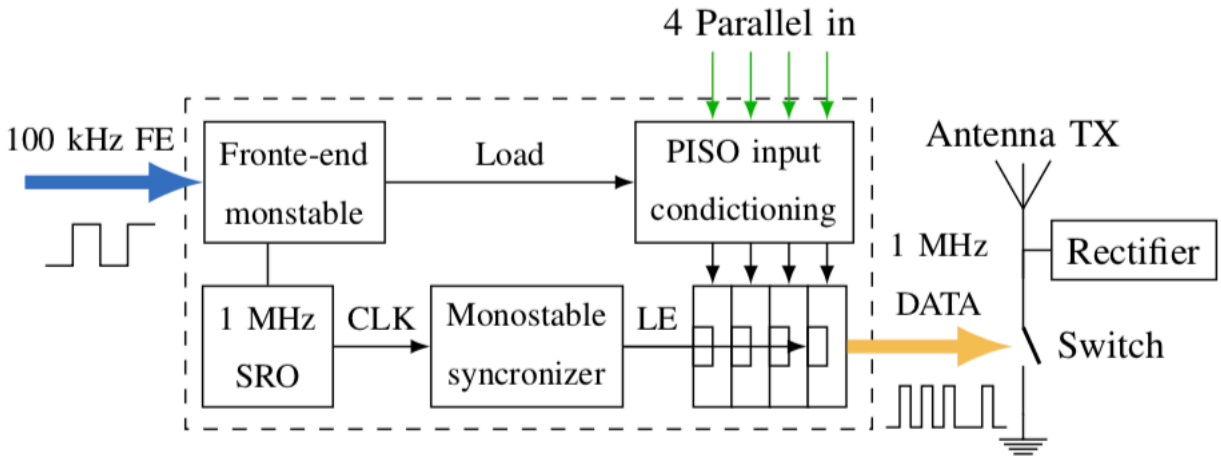


Figure 2.6 Communication circuit block diagram; reprinted with permission from [2.7]

It consists in a front end monostable that receives the FE signal and whenever a rising edge is detected a pulse is generated. A Starved Ring Oscillator (SRO) which provides a 1MHz data. It is one of the most critical elements in the circuit because is realized using three equal capacitors whose value was define with the final aim of occupy less area as possible but still of 0.00116 mm^2, and its power consumption is more than 95% of the total averaged value. The PISO register is composed of four D-latches triggered by a Letch Enable (LE), generated by the monostable synchronizer, and the minimum transistor's sizes provided by the Process Designed Kit (PDK), again to optimize the area. The transmitted data packet from the register is composed by a header (bit 1 always) to declare the starting of the transmission, and three for the signal address which are the minimum to distinguish all signals derived from a multiplexing layer conceived to switch among five different channels. In the end an On-Off Keying modulator is implemented using a nMOS as a switch (Figure 2.7): when the switch is open, Rm is equal to Rp, and the full matched condition is achieved, while when the switch is closed Rm is equal and the mismatched condition is realized.

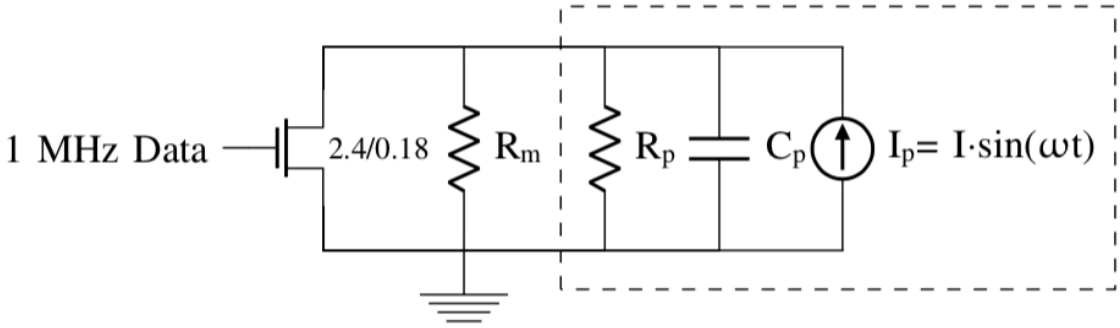


Figure 2.7 Electrical model of the piezo and incident wave and nMOS switch; reprinted with permission from [2.7]

This new architecture for a communication system in the Body Dust diagnostic demonstrates the feasibility to design a data transmission US transponder, in UMC 180nm, with an averaged power consumption less then 10 μW and a total chip area of 43X44 μm^2 (Figure 2.8).

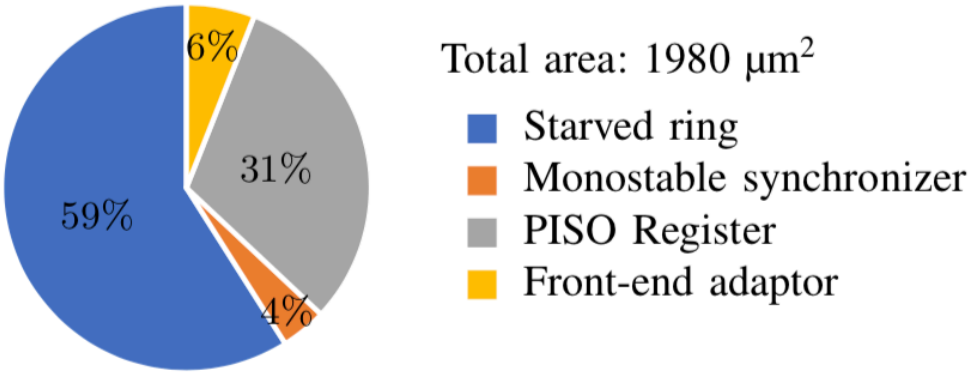


Figure 2.8 Total area of each block of the circuit; reprinted with permission from [2.7]

2.2 MULTIPLEXING LAYER

Starting from the proposed architecture of the communication layer in [2.7] I started my work with the aim to implement a multiplexer circuit that can interface the blocks already designed. So, the starting point was to create a circuit that can manage five channels, each of them functionalized for the recognition of different biomolecules, and in the end provides the information needed by the communication layer to transmit the data packet. As it was for all the previous researches presented, also in this case the final design should follow the boundaries of lateral area and power consumption, with the addition of a sub-Hz frequency limit.
In this thesis I will investigate the possibility of a design for the multiplexer circuit with aim to compromise between area and frequency.

2.2.1 PROPOSED DESIGN

First of all for the realization of the multiplexing circuit it was necessary to keep into consideration that, for how the 3D CMOS Body Dust was conceived, there should be interaction among different layers, this means that the information derived from the multiplexer will be sent to the communication circuit in order to be transmitted outside the body. In particular, these information are: the biomolecular concentration measurement and the three bits necessary to distinguish the signal address.

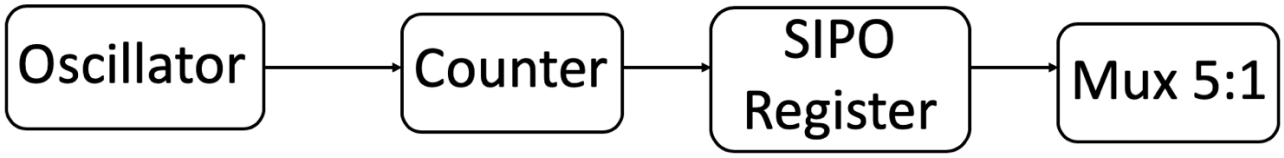


Figure 2.9 Diagram block for the multiplexer

According to all of that, the multiplexer design created for this application is the one summarized in the diagram block of Figure 2.9:

- Oscillator: as I want to control five different channels the multiplexer needs to switch from one to another according to a known frequency fixed by an oscillator. Because of the interaction between the multiplexing layer and the communication circuit it could be even possible to use a common oscillator for the both of them.
- Word Generator: which is a counter (Figure 2.10), so a sequential digital circuit that can count a certain number of events depending on a clock signal. For this application I decided to use three flip-flop JK in series, each of them triggered by a different clock, realizing an asynchronous counter. This one generates a binary "word" to control the multiplexer. The circuit is simulated through a transient analysis and the result is shown in Figure 2.11.

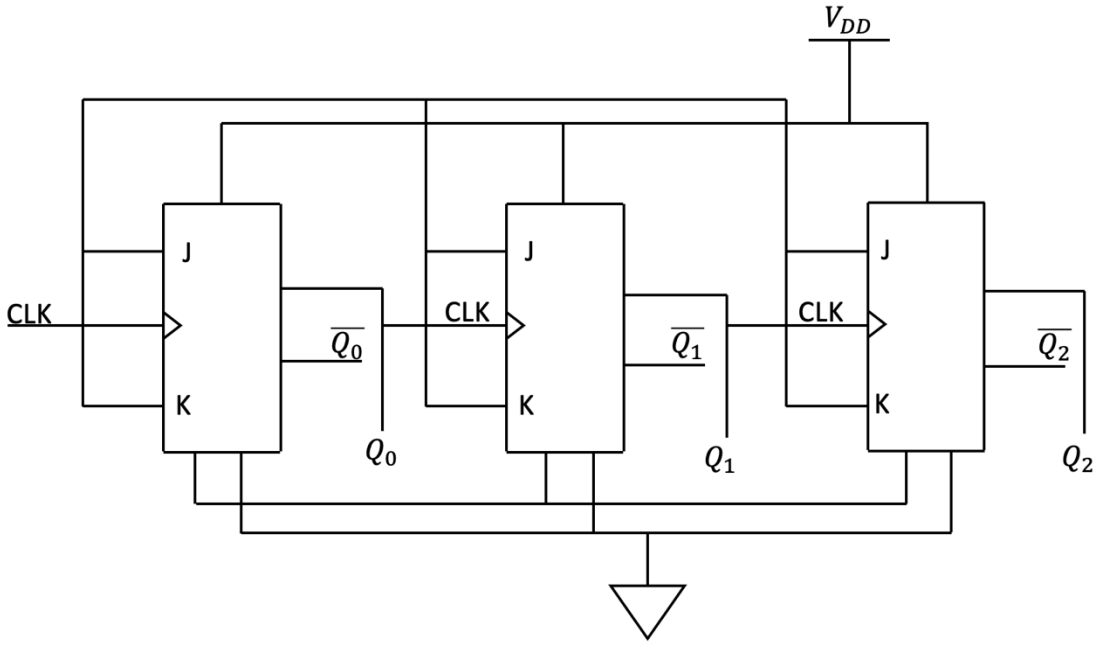


Figure 2.10 Asynchronous Counter schematic implementation

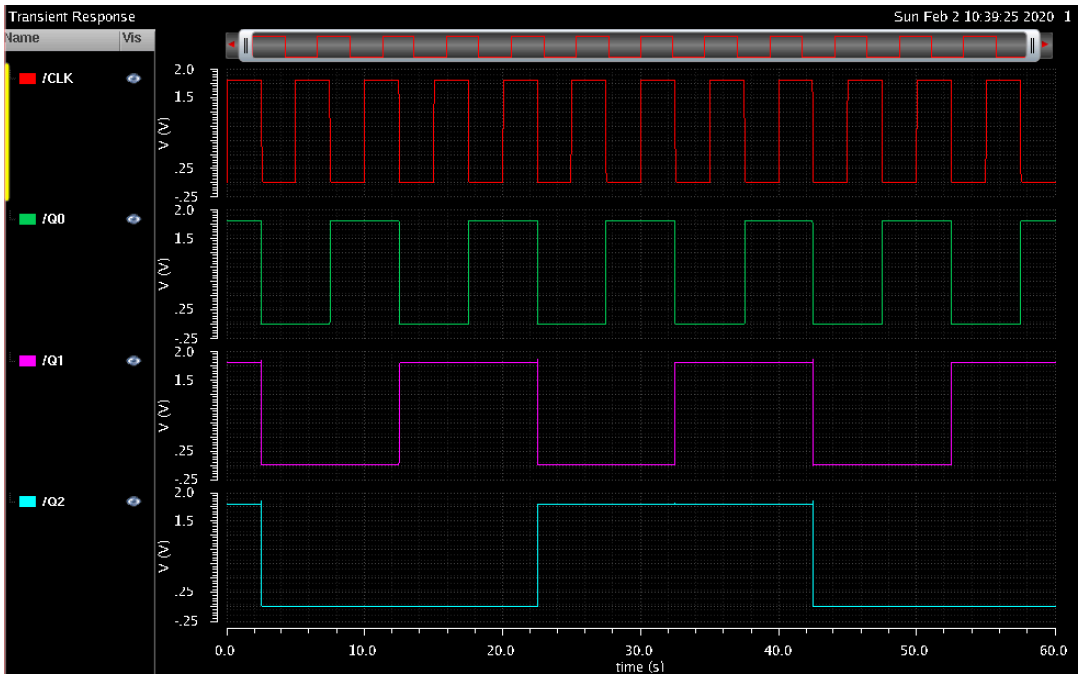


Figure 2.11 Transient Response of asynchronous counter

This configuration is then adapted to the aim of the circuit: the word generator has to count only until the number of channels the multiplexer needs to manage, every time the counter reaches "101" a clear signal allows to reset the count and restart from the beginning.

- SIPO Register: a shift register, so a cascade of N flip-flop that can shift a digital word every rising/falling edge of a shared clock signal. The output of the counter is a serial sequence of bits which have to be transformed to a parallel word before being sent to the mux, from here the necessity to use a SIPO register. It is implemented using three flip-flop D (Figure 2.12) with a common synchronizing signal.

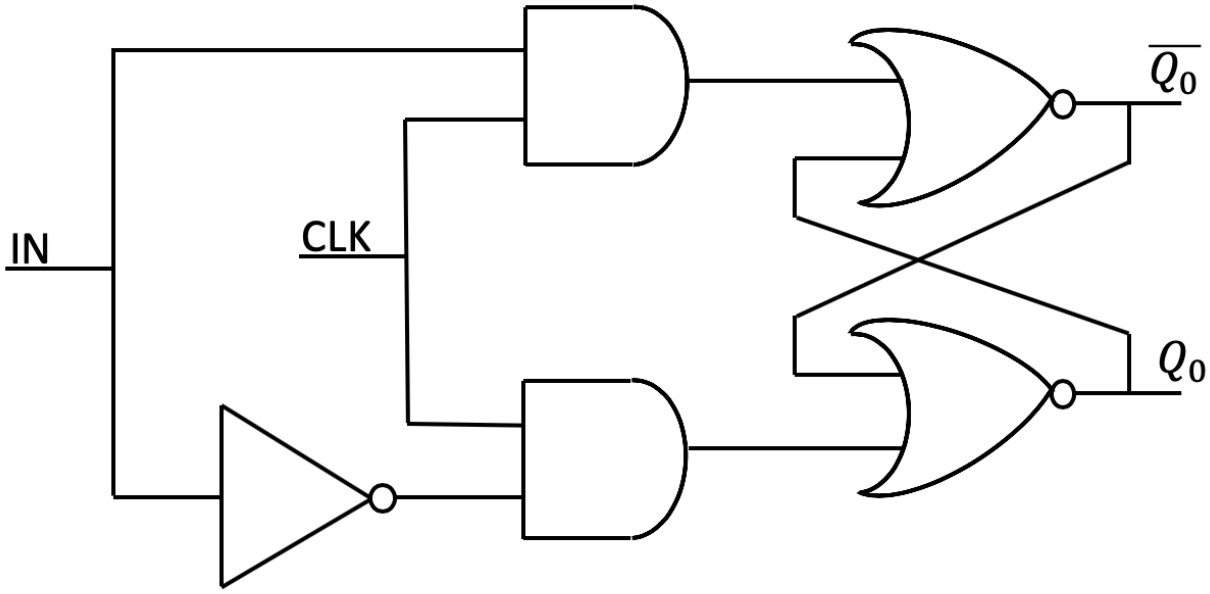


Figure 2.12 Schematic design of Flip-Flop D

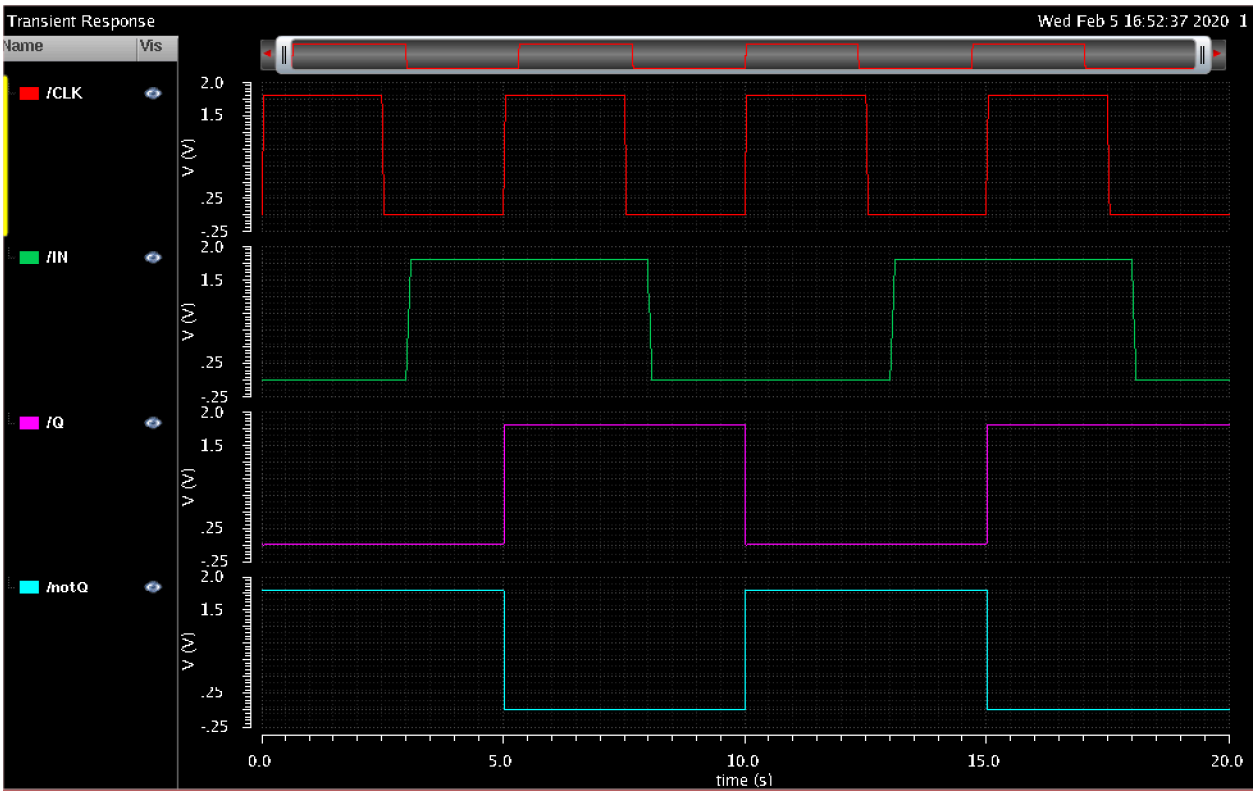


Figure 2.13 Transient Response of flip-flop D

The configuration of the register and its transient response are shown in Figure 2.14 and Figure 2.15.

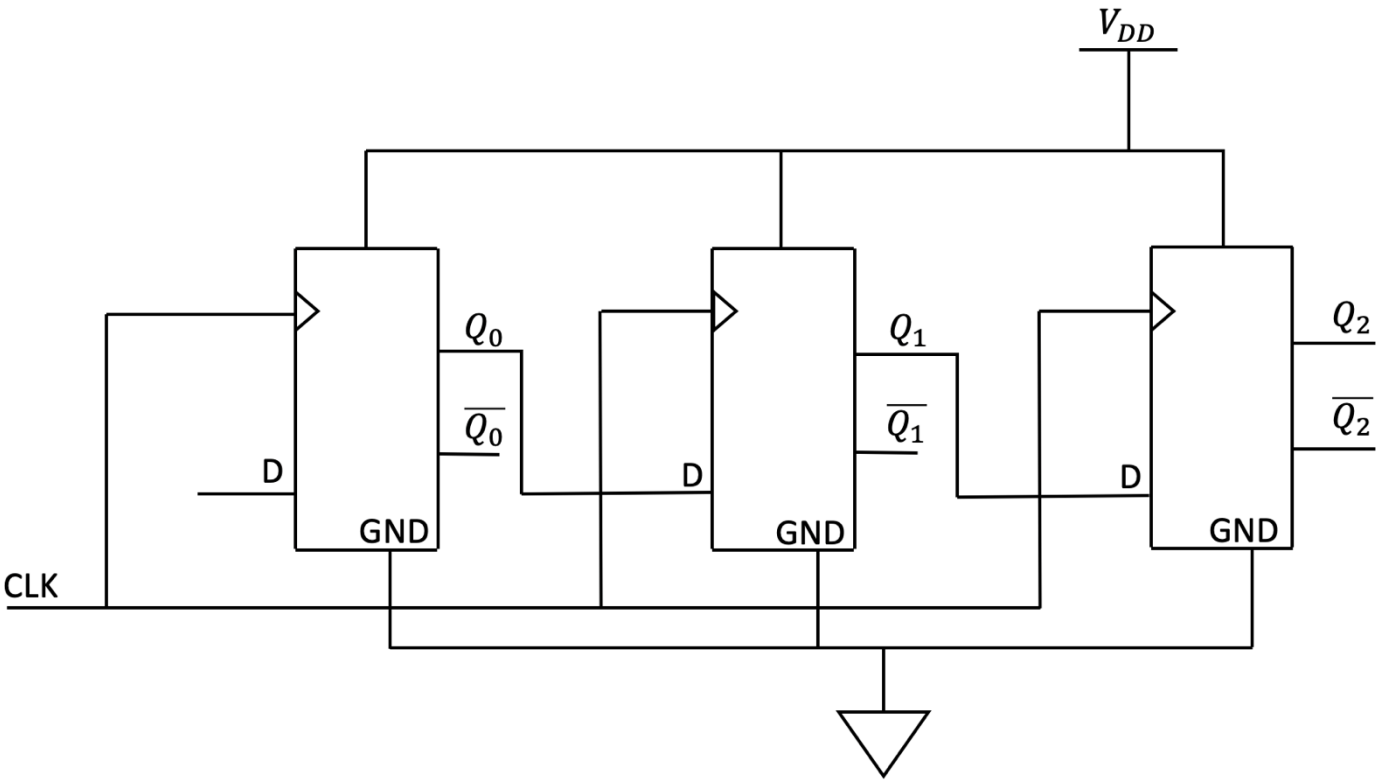


Figure 2.14 Schematic design of SIPO Register

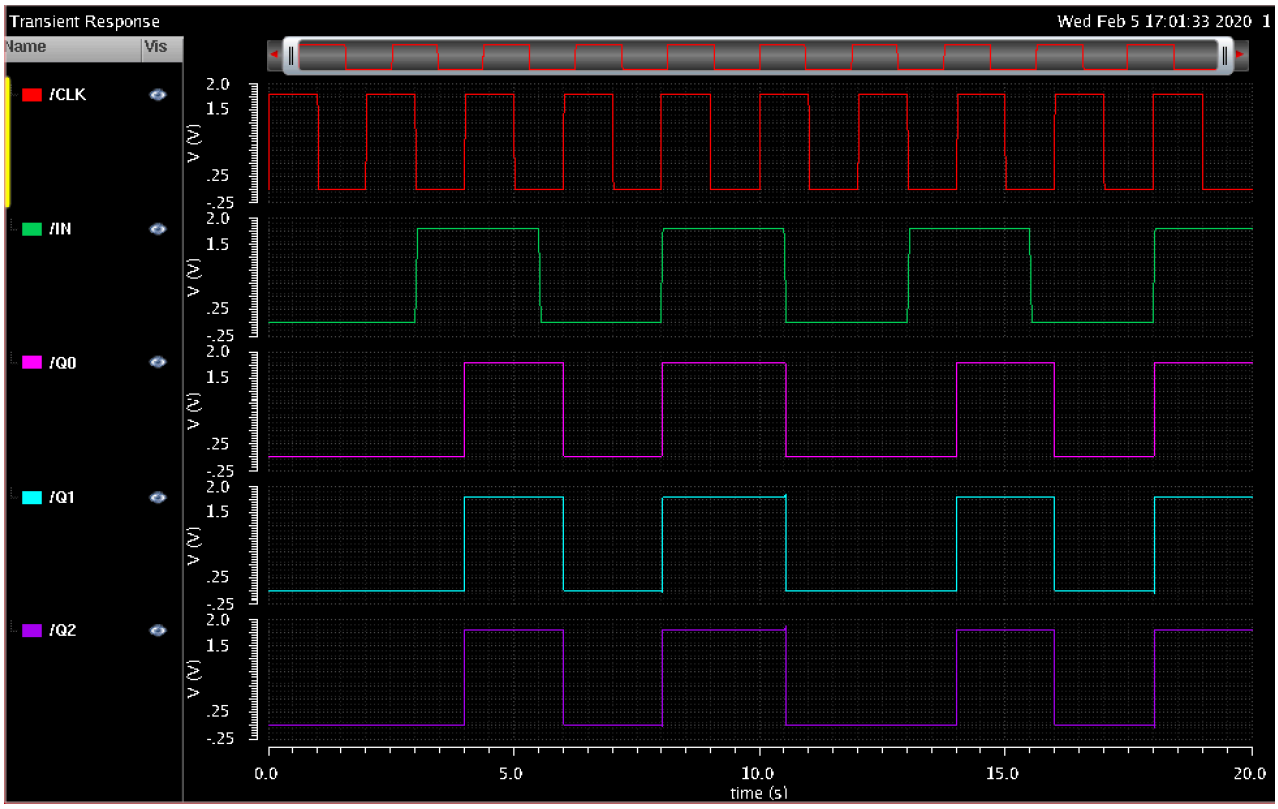


Figure 2.15 Transient Response SIPO register

- Mux 5:1 : It take the 3 bits parallel word from the register and selects the corresponding channel. For its implementation I used simple mux 2:1 to realize the configuration in Figure 2.16.

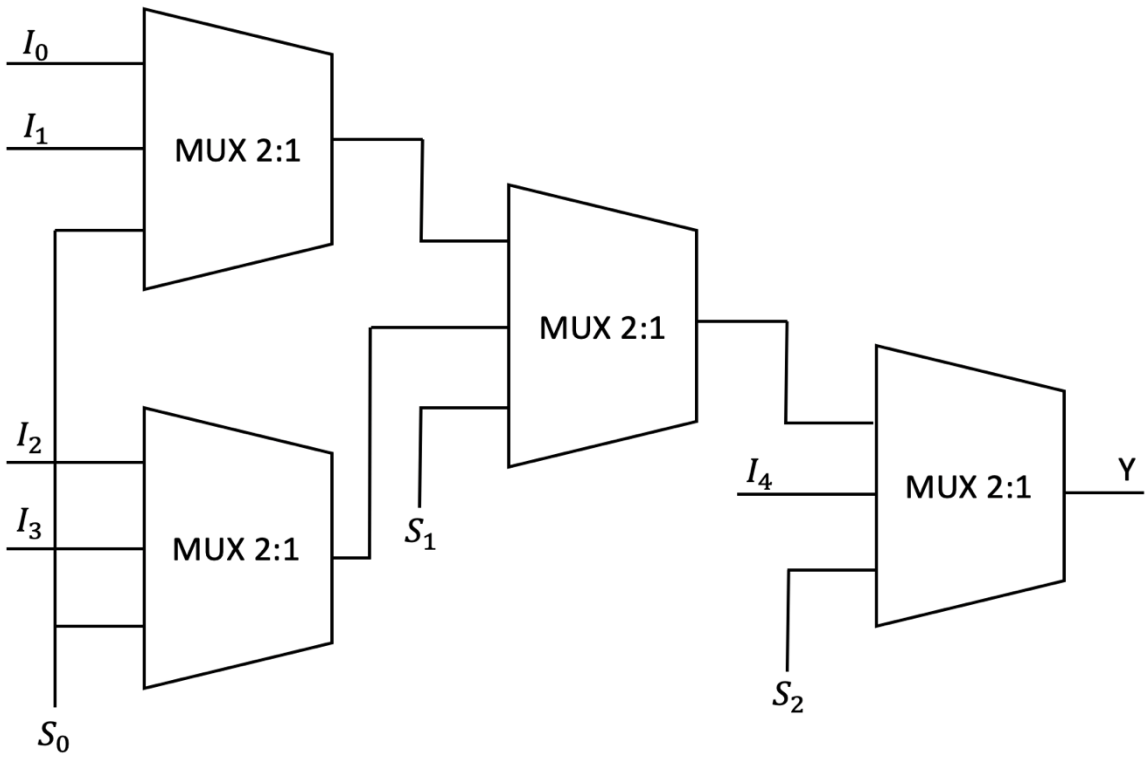


Figure 2.16 Schematic representation of mux 5:1

According to the input received in S_0, S_1, S_2, the output will be the incoming signal from one of the five channels (I_0, I_1, I_2, I_3, I_4). An example is shown in the Figure 2.17 below in which the digital input word "000" forced the output Y to correspond to I_0.

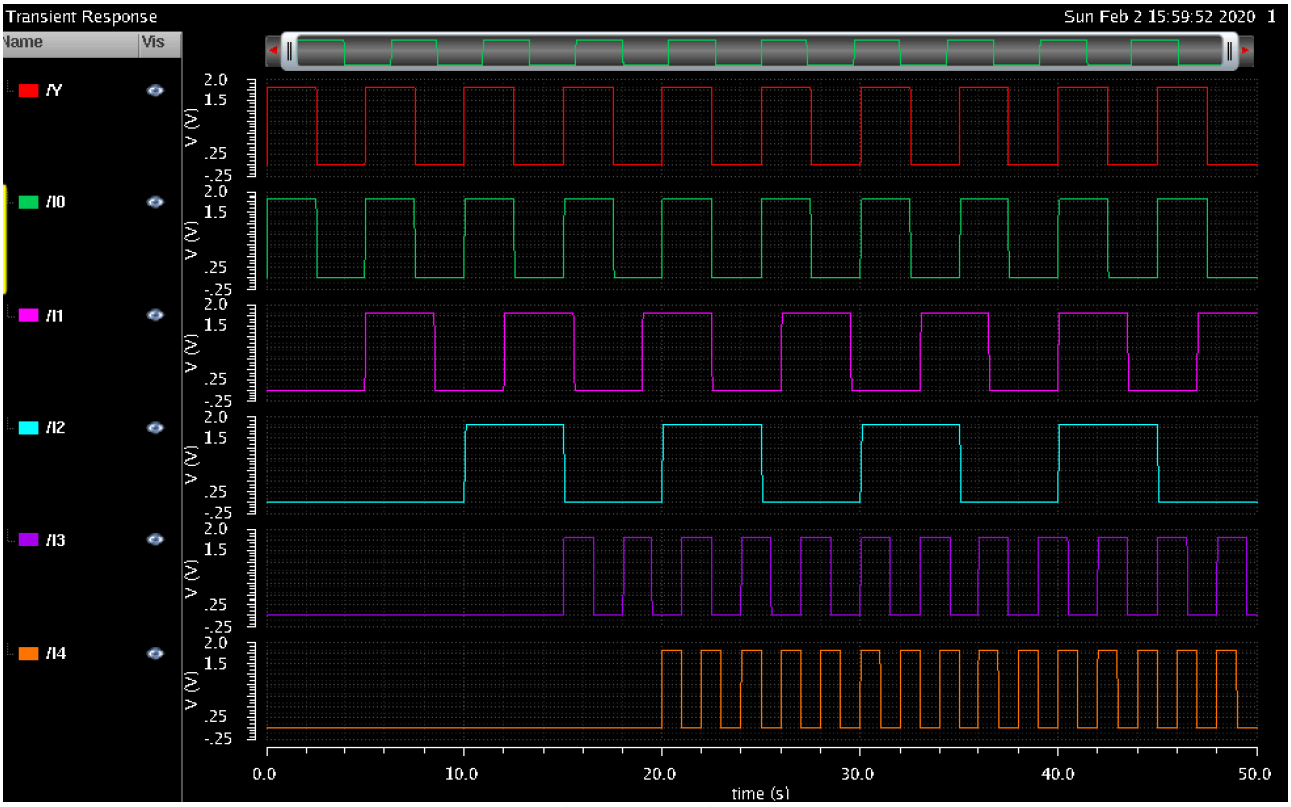


Figure 2.17 Transient Response of the mux 5:1 after applying the parallel input "000"

2.2.2 CHALLENGES

This is a possible way to design the multiplexer circuit required for the Body Dust but there was a main problem that I had to faced: according to the aim of the project millions of nanoparticles, after being drunk by the patient, should give information about the concentrations of both endogenous and exogenous entities; to do that voltammetry and chronoamperometry techniques have to be performed, according to what biomolecules are analyzed. This is exactly where the problem born: in the next section these two techniques will be explained in more detail but the key point is the time necessary to perform them, which require the multiplexer to stay fixed on each channel for minutes and so to have an oscillating frequency in the range of sub-Hz.
From this point on the main goal of my thesis became to find a proper solution to reach the wanted frequency, following an analog path, that observe the boundaries of area, power consumption and frequency.

2.3 CHRONOAMPEROMETRY & VOLTAMMETRY

There are two commons techniques used to measure the concentration of biomolecules: chronoamperometry and voltammetry.
The first one is an electrochemical, time-dependent technique in which a square wave potential is applied to a working electrode. Thanks to a redox reaction is produced a current which can be measured as a function of time and fluctuates according to the diffusion of an analyte from a bulk solution toward a sensor surface.
This process is described by Cottrell equation which explains the change in electric current, with respect to time, in a controlled potential experiment. Specifically, it describes the current response when the potential is a step function, according to the following (2.1):

$$i = \frac{n * F * A * c_j^0 * \sqrt{D_j}}{\sqrt{\pi * t}} \tag{2.2}$$

Where:
i = current, in unit A
n = number of electrons (to reduce/oxidize one molecule of analyte j, for example)
F = Faraday constant, 96485 C/mol
A = area of the (planar) electrode in cm^2
cj0 = initial concentration of the reducible analyte j in mol/cm^3;
Dj = diffusion coefficient for species j in cm^2/s
t = time in s

Sometimes deviations from linearity in the plot of i vs $\sqrt{t}$ can indicate that the redox event is associated with other processes, such as association/dissociation of a ligand, or a change in geometry. In practice, the Cottrell equation is simplified to (2.2):

$$i = k * t - \frac{1}{2} \tag{2.3}$$

where k is the collection of constants for a given system (n, F, A, cj0, Dj).
Chronoamperometry is performed like follows: the potential is held constant for a certain time (for example 100 ms) during how the oxidation at the electrode produce an oxidation current. After this the potential is lead to a resting value (around 0 V) so that a reduction can be performed, producing a reduction current. This means that a square wave pulse (Figure 2.18) is applied at the working electrode and usually it is repeated multiple time for second, with measurements made at the same time (steady state) during each of the voltage pulses. Because the applied voltage is held at a constant potential and is instantaneously ramped up from the resting value, the measured current is directly proportional to the concentration of the species electrolyzed, and the electrode is sensitive to rapid changes in concentration.

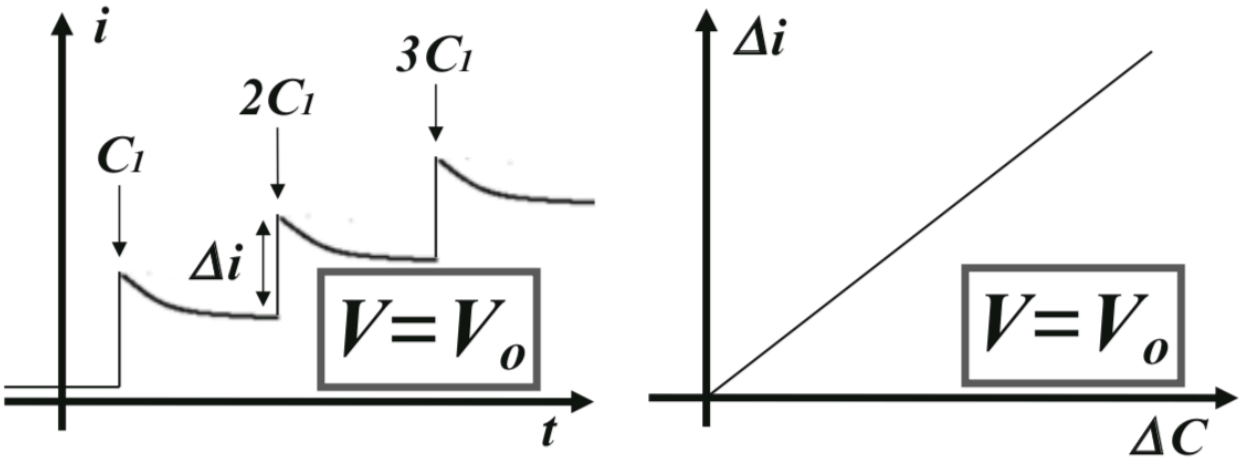


Figure 2.18 Chronoamperometry at fixed potential

The second technique commonly used to make this type of measurement is the voltammetry. There are different kind of voltammetry techniques, and each of them is based on the fact that the current flowing through the system is a function of a potential applied across the electrodes. A few examples are: cyclic voltammetry, based on a voltage scan (triangular wave) toward positive and then negative potentials to a stationary electrode submerged in a stable solution (Figure 2.19), with continuous acquisition of current, or the linear sweep voltammetry, in which the potential of the working electrode changes in a linear way during the experiment (Figure 2.20).

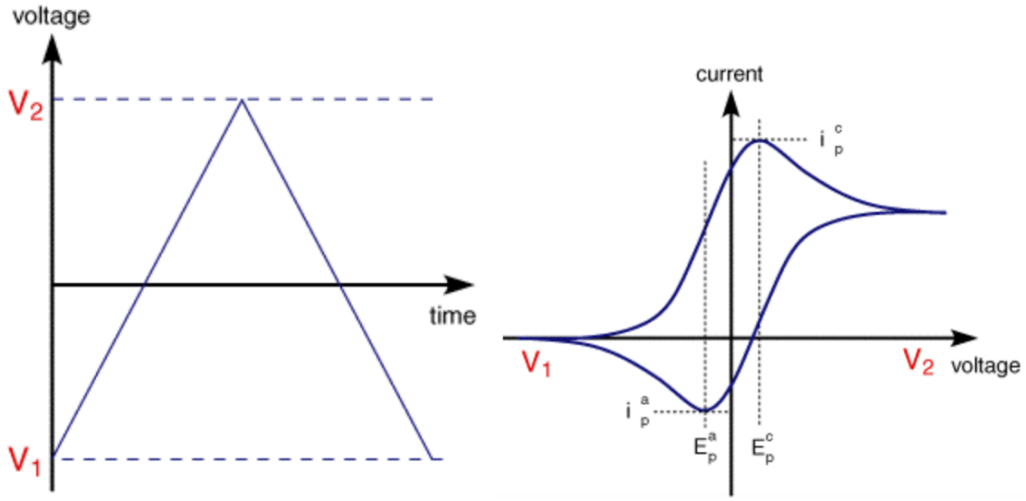


Figure 2.19 Triangular wave potential applied to the working electrode during cyclic voltammetry (left), wave response of the current of the input potential (right)

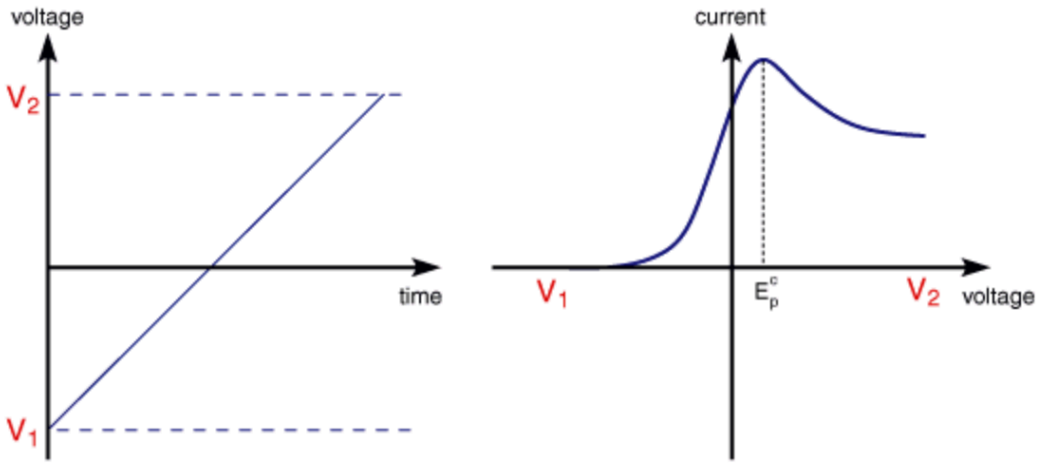


Figure 2.20 Linear change of potential applied to the working electrode during linear sweep voltammetry (left), wave response of the current of the input potential (right)

These processes are based on a well-known chemistry law. In fact, from the literature of equilibrium electrochemistry is known that the Nernst equation (4) relates the reduction potential of an electrochemical reaction to the standard electrode potential, temperature, and activities of the chemical species undergoing reduction and oxidation, giving the position of the oxidation/reduction peaks by metabolite concentration:

$$E = \frac{RT}{zF} \ln \frac{[\text{ion outside cell}]}{[\text{ion inside cell}]} = 2.3026 \frac{RT}{zF} \log_{10} \frac{[\text{ion outside cell}]}{[\text{ion inside cell}]} \qquad (2.4)$$

Where:
R = ideal gas constant (mol*m^3)
T = temperature (K)
z = charge of the ion
F = Faraday's constant (C*mol)

The cyclic voltammetry is useful if there are redox reaction of metabolites that have never been characterized, because gives the potentials at which oxidations and reductions occur. These potentials are respectively called: oxidation potential and reduction potential, and the half-difference between the two of them is called standard potential (in dependence of the surface of the reference electrode).
Therefore, the experimental setup for linear sweep voltammetry uses a potentiostat and a three-electrode setup (working, reference and counter electrode) to deliver a potential to a solution and monitor its change in current. The working electrode (WE) is the one at which the redox occurs and the process is monitored.
After the redox reaction is performed and some molecules on the surface of the WE are oxidized/reduced, so they move away from its surface, new molecules come into contact with the WE. This flow of electrons generates a current, which is a direct measure of the rate at which electrons are being exchanged through the electrode-electrolyte interface. When it became higher than the rate at which the oxidizing or

reducing species can diffuse from the bulk of the electrolyte to the surface of the electrode, the current reaches a plateau or exhibits a peak.

CHAPTER 3

CMOS DESIGN

Starting from this chapter on, I will present the work done to reach the main goal of this master thesis, so the feasibility study to implement an analog oscillator able to generate a sub-Hz frequency and occupies a total area of 10X10 μm^2.
In particular, four configurations were analyzed and all of them were implemented using the software "Cadence Virtuoso IC6.1" in UMC 180 nm technology that, even if is relatively elderly, allows to test the defined limits of the circuit so that, after obtained the final architecture, it could be easy to reproduce it with lower technologies, improving its properties.
All the designer in CMOS environment needs to know the flowchart below (Figure 3.1), which shows the fundamental steps to follow. For my project I needed to respect what is surround by the red circle.

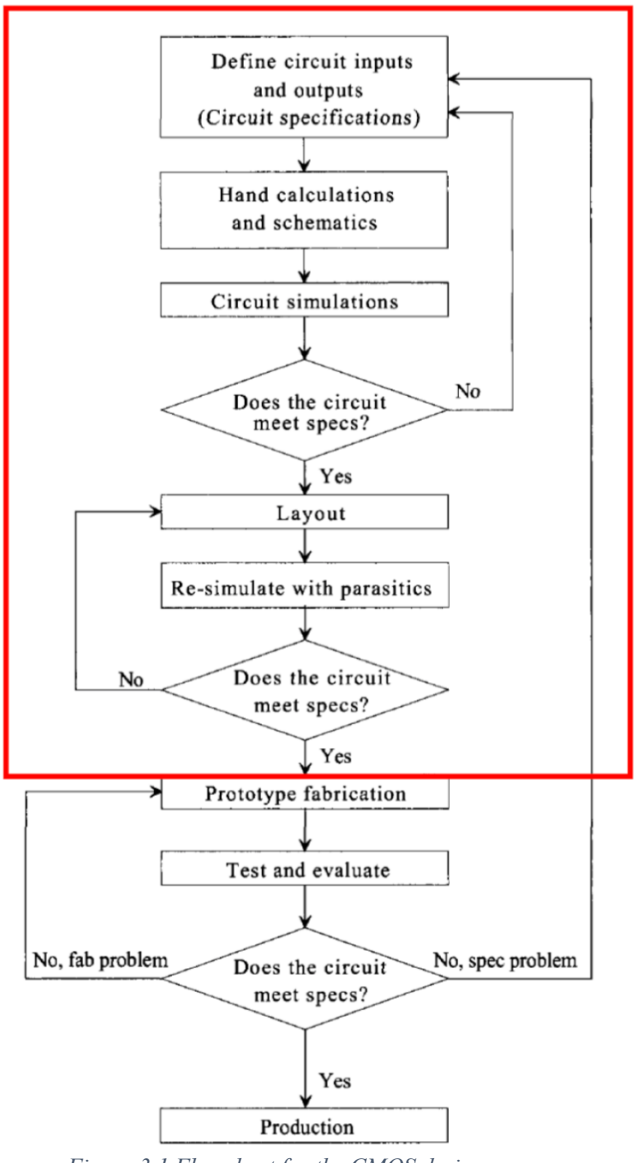


Figure 3.1 Flowchart for the CMOS design process

3.1 CADENCE LIBRARY

As a first step, some basic components are introduced here as fundamental building-blocks for the realization of each configuration I'm going to present: the logic gates. There are in particular, five components: inverter, NAND, NOR, AND, OR.

3.1.1 INVERTER (NOT)

The inverter is the simplest among all the logic gates, made using only a nMOS and a pMOS transistor (Figure 2.2), creating four pins: one input (in), one output (out), ground (GND) and the supply voltage (Vdd).

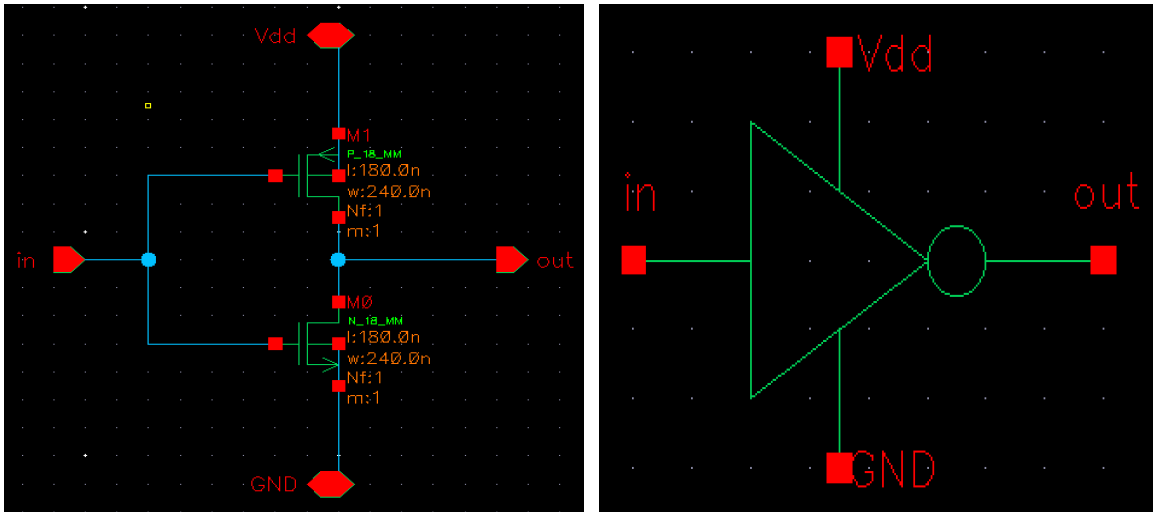


Figure 3.2 Schematic circuit of the inverter with p-MOS and n-MOS transistors (right) and symbol configuration (left)

This gate performs the logic operation of A to not(A) (Figure 3.3): when the input pin is connected to the ground the output is pulled to Vdd thanks to the p-MOS (M1) while, if the input is connected to the voltage supply, then the output is dragged to GND by the n-MOS transistor (M0) and M1 is shout off.

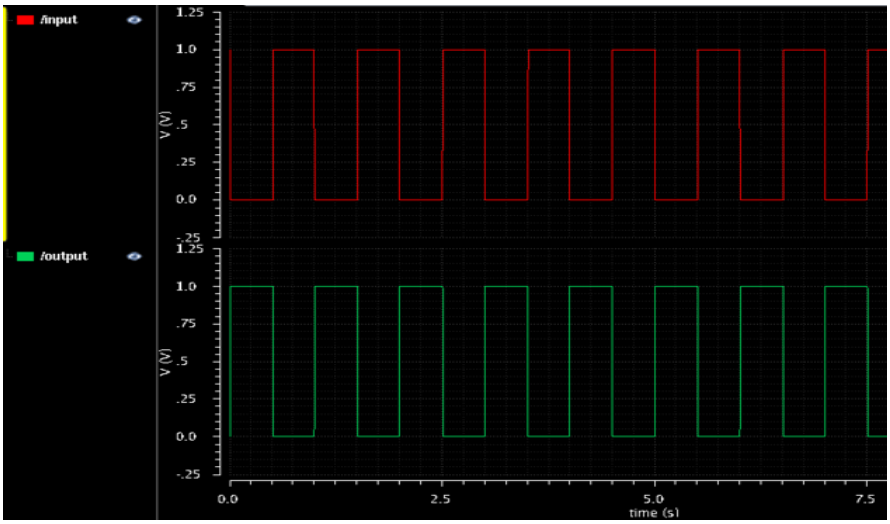


Figure 3.3 Transient response of the inverter

For all the logic gates I'm going to present, is important to remember that their components are not ideal and so the switching from high logic state (Vdd or 1) to low logic state (GND or 0) and vice versa, are time dependent. So, it is possible to describe the transfer characteristic, for example of the inverter, through its switching point (Figure 3.4).

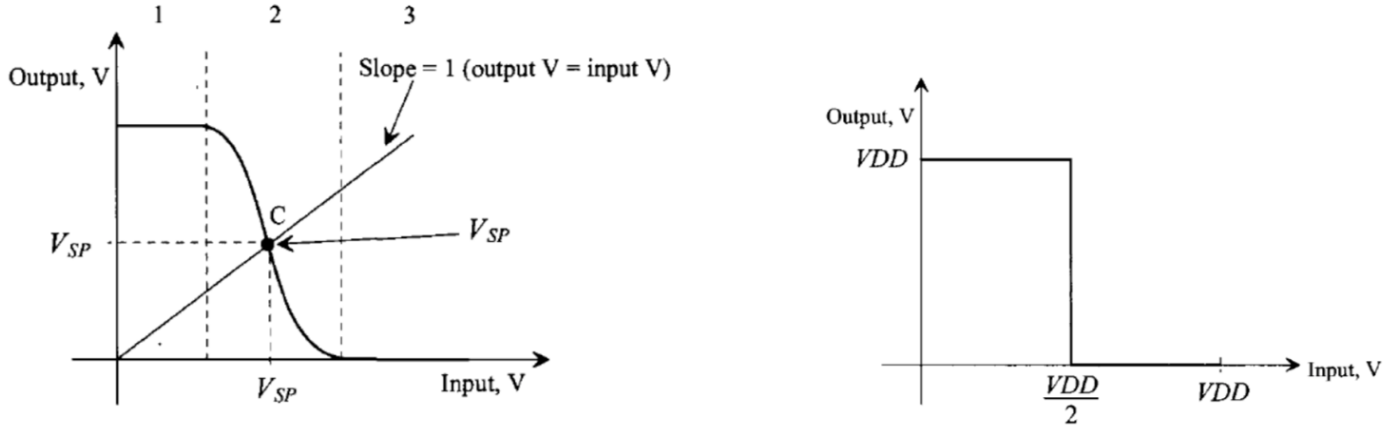


Figure 3.1 Real transfer characteristic of an inverter highlighting its switching point (right) ideal transfer characteristic of an inverter (left)

From the figure is noticeable that the wave transfer characteristic of the inverter can be divided in three parts:

- Region 1: pMOS is active while the nMOS is off
- Region 2: both the MOSFTEs are on
- Region 3: nMOS is on while the pMOS is off

C is the switching point of the inverter, here both pMOS and nMOS are in saturation region and ideally it is exactly half of Vdd supply voltage. In reality, it depends on many factors that cause its shift, modifying also the transition times from one logic level to the other.

Finally, the layout configuration was created using ME1 for metal connections (light blue) and PO1 (dark blue) for polysilicon connections. Two VIAs were also created: N-WELL implant for the voltage supply Vdd and P-WELL diffusion for the ground (Figure 3.5).

After designing the inverter layout, I used Assura in order to verify DRC (Drawing Rule Check) and LVS (Layout Versus Schematic). Then by running Quantus QRC, it was possible to extract all the parasitic capacitances (Figure 3.5) and so making another time the simulation in order to observe if the parasitic capacitances influence the functionality of the device. In particular, studying the extracted architecture is possible to highlight a few differences between pre- and post-layout simulations.

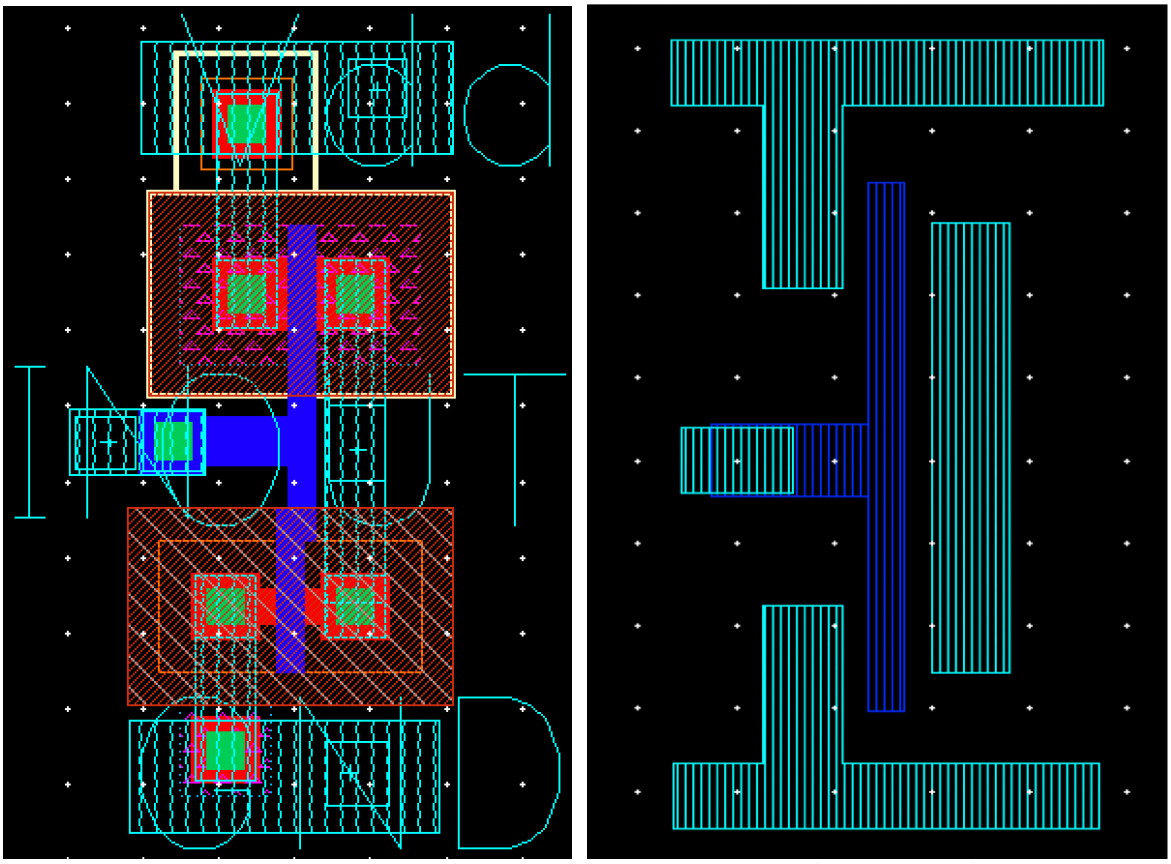


Figure 3.2 Layout design of inverter (right) and extracted view of the inverter (left)

3.1.2 NAND

The NAND gate here presented is formed by four transistors: two pMOS on the top and two nMOS below (Figure 3.6). The number of pins can change according to how many inputs the gate has, in fact it is possible to create NANDs port with 3, 4, 8 and so on inputs.

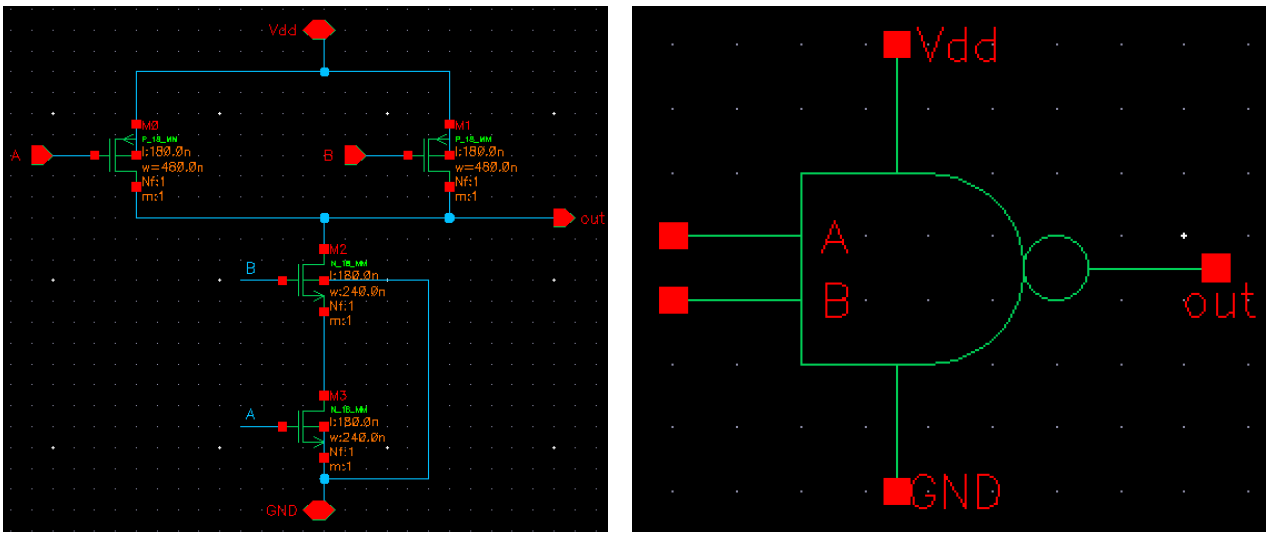
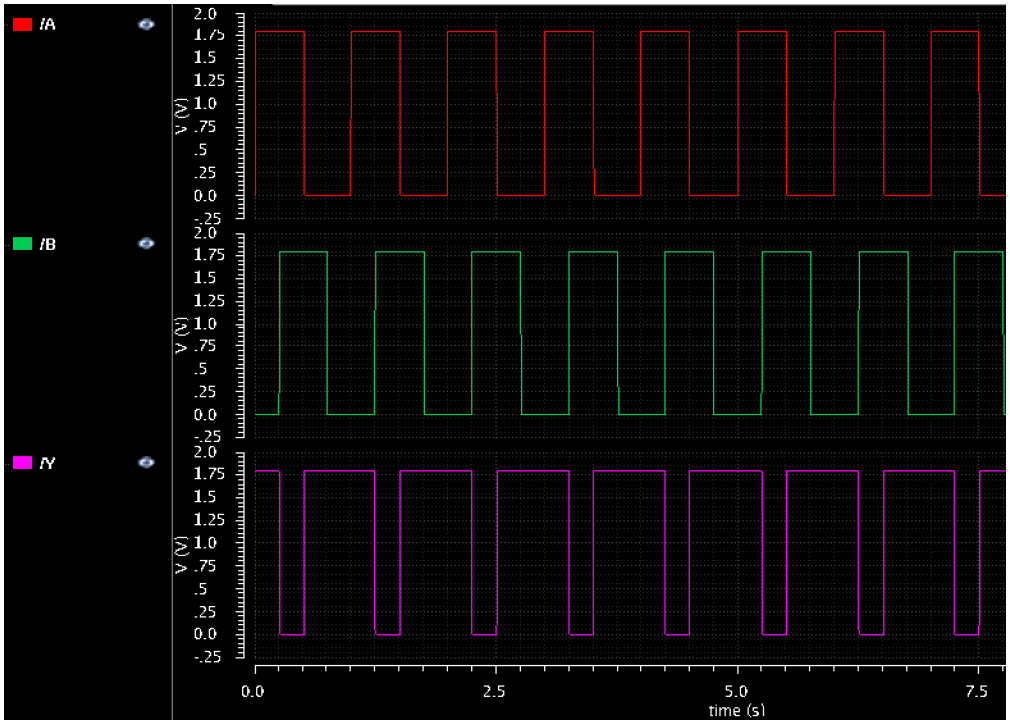


Figure 3.3 Schematic circuit of NAND gate with two input (right) and symbol configuration (left)

The gate performs the logic operation not (AB), following the truth table. The transient response was simulated using two square waves with period of 1s and mutual delay of 250ms (Figure 3.7).



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure 3.4 Transient response of NAND gate (right) truth table (left)

Finally, the layout and the extracted view are presented in the following Figure 3.8. Again, observing the extracted view because of the parasitic capacitances there are a few little differences between pre- and post-layout simulations.

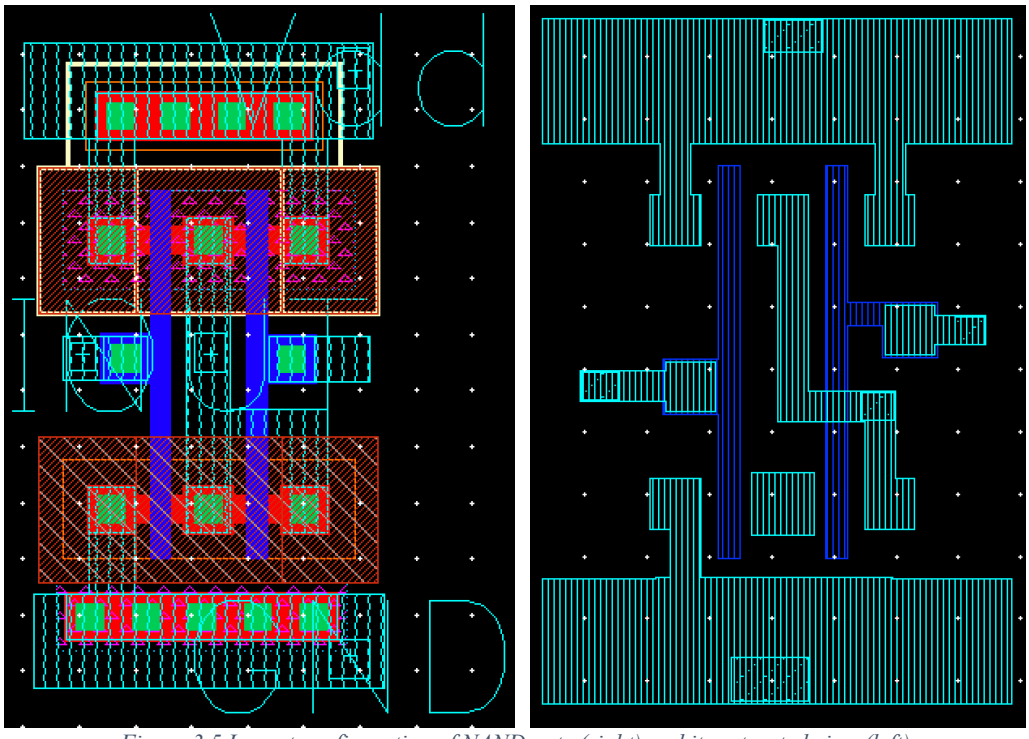


Figure 3.5 Layout configuration of NAND gate (right) and its extracted view (left)

3.1.3 NOR

The NOR gate here presented is formed by four transistors: two nMOS on the top and two pMOS below (Figure 3.9). Exactly like I explain for the NAND port the number of pins can change according to how many inputs the gate has.

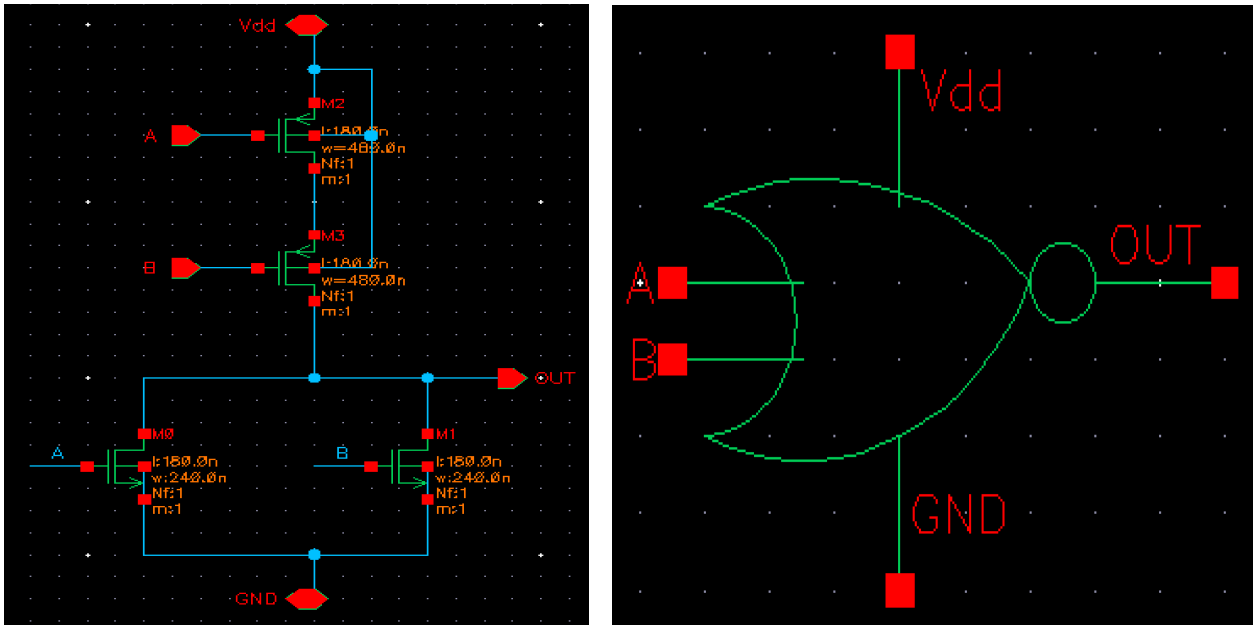
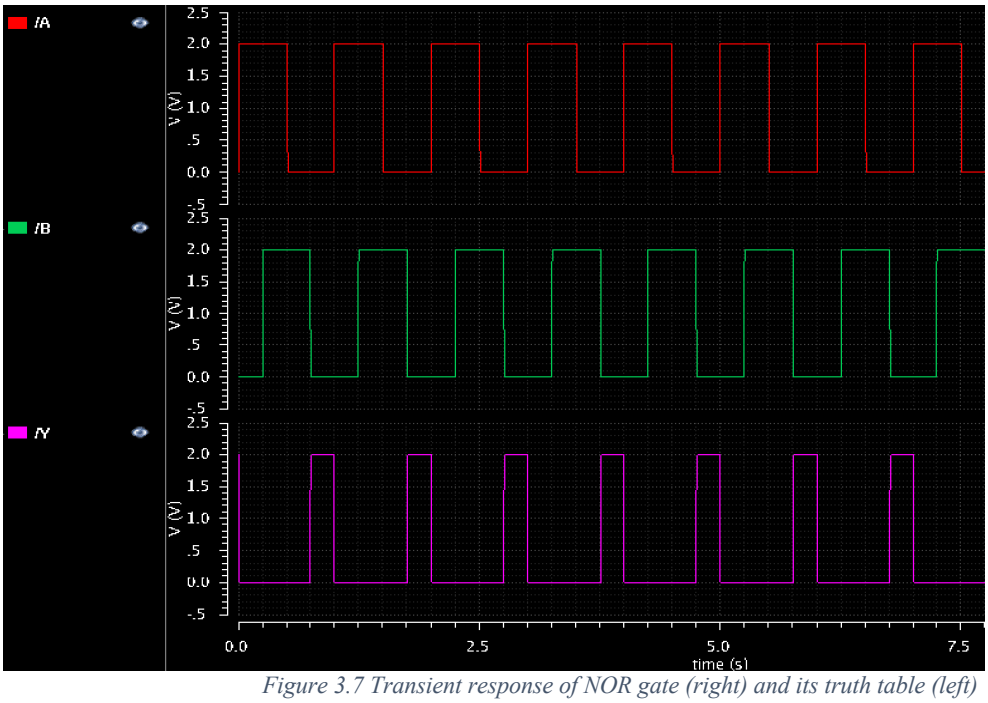


Figure 3.6 Schematic circuit of NOR gate with two inputs (right) and symbol configuration (left)

The gate performs the logic operation not (A+B), following the truth table. The transient response was simulated using two square waves with period of 1s and mutual delay of 250ms (Figure 3.10).



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Figure 3.7 Transient response of NOR gate (right) and its truth table (left)

Finally, the layout and the extracted view are presented in the following Figure 3.11 and as it was for the other cases in order to optimize the final area the transistors were overlapped one to each other.

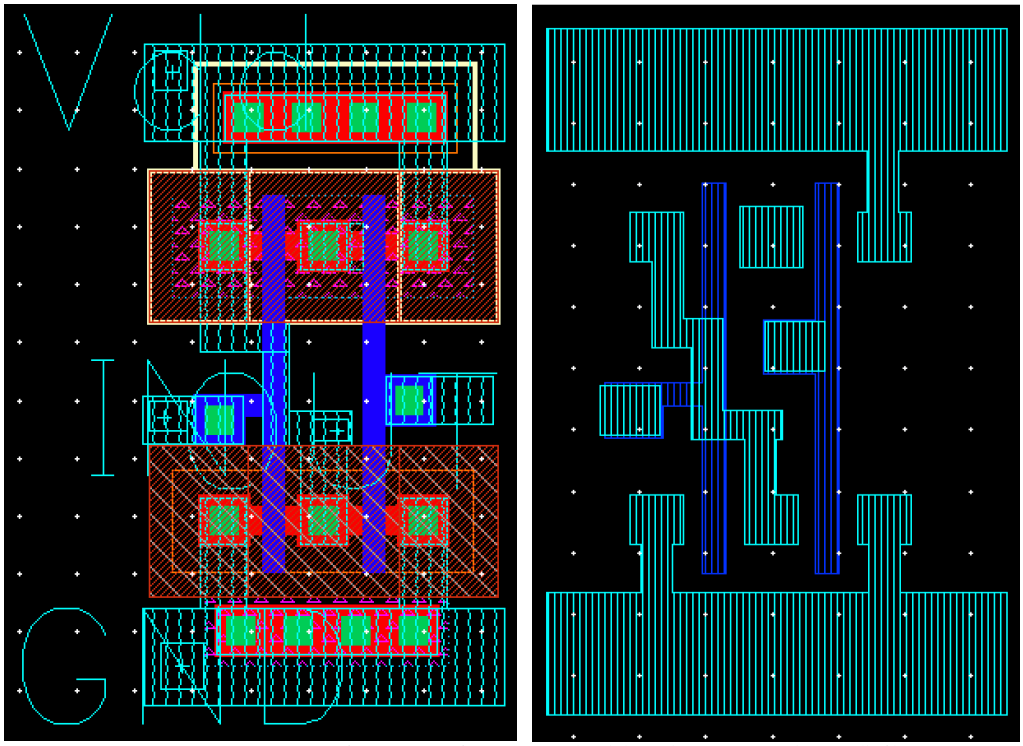


Figure 3.8 Layout configuration of NOR gate (right) and its extracted view (left)

3.1.4 AND

To create the AND gate a simple change in the NAND configuration was done, which is to put and inverter just before the output (Figure 3.12).

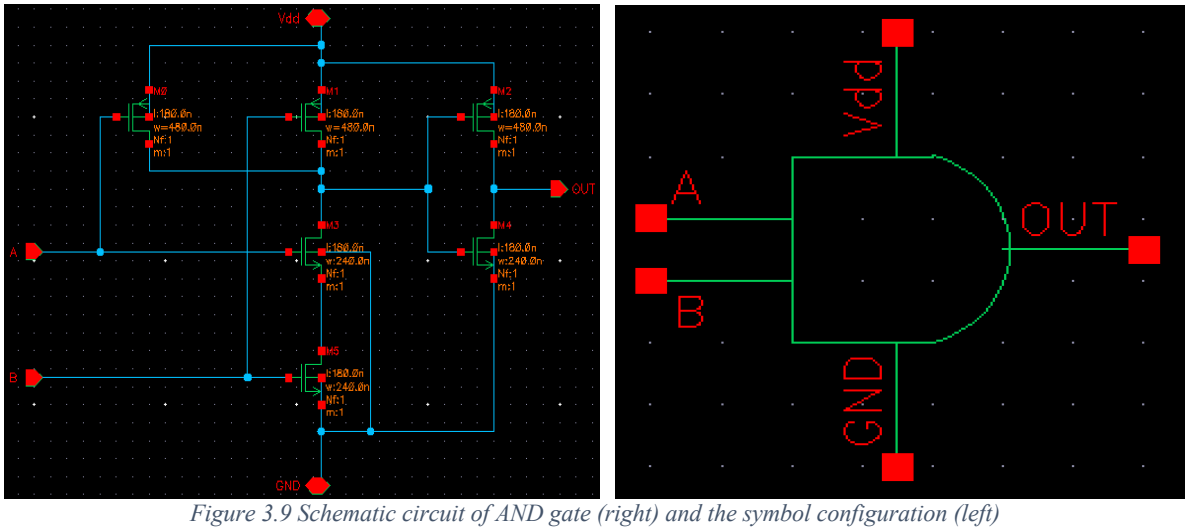
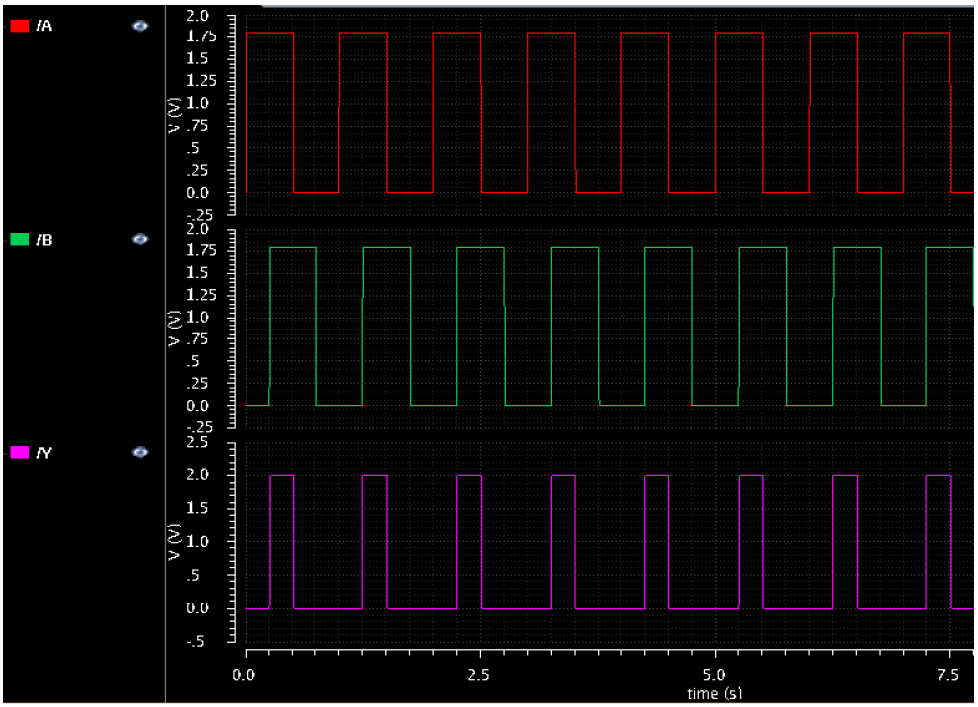


Figure 3.9 Schematic circuit of AND gate (right) and the symbol configuration (left)

The gate performs the logic operation (A*B), following the truth table in Figure 3.13. The transient response was simulated using the same two square waves generated for the NAND gate and the result, according to what already said, is the same of that port but inverted.



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Figure 3.10 Transient response of AND gate (right) and its truth table (left)

In the end the layout and post-layout views (Figure 3.14) with some small differences due to the parasitic capacitances.

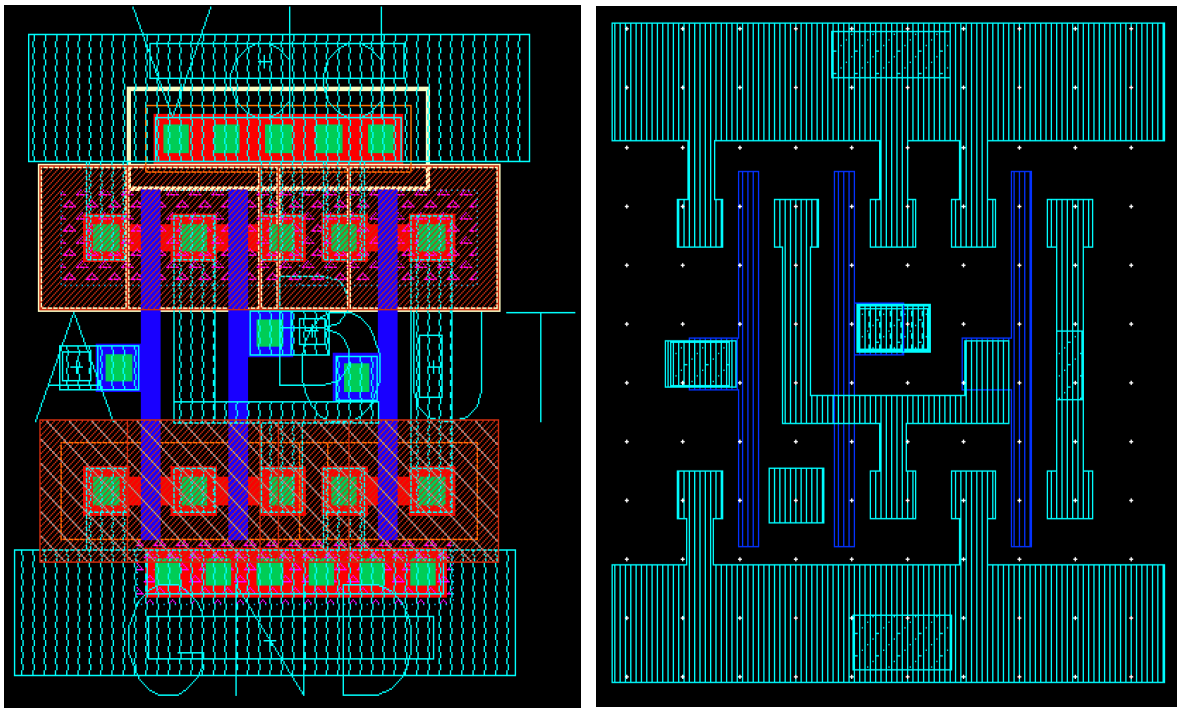


Figure 3.11 Layout configuration of AND gate (right) and its extracted view (left)

3.1.5 OR

In the same way for the AND gate I simply made a configuration change of the NAND port by adding two transistors at the output, to create the OR one I did the same thing but to a NOR gate (Figure 3.15).

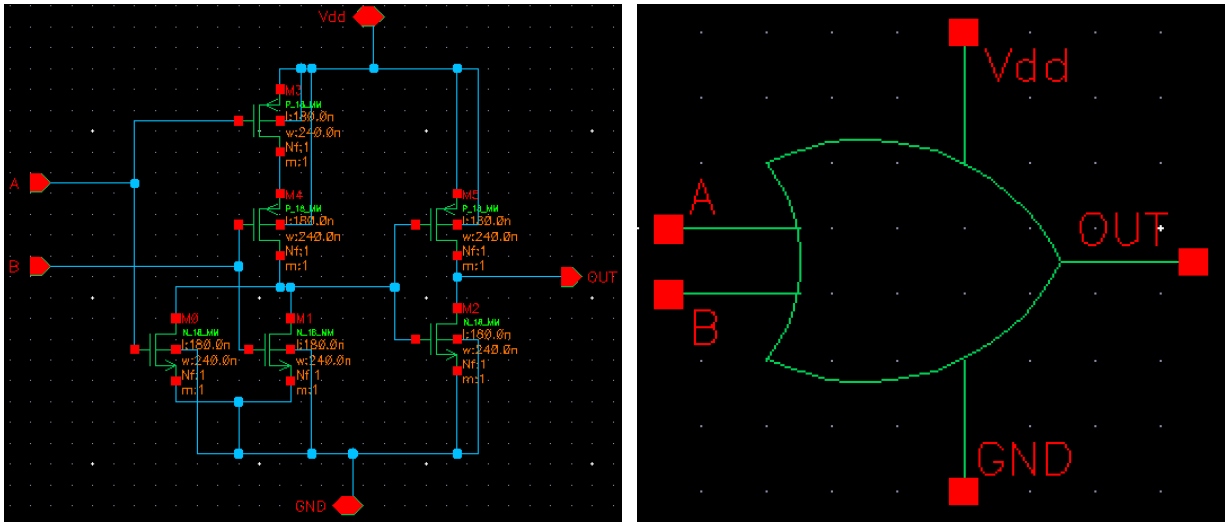
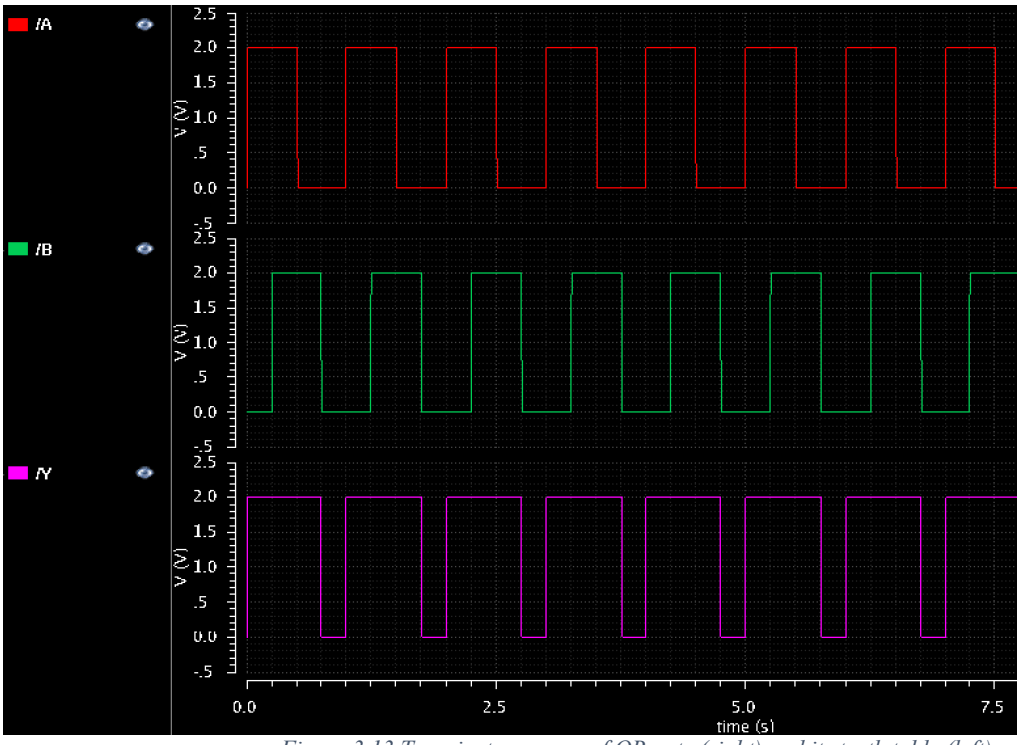


Figure 3.12 Schematic circuit of OR gate (right) and the symbol configuration (left)

The gate performs the logic operation (A+B), following the truth table in Figure 3.16. The transient response was simulated using the same two square waves generated for the NOR gate and the result, according to what already said, is the same of that port but inverted.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Figure 3.13 Transient response of OR gate (right) and its truth table (left)

The layout and the extracted view are here presented in the Figure 3.17.

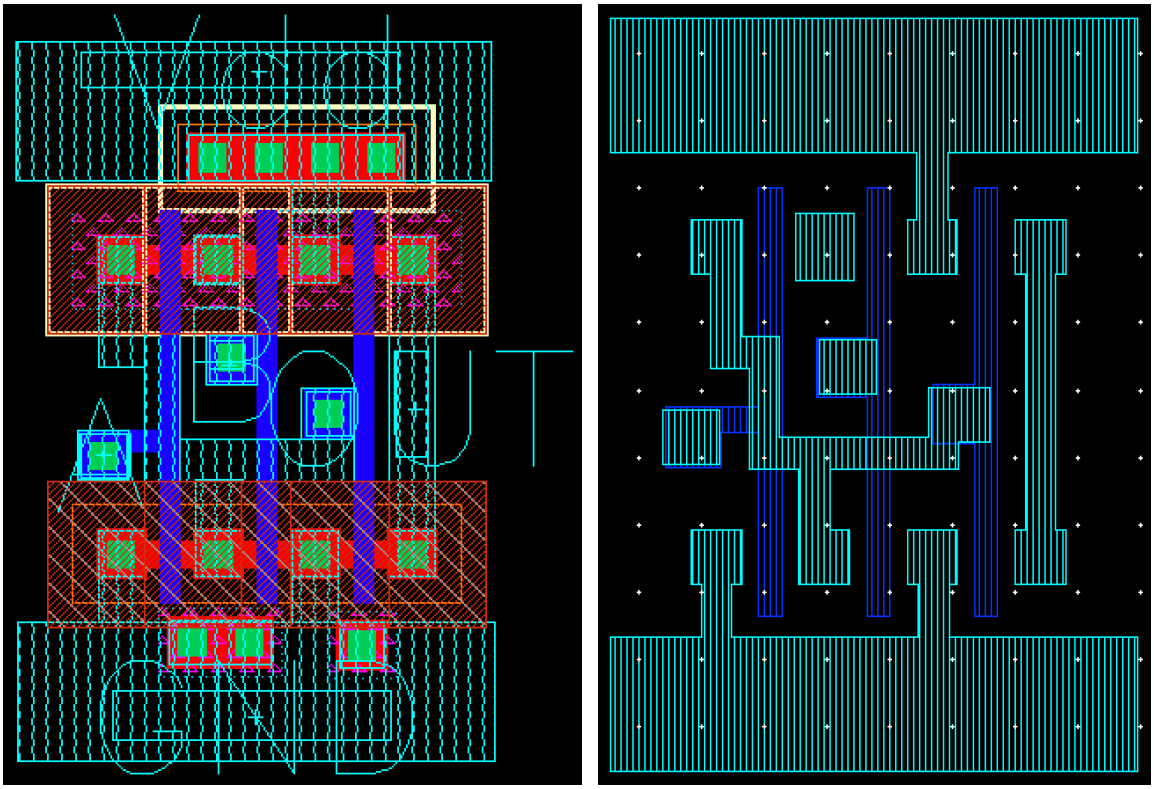


Figure 3.14 Layout configuration of OR gate (right) and its extracted view (left)

3.2 LOW POWER TIMER USING GATE LEAKAGE

My research work in literature highlights the oscillator of [3.1], in which the premises were almost perfect for my purpose. In the paper is described a clock used for monitoring intraocular eye pressure, with the aim to save as much energy as possible, and its implementation, using 130 nm technology, demonstrate that it can be done with the following characteristics (Table 3.1):

Supply Voltage (V)	Power (pW)	Frequency (Hz)	Area (um^2)
0,45	120	0,09	480

Table 3.1 Performances of One-Hot Timer from [3.1]

3.2.1 ONE-SHOT TIMER

Generally speaking, a one-shot timer works generating a pulse and its inverse every time the triggered-input goes to high logic level (Figure 3.18) and in the end, also a triggered-output that can controls another timer.

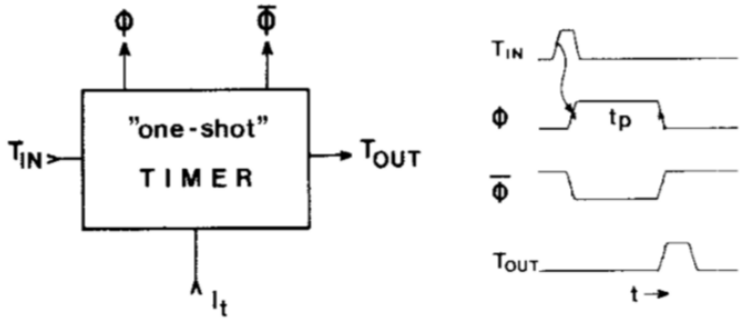


Figure 3.18 Current controlled one-shot timer (right) and temporal diagram (left); reprinted from [3.2]

The oscillator proposed in [3.1] is inspired by [3.2] in which a current controlled one-shot timer is described, using a flip-flop SR, a Schmitt trigger and a charge pump (Figure 3.19).

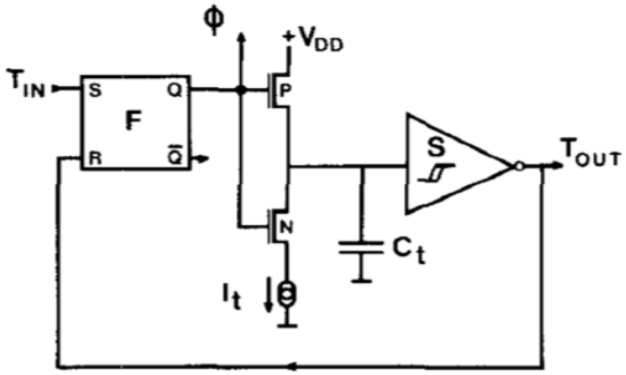


Figure 3.19 Implementation of the current controlled one-shot timer; reprinted from [3.2]

From Figure 3.19 is clear that the output of the flip-flop is also the clock pulse of the timer (ϕ) so, when Q is 0 (low level) then also ϕ will be 0, which means that the capacitor C_t will be charged to Vdd thanks to the pMOS, while the nMOS is off. The Schmitt Trigger, working as an inverter, will generate a low output, that will also be the reset input for the flip-flop, guaranteeing a stable condition until T_{in} is low. When the trigger input change then the timer will work in a opposite way, because Q will be high, exactly like the clock pulse, which will shut off the pMOS, discharging the capacitor to GND and giving a T_{out} at 1 as output of the Schmitt Trigger and reset input of the flip-flop.

3.2.2 GATE LEAKAGE

A second architecture, that inspired the final configuration of the intraocular monitoring oscillator is shown in Figure 3.20, very similar to the previous one: the two ideal current generators are used to charge and discharge the capacitor C_t and the double threshold comparator is used to change V_{out} every time V_{in} exceed or goes below the corresponding threshold.

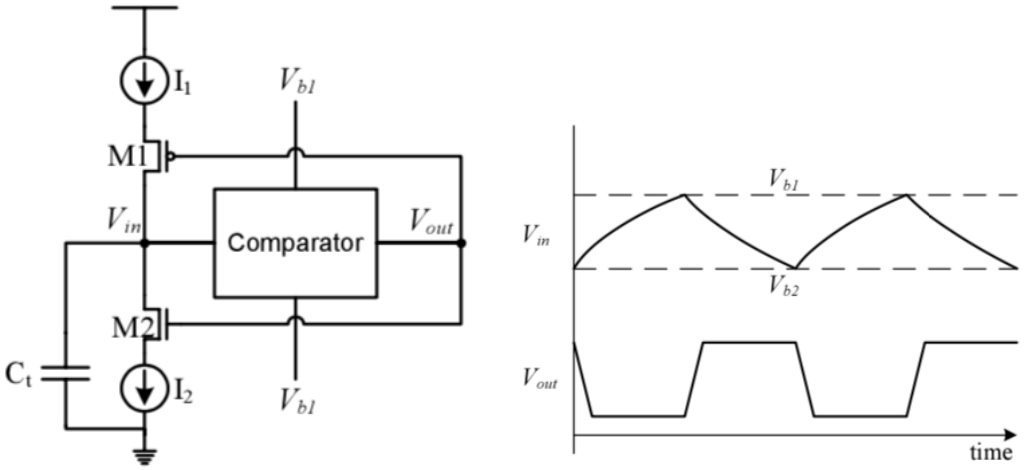


Figure 3.20 One-hot time with ideal current sources (right) and timing diagram (left); reprinted from [3.1]

Assuming that $I_1 = I_2 = I_{on}$ the frequency of the timer is:

$$f = \frac{2 * I_{on}}{C_t * (V_{b1} - V_{b2})} \tag{3.1}$$

In order to reduce the active energy, a good solution is to make the clock works at very low frequency, which means that the capacitance value or the RC constant, need to be extremely large. To guarantee this is possible to replace the two ideal current sources (I_1, I_2) with gate leakage. In CMOS design the downscaling of component's sizes lead to very thin oxide-gate so that, the leakage currents are no more negligible. Therefore,

gate leakage is due to different tunneling currents, like direct tunneling, typical of MOS structures with ultra-thin oxide (< 4 nm) during which electrons, from the conduction band in semiconductor, are transferred across the oxide directly into the conduction band of metal, or Fowler-Nordheim tunneling, characteristic of MOS with oxide 5-10 nm thickness, where electrons tunnel from semiconductor conduction band into oxide conduction band. In general gate current density can be calculated according to:

$$J_g = A * T_{oxratio} * \frac{V_g * V_{aux}}{t_{ox}^2} * e^{[-B*(\alpha-\beta*V_{ox})(1+\gamma*V_{ox})*t_{ox}]} \quad (3.2)$$

Where:

$$A = \frac{q^2}{8 * \pi * h * \phi_b}$$

$$B = \frac{8 * \pi * \sqrt{2 * q * m_{ox}}}{3 * h} * \phi^{\frac{3}{2}}$$

m_{ox}: effective carrier mass in the oxide
ϕ_b : tunneling barrier height
t_{ox}: oxide thickness
V_{aux} : fitting function of the tunneling carrier density and available states

3.2.3 FINAL TIMER CONFIGURATION

The architecture of the proposed oscillator in [3.1] bases its functioning on what said in the previous sections and so the final configuration is shown in Figure 3.19 in which there are:

- MC1 and MC2: thin oxide MOS capacitors used to replace the two ideal current sources explained in Figure 3.18, whose task is to charge/discharge V_{in}.
- ML1: load capacitance realized using thick oxide gate transistor.
- Schmitt Trigger inverter: used as a comparator with the configuration in Figure 3.20. What previously were indicated as V_{b1} and V_{b2} are now the high-to-low transition voltage V_{M-} and the low-to-high transition voltage V_{M+} (two crossover points in the voltage transfer characteristic).
- INV1 and INV2: simple inverters used to make sharper the transition of the clock and to reduce the leakage power.
- TINV: buffer that provide the V_{clk} signal output.

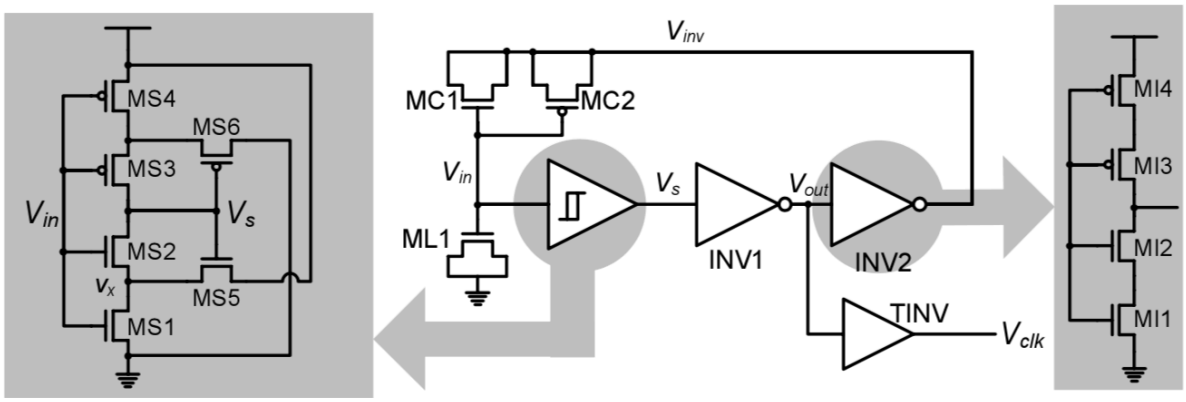


Figure 3.21 Final timer configuration for subthreshold operation; reprinted from [3.1]

The output waveform is the same as in Figure 3.18: every time V_{out} is pulled-up then V_{inv} is pulled-down in order to use MC1 and MC2 to discharge V_{in} until it reaches a value under the lower threshold of the Schmitt Trigger, and vice versa.

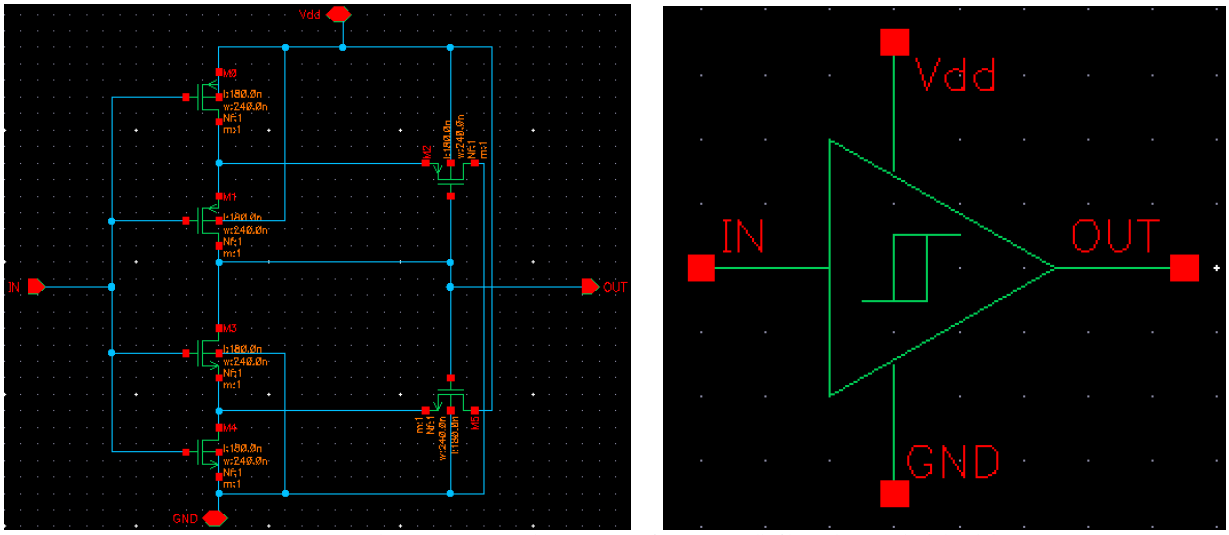


Figure 3.22 Schmitt Trigger schematic configuration (left) and it symbol (right)

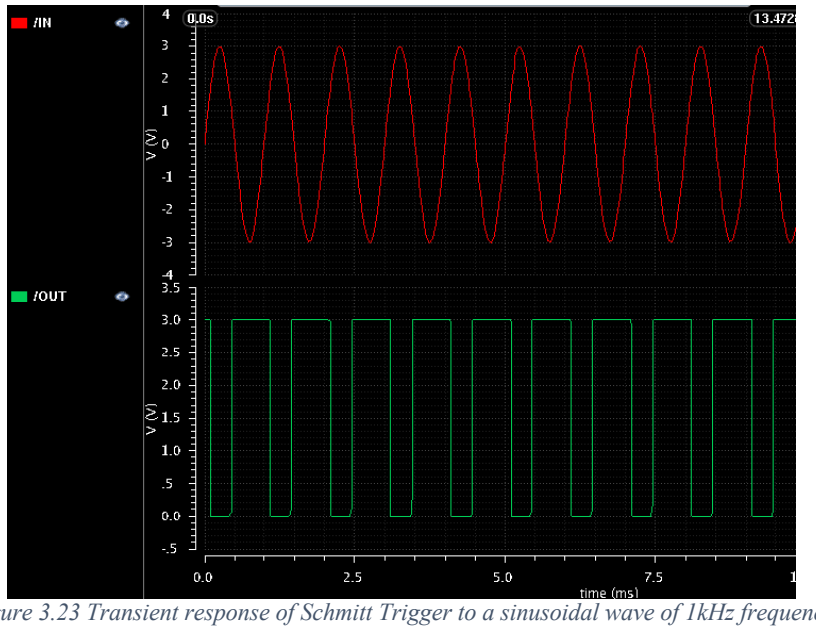


Figure 3.23 Transient response of Schmitt Trigger to a sinusoidal wave of 1kHz frequency

The Schmitt Trigger is widely used in both analog and digital circuits, to reduce noise. It is a comparator circuit with hysteresis, whose name “Trigger” is due to the fact that the output is in a stable condition until the input changes enough to trigger a different value. Its conventional circuit is proposed in Figure 3.20, with two sub-circuits: P channel (made by M0, M1 and M2) and N channel (made by M3, mìM4 and M5). As is shown in the Figure 3.20, there isn’t a direct path between the voltage supply and the ground, because the P-part is connected to the path between Vdd and the output, and the N-part is connected to the path between the output and GND. If the output is low, then M2 is on while M5 is off, which means that for the calculation of the switching point voltages it’s needed only the P sub-circuit, while if the output is high the working mode will be opposite.
The layout configuration of this circuit is then shown in Figure 3.22.

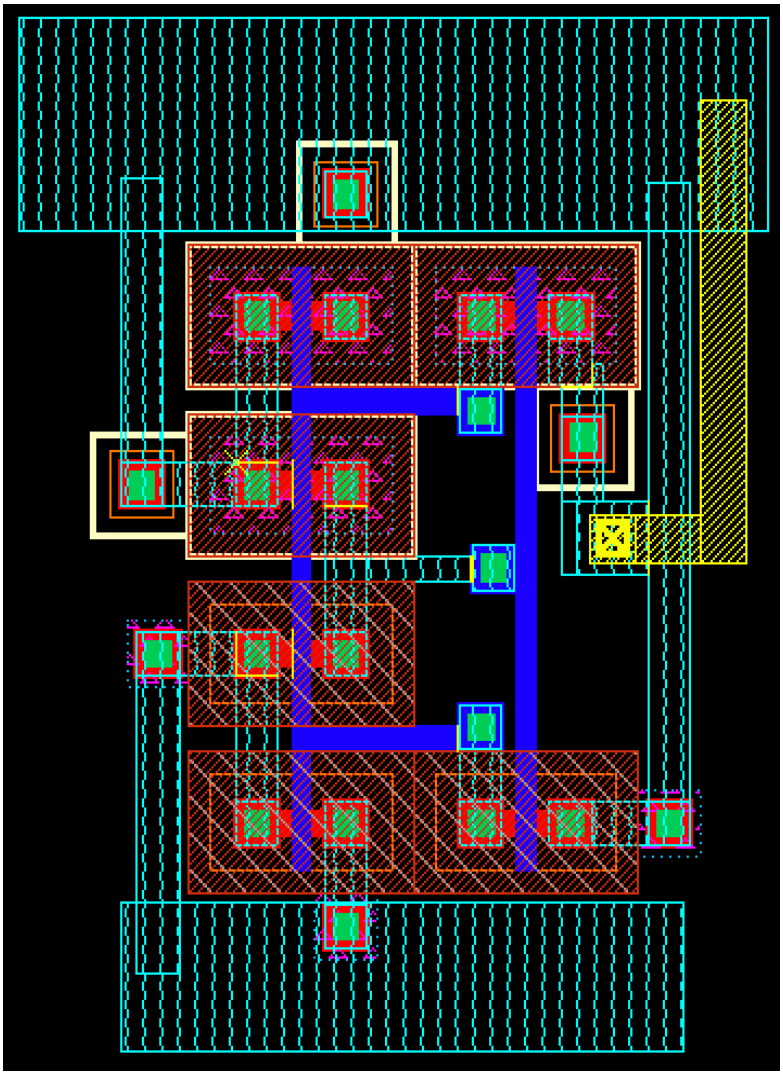


Figure 3.24 Layout configuration of Schmitt Trigger circuit

After the implementation of the Schmitt Trigger, I realized the timer configuration in Cadence Virtuoso (Figure 3.23) to see its transient response and test the results defined in [3.1]. It was necessary to replace the three transistors on the left with two parallel

resistances connected with a capacitor, because unfortunately the results prospected by [3.1] didn't attend the reality. As I will explain better later, many simulations were performed in order to reach the 0,09 Hz frequency of Table 3.1 without success.

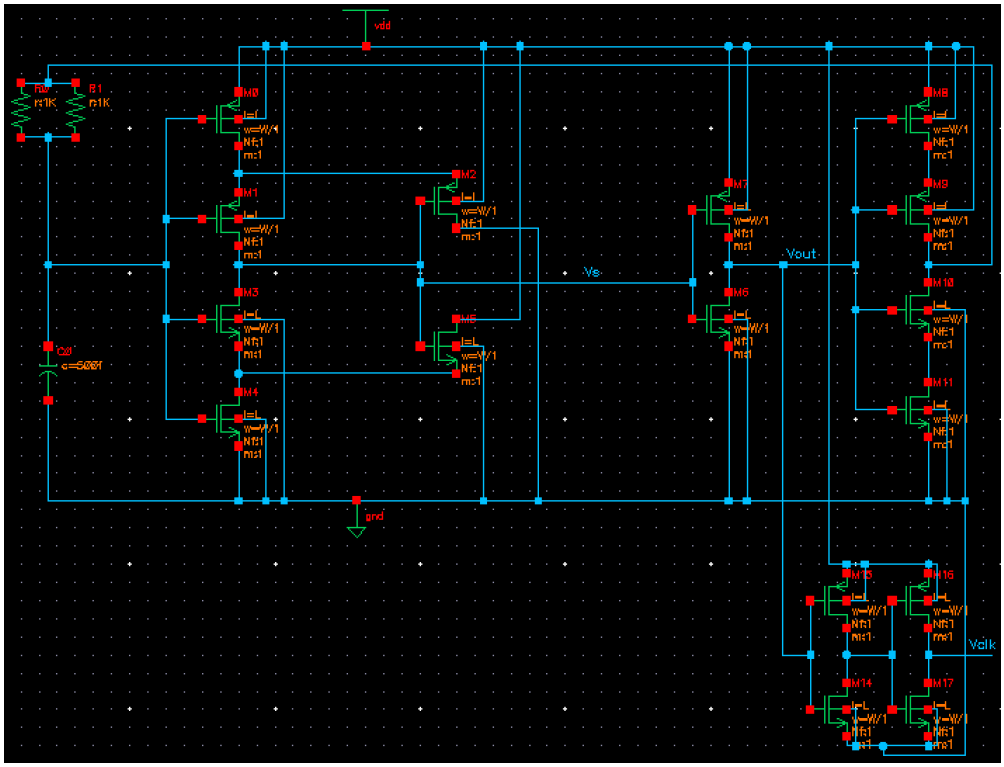


Figure 3.25 Schematic transistors configuration of the timer with parallel resistances and capacitor

Using a voltage supply of 450 mV, a capacitor C = 500 fF, two parallel resistances with common value R = 1 kΩ and the minimum size for the transistors, the final frequency obtained through transient response (Figure 3.24) is f = 440, 95 kHz.

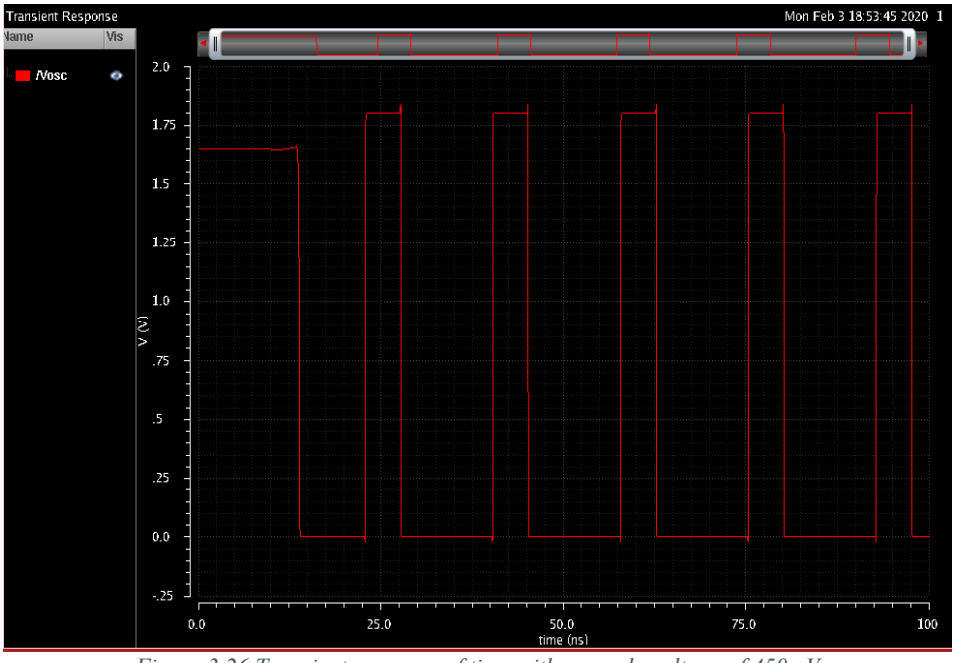


Figure 3.26 Transient response of time with a supply voltage of 450mV

3.3 VOLTAGE CONTROLLED OSCILLATOR (VCO)

An alternative oscillator implemented using the Schmitt Trigger is shown in Figure 3.25, where the MOSFETs Ml and M4 behave as current sources, mirroring the current in M5 and M6. When the output of the oscillator is 0 (low level) the pMOS M3 is on, while the nMOS M2 is off, this means that the current from M4 can charge the capacitor C. When the voltage across this capacitor exceeds the higher threshold of the Schmitt Trigger, the output of this last one will go to 0. Thanks to the last inverter stage, the final output of the oscillator will be high, so that M3 will be shut off and M2 will allow to discharge the capacitor through M1. In this case, when C goes below the lower threshold of the Schmitt Trigger, this one will change state.

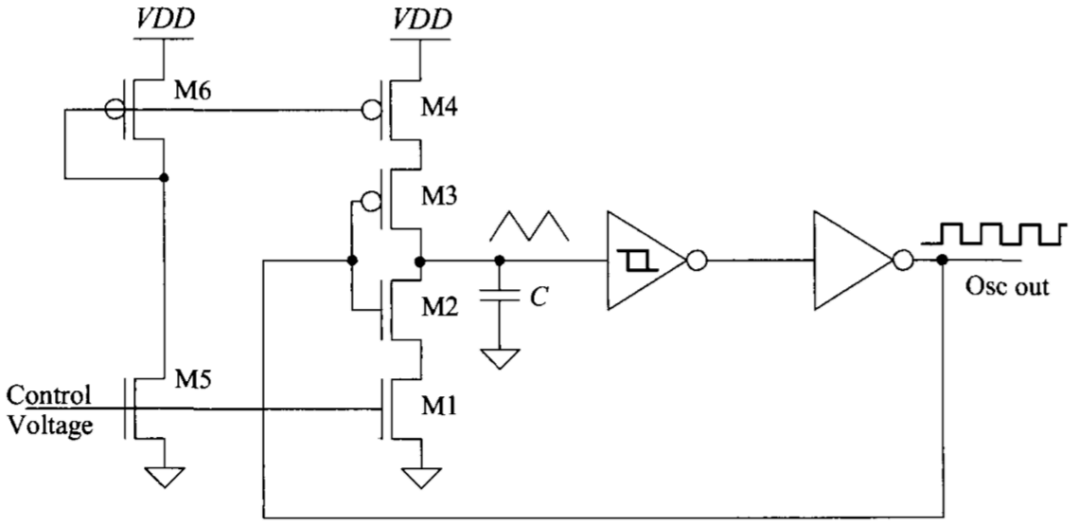


Figure 3.27 Voltage controlled oscillator using Schmitt Trigger and current sources

The name of this oscillator comes from the fact that its frequency can change according to an external voltage. Its schematic configuration is presented in Figure 3.26 and starting from this, a transient simulation (Figure 3.27) was performed studying at the beginning two limit cases: the first one with a supply voltage of 400 mV the second one with a supply voltage of 1,8 V.
The results are summarized in Table 3.2.

Vdd	C	f
400mV	500fF	153,139Hz
1,8V	500fF	162,265Hz

Table 3.2 Performances of Voltage Control Oscillator changing its supply voltage

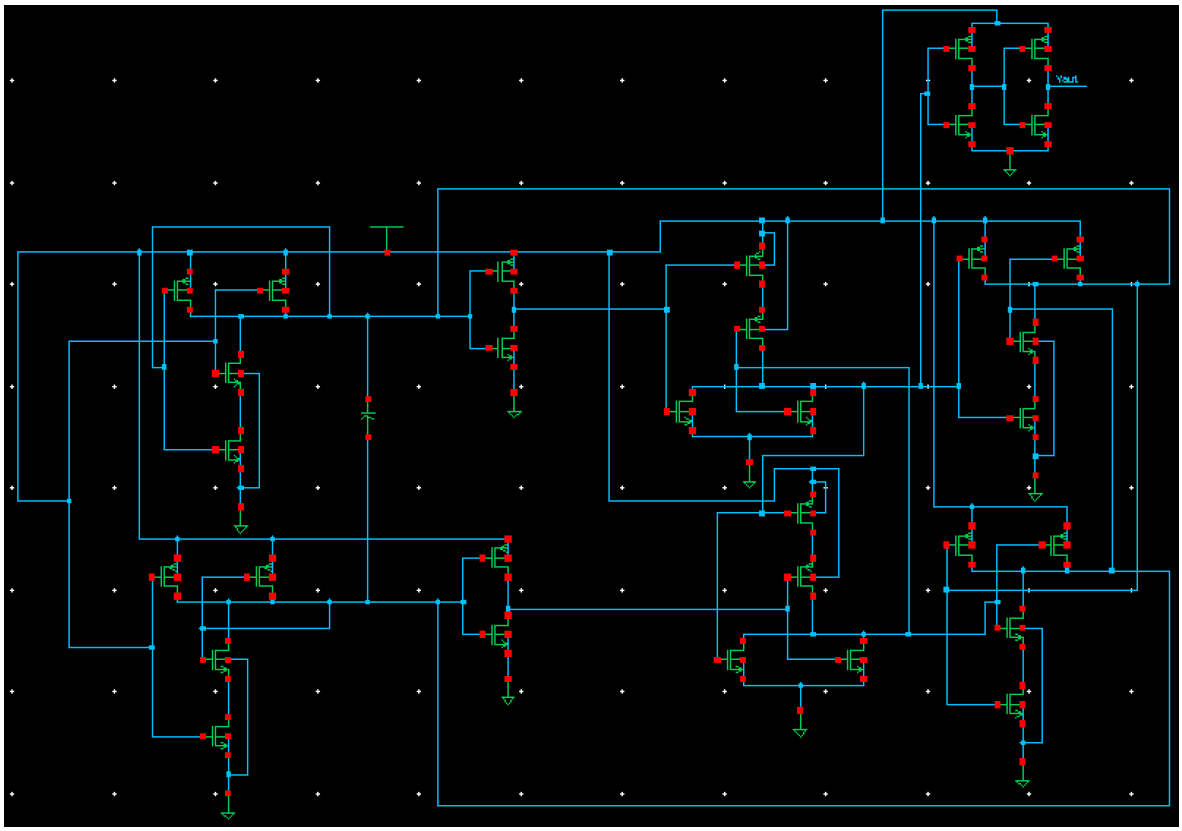


Figure 3.28 schematic transistors circuit of VCO

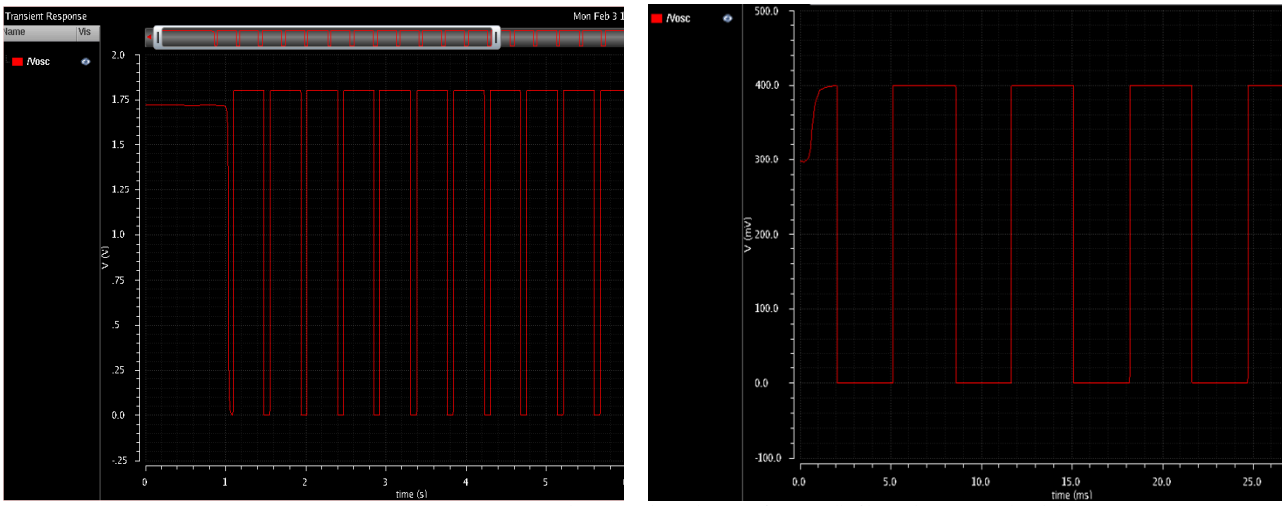


Figure 3.29 Transient response with a supply voltage of 1,8 V (left) and 400 mV (right)

Also, this time the results were obtained imposing minimum sizes from PDK for all the transistors, which correspond to a length of 180 nm and a width of 240 nm. I decided to do this to optimize the complex lateral area (which need to be less than 100 μm^2), and to have a starting point checking at which frequency the oscillator can work and from here decide what strategy to use in order to reach a sub-Hz value.

3.4 RELAXION OSCILLATOR WITH DLS LOGIC STYLE

Analyzing the frequencies obtained from the two previous oscillators, is evident that the aim to have a "mHz" frequency range is still far away. So, I studied another architecture, taken from [3.3] in which it's described a relaxion oscillator implemented using the Dynamic Leakage Suppression (DLS) logic.
According to what is said in [3.3]: "DLS logic style was introduced to drastically reduce the standby power of digital standard cells, at the cost of substantially degraded speed". In fact, logic gate implemented with DLS logic delivers very small and almost supply-independent on-current allowing low oscillation frequency. Furthermore, most of the power consumption is due to a very small current, lower than the regular transistor leakage, so it will result in a very low consumption.
The proposed configuration of this relaxion oscillator is shown in Figure 3.28.

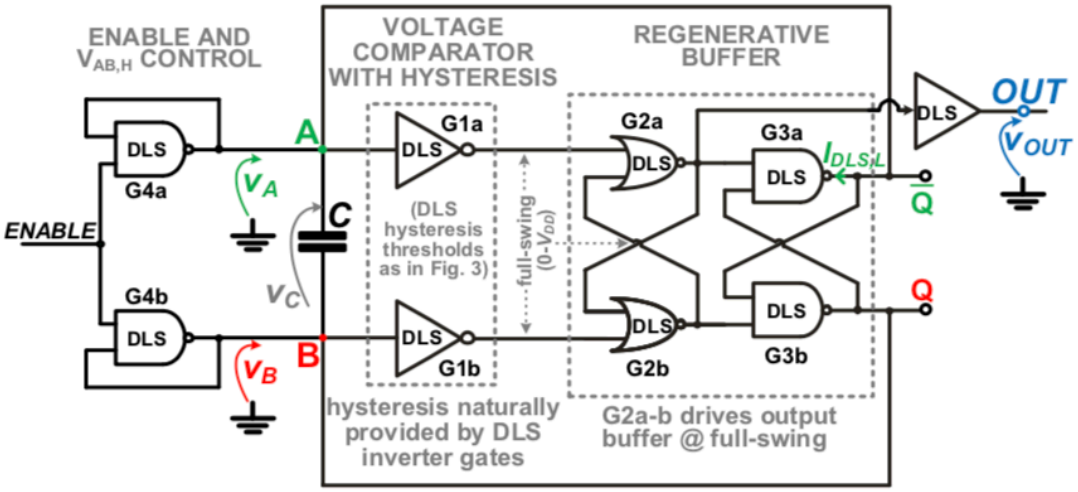


Figure 3.30 Relaxion Oscillator architecture with DLS logic style; reprinted from [3.3]

To implement this oscillator the first step was, of course to re-create all the logic gates using DLS logic and understand their working mode.

3.4.1 DYNAMIC LOGIC SUPPRESSION (DLS)

A representative example to explain the differences among standard and DLS ports is shown in Figure 3.29, that represents the inverter DLS configuration. First of all, the number of transistors is different: in a standard configuration there are only one pMOS and one nMOS which in turn are shut off to change the input signal. In case of DLS implementation are added a pMOS-footer (MP) and a nMOS-header (MN), with their gates connected to the output of the standard inverter creating a feedback loop.
According to Figure 3.29 a low input turns off MPD, generated a high logic level for the output, which is in turn responsible of the MP shut off. Since the drain current of these two transistors is equal, in the common node X there is a voltage $V_x = \frac{V_{DD}}{2}$. This

caused a negative source-gate voltage for MP (and gate-source voltage for MPD) equal to $-\frac{V_{DD}}{2}$. This process is named "Super-Cutoff" operation.

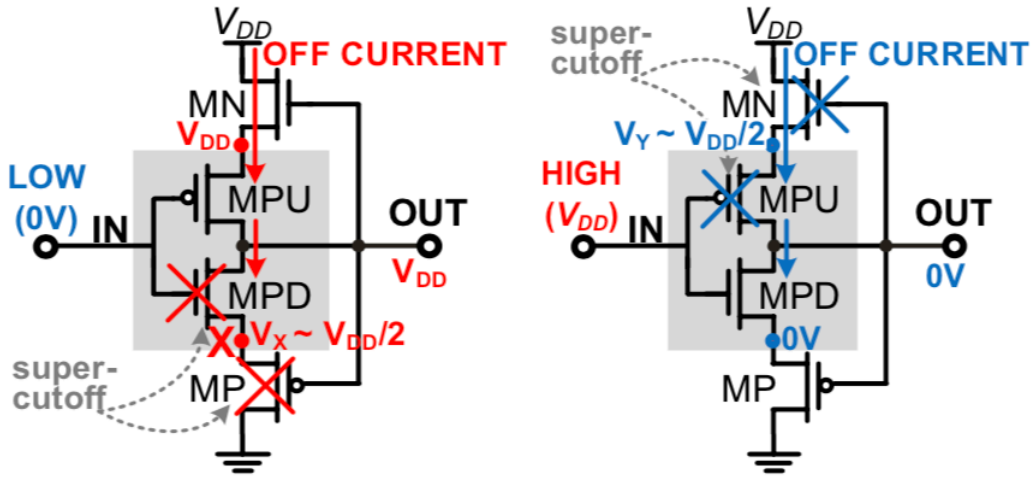


Figure 3.31 Circuit analysis of DLS inverter gate with super-cutoff; reprinted from [3.3]

The same considerations can be done in case of high-level input, performing a super-cutoff of the MPU and MN transistors.
Besides the feedback loop is responsible of the hysteretic behavior of these ports (Figure 3.30). Analyzing the figure below are noticeable two threshold values, $V_{DLS,L}$ e $V_{DLS,H}$, which weakly depend on V_{DD}.

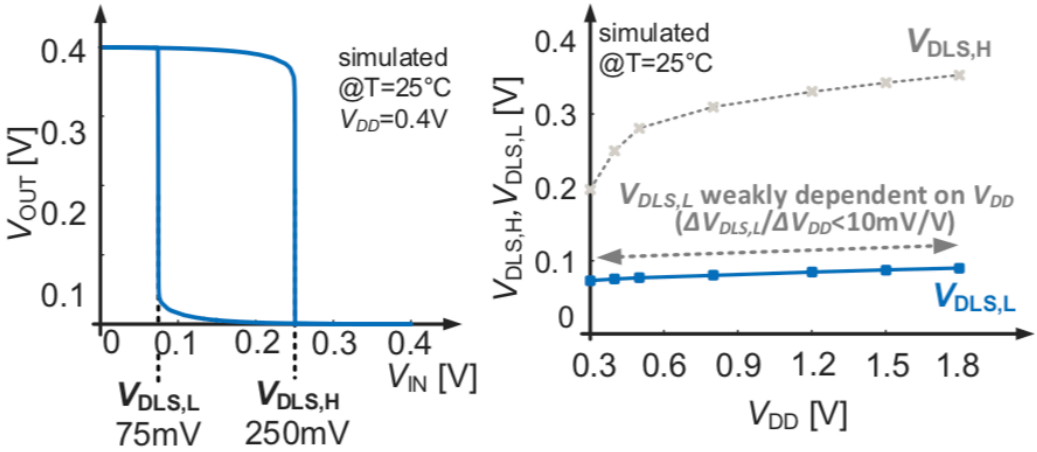


Figure 3.32 Static transfer curve characteristic (left) and hysteresis amplitude over power supply; reprinted from [3.3]

I will now briefly present the implementation of all DLS gates needed to implement this oscillator, with their transient response. For their transient analysis I impose an input square wave with period of 10 s because DLS logic requires a longer time interval than the standard gates for a correct behavior. Furthermore, in the output wave it will be noticeable a small, and negligible amplitude attenuation for all the logic ports. In order I will show: DLS inverter, DLS NAND, DLS NOR, DLS buffer.

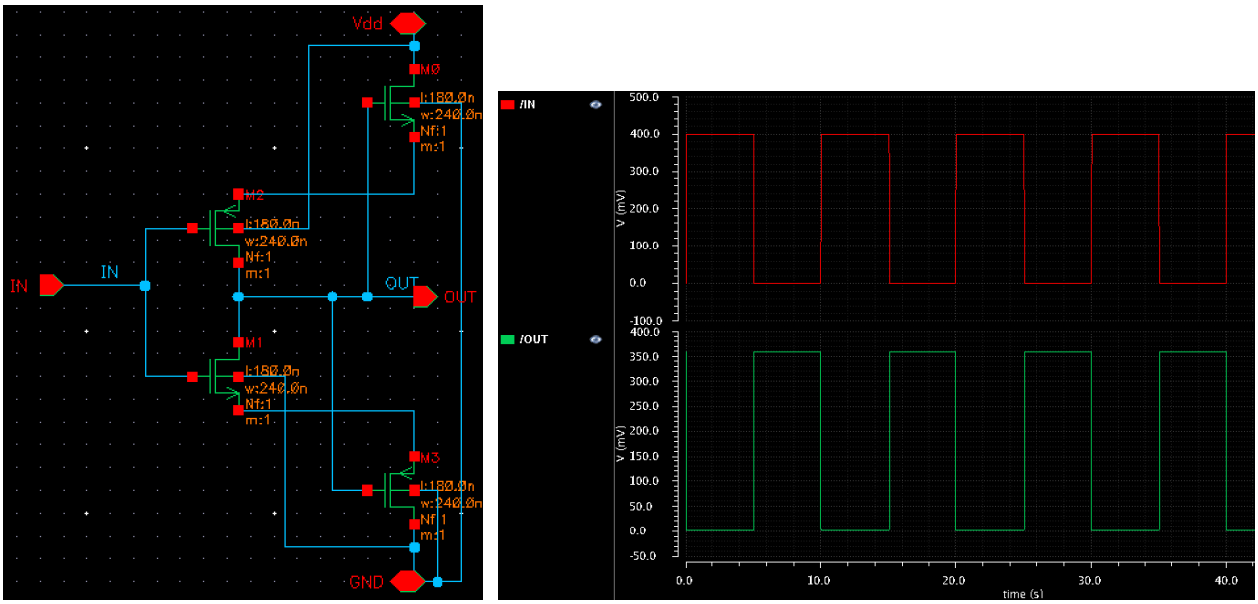


Figure 3.33 Schematic configuration of DLS inverter (left) and its transient response (right)

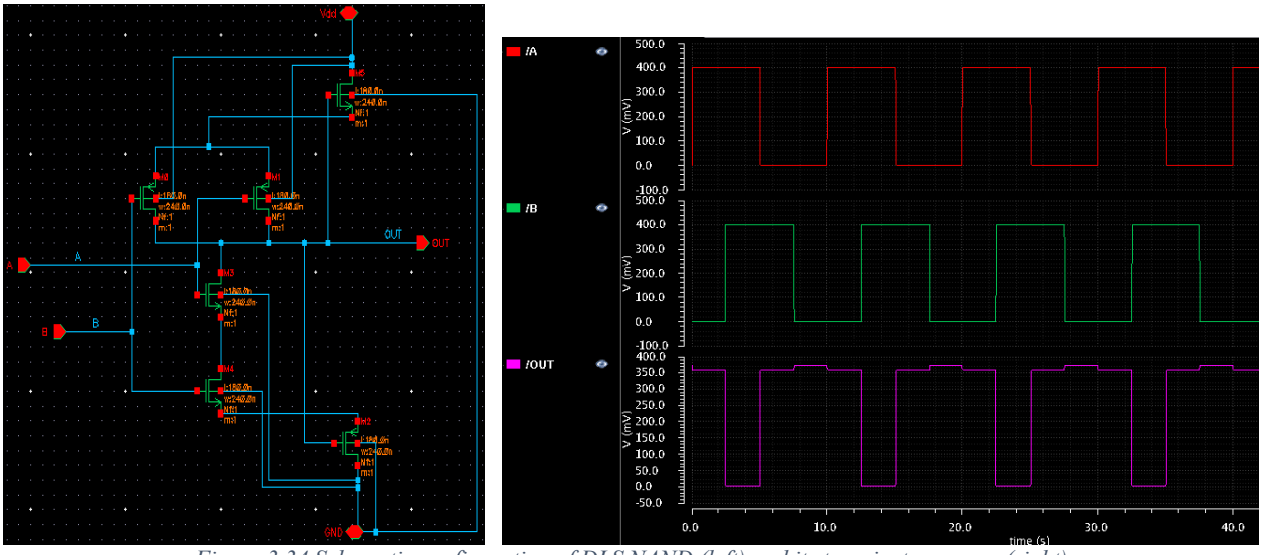


Figure 3.34 Schematic configuration of DLS NAND (left) and its transient response (right)

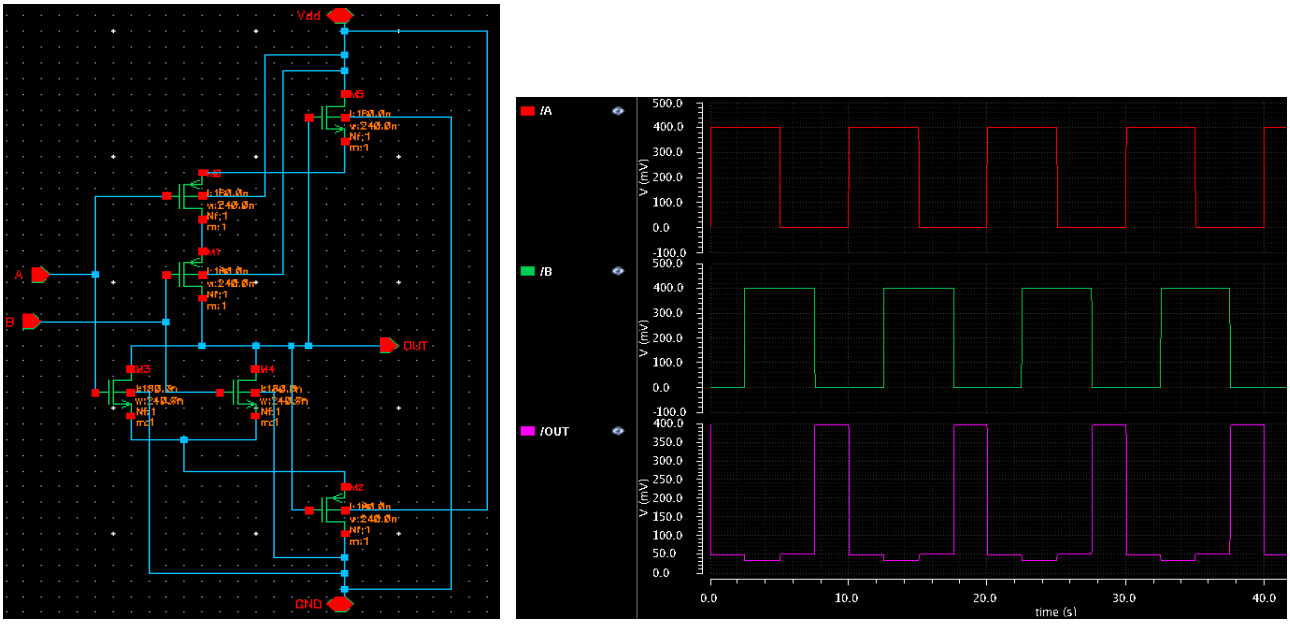


Figure 3.35 Schematic configuration of DLS NOR (left) and its transient response (right)

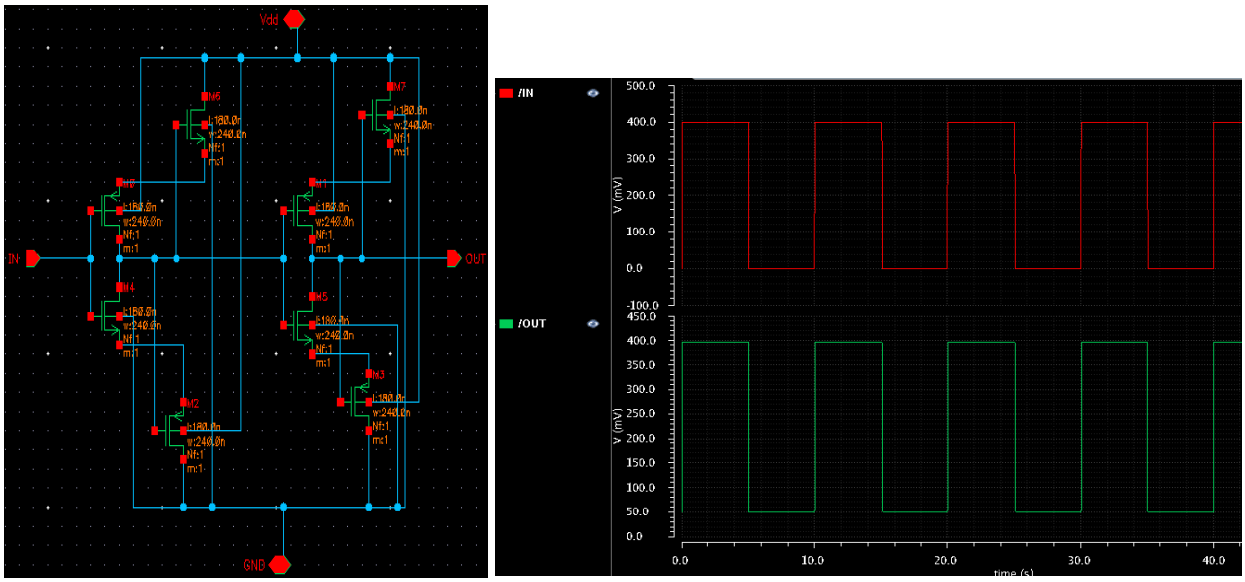


Figure 3.36 Schematic configuration of DLS buffer (left) and its transient response (right)

3.4.2 PROPOSED ARCHITECTURE

The architecture of Figure 3.28 was implemented in Cadence (Figure 3.36) and then tested using, like in the previous cases, minimum sizes for both length and width of the transistors.

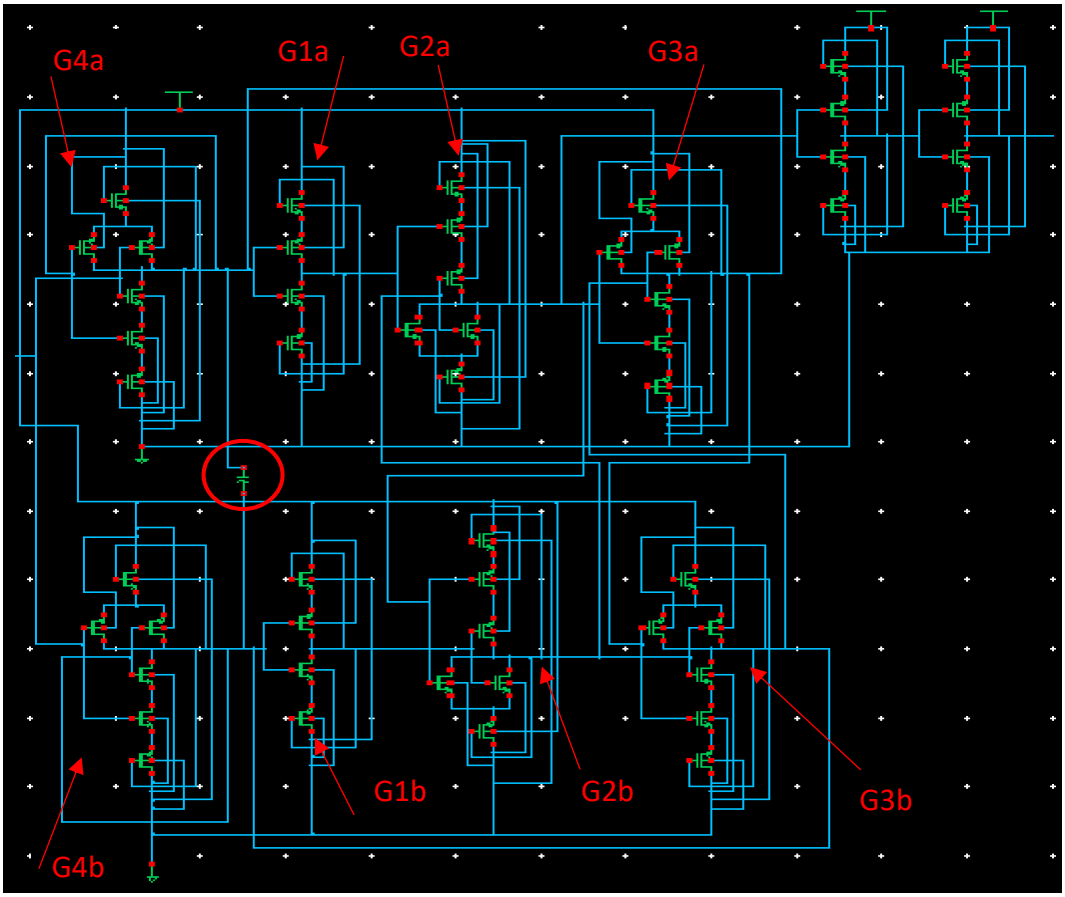


Figure 3.37 Schematic transistors architecture of relaxion oscillator with DLS gate

The key for the oscillation is obviously the periodic charge and discharge of the capacitor through the small on-current I_{DLS}. The oscillations frequency depends on the swing of V_a and V_b from the lower threshold $V_{DLS,L}$ and the V_{MAX}. Going into more details there are four main blocks in the architecture:

1) G1a-G1b inverters that work as voltage comparators, sensing voltages V_a and V_b.
2) G2a-G2b latch set-reset based on NOR gates, which periodically regenerates and holds the output at high or low level. From Figure 3.28 and Figure 3.36 is possible to see that G2a output is connected with a buffer gate which gives the final output of the oscillator.
3) G3a-G3b latch set-reset based on NAND gates essential to establish a positive feedback loop and sustain the oscillation.
4) G4a-G4b NAND ports which act like inverters with short-circuited input/output according to the ENABLE signal.

Let's now see in detail how this oscillator works. When the ENABLE is set to ground then A, B, Q and $\bar{Q}$ are led to low logic level while, if ENABLE is connected to the supply voltage then there is an output oscillation. Starting from a reference time t_0, with Q=0, the voltage V_a is set to the value $V_{AB,H}$, thanks to the active load G4a-G4b. From Figure 3.37 is possible to see the transistors equivalent circuit where $V_{AB,H}$ is defined through the gate-source voltages across the two transistors MN3a and MPU3a, which in turn depend on the difference between the two currents I_P and I_N. Currents that are in turn equal to the on-current delivered by a DLS inverter port, which is almost supply-independent.

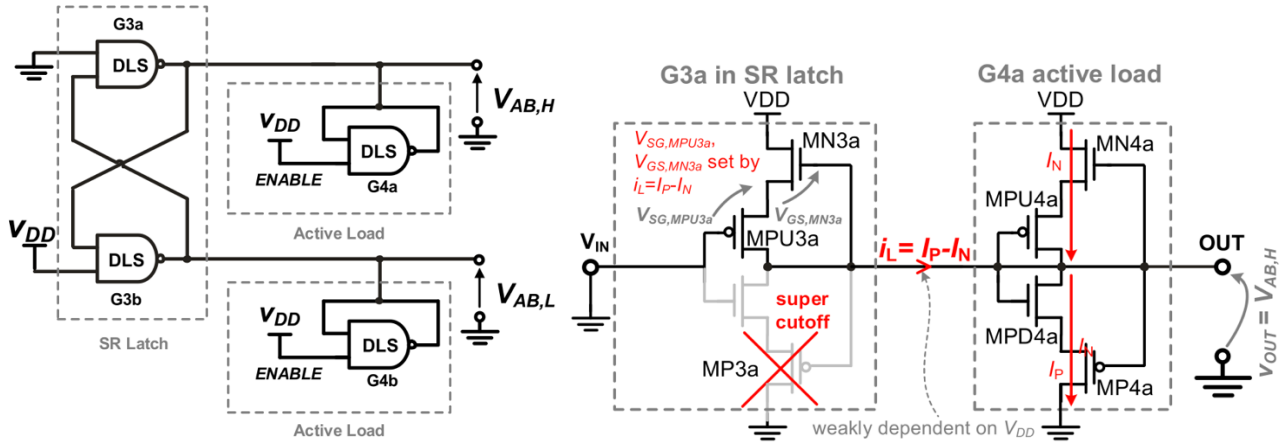


Figure 3.38 Equivalent circuit for the description of the latch G3a-G3b output voltage loaded by G4a-G4b (left) and Transistor equivalent circuit for the evaluation of $V_{AB,H}$; reprinted from [3.3]

Therefore while $V_a = V_{AB,H}, V_b = V_{MAX} > V_{AB,H}$ from the end of the previous period (equation (5) below for V_{MAX} definition). With these two values higher than the lower threshold of the comparator G1a-G1b, the outputs of the inverter will be low, forcing the hold condition in the NOR latch. Because of the initial assumption of Q = 0 and the inverting behavior of the NAND latch, the output of G2b will be high while the output of G2a will be low, setting in this way also the final output of the oscillator to 0. After

t_0, V_b is gradually pulled-down till it reaches the lower threshold $V_{DLS,L}$ of the comparator G1a-G1b at time t = t_1, because of the current I_{DLS} generated from G3b low output, which is also responsible for the discharge of the capacitor with a slope defines by:

$$\frac{dV_b}{dt} = -\frac{I_{DLS}}{C} \tag{3.3}$$

Because during this interval of time V_a remained constant, the voltage across the capacitor C can be defined as follow:

$$V_c = V_a - V_b = V_{AB,H} - V_{DLS,L} \tag{3.4}$$

After t_1 the high logic level of G1b triggers the falling transition of G2b output and the rising one of G3b. Because of this V_b increase till it reaches $V_{AB,H}$ at t = t_2. During the period from $t_1$to t_2, C value remained constant so:

$$Va = 2V_{AB,H} - V_{DLS,L} = V_{MAX} \tag{3.5}$$

At this point Va starts to be pulled-down because of the NAND latch G3a, the inverting nature of G1a and the NOR latch G2a-G2b, till it also reaches $V_{DLS,L}$, and so at t_3 starting the second half of the oscillating period with Va and Vb switched behavior.
All the steps described before are then summarized in Figure 3.38, in which is possible to observe the waveform Va, Vb and $Vout$ and in Table 3.3-3.4.

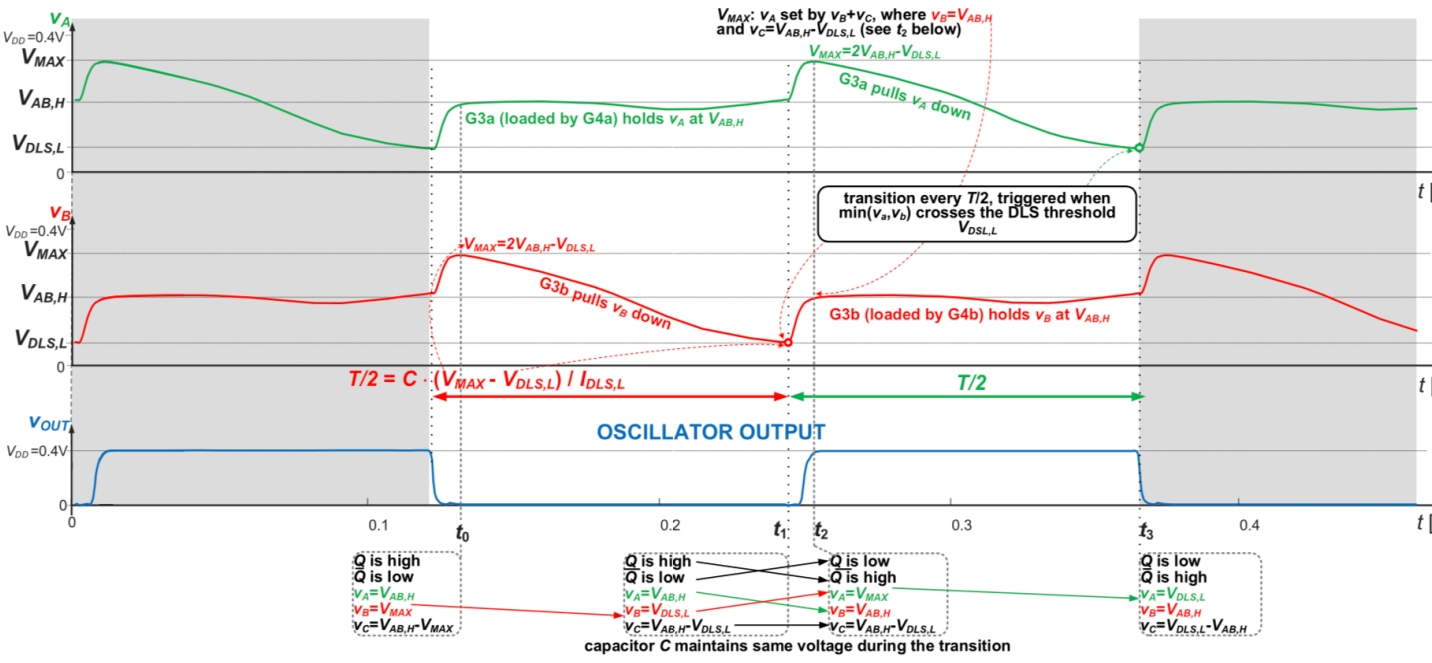


Figure 3.39 Waveform of the three main voltages during one period working of the oscillator; reprinted from [3.3]

G_{1a}	G_{2a}	G_{3a}	G_{1b}	G_{2b}	G_{3b}
Y=0	Y=0	Y=1	Y=0	Y=1	Y=0
X=1	A=0	A=0	X=1	A=0	A=1
	B=1	B=0		B=0	B=1

Table 3.3 Truth table of gates and latches of the relaxion oscillator at t_0

G_{1a}	G_{2a}	G_{3a}	G_{1b}	G_{2b}	G_{3b}
Y=0	Y=1	Y=0	Y=1	Y=0	Y=1
X=1	A=0	A=1	X=0	A=1	A=0
	B=0	B=1		B=1	B=0

Table 3.4 Truth table of gates and latches of the relaxion oscillator for the first half period

I tested this relaxion oscillator imposing, like in all the other cases, the minimum sizes for all the components, a supply voltage $V_{DD} = 400\ mV$ and a capacitance C= 500 fF, obtaining a frequency f = 5 Hz.

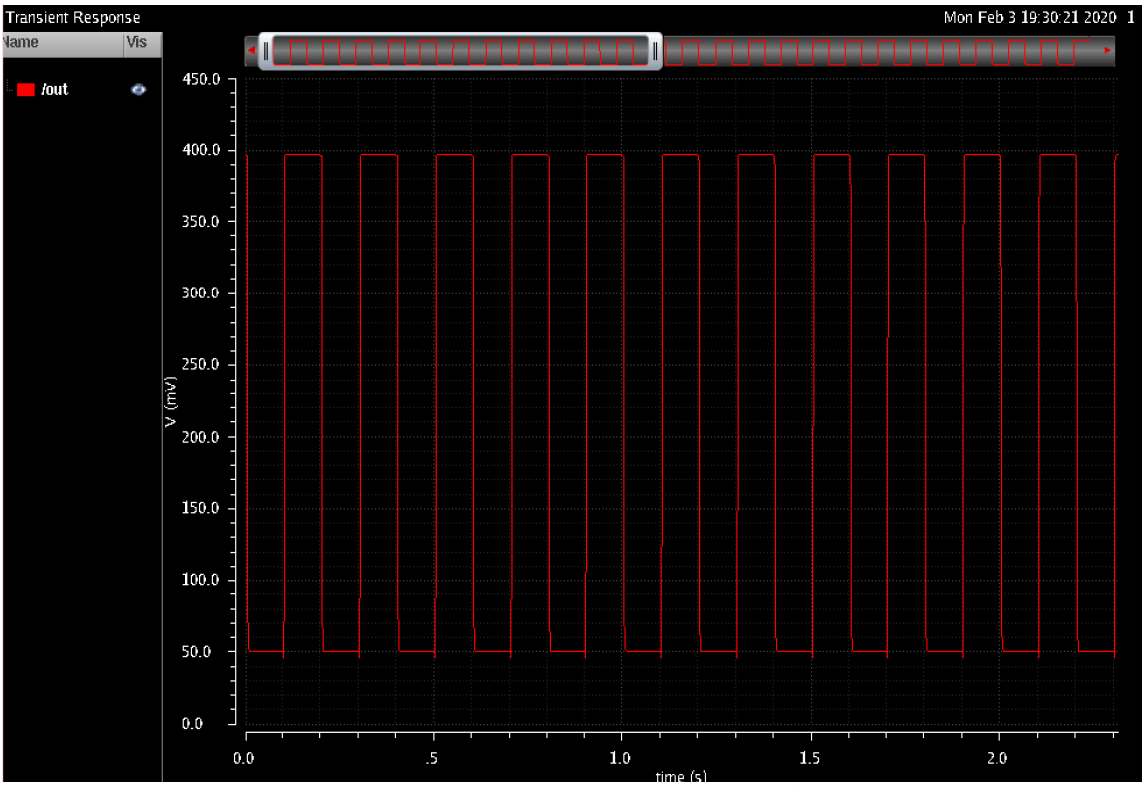


Figure 3.40 Transient response with supply voltage of 400 mV

3.5 RELAXION OSCILLATOR WITHOUT DLS

From the previous discussion about the relaxion oscillator implemented using DLS logic style gates, it is understandable that the total area of the circuit will definitely be higher than the imposed limit. However, the frequency obtained from the transient analysis was already in the range of Hz, a very promising result for future improvements. For this reason, I wanted to try and implement the same oscillator without DLS, to see the frequency change in the transient response. In fact, if the swing between the two results wouldn't be too high, the implementation without DLS could ensure a smaller area: for the relaxion oscillator with DLS proposed in the previous section the overall number of transistors is 52, while by using standard gates this amount decreases to 32. The working principle obviously remain the same as before, the only change done is in the configuration of the logic ports.
In the following Figure 3.40 and 3.41 I will show the architecture of the relaxion oscillator implemented without DLS, and later its transient response (Figure 3.42).

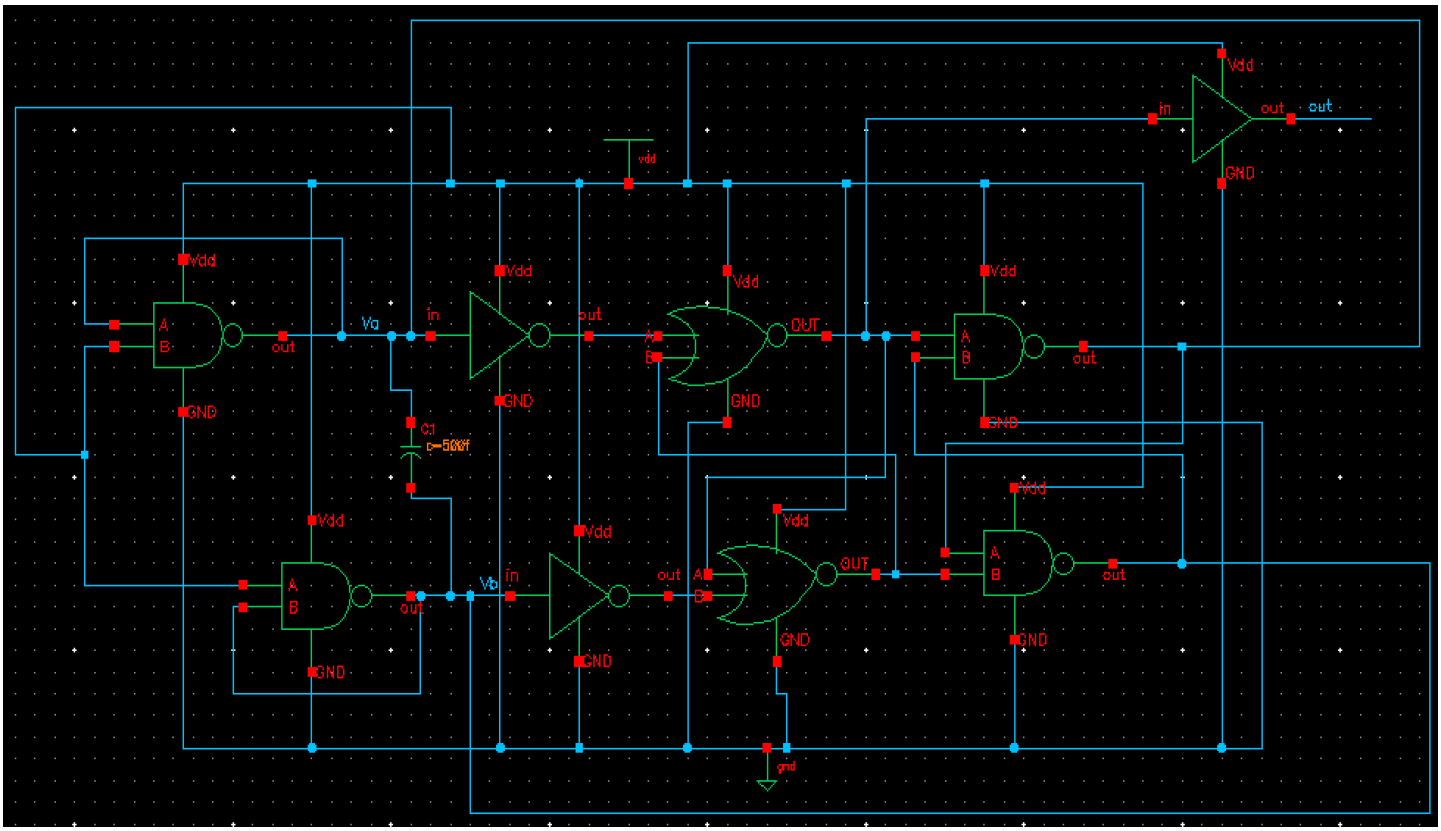


Figure 3.41 Schematic symbol architecture of relaxion oscillator without DLS implementation

To test this configuration, I imposed the same parameter as for the relaxion oscillator with DLS (V_{DD}=400mV, C=500fF), the result frequency is f = 113,62 kHz. Of course, this value is not acceptable so even if the area is bigger the best option between these two oscillators is the one with DLS implementation.

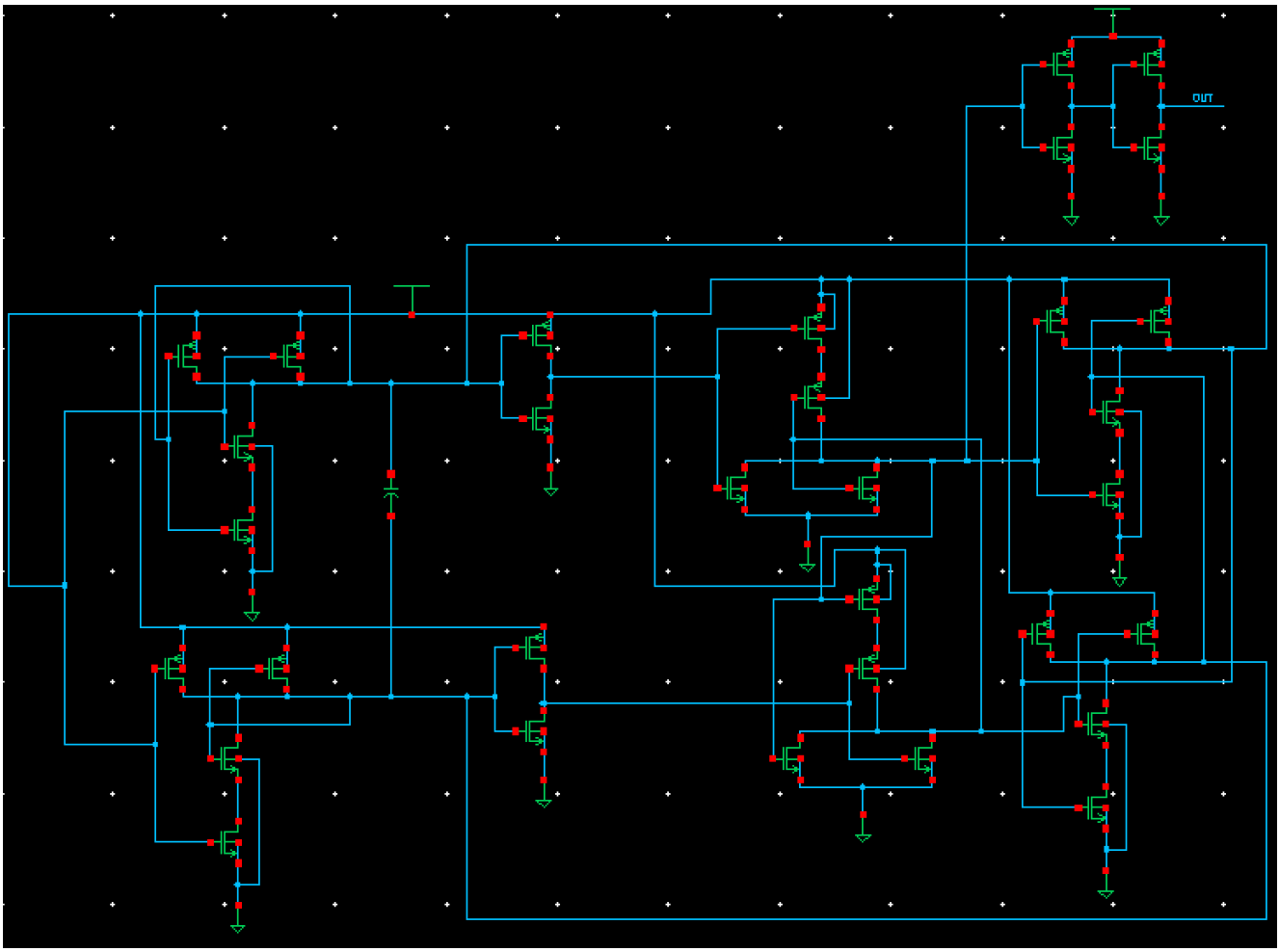


Figure 3.42 Schematic transistors configuration of relaxion oscillator without DLS implementation

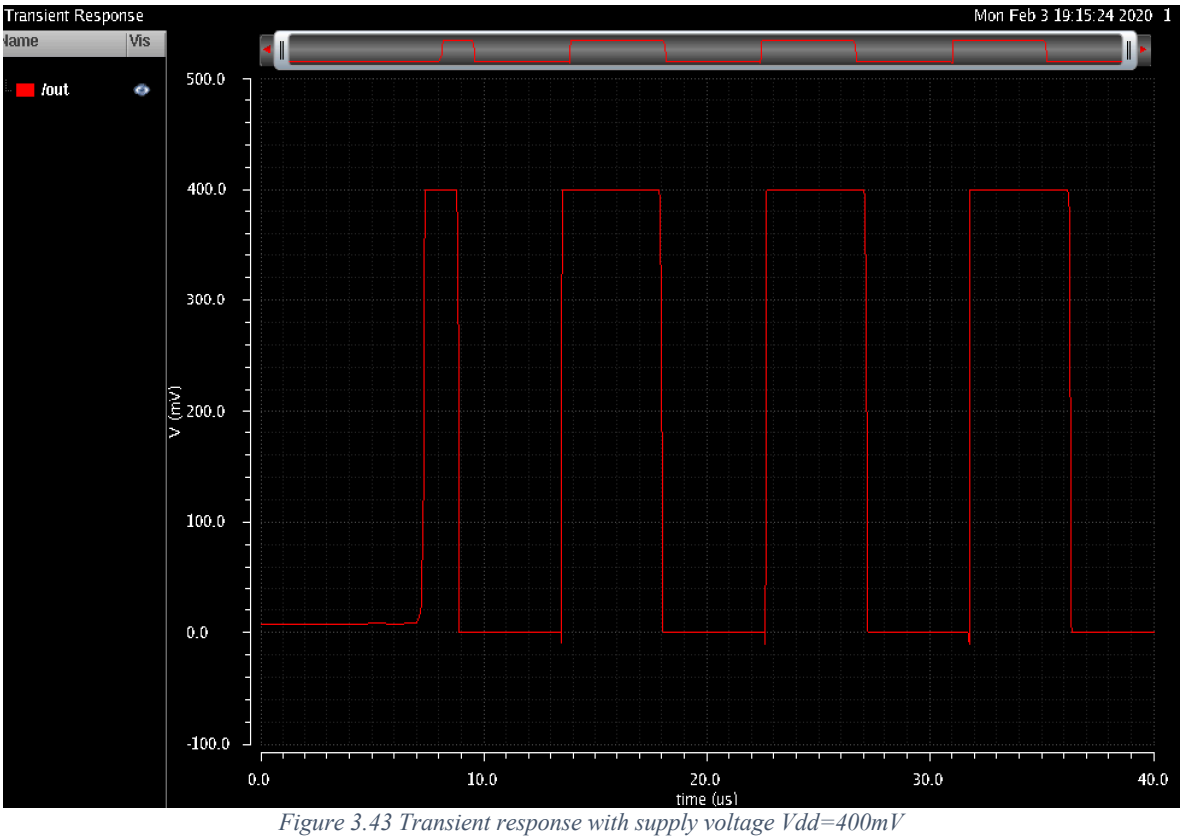


Figure 3.43 Transient response with supply voltage Vdd=400mV

CHAPTER 4

FREQUENCY AND AREA OPTIMIZATION

Four different architectures were implemented and tested in Cadence Virtuoso imposing, as a first simulation, minimum sizes for all the components and supply voltages compatible with the ranges provided by the papers. From the results already presented, it is evident that for now there is none configuration that allows a sub-Hz frequency oscillation. For this reason, the next step in my work was to try to find a solution by keeping into consideration that the mHz frequency range is not the only limit to respect, because the total area occupied by the oscillator and all the other components of the multiplexer need to be less than 100 μm^2.
What I will present now are all the simulations done to reach the wanted period of the oscillating wave, trying to optimize the area and considering as a starting point what is summarized in Table 4.1.

Oscillator	Vdd	C	R	n° transistors
Timer with gate leakage	450 mV	500 fF	1 kΩ	15
Voltage controlled oscillator	400 mV 1,8 V	500 fF	\	14
Relaxion oscillator with DLS	400 mV	500 fF	\	52
Relaxion oscillator without DLS	400 mV	500 fF	\	32

Table 4.1 Parameters imposed for testing the four architecture and the corresponding frequency

4.1 SIMULATION TESTS

For each oscillator I decided to work on two main elements: the transistors sizes (length and width) and the capacitance value. All the simulations were done keeping into consideration the values allowed by the PDK of Cadence. As I will show in the next sections, the maximum limits defined by the software are over the total area acceptable for the “Body Dust” application but still, I wanted to verify how much the frequency depends on certain parameters.

4.1.1 SIMULATION TESTS: LOW POWER TIMER

For the first architecture I already disclosed that, unfortunately, there were some problems to obtain exactly the same results proposed in [3.1]. In this paper there were no precise indications about the ratio $\frac{W}{L}$ between the width (W) and the length (L) of the transistors, except for three main elements in the configuration: "MC1 and MC2 are thin oxide MOS capacitors […]. The load capacitance ML1 is implemented with thick gate oxide transistor". So, first of all, I tested the transient response of the oscillator trying to simulate three capacitors, changing appropriately the sizes of the transistors. However, I couldn't obtain any oscillation. After this failure I decided to make safer simulations changing these three transistors with two resistances in parallel connected to a capacitor (Figure 4.1).

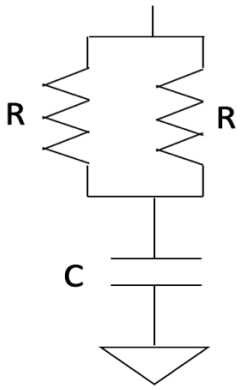


Figure 4.1 Parallel resistance connected to a capacitor to substitute the three transistors in oscillator architecture

Even if in [3.1] is specifically described that the two transistors MC1 and MC2 (Figure 3.19) act like two capacitors, it is also specified that they need to have thin oxide gates. According to the usual design for transistors, if they are characterized by long and thin gates they act more like resistances, so I preferred to implement them like this.
The first two simulations to see how the frequency change were done increasing the resistances and the capacitance values.

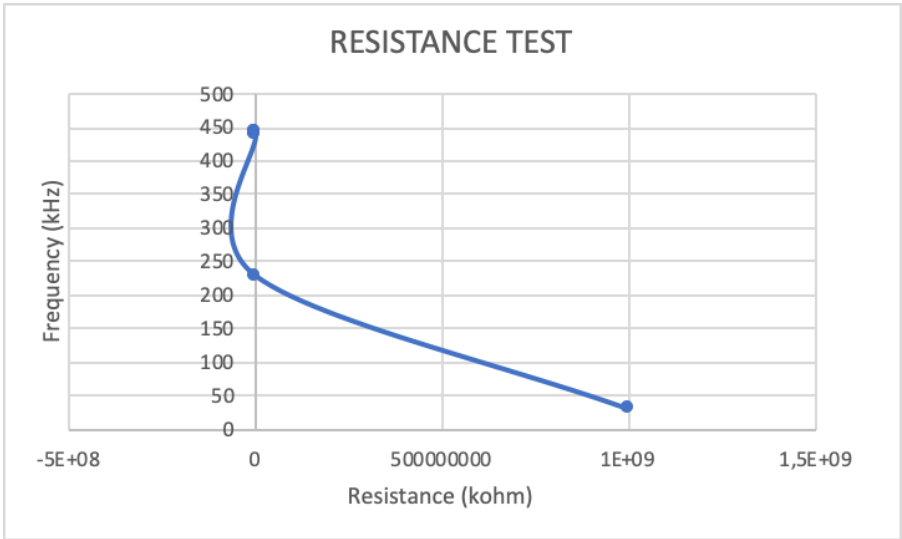


Figure 4.2 Frequency change by increasing resistances values

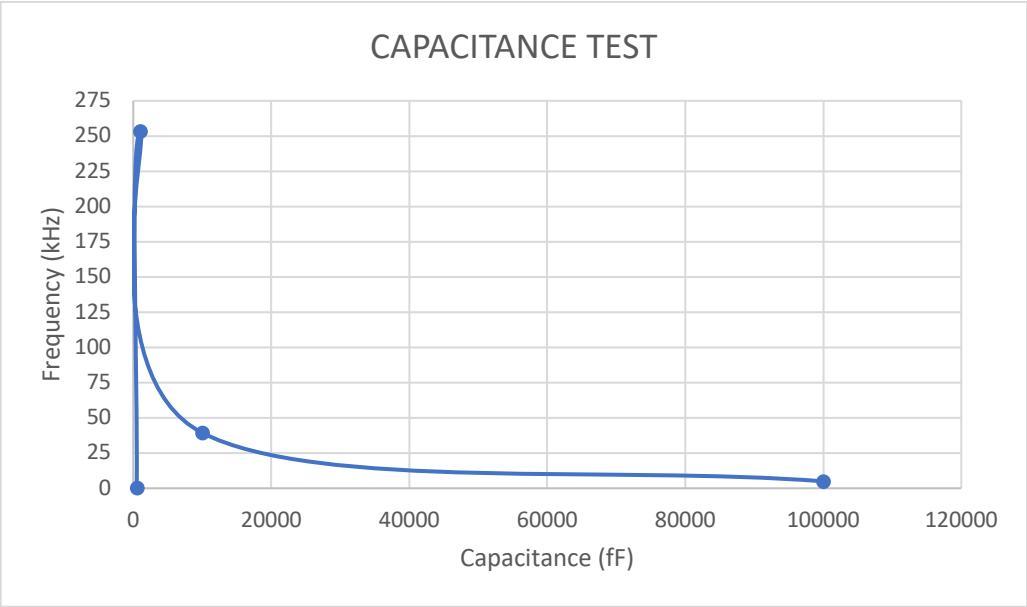


Figure 4.3 Frequency change by increasing capacitance value

From these two graphs there is a significant reduction of the frequency in both cases: by changing the two resistances values is possible to reach tens kHz of frequency, while by changing the capacitance a few kHz. Of course, these results are very far from the sub-Hz range desired as well as from the area of 10X10 μm^2.
Then I tried to work on the ratio $\frac{W}{L}$, at first by changing the length then by increasing the width. The results are shown in Figure 4.4 and Figure 4.5.

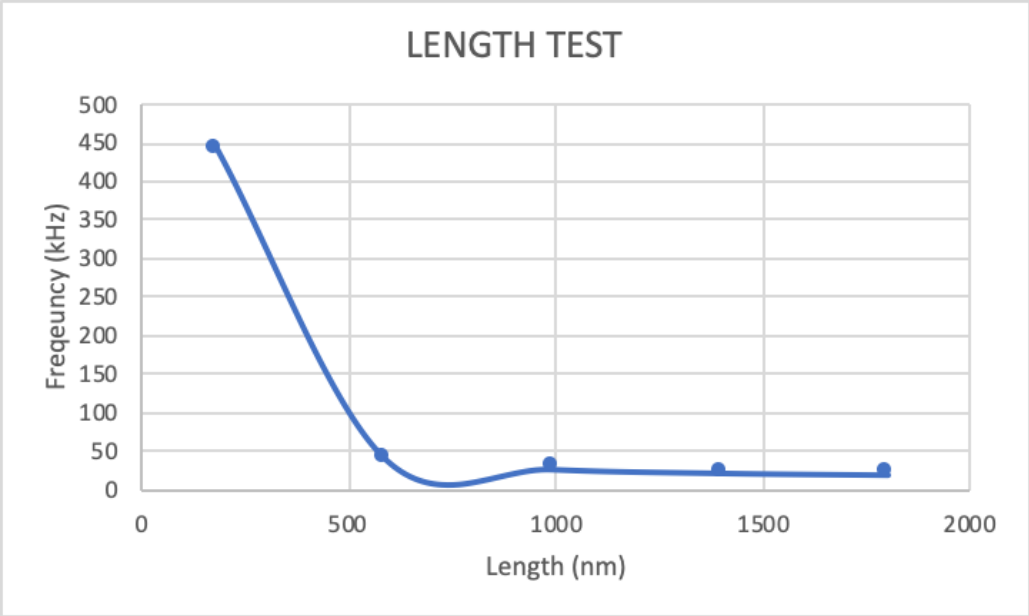


Figure 4.4 Frequency change by increasing transistors length

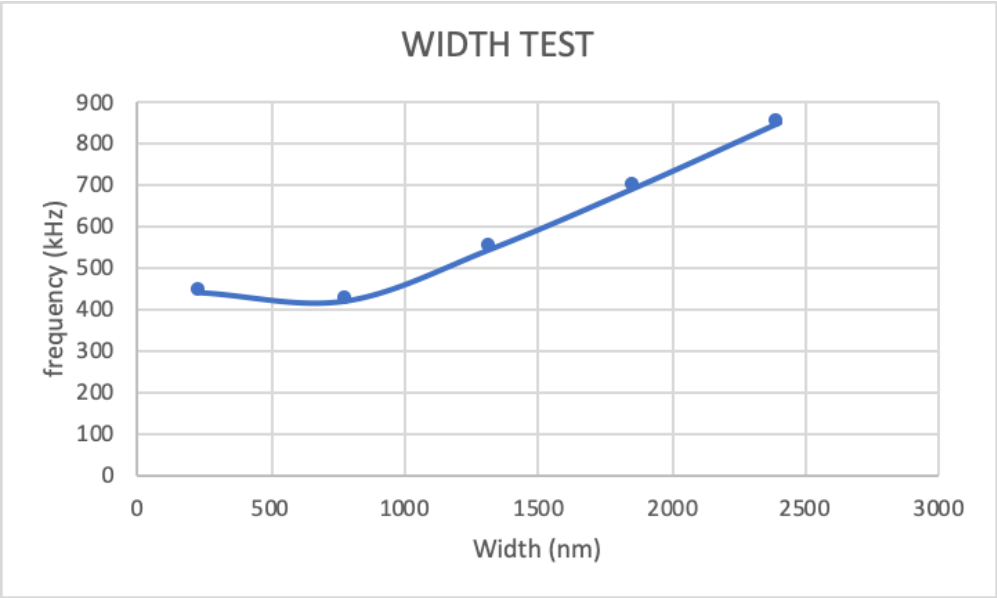


Figure 4.5 Frequency change by increasing transistors width

By changing the length is possible to notice a similar improvement as for the resistances, while by increasing the width the effect is the opposite: in fact, the frequency goes up over 850 kHz.

4.1.2 SIMULATION TESTS: VOLTAGE CONTROL OSCILLATOR

Like the name suggests, this oscillator is dependent on the voltage supply and for this reason I tested how its frequency changes according to Vdd. In particular I take as voltage limits: 400 mV and 1,8 V. The first is in the same range as for all the other oscillators, the second is the typical voltage used in 180 nm technology.
Even this time, I tried to increase the ratio $\frac{W}{L}$ and change the capacitance value.

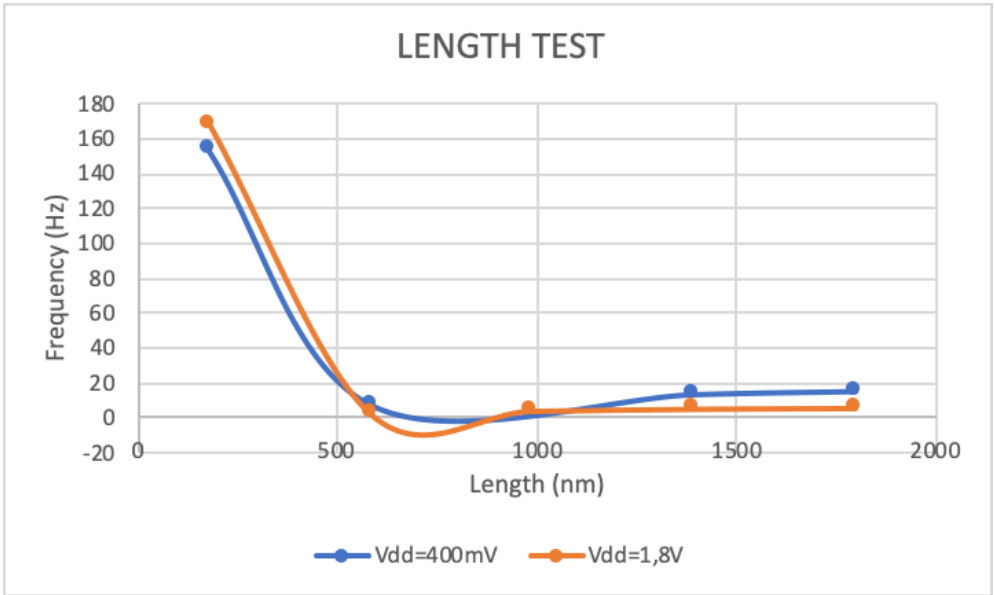


Figure 4.6 Frequency change by increasing transistors length with supply voltages of 400mV and 1,8V

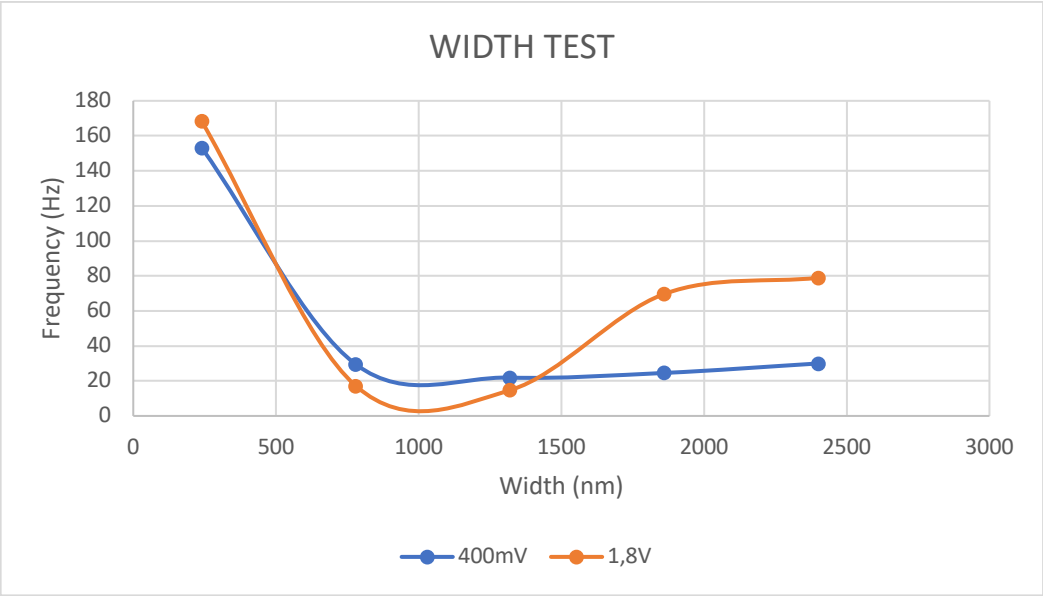


Figure 4.7 Frequency change by increasing transistors width with supply voltages of 400mV and 1,8V

Starting from the frequency change with transistors length, shown Figure 4.6, the results are more promising than the previous timer. In particular a few Hz frequency range is reached: the best length for both voltage supply cases is L=585nm obtaining $f_1 = 7{,}69\ Hz$ (Vdd=400mV) and $f_2 = 1{,}823\ Hz$ (Vdd=1,8V). By further increasing the length of the transistors the frequency starts to increase as well.
In Figure 4.7 are presented the results obtained changing the width, and again is possible to notice an improvement in the frequency till a certain value, after that it starts again to increase. Also in this case, with a supply voltage of 1,8V, there is the best result of a few Hz but, even with Vdd=400mV the frequency remain around 20 Hz.
In the last, I also tried to change the capacitance value from 200 fF to 1 pF. The results are shown in Figure 4.8.

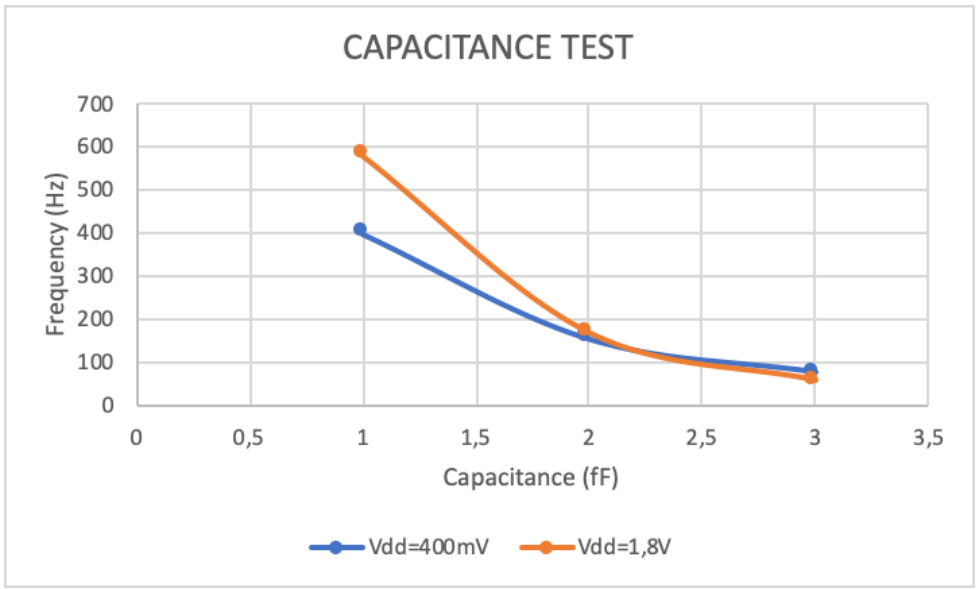


Figure 4.8 Frequency change by increasing capacitance value with supply voltage of 400mV and 1,8V

4.1.3 SIMULATION TESTS: RELAXION OSCILLATOR

Starting from the configuration explained in [3.3] I developed the same oscillator with and without the DLS logic style in order to compare the final frequency. In [3.3] were already expressed the appropriate length and width for all the transistors, as well as the voltage supply and the capacitance value to obtain the best compromise between area and frequency. In fact, by testing this oscillator, implemented using DLS logic the frequency swung between 3,47 Hz and 5,16 Hz. Besides, considering the high number of transistors in this architecture, the fact that these frequencies are reached using minimum sizes and a capacitor of 500 fF, is already a good result.
For this reason, I tried to accomplish the same using the other configuration, implemented without DLS logic gates. Once again, the simulations were done changing the capacitance value and the ratio $\frac{W}{L}$.

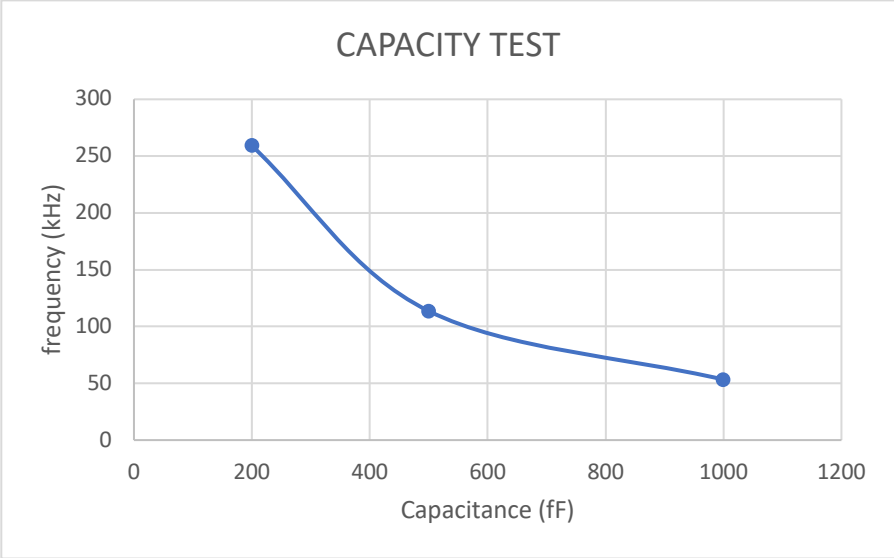


Figure 4.9 Frequency change by increasing capacitance value

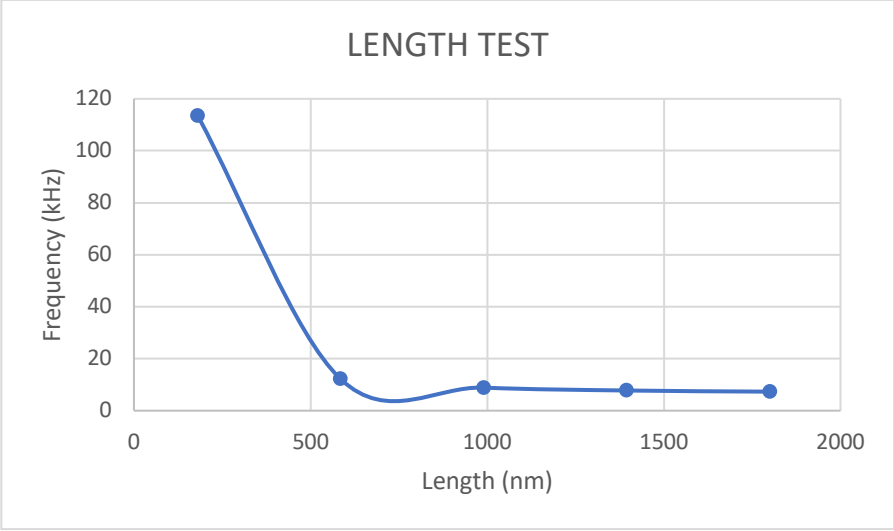


Figure 4.10 Frequency change by increasing transistors length

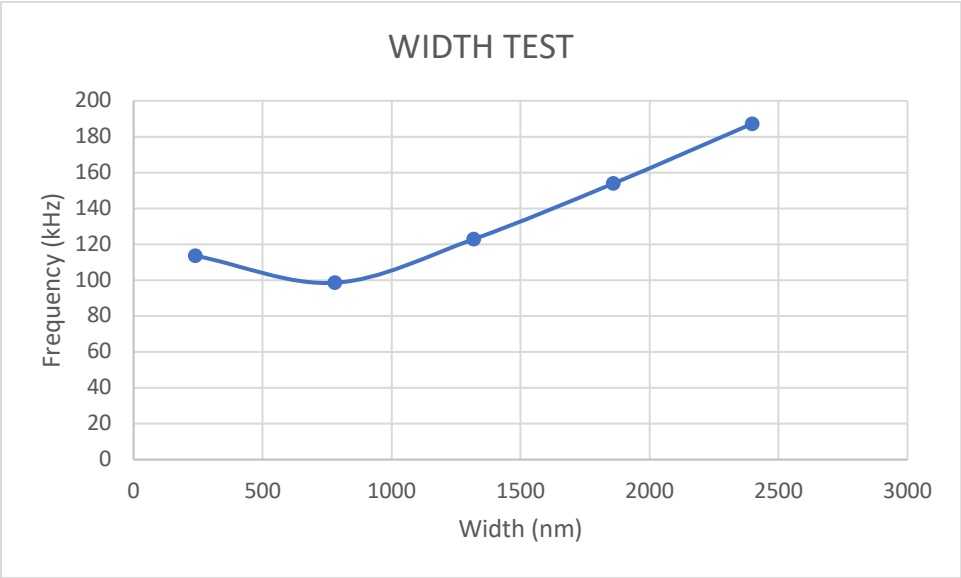


Figure 4.11 Frequency change by increasing transistors width

Simulation's results show the best improvement by increasing the length of the transistors (from 113,624 kHz with L=180nm to around 7 kHz with L=1800nm) even if these frequencies are still not acceptable for our purpose. A width over 780nm instead, will generate an opposite effect and the changes in the overall frequency are almost negligible. Lastly, increasing more the capacitance value would be inefficient, because the bigger the capacitor is, the bigger is the total area occupied by the component itself.
After all these attempts, I concluded that only by working on the transistor's sizes, the capacitance values and the supply voltages is not possible to reach a mHz frequency oscillation using 180 nm technology. The best frequency results for each oscillator, without taking into consideration the area occupied, are summarized in the Table 4.2 below.

Oscillator	Vdd	C	R	Sizes	f
Timer with gate leakage	450 mV	100 pF	1 kΩ	L=180 nm W=240 nm	4,938 kHz
Voltage control oscillator	1,8 V	500 fF	\	L=585 nm W=240nm	1,823 Hz
Relaxion oscillator with DLS	400 mV	500 fF	\	L=180 nm W=240 nm	~ 4 Hz
Relaxion oscillator without DLS	400 mV	500 fF	\	L=800nm W=240nm	7,321 Hz

Table 4.2 Best frequency results for each oscillator with respective parameters

4.2 ALTERNATIVE SOLUTION

The last section unfortunately didn't show the wanted results but, for both the voltage control oscillator and the relaxion oscillator with DLS logic style, the final frequencies are very promising. For the first architecture $f_1 = 1{,}823\ Hz$, using the minimum width and an acceptable length, in the second case $f_2 \sim 4\ Hz$ with minimum sizes for all the transistors. With the prospective to respect the area boundary, an alternative solution to decrease the frequency of these two oscillators, is to create a frequency divider. In fact, considering the best case of f_1, with a ten stages frequency divider is possible to obtain a mHz frequency oscillation ($2^{10} = 1024$ so $\frac{2\ Hz}{1024} = 2\ mHz$).
To build a frequency divider the basic element is the flip-flop. Traditional configurations use flip-flop D or flip-flop JK, like in Figure 4.12.

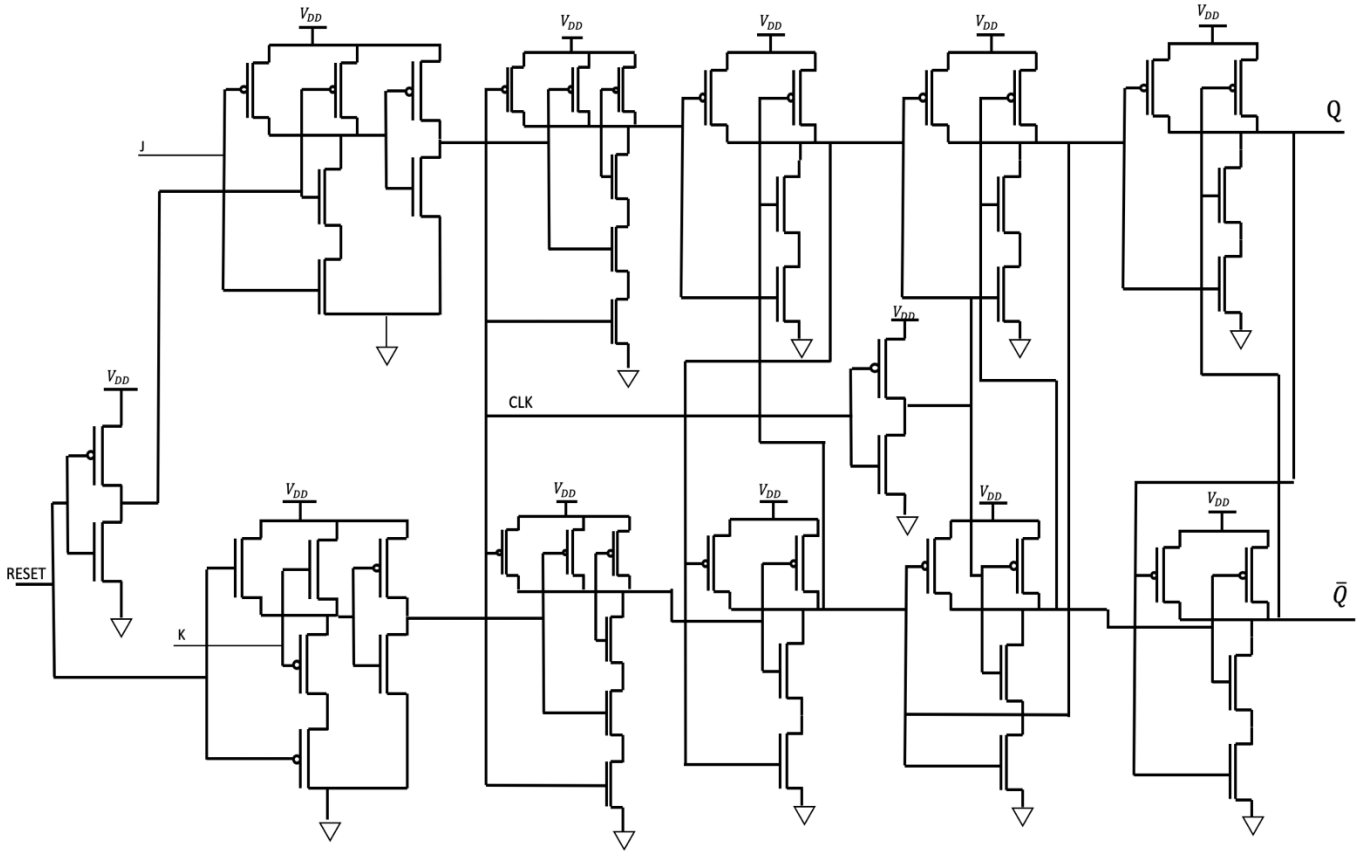


Figure 4.12 Schematic configuration of flipflop JK with RESET input

Using a flip flop JK is possible to realize an asynchronous counter, in which the output Q of each stage is the clock signal of the next block (Figure 4.13). In this way at each step there is a delay that makes the counter works as a frequency divider (Figure 4.14).

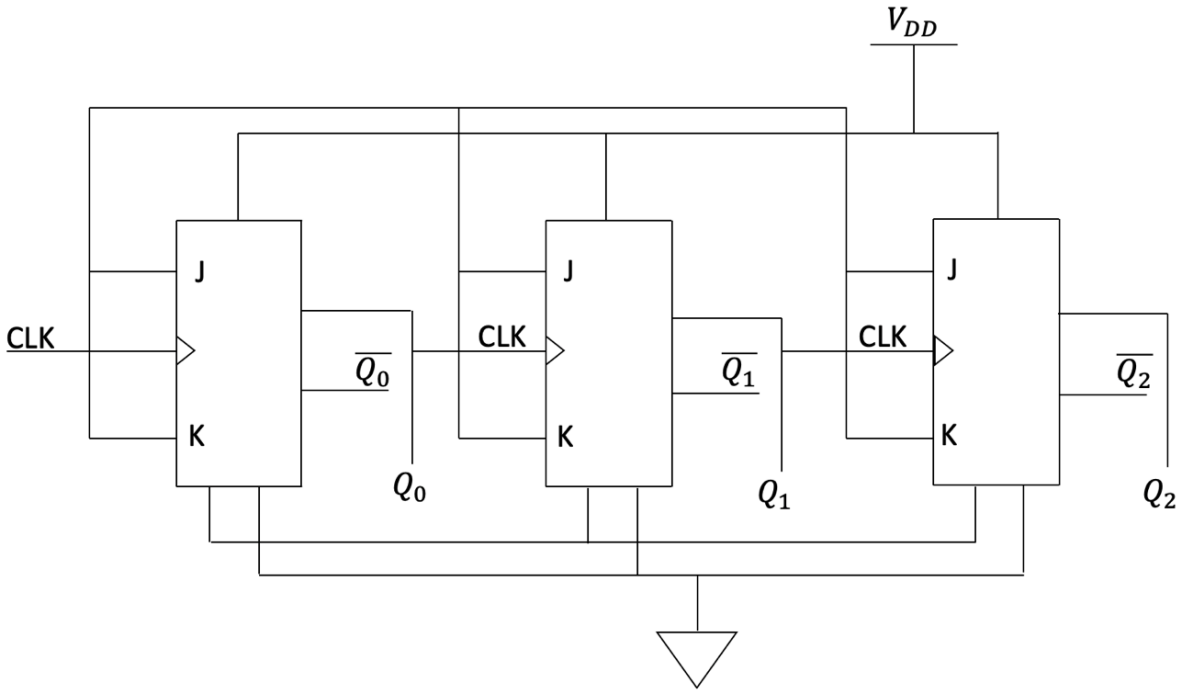


Figure 4.13 Schematic diagram od frequency divider implemented using flipflop JK

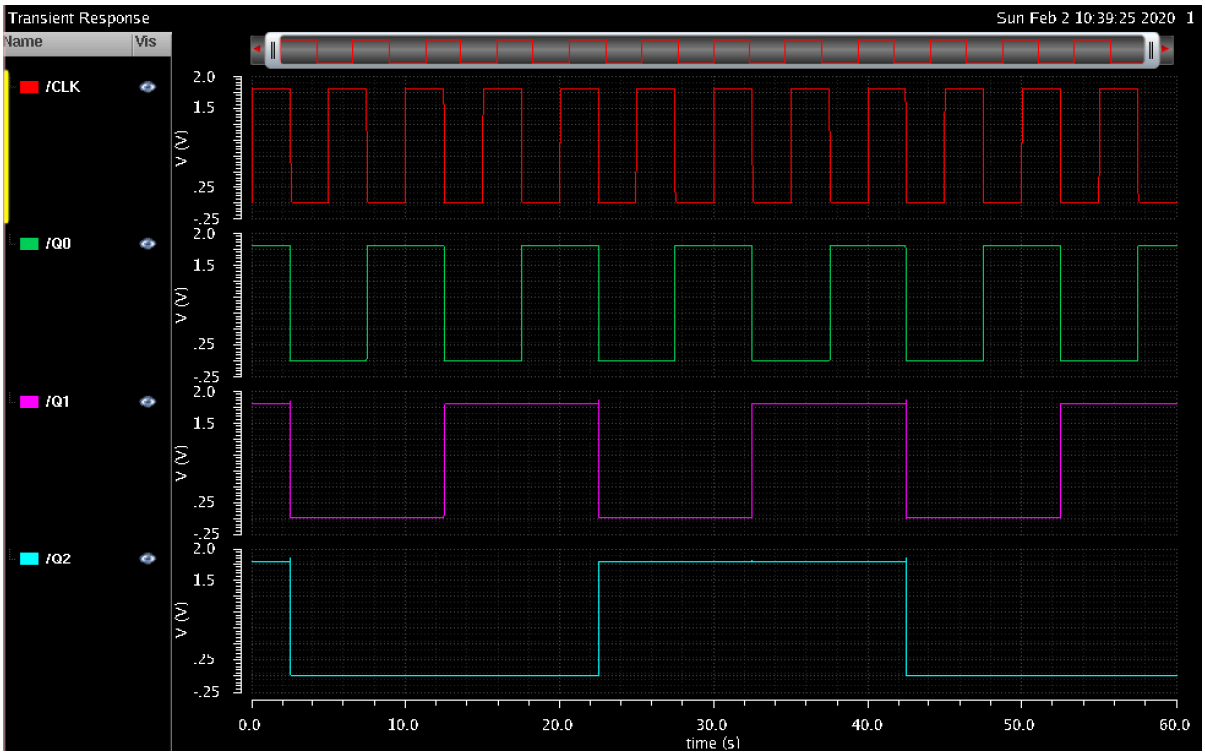


Figure 4.14 Transient response of asynchronous counter with square wave input

Therefore, the architecture implemented in this way requires an elevate number of transistors, in particular 52. There is a main problem that derived from this architecture: the total area occupied by the counter, because 52 flip-flops are way too much for the 10X10 μm^2 constrain considered.

For this reason, I tried to implement another frequency divider using one of the smallest flip-flops in literature: the TSCP flip-flop. Its configuration and transient response are shown in Figure 4.15 and Figure 4.16.

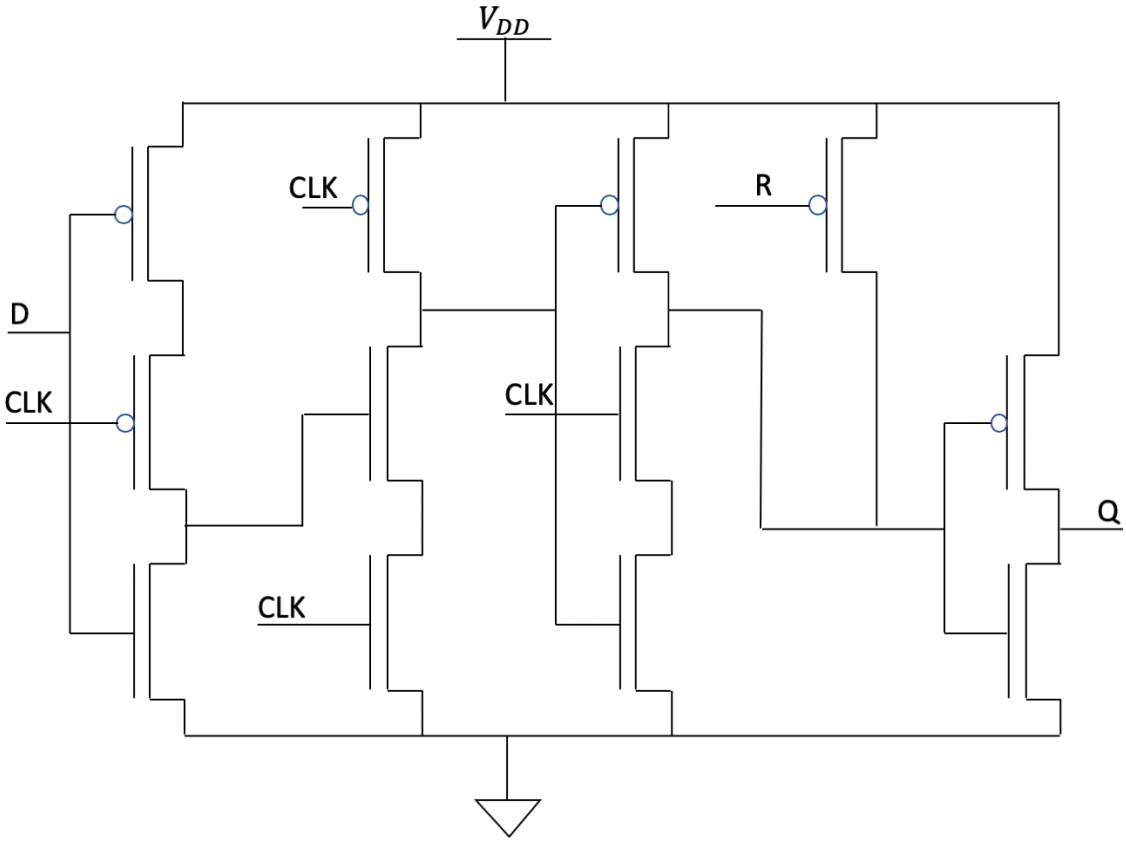


Figure 4.15 Schematic configuration of TSCP flipflop

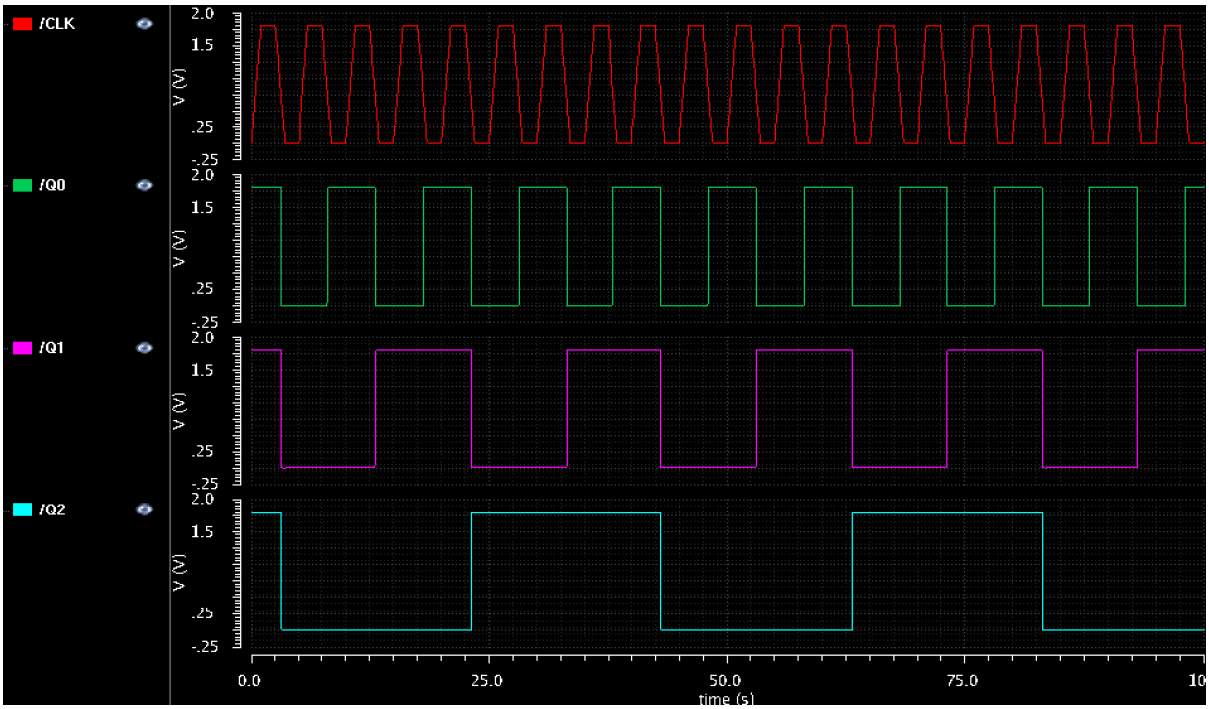


Figure 4.16 Transient response of frequency divider implemented with TSCP flipflops

The total number of transistors in TSCP flip-flop is considerably less than the case before. Therefore, analyzing the layout configuration, each TSCP flip-flop has an area of 77,812 μm^2, using minimum sizes for all the elements (Figure 4.17). This means that if I want to reduce the frequency from 2 Hz to 2 mHz, with ten stages of TSCP flip-flop, the total area occupied only by the frequency divider will be around 778 μm^2, way too much.

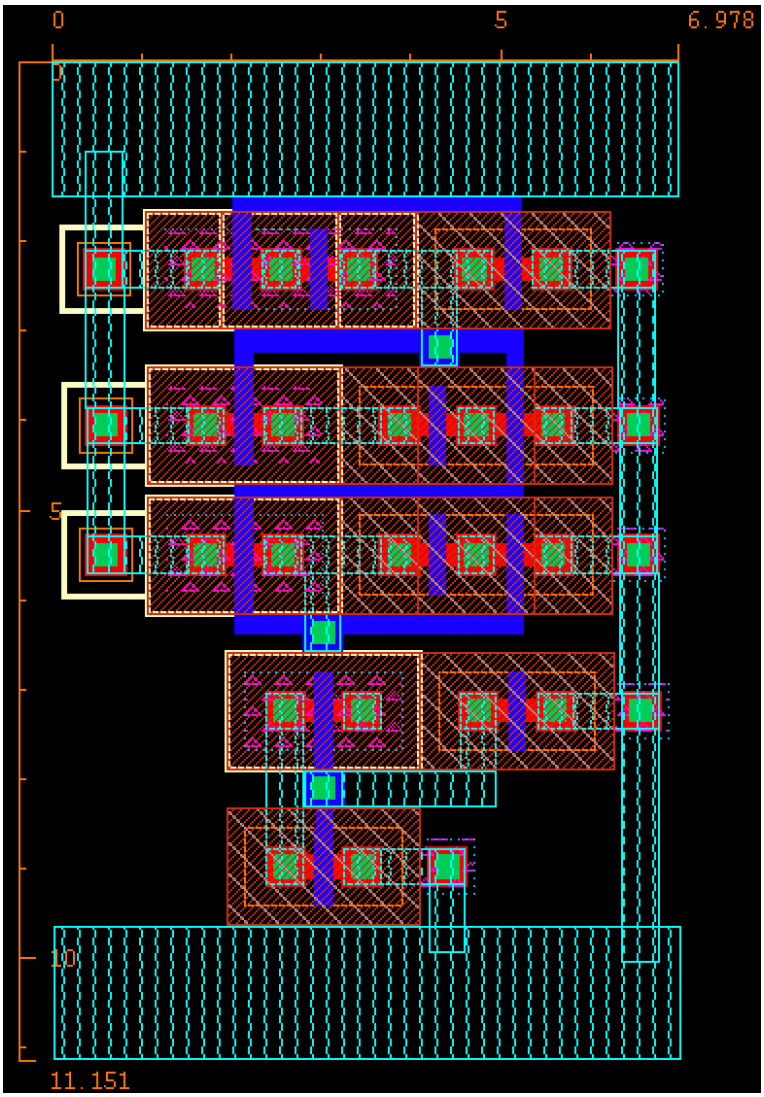


Figure 4.17 Layout configuration of TSCP flipflop

So, the area is a very restrictive factor if combined with the sub-Hz frequency investigated in my research. Developing the circuit with 180 nm technology, the minimum sizes of length and width for the transistors bring to very big areas for the "Body Dust" application. Because of that, the implementation of a frequency divider, is not a possible solution starting from the frequency values obtained with the four oscillators described before.

At this point, in order to have a clearer idea of how to proceed it is fundamental to create the layout configuration of each oscillator, to define their minimum area and so know which fringe is still available and what is the best way to use it.

4.3 LAYOUT AND AREA DEFINITION

For every oscillator I created its layout configuration. In this way, like I already explained, is possible to know the real area occupied just by the oscillator, considering minimum sizes for every transistor, and so make the right changes to decrease its frequency. To create the layout design of the three configurations with a capacitor in their architecture, I decided to use a standard value for all of them, equal to 500 fF. For the relaxion oscillator it's the capacitance value necessary to obtain the 4 Hz oscillating frequency, like for the Voltage Controlled Oscillator it is the one used to reach 2 Hz. In the following figures I will show the four layout configurations.

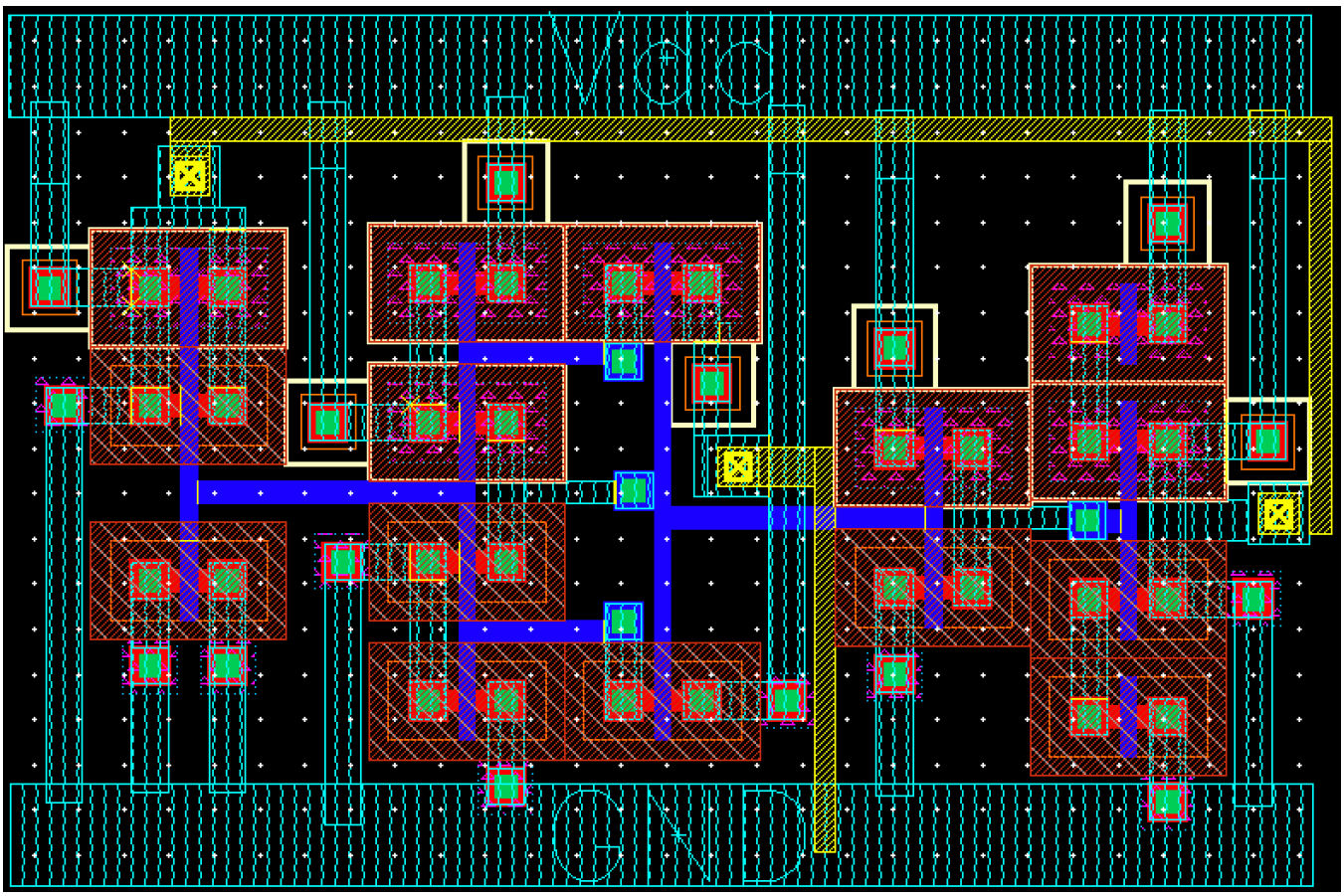


Figure 4.18 Layout configuration of one hot timer using gate leakage

In Figure 4.18 it's represented the one hot timer layout configuration that I decided to implement, according to the literature, with 15 transistors even if, like I discussed before, in order to make it works its necessary to replace the three transistors on the left (one pMOS and two nMOS) with two resistances in parallel, connected with a capacitor. Therefore, because the goal of this simulation was to understand the minimum area of each architecture, I decided to not consider these changes and analyze the standard configuration. The area measured from this layout is 107,392 μm^2.

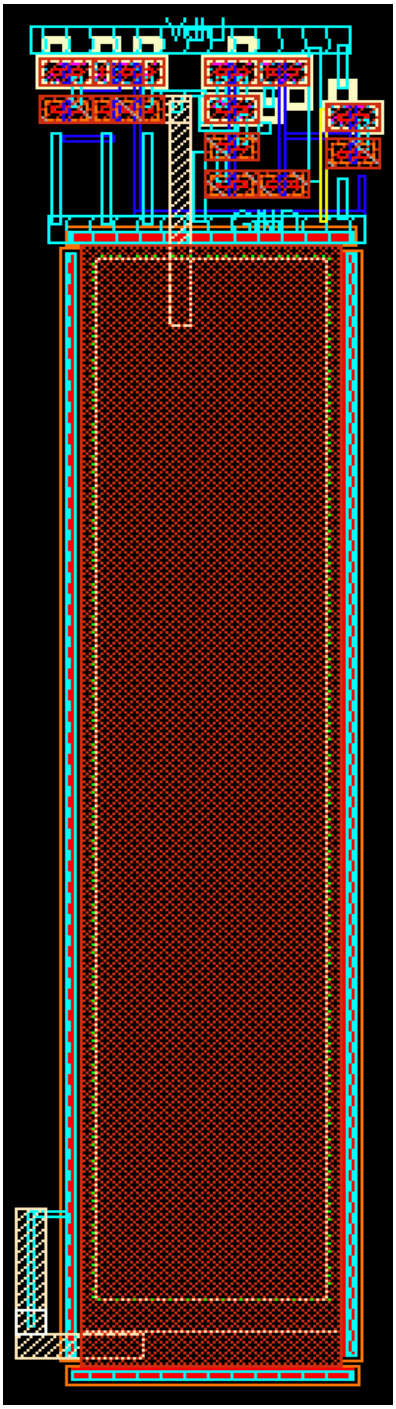


Figure 4.19 Layout configuration of the Voltage Controll Oscillator with a capacitance value of 500fF

In Figure 4.19 is shown the layout configuration of the Voltage Controlled Oscillator (VCO).
It consists in 14 transistors and one capacitor. For all the transistors I imposed a length of 180 nm and a width of 240 nm while for the capacitance 500 fF. It is evident that most of the area is occupied by the capacitor. In fact, alone it takes 580,14 μm^2. This means that with only the capacitor the oscillator exceeds the maximum area allowed by the initial constrains imposed on the circuit.
The total area, considering also the transistors, is 819,582μm^2.

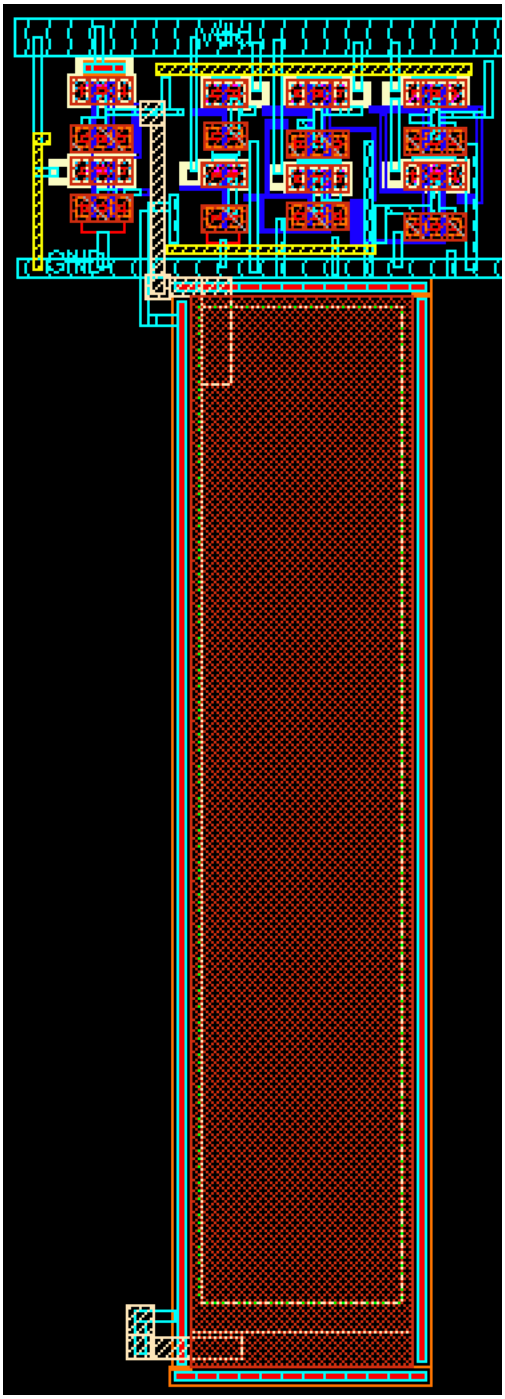


Figure 4.20 Layout configuration of the relaxion oscillator without DLS and a capacitance of 500fF

In Figure 4.20 is shown the layout configuration of the relaxion oscillator without DLS logic style.
It consists in 32 transistors, again designed with minimum length and width, and a capacitor of 500 fF. As expected, the biggest element in the configuration is the capacitor itself, which occupies more than half of the total area that is 1396 μm^2.

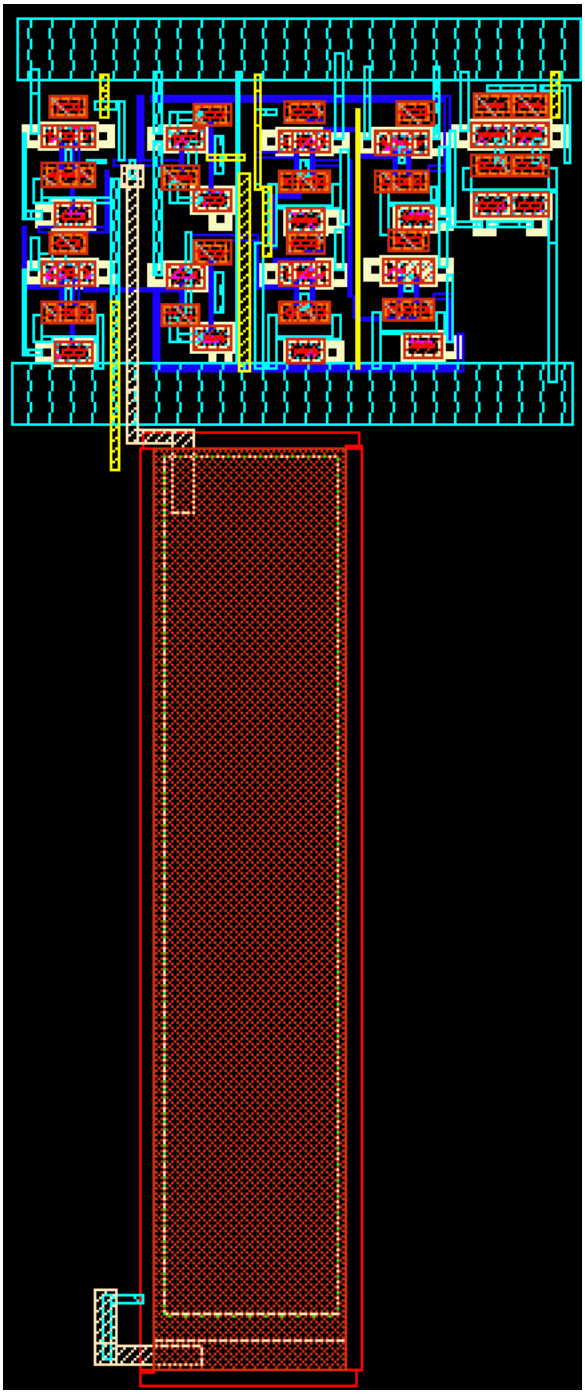


Figure 4.21 Layout configuration of relaxion oscillator with DLS logic style and a capacitor of 500fF

In Figure 4.21 is shown the layout configuration of the relaxion oscillator with DLS logic style.
It consists in 52 transistors and a capacitor of 500 fF. As expected it is the most expensive in term of area occupied, seeing the elevate number of transistors. In this case the total area is of 1600 μm^2.

From the simulations done till now, emerged the great effort needed to combine restrictive boundaries like the ones for the "Body Dust" project. The research I've done in literature, brought me to studied four of the most promising configurations in the environment of low frequency oscillators, which therefore didn't allow to obtain the wanted results. For this reason, I tried to study more deeply these configurations searching for a suitable solution for both the area restriction and the oscillation frequency, by changing the length and the width of the components. It was not enough, so the next step was to analyze how much the presence of a capacitor can influence the

output frequency. With all these attempts the best results brought to a value of a few Hz. From this point on I tried alternative solutions using frequency dividers to reduce the period of the output oscillation. However, even if by using these tools is possible to reach the desired frequency, the layout analysis of the flip-flops, which constitute the asynchronous counters, highlights the impossibility to use them because of the big area occupied. In the end, in order to understand how much the architecture of each oscillator can be changed and which type of solutions can be implemented to reduce their frequency, I realized the layout of the four configurations to study their minimum area. The results are summarized in the following Table 4.3.

Oscillator	n° of transistors	n° of capacitors	Total Area (μm^2)
Timer with Gate Leakage	15	\	107,392
Voltage Control Oscillator	14	1	819,582
Relaxion Oscillator without DLS	32	1	1396
Relaxion Oscillator with DLS	52	1	1600

Table 4.3 Overall number of elements for each oscillator and corresponding total area

It can be deduced that none of the configurations studied allow to respect the 10X10μm^2 of lateral area, even with the minimum values the PDK defined at 180 nm. For this reason, I can conclude that with a 180 nm technology is not possible to develop a multiplexing layer which can guarantee a switch frequency from one channel to another enough slow, to allow the concentrations measurement of endogenous and exogenous molecules and at the same time is hold in a 10X10μm^2 area.
A possible path to chase is the reduction of the technology used to implement these oscillators. In fact, with a lower technology the overall area will be reduced but it's necessary to know how the frequency change according to this.

CHAPTER 5

CLOSE TO A POSSIBLE SOLUTION

The first and main part of my work was concluded with the awareness that, with 180nm technology, is not possible to implement an oscillator that respects all the wanted properties. However, even if is not possible to do it in this way, it doesn't mean it can't be done using, for example, a different technology which can reduce the overall sizes of the components and so the total area of the circuit. For this reason, I developed all the architectures tested till now, using a 28nm technology. The hope was that, by using different sizes for each element, will be possible to reach the final aim. In particular, what I did, was to start a work that needs to be deepened in more detail, just to verify if the path of a lower technology can really be a possible solution to follow or if it's better to completely change the approach.
In the next sections I will chase again the same steps I did for implementing and simulating the four architectures, already developed in 180nm but, this time using a 28nm technology.

5.1 TECHNOLOGY REDUCTION: 28nm IMPLEMENTATIONS

To implement again all the oscillator's configurations, I used "Cadence Virtuoso tsmc28nm". According to the new technology rules the sizes for every element are different than what was defined in 180nm. In particular, for transistors the minimum length is 30nm while the minimum width is 100nm (as compared to 180nm length and 240nm width in the previous technology).

5.1.1 LOGIC GATES

Of course, the first step to develop all the architecture, was to create again all the basic components necessary to do that: the logic gates. So, I create from the beginning all the ports needed, analyzing their working mode through the transient response and measuring their area through the layout configuration, for both the standard implementation and the DLS one.
In the following figures I will briefly show all the gates, starting from the ones without DLS and then the others with logic style.

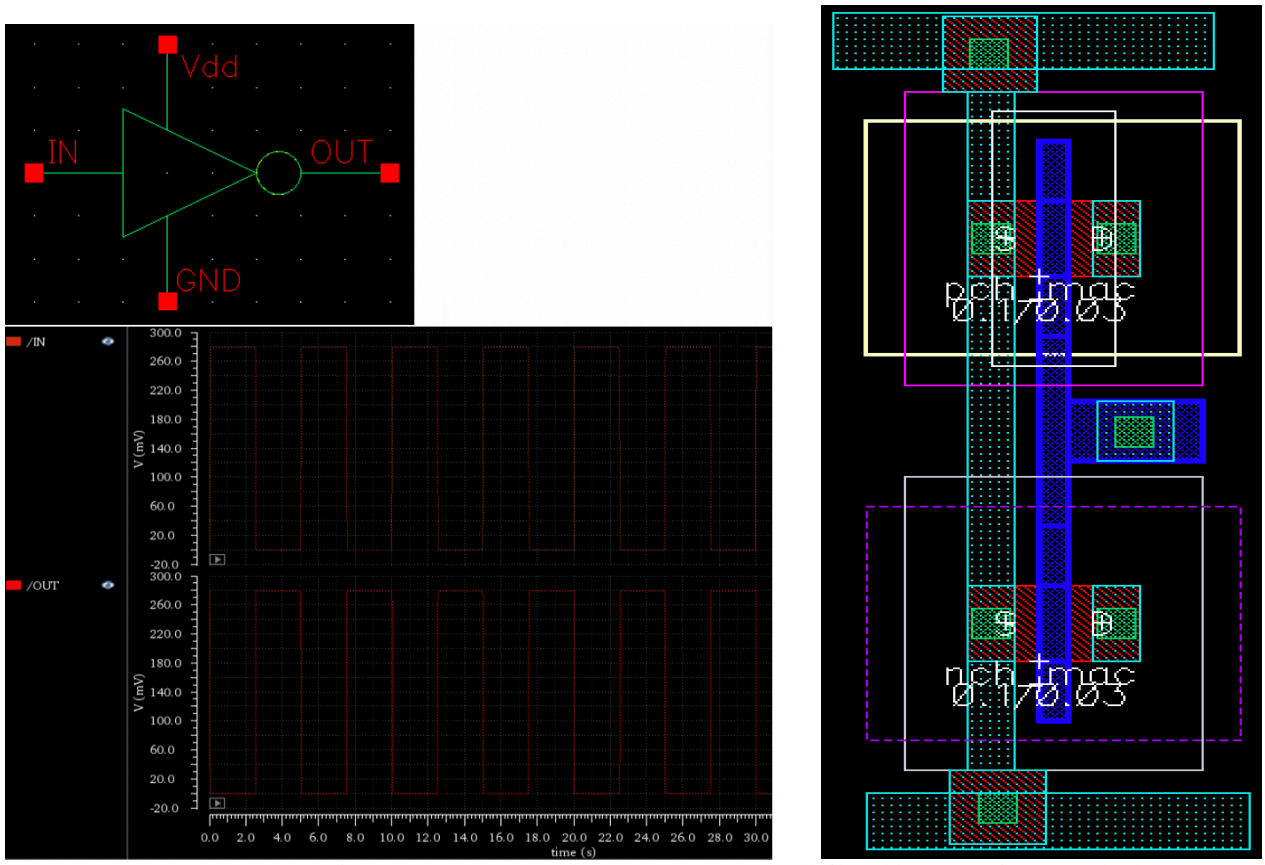


Figure 5.1 Inverter implementation in 28nm with its transient response (left) and layout configuration (right)

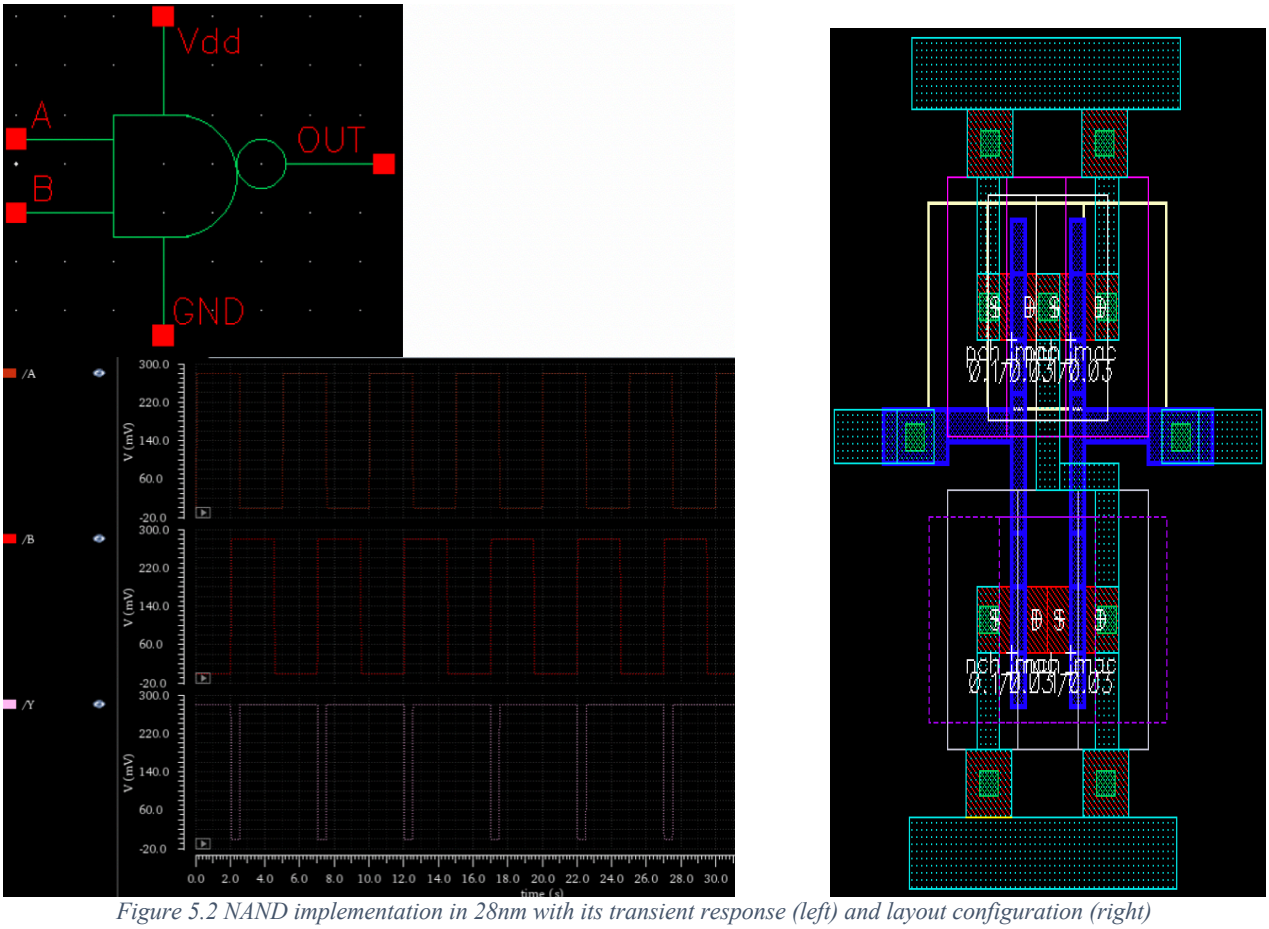


Figure 5.2 NAND implementation in 28nm with its transient response (left) and layout configuration (right)

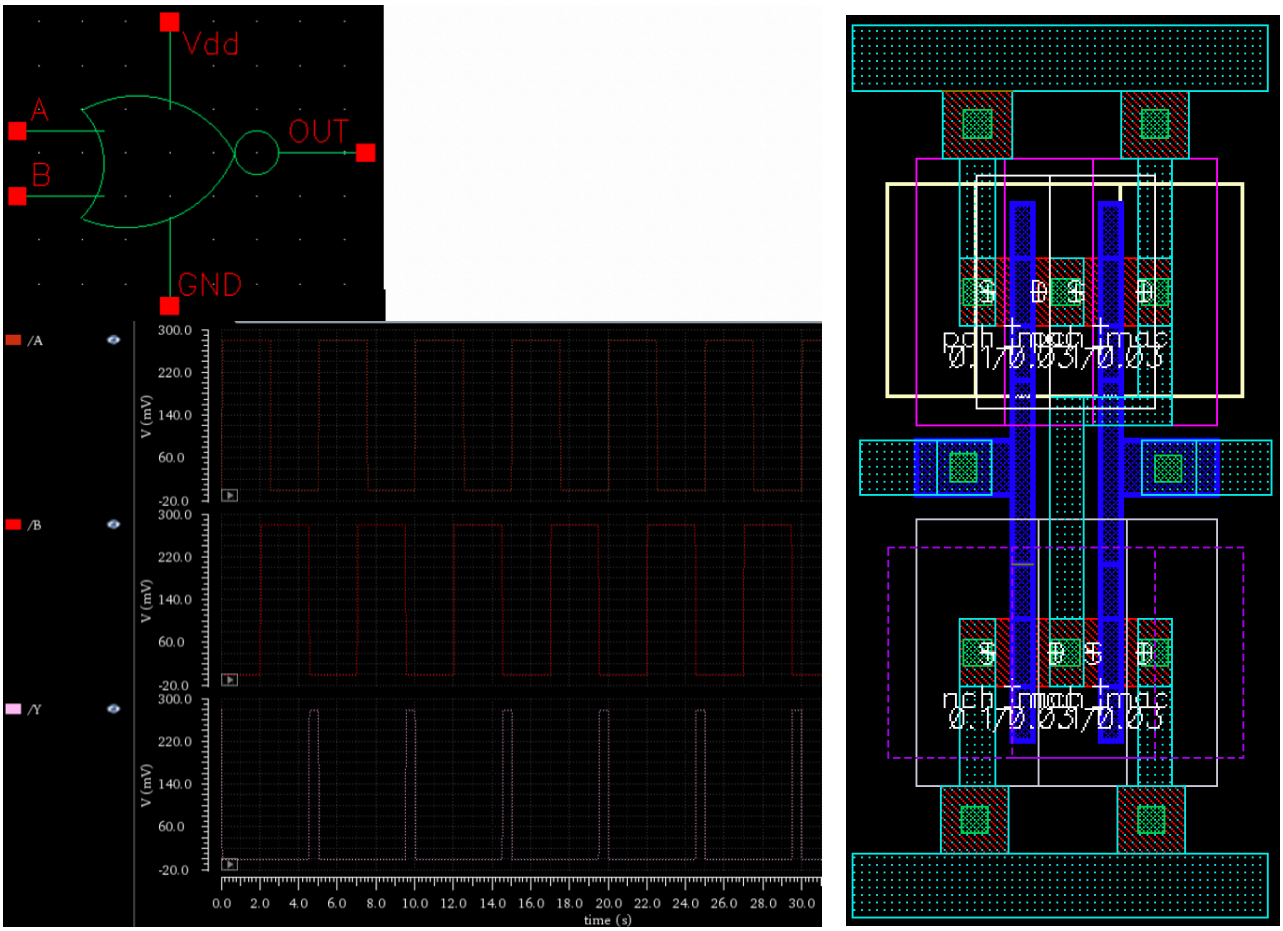


Figure 5.3 NOR implementation in 28nm with its transient response (left) and layout configuration (right)

From the analysis of the layout configurations, the area occupied by each logic gate is considerably lower than in the implementation using 180nm technology. The measurements are summarized in the following Table 5.1.

AREA COMPARISON BETWEEN 180 nm AND 28nm		
Logic Gate	Technology	Area (μm^2)
NOT	180nm	10,929
	28nm	0,425
NAND	180nm	15,792
	28nm	0,58
NOR	180nm	15,792
	28nm	0,58
BUFFER	180nm	24,898
	28nm	0,827

Table 5.1 Logic Gate's area comparison: 180nm VS 28nm

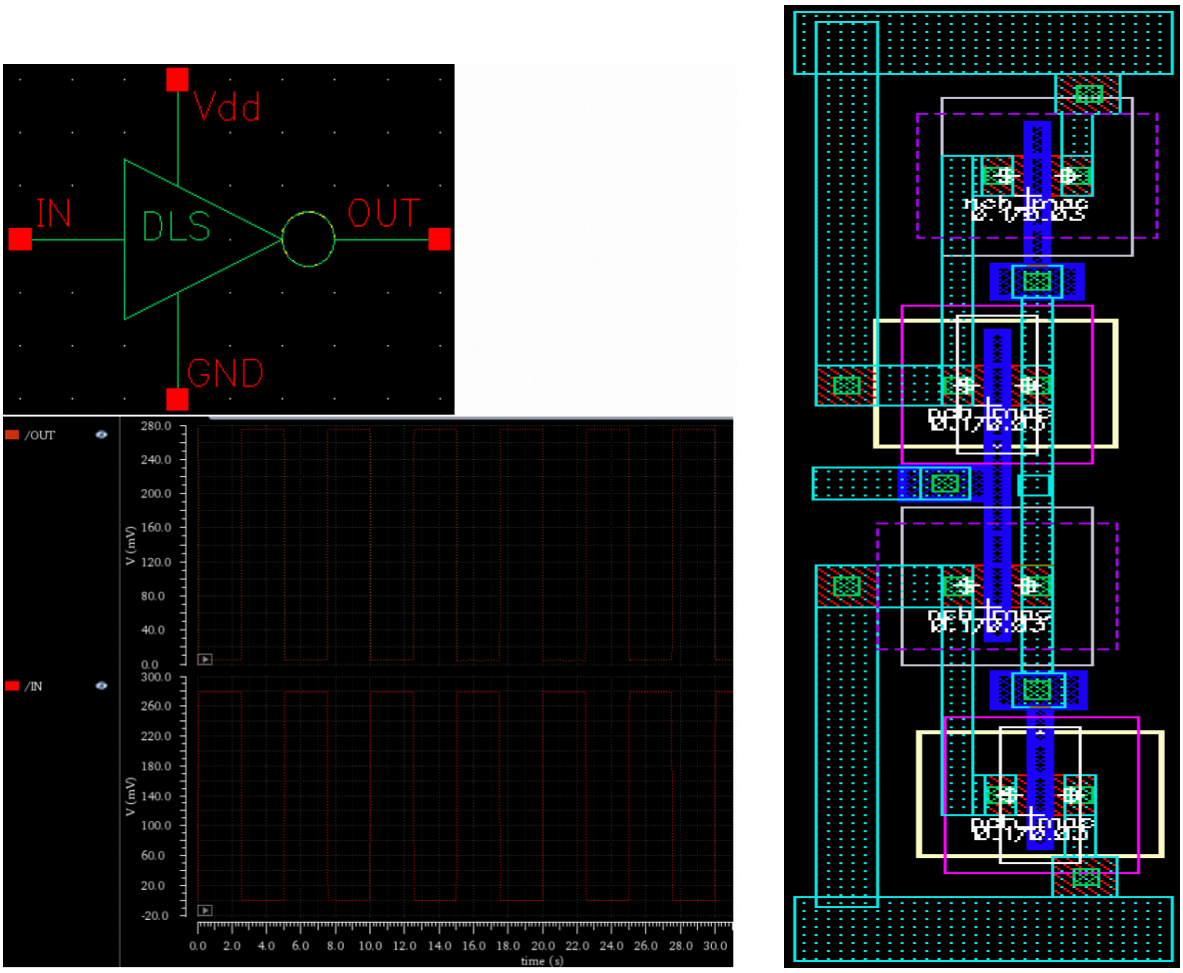


Figure 5.4 DLS Inverter implementation in 28nm with its transient response (left) and layout configuration (right)

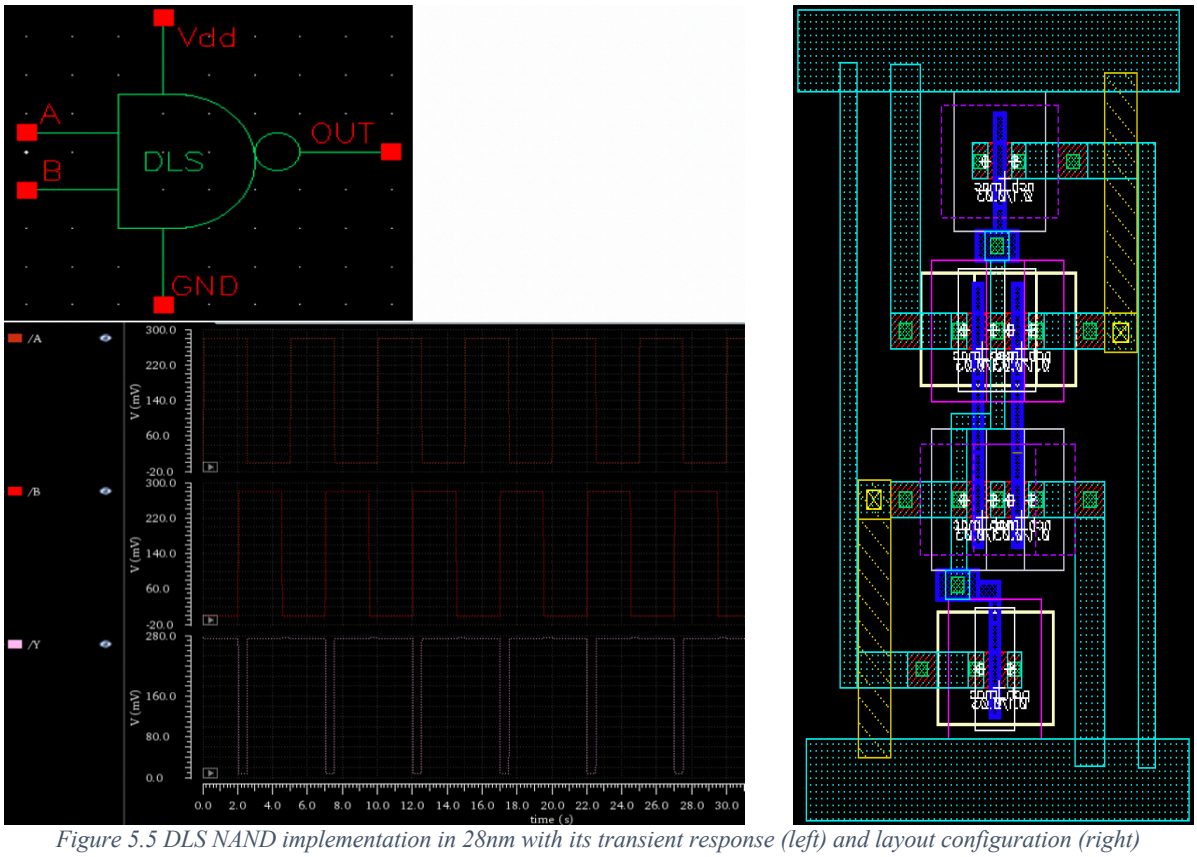


Figure 5.5 DLS NAND implementation in 28nm with its transient response (left) and layout configuration (right)

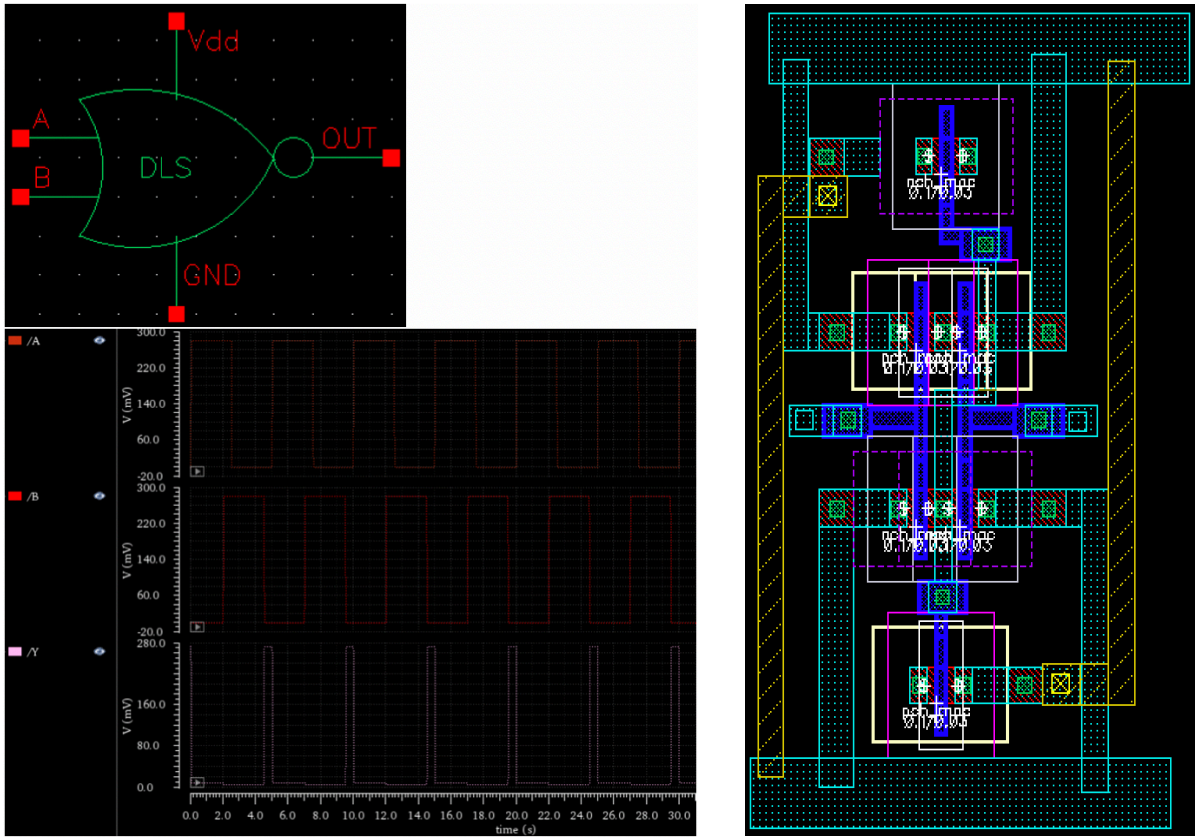


Figure 5.6 DLS NOR implementation in 28nm with its transient response (left) and layout configuration (right)

Also in this case, like it was for standard logic gates, the area of the ports implemented in 28nm is considerably less than using 180nm technology.

AREA COMPARISON BETWEEN 180 nm AND 28nm		
Logic Gate	Technology	Area (μm^2)
NOT DLS	180nm	33,915
	28nm	1,158
NAND DLS	180nm	43,487
	28nm	1,908
NOR DLS	180nm	43,487
	28nm	1,908
BUFFER DLS	180nm	61,133
	28nm	2,123

Table 5.2 DLS Logic Gate's area comparison: 180nm VS 28nm

5.2 NEW SIMULATION TESTS

Concluding this preliminary part, I recreate the schematic of all the oscillators using the software and minimum sizes for each transistor, exactly like during the first part of my work. I decided to do that to verify the differences, in the output frequency, between the two technologies, if are used for both minimum values of length and width. What I expect from these simulations is to obtain higher frequencies, because of the lower ratio $\frac{W}{L}$ and equal supply voltages and capacitance values imposed.

5.2.1 ONE HOT TIMER IN 28nm

The first configuration tested was the one hot timer developed, according to the paper, with all the transistors (Figure 5.7 below). Once again, unfortunately, there is no output oscillation and for this reason I tested it again replacing the three transistors on the left with two parallel resistances and a capacitor (Figure 5.7).

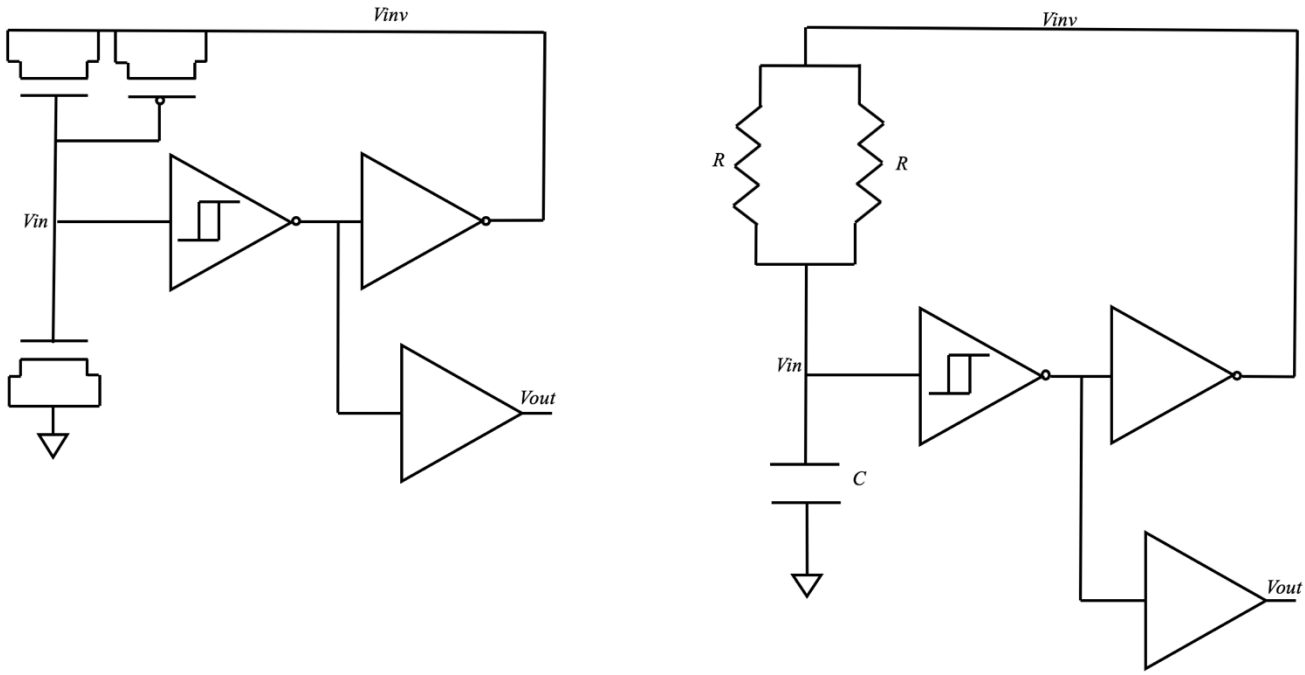


Figure 5.7 Schematic of one hot timer: configuration with all transistors (left) and configuration with resistances and capacitor connected (right)

Using R = 1kΩ, C = 1pF and Vdd = 450mV (which are the same parameters imposed during the simulations in 180nm technology) the transient response (Figure 5.8) shows a frequency f = 2,756MHz, a lot higher than in the previous case in which it was 440,95kHz.

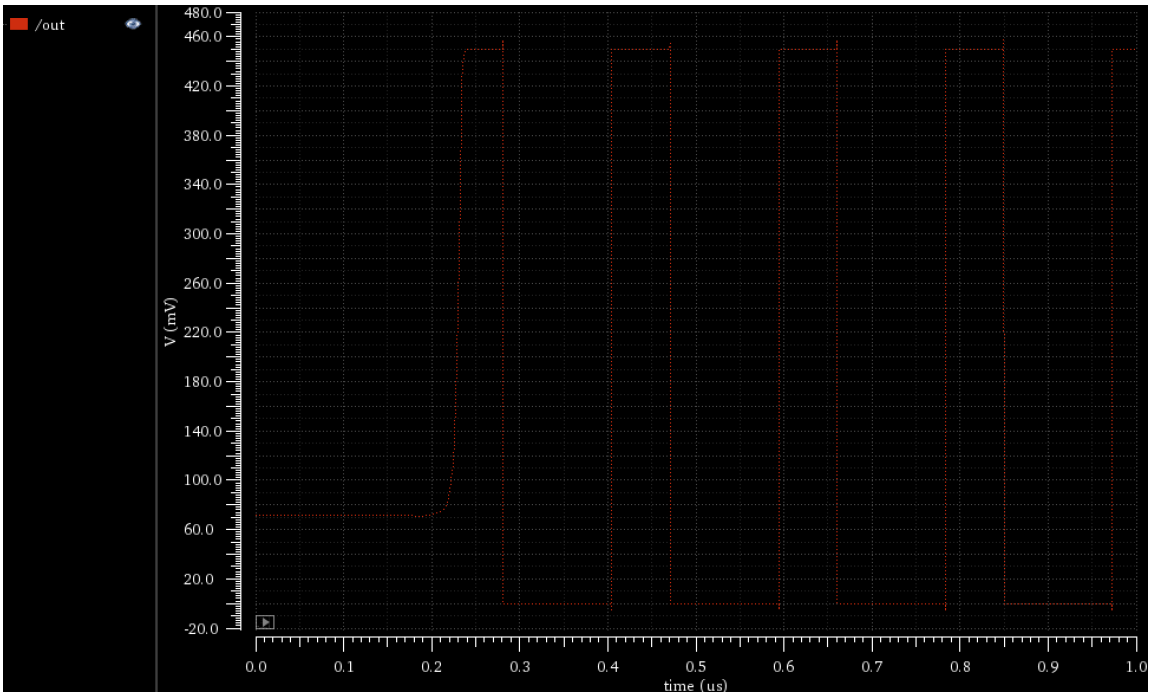


Figure 5.8 Transient response of one hot timer

Starting from this point on, I tried again to reduce the frequency testing what happen by changing length, width, resistances value and the capacitor value. The results of these changes are shown in the following figures.

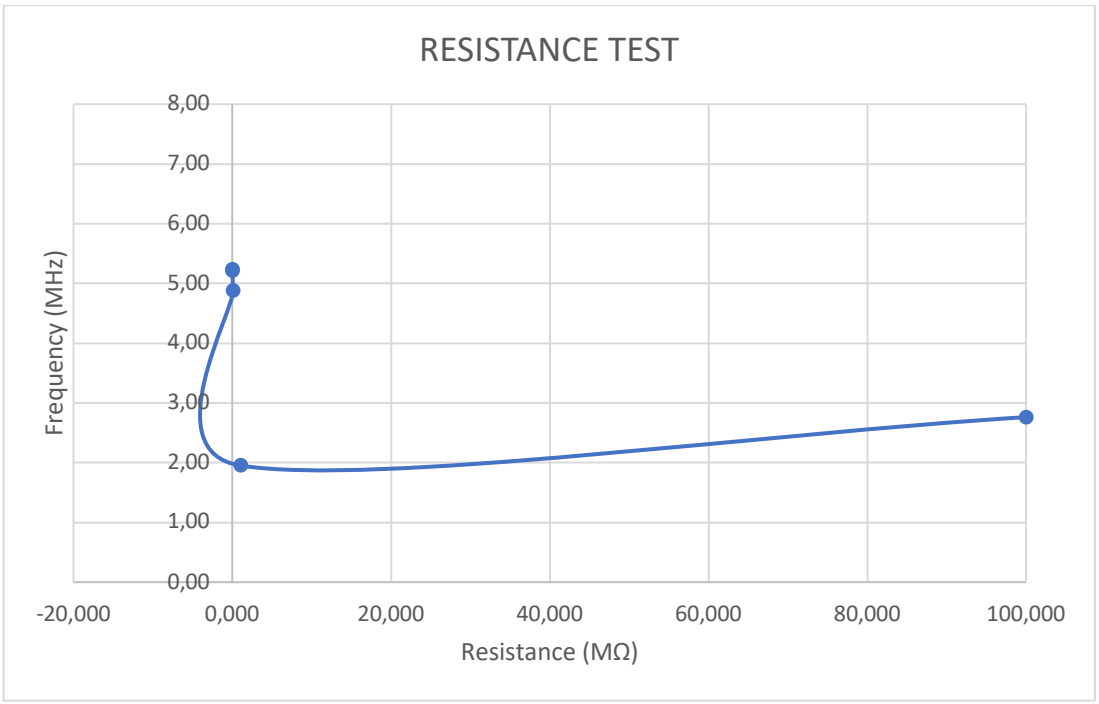


Figure 5.9 Frequency changes with resistances value imposing Vdd=450mV and C=1pF

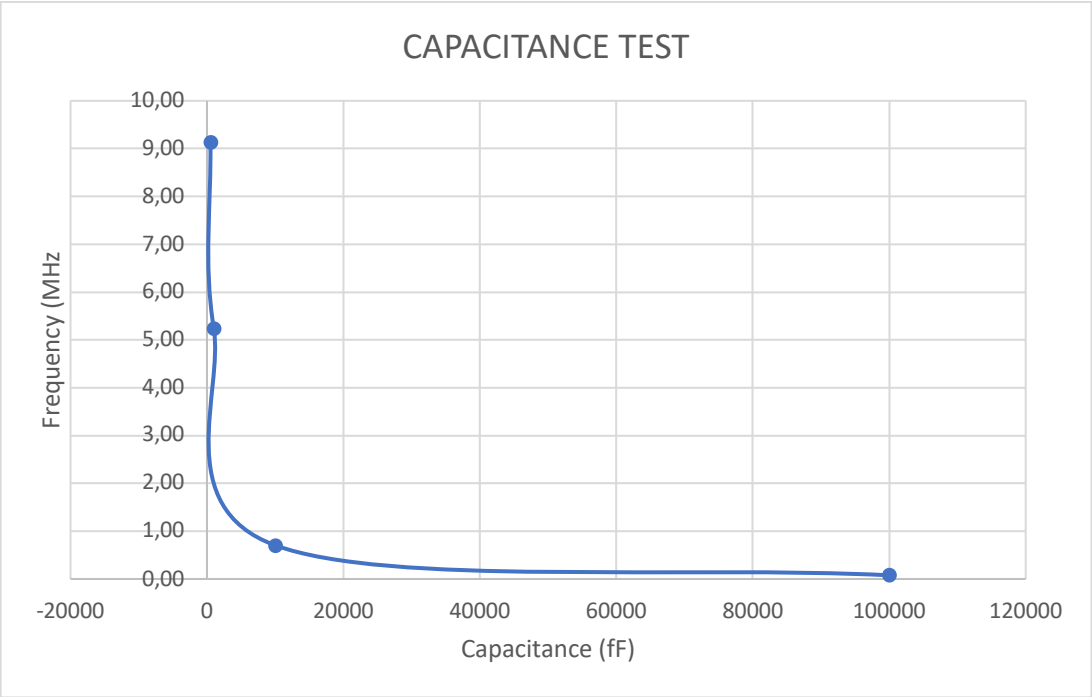


Figure 5.10 Frequency changes with capacitance value imposing Vdd=450mV and R=1kΩ

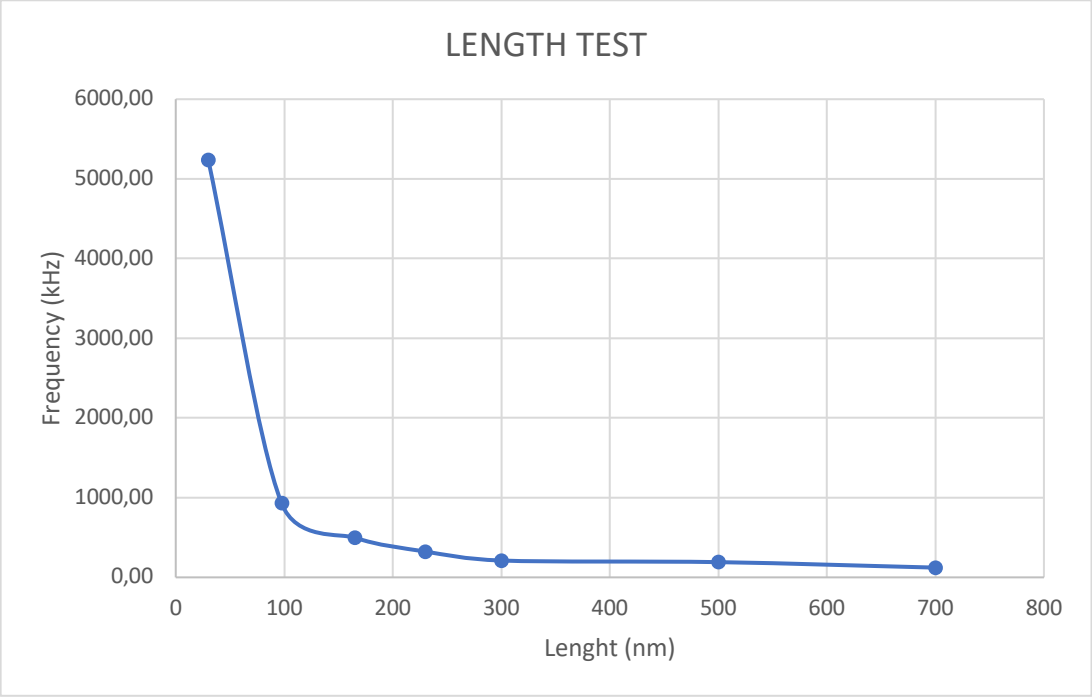


Figure 5.11 Frequency changes with length value imposing Vdd=450mV, C=1pF and R=1kΩ

Figure 5.12 Frequency changes with width value imposing Vdd=450mV, C=1pF and R=1kΩ

From the resistances and capacitance test's results it is evident that the frequency doesn't change in a relevant way, because the range is still of a few MHz. Instead, by changing the length value, from 30nm to 700nm, the frequency oscillation swaps from thousands of kHz to almost one hundred of kHz. In the end the width gives even worst outputs by increasing in value. Although the most significant result can be obtained through the comparison with the output frequency derived from the implementation in 180nm. Testing similar values of length, it's noticeable that in 180nm the situation is better: for example, considering a length L ≅ 500nm in 180nm the frequency is around 41 kHz while in 28nm is about 180 kHz. This means that even using a lower technology this oscillator is still not a good option. Least, from the layout configuration the total area occupied by the oscillator is 5,564 μm^2.

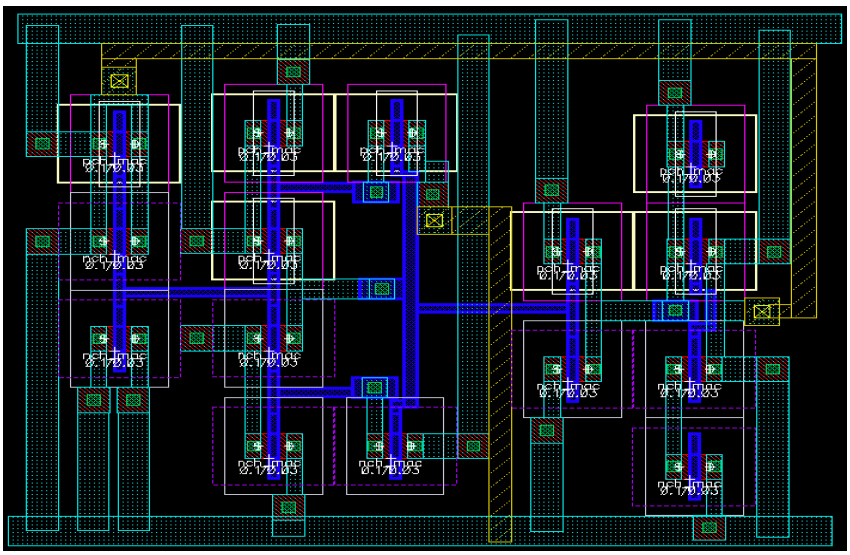


Figure 5.13 Layout configuration of one-hot timer in 28 nm technology

5.2.2 VOLTAGE CONTROL OSCILLATOR (VCO) IN 28nm

The second architecture tested was the Voltage Control Oscillator, which is the one that gave the best results in the simulations using 180nm technology. Once again, I started by testing its work imposing minimum length and width values. Because its output depends on the voltage, I analyzed the transient response in two cases: with supply voltage Vdd = 400mV and Vdd = 1V. The corresponding frequencies are f = 7,228 kHz and f = 127,572 kHz). The results are shown in Figure 5.13 and Figure 5.14.

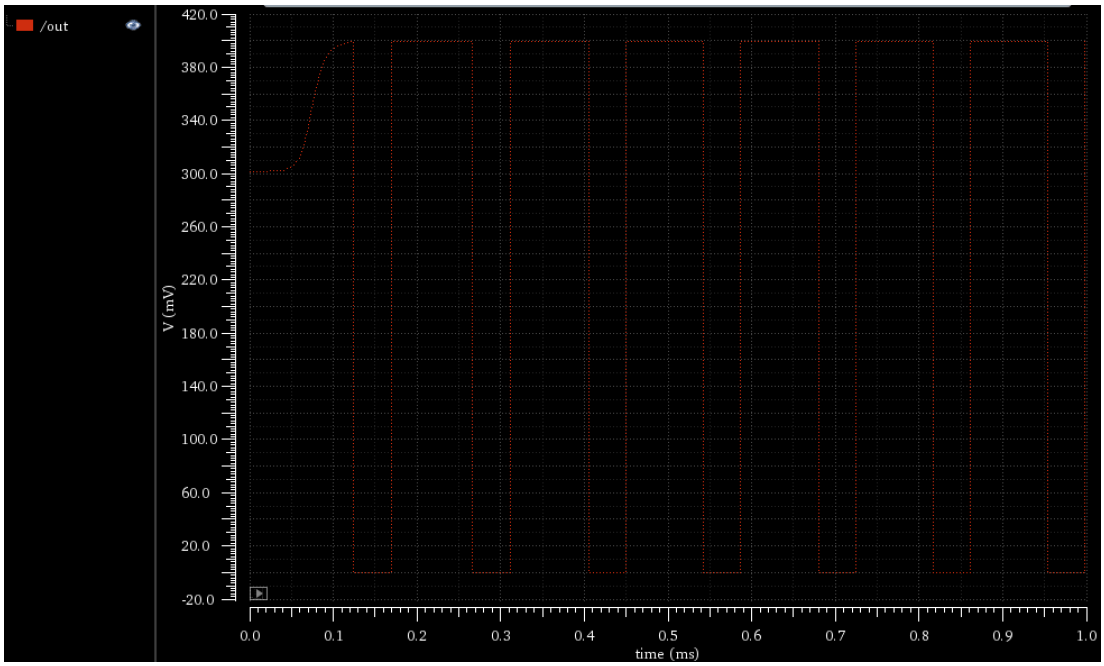


Figure 5.14 Transient response of VCO imposing a supply voltage Vdd = 400mV

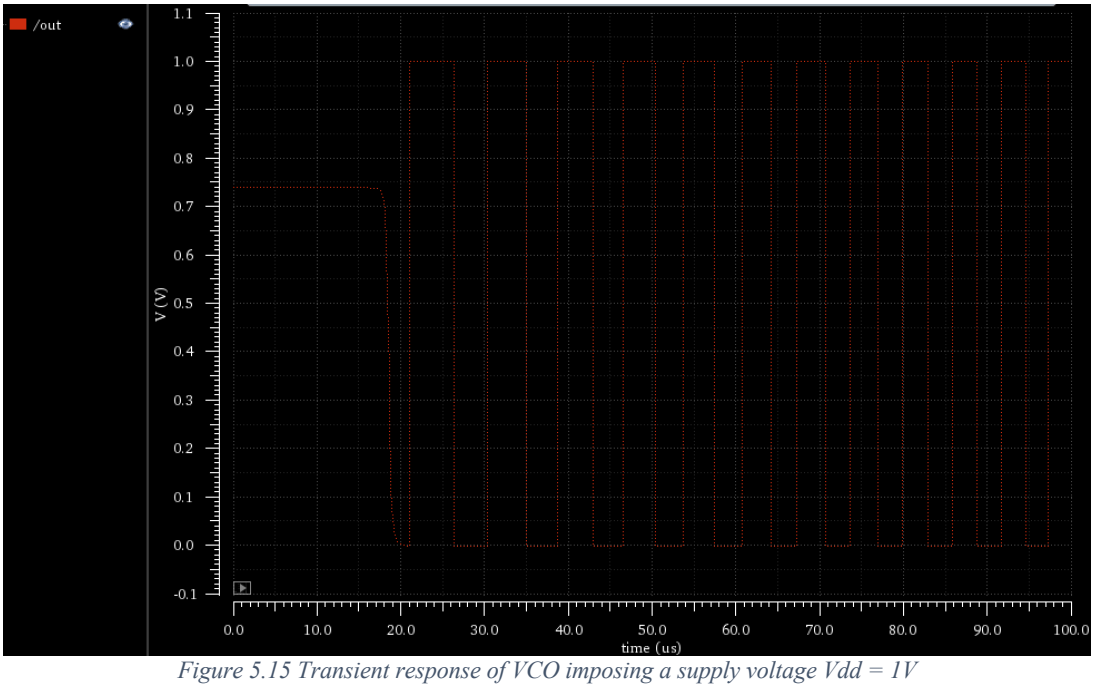


Figure 5.15 Transient response of VCO imposing a supply voltage Vdd = 1V

As expected, also in this case the starting frequency obtained with minimum sizes, are higher than in the oscillator developed in 180nm. In fact, in that case the initial frequency value was of 153,139 Hz with a supply voltage of 400mV and 168,265 Hz with 1,8V. For this reason, I made some other tests to check what happened by changing the length, the width and the capacitance value with three different supply voltages: 280mV, 400mV and 1V. The simulations results are shown in the following figures where, because of the big gap among the values derived from the three supply voltages, of 280mV and 400mV and the ones with 1V, I decided to split them in two different graphs.

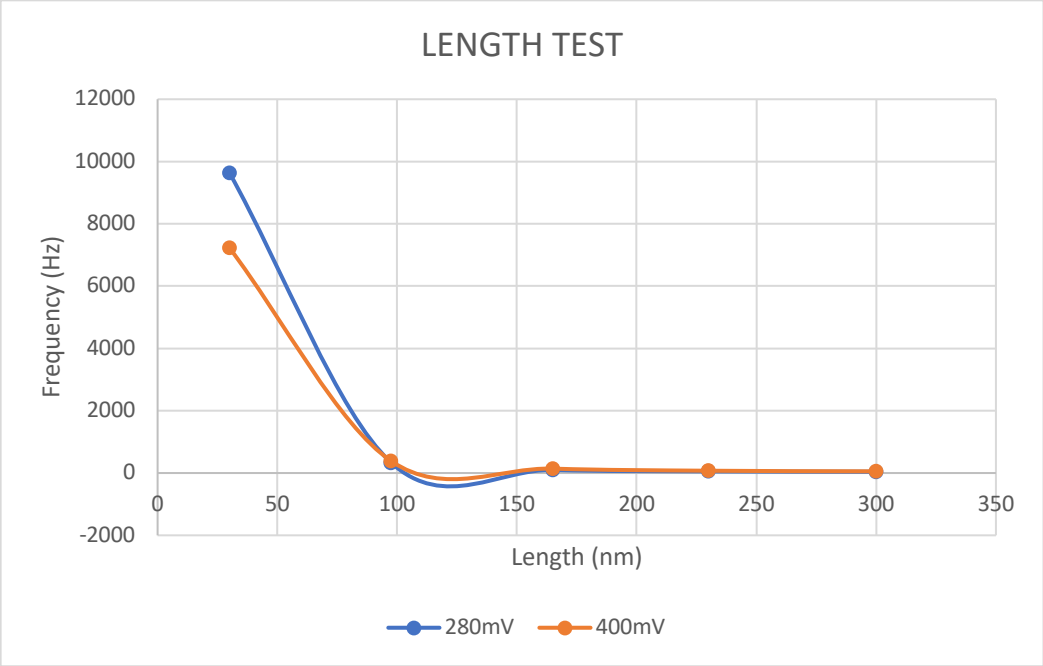


Figure 5.16 Frequency changes with length imposing two different supply voltages: 280mV and 400mV

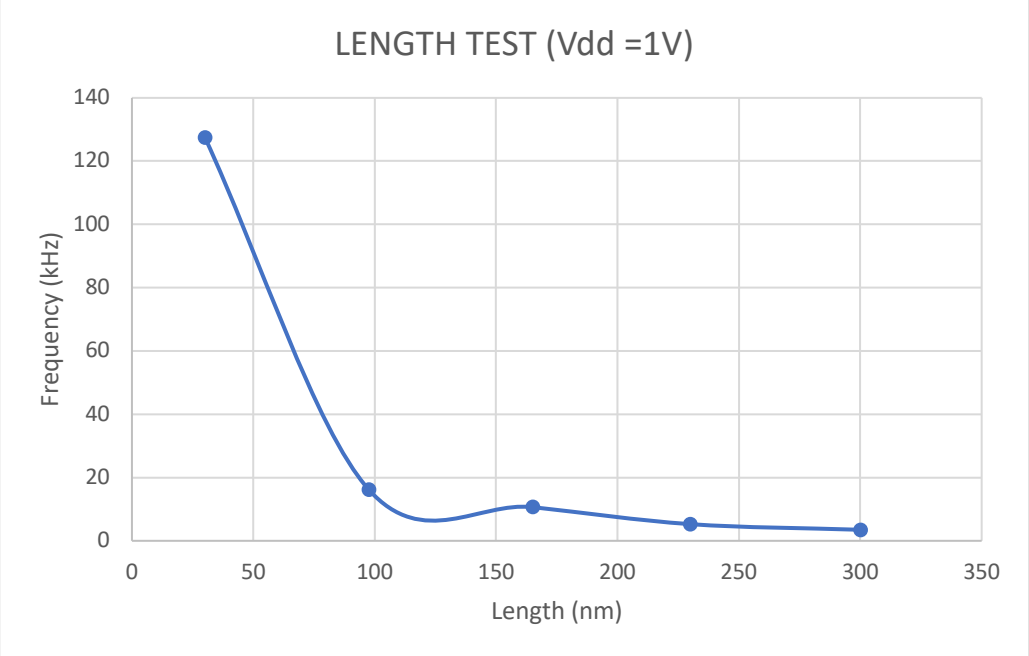


Figure 5.17 Frequency changes with length imposing supply voltage 1V

The length was increased from 30nm to 300nm for the three cases. The best results are obtained with the lower supply voltage (Vdd=280mV) reaching a few tens of Hz, while the worst with 1V, in which the range swing is still of kHz. These results are comparable with what was obtained in 180nm, testing the oscillator with a supply voltage of 400mV. Higher voltage values than 1V are not suitable for testing this oscillator in 28nm technology, so I considered the results derived from 280mV as the best for this case.

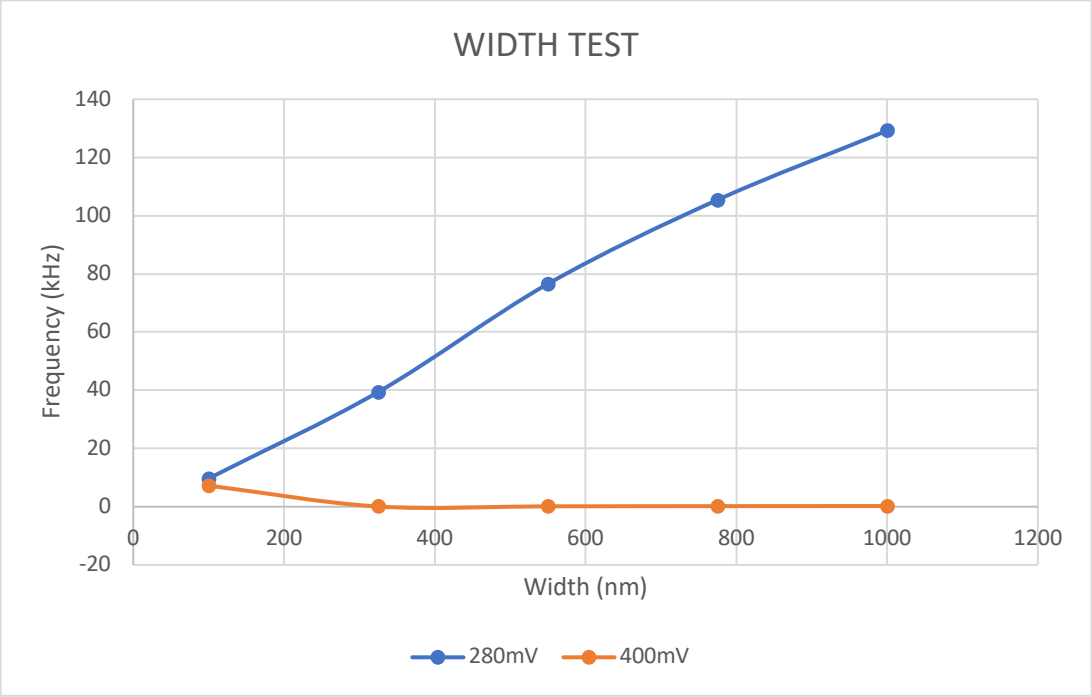


Figure 5.18 Frequency changes with width imposing two different supply voltages: 280mV and 400mV

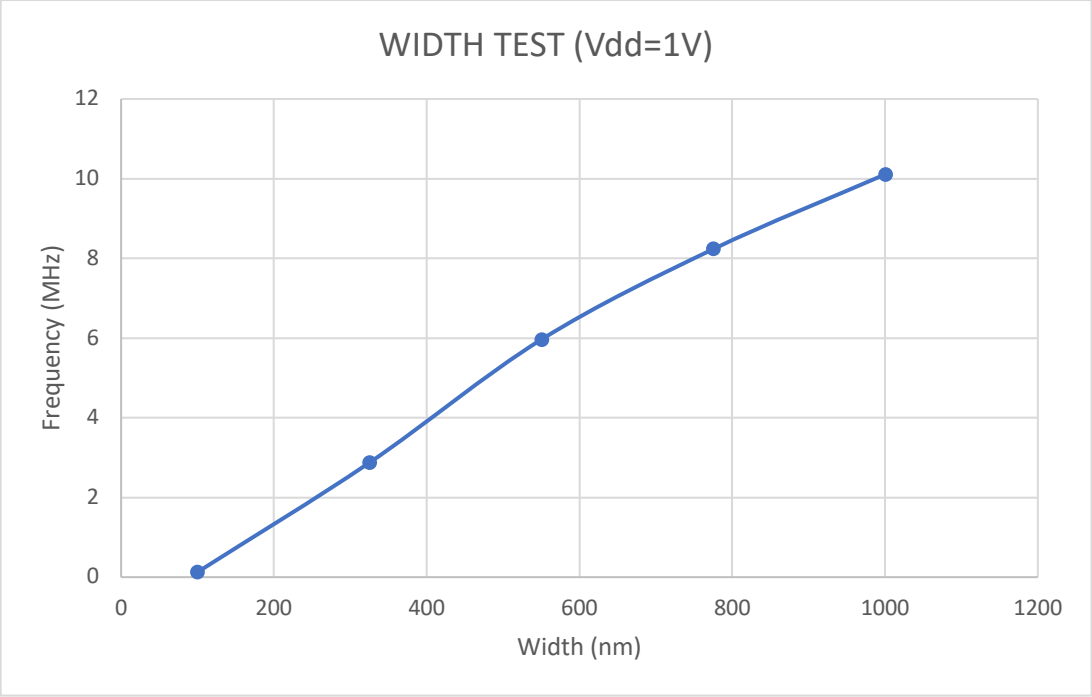


Figure 5.19 Frequency changes with width imposing supply voltage 1V

The width was changed from 100nm to 1000nm and for all cases the result was an increment of the frequency.
The last simulations were done changing the capacitance value.

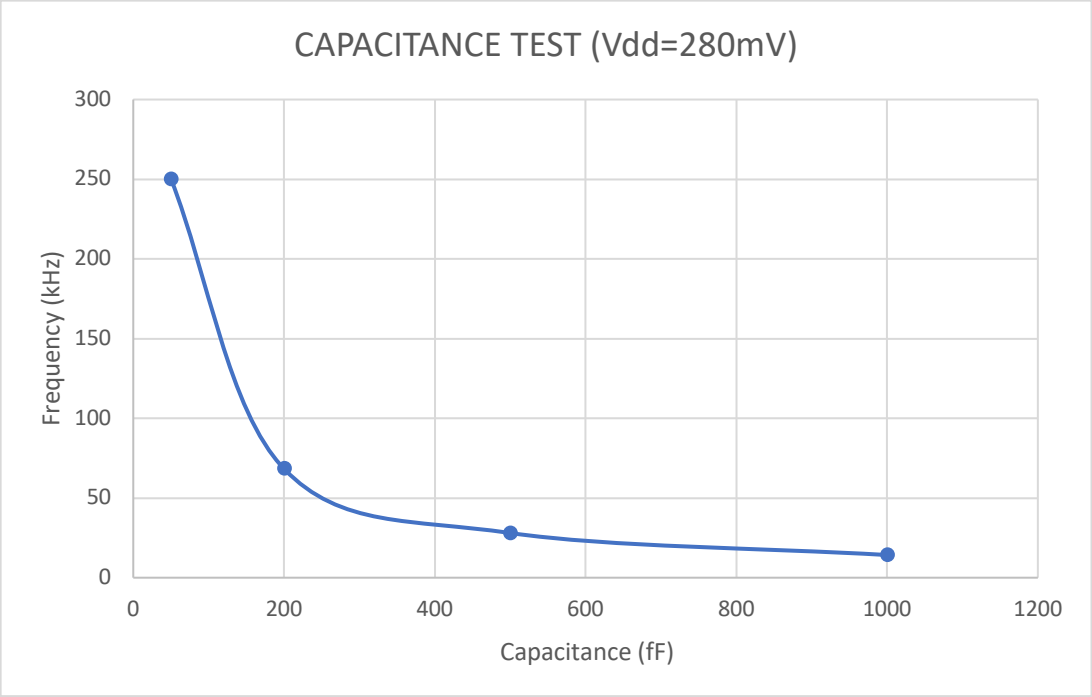


Figure 5.20 Frequency changes with capacitance value and supply voltage of 280mV

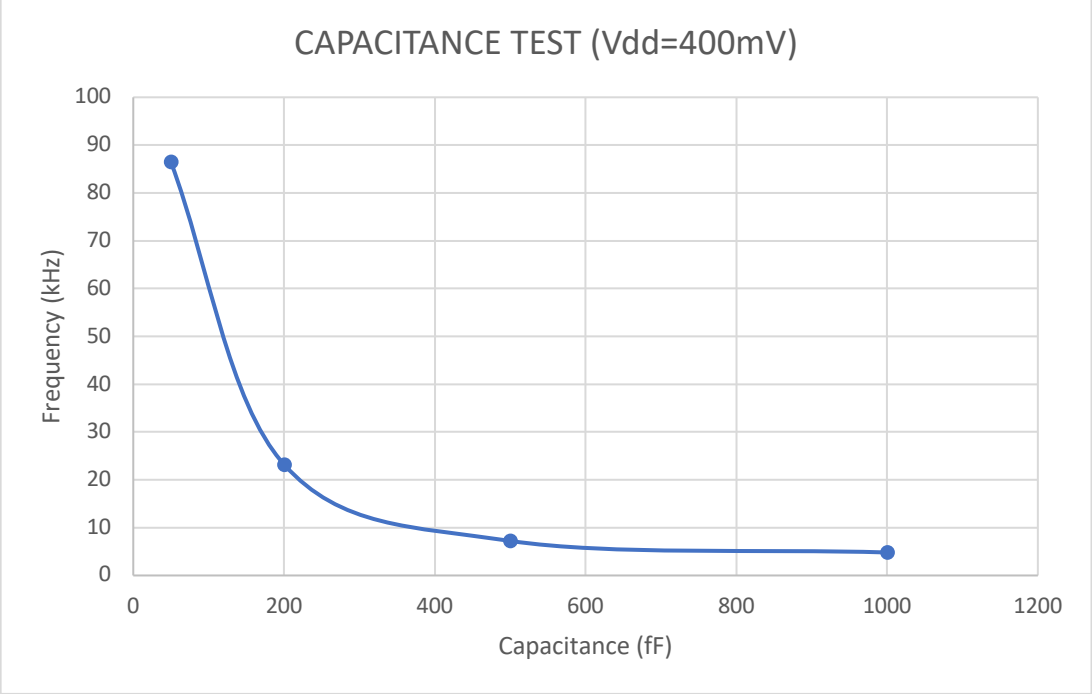


Figure 5.21 Frequency changes with capacitance value and supply voltage of 400mV

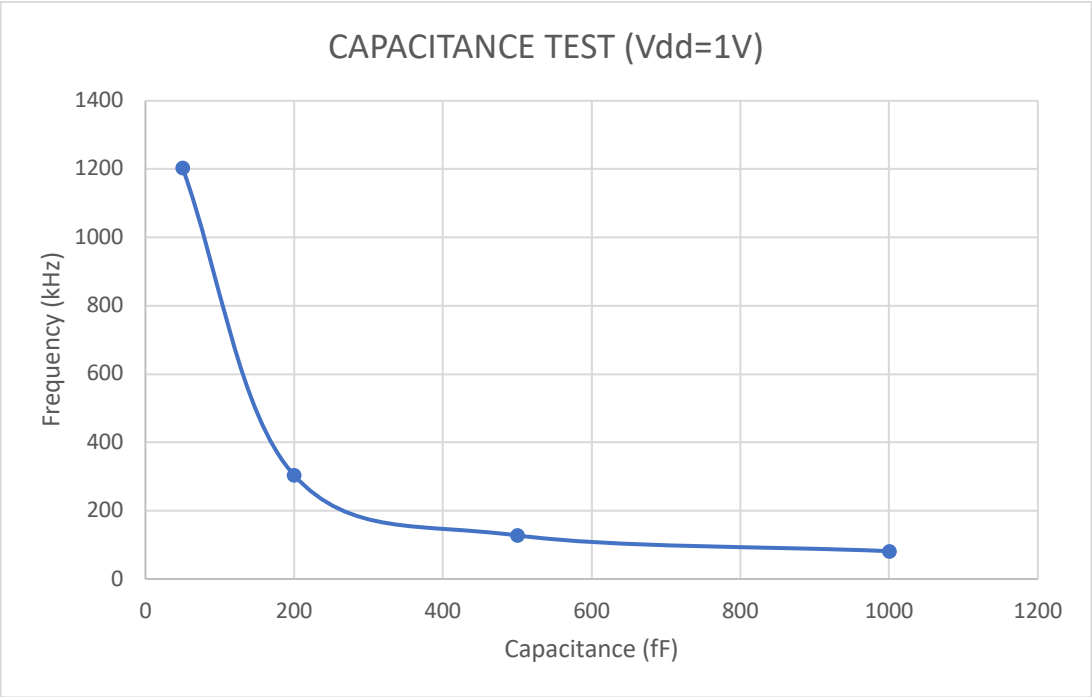


Figure 5.22 Frequency changes with capacitance value and supply voltage of 1V

Changing the capacitance value bring to good results in Hz range, with the best for 1pF and minimum values of both length and frequency.
An advantage of using a lower technology is also that is possible to work on these kinds of parameters: use very little capacitance values but bigger transistors sizes or the opposite reaching, like these simulations shown, acceptable frequency oscillations for our application.

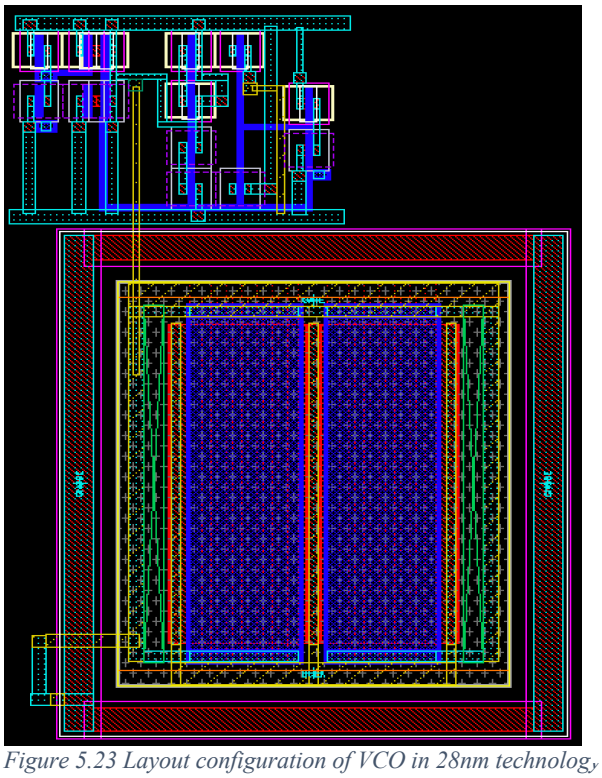


Figure 5.23 Layout configuration of VCO in 28nm technology

From the layout configuration of the VCO, I could measure the total area which is of 232,998 μm^2, considering a capacitance of 50fF. In fact, using this technology there are limited values for the capacitors, lower than the ones available in 180nm. By testing the oscillator imposing this capacitance value and a length of 700nm and a width of 100nm for all the transistors, the output frequency is 197,579Hz.
Even if both the area and the frequency results are over the limits imposed by the "Body Dust" application, they are considerably better than the values obtained in 180nm (819,582μm^2), considering the overall situation.

5.2.3 RELAXION OSCILLATOR IN 28nm

The last architectures left to implement are the relaxion oscillators, with and without DLS logic style. First of all, I tried to start with the DLS one, but this type of logic is very sensitive to parasitic capacitances and using a technology lower than 180nm makes it very difficult to work correctly. In fact, these components become more important in 28nm, compromising the oscillator functioning so that the output was just noise.
By implementing the same architecture without DLS is possible to observe an initial oscillation but, it extinguishes very fast.
So, these two oscillators couldn't be tested in 28nm technology.

5.2.4 FREQUENCY DIVIDER

The Voltage Control Oscillator implemented in 28nm gives good results in term of output frequency, even if these values are still far from the sub-Hz range necessary for the "Body Dust" application. However, a possible solution can be the support of a frequency divider because, even if in 180 nm the total area was too big for the 10X10μm^2 set up for the application, a lower technology implies smaller transistors sizes. From the layout of a TSCP flip flop (Figure 5.22) the overall area is 2,798 μm^2, which means that a 10 stages frequency divider will need only around 27,98 μm^2. With this value an output frequency in the sub-Hz range seems feasible.

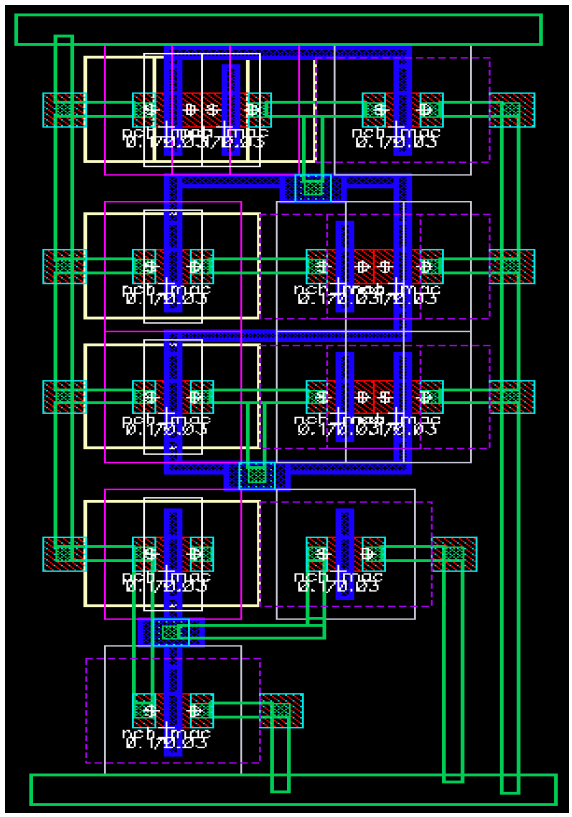


Figure 5.24 Layout configuration of a TSCP flip-flop implemented in 28nm technology

This means that even with a higher frequency, like the one obtained using a capacitor of 50fF, it could be possible to use a frequency divider with 12 stages (corresponding to an area of 33,576μm^2) to reach around 1mHz oscillation frequency.

5.3 TECHNOLOGY CHALLENGE: 180nm VS 28nm

With this, is also concluded the work I've done using a 28nm technology. The results are definitely promising, because it seems to be feasible to reach a sub-Hz frequency combining the work of a Voltage Control Oscillator with a frequency divider, limiting the capacitance value. From the comparison between the two technologies it also seems to be better to use a lower technology because, even if the frequency is higher in 28nm for same parameters value, the difference is not too big, and the average area is lower. In the next tables I summarized all the main results obtained from the simulations done in the two cases.

Technology	Oscillator	Parameters	Frequency
180nm	One-Hot Timer	Vdd=450mV R=1kohm C=1pF L=1800nm W=240nm	19,349kHz
28nm	One-Hot Timer	Vdd=450mV R=1kohm C=1pF L=700nm W=100nm	122,41kHz
180nm	Relaxion Oscillato (no DLS)	Vdd=400mV L=990nm W=240nm C=500fF	8,868kHz
180nm	Relaxion Oscillator with DLS	Vdd=400mV L=180nm W=240nm C=500fF	4Hz
180nm	VCO	Vdd=1,8V C=500fF L=585nm W=240nm	1,823Hz
28nm	VCO	Vdd=280mV C=500fF L=700nm W=100nm	22,955Hz

Table 5.3 Best results for each oscillator implemented with 180nm and 28 nm technology

Technology	Oscillator	Area (μm^2)
180nm	One-Hot Timer	107,392
	Relaxion Oscillator (no DLS)	1396
	Relaxion Oscillator with DLS	1600
	VCO	819,582
28nm	One-Hot Timer	5,564
	VCO	232,998

Table 5.4 Minimum Area occupied by each configuration tested in both 180nm and 28nm technology

From the previous tables is clear that the best oscillator is the VCO, in both term of frequency and area occupied. In particular, the architecture in 180nm gives better results for the output, with a minimum value of 1,823Hz, while in 28 nm there is a frequency of 22,955Hz but, the area in this second case is almost reduced of four times, respect to the other case. Considering the complete design proposed at the beginning for the multiplexer it is evident, from the cake graphs below, that the element which cost most in term of area is always the oscillator.

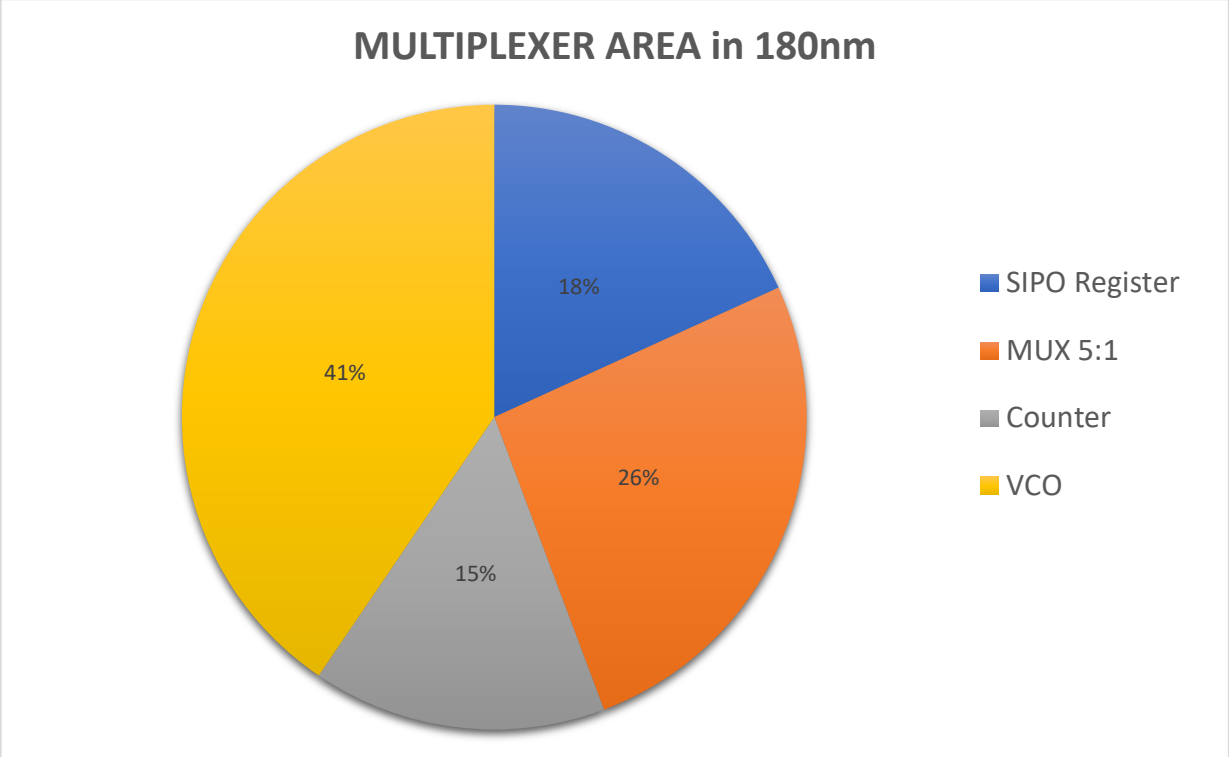


Figure 5.25 Percentage of area occupied by the multiplexer's elements in 180nm

From the layout design of the multiplexer in 180nm the total area required from the circuit is 2021 μm^2.

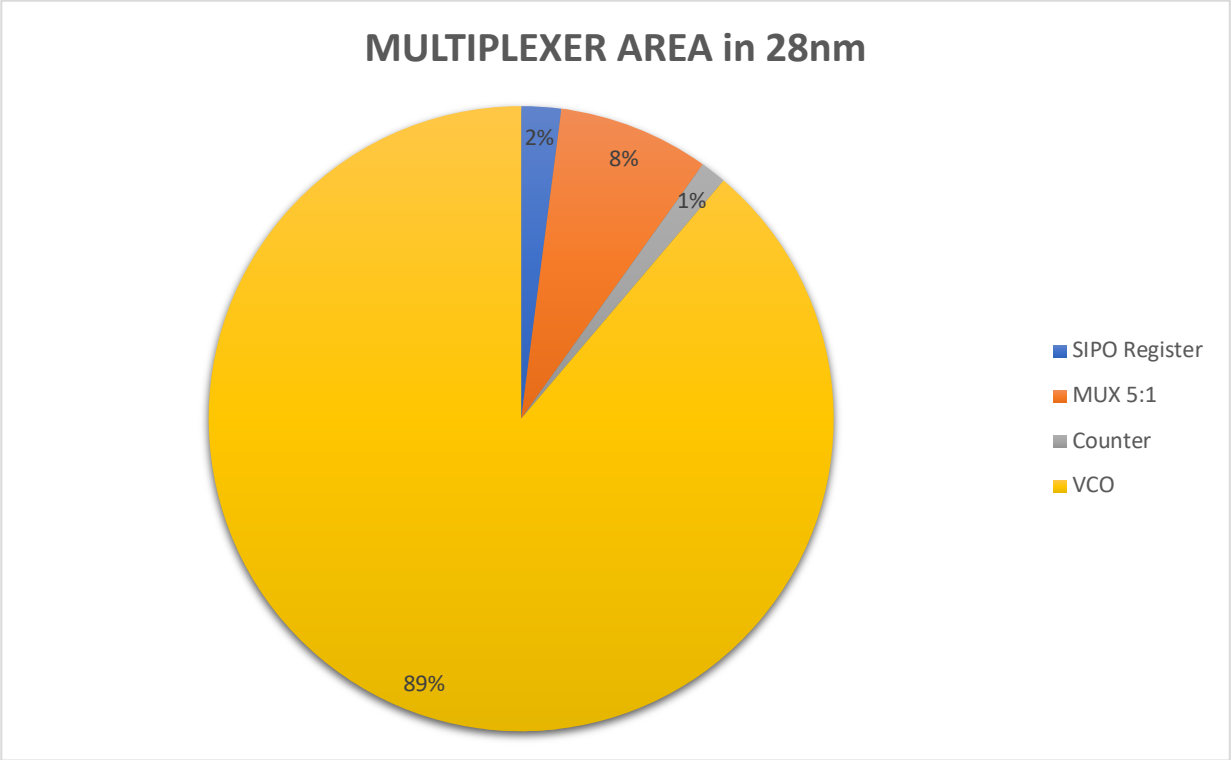


Figure 5.26 Percentage of area occupied by the multiplexer's elements in 28 nm

For the layout configuration of the multiplexer developed in 28 nm the VCO is certainly the biggest element in the circuit, occupying the 89% of the total area, which is 266 μm^2. The difference with the value measured for the same implementation with a higher technology is evident: almost eight time less than the area necessary in 180nm. However, the area still remains over the limit imposed for the “Body Dust”.

CHAPTER 6

CONCLUSIONS

During my work I could introduce a new concept in the CMOS biosensing technology environment. I could propose a possible design for a multiplexer system, which can scan the acquisition of five different signals, associated with a corresponding channel. Moreover, I could study the feasibility to implement a circuit, testing the properties of four oscillator's architectures, judging their limits in term of frequency and area. Moreover, I had to take into consideration that the system wants to measure the concentration of both, endogenous and exogenous molecules, making the design definitely more complicated, than it would be with the analysis of only one component.
At the beginning, my work focused on a 180nm technology, with simulations that show the unfeasibility to find a good compromise between the boundaries imposed by the "Body Dust" application. In fact, the goal was to obtain a switch period for the multiplexer, from one channel to another, of a few minutes, using a circuit hold in a square area of 10X10 μm^2. Through my work I could demonstrate that, using 180nm technology, a multiplexer circuit can generate 1,823 Hz frequency, through a Voltage Control Oscillator, with a total layer's area of $2021\mu m^2$. This result is, of course, far from the aim of the project.
Even if in the scientific field, a failure is still an important result, I wanted to find a path to follow, in order to have a new starting point for this research. This is the reason why I tested a possible solution for the limits imposed by the 180nm technology, developing all the circuit using a lower one: 28nm. This new technology seems to be a good way to proceed, thanks to the results obtained by the simulations. In fact, I could demonstrate the feasibility to develop, with the help of an asynchronous counter, a sub-Hz frequency oscillation, designing a circuit with total area of $266\mu m^2$. This work needs to be deepened, in order to optimize all the components but, the premises are very promising.
So, the results derived from this thesis didn't bring to a final solution for the realization of a multiplexer circuit, compatible with the Body Dust application but, they were still fundamental to understand the limits of the current technology used. Thanks to that, it is possible to address new progressions in other directions, like lower technologies, or digital circuits, or even a completely revolution of the system like it was conceive till now.

The Body Dust is certainly a great challenge, and it can represent a major transformation in the biomedical, IC and pharma industry. Even if the obstacles are still a lot, the research is very promising, and in a not so far future it can be possible to reach a real functioning of the system.

List of Figures

Chapter 2

Chapter 3

Chapter 4

Chapter 5

List of Tables

List of Equation

(2.1) $f = \frac{1}{N*C_{TOT}*V_{DD}}$

(2.2) $i = \frac{n*F*A*c_j^0*\sqrt{D_j}}{\sqrt{\pi*t}}$

(2.3) $i = k * t - \frac{1}{2}$

(2.4) $E = \frac{R*T}{z*F} * ln\frac{[ion\ outside\ cell]}{[ion\ inside\ cell]}$

(3.1) $f = \frac{2*I_{ON}}{C_t*(V_{b1}-V_{b2})}$

(3.2) $J_g = A * T_{oxratio} * \frac{V_g*V_{aux}}{t_{ox}^2} * e^{[-B*(\alpha-\beta*V_{ox})(1+\gamma*V_{ox})*t_{ox}}$

(3.3) $\frac{dV_b}{dt} = -\frac{I_{DLS}}{C}$

(3.4) $Vc = V_{AB,H} - V_{DLS,L}$

(3.5) $Va = 2 * V_{AB,H} - V_{DLS,L}$

BIBLIOGRAPHY

Chapter 2

[2.1] Y.-T. Liao, H. Yao, A. Lingley, B. Parviz, and B. P. Otis, "A 3-uw cmos glucose sensor for wireless contact-lens tear glucose monitoring," IEEE Journal of Solid-State Circuits, vol. 47, no. 1, pp. 335–344, 2012

[2.2] J. Rothe, O. Frey, A. Stettler, Y. Chen, and A. Hierlemann, "Fully integrated cmos microsystem for electrochemical measurements on 32→ 32 working electrodes at 90 frames per second," Analytical chemistry, vol. 86, no. 13, pp. 6425–6432, 2014

[2.3] S. W. Lee, F. Fallegger, B. D. Casse, and S. I. Fried, "Implantable microcoils for intracortical magnetic stimulation," Science Advances, vol. 2, no. 12, p. e1600889, 2016

[2.4] Baj-Rossi, C., Cavallini, A., Kilinc, E. G., Stradolini, F., Jost, T. R., Proietti, M., ... & Carrara, S. (2016). In-vivo validation of fully implantable multi-panel devices for remote monitoring of metabolism. IEEE transactions on biomedical circuits and systems, 10(5), 955-962

[2.5] Sandro Carrara and Pantelis Georgiou, "Body Dust: Miniaturized Highly-integrated Low Power Sensing for Remotely Powered Drinkable CMOS Bioelectronics, IEEE Conference BioCAS, 2017

[2.6] Snoeijs, J., Georgiou, P., & Carrara, S. (2017, October). CMOS body dust Towards drinkable diagnostics. In 2017 IEEE Biomedical Circuits and Systems Conference (BioCAS) (pp. 1-4). IEEE

[2.7] Gian Luca Barbruni, Paolo Motto Ros, Simone Aiassa, Danilo Demarchi, Sandro Carrara, "Body Dust: Ultra-Low Power OOK Modulation Circuit for Wireless Data Transmission in Drinkable sub-100um-sized Biochips"

Chapter 3

[3.1] Yu-Shiang Lin, Dennis Sylvester and David Blaauw, "A sub-pW timer using gate leakage for ul- tra low-power sub-Hz monitoring systems"

[3.2] ROB WOUDSMA ANDJOS M. NOTEBOOM, "The Modular Design of Clock-Generator Circuits in a CMOS Building-Block System"

[3.3] Orazio Aiello, Paolo Crovetti, Massimo Alioto, "Wake-Up Oscillators with pW Power Consumption in Dynamic Leakage Suppression Logic"

[3.4] Orazio Aiello, Member, IEEE, Paolo Crovetti, Member, IEEE, Longyang Lin, Student Member, IEEE, and Massimo Alioto, Fellow, IEEE, "A pW-Power Hz-Range Oscillator Operating With a 0.3-1.8-V Unregulated Supply"

[3.5] Faiz Arith, M.Idzdihar.Idris, M.N.Shah Zainudin, S. A. M. Chachuli, "Low voltage CMOS Schmitt Trigger in 0.18μm technology"

[3.6] Pranay Kumar Rahi, Shashi Dewangan, Tanuj Yadav, Md Muzaherul Haque, "Design and Simulation of CMOS Schmitt Trigger"

[3.7] Wootaek Lim, "Ultra-Low Power Circuit Design for Miniaturized IoT Platform"

[3.8] Francesco Barale, "frequency dividers design for multi-ghz pll systems"

[3.9] M. Jurgo, K. Kiela, R. Navickas, Departament of Computer Engineering, Vilnius Gediminas Technical University, "Design of Low Noise 10 GHz divide–by–16...511 Frequency Divider"

[3.10] Ms. Chaitali V. Matey, Ms. Shraddha K. Mendhe, Mr. Sandip A. Zade, Electronics and Comm. Dept, Suresh Deshmukh College of Engg. Wardha (MS), "a novel design of counter using tspc d flip-flop for high performance and low power vlsi design applications using 45nm cmos technology"