

POLITECNICO DI TORINO

Master of Science in Electronic engineering

Master Degree Thesis

A test system for PCBs



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*«Non è la conoscenza, ma l'atto dell'apprendimento,
e non il possesso, ma l'atto di arrivare fino alla meta,
che ci garantisce il maggior godimento.»
Carl Friedrich Gauss.*

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Acronyms

PCBA	Printed Circuit Board Assembly
BON	Bed Of Nails tester
UUT	Unit Under Test
TPGM	Test Program
TH	Through Hole
SMD	Surface Mounted Device
OBP	On Board Programming
ATE	Automatic Test Equipment
QC	Quality Control
PCB	Printed Circuit Board
DFT	Design For Testability
DUT	Device Under Test
ATPG	Automatic Test Program Generator
UUT	Unit Under Test
ICT	In-Circuit Test
FCT	Functional Test

Introduction

Testability is a fundamental concept to be introduced already in the first phase of a project development, trying to identify a series of guidelines for the layout of a Printed Circuit Board (PCB). Testing of an electronic board is one of the fundamental points to guarantee quality certification, defined as the procedure to verify the correspondence between the specifications and the actual operation of the product. Modern technology over the years, following what was predicted by the law stated by Gordon Moore, which had been valid since 1965, had predicted the number of transistor/IC will double every 1.5 years. The success of electronic technologies due to the increasing level of integration is reaching a saturation since it is becoming harder to fatherly scale devices. This low, still valid nowadays, cannot be applied in the future because the technology's ideas on which it is based are those of the past. Migration towards more advanced technological nodes, hence the integration of active and passive components and increasingly miniaturized geometric processes have led to the development of increasingly more technologically advanced electronic systems capable of facing the challenges of testing.

Modern electronic devices becoming smaller and more compositive while their function and structure more complex, outline an evolution that has a negative impact on the entire supply chain of the electronic sector and represents a challenge that all suppliers must face. It is up to the designer to optimally exploit these new rules and aspects, which can be treated already in the early phases of the design and implementation of PCB boards. It is enough to focus the attention, for example, on the evolution of the Surface Mount Technology (SMT) which involves the application of electronic components directly on the circuit surface, without the need of holes.

The advantages deriving from this technology have made it possible to reduce not only the dimensions of the components used, but with the same area having a greater integration density. The possibility of high integration, as explained previously, has made it necessary to follow particular criteria known under the name of *design for testability* applied in the design phase, so as to have savings immediately visible during the testing phase which will be analyzed in the following chapters. The design for testability allows not only to reduce the time needed to move from project to production, but also to reduce the number of designers involved during the start up of production with a better redistribution of resources,

thus reducing the initial costs of a productive cycle guaranteeing better diagnostics at the component level, with a consequent reduction in the average debug time. The *design for testability* establishes the degree of precision with which a board will be tested. Know the degree of accessibility of the components, how fast the generation of a test program can be and how simply the correspondence between the specifications and the real operation can be verified, grant to define the testability of an electronic board, i.e. the possibility of testing circuits/systems that are not otherwise testable.

My thesis work, carried out in SPEA, leading company in the field of electronic device testing, aimed to analyze the testing of an electronic board to be integrated in a domotic environment. In particular, in a first phase of my project, I had the opportunity to interface directly with the customer to analyze the testing critical points, and then provide a feasibility analysis concerning the in-circuit and functional test of the device. Even more important it is what dictated the choice of the automatic system to be used. In particular, to carry out the testing of the UUT, a Bed of Nails system is used, a traditional electronic tester which uses a mechanical interface between the system and the board to be tested. It is designed to adapt in a flexible way to the most different test needs, thanks to the range of models available and its modular and scalable architecture. A suitable test program has been generated, using a software tool, developed by SPEA, called Leonardo, to perform the test of the board. Circuit analysis enabled to identify circuit nodal impedance, highlighting low impedance connections, available contact points and all the configurations and components of the board with the aim to reduce the debug operations as much as possible. In this phase the In-Circuit Test and the On Board Programming are exploited. The In-Circuit Test (ICT) represents an important part of a production process in which passive and discrete components mounted on the PCB are tested without supplying the necessary power for the complete functioning of the board. Concurrently, due to the presence of flash memory based micro controllers, the On Board Programming can be performed through the use of a proprietary interface (a bidirectional one-wire serial bus system able to update only a set of data where results of ICT are memorized) or through a direct connection with system resources. Finally, the complete functionality of the power module is tested during the final inspection. The Board Functional Test (FCT) measures and verifies the electrical characteristics of the board, according to what is specified by the customer and ensures the test of components which could not be tested by the ICT. In particular, I focused on the functional test of a voltage-dependent resistor, varistor, present in the power supply module, a critical component within the circuit under examination. The test was carried out designing the schematic of a conditioning circuit and in a second phase the development of a PCB, of a DC/DC converter capable of delivering 1000V and a maximum power of 6mW. The tests were developed using the *C#* language, which allowed me to access the machine settings to start the tests and analyze the nonlinear, non-ohmic

current–voltage characteristic.

Document structure

The objectives achieved during my stay in SPEA are listed gradually in the different chapters, but to give a greater understanding of the work carried out I report a brief structure of the document.

The first chapter introduces the concept of design for testability, a set of rules that must be adopted to ensure the testability of a device before the development of an application. A general description of the electronic appliance used during the test will be provided along with the specifications and requests of the customer in order to proceed with the testing of the device.

In the second chapter follows a brief explanation of the system used for the testing of the electronic board automatically, i.e. Automatic Test Equipment (ATE). In particular it will be explained how the SPEA 3030 system is used, also analyzing the mechanical adapters made for the board to be tested, including fixture and presser plate, essential parts in a bed of nail tester. The Leonardo software is also introduced to perform the different tests of the board explained in the central part of the thesis.

Introduction of the notion of the in-circuit test and reasons for using automatic test equipment, are provided in the third chapter. In the first part are analyzed the various test models adopted in the debug of single standard components and then, the solution embraced to test an IC smart power module FSB50550AB will be shown starting from the assumption that the client had not provided any provision on the test to be performed.

After completion of the in-circuit test, the programming steps for the on board programming are implemented on the STM32F301 mixed-signal microcontrollers and shown in Chapter 4.

In the last part, the functionality of a varistor and the discharge of a capacitor related to the power module test are outlined. To carry out these steps, the realization phases of an high voltage DC/DC converter and how it is used will be explained.

Finally, an analysis of the stability is carried out on the tests performed.

Chapter 1

PCBA Design for Testability

The manufacturing process of the board to be tested will affect the choice of the design strategy of the board itself. For this reason, it is essential to take the manufacturing process into account when adopting the Design for Testability rules.

The *Design for Testing* or *Design for Testability* consists of a series of rules for the design of electronic boards in order to:

- *Ensure the testability of each mounted component (In-Circuit Test);*
- *Simplify the testability of the functions (Functional Test);*
- *Allow for programming the programmable components (On-Board Programming);*
- *Make the automatic test generation possible;*
- *Make the In-Line transport of the board possible.*

The goal of the *production testing* of an electronic board is to ensure that there are no defects, which may cause malfunction of the circuits or early on field failure of the mounted components. In addition, the purpose of Manufacturing Test is the production process control. This prevents the production line to start producing defects as the time goes by. Each net of the circuit needs available test points in order to allow the complete testing of each component and the automatic generation of the test program (ATPG). This is to ensure the maximum failures coverage and the minimum cost of testing.

1.1 Test and specification

A guide for the Test Engineers is the one displayed in figure 1.1. Here a simple diagram shows how an application is generally developed. Some of those are also the focal points of the following chapters.

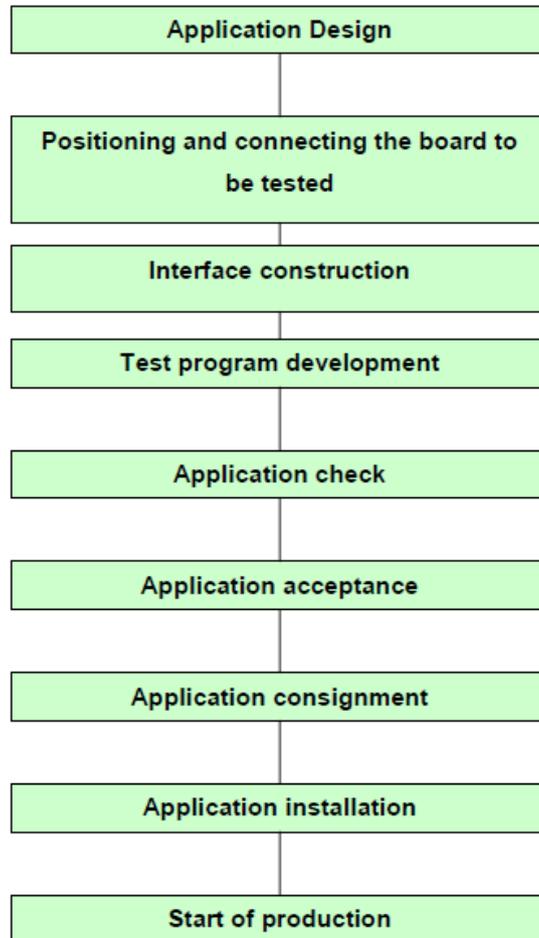


Figure 1.1: Application development chain

Before starting the development of the application, it is necessary to be clear about the objectives of the test, and to have all the essential input data at your disposal.

It is important to receive all the information on the product to be tested, in order to develop an application, and in particular:

- **Type of board**

The type of test depends very much on the board to be tested. For example, the test of a board which will be installed in a satellite, must be checked 100%, so as to avoid any type of problem (no components may be left uncovered).

- **Type of test to apply**

Based mainly on the type of board and on the type of system, the customer may request different types of tests on its board (also concatenated).

- **Number of boards to be tested**

It is important to know approximately how many boards will be produced. For example, if there are a large number of boards to be tested, a brief testing time will be required.

- **Start of production**

It is essential to know when the customer will start production of the boards, and consequently when the application can work on its testing systems.

- **Mechanical constraints**

It is also sometimes necessary to ascertain at the customer's site that there are no mechanical constraints for the UUT testing or for the interface construction. This is very important so as to avoid any damage to the production boards during their testing.

All information regarding the boards and the test, received from the customer, can be included in a specific test document. This document is necessary for the writing and designing of an in-circuit, and functional test. It includes all the various steps necessary to complete the test, such as the steps to follow to avoid damages to the UUT, the range of values to achieve during each single task and the related tolerances.

For simplicity, some parts of the document related to the application I developed during my thesis work, which I will discuss in the next chapters, are listed below. In the first part of the document given by the client, there is a general description of the electronic appliance, as for example the Power Module which constitutes the main control electronic for the dishwasher application. It consists of the EMI-filter, the power supply, a microcontroller, the communication interfaces (D-Bus II), the sensor inputs and the actuator outputs. There will be HW-variants with different functionality for nominal power supply voltage (220V-240V).

The block diagram reported in the manufacturing and test specification document of the board to be tested is shown in figure 1.2 on the next page.

1.2 Manufacturing flow and special requirements

The manufacturing flow it is important to achieve superior customer response. In fact the producers are able to obtain significant cost savings, increasing revenues thanks to a deeper one understanding of the signals of the demand and customer response to more narrow production cycles and on-time deliveries. In this section the customer inserts some particular indications, which are critical in the insertion and soldering phase, e.g. Requirement for THT¹-insertion and -soldering. Requirements for THT reported in the aforementioned *Manufacturing and Test specification* document, provide the analysis of the distance between resistors. The gap of at least 1 mm ensure that the connectors seat solidly on PCB and the maximum distance of the through hole connectors between PCB and general component is of 0.2 mm.

Leaving aside these requests, it is important to focus the attention on figure 1.4 on page 18, where the production flow for the analyzed board is reported. Here it is important to highlight the different step that lead to obtain the pack and deliver of the product which has been tested.

After SMT and THT soldering, visual inspections of placement and soldering quality of the mounted PCB have to be done or check with AOI². In this phase is important to verify the solder and leads defects, the presence and the current position of the components, shortcut pad to pad or via and the polarity of capacitors.

In particular in the board analyzed, due to the component requirements and

¹THT stands for Through-Hole Technology - electronic components are mounted on one side of the board exit hole. Their extremities in the form of wires are threaded through the prepared holes in the plates and soldered on the opposite side of the plate.

²Automated optical inspection (AOI) is an automated visual inspection of printed circuit board(or LCD, transistor) manufacture where a camera autonomously scans the device under test for both catastrophic failure (e.g. missing component) and quality defects (e.g. fillet size or shape or component skew). It is commonly used in the manufacturing process because it is a non-contact test method. It is implemented at many stages through the manufacturing process including bare board inspection, solder paste inspection (SPI), pre-reflow and post-reflow as well as other stages.[2]

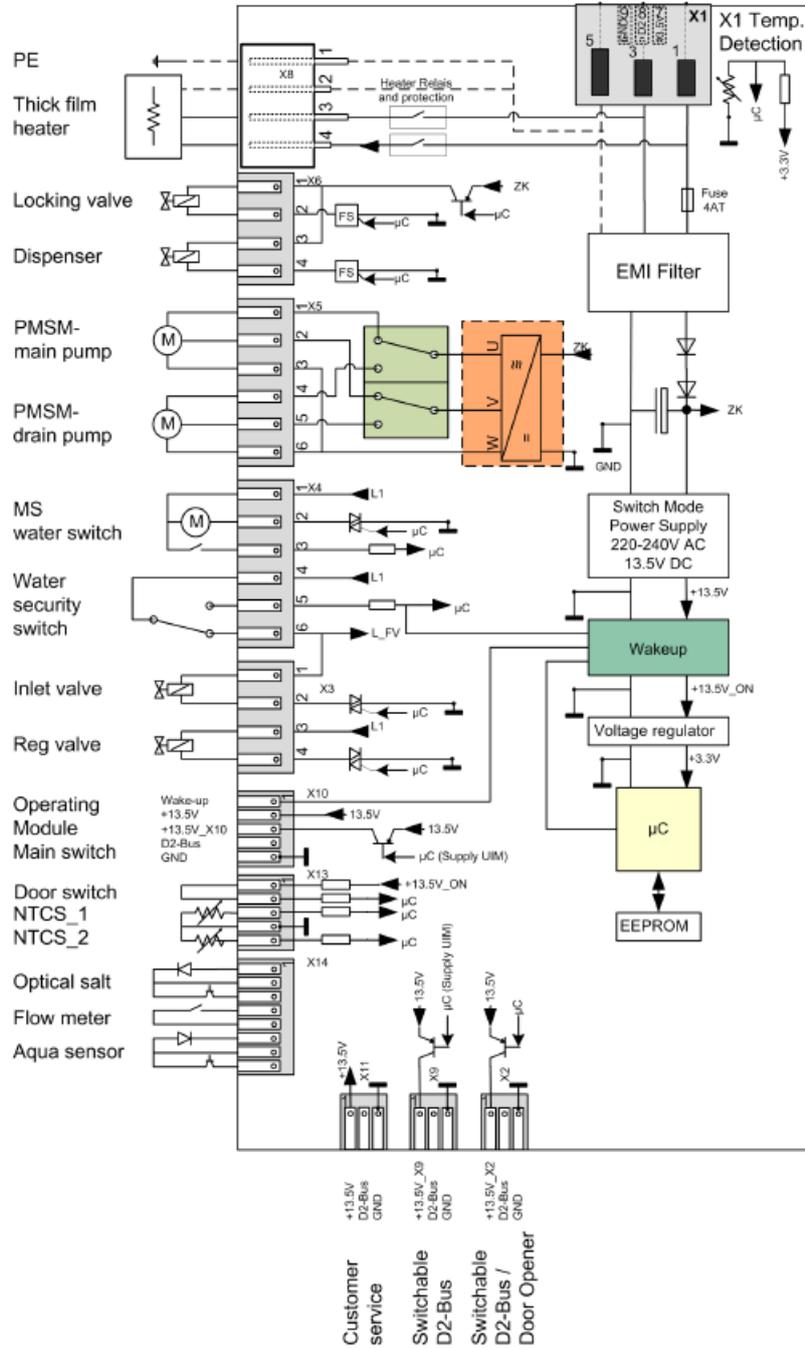


Figure 1.2: Block diagram of the board under test

layout, it is present an electrolytic capacitor with 3 pins. The third pin of capacitor, see figure 1.3, is needed for assembly only, and in particular to guarantee the correct polarization position on the board and has no electrical or mechanical function after soldering. Due to this reason customer does accept also solder joints with a fillet and wetting of lead and land lower than 270° for the particular pin case (required minimum 90°). Going forward through the flowchart it is possible to highlight two

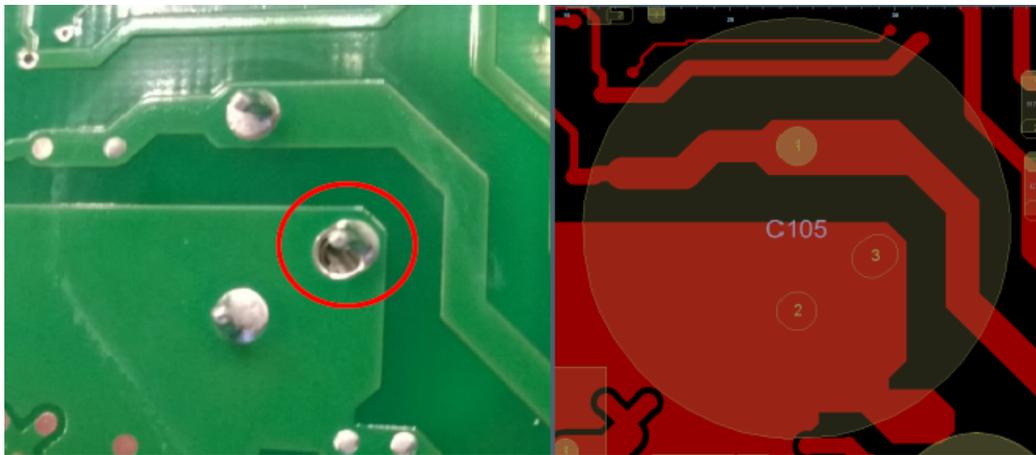


Figure 1.3: Product specific exception - 3 pins electrolytic capacitor

other fundamental points, which are the focus of the development of my project: In circuit test and functional test. For obvious reasons, these two focal points will be discussed separately in the next chapters, trying to highlight the most salient points that have distinguished the various steps performed during my work. In figure 1.4 on the following page, it can be seen how the last step *Pack and deliver*, it is possible only passing thought a vital step that is called Audit test, explained in Section 1.2.1.

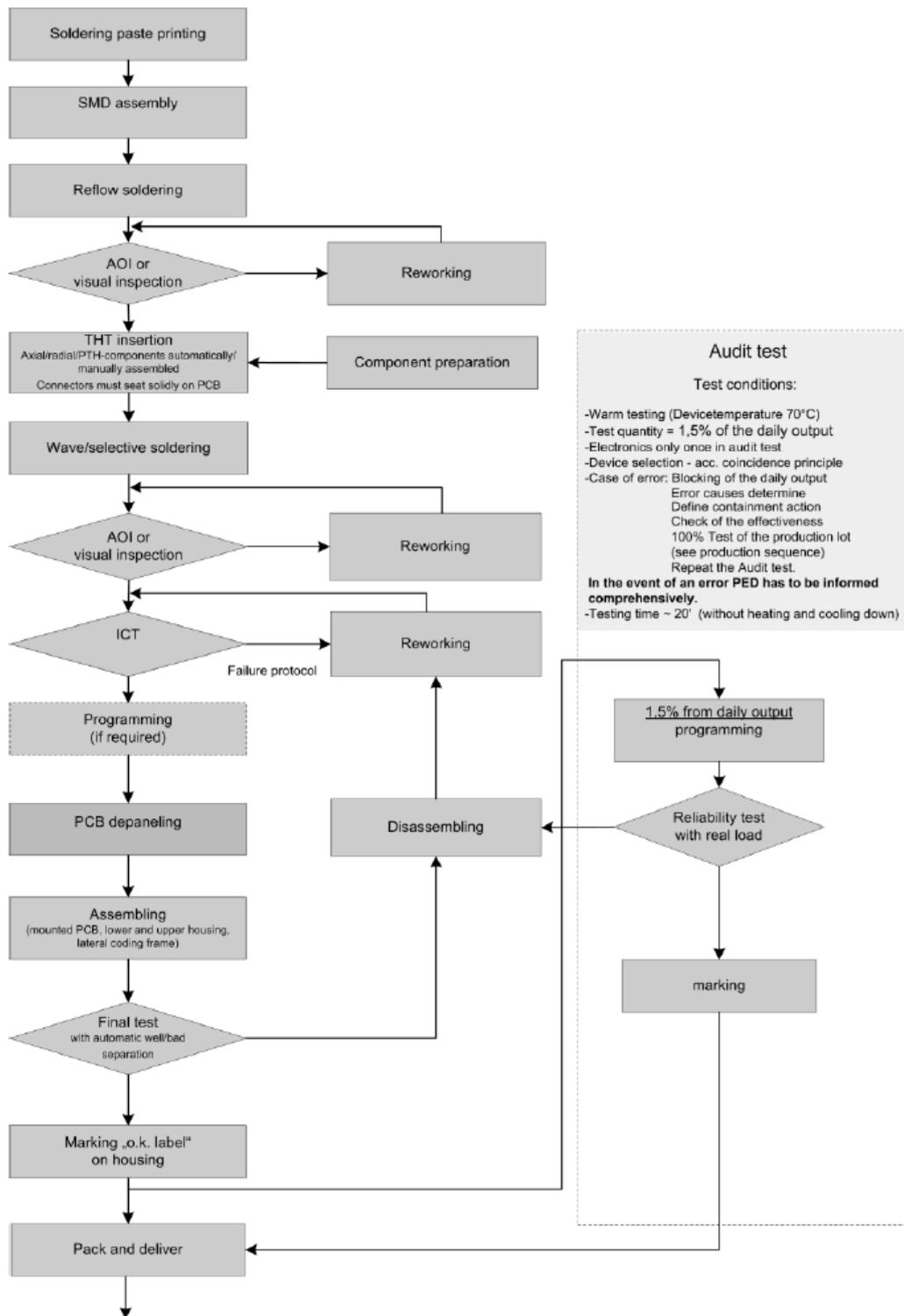


Figure 1.4: Manufacturing process

1.2.1 Audit test

Audits are activities designed to measure the compliance of systems, processes, products with certain required characteristics and a verification of the application.

Plan audit activities and developing an effective work strategy, it is first necessary to identify the significant cycles, link them to the underlying activities and then "map" the evidence. This will then provide a first database to arrive at an initial assessment of the risks inherent in each cycle and therefore the risk of internal control. Understanding these risk concepts, will be an integral part, along with business risk and the risk related to the work of the auditor, for determine the qualitative and quantitative extent of the control work.

The audits that are carried out in the initial phase of the design, if requested by the customer, go to clarify the point on feasibility analysis. In the event of a positive outcome, the various testing phases follow, in which the different steps reported in *Manufacturing and Test Specification* are dealt with.

In the specific case addressed, test of the power consumption, measuring of the temperatures (ambient, inside of the housing and on some components) and readout of the audit tested electronics are made during launch of series production. The release of audit test has to be done during two days production acceptance.

Indeed is specified that to guarantee quality for mass production a certain percentage of units have to be inspected with an audit test, analogous to real conditions. Compared to functional test, it runs with an elevated ambient temperature of 70°C and increased operating time (about 14 minutes). The test is used primarily to monitor voltages and to review the correct triac- and relay-switching. The test is performed with the majority of real loads.

Whenever the specifications reported in the audit are respected, what follows, is to proceed with the mass production and therefore the introduction of the product on the market, with the necessary guarantees provided to the customer where no field return is acceptable.

The pursuit of quality in all aspects of production, from initial studies to implementation and product delivery, is one of the strengths of SPEA's quality system, which is UNI EN ISO 9001: 2015 certified. The Company guarantees the constant compliance with high quality standards, through a solid project management. Accurate selection and control of suppliers and production processes, the execution of tests and controls, allow to reach, with a defined and accessible quality, the highest customer satisfaction levels.[3]

Chapter 2

Test system and program development

Testing of electronic boards represents one of the fundamental points in guaranteeing quality certificates. The board is built using a more or less complex manufacturing process depending on the technology used. Process defects and component damage may occur during manufacture. Defects are usually due to assembly or welding errors, while component damage can occur because of mechanical, thermal or electrostatic stress. To this type of anomalies should be added any failures due to broken or malfunctioning components. Furthermore, the percentage of these drawbacks is greater in the case of surface-mounting technologies compared to the conventional through hole technology due to the fact that THT provides stronger and so better mechanical bonds than SMT, making through-hole suitable for components that might undergo mechanical stress, such as transformers or connectors.

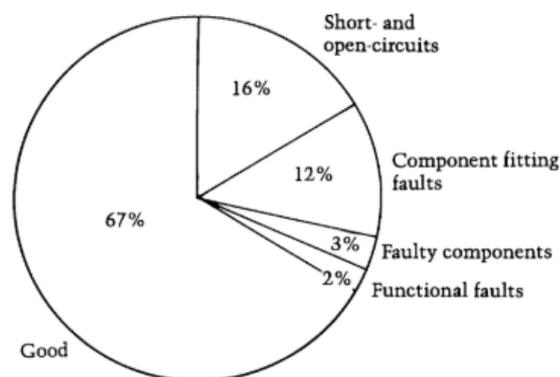


Figure 2.1: Faults of a printed circuit board

The test therefore represents a specific phase in the manufacturing process of an electronic board. It is used to ensure that the board produced is perfectly compatible with the project specifications in terms of functional and over time performances, e.g. evaluation of mean time to failure.

Figure 2.1 on the previous page is a pie chart of typical printed circuit board faults as percentages of total boards after assembly and soldering. While, ideally most of the boards are good and work first time, the majority of faults are seen to occur in areas which are simply manufacturing defects problems: solder-bridge, open circuit, missing, wrong and incorrectly inserted components, components damage during production.[4]

To carry out the testing of an electronic board, the Automatic test equipment (ATE) is the system used to check semiconductors, electronic circuits and printed circuit boards automatically. The most important types of ATE are the *Flying Probes* and the *Bed of Nails* systems.

2.1 *Flying probe systems*

Flying probe test systems use electro-mechanically controlled test probes to make contact with the board to be tested and it is designed to be applied for prototypes and short production runs.

SPEA *Flying Probe Series* is designed to cover the widest range of test requirements for electronic boards offering everything necessary to respond flexibly to production needs. All this is possible thanks to the high mechanical speed, probing on one or two sides, extreme precision, automatic loading of the board, overall configurability and rapid configuration changes.

Extreme mechanical accuracy enables the flying probes to directly contact the smallest pins of micro-SMD packages, as it can be seen in figure 2.3 on the following page.

Flying probe system is an innovative multi-process platform with high-resolution measurement electronics that allow to reduce the acquisition time to a few microseconds. Performances accuracy are supported by on-axis and sub-micron resolution Linear Optical Encoders on each XYZ axis, making 4080 suitable to touch 50 μ m pads at high speed and without leaving marks on them, like no other flying probe system can do.[5]



Figure 2.2: 4080 Flying Probe Tester

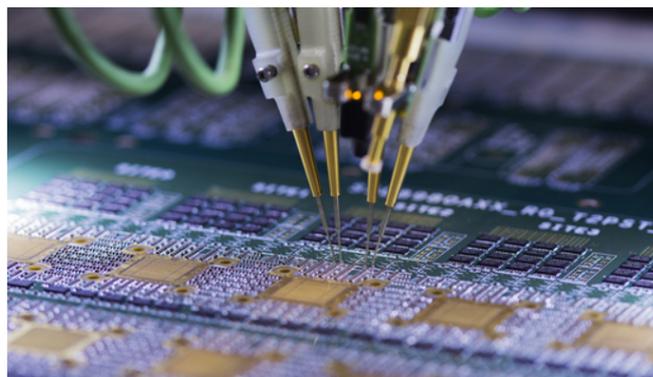


Figure 2.3: 4080 Flying Probe Tester contacting

The structure of the 4080 system is made by granite, that combined with state-of-art linear motion technologies ensuring unprecedented probing precision at ultra-fast test speed. Compared to conventional iron or steel, natural granite offers best damping characteristics and thermal stability, minimizing vibrations and deformation effects that would affect accuracy and reliability through time avoiding risk of damage even for the most delicate electronics board.

2.2 *Bed of nails system*

Bed of nails systems (BON), is a traditional electronic tester witch use a mechanical interface between the system and the board to be tested, called a testing adapter or, more commonly, “fixture”. The fixture has numerous pins which are inserted into holes in a epoxy glass panel aligned using *nails* to make contact with test points on a PCB. Each nail is also connected to a measuring unit of the system through a wire. The unit under test is pressed down on the fixture, to allow the contact of each test point, through the use of a mechanical presser plate called also called *castle*. For a better understanding each part will be explained in detail in the following chapter. For the test of the boar that has been analyzed, the In line 3030 series has been used, the one reported in figure 2.4.



Figure 2.4: 3030 Bad of nails tester

The 3030 tester can be equipped with up to 8 *test cores* that operate in parallel. Each core has independent CPU that guarantees no delay between instrumentation and PC local memory. High-performance relays provide fast switching time connecting instrumentation resources through wiring with the test points of the device under test. The instrumentation included in each *test core* is related to the type of test that should be performed, in fact there is the possibility to execute different measurements at the same time, reducing the test time thanks to a single test Core. As it can be seen from figure 2.5, provided a UUT, a panel of 8 boards, the time required to test it using an octa-core system equals the time spent to test just 1 board.

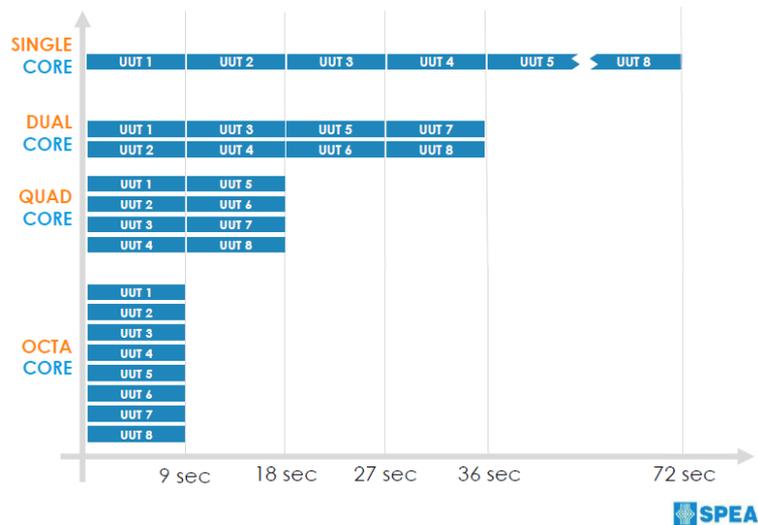


Figure 2.5: 3030 Multicore application

2.2.1 Fixture design

Analysis of the initial data, as reported in section 1.1, are useful information for designing an application and in particular, it is what dictates the choice of the system to be used. From now on, the first step is to define how the UUT must be positioned in the test area of the chosen system.

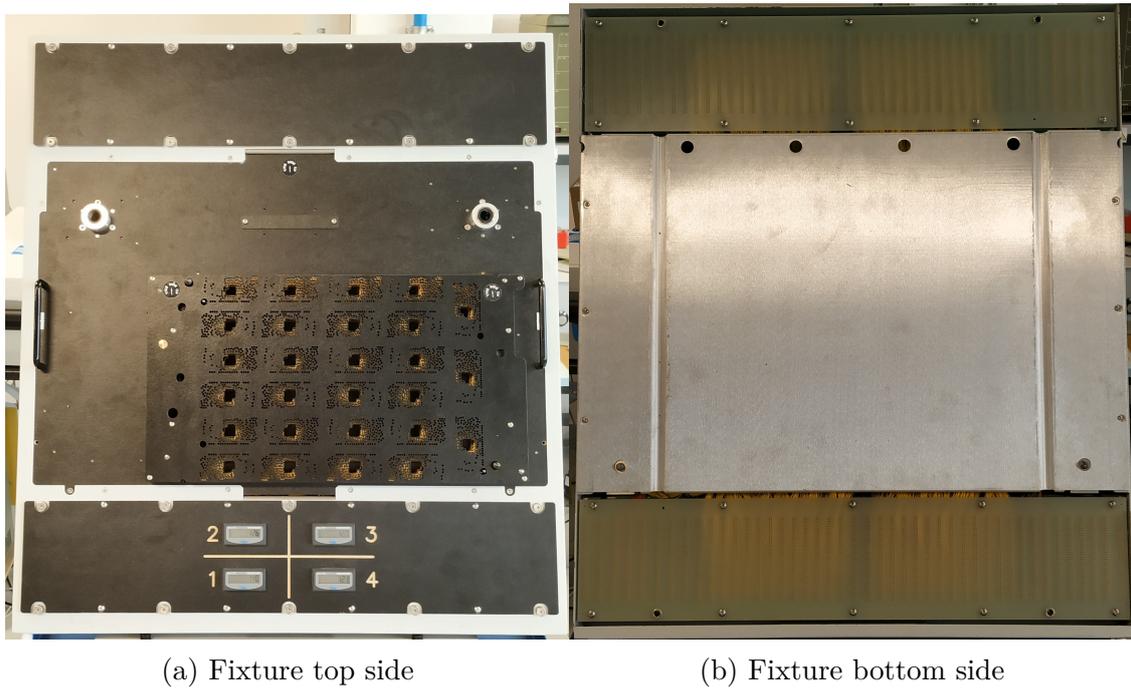


Figure 2.6: Fixture design

Indeed, it is fundamental define the best side on which the board must be contacted. In the case of a bed of nails tester, the fixture acts as the interface adapter between the board to be tested and the system. The mechanical fixture designed procedure is carried out through the *Test program generation* which is described in the next section. The first target is to obtain the drilling file, so that the plates which make up the adapter can be drilled. This file contains all the X/Y coordinates corresponding to the board test points that must be contacted and in correspondence of which the hole must be drilled for the insertion of nail receptacles. The fixture, figure 2.6, contains specifically positioned test points or probes (commonly called *nails*), in order to contact the board test points.

Typical structure of the probe, reported in figure 2.7 [6], is made by a receptacle, on which is inserted under pressure granted by a spring, the nail tip, used to contact the test point of the unit under test. The most important elements of a probe are the type of tip, the collar height, the receptacle and the spring force at working stroke.

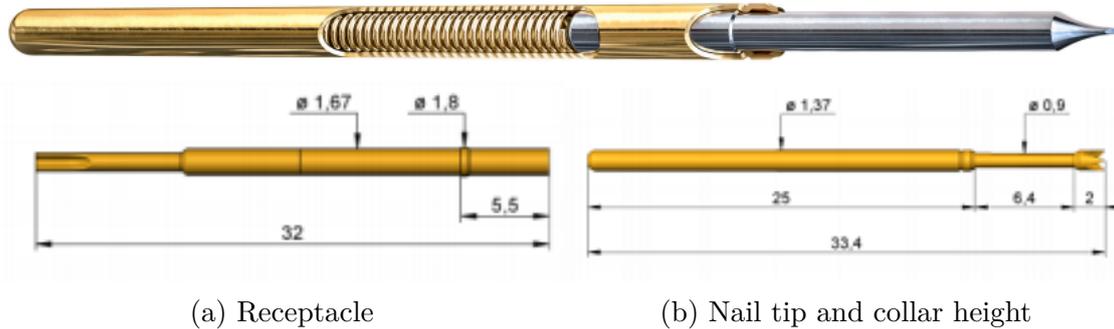


Figure 2.7: Test Probes

It may be necessary to construct a test interface between the testing system and the UUT itself, in order to test a unit under test. The interface makes system channels, generators, power supply, and others HW resources totally or partially available so that they can be used for the design of a test adapter. For bed of nails systems the adapter takes all the available HW resources to the system interface, by means of the interface connection that can be noted in figure 2.6.

For the underlined system, the fixture is made by two system interfaces, where each of them are based on two core, for the total of four bay. The number of available channels depends mostly on the number of bay used, because of the fact that each bay work independently from the others with their own stimulus and power supply unit. Of course the numbers of available channels decreases if compered with a system interface with single bay. Every channel of the system, is connected with the designed test point on the UUT. For a better understanding of how these connection are carried out, we must focus our attention on the pre-assembly phase of the fixture interface.

The type of application that has been analyzed require test in which the accuracy of the signals is of particular importance, as the On Board Programming and the functional test, so for these reasons the use of a plate, called ground plate(Copper plate) has been inserted from the bottom side of the adapter for each bay of the system used, as shown in Figure 2.8

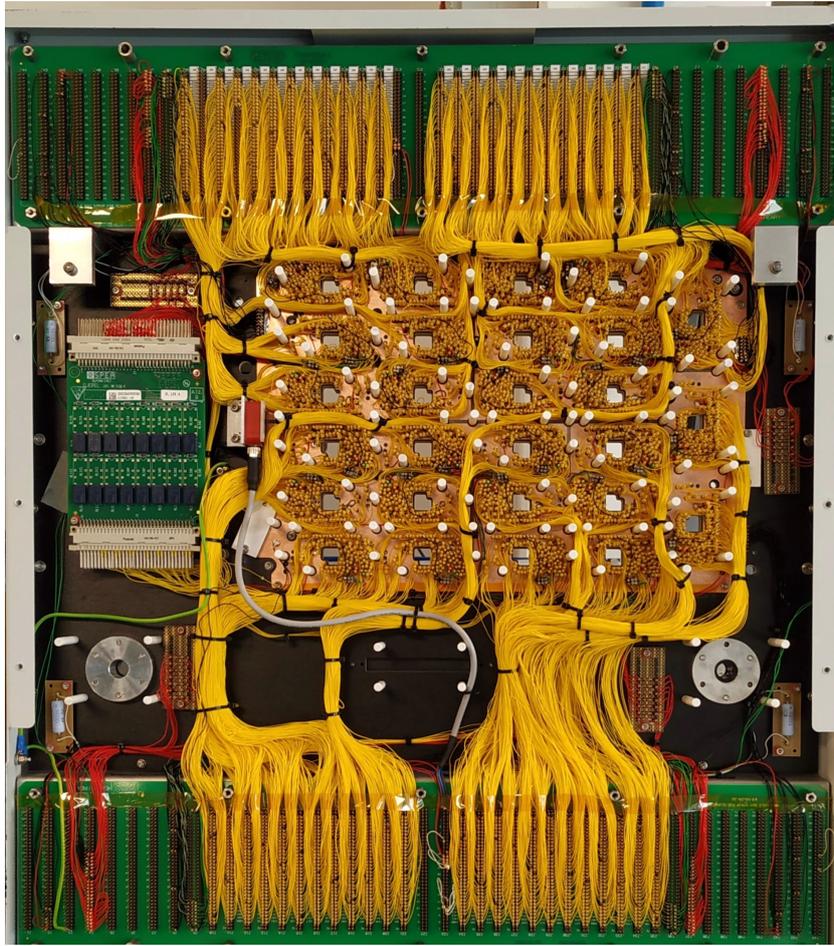


Figure 2.8: Fixture wiring

This plate is used to distribute the UUT ground net uniformly over all the area, where the receptacles are assembled. The cables, which are connected to the UUT, carry the grounds of the generators and the power supply of the test system. On the top of the ground plate is present the drilling hole plate where the receptacles are inserted. On the other side, it can be seen how the termination of the receptacle is connected through wires to the system interface, visible on the top and bottom of the figure 2.8. Obviously the wiring between the pins of the system interfaces and the receptacles, corresponding to the assignment of the machine channels and test point of the board, is designed by the Leonardo software in the test program generation phase. Furthermore, when additional add-ons or special connections are required, a schematic wiring fixture is constructed, shown in appendix A on page 83.

In the Automation page, the connections of the discharge resistors, used during the in-circuit and functional test, for the discharge of the capacitors of the device are shown. Additionally, a section regarding the selection of the presser plate and fixture codes can be observed. During testing, the system must be able to recognize which type of presser and fixture are present inside the test area. In this way, if the codes do not match, there will be an error message that will not allow the presser to go down destructively. This safety mechanism is adopted because unconsciously the operator may insert the presser relative to another fixture or vice versa. In the following pages the connection to the mass chain of the instruments involved are shown, and how their outputs are connected to the TPs of the DUT power supply. In particular, given the presence of the DC/DC used in the functional test phase, here are reported the connections of the input signals and therefore the machine channels that will be adopted in the functional code to allow its operation.

The connection of the fixture, with the overall system is realized through a system interface pin, called *strips*, that results connected with the machine boards, figure 2.9. The use of direct connection between the instrument output and the system interface pins represent one of the advantage of the 3030 model, where no wire are needed for instrument connection.

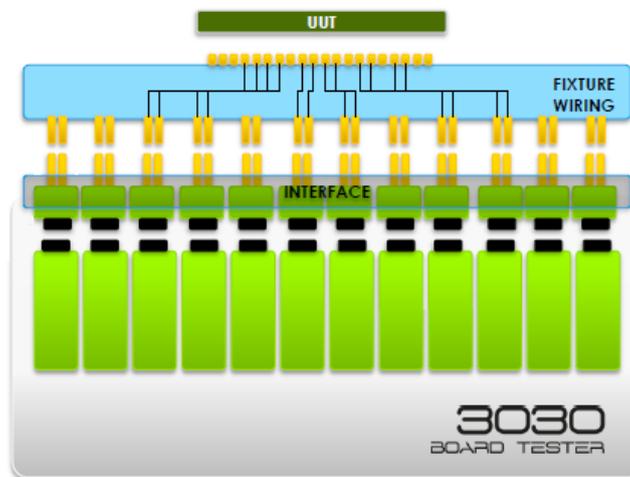


Figure 2.9: System interface connection

Once the cabling has been completed and checked, the adapter is then assembled so that it can be used.

2.2.2 Presser Plate design

The presser plate is used to press the UUT to contact the probes that have been disposed in the fixture design phase; in this way all the nails enter in contact with the relative test points of the unit under test. The presser plate is composed of a special plate made of plexiglass, delmat or aluminium where, after the appropriate design phase, pressure rods are positioned to press the UUT. Particular attention must be paid when deciding where to position the pressure rods and where they will rest on the board. Depending on the type of board to be tested, the design must guarantee the planarity of the board where there must be no indication of deformations of the board when pressed by the plate. The pressure rods must be at a safe distance from the component assembly of at least 2mm to ensure during the descent phase that everything is done in such a way that no component can be damaged. Figure of the realized pressure plate for better understanding is reported in figure 2.10

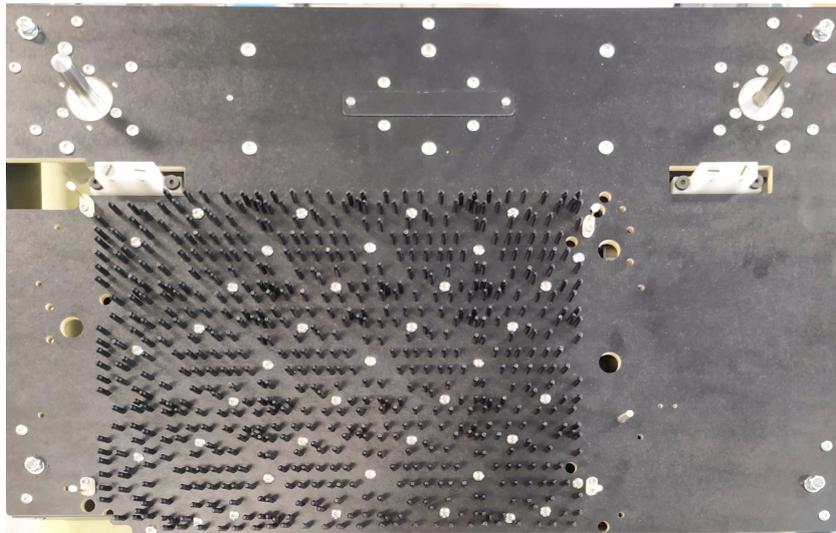


Figure 2.10: Presser Plate

2.3 Test program development

The test program (abbreviated TPGM) is a software tool, which has been automatically developed by SPEA, called *Leonardo*, to perform the test of the board. The SPEA software is able to generate a test program automatically, based on the indications supplied by the operator, starting from the construction data of the board

included in the CAD files, provided by the customer, which contain the information regarding the electrical connections of the board, the values and the names of the components assembled and the space required to assemble each component. The program is generated, based on the requests and by exploiting the potentiality of the test system of whoever has ordered the work.

The accessibility and testability circuit analysis enables to know the diagnostic coverage already during the generation phase, with no need to use the test system. The circuit analysis enables to identify the parallel of components, both direct and indirect, to calculate the circuit nodal impedance, to highlight low impedance connections and all the configurations or peculiarities of the board with the aim to reduce the debug operations as much as it is possible. All the analysis results are stored in a data bank available for the next phases of the automatic generation. The available contact points are analyzed and classified by Leonardo in order to define the board accessibility.

The creation of a project is fundamental for the generation of the test program. The project will also include all the information necessary for the construction of the test adapter, which may have to be used for the test.

The board data necessary for the generation of a test program, are grouped as follows:

- CAD file (i.e. the files which contain the information regarding the board electrical connections (net list), the values and the names of the assembled components (part list)). They are essential for the maximum performance of the SW generating the program;
- Electrical diagram of the board;
- Board part list or Bill of Material(BOM), which consist of an assembly list of the components related to the layout of the board from the top and bottom sides;
- GERBER files which contain all the data necessary for the construction of the printed circuit of the board;
- Test specifications request essential if a functionality test of the UUT is required, as reported in the Chapter 1;
- Programming files and drivers to perform the *OBP* if it is necessary to program a component during the test.

It is essential to know the configuration of the system that has been installed from the client in order to validate every operation during the test, because there are different input data to be supplied for the creation of the project, depending of the type of SW/HW to be used. In particular, on the board that has been tested, with the use of the 3030 system, particular attention had been dedicated to the choice of the number of core used and so of the bay on which the fixture developed was based, as was previously described in the section 2.2.1. Since a panel composed of four board has to be tested, a system with 4 cores was chosen in order to perform parallel operation.

Indeed, for the application that has been developed, the customer's request to be satisfied was to create a program capable of testing not only one type of board but capable of handling different assembly on products which have the same printed circuit, generally called *variant* that differs of some mounted or not mounted component. Strategies used by the customer to attack the various market segments, thanks to the creation of products that although internally are similar, differ in the functions that they are able to fulfill and this automatically reflects on the selling price.

In this particular case, the customer has made available the schematics and the bill of material related to each variant that have been uploaded in Leonardo. There are different types of TPGM which can also be performed in sequence, depending on what has been requested.

Following are a few program types:

- *ICT Power Off*
Test including the check of discrete and passive components;
- *ICT Power On*
Test which powers the UUT and performs the test of the components which need power to be checked;
- *OBP*
Test for the programming (loading of data) of one or more components during the test;
- *FCT*
Test which verifies the functionality of the UUT, based on the test specifications generally written by the designer of the board;

- *Optical Test*
which verifies the correct assembly of the components and that the soldering is optimum;
- *Open pin*
Test which verifies that the pins of the integrated components have been correctly soldered.

Chapter 3

In-Circuit Test

To develop a test program, it is important to know the test concept. This chapter provides an introduction of the notion and reasons for using Automatic Test Equipment. The in-circuit test verifies the functionality of the single component and checks that it is correctly mounted on the board. Different ICT test concepts are analyzed:

- *Process test*, also defined as Manufacturing Defect Analyzer (MDA), needed to detect process defect such as missing, misplaced, or wrong components, not soldered pins and short circuits.
- *Component test*, needed for verification of the functionality of the individual active and passive components, so coincide with “common” definition for in-circuit test.
- *Parametric test*, it is the test conceived to measure the components typical parameters in addition to the basic function and process defects.

3.1 Test Program debug

The in-circuit test is also defined power-off in-circuit test and establish an important part of a production process in which passive and discrete components mounted on the PCB are tested without supplying the necessary power for the complete functioning of the board. The Leonardo software uses an adequate test profile for each type of system to be used, which can be varied by the user depending on the needs. Based on the elaborated data coming from the libraries, the circuital analysis, the rules and structures implemented, the software will proceed with the generation of a test program automatically. When generating a test program, it is

essential to build the *organizer*, i.e. set of instructions which are performed by the system (the handling of the system and the execution of the parts of the test program of the components) in automatic mode. The generated program, moreover, consist of another fundamental part called *test plan* where tasks for each testable component present in the UUT are generated. There can be several test models in the libraries for each component type of the UUT; the most suitable model is chosen by the software from the calculation sheets, which take into account all the input data supplied by the designer. Such a test model can be varied in the debug phase to try to obtain the best possible component test result. In 3030 environment it is common procedure before starting any in-circuit or functional test to proceed with the so called *fixture check test*. Based on the type of system, this also called “pre-screening” test and it is generated for identifying some types of errors due to the presence and use of a test adapter. This test is basically composed of two parts : *short test* and *floating test*. Respectively in the short test, the unit under test is replaced by an isolated plate, generally made of fiberglass, to check for the presence of any unwanted shorts during wiring inside the fixture. In the floating test instead, a copper plate is used to check that all the nails necessary for contacting the board are present. Furthermore, to ensure the correct functioning of the ICT test, additional tasks have been included, such as the presence of capacitor discharges task. Electronic component circuit must be discharged in order to protect the ICT against external voltages leading to measuring errors and damage of the test adapter and so to avoid the risk of compromising the correct operation of the UUT. Last, the verification of the correct power supply through the use of the system buster or driver depending on the voltage required. My job was to adapt the layout of the organizer according to the specifications requested by the client. In particular, a test sequence ICT, figure 3.1, has been adopted in order to guarantee no errors. In fact after the verification carried out through the fixture check program, a second organizer was compiled and adapted to the 3030 model present by the customer. In particular, the written program allows the user to be able to start a completely automated production, where the board or the panel of board present in the production chain are subjected to the test and sent to the next step without the user having the need to intervene.

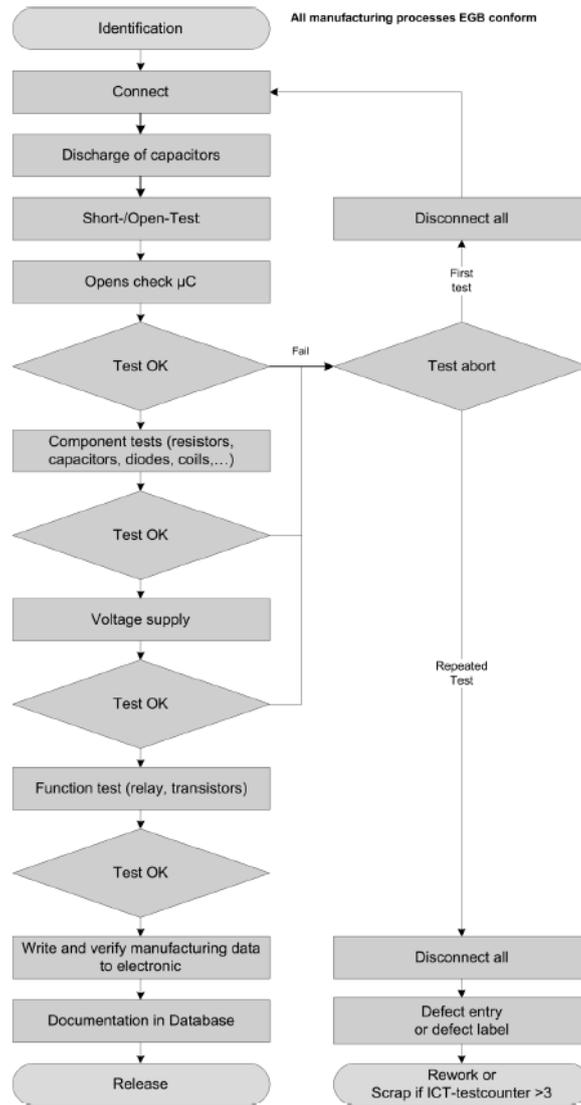


Figure 3.1: Test sequence ICT

3.2 Power Off test

Debugging a test program means debugging the test of every single component, so as obtain the positive test result or the complete functioning of the device. In figure 3.2, are summarized the principal class test conducting on the examined UUT.

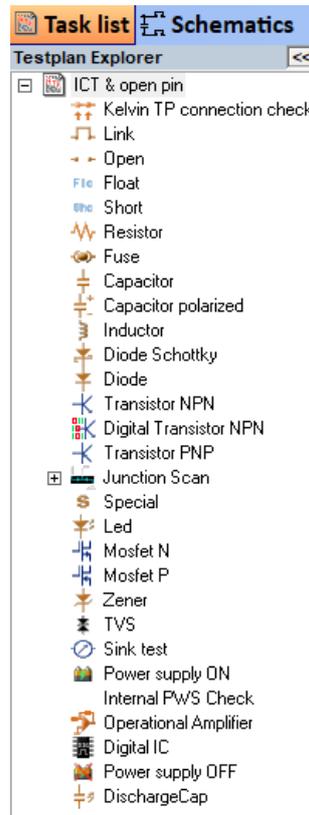


Figure 3.2: Task list

Before the software generation, some rules have been adopted for the correct formulation of each task following specification from the client. Indeed, before starting the test, it is a good idea to analyze a file generated by the software, called coverage analysis, where the software supplies a report for every phase performed, in which any anomalies found in the process are noted, an example is shown in figure 3.3 on the next page.

An anomaly in the test program generation could be the lack of a test generation for a component. There can be different reasons:

- *Component not present in the libraries;*
- *Incorrect task generation;*
- *Test in the libraries is not usable because of the circuital configuration of the board.*

The program must therefore be completed by inserting the missing test manually.

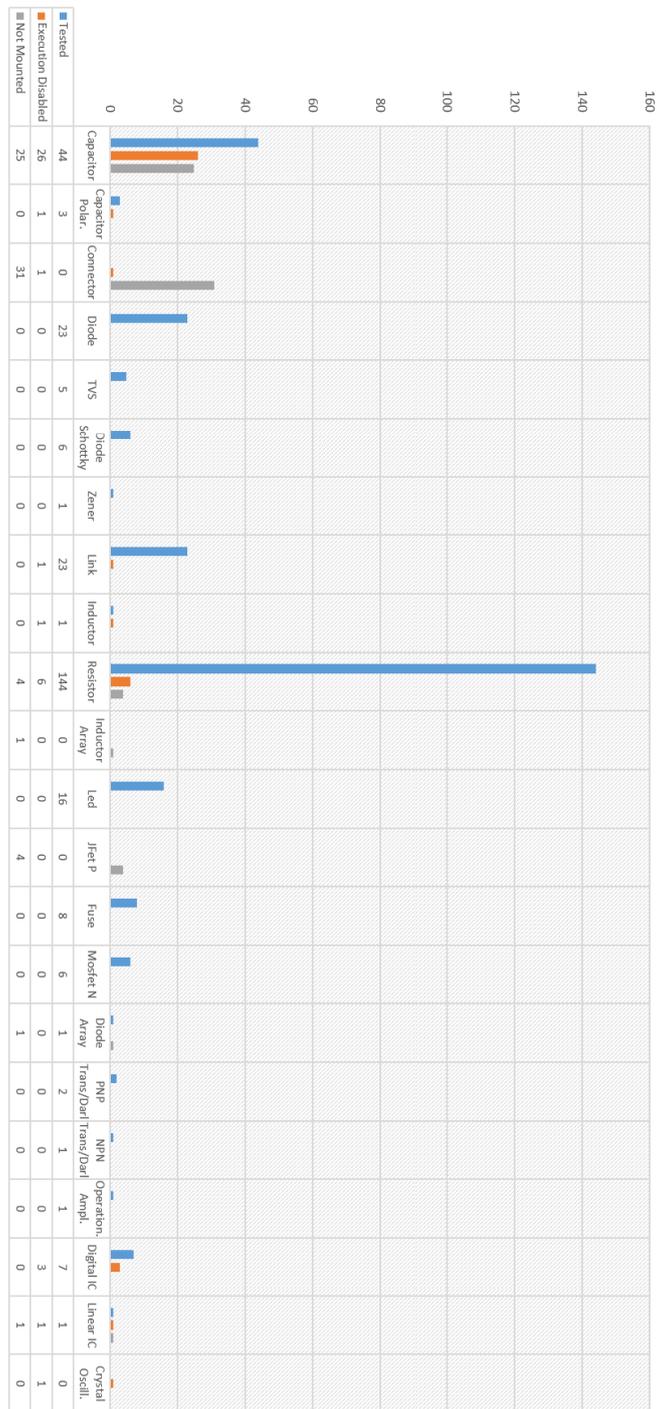


Figure 3.3: Coverage analysis

Each task can be written by withdrawing a component with similar characteristics from the library and then using the bus lines; connect the possible drivers and DVM associating the correct test point present on the board to each of them. The most relevant specifications provided by the client are listed respectively in each relevant subsection, where an explanation of which test and how is conducted in order to adopt every customer's request. Before to proceed with the explanation of every task, passive test method such as *guard* and *kelvin* methods will be analyzed first, because they represent a fundamental concept that is integrated when necessary in each task. Of course, to avoid falling into banality, only the most significant debugging methods are analyzed.

3.2.1 *Guard techniques*

The target of the in-circuit test is to test each single device considerable insulated from the other devices of the board under test. The guard is one of the techniques used to insulate the device from rest of the board. There are two different type of guard to use according the instruments connection:

- Active guard
- Passive guard

Active guard

The measurement of a device can be influenced by the circuitry in which it is included and so the measured value can be result lowest than the expected one. There are cases where the current measured on the Z_x device under test does not reflect the one forced by the driver, because other devices influence the measure absorbing the leakage current.

With reference to the figure 3.4 on the following page, it is possible to draw the following observation: $I_0 \neq I_{Z_x}$ because $I_0 = I_{Z_x} + I_{Z1} + I_{Z2}$. It is possible to insert a guard point, voltage follower, to bring point A to the same potential as point B, obtaining a nil potential difference. In this way the $I_{Z1} + I_{Z2}$ current that flows in the series $Z1 + Z2$ will then be nil and consequently the measurement of Z_x can be taken with the required accuracy.

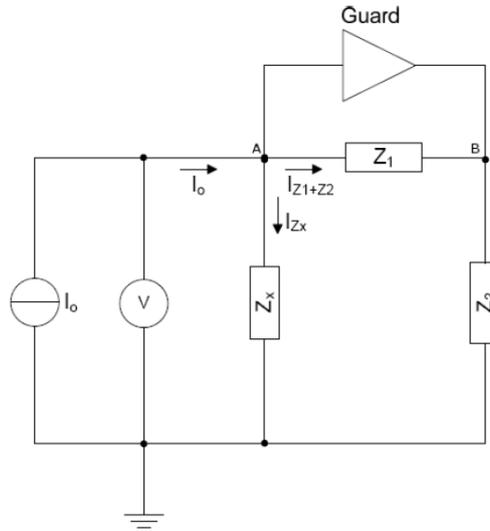


Figure 3.4: Active Guard

The active guard is used in the *Grounded measure test* where device under test Z_x is connect in parallel to the Generator (Voltmeter or Ammeter).

3.2.2 Kelvin method

When the value of the resistor to be measured is $\leq 100\Omega$, the contact parasite resistors $R_h - R_c$ and wiring harness resistors of the system and fixture might influence the measurement. To compensate for these parasite resistors it is necessary to apply

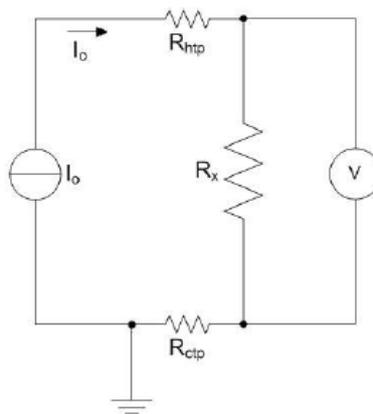


Figure 3.5: Kelvin Grounded Voltage measurement test

the four-wire technique (Kelvin) on the device to be measured. The Kelvin measurement uses a current generator and measures the voltage of the resistor removing the effect of the parasite resistors of the channels. Due to the high impedance of the input circuit of the measure board, the current running in the branch in which the voltmeter is connected is nil and therefore the measured voltage corresponds only to the difference in potential of resistor. The measurement method consists of adding a Kelvin test point for each resistor's pole, but it is possible only if the net on which the resistor is connected are equipped with at least four test points. The instruments are connected as shown in figure 3.5 on the previous page. The current trend at the terminals of the resistor is shown in figure 3.6:

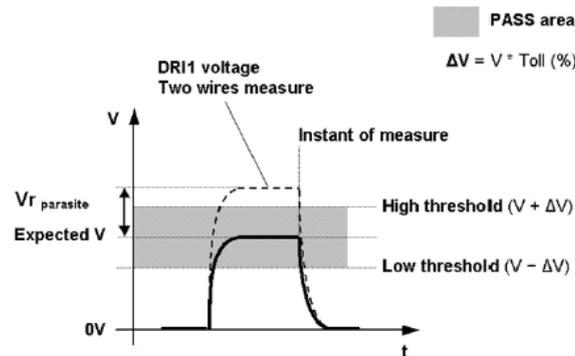


Figure 3.6: Kelvin Grounded Voltage measurement test result

3.2.3 Float test debug

The purpose of the following test as previously mentioned is to verify the contact between the system channels and the test point of the UUT. The system measures the equivalent resistance of a test point with respect to all the others in short for each channel connected to the UUT. The resistance is measured by forcing a very low current and measuring the fall that it creates. This voltage will be as low as the equivalent resistance is less between the test point under test and all the others. If the test result is lower than the expected resistance threshold imposed to $200k\Omega$, we will have a positive test result. If a floating error will be shown with the number of test points in error indicated the possible parameter subjected to modifications for the debug are:

- Exclusion of a test point due to circuital configuration. i.e. test point is not connected to any component;

- Modification of test time;
- Modification of resistance threshold;
- Change of test model.

3.2.4 Short test debug

The purpose of the following test is to verify the absence of short circuits between the UUT nets. For each channel connected to the UUT the system injects a known current and verifies the voltage with respect to all the others channels in short between each other. This voltage will be as high as the equivalent resistance is greater between the examined test point and all the others.

3.2.5 Resistor test debug

Tests resistance follow the Ohm's law. Based on the value of the resistance to measure and how the latter is influenced by other component present on the UUT, a suitable test model is chosen.

Resistance	Measurement method
$\leq 100\Omega$	KELVIN measurement
$100\Omega < R_x < 100\text{ K}\Omega$	FORCE I MEASURE V measurement
$\geq 100\text{ K}\Omega$	CURRENT COMPENSATED measurement

The resistor test is performed by measuring the value and comparing it with the predetermined positive and negative tolerance thresholds. These tolerance values, has been provided by the customer, where a resistors with a nominal tolerance of 1% and of 3% must be tested for a precision respectively of 5% and of 7%.

The resistive value must be measured when the voltage (or current) measured has become stable in time. It may happen that the test time generated automatically is not enough to stabilize the value measured, one of the causes of this may be an unexpected capacitors value.

The measured signal for each task, not only resistive, is monitored by an oscilloscope, so it is sufficient to visualize on the screen the measured signal and increase the test time so that the measurement is taken when the measured signal start to be stable. In some cases it is possible that the resistor introduced into an electric circuit, do not behave solely as a resistive component. There are cases in which the resistor being measured is in parallel, so a guard technique could be useful for

the testing, as explained previously, or cases in which the resistor under test is influenced by parasite capacitors and inductors in the circuit. In the latter case, if the resistor is positioned in parallel to a “high” capacitor, the high time constant $\tau = R * C$ determines a long transit time in order that voltage can stabilize and the measurement can be performed. If we are measuring the voltage drop on the resistor under test, the correct value in this case is not viewed immediately, because there is a minimum test time t needed to charge the capacitance under observation. To compensate this issue, it is required to use the current measurement method. The current limit programmed on the driver will be greater than the nominal current that will flow in the resistor under test, therefore faster transient time, see figure 3.7

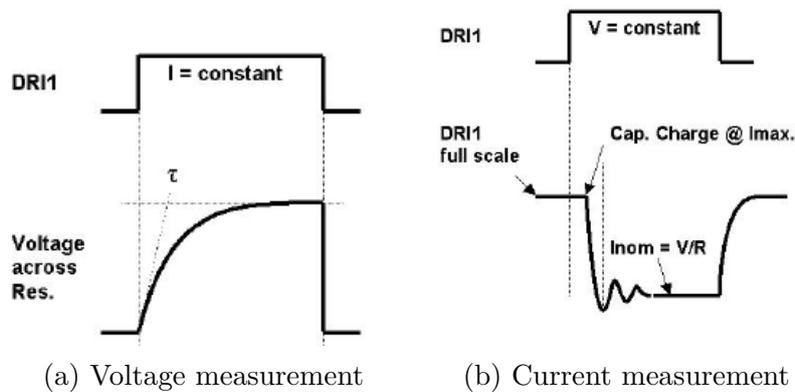


Figure 3.7: Voltage and Current measurement methods behaviour

3.2.6 Capacitor test debug

Capacitor test is obtained exploiting the relation between the voltage and current of a capacitor expressed by $I = C \cdot \frac{\Delta V}{\Delta t}$ for DC signals and by $V = \frac{I}{J\omega C}$ for AC signals. Based on the capacitor value under test and the circuit configuration, different test method can be choose. Customer request, I had deal with are the following:

- Aluminium electrolytic capacitors $\pm 20\%$ component tolerance
- Wired film capacitors $\pm 20\%$ component tolerance
- Ceramic capacitors $\pm 10\%$ component tolerance
- Process and system tolerance $\leq \pm 5\%$

- Minimum tested capacitance $100pF$

From here on, some test examples of capacitor I cope with during the test are shown.

Voltage measurement test

In a typical $R // C$ circuit, with a capacitance range between $100nF - 10\mu F$, it is possible to drive a known current into the capacitor under test and measure after a given time interval ΔT , the voltage drop, following : $V_{Cx} = I \cdot \frac{T}{C_x}$, see figure 3.8.

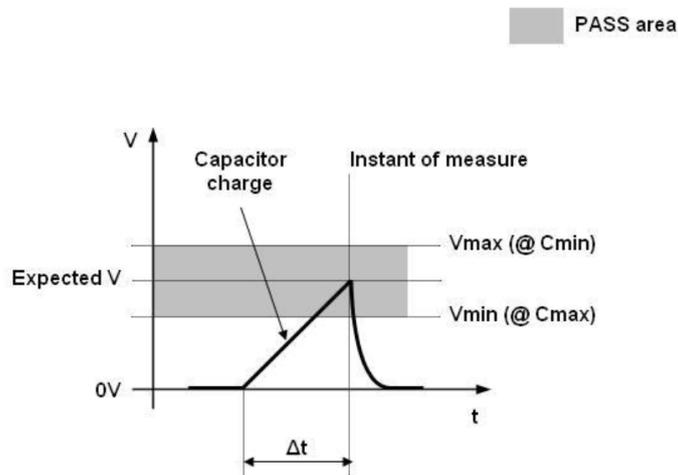


Figure 3.8: Capacitor behaviour

Time Interval measurement test

Generally, this measurement method is applied for medium-low capacitance. A known current is forced through the capacitor under test, and a counter, connected through the DVM as timer, measure the time elapsed between two threshold voltage, following $T = C_x \cdot \frac{(V_2 - V_1)}{I}$. The lower and higher threshold determine respectively the start and stop counting.

AC current measurement

Relative low capacitor values, require before starting the measure, to store the parasite capacitance of the system resulting from channels and instrument of the latter. To reduce the channel store capacitance, during the test program generation, for all the capacities of the order of hundreds of picofards and less, a dummy channel twisted to the measure one is added. The twisted wire is connected to the nearest

odd or even measure channel. This method uses an AC generator, figure 3.9, which forces two sinusoidal signals at different fixed frequencies on the capacitor under test. The *Z Meter*, used as ammeter, measure the current flowing through the capacitor and the *Measure* is used as peak to peak voltmeter to lead for each frequency the evaluation of the impedance.

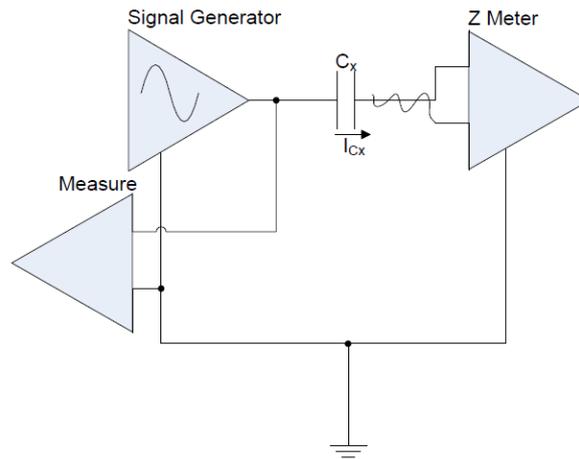


Figure 3.9: Impedance measurement test

3.2.7 Transistor test debug

Bipolar transistor test models that can be carried out are the following:

- I_{CE0} measurement.
- V_{CEsat} measurement.

In the first case the transistor as it can be seen from the figure 3.10 on the next page, is in *interdiction* mode, so it means that we measure the dispersion of collector-emitter when the $V_{BE} = 0V$, so the transistor is *OFF*. To achieve such condition, a short circuit is made between the base and the emitter(collector) of an *NPN*, (*PNP*) transistor. A generator forces a low current between the collector and the emitter, allowing to measure a voltage drop high enough as the transistor behaves as an open circuit, where of course the measured current $I \rightarrow 0$.

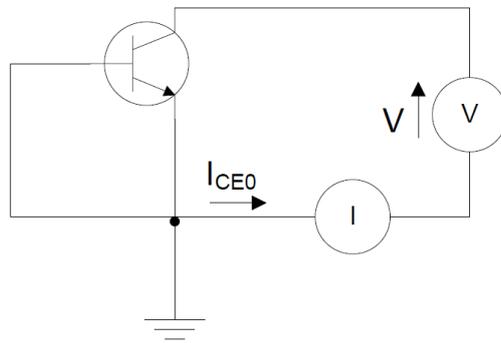


Figure 3.10: Interdiction mode - NPN transistor

In the second case the transistor is in *saturation*, meaning that the base is polarized forced the necessary current. Indeed, figure 3.11, shows a second current forced between the collector and the emitter, to create a voltage drop which is as low as the transistor behaves as an ideal short circuit.

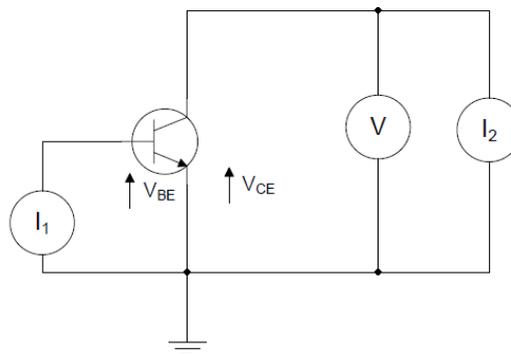


Figure 3.11: Saturation mode - NPN transistor

3.2.8 MOSFET test debug

Test to verify the correct functioning of a MOSFET are the measure of the I_{ON} and the I_{OFF} current. Obviously, first the verification of the protection diode between drain and source is conducted. This is accomplished forcing a known current and measuring the voltage drop on the underlined pins. Analogue procedure, as seen during the transistor's test, are carried out for MOSFET. Evaluating the I_{off} current means MOSFET in OFF condition, and so an open-circuit between Drain and Source is verified. On the other hand when the MOSFET is into conduction,

the gate is polarized and a current is supplied to the drain-source, where a voltage drop is measured. The Ohm's law, let us to evaluate the resistance between the drain and source for the test validation R_{DSon} .

3.3 Power On test

Power on in-circuit test, is the part of the generated program needed to test digital and analog integrated circuits. As evidenced, in this phase the necessary power is supplied to the UUT. In order to ensure the correct function of the operation, firstly, as reported in figure 3.2 on page 36, *sink* test are performed. Each supply net on the board, starting from the net at 3.3V and moving at the end to the net at 24V, they are tested by forcing a suitable voltage as indicated in the schematic, and verifying the correct current absorption. This operation is traced before the power on test to avoid the presence of any masked shorts that could lead to the breaking of the device under test. This section will show the solution adopted to test an integrated circuit. Starting from the assumption that the client had not provided any provision on the test to be performed, I started after the identification of the component in the circuit diagram, to study its data-sheet.

3.3.1 Power module test

Circuit analysis, as mentioned above, turned out that the device is a *smart power module FSB50550AB*. Analyzing the related datasheet, *FSB50550AB* is a tiny smart power module based on FRFET¹ [8] technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET, and 3 half-bridge HVICs for FRFET gate driving, as it can be seen from figure 3.12 on the following page.[9]

¹FRFET, fast-recovery MOSFET is designed to provide a very fast recovery (turn-off) of the body diode, making it convenient for driving inductive loads such as electric motors

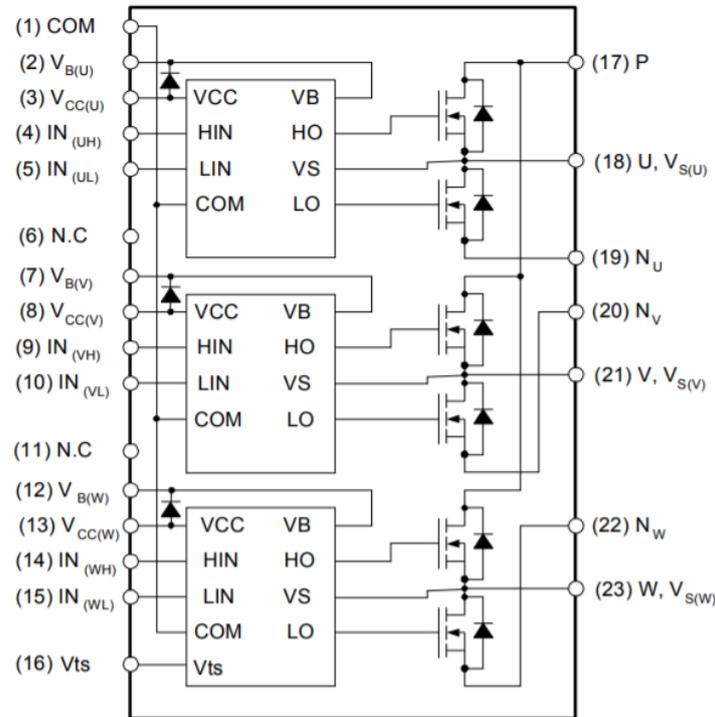


Figure 3.12: Power module - Internal block diagram

During the in-circuit test of the power module, to test its correct behaviour I start to check if the right MOSFET-drivers parameter were comparable with those shown in the datasheet. The best to use for such a measurement are the voltage across the MOSFETs and the resistance in the on state, R_{DSon} . To measure such resistance, the driving unit has to be supplied with voltage, the control input of the FET must be connected to high-level and a current source has to be connected to the Drain-Pin of the FET, phases explained in the previous section *Mosfet test debug*.

Looking at the figure 3.13 on the next page, it is possible understand how the following step are applied:

- Step 1 - Connection of the supply voltage VCC_U for the driving unit at $+13.5V$ (test point P72) and GND;
- Step 2 - Activation of the low-side MOSFETs of the phase U by connecting a voltage of 3,3V at P249 and GND. This operation correspond to a μC output abilitation;

- Step 3 - Flowing of current through the MOSFETs imposed at 200mA by using a current source between P241 and P236;
- Test Step 4 - Measure the voltage over the FET between P241 and P236.

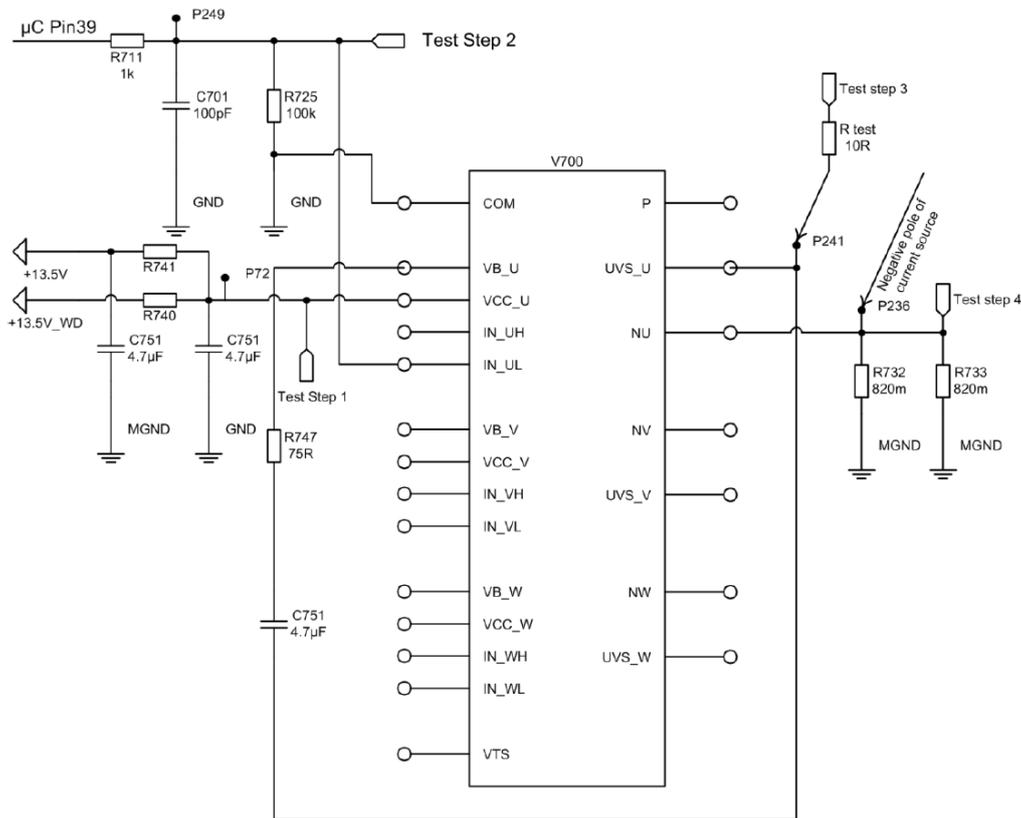


Figure 3.13: Power module - Test circuit proposal

The voltage drop measured over the FET, reflects the expected typical values reported in the datasheet. Following the power module pin configuration this type of test is executed for all the other FRFET, as experienced for the first one.

3.4 Application check

In this phase the tools and software are described to verify the reliability and the coverage of the test program, which has been previously generated and debugged. As explained at the beginning of this chapter, the *coverage analysis* helps to understand which are the task generated automatically from the software, and which need to be added for a correct debug of component of the UUT. When the debug

is performed, its common to re-edit the *coverage* file analysis because essential to check the coverage of the test program; in fact it enables to verify the absence of various types of “not coverade elements” such as, for example, untested components. This document is important because contains all the details about each test conducted and which tests are omitted, the net list contacted and not accessible. Moreover contains the time elapsed for each board test, important parameter to take into account during an *in-line production*. Before pack and deliver the application to the customer, the stability and repeatability are verified as it is shown in the final part of the project on page 70.

Chapter 4

On Board Programming

On Board Programming (OBP) is a technique to program on-board assembled electronic devices based on different technologies or programming systems by using different protocols and interfaces.

SPEA bed of nail system is provided by the *On Board Programming module* suitable to flash the content of components directly on the board to be tested. Through special commands, the test system supplies voltages, control signals, addresses and data in order to reset and program the device. Programming can be achieved both on a single component or in parallel on several components. It can be performed by using specific connectors or the traditional spring contacts inside the fixture.

The OBP hardware is made of the CPU module which communicates with the I/O channels by means of the Vme bus and the operating system. On the other hand, OBP channels are equipped with drivers and digital sensors whose voltage level are programmable and configurable. Components programming is performed through OBP software drivers which contain protocol, timing and instructions. In fact the OBP module is programmable by a dedicated test plan that contains instructions written by using the syntax of the most common programming languages.

4.1 Programming the STM32F301

In the following application, the programming steps for the OBP are performed in parallel on a panel of four boards under test equipped with the STM32F301 .

The STM32F301 are mixed-signal microcontrollers with an Arm Cortex-M4 core and made of a 64 Kbytes of embedded Flash memory for storing programs and data [18].

Before proceeding with the realization of the OBP, various precautions were

followed both during the first phases of the realization of the fixture project and in the choice of using dedicated machine channels. For the latter, in fact, the use of an electronic unit, called DBDIO, integrated on a main channels unit system board, allows the use of 64 analogue/digital channels, 8 of which can transfer a clock signal.

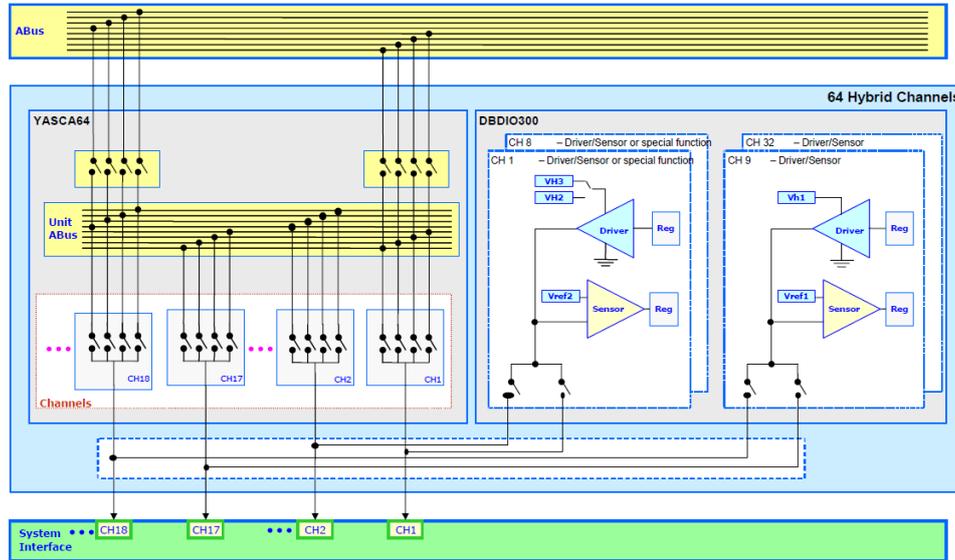


Figure 4.1: OBP channel board

In the diagram each channel can be configured as input or/and output. The first 8 channels can be programmed from 0.5V to 14V both in input and in output, furthermore they can supply a digital pattern of three levels.

Making an OBP means facing problems due to electromagnetic interference and therefore to capacitive and inductive coupling that the signals can undergo. To prevent data corruption from causing a failure during programming, the following specifications have been adopted:

- *Use of twisted cables to reduce noise;*
- *Use in fixture of long-stroke nails.* In this case, the OBP is realized by directly connecting the digital channels present in the system to the test points relating to the clock, reset and flash pins of the microcontroller through the user interface. To try to limit electromagnetic couplings, after performing the circuit test, the adapter goes to middle position. In this way, only the long-stroke nails to which the digital channels are connected are still in contact with the device, while all the others are floating.

As shown at page *STM32F301 On Board Programming* reported in the diagram of the appendix A, the boards can be programmed in parallel, with 4 system cores available. Taking as an example figure 1 - bay 1, the digital channels have been connected to the test points through the use of twisted cables and moreover to get the best performance, the wiring is performed when all the non-obp connections are terminated so as to avoid crossing other device wiring. The clock signal through channel *CH 1345* is connected to the *TP 595* of the microcontroller corresponding to the *SWCLK* pin. The reset signal is supplied through the digital channel *CH 1347* to *TP 134*. In the same way, the association of channel *CH 1346* with *TP 594*(*SWDIO*), allowed through a pullup resistor and the closing and opening of a *UFL3* relay to be able to send the data to be written into the flash memory. Obviously the procedure that allows the execution of the OBP has been implemented through the use of the visual basic programming language. In this chapter the test plan is reported, corresponding to the high-level programming part for a clearer understanding.

In the reported test plan after the read of the *OBPsetting.ini* file, the micro-processor should result programmed. To check that the programming has been completed, the OBP status is analyzed. Three cases are possible:

- **ENABLED** : the *On Board Programming* is successful and the following print log appear on Leonardo software : Get settings from ini file -> OBP ENABLE";
- **DISABLED** : the *On Board Programming* is not successful and the following print log appear on Leonardo software : Get settings from ini file -> OBP DISENABLE";
- **NOT ENABLED AND NOT DISABLE** : When the OBP status is not in one of the conditions stated before, it is forced DISABLED.

```
1
2 TESTPLAN_FUNCTION UserTplan ()
3 {
4     long FailFlag = FAIL;
5     WORD aUsedChList [65];
6     long rSiteResult;
7
```

```
8  ObpProgrammingSelect(OBP500A, "V600");
9  ObpSiteSet(OBP500A, "1");
10 ObpModelOptionsSet(OBP500A, "DEVICE=STM32F301xC;COMMFREQ=10M")
    ;
11
12 S2A("1345,1346,1347", aUsedChList, 64);
13 ObpChLevelSet(OBP500A, aUsedChList, 3.3, 0.0);
14 ObpChSensorSet(OBP500A, aUsedChList, 1.5);
15 ObpChConnect(OBP500A, aUsedChList);
16
17 ObpInterfaceEnable(OBP500A);
18
19 // Board Power On
20
21 ObpChipErase(OBP500A, TYP_WORD);
22 ObpWriteFile(OBP500A, TYP_WORD, 1, 0, 0, ALLFILE, NOSKIP);
23 ObpVerifyFile(OBP500A, TYP_WORD, 1, 0, 0, ALLFILE);
24
25 // Board Power Off
26
27 ObpChDisconnect(OBP500A, aUsedChList);
28
29 if (ObpGetSiteResult(OBP500A, 1, &rSiteResult) == 0)
30     if (rSiteResult == PASS)
31         FailFlag = PASS;
32
33 TplanResultSet(FailFlag);
34
35 return (1);
36 }
```

Chapter 5

Functional Test

The Board Functional Test (FCT), normally measures and verifies the electrical characteristics of the board, according to what is described in the electrical specifications of the board. These electrical specifications are normally provided by the board designer and revised in order to be applied on SPEA test system. In order to help the programmer in this job, SPEA has developed Leonardo F which enables to control the system instrumentation with Windows based languages. The instruments programming is performed through a set of instructions and use it to edit the source and compile the executable Functional Test plan. Leonardo has for each programming language a profile ready to program the system. This means that the programmer needs only to write the instructions to program the system. Actually Leonardo F is available for the most common languages (Builder C++, Visual Basic, DELPHI).

It is suggested to use this programming mode to write Functional Tests for the following reason: the program has all the instruments functions at its disposal. An high-level language is used in order to interact with the system and possible external instruments (serial ports, multimeters, oscilloscopes). Before executing each instruction, the software checks that the instruments programming sequences are respected filtering possible programming errors.

5.1 Test sequence FCT

An accurate definition of the test sequence must take place in co-operation with costumer, which define an adequate test sequence. When some parameters, or test sequence behaviour are changed, the customer must be informed about the differences. During final inspection, the UUT is primarily tested for specific appliance

functionalities. This is the reason why functions already tested before, are tested once again. Since it is possible that boards by mistake reach the final inspection even without ICT test, the voltages must be applied in stages for safety reasons and the current must be measured during each stage. This is the reason why after the ICT test, the *On Board Programming* is performed, in fact it is important to keep track of the operations performed on the board. Writing the correct information on the Flash memory, is vital to know the history of the board. Furthermore, thinking of a production chain, another way of identification is not only the writing of information inside the microcontrollers, but also the presence of a QRcode physically glued on the device which allows in the next step a PASS or FAIL identification of the UUT. Figure 5.1 on the following page, shows the steps to take into account to avoid error during Functional Test. The purpose of FCT is to ensure the function of the electronics circuit specified by the customer testing moreover components which could not be tested in the ICT power on. In this case, the power on test, as explained in 3, has to not be confused with the Functional Test. The first one, was limited by the max supply voltage of the board. In a Functional Test, the difference lie in the fact that we simulate real load, with the relative power supply and power deriving from each task. Writing of the final test status and device-specific identification data during the execution, since we deal with voltages and currents that could damage not only the device under test but even the system itself, no error are permitted. So *execution* of an FCT means something that goes beyond the test itself. The following steps are clarifying:

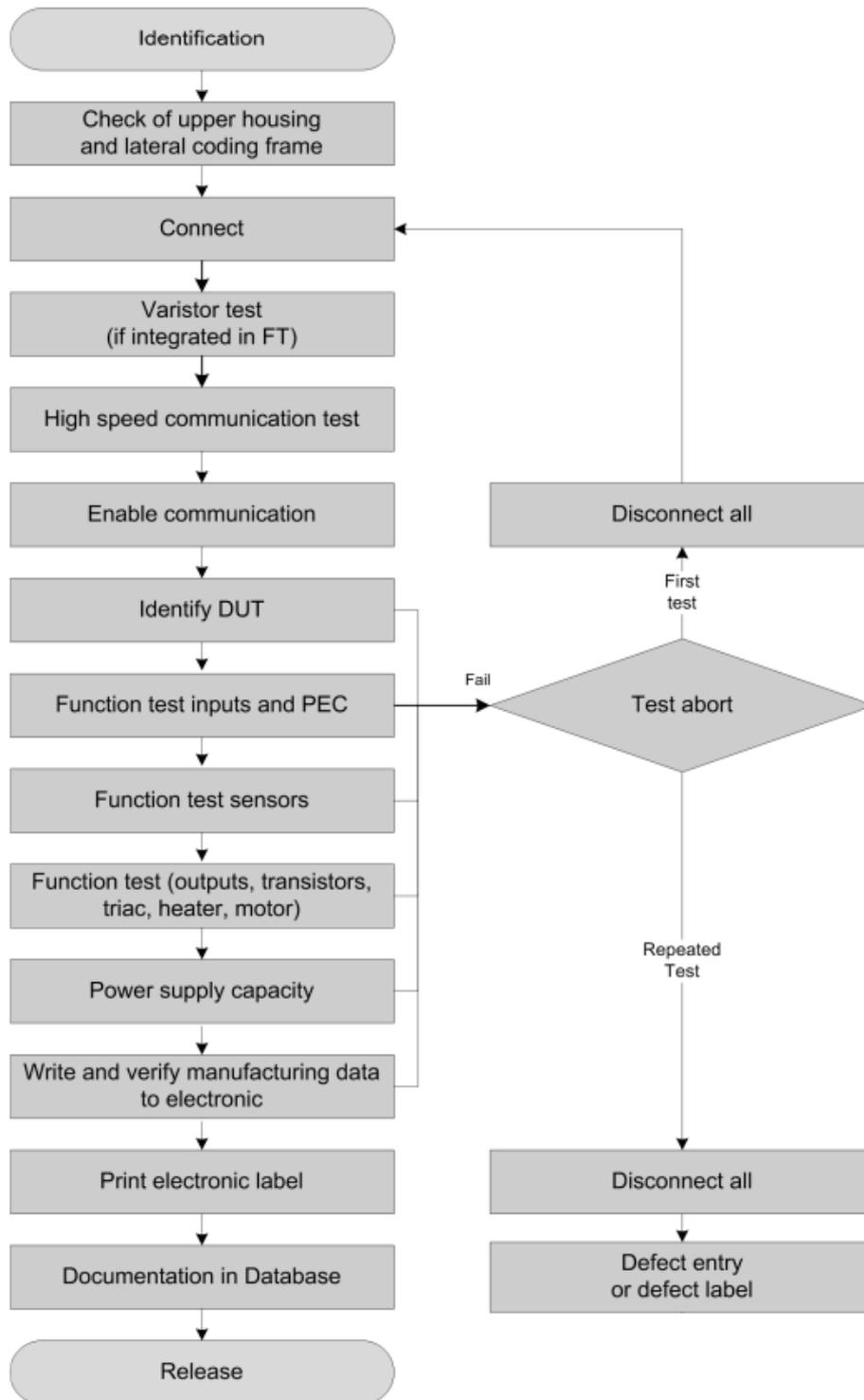


Figure 5.1: Functional Test Flow chart

Execution:

- Identification: measure must be taken to ensure that only the boards with *ICT_GOOD* will be tested in the final inspection. Identification code is present the Flash memory, and as it happen in this case, since the UUT presents an housing, it has a coding frame regarding the previous test history, as explained before;
- Connection : outputs are activated and the inputs are read via the serial interface. The assignment of the variables to the functions and the bit pattern within the variables are supplied by PED connector, since are the only point which can be contacted due to the housing;
- Functional test operation : during Functional Test, when an error is detected, the test is aborted, all the system instrument are disconnected and test is repeated; If the repeated test is passed with "good", the board is to be considered as good but if the repeated test is not successfully passed, the device under test is passed on to the analysis station with a "defect label". The test counter eliminates permanently reject boards.
- Write and verify all manufacturing data to electronic : FCT test data are to be registered in Flash memory, as done previously for the ICT. All the data relating to the individual tests are stored in a file created automatically by the system that keeps track of the individual operations carried out, and therefore of the values provided by the instruments in each test. The results can then be consulted, as a backup copy is made locally. Indeed on a production chain, since hundreds of devices are tested every hour, a tracking mechanism helps the operator to see which are the UUT *PASS* or *FAIL* and in the latter the tracking software has the ability to show failures to which components are due.
- If the DC link capacitor is not discharged by the switched-mode power supply unit, there is a risk of fatal injury when the enclosure is open. The capacitor must be discharged at the end of final inspection via the test points and a discharging resistor. (If none of the two voltages (13.5V, 3.3V) can be measured).
- When FCT is *PASSING* parts are provided with a sticker (or label content printed on the housing) and packed for the delivery.

5.2 Varistor test

The execution of the Functional Test regarded the test of a varistor, present in the power supply module.

A varistor is an electronic component with an electrical resistance that varies with the applied voltage. [10] The varistors, also known as "non-linear resistances" or voltage-dependent resistor (VDR), are composed of silicon carbide and zinc oxide. Varistors are used as control or compensation elements in circuits either to provide optimal operating conditions or to protect against excessive transient voltages. When used as protection devices, they shunt the current created by the excessive voltage away from sensitive components when triggered.[11] Below a certain voltage, the current is low because the resistance is high. When the voltage increases, the resistance decreases or the current increases with exponential law. For these reason, this type of element are inserted after a fuse device and generally is used in parallel to a mechanical contact and to the supply voltage promptly to avoid that any downstream inductive load (a DC motor, a coil of a contact) pours a over-voltage on the contact itself such as to generate an electric arc and / or in any case such as to exceed the maximum voltage contact specifications. The varistor under test is shown in figure 5.2.

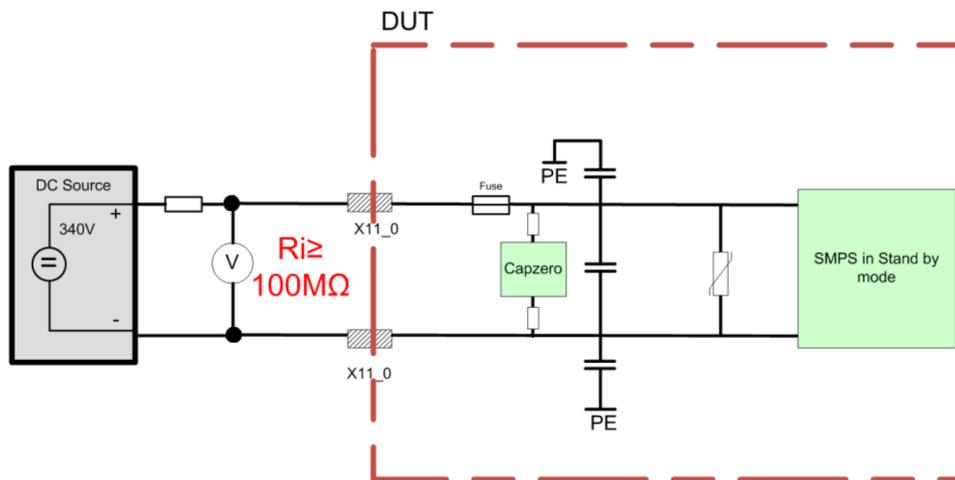


Figure 5.2: Test station for discharge and residual voltage measurement

Possible test procedure and specification provided by the customer: A test DC voltage of VDC <+630V with current limitation is applied to the varistor.

- Connect + to N and connect – to L;
- Start at a voltage of 200V;
- Increase the voltage until the current exceeds 1mA through VDR plus self consumption of electronic
- Time between exceeding the test current of 1mA and switch off the voltage is maximum of 1s.
- The measured voltage must be between 400 – 561V

The power module has parallel resistors and capacitors to the varistor. Due to this fact it's important to minimize the test time and be sure that there is no damage on the resistor.

Analyzing the available specifications, and the fact that the 3030 system is not able to generate such high voltages, it was decided to design a circuit with a voltage converter capable of providing a reverse voltage and a sufficiently high power when one rises with tension. The choice of DC/DC fell on the UltraVolt D Series of microsize high-voltage power supplies 1D-15-N6. The D Series microsize units deliver 0 to 1kV in a 6W miniature package. The input voltages available is 15 ± 1.5 VDC. From figure 5.3[12], is to possible to see a connection overview of pin and leads of DC/DC converter.

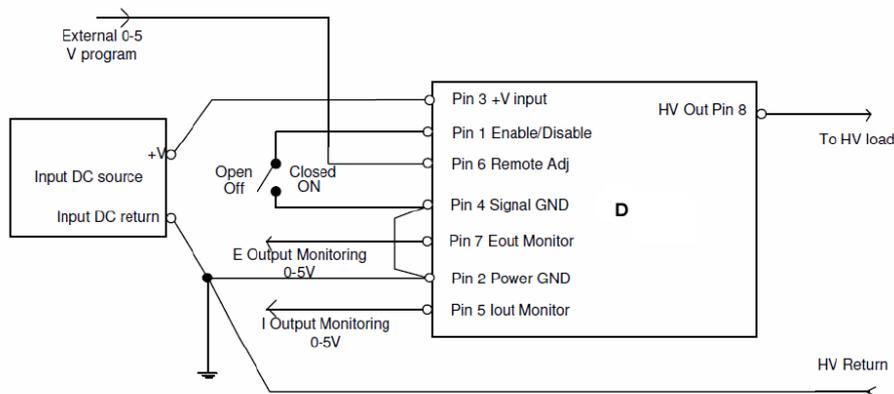


Figure 5.3: DC/DC functional diagram

Before proceeding with the design of a conditioning circuit, useful to carry out the appropriate requests, I report the function of the individual pins of the ultravolt

high power supply, as it is on them that the aforementioned circuit project that I will explain later was born.

- Pin 1, Enable / Disable: This pin is used to inhibit the output voltage using a logic signal. A short or zero logic will turn the unit ON. When pin 1 is left open or at logic High the output will turn OFF. If this function is not used, Pin 1 should be connected to Pin 4 otherwise no output voltage will be available;
- Pin 2, Input Power Ground Return: This pin is the return to the input DC source. The connection to this pin is also used in the system as the HV return;
- Pin 3, Positive power input;
- Pin 4, Signal Ground Return: This pin is used as the return for the voltage control signal, voltage monitor signal, and current monitor signal. It is provided as a separate ground for low-power signals in order to avoid any interference with the HV Return and Input DC Return. Do not use this pin as a direct connection to the HV Return;
- Pin 5, Output Current (I_{out}) monitor: The analog buffered output signal, 0-5V, is proportional with the output current draw (Pin 5 output impedance = $1k\Omega$). The signal goes from zero to five volts for output currents from zero to maximum. Accuracy of the signal is $\pm 0.2\%$.
- Pin 6, Control Input (Remote Adjust): This pin allows the control of the high-voltage output by a low-voltage signal. Using a 0 to 5V $\pm 0.1\%$ positive DC voltage. Pin 6 input impedance is $94k\Omega$. This signal is clamped to 5.3V for protection against overdrive. When zero volts is provided, no output voltage will be present;
- Pin 7, Output Voltage Monitor: This pin provides a low-voltage 0 to 5V signal proportional with the HV output voltage. The accuracy of the voltage monitor is $\pm 0.2\%$.
- Pin 8, High Voltage Output: This is the high-voltage output up to 6kV. The pin is located farther away from the other seven pins in order to provide the proper clearance for the high-voltage circuit. When designing a system PC board, adequate creepage and clearance spacing must be observed.

For the circuit design, it was decided to use *molex connectors*; 14 and 10 pins respectively to manage the control and input signals and a 16 pins connector for the outputs. For the latter, a greater number of pins are used in order to be able to correctly outrange the 4 high voltage outputs (HV +) between them and so increase the isolation factor already employed by the connector itself. In figure 5.14 on page 82, it is possible to see how the DC/DC board is projected to be supplied with 15 V but also with higher voltages. In particular, two voltage regulators are used. The first regulator, TPSM84212EAB¹, is able to regulate the input voltage from 15 V, also used for the power supply of the DC/DC itself, and bring it to 12 V necessary for supplying the relays present at the output, eliminating loop compensation simply adding input and output capacitors. The second regulator, R-7815-0.5 ², is designed to regulate higher in-game voltages. In fact it converts input voltages from 18-34 V to 15V, and therefore usable as can be seen from schematic both as power supply for the DC/DC and for the relays once converted as explained above. It was decided to adopt a security measure, to proceed with enabling the DC/DC, using the pins on connector J3:

- *Safety_Chain+*
- *Safety_Chain-*

The *Safety Chain*, is present in any system. On this chain, are connected all the signals that allow the operator to understand that it is possible to act in total safety. When one of the signals, which is closed to ground through the safety chain, is not present, it is not possible to proceed with any normal operation of the system. Connecting *Safety_Chain+* and *Safety_Chain-* at the respective points, and shorting *Ext_DC/DC_Enable+* and *Ext_DC/DC_Enable-* (additional security operation), it is possible through the use of 3 photocoupler TLP185³, to bring

¹The TPSM842xx power module is an easy-to-use integrated power solution that combines a 1.5-A DC/DC converter with power MOSFETs, an inductor, and passives into a 3-pin, through-hole package[13]

²RECOM Power InnoLine non-isolated R-78 Series DC/DC Converters offer efficiency up to 97%, eliminating the need for heatsinks[14]

³The TOSHIBA mini flat coupler TLP185 is a small outline coupler, suitable for surface mount assembly. TLP185 consists of a photo transistor optically coupled to an infrared emitting diode [15]

pin *DC/DC_Enable* to ground, and then to enable the high voltage converter, as explained in pin component description.

In figure 5.15 on page 83, the drawing shows how the DC/DC output and HV return signal are splitted up into outputs connector thanks to the use of 8 Pickering 119-1-A-12 high voltage Micro-SIL relays⁴. This type of relay present a maximum switching voltage of 1000V and a maximum stand-off voltage of 3000V, and therefore perfectly sized to manage the considered output voltages. The coil is fed to a 12 V , and by connecting the other end (Enable output) to ground, it is possible to trigger the contact and then select the desired output. When it is not possible to enable the relays directly to ground, it is thought to study a high logic level enabling. Looking on the right of figure 5.15, in fact, we note the use of 4 dual N-channel MOSFET SI1902DL-T1[17], used as switches. When the signal on the gate is set to a high logic value, and therefore connected through the connector on the system bus, the drain is brought to the same logic level as the source. The latter, is connected to the *HV return* signal allowing to enable the selected relay with a low logic level. Obviously the output voltage is read taking into consideration *HVout1_return* and *HVout1*, and so respectively for the other 3 deliverable voltages. In the last drawing page, figure 5.16 on page 84, it is shown the discharge part of the DC/DC conditioning circuit. In short, enabling the signal of discharge, *Discharge_Disable.0*, thus placing it at the logical zero, it is possible to enable the MOSFET *Q4*. This is therefore able to activate the relay, which by closing its contact, allows the discharge of the high voltage, appropriately partitioned using resistors through ground. This type of operation is carried out not only to discharge any charged capacities on the line, but also in the event of an emergency, to prevent high voltages return upstream to the DC/DC, affecting its functionality.

After the drafting of the analyzed electrical diagram, we proceeded to the unraveling of the circuit and then to its physical realization. This operation is preceded by the study of the choice of component positioning through the use of specific software. Given the large number of components, the use of a two-level PCB has been chosen. The connections are made regarding the positioning of the enabling signals mainly on one face and those which involve supply and high voltages on the other one. This systematically adopted approach allows to obtain a PCB in

⁴The Pickering Series 119 is a new range of very small Single-in-Line Reed Relays intended for voltages very much higher than standard small SIL relays. [16]

which inductive and capacitive effects are the most contained possible. Component positioning and routing design are shown respectively in figure 5.4 and 5.5.

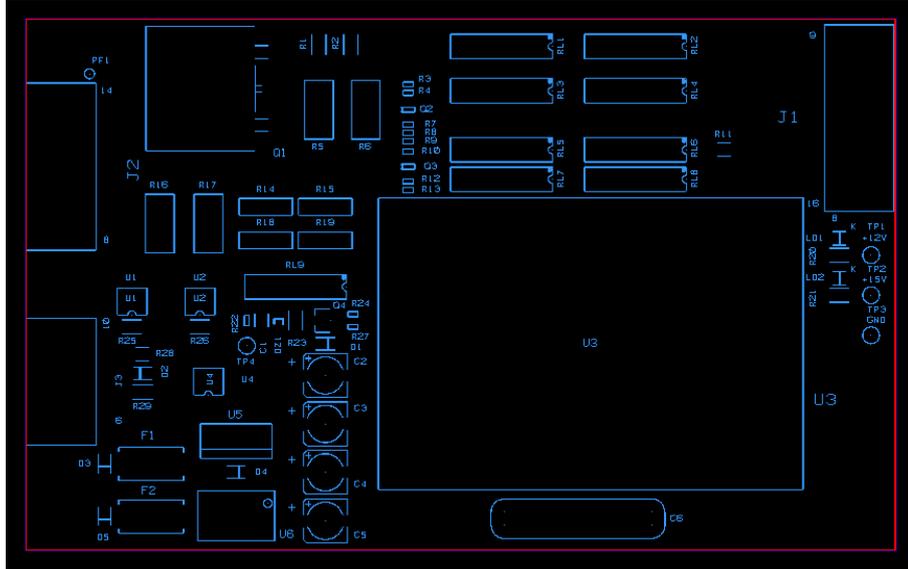


Figure 5.4: PCB - Component positioning

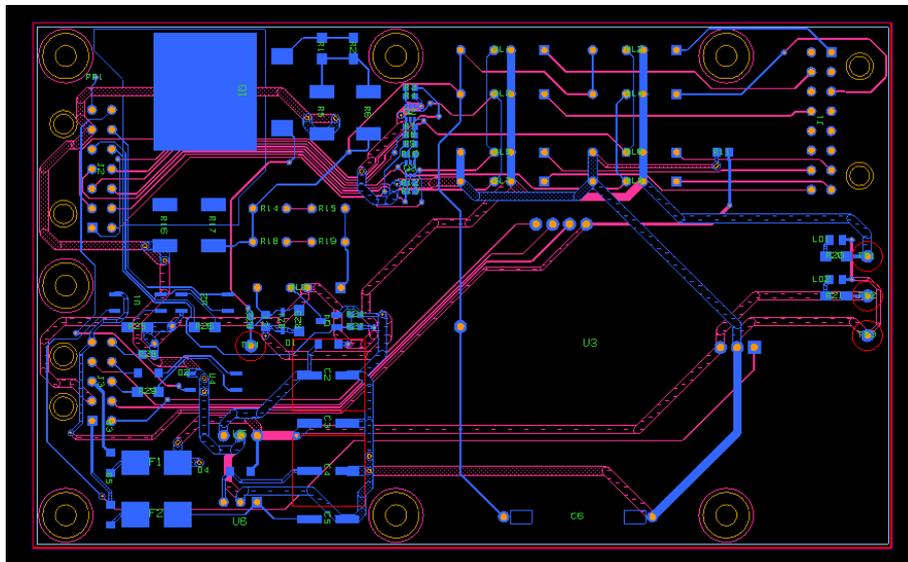


Figure 5.5: PCB - Routing design

The PCBA, finally is then integrated with the proper connection inside the fixture, and so through the system interface with the DUT. Through the use of

the *C#* programming language, it was possible to connect the system resources, following the specifications dictated by the customer, to the DUT. An example of a code used for the varistor test is shown below. From code we can see how after the various driver settings, useful for signal generation, and to DVM, used for reading them, we proceeded to generate a voltage ramp up to a current exceeding 1mA. This was also relying on a test time limit. During the first test, the output signal was monitored by analyzing it on an oscilloscope. This allowed to extrapolate and analyze the obtained data through MATLAB software. From figure 5.6 on the following page, it can be shown how the linear feature of the DC/DC reflects what was mentioned in the description given above for the control pin. A linear behaviour is shown between the V_{out} and V_{in} . The most awaited curve is the verification of the varistor operation, as can be seen from the figure 5.7 on the next page, as soon as the voltage exceeds 500 V, this is limited by a current increases as expected by the customer's specifications. In addition, a particular request from the customer was to identify the type of varistor present inside the device, as there are different variants of the proposed board, depending on the type of Control Power Module (CPM), to be used in different parts of the world, and based on the type of mounted varistor. In particular, looking at the graph shown in the figure 5.8 on page 66, the varistor present on the device under test has the same behavior as the curve CPM_III_R_EU with 320V-VDR.

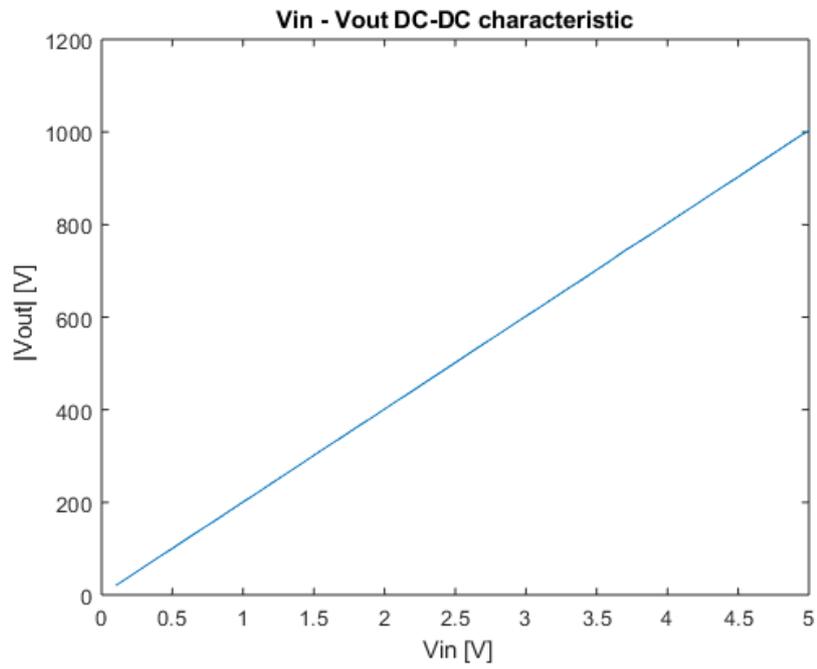


Figure 5.6: V_{in} - V_{out} DC/DC characteristic

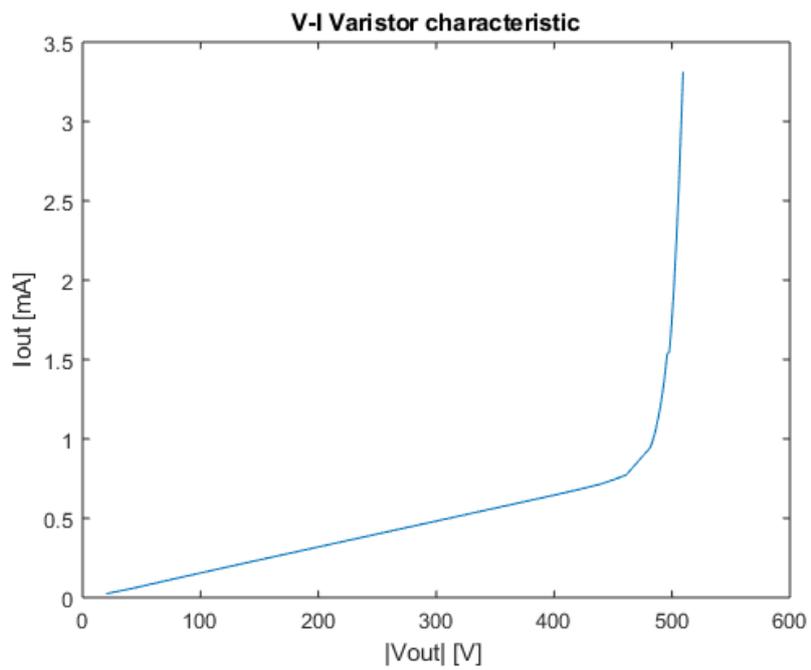


Figure 5.7: Varistor characteristic

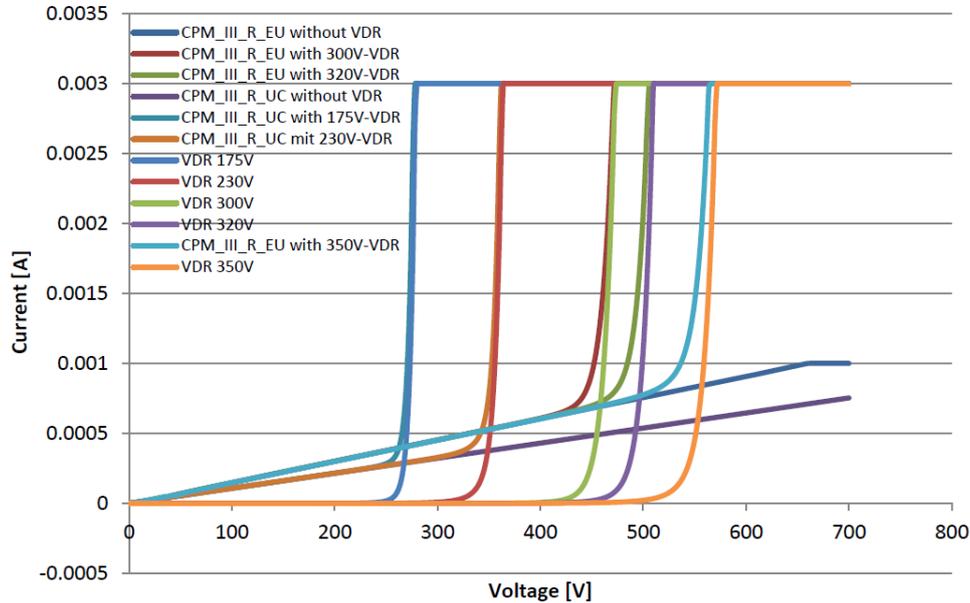


Figure 5.8: Comparison CPMs with and without VDRs, single VDRs

5.3 Capacitor discharge test

In this section it is possible to analyze the discharge behaviour of a capacitor present in the power module as shown in figure /vref 5.3 on page 59.

Requirements for the test system are listed below :

- DC source nominal AC voltage $\ast\sqrt{2},3A,1\%$;
- The test system must be designed for the inrush current of the DC- Link capacitor;
- The plug discharge test shall be performed using a voltage probe with an input impedance of $100 \pm 5M\Omega$ and a maximum input capacitance off $20 \pm 5pF$;
- Switch the voltage Control + on;
- Check the voltage before the disconnection $V= \text{nominal } AC\text{voltage} \ast \sqrt{2}$;
- Discharge the PCB;

- The residual voltage must be measured after 800ms and the voltage must be lower of <30V.

The following test is the continuation of what started with the varistor test. In fact, the use of DC/DC is essential. Following the aforementioned customer specifications, the code present in the codes section at appendix C is developed. In particular, following the code, it can be observed after the initialization of the driver and the DVM, as this last one is set to ensure 1000 number of samples, spaced by 1 ms for the discharge acquisition. After setting the DC/DC to a voltage of -340 V, the driver was switched off and consequently the power supply to the DC/DC itself observing the discharge curve of the capacitor. The values obtained from the test, were first acquired through the function : *FuncTest.OnceForBay()* \leq *DVM.DVM1.ReadAll(acquisitionNumber, out dischargingCurve, out_)*, and then analyzed through the use of MATLAB software. In particular, it can be seen from the figure 5.9, the discharge curve of the capacitor under observation. The customer specification to be respected requires that after a discharge time of 800 ms, the residual voltage must be less than 30V. As can be seen, the test for the DUT is exceeded since the voltage value at a Δt of 644 ms is already less than 30 V.

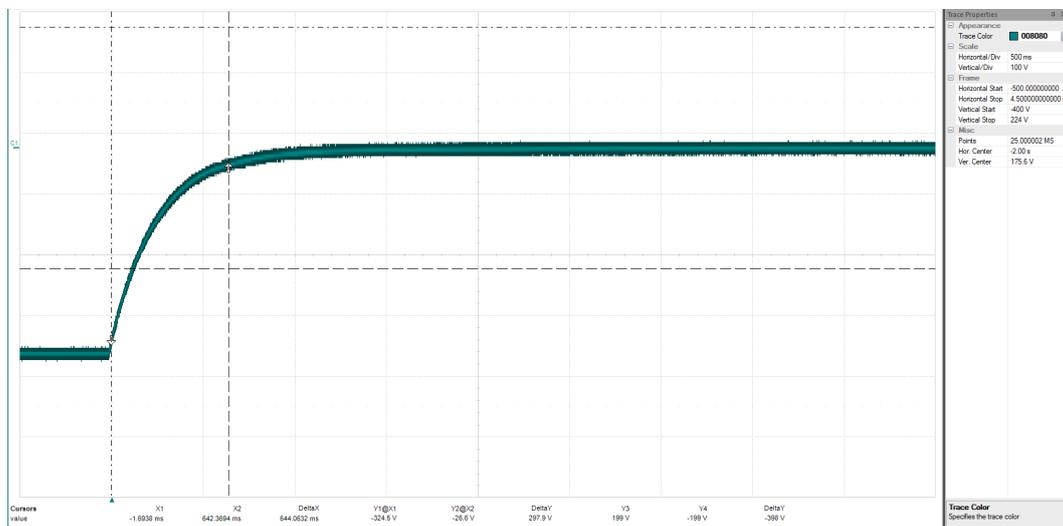


Figure 5.9: Discharge Capacitance

In figure 5.10 on the next page, looking at the curve in yellow it is possible to see the charge and consequently the discharge of the capacitor. Meanwhile, the pink curve represents the monitoring of the V_{out} , thought the use of *Vout monitoring*

pin of the DC/DC. In particular, when the DC/DC is enabled, the Vout monitor curve rising, and the capacitor starts to charge, whereas the Enable is disconnected, the Vout monitor signal falls to zero and the capacitor starts to discharge.

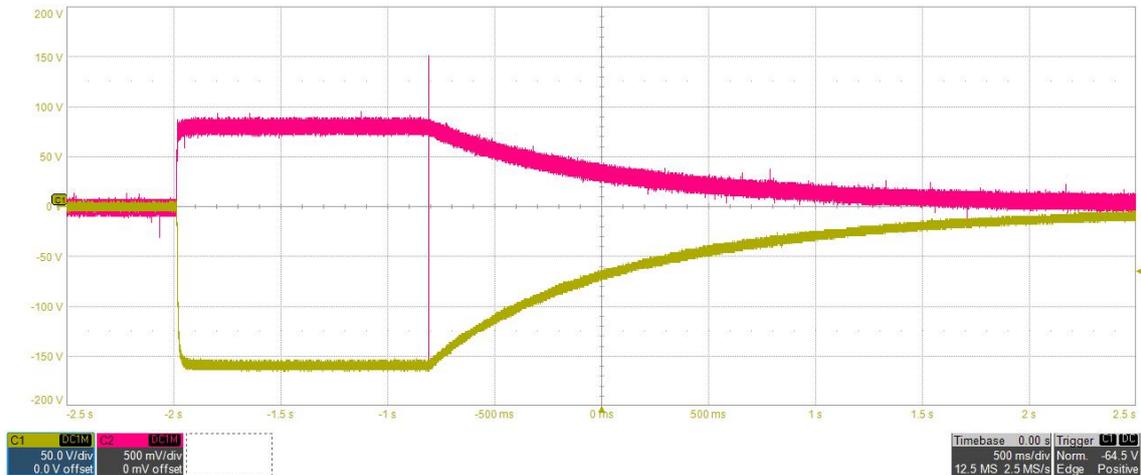


Figure 5.10: Vout monitoring and capacitance discharge

5.4 Code

When a new test program is created, it is possible to start from a preset modular format. The module from which the test program tracing is started is the *test plan* where the whole of the tasks are recalled (Main Program). The *test plan* routines are the highest level ones and they determine the tasks execution sequence.

ATOS F software is the test equipment operating system. It is employed to realize functional test programs, that means simulating the real electronic equipments operation. It enables to create and use the test programs. In Atos F libraries, all the instructions for system instruments programming are contained. In the appendix C are listed parts of the code developed for the Functional Test, and in particular that concerning the tests explained. In fact, in the test plan all the functional tasks carried out are reported, but only those of greater relevance, where the writing of the code was made possible only after having adopted particular circuit choices, see *varistor* and *discharge capacitor test*, are listed.

Results and conclusion

Development of the test program leads to the use of the Test Result Analyzer(TRA) for the analysis of the acquired measures. The performance of the application can be determined through the evaluation of the accuracy, stability and the distribution of the measures adjusting the test program according to the TRA reports.

At the end of the adjustment of the critical component, obviously where it is possible, the TRA is used for generating reports for test program certification. The progress of the application proceeds by testing the entire test program on a single panel of boards, called golden sample. After the development of a preliminary TRA, it is possible to adjust those components that present limit values and therefore can slow down a mass production chain showing unmotivated fail. The golden sample truly represent the starting point before any mass production.

TRA is used to monitor production efficiency and fault distribution, therefore after the analysis of the golden sample, the test result analysis was conducted on another 10 panel of boards. Compared to mass production, this number seems to be trifling, but it can still provide which component could return to fail.

The panel of board have been tested simulating an in-line chain, meaning that the 11 panel are stacked in a loader that is able to insert a panel on the line as soon as the previous one has been collected at the output.

Panel of board	UUT on panel	Test per Panel	UUT tested	PASS
11	4	1	44	44

Production summary

Production summary panel gives information in order to evaluate production efficiency. It displays statistic about the number of boards tested and the percentage of pass and fail results showing the yield of production.

The analysis also consists in the evaluation of the process capability indexes :

- C_p : statistical parameter that relates measurements dispersion with the threshold amplitude. The more the measured values are scattered, the more the C_p value reduces. Vice versa, a C_p great value means a little scattering of the measurements;

- C_{pk} : indicates how much the measurements are near the nominal value. The measurements are near the nominal value the more the C_{pk} equals C_p .

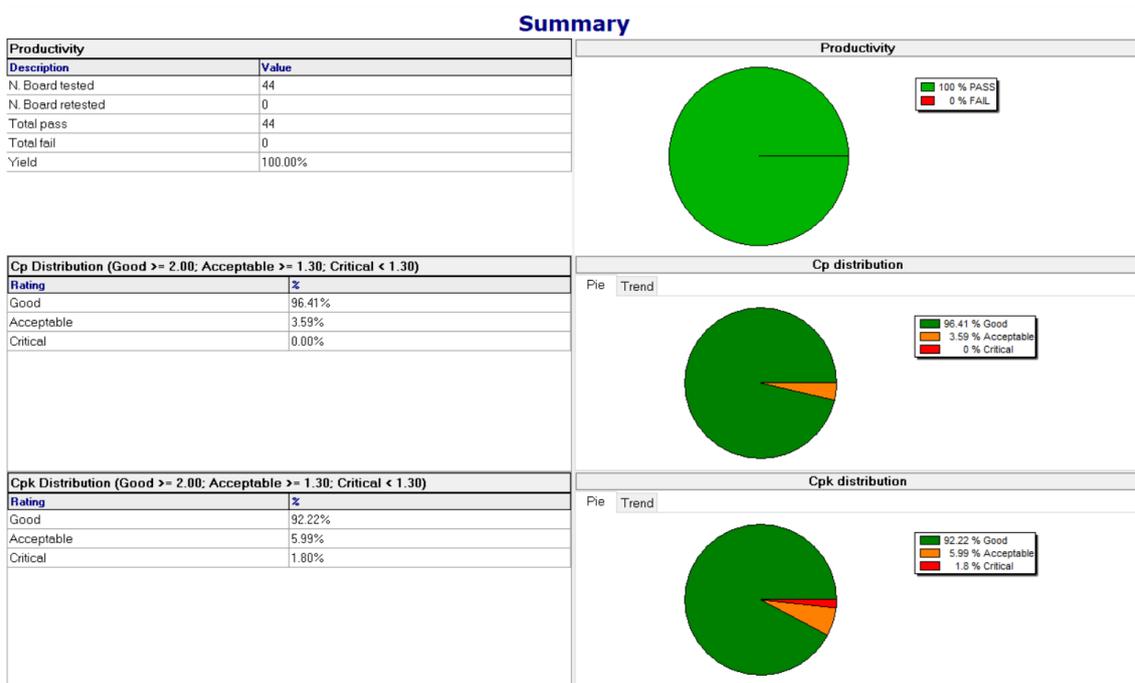


Figure 5.11: TRA - Production summary

In figure 5.11, it is reported the overall production summary analysis, and it can be seen the limit values of the capability indexes for which a component is classified as good, acceptable and critical.

Stability

Capability indexes are stability indicator of the test performed. In the worksheet panel displayed in figure 5.12, it can be seen how this instability is related to the capacitors tests. The resistor referred to the task number 142 and 131 show a low standard deviation and high capability values, instead the tasks of the capacitor reported present an high standard deviation and a low but acceptable value for C_p and C_{pk} indexes. Looking at the bottom of the figure, the frequency distribution plot is reporter for capacitor C705 of 100pF. On the chart is possible to identify the mean value vertical line, and $\pm 3\sigma$ vertical dashed lines.

Results and conclusion

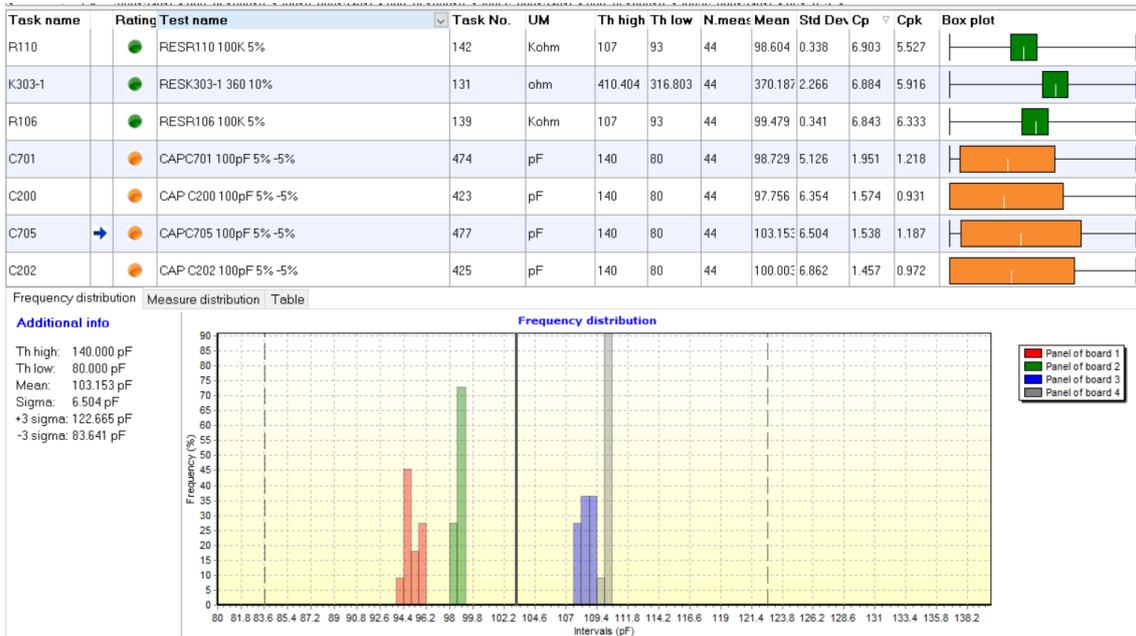


Figure 5.12: TRA - Low capacitor test frequency distribution

It can be noted how the values change relating to the UUT under test indicated in the plot with different colors. Tight and tall frequency distribution means that the measures have a good stability. Otherwise, a large distribution means a bad stability. The panel of board 1 and 2 show small capacitive values respect to the the panel of board 3 and 4. This depends on the fact that we are testing a capacity with a value of 100pF, therefore, we must consider electromagnetic interference that are generated during the measurement and at the different length of the cables inside the fixture. In fact for capacity with higher values, as shown in the example in figures 5.13 on the following page, the C107 1 μ F capacity has a much lower standard deviation than the 100pF one. In fact the disturbances for such high values are negligible.

Finally, when a desired TRA is achieved, the last step is to install the application in the customer's ATE system. Unfortunately there are tolerances that vary from system to system, so what needs to be done is to fix those critical tasks. In this case, given the stability of most of the components, only the tuning of the capacitor tests that result critical have to be done during the adapter installation. It is therefore important to draw up an analysis in which the C_{pk} values are the highest possible so as to have less issue during the configuration of the customer system.

Results and conclusion

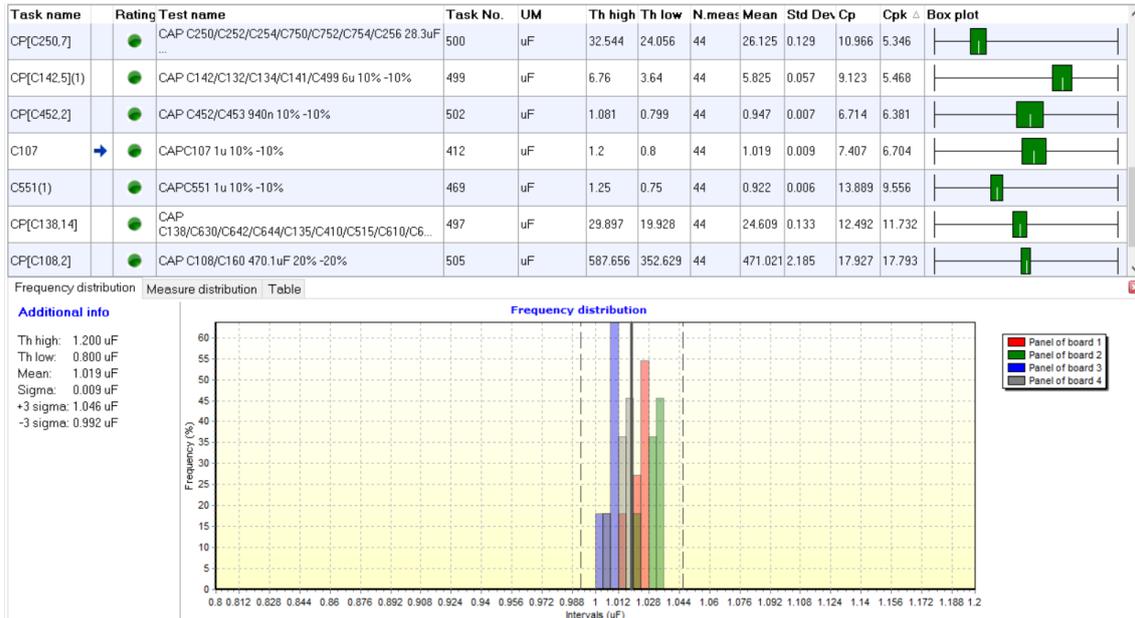


Figure 5.13: TRA - High capacitor test frequency distribution

Timing

The customer's last request is to respect the timing for the various tests conducted, an important parameter in the mass production market. The following table summarizes the values found for the tests carried out on a single panel of boards.

Type of test	UUT on panel	Time for single UUT	Total test time	Customer required time
ICT	4	59 s	59 s	-
OBP	4	31 s	31 s	-
FCT	4	78 s	78 s	-
Total Time	-	-	168 s	<180 s

Discharge Resistors

Figure 1 -> Bay 1 **Figure 2 -> Bay 4**

Figure 3 -> Bay 2 **Figure 4 -> Bay 3**

TABLE 1 - Discharge Resistors

Pol. Check Resistors

Figure 1 -> Bay 1 **Figure 2 -> Bay 4**

Figure 3 -> Bay 2 **Figure 4 -> Bay 3**

TABLE 1 - Discharge Resistors

Presser Plate

Fixture

	SHEET DESCRIPTION 02 - Automations	This drawing is the property of SPEA and is intended for the use of the client. It is not to be reproduced or distributed without permission from SPEA.	DRAWING TYPE ELECTRICAL DISCONNECT	DRWN Marco Marino	FILE NAME 02 - Automations	SPEA Automations Department E-mail: info@spea.com Web: www.spea.com
	DRWN Marco Marino	FILE NAME 02 - Automations	Documant name Fixture Wiring	Documant number 02 - Automations	Documant date 02 - Automations	Documant version 02 - Automations

GND Chain - Bay 1 + Bay 2

Figura 1 -> Bay 1

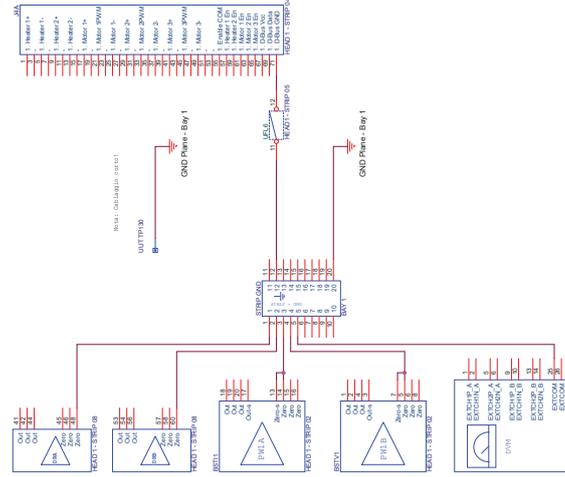
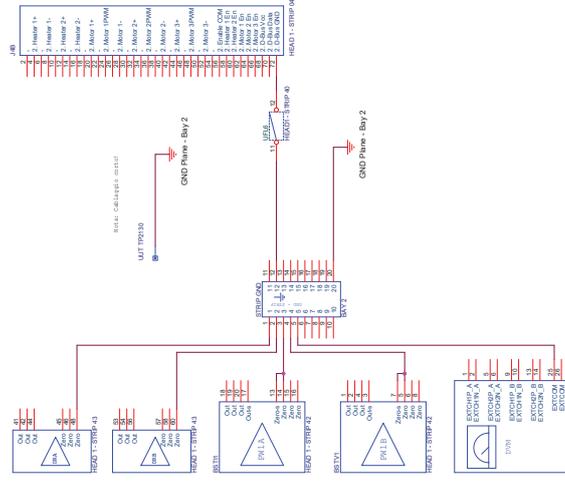


Figura 3 -> Bay 2



Tutti i cablaggi: AMG24 Nero

	SHEET DESCRIPTION 03 - GND Chain Bay 1 + 2	This drawing is the property of SPEA and is subject to the responsibility of the author. It is not to be reproduced or distributed without permission from SPEA.	DRAWING TYPE ELECTRICAL DISCONNECT	DRWIN Marco Marino	FILE NAME FUTURE WIRING	SPEA s.p.a. - Via Salaria 115 - 00198 Roma - Italy E-mail: info@spea.com - Web: www.spea.com
	DOCUMENT NUMBER 03	DRAWN BY Denis Bin	PAPER SIZE A3	DOCUMENT NUMBER 03	PAPER SIZE A3	TITLE FUTURE WIRING

GND Chain - Bay 3 + Bay 4

Figura 2 - Bay 4

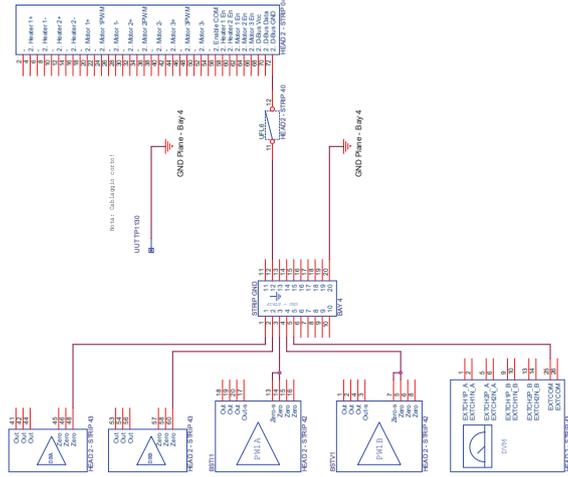
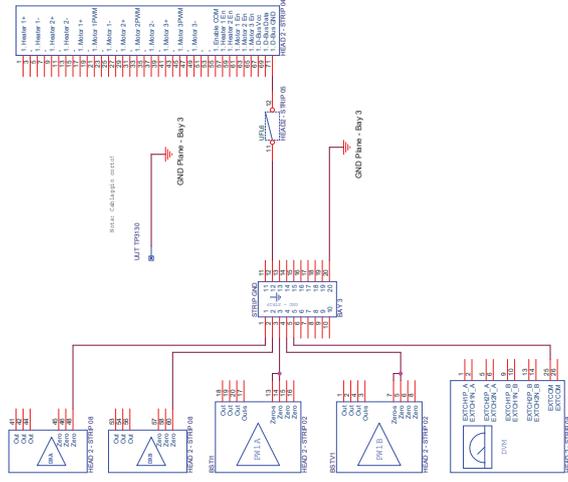


Figura 4 - Bay 3



Tutti i cablaggi: AMG24 Nero



SHEET DESCRIPTION
04 - GND Chain Bay 3 + 4

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DRAWING TYPE
ELECTRICAL
DISCONNECT

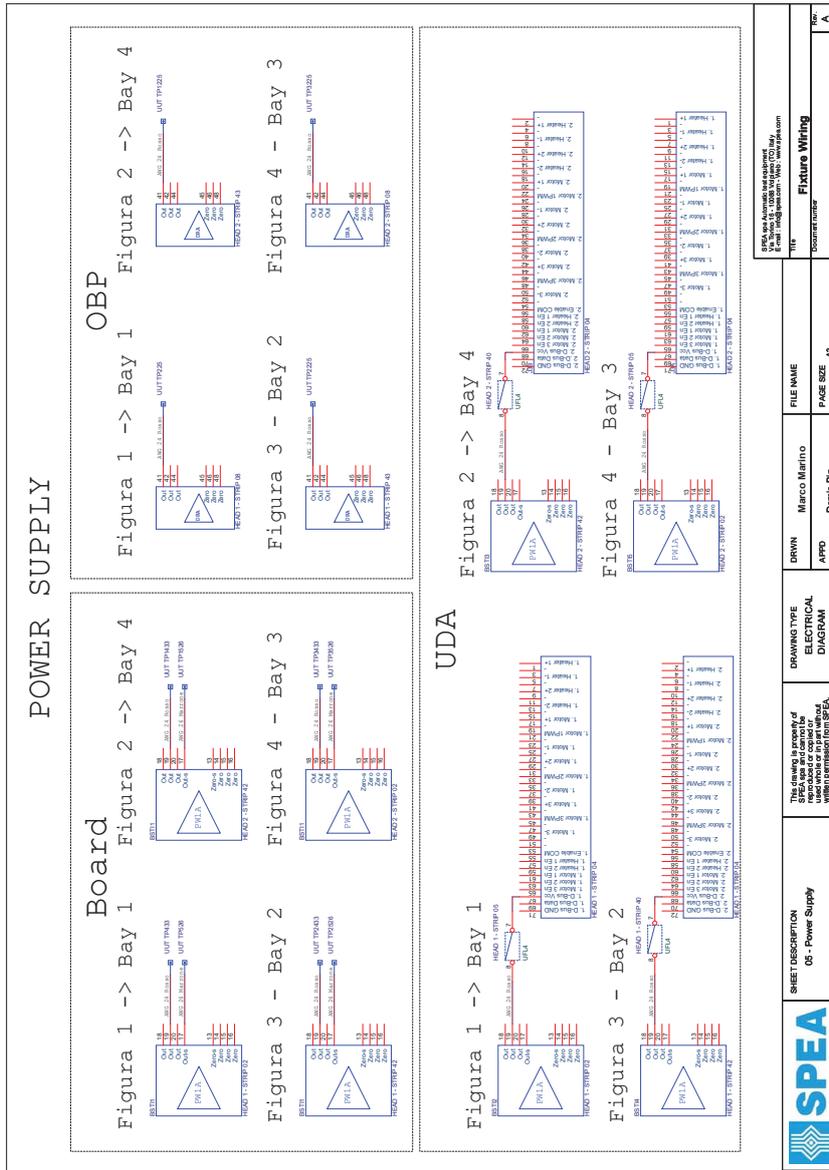
DRWIN Marco Marino
APPD Denis Bin

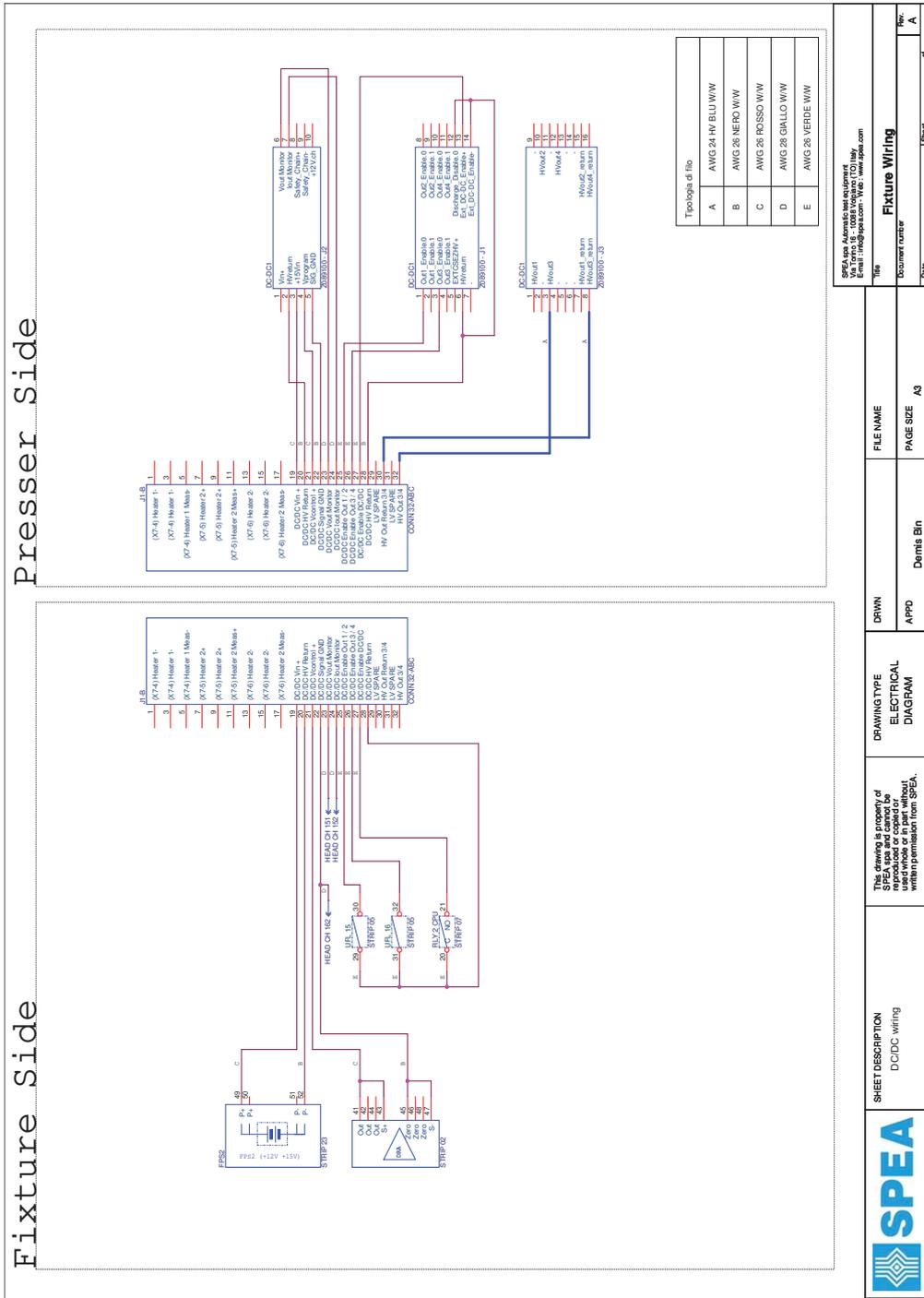
FILE NAME
FASE SIZE A3

SPESA Automobili Industriale S.p.A.
E-Post: info@spesa.com Web: www.spesa.com

Title Fixture Wiring
Document number
Scale 1:1

Rev. A





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SHEET DESCRIPTION		DRAWING TYPE		FILE NAME	
DC/DC wiring		ELECTRICAL DIAGRAM		DC/DC	
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		APPD		180007_33	
		Demis Bin		PAGE SIZE A3	
				REV	
				A	

Appendix B

HV DC/DC converter electrical scheme

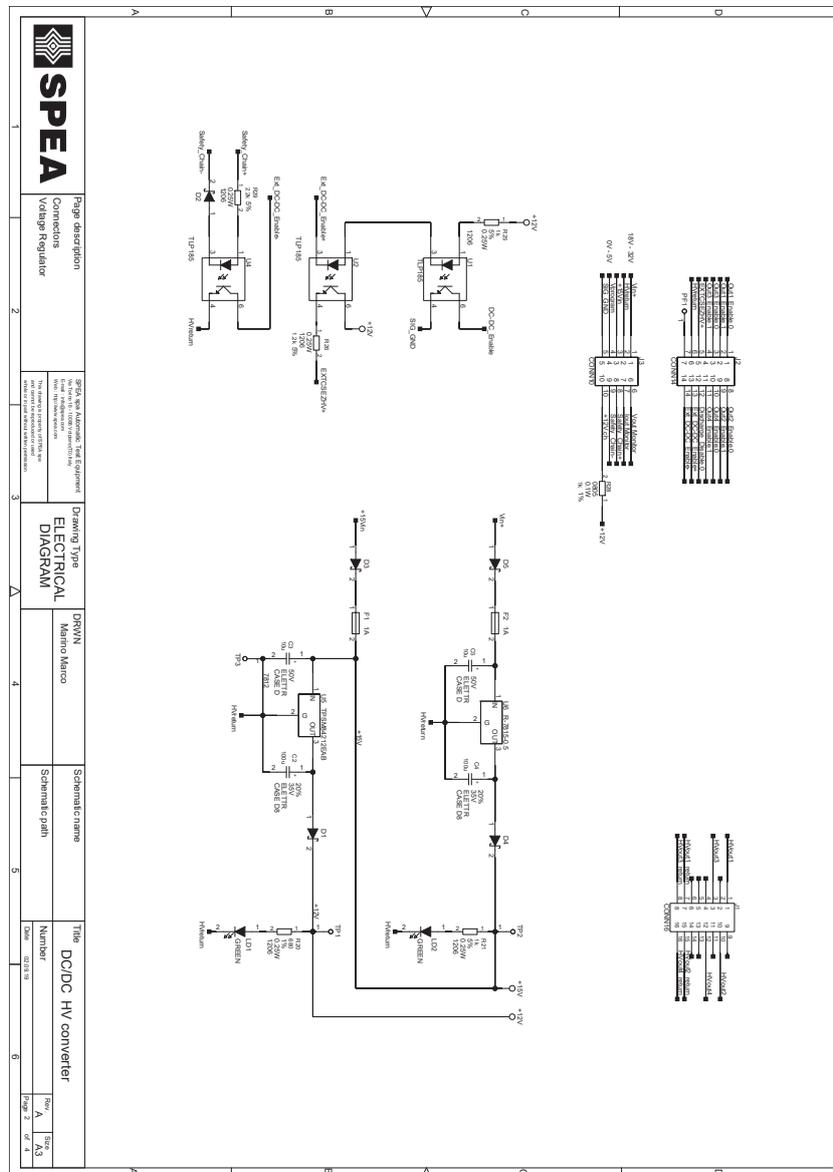
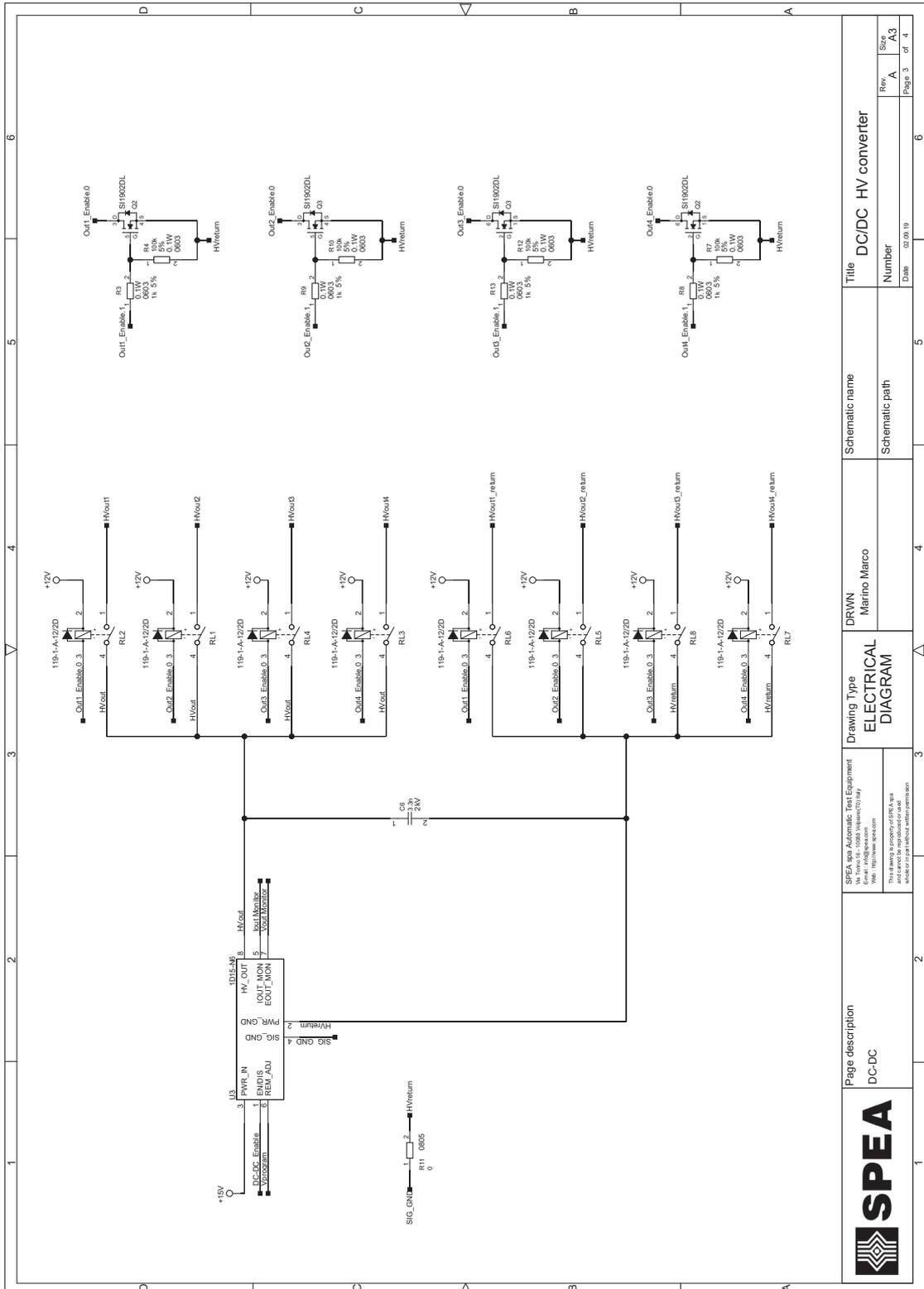


Figure 5.14: Drawing DC/DC HV Converter - Connectors, Voltage regulators



	Page description	DRWN	Title DC/DC HV converter
	DC-DC	Marino Marco	
SPEA spa Automatic Test Equipment Via Torino 16 - 10085 Vigonovo (TO) Italy Web: http://www.spea.com This is a proprietary document of SPEA spa and cannot be reproduced or used without the prior written permission.		Drawing Type	Schematic name Schematic path
		ELECTRICAL DIAGRAM	
		Number	Rev. A Page 3 of 4
		Date	02/06/19

Figure 5.15: Drawing DC/DC HV Converter - Output configuration

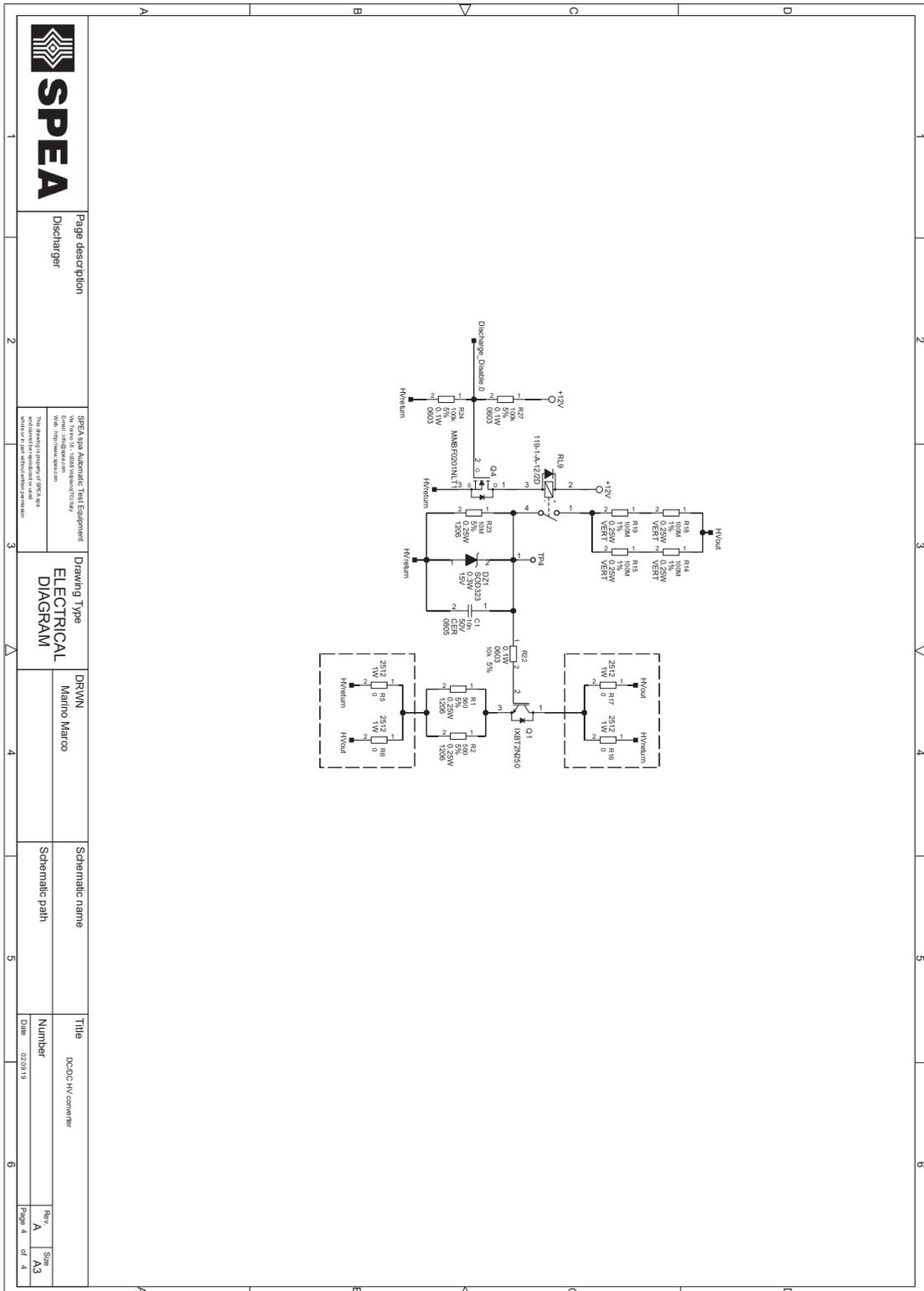


Figure 5.16: Drawing DC/DC HV Converter - Discharge

Appendix C

Test Plan code

```
1 using Serilog;
2 using Serilog.Core;
3 using Serilog.Events;
4 using Spea.DBusWrapper;
5 using Spea.LeonardoF;
6 using System;
7 using System.Linq;
8
9 namespace TPGM
10 {
11     public static partial class TestPlan
12     {
13         static Variant variant;
14         static string productCode = string.Empty;
15         static string testStationID = string.Empty;
16         static string date = string.Empty;
17         static string palletSerialNumber;
18         static string[] EEP;
19
20         // Shortcut for Current Site
21         static Site CurrentSite => Tester.GetCurrentSite<Site>()
22         ;
23
24         public static int TestPlanStart()
25         {
26             // Read Sites and set Offsets
27             Tester.ReadSites<Site>();
28             Tester.UserFlagOffset = 16;
29
30             // Configure Logger
31             var consoleLogLevel = new LoggingLevelSwitch();
32             Log.Logger = new LoggerConfiguration()
33                 .MinimumLevel.ControlledBy(Tester.LogLevelSwitch
34                 )
35                 .Enrich.FromLogContext()
```

```
34         .WriteTo.LeonardoLogWrapper(wt => wt.  
           LeonardoConsole(levelSwitch: consoleLogLevel,  
                           sitePadding: 4)  
35         //.WriteTo.File(new LeonardoTextFormatter(  
           sitePadding: 4), @"C:\Users\SPEA\Desktop\  
           MainEntryLog.txt")  
36         .WriteTo.Seq("http://localhost:5341")  
37         .WriteTo.CdColl(logFilter: SerilogExtensions.  
           LogFilter.EqualityAndRangeChecks))  
38         .CreateLogger();  
39  
40     // Tracemark  
41     palletSerialNumber = System.Diagnostics.Debugger.  
           IsAttached ? "M3E001" : CustomFunctions.  
           GetPalletSerialNumber();  
42     if (!CustomFunctions.TracemarkFCT($"X:\FENIX\  
           TracemarkPallet\{palletSerialNumber}.txt", @"L\  
           SPEA-FCT\GV640-Main3Entry-Variants", out variant,  
           out productCode))  
43     {  
44         Program.TplanResultSet((int)LeoResult.FAIL);  
45         return 1;  
46     }  
47  
48     // Update Debug Levels of Runpack Console  
49     consoleLogLevel.MinimumLevel = variant.  
           DebugPrintEnabled ? LogEventLevel.Debug :  
           LogEventLevel.Information;  
50  
51     // Set Dbus Receive Timeout  
52     DBus.ReceiveTimeoutSeconds = 5;  
53  
54     // Save test station ID and current Date  
55     string systemSN;  
56     using (Tester.IncreaseLogLevel(LogEventLevel.Error))  
57     {  
58         Tester.SystemSerialNumberRead(out systemSN);  
59     }  
60     testStationID = systemSN == "TFTD60AB" ? "02" : "01"  
           ;  
61     date = DateTime.Now.ToString("yyMMddHH");  
62  
63     FuncTestPlan.Add(  
64         SystemInitialization,  
65         CodingFrame,  
66         Varistor,  
67         xCapacitor,  
68         ConnectionPE,  
69         PowerOn,  
70         DBusInit,
```

```

71         IDCheck ,
72         SupplyCurrent ,
73         SupplyVoltages ,
74         HighSpeedCommunication ,
75         LowSpeedCommunicationTest ,
76         NetVoltageCalibration ,
77         DigitalHighVoltageInputs ,
78         MainSwitch ,
79         WakeUp ,
80         TemperatureSensor ,
81         AquaSensor ,
82         DoorSwitch ,
83         FlowMeter ,
84         OpticalSalt ,
85         PTC ,
86         EEPROM ,
87         Watchdog ,
88         Motors ,
89         Triac ,
90         DcActuators ,
91         Heaters ,
92         LowCostDoorOpener ,
93         SupplyVoltages ,
94         MaximumStress ,
95         WriteProductionData ,
96         PowerOff
97     );
98
99     /******* AUTOMATIC *****/
100    FuncTestPlan.Start(InitialResults.ReadFromLeonardo);
101    /******* AUTOMATIC *****/
102
103    Program.TplanResultSet((int)FuncTestPlan.Result);
104    return 1;
105 }
106 }
107 }

```

Varistor test code

```

1 using Spea.LeonardoF;
2 using System;
3 using System.Collections.Generic;
4 using System.Linq;
5 using System.Text;
6 using System.Threading.Tasks;
7 namespace TPGM
8 {
9     public static partial class TestPlan

```

```
10     {
11
12     static double measuredVoltage = 0;
13     static readonly FuncTask Varistor =
14     FuncTask.ForEachSite("Varistor",
15
16 // Enable DC/DC Output 1/3
17
18     FuncTest.OnceForBay(() => UserFlags.Set(
19     UserFlags.Group.RelayNO,
20     UserFlags.Position.Rack1_Option2, "15")),
21
22 // Preset Driver
23
24     FuncTest.OnceForBay(() => Driver.DRI1.On(
25     Driver.ConnectionPoint.InterfaceHot,
26     Driver.ConnectionPoint.InterfaceCold,
27     voltageValue: 0,
28     currentValue: 0.1,
29     Driver.VoltageRange._10V,
30     Driver.CurrentRange._1A,
31     Driver.OutputMode.Direct,
32     Driver.OutputFormat.ContinuousON,
33     Driver.SlewRate.Normal,
34     Driver.CurrentLimitBypass.OFF,
35     connectInterfaceSense: true)),
36
37 // Preset DVM
38
39     FuncTest.OnceForBay(() => DVM.DVM1.Preset(
40     DVM.InputStage.LowVoltage,
41     DVM.Coupling.DC,
42     DVM.Filter.LowPass25Hz,
43     DVM.Range._10V,
44     DVM.MeasurementType.DC,
45     DVM.RamAcquisition.Disable,
46     Ton_seconds: 0.035,
47     Toff_seconds: 0.000001, cycles: 1)),
48     FuncTest.OnceForBay(() =>
49     DVM.DVM1.Connect(DVM.ConnectionPoint.Row2,
50     DVM.ConnectionPoint.Row3)),
51
52 // ABUS Connection: Current Measure by Shunt(ABUS1-ABUS4) +
53 HV voltage measure by onboard HW divider (ABUS2-ABUS3)
54
55     FuncTest.OnceForBay(() => Matrix.TpConnect(
56     "227","230", "231", "226")),
57
58 // Start the Voltage Ramp
59
```

```
60         FuncTest.OnceForBay(() =>
61             CustomFunctions.VaristorRamp(
62                 380, 25, out measuredVoltage)),
63
64     // Reset Driver
65
66         FuncTest.OnceForBay(() => Driver.DRI1.Clear(),
67             alwaysExecute: true),
68
69     // Check measured voltage @ 1mA is in range
70
71         FuncTest.OnceForBay(() => Test.CheckInRange(
72             actual:measuredVoltage, high: 591, low: 430,
73             diagnosticRemark:"Varistor Voltage @1mA")),
74
75     // ABUS Disconnections
76
77         FuncTest.OnceForBay(() => Matrix.DisconnectAll(),
78             alwaysExecute: true),
79
80     // Reset DVM
81
82         FuncTest.OnceForBay(() => AnalogTiming.Clear(),
83             alwaysExecute: true),
84         FuncTest.OnceForBay(() => DVM.DVM1.Clear(),
85             alwaysExecute: true),
86
87     // Disconnect DC/DC Output from Line and Neutral
88
89         FuncTest.OnceForBay(() =>
90             UserFlags.Reset(UserFlags.Group.RelayNO,
91                 UserFlags.Position.Rack1_Option2, "16"),
92             alwaysExecute: true),
93
94     // Disconnect Shunt Resistor
95
96         FuncTest.OnceForBay(() =>
97             UserFlags.Reset(UserFlags.Group.RelayNO,
98                 UserFlags.Position.Rack1_Option2, "12"),
99             alwaysExecute: true)
100         );
101
102     }
103 }
```

Discharge capacitor test code

```
1 using Spea.LeonardoF;
2 using System;
```

```
3 using System.Collections.Generic;
4 using System.Linq;
5 using System.Text;
6 using System.Threading.Tasks;
7
8 namespace TPGM
9 {
10     public static partial class TestPlan
11     {
12         static int acquisitionNumber = 1000;
13         static double[] dischargingCurve = new double[
14             acquisitionNumber];
15
16         static readonly FuncTask xCapacitor = FuncTask.
17             ForEachSite(
18                 "X-Capacitor",
19                 // Connect DC/DC Output to Line and Neutral
20                 FuncTest.OnceForBay(() => UserFlags.Set(UserFlags.
21                     Group.RelayNO, UserFlags.Position.Rack1_Option2,
22                     "13")),
23                 // Preset Driver
24                 FuncTest.OnceForBay(() => Driver.DRI1.On(Driver.
25                     ConnectionPoint.InterfaceHot,
26                     Driver.ConnectionPoint.InterfaceCold,
27                     voltageValue: 0, currentValue:
28                     0.1,
29
30                     Driver.VoltageRange._10V,
31                     Driver.CurrentRange._1A,
32                     Driver.OutputMode.Direct,
33                     Driver.OutputFormat.ContinuousON,
34                     Driver.SlewRate.Normal,
35                     Driver.CurrentLimitBypass.OFF,
36                     connectInterfaceSense: true)),
37
38                 // Preset DVM
39                 FuncTest.OnceForBay(() => DVM.DVM1.Preset(DVM.
40                     InputStage.LowVoltage,
41                     DVM.Coupling.DC,
42                     DVM.Filter.LowPass25Hz,
43                     DVM.Range._10V,
44                     DVM.MeasurementType.DC,
45                     DVM.RamAcquisition.Disable,
46                     Ton_seconds: 0.05, Toff_seconds:
47                     0.001, cycles: 1)),
48
49                 FuncTest.OnceForBay(() => DVM.DVM1.Connect(DVM.
50                     ConnectionPoint.Row1, DVM.ConnectionPoint.Row2)),
51                 // ABUS Connection: HV voltage measure by onboard HW
52                 divider (ABUS1 - ABUS2)
```

```
40     FuncTest.OnceForBay(() => Matrix.TpConnect("230", "
41         231", null, null)),
42     // Set DC/DC
43     FuncTest.OnceForBay(() => CustomFunctions.DcDcSet
44         (340, 0.01, out _, out _)),
45     // Preset DVM for RAM Acquisition (1 ms between each
46         aquisition * 1000 aquisitions)
47     FuncTest.OnceForBay(() => DVM.DVM1.Set(DVM.
48         InputStage.LowVoltage, DVM.Coupling.DC, DVM.
49         Filter.LowPass2_5KHz, DVM.Range._10V, DVM.
50         MeasurementMode.Normal, DVM.MeasurementType.DC,
51         DVM.RamAcquisition.Enable)),
52     FuncTest.OnceForBay(() => AnalogTiming.APH2.
53         EnableAndSet(0.0005, 0.0005, 0.000001,
54         acquisitionNumber)),
55     // Turn Off Driver
56     FuncTest.OnceForBay(() => Driver.DRI1.Disable()),
57     // Acquire the discharging curve
58     FuncTest.OnceForBay(() => Tester.RunA(0)),
59     FuncTest.OnceForBay(() => DVM.DVM1.ReadAll(
60         acquisitionNumber, out dischargingCurve, out _)),
61     // Check value after 800ms is below 30V
62     FuncTest.OnceForBay(() => Test.CheckInRange(actual:
63         dischargingCurve[800] * 100, high: 30, low: -1,
64         diagnosticRemark: "X-Capacitor Voltage after 800
65         ms")),
66     // ABUS Disconnection: HV voltage measure by onboard
67         HW divider (ABUS1 - ABUS2)
68     FuncTest.OnceForBay(() => Matrix.DisconnectAll(),
69         alwaysExecute: true),
70     // Reset Driver
71     FuncTest.OnceForBay(() => Driver.DRI1.Clear(),
72         alwaysExecute: true),
73     // Reset DVM
74     FuncTest.OnceForBay(() => AnalogTiming.Clear(),
75         alwaysExecute: true),
76     FuncTest.OnceForBay(() => DVM.DVM1.Clear(),
77         alwaysExecute: true),
78     // Disconnect DC/DC Output from Line and Neutral
79     FuncTest.OnceForBay(() => UserFlags.Reset(UserFlags.
80         Group.RelayNO, UserFlags.Position.Rack1_Option2,
81         "13"), alwaysExecute: true)
82 );
83
84 }
85 }
```

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