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Modulation techniques for AC/DC converters in ultrafast battery charger applications

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LIST OF CHAPTERS

“Non multa,

sed multum”

LIST OF SYMBOLS

B	*flux density*	*[T]*
Ψ	*flux (RMS and peak-to-peak values)*	*[Wb]*
S	*surface*	*[mm^2]*
N	*numbers of turns of the coil*	*[-]*
f	*frequency*	*[Hz]*
ω	*angular frequency*	*[rad/s]*
V	*voltage*	*[V]*
v_M	*mid-point voltage*	*[V]*
I	*current*	*[A]*
i_M	*mid-point current*	*[A]*
Q	*charge*	*[C]*
C	*capacitance*	*[F]*
L	*inductance*	*[H]*
m	*modulation index*	*[-]*
α	*carrier phase shift*	*[°]*
k_p	*PI proportional gain*	*[V/A]*
k_i	*PI integral gain*	*[V/As]*
d	*duty cycle*	*[-]*
s	*switch state*	*[-]*
sgn(x)	*{(x) < 0) = -1: [(x) == 0) = 0]: 1}*	*[sign function]*

LIST OF FIGURES

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ACKNOWLEDGEMENT - RINGRAZIAMENTI

Il lavoro di tesi è stato interamente scritto in lingua inglese. Nonostante questo, ritengo necessario esprimere i miei ringraziamenti in lingua italiana.

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ABSTRACT

Concerning today's exigencies of electrical mains, the possibility to build a reliable technology of electric energy distributed storage in conjunction with the growing market of electric and hybrid vehicles (EV and HEV) address the actual producers' interest mostly on batteries and charger station. Indeed, the UFC (ultrafast charger) technology has been becoming dominant in this ambit for last years, because these devices guarantee high density of power and a variety of combinations in terms of layout (bidirectional or unidirectional applications).

According to the previous motivations, this thesis regards the report of a project of an ultrafast charger conceived by *PEIC (Power Electronics Innovation Center)* of the Turin Polytechnic, patented in symbiosis with *"VISHAY Semiconductor Italia"*, a leader company in the electronic and electric components market.

The charger consists of two different converters: the first one is an AC/DC (active front end) converter while the second one a DC/DC converter (LLC resonant). This paper focuses on the AC/DC stage and highlights how to set up the most efficient control strategy for the structure. In particular, in this AC/DC application an AFE (active front end) converter has been realized. This topology represents an example of multi-level converter, with 3 output connections (p, m, n) instead of 2 (1, 0). It leverages bidirectional T-type switches for mid-point connection.

The principal points of the thesis deal with the advantages guaranteed by the converter (unitary cosφ, low impact on absorbed current by the grid so low THD and TDD, galvanic isolation of the battery, possibility to charge more vehicles contemporaneously, power sharing strategy, and so on) and also with the major issues affecting it (mid-point current control and DC-link balance).

The main problem concerning the control of the structure regards the mid-point balancing. A suitable modulation technique and a proper voltage control are presented as methods to overcome this problematic. This modulation technique is known in technical literature as ZMPC (Zero-Mid-Point-Current) PWM and it is feasible for this application since it acts by nulling the periodic value of the mid-point current on the central connection of the DC-link.

In the end, several considerations, supported by proper figures and comments, are presented in this paper and a final section reports further conclusions about the treated topics.

INTRODUCTION

The growing interest in electric mobility (HEV, PEV and EV) in conjunction with the possibility to achieve demand-side-management, have been the motivations leading the efforts of power electronic researches on ultrafast charger technologies for last years, in order to satisfy different market and users necessities. The main pointed out topics of interest regard:

- the possibility to build an *new electric infrastructure* for users' direct grid connection, in order to permit them to recharge their vehicles anywhere (like petrol stations) and in the lowest possible time (so with the highest possible current flow);
- the necessity, for the grid owner, to create a real high capacity *distributed storage* that, in specific circumstances, could be used to guarantee a bidirectional power flow (the charger is as a load for the grid in case of vehicle recharge but it may act as a generator in case of electric energy peak demand).
- the obligation to meet the *EMI requirements* for these kind of electronic devices;
- the responsibility of today's generation to evaluate the possibility for a new way of intending mobility as electric and sustainable (*zero emission mobility challenge*);

The main issue tied with the proposal targets regards the huge required power density of this kind of chargers. They have to be not only compact but also powerful (up to 300 kW of power provided per single charger). As a first sight, it is not trivial to highlight that, in almost all the cases, these kind of devices are made up of more than a single unit. Usually, 5 or more units are connected in parallel and in this way the power absorbed by the single unit can be significantly lower than the whole power absorbed by the charger. Without this shrewdness, the realization of the charger could even be impossible.

A simple solution might be searched in MV grid connection (up to 1 kV) but at the moment the state of art of semiconductors for such kind of applications can be really complex, due to the voltage rating of the components (IGBTs, MOSFETs switches and diodes). Consequently, the majority of producers prefer to deal with LV grid connected converters, providing then a higher current flow to fulfill the power request. Nevertheless, the power demand of these devices cannot be reached without the use of a specific topology for the converter and this is the reason why the interleaved topology is the preferred one. It is the most diffused and suitable since enables both to obtain the condition of LV grid connection

and high current request in order to achieve the desired power demand. UFC (UltraFast Charger) is the name used in literature to describe these kind of devices.

The UFC has to be connected in any time both to the grid and to loads (the vehicles to recharge). As a consequence, the UFC is indeed a back-to-back converter, with an AC/DC interface (for grid-converter connection) and a DC/DC stage (for converter-load connection). Between the stages of the converter is interposed a voltage DC-LINK in order to guarantee continuity of voltage for loads and also protection from voltage dips and swells originated by the grid.

The purpose of the thesis is to provide an accurate and precise study, both simulative and experimental, of the AC/DC stage of an UFC, with a specific focus on the control of the converter, considering the main issues of the case, for example:

- **the optimal choose of the converter to use among different alternatives in literature (in terms of layouts, components and technologies);**
- **the necessity to guarantee the immunity of the converter from the disturbances coming from the grid (in order to satisfy the EMI standards for the phase current absorbed by the grid in terms of TDD, Total Demand Distortion);**
- **the critical point of the control of the converter;**
- **the performances that may be obtained by the converter using a variety of different modulation techniques;**

In addition, a conclusive chapter is proposed to summarize the activities of the thesis and to provide further considerations about the treated topic and their eventual future scenarios.

CHAPTER 1: STATE OF ART OF UFC

1.1 Advantages of multi-level conversion

Today's state of art of UFC charger permits to recharge the battery pack of an electric vehicle in a reasonable time (400 km of autonomy in 10 minutes of recharge). In order to achieve this result, it is necessary to have a huge power density (at least 300 kW), to guarantee a sufficient current flow (up to 300 A_{RMS}). As already suggested in the introduction, the use of MV grid (up to 1 kV) is not really feasible, due to the voltage rating of switches and semiconductors properties. For this reason, the use of classical 2-levels topologies for the converters within the charger could result in an inefficient structure or even in a not achievable one in certain cases. As a consequence, preferred topologies for these kind of devices are oriented to multi-level converters and interleaved topology. These are the two main features of the UFC that will be described in the case study of this thesis. In this paragraph and in the following one, it will be shown both the advantages of multi-level conversion and the mainly used topologies for this kind of applications. As a useful example, let introduce firstly, same practical measure of grid/battery connection in terms of voltage and current values [7]:

- existent electric vehicle batteries may have a wide voltage range, usually:

$$V_{batt} = 200 \div 1000\ V$$

- considering a *boost-type* AC/DC converter topology (as it is normally the case), the actual value of voltage could float among 0.9 pu and 1.1 pu of the nominal value of voltage, thus:

$$V_{grid} = (400 \pm 10\%)\ V_{RMS}\ yields\ to\ V_{dc,min} = \sqrt{3} \cdot 400 \cdot 0.9\ V_{RMS} \cong 625\ V_{RMS}$$

The V_{dc} choice is of utmost importance, since it influences the voltage rating of the semiconductor devices and the DC/DC converter topology;

- the maximum battery charging current impacts the DC/DC converter design and it is limited by the connector, according to the *CCS Combo* standard to:

$$I_{batt} = 350\ A_{RMS}\ at\ 1000\ V$$

Thus, in this case:

$$I_{grid} = 565\ A_{RMS}\ at\ 625\ V_{RMS}$$

Where the last value of current (I_{grid}) represents the actual current absorbed by the grid at the fixed voltage of $V_{dc,min}$ (for the assigned power of 350 kW).

The power electronics supply of high-power electrical systems from the three-phase ac mains to the load is usually carried out in two stages, i.e., the mains ac voltage is first converted into a dc voltage and then adapted to the load voltage level with a DC/DC converter (with or without galvanic isolation). Therefore, the typical grid-load connection consists in [7]:

- grid/transformer interface;
- AC/DC stage (conversion stage);
- Voltage DC - link;
- DC/DC stage (for battery/grid connection);

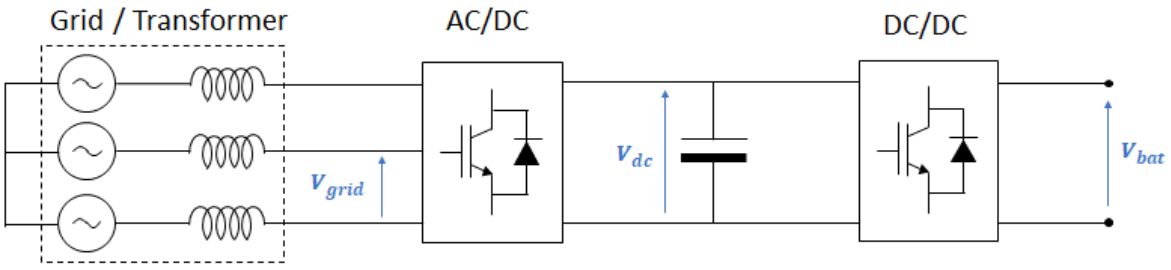


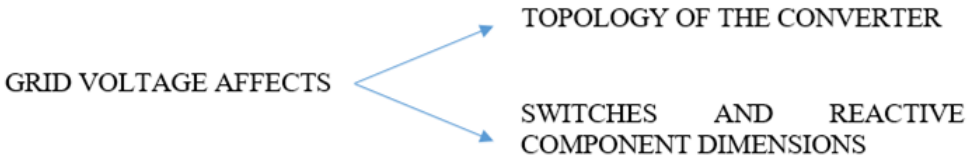
Fig. 1: Example of grid-battery connection.

In the simplest case, the rectifier consists in a unidirectional three-phase diode rectifiers with capacitive smoothing of the output voltage and inductors on the AC or DC side (assuring voltage and current continuity for loads). Despite the low complexity and high robustness (no control, sensors, auxiliary supplies, or electromagnetic interference EMI filtering) of this concept must, this structure has to face against the disadvantages of relatively high effects on the mains and an unregulated output voltage directly dependent on the mains voltage level. Then, the AC/DC stage has to be chosen carefully in order to guarantee both load and grid specifications, for example:

- *unitary power factor* ($\cos\varphi \approx 1$);
- low THD and TDD (*TDD* < *0.05*, in order to assume current waveform as sinusoidal);
- high efficiency (so, *reduced losses* in nominal working conditions);
- *high power density* (reduced devices and reactive components encumbrance).

Consequently, a proper AC/DC structure has to be patented in order to match this requirements. The *AFE converter (Active Front End)* is a AC/DC converter derived from the one-phase PFC (Power Factor Corrector) that permits to mitigate the harmonic distortion of the current absorbed by the converter from the grid, in order to eliminate the disturbances on

the load reducing further the dimensions and the cost of the reactive components (capacitors and inductors) necessary for the filtering operations.



A primal split among AFE applications for UFC regards *low frequency solutions* and *high frequency solutions*. In both cases, it is necessary to provide an effective galvanic isolation between the grid and the load, definitely [7].

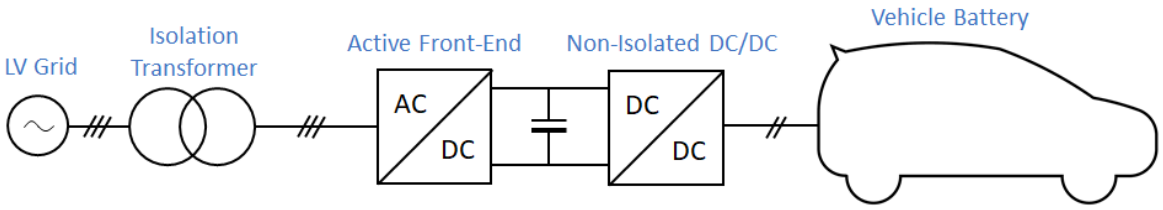


Fig. 2: LF solution with galvanic isolation.

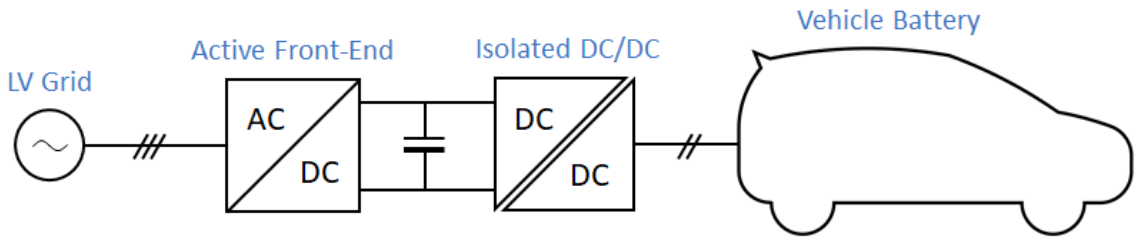


Fig. 3: HF solution with galvanic isolation.

In LF applications the isolation is provided through the use of a dedicated *isolation transformer* that permit to isolate the load from the grid and further it keeps constant the voltage at the AC/DC stage input (in an independent grid manner). These kind of devices have the drawback of being bulky. Anyway, they enable the use of a non-isolated DC/DC converter stage (reducing costs and complexity of the system). On the contrary, in HF application, the isolation is provided by the DC/DC stage directly, since the system layout can be "*transformer-less*". This is the direction followed by the majority of UFC constructor, since it guarantees the main advantages (low costs, high efficiency, compactness and so on). A *high-frequency transformer* is a special transformer used in HF application (f_{sw} almost of kHz or even MHz) to guarantee galvanic isolation between grid and load or between two different levels of a multi-level converter.

These kind of devices are characterized by:

- *reduced encumbrance* in comparison with traditional LF transformer, due to the fact that for transformer the RMS value of the voltage depends on:

$$V_{RMS} = \frac{2\pi}{\sqrt{2}} BfSN \tag{1.1}$$

  the flux density B [T], the frequency f [Hz], the surface S the flux density insists on [mm^2] and the numbers of turns of the coil N [-]; therefore, at constant flux density B, if frequency f increases, the surface S decreases proportionally.
- the *iron losses P_{fe} are reduced* thanks to the creation of internal air gaps within the conductors (sintering ferrite), that mitigate the circulation of parasitic current;
- *high power density* (thanks to a reduced surfaces S).

These are the major motivations that have been orienting the developing of AFE technology for last years. The AFE converters are examples of multi-level converters. *Multi-level converters* are converters in which the base layout is not represented by the canonical cell for hard commutation (combination of switch and diode for freewheeling operations) but they consist of the combination of more devices with a specific topology.
The NPC circuits (isolated or non-isolated), the Vienna rectifier and the T-type rectifier are examples of 3-levels converters. The AC/DC stage is configured as follow

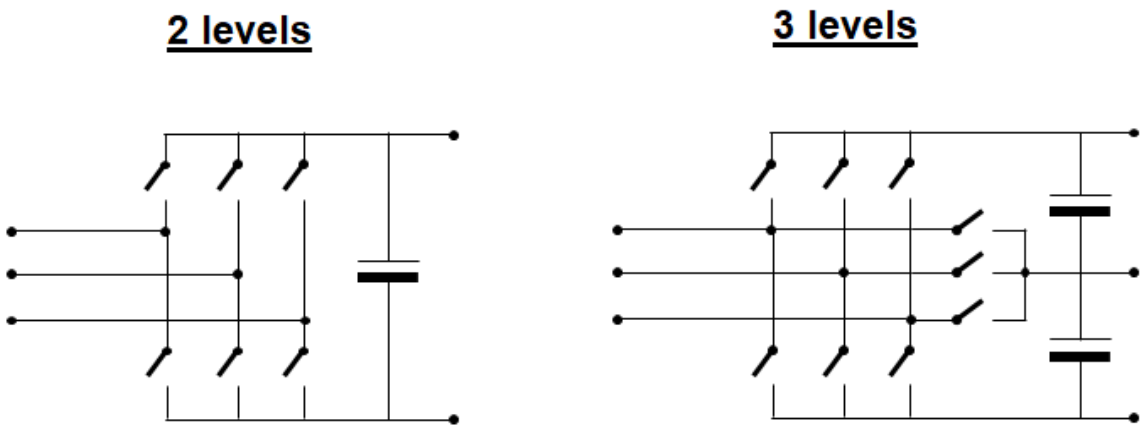


Fig. 4: Model of a 2 levels and a 3 levels converter.

With the use of a 2 levels converter it is possible to control switches only up and down (thus 1 or -1 as modulation index or 1 and 0 as bits). The chance to have more possible states for switches (for example in a 3 levels converter switches state can vary between up, down and mid, thus p, n and m state) enables to *increase the resolution of regulation in amplitude*.

This fact leads to a variety of advantages, for example:

- *increase the accuracy and precision of regulation*, since the *error* of regulation can be *halved* increasing the number of levels from 2 to 3;
- as a consequence, the previous fact permits to *decrease the dimensions of reactive filters* necessary to provide EMI standard and guarantee the quality of the voltage profile for loads (assuring also a reduction of cost of the reactive components);
- *decrease the boost inductance dimensions* at converter input;
- *reduce the commutation losses* P_{comm}, since it is now possible commutate within smaller field of regulation. Thus:

$$P_{comm} = f(V_c, I_L)$$

V_c represented the commutated voltage and I_L represents the current absorbed by the load.

In 2-levels converters (for example in a 2-levels VSI) the load voltage regulation is realized through the use of the *triangulation method* (within the regulation hexagon), thus with the use of a single carrier PWM and the BEM technique. Therefore, the vector $\vec{v}_m$ (shown in fig. 5) can be realized only generating a proper error in magnitude and phase. In this example, $\vec{v}_m$ belongs to the sector $(1_p 3_n 0_n^p)$ and for this reason only the m_2 (modulation index of leg 2) varies to realize the desired regulation. As an example, it is to note the following figure.

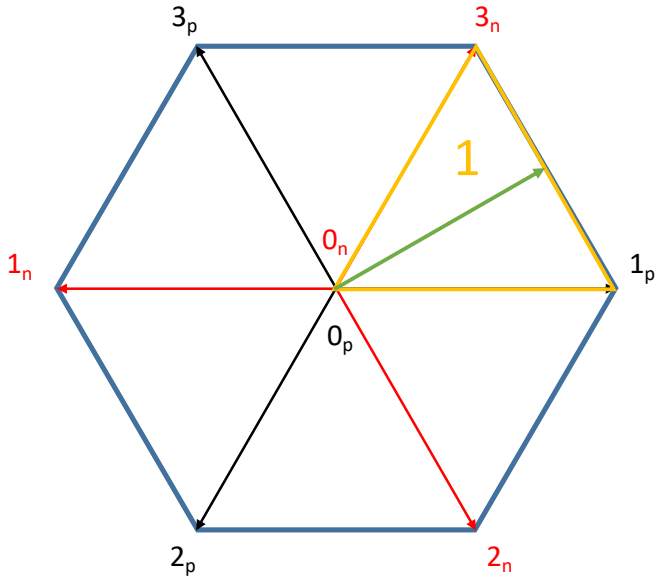


Fig. 5: Vectors to control in sector 1 in a 2 levels 3-phases hexagon

$SECTOR\ [1]\ (1_p, 3_n, 0_n^p)$	
$VECTORS$	
1_p	$(1,-1,-1)$
3_n	$(1,1,-1)$
0_p	$(1,1,1)$
0_n	$(-1,-1,-1)$

Chart 1: Vectors to control in sector 1.

To obtain the vector $\vec{v}_m$ (within sector 1), only the second switch varies from -1 to 1 (the others maintain their states), according to the following statement:

$$m_f \in [-1,1] \text{ where } f = 1,2,3 \tag{1.2}$$

Increasing the switch states from 2 to 3 it is possible to double the resolution in magnitude, which means, at the same time, a halved error of regulation. A multi-level converter is always more precise and accurate than a single-level converter.

MULTI-LEVEL CONVERSION ⟶ NEW MODULATION STRATEGIES

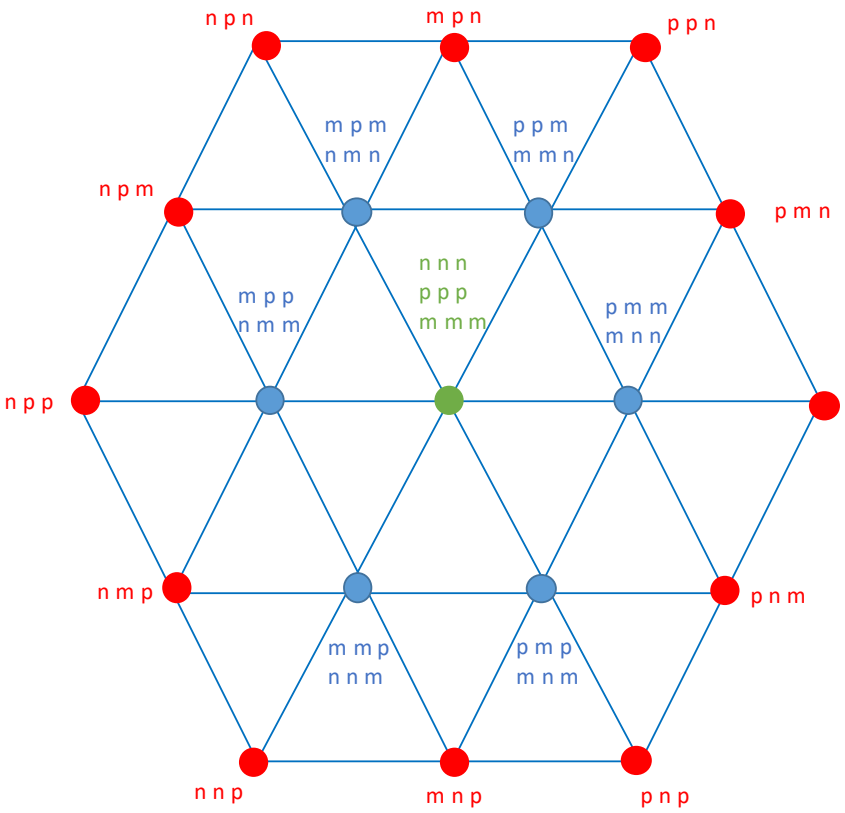


Fig. 6: Model of a 3 levels regulation on the 3-phase hexagon.

Figure 6 has to be interpreted defining the *multiplicity of a state* (ν). In particular:

$\upsilon_a = 1$ (3-levels VSI)
$\upsilon_a = 2$ (2-levels VSI)
$\upsilon_a = 3$ (numbers of zeros of the system)

In each multi-level converter the multiplicity of zeros, (p p p), (m m m) and (n n n), is equal to the number of switch states permitted N_L. Consequently:

$$\boldsymbol{N_L = \upsilon} \tag{1.3}$$

On the contrary, in a 3-levels converters (for example in a 3-levels VSI) the regulation hexagon will be characterized by 3 levels of *zero multiplicity* instead of 2 (as shown in fig.6). As a reference model, the canonical cell for hard commutation (2 levels multiplexer) is substituted by a *4-pole model* (3 levels multiplexer) as shown in figure 7.

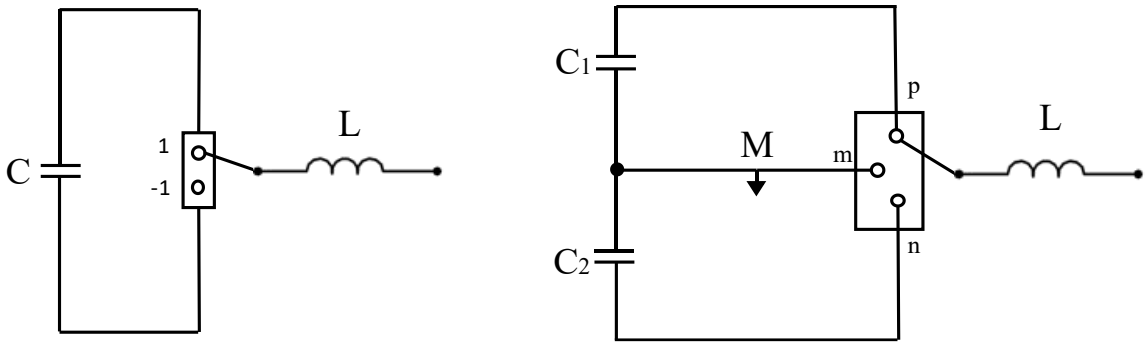


Fig. 7: Comparison between 3-pole and 4-pole model for single-level and multi-level conversion.

In the second figure it is to note that in a multi-level converter (3 levels), it is possible to control 3 different hard switching states (m, p and n). The *mid-point of the 4-pole* is the point M. It represents the mid-point of a split DC link and the centre of the triad (p, n, m).
Differently from 2 levels converters, it is possible to see the mid-point M from outside and v_M moves due to the presence of differential mode component of DC-link voltage. For example, the control strategy of the converter could be addressed to manage the mean value of that voltage (v_M) to zero. As a first sight, the major *drawbacks* of multi-level conversion regard:

- ***high circuit complexity (higher number of switches and degrees of freedom);***
- ***control of the output voltage mid-point required.***

A variety of modulation strategies has been developed for mid-point voltage and current control. The reader has to move to paragraph 1.5 to see a brief review of modulation strategies reported in the thesis (for simulative goals).

1.2 List of topologies for AC/DC converters

A variety of different topologies have been presented in technical literature about 2-levels or 3-levels converters in AC/DC applications. Indeed, these devices can be used both as inverter or rectifier, according to the specific connection source-load of the components (diodes and switches) and their properties (unidirectional or bidirectional switches). Concerning low voltage ultrafast-charging solutions (LV UFC), the utmost interesting solutions for AFE converters (AC/DC interface) existing and/or proposed in literature regards the following topologies:

- **2-levels rectifier/inverter;**
- **NPC (neutral point clamped);**
- **Vienna rectifier;**
- **T-type rectifier/inverter.**

As a basic model, a *2-levels rectifier/inverter* (both for AC/DC and DC/AC conversion) is shown in the following figure.

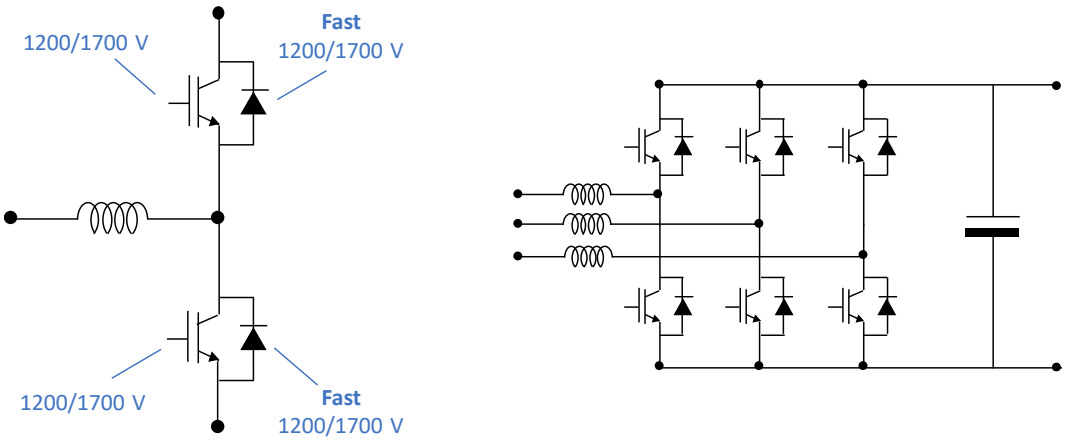


Fig. 8: AFE with 2-levels rectifier/inverter

Each converter leg requires at least 2 fast diodes ($V_{rated,D}$ = 1200/1700 V) and 2 transistors ($V_{rated,MOS}$ = 1200/1700 V). This structure guarantees same interesting advantages:

- *simplicity* of topology;
- *low conduction losses* (due to the low number of active devices required);
- *possibility of bidirectional flow and storage capability* (even if the bi-directionality of the converter should be evaluated from an economic perspective, it does not represent a prime specification for these kind of devices, especially without the integration of an energy storage into the charging facility);

On the other hand, the main disadvantage of the structure is the fact that the semiconductor devices are full-voltage rated and this obliges to use IGBTs for high voltage applications (up to 1 kV of operating voltage) and fast diodes for freewheeling operations. These components have high costs and limitations in terms of voltage rating and frequency since, if frequency increases, then the switching losses can lead to an overall low efficiency of the converter.
A more suitable topology for AC/DC converters is represented by *NPC (neutral point clamped) topology*. The NPC technology is an example of multi-level converter. The NPC-type can be both integrated or not integrated and used in rectifier or inverter application independently. The schematics are represented in the following figures (9 and 10)

NPC RECTIFIER (AC/DC)

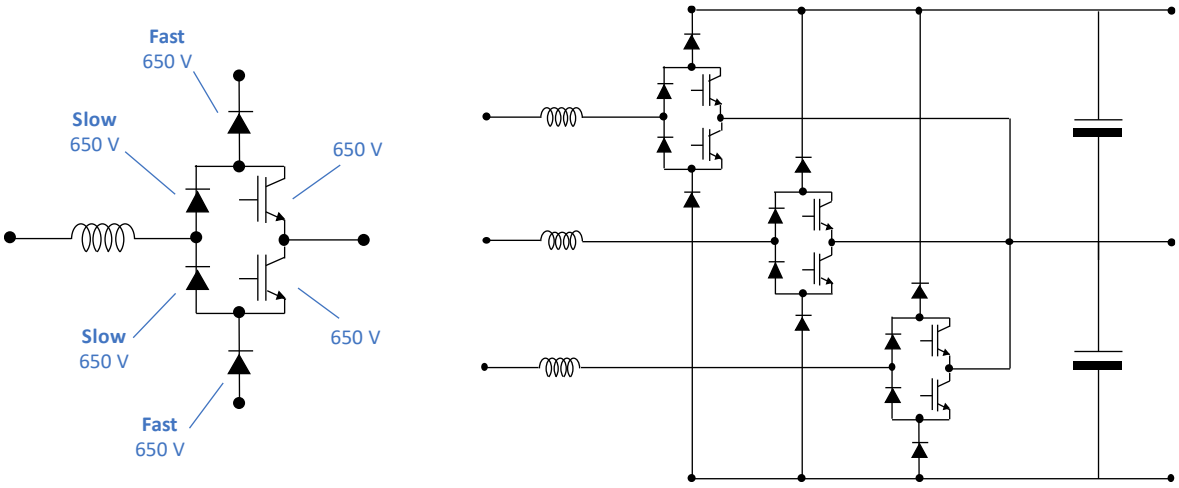


Fig. 9: AFE rectifier with NPC technology (1).

Each converter leg requires 2 fast diodes (V_{rated,D_fast} = 650 V), 2 slow diodes (V_{rated,D_slow} = 650 V) and 2 transistors ($V_{rated,MOS}$ = 650 V). In this layout only 6 active switches are required (they can be unidirectional). As shown in figure 10, the NPC technology can be used also in inverter DC/AC applications. In this case, each converter leg requires 6 fast diodes (V_{rated,D_fast} = 650 V) and 4 transistors ($V_{rated,MOS}$ = 650 V), thus at least 10 active switches (bidirectional) are required.

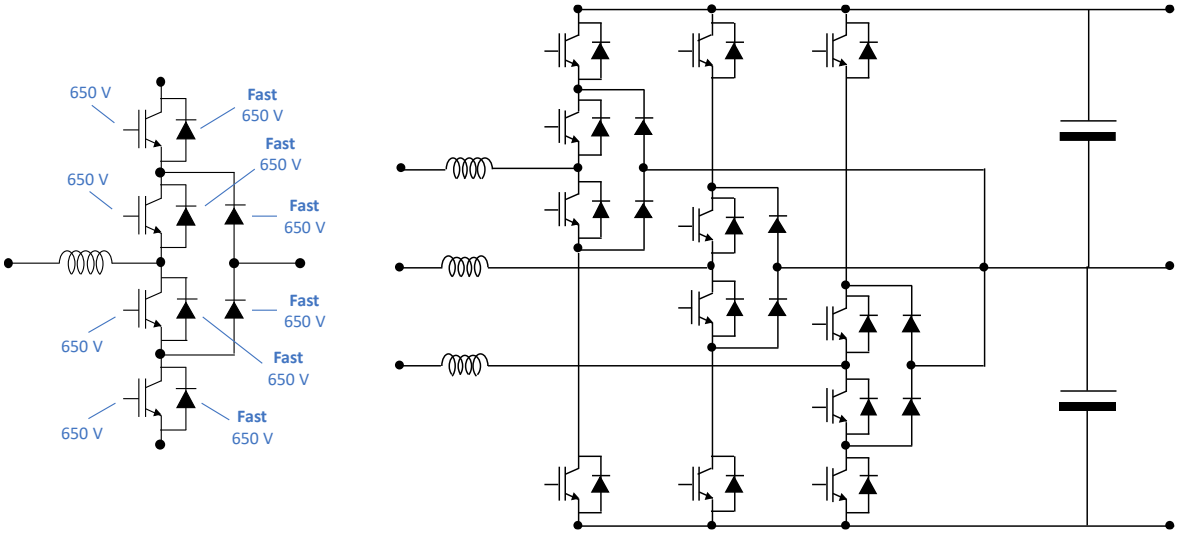


Fig. 10: AFE inverter with NPC technology (2).

NPC technology represents today's state of art for 3-levels converters. It guarantees:

- *half-voltage rated for semiconductor devices*, permitting to use LV devices also in MV applications with minimum voltage rating (until 1,7 kV of rated voltage);
- *reduced conduction losses* in comparison with an equivalent 2-levels structure (due to the decreasing of devices operating voltage).

Contrariwise, the main disadvantages regard:

- *increase in terms of cost* (more devices necessary);
- *high parasitic capacitance* (this issue is reduced if NPC is realized on an IC – integrated circuit);
- more *complexity* of drivers and control systems.

Among 3-levels topologies, *Vienna rectifier* has been widely used to achieve high conversion efficiency. Each converter leg requires 2 fast diodes (V_{rated,D_fast} = 650 V), 4 slow diodes (V_{rated,D_slow} = 650 V) and only 1 transistor ($V_{rated,MOS}$ = 650 V). The configuration proposed (figure 11) is the integrated one but Vienna-type can be both realized in integrated and not integrated configuration as shown in figure 12.

In Vienna-type only one transistor per leg is required. In comparison with NPC layout an inferior number of active switches is needed (reducing costs and losses of the converter). In non-integrated layout the losses can be even reduced with respect to integrated one, since clamping diode (up and down rail connections) are used only in freewheeling operations (but they have to be voltage fully rated). On the contrary, integrated topology is preferred for

higher voltage applications (because all devices are half voltage rated). The following pictures show the layout of the converters in integrated and not integrated topology.

VIENNA RECTIFIER (AC/DC)

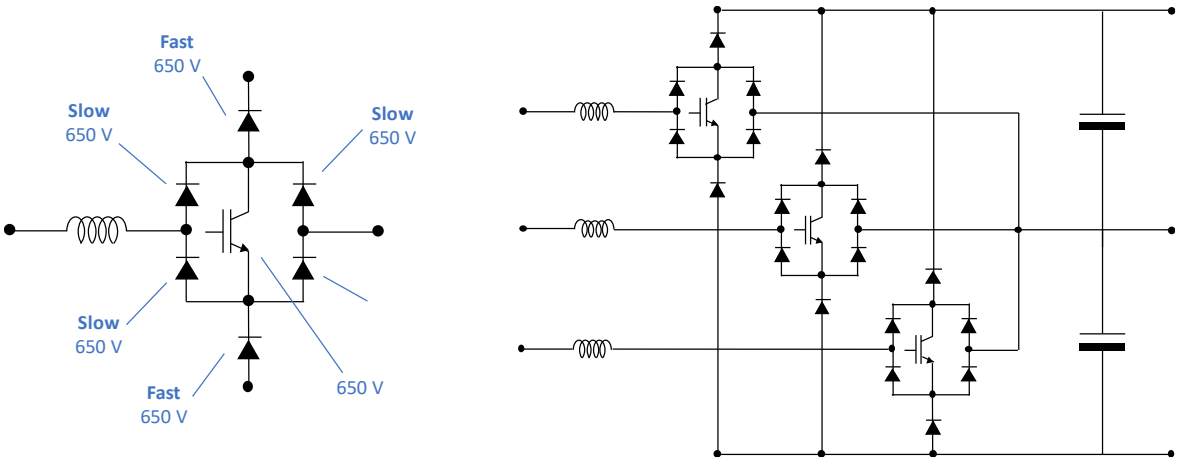


Fig. 11: AFE technology with Vienna rectifier layout.

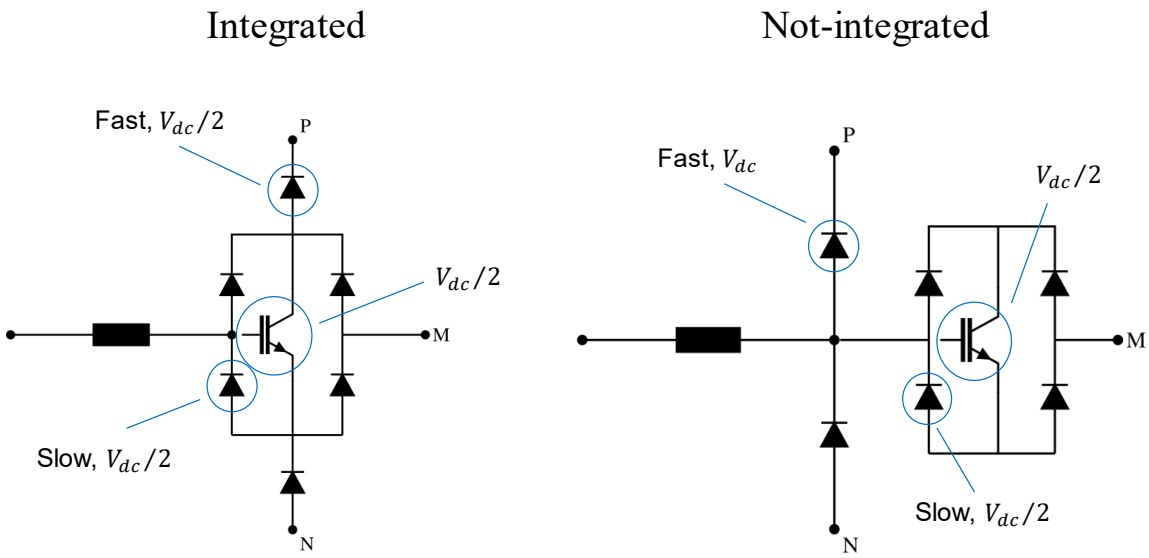


Fig. 12: Vienna topology in integrated and non-integrated layout.

In conclusion, the T-type converter is presented. This converter represents an innovative layout among 3-levels AC/DC or DC/AC applications, since it combines both the advantages of NPC structure and non-integrated Vienna-type. Thus, T-type guarantees:

- low conduction losses (like Vienna-type);
- low number of active components per leg required;
- simplicity of control (only one driver per leg is required).

The T-type structure can be used both in AC/DC (as a rectifier) and in DC/AC application (as a multi-level VSI). The schematics of those converters are shown in the following figures (13 and 14).

T-TYPE RECTIFIER (AC/DC)

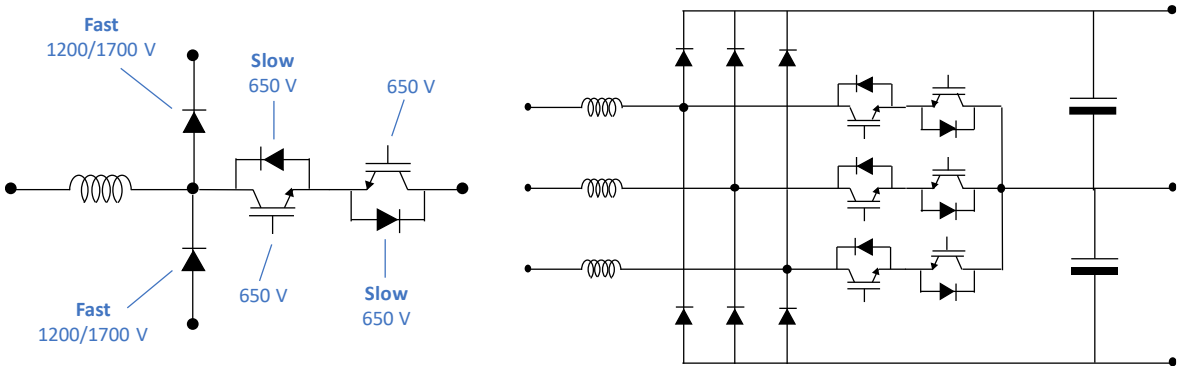


Fig. 13: AFE technology with T-type rectifier layout.

Each converter leg requires 2 fast diodes (V_{rated,D_fast} = (1200 ÷ 1700) V), 2 slow diodes (V_{rated,D_slow} = 650 V) and 2 transistors ($V_{rated,MOS}$ = 650 V). The last two couples of devices can be substituted by two MOSFETs (using as a slow diode the embedded diode within the transistors). Only 6 active switches (unidirectional) are required.

Per each phase leg, one diode is used for positive or negative rail clamping while the remaining ones are anti-series connected to two switches (MOSFETs) to realized middle point connection. This is the striking difference between NPC-non-integrated and T-type converter: in the former the mid-point connection was realized by two anti-parallel switches, in the latter by anti-series ones.

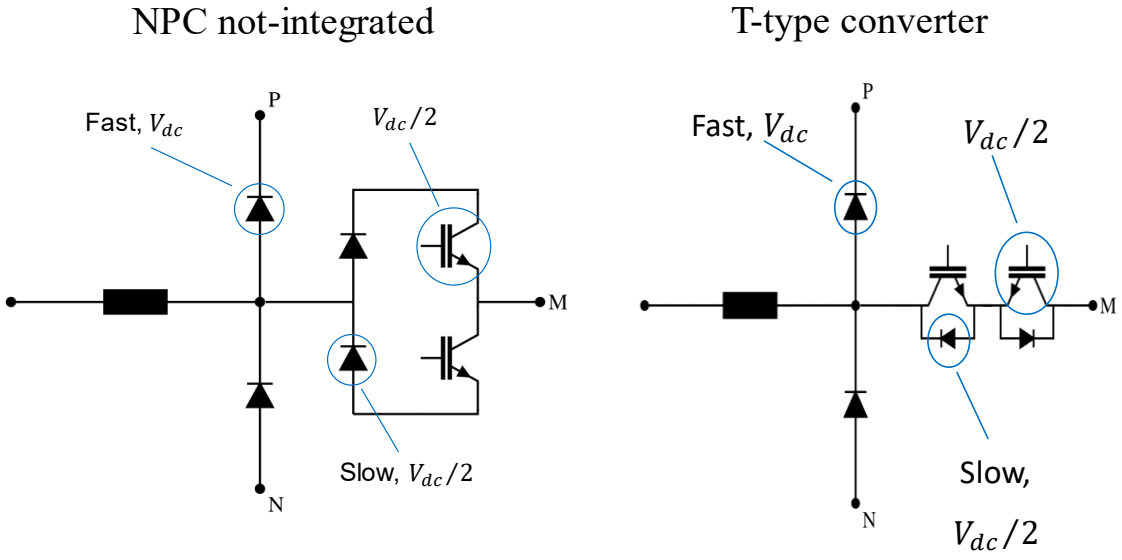


Fig. 14: Comparison layout between T-type and NPC-non-integrated.

As a reminder, the 3-levels T-type converter basically combines the positive aspects of the two-level converter (such as low conduction losses, small part count and a simple operation principle) with the advantages of the 3-levels converter such as low switching losses and superior output voltage quality. Furthermore, with the use of SiC Schottky diodes, the reverse recovery loss from diodes can be eliminated, which makes T-type rectifier a promising topology in achieving high efficiency for today and future applications. Additionally, it is suitable for bidirectional current flow. For these reasons, *T-type rectifier is regarded as the basic converter unit for interleaved system.*

Finally, the T-type for DC/AC application is presented (figure 15). Each converter leg requires 2 fast diodes (V_{rated,D_fast_HV} = (1200 ÷ 1700) V), 2 transistors (V_{rated,MOS_HV} = (1200 ÷ 1700) V), 2 fast diodes (V_{rated,D_fast_LV} = 650 V) and 2 transistors (V_{rated,MOS_LV} = 650 V). The last two couples of devices can be substituted by two MOSFETs (using as a slow diode the body diode within the transistors). At least 12 switches (bidirectional) are required in DC/AC applications. Both structures guarantee very low conduction losses.

T-TYPE INVERTER (DC/AC)

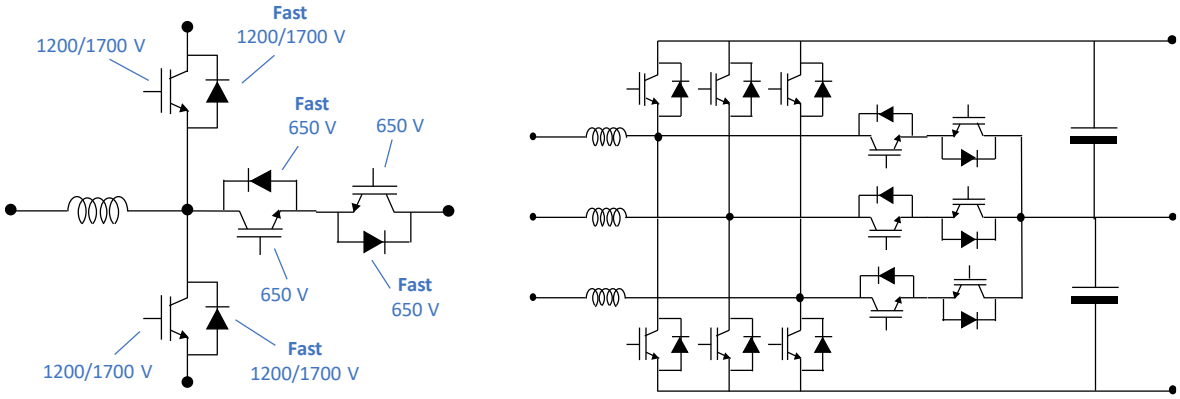


Fig. 15: AFE technology with T-type inverter layout.

The state of art for multi-level converters for UFC is oriented to obtain a reliable and efficient structure, in order to manage easily switching operation at higher and higher rated voltage values. The use of parallel T-type structures is the preferred layout for AFE application in UFC, since it leads to a converter with very low conduction losses, easy control drivers and interleaved connection for high voltage application. This converter is called as *T-type interleaved*. The following schematic has been already presented in [5].

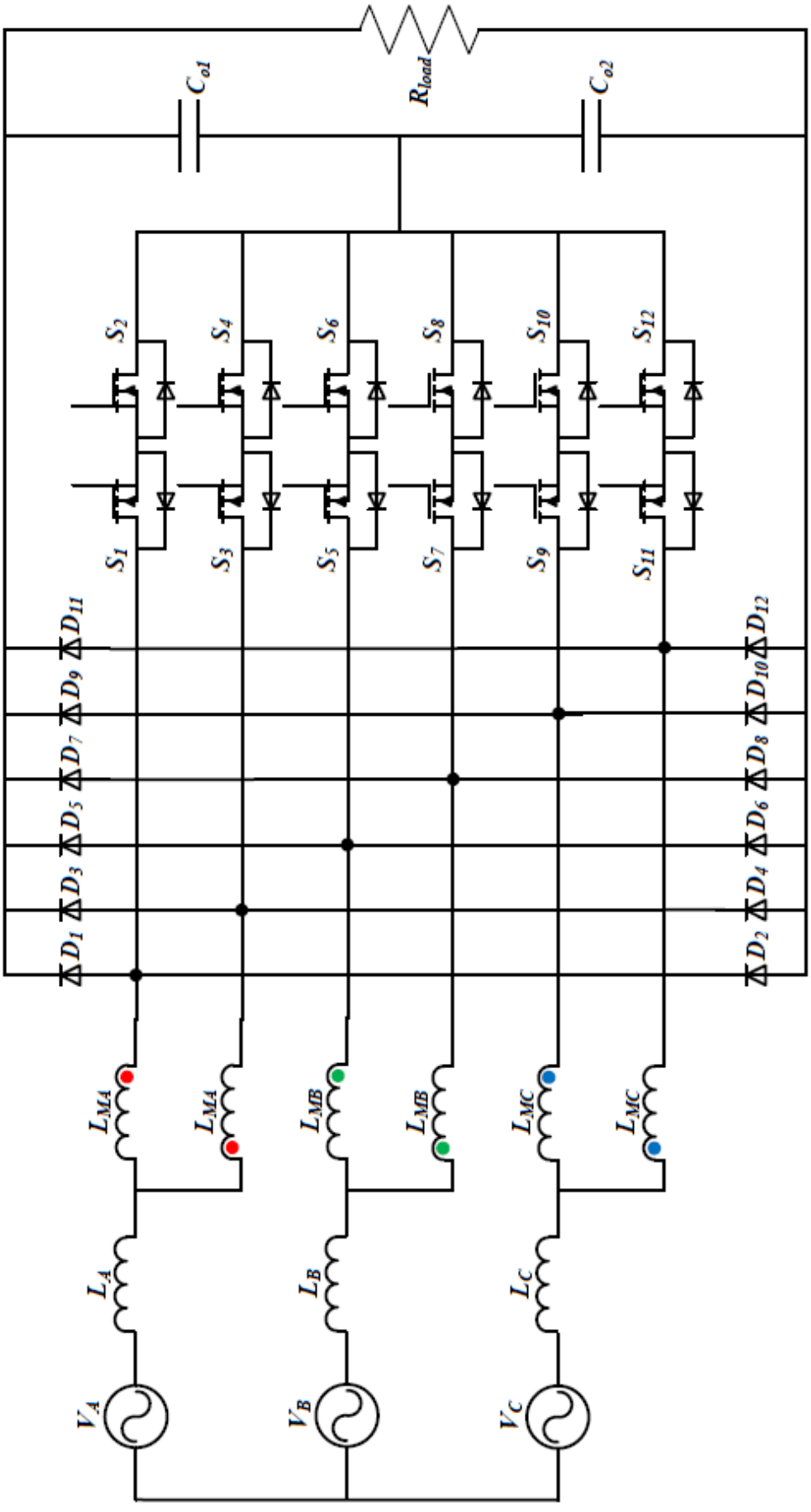


Fig. 16: T-type interleaved AFE.

1.3 T-type interleaved as active rectifier

[5] In high power applications, the multi-level, mixed topologies, or parallel multiple methods (interleaving) is an effective way for expansion of the capacity of the converter. In three-phase parallel systems there are many advantages, such as increasing the current level, reducing the current and voltage ripple, and last but not least, achieving higher bandwidth. In addition, the cancellation effect among interleaved sub-converters allows smaller input filters (lower filtering inductance L_F) and helps to meet EMI requirements. In other words, interleaving permits to obtain the same power quality with the same passive components but with lower *switching frequency* f_{sw} of each sub-converter than a single converter layout, ensuring smaller switching loss. The basic scheme of a single unit of the AC/DC interface is shown in figure 17.

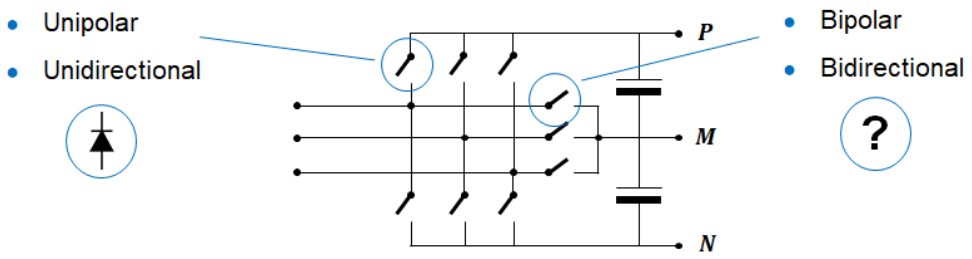


Fig. 17: Basic model for AC/DC interface.

The P and N rails of AFE converter are simple diodes of a bridge rectifier (AC/DC interface) and for this reason they are chosen only in terms of rated voltage. Diodes are simple unidirectional and unipolar devices and this leads to a remarkable robustness and easiness of control. Conversely, the mid-point switches have to be *bipolar and bidirectional*. This is the main issue of the converter because in practice, those devices *do not exist*.

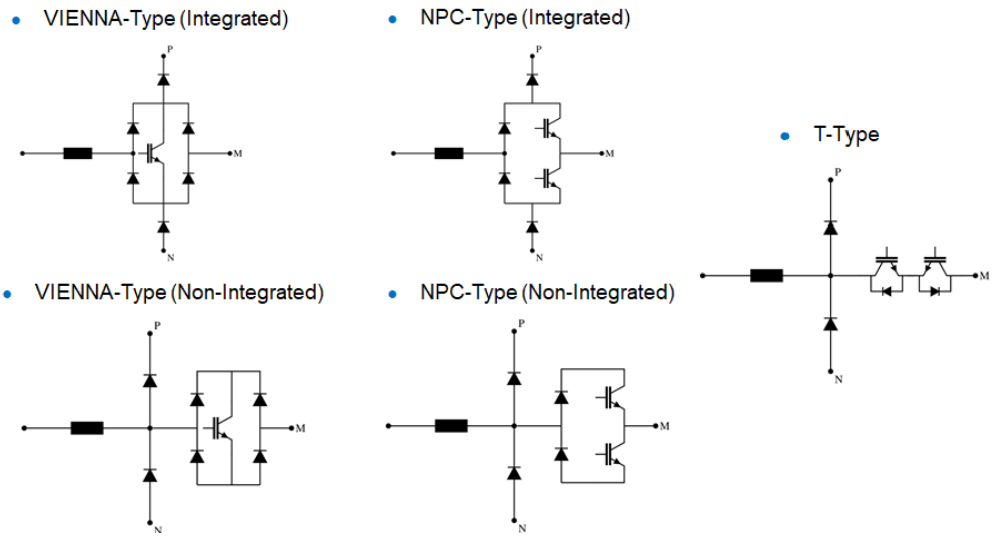


Fig. 18: Examples of bipolar and bidirectional switches.

Therefore, these switches are realized by a suitable combination of existing semiconductor devices, through the use of one of the topology already seen in the previous section (paragraph 1.2).

The T-type interleaved converter is obtained connecting in parallel at least two identical T-type converters. Thus, *T-type interleaved converter* represents the fittest device for AFE application (and active power filters in general).

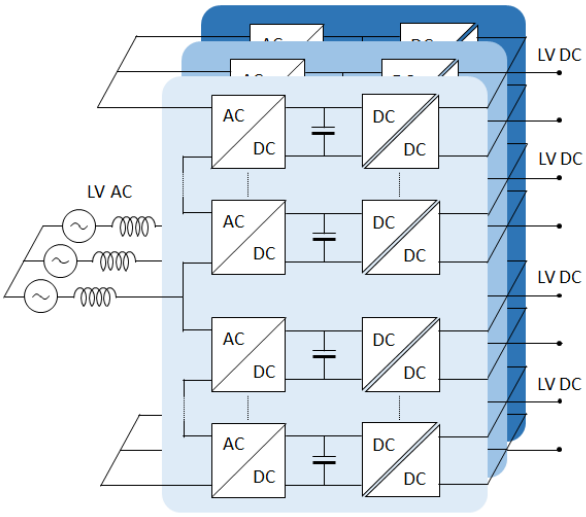


Fig. 19: Interleaved T-type converter.

The operation principle of the T-type converter is explained in figure 20 (with reference to the single operating unit).

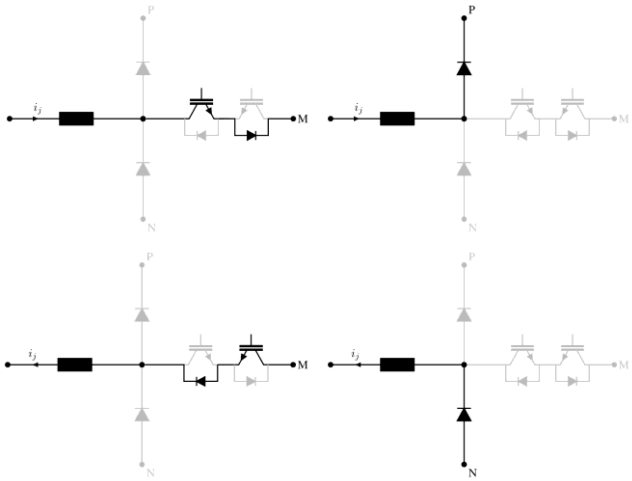


Fig. 20: Operation principle of T-type converter, single unit (1)

The circuit on the left shows the active phase switching of the converter, while the right ones display freewheeling operations. A boost inductor is usually collocated upstream the converter to perform both boost and filtering tasks. In certain application, the two corresponding phase legs (in different sub-converters) are then linked together with an

ulterior inter-phase inductor in series to the boost inductors (figure 21), to increase the whole input inductance of the converter (for flux ripple and HF circulating current reduction).

The T-type converter is a *current-commutated converter*: the devices participating in commutation are determined by current direction. With reference to figure 21, if current I_{A1} is positive [5], the commutation will involve the components D_1, S_1 and S_2. As a result, the voltage potential at point A_1 with reference to the middle point of DC bus will be either half of whole DC bus voltage (with S_1 and S_2 off) or zero (with S_1 and S_2 on).

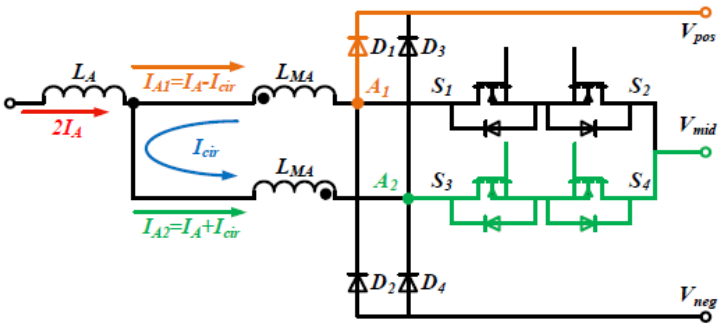


Fig. 21: Operation principle of T-type converter, interleaved, single unit (2).

Indeed, the previous consideration it is valid for all phases; thus, the input voltage formation depends only on (see figure 22)

- the mid-point switch state s_x (the only one controllable by the driver);
- the current direction $sgn(i_x)$ due to the unidirectional nature of the rectifier stage.

$$v_{\bar{x}m} = (1 - s_x) \cdot sgn(i_x) \cdot \frac{V_{dc}}{2} \tag{1.4}$$

Consequently, only three values of voltage can be realized by the converter:

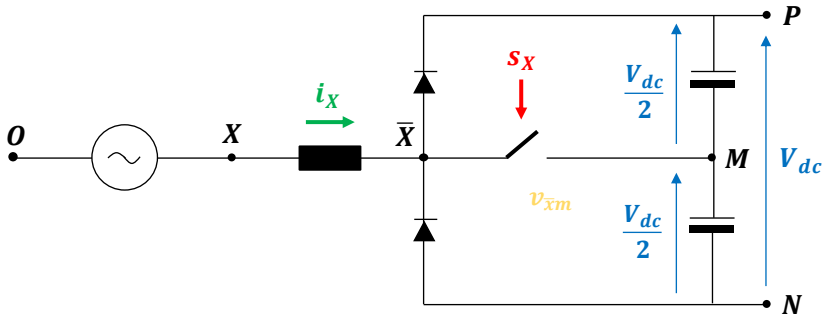


Fig. 22: Input voltage formation.

Vector selection for instantaneous voltage regulation is depicted in a 3-levels 3-phase hexagon, shown in figure 23 [5]. The blue circle in the picture represents the track of the output voltage vector.

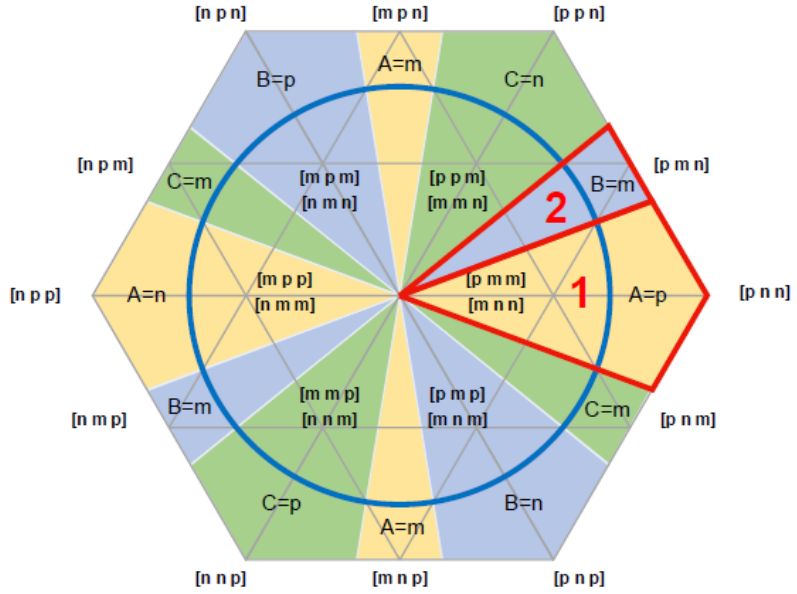


Fig. 23: Voltage selection in a 3-levels 3-phase hexagon.

In particular, the states m, n and p stand for three different instantaneous voltage values performed by the converter.

$$\begin{cases} \boldsymbol{P} \text{ state } \Rightarrow v_{\bar{X}M} = +\dfrac{V_{dc}}{2} \\ \boldsymbol{M} \text{ state } \Rightarrow v_{\bar{X}M} = 0 \\ \boldsymbol{N} \text{ state } \Rightarrow v_{\bar{X}M} = -\dfrac{V_{dc}}{2} \end{cases}$$

Space vector representation is useful to understand the operation of the 3-level converter.

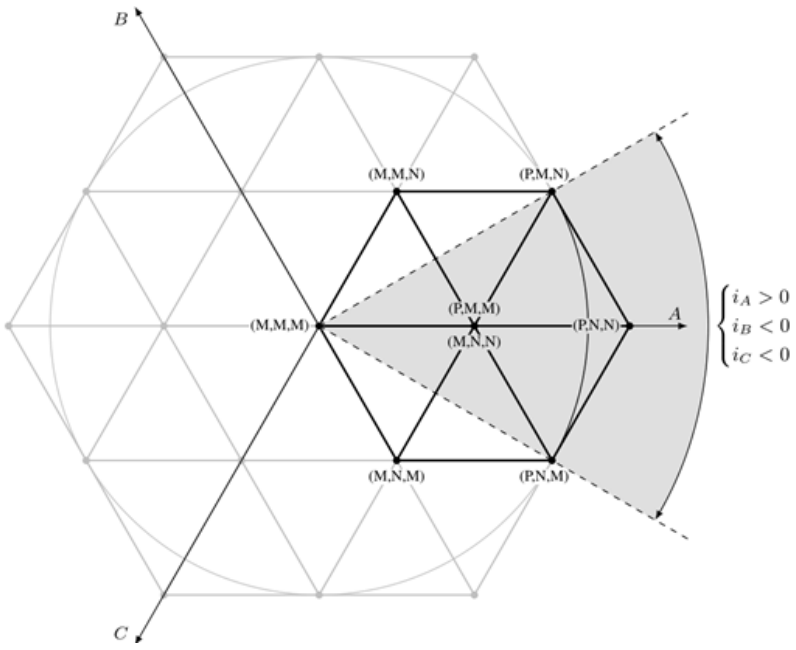


Fig. 24: SV representation of instantaneous voltage vector.

There are 6 different sextants, defined by the 3 currents directions. In each one, there are 2^3 switching states and 7 voltage vectors (then, 2 are redundant). Thus, those $3^3 = 27$ switching states (p, m, n for each bridge leg) yield to 19 voltage vectors (considering redundant states). Voltage and current vectors can be expressed through the following formulas

$$\begin{cases} \vec{v} = \frac{2}{3} \cdot \left(v_{\bar{A}} + v_{\bar{B}} \cdot e^{j\frac{2\pi}{3}} + v_{\bar{C}} \cdot e^{j\frac{4\pi}{3}} \right) \\ \vec{\imath} = \frac{2}{3} \cdot \left(i_A + i_B \cdot e^{j\frac{2\pi}{3}} + i_C \cdot e^{j\frac{4\pi}{3}} \right) \end{cases} \tag{1.5}$$

The space vector representation directly highlights the upper voltage limit in linearity (figure 25): the max phase voltage value is calculated as usually, assuming V_{dc} for voltage DC-link maximum amplitude.

$$v_{\bar{x},max} = \frac{V_{dc}}{\sqrt{3}} \; in \; non - linearity \; operations \tag{1.6}$$

The formula (1.6) displays the advantage in terms of regulation to master the common mode voltage, since the max output voltage increase as shown in figure 25 (from $\frac{1}{3}$ to $\frac{1}{\sqrt{3}}$ of the voltage DC-link max value V_{dc}).

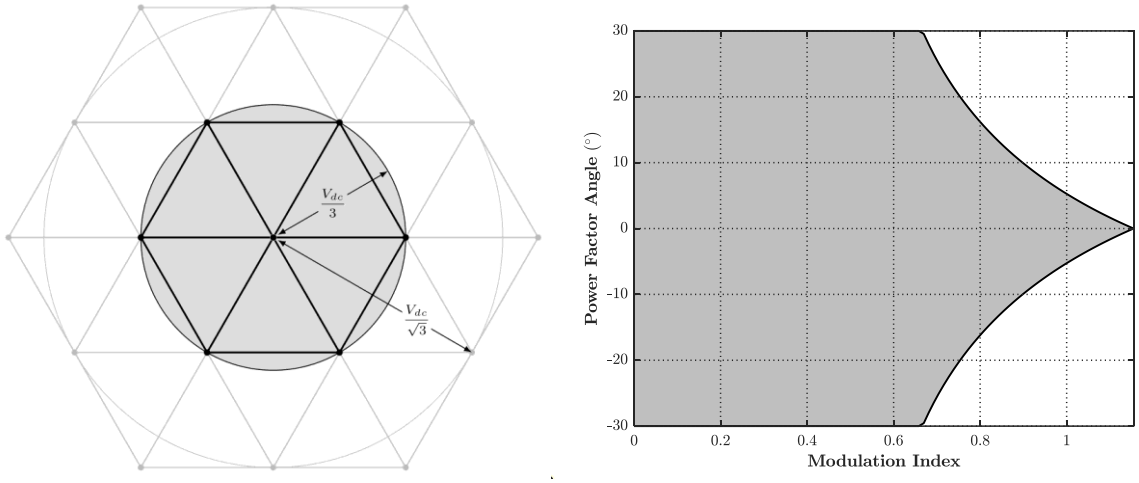


Fig. 25: Limits of regulation in 3-phase 3-levels hexagon and (m, cosφ) chart of the converter.

As usually, the modulation index is defined as by the following formula

$$m = \frac{|\vec{v}|}{\frac{V_{dc}}{2}}, \;\; m \in \left[0, \frac{2}{\sqrt{3}}\right] \tag{1.7}$$

Since 2 of the 7 voltage vectors are located ±30° outside the 60° current sector, it is possible to operate the rectifier with up to -30° < φ < +30° phase shift between input voltage and current vectors. However, as the rectifier input voltage amplitude $|\vec{v}|$ approaches its maximum value $v_{\bar{x},max} = \frac{V_{dc}}{\sqrt{3}}$, the maximum phase shift decreases until it reaches zero at the

maximum rectifier input voltage amplitude (as shown in figure 24 and 25). In this manner, the (m, cosφ) chart of the converter is plotted according to (1.6) equations (figure 25, right).

$$|\varphi|_{max} < \begin{cases} \frac{\pi}{6}\ if\ m \leq \frac{2}{\sqrt{3}}\ linearity\ operation \\ \frac{\pi}{3} - arcos\left(\frac{1}{\sqrt{3}\cdot m}\right)\ otherwise\ (non-linearity) \end{cases} \tag{1.8}$$

In non-linearity operation, the common mode voltage component $v_{0_{LF}}$ is used to adjust the voltage output to the desired value (over-modulation). The common mode voltage component $v_{0_{LF}}$ is limited since the rectifier input voltage of each phase (i.e.$v_{\bar{X}M}$) is limited between 0 and $sgn(i_X) \cdot V_{dc}/2$. Consequently,

$$\begin{cases} \boldsymbol{v_{0,max}} = min\left(\frac{V_{dc}}{4} \cdot (sign(i_X) + 1) - v_{\bar{X}_{LF}}\right) \\ \boldsymbol{v_{0,min}} = max\left(\frac{V_{dc}}{4} \cdot (sign(i_X) - 1) - v_{\bar{X}_{LF}}\right) \end{cases} \tag{1.9}$$

The waveform of the common mode voltage $v_{0_{LF}}$ depends on the specific modulation strategy used to control the converter. Figure 27 shows same examples of common mode voltage component using 4 different modulation techniques reported in literature (PWMC, ZMPC, CSVM and DPWMC).

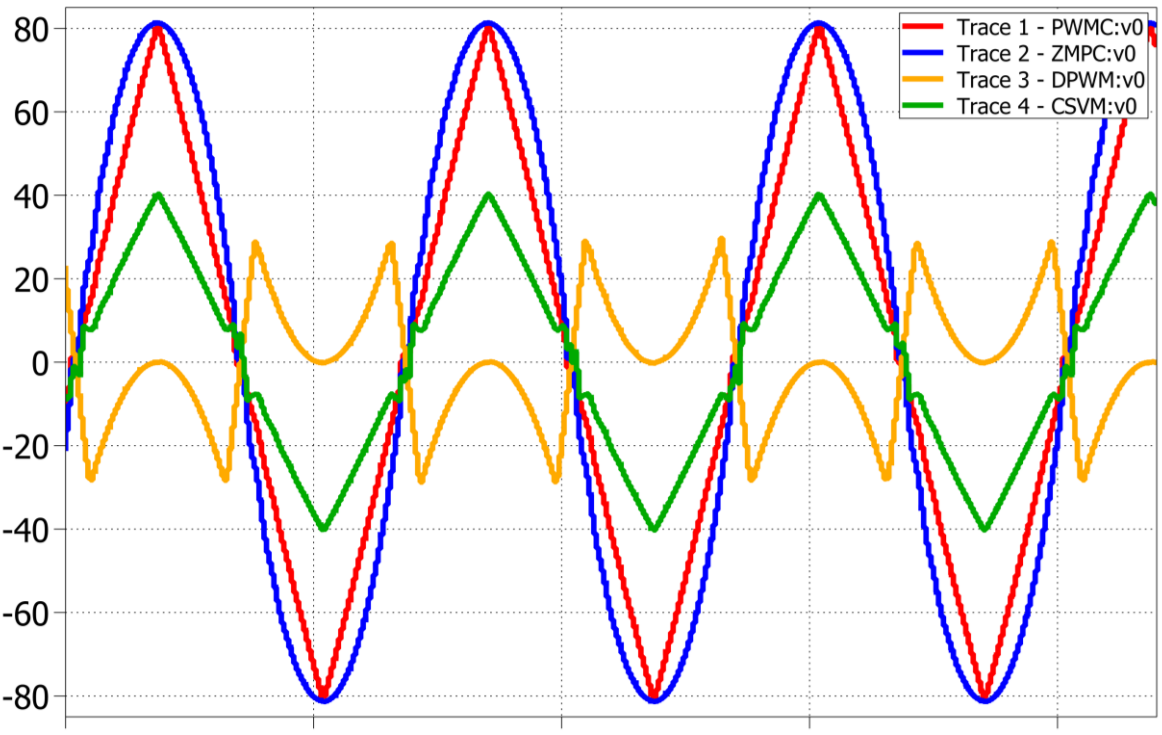


Fig. 26: Examples of $v_{0_{LF}}$ for different modulation strategies (PWMC, ZMPC, CSVM and DPWMC).

Furthermore, to operate the whole converter in interleaved manner, the control can introduce a *phase shift* α between the carriers of the two corresponding phases in different sub-converters. The phase shift between the carriers can be used to achieve different results, for example, reduction of flux ripple on L_{Boost}, current distortion cancellation (to obtain a considerable low THD or TDD) and mitigation of current ripple on output DC-link. A specific paragraph will be dedicated to the topic (*2.2 Hardware design*).

In an interleaved system, all phases operate in a simultaneous way and for this reason, the common mode voltage v_0 results as a linear combination of the phase voltages v_{AM}, v_{BM} and v_{CM}.

$$v_0 = \frac{v_{\bar{A}M} + v_{\bar{B}M} + v_{\bar{C}M}}{3} \tag{1.10}$$

And then, the p*hase voltages*

$$\begin{cases} v_{\bar{A}} = v_{\bar{A}M} - v_0 \\ v_{\bar{B}} = v_{\bar{B}M} - v_0 \\ v_{\bar{C}} = v_{\bar{C}M} - v_0 \end{cases} \tag{1.11}$$

The equivalent circuit (EC) of the t-Type converter is described in the following figure.

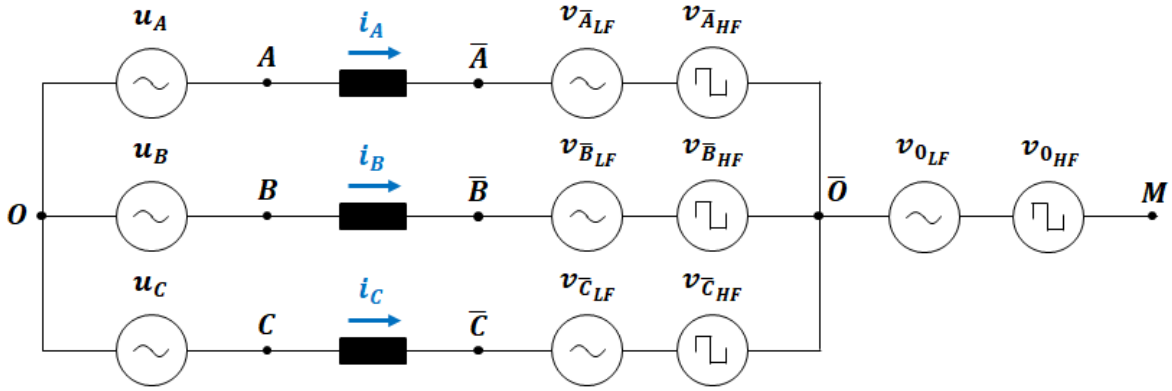


Fig. 27: EC of the T-type interleaved converter.

The phase voltages are classified in LF (low frequency) and HF (high frequency) components. LF voltages components ($v_{\bar{A}_{LF}}, v_{\bar{B}_{LF}}, v_{\bar{C}_{LF}}$) permits to generate the mains current fundamental components ($i_{A_{LF}}, i_{B_{LF}}, i_{C_{LF}}$), while the HF components ($v_{\bar{A}_{HF}}, v_{\bar{B}_{HF}}, v_{\bar{C}_{HF}}$) deals with the mains current at switching frequency (ripple component generation, $i_{A_{HF}}, i_{B_{HF}}, i_{C_{HF}}$). For this reason, it is necessary to tune an appropriate filter (LCL design) in order to reduce those HF residual component and meet EMI standards, moreover eliminating ripple and noise component (see paragraph *2.2.2 Grid-converter interface, LCL filter design*).

The phase current is generated by the interaction between the mains phase voltage and the 1st harmonic of the formed bridge voltage (u_A, u_B, u_C). The δ angle is negligible since L is small (due to *high* f_{sw}).

$$\begin{cases} i_A = \frac{u_A - v_{\bar{A}_{LF}}}{j\omega L} \\ i_B = \frac{u_B - v_{\bar{B}_{LF}}}{j\omega L} \\ i_C = \frac{u_C - v_{\bar{C}_{LF}}}{j\omega L} \end{cases} \tag{1.12}$$

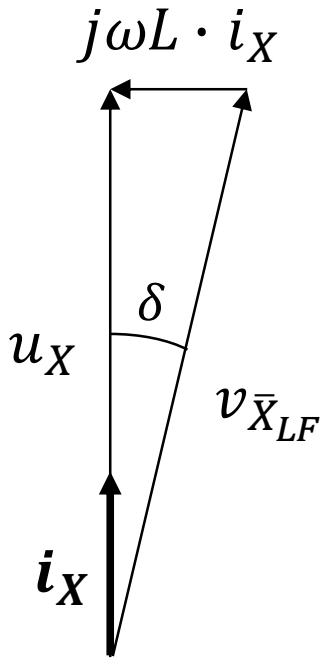


Fig. 28: Vector illustration of phase currents.

The LF common mode voltage ($v_{0_{LF}}$) is used in usual regulation operations (extension of the modulation range, DC-link mid-point voltage balancing, switching loss minimization, etc.) but at the same time it generates a switching frequency common-mode current ripple that is a unique issue for interleaved converter, known as *circulation current* $i_{CM_{HF}}$.

1.4 Mid-point balancing

[5] Interleaving two sub-converters brings unwanted circulating current into the system. Circulating current is the current produced by LF differential mode voltage ($v_M{}^{LF}$), calculated as the difference between interleaved phases (called V_+ and V_- in figure 29).
In accordance with figure 21, the current flowing through input boost inductor is defined as $2I_A$. In both interconnected sub-converter, each complementary phase is crossed by currents I_{A1}, I_{A2}. If the system had been ideal, the magnitude of those currents would have been equal for both phases, thus

$$I_{A1} = I_{A2} = I_A \tag{1.13}$$

Because the circulating current would have been null. In real system, is necessary to assume

$$\begin{cases} I_{A1} = I_A - I_{circ} \\ I_{A2} = I_A + I_{circ} \end{cases} \tag{1.14}$$

Then, the system results to be inherently unbalanced. The *circulating current* is highlighted as the halved-difference between the two phase currents.

$$\boldsymbol{I_{circ} = \frac{1}{2}(I_{A2} - I_{A1})} \tag{1.15}$$

[5] For example, if point A_1 is clamped to positive rail by diode D_1 and A_2 is connected to middle point of DC-bus by S_3 and S_4 (coloured in green in figure 21), the voltage difference between A_1 and A_2 will generate the circulating current within the two phases. If the impedance between the two points is not large enough, the circulating current will not only create additional conduction loss and HF disturbances emission but also impede the functionality of the converter. In extremal unbalanced situations, when I_A is positive, point A1 should be clamped to either positive rail by D_1 or middle point of DC bus by S_1 and S_2. However, if I_{cir} is so high that $I_{A1} = I_A - I_{cir} < 0$, point A_1 will not be able to be connected to positive rail when S_1 and S_2 are off, instead, it will be clamped to negative rail, resulting in *false modulation*. In conclusion, circulating current in interleaved current-commutated converters should be well controlled (it has to be the lowest possible, in ideal system, it should be null). Anyway, in real interleaved converters, the voltage difference between the two points A_1 and A_2 is inevitable.
A practical way to attenuate the circulating current would be to increase the impedance between the two interleaved points A_1 and A_2 (or others) at frequencies close to switching frequency. Adding *coupled inductors (inter-phase inductors)* between interleaved phases (like L_{MA} for phase A_1 and A_2 in figure 21) can effectively increase the impedance of the

circulating loop, while keeping minor influence on the common current (I_A). However, the use of inter-phase inductors could lead to a global increase in terms of cost (more components necessary) and losses. Moreover, design of the inter-phase inductors has not been explicitly described in any literature yet. For these reasons, it is preferred not to use inter-phase inductors and rather to search for specific modulation strategies to manage the circulating current to zero. An example of a suited modulation technique is *Zero-Mid-Point-Current* modulation (that permits to reduce to minimum the mean value of circulating current, even to zero if the system is studied under ideal switching hypothesis). For a comprehensive description of this and other modulation techniques cited in this paper, the reader should move to paragraph 1.5.

The circulation current issue is directly connected with *mid-point balancing*. In fact, it is to note that, referring to figure 29, the current i_P, i_N and i_M are tied together by the Kirchhoff's current law applied to point M.

$$i_P + i_N + i_M = 0 \tag{1.16}$$

In this way, the voltage difference between positive and negative voltages (V_+ and V_-) of the split DC-link may be expressed through the mid-point current in the Laplace's domain as:

$$v_M(s) = [V_+ - V_-](s) = \frac{1}{sC_{dc}}(i_P + i_N) = -\frac{i_M}{sC_{dc}} \tag{1.17}$$

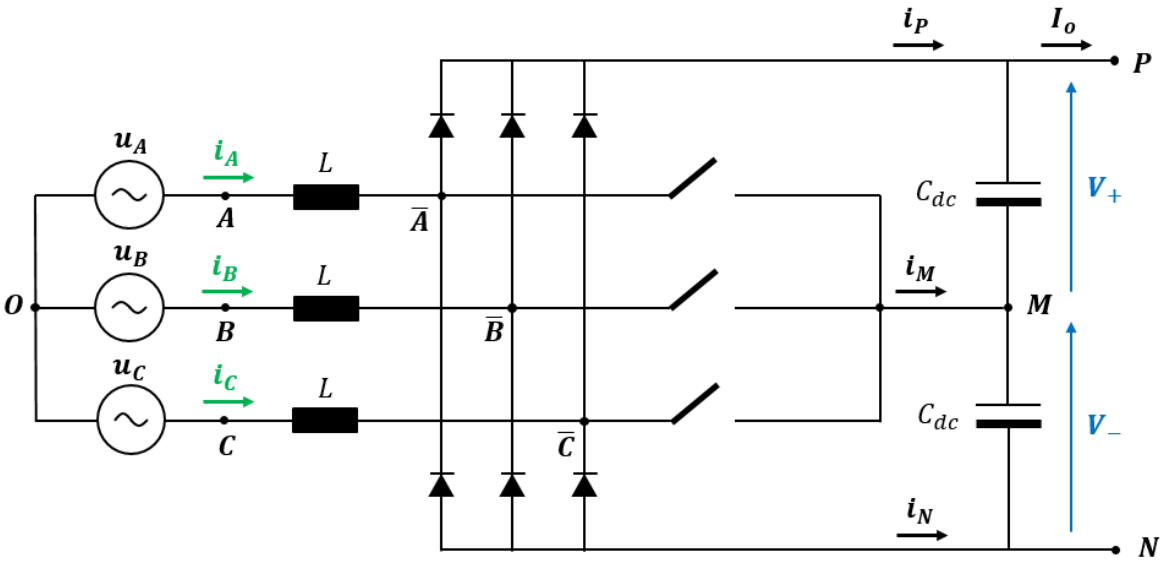


Fig. 29: AFE overview.

In other words, the mid-point current causes a voltage unbalance at the output of the AC/DC stage. Theoretically, the two output DC-link capacitors in series should split the output voltage in two

equal parts (i.e.$\frac{V_{dc}}{2}$). Nevertheless, in real working conditions not only the non-null circulating current but also other factors could lead to a global voltage unbalance for the system, for example:

- physical difference between the two capacitors ($C_{dc+} \neq C_{dc-}$);
- mains-side voltage unbalance;
- different switching dead-times between bridge legs;
- load unbalance on the DC-link side.

Two voltage control loops must be realized to provide an efficient converter voltage control: **the first one which regulates the full V_{dc} output voltage** (i.e. by regulating the input power) and **the second one which controls the voltage difference between the two capacitors to zero** (i.e. by means of a suitable common-mode voltage injection). It is to note that, the first voltage loop acts at the main period (50 or 60 Hz, for UE or USA grid), while the second it is to intend as a *third harmonic voltage control*. Thus, a couple of relations may be verified by the control instantaneously:

$$\begin{cases} V_+ + V_- = V_{dc} \\ V_+ - V_- = v_M = 0 \end{cases} \tag{1.18}$$

Considering all the possible state for the structure (figure 30), the redundant states $(\boldsymbol{P}, \boldsymbol{M}, \boldsymbol{M})$ and $(\boldsymbol{M}, \boldsymbol{N}, \boldsymbol{N})$ (they represent the same voltage vector) can be used to balance the mid-point current, by time partitioning the two intervals (state duration).

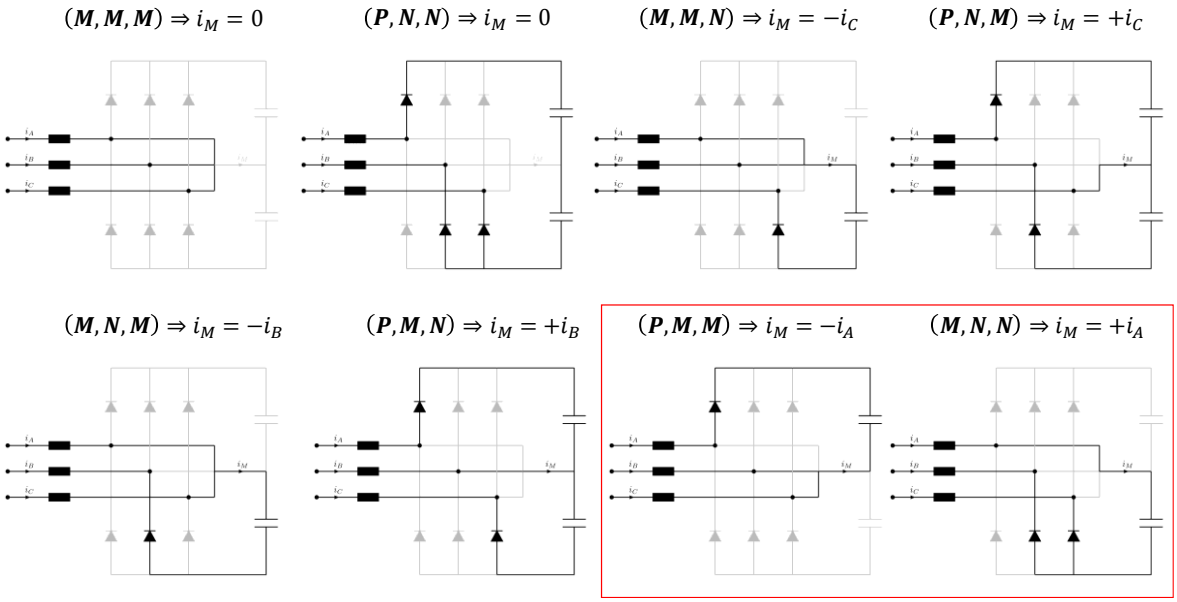


Fig. 30: AFE possible switch states.

There is a strict correlation between the time partitioning of the redundant space vectors (SVM control) and the third-harmonic common-mode voltage injection (PWM control). By defining, (α_A, α_B, α_C) as the *relative ON-times of bridge leg switches*:

$$\begin{cases} \alpha_A = 1 - \frac{\left|v_{\bar{A}M_{LF}}\right|}{V_{dc}/2} \\ \alpha_B = 1 - \frac{\left|v_{\bar{B}M_{LF}}\right|}{V_{dc}/2} \\ \alpha_C = 1 - \frac{\left|v_{\bar{C}M_{LF}}\right|}{V_{dc}/2} \end{cases} \tag{1.19}$$

Assuming that $v_{\bar{X}M_{LF}} = v_{\bar{X}_{LF}} + v_{0_{LF}}$ (and $x = A, B, C$) it will be

$$i_M = \alpha_A \cdot i_A + \alpha_B \cdot i_B + \alpha_C \cdot i_C \tag{1.20}$$

Formula 1.20 demonstrates the fact that the mid-point current local average i_M depends on the common-mode voltage component $v_{\bar{X}M_{LF}}$ (where $\bar{X} = \{\bar{A}, \bar{B}, \bar{C}\}$. Consequently, also the i_M waveform varies depending on the modulation technique used to achieve a certain common mode voltage (PWMC, DPWMC, CSVM or ZMPC). Due to the common-mode voltage limits, also the mid-current regulation is limited. Finally, 1.21 and 1.22 formulas state this dependency.

$$\begin{cases} \boldsymbol{i_{M,max}} = -\frac{1}{V_{dc}/2} \cdot \left(\left(v_{\bar{A}_{LF}} + v_{0_{max}}\right) \cdot |i_A| + \left(v_{\bar{B}_{LF}} + v_{0_{max}}\right) \cdot |i_B| + \left(v_{\bar{C}_{LF}} + v_{0_{max}}\right) \cdot |i_C| \right) \\ \boldsymbol{i_{M,min}} = -\frac{1}{V_{dc}/2} \cdot \left(\left(v_{\bar{A}_{LF}} + v_{0_{min}}\right) \cdot |i_A| + \left(v_{\bar{B}_{LF}} + v_{0_{min}}\right) \cdot |i_B| + \left(v_{\bar{C}_{LF}} + v_{0_{min}}\right) \cdot |i_C| \right) \end{cases}$$

(1.21, 1.22)

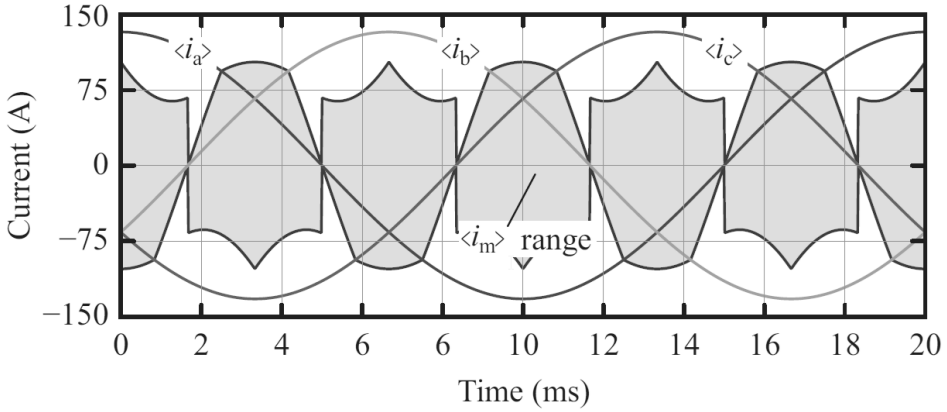


Fig. 31: Maximum instantaneous range of i_M.

In conclusion, the output voltage balance is inherently limited by the mid-point current restrictions (could become more difficult as voltage magnitude increases).

1.5 Modulation strategies

A variety of different modulation techniques have been presented in literature about 2-levels and 3-levels converters control. The modulation technique largely defines the generated harmonic content of voltages and currents, making this aspect of the project of the converter a key point that must be studied in depth; thus, depending on the application, there will be a modulation technique more suitable than others. All modulation schemes applicable to 2-levels rectifiers can be applied to interleaved or multi-level converters since any sub-unit can generate their outputs independently.

A primal characterization concerns *continuous* and *discontinuous modulation techniques*. In continuous technique each phase modulation index m_f, with f = {a, b, c} (or duties d_A, d_B, d_C), varies with continuity instantaneously, while in discontinuous techniques, for a certain interval of time (or exactly, phase), one or more phase indexes result to be clamped to the to the upper and lower DC-link rails (both or singularly). In this way, discontinuous techniques avoid switching around the maxima [5] (because the clamping happens when the phase current results close to its maximum value) but they are not suited for i_M control.

Consequently, discontinuous techniques are chosen if the purpose of control is oriented to switching loss reduction, while continuous one are preferred in terms of performance (ripple reduction), flexibility, and high frequency component attenuation.

In this paper, 4 different techniques will be presented:

- *Space Vector PWM (SVPWM)*, where the common-mode voltage v_0 is the one obtained by the standard space-vector approach (PWM compute as in 2-levels converter);
- *Discontinuous PWM with 30° Upper/Lower Clamping (DPWM4)* in which each phase is alternatively clamped to the upper and lower DC-link rails, each for 30°;
- *Three Level SVPWM (TLSVPWM or simply CSVM, continuous space vector modulation)*, in which the duty calculation works in a continuous manner in all phases (PWM compute for 3-levels converters);
- *Zero Mid-Point Current PWM (ZMPCPWM)*, in which the modulation strategies is wholly oriented to mid-point current magnitude minimization.

Next paragraphs will explain in a comprehensive way the main features of those techniques, considering phase voltages, common-mode voltage injection, duties waveform and grid current harmonic content.

In a 3-levels AC/DC converter *the only state that can be controlled is the M state*. In fact, P and N states represents respectively the upper and lower rails connection, which work like in a 2-levels rectifier (thus they reach the output voltage of ±½V_{dc}, respectively). The control function of the entire converter is $s = (s_A, s_B, s_C)$ is then calculated with the use of a *3-levels PWM modulation*, implemented in a logical way only with the use of a Boolean algorithm. In a 3-levels PWM are used two carriers (one called as low carrier c_L and the other as high carrier c_H)

$$\begin{cases} d(t) > c_H(t) \rightarrow P\ state \rightarrow v(t) = V_{dc} \\ c_L(t) < d(t) < c_H(t) \rightarrow M\ state \rightarrow v(t) = 0 \\ d(t) < c_L(t) \rightarrow N\ state \rightarrow v(t) = -V_{dc} \end{cases} \quad (1.23)$$

Thus, the t-Type M switch is enabled (ON) while the duty cycle of a certain phase x is inside the low and high carriers. In this case the output voltage is equal to zero. In a similar way, the output voltage is equal to (-V_{dc}) and the transistor is disabled (OFF) if the duty is beneath both carriers (otherwise, is equal to V_{dc} if the duty stays over both carriers). Duty cycles are expressed analytically through (1.24) formula (where the x = {a, b, c} as usually).

$$d_x = \frac{1}{2} + \frac{v_x + v_0}{V_{dc}} \quad (1.24)$$

Figure 33 displays considerations shown by 1.21 (valid for any modulation technique).

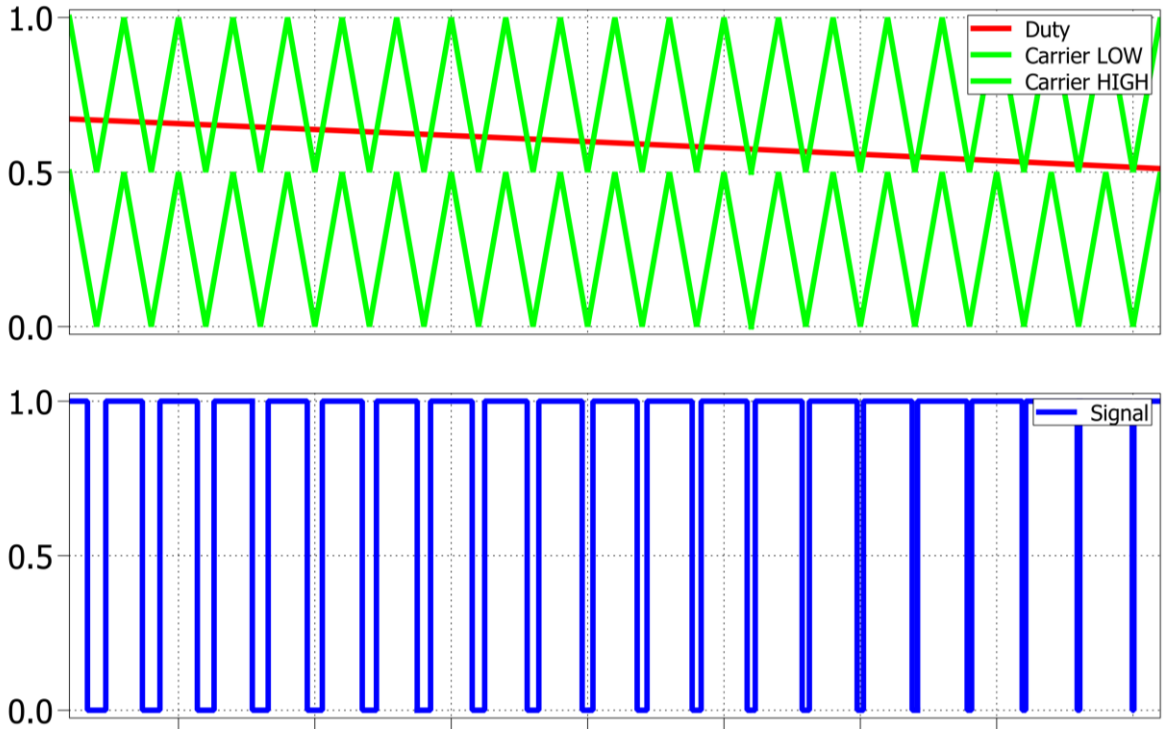


Fig. 32: Example of 3-levels PWM modulation.

Thus, the logical control of mid-point switches could be rewrite in a simple way as follow

$$\begin{cases} s_x = 0 \; if \; (d_x \geq c_H) \; or \; (d_x \leq c_L) \\ s_x = 1 \; if \; (d_x < c_H) \; and \; (d_x > c_L) \end{cases} \tag{1.25}$$

The BEM (balanced enveloped modulation) can be implemented also in a 3-levels converters. In this way, it is possible to guarantee the best voltage usage of the converter, since the balancing of positive and negative envelops permits to over-modulate the output voltage (accordingly, $m_{max,notmodulated} = 1$ and $m_{max,BEM} = 2/\sqrt{3} \approx 1{,}15$) without distortions when working in non-linearity conditions (thus, between 1 and $2/\sqrt{3}$). The next figure shows the waveforms of the duties in both circumstances.

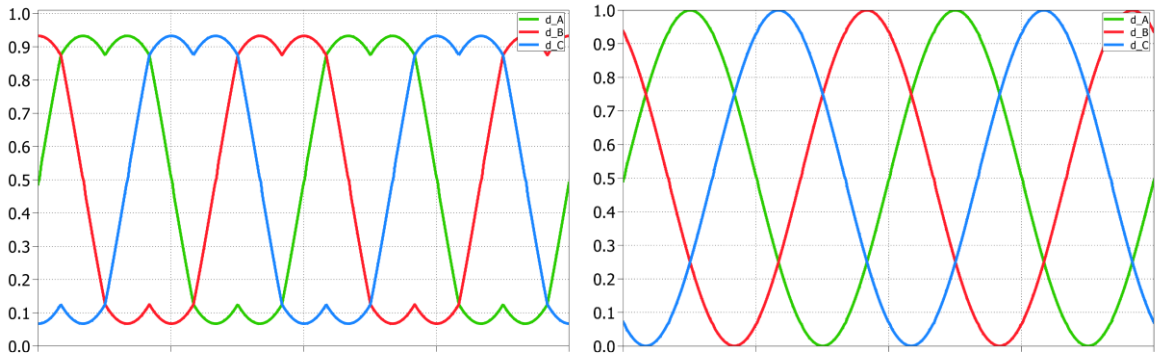


Fig. 33: Duties comparison with disabled or enabled BEM.

In conclusion, the control routine for duty generation is reported in the appendix A1.

1.5.1 Space Vector Modulation (SVPWM)

The PWMCompute function is used to calculate abc duty-cycles starting from phase voltages reference. It is the easiest technique which permits to apply BEM to the output voltages. In practical, the control algorithm works as in a 2-levels converter.

However, it is necessary in any case to evaluate exactly the *voltage zero sequence* v_{zs} (called v_o in the code, appendix A2). Consequently, the duties are distorted by the control to achieve the increase of the output voltage with a proper common mode addition (v_{zs}). The v_{zs} can be obtained in many manners: in the code it is half of the medium voltage of the abc triad (then it is necessary to provide to an adequate sorting algorithm).

$$v_0^{LF} = v_{zs} = -\frac{1}{2}(EN_n + EP_n) \tag{1.26}$$

EN_n and EP_n are the non-modulated positive and negative voltage envelops (instantaneous max and min voltages of the triad abc). The following figure shows the periodic average of expected waveforms using this technique.

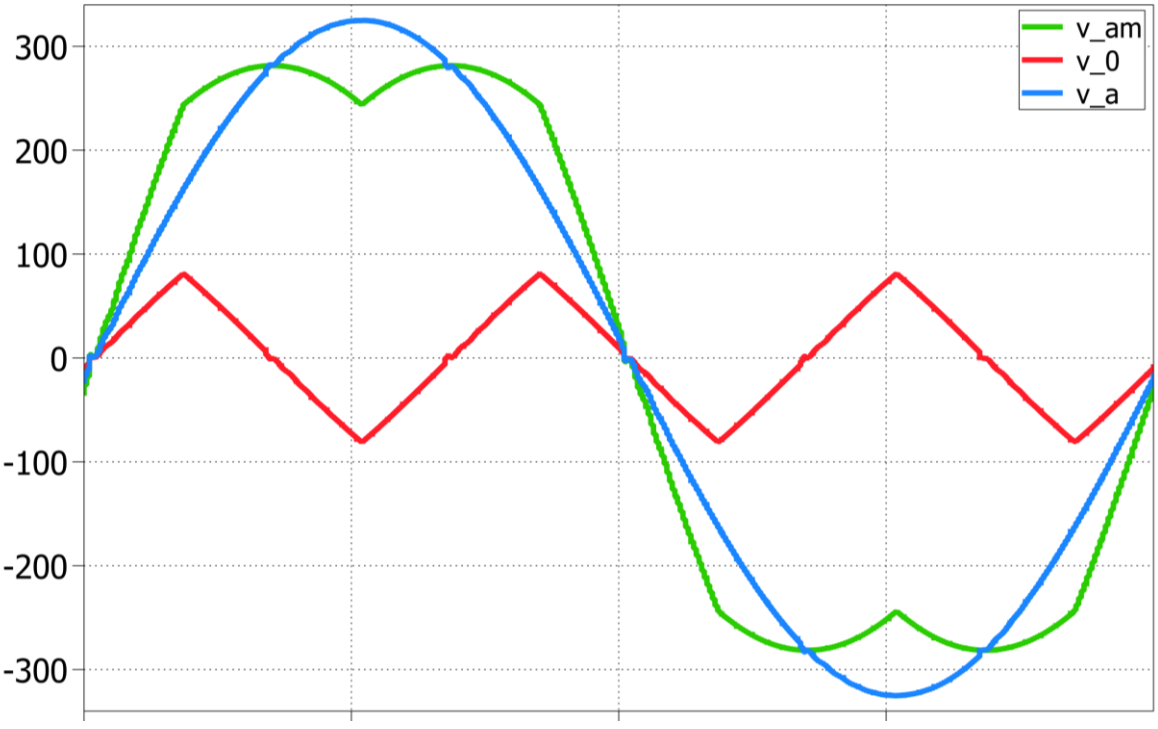


Fig. 34: Expected waveforms with PWMCompute.

A comparison may be relevant, between SPWM (sinusoidal PWM, in which no voltage common mode is injected) and Space Vector PWM Computation (PWMC) already described. As shown in figure 33, the former has high quality of the output waveform, but the more switching frequency increase the more switching losses become relevant, and in

any case it has low utilization of DC voltage. On the contrary, the latter can get better output voltage waveform with not very high switching frequency, and maintaining a higher utilization rates of DC voltage. In addition, SVPWM together with inter-leaving paralleled technology would be a better method to mitigate the circulation current.
In conclusion, is reported in the Appendix A2 the code implemented to run PWMCompute technique.

1.5.2 Discontinuous PWM with 30° Upper/Lower Clamping (DPWM4)

The crucial point of discontinuous PWM modulation strategies regards the reduction of switching loss of the converter. As presented in article [4], the turn-on loss energy for a single conversion unit (switch and diode) can be expressed through the following formula:

$$E_{turn-ON} = \frac{1}{2} V_{out} I_{load} \Delta t_{turn-ON} + \frac{1}{2} V_{out} Q_{diode} \tag{1.27}$$

In the last formula (1.23), it is assumed that:

- V_{out} is the DC bus voltage;
- I_{load} is the current absorbed by the load (different load currents could lead to different turn-ON energy);
- Q_{diode} is the total capacitive charge of the junction capacitor of the fast diodes, which could be found in datasheet of the diodes (it could be consider negligible using Schottky SiC diodes). It is to note that diodes with higher current capability ($I_{MAX,rated}$) have higher Q_{diode} (that means at the same time higher switching loss);

The expression of turn-OFF energy is not reported in this paper (but it results to be quite similar to 1.27). The discontinuous PWM technique are then oriented to reducing of switching loss without reducing the switching frequency f_{sw}, through the reduction of the numbers of commutation per period of switching (2 per 3 switches, thus 6 commutations). Consequently, discontinuous techniques have to work in a trivial way: the output phase with the momentary highest current is not switched over a fixed electrical angle (30°, 60° or 120°) and it remains clamped to the maximum voltage value permitted, that is the DC-link rail voltage (positive or negative, as appropriate). This keeps a significant reduction of switching losses but could lead to an increasing mains current ripple (constraining to use bigger filter). [5] To achieve phase clamping, for example, in area 1 (figure 23), vector [p n n], [p n m] and [p m m] are selected for the lower part, while vector [p m m], [p m n] and [p n n] are selected

for the upper part. These selections ensure that phase *A* is clamped to positive rail when the desired output voltage vector is in area 1. It is worth noting that, in area 1, current in phase *A* is close to its maxima. In area 2, vector [p m m], [p m n] and [m m n] are selected to ensure phase B is clamped to middle point, where current in phase B crosses zero. Thus, this scheme not only avoids switching around the maxima but also avoids switching around zero crossing of associated phase current. The last phenomenon is caused by O_p and O_n states overlapping within the interleaved structure. A suitable discontinuous modulation technique should be oriented to avoid zero overlapping through the elimination of one zero state ([n n n] or [p p p], as reported in [4]). For example, a 30° DPWM technique (DPWM4) for lower and upper 30° phase rail clamping, can be implemented as described in appendix A3.

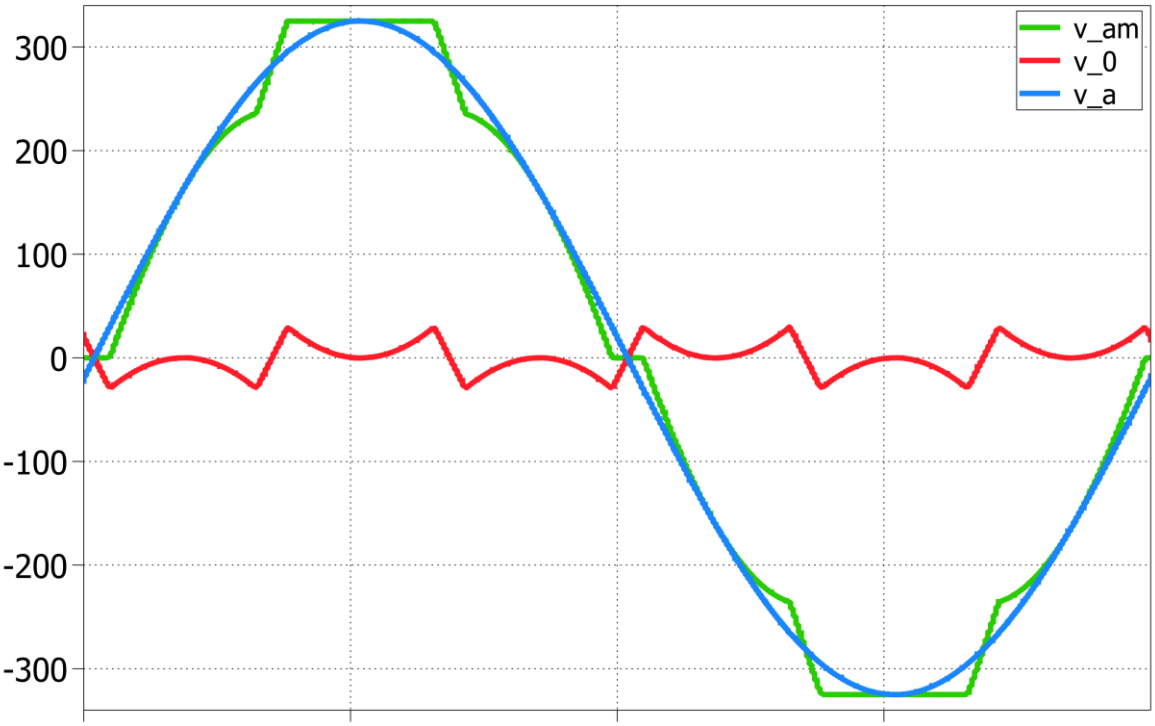


Fig. 35: DPWM4 expected waveforms.

1.5.3 Three levels Space Vector PWM (TLSVPWMC)

In TLSVPWMC (3-levels Space Vector Pulse Width Modulation Compute or simply continuous space vector modulation, CSVM) technique the v_{zs} component is obtained in a similar way of SVPWM (using a sorting algorithm) but in this case all phases contribute simultaneously to common mode calculation. In addition, an ulterior voltage common mode component (called v_shift in the code) is used to duty calculation, defined as follow:

$$v_{shift} = \frac{1}{2} \cdot [V_{dc} - (EP_n + EN_n)] \tag{1.28}$$

EP_n and EN_n are also in this case the instantaneous maximum and minimum value of phase voltages of the triad abc (not modulated). Then, the modulated voltages, v_a, v_b, v_c are calculated through the use of *fmod* function which returns the floating-point remainder of *numerator*/*denominator* (rounded towards zero). Assuming that u_a, u_b, u_c are the initial voltage value (not shifted), the modulated voltages (shifted), are calculated analytically as follow:

$$\begin{cases} v_a = fmod\left[\left(u_a + v_{shift}\right), \left({}^{1}/_{2} \cdot V_{dc}\right)\right] \\ v_b = fmod\left[\left(u_b + v_{shift}\right), \left({}^{1}/_{2} \cdot V_{dc}\right)\right] \\ v_c = fmod\left[\left(u_c + v_{shift}\right), \left({}^{1}/_{2} \cdot V_{dc}\right)\right] \end{cases} \tag{1.29}$$

The sorting procedure starts like in SVPWM and EP_m and EN_m are calculated (were EP_m and EN_m stand for the positive and negative envelop of modulated voltages v_a, v_b, v_c); then, duties are evaluated with the use of a new v_{zs} defined as:

$$v_{zs} = -\frac{1}{2} \cdot (EP_n + EN_n) - \frac{1}{2} \cdot (EP_m + EN_m) + \frac{1}{4} \cdot V_{dc} \tag{1.30}$$

The last formula (1.30) demonstrated that all phases are used by this modulation strategy for v_{zs} calculation, resulting finally in an overall improving of voltage output quality for the load with respect to the simple SVPWM compute for 2-levels converters described in paragraph 1.5.1.

The next figure shows the expected waveform for CSVM technique.

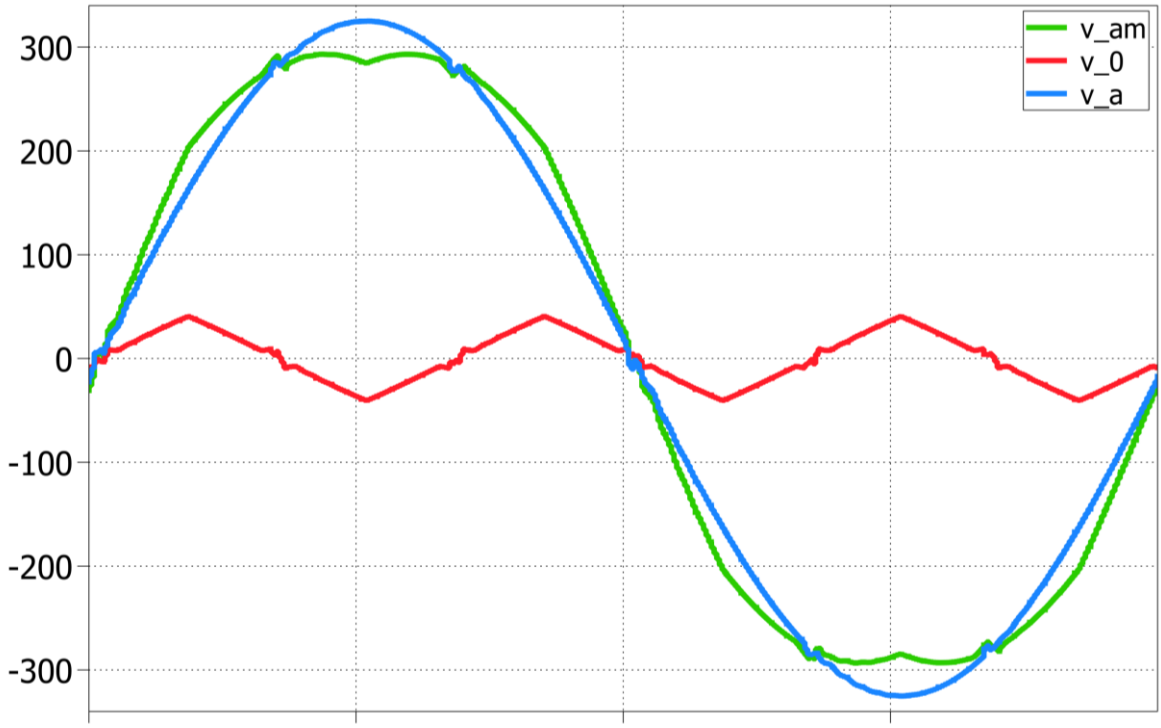


Fig. 36: CSVM expected waveforms.

Finally, the appendix A4 shows an example of code to implement CSVM.

1.5.4 Zero Mid-Point Current PWM (ZMPCPWM)

Nevertheless multi-level and parallel converters are effective methods for enhancing both the voltage and current capacity and the performances of a power electronic converter, putting modules in parallel is not risk free.

Zero Mid-Point Current PWM is the most appropriate modulation technique for AFE interleaved converters. [4] In fact, one of the major concerns for the parallel operation of a three-phase interleaved system is the *cross-coupling* between the three-phase system parallel modules. For example, when each module of a converter, in a certain switching state, is connected contemporaneously to the same DC bus and to a common power supply or load, a privileged path for circulating current may occurs (cross coupling effect). In order to avoid this problem, the traditional method is to use an isolation transformer. However, the use of transformer will undoubtedly increase the size and cost of the entire system, especially in high power and low switching frequency occasions, where this problem results prominent.

Therefore, the circulating current result to be generated from the difference of voltage between two analogous points of the same phase of the two (or more) interleaved units. The expected waveform of circulating current is then associated to the state of 2 coupled switches of 3 belonging to a single 3-phase module.

The main disadvantages related to the circulating current issue regard:

- *increasing of passive component dimensions* (the size of boost and filter inductors increases in comparison with ideal condition in which there is not any circulating current effect);
- in extremal unbalanced systems the circulating current issue could even lead to a whole *impossibility of control* (false modulation);

A winning way to deal with circulating current without using further hardware components is to manage an adequate common mode voltage v_0^{LF} to obtain the minimum mean value of i_M. The ZMPC modulation strategy is used to achieve this result. It guarantees a variety of advantages:

- reduction of flux ripple $\Delta\Psi_{pp}$ on the boost inductance;
- reduction of peak value of circulating current i_M (that is in any circumstance a zero mean value waveform);
- reduction of RMS value of capacitor current of the split DC-link;
- reduction of THD and TDD of the current absorbed from the grid.

As a consequence, the ZMPC is suitable for optimal hardware design project and it represents a consistent and robust solution to manage mid-point balancing in interleaved multi-level converters. The following figure shows the expected waveforms of phase and common mode voltages generated with ZMPC technique. In addition, a code example for ZMPC implementation is described in appendix A5.

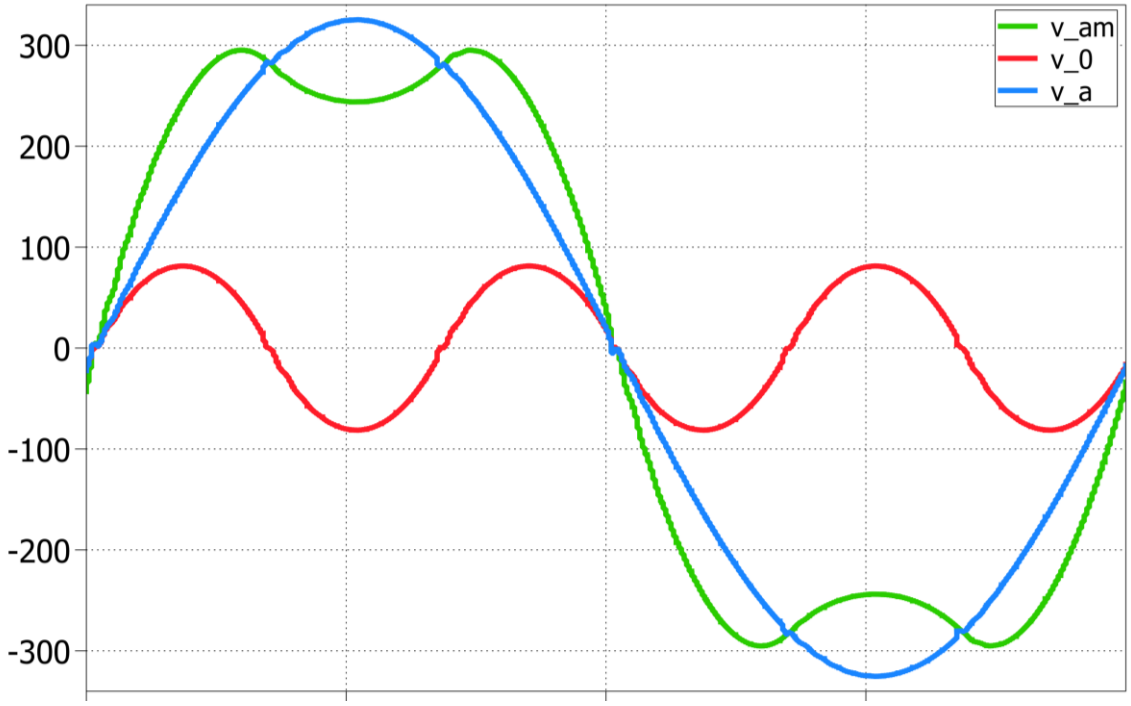


Fig. 37: ZMPC expected waveforms.

The common mode voltage v_0 results to be a purely 3th harmonic waveform, with null fundamental component. This leads to a magnitude reduction of the mid-point current, which in ideal conditions result even to be null. The phase medium-point voltage seems to follow a "helmet waveform" due to the fact that $v_{\bar{A}M} = v_{\bar{A}} + v_0$ (formula 1.11) and thus it depends on the common mode component (it decreases, with respect to the phase voltage, as v_0 decreases).

The following pictures (figure 38 and 39) display a comparison of mid-point current per modulation techniques in terms both of ripple and periodic average component (from left to right, left top PWMC, right top DPWM, left bottom ZMPC and finally right bottom CSVM).

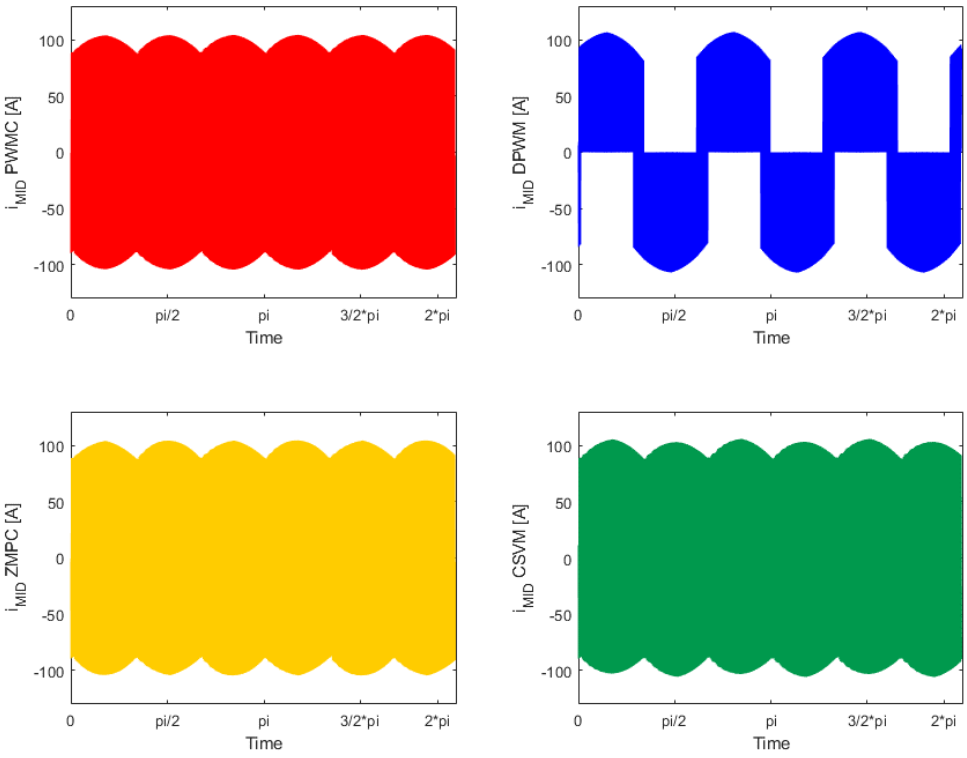


Fig. 38: i_M ripple component for different modulation techniques.

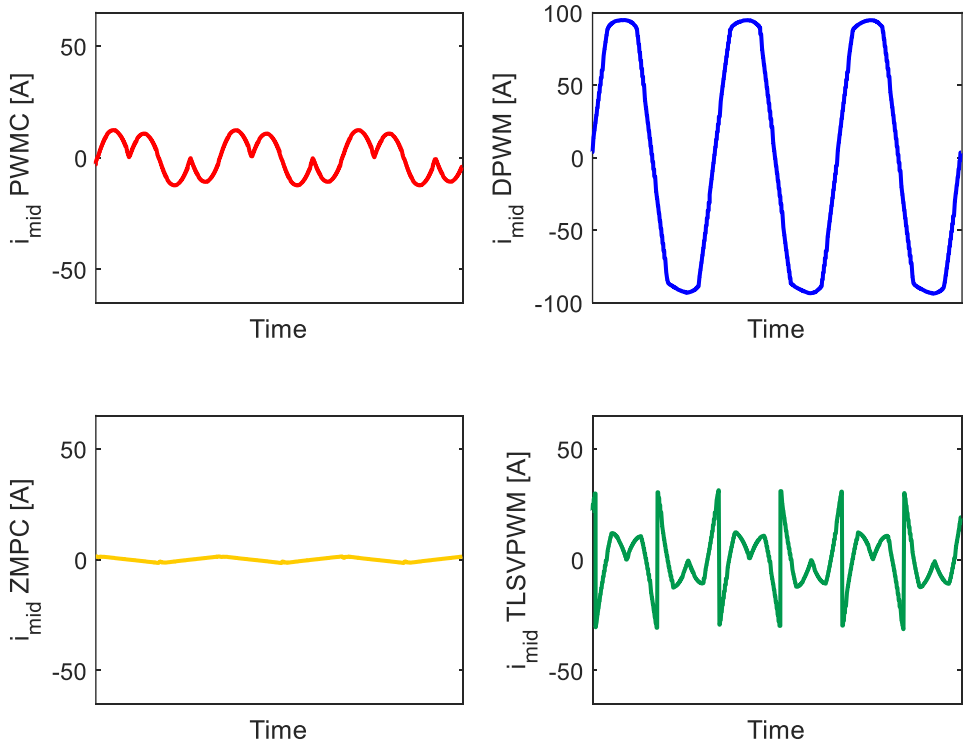


Fig. 39: i_M periodic average values for different modulation techniques.

1.5.5 Duty cycles comparison table

Finally, a comparison between different duty cycles generated with each modulation technique is reported in this paragraph. The expected waveform take in account of all phases of the triad abc (thus (d_A, d_B, d_C) as reported in in the following figures) of a single sub-converter unit and also the common mode index (called as d_0).

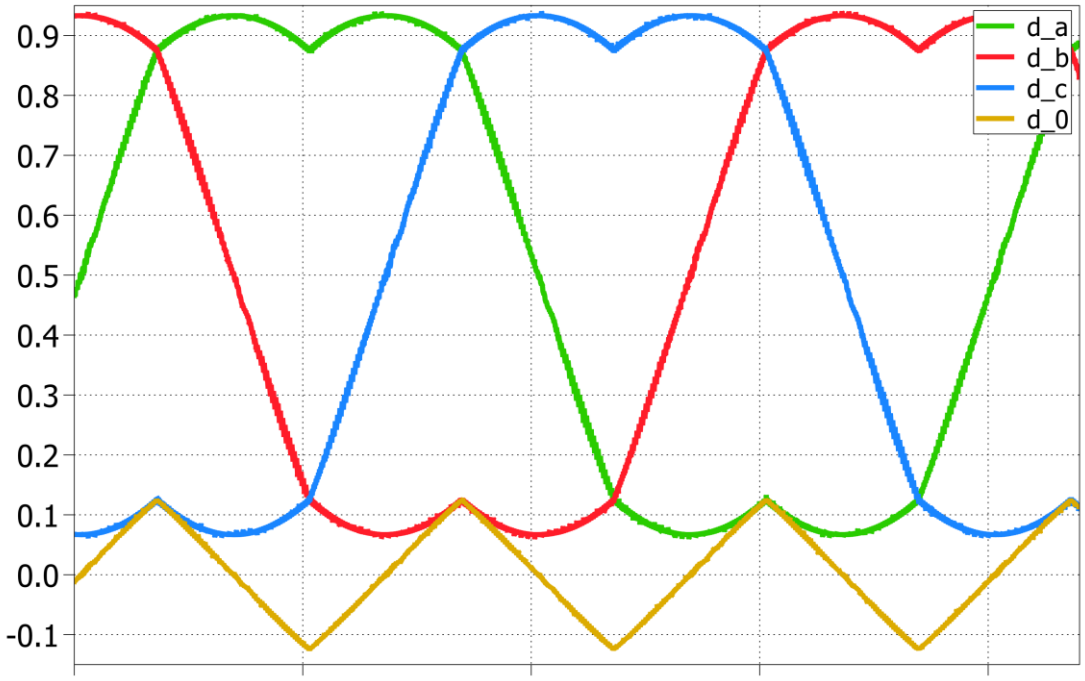


Fig. 40: PWMC duties.

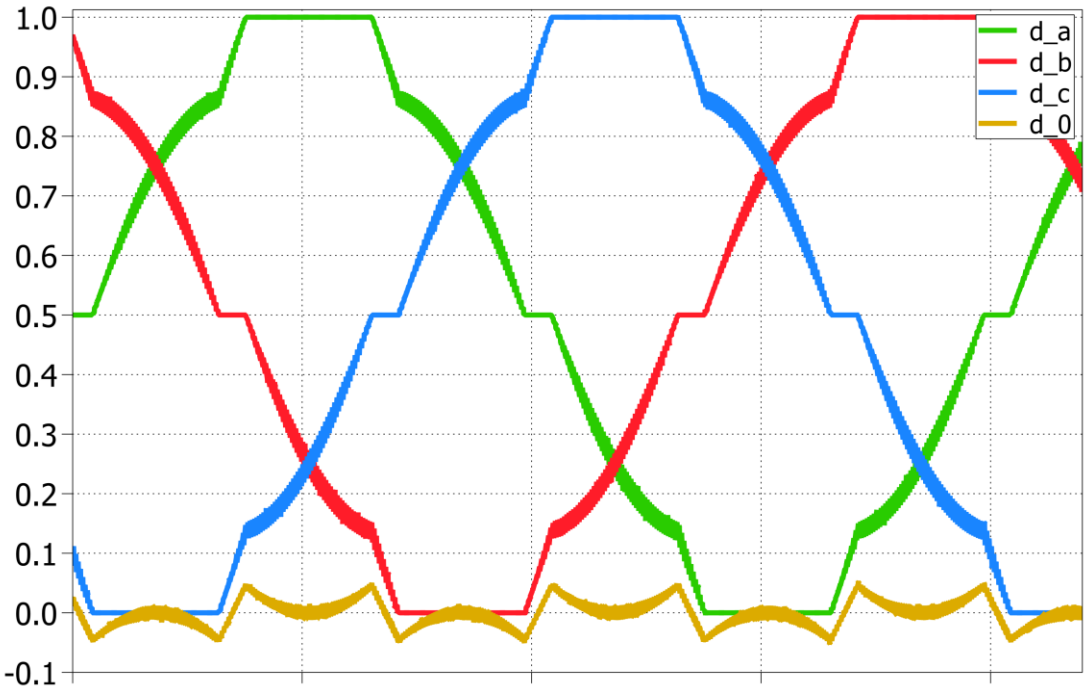


Fig. 41: DPWMC duties.

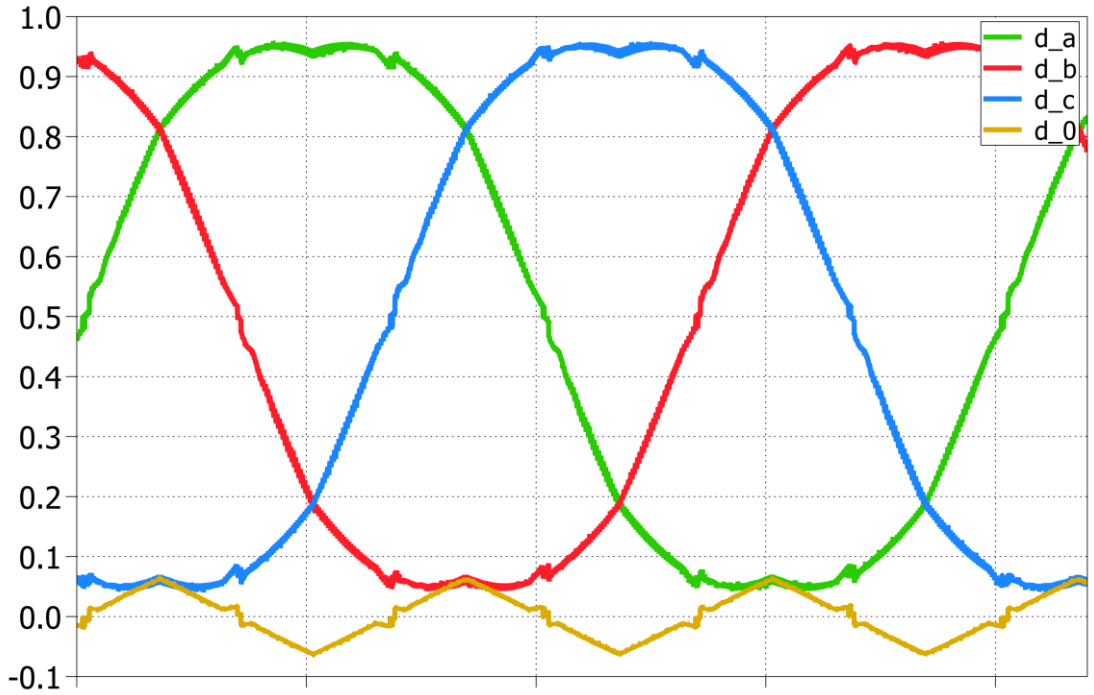


Fig. 42: CSVM duties.

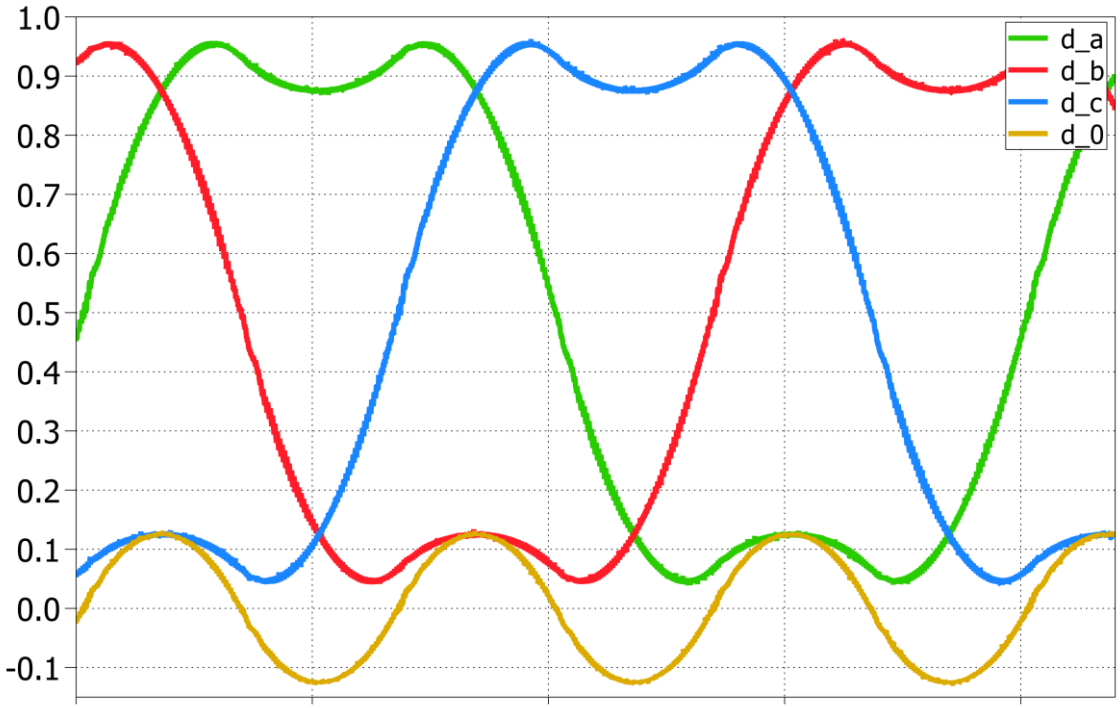


Fig. 43: ZMPC duties.

Duty d_0 represents the additional duty cycle contribute that is generated in order to achieve the proper ${v_0}^{LF}$ addition. Furthermore, the *total duty function* $d_{tot,X}$ is defined as follows:

$$\begin{cases} d_{tot,A} = d_A + d_0 \\ d_{tot,B} = d_B + d_0 \\ d_{tot,C} = d_C + d_0 \end{cases} \tag{1.31}$$

CHAPTER 2: SIMULATIVE RESULTS

2.1 Case study

The purpose of the thesis is to provide a comprehensive and systematic study about the project of the AC/DC stage of an ultrafast charger (UFC) for EV charging station applications. The project has been realized in association with "*Vishay Semiconductor Italia SPA"*. The whole charger consists in a *two stages back-to-back converter*, in which, the grid interface is a 3-levels active rectifier (AFE, downstream of a LCL filter for EM compatibility) while the load interface is a HF DC/DC converter (resonant LLC converter). The two stages are connected through a voltage DC-link providing voltage continuity for the load and protection for the converter from voltage dips and swells.

The simulation results have been prepared with the use of a proper Power Electronic software (PLECS) and the post-processing analysis with the use of MATLAB.

In particular, the target of the thesis regards both the evaluation of the most adequate modulation technique to use in order to control the device and the experimental test in HIL (hardware in the loop) ambient to validate the simulation results.

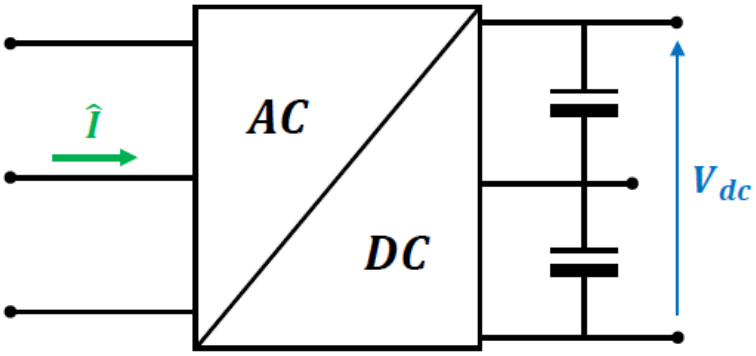


Fig. 44: Model of the AC/DC stage and voltage DC-link.

The entire charger consists in a charging station of 360 kW, made up of 6 charging units each one of 60 kW. This shrewdness leads to several advantages:

- it permits to regulate the output power request by the load in the most efficient way *(power sharing strategy)*;
- it has a *modular layout* (for example, in case of fault is sufficient to substitute a single unit instead of the whole converter);
- it guarantees a considerable flexibility in terms of switches and components to use within the converter (enabling to high current density purposes without too high level of voltage, so it is a *suitable solution also for LV application*).

A primal hypothesis to prepare an accurate model of the plant consist in assuming a *unitary power factor value*, that means, for a single unit of P = 60 kW

$$cos\varphi \cong 1 \; and \; S = \frac{P}{cos\varphi} \cong 60 \; kVA \; thus \begin{cases} V = V_n = 230 \; V \; (LV \; application) \\ I = \frac{2 \cdot S}{3 \cdot V} \cong 125 \; A \cong 88 \; A_{RMS} \end{cases} \quad (2.1)$$

This hypothesis is validated assuming that the AFE interface works correctly as an active rectifier, adjusting the output to maintain cosφ = 1 (a 0.5% of deviation is assumed as maximum). In addition, it is to note that the single module should carry 88 A_{RMS} of current by the use a single-module layout (not-interleaved). The output current peak value per module (I_{peak} = 125 A) results to be superior to the major low cost switches rated current. For this reason, the interleaved topology represents a valid technical expedient to halve the output current carried by each single module (with a striking reduction in terms of cost and losses). The output DC-link voltage V_{dc} has to be chosen carefully, considering:

- that the rectifier must be able to handle the peak input phase voltage (at least 325 V);
- the boost inductors stress increase with V_{dc};
- switching loss increases roughly with $\left({V_{dc}}^2\right)$;
- the DC-link capacitor volume increases with $\left({V_{dc}}^2\right)$.

Consequently, the V_{dc} *must be the lowest possible*. As reported in literature [7], using the ZMPC modulation technique, the V_{dc} voltage can be evaluated through the following formula (2.2):

$$V_{dc,min} = \frac{\frac{2}{\sqrt{3}}}{1.1} \cdot \sqrt{3 \cdot \left(V_{peak,max}\right)^2 + 3 \cdot \left[\omega \cdot L \cdot \left(I_{peak,max}\right)\right]^2} \cong \frac{2}{1.1} \cdot V_{peak,max} \quad (2.2)$$

Yields to

$$V_{dc,min} = \frac{2}{1.1} \cdot \sqrt{2} \cdot V_n \cong 591 \; V$$

Thus a V_{dc} of 800 V is assumed as a reference precautionary value (at least ±30% of margin).

$$\boldsymbol{V_{dc} = 800 \; V}$$

The main advantages of T-type interleaved topology regard:

- the single-leg current is reduced, allowing to use discrete semiconductor devices (not in parallel) and standard available cores for boost inductors;
- lower input phase current ripple (design of DM EMI filter);
- lower DC-link RMS current and charge ripple (design of DC-link capacitors).

The main drawbacks of T-type interleaved topology concern:

- higher boost inductor flux ripple (higher losses and/or greater size), binding to use ZMPC modulation technique to mitigate i_M current and reduce input current TDD (reducing in terms of ripple and increasing of the quality of the waveform);
- higher number of gate drivers and current sensors (for microcontroller routine);
- higher control complexity;
- both diodes (D_p and D_n) for upper and lower DC-link rail connection must be fast diodes and they must guarantee a rated voltage of V_{dc}.

The final layout of the converter is depicted in the following figure.

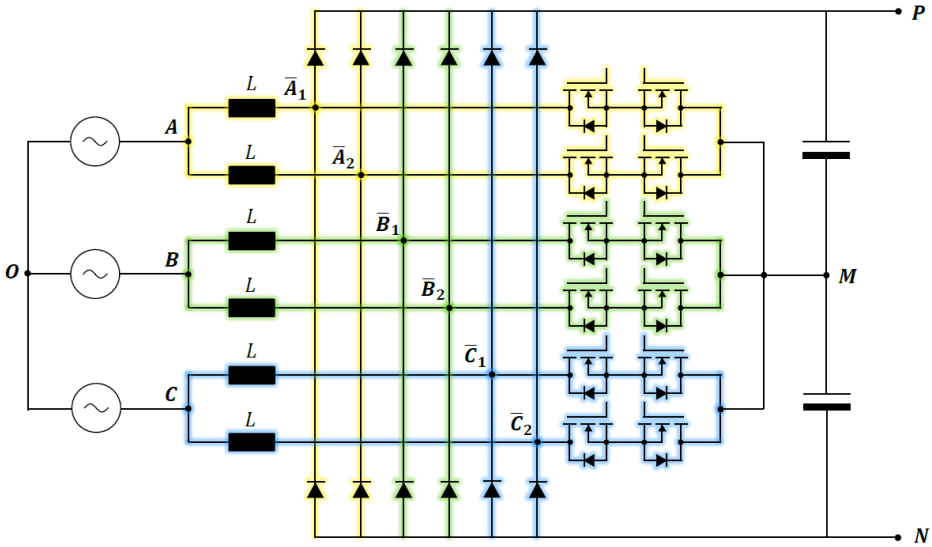


Fig. 45: Final model of the interleaved T-type rectifier.

[7] The control of the converter (whatever the number of levels it is) can be realized through the PWM method. When a 3-levels converter is used, a 2 carriers based PWM method is leveraged for controlling purposes. As a consequence, the expected output voltage waveforms on the load must be composed both by harmonics stemming from the PWM carriers and reference waveforms (these harmonics are clear shown through Fourier's series expansion). Nevertheless, if a standard 3-levels-3-phases system is considered, a certain degree of harmonic cancellation in the phase voltage is naturally obtained. In fact:

- *even order harmonics* are eliminated at the leg level, since half-wave symmetry is assumed;
- *odd carrier harmonics* are eliminated (since they are the same for every leg-applied voltage, the three phase system works indirectly as filter for that frequencies waveforms);

- *odd triple sideband harmonics* are eliminated (i.e. they are rotated by integer multiples of 2π, thus remaining the same for all leg-applied voltages). Harmonic sidebands consist of all the spectral components of the modulated input signal (or voltage in this case) except the carrier. All forms of modulation produce sidebands.

Figure 50 displays graphically the previous considerations about PWM harmonics cancellation for the highlighted family of frequencies (even, odd carrier harmonics, odd triple sideband harmonics). From left to right, it shows the phase to medium, the common mode voltage and the input phase voltages waveforms (considering instantaneous value in green, periodic average in red and Fourier expansion in the bottom graphs), that are tied together by the following formula (1.11).

$$v_{\bar{A}M}, v_0, v_A \rightarrow v_A = v_{\bar{A}M} - v_0$$

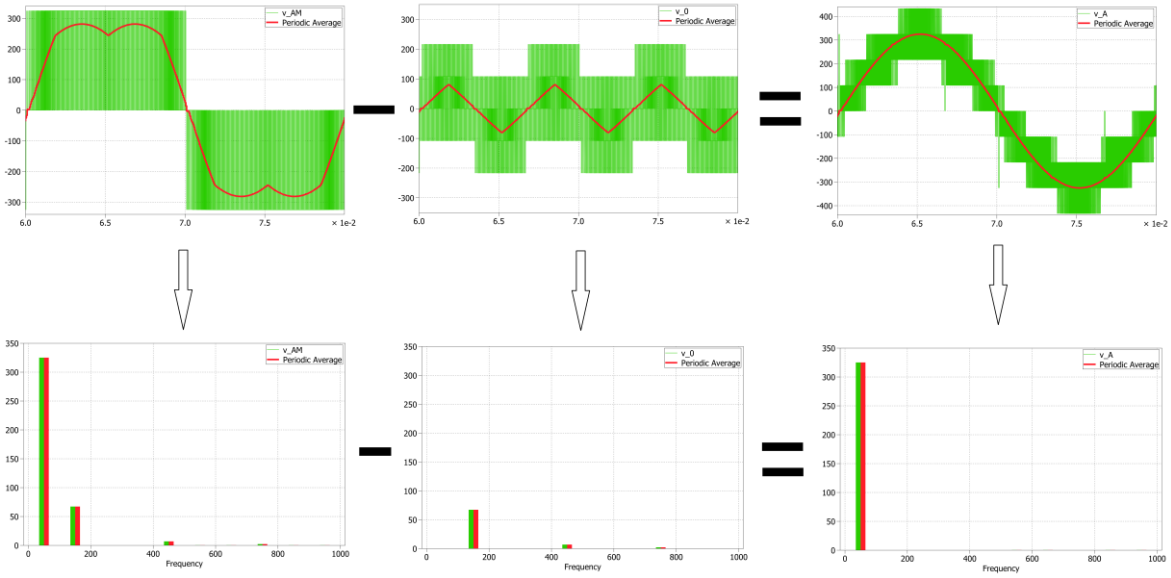


Fig. 46: Harmonic properties of voltages generated by a 3-levels T-type rectifier.

Another curious phenomena to observe (in voltage or current Fourier's series expansion) is the generation of high frequency modulation residuals at each even-integer-multiple of fsw. Indeed this phenomena becomes negligible since a correct LCL input filter design is tuned and the modulation generates only fundamental component of load current. Paragraph 2.2 is dedicated to hardware design (LCL tuning and reactive component sizing).

The previous phenomena affect the THD of absorbed current and it is worse (so it increases) as the magnitude of the load current decreases. Regulation allow to consider a waveform as sinusoidal if a lower than 5% of THD is reached. Thus, a low current request by the load could lead to an overall decrease of current quality (harmonic distortion becomes evident

especially among phase current zero crossing) or even in an impossibility of control, principally due to:

- impossibility of current reference synchronization for load current (control is not able to master low current operation);
- unidirectional behaviour of the AFE converter (it is an AC/DC rectifier composed by unidirectional components and it can be affected by DCM issue).

For these reasons, the use of 6 separated units (of 60 kW each one) is also a choice to increase the efficiency of AC/DC conversion, since, in low current operating mode, instead of working contemporaneously with all the units, it is possible to control only a part of them at max load (same module may be off). In this manner, a better quality current waveform is obtained in any working condition, since each unit of the charger works at high current reference values (even in cases of low load). In this sense, simulations focus on a minimum current request (worst case design) of 80% of the project $I_{ref,MAX}$.

The cause of *DCM (discontinuous conduction mode)* has to be searched in the AC/DC rectifier topology: AFE is a unidirectional converter and *DCM* results as a natural consequence of impossibility for the phase current to change direction due to semiconductors characteristics. The only current path allowed is the grid-converter one, not vice versa. Furthermore, no-load operations are forbidden for AFE, because T-type converter can only charge the DC-link and thus it cannot work with null magnitude current reference.

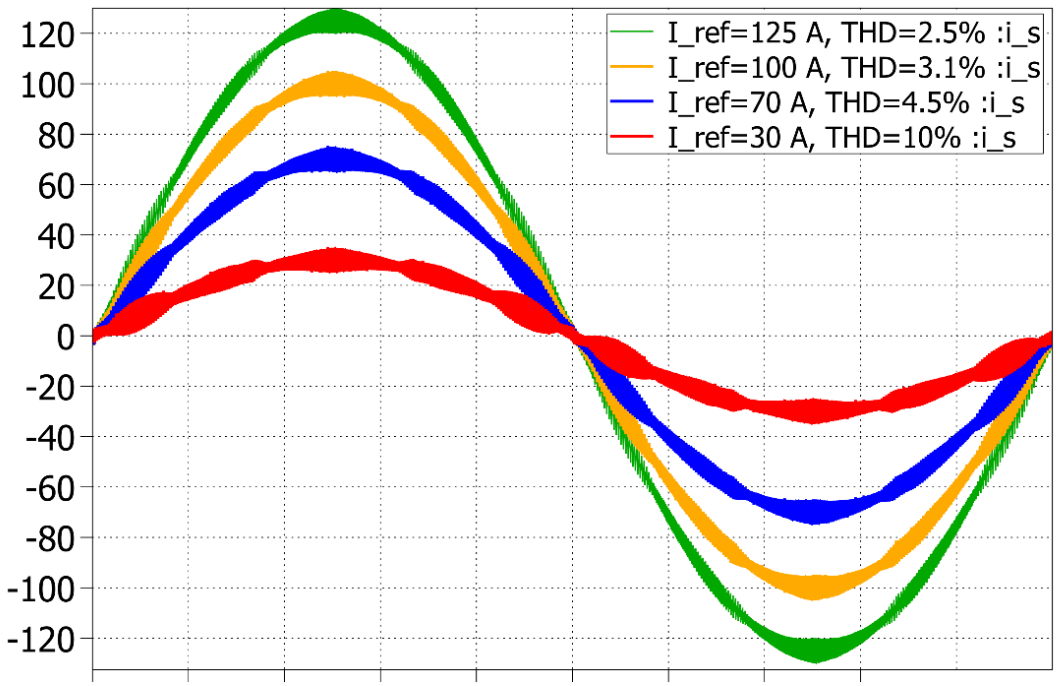


Fig. 47: Single phase source currents (i_s) for different current reference values.

With this brief summary, the introduction of the second chapter ends, highlighting the crucial point to investigate in order to realize an adequate control of the converter; they are:

- **mid-point balancing and circulating current (i_M) control;**
- **DC-link voltages control (both common and differential mode);**

2.2 Hardware design

The aim of this paragraph is to provide a concise report of hardware sizing of the converter. This seems necessary in order to justify the value to use to correct tune the LCL input filter, to calculate the bandwidth that is possible to obtain from the converter and the gains of the current and voltage loops, respectively.
In order to correctly design the converter passive components (inductors and capacitors) the following quantities, together with their parameter dependencies, must be identified:

- Boost inductor peak-to-peak flux ripple ($\Delta\Psi_{pp}$) and its RMS value ($\Delta\Psi_{RMS}$);
- DC-link RMS current ($I_{c,RMS}$);
- DC-link peak-to-peak charge ripple (ΔQ_{pp});

They depend on certain parameters that can be adjusted by the control to achieve the fittest hardware design; these parameters are:

- the phase shift angle between the two carriers ($\alpha_{PWM} = 0°\div180°$);
- the rectifier modulation index ($m = 0 \div 2/\sqrt{3}$);
- the modulation strategy (*PWMC, DPWM4, ZMPC, TLSVPWM*);
- the power factor angle at the rectifier input (for a simplified analysis the *unitary cosφ* hypothesis can be used).

In our simulative study the ZMPC modulation is used to permit mid-point current optimal control, thus only the changing due to α_{PWM} and m (by considering different value of V_{dc}) on flux ripple and capacitor current and charge are investigated in the following paragraphs.

Fig. 48: Aluminium electrolytic capacitor used in DC-link of AFE.

2.2.1 Interleaving layout and reactive components design

By paralleling an additional leg per phase, a degree of freedom is unlocked, since PWM carriers with a phase shift between them (α_{PWM}) may be adopted [7]. This degree of freedom may be leveraged to increase/decrease the following quantities:

- input *phase current ripple* (affects EMI filtering effort);
- individual leg *current and flux ripple* (affects boost inductor design);
- output *DC-link RMS current* (affects DC-link capacitor current rating and losses);
- output *DC-link charge ripple* (affects DC-link capacitor total required capacitance).

Fig. 49: Shifted carriers for 3-levels PWM control routine.

To study in deep the advantages and disadvantages of the interleaving layout, it is firstly necessary to remember

$$\begin{cases} v_{\bar{x}M} = v_{CM} + v_{DM} \\ v_{\bar{x}M} = v_{CM} - v_{DM} \end{cases} \quad \text{where} \quad x = a, b, c \tag{2.3}$$

In any case, a phase-medium voltage (or a signal in general) can be written as a sum or difference of two components, the v_{CM} common mode voltage and the v_{DM} the differential mode voltage. It is to note that the power transfer is controlled by the common mode component, in this particular application.

The *superposition principle* permits to highlight the circulating current phenomena, caused by paralleling two identical units (interleaving topology), that may lead to an unbalance of homologous phase-medium voltages in the two sub-converter: changing α_{PWM} allows to reduce (or eliminate) certain harmonic orders from the phase voltage. However, this also generates/amplifies differential mode harmonics, which can accentuate the circulating current issue. Therefore, a trade-off solution must be found. For example, calling as 1 and 2 the homologous units of the converter, some marked alignment cases can be observed in the following figure.

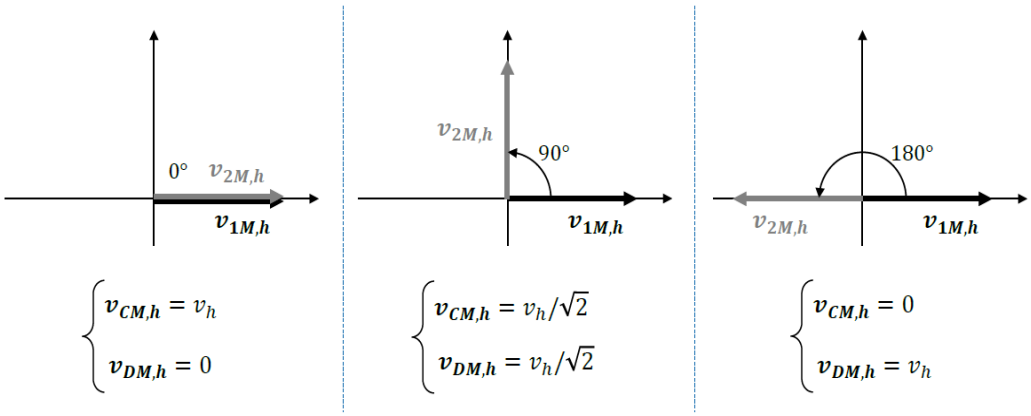


Fig. 50: Some remarkable α_{PWM} alignment cases.

Figure 51 describes how the superposition principle works (it permits to study the system as two independent common mode and differential mode circuits where the sum of the responses returns the whole response of the system).

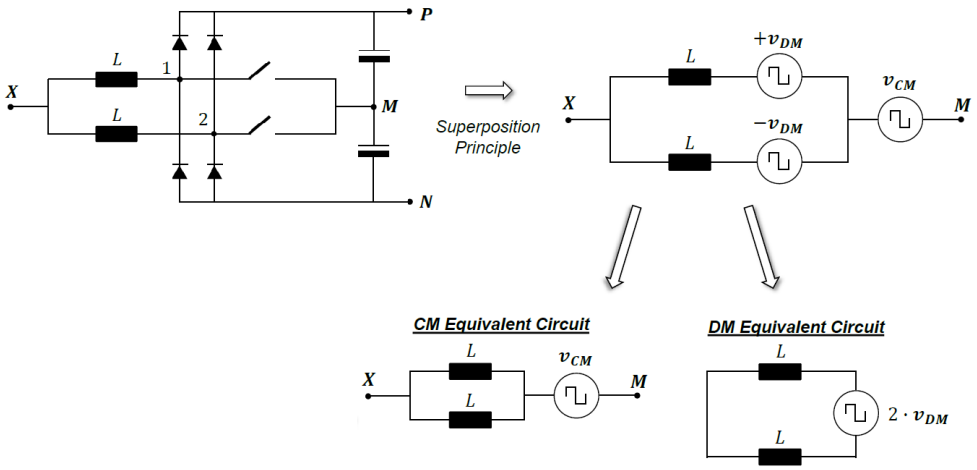


Fig. 51: Identification of common and differential voltage components.

When connected as a three-phase system, only the phase common-mode components interact with each other. As expected, the differential mode voltages generate circulating currents which do not affect line currents.

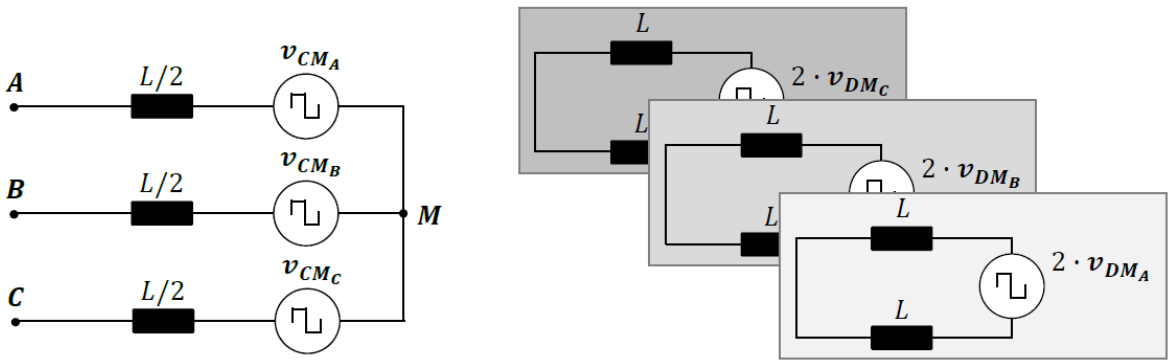


Fig. 52: 3-phase EC (equivalent circuit) of common and differential voltage components.

Under these hypothesis, the voltage applied on the boost inductors can be expressed as:

$$v_{L,x} = v_{DM,x} + v_{CM,x} - \sum_{x=a,b,c} \frac{v_{CM,x}}{3} \tag{2.4}$$

The voltage applied to the inductor is directly linked to its flux ripple ($\Delta\Psi_{RMS}$ affects the inductor losses while the $\Delta\Psi_{pp}$ affects the voltage rating of the component); the $v_{L,x}$ voltage consists in:

- *odd carrier harmonics*, which are partially contained in $v_{DM,x}$ (their incidence depend on the shifting between the carriers, thus on α_{PWM});
- *odd triple sideband harmonics*, which are not equally partitioned on the two legs of the interleaved converter (due to α_{PWM}).

These harmonic orders are still not visible from the output: in general, they are content both in differential and common mode contemporaneously, but if the shifting angle α_{PWM} is equal to 180° they entirely fill in the differential mode. As a matter of fact, this situation is the most stressful for the converter, since the two units are not leveraged at the same manner. For this reason, it is suggested to prefer a *no shifted PWM (α_{PWM} = 0) in the perspective of flux ripple minimization on boost inductor*. It is to know that this is one of the key point of the design of the converter, since its dimensions can affect hugely the costs and the encumbrance of the converter.

Another parameter that the control can use to manage the performances of the converter is the *modulation index of the rectifier (m*), which can affect the flux ripple ($\Delta\Psi_{pp}$) and its RMS value ($\Delta\Psi_{RMS}$). The easiest way to master the modulation index m is to vary the magnitude of voltage DC-link. The more the required output DC-link voltage increase, the more the flux ripple will increase (dealing with bigger boost inductor size).

Consequently, with the idea to evaluate properly how flux ripple can vary by changing both α_{PWM} and m of the single leg, a simulative report is displayed in the following figures (realized in MATLAB). Simulative results are reported considering different α_{PWM} (from 0 to 180° of shifting) and V_{dc} values (from 650 V to 800 V, by increasing of 15 V each voltage testing value).

Accordingly to the previous consideration, the flux ripple increase as both α_{PWM} and m_f increase (that means that the max flux occurs for V_{dc} = 800 V and α_{PWM} = 180°).

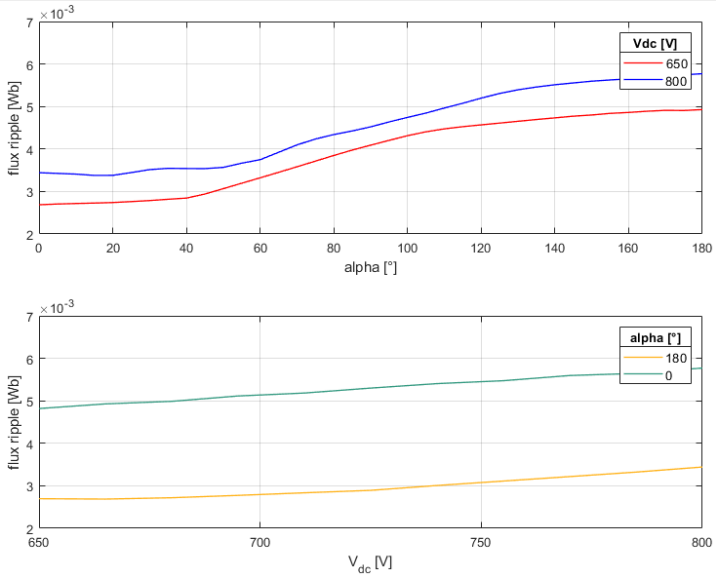


Fig. 53: Peak-to-peak flux evaluation for different values of α_{PWM} and V_{dc}.

A similar harmonic cancellation process affects the DC-link current $I_{c,RMS}$, decreasing both the total RMS current $I_{c,RMS}$ (due to ripple component on the single capacitor of the split DC-link) and the capacitor charge ripple ΔQ_{pp} (tied to $I_{c,RMS}$ from a derivative law): *increasing the PWM phase shift results in a smaller DC-link capacitance requirement*. Thus the efficient design of L_{boost} and DC-link capacitors C_{dc} moves to opposite directions.

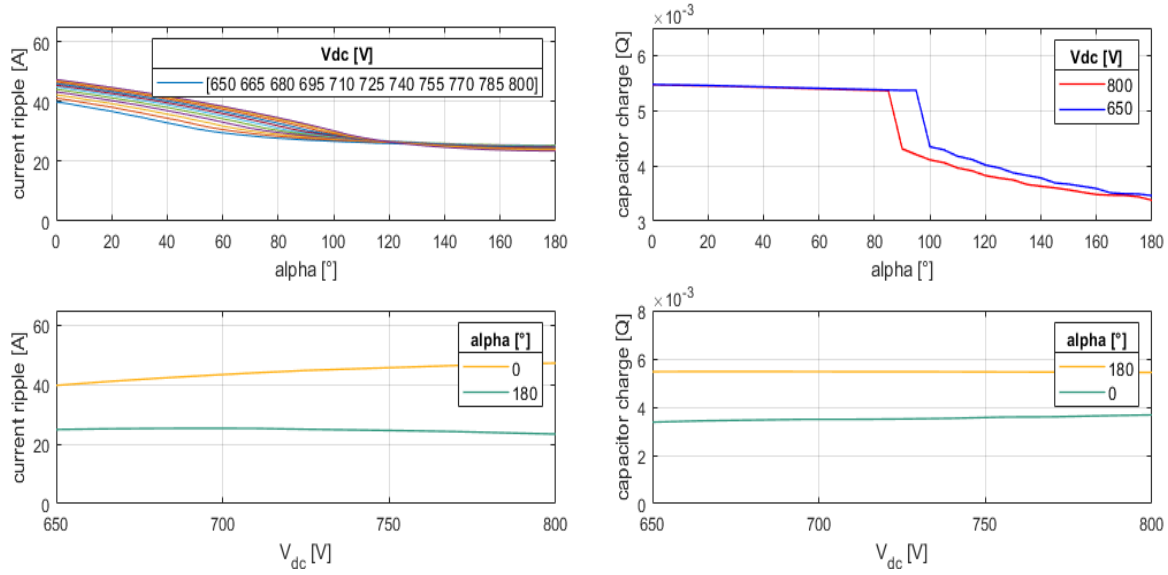


Fig. 54: capacitor current and charge peak-to-peak ripple evaluation for different values of α_{PWM} and V_{dc}

Figure 54 shows the current and the charge values for different modulation indexes and different phase shifts. It is to note that if a modulation strategy with a low-frequency triple harmonic mid-point current component is adopted (e.g. DPWM4 or TLSVPWM), even increasing the α_{PWM} value to its max ($\alpha_{PWM} = 180°$) an high value of charge ripple is obtained (which is also reflected in an overall higher absorbed current ripple and then in a worse

quality of the absorbed current waveform); thus *there is no great improvement in increasing* α_{PWM}. For this reason, it the primal design of the converter it is preferred to define:

$$\begin{cases} \alpha_{PWM} = 0° \; for \; optimal \; boost \; inductor \; design \\ V_{dc} = 650 \; V \; for \; the \; lowest \; flux \; ripple \; on \; boost \; inductor \end{cases} \tag{2.5}$$

Even if it is not possible to define an absolute optimum for α_{PWM} for the converter, a trade-off solution between inductor flux ripple, DC-link RMS current, required DC-link capacitance and EM compatibility must be found. **The min ($\Delta\Psi_{pp}$) and min ($\Delta\Psi_{RMS}$) criteria, which affect the boost inductor design, are to be considered more important than min $I_{c,RMS}$ and min ΔQ_{pp}, which affect the DC-link capacitor selection.** Therefore, a considerable higher weight should be assigned to the first two criteria, being directly linked to the boost inductor size and losses. This proves formula 2.5. As a reminder:

$$\begin{cases} \boldsymbol{min\left(\Delta\Psi_{pp}\right) \leftrightarrow \alpha_{PWM} = 0°} \\ \boldsymbol{min\left(\Delta\Psi_{RMS}\right) \leftrightarrow \alpha_{PWM} = 0°} \\ \boldsymbol{min\left(I_{c,RMS}\right) \leftrightarrow \alpha_{PWM} = 180°} \\ \boldsymbol{min\left(\Delta Q_{pp}\right) \leftrightarrow \alpha_{PWM} = 180°} \end{cases} \rightarrow \boldsymbol{\alpha_{PWM} = 0° \; (the \; inductor \; size \; is \; minimized)}$$

It is now possible to evaluate precisely the $C_{dc,min}$ (minimum value for C_{dc}) and the L_{min} (minimum value for L_{boost}) required by the converter under the previous hypothesis. The following design guidelines are therefore provided:

$$\begin{cases} max\left(\Delta\Psi_{pp}\right) = 3 \; AmH \\ max\left(\Delta\Psi_{RMS}\right) = 0{,}5 \; AmH \\ max\left(I_{c,RMS}\right) = 56{,}4 \; A \\ max\left(\Delta Q_{pp}\right) = 6{,}8 \; VmF \end{cases} \tag{2.6}$$

The minimum DC-link capacitance value may be calculated by the following expression:

$$C_{dc,min} = \frac{\Delta Q_{pp,max}}{\Delta V_{pp,max}} \tag{2.7}$$

The previous values refer to one half of the DC-link. The $\Delta Q_{pp,max}$, is known from 2.6, while the $\Delta V_{pp,max}$ is calculated as follow:

$$\Delta V_{pp,max} = 5\% \cdot \frac{V_{dc,min}}{2} = 0.05 \cdot \frac{650 \; V}{2} = 16{,}25 \; V$$

Indeed,

$$C_{dc,min} = \frac{\Delta Q_{pp,max}}{\Delta V_{pp,max}} = \frac{6{,}8 \; VmF}{16{,}25 \; V} = 418 \; \mu F \cong 500 \; \mu F$$

Finally,

$$\boldsymbol{C_{dc,min} = 500 \; \mu F}$$

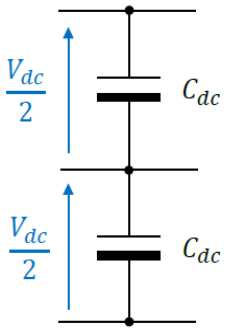


Fig. 55: Split DC-link capacitor.

DC-link capacitors are chosen among the Vishay electrolytic capacitors presented in the following datasheet (figure 56). They are preferred because guarantee compact design and high capacitance. In particular, the following requirements are to be met:

$$\begin{cases} C_{dc,min} \geq 500\ \mu F \\ V_{dc,min} \geq 325\ V (= U_R) \\ I_{C_{RMS}} \geq 55A \end{cases} \tag{2.7}$$

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ELECTRICAL DATA AND ORDERING INFORMATION

U_R (V)	C_R 100 Hz (µF)	NOMINAL CASE SIZE Ø D x L (mm)	I_R 100 Hz 105 °C (A)	I_{LS} 5 min (mA)	TYP. ESR 100 Hz 60 °C (mΩ)	TYP. ESR 300 Hz 60 °C (mΩ)	MAX. ESR 100 Hz (mΩ)	MAX. Z 10 kHz (mΩ)	ORDERING CODE MAL2259..... 2-TERM.	3-TERM.
450	68	22 x 25	0.69	0.31	787	361	1640	1120	57689E3	17689E3
	82	25 x 25	0.79	0.37	658	301	1370	940	57829E3	17829E3
	100	22 x 30	0.87	0.45	538	246	1120	760	57101E3	17101E3
	120	22 x 35	0.99	0.54	446	205	930	630	57121E3	17121E3
	120	25 x 30	0.99	0.54	451	207	940	640	67121E3	27121E3
	120	30 x 25	1.03	0.54	466	213	970	670	77121E3	37121E3
	150	22 x 40	1.16	0.68	360	165	750	510	57151E3	17151E3
	150	25 x 35	1.15	0.68	360	165	750	520	67151E3	27151E3
	180	22 x 45	1.31	0.81	298	136	620	430	57181E3	17181E3
	180	25 x 40	1.32	0.81	302	139	630	430	67181E3	27181E3
	180	30 x 30	1.29	0.81	312	143	650	460	77181E3	37181E3
	180	35 x 25	1.34	0.81	336	154	700	500	87181E3	47181E3
	220	25 x 50	1.60	0.99	254	117	530	360	57221E3	17221E3
	220	30 x 35	1.48	0.99	259	119	540	380	67221E3	27221E3
	220	35 x 30	1.56	0.99	269	123	560	400	77221E3	37221E3
	270	30 x 40	1.68	1.22	216	99	450	310	57271E3	17271E3
	330	30 x 45	1.92	1.49	178	81	370	260	57331E3	17331E3
	330	35 x 35	1.89	1.49	187	86	390	280	67331E3	27331E3
	390	35 x 40	2.11	1.76	158	73	330	240	57391E3	17391E3
	470	35 x 45	2.12	2.36	134	62	280	200	57471E3	17471E3
	560	35 x 55	2.76	2.52	110	51	230	170	57561E3	17561E3
	680	35 x 60	3.06	3.06	91	42	190	140	57681E3	17681E3

Fig. 56: Vishay datasheet forMAL2259 series.

Considering the previous specification for DC-link capacitors, two banks of 6 capacitors are necessary (in total 12 devices), with a total capacitance per bank of:

$$C_{dc_{tot}} = 6 \cdot C_R = 6 \cdot 680\mu F = 4{,}080\ mF \tag{2.8}$$

In a similar manner, the minimum boost inductance value may be calculated by the following expression:

$$L_{min} = \frac{\Delta\Psi_{pp,max}}{\Delta I_{pp,max}} \tag{2.9}$$

The worst case peak current of the inductor is given by the peak-leg-current added to the peak-design-current ripple (considering also a caution increase of 20% of the leg current value). Then, it will be

$$I_{L,max} \cong I_{leg,pk} + \Delta I_{pp} = 1{,}2 \cdot I_{leg,pk} \rightarrow \Delta I_{pp,max} = 0{,}2 \cdot I_{leg,pk} = 0{,}2 \cdot \frac{125\ A}{2} = 12{,}5\ A$$

Consequently,

$$L_{min} = \frac{\Delta\Psi_{pp,max}}{\Delta I_{pp,max}} = \frac{3\ AmH}{12{,}5\ A} \cong 250\ \mu H$$

The last value of inductance L_{min} will be the reference value for input converter inductance. This inductance is usually called as L_m. Consequently, it will be

$$\boldsymbol{L_{min} = L_m = 250\ \mu H}$$

2.2.2 Grid-converter interface, LCL filter design

[3] Passive filters are used as grid/converter interface in order to mitigate the current harmonic content and meet the EM compatibility standards. Many topologies of passive filters have been presented in literature. Initially pure inductive filters (L) were proposed in literature. L filter topology is a first order filter, thus a high-value inductor is generally necessary to attenuate the harmonics current. Large inductance values generate a high voltage drop and affect moreover, the control time response. Therefore, higher switching frequencies f_{sw} need to be employed in order to reduce the size of the reactive elements. Nevertheless, the increased switching frequency raises the losses in the power converter. The LC filter second order characteristic increases the attenuation for high frequencies and reduces filter volume. The drawback of this topology are the existence of a *resonance frequency* which can amplify the high-orders current harmonic components (leading to an overall instability of the system), and further, the incoming issue of the inrush currents in the output capacitance. *LCL filter* is a third order filter, which has recently gained attention as an alternative to traditional LC filters and has been used in most voltage sources applications. This topology results in volume and voltage drop reduction through the inductors, if compared to the simplest L topology. Furthermore, the second inductance guarantees the benefit to limits the capacitor inrush current and increases the converter robustness due to grid inductance variation. The complexity of the system and the correct tuning of the resonance frequency are the main drawbacks of this topology. To summarize:

- **LCL benefits**
    - higher level of (theoretical) attenuation (after the resonance): 60 dB/dec instead of 20 dB/dec of a simple L filter;
    - lower overall inductance between grid and converter, therefore lower voltage drop during operation (thus lower V_{dc} required) and higher saturated control dynamics.

– **LCL drawbacks**

- high current ripple on the converter-side inductor;
- reactive power generation by the capacitor (sometimes to be actively compensated);
- higher control complexity than a simple first order filter.

However, it should be noted that is not reported in literature a systematic design study for LCL filters as grid-connected active front-end (AFE); in this sense, this paper presents a unique example of LCL tuning.

This section presents the main aspects of frequency response and parameters limits and how they affect LCL design. Firstly, the LCL filter is located between the AFE and the mains.

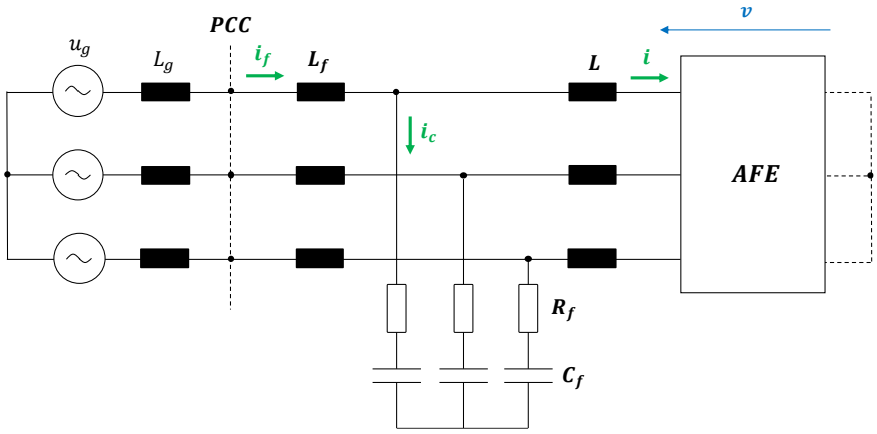

Fig. 57: LCL collocation as grid/converter interface for EM compatibility.

The approach of LCL design is the simplest possible: the filter is considered *ideal*, thus magnetic and electrical losses are assumed as negligible.

As a primal hypothesis is to set properly the *switching frequency* f_{sw} of the converter. It has to be a trade-off between fast switching operations and controlled switching losses. In this kind of applications (3-levels converters) it is allowed to use lower switching frequency to achieve great results in terms of waveform quality and EM compatibility than a first order L filter. In particular, it is assumed as a reference value:

$$\boldsymbol{f_{sw} = 20\ kHz} \tag{2.10}$$

This frequency, in conjunction with the grid frequency f_{grid} (that is equal to $f = f_{grid} = 50$ Hz as usually), represents a key value to set properly the resonance frequency of the filter. As reported in [1], it is necessary to check that the resonance frequency of the filter f_{res} must obey to the condition expressed by (2.11)

$$10 f_{grid} \leq f_{res} \leq {}^{f_{sw}}/_{2} \tag{2.11}$$

If the resonance frequency was lower than 10 times the grid frequency (in this case 50 Hz), the designer would be obliged to increase the filter capacitor. Otherwise, if it exceeded the half of the switching frequency there would be interferences between the converter control and the filter. In this case the resonance frequency must be set thus, between

$$500\ Hz \leq f_{res} \leq 10\ kHz \rightarrow 1\ kHz \leq f_{res} \leq 5kHz \tag{2.12}$$

The second relation of 2.12 is a caution margin to meet the assigned standards in terms of EM compatibility. The resonance frequency can be also calculated as reported in [3]

$$f_{res} = \frac{\omega_{res}}{2\pi} = \frac{1}{2\pi}\sqrt{\frac{1}{C_f}\left(\frac{1}{L} + \frac{1}{L_f}\right)} \tag{2.13}$$

The L_f value is the filtering inductance while the other one (L) is the input inductance of the converter called as *boost inductance* L_{boost}. The purpose of that inductance is to boost the input voltage to the desired DC-link voltage value (from V_{RMS} = 230 V to V_{dc} = 800 V in this application). Therefore, the f_{res} value depends on the reactive components used in the converter (2.13). Considering one by one those components, it is to note that:

- the filter capacitance C_f is a compromise between power factor decrease and injected harmonic current distortion. The maximum suggested value for the filter capacitance is 5% of the nominal power of the converter (in order to avoid overrating the converter). In other words, the maximum capacitance value is determined only for the maximum admissible reactive power. Thus, it must be:

$$\begin{cases} Q_{max} = 0{,}05 \cdot P_n \\ X_c = \frac{\left[3 \cdot \left(\sqrt{2} \cdot V_n\right)^2\right]}{Q_{max}} \\ C_f = \frac{1}{2\pi f_{grid} \cdot X_c} \end{cases} \tag{2.14}$$

- the design of the inductors depends on the power level and the application. The total inductance of the filter should guarantee a maximum voltage drop of 0.1 pu of the voltage nominal value. Indeed, the first inductance value Lf is determined for the maximum acceptable absorbed current ripple while the second inductance L is determined for the desired harmonic current attenuation and the wanted output voltage increment. With the interleaved topology, the boost inductance result to be an half of Lm, since at the AFE input the two homologous units of the converter result to be in parallel. Thus,

$$\frac{1}{L_{eq}} = \frac{1}{L_m} + \frac{1}{L_m} \rightarrow L_{eq} = L_{boost} = \frac{L_m}{2} \tag{2.15}$$

Then, the only unknown parameter is the input inductance of the LCL filter (L_f) that can be calculated by inversion of 2.13, as reported in 2.16.

$$L_{input} = L_f = \frac{1}{\left[(2\pi f_{res})^2 \cdot C_f - \frac{1}{L}\right]} \tag{2.16}$$

It is then sufficient to substitute the desired f_{res} value and the already known parameters (C_f and L). Design specifications about f_{res} fixed a corner frequency of LCL filter to

$$\boldsymbol{f_{res} = 5\ kHz}$$

An iterative algorithm for LCL tuning can be implemented in MATLAB reported in appendix A6. Reactive components results from previous algorithm are reported in chart 2.

C_f	L_f	L	L_{grid}	L_{tot}	r_L	R_f
30.082 µF	46.09 µH	125 µH	10 µH	181.09 µH	0.448	0,352 Ω

Chart 2: Size of LCL reactive components.

A useful parameter to be defined, is the output-to-input inductance ratio:

$$r_L = \frac{L_f + L_g}{L} \tag{2.17}$$

This parameter allows to identify the best ratio between converter-side and grid-side inductances in respect to a user-defined criteria. As reported in [7], in order to maximize the total grid current noise attenuation for a certain value of total inductance L_{tot}, the optimal output-to-input inductance ratio r_L is equal to

$$r_{L_{opt}} = 1 \tag{2.18}$$

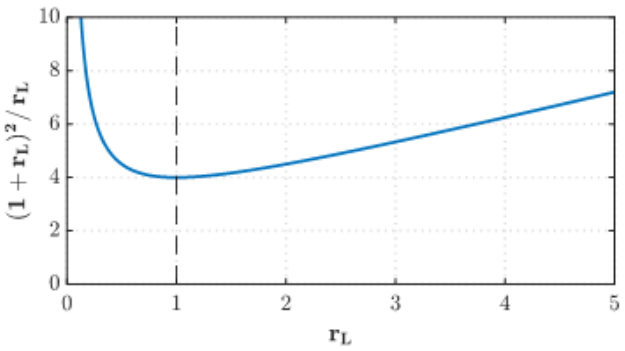

Fig. 58: Sensitivity of output-to-input inductance ratio r_L.

Assuming $r_L \approx 1$, the fittest inductance design can be obtained, since it is guaranteed an optimal trade-off between filter encumbrance and harmonics attenuation.

The value L_{bw} represents the whole inductance necessary to tune the current control: the current PI regulation and dynamic response will be affected both by the inductance of the converter itself and by the inductance of the LCL filter.

By assuming a small-signal analysis ($v_g = 0$) for the system, the following single phase equivalent circuit (EC) is valid as shown in figure 59.

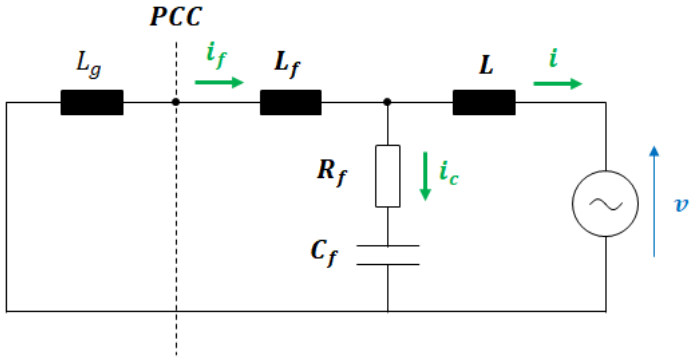

Fig. 59: Small signal EC for LCL filter.

It is possible to highlight two transfer functions to describe the filter and the system in which the filter is inserted in. They are described in the following formulas 2.19 and 2.20 (the transfer function of the system Y(s) and the transfer function of the filter $Y_f(s)$, respectively).

$$Y(s) = \frac{i(s)}{v(s)} = \frac{1}{s \cdot L} \cdot \frac{s^2 + {\omega_f}^2}{s^2 + {\omega_0}^2} \quad where \begin{cases} {\omega_f}^2 = \frac{1}{C_f \cdot (L_f + L_g)} \\ {\omega_0}^2 = \frac{L + L_f + L_g}{C_f \cdot L \cdot (L_f + L_g)} \end{cases} \tag{2.19}$$

$$Y_f(s) = \frac{i_f(s)}{v(s)} = \frac{{\omega_0}^2}{s \cdot (L + L_f + L_g) \cdot (s^2 + {\omega_0}^2)} \quad where \begin{cases} {\omega_f}^2 = \frac{1}{C_f \cdot (L_f + L_g)} \\ {\omega_0}^2 = \frac{L + L_f + L_g}{C_f \cdot L \cdot (L_f + L_g)} \end{cases} \tag{2.20}$$

The 2.19 is the transfer function of the system Y(s) and it is used to evaluate the current closed-loop control stability, while the formula 2.20 describes the transfer function of the filter $Y_f(s)$, necessary to evaluate the DM noise attenuation towards the mains. The plot of the two transfer functions permits to understand how the LCL filters work:

- in low frequency range, the inductive effect is predominant and the transfer function attenuation is 20 dB/dec (harmonics are dealt with by the control, if enough bandwidth is available);
- in average frequency range, an *anti-resonant* ω_f and a *resonant frequency* ω_0 are observed (compensation effect);

– after the resonant frequency, thus at high frequency range, the filter behaves as a third order system, increasing the attenuation to 60 dB/dec (harmonics are filtered by the LCL structure).

The following pictures show the Bode plot of the previous described transfer functions.

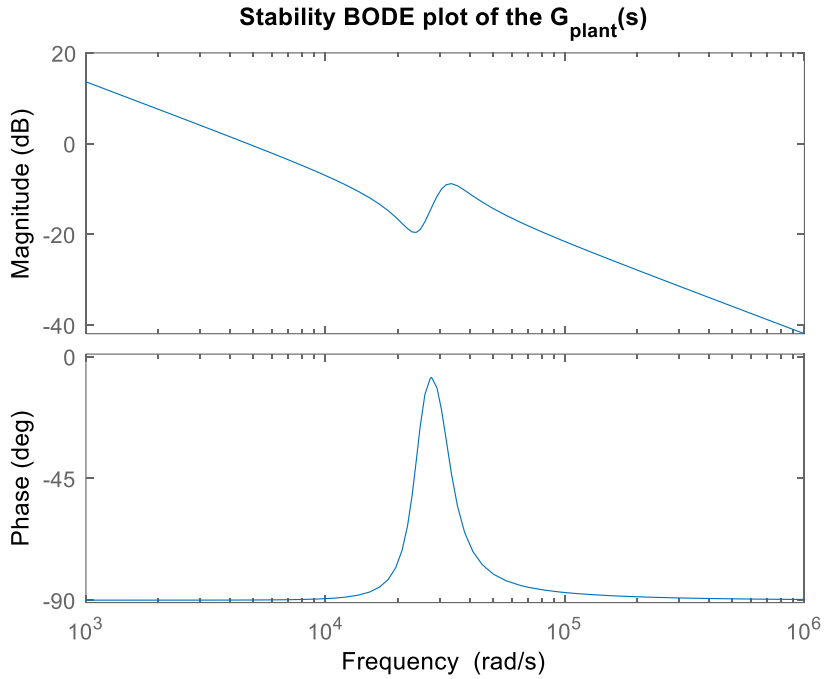

Fig. 60: Bode plot of the transfer function of the system Y(s).

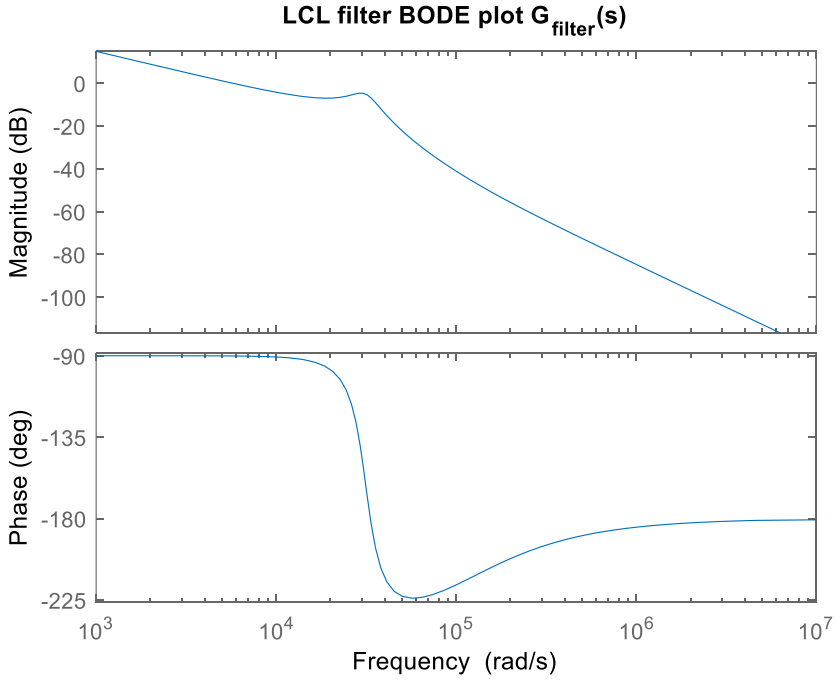

Fig. 61: Bode plot of the transfer function of the filter $Y_f(s)$.

The previous graphs (figures 60 and 61) are obtained through the algorithm implemented in MATLAB and reported in appendix A7, in order to validate the stability check and to calculate the expected attenuation for a wide range of frequencies (from 50 Hz to 120 kHz, chart 3). In the following chart the attenuation gain value per fixed frequency is reported:

Frequency [Hz]	Gain [-]	Phase [°]
50	40.862	-90.0000
20000	-6.994	-149.9628
40000	-14.001	-223.9632
60000	-27.995	-218.5803
80000	-35.749	-212.5753
100000	-41.153	-207.7523
120000	-45.259	-204.0030

Chart 3: LCL guaranteed attenuation per fixed frequency.

The previous chart shows that in high frequency range ($f \geq f_{sw}$) LCL filter guarantees a higher attenuation than a simple first order L filter. Nevertheless, the high frequency attenuation value to be inferior to the theoretical 60 dB/dec since the presence of a damping resistor R_f affects the attenuation performances of the LCL filter.

The damping resistor R_f is quickly calculated: different approaches are found in literature, but the most straightforward is to choose R_f equal to one third of the value of the filter capacitance impedance at the resonance frequency:

$$R_f = \frac{1}{3 \cdot \omega_0 \cdot C_f} \tag{2.20}$$

With this simplified approach, R_f value results valid only in dependency of very specific assumptions on the control tuning (assuming for example that $f_{bw} \approx f_{sw}/20$). If a higher control performance has to be obtained, the R_f value should be reconsidered. Anyway, passive damping leads to several benefits, like stabilization of the closed loop control without active damping methods and lower control sensitivity towards parameter variations (especially L_{grid}) but also may cause lower frequency DM noise attenuation (it becomes almost -40 dB/dec instead of -60 dB/dec) and increasing in terms of power losses (additional damping resistors may increase the heating losses of the converter).

Finally, a comparison between a simple L filter and an LCL filter on the grid absorbed current is reported in figure 62. With the use of L filter a certain high frequency noise is

contented in the current absorbed from the source (the grid) and this could lead to a decrease in terms of waveform quality for the user (since TDD and THD of the waveform increase). On the contrary, with a correct tune of the LCL filter it is possible to obtain a perfectly sinusoidal absorbed grid current for the load, without affecting the control of the converter.

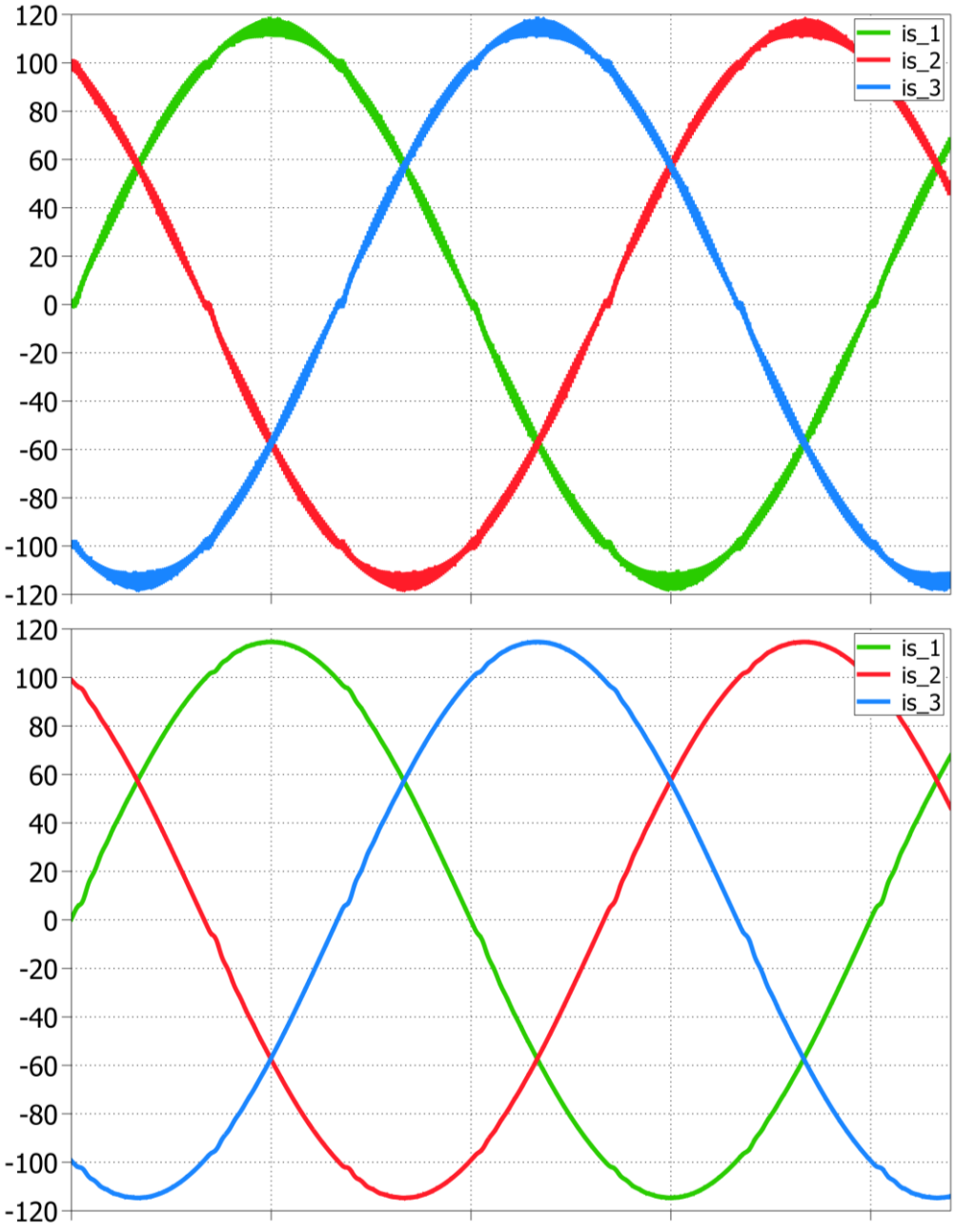

Fig. 62: Comparison about L filter and LCL filter absorbed grid current.

2.3 Block simulation of the T-type converter

The simulation of the converter is run through the use of a specific Power Electronics software called as PLECS. The schematic of the plant is reported in the following figure.

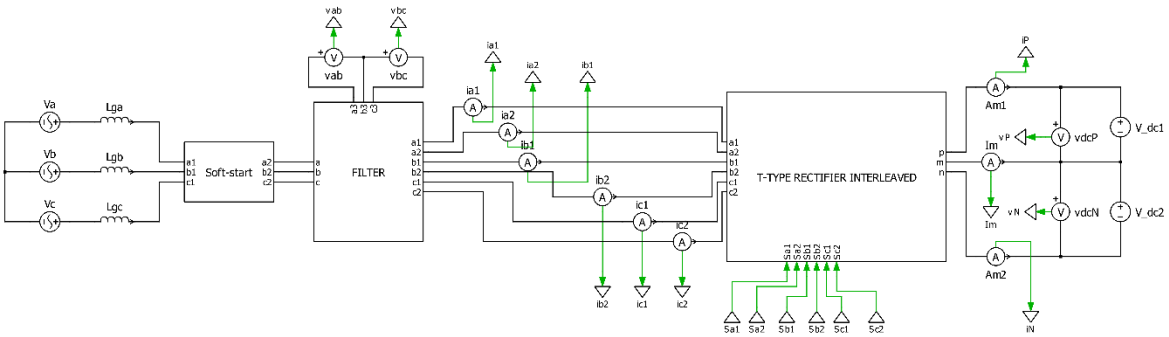

Fig. 63: Schematic of the converter T-type.

It consists in:

- a real voltage source that simulates the grid ($|V_{g,peak}| = 230 \cdot \sqrt{2}$) in series an estimated L_g = 10 μH;
- a soft-start subsystem to avoid a whole load start-up (R_{prec} = (2,5 ÷ 15) Ω);
- an LCL filter tuned with the parameters calculated in the previous paragraph;
- the T-type interleaved converter;
- a voltage generator used to simulate the load (it substitutes the real capacitor DC-link). Assuming ideal behaviour of the generator is possible to run the simulation without the voltage control for charge balancing between the capacitors of the split DC-link.

The filter is composed of 3 reactive elements, as reported in the following picture.

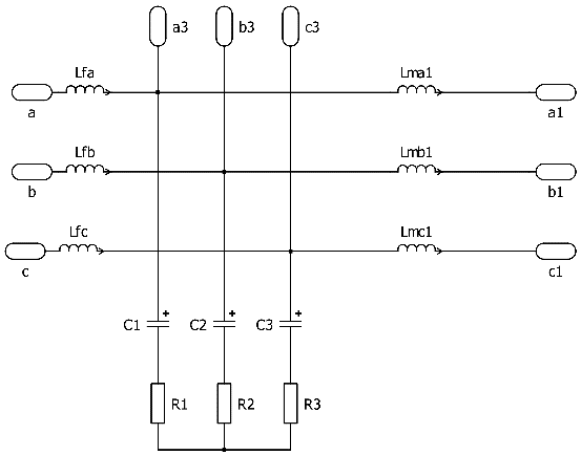

Fig. 64: Schematic of the LCL filter with interleaved topology.

The T-type converter is implemented as already seen in paragraph 1.2 (*List of topologies for AC/DC converters*). The p and n rails are the outputs of the rectifier stage (acting as a unidirectional converter), while the mid-point connection m results to be characterized by two anti-series MOSFETs for bidirectional purposes (the mid-point current i_M changes its sign at least once per period).

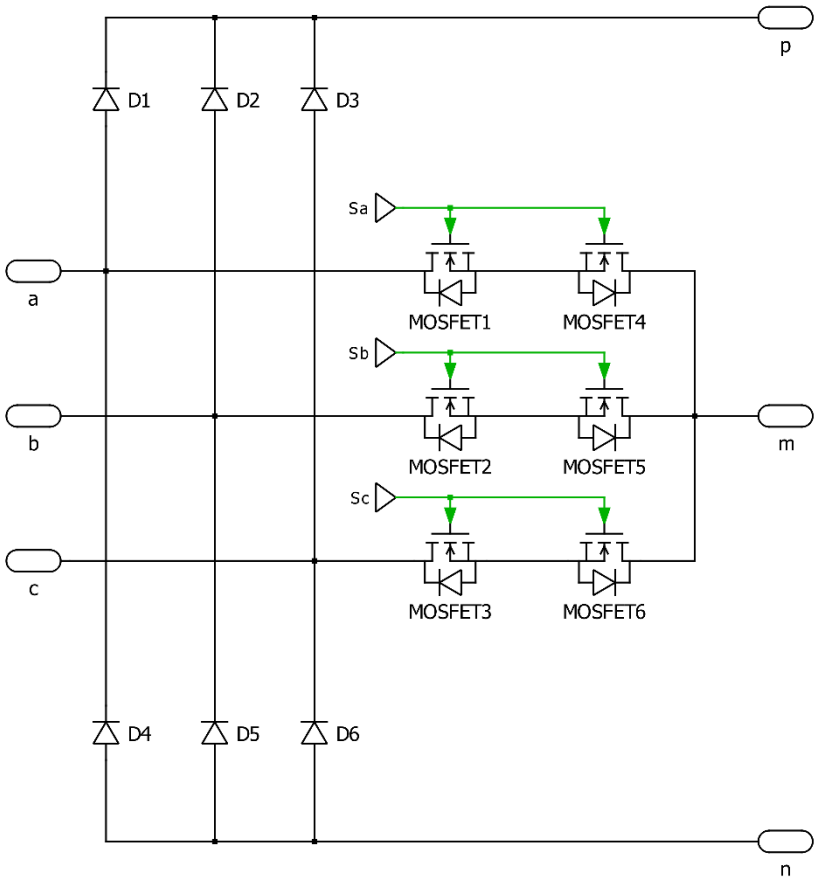

Fig. 65: Schematic of the AC/DC stage (T-type layout) with interleaved topology.

In this fist block simulation, the converter is controlled through a continuous PI as shown in the following figure.

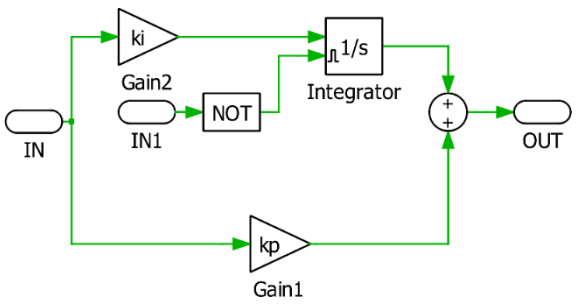

Fig. 66: Schematic of the PI.

As a primal control strategy, a simple BEM algorithm is implemented to verify the expected waveforms for the source current i_s and to test the values for f_{bw}, k_p and k_i. The PI tuning is

carried out by a typical trial and error approach. Firstly, the f_{sw} of the converter is set to 20 kHz. The f_{bw} of the PI is set to 1 kHz; it guarantees an optimal dynamic response and a proper quality of output waveforms. The gains of the PI are tuned in a straighforward manner as reported in the following formula (2.21).

$$\begin{cases} \boldsymbol{f_{sw} = 20\ kHz} \\ \boldsymbol{f_{bw_i} \cong \frac{f_{sw}}{20}} \\ \omega_{bw} = 2\pi f_{bw} \\ L_{bw} = L_g + L_f + \frac{1}{2}L_m \\ k_{pi} = \omega_{bw} L_{bw} \\ \boldsymbol{\omega_z = \frac{1}{5}\omega_{bw}} \\ k_{ii} = \omega_z k_{pi} \end{cases} \tag{2.21}$$

The inductance to use in order to adjust the k_{pi} of the PI is L_{bw} defined as the sum of all the inductances seen by a single phase of the converter, thus it has to consider the grid inductance, the filter inductance and further a half of the boost inductance of the converter (due to interleaved topology). The k_{ii} gain is set to recover the error generated by k_{pi} to follow the current reference in the slightest manner, in order to avoid the wind-up effect and a nervous behaviour of the PI. The control schematic is reported in figure 67.

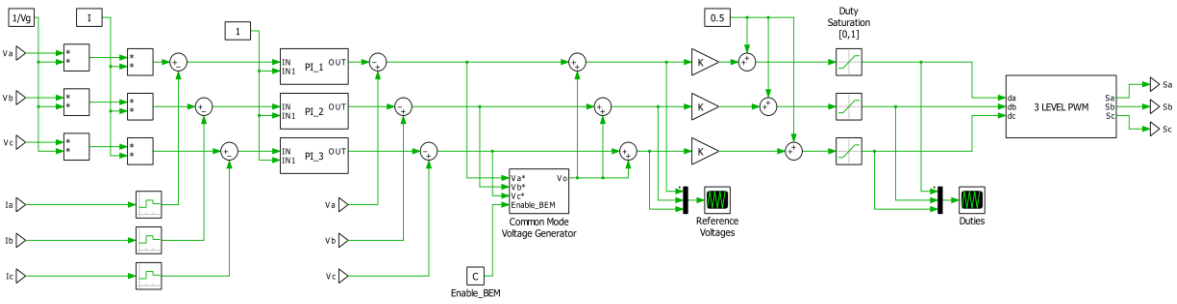

Fig. 67: Schematic of the control of the converter in block simulation.

The previous schematic display the model for implementing a minimal grid-synchronized current control: the instantaneous phase voltage is normalized to the peak value of the grid voltage ($|V_{g,peak}|$) and it is then multiplicated for a current reference. The PI acts by nulling the error generated for the difference between the current reference and the phase current (on the stationary frame abc).

$$\varepsilon_I = I_{ref} - i_{phase} \tag{2.22}$$

The output of the controller permits to generate three phase voltages value that are used to calculate properly the v_{zs} (voltage zero sequence) for BEM purposes.

The control output is the vector (d_a, d_b, d_c) of duties of the triad abc that are firstly saturated between 0 and 1 and then they are sent to a 3-level PWM unit (acting as already described in figure 32) to generate the vector of signals (s_a, s_b, s_c) used to control the switches of the mid-point connection (they become the input of the MOSFETs).

Although the simplicity of the control routine, the system guarantees excellent performances in terms of dynamic response and precision of regulation also in case of very low current reference value, namely in DCM. The following figures demonstrate the previous assertions (the correct tuning of the PI controller is highlighted in figure 70, since the current reference and the phase a current instantaneous value result to be indistinguishable).

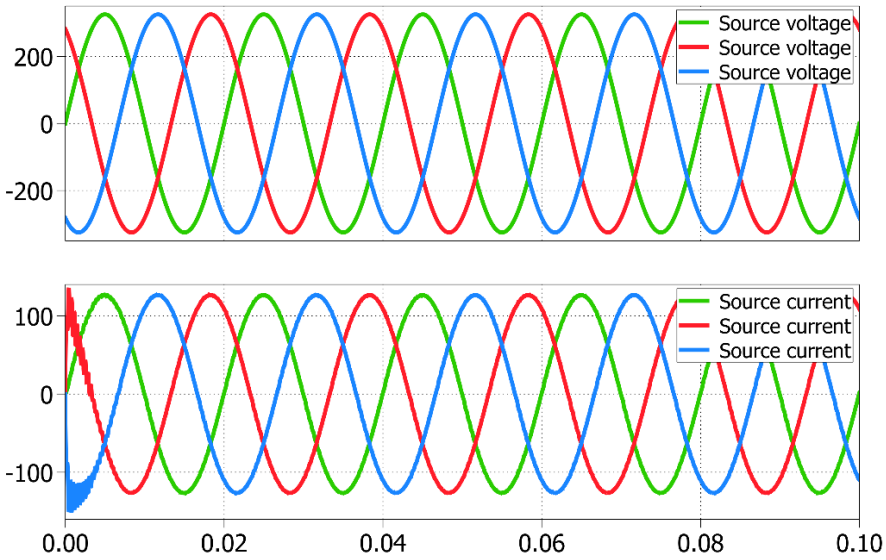

Fig. 68: Grid voltages and current absorbed by the converter.

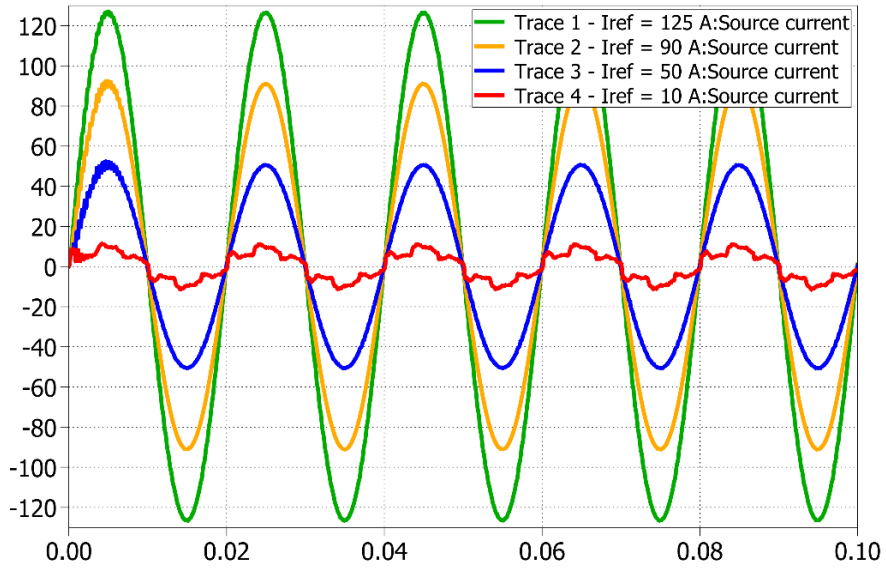

Fig. 69: Current absorbed by the converter with different current reference values.

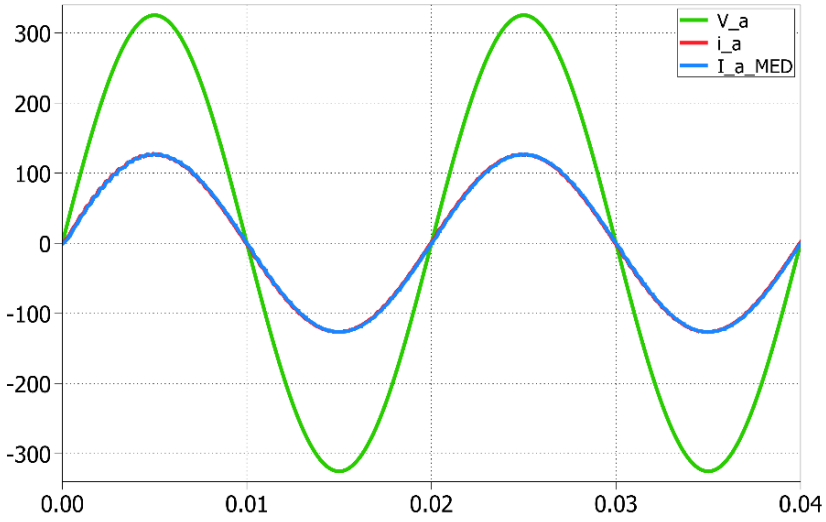

Fig. 70: Current reference and periodic average of phase a current.

2.4 Design of current and voltage loops

Preambles of the previous paragraph permit to establish a guideline to correctly tune the control of the converter but, in usual applications, the control has to be implemented through a microcontroller. In addition, a coherent space-state model has to be evaluated in order to master these kind of devices (to develop a proper control theory). For these reasons, the aim of this chapter is to provide a comprehensive treatment of the subjected targets, leading to:

- **a C code implementation of the control routine of the converter (to be used in microcontroller applications and HIL experimental testing);**
- **a current loop tuning in the stationary abc frame;**
- **a voltage loop tuning with a current control loop in the rotational dq frame, in order to guarantee DC-link voltage control and suited mid-point balancing.**

With reference to figure 71, the main pointed out targets of the control in the stationary frame can be summarized with the following equations:

$$\begin{cases} i_A = \frac{u_A - v_{\bar{A}}}{s \cdot L} \\ i_B = \frac{u_B - v_{\bar{B}}}{s \cdot L} \\ i_C = \frac{u_C - v_{\bar{C}}}{s \cdot L} \end{cases} \tag{2.23}$$

The parameter L stands for the equivalent inductance seen by a phase of the converter, as already stated in the previous paragraph (formula 2.21), thus:

$$L = L_{bw} = L_{tot} = L_g + L_f + \frac{1}{2} L_m$$

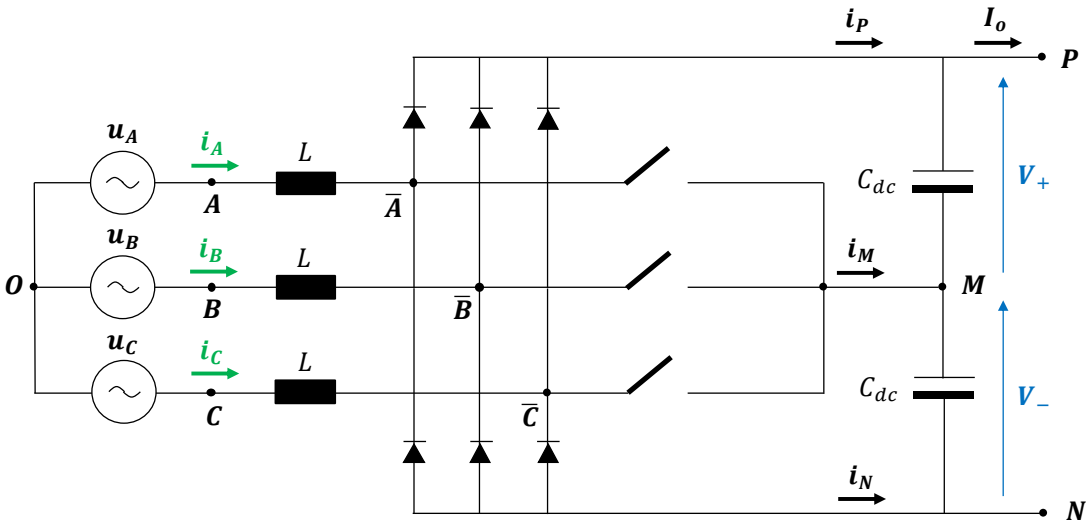

Fig. 71: Simplified model of the T-type converter.

In appendix A8 is reported a C code routine used for PI current control. The current control is the easiest to implement, since the PI works directly in the abc stationary frame. The stationary error generated on the phase current in SS operations (with respect to the current reference) is negligible, since the f_{sw} of the converter is more larger than the frequency of the electric phenomena to control (f = 50 Hz). Anyway a voltage feed-forward addition is used to recover the aforementioned error.

The simulations are carried out using the ZMPC (Zero Mid-Point Compute) technique.

Fig. 72: Current control check.

In the previous graph are displayed the reference current (in red) and the phase current of the first interleaved unit $i_{a,1}$ (in green). It is to note total absence of ripple thanks to LCL filter noise attenuation. Appendix A9 shows the parameters of the current loop tuning.

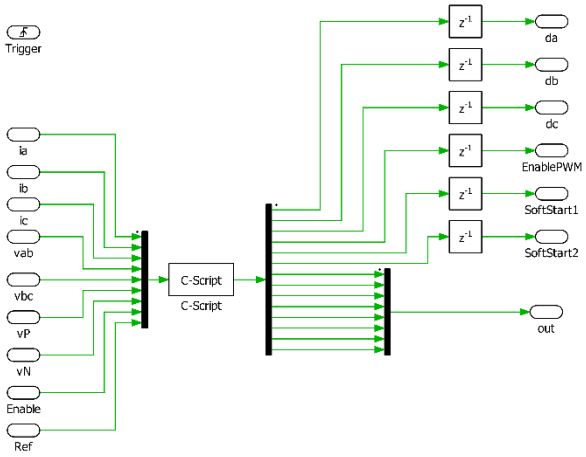

Fig. 73: Schematic of the control routine (C-Script).

The major issue to deals with in real application, results to be tied to the *mid-point current control*, tethering with the DC-link voltage balance, responding to the following formulas (I_0 represents the load current as shown in figure 71):

$$\begin{cases} V_+ + V_- = \frac{i_P - i_N - 2 \cdot I_o}{s \cdot C_{dc}} \\ V_+ - V_- = \frac{i_P + i_N}{s \cdot C_{dc}} = \frac{-i_M}{s \cdot C_{dc}} \end{cases} \tag{2.24}$$

Indeed, the voltage control must be addressed to realize the following statement (2.25):

$$\begin{cases} \boldsymbol{V_+ + V_- = V_{dc}} \\ \boldsymbol{V_+ - V_- = 0} \end{cases} \tag{2.25}$$

The second formula of 2.24 established that the differential mode voltage originates the circulating current i_M. Consequently, the primary target of the voltage closed loop control for real applications, is to *set a proper current reference in the dq frame and guarantee that the voltages applied on the split DC-link have been constrained by formula 2.25 (in order to maintain the i_M periodic average value as closest as possible to 0)*. In this kind of converters, the energetic purpose is all tied with the common mode voltage, while the differential mode results useless in terms of power transmission to the load. The previous considerations can be summarized as shown figure 74 [7].

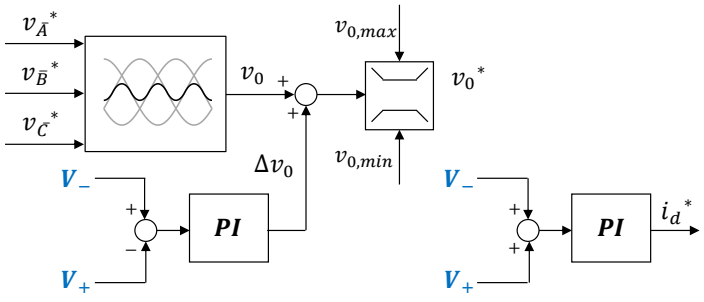

Fig. 74: Block model of the voltage control.

Then, it seems to be necessary to define correctly a state-space model for the converter. As a first sight a d-axis equivalent circuit and a q-axis equivalent circuit can be highlighted to understand the *cross-coupling effect*.

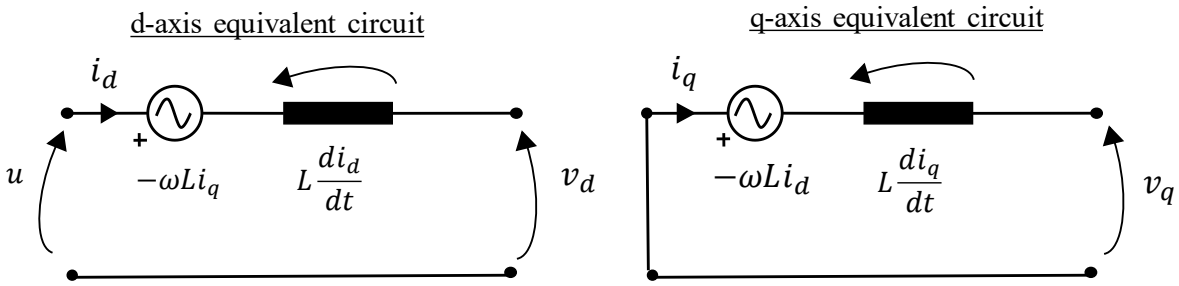

Fig. 75: EC of the converter on dq frame.

As shown in the previous figure, the voltage generated on the d reference results to depend on the current of the other frame. For example, the d-axis voltage will depend on i_q and on the source voltage u while the q-axis one will depend only on i_d. The cross coupling effect is visible due to the terms $-\omega L i_q$ and $-\omega L i_d$ (additive disturbances on reference voltages). The voltage control block diagram is shown in figure 76.

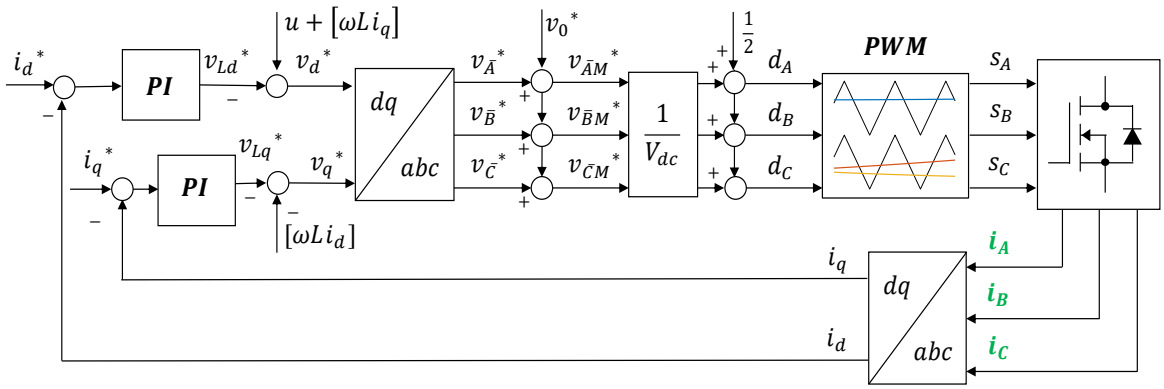

Fig. 76: Block model of the control of the whole converter.

[7] Mathematically, it is possible to write the following formulas (2.26):

$$\begin{cases} v_d = u + \omega L i_q - L\frac{di_d}{dt} \\ v_q = -\omega L i_d - L\frac{di_q}{dt} \end{cases} \tag{2.26}$$

States variables

$$\begin{cases} i_d = \dfrac{-v_d + u + \omega L i_q}{sL} \\ i_q = \dfrac{-v_q - \omega L i_d}{sL} \end{cases}$$

States-space model

$$\begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} \frac{u-v_d}{L} \\ -\frac{v_q}{L} \end{bmatrix} \tag{2.27}$$

The space-state model displays clearly the two component of current and it can be used to manage an optimal strategy of control for the converter: it would be useful to orient the current i_{dq} vector only to one axis (like as in the majority of the control strategies for electrical drives) and to limit the cross-coupling effect. In 2.28 the control strategy adopted is stated:

$$\begin{cases} \boldsymbol{i_d}^* = \boldsymbol{I_{dc}} \\ \boldsymbol{i_q}^* = \boldsymbol{0} \end{cases} \tag{2.28}$$

In order to define the I_{dc} component it is necessary to manage a power balance of the DC-link; in this way, the i_{dc} component became the reference value to adjust the current control. In fact:

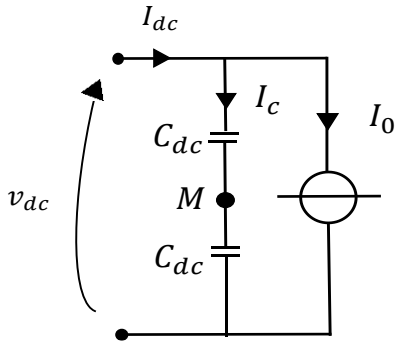

Fig. 77: EC of the DC-link.

From the previous figure:

$$\frac{C_{dc}}{2} \cdot \frac{dv_c}{dt} = I_C = I_{dc} - I_0 \tag{2.29}$$

In terms of state variables:

$$v_{dc}(s) = \frac{2 \cdot (I_c)}{sC_{dc}} = \frac{2(I_{dc} - I_0)}{sC_{dc}} \tag{2.30}$$

The two current components represent respectively the new current reference (I_{dc}) in the voltage control loop and the current feedforward I_0 (configured as an additive disturbance on the system and variable as function of the load request of current). *It is set to zero as a first PI tuning approach.* In order to link the I_{dc} current component to the input phase current the power balance can be leveraged as follows:

$$P = \frac{3}{2} V_{peak} I_{peak} cos\varphi \cong \frac{3}{2} v_{peak} i_d \tag{2.31}$$

In the last formula it has been assumed the hypothesis of unitary cosφ. The power balance has to be verified per each instant of time, thus it will be

$$\frac{3}{2} v_{peak} i_d = V_{dc} I_{dc} \tag{2.32}$$

From which:

$$I_{dc} = \frac{\frac{3}{2} v_{peak}}{V_{dc}} \cdot i_d \tag{2.33}$$

From equations (2.30) and (2.33) it is evident that the v_{dc} differential equation is non-linear. However, this non linearity can be compensated via control. The following state-space model is obtained:

$$\left[\frac{dv_{dc}}{dt}\right] = [0] \cdot [v_{dc}] + \left[\frac{2}{C_{dc}} \cdot \left(\frac{3}{2} \cdot \frac{v_{peak}}{V_{dc}} i_d + I_0\right)\right] \tag{2.34}$$

The voltage loop of the whole plant can be represented as follows:

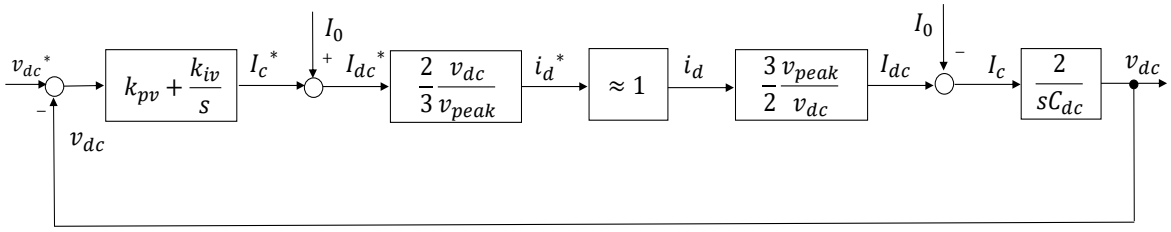

Fig. 78: Voltage loop of the plant.

The bandwidth of the voltage loop should be sensibly lower than the one of the current loop. In any case, a new strategy of control has to be evaluated in order to use effectively the voltage loop as reference generator for current control since it works on the rotational dq frame instead of the stationary one. For this reason, it results to be necessary to leverage the usual Clark (abc to αβ) and Park (αβ to dq) transformations. The dq-reference is oriented as indicated from a PLL that permit to synchronize the current of the converter to the grid voltages (generate a proper ϑ value for this purpose). Voltage control has a striking importance for the converter since it permits to realize the *mid-point balancing of the split DC-link*. Typical values for voltage bandwidth are almost:

$$\boldsymbol{f_{bw_v} = \left(\frac{f_{bw_i}}{10}\right) = \left(\frac{f_{sw}}{200}\right)}$$

Considering the bandwidth frequencies of current and voltage loops, it might appear clear that the i_d^* component results to coincide with the real i_d (the internal current loop may be

represented then as a unitary gain block in figure 78) since it works considerably quicker than the voltage loop. Moreover, the v_{peak} value results to variate instantaneously (it affects hugely the control precision and dynamic, figure 79).

Finally, the open loop transfer function of the current and voltage loops and the tuning choice for k_{pv} and k_{iv} gains are reported in formulas 2.35 and 2.36. Moreover, the appendixes A9 and A10 contain the control tuning (for voltage and current gains) implemented in the simulative header files.

$$\begin{cases} G_{OL_i}(s) = \frac{1}{sL}\left(k_{p_d} + \frac{k_{i_d}}{s}\right) \\ G_{OL_v}(s) = \frac{2}{sC_{dc}}\left(k_{p_v} + \frac{k_{i_v}}{s}\right) \end{cases} \quad (2.35)$$

$$\begin{cases} k_{p_d} = \omega_{bw_d} L \rightarrow \omega_{bw_d} \cong \frac{2\pi f_{sw}}{20} \\ k_{i_d} = k_{p_d}\omega_{z_d} \rightarrow \omega_{z_d} \cong \frac{\omega_{bw_d}}{5} \\ k_{p_v} = \omega_{bw_v}\frac{C_{dc}}{2} \rightarrow \omega_{bw_v} \cong \frac{\omega_{bw_d}}{10} \\ k_{i_v} = k_{p_v}\omega_{z_v} \rightarrow \omega_{z_v} \cong \frac{\omega_{bw_v}}{5} \end{cases} \quad (2.36)$$

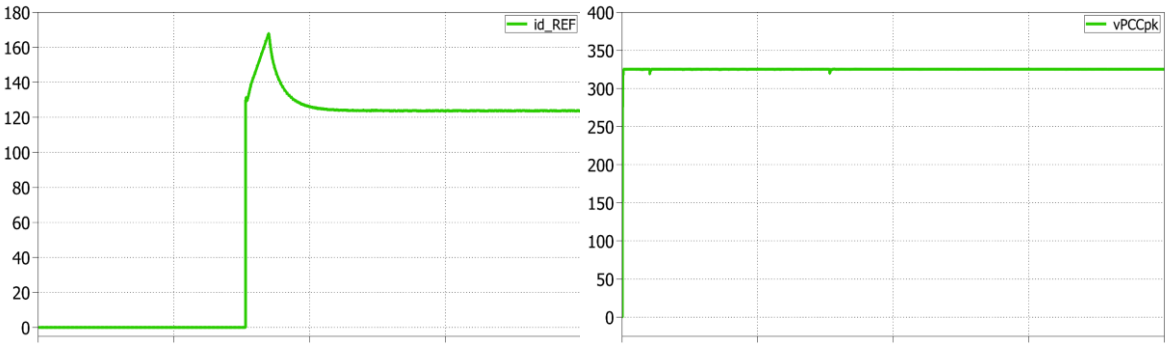

Fig. 79: Instantaneous v_{peak} values and i_d reference for voltage control.

In the end, the voltage control loop will act as described in figure 80.

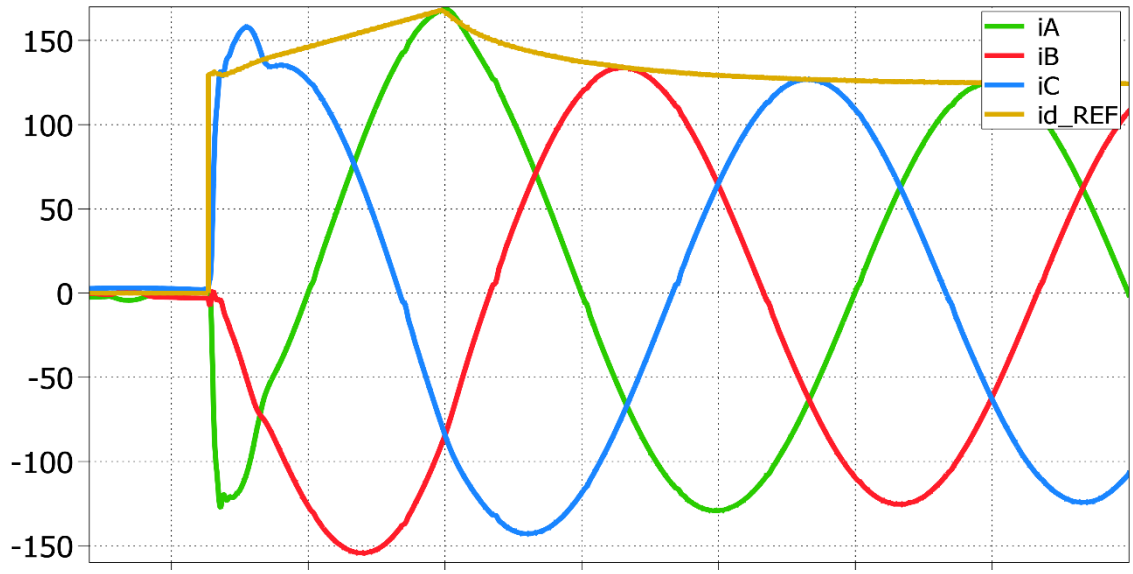

Fig. 80: Current control via voltage loop reference current i_d.

As stated by the previous formulas (2.35 and 2.36), through the voltage control it is possible to realize a proper mid-point balancing. It is to know that the mid-point balancing is sensible to the III harmonics and for this reason it must be implemented by controlling the v_M with a reference frequency of 150 Hz, instead of the usual fundamental frequency control (thus 50 Hz). In particular, considering the equivalent circuit (EC) for the differential mode voltage (v_M) it will be:

$$v_M = \frac{v_+ - v_-}{2} \; by\; expliciting\; the\; state\; variable\; v_M = \frac{1}{2}\frac{I_M}{sC_{dc}} \tag{2.37}$$

The two capacitors of the split DC-link act as they were in parallel when V_{dc} is imposed as voltage loop reference value for the voltage PI controller.

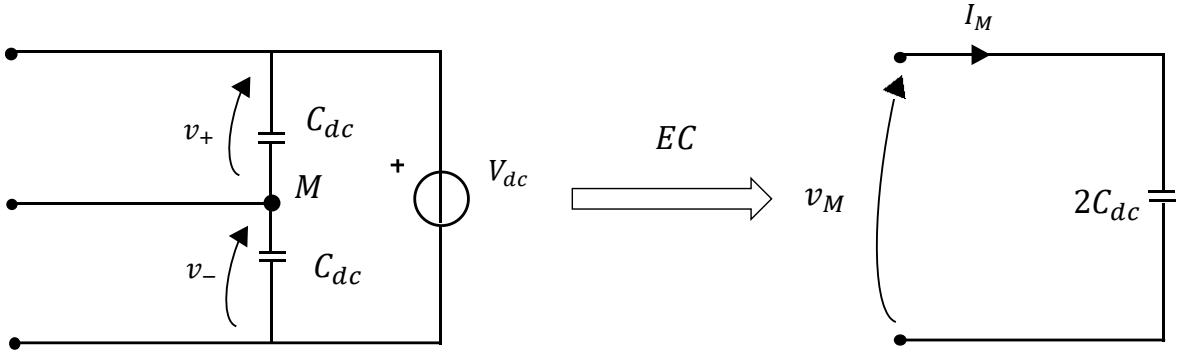

Fig. 81: Differential mode equivalent circuit.

[7] A link between current I_M and a control variable (for example the input phase current in the stationary frame) is necessary in order to tune the control loop.

$$\boldsymbol{i_M = \sum_{k=a,b,c}\left(1 - \frac{2}{V_{dc}}|v_{kM}|\right)\cdot i_k \; where \; v_{kM} = v_k + v_0} \tag{2.38}$$

The voltages v_{kM}, v_k and v_0 represent respectively, the medium-to-phase voltages, the phase voltages and the zero-sequence voltage. Consequently:

$$I_M = \frac{1}{T}\int_0^T i_M(t)dt = \frac{1}{T}\int_0^T \left[\cancel{\sum_{k=a,b,c} i_k} - \sum_{k=a,b,c}\frac{2}{V_{dc}}|v_{kM}|\cdot i_k\right]dt \tag{2.39}$$

In 2.37 the star with no neutral current law $\left(\sum_{k=a,b,c} i_k = 0\right)$ has been used to simplify the integral. By the use of FHA, the main frequency solution is carried out as follows:

$$I_M = -\frac{2}{V_{dc}}\cdot f \cdot \int_0^{1/f}\sum_{k=a,b,c}|v_k + v_0|\cdot i_k \cdot dt \tag{2.40}$$

For a rectifier, if the zero-sequence voltage limits are met, the following relationship is valid:

$$|v_k + v_0|\cdot i_k = (v_k + v_0)|i_k| \tag{2.41}$$

As a consequence:

$$I_M = -\frac{2}{V_{dc}}\cdot f \cdot \int_0^{1/f}\sum_{k=a,b,c} v_0 \cdot |i_k|\cdot dt = -\frac{2}{V_{dc}}\cdot f \cdot \int_0^{1/f} v_0(|i_a| + |i_b| + |i_c|) \tag{2.42}$$

In formula 2.42 the relation $\sum_{k=a,b,c} v_k = v_a + v_b + v_c = 0$ has been applied to simplify the integral. The 2.42 equation may estimate the impact of adding a constant v_0 contribution to all legs. However, since in rectifiers common mode voltage v_0 result to be dynamically limited during the fundamental period (e.g. across the current zero crossing), the applied v_0 will be a function of time and for this reason, the previous equation is not straightforward to solve. As reported in literature [7], the maximum and minimum v_0 instantaneous values are:

$$\begin{cases} v_{0_{MAX}} = min\left\{\frac{V_{dc}}{4} \cdot [sgn(i_k) + 1] - v_k\right\} \\ v_{0_{MIN}} = max\left\{\frac{V_{dc}}{4} \cdot [sgn(i_k) - 1] - v_k\right\} \end{cases} \tag{2.43}$$

The maximum gain between v_0 and I_M is observed in the absence of common-mode limits:

$$I_{M,MAX} = -\frac{2}{V_{dc}} \cdot f \cdot v_0 \cdot \frac{6}{\pi} \cdot \frac{1}{f} \cdot I_{peak} = -\frac{12}{\pi} \cdot \frac{v_0}{V_{dc}} \cdot I_{peak} \tag{2.44}$$

The last formula expresses the maximum mid-point current value in case of no zero-sequence voltage restrictions. Therefore, it is evident that the v_0 voltage component may be leveraged as a control variable for the mid-point voltage control loop; the space-state model becomes:

$$\left[\frac{dv_M}{dt}\right] = [0][v_M] + \left[-\frac{6}{\pi}\frac{v_0}{V_{dc}}\frac{I_{peak}}{C_{dc}}\right] \tag{2.45}$$

In conclusion, a dedicated voltage control loop can be realized for mid-point voltage control and it can be used in conjunction with the ZMPC technique, to master to zero the periodic average of the i_M current. The voltage PI for differential mode voltage control acts as usually by controlling the reference value of the mid-point voltage to zero and producing as output an additive contribute to sum to the duties generated by the selected modulation technique.

$$\boldsymbol{f_{bw_b} = (15 \div 20)Hz}$$

In order to tune correctly that additional PI, its open-loop transfer function can be written as reported in formula (2.46).

$$\begin{cases} G_{M_{OL}}(s) = \frac{1}{s}\frac{1}{2 \cdot C_{dc}}\left(k_{pM} + \frac{k_{iM}}{s}\right) \\ \boldsymbol{\omega_{z_b} = \frac{2\pi f_{bw_b}}{2} = \pi f_{bw_b}} \\ k_{pM} \cong 2 \cdot C_{dc} \cdot \left(2\pi f_{bw_b}\right) \\ k_{iM} = \omega_{z_b} k_{pM} \cdot \frac{f_{sw}}{150} \end{cases} \tag{2.46}$$

The mid-point loop results to be sensible to the III harmonic of the v_M voltage. For this reason the correct tune of the PI controller should act each synchronously to the III harmonic

period. In this way, it won't be in any case affected by the III harmonic differential mode disturbances generated by the converter itself. Appendix A11 and A12 report the voltage loops (for current control and for mid-point balancing) and the duties calculation implemented in PLECS in C code. Simulative results will be reported in the conclusive paragraph of this chapter.

2.5 Simulative results and analysis

In the end, the simulative results (run with PLECS) are reported in this conclusive paragraph. They have been obtained by controlling the converter with the previous state-space-model (2.27). In addition, a variety of tables have been prepared in MATLAB (by data post-processing) in order to realize a global comparison about the modulation techniques used to control the AC/DC active rectifier (AFE).

Firstly, the analysis of the source current absorbed by the converter has been figured out by evaluating the RMS value, the RMS of the ripple component, the TDD of the phase currents and the flux peak value Ψ_p (calculated on the input inductance ½ L_m).

TECHNIQUE	$I_{a,RMS}\ [A_{RMS}]$	$I_{a\sim,RMS}[A_{RMS}]$	TDD [%]	$\Psi_p\ [mAH]$
PWMC	87.544	1.433	0.186	3.094
DPWM	87.532	1.465	**3.294**	3.091
ZMPC	87.535	1.434	0.219	**3.091**
CSVM	87.546	1.458	0.325	3.096

Chart 4: Source current (phase a) characteristics.

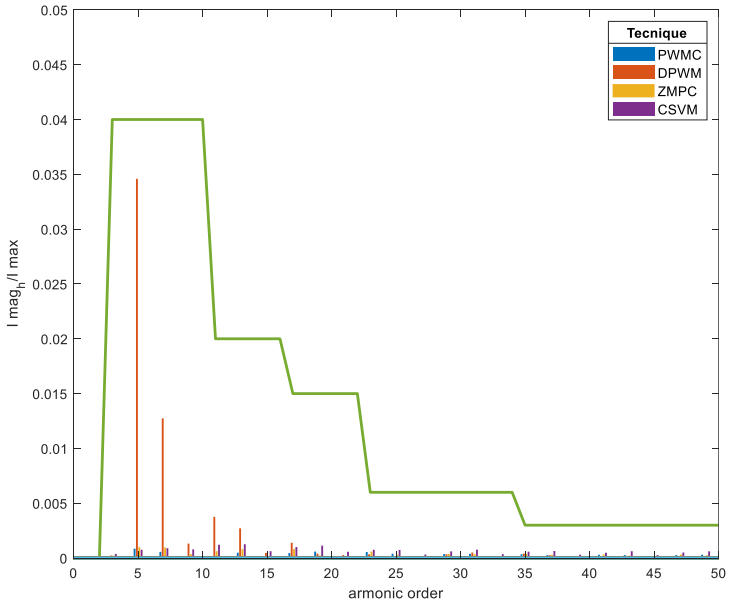

Fig. 82: EM compatibility of high harmonic orders of source current.

As shown in chart 4, all the modulation strategies assure the same value of RMS current on the load. The worst technique in terms of TDD is the DPWM (TDD_{DPWM} = 3.92%). It should be used only with the aim of reduce the switching losses of the converter (but it does not produce a good quality waveform of current). On the contrary, the other techniques have very low value of TDD, guaranteeing the highest current waveforms quality. In figure 82, an EM compatibility mask (in green) has been built to validate that the harmonic content of the absorbed currents, for all modulation strategies, results compatible to the requirements claimed by the EMI regulations. The ordinate represents the pu (per unit) value of the harmonic current (assuming as base value the FH magnitude), while on the abscissa are marked the harmonic orders under test (from 1st to 50th harmonic order).

Furthermore, the effect of decreasing of current quality (due to high TDD) can be also observed in the figure 83. The blue plot (referred to DPWM) shows a certain alteration of the phase current due to an increase of TDD. Furthermore, in the CSVM technique plot (in green) results evident a *zero-current-clamping effect* at each zero-crossing (thus 6 times per period). The PWMC and ZMPC technique are the best technique regarding the absorbed phase current (lowest TDD and absence of zero-crossing).

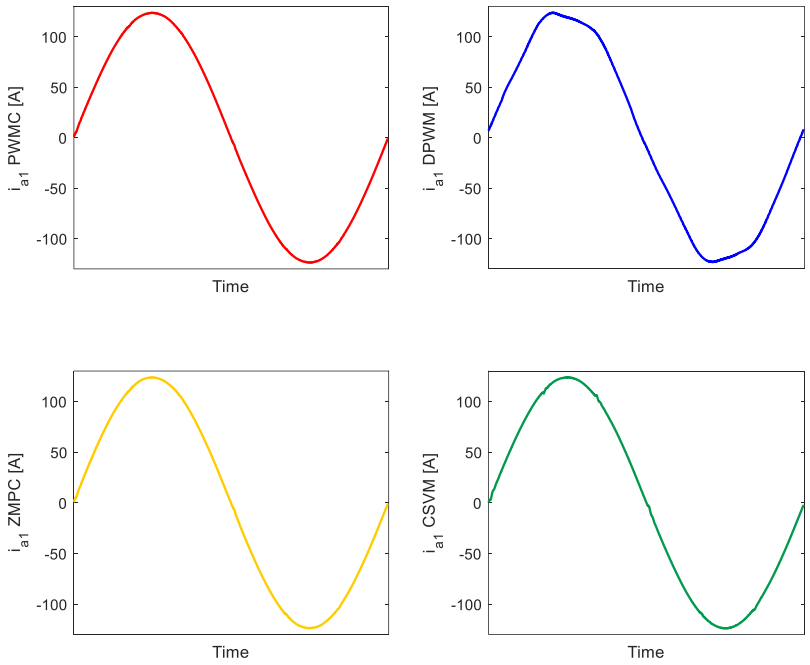

Fig. 83: Comparison of waveforms of absorbed phase current per different modulation strategies.

Concerning the flux peak value, by assuming the hypothesis of orthonormal waveforms, with respect to gate signals, the flux ripple on the input inductance can be assumed symmetrical. Thus, it will be:

$$\Delta\Psi_{pp} = 2\Psi_p \tag{2.47}$$

Despite the previous consideration, all the modulation technique generates a restrained flux ripple on the input inductance (also in case of DPWM, in which a certain compensation symmetry is realized due to orthonormal hypothesis). Considering the i_M current:

TECHNIQUE	$\Delta i_{M,avg}\ [A]$	$i_{M\sim,RMS}[A_{RMS}]$
PWMC	24.759	96.294
DPWM	188.467	96.129
ZMPC	**2.996**	96.349
CSVM	62.682	96.348

Chart 5: Mid-point current (i_M) characteristics.

The periodic average waveforms of the i_M current of the real converter validate the expected results of the theory (as shown in figure 39). It is necessary underline the fact that the ZMPC really guarantee the lowest possible peak-to-peak variation of the i_M periodic average value (as reported in chart 5). The last statement validate the purpose of the thesis, since it shows the efficiency of the control in terms of both **choice of optimal modulation technique (ZMPC) and proper mid-point voltage balance** as displayed in the following figure.

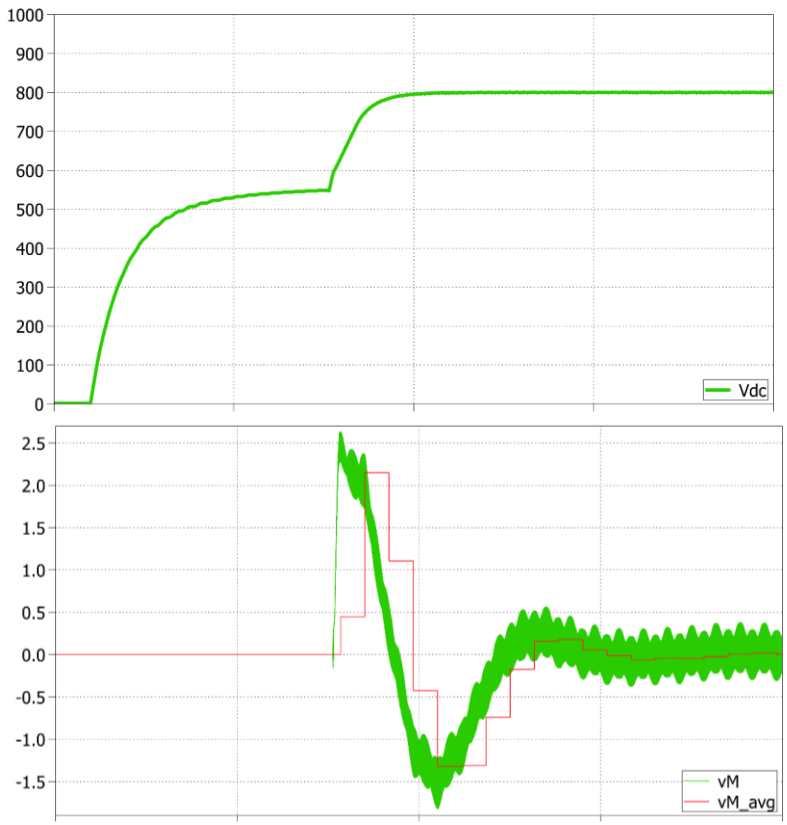

Fig. 84: V_{dc} and v_M voltage waveforms.

The V_{dc} plot is characterized by an excellent precision of regulation and an overdamped dynamic. Regarding the v_M mid-point voltage, the last plot shows how to correctly control the central point of the split DC-link, since the periodic value of the mid-point voltage result to be null after the start-up transient.

Finally, a comparison among v_M differential voltage components per each modulation technique is displayed in figure 85. Even in this case, the DPWM technique plot highlights a too high value of peak-to-peak variation of mid-point voltage v_M (80 V_{pp} as maximum value), while the ZMPC (the red one) has a negligible amplitude. Consequently, also the mid-point current will result to be null (the periodic average value has a negligible peak-to-peak variation in each first harmonic period).

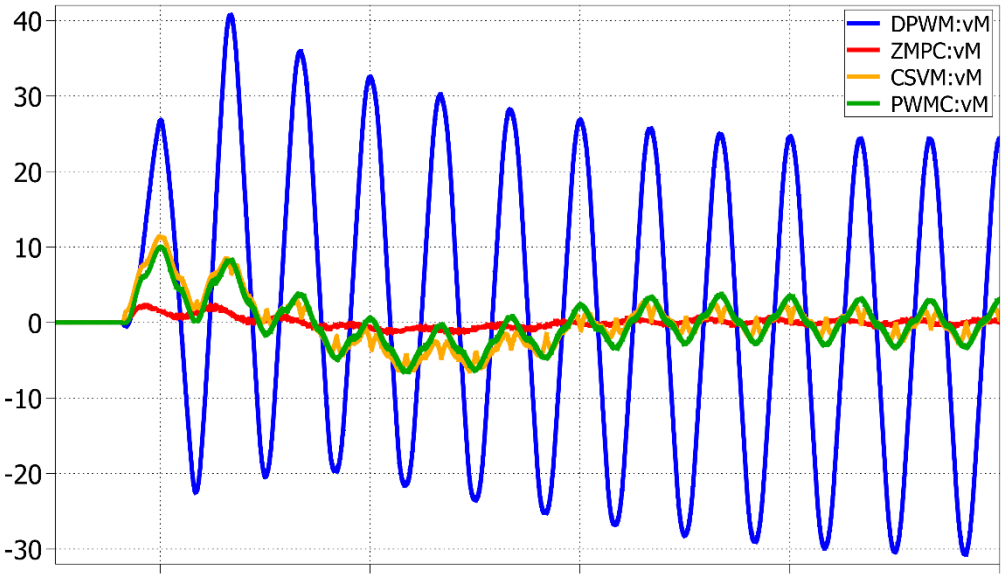

Fig. 85: Comparison of v_M voltage waveforms per different modulation strategies.

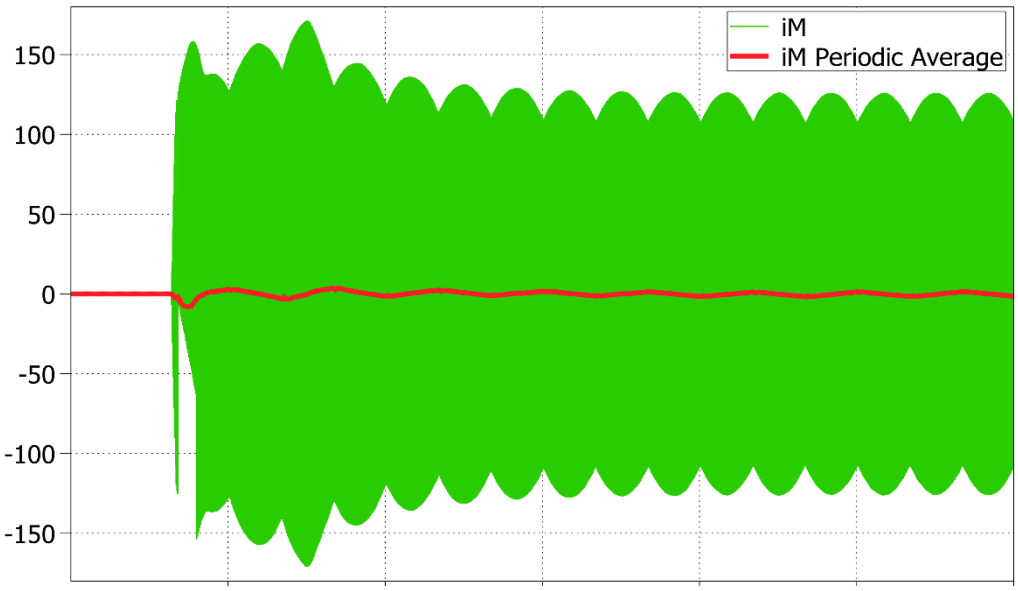

Fig. 86: Real waveform of mid-point current (periodic average and instantaneous value) with the use of ZMPC.

CONCLUSIONS

In this paper, an innovative AC/DC converter suitable for *UFC (ultrafast charger)* applications has been presented. In particular, the *AFE (active front end)* technology has been used to realize that purpose. It is a multi-level converter in which mid-point connection consists of bidirectional and bipolar switches known in literature as *T-type topology* (a combination of antiseries diodes and MOSFETs).

The main aspects of the thesis concern the development of a proper control of the structure in order to achieve the best performances from the converter (in terms of low TDD of absorbed current, unitary cosφ operation and fittest hardware design above all) and mitigate same unique drawbacks of the structure (DC-link voltage control and mid-point balancing).

To evaluate those points of interest, a comparison of different modulation techniques to control the AFE has been carried out. Each modulation strategy result in a discriminating factor for current and voltage expected waveforms (as reported in the first chapter of the thesis). The final project of the AC/DC stage relies to the use of a ZMPC (Zero-Mid-Point-Current) modulation strategy and its advantages are clearly shown in the simulative results of the thesis (low flux ripple on the input inductance, adequate mid-point voltage balancing and negligible periodic average value of mid-point current, as a consequence).

The C codes written to run the simulations within PLECS software (C-Script) are reported in the appendix section; they are already mature for their implementation in a microcontroller for real control testing (HIL, hardware in the loop) and real converter application.

The results, both simulative and experimental, totally coincide with the theoretical ones, achieving great results in terms of accuracy of regulation and robustness of control. For these reasons, the present paper rises as a guideline text for future AC/DC converters control tuning and design.

APPENDIX

This appendix contains all the C code implemented in the simulative tools (PLECS and MATLAB).

A1. duty cycles routine

```
//Duty Cycle Saturation
void DutySaturation(Xabc *Duty)
{       if (duty.a>DUTY_MAX)
                duty.a=DUTY_MAX;
        if (duty.a<DUTY_MIN)
                duty.a=DUTY_MIN;
        if (duty.b>DUTY_MAX)
                duty.b=DUTY_MAX;
        if (duty.b<DUTY_MIN)
                duty.b=DUTY_MIN;
        if (duty.c>DUTY_MAX)
                duty.c=DUTY_MAX;
        if (duty.c<DUTY_MIN)
                duty.c=DUTY_MIN;        }

//Zero Sequence Duty Cycle Saturation due to Current Sign (Unidirectional Rectifier)
void DutyCommonModeSaturation (float *Duty0,Xabc *Duty,Xabc *Current)
{       float Sa,Sb,Sc,do_max,do_min,tmp1,tmp2,tmp3;
        //Current Sign
        Sa = sgn(Current->a);
        Sb = sgn(Current->b);
        Sc = sgn(Current->c);
        tmp1 = 0.25*(Sa+1)-(Duty->a-0.5);
        tmp2 = 0.25*(Sb+1)-(Duty->b-0.5);
        tmp3 = 0.25*(Sc+1)-(Duty->c-0.5);
//do_max
        tmp1 = 0.25*(Sa+1)-(Duty->a-0.5);
        tmp2 = 0.25*(Sb+1)-(Duty->b-0.5);
        tmp3 = 0.25*(Sc+1)-(Duty->c-0.5);
        do_max = tmp1;
        if (tmp2<do_max) do_max = tmp2;
        if (tmp3<do_max) do_max = tmp3;
//do_min
        tmp1 = 0.25*(Sa-1)-(Duty->a-0.5);
        tmp2 = 0.25*(Sb-1)-(Duty->b-0.5);
        tmp3 = 0.25*(Sc-1)-(Duty->c-0.5);
        do_min = tmp1;
        if (tmp2>do_min) do_min = tmp2;
        if (tmp3>do_min) do_min = tmp3;
//Saturation
if ((*Duty0)>do_max) (*Duty0) = do_max;
if ((*Duty0)<do_min) (*Duty0) = do_min;                 }
```

A2. PWMCompute example code

```
//Space Vector PWM Duty Cycle Computation
void SVPWMCompute(Xabc *ABC,float *Duty0,float *Vdc)
{
float a,b,c,Umax,Umin,Umid,v_shift,v_o,tmp1,tmp2,tmp3,tmp4;
        a = ABC->a;
        b = ABC->b;
        c = ABC->c;
// Find Max, Min and Mid (SORTING PROCEDURE)
                Umax = a;
                Umin = b;
                if (a<b)
                {       Umax = b;
                        Umin = a;               }
        else
                {       Umax = a;
                        Umin = b;               }
if (Umax<c)
                {       Umid = Umax;
                        Umax = c;               }
else
{
if (Umin>c)
                {       Umid = Umin;
                        Umin = c;               }
else
                {       Umid = c;               }
}
//Zero Sequence Voltage
v_o = 0.5*Umid;
//Zero Sequence Duty
(*Duty0) = v_o/(*Vdc);      }
```

A3. DPWM4 code example

```
//Discontinuous 30° PWM Duty Cycle Computation (Alternating Upper-Middle-Lower Rails)
void D30PWMCompute(Xabc *ABC,float *Duty0,float *Vdc)
{       float a,b,c,Umax,Umin,Umid,v_shift,v_o,tmp1,tmp2,tmp3,tmp4;
        a = ABC->a;
        b = ABC->b;
        c = ABC->c;
        // Find Max, Min and Mid
        Umax = a;
        Umin = b;
        if (a<b)
        {       Umax = b;
                Umin = a;       }
                else
                {       Umax = a;
                        Umin = b;       }
if (Umax<c)
        {       Umid = Umax;
```

```
                Umax = c;               }
else
        {if (Umin>c)
                {       Umid = Umin;
                        Umin = c;       }
else
                {       Umid = c;       }
}
//Voltage Shift
if(abs(Umax)>=abs(Umin)) v_shift = 0.5*(*Vdc)-Umax;
if(abs(Umax)<abs(Umin)) v_shift = -0.5*(*Vdc)-Umin;
//Zero Sequence Voltage
if((abs(Umax)>=abs(Umin)) && (v_shift>=-Umid)) v_o = -Umid;
if((abs(Umax)>=abs(Umin)) && (v_shift<-Umid)) v_o = 0.5*(*Vdc)-Umax;
if((abs(Umax)<abs(Umin)) && (v_shift<-Umid)) v_o = -Umid;
if((abs(Umax)<abs(Umin)) && (v_shift>=-Umid)) v_o = -0.5*(*Vdc)-Umin;
//Zero Sequence Duty
        (*Duty0) = v_o/(*Vdc);
```

A4. CSVM (TLSVPWM) code example

```
//3-Level Space Vector PWM Duty Cycle Computation
void TLSVPWMCompute(Xabc *ABC,float *Duty0,float *Vdc)
{       float a,b,c,Umin,Umax,v_shift,v_a,v_b,v_c,v_max,v_min,v_o;
        a = ABC->a;
        b = ABC->b;
        c = ABC->c;
//Find Max and Min
Umax = a;
if(Umax<b) Umax = b;
if(Umax<c) Umax = c;
Umin = a;
if(Umin>b) Umin = b;
if(Umin>c) Umin = c;
//Shift
        v_shift = 0.5*((*Vdc)-(Umax+Umin));
        v_a = fmod(a+v_shift,0.5*(*Vdc));
        v_b = fmod(b+v_shift,0.5*(*Vdc));
        v_c = fmod(c+v_shift,0.5*(*Vdc));
//Find Max and Min
v_max = v_a;
if(v_max<v_b) v_max = v_b;
if(v_max<v_c) v_max = v_c;
v_min = v_a;
if(v_min>v_b) v_min = v_b;
if(v_min>v_c) v_min = v_c;
//Zero Sequence Voltage
v_o = -0.5*(Umax+Umin)+0.25*(*Vdc)-0.5*(v_max+v_min);
//Zero Sequence Duty
        (*Duty0) = v_o/(*Vdc);
}
```

A5. ZMPC code example

```
//Zero Mid Point Current PWM Duty Cycle Computation
void ZMPCPWMCompute(Xabc *ABC,float *Duty0,float *Vdc)
{       float a,b,c,Umax,Umin,Smax,Smin,v_o,tmp1,tmp2,tmp3;
        a = ABC->a;
        b = ABC->b;
        c = ABC->c;
        //Find Max and Min
        tmp1 = fabs(a);
        tmp2 = fabs(b);
        tmp3 = fabs(c);
        Umax = tmp1;
        Smax = sgn(a);
        if(Umax<tmp2)
{       Umax = tmp2;
        Smax = sgn(b);      }
                if(Umax<tmp3)
                {       Umax = tmp3;
                        Smax = sgn(c);      }
        Umin = tmp1;
        Smin = sgn(a);
                if(Umin>tmp2)
            {       Umin = tmp2;
                Smin = sgn(b);      }
                if(Umin>tmp3)
            {       Umin = tmp3;
                Smin = sgn(c);      }
//Zero Sequence Voltage
v_o = (Smin*Umin)*(Smin*Umin/(Smax*Umax)+1);
//Zero Sequence Duty
        (*Duty0) = v_o/(*Vdc);      }
```

A6. Algorithm for LCL parameters calculation

```
clear all
close all
clc
%-------------------------------
%
%algoritm for LCL parameters calculation
%
%-------------------------------
fsw = 20e3;
wsw = 2*pi*fsw;
f = 50;
w = 2*pi*f;
Pn = 60e3;
Q_max = 0.05*Pn;
V_bus = 230*sqrt(2);
Xc = ((3*(V_bus)^2)/(Q_max));
Cf = 1/(Xc*w) %reactive power limit
Lg = 10e-6; %grid
Lm = 250e-6; %interleaved, inductance for single unit
Lboost = 0.5*Lm; %Leq
fres = 5e3; %put value here [ref 2kHz]
wris = 2*pi*fres;
format shortEng;
%f_ris = 1/(2*pi)*sqrt(1/Cf*(1/Lboost+1/Lf))
Lf = 1/((wris)^2*Cf-1/Lboost)

 if Lf<0
     return
 end

 rL = (Lf + Lg)/Lboost

  if 0.5 < rL && rL < 2.5
    ("optimal value")
  end
Rf = 1/(3*wris*Cf)
Risultati=fopen ("Risultati_filter_parameters.txt","w+");
              fprintf(Risultati,"f_ris = %f Hz  \n", fres);
              fprintf(Risultati,"Rf = %f ohm\n", Rf);
              fprintf(Risultati,"Cf = %f F  \n", Cf);
              fprintf(Risultati,"Lboost = %f  H  \n", Lboost);
              fprintf(Risultati,"L = %f H  \n", Lf);
              fprintf(Risultati,"Lg = %f H  \n", Lg);
              fprintf(Risultati,"rL = %f [-] \n", rL);
              fclose(Risultati);

wf=sqrt(1/(Cf*(Lf+Lg)));
chi_f = 0.5*Cf*Rf*wf;
chi_0 = 0.5*Cf*Rf*wris;
L_bw = Lboost + Lf + Lg
L_tot = Lboost + Lf + Lg;
```

A7. Algorithm for LCL plots

```
%%
%transfer function
s = tf('s');
numerator = [1 2*chi_f*wf wf^2];
denominator = [Lboost 2*chi_0*wris*Lboost Lboost*wris^2 0];
sys = tf(numerator,denominator); %stability with damping
lambda = eig(sys);
lambda_1 = lambda (1);
lambda_2 = lambda (2);
lambda_3 = lambda (3);
lambda_real_1 = real (lambda_1);
lambda_real_2 = real (lambda_2);
lambda_real_3 = real (lambda_3);

%stability_check
if lambda_real_1 > 0
   return
end
if lambda_real_2 > 0
   return
end
if lambda_real_3 > 0
   return
end
figure (1)
bodeplot (sys);
title('Stability BODE plot of the G_{plant}(s)')
[mag,phase,wout] = bode(sys);
%transfer function of the filter
p = tf ('p');
numerator_filter = [2*chi_0*wris wris^2];
denominator_filter = [L_tot 2*L_tot*chi_0*wris L_tot*wris^2 0];
filterLCL = tf(numerator_filter,denominator_filter) %filter_trasfer_function

figure (2)
bodeplot (filterLCL);
title('LCL filter BODE plot G_{filter}(s)')
[mag,phase,wout] = bode(filterLCL);
[Mg, Mph, wgain, wcrossover] = margin (filterLCL) %gain margin, phase margin, Mf(w) and corner
frequency
if Mph > 145;
   return
end

value = [50 20000 40000 60000 80000 100000 120000]; %frequencies vector
[tmp, f]=bode(filterLCL,value');
m=20*log10(tmp);
attenuation = [m(:),f(:), value'] %attenuation at a certain frequency value
```

A8. C routine for PI current control for all the current loop of the converter

```
//State machine
switch(State)
{
        case ERROR:
        EnablePWM_AFE=0;
        EnablePWM_AFE2=0;
        CrtReg1.integral=0.0;
        CrtReg2.integral=0.0;
        CrtReg3.integral=0.0;
        iRefPk=0.0;
        CrtReg4.integral=0.0;
        CrtReg5.integral=0.0;
        CrtReg6.integral=0.0;
        iRefPk2=0.0;
        //VLTReg0.integral=0.0;
        //VLTReg.integral=0.0;
if (Enable>0.5)
          State=GO;
break;
        case GO:
        EnablePWM_AFE=1;
        EnablePWM_AFE2=1;
        vMax=vdc*sqrt3_inv;
        vMax2=vdc*sqrt3_inv;
//Current control
tmp1=1.0/vpccPk;
iabcRef1.a=(RefIn)*vabc.a*tmp1;
iabcRef1.b=(RefIn)*vabc.b*tmp1;
iabcRef1.c=(RefIn)*vabc.c*tmp1;

//Phase 1a (equal for other 1b, 1c, 2a, 2b, 2c phases and units)
CrtReg1.ref=iabcRef1.a;
CrtReg1.actual=iabc1.a;
CrtReg1.kp=kpi;
CrtReg1.ki=kii;
CrtReg1.lim=vMax;
CrtReg1.vfw=-vabc.a;
PIReg(&CrtReg1);
vabcRef.a=-CrtReg1.out;
```

A9. Current control parameters setup

```
//-------------------------------------------
//Filename:    UserSetup.h
//Description:  header file containing control routines
//-------------------------------------------
//Define general purpose constants
#define double_pi          6.2831853
#define pi                 3.1415926
#define sqrt2              1.4142135
#define sqrt3              1.7320508
#define sqrt2_inv          0.7071067
#define sqrt3_inv          0.5773502
#define one_over_pi        0.31830988
#define one_third          0.33333333
//Sampling time
#define fsw 20000.0
#define fs 20000.0
#define Ts (1.0/fs)
//Define states
#define ERROR              0
#define SOFT_START         1
#define GO                 2
//Define DC voltage ramp
#define DUTY_MIN           0.0
#define DUTY_MAX           1.0
//Modulation limits
//Filters cut-off frequencies
#define f_ris              5000
//Grid
#define Vrms               220.0
//Input inductor current loop
#define IntLim                  200.0
#define f_band_current          (fs/20.0) //1kHz
#define L                       (181e-006)
#define f_zero_current          (f_band_current/2.0)
#define kpi                     (double_pi*f_band_current*L)
#define kii                     (double_pi*f_zero_current*kpi)
```

A10. Voltage control parameters setup

```
//DC-link Voltage Loop Tuning
#define Cdc                     (4080e-6)
#define f_bw_voltage            (f_bw_current/10.0)
#define f_z_voltage             (f_bw_voltage/5.0)
#define kpv                     (double_pi*f_bw_voltage*Cdc/2)
#define kiv                     (double_pi*f_z_voltage*kpv)

//Mid-Point Voltage Loop Tuning
#define f_bw_balance            (150/10)
#define f_z_balance             (f_bw_balance/2.0)
#define kpb                     (double_pi*f_bw_balance*Cdc)
#define kib                     (fs/150*double_pi*f_z_balance*kpb)
```

A11. C routine for PI voltage control

```
//Read inputs
iabc.a = InputSignal(0,0);
iabc.b = InputSignal(0,1);
iabc.c = InputSignal(0,2);
vab = InputSignal(0,3);
vbc = InputSignal(0,4);
vP = InputSignal(0,5);
vN = InputSignal(0,6);
Enable = InputSignal(0,7);
Ref = InputSignal(0,8);
Mod = InputSignal(0,9);

//DC-Link Voltage
vdc = vP + vN;
//Mid-Point Voltage
vM = vP - vN;
//Maximum Output Voltage
vMax = vdc*sqrt3_inv;

//Resonant Filter on the PCC Voltages
tmp1 =  a1res1*x1res_vab + a2res1*x2res_vab + b1res1*(vab-vabFilt);
tmp2 = -a2res1*x1res_vab + a1res1*x2res_vab + b2res1*(vab-vabFilt);
x1res_vab = tmp1;
x2res_vab = tmp2;
vabFilt = x1res_vab;

tmp1 =  a1res1*x1res_vbc + a2res1*x2res_vbc + b1res1*(vbc-vbcFilt);
tmp2 = -a2res1*x1res_vbc + a1res1*x2res_vbc + b2res1*(vbc-vbcFilt);
x1res_vbc = tmp1;
x2res_vbc = tmp2;
vbcFilt = x1res_vbc;

vca = -(vab+vbc);
valphabeta.alpha = (vab-vca)*one_third;
valphabeta.beta = vbc*sqrt3_inv;
vPCCpk = sqrt(valphabeta.alpha*valphabeta.alpha+valphabeta.beta*valphabeta.beta);

//First Harmonic
sincosTheta.sin = valphabeta.beta/vPCCpk;
sincosTheta.cos = valphabeta.alpha/vPCCpk;
theta = atan2(sincosTheta.sin,sincosTheta.cos);
//Third Harmonic
theta3 = 3*theta;
sincosTheta3.sin = sin(theta3);
sincosTheta3.cos = cos(theta3);
//Moving Average
signSinTheta3Old = signSinTheta3;
signSinTheta3 = sgn(sincosTheta3.sin);
FlagVmLoop = 0;
vMsum += vM;
vMcounter++;
```

```
if (signSinTheta3>signSinTheta3Old)
{       FlagVmLoop = 1;
        vMavg = vMsum/vMcounter;
        vMsum = 0.0;
        vMcounter = 0;      }
vMin = 0.975*sqrt3*vPCCpk;
if (vMin < 500)
        vMin = 500;
//Current Transformations
DirectClarke(&iabc,&ialphabeta);
DirectRot(&ialphabeta,&sincosTheta,&idq);

//State Machine
switch(State)
{       case ERROR:
        EnablePWM = 0;
        EnableLoad = 0;
        CrtReg1.integral = 0.0;
        CrtReg2.integral = 0.0;
        VltReg1.integral = 0.0;
        VltReg2.integral = 0.0;
        if (Enable>0.5) {
                if (vdc<vMin) {
                        State = SOFT_START;
                        }
                else {
                        State = GO;
                        }
        }
        break;
        case SOFT_START:
                SoftStart1 = 1;

                if (vdc<vMin) {
                        SoftStart2 = 0;
                        }
                else {
                        SoftStart2 = 1;
                        State = GO;
                        }
                        break;
        case GO:
        SoftStart1 = 0;
        EnablePWM = 1;
        EnableLoad = 1;

//DC-Link Voltage Control
VltReg1.ref = Ref;
VltReg1.actual = vdc;
VltReg1.kp = kpv;
VltReg1.ki = kiv;
VltReg1.lim = IdcMax;
VltReg1.vfw = 0.0;
```

```
PIReg(&VltReg1);
idqRef.d = VltReg1.out * (vdc)/(1.5*vPCCpk); //dq-frame reference with power balance
idqRef.q = 0.0;

        //Mid-Point Voltage Control (executed every 150 Hz)
        if (FlagVmLoop==1)
        {       VltReg2.ref = 0;
                VltReg2.actual = vMavg;
                VltReg2.kp = kpb;
                VltReg2.ki = kib;
                VltReg2.lim = IdcMax;
                VltReg2.vfw = 0.0;
                PIReg(&VltReg2);
                duty0Reg = pi/12/idq.d*VltReg2.out;       }

        //d-Axis Current Control
        CrtReg1.ref = idqRef.d;
        CrtReg1.actual = idq.d;
        CrtReg1.kp = kpi;
        CrtReg1.ki = kii;
        CrtReg1.lim = vMax;
        CrtReg1.vfw = -vPCCpk;
        PIReg(&CrtReg1);
        vdqRef.d = -CrtReg1.out;
        //q-Axis Current Control
        CrtReg2.ref = idqRef.q;
        CrtReg2.actual = idq.q;
        CrtReg2.kp = kpi;
        CrtReg2.ki = kii;
        CrtReg2.lim = vMax;
        CrtReg2.vfw = 0.0;
        PIReg(&CrtReg2);
        vdqRef.q = -CrtReg2.out;

        //Duty Cycle Calculation
        InvRot(&vdqRef,&sincosTheta,&valphabetaRef);
        InvClarke(&valphabetaRef,&vabcRef);
switch (Mod)
{       case 1:
                SVPWMCompute(&vabcRef,&duty0,&vdc);
        break;
        case 2:
                ZMPCPWMCompute(&vabcRef,&duty0,&vdc);
        break;
        case 3:
                TLSVPWMCompute(&vabcRef,&duty0,&vdc);
        break;
        case 4:
                D30PWMCompute(&vabcRef,&duty0,&vdc);
        break;
        }
```

```
// Common-Mode Duty Cycle
duty0 = duty0 + duty0Reg;
//Duty Cycles
duty.a = (0.5+vabcRef.a/vdc) + duty0;
duty.b = (0.5+vabcRef.b/vdc) + duty0;
duty.c = (0.5+vabcRef.c/vdc) + duty0;
//Duty Cycle Saturation
        DutySaturation(&duty);
        break;
}
```

A12. C routine duties calculation for voltage control

```
//total duty
duty1.a=duty1.a+duty0;
duty1.b=duty1.b+duty0;
duty1.c=duty1.c+duty0;
duty2.a=duty2.a+duty0;
duty2.b=duty2.b+duty0;
duty2.c=duty2.c+duty0;
//duty saturator
        if (duty1.a>DUTY_MAX)
                duty1.a=DUTY_MAX;
        if (duty1.a<DUTY_MIN)
                duty1.a=DUTY_MIN;

        if (duty1.b>DUTY_MAX)
                duty1.b=DUTY_MAX;
        if (duty1.b<DUTY_MIN)
                duty1.b=DUTY_MIN;

        if (duty1.c>DUTY_MAX)
                duty1.c=DUTY_MAX;
        if (duty1.c<DUTY_MIN)
                duty1.c=DUTY_MIN;
        if (duty2.a>DUTY_MAX)
                duty2.a=DUTY_MAX;
        if (duty2.a<DUTY_MIN)
                duty2.a=DUTY_MIN;

        if (duty2.b>DUTY_MAX)
                duty2.b=DUTY_MAX;
        if (duty2.b<DUTY_MIN)
                duty2.b=DUTY_MIN;

        if (duty2.c>DUTY_MAX)
                duty2.c=DUTY_MAX;
        if (duty2.c<DUTY_MIN)
                duty2.c=DUTY_MIN;
        break;
}
```

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