POLITECNICO DI TORINO

III Facoltà di Ingegneria

Corso di Laurea in Ingegneria Elettronica

Tesi di Laurea Magistrale

Ultralow area and power self-localization in sensor motes

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Anno accademico 2017-2018

Summary

The self-localization problem is becoming every day much more important especially with autonomous cars/robots. Since these devices has to work without any supervision, they need to know constantly which is their position inside the space where they are moving.

This problem can be solved in many different ways and using many technologies. However there is not a better method: the quality of the solution is related mainly to the application where it is adopted.

This thesis proposes a new approach to this problem and design a circuit in order to accomplish the task. On the contrary of the standard solution adopted in literature, the design of the circuit has been done using an analog electronics rather than digital one. This allows to keep the structure as small, giving the opportunity to produce a final device that can be used in many different applications (from robotics to medicine). The analog approach guarantees also a low power consumption, particular important where the device has not a big battery.

After the theory and the circuit, it is proposed the design of the main components (OTA and OpAmp) needed to implement the circuit. In particular the OTA has to exploit all the input available and the output curve has to be as linear as possible in order to fit inside the design. Then both the OTA and the OpAmp have been implemented and simulated.

At the end, it is shown an example of the results expected by the theory and the one derived from the simulation.

Acknowledgements

I would thank all the people that helped me during the thesis with suggestions and observations.

First of all I would thank my UIC advisor, Amit Ranjan Trivedi, for the constant help and support during all the time. I would thank also Mariagrazia Graziano for having accepted to be my advisor for Politecnico di Torino.

My thought goes immediately to my parents. Without their support and help, I would not be here today. Thank you for everything you have done!

A special mention is for Laura Palmieri that helped me during these months with moral and bureaucratic help. I also want to thank Marco Mele, my trip mate in Canada (with Laura and Giorgia) and California during these months in the US. It has been a pleasure visit the US with you and spend many evenings visiting Chicago. I'm also grateful to the other Italian friend that has filled my days and holidays, avoiding me to feel nostalgic of home. Thank you guys!

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Chapter 1

State of the Art

1.1 Sensor motes

"A sensor mote is a node inside a sensor network that can perform processing, gather information and communicate with other motes in the network" [1]. Sensor motes are the key part of a Wireless Sensor Network (WSN).

In Figure 1.1, it is presented the common structure of a sensor motes. Most of the sensor motes adopt a digital structure.

1.1.1 Sensor motes internal structure

The internal structure of a standard sensor mote design using digital electronics is analyzed. Normally it has 5 components.

1. "The controller performs tasks, processes data gathered by the sensors and controls the functionality of other components" [1]. The most common controller adopted is a microcontroller because it is cheap, flexible, easy to program and it needs few energy to work (this means a smaller battery and a smaller overall device). Other options for the controller are: a general purpose microprocessor, digital signal processors (DSPs), FPGAs and ASICs. However these alternatives has some drawbacks with the respect to a microcontroller. A general purpose microprocessor has a higher power consumption generally and in sensor motes application where the low power factor is crucial this is a big problem. Digital Signal Processors (DSPs) are used especially for broadband wireless communication applications, but in general the communication in sensor motes network is quite limited. Then FPGAs are very versatile (it is possible to reconfigure and reprogram them), but they have a high cost per unit and also the power consumption is not contained. Finally ASICs are probably

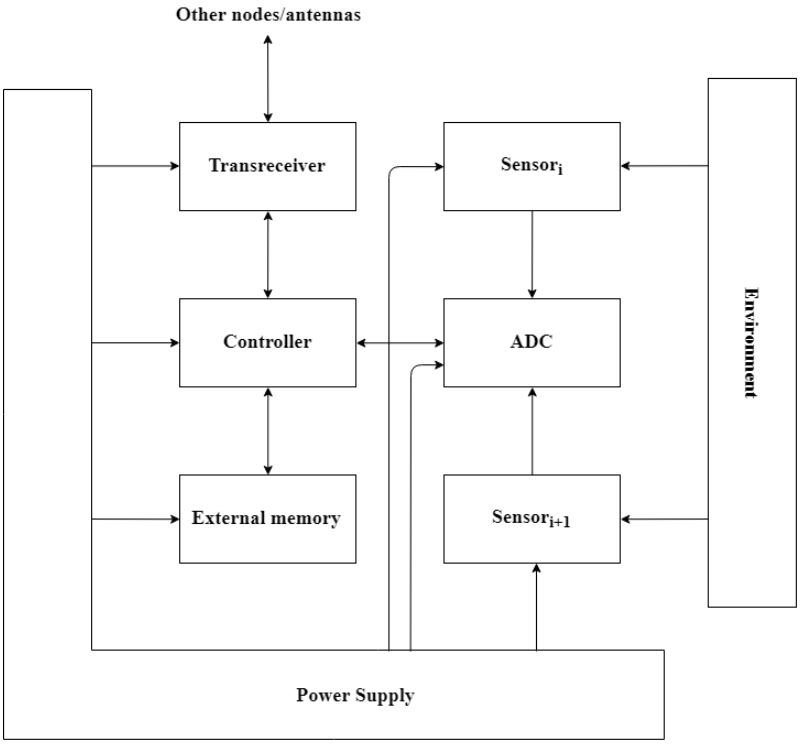

Figure 1.1: Scheme of a sensor mote structure

the best solution in term of power consumption and area, but it is necessary to spend more time in the design process compared to a microcontroller.

2. The external memory contains the program executed by the microprocessor and store the input data and the data processed. The most used technology is flash memory due to its cost and storage capacity.

3. Sensors gather data from the environment and they are hardware devices that transform a physical quantity (i.e. air pressure, temperature, ecc) into an electrical quantity (voltage or current). In particular sensors differ in terms of accuracy, precision, drift, linerarity and sensitivity. The continuous analog signal produced by the sensors is then digitized by an ADC (analog to digital converter). Sensors are classified in two main categories:

   - passive sensors, that gather data from the environment without manipulating it (i.e. temperature sensors);
   - active sensors, that perform an operation to modify the environment (i.e. actuators or radars).

4. A transreceiver is a device that embeds the functionality of a transmitter and a receiver at the same time. It is used to transmit and receive data from antennas or other motes. The possible choices of wireless transmission are radio frequency (RF), optical communication (laser) and infrared.

5. In order to power up all the devices inside the sensor motes, it is necessary have a power supply, that consists in a battery. This device grants power to all the other components in order to perform their tasks.

1.1.2 Examples

As written in the previous subsection, most of the sensor motes have a digital architecture, since it is easier to design, prototype, maintain and it is also noise tolerant with the respect to the analog counterpart. However there are some drawbacks. The most important one are the higher power consumption and a bigger area occupation. This is due to the fact that digital design uses mainly standard cells, while in analog design design is particularly designed for this purpose. The same consideration can be applied again for the power consumption.

1.2 Self-Localization State of the Art

Nowadays self-localization has a very key role in many systems and it is finding many more application every day. The problem can be solved in many different ways and for this reason there is not a better absolute solution because it depends on the context where the self-localization in inserted into.

1.2.1 Introduction

First it is necessary to understand what is self-localization, before explaining any solution adopted.

Self-localization means that an object is capable to retrieve his position automatically without any external help. This is necessary because a manual calibration of the position is not always possible (it is also a very time consuming operation) and sometimes it is not possible to equip the object with antennas in order to communicate its absolute position. For this reason methods of self-localization that use relative information (i.e. obtained from received signal strength or time delay between sensors) and some absolute information are in general preferred [2].

1.2.2 Solutions adopted

In order to perform self-localization, it is necessary to have a circuitry capable to perform computation in order to retrieve the position. There two possible approaches are: analog and digital.

In literature there is not any presence of solving the problem using the analog approach using any standard CMOS technology. There are different motivation behind this choice. First, as written before, the analog approach requests more effort in the design phase; this involves a longer design phase for a circuit, build specifically for the task. In terms of costs for the company that needs the sensor, this will be a huge cost, even if the analog circuit will have a smaller area and a reduced power consumption.

However recently the trend is changing. Nowadays the WSNs are composed by very small nodes (especially in case of smart dust or in biomedical applications), that cannot have complex digital circuits since there batteries have the space constraint. The reduced amount of power available makes impossible to power up all the components presents in a digital node (controller, external memory, transreceiver, ecc).

Moreover existing technologies cannot precisely find the location of microscale devices inside the body and establish a communication with it specifically. Current techniques based on radio frequency signals have a limited resolution and possibility to track devices inside a body because of the different properties of the material where the signals have to travel (i.e. air, skin, blood, water, ecc).

For this reason, designers are starting to explore the analog approach and even new technologies like magnetic spin technology embedded in silicon-integrated circuits realized by using a standard CMOS process [3]. In this way by applying a local magnetic field will shift the output frequency of the devices. So, measuring the magnetic file gradient, it is possible to find the accurate position of the device inside the body with a resolution of $\sim 100\,\mu m$. By integrating the circuit in a device smaller that 0.7 mm^3, it is possible to build an indigestible/injectable sensor that can perform specific tissue or blood analysis knowing the exact position inside the body of the patient.

The basic device built with CMOS technology is called ATOMS (Addressable transmitters operated as magnetic spins). As written before, when a magnetic field gradient is applied, spins in a certain position resonate at a different frequency from others at another location. Using ATOMS to copy the behavior of nuclear spins, it is possible to localize the device using magnetic field. After done that, a local RF signal communication is established in order to exchange data. The great advantage is that multiple devices can be tracked in parallel even if they are in different locations. Moreover, with the respect to MRI, it is not necessary to have a strong static magnetic field.

In spite of the use of new technologies, the main approach used in self-localization is still the digital one. The reason is that self-localization is needed mainly in autonomous driving objects like drones and robots. Autonomous driving cars uses an absolute self-localization method (GPS) and they do not have any power issue thanks to the batteries present in them. In literature there are many example of self-localization techniques done by using this approach.

In the case where the object is inside a known environment, the self-localization can be solved simply using maps. The maps and the starting point are loaded inside the object and, by keeping track of the movements, it is possible to know the position every moment. An example of this method is described in [4]. Unfortunately this is is possible only in the case where the environment is known a priori. The following solutions provide some techniques that can be applied also in case of unknown environments.

In [5], a robot, that can independently move in 2D plane, can localize itself using camera images and optical flow calculation. In this case the the camera is used as a velocity sensor. This method is more reliable with the respect to dead reckoning[1] because in omni-directional robot, it is easy that the current position drift from the original one. However this method has the drawback to be computational intense since optical flow consists in subtracting two consecutive images. For this reason in [5] the overall architecture consists in a camera and a FPGA.

Another solution, proposed in [4], solve the problem of self-localization in small autonomous robots. The system designed especially for condition where the robots could have instability and undesired movements (i.e. collisions), that can affect the correctness of the localization in many simpler methods. The system works exploiting the combination between azimuth, retrieved from an analog compass, and odometry from an optical PC mouse.

There are also theoretical approaches that have been proposed. In particular, the ones that exploit machine learning techniques in order to be implemented require a digital architecture due to the big amount of computation needed to solve the problem.

An example is [6], where passive RFID and machine learning are combined. The environment is filled with RFID tags with unidentified location; when the device (i.e. a robot) is in the proximity the data are gathered and using support vectors machines (SVM) the final location is computed.

Finally there is the group of self-localization techniques inside WSNs (which is the case that is most similar to the argument of the thesis). This problem can be

[1]Dead reckoning is the process of calculating an object current position by using a previous known position and the estimated speed over an elapsed time and path. It has been been used for centuries by navigators.

solved in different ways: using Taylor series [7], least square [8] or machine learning [9]. The last one gathers many different solutions for self-localization done with machine learning.

The most interesting to focus on is [8] because solve the problem using least square, that is the same technique adopted in the thesis case. This technique is adopted in order to reduce as much as possible the errors. The range-free algorithm used is composed by three different steps. The first one is the estimation of the distance between the sensor node and beacon node. The second one is to calculate the localization of the sensor node with trilateration [2]. The last step consists of optimizing the result through an iterative method.

Using this method are necessary at least three beacon in order to successfully retrieve the position. However the estimation error increases when more beacon are present. For this reason

Inside the algorithm the numbers and distribution of the beacons are particularly important in order to enhance the precision of the localization. For this reason only the beacons with smaller errors are selected, while the other beacons are discarded. It is important to remember that in trilateration are necessary at least three nodes in order to find the localization (only the three best nodes are kept). Unfortunately, due to estimation error, the intersection of the localization circle of the three beacons is not a point as in the ideal case, but an area. So the problem of improving the localization accuracy becomes a problem of making this particular area as small as possible. The solution proposed consists of estimating the distance between objects and beacons, creating a grid and a beacon distribution and finally solve it using the least square method.

Even if applied to two different concepts (the thesis proposed and [8]), the least square methods is used to obtain the same goal: reduce as much as possible the error in order to obtain the best localization.

1.2.3 Applications

As written in the previous subsection, there are multiples applications for the application of the self-localization sensors. The most straight forward one is the implementation of this sensors inside robots. In this way, it is possible for the robots to know its exactly position and so decide which is the following movement to make in order to complete the task. This is particularly useful especially in the case of the WSNs where there are multiple sensors connected. For instance, knowing the position can avoid collisions inside a swarm of drones or the best route to follow to

[2]Trilateration is the process to determine the locations of points by measurement of distances, using the geometry of circles or triangles. The position computed can be absolute or relative.

reach the target.

Other applications are in the biomedical field. In this case, the chip integration has to be maximum because the amount of power and area available are a bigger constraint compared to other applications. In this case it is possible to perform medical analysis inside a specific body location in order to know the health status of an organ.

Chapter 2

Analog approach to Self-Localization

2.1 Mathematical model for 2D localization

In this section, it is present the mathematical framework to self-localize sensor nodes.

The target's location, defined as $[x_s, y_s]$, is estimated from angle of arrival (AOA) measurements taken from M beacons that have a known location. The spatial coordinates of anchors are defined as $[x_i, y_i] \in i = 1, ..., M$. So, if AOA from a beacon "i" is α_i, target's location is related to beacon's location as

$$\sin(\alpha_i) \cdot x_s - \cos(\alpha_i) \cdot y_s = \sin(\alpha_i) \cdot x_i - \cos(\alpha_i) \cdot y_i \tag{2.1}$$

Extending from one beacon to all the M beacons, this leads to the following system of linear equation

$$\begin{bmatrix} \sin(\alpha_1) & -\cos(\alpha_1) \\ \vdots & \vdots \\ \sin(\alpha_M) & -\cos(\alpha_M) \end{bmatrix} \begin{bmatrix} x_s \\ y_s \end{bmatrix} = \begin{bmatrix} \sin(\alpha_1) \cdot x_1 - \cos(\alpha_1) \cdot y_1 \\ \vdots \\ \sin(\alpha_M) \cdot x_M - \cos(\alpha_M) \cdot y_M \end{bmatrix} \tag{2.2}$$

Assuming absence of noise, Equation 2.2 is consistent. Unfortunately, since there is noise presence in AOA measurements, the system has to be solved using least square method. So the Equation 2.2 is written as:

$$\begin{aligned} \begin{bmatrix} f_1 \\ \vdots \\ f_M \end{bmatrix} &= \begin{bmatrix} \sin(\alpha_1) \cdot x_s - \cos(\alpha_1) \cdot y_s \\ \vdots \\ \sin(\alpha_M) \cdot x_s - \cos(\alpha_M) \cdot y_s \end{bmatrix} - \begin{bmatrix} \sin(\alpha_1) \cdot x_1 - \cos(\alpha_1) \cdot y_1 \\ \vdots \\ \sin(\alpha_M) \cdot x_M - \cos(\alpha_M) \cdot y_M \end{bmatrix} \\ &= \begin{bmatrix} \sin(\alpha_1) & -\cos(\alpha_1) & -\sin(\alpha_1) \cdot x_1 + \cos(\alpha_1) \cdot y_1 \\ \vdots & \vdots & \vdots \\ \sin(\alpha_M) & -\cos(\alpha_M) & -\sin(\alpha_M) \cdot x_M + \cos(\alpha_M) \cdot y_M \end{bmatrix} \begin{bmatrix} x_s \\ y_s \\ 1 \end{bmatrix} \end{aligned} \tag{2.3}$$

In order to estimate the location of the sensor estimated, it is used the following function

$$[x_s, y_s] = argmin \left\{ \sum_{i=1}^{M} f_i^2 \right\} \tag{2.4}$$

Supposing that $H = \sum_{i=1}^{M} f_i^2$, the total error is minimized when $\frac{dH}{dt} = 0$. However, since $H \geq 0$ (beacuse it is the sum of squares), $\frac{dH}{dt} \leq 0$ is also a sufficient condition to minimize H. $\frac{dH}{dt}$ is expressed as

$$\begin{aligned} \frac{dH}{dt} = \begin{bmatrix} x_s & y_s & 1 \end{bmatrix} & \begin{bmatrix} \sin(\alpha_1) & -\cos(\alpha_1) & \sin(\alpha_1) \cdot x_1 - \cos(\alpha_1) \cdot y_1 \\ \vdots & \vdots & \vdots \\ \sin(\alpha_M) & -\cos(\alpha_M) & \sin(\alpha_M) \cdot x_M - \cos(\alpha_M) \cdot y_M \end{bmatrix}^T \\ & \begin{bmatrix} \sin(\alpha_1) & -\cos(\alpha_1) \\ \vdots & \vdots \\ \sin(\alpha_M) & -\cos(\alpha_M) \end{bmatrix} \begin{bmatrix} \frac{dx_s}{dt} \\ \frac{dy_s}{dt} \end{bmatrix} = 0 \end{aligned} \tag{2.5}$$

The following inequality implies $\frac{dH}{dt} \leq 0$,

$$\begin{aligned} \begin{bmatrix} \frac{dx_s}{dt} \\ \frac{dy_s}{dt} \end{bmatrix} = - & \begin{bmatrix} \sin(\alpha_1) & -\cos(\alpha_1) \\ \vdots & \vdots \\ \sin(\alpha_M) & -\cos(\alpha_M) \end{bmatrix}^T \\ & \begin{bmatrix} \sin(\alpha_1) & -\cos(\alpha_1) & \sin(\alpha_1) \cdot x_1 - \cos(\alpha_1) \cdot y_1 \\ \vdots & \vdots & \vdots \\ \sin(\alpha_M) & -\cos(\alpha_M) & \sin(\alpha_M) \cdot x_M - \cos(\alpha_M) \cdot y_M \end{bmatrix} \begin{bmatrix} x_s \\ y_s \\ 1 \end{bmatrix} \end{aligned} \tag{2.6}$$

Equation 2.6 can be arranged as

$$\begin{aligned} \begin{bmatrix} \frac{dx_s}{dt} \\ \frac{dy_s}{dt} \end{bmatrix} = - & \begin{bmatrix} \sum_{i=1}^{M} \sin^2(\alpha_i) & -\sum_{i=1}^{M} \sin(\alpha_i) \cdot \cos(\alpha_i) \\ -\sum_{i=1}^{M} \sin(\alpha_i) \cdot \cos(\alpha_i) & \sum_{i=1}^{M} \cos^2(\alpha_i) \end{bmatrix} \begin{bmatrix} x_s \\ y_s \end{bmatrix} + \\ & - \begin{bmatrix} \sum_{i=1}^{M} [-\sin^2(\alpha_i) \cdot x_i + \sin(\alpha_i) \cdot \cos(\alpha_i) \cdot y_i] \\ \sum_{i=1}^{M} [-\sin(\alpha_i) \cdot \cos(\alpha_i) \cdot x_i - \cos^2(\alpha_i) \cdot y_i] \end{bmatrix} \end{aligned} \tag{2.7}$$

Equation 2.7 is abbreviated as

$$\begin{bmatrix} \frac{dx_s}{dt} \\ \frac{dy_s}{dt} \end{bmatrix} = -A \begin{bmatrix} x_s \\ y_s \end{bmatrix} - B \tag{2.8}$$

The convergence of Equation 2.8 is guaranteed if A has all non-negative Eigen values. The eigen values of A are computed as

$$\lambda = \frac{A_{11} + A_{22} \pm \sqrt{(A_{11} - A_{22})^2 + 4A_{12}^2}}{2} \tag{2.9}$$

Note that $A_{11} \geq 0$, $A_{22} \geq 0$. Moreover, $A_{11} + A_{22} \geq \sqrt{(A_{11} - A_{22})^2 + 4A_{12}^2}$. The later implies due to,

$$A_{11}A_{22} - A_{12}^2 \geq 0 \tag{2.10a}$$

$$\left[\sum_{i=1}^{M} \sin^2(\alpha_i)\right]\left[\sum_{i=1}^{M} \cos^2(\alpha_i)\right] - \left[\sum_{i=1}^{M} \sin(\alpha_i) \cdot \cos(\alpha_i)\right]^2 \geq 0 \tag{2.10b}$$

Equation 2.10b can be simplified to obtain

$$\sum_{i=1}^{M}\sum_{j=1}^{M}\left[\frac{1}{2}\sin(\alpha_i - \alpha_j)^2\right] \geq 0 \tag{2.11}$$

For this reason, Equation 2.8 is guaranteed to converge, regardless the AOA set $\alpha_1, ..., \alpha_M$ at a sensor node.

2.2 Analog circuit for 2D localization

Once explained the mathematical model behind the 2D self-localization, it is necessary to design a circuit that can accomplish the task. In particular it has been developed an analog circuit because the area and the power consumed are less compared to an equivalent analog solution.

In Figure 2.1 it is proposed the analog solution designed. In order to retrieve the position using the two output voltages, it is necessary to tune the value of the current produced by the current generators, the value of the resistors and the value of the OTAs transconductances. In Table 2.1 there are the quantities that has tu be tuned in the circuit and the corresponding values.

Quantity	**Value**	**Simulation value**
gm_1	A_{12}	$A_{12} \cdot 10^{-9}$
gm_2	A_{12}	$A_{12} \cdot 10^{-9}$
I_1	$-B_{11}$	$-B_{11} \cdot 10^{-9}$
I_2	$-B_{21}$	$-B_{21} \cdot 10^{-9}$
R_1	$1/A_{11}$	$10^9/A_{11}$
R_2	$1/A_{22}$	$10^9/A_{22}$

Table 2.1: Values inside the analog circuit proposed

The circuit in Figure 2.1 is now analyzed. The discussion is done on the upper half of the circuit because since the structure is identical and the only difference is at the input of the OTAs.

In order to implement them in a simulation, both members in Equation 2.8 has to be multiplied by 10^{-9}.

Suppose that the current at the output port of the upper OTA is called I_{out1} and the voltage at negative input of the upper OpAmp is called V_{in1}. So the current in output of the OTA is defined as follows:

$$I_{out1} = gm \cdot (V_{ys}(t) - V_{cm}) = A_{12} \cdot 10^{-9} \cdot (V_{ys} - V_{cm}) \tag{2.12}$$

The current at the node in input of the negative terminal of the OpAmp is

$$I_1 + I_{out1} = -I_{R1} - I_{C1} \tag{2.13}$$

Substituting I_{C1} with the equation of the current inside a capacitor $\left(i = C\frac{dV(t)}{dt}\right)$, the final result is

$$-C_1 \cdot \frac{dV_{R1}(t)}{dt} + \frac{V_{R1}(t)}{R_1} = I_1 + I_{out1} \tag{2.14}$$

The solution to this equation is

$$V_{R1}(t) = R_1 \cdot (I_1 + I_{out1}) \left(e^{-\frac{R1}{C1} \cdot t} - 1\right) \tag{2.15}$$

The output voltage V_{xs} is defined as

$$V_{xs}(t) = A_v(V_{cm} - V_{in1}(t)) = A_v(V_{cm} - V_{xs}(t) - V_{R1}(t)) = \frac{A_v}{1 + A_v}(V_{cm} - V_{R1}(t)) \tag{2.16}$$

Substituting $V_{R1}(t)$ using the Equation 2.15 and the values in Table 2.1 doing some calculus, the final result is

$$\begin{aligned} V_{xs} = \frac{A_v}{1 + A_v} \Bigg[\left(1 - \frac{A_{21}}{A_{11}} \cdot \left(e^{-\frac{10^9}{A_{11} \cdot C1} \cdot t} - 1\right)\right) \cdot V_{cm} - \frac{B_{11}}{A_{11}} \cdot \left(e^{-\frac{10^9}{A_{11} \cdot C1} \cdot t} - 1\right) + \\ + \frac{A_{21}}{A_{11}} \cdot \left(e^{-\frac{10^9}{A_{11} \cdot C1} \cdot t} - 1\right) \cdot V_{ys}(t) \Bigg] \end{aligned} \tag{2.17}$$

For duality the V_{ys} can be find using the same steps and the final value is

$$\begin{aligned} V_{ys} = \frac{A_v}{1 + A_v} \Bigg[\left(1 - \frac{A_{21}}{A_{22}} \cdot \left(e^{-\frac{10^9}{A_{22} \cdot C2} \cdot t} - 1\right)\right) \cdot V_{cm} - \frac{B_{21}}{A_{22}} \cdot \left(e^{-\frac{10^9}{A_{22} \cdot C2} \cdot t} - 1\right) + \\ + \frac{A_{21}}{A_{22}} \cdot \left(e^{-\frac{10^9}{A_{22} \cdot C2} \cdot t} - 1\right) \cdot V_{xs}(t) \Bigg] \end{aligned} \tag{2.18}$$

Now there is a system of equation with two unknowns. This can be solved in order to find the final values of $V_{xs}(t)$ and $V_{ys}(t)$.

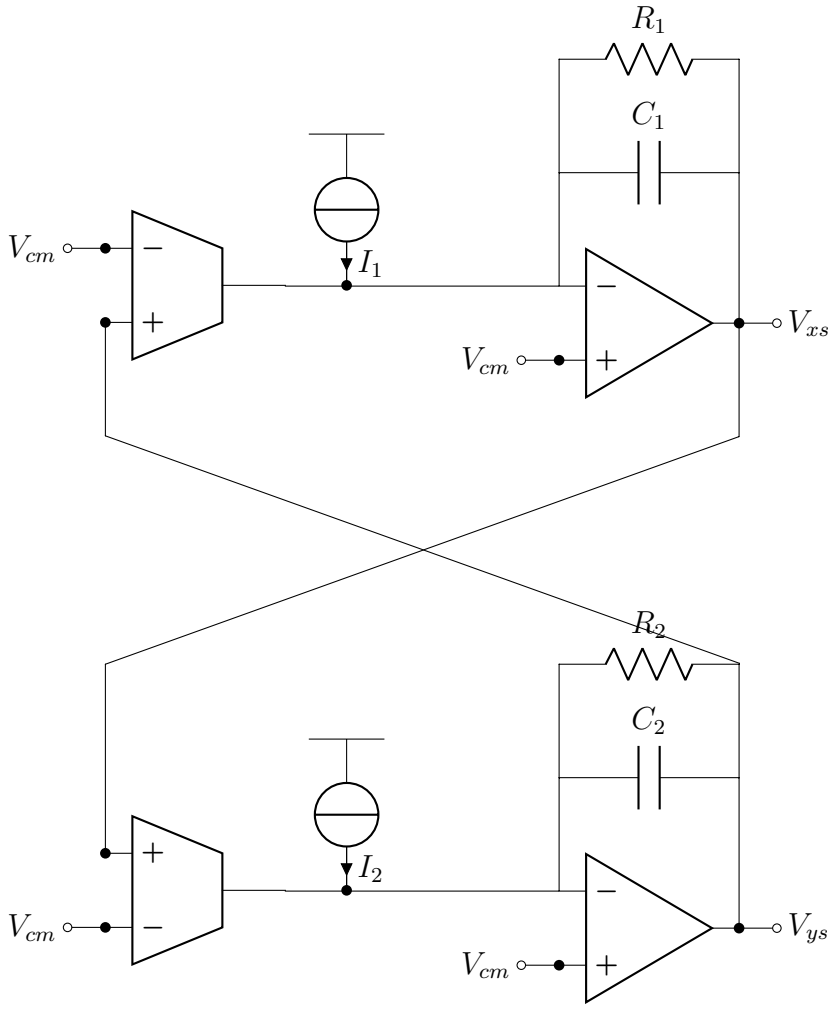

Figure 2.1: Schematics of the analog circuit for 2D self-localization

Chapter 3

OTA design

3.1 Basic concepts

The OTA is an amplifier where the differential input voltage is used to produced an output current. For this reason, it is a voltage controlled current source (VCCS). There is usually an additional input, called *Bias* in order to tune the transconductance. [10]

The OTA is usually composed by these inputs:

- V_+, the positive input voltage terminal;
- V_-, the negative input voltage terminals;
- V_{Bias}, the bias input terminal used to tune the g_m;
- V_{S+}, the input terminal for the positive supply voltage;
- V_{S-}, the input terminal for the negative supply voltage.

On the contrary, there is only one output:

- I_{out}, the output terminal where the output current is measured.

The basic OTA is described by the following the following equation:

$$I_{out} = g_m \cdot (V_+ - V_-) \tag{3.1}$$

where g_m is the OTA transconductance.

In 3.2 is showed the schematic symbol for the OTA.

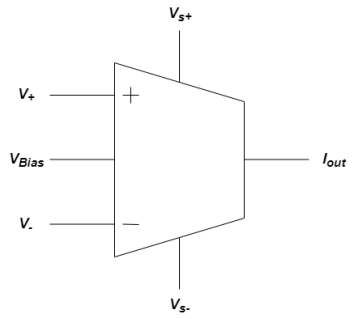

Figure 3.1: Schematic symbol for OTA

3.1.1 OTA design techniques

After having introduced the ideal OTA behavior, it is analyzed what are the design techniques to build an OTA. In particular, there are 3 main techniques:

- simple OTAs, composed in general by a differential stage as input and current mirrors to drive the current to the output [11];
- Miller compensated OTAs, where there are usually some DC voltage generators inside the circuit to compensate the output current [12];
- OTAs that uses well-driven transistor in the input stage [12][13].

The first technique is not often used today since it is difficult to achieve rail-to-rail input/output swing and because it is impossible to reach low-power consumption.

For this reason the second and the third are preferred. Furthermore the third is particularly useful where there is to achieve rail-to-rail input/output swing. This can be achieved because the well-driven transistors area used. Well-driven transistors are regular transistor where the input is applied to the well terminal instead of the gate. In 3.2.1, the behavior of this transistors will be explained.

Moreover, the second and the third techniques can be combined together as presented to achieve maximum power saving and rail-to-rail input/output swing at the same time [12][13].

3.2 OTA behavior

In the analog circuit for self localizing, as presented in the previous chapter, it is necessary an OTA with maximum rail-to-rail input/output swing in order to use all the voltage range available. For this reason the choice is an OTA that uses well-driven MOSFET transistors. Miller technique OTAs has not been considered since

the integration of DC voltage generators can be sometimes quite difficult to handle. Moreover the other requirements of the OTA is to be as more linear as possible.

Having listed all the constraint and the reason of the decision about the OTA tecnique choice, it is possible to start presenting the behavior of the component. The design has been taken from [13] and only some modifications has been made in order to adapt the component to the analog circuit for 2D self-localization.

In [13], four techniques has been used in order to obtain a wider linear range as possible. As written before, first it is necessary to use the well terminal of the transistors. After that, other techniques known as source degeneration [14] and gate degeneration are used in order to enhance the linerarity. The last technique used is called bump-linearization and it widens the current range as much as possible. The overall structure is composed by 13 transistors, ensuring that the power dissipation is very small.

The MOSFET linearity has been achieved especially in the above-threshold region. This region brings some problem, especially related to the current levels that become very high so that is necessary to use large capacitances or transistor with very small aspect ratio W/L to create low-frequency poles. This lead to a waste in term of power and area. However in this region it is easier to achieve a wide linear range.

Moreover in above-threshold operation, it is possible to use identities as $2(x-a)-2(x-b) = (b-a)(2x-a-b)$ to enhance the wide linear range even more. The current solution to this problem is to use the feedback technique of emitter degeneration to have a wide linear range and at the same time to reduce transconductance, as illustrated in [15].

[16] proposed a solution for widening the linear range of a bipolar transconductor that cancels nonlinearities up to fifth order and lower the transconductance. Another method, proposed and demonstrated by Chung [17], in order to have maximum linearity in a bipolar transconductor, is to use a translinear circuit and a resistor. However these two methods use resistors to achieve linearity, but unfortunately resistors are impossible to tune electronically.

A MOS device can be used as the resistive element (many authors have used it in this way) in an emitter-degeneration configuration to have a BiCMOS transconductor. The configuration proposed in [18] is a clear example.

A dilatation of the linear range in a differential pair can be achieved through the use of the simple technique of using a diode as source-degeneration factor. For example in [19], it is possible to notice that has been enhanced of more or less ± 150 mV.

There are other techniques to get a more linear range inside a differential pair. In particular, three of them are described in [20]. The point where the transconductance decrease by 1% becomes the definition for the linear range. Using that

supposition, the new output relation is $I_{out} = I_B \cdot \tanh\left(\frac{x}{V_L}\right)$ and the final range is $\frac{V_L}{5}$. This result is achieved by applying a common-mode biasing circuit, that has the drawbacks of occupying a huge amount of area and consuming power. On the other hand, the technique developed in [13] lead to have a $V_L = 1.7\,\mathrm{V}$ without using any additional circuit for the bias.

In order to have the lowest transconductance possible in [13], different techniques are used:

- well terminal, that is used as input of the amplifier (one of the techniques described in [12] and [13]). This input terminal has, in fact, an intrinsic low transconductance;
- source-degeneration, that is a very common technique adopted [14];
- gate-degeneration, that is a innovative technique, used the first time in [13];
- bump linearization, that is also an innovative technique, but it has been already used in [21].

The final structure uses all the listed techniques and it is shown in 3.2.

The two input are the well terminal of M3 and M4. The M3 well terminal corresponds to the negative input terminal and according to 2.1 the voltage V_{in} is applied. Vice versa the well input is the positive input terminal and the voltage V_{cm} is applied. The voltage V_{bias} is used to tune the bias current (and so also the transconductance) and the voltage V_{os} allows an offset adjustment. Moreover in this structure the M1 and the M2 transistors, by applying the source-degeneration technique, reduce the transconductance of M3 and M4. The same is done by the M5 and M6; they reduce the transconductance of M3 and M4 by applying the gate-degeneration technique.

In order to simplify the discussion about the OTA, only the first order effects are explained. There are higher degree effects, but for this thesis purpose are not relevant.

Before explaining the mathematical model behind [13], it is necessary to establish a symbol convention. The standard IEEE convention has been used. So the large-signal and DC large signal are written respectively as (i_{DS}) and (I_{DS}), while the small-signal are written as (i_{ds}).

It is important to remind that in this analysis in the first two subsections does not include the bump linearization transistors (M12 and M13 in 3.2).

3.2.1 Well-driven input transistors behavior

Starting from the first technique used, it is necessary to define the saturation current in a MOSFET transistor that uses the well as input terminal. This quantity is

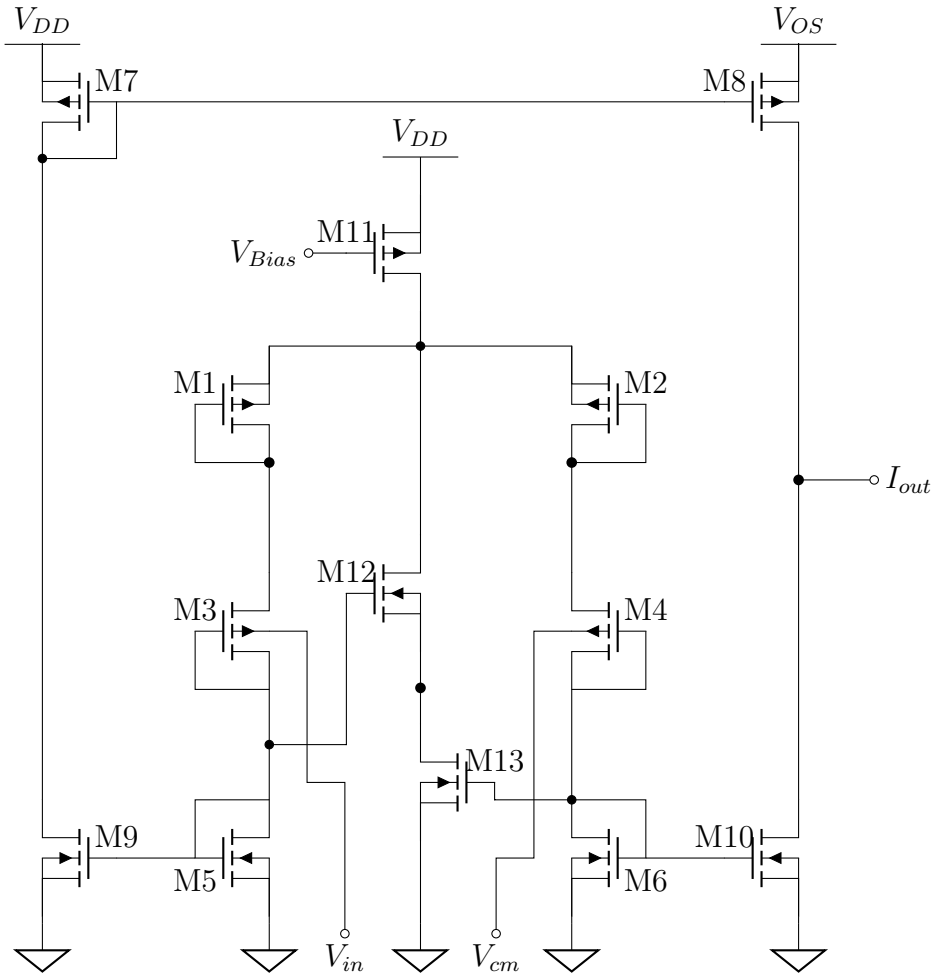

Figure 3.2: OTA internal circuit schematic

defined as

$$i_{DS} = I_0 \cdot \exp\left(-\frac{\kappa \cdot v_{GS}}{U_T}\right) \cdot \exp\left(-\frac{(1-\kappa) \cdot v_{WS}}{U_T}\right) \tag{3.2}$$

where v_{GS} is the gate-source voltage, v_{WS} is the well-source voltage, κ is the sub-threshold exponential coefficient, I_0 is the sub-threshold current-scaling parameter, $U_T = \frac{kT}{q}$ is the thermal voltage and $v_{DS} \gg 5U_T$.

It is possible to notice that in 3.2 the gate and the well influence the saturation current with two exponential terms: κ and $(1-\kappa)$, respectively. For this reason, the two quantities cannot work at the same time: when the gate is modulating the current, the well is ineffective, and vice versa.

Through the differentiation of 3.2, it is possible to retrieve the gate, well, and

source transconductances.

$$\begin{aligned} g_{gt} &= \frac{\partial i_{DS}}{\partial v_G} = \frac{i_{ds}}{v_g} = -\kappa \cdot \frac{I_{DS}}{U_T} \\ g_{wl} &= \frac{\partial i_{DS}}{\partial v_W} = \frac{i_{ds}}{v_w} = (1-\kappa) \cdot \frac{I_{DS}}{U_T} \\ g_s &= \frac{\partial i_{DS}}{\partial v_S} = \frac{i_{ds}}{v_s} = \frac{I_{DS}}{U_T} \end{aligned} \tag{3.3}$$

From 3.3, it is clear that if and only if $\kappa > 0.5$ (which happens most of the times) the well transconductance has a lower magnitude than the gate one. Thus the well is preferable over the gate in order to obtain a low transconductance input.

In order to simplify the discussion by using dimensionless small-signal variables. Supposing that i_d and v_d are arbitrary small-signal variables, it is possible to obtain the dimensionless variables:

$$i = \frac{i_d}{I_D} \qquad v = \frac{v_d}{U_T} \tag{3.4}$$

Using a relation such as

$$i_d = g_d \cdot v_d = \kappa \cdot I_D \cdot \frac{v_d}{U_T} \tag{3.5}$$

at the end the dimensionless quantity i can be expressed in the form

$$i = \kappa \cdot v \tag{3.6}$$

κ is comparable to a dimensionless transconductance, that is defined as

$$\kappa = \frac{g_d}{\frac{I_D}{U_T}} = g_d \cdot \frac{U_T}{I_D} \tag{3.7}$$

Most of the discussion in [13] is made using this dimensionless variable and it is convert back only at the end. So 3.3, if expressed with dimensionless variables, assume the form

$$\begin{aligned} g_{gt} &= -\kappa \\ g_{wl} &= -(1-\kappa) \\ g_s &= 1 \end{aligned} \tag{3.8}$$

In order to understand better, 3.3 and 3.4 show the schematic symbol of well transistor with the terminal name. In 3.5 it is shown the small signal circuit model of the well driven transistor and in 3.6 is present the block diagram derived from the small signal model circuit.

It is important to notice that in [13], the capacitances, that would be represented in a complete small-signal model of the well input transistor, are ignored.

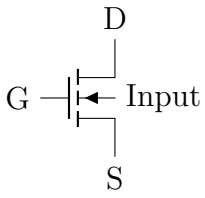

Figure 3.3: nMOSFET well-driven transistor

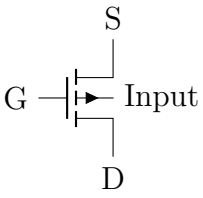

Figure 3.4: pMOSFET well-driven transistor

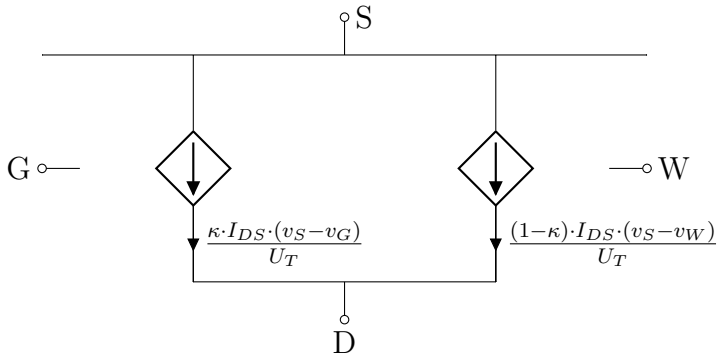

Figure 3.5: Small signal model for well-driven pMOSFET transistors

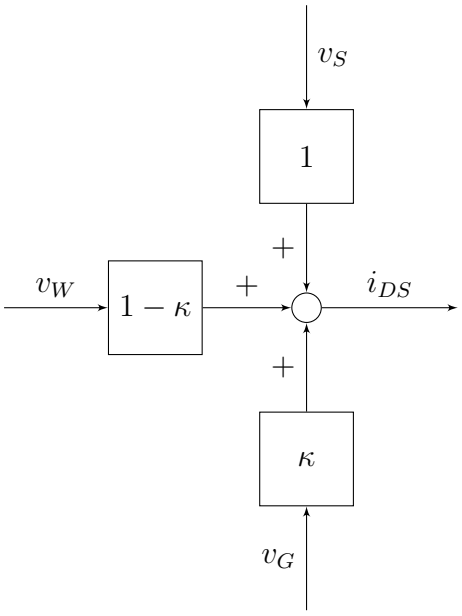

Figure 3.6: Block diagram of the well driven transistor

3.2.2 Degeneration techniques to achieve transconductance reduction

The second and the third techniques used in [13] are source and gate degeneration.

Source degeneration is already well known and widely used. In bipolar bipolar transistors it is called *emitter degeneration* [15]. "The idea behind *source degeneration* is to convert the current flowing through a transistor into a voltage through a resistor or diode, and then to feed this voltage back to the emitter or source of the transistor to decrease its current" [13].

On the contrary, *gate degeneration* is an innovative technique and no previous use have been done before [13]. The reason behind is that normally the gate is used as input terminal of the circuit and, for this reason, it is impossible to apply this degeneration technique. "The idea behind *gate degeneration* is to convert the current flowing through a transistor into a voltage through a diode, and then to feed this voltage back to the gate of the transistor to decrease its current" [13].

In 3.7, one arm of the differential pair of the circuit is analyzed in order to comprehend better the role of the degeneration. The upper node of the figure corresponds to the connection between the source of the M1/M2 transistors and the drain of the M11 transistor (see 3.2)

In 3.2, if $v_{cm} = v_{in}$ (and so $v_+ = v_-$) the amplifier is matched. A current of exactly $\frac{I_B}{2}$ flows inside each branch of the differential input stage and $i_{out} = 0$. Changing the differential voltage, defined as $vd = v_+ - v_- = v_{cm} - v_{in}$, by a small amount, the output current will be different and in particular it will be $i_{out} = g \cdot v_d$, where g is the transconductance of the amplifier.

In order to compute this transconductance, it is necessary that v_{cm} changes by $+\frac{v_d}{2}$ and v_{in} changes by $-\frac{v_d}{2}$. Now the common node of the two differential halves (the source of the M1 and M2 transistors) maintains the same voltage. For small-signal analysis, the common node is treated as a virtual ground. So, if g_h is the transconductance of the arm of the differential pair shown in 3.7, $i_{out} = g_h \cdot \frac{v_d}{2} - (-\frac{g_h \cdot v_d}{2}) = g_h \cdot v_d$. For this reason, the transconductance of one arm of the differential pair, biased to $\frac{I_B}{2}$, is the amplifier transconductance itself.

In particular, the most interesting part of the circuit shown in 3.2 is the differential input stage. In 3.7 it is shown one arm of the differential stage. From this circuit, it can be derived the corresponding small-signal model (3.8), where a dimensionless resistor of $\frac{1}{\kappa_p}$ corresponds to the source degeneration diode. Another dimensionless resistor $\frac{1}{\kappa_n}$ represents the gate degeneration diode and finally another dimensionless resistor $\frac{1}{\kappa}$ reproduces the gate controlled current source. Finally, the well input corresponds to the voltage controlled current generator.

The signal flow diagram for the well-input transistor in 3.9 has been derived from 3.8. The right half of 3.9 corresponds to the source or gate degeneration diodes that

are injecting current back to the source and gate, respectively. For this reason, there are two negative feedback loops that are lowering the transconductance in parallel. The two loops feeds back the output current to:

- the source through a block of value $-\frac{1}{\kappa_p}$;
- the gate though a block of value $\frac{1}{\kappa_n}$.

Therefore the final value of the loop gain will be

- for the loop feeding to the source $A_s = \frac{1}{\kappa_p}$;
- for the loop feeding to the gate $A_g = \frac{\kappa}{\kappa_n}$.

Knowing that is possible to compute the output-input relationship, that in this case is the transconductance g. It is defined as

$$g = \frac{1-\kappa}{1+\frac{1}{\kappa_p}+\frac{\kappa}{\kappa_n}} \tag{3.9}$$

This value is dimensionless and so to compute the real transconductance of the component is necessary to multiply it by $\frac{I_B}{2 \cdot U_T}$ (because the current flowing in each branch is $\frac{I_B}{2}$).

The transistors of each differential branch can be treated as a big single transistor that has the following I-V characteristics

$$I \propto \exp\left(-\frac{v_S - g \cdot v_W}{U_T}\right) \tag{3.10}$$

In [22] all the steps to find the final relationship are showed. At the end the final result for the output current is:

$$i_{OUT} = I_B \cdot \tanh\left[\frac{g \cdot (v_+ - v_-)}{2 \cdot U_T}\right] \tag{3.11}$$

3.2.3 Linearization using bump transistors

The last technique used in [13] is the bump linearization. This is adopted in order to linearize the tanh inside 3.11, so that the linear range of the differential pair is increased [26].

First the bump linearization is explained using a normal differential pair and then the concept is extended to the case of [13].

The difference between a bump differential pair and a standard differential pair is that the one bump linearized has, in addition to the two outer arms, a central

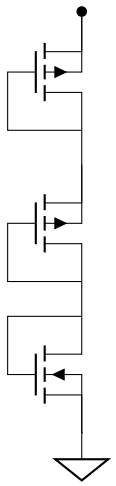

Figure 3.7: Branch of the differential stage

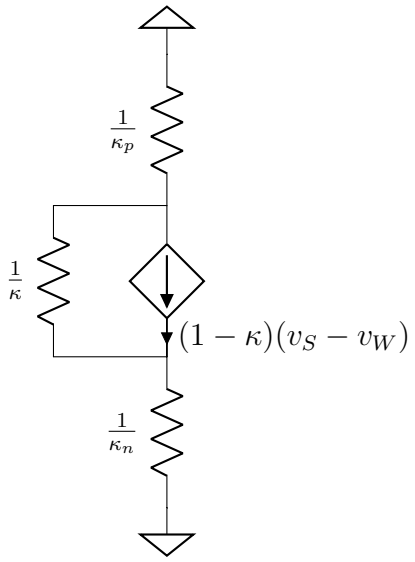

Figure 3.8: Small signal model for one arm of the differential pair

arm with two series connected transistors [21]. The current that is flowing inside these transistors is a bump-shaped function of the differential voltage.

In this way the differential current of the two arms continues to maintain the same tanh behavior, except in the origin where the bump transistors are activated and so part of this current flows also in them. With a proper W/L ratio of these transistors (this ration has to be w times the ratio of the M5/M6 transistors in the differential arms), it is possible to control the I-V curve.

Basically a small value of w (~ 0) does not change the curve. On the contrary, a

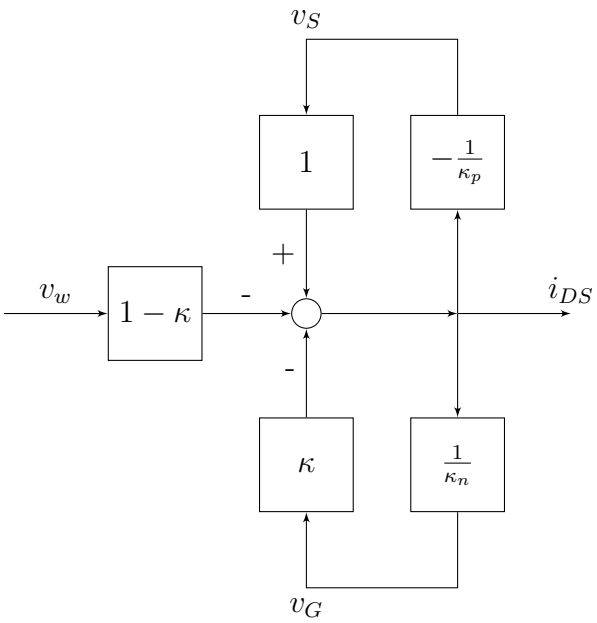

Figure 3.9: Flow diagram of the differential branch

large w will have the effect to flatten the current near the origin due to the activation of the bump transistors. For this reason, "the larger will be the w, the larger will also be the width and flatness of this zone" [13]. Keeping the value of w in an intermediate range, it will bring the best results for linearity and the tanh curve becomes more linear. In [13], it is shown that at $w = 2$ the curve is maximally linear.

Assuming to have a bump scaling of w, in bump amplifier the differential output current is defined as

$$i_{out} = \frac{\sinh(x)}{\beta + \cosh(x)} \tag{3.12}$$

where

$$\beta = 1 + \frac{w}{2} \tag{3.13}$$

and

$$x = \frac{q \cdot \kappa \cdot (v_+ - v_-)}{kT} = \frac{\kappa \cdot (v_+ - v_-)}{U_T} \tag{3.14}$$

Supposing that the bias current is 1 (this is the simplest case), in [13] it is shown that the first and second derivatives of 3.12 are:

$$\frac{di_{out}}{dx} = \frac{1 + \beta \cdot \cosh(x)}{(\beta + \cosh(x))^2} \tag{3.15}$$

$$\frac{d^2 i_{out}}{d^2 x} = \frac{\sinh(x)(\beta^2 - \beta \cdot \cosh(x) - 2)}{(\beta + \cosh(x))^3} \tag{3.16}$$

The final goal is to obtain a output current-vs-x with no inflection (except for the origin). This means that the curve has to be convex or concave in the first or third quadrant. For this reason, 3.16 has to respect this constraint:

$$\beta^2 - \beta \cdot \cosh(x) - 2 \leq 0 \qquad \forall x \tag{3.17}$$

It is important to notice that, by deriving 3.17, it is exploited the positive sign of the denominator of 3.16 and also the $\sinh(x)$ sign change at the origin. The worst case when the constraint of 3.17 is not respected, it happens when $\cosh(x)$ has its minimum of 1 (at $x = 0$). So, by setting $\cosh x = 1$ and solving the resulting quadratic for β, the result obtained is

$$\beta \leq 2 \qquad \Rightarrow \qquad w \leq 2 \tag{3.18}$$

For this reason at $w = 2$, the constraint is surely met and the output curve curve reaches a high linearity. By Taylor expand 3.12 at $\beta = w = 2$, it is possible to notice that there is no cubic distortion term. On the contrary function $\tanh\left(\frac{x}{2}\right)$, that is to what 3.12 reduces when $w = 0$ or $\beta = 1$, has cubic distortion.

$$\tanh\frac{x}{2} = \frac{x}{2} - \frac{x^3}{24} + \frac{x^5}{240} - \frac{17x^7}{40320} + \dots \tag{3.19}$$

$$\frac{\sinh x}{2 + \cosh x} = \frac{x}{3} - \frac{x^5}{540} + \frac{x^7}{4563} - \frac{x^9}{77760} + \dots \tag{3.20}$$

At $x = 1$, the tanh function has almost 8% of error derived by the cubic term. On the other hand the linearized tanh function does not have any error, since it has not any cubic term. Hoverer there is still a little distortion, but it is due a fifth-harmonic distortion and it is very little (less than 1%). For this reason in [13] it is possible to say that the tanh has been linearized.

The circuit in 3.2 implements a wide-linear-range bump differential pair. The W/L ratio of the nFET M12 and M13 transistors (bump transistors) is w times the W/L ratio of the nFET M5 and M6 transistors.

Explained how it is the behavior in case of a simple bump circuit, the mathematical analysis of the final circuit is identical to explained. The only difference is that is necessary to substitute the κ of 3.14 with the g of 3.9. Doing this the final equation that describes the output current is:

$$I_{out} = I_B \frac{\sinh(2x)}{1 + \frac{w}{2} + \cosh(2x)} \tag{3.21}$$

where $x = V_d/V_L$.

3.3 Results

The component described in the previous sections has been implemented using a 130 nm technology in HSPICE®. The V_{DD} is 1.2 V and the transistor sizing (in nm) is the following:

- 260/130 for M1 and M2 transistors;
- 130/130 for M3 and M4 transistors;
- 180/130 for M5 and M6 transistors;
- 200/130 for M7 and M8 transistors;
- 130/130 for M9 and M10 transistors;
- 300/130 for M11 transistor;
- 350/130 for M12 and M13 transistors.

In order to gather the results the negative input terminal has been driven by a common mode voltage $V_{cm} = 0.5 \cdot V_{dd} = 0.6\,\text{V}$. In order to test the behavior of the component the positive input terminal has been driven with a voltage in the range $[-0.3\,\text{V}; 0.9\,\text{V}]$. In the figures the differential voltage V_{diff} has the following value: $V_{diff} = V_{in} - V_{cm} = V_+ - V_-$

Since the bias voltage V_{bias} is crucial to drive the transconductance of the component, the simulation has been also done changing the V_{bias} in the range $[0.75\,\text{V}; 1.2\,\text{V}]$. The behavior of the transconductance in relation to the bias voltage is very important because the circuit in 2.1 needs to tune the transconductance of the OTAs. This can be done by setting the correct V_{bias}.

In 3.10, it is presented the behavior of the output current in relation to the bias voltage V_{bias} and the input differential voltage V_{diff}, while in 3.11 the bias voltage V_{bias} is fixed to 1 V.

Especially in 3.11, it is possible to notice the linearity of the current output curve. It still remains a slightly non linear part in the beginning, but it is negligible compared to the overall behavior. In 3.10, it is possible to notice how much the bias voltage V_{bias} affects the output current. In fact, since V_{bias} drives the gate of M11 (3.2), the current flowing in the differential branches (and so the output current) is controlled by this transistor. Putting this transistor in cut-off region, means to have an output current I_{out} equal to zero. Vice versa, decreasing the V_{bias} (it is a pMOS) means to put the transistor in an even more saturation region and so the current flowing will be much more high.

In 3.13 it is shown a graph of the transconductance gm with the bias voltage V_{bias} fixed to 1 V. The transconductance, that is $gm = \frac{dI_{out}}{dV_{diff}}$, is almost constant in

among all the curve, showing how much the output current I_{out} is linear. The only part where it is not constant is in the initial part where some non linear behavior still remains. However the the non linearity does not exceed too much and this is acceptable. In 3.12, the graph shows how much the transconductance is constant, especially where the bias current V_{bias} does not bring the M11 (3.2) in deep saturation region. It is also possible to notice how much the transconductance gm is affected by the bias voltage. This is much more clear in 3.14, where it is shown the average transconductance at different bias voltages. When the V_{bias} is maximum the transistor is in cut-off and so the transconductance gm is 0, on the contrary, driving the M11 transistor in saturation region (lower V_{bias}) will increase the transconductance of the component.

About the power dissipation, since it is proportional to the current flowing in the circuit, the same consideration of the output current can be applied. Incrementing the differential input voltage difference, the power consumption grows as well as incrementing the V_{bias}. In both cases more current is flowing inside the two arms of the differential pair and so the output current will be higher too.

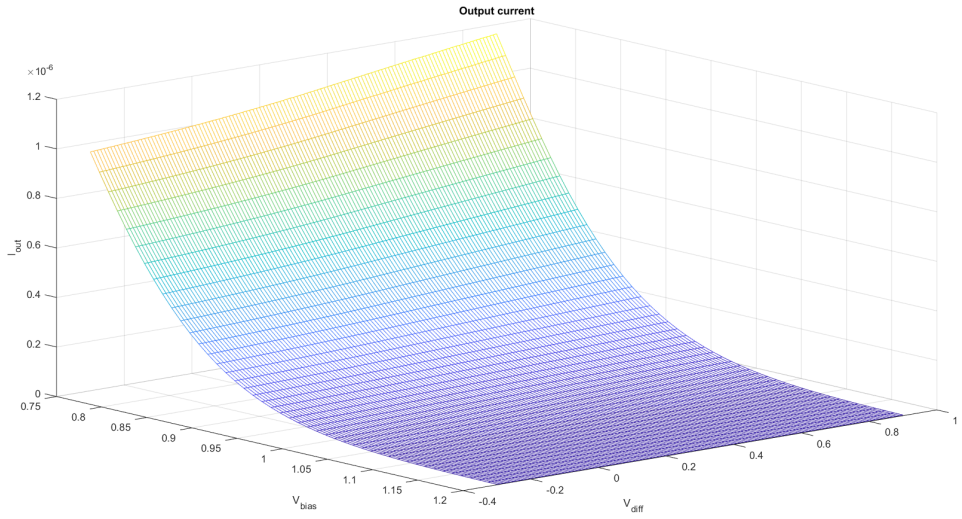

Figure 3.10: 3D graph showing the output current I_{out} in relation to the bias voltage V_{bias} and the input differential voltage V_{diff}

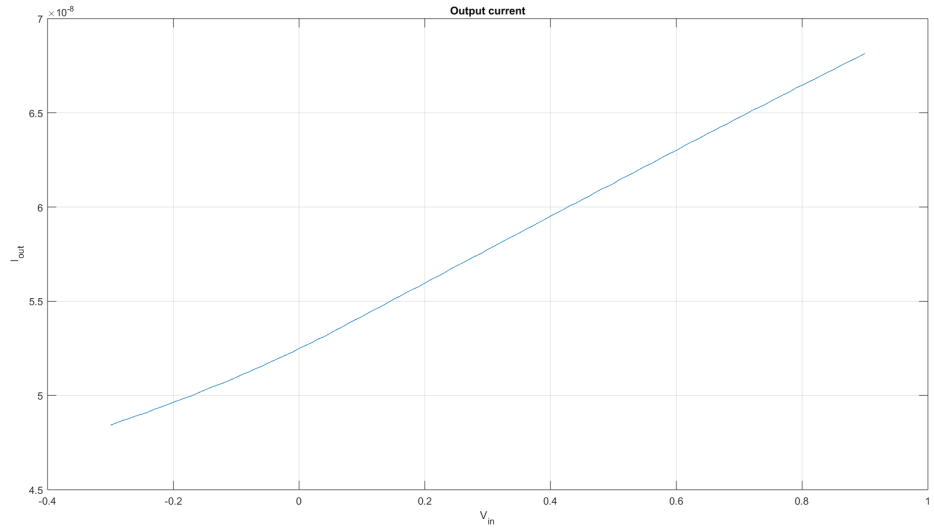

Figure 3.11: 2D graph showing the output current I_{out} in relation to the input differential voltage V_{diff} when the bias voltage $V_{bias} = 1\,\mathrm{V}$

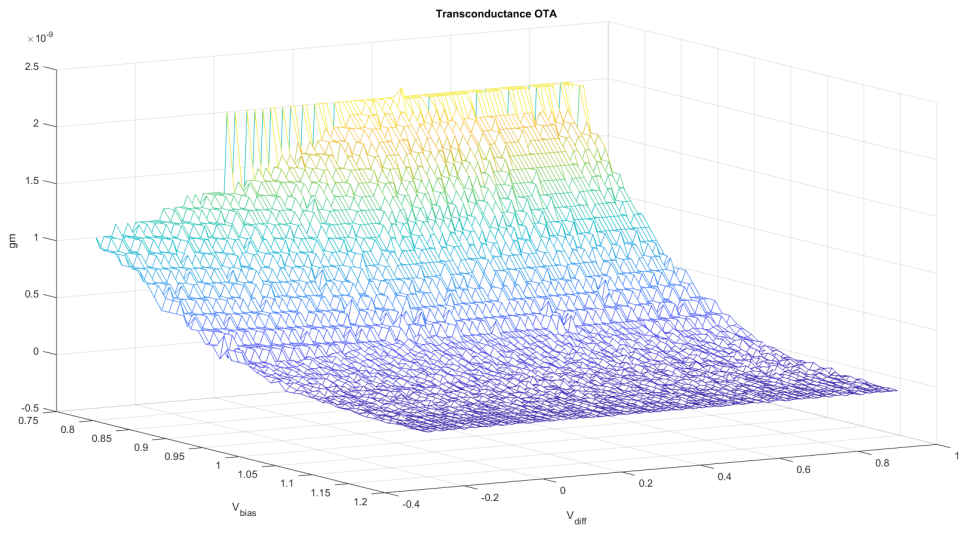

Figure 3.12: 3D graph showing the transconductance gm in relation to the bias voltage V_{bias} and the input differential voltage V_{diff}

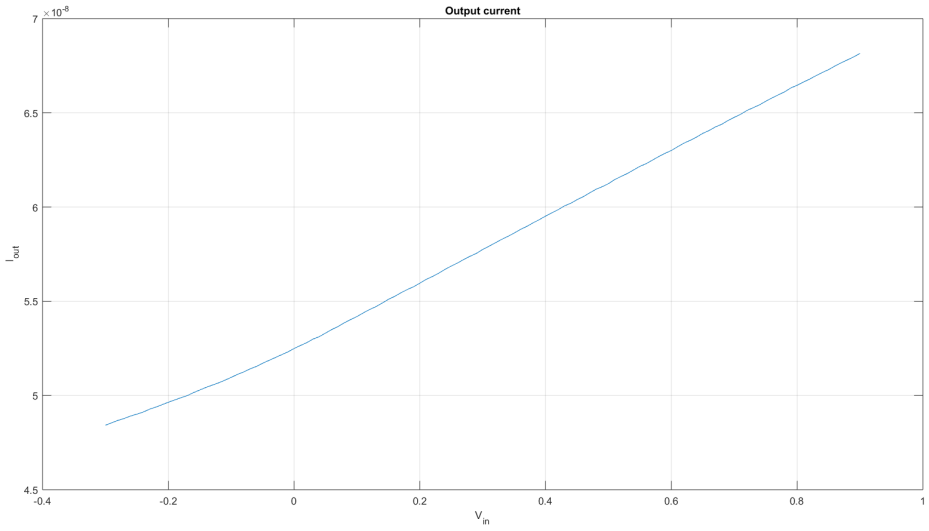

Figure 3.13: 2D graph showing the transconductance gm in relation to the input differential voltage V_{diff} when the bias voltage $V_{bias} = 1\,\mathrm{V}$

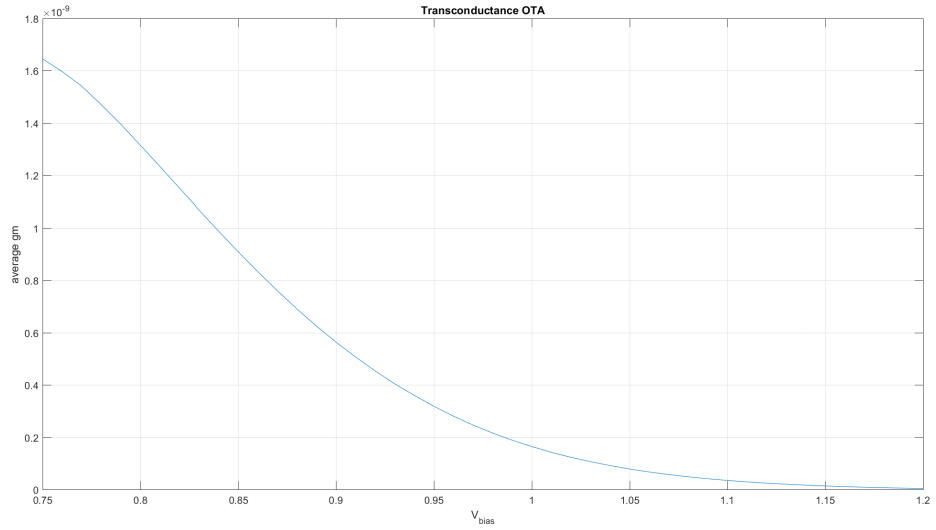

Figure 3.14: 2D graph showing the average transconductance in relation to the bias voltage V_{bias}

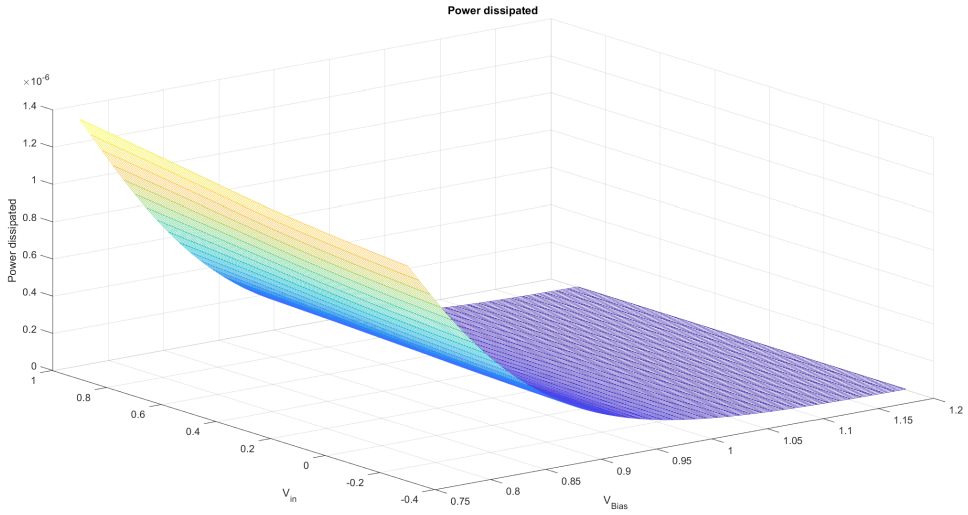

Figure 3.15: 3D graph showing the power dissipated in relation to the bias voltage V_{bias} and the input differential voltage V_{diff}

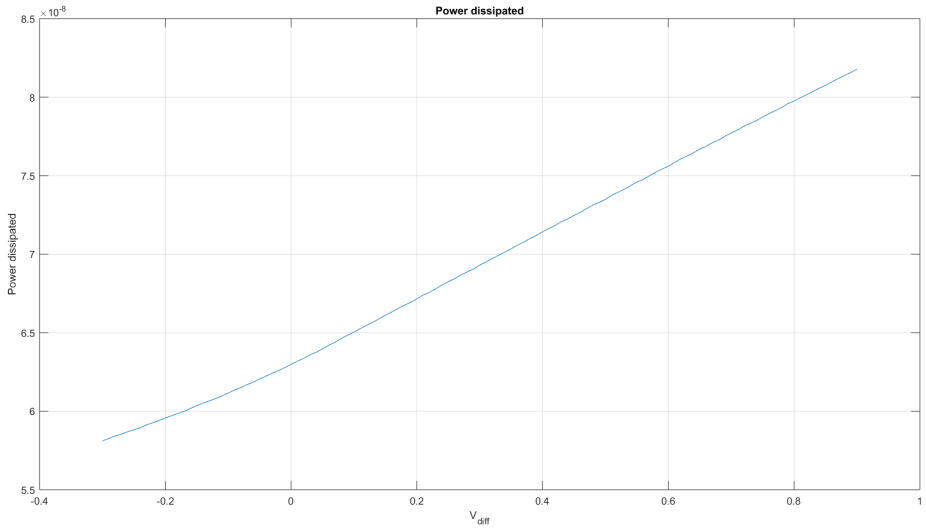

Figure 3.16: 2D graph showing the power dissipated in relation to the input differential voltage V_{diff} when the bias voltage $V_{bias} = 1\,\mathrm{V}$

Chapter 4

OpAmp design

4.1 Basic concepts

The OpAmp is a voltage amplifier with a differential input and a single-ended output. The OpAmp produces an output voltage that is typically hundreds of thousands of times larger than the differential input voltage. Since the OpAmp produces a voltage that is proportional to the input differential voltage, it is considered a VCVS. The OpAmp can be used in open-loop or closed loop configuration. Open-loop means that the output is not connected to none of the two input terminals (Figure 4.1 is an open-loop example), while in closed-loop the output is connected to one of the two input pins. [23]

In open-loop configuration, the equation that describe the behavior of the component is

$$V_{out} = A_{ol} \cdot (V_+ - V_-) \tag{4.1}$$

where A_{ol} is the gain of the amplifier. This value is variable and depends on how many stages there are inside the amplifier.

The OpAmp has in general the following structure (Figure 4.1):

- a positive input terminal where V_+ is applied;
- a negative input terminal where V_- is applied;
- a positive power supply terminal where V_{dd} is applied;
- a negative power supply terminal where V_{ss} is applied;
- an output terminal where V_{out} is measured;

The OpAmp can be also used in many different closed-loop configuration (when the output is fed again to one of the two input). Since none of these applications is discussed in this thesis the closed-loop part is not treated.

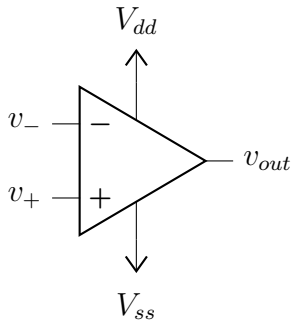

Figure 4.1: OpAmp schematic symbol

4.2 OpAmp behavior

Since the OpAmp is not the most critical structure inside the circuit in Figure 2.1, the schematic structure is kept as simple as possible in order to reduce the power dissipation.

The final structure is the simple two stage differential amplifier in [14]. The overall structure is composed by two stages:

- a differential input stage with single output with gain magnitude $-A_1$;
- a gain stage with gain magnitude $-A_2$;

It is possible to have also a third stage that consists in a output buffer.

To design this OpAmp it is necessary to know the supply voltage V_{DD}, the bias current I_{bias} and the technology process of the transistors (this means that the channel length L of the transistors is know). The value of the resistor R_C and the capacitor C_C are chosen depending the position of the pole wanted in the frequency domain (in this application is not important the pole, it is more important the value of the gain). Having these hypothesis, it is possible to design the component.

From Figure 4.2, it is possible to derive that

$$I_{DS1} = I_{DS3}, \qquad I_{DS2} = I_{DS4}, \qquad I_{DS6} = I_{DS7} \tag{4.2}$$

and

$$I_{DS5} = I_{DS1} + I_{DS3} \tag{4.3}$$

Since it is better to split the current in half inside the differential pair, using Equation 4.2 and Equation 4.3, it is derived the following equality:

$$I_{DS1} = I_{DS3} = I_{DS2} = I_{DS4} = \frac{I_{DS5}}{2} \tag{4.4}$$

In order to find the transistor sizing, it is necessary to use the current mirror relationship between M5 and M8

$$I_{DS5} = \frac{W_5}{W_8} \cdot I_{Bias} \tag{4.5}$$

The OpAmp to work properly needs that all the transistors are in saturation region. In this region the current flowing inside a transistor is described with $I_{DS} = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{th})^2$. By choosing a proper $V_{GS8} = VGS5$ to put M5 and M8 in saturation, it is possible to retrieve the width of both transistors. Once W_5 is found, I_{DS5} is computed and using Equation 4.4 W_1, W_2s, W_3 and W_4 are found.

In order to find the sizing of M6 and M7, it is use the the case where $V_{in} = V_{cm} = 0$. Since the last equality in Equation 4.2 has to respected, this means that in order to have all transistor in saturation the gate-source voltage in M7 has to be

$$V_{GS7} = \sqrt{\frac{2 \cdot I_{DS6} \cdot L}{\mu_n \cdot C_{ox,n} \cdot W_7}} + V_{th,n} \tag{4.6}$$

Exploiting the fact that the input voltage are both 0, the following equality is also true

$$V_{GS4} = V_{DS3} = V_{GS7} \tag{4.7}$$

If the V_{GS4} is expressed in the same way of the Equation 4.6, using the Equation 4.7 it is obtained the following equation

$$\frac{L}{W_7} \cdot I_{DS6} = \frac{L}{W_4} \cdot I_{DS4} \tag{4.8}$$

Since $I_{DS4} = \frac{I_{DS5}}{2}$, using Equation 4.8 it is possible to obtain:

$$\frac{W_7}{W_4} = 2 \cdot \frac{W_6}{W_5} \tag{4.9}$$

In order to compute the overall gain, as written before, it is necessary compute the gain of the two stages. Recalling the transconductance formula defined as $gm = \sqrt{2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot I_{DS}}$, it is possible to compute the gain of the first stage as:

$$A_{v1} = -gm_1 \cdot (r_{ds2} // r_{ds4}) \tag{4.10}$$

and the gain of the second stage as

$$A_{v2} = -gm_7 \cdot (r_{ds6} // r_{ds7}) \tag{4.11}$$

where $gm_1 = \left(\sqrt{2 \cdot \mu_p \cdot C_{ox,p} \cdot \frac{W_1}{L} \cdot I_{DS1}}\right)$ and $gm_7 = \left(\sqrt{2 \cdot \mu_n \cdot C_{ox,n} \cdot \frac{W_7}{L} \cdot I_{DS6}}\right)$. The final gain is the multiplication of the gain of the two stages:

$$A_v = A_{v1} \cdot A_{v2} \tag{4.12}$$

The other parameter important inside a OpAmp is the slew rate that is "the maximum rate at which the output of an OpAmp changes when a large differential input signal is present" [14]. In this case the slew rate is computed as

$$SR = \left.\frac{dV_{out}}{dt}\right|_{max} = \frac{I_{DS5}}{C_c} \tag{4.13}$$

The unity gain frequency is defined as

$$f_{opamp} = \frac{\omega_{opamp}}{2 \cdot \pi} = \frac{gm_1}{2 \cdot \pi \cdot C_C} \tag{4.14}$$

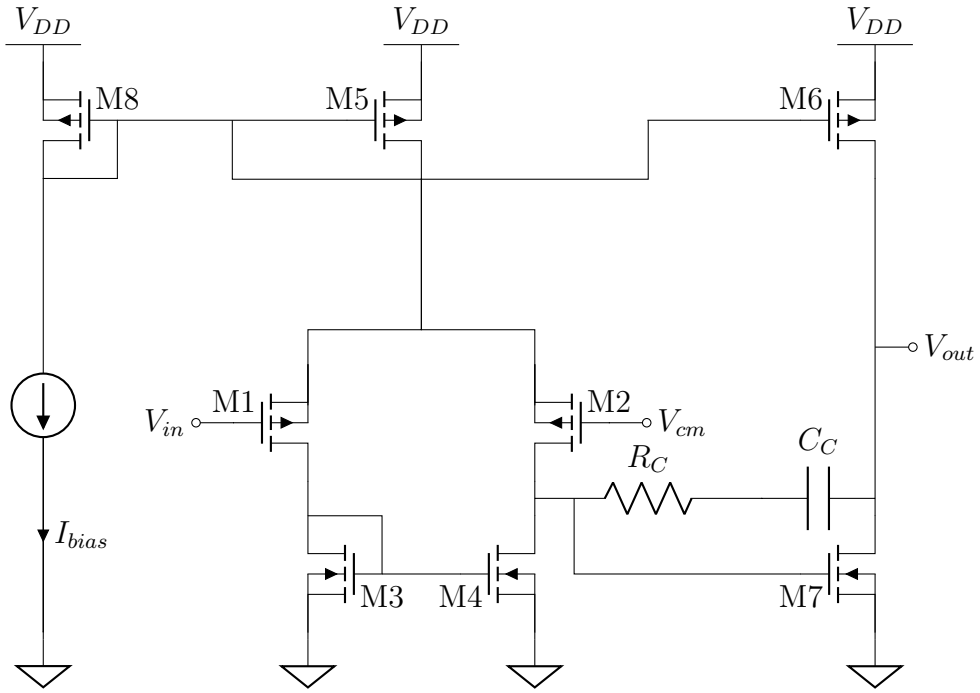

Figure 4.2: OpAmp circuit schematic

4.3 Results

The component described in the previous sections has been implemented using a 130 nm technology in HSPICE®. The $V_{DD} = 1.2\,\text{V}$, the R_C =350 Ω, the $C_C = 1\,\text{pF}$, the $I_{Bias} = 20\,\mu\text{A}$ and the transistor sizing (in µm) is the following:

- 36/0.3 for M1 and M2 transistors;
- 6/0.3 for M3 and M4 transistors;

- 30/0.3 for M5 transistor;
- 45/0.3 for M6 transistor;
- 18/0.3 for M7 transistor;
- 3/0.3 for M8 transistor.

In Figure 4.3, it is shown the gain magnitude of the OpAmp at different frequencies. Since this application works on the base band, there were not any poles constraint. In base band there is a gain of 1131.

In figure Figure 4.4, it is presented the output voltage at different differential input voltage V_{diff}.

At the end the average power consumption of the component is 391 µW.

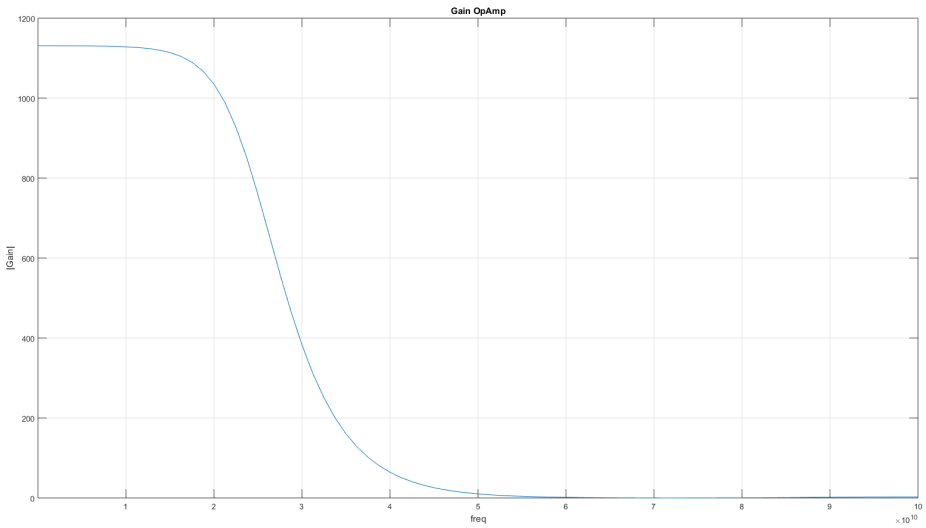

Figure 4.3: Gain magnitude of the OpAmp

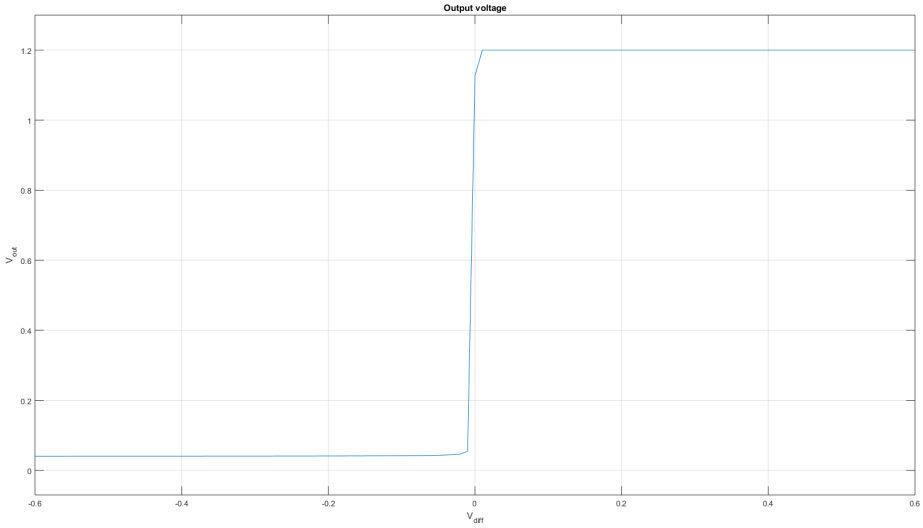

Figure 4.4: Output voltage V_{out} vs differential input V_{diff}

Chapter 5

Results

5.1 Example

In order to check the correct the correctness of the mathematical model discussed in Section 2.1, all the equation has been implemented in Matlab®. The input data to solve the problem are:

1. the beacon positions $[x_i, y_i]$;

2. the AOA from each beacon.

The expected output is the final coordinate of the object $[x_s, y_s]$.

In order to show the final result an example is used. In Table 5.1 there are the input data. The beacons number of the table can be seen in Equation 2.8 and the angle is expressed in degrees. In this case the final value of the object is $[x_s, y_s] = [0.4475, 0.6322]$.

Beacon	**x coord**	**y coord**	**AOA**
1	0.1	0.3	63
2	0.6	0.2	153
3	0.4	0.9	-50
4	0.8	0.5	124

Table 5.1: Input data of the example

In Equation 2.8, the blue circles represents the beacons, while the red cross has the coordinates computed using the theory in Chapter 2.

First the circuit has been implemented in HSPICE® using ideal component to build the circuit in Figure 2.1. The values implemented in the circuit are present

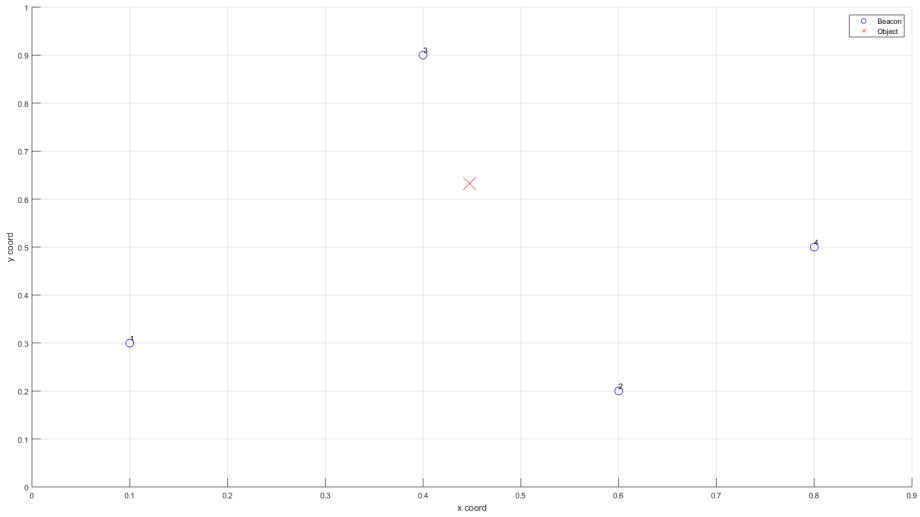

Figure 5.1: 2D space disposition of the beacons and the object

in Table 5.2. The expected value derived by solving Equation 2.17 and Equation 2.18 are $[-0.8097\,\mathrm{V}, -1.0595\,\mathrm{V}]$. The simulation value at steady state are $[-0.805\,\mathrm{V}, -1.11\,\mathrm{V}]$ and so the result obtained matches almost the ideal value computed using Matlab®.

Quantity	Value
gm_1	0.956 nS
gm_2	0.956 nS
R_1	440 MΩ
R_2	580 MΩ
C_1	10 fF
C_2	10 fF
I_1	1.62 nA
I_2	1.52 nA

Table 5.2: Values of the components in the circuit

5.2 Process variation

After showing an example of how the solution works, it is important establish the maximum noise level introduced by the components allowed to estimate the final position.

Starting from the example in the previous section, in order to understand the noise impact inside the system the noise is added to the vales inside the matrices A and B and in this way it is possible to simulate the noise inside the components.

By solving the system in Equation 2.8 applying different noise conditions, it is possible to determine the maximum amount of noise tolerated. In order to have more reliable measurements for each value of SNR, the noise injections and the measurements are repeated many times (in this case 10000). At the end of each measurement, it is computed the distance between the ideal point and the one affected by the noise. Then for each value of SNR it is find the mean of all distance measurements.

In Figure 5.2 the black dashed lines indicates where the distance error starts to be within the 20% from the original value.

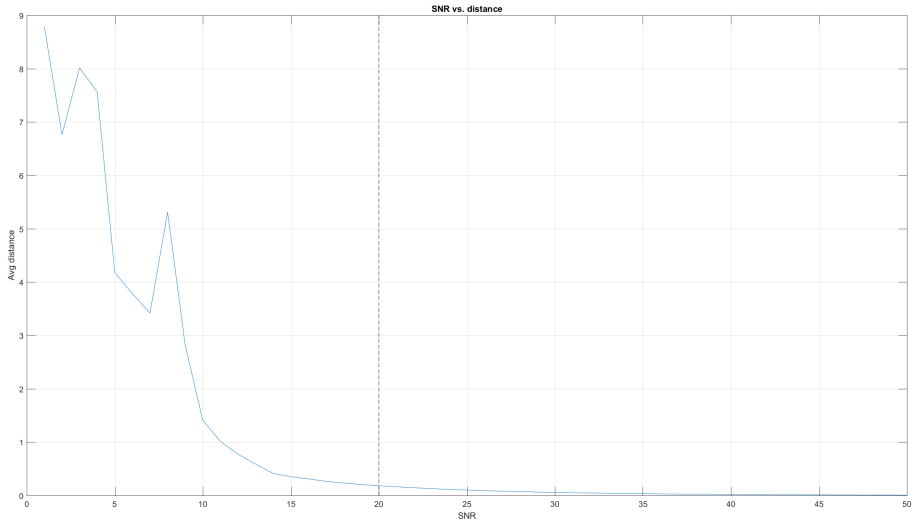

Figure 5.2: Average distance on different noise level

The same discussions can be extended also to the expected voltage value. After computing the point distance, the expected ideal voltage and the one affected by the noise are compared and the mean between the difference on all measurements is computed for each SNR.

In Figure 5.3 again the black dashed line indicates where the difference starts to be within the 20% of the original value.

It is possible to notice that the voltage is more influenced by the SNR and the minimum SNR should be greater than 25 to be sure to obtain a final value acceptable.

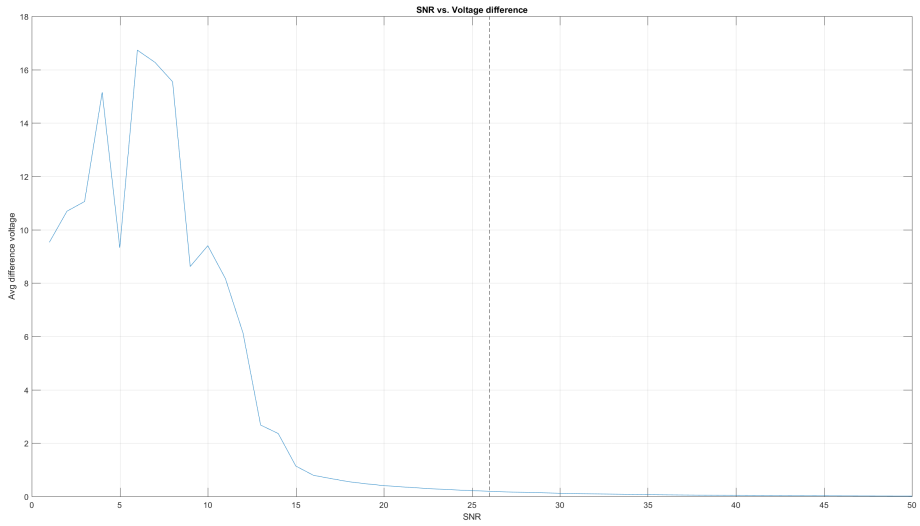

Figure 5.3: Average voltage difference on different noise level

5.3 Power consumption and comparison to a similar digital solution

It is interesting the comparison with a digital solution in [24] that perform a similar task. In [24], the self-localization model is similar because in both cases the AOI and the beacon position is used to find the object position.

The digital solution has been implemented using an FPGA and an ASIC. The first one has a power dissipation of 301.219 mW (180 mW only for the core) with a supply voltage of 1.5 V for the core and 3.3 V for the I/O pads. On the contrary, the ASIC solution, that works at 1 V V_{DD}, has a power dissipation of 6.15 mW. As expected, the ASIC solution is optimized for the task and needs less power.

The average power consumption in the example for the analog solution is 756 µW.

It is possible to notice that the analog solution is even more optimized than the ASIC solution and this leads to a less power consumption.

Chapter 6

Conclusions

The thesis has been very interesting, but at the same time also very challenging because the design of the analog circuits has to take in account many constraint and limitations.

The design phase for the circuit and the components (OTA and OpAmp) tool most of the time and for this reason, it has been impossible to test accurately all the components inside the circuit. In fact, before implementing the final circuit, first the analog circuit was tested using Matlab®. However most of the time has been spent to design the OTA because in order to achieve the desired linearity many techniques has been implemented. This has consequences during the testing of the component behavior using HSPICE®, that it took much time.

For this reason, the final circuit has been tested only ideal components since the results using the designed OTA and OpAmp were not so accurate. This means that the designed OTA and OpAmp needs a more refined tuning in order to work properly and obtain a correct localization.

The future developments of the thesis consists in complete the circuit testing using the designed components, that will have to be tuned properly (especially the OpAmp).

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