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Corso di Laurea Magistrale in

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Evaluation of methodologies for the estimation of power consumption in integrated digital systems

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A chi ha creduto in me,

ai miei genitori, che mi hanno sempre sostenuto,

a mio fratello, sin dalla nascita il mio migliore amico

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Introduction

Improvements in nano-scale digital designs are focused on increasing transistor density and the operating frequency and reduce size and power supply. As a result, the vulnerability to power supply noise greatly increases, affecting the chip performances and causing problems like signal integrity or additional delay. One of the main source of power supply noise is IR drop, i.e., an electrical phenomenon that produce fluctuations in the supply voltage caused by the combination of parasitic resistive elements in the power distribution network (*R*) and the current (*I*) needed to operate the device. Moreover, there can be other factors that can cause IR drop, and identifying the real problem and devising a good solution is not an easy task.

From a test perspective, performing the right analysis for each specific case is crucial.

These analyses are done at the end of the physical implementation (or back-end) phase, in which all the components are placed and connected, and the logical and temporal functionalities are verified. In order to avoid misunderstanding results and wasting time, designers need to perform the most suitable measurements and simulations in the specific condition enabling the identification of the problem, since there are many factors that can affect results in the IR drop analysis, such as temperature and supply voltage.

There are different types of analyses that can be made to evaluate IR drop and predict possible circuit misbehaviors, each with its own goals, advantages and disadvantages.

We will focus on three different types of analyses:

- *Static voltage drop analysis*: this analysis can be performed in early design steps and produces an average estimation of IR drop. It gives a global view about the physical problems in the design of the supply distribution lines
- *Dynamic vector-free voltage drop analysis*: this analysis considers also the temporal effect. It gives results about voltage drop caused by instantaneous current demand produced when a large amount of circuitry switches simultaneously. However, the activity of the circuit is estimated by the tool itself, therefore it is subject to approximations
- *Dynamic vector-driven voltage drop analysis*: this analysis takes care of the real logic switching activity of the gates in the design. It is the most accurate analysis among the ones employed, but in has the highest cost in terms of simulation time.

This work aims to analyze the most relevant characteristics of different analysis approaches, underlining the different possibilities to increase accuracy and highlighting the impact of temperature variations during the static voltage drop analysis. We will also compare the different results to evaluate the trustworthiness of the different approaches and their cost.

This document is structured in five chapters followed by a general conclusion.

Chapter 1 presents a description of the state of art. It will describe the realization of the physical design of a VLSI circuit, the structure of the power distribution network and the basic concepts of power dissipation.

Chapter 2 will introduce the IR drop phenomenon from a theoretical point of view, including logic gate characterization and hot spots.

In Chapter 3 the general approach is proposed. IR drop analysis will be described, pointing out the various solutions and possibilities.

Chapter 4 explains the requirements and parameters used for the analyses, describing also the used flows. Finally, the results of the analyses are reported in Chapter 5.

Chapter 1 – State of art

1.1 Design flow and physical structure of VLSI circuits

The design of a VLSI (Very Large Scale Integrated)synchronous sequential circuit is a complex process that can be generally divided into 2 halves.

In the first half, known as front-end, the functionality of the circuit is defined and transformed into an abstract version called *Register Transfer Level* (RTL), using a hardware description language (HDL). Then the circuit is converted into low-level circuit elements by means of *synthesis* tools, which can map the previous functionality to a list of combinational and sequential elements (logic gates, flip-flops, memories, etc.) connected by nets, known as *netlist*. At this point, the circuit undergoes the back-end flow, where all elements in the circuit are instantiated with their specific sizes and shapes in specific areas of a silicon substrate. The first part of back-end, called physical design, includes *Partitioning*, *Floorplanning*, and *Place & Route*[1]. Partitioning means dividing the circuit in smaller hierarchical blocks, which, if necessary, can be analyzed individually. Floorplanning decides the shapes and positions of these blocks, as well as the location of external ports and macro blocks, that are usually bigger pieces of logic that perform reusable functionalities, like adders, multipliers, memories etc. Moreover, this phase includes the distribution of power supply (VDD) and ground (GND) nets. Finally, Place & Route incorporates the placement of cells within each block, the generation and

routing of the clock network and the whole routing for connections. At the end of this stage, a major review of the initial floorplan may be necessary if critical parameters diverge too much from earlier estimates, like area, long path delay or power dissipation[1].

After physical design, the circuit must be fully verified to ensure electrical and logical functionality in a process usually referred to as *sign-off*. These checks can highlight problems that could be negligible or require the application of changes that, in turn, should not introduce other errors. First, it is needed to verify if the layout meets parameters imposed by the manufacturing flow in the used technology. This is called *Design Rule Checking* (DRC). Then two descriptions are generated from the design, in two different formats:

- A database, often in the DEF (Design Exchange Format) standard, that describes the physical implementation, thus the layout.
- A post-layout netlist, usually in Verilog, that describes the logical connections, thus the schematic.

Then, these two files are processed in such a way to be compared and to ensure that the layout is identical to the schematic. This verification is called *Layout vs. Schematic* (LVS). Finally, the *Electrical Rule Checking* (ERC) is performed, verifying the correctness of power and ground connections and bounding the signal transition times (slew), capacitive loads and so on. This can be done after extracting the parasitic resistance, capacitance and inductance from the layout. During the all processes of optimization (i.e., after place & route) until the end of the verification phase, the temporal requirements is repeatedly checked with the Static timing analysis (STA). This analysis checks the setup and hold time violations, that is if paths are fast enough or too fast, calculating the maximum and minimum delay. The paths exceeding timing

requirements have obviously to be corrected. After the last verification, the correctness of the physical design is verified and the final layout is then sent to manufacturing, packaging and testing, other processes not addressed here.

Integrated circuits are made up of a silicon substrate where active devices are built and different upper layers. Each layer has its own role. For example, a layers made of silicon dioxide are used as insulators. Other layers act as interconnections and they are made with polysilicon, called “poly”, and aluminum or copper, called Metal1 (M1), Metal2 (M2), etc., depending on their position, from bottom to top. The connections between layers are achieved by contacts and vias. Contacts connect metal layers to silicon layers. A via is a connection between two superimposed metal layers.

Up to 40% of metal resources are used for power and ground nets, which compose the Power Distribution Network (PDN).

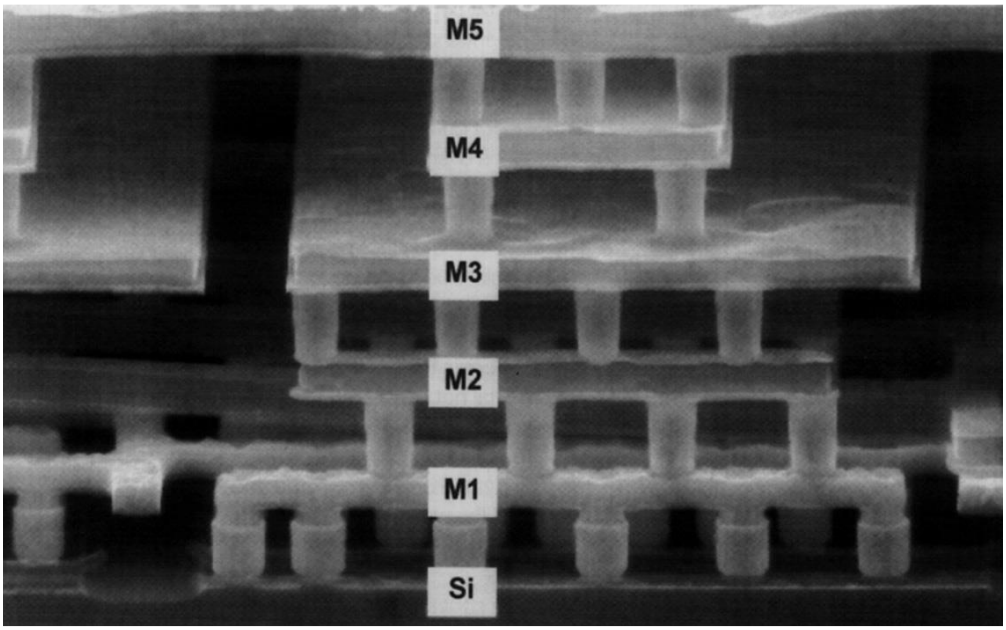

Figure 1 - Cross section of five layers

1.2 Power Distribution Network

The power distribution network, or power grid, is used to deliver power and ground voltage references from pads, which are physically connected to the power supply, to all active devices on the chip.

Most of the devices used in the implementation are the so-called standard cells. Standard cells are models of blocks that have fixed functionality and size, distributed by the foundries in different cell libraries. They are placed in parallel rows such that power and ground are distributed by abutment [3]. They are used in modern technology in order to reduce complexity and cost as well.

Metal layers are used for both supply nets and for signals. Generally, the ones used for supply nets are usually thicker and belong in the top levels and have a significantly lower resistance, higher pitch, higher width. For these reasons, they are more suitable for longer routes. On the contrary, metal layers used for signals are placed deeper within the die, have lower pitch and lower width, and therefore higher resistance [8]. This topology used for power-ground routing in digital ICs is called mesh routing.

In figure 2, we can see a hierarchical view of a typical PDN with 8 layers with a mesh topology. First, it includes a ring that surrounds the entire chip It is made of segments in multiple metal layers, and it is in charge of protecting the chip from electrostatic discharge and connecting the supply I/O cells [1]. In some cases smaller rings are used to encircle macro blocks. Pads are the physical supply connection to the chip. They need to be strongly connected to the ring, i.e., using lower resistance metal, in order to ensure a good flow of current to the core. Then, a mesh routing is characterized by parallel stripes with a fixed distance sufficient to ensure

pervasive power distribution. They are placed in pairs, alternating VDD and GND. In the lower metal layer those stripes are called *followpins* and they are in charge of connecting the power-ground distribution network to the standard cells.

One of the major challenges of chip design is to obtain a robust power grid [5][6][7]. On one hand, we need to have enough metal power lines in all metal layers to deliver current efficiently, but this may waste many routing resources, and it cannot be always possible.

On the other hand, in order to reduce area and metal layers, we use thinner metals, but this can create risks of IR drop and L · di/dt noise [4]. Such concepts are explained in the following.

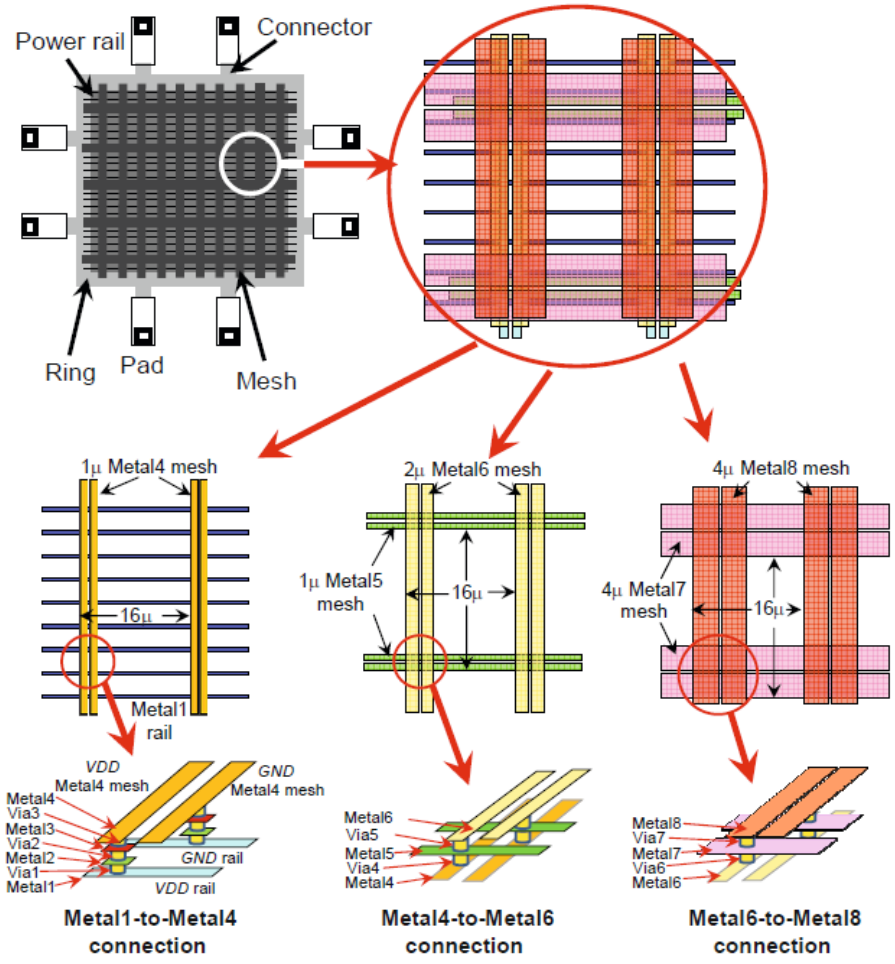

Figure 2-Power-ground distribution network [1]

Bad PDN can lead to IR Drop problems, such as the reduction of the local supply voltage due to the supply network resistance and the current needed to operate the device. In order to understand the causes of those IR drop problems, one needs to know the theory around that.

Power lines are modeled as RLC segments, in order to represent the unit-length resistance, the unit-length inductance (self and mutual), and the decoupling capacitor. However, in most cases, to simplify the computation, only the resistance and capacitance are used to model the power grid, ignoring the inductance without introducing significant errors. The model used is called Pai-RC model, because of its likeness of the pi (π) symbol. Therefore, all segments of the power lines are modeled as a series of resistors with two capacitances at the extremities.

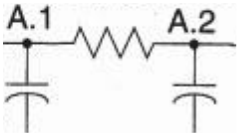

Figure 3-Pai-RC model

All this information, together with the value of all RC elements that depend on the device materials and physical structure, are usually described in a Standard Parasitic Exchange Format (SPEF) file.

Knowing the equation of the resistance

$$R = \frac{sl}{w}\ \Omega$$

where *s* is the sheet resistance (Ω/square), *l* is the length and *w* is the width of the line. Since IR drop depends on resistance of lines, we can easily understand how the type of metal and its shape are important for the IR drop.

In addition to this, also the position of power lines is important. The reason why the lines are put in a grid architecture is to create parallels between lines, decreasing the value of the effective resistance. The union of all segments creates a distributed RC parasitic network, as Figure 4 shows.

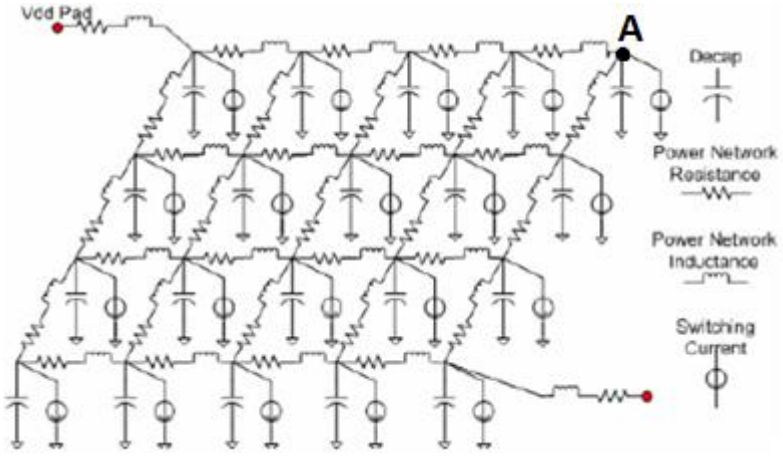

Figure 4– Power grid model

Figure 5 shows one piece of power grid connected to power supply.

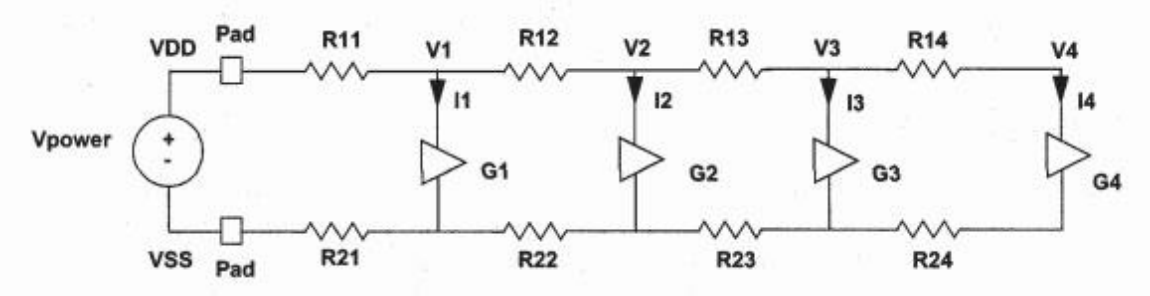

Figure 5-Model of power grid [9]

The resistors are the effective resistances in the V_{dd} and V_{ss}power grid distribution and G1-G4 are the gates switching with their own capacity. Ideally, the voltage coming from the power supply to the gate G4 is the same. Actually, the voltage in that node is reduced due to current flowing through the resistancesR11-R14 that cause a voltage drop. Vice versa, the voltage in the ground line will rise because the current for G4 to VSS will pass through R21-R24. This can be applied for every cell in the design. This variation will be equal to:

$$\Delta V_{max} = I_{avg}(R_{V_{dd}} + R_{V_{ss}})$$

This is why it is called IR drop, since $V = I \cdot R$. In this case I_{avg} is the current consumed by the cell switching and R is the sum of the effective resistance of the power grid for the pair V_{dd} andV_{ss}[9][9].

1.3 Power dissipation basics

As mentioned before, the continuous scaling of the feature size of CMOS technology has resulted in an exponential growth in transistor and power density, leading to heat and power dissipation.

In a CMOS circuit, there are two types of power dissipation: Static dissipation and Dynamic dissipation.

1.3.1 Static dissipation

The static dissipation depends on the leakage current or other current contributions drawn from the power supply. The power dissipation is derived by the follow equation:

$$P_{stat} = \sum_{i=1}^{n} I_{stat_i} \cdot V_{DD}$$

Ideally, the static power dissipation should be equal to zero because transistors in the off state are not supposed to drawn any current. However there are some leakage currents that cause static dissipation. The sources of leakage current are showed in Figure 6 [34].

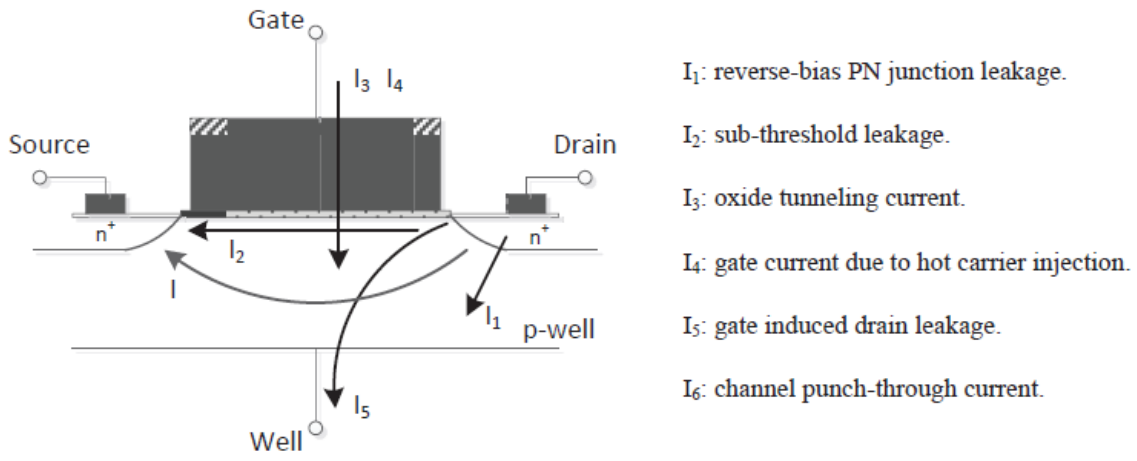

Figure 6 - Leakage current of deep-submicron transistor [34]

The first three currents are the ones that give a greater contribution to the leakage current. Drain- and source-to well junctions are typically reverse-biased, causing PN junction leakage current (I_1).

If both N and P regions are heavily doped, the depletion width is smaller and the electric field across the depletion region is higher. Under these conditions, the tunneling effect of electrons from the valence of the P region to the conduction band of the N region become significant. Sub-threshold current (I_2) is the most dominant among all sources of leakage. This current depends on doping concentration, channel length, threshold voltage and temperature. The subthreshold current is usually specified at 25 °C and grows exponentially with temperature, with atypical increase by one or two order of magnitude at 125 °C [1].

The oxide tunneling current (I_3) are electrons that move from substrate to gate and vice versa. The reduction of the oxide gate thickness creates an electric field that, together with the reduction itself, results in tunneling of electrons through the gate oxide, creating this current.

This high electric field near the poly-silicon can gives enough energy to the electrons or holes to enter in the oxide layer from the silicon side. This phenomenon is known as hot-carrier injection (I_4).

Furthermore, the gate induced drain leakage (I_5) is a result of high electric field in the drain junction, in which the silicon surface acts like a p region more heavily doped than the substrate.

Finally, the channel punch-through current (I_6)are carriers that escape from the source junction, moving to the substrate and collected by the drain and this occurs when the distance of the depletion regions decrease.

1.3.2 Dynamic dissipation

The dynamic power is dissipated by two contributions [35]:

- Charging and discharging of the load capacitance C_L
- "shot-circuit" currents when both nMOS and pMOS transistors are partially ON

Considering a CMOS inverter, when the input switches to logic state 0, the pMOS is turned ON and the nMOS is turned OFF. During this phase, the load capacitor starts charging and a certain amount of energy is drawn from the power supply. Part of this energy is dissipated from the pMOS device, which acts as a resistor, the rest is stored onC_L. Vice versa, when the input switches to logic state 1, the nMOS is ON and the pMOS is OFF. In this phase the capacitor starts discharging the stored energy, which is dissipated in the nMOS [35][1]. Supposing that the nMOS and pMOS are not ON simultaneously, the energy delivered from the power supply and the energy stored on the capacitor can be derived by integrating the power over the time of interest:

$$E_{V_{DD}} = \int_0^{\infty} I(t)V_{DD}dt = \int_0^{\infty} C\frac{dV}{dt}V_{DD}dt = CV_{DD}\int_0^{V_{DD}} dV = CV_{DD}^2$$

$$E_C = \int_0^{\infty} I(t)V(t)dt = \int_0^{\infty} C\frac{dV}{dt}V(t)dt = C\int_0^{V_c} V(t)dV = \frac{1}{2}CV_C^2$$

So, the power dissipation during switching can be expressed as:

$$\mathrm{P}_{switching} = \frac{1}{2}\alpha CV_{DD}^2 f$$

α is the activity factor or switching activity and f is the frequency .

The switching activity is defined as the probability of a net or an instance switching from 0 to 1 or 1 to 0 in one clock cycle. Therefore, if one cell has 0.2, it means that the cell will switch 2 times every ten clock cycles.

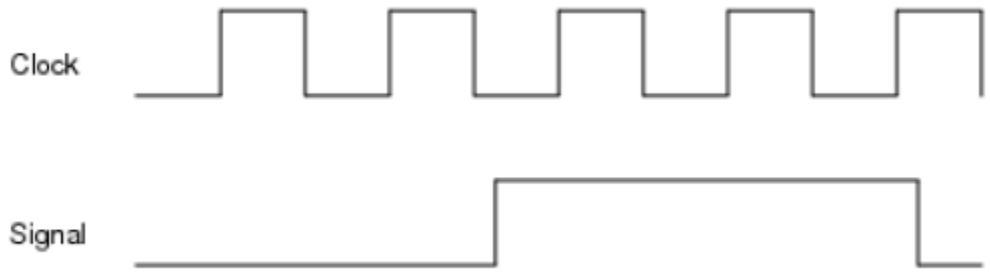

Figure 7- Switching activity over 10 clock cycles[4]

$$\alpha = \frac{Number\ of\ (0 \to 1\ or\ 1 \to 0)}{Number\ of\ clock\ cycles} = \frac{2}{10} = 0.2$$

The second contribution for the dynamic power dissipation is the short-circuit current. The latter is present during transitions when both the nMOS and the pMOS stay ON simultaneously[36].

Consider again a simple inverter driven by a rising ramp. Assuming the input device starts rising at the origin, the short-circuit current starts at time t_0 and end at time t_1, where, in timet_0, the nMOS device is turned ON and in time t_1 the pMOS is turned OFF. Knowing the rising time T_R, we can derive t_0 and t_1[37][37]:

$$t_0 = T_R \frac{V_{THN}}{V_{DD}}$$

$$t_1 = T_R \frac{(V_{DD} + V_{THP})}{V_{DD}}$$

Where V_{THN} and V_{THP} are the threshold voltages on nMOS and pMOS.

Finally, we can express the average short-circuit power integrating the short circuit current between the two time intervals:

$$P_{SC} = V_{DD} \int_{t_0}^{t_1} \frac{I_{SC}(\tau)}{(t_1 - t_0)} d\tau$$

We can see the behavior in Figure 8.

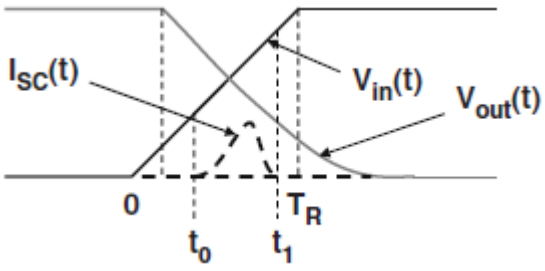

Figure 8 - Short circuit current

The total power consumption is the sum of the three components:

$$P_{total} = P_{stat} + P_{switching} + P_{SC}$$

Chapter 2 - IR drop

As mentioned before, the IR drop phenomenon consists of variations in voltage caused by the current flowing through the resistive elements in the power grid. In the past, designers rarely encountered IR drop issues. However, due to the increasing complexity and the technology shrinking size, the risks of IR drop increase in recent designs [11].

There are different factors that contribute to IR failures. The first contribution is the already said process technology. According to the Moore's law, transistor feature size decreases to enable the manufacturing of higher density designs. Moreover, commercial requests of increasingly complex chips lead to the development of larger chips overall (with higher power consumption)[12], with multiple metal layers and narrower wires with higher resistance. Another cause is in the increasing of clock frequencies [13][14]. Simultaneous clock switching introduce large IR drop on the power grid: together with the clock distribution, most circuit activity of cells in a design occurs at the same time, just beyond the clock edge, creating an instantaneous power demand and increasing the frequency will increase the hazard [8]. Missing connections due to manufacturing defects can also lead to IR drop: One example is missing vias. It may happen that, during the process to insert vias in the design, some attached points are missed, resulting in a large IR drop to a portion of the chip. Another problem concerns buffers inside the clock network. In most cases, buffers are used in some critical speed path of the clock

network, in order to speed and synchronize the entire chip. Oversized buffers increase power consumption and can create IR drop problems. Furthermore, the location and the design of pads are a further source of problems. The simultaneous working of these pads in the I/O ring, that usually have a large load, creates a strong current demand and causes IR drop.

IR drop analysis is done in order to anticipate these potential problems and prevent their effects. The consequences of IR drop affect not only one cell but also the neighboring ones and is amplified on cells having the power/ground rail in the lowest metal layers or closer to vias, which usually are more resistive [15]. The main effects are on circuit timing and logical errors. Since the voltage drop will result in a power supply reduction, this will slow the gate transition and so it will produce extra delays [16]that may compromise the circuit functionality.

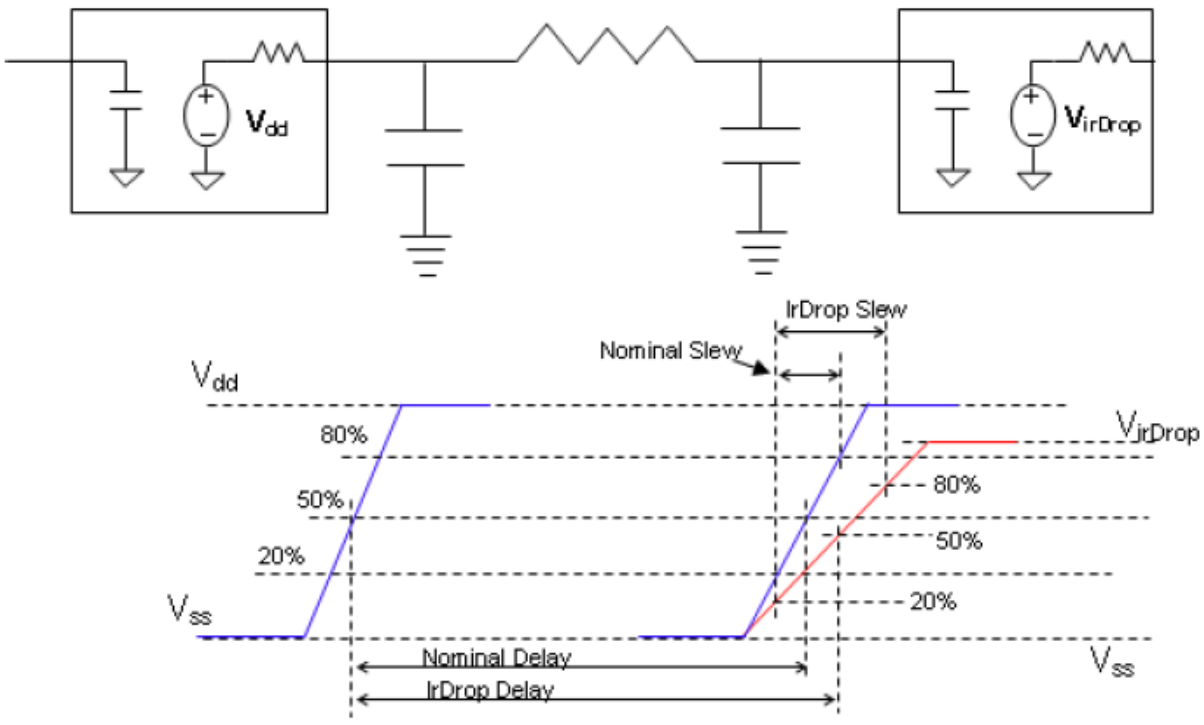

Figure 9- Effect of IR Drop [4]

A typical value for gate delay associated to a 10% voltage drop in the supply voltage can be estimated in more than 10% with respect to the nominal one[17].

Power grid analysis helps to identify regions where there is high IR drop probability. In order to do that it is needed to extract the RC (resistance and capacitance) values from the database and the netlist to simulate the power grid, and to identify the position of “virtual pads” to simulate the sources of current. In addition, the more data are available about the functionality of the chip, the more precise the evaluation can be. For this reason, we can distinguish different types of analyses: static and dynamic. Usually, all these analyses are performed in a pessimistic way, i.e., in the condition in which the circuit has the highest chance of IR drop. This leads of a production of ICs that are adjusted to work at the worst conditions that they could reach.

2.1Static IR drop analysis

Static IR drop is the simplest analysis possible. It is used in the early stages of design development in order to give some initial information about the robustness of the power grid [18][19]. In general, it consists of a simulation requiring little information, but it cannot guarantee a very realistic value of IR drop; however, a short time will be needed to simulate the circuit and it could provide an early estimation so as to highlight the most significant power grid problems. The verification with static voltage drop is not enough to ensure chip integrity because it considers only the parasitic resistance of the power grid and the average current, which is used to calculate the average voltage drop[20].

The static analysis computes an estimation of the peak current in order to determine the maximum voltage drop on each node. A typical flow for a complete IR drop analysis involves

simulating the chip with static analysis first, then verifying that the IR drop is below a user-specified threshold and then, using the results as a baseline for the dynamic analysis.

In the static analysis, a typical approaches follows the following steps [21][23]:

1. Extract the parasitic resistance of the power grid
2. Create the power grid as a resistor matrix (Figure 10)

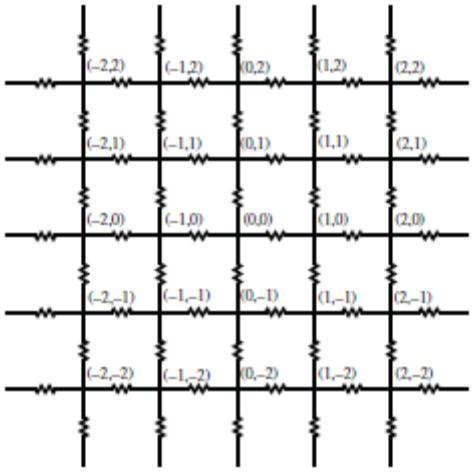

Figure 10 - Resistance power grid

3. Calculate the average current for each gate connected to the power grid
4. Distribute this average current around the resistance matrix, according to the physical location of considered gate
5. Apply for each power pad a source of VDD
6. Calculate the voltage on each cell using the current and the resistance matrix.

2.2 Dynamic IR drop analysis

Dynamic voltage drop analysis is the next step for the IR drop analysis. Dynamic analysis is used to detect integrity problems, evaluating the IR drop caused by peak current demand, due to simultaneous switching of gates, and considering the impact of decoupling capacitors and inductors[19]. To understand the very basic difference between static or dynamic analysis we can see a simple example[8]. Let us consider two timing diagrams (Figure 11).These diagrams show the current pulse for different transistors. Each current pulse has the same magnitude but a different timing. In fact, in the first one all pulses occur at once, in the second one they are spread over a period of time. In both cases, the current has the same average value for all transistors. For this reason, the static analysis will not see any difference. On the contrary, the dynamic one will see a worst IR drop in the first case, caused by the simultaneous pulse of the transistors.

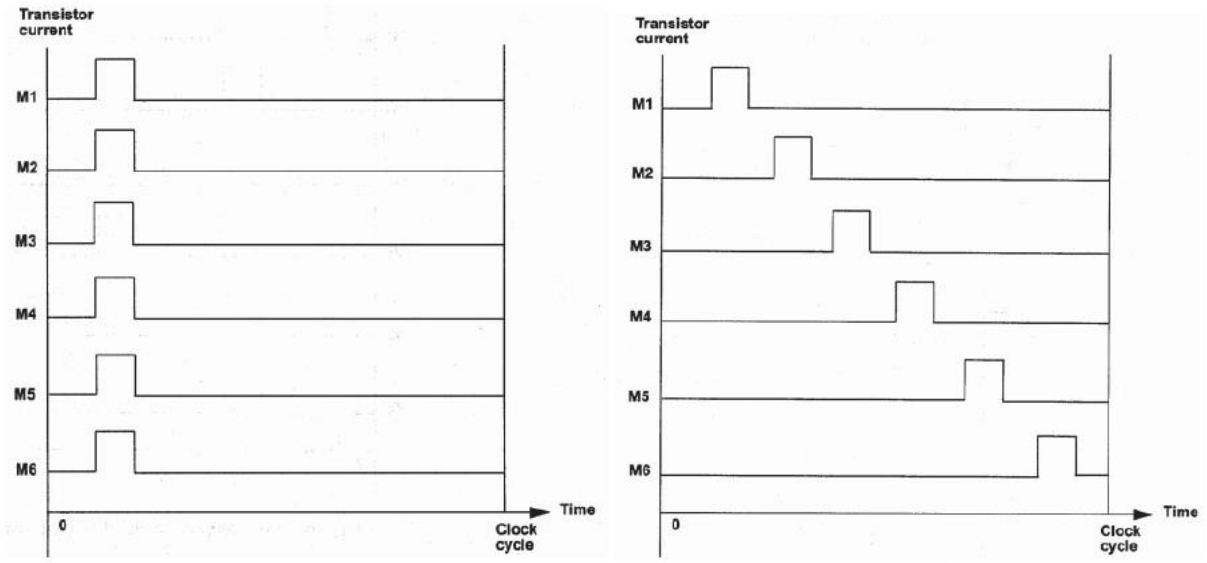

Figure 11 – Current waveform of different transistor

Dynamic analysis gives a more realistic value of IR drop and helps identifying which input activates a certain problem in the design. Depending on the input data, we can distinguish two different dynamic analyses: Vector-driven and Vectorless.

The vector-driven approach requires a preliminary functional simulation of the device. The back-annotated gate-level or post-layout simulation (i.e., considering cell and propagation delays) precisely identifies the occurrence of signal switching in time. With this data, IR-drop analysis can accurately evaluate voltage values on the power grid in time and space. From an operative point of view, signal and cell activity data is produced by the simulator in a standard file format known as Value change dump (VCD).Knowing which cells are switching and when, the tool can create a current waveform based on the internal power consumption of each cell.

Generally, the VCD file generation can be a very time-consuming process, and the result is a huge database. For this reason, the application of the analysis process using the VCD associated with a long simulation is impracticable, due to the limited resources; one method is selecting a time interval from the available dataset, based on the highest activity and the worst-case power[4].

One the other hand, the vectorless approach can be very useful for an early-stage and full-chip verification [24]. In the vectorless approach, through a probabilistic calculation, the analysis tool generates a worst-case input vector, without using actual simulation. To do that, it needs timing and activity information in order to know when and how often an instance is switching. The timing information is extracted from the data generated from static timing analysis, done during all the phases of the implementation in order to check the timing correctness.

The switching activity is set in a statistical way.

Once the power analysis is done, the tool will generate time-varying current waveforms for all instances based on the internal power defined in the cell libraries.

The calculated waveforms are then fed into the dynamic analysis tool for the calculation of the IR drop. In general, the vectorless approach is less accurate than the VCD based one, because the switching activity comes from a statistical distribution. However, constructing a worst-case dynamic voltage profile in an early stage can be very useful and offers a great improvement in terms of run time over the vector-based approach, which is not feasible for a full chip verification[25].

2.3 Gate characterization

As mentioned before, when a gate switches, due to the current flowing through the PDN to that gate, a voltage drop may appear affecting the delays of the switching gate, thus generating timing failures. In the IR drop analysis, the simulation computes this current flow and propagates it through the PDN in order to estimate the voltage drop range on each PDN node. To have a good estimation, the process requires a good characterization of the cells in terms of current draw and delay. A gate library can include current modes with different levels of approximation.

In some cases, the peak current is modeled as a simple triangular function or as a trapezoidal function as shown if Figure 12[26][27][28], where $I_{peak}$is the peak current, I_{ave} is the average current, T_{cycle} is the cycle time and T_d is the rise or fall time, assuming they are equal. If I_{ave} is less or equal than one half of I_{peak}, the current is modeled as a triangular waveform; in the other case it is modeled as a trapezoidal one.

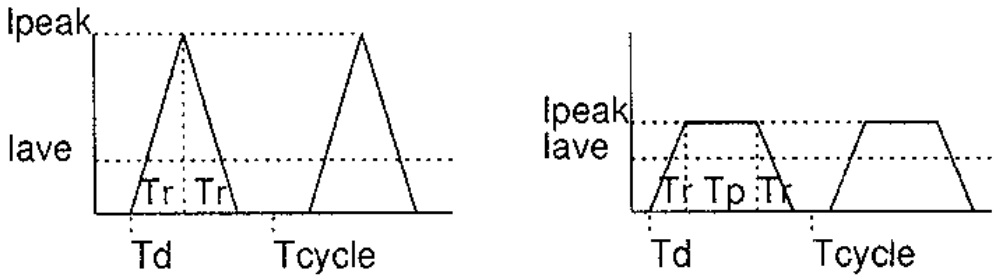

Figure 11 - Triangular and trapezoidal current models

Obviously, this implies some approximations. The cell library must include the model of all currents and the model of the delay for each gate. Keep in mind that, all these models depend on the technology. There are different parameters to consider in order to perform these characterizations [26][29]:

- **Direction of input transition**

  As explained in the previous chapter, the dynamic current depends on the operating region of MOS. Let us consider the gate of an inverter for simplicity.

  There are two different currents: I_{short}, that is the current flowing from Vdd to Gnd, and I_{load}, the current that charges and discharges the output capacitor. In a high-to-low transition I_{short} is smaller than I_{load}; part of the current flowing through the PMOS charges the output capacitance and only the rest goes toward ground.

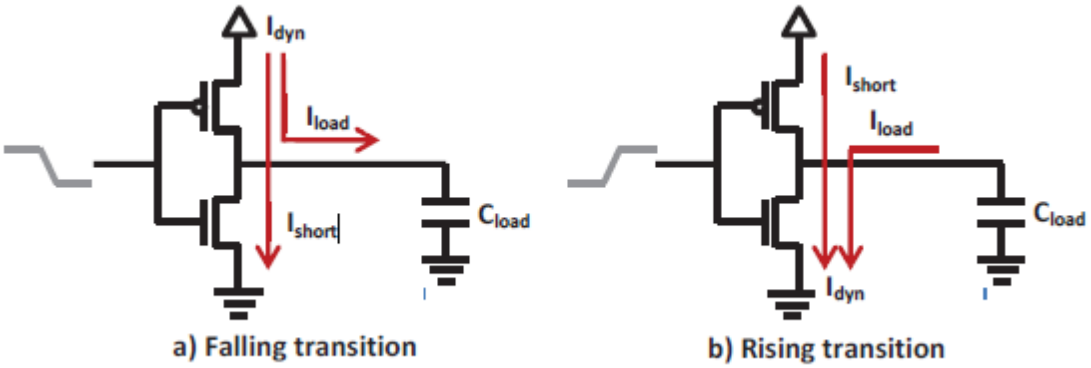

Figure 12 - Dynamic current in an inverter [29]

Vice versa, in a low to high transition, the output capacitance discharge and the current towards ground become predominant. For this reason, the dynamic current is modeled as a function of transition direction. Moreover, also the delay and static current depend on that.

- **Supply and input swings:**

  The voltage drop on power and/or ground supplies may affect current draw and delay of the gate. In addition, the upstream gate may be affected by voltage drop, which in turn can affect the considered gate. These variations in the power/ground supply and in the upstream gate produce changes in the operating region of the transistors. Therefore, it is important to consider the voltage swing of the upstream gate, called V_{swing1} or (input swing), and the voltage swing of the considered gate, called V_{swing2}or (supply swing), as defined by the equations:

$$V_{swing1}(t) = Vdd_1(t) - Gnd_1(t)$$

$$V_{swing2}(t) = Vdd_2(t) - Gnd_2(t)$$

Where $Vdd_1(t) - Gnd_1(t)$ and $Vdd_2(t) - Gnd_2(t)$ are the power/ground supply levels of the upstream gate with respect to the considered gate.

- **Capacitance load:**

  An equivalent capacitance load is used to simulate the intrinsic capacitance of the downstream gates. This equivalent capacitance load is charged and discharged during the switching process. Therefore, this output capacitance has an impact on current and delay.

Figure 14 shows the standard circuit of an inverter used for the SPICE simulation in order to characterize the gate (an inverter in this case) in all possible conditions that are likely to exist in a realistic environment.

The input inverter is used to make the input transition more realistic in terms of rise and fall time. The inverter has at the input a traditional voltage source and at the output a controlled voltage source, used to filter all the spurious variations resulting from the ideal voltage source.

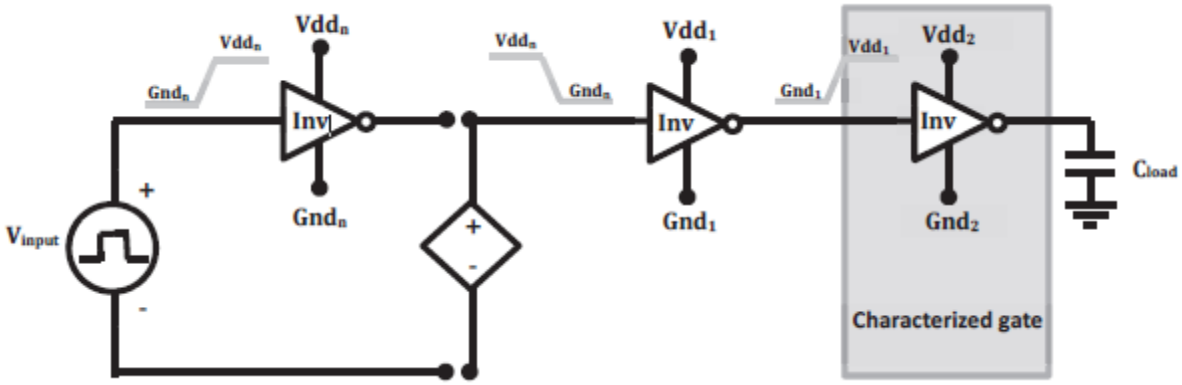

Figure 13 - Electrical schematic for the characterization of currents and delays of an inverter

At the input of the characterized gate, there is the upstream gate in order to model the supply voltage swing.

Finally, the output of the inverter is connected to the capacitance load in order to simulate the fan-out of the characterized gate, i.e., the connection to downstream gates.

As a result, Figure 15shows an example of dynamic current during the switching phase of an inverter excited by a positive transition for different values of V_{swing1}, V_{swing2} and C_{load} obtained from a SPICE simulation[26].

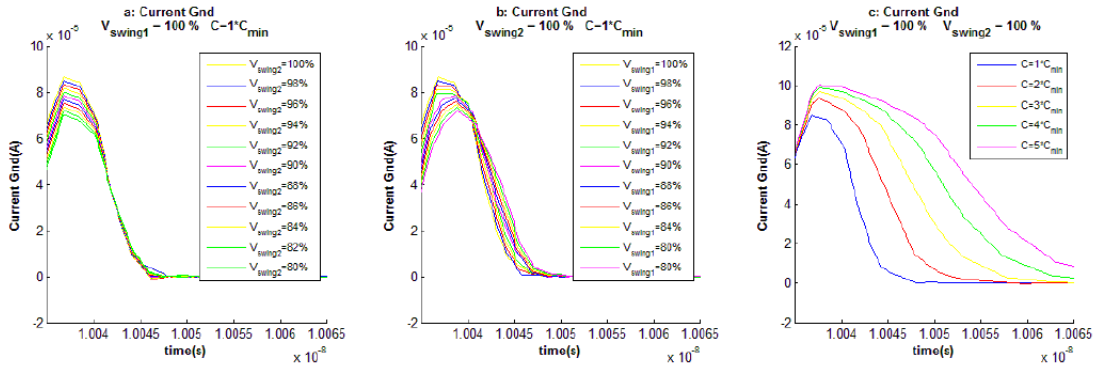

Figure 14 - Current waveforms with different values of V_{swing1}, V_{swing2} and C_{load}

The graph in a) represents the current drawn acquired by a SPICE simulation for different values of supply swing, graph b) for different values of input swing, while graph c) for different values of capacitance load. In all graphs the other two variables that are not changing are kept constant.

2.4 Thermal effect and Hot spots

During the operation of a circuit the power dissipated produces heat in the circuit.

This relationship can be derived from the laws of thermodynamics [30]:

$$T_{die} = T_{air} + \theta \cdot P_d$$

T_{die} represents the die temperature, T_{air} is the temperature of the surrounding air, θ is the package thermal impedance and P_d is the average power dissipated. As we can see from the equation, the heat on the chip is directly proportional to the dissipated power. If the temperature becomes too high, it can result in an irreversible degradation of the chip, causing a premature destruction [31]. One of the main purposes of IR drop analysis is to find these "hot-spots" caused by extensive switching activity and power dissipation. Usually the hot-spots are showed with colored maps, like in figure 16[32].

The red spot represents an extensive switching activity or some problem in the power grid. With the localization of hot-spot it is possible to identify the worst IR drop areas and react accordingly.

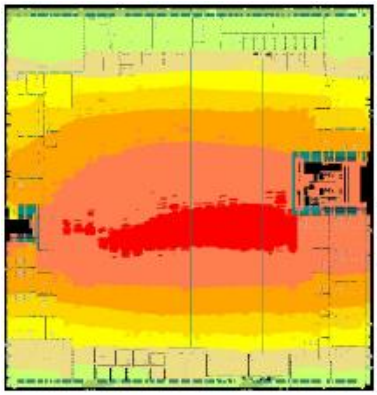

Figure 15 – IR drop map as example

Chapter 3 - Focus of this work

With modern technology, the problem of IR drop is becoming more frequent and critical. The intentions to increase circuit performance and reduce size introduce important power density problems due to the large amount of instantaneous current required from the power distribution network. This current demand, created by the logic gate switching, together with the intrinsic parasitic resistive elements of the PDN, create fluctuations in the voltage, or IR drop. It is important to understand the differences among the possible analyses, since every methodology has its own role. The focus of this thesis is pointing out the different type of analyses, including:

- Static IR drop analysis
- Dynamic Vector-free IR drop analysis
- Dynamic Vector-based (with VCD) IR drop analysis.

For static analysis, the thesis will show the resistance dependency on temperature. For this reason, I will highlight different results using different temperature. Then we will compare the most relevant result with the result produced by the vector-free and VCD-driven analysis, in order to highlight the differences.

Finally, I propose a method for a full chip dynamic vector-based analysis, called cycle selection. This method is used to select automatically a critical cycle from a large vector dump. It calculates the power for each cycle and select the one consuming the highest average power.

3.1 Proposed approaches

3.1.1 Static analysis

The static analysis is the first step for a complete IR drop analysis. The static IR drop analysis is widely used early in the flow to detect and correct problems in the power grid, such us missing vias, shorts, insufficient power routing width, etc. It is also used to simulate the average impact of the design operating for a long period; in fact, it calculates the average voltage drop associated to a user-defined circuit activity.

Even if static analysis is not optimal in precision, depending on how many input data we give to the simulation, we can have different levels of accuracy. In the analysis without functional simulation data (VCD file), the exact value of the switching current of cells is not known, because we do not know when they will switch and their exact activity. In this case, the activity is calculated with probabilistic computations, so the power dissipated will be an approximate value. Moreover, as explained in the previous chapter, the gate characterizations give better accuracy, since the tool will know the exact current behavior of each cell, and so on. It must be noted, however, that the objective of static analysis, generally, is not the highest accuracy, because the detection of power grid problems can be accomplished even without the computation of exact voltage drop values.

Since the leakage current will contribute to the value of power dissipation, it is easy to understand how the temperature can influence the voltage drop. As explained in the previous chapter, the leakage current increases exponentially with temperature, thus changing the voltage drop value as well.

Therefore, the static analysis is performed using low, nominal and high temperature.

In order to do that we need to change the corners for each simulation.

These corners are a triad of values, representing the performance of process(worst, nominal and best), voltage, and temperature. They are usually identified with the PVT acronym (from process, voltage and temperature).

By changing corner, it is possible to simulate the circuit in different conditions. Usually the worst corner for the IR drop analysis is best process, high voltage and high temperature [19].

3.1.2 Dynamic vector-free analysis

The vector-free analysis is a good surrogate for a dynamic analysis if simulation data are not available. In this type of analysis, the tool does not compute the average voltage drop over a clock cycle; instead, it performs the voltage drop calculation considering the sum of peak currents. These currents are calculated every time instant, called steps, and for each step, the voltage drop is computed.

Since we are not working with average voltage drop, we will expect higher values with respect to the static analysis. Like the static analysis, different levels of accuracy can be obtained depending on the data input given to the tool. As an example, in the vector-free analysis current gate characterization has an important weight for the same reason seen before, that is

because we are performing instantaneous peak current calculations. In fact, a the triangular or trapezoidal model can lead to inaccurate results, while more detailed models can better approximate the exact current values. In this analysis it is usually possible to obtain current waveforms for the entire chip, analyzing the time interval with highest simultaneous activity. We will see that this graph can be compared to the graph generated from the analysis with VCD.

3.1.3 Dynamic vector-based analysis with critical cycle selection

The dynamic vector-based analysis is the optimal analysis in terms of accuracy, but it requires more resources and time. The simulation vectors (VCD) are used to provide the most accurate switching information in order to construct a realistic switching scenario. In fact, every net or instance activity is determined entirely from the VCD. Similarly as for the vectorless analysis, the tool analyzes peak currents, but now it knows the exact activity of each net or instance, so the analysis can be more accurate and realistic. However, the simulation becomes much longer than in the previous case. In fact, since the large number of instances that need to be simulated, generally it is unfeasible to use the complete set of data deriving from a functional simulation of the circuit. So, the analysis is applied in the worst case only. One possible method involves the selection of the time interval during which it is present the higher activity, and perform the analysis in that interval. We can see Figure17 as an example: this represents the power waveform acquired performing the power calculation of an entire VCD. This is called FSDB (Fast Signal Database) and represent the power demand of the entire design with respect to the entire simulation time of the VCD. From that waveform, we clearly see that there are

two time intervals (inside the red rectangles) with high power demand. Therefore, one way to go is to apply the analysis in those intervals only. Therefore, if there is the possibility to produce the FSDB, one can select the intervals manually. By the way, this waveform may be difficult or time consuming to obtain, or maybe the waveform coming from the simulation can be quite regular, so selecting the right interval can be tricky.

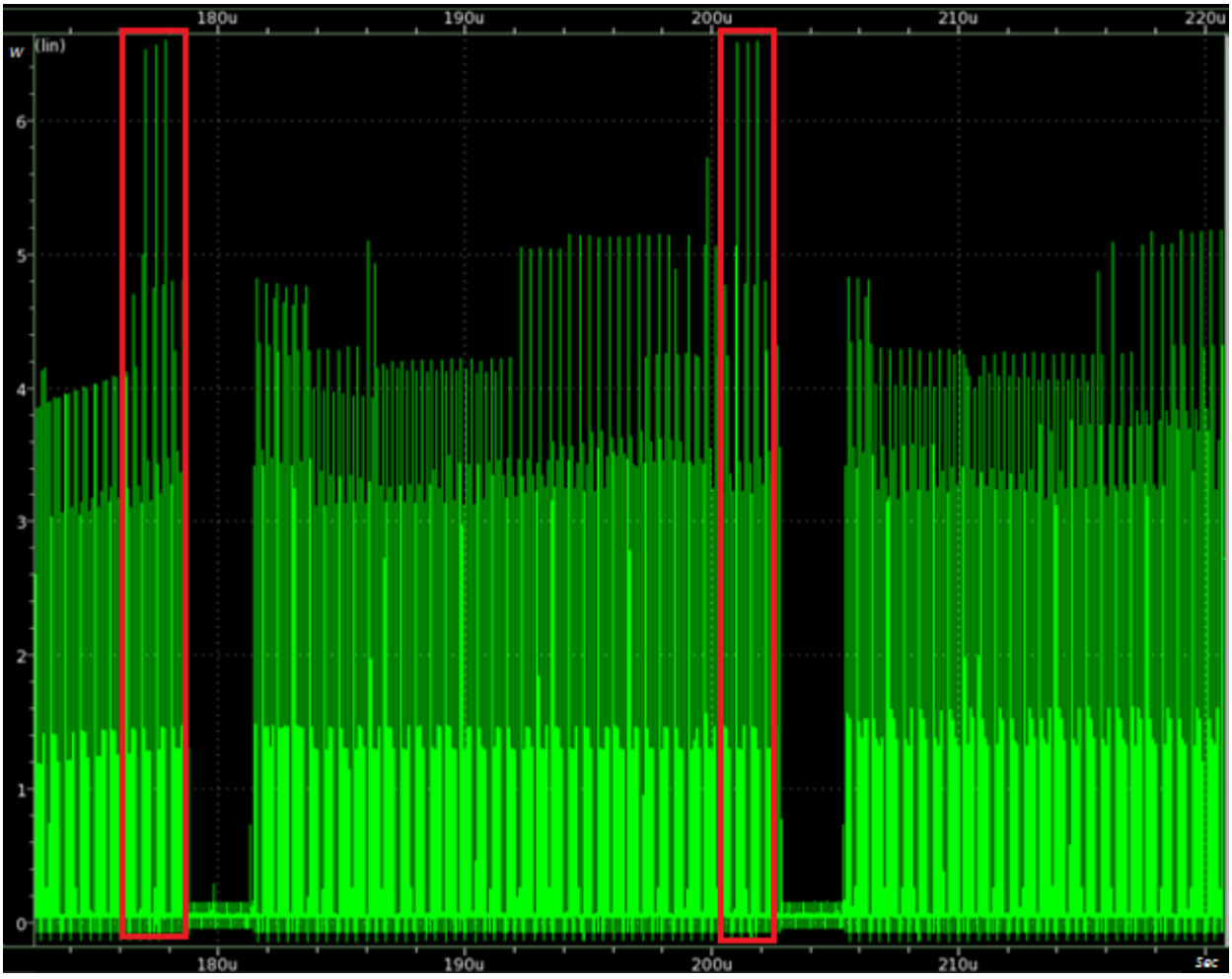

Figure 16 - Power waveform of an entire VCD

Another option is the critical cycle selection method, which is a feature offered by some analysis tools that select automatically the worst power interval. During power calculation, the tool calculates the power demand for each time span of a fixed length. Then it will apply the voltage drop analysis in the selected interval, i.e., the one with most average power consumption. Moreover, it will report a ranking in terms of average power demand and voltage change per cycle for future debug. The latter represents how much the voltage changes form one cycle to another and this can be a further cause of IR drop. By the way, the manual method is expected to be more accurate than the automatic way. The reason is that the power calculation done in the cycle selection is built to be fast, so it is less precise then the one used for the production of the FSDB, produced by a simulation of the VCD. We will see the differences in the results in the next chapters.

Chapter 4 - Implementation

Fig. 18 shows the general requirements for the Static analysis and for vectorless analysis. However, for the vector-based flow one just needs to add the VCD file.

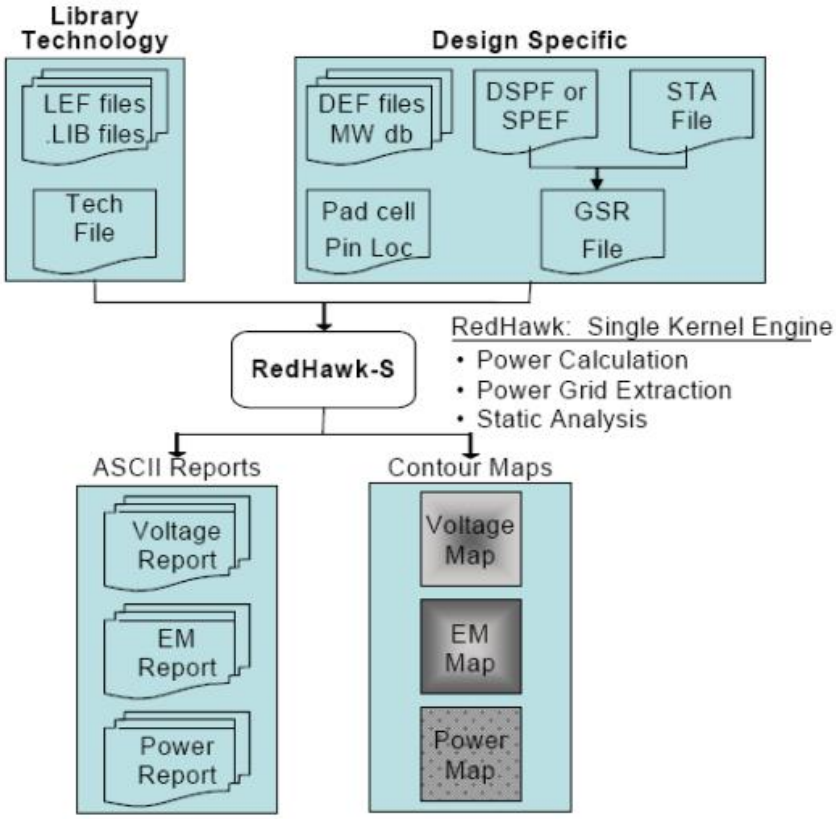

Figure 17 - General Redhawk flow [38]

The list of data file to be used by the tool is written in the GSR file (Global system requirements), that is then uploaded in Redhawk, ready for the simulation.

The LEF (Library exchange format) and LIB (Liberty format) files contain, respectively, the physical and logical description of cells, macros and pads. The LIB file also contains power and timing tables used for power calculation.

The Tech (technology format) file contains design-specific information about metal layer for each process corner. Moreover, the DEF (Design exchange format) contains physical information about the power and ground network.

These files, together with the pad file, containing the physical locations of the voltage sources, are enough for the power calculation.

It is useful to note that, in order to add more accuracy to the simulation, the SPEF (Standard parasitic exchange format) and the STA (static timing analysis) file should be used when available. The first is used to extract the signal wire parasitic data, greatly recommended for dynamic simulation. The STA file is used to add delay information, as explained in chapter 1. It includes information about minimum and maximum transition times and defines timing windows, which is the simulation time, and clock network data. This file will also provide precision in Static analysis, in fact if the timing window for a specific instance is missing, the power for that instance is assumed to be zero, unless the VCD is available.

Moreover, the Apache power library (APL) files was utilized for gate characterization. The APL is used to characterize cells, creating different samples of switching waveforms, output-state dependent decoupling capacitance, switching delay and leakage current, etc. Figure 19 shows the flow utilized for APL generation.

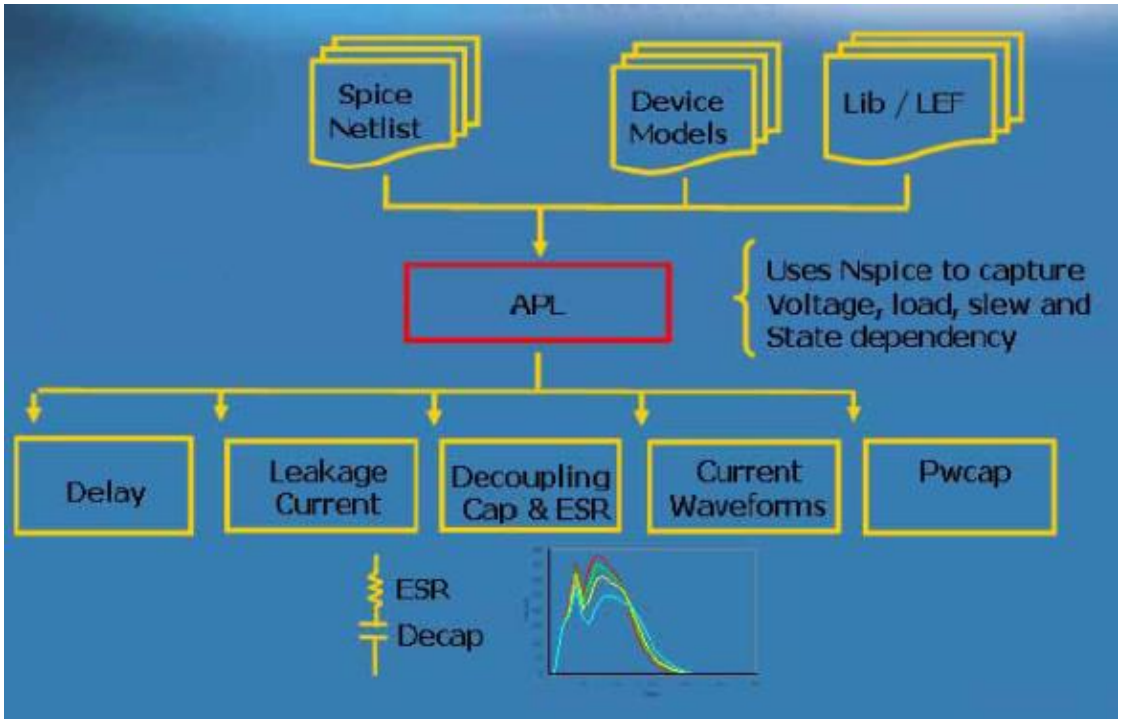

Figure 18 - APL flow for cell characterization [38]

Chapter 5 - Experimental Results

5.1 Case of study

As a case study, a design in 90nm technology with six levels of metal was selected. It is made of 792,030 Instances, with 48 hard macros including 42 memories. Figure 20 shows the floorplan of the design, with the white and yellow dots representing respectively the GND and VDD pads. The nominal voltage for this technology is supposed to be at 1.2V.

The experiments presented here are made with Apache Redhawk, one of the most used tools at the state of the art, while Cadence Incisive is the logic simulator employed.

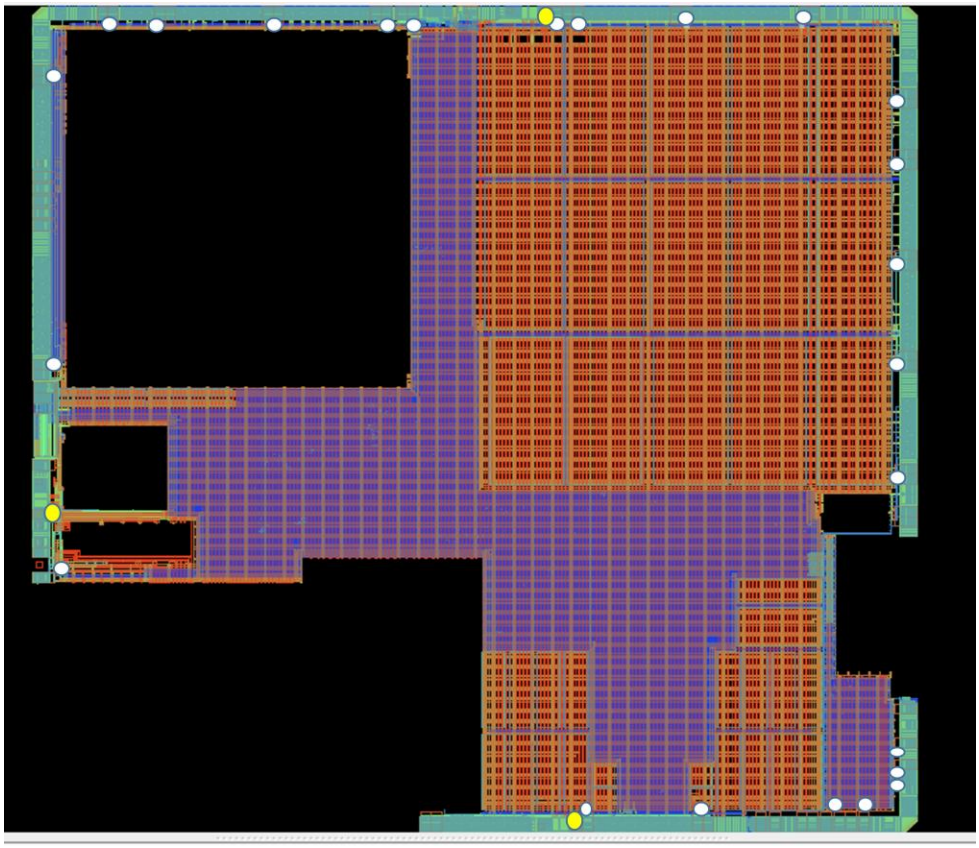

Figure 20 - Floorplan of the test case

5.2 Temperature dependency

Starting with the static analysis, three different results with different temperature values are produced. The temperature values used for this analysis are 25°C, 85°C and 125°C. The frequency is the same for all analysis, i.e.10MHz, which is the frequency of the fastest clock. We are using the worst corner, i.e. best process and high voltage, which is 1,32V that is 10% higher than the nominal voltage. The period in which the tool performs the calculation of the average current demand is the inverse of the frequency. Finally, the values of the parasitic resistances are extracted from the tech file.

Table I shows the IR drop violations for the wire and instance

Table I - Static Voltage Drop results

Temperature	**Worst Wire IR Drop (VDD)**	**Worst Wire IR Bounce (GND)**	**Worst Inst. IR Drop**
25°C	26.40 mV	19.40 mV	45.60 mV
85°C	38.00 mV	28.10 mV	65.80 mV
125°C	42.40 mV	31.40 mV	73.50 mV

In the table above, we have three types of information. The VDD drop is a reduction in voltage that occurs in the VDD network. While the GND bounce is an increment that occurs in the GND network. The combination of the VDD drop and the GND bounce is the instance voltage drop.

As we can see, when a higher temperature is applied, the VDD drop and the GND bounce increase. This is because the wires and the instances are more resistive, according to this formula:

$$R = R_{ref}[1 + \alpha(T - T_{ref})]$$

where *R* is the resistance at temperature *T*, R_{ref} is the resistance at temperature T_{ref} that usually is 20°C or 0°C. The term α is the *temperature coefficient of resistance,* which is positive for metals. Increasing the temperature will increase the resistance, and this increase the overall drop. Figures 21, 22 and 23 show the IR drop maps respectively at 25°C, 85°C and 125°C.

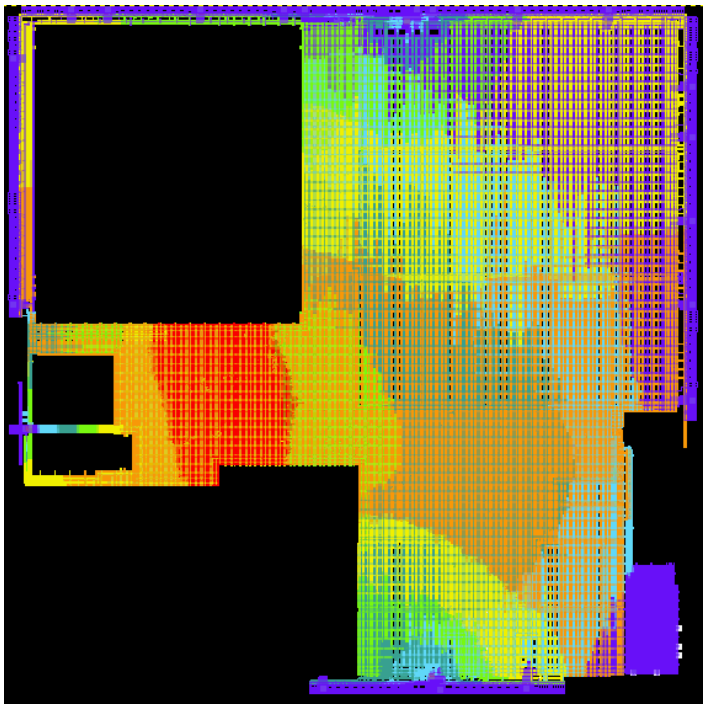

Figure 21 - Static IR drop at 25°C

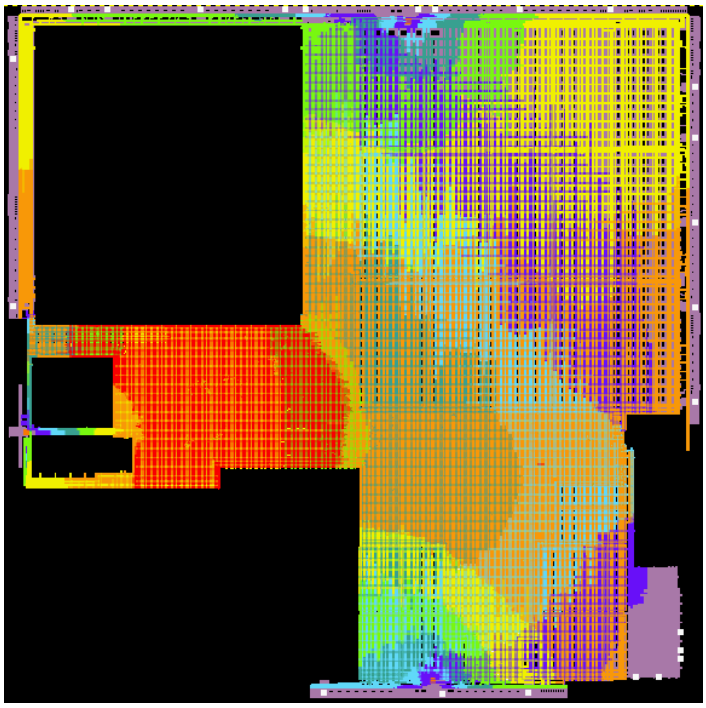

Figure 192 - Static IR drop map at 85°C

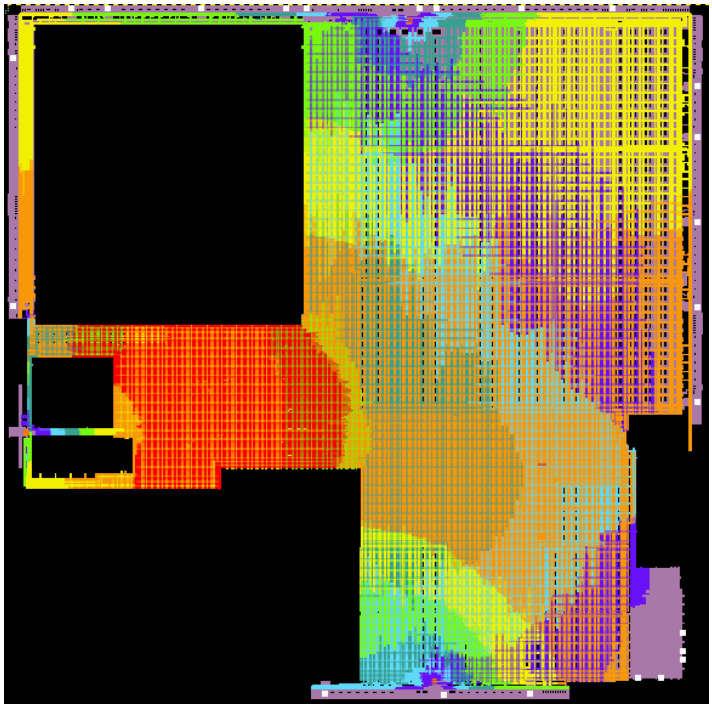

Figure 203 - Static IR drop map at 125°C

We can see clearly that the hot-spot is larger for the last analysis, highlighting a higher voltage drop.

Another important investigation that can be performed is the resistance analysis. With this process, high impedance instances can be highlighted in order to find weak points in the power/ground network. The tool calculates the effective resistance for a limited number of instances that is defined as:

$$R_{eff} = (R_{VDD} + R_{GND})$$

R_{VDD}andR_{GND} are the relative resistances seen in the VDD and GND nets.

In order to underline the resistance variation, the results of the analysis is presented. Figures23 and24 show the different resistance maps generated from the static analyses at 25°C and at 125°C.

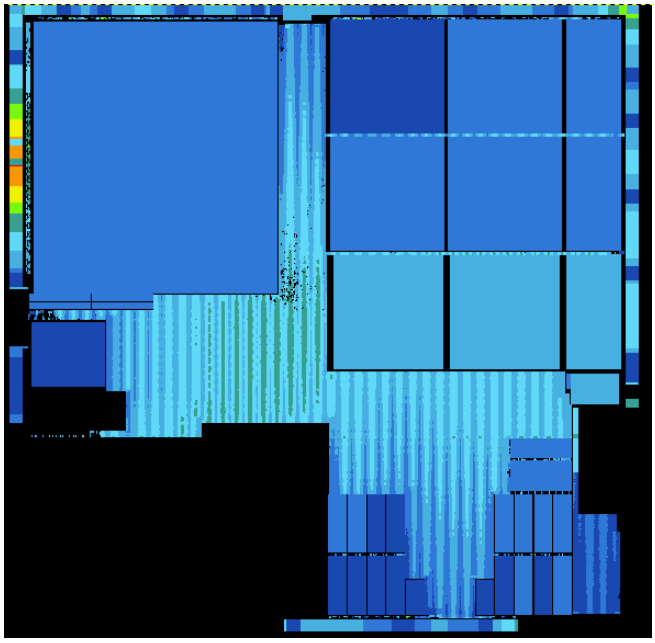

Figure 24 - Resistance map at 25°C

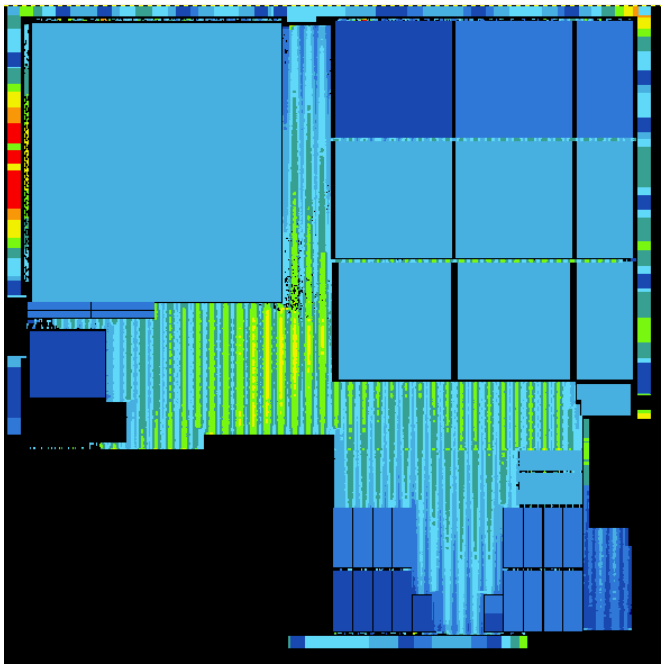

Figure 25 - Resistance map at 125°C

The yellow zonedenotes an increment of the resistance for the instances in that location and the realtive values are showed in the table II.

Table II – List of the worst instances resistance

Instance	**Res. at 25°C (Ω)**	**Res. at 125 °C (Ω)**	**Increment (%)**
i1	23.8429	28.9149	21.27%
i2	22.4972	27.073	20.34%
i3	21.0962	25.3484	20.16%
i4	19.8295	23.6117	19.07%
i5	19.2541	26.2307	36.23%
i6	19.2541	26.2307	36.23%
i7	19.0154	25.9038	36.23%
i8	18.6442	25.3953	36.21%
i9	18.3548	21.8341	18.96%
i10	18.3261	24.9593	36.20%

We can see that the resistance is greatly increased for all instances and for some of them it will exceed the 30%.

5.3 Vector-free analysis

In the vector-free analysis the results are usuallyworsebecausethe tool performs the power calculation and then the voltage drop with peak currents, so it goes without saying that the worst voltage drop will be larger. In this experiment, the switching activity is set at 0.15 for all instances, which is the default value in Redhawk for the vector-free analysis; it means that cells have 15% of chance to change state in a clock cycle. Finally we are using the worst corner possible, i.e., best process, high voltage and high temperature.Moreover, the frequency 10MHz that is the same of the static analysis and the total simulation time is1us in order to cover 10 clock periods, with a resolution of 3ns.

Since now we have the contribution of the switching activity of cells, a new hot-spot was found, as we can see in Figure 26.

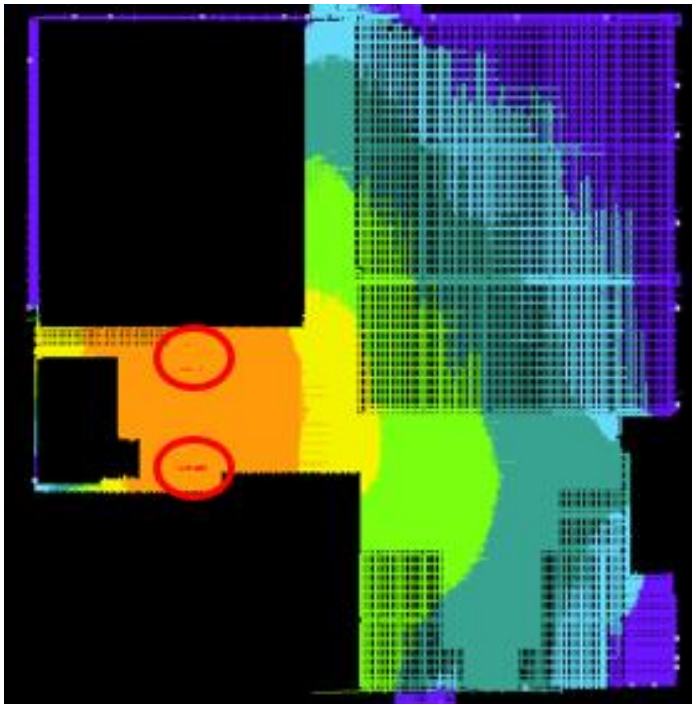

Figure 26 - IR drop map in vector-free analysis

The value of voltage drop for this analysis is 400mV, 221mV for the VDD net and 179 for the ground, higher than expected. In the vector-free analysis, the hot-spot is more localized and it is easier to identify the area with problems.

One example of solution in cases like this oneis to reinforce the stripesused by the current to reach the cells localized in the hot-spot. The red circle in figure 27(a) shows a ground pad connected to the groung network. This pad is used by a large number of cells identified by the hot-spot.

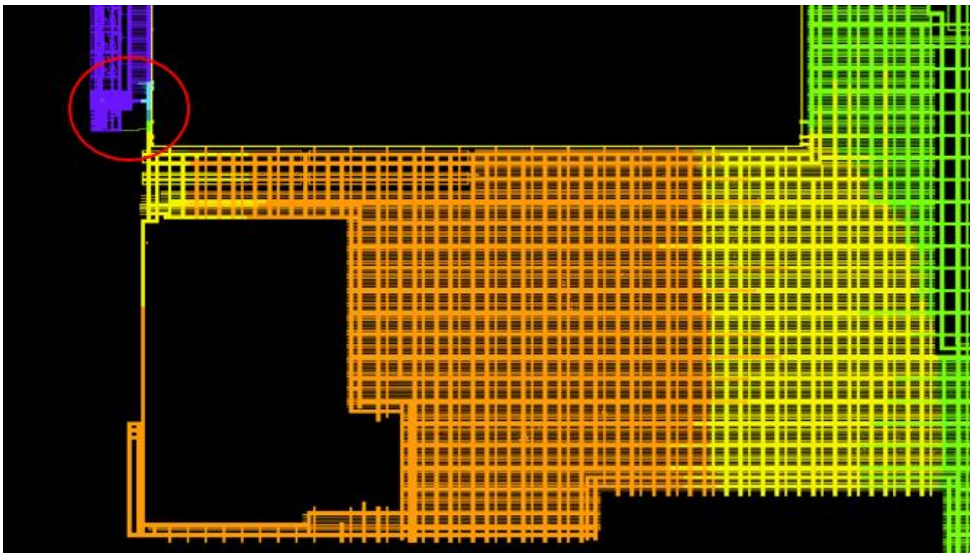

Figure 27(a) - Ground network weakness

However, the connection with the pad is made with only one stripe of metal, as we can see in figure 27(b), which is not enough for the amount of current flowing.

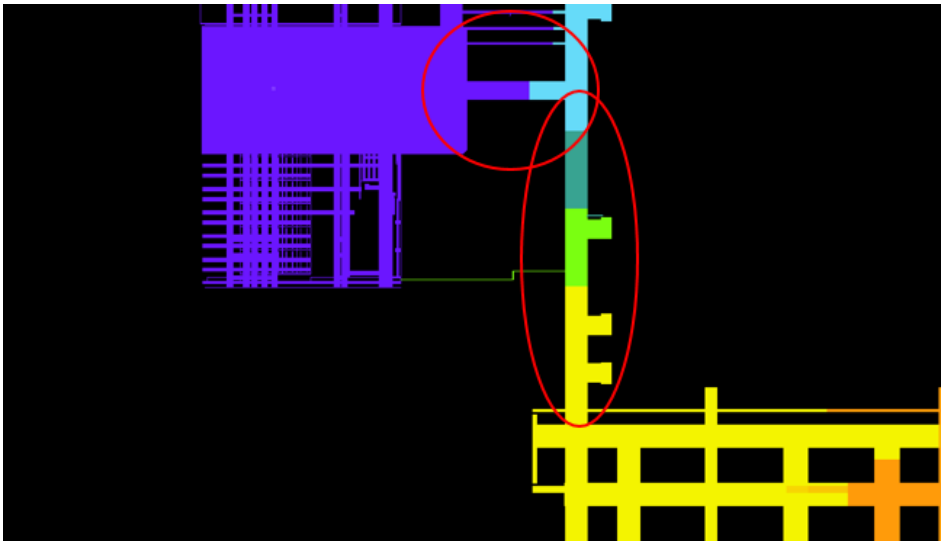

Figure 27(b)– Ground network weakness

Consequently, a solution could be reinforce this connection adding more stripes in parallel in order to reduce the resistence and to ptovide to the current another path (figure 28).

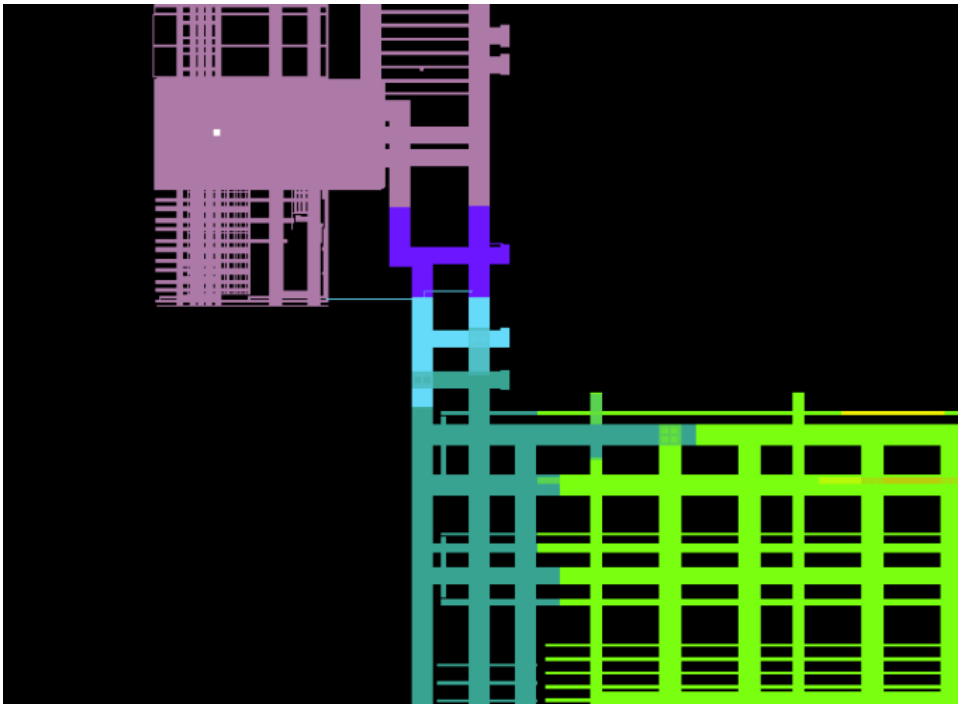

Figure 28 - Grid reinforce

With this solution we reach a value of 129 mV for the VDD net and 55 mV for the GND, with a total of 184 mV. Figure 29 shows the IR drop map after the fix.

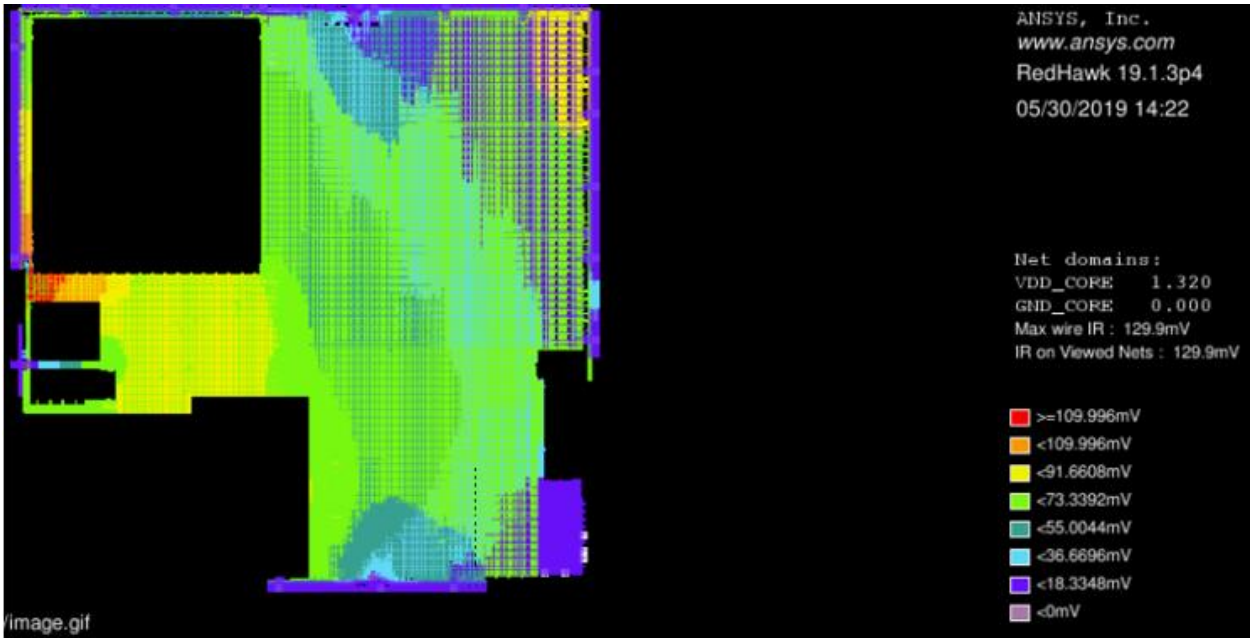

Figure 29 - Vector-free IR Drop map

To check the activity, we can see the current waveform of the entire simulation.

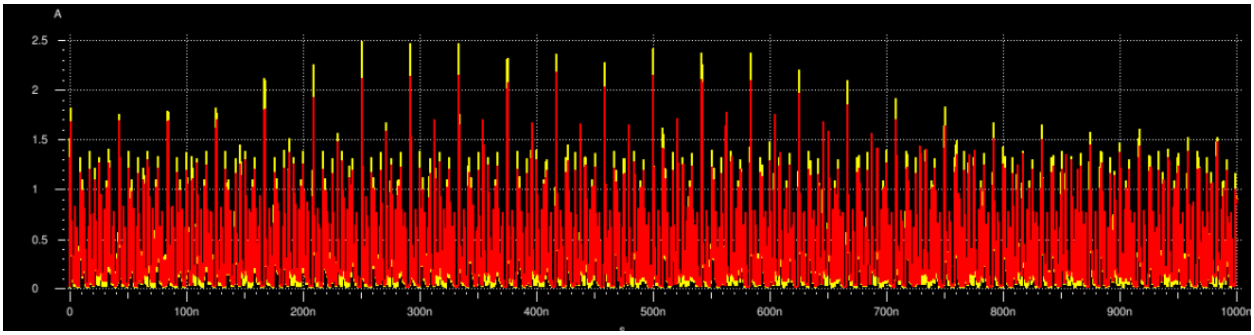

Figure 30 - Current demand waveform

The highest activity seems to be localized in the middle of the simulation. One can reduce the simulation time window in order to analyze the activity with more detail and find the interval that provides the largest contribution to the voltage drop.

5.4 Vector driven analysis and cycle selection

For the last analysis, we add the VCD file that is generated by a gate-level, back-annotated simulation. Then, the interval in which to apply the simulation is selected manually from the analysis of the FSDB, by identifying the periods with the highest current peaks. The activity is now taken from the VCD and the graph of the current demand waveform is different from the one produced by the vector-free analysis.

The results of voltage drop analysis are showed in table III, while the current demand waveform is in figure 31. Table III also shows the results of the other analyses.

Table III – Compared IR drop results

Analysis	**Worst voltage drop**
Static Analysis	73.50 mV
Dynamic Vector-free	184.30 mV
Dynamic VCD - driven	288.87 mV

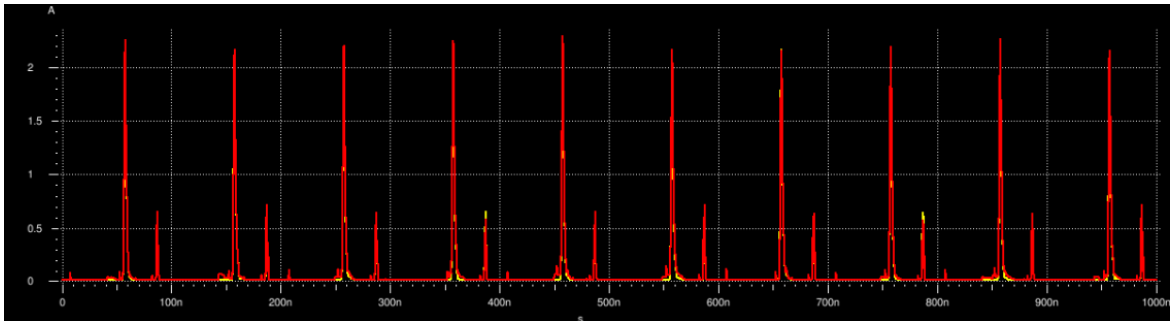

Figure 31- Peak current waveform of VCD - driven analysis

The voltage drop of the last analysis is increased due to the real simultaneous switching activity of cells and for the same reason also the peak current waveform and the IR drop map are different, as we can see in Fig. 31 and Fig. 32.However in this specific case, the obtained value can be considered acceptable.

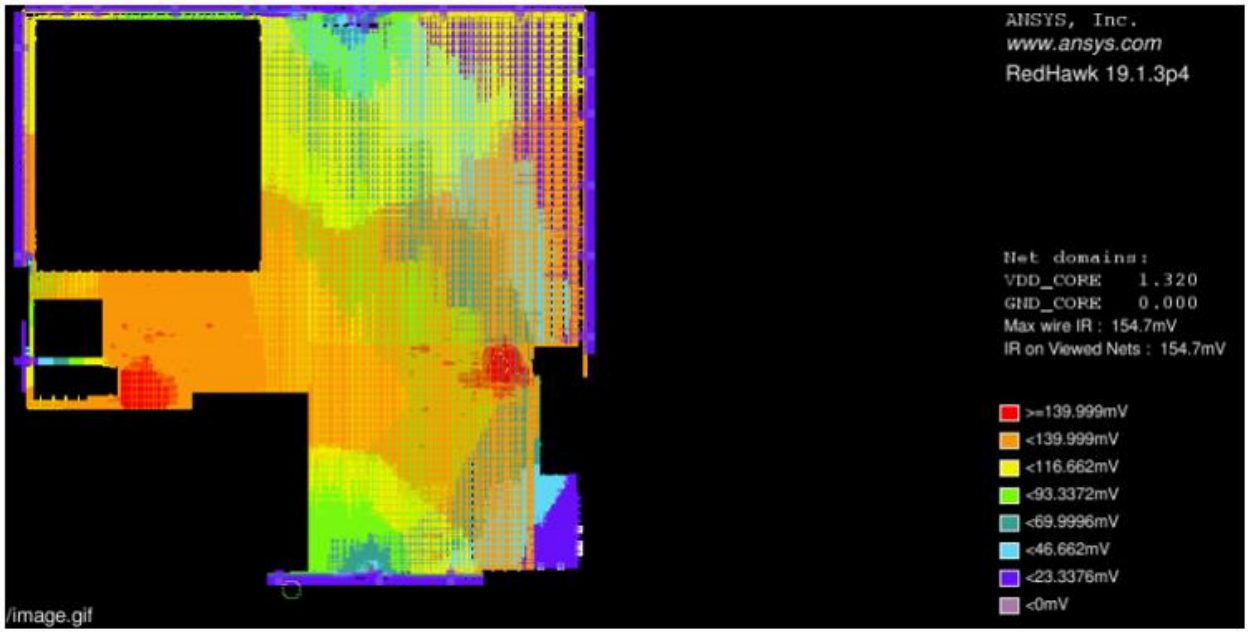

Figure 32- IR drop map of VCD - driven analysis

As mentioned in the previous chapter, if we don't have the possibility to recognize a right time interval in which to perform the simulation, we can use the cycle selection feature. Figure33 shows the IR drop map of the VCD-driven analysis in the interval chosen by the cycle selection. The map is quite similar to the one obtained with the manual method but with smaller values.

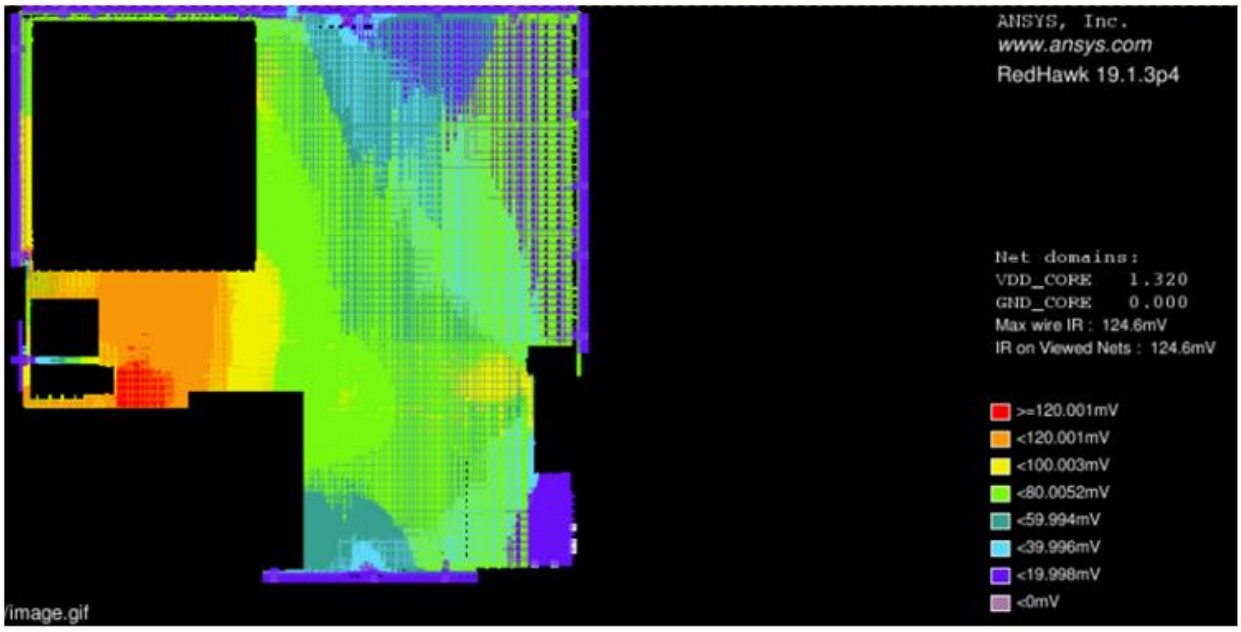

Figure 33 - Cycle selection IR drop map

In fact, the worst voltage drop registered for the instances is 234.77 mV with respect to the 288.87 mV obtained with the manual approach.

We can also see the power calculation done by the cycle selection. Table IV shows the ranking of intervals in terms of average power calculation. The interval chosen is the first one, that is from 193 µs to 194 µs. If we refer to figure 17 we can see that is different from the interval chosen previously, i.e. from 200u to 201u. By the way, this method can be used in the absence of FSDB or as double check of the manual method, because in general we cannot be sure that during the peak of power we have the worst voltage drop, since the power calculated can be equally distributed in the entire chip without creating hot spots.

Table IV - Cycle selection report

Cycle time [µs]		
Start time	**End time**	**Average power[W]**
193.083	194.083	0.163542
193.077	194.077	0.163424
193.071	194.071	0.163296
193.154	194.154	0.162314
192.946	193.946	0.162232
193.148	194.148	0.162171
193.142	194.142	0.162167

Conclusions

In today's digital integrated circuits, power consumption and IR drop problems are becoming more frequent, and knowing the power dissipation principles and the available analysis methodologies is fundamental in order to anticipate possible product issues and develop suitable countermeasures.

Three different types of analyses were presented in this work for IR drop. The static analysis is very useful in an early stage, as it can highlight most of the physical problems in the PDN with little information about the circuit and its mission. In addition, the simulation time is very fast, so it is possible to perform multiple analyses, while iteratively fixing the design in order to improve the performance. Then, the vector-free analysis is useful to improve the accuracy of the results when a functional simulation (VCD file) is not available, as it is often the case in physical implementation teams within semiconductor companies. It can give information about the possible behavior of the design during activity, even if with some approximations. Finally, the VCD driven analysis should be done for signoff. It has the best accuracy, but requires more simulation time. The analysis for an extensive simulation is often impracticable; therefore, a time interval should be selected, and ideally the one with the highest voltage drop. The problem is that the value of the drop is not known until the analysis is performed. So, it is common to select the interval with the highest power demand, even if this does not ensure the

identification of the worst voltage drop. Two methods for time selection were presented: the manual and automatic one.

All kind of analyses were performed on a device designed by STMicroelectronics in a 90 nm technology. The examination of the results helped improving the PDN, minimizing the effect of IR drop in the most critical areas. In the VCD driven experiments, the manual method has proven to be more accurate than the automated one for simulation cycle selection.

The temperature dependency was also investigated in the static analysis. However, since this variation in the voltage drop seems to be affected mainly by the resistance of the PDN, that is equal for all the analyses, we can expect the same behavior for all the cases. Therefore, it is suggested to apply the analysis with high temperature, together with best process and high voltage, in order to have the worst condition.

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