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Evaluation of TFETs perfromances for low power applications

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Indice

Summary

The main goal of the thesis was to evaluate the performances of the Tunnel FETs inside logic circuit for low power applications, highlighting the power consumption and the working frequencies reachable by this new technology. The Tunnel FETs are structurally very similar to p-i-n gated diodes, with drain and source doped in an opposite way. This particular structure allows them to generate current by means Band-To-Band-Tunneling, while the traditional MOSFETs use the thermionic emission phenomenon. The thermionic emission is ruled by the Fermi-Dirac distribution that limits the minimum subthreshold swing reachable to $60mV/dec$. The main characteristic of TFETs and the reason why the interest for these new devices rapidily increased in the last years is the possibility to break this limit leading to a steeper transcharacteristic, making possible to reach a lower voltage threshold without sacrificing the I_{ON}/I_{OFF} ratio. Thanks to this feature, it is possible to have more stable and reliable applications working at very low power supplies, in order to drastically reduce the power consumptions. The first studies done on these new promising devices pointed out that, despite the extremely low I_{OFF} guaranteed by these transistors($\leq 1fA$), they were pratically unusable for electronic applications due to the correspondingly too much low I_{ON} ($\leq 10nA/\mu m$). One of the first points of this work was, therefore, to figure out how the choice of different materials for source, drain and the channel can affect the drain current contributing to pull up the on-current. Starting from the transmission probability equation 1 , calculated using the *Wentzel–Kramer–Brillouin* (WKB) approximation, it has been showed how the energy band gap, E_g, and the potential difference between the source valence band and the channel conduction bands, $\Delta\Phi$, influence the BTBT phenomenon.

$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g+\Delta\Phi)}\right) \tag{1}$$

After a first theoretical approach to the TFET, the SPICE models of several TFET structures, derived from the results of physical TCAD simulations, have been simulated. The models have been implemented using the Verilog-A, an industry standard modeling language for analog circuits, on a Virtuoso environment. They have been explored two different kinds of approach to the modeling:

- Modeling through a Look Up Table;
- Modeling through an analytical model;

The thesis is especially focused on the latest review of the analytical model of Hao Lu whereby it has been possible to replicate the electrical behavior of the TFETs into a schematic block that can be simulated by Spectre. The circuit components obtained have been validated comparing the results obtained by Virtuoso with the ones (available online) obtained with the TCAD simulations. The simulations, firstly, have been carried out on the single devices, evaluating the main electrical parameters of the devices ($I_{ON}, I_{OFF}, SS, V_{TH}, DIBL$) and making a comparison between the various technologies. But the aim of this work of thesis is not only to examine the capabilities of the TFETs in absolute sense, but to make a comparison with the performances of a technology already used by the main foundaries, trying to understand if the interest toward this new devices is well-justified by an effective improvement of performances respect to the actual devices. The major foundaries in the world use the BSIM-CMG analytical model, developed by the Berkley's University, for the FinFETs technology, to do accurate simulations of their devices. So the parameters of this model have been tuned in order to match the electrical characteristics, found in literature, for low power FinFETs. In a second step the devices have been evaluated inside two main logic circuits for the digital electronics such as ring oscillators and SRAM cells. For the power oscillators have been evaluated the static and the dynamic consumptions, the oscillating frequency and the product power-delay, so to estimate which device guarantees the best trade-off between speed and power. In the last chapter the study of two different SRAM cells has been used as a pretext to focus on the unipolarity of the TFETs (while the traditional MOSFETs are ambipolar devices) explaining how this feature opens the way to new architectural solutions for the logic circuits. It has been analyzed a special 9-Transistors SRAM cell, developed for low power purposes, that can work only thanks to the strong unipolarity

of the tunneling FETs used, and it has been compared to another 9-transistored SRAM cell that can work only thanks to the ambipolarity of traditional MOSFETs. They have been evaluated the noise margins, the read/write delays, the energy needed for the operations and the static power consumptions. The results obtained are very promising, for low V_{DD}s the TFETs consume less static and dynamic power compared to the FinFET and in many cases they are also faster. Moreover the performances shows a weaker dependency from V_{DD} making the TFETs more robust to process variations. The drawbacks regard only the noise margins in SRAM cell, since SNMs strongly depend from the voltage threshold, but it has also been found that the difference in reliability is not as big as the difference in static and dynamic power dissipation. The TFETs seem to be the future of the electronics, but a lot of work must be done to improve the already provided analytical models, in order to be able to perform more accurate and reliable simulations, to be sure about the improvements that can be obtained with the tunneling FETs. Moreover the switch to a TFET technology could represent the end of the silicon era for the digital electronics, since the the Si TFETs show very bad performance respect to the TFETs composed by III-V groups binary and ternary compounds.

CHAPTER 1

Introduction to Tunnel FETs

The Moore's law represents the fundamental guideline for the semiconductor industry, it states the doubling of the number of transistors on an integrated circuit almost every 2 years [1]. Through the years it has led to an aggressive down-scaling of conventional MOSFETs, provoking a power crisis due to the increasing of static power consumptions [2] . In order to overcome this problem, during the last years many low leakage architectural solutions were developed but, despite the efforts made, the power crisis still exists [3] . The fastest and easiest way to reduce the power consumption is to reduce the power supply that must be at least equal to the voltage threshold of the transistors, since this value represents the minimum voltage at which the transistors can work properly. In the last years many near-threshold architectural solutions were born in order to minimize the dynamic and static power consumptions, but working in the threshold region can provoke reliability problems, since in this region the performances of the transistors are highly sensitive to the process variations. The solution is doing transistors with a lower threshold but lowering the V_{TH} implies decreasing the I_{ON}/I_{OFF} ratio. Because of the 60mV/dec limit imposed by the Fermi-Dirac distribution (that rules the thermionic emission) to the subthreshold swing, in order to have a reasonable I_{ON}/I_{OFF} ratio (greater than 10^4 at least) the threshold voltage for the traditional MOSFETs cannot go below the 300mV. In order to reduce the threshold voltage, and therefore the voltage supply, the subthreshold swing of the transistors must be lowered, but this means bypassing the Fermi-Dirac limitation using transistors with different working principles respect to the traditional ones [4] [5] . This is the reason why during the last ten years the focus on the

Tunneling FETs increased.

1.1 Tunnel FETs generality

1.1.1 Structure

Tunnel FETs structure is a MOS-like structure with the only difference that drain and source are doped differently, just like in the p-i-n diodes.

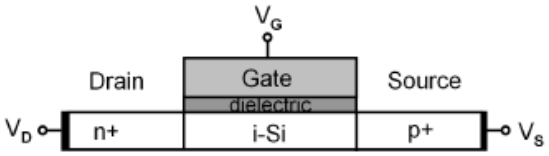

Figura 1.1: Basic structure for a single gated silicon TFET [4] .

In order to create the tunneling, the p-i-n structure must be reverse biased. In order to mantain the same logic of the traditional transistors, where conduction happens when both V_{DS} and V_{GS} are positive, in a TFET the n^+ region is referred to as its drain while the p^+ as its source. This for an ntype device(for a ptype it is the opposite) [4] [6] . Fig.1.1 represents the simpliest structure for a TFET, but in order to improve the performances of these devices more complex and advanced device structure have been explored during the last years.

1.1.2 TFETs doping

When a Tunnel FET is designed with symmetry between drain and source,and source and drain doping levels are equal, the Tunnel FET has an ambipolar characteristic. This feature is not desireable for circuit designers, because for negative gate voltages the device will conduce in the opposite sense, like a p-type device. So in this way the transfer characteristic will resemble that of a pFET when a negative voltage is applied to the gate, and that of an nFET when a positive voltage is applied to the gate (Fig.1.2) [4] .

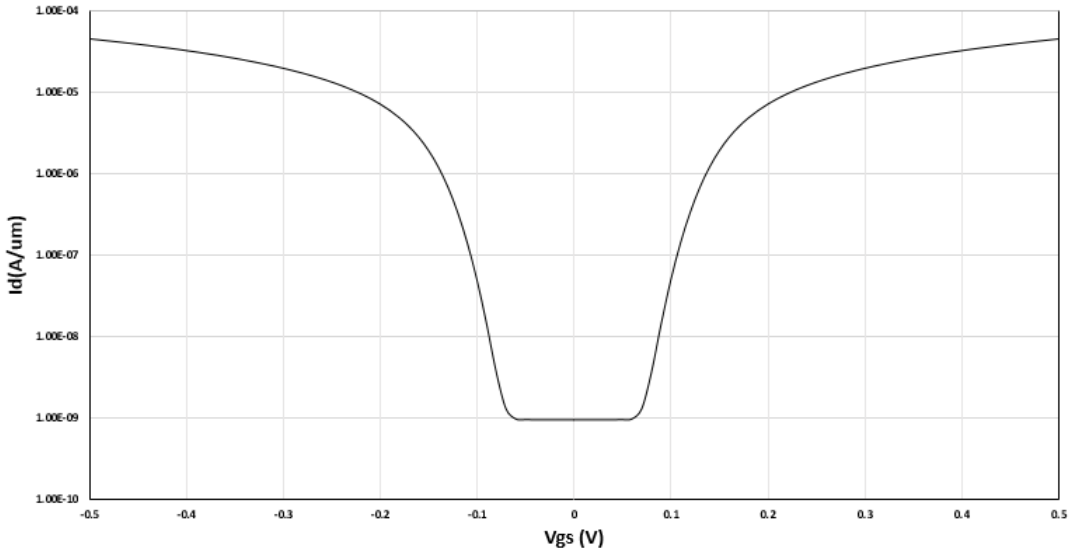

Figura 1.2: Transcharacteristic for an ambipolar TFET.

The doping levels of the Tunnel FET source and drain must be carefully optimized not only in order to maximize on-current and minimize off-current, but also to suppress the ambipolarity of the device. In particular, by increasing the source doping it is possible to increase the I_{ON} since the tunneling takes place between the source and the intrinsic region, while by lowering the drain doping the I_{OFF} decreases and the ambipolarity is suppressed (Fig.1.3). The doping of the intrinsic region does not impact in a meaningful way on the transistor behaviour until it is lower than $10^{17}cm^{-3}$ [4] .

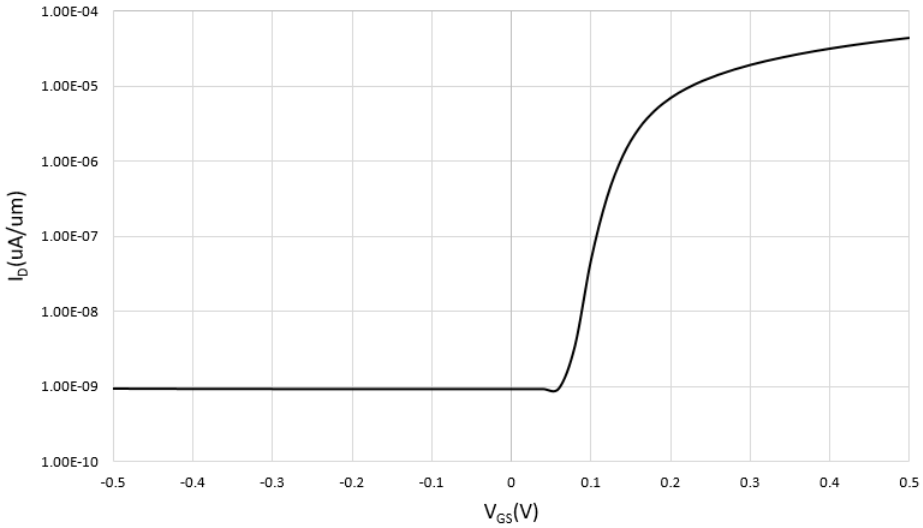

Figura 1.3: Transcharacteristic for an unipolar TFET.

1.1.3 Band To Band Tunneling

In the Tunneling FETs the carrier injection is due to the Band to Band Tunneling(BTBT) while in the MOSFETs the carriers injection is due to the thermionic emission.

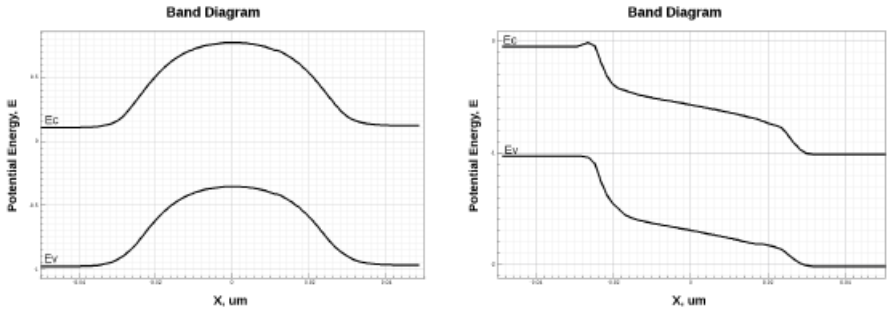

Figura 1.4: MOSFETs, OFF-state and ON-state band diagram [6] .

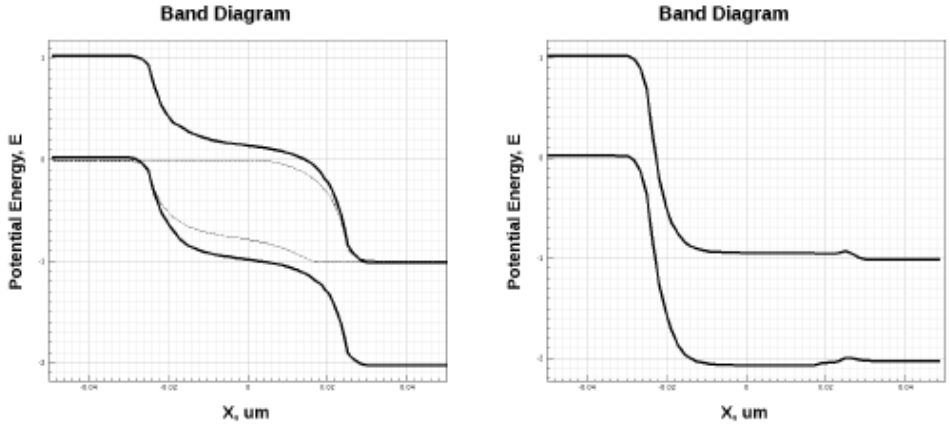

Figura 1.5: TFETs, OFF-state and ON-state band diagram [6] .

From Fig.1.4 and Fig.1.5 can be seen that while in the MOSFETs case the ON/OFF state depends from the 'height' of the pontential barrier between the n-p interface, in the TFETs case it will depends from the 'width' of the barrier between the intrinsic region and p^+. In the OFF state, the conduction for the MOSFETs is limited by the height of the junction barrier, while in ON state the positive V_{GS} lower the barrier allowing the thermionic emission of carriers [6] . In the TFETs the conduction will depend from the tunnel probability. V_{GS} modulates horizontally the junction barrier reducing the so-called *screening length* , λ, that describes the spatial extent of the transition region at the source–channel interface [6] [7] .

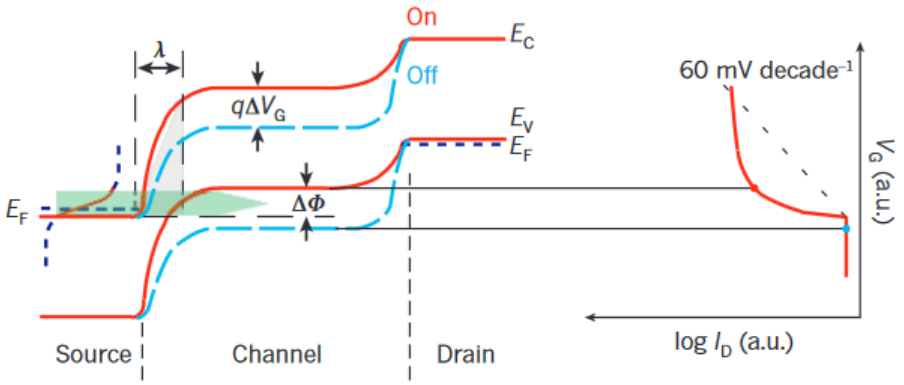

Figura 1.6: Graphical meaning of the screening lenght [8] .

The TFETs I_{ON} strongly depends on the transmission probability, T_{WKB}, of the interband tunnelling barrier, that in turn depends exponentially from λ. This barrier can be approximated by a triangular potential, as indicated by the grey shading in Fig.1.6, so T can be calculated using the *Wentzel–Kramer–Brillouin (WKB) approximation* [8] [4] :

$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g+\Delta\Phi)}\right) \tag{1.1}$$

where m^* is the effective mass and E_g is the bandgap. The drain current can be evaluated as:

$$I = A\int_{E_c}^{E_v}[F_S(E)-F_D(E)]T_{WKB}N_SN_DdE \tag{1.2}$$

Where $F_S(E)$ and $F_D(E)$ are the source and drain side Fermi-Dirac distribution and N_S and N_D are the corresponding density of states [8] [4] .

1.2 Electrical properties

The reason why the scientific community is so interested in this new technology is the possibility to overcome the limits of the Fermi-Dirac distribution, that rules the thermionic emission, allowing the TFETs to have electrical parameters that cannot be reached by the traditional transistors.

1.2.1 Subthreshold Swing

The key feature of the TFETs is the chance of achieving a subthreshold slope(SS), also referred as subthreshold swing, lower than $60mV/dec$. The point SS is defined as [5] :

$$SS = \frac{\partial V_{GS}}{\partial log(I_D)}[mV/dec] \tag{1.3}$$

But for analyzing the switching performances of these devices the parameter considered is the average subthreshold swing, that can be defined as the inverse slope of the rect that best approximates the logarithmic transcharacteristic from $V_{GS} = 0$ to $V_{GS} = V_{TH}$ [9] [8] :

$$SS_{AVG} = \frac{V_{TH} - 0}{log\frac{I_{TH}}{I_{OFF}}}[mV/dec] \tag{1.4}$$

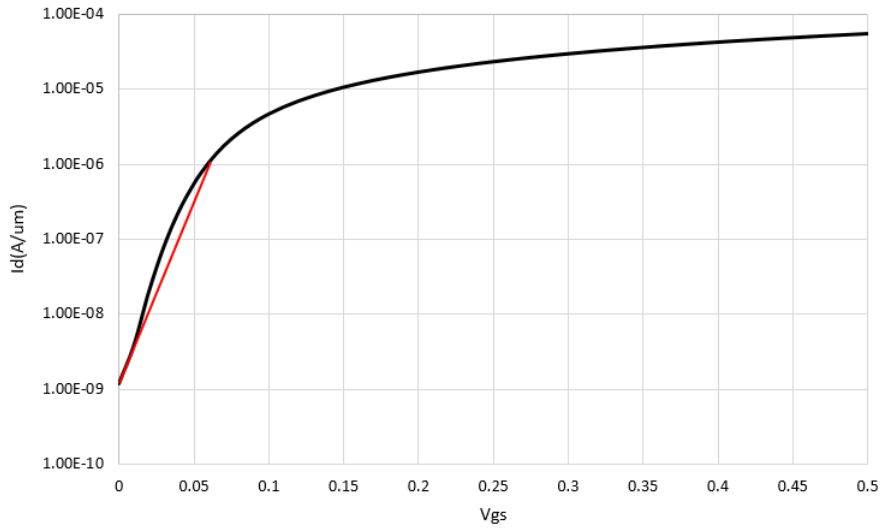

Figura 1.7: The subthreshold swing is the inverse of the slope of the rect that best fits the subthreshold transcharacteristic.

From Fig.1.7 it is possible to see the graphical meaning of the SS parameter. The

inverse of the slope of the red rect is the SS of the TFET. Why is so important having a low Subthreshold Slope?

The SS is the variation of V_{GS} needed to increase of one decade the magnitude of the drain current. The lower will be SS the greater will be the growth of I_D for a same ΔV_{GS}. This means that the TFETs are able to reach a much higher $\frac{I_{ON}}{I_{OFF}}$ ratio, or better, for the same I_{OFF} it is possible to have a greater I_{ON}, but most important mantaining the same I_{ON} respect to the traditional MOSFETs it is possible to reach a much lower I_{OFF}. In this way the static power consumption can be reduced. But it is also possible to reduce the voltage threshold of the transistors mantaining a reasonable $\frac{I_{ON}}{I_{OFF}}$ ratio. By lowering the V_{TH} of the transistors it is possible to lower the power supplies for the circuits and since the power consumptions for a single transistor are given by [8] [10] :

$$P_{DYNAMIC} = fC_L V_{DD}^2 \tag{1.5}$$

$$P_{STATIC} = I_{OFF} * V_{DD} \tag{1.6}$$

both static and dynamic consumptions can be strongly limited by lowering V_{DD}. For the classical MOSFETs the theoretical lowest SS reachable is $60mV/dec$ and this is due to the fact that the thermionic carriers injection obeys to the Fermi-Dirac distribution [8] [10] :

$$f(E) = \frac{1}{1 + e^{\frac{E-E_F}{K_B T}}} \tag{1.7}$$

This led to the SS expression:

$$SS \simeq \left(1 + \frac{C_d}{C_{ox}}\right) ln\left(10\frac{K_B T}{q}\right) \tag{1.8}$$

Since for the FD-SOI technology $C_{ox} >> C_d$:

$$SS_{MIN} \simeq ln\left(10\frac{K_B T}{q}\right) \simeq 60mV/dec \tag{1.9}$$

TFETs instead deal with the direct Band To Band Tunnelling (BTBT) as the main mechanism for electrons injection in the channel and this allows to circumvent the limitations of the classic devices.

1.2.2 Low Ion problems

The most frequent criticism of Tunnel FETs, as a conventional MOSFETs replacement, regards the extremely low on-current [4]. In fact, silicon double gated TFETs I_{ON} can reach only few dozens of nA, making them non competitive with highly scaled MOSFET[6]. In order to enhance the I_{ON} it is possible to create hetero-junctions with a narrow band gap channel materials while source and drain must have an higher E_g. It can be useful to recall the equation for the transmission coefficient T_WKB:

$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g+\Delta\Phi)}\right) \tag{1.10}$$

Where E_g is the Energy Gap for the channel, while $\Delta\Phi$ is the potential difference between the source valence band and the channel conduction bands [6] . Reducing the band gap at the source-intrinsic region junction allows to raise the on-current by several orders of magnitude. For example using an homojunction TFET in InAs it is possible to reach an $I_{ON} = 80\mu A/\mu m$. However reducing the channel band gap not only has effect on the on-current, but increases also the off-current [11] .

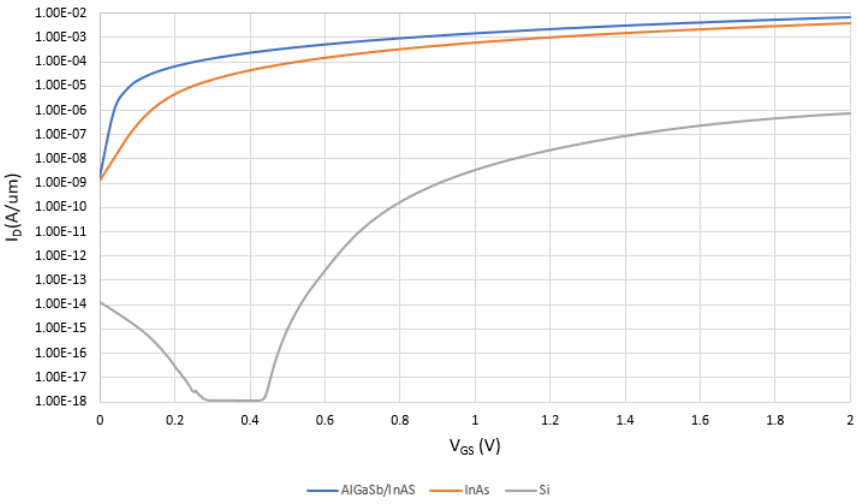

Figura 1.8: Comparison between a double-gated silicon TFET [6], an InAs (narrow band gap material)homojunction TFET, and an heterojunction TFET.

From the Fig.1.8 and from literature can be noticed that the TFETs that show better performances are the hetero-junctions composed by III-V ternary or binary compounds. The compounds with lower energy band gap are usually used for the channel while

the compounds with higher band gap are used for source, as a result T_{WKB} and I_{ON} exponentially increase.

MATERIAL	BAND GAP (eV)
InAs	0.354
InN	0.7
Si	1.11
InGaAs	0.75

Tabella 1.1: Materials used for TFETs channel [12] [13] [11] [14] [15] [16] [17].

MATERIAL	BAND GAP (eV)
Si	1.11
AlGaSb	-1.18 - 0.69
GaSb	0.68
InAs	0.354
GaN	3.2
AlGaAs	-0.127 - 1.183

Tabella 1.2: Materials tipically used for TFETs Source and Drain [12] [13] [11] [14] [15] [16] [17].

1.2.3 Tunnel FET temperature characteristics

It has been also demonstrated that TFETs are weakly dependent on temperature, since they works on the base of band-to-band tunneling mechanism that has lower dependency from temperature respect to the thermionic emission [6] [14] .

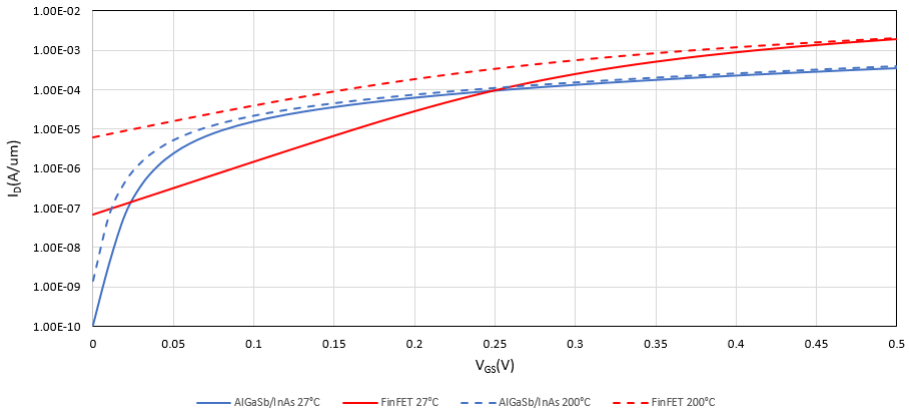

Figura 1.9: Comparison between the transcharacteristic of a FinFET and the transcharacteristic of an AlGaSb/InAs TFET at 27°C and 200°C.

In Fig.1.9 a difference in temperature dependency was evaluated, and was demonstrated that the conventional FinFET shows an higher variation in the subthreshold current respect to the Tunnel FETs. This is mainly due to the temperature dependence of TFET only on the energy band-gap term, rather than on mobility and threshold voltage as in the traditional MOSFETs case [6]. This has a great impact also on circuit reliability.

CHAPTER 2

Hao Lu Model

The first step to evaluate the electrical characteristics of a new technology is configuring physical simulations with TCAD softwares like Silvaco or Sentaurus. Then in order to move from the 'device world' to the 'circuit world', the results obtained from the physical simulations must be organized into a model cards that can be simulated by circuit simulators, like Spectre or HSPICE, so to make accurate performance predictions also at a circuit level. There are two ways of approaching this problem:

- Through a Look Up Table (LUT approach). With this method the data obtained with TCADs are passed to the circuit simulators without any elaboration. This is surely the simpliest and the easiest way, ,but the simulators tipically do not deal very well with a LUT approach and can have divergence issues;
- Through an Analytical Model. With this method the data obtained at physical level are used to fit the parameters of a chosen mathematical model, supposed to best describe the behaviour of the device. This method is much more complex but it is the preferred by the simulators, and allows to do faster circuit simulations, with clean waveforms and more reliable results.

Both these methods can be implemented in Verilog-A, an industry standard modeling language for analog circuits [18] .

2.1 Analytical Models

Various analytical models have been implemented, during the last years, in order to describe as precisely as possible the behaviour of the FinFETs, so to be able to predict the possibilities of this technology. Every model has its strenghts and its weakness and the user must choice the most appropriate for his own purpose.

2.1.1 Praveen Model

The strenght of the model defined by Praveen is to be strongly dependent on the gate geometry [6] . Since the screening length is defi

ned as the spatial extent of the electric

field, or the length over which an electric charge has an influence before being screened out by the opposite charges around it [19] , it is possible to define three different expressions for λ:

- For a single gated transistor:

$$\lambda_{SG} = \sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}} t_{si} t_{ox}} \tag{2.1}$$

- For a double gated transistor:

$$\lambda_{DG} = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}} t_{si} t_{ox}} \tag{2.2}$$

- For an all around gated transistor:

$$\lambda_{GAA} = \sqrt{\frac{2\epsilon_{si} t_{si}^2 (1 + \frac{2t_{ox}}{t_{si}}) + \epsilon_{si} t_{si}^2}{16\epsilon_{ox}}} \tag{2.3}$$

Where ϵ_{si} and t_{si} are the dielectric permittivity and thickness of the silicon (or semiconductor in general), and ϵ_{ox} and t_{ox} are the dielectric permittivity and thickness of the gate dielectric [20] . The current expression in the TFET model is an experimentally well-estabilished equation for band-to-band Zener tunneling in planar p-n junctions [21] , used also in other models:

$$I_{dt} = afEV_{tw}e^{-b/E} \tag{2.4}$$

with the electric field that is dependent on the gate geometry:

$$E = (\Delta\Phi + E_g)/\lambda \tag{2.5}$$

where the parameters a and b are defined as:

$$a = \frac{WT_{ch}q^3}{8\pi^2\hbar^2}\sqrt{\frac{m_r^*}{E_g}} \tag{2.6}$$

$$b = \frac{4\sqrt{2m_r^*E_g^3}}{3q\hbar} \tag{2.7}$$

the f factor is given by:

$$f = \frac{1 - e^{-\frac{V_{dse}}{\Gamma}}}{1 + e^{\frac{V_{thds} - V_{dse}}{\Gamma}}} \tag{2.8}$$

Γ is defined as *saturation shape parameter*, V_{dse} is dependent on the drain-to-source voltage:

$$V_{dse} = V_{dsmin}\left[\frac{V_{ds}}{2V_{dsmin}} + \sqrt{\Delta^2 + \left(\frac{V_{ds}}{2V_{dsmin}}\right)^2} - \sqrt{\Delta^2 + 1}\right] \tag{2.9}$$

$$V_{thds} = \Lambda tanh(V_{gs}) \tag{2.10}$$

The tunneling window, V_{tw} is defined as:

$$V_{tw} = ln\left(1 + e^{\frac{V_{gs} - V_{th}}{U}}\right) \tag{2.11}$$

And U is called *Urbach Factor* [20] [6] [21] .
By implementing these equations in Verilog-A it would be possible to explore the performances between the different gate geometries inside logical circuits.

2.1.2 Dash Model

Dash developed a single gate SOI–TFET analytical model to calculate the tunneling current using nonlocal BTBT phenomena. The tunneling process of charge carriers has been realized analytically using initial and final tunneling point, which both play an important

role for the estimation of the DC parameters such as SS,ON-current and transconductance. The surface potential profile and electric field characteristics are also derived for the developed model [22] .

Dash, Kumari and Mishra started from Laplace equation for the potential along the channel:

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = 0 \tag{2.12}$$

then defining:

$$\phi(x,y)|_{y=0} = V_s(x) \tag{2.13}$$

they found:

$$V_s(x) = C_0 e^{\alpha x} + C_1 e^{-\alpha x} - (V_{FB} - V_{gs}) \tag{2.14}$$

where:

$$C_0 = \frac{1}{2sinh(\alpha l)}\left[-V_{bi}(1+e^{-\alpha l}) + (V_{FB}-V_{gs})(1-e^{-\alpha l}) + V_{ds}\right] \tag{2.15}$$

$$C_1 = -\frac{1}{2sinh(\alpha l)}\left[-V_{bi}(1+e^{\alpha l}) + (V_{FB}-V_{gs})(1-e^{\alpha l}) + V_{ds}\right] \tag{2.16}$$

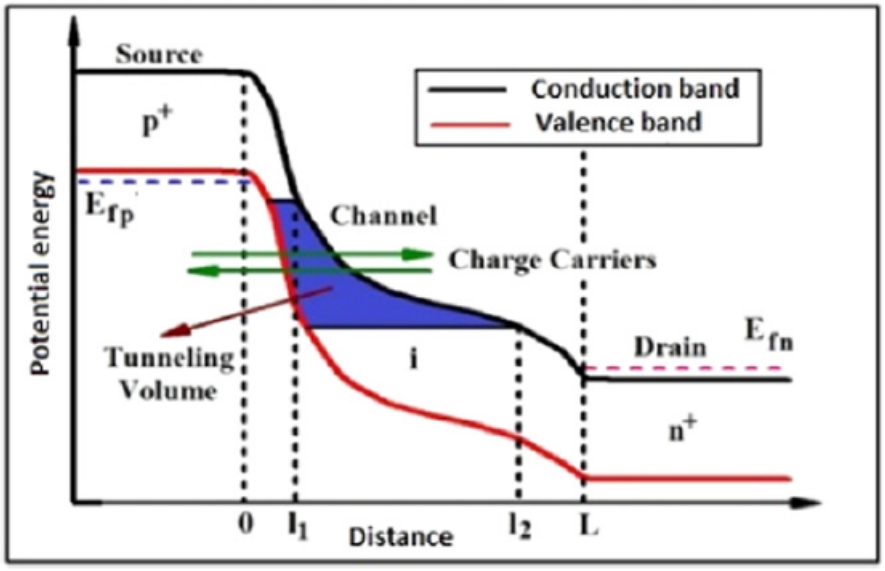

Figura 2.1: Energy band diagram of n-channel SOI–TFET in ON-state [22] .

From Fig.2.1 can be seen that this model does not use the WKB approximation, and tunneling path is defined as the distance between l_1 and l_2 along the x-axis of the channel and is responsible for BTBT of carriers:

- l_1 is defined as the initial tunneling length from the source which indicates the start of the BTBT tunneling process and can be evaluated as

$$l_1 = \frac{1}{\alpha} ln \left(\frac{Z + \sqrt{Z^2 - 4C_0C_1}}{2C_0} \right) \tag{2.17}$$

  where:

$$Z = V_{bi} + \frac{E_g}{q} + (V_{FB} - V_{gs}) \tag{2.18}$$

- the final tunneling length l_2 indicates the end of the tunneling process and can be calculated as the value of x in the channel region at which surface potential is maximum:

$$l_2 = \frac{1}{\alpha} ln \left(\sqrt{\frac{C_1}{C_0}} \right) \tag{2.19}$$

The drain current in the BTBT process can be evaluated by the help of band to band generation rate, $G_R(x, y)$, that for a single gate TFET is defined as:

$$G_R(x, y) = A_K E_{avg}^{D-1} E_x e^{-B_K/E_{avg}} \tag{2.20}$$

where:

- A_K and B_K are the Kane's tunneling-dependent parameters;
- D defines the type of BTBT tunneling phenomena: in Kane's model, D=2 represents direct tunneling process and D=2.5 is for indirect tunneling;
- E_{avg} is the average elctric field, expressed as $E_{avg} = \frac{Eg}{q(l_2-l_1)}$;
- E_x is the electric field along the x-axis and is defined as the derivative of the potential along x: $E_x = -\frac{\partial\phi(x,y)}{\partial x} = -C_0\alpha e^{\alpha l} + C_1\alpha e^{-\alpha l}$;

The tunneling current can be determined by integrating the band to band generation rate over the tunneling volume:

$$I_D = \int\int G_R(x, y)dxdy \tag{2.21}$$

but since tunneling process mainly takes place along the channel in the x-axis, therefore the lateral electric field has been considered in the drain current analysis:

$$I_D = q\int_0^{t_{si}}\int_{l_1}^{l_2} A_K \frac{Eg}{qx}(-C_0\alpha e^{\alpha x} + C_1\alpha e^{-\alpha x})e^{\frac{-B_K qx}{Eg}}dxdy \tag{2.22}$$

It is possible to see that the Dash model represents a completely different approach, respect to the Praveen model, to the task of giving an analytical description of the drain current in TFETs [22] [6] .

2.2 Hao Lu Model

The Hao Lu model represents maybe the most famous analytical model for the description of the TFETs, and the model cards based on it have been largely used to evaluate the performances of this technology [23] [24] . The model is valid in all four operating quadrants of the TFET and it is based on the Kane-Sze formula for tunneling. The model captures the distinctive features of TFETs such as bias dependent subthreshold swing, superlinear drain current on-set, ambipolar conduction, and negative differential resistance (NDR). In 2016 the model has been enhanced by adding a gate tunneling current model, a charge-based capacitance model, since the previous capacitance model was not charge based and the charge conservation was not guaranteed for all possible parameters values [24] [25] .

2.2.1 Drain Current

From Fig.2.2 can be noticed that for $V_{gs} = 0$ the device is in an off-state. When zero bias is applied to the gate, the conduction band minimum of the channel is above the valence band maximum of the source, so band-to-band tunneling is suppressed. A tunneling window, qV_{tw}, opens as the conduction band of the channel is shifted below the valence band of the source. Electrons in the valence band with energy in this tunneling window tunnel into empty states in the channel and the transistor is ON. The principle of operation is the same for the p-channel TFET with source, channel and drain conductivity types switched. However, the TFET can turn-on at the channel drain junction when the gate bias is sufficiently negative, when this happens the tunneling window opens up again, with the tunnel junction shifted from the source-channel junction to the drain-channel junction, the channel conduction changes from one carrier type to another and the transfer characteristic is said to be ambipolar [24] [25] .

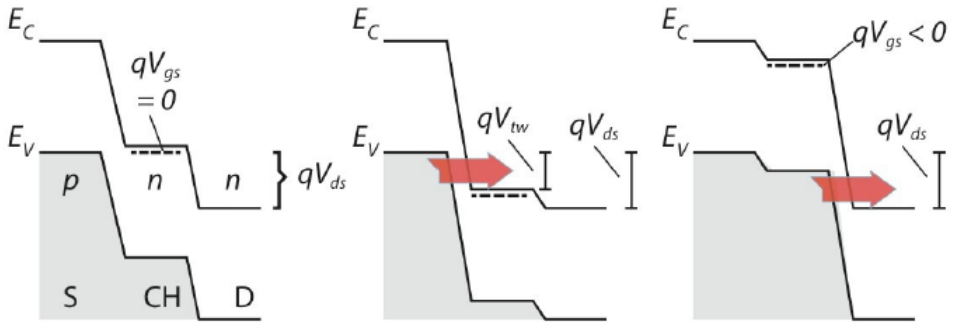

Figura 2.2: Energy band diagram of an n-channel TFET when the device is biased in OFF, ON and in ambipolar state [25] .

The TFETs are tipically projected in such a way as to be strongly unipolar with an asymmetric source/drain junction that results in asymmetric characteristics both as a function of drain-source bias, V_{ds}, and gate-source bias V_{gs}. In the negative drain-source bias polarity, $V_{ds} < 0$ with positive V_{gs},TFET behaves like an Esaki diode, band-to-band tunneling current first increases toward a current maxima, followed by a region of NDR or a current plateau, followed by an exponentially-increasing diffusion current [24] [25] .

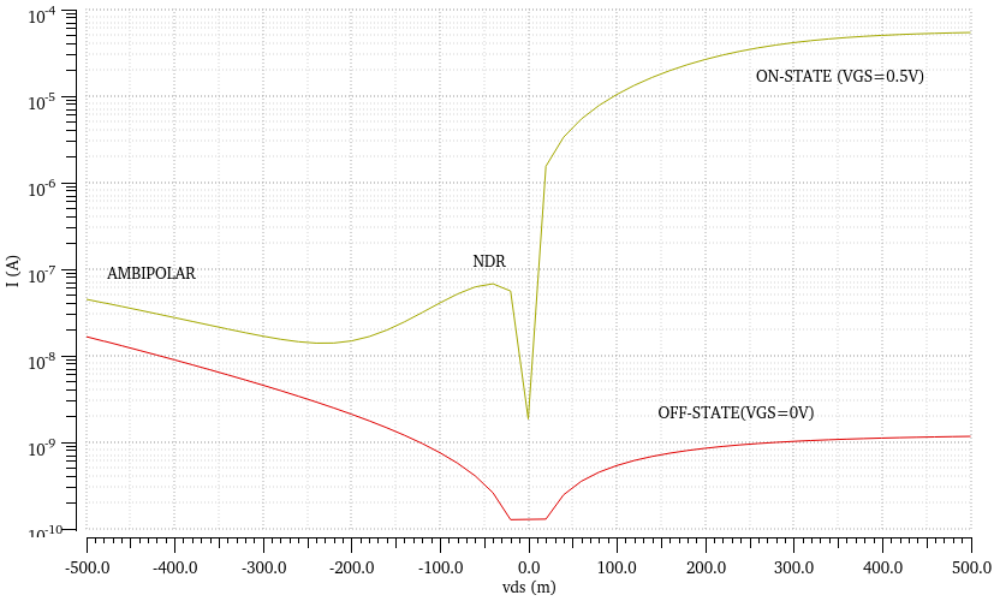

Figura 2.3: Characteristic of a GaN/InN/GaN TFET.

When the gate-bias becomes negative, with positive drain-source bias, the tunnel junction can shift from the source-channel junction to the drain-channel junction. The drain current is therefore modeled by summing three currents[25] :

$$I_{ds} = I_{dst} + I_{dsa} + I_{dse} \tag{2.23}$$

where:

- I_{dst} is the drain-source tunneling current (Q1);
- I_{dsa} is the drain-source ambipolar current (Q2);
- I_{dse} Esaki drain-source tunneling current and diode current (Q3 and Q4);

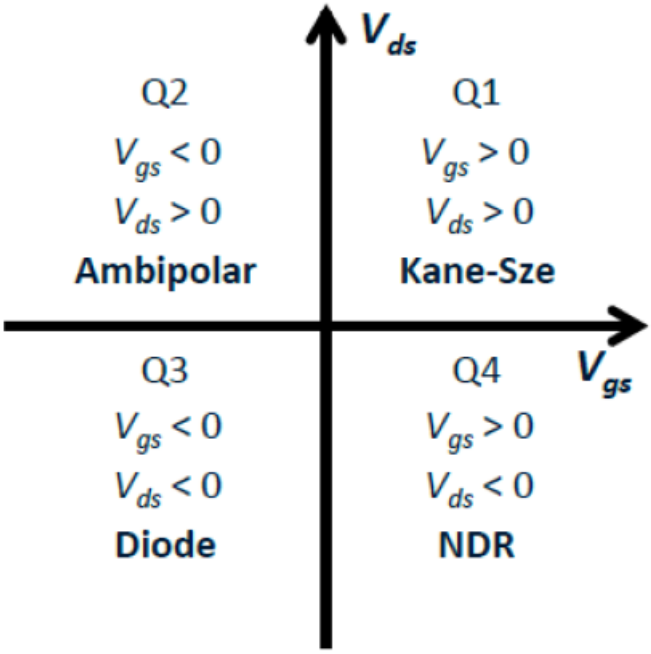

Figura 2.4: The definition of quadrants.

The Kane-Sze tunneling current, I_{dst}, is only nonzero in Q1. The ambipolar current I_{dsa} is nonzero only in Q2. The Esaki current I_{dse} is the sum of the Esaki tunneling current and the diode current, with the Esaki tunneling current being nonzero only in Q4 and the diode current being non-zero in both Q3 and Q4 [25] .

2.2.2 Equivalent Circuit

The equivalent circuit of the previous Hao Lu model included only a voltage controlled current source I_{ds} to model the drain current, capacitors C_{gs} and C_{gd}, and source and drain series resistors R_S and R_D. The revisited model equivalent circuit, Fig.2.5 , includes also the gate resistance and a voltage controlled current source I_{gd} in order to model the gate leakages. They have been added also the fringe capacitances.

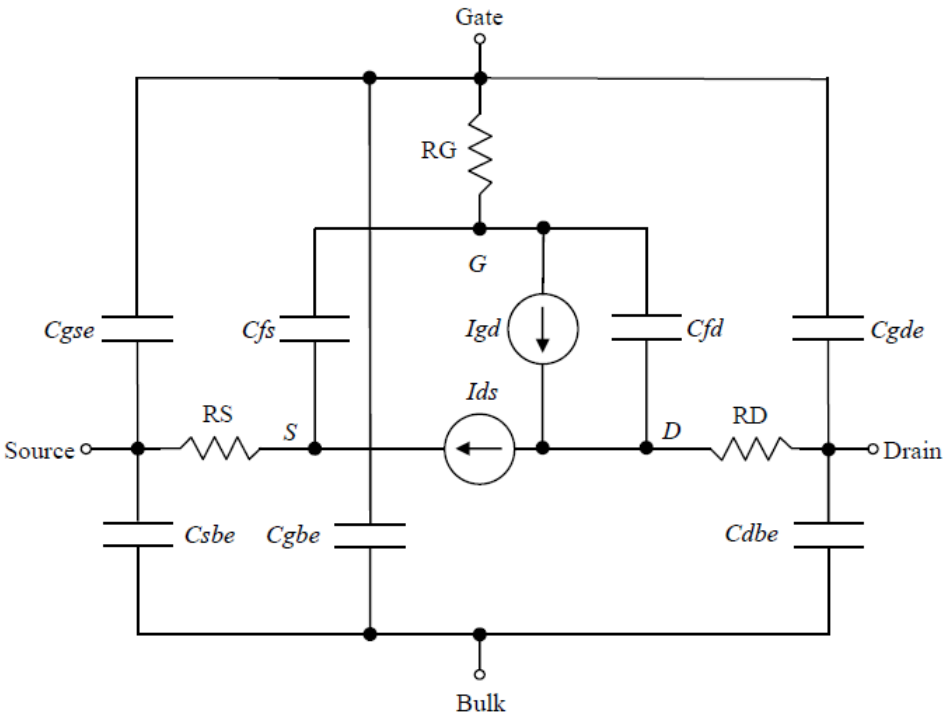

Figura 2.5: Equivalent TFETs circuit.

2.2.3 Drain-source tunneling current

The expression in the TFETs model is the same experimentally well-established equation for band-to-band, Zener tunneling in planar p-n junctions, already found in the Praveen model. The two-terminals Zener tunneling behavior is then generalized to three terminals by introducing physics-based expressions for the bias dependent tunneling window V_{tw} and a dimensionless factor f, which accounts for the superlinear current onset in the output characteristicas follows [21] [25] :

$$I_{dt} = afEV_{tw}e^{-b/E} \tag{2.24}$$

where the parameters a and b are defined as:

$$a = \frac{WT_{ch}q^3}{8\pi^2\hbar^2}\sqrt{\frac{m_r^*}{E_g}} \tag{2.25}$$

$$b = \frac{4\sqrt{2m_r^* E_g^3}}{3q\hbar} \tag{2.26}$$

the f factor is given by:

$$f = \frac{1 - e^{-\frac{V_{dse}}{\Gamma}}}{1 + e^{\frac{V_{thds} - V_{dse}}{\Gamma}}} \tag{2.27}$$

Γ is defined as *saturation shape parameter*, V_{dse} is dependent on the drain-to-source voltage:

$$V_{dse} = V_{dsmin}\left[\frac{V_{ds}}{2V_{dsmin}} + \sqrt{\Delta^2 + \left(\frac{V_{ds}}{2V_{dsmin}}\right)^2} - \sqrt{\Delta^2 + 1}\right] \tag{2.28}$$

$$V_{thds} = \Lambda tanh(V_{gs}) \tag{2.29}$$

The tunneling window, V_{tw} is defined as:

$$V_{tw} = ln\left(1 + e^{\frac{V_{gs} - V_{th}}{U}}\right) \tag{2.30}$$

And U is called *Urbach Factor* [25] .

2.2.4 Gate leakage current

One of the key feature of this model is the modeling of the gate leakage current, showing that in TFETs the gate current is mainly collected at the drain [24].

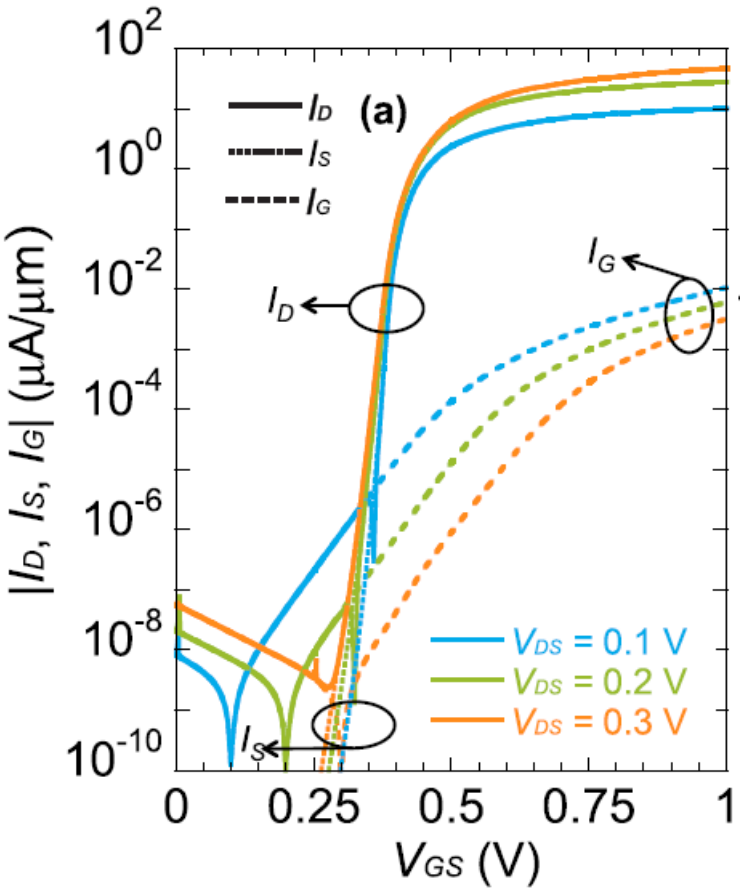

Figura 2.6: TCAD-simulated transfer characteristics of a GaN/InN/GaN TFET with currents of all three terminals [24] .

The Fig.2.6 shows the TCAD simulations of the transcharacteristic of a GaN/InN TFET for all the three terminals. Under these bias conditions more than 99% of the gate tunneling current is collected at the drain [24] .

2.2.5 Charge-based capacitance model

The first version of the Hao Lu model [21] was enhanced with a charge-based capacitance model. In order to model the charge on the three terminals they have been chosen three parametrized logarithmic espressions such as to match the form of the TCAD-simulated terminals charge. The channel charge is not directly obtained from measurements on transistors but is obtained by fitting the data produced by TCAD, or other simulation tools, with a fitting routines implemented in MATLAB [24]. Once obtained the parameters needed to complete the charge espressions, the capacitance model can be obtained

by:

$$C_{ij} = -\frac{\partial Q_i}{\partial V_j} i \neq j, i, j = G, D, S \tag{2.31}$$

$$C_{ii} = \frac{\partial Q_i}{\partial V_i} \tag{2.32}$$

The most significant capacitances for the transitors, TFETs and standard MOSFETs, are C_{DG} and C_{SG} that are computed as:

$$C_{DG} = -\frac{\partial Q_D}{\partial V_G} \tag{2.33}$$

$$C_{DG} = -\frac{\partial Q_S}{\partial V_G} \tag{2.34}$$

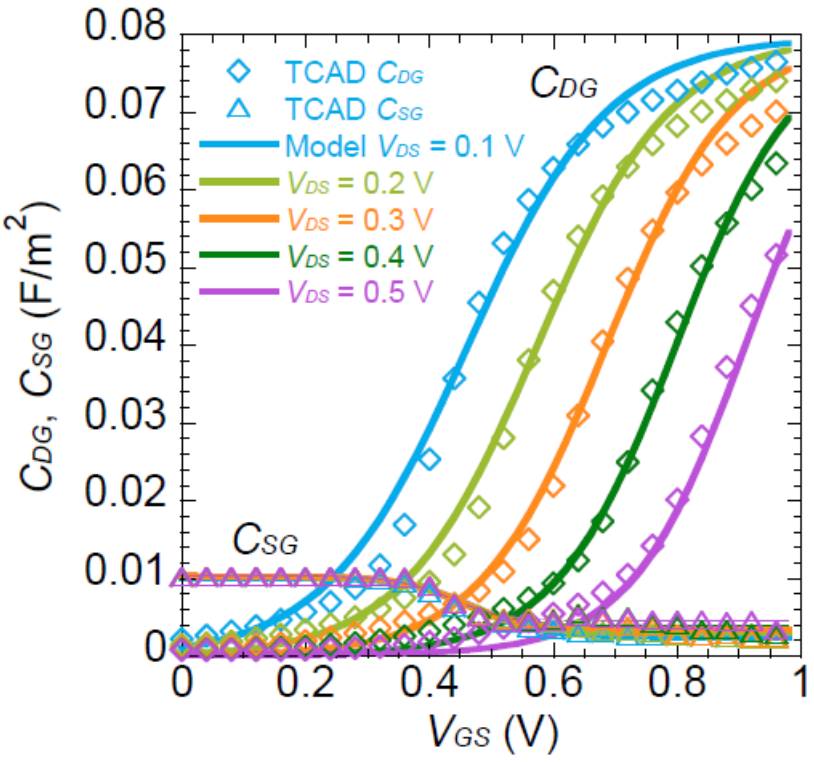

Figura 2.7: TCAD-simulated(symbols)and modeled(solid) C_{DG} and C_{SG} [24] [25] .

Due to the asymmetric drain/source channel charge partition, C_{DG} is significantly larger than C_{SG} at large V_{GS} and saturates with increasing V_{GS}. At low V_{GS}, C_{SG} is

dominant over C_{DG} and controlled by the tunnel junction capacitance [24] .

2.2.6 TFETs Noise Model

Since the TFETs are transistors thought to be used in low power applications, with voltages under the 500mV, the effects of the noise cannot be neglected [24] .

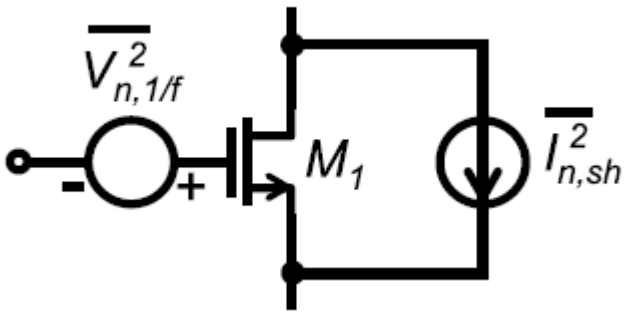

Figura 2.8: Tunnel FET noise model consisting of flicker 1/f noise in the gate and shot noise source at the source/channel junction [24] .

From Fig.2.8 it can be seen that the electrical noise is modeled inside the Hao Lu model as:

- a shot noise caused by trapping/detrapping at the source/channel junction, which changes the internal tunnel-junction field and the tunnel current:

$$\overline{I^2_{n,1/f}} = 2qI_D[A^2/Hz] \tag{2.35}$$

- a frequency dependent flickr noise at the gate:

$$\overline{V^2_{n,1/f}} = \frac{K}{f^n}[V^2/Hz] \tag{2.36}$$

  where K is a constant and n is a factor to account for the frequency dependence (n=1 for 1/f noise, and n=2 for RTN noise, both of which can be extracted from measurements or simulation data [24] .

2.2.7 Temperature Effect

The temperature appears explicitly in several exponential terms in the model [25] .

CHAPTER 3

Simulated Devices

The different devices used to evaluate the performances of the TFET technology are shown in this chapter. Moreover, this part of the thesis contains the characterizations done in order to evaluate important device parameters such as SS, I_{ON}, I_{OFF}, voltage threshold, V_{th}, drain-induced barrier lowering(DIBL) and $I_{ON}/I_{OFF}ratio$.
The simulations have been carried out on the Virtuoso environment using Spectre as simulator.

3.1 Homojunction InAs DG-TFET

The InAs double-gate (DG) TFET is the only homojunction TFET taken into account in this work. The model developed with the previous analytical Hao Lu model [25] has been widely used by to explore the TFETs capabilities inside SRAMs [23], but in this work are used model cards developed with last review of the model.

3.1.1 Structure

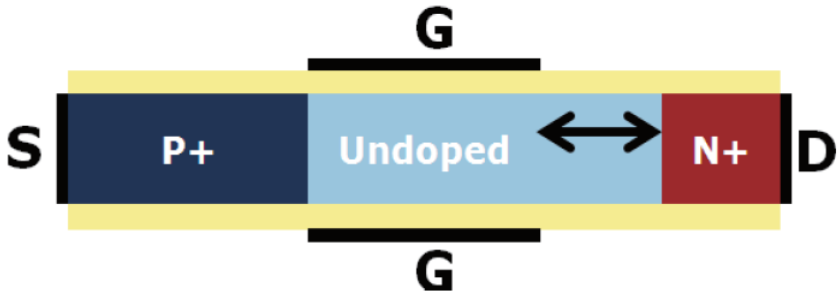

Figura 3.1: InAs TFET structure [26] .

The indium arsenide is a semiconductor composed of indium and arsenic. It is a III-V binary compound characterized by a narrow direct bandgap(0.354 eV) [27] and this permits to increase the tunneling probability T_{WKB} and to increase the on-state current, decreasing the E_g parameter in 3.1 .

$$T_{WKB} \approx exp(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g + \Delta\Phi)}) \tag{3.1}$$

The structure in 3.1 is characterized by:

- $L_G = 20nm$;
- $EOT = 1nm$;
- $t_{body} = 5nm$;
- $N^+ = 10^{17}cm^{-3}$;
- $P^+ = 10^{19}cm^{-3}$;

One key device design obstacle for the TFET is to minimize ambipolar current that occurs due to the narrow bandgap material. Here, it is been increased the drain-underlap design to lower ambipolar current, achieving a low I_{OFF} with a subthreshold swing lower than 60mV/dec [26].

3.1.2 Characteristics

The TFET has been characterized in Virtuoso using a DC power supply between gate and source (with parametric value vgs) and another DC power supply between drain and

source (with parametric value *vds*).

The *trancharacteristic* has been obtained by sweepping *vgs* from 0 to 500mV keeping *vds* constant to 500mV. The results obtained have been validated with the data on the reference paper, and the Hao Lu model itself has been validated comparing the data obtained by Spectre with those obtained with TCAD simulations(available online [28]).

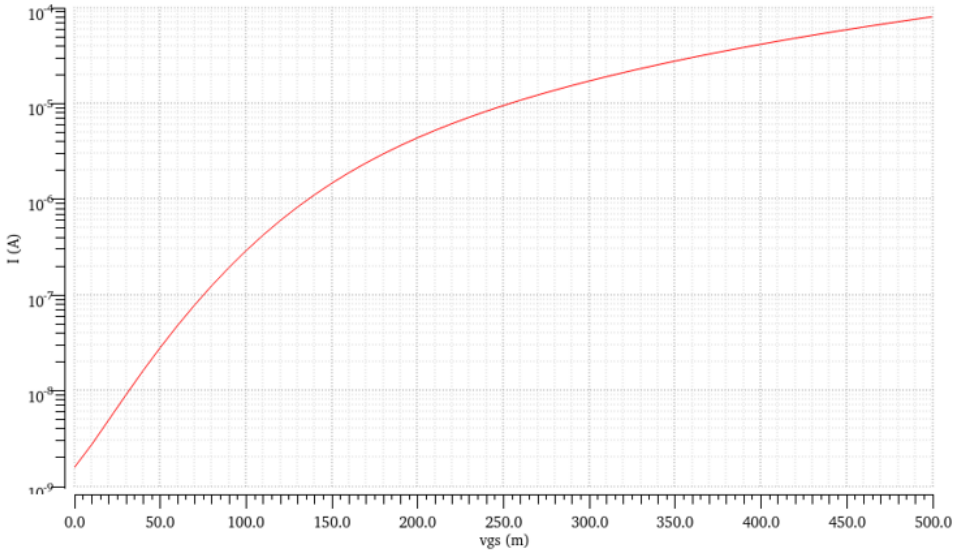

Figura 3.2: InAs DG-TFET transcharacteristic for $V_{DD} = 0.5V$.

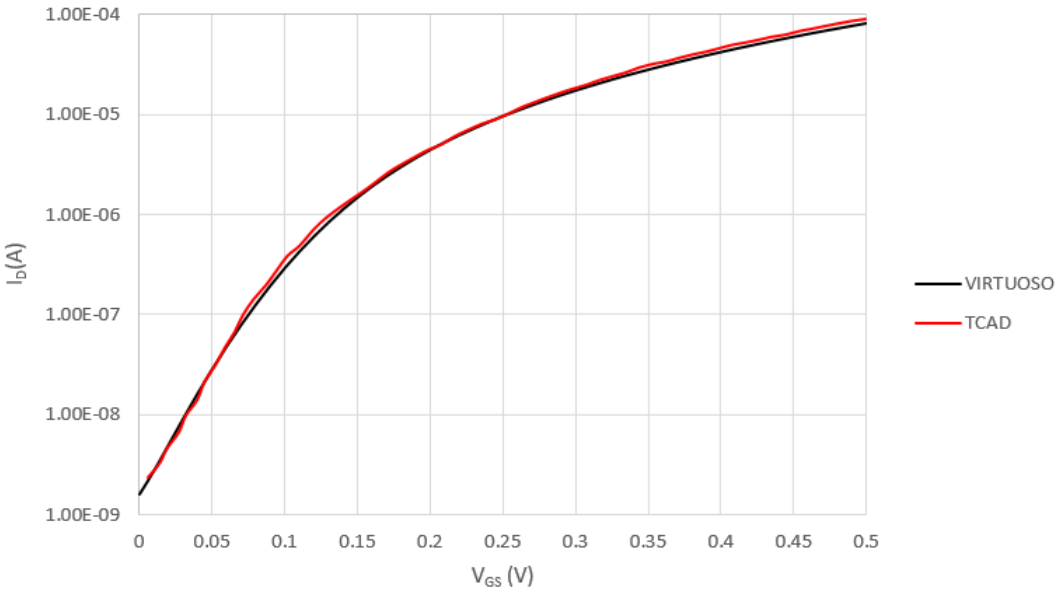

Figura 3.3: Comparison between Virtuoso results and TCAD results

For $V_{DD} = 500mV$ they have been found an on-current ($I_{DD}(vgs = vds = 500mV)$)

of $80.29\mu A/\mu m$ and an off-current ($I_D(vgs = 0V, vds = 500mV)$) of $1.6nA/\mu m$, and consequently an I_{on}/I_{off} ratio of $5.02 * 10^4$.

The *trancharacteristic* has been obtained with a parametric simulation by sweepping vds from 0 to 500mV and using vgs as parameter.

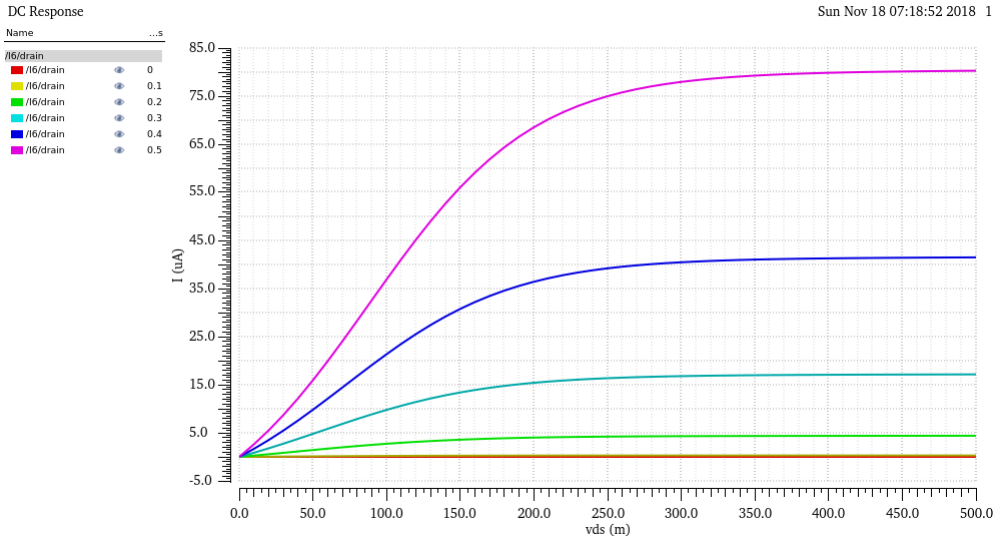

Figura 3.4: InAs DG-TFET characteristic.

The fact that the drain-current in TFETs is due to the Band-To-Band-Tunneling, instead of thermionic emission, lead to another peculiarity for these devices. In fact, the BTBT phenomenon is pratically independent from the carriers mobility [4], so there is no more need to change the channel width in order to have a specular characteristic between n-type and p-type transistors.

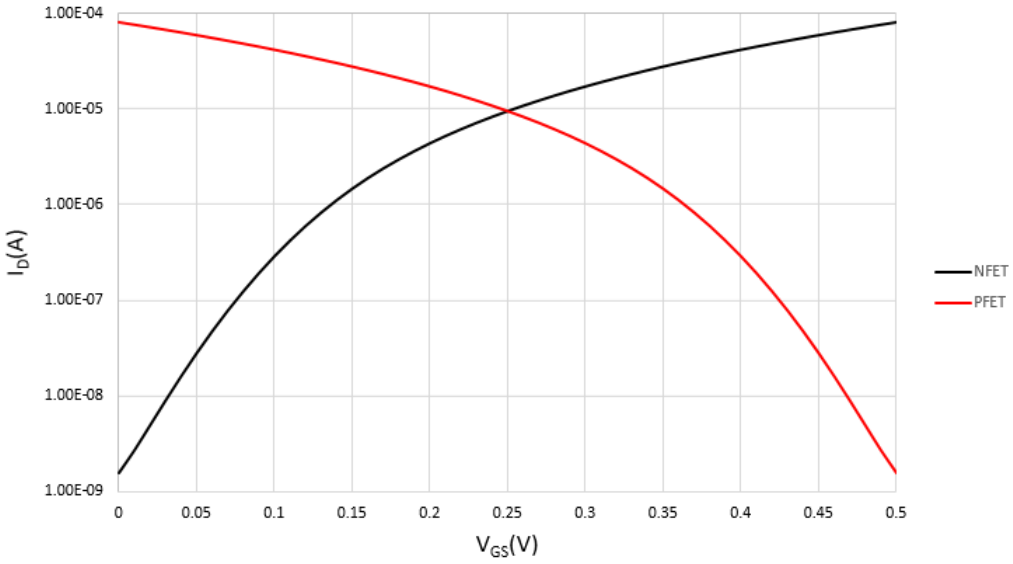

Figura 3.5: InAs DG-TFET n-type and p-type transcharacteristic comparison.

3.1.3 Voltage Threshold and Subthreshold Swing

The Subthreshold Swing is defined as the average slope of logarithmic transcharacteristic from $vgs = 0$ to $vgs = V_{TH}$ [5] :

$$SS = \frac{V_{TH}}{log\frac{I_{D(vgs=V_{TH})}}{I_{OFF}}} \tag{3.2}$$

The voltage threshold must be evaluated in order to calculate the subthreshold slope. The voltage threshold is not a well-defined parameter because it is difficult to estabilish when the device turns on. Among the various methods developed in the years to give a numerical value to the threshold, the study of the second derivative of the transcharacteristic 3.6(that is the first derivative of the transconductance) has been considered the most reliable [29] [30] . V_{TH} is defined as the vgs value for the which there is the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

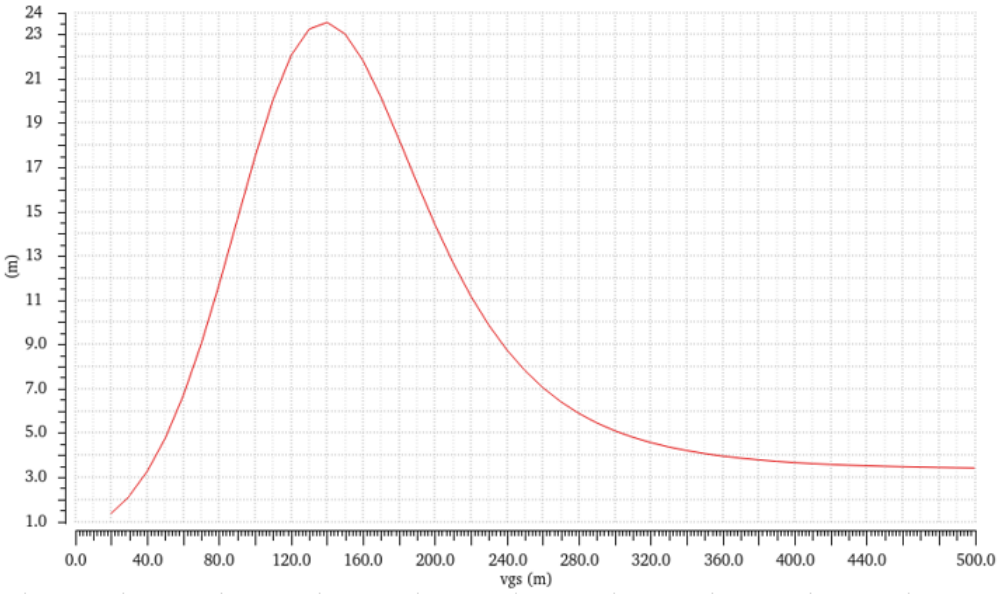

Figura 3.6: InAs DG-TFET plot of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

The curve has been plotted thanks to the function *deriv* of the Virtuoso Calculator. For the InAs DG-TFET it has been estimated a voltage threshold of 140mV, and using this value in the 3.2 it has been found $SS = 49mV/dec$.

3.1.4 Drain Induced Barrier Lowering

Drain-induced barrier lowering (DIBL) is a short-channel effect referring to a dependency of threshold voltage of the transistor from drain voltages. In particular the V_{TH} decreases with V_{DD} and this can lead to a prematurely turn-on of the transistor, and increases the leakage current of the device. On the other hand, the fact that V_{TH} increases with V_{DD} implies a penalty in the working frequency going up with the power supply.

$$DIBL = \frac{V_{TH}^{VDD} - V_{TH}^{VDS_{low}}}{VDD - VDS_{low}}[mV/V] \tag{3.3}$$

The DIBL has been evaluated with a parametric simulation in Virtuoso by plotting $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ for different values of *vds* (taken as parameter):

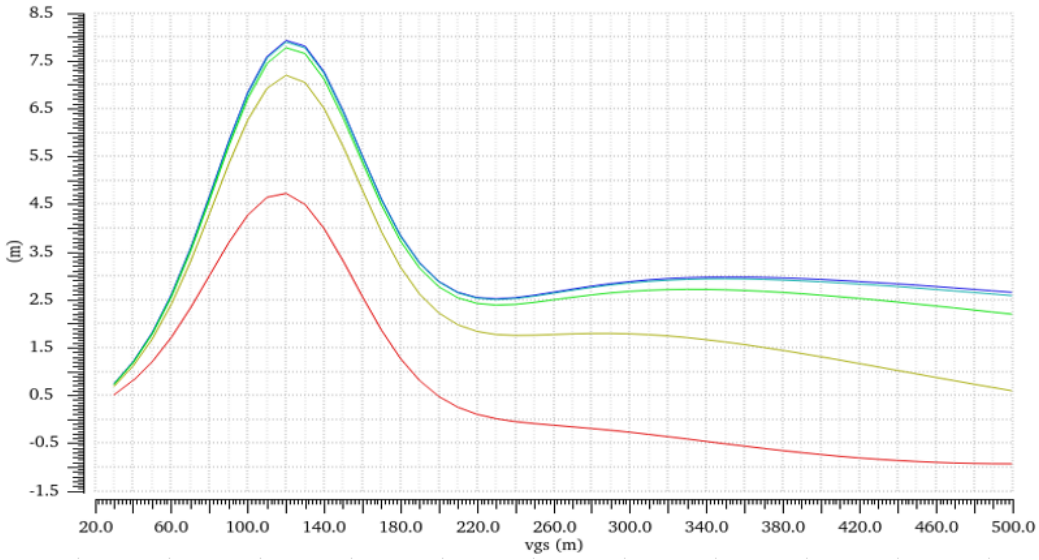

Figura 3.7: For the InAs DG-TFET the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ is independent from V_{DD}, this means a null DIBL.

For the InAs DG-TFET it has been found that DIBL= 0 mV/V. But this is due to the fact that in the Hao Lu model the DIBL phenomenon has not been implemented yet [25].

3.2 Heterojunction AlGaSb/InAs TFET

The AlGaSb/InAs TFET is an heterojunction device composed by a III-V ternary compound(AlGaSb) for the source and a III-V binary compound(InAs) for drain and channel.

3.2.1 Structure

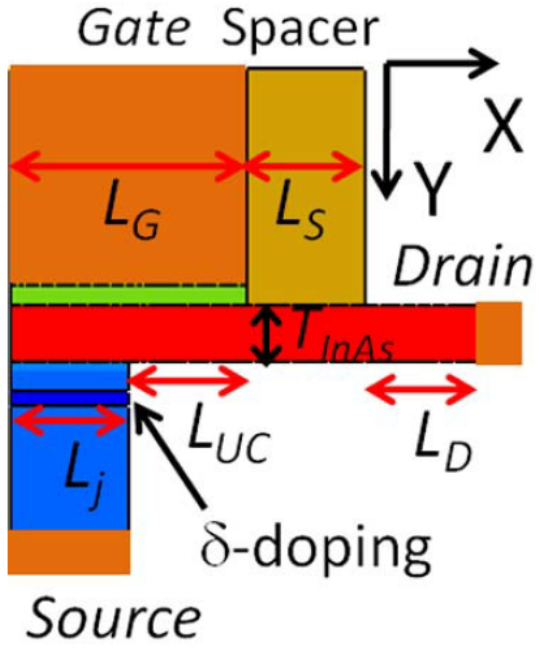

Figura 3.8: AlGaSb/InAs TFET structure [15] .

The structure in 3.8 is characterized by:

- $L_G = 20nm$;
- $EOT = 0.6nm$;
- $L_{UC} = 10nm$;
- $L_S = 10nm$;
- $L_j = 10nm$;
- $L_D = 10nm$;
- $T_{InAs} = 4nm$;

The cross section of the simulated device structure is shown in 3.8. A metal gate (work function = 4.93 eV) with a thicknesse of 1.4 nm and a gate oxide in Al_2O_3 high-k dielectric was used. A HfO_2 spacer with an underlap (L_D) between the spacer and drain contact was utilized to reduce the ambipolar conduction caused by gate–drain coupling. The InAs channel was undercut by a length L_{UC}, and thus the gate overlaps the channel as shown in 3.8. This undercut is necessary for the TFET to achieve a steeper subthreshold swing. The heterostructure, starting from the substrate, consists of a p-type AlGaSb source injector with thickness 40 nm and doping $4 * 10^{18} cm^{-3}$ and a n-type InAs channel with thickness 4 nm and doping $5 * 10^{17} cm^{-3}$. A p-type $\delta - dopingplane$ plane with a sheet concentration of $6 * 10^{12} cm^{-2}$ was inserted in the source 2 nm away from the tunnel junction. This $\delta - doping$ was implemented by doping a 1-nm-thick layer at $6 * 10^{19} cm^{-3}$, with a 2-nm/dec exponential decay profile on both sides [15] . The indium arsenide is a semiconductor composed of indium and arsenic. It is a III-V binary compound characterized by a narrow direct bandgap(0.354 eV). The AlGaSb is a III-V ternary compound and is an important material employed in high-speed electronic and infrared optoelectronic devices [27]. The energy gap between the InAs conduction and AlGaSb valence bands [15] jointly to the narrow bandgap of the InAs, permits to increase the tunneling probability T_{WKB} and to boost the on-state current, decreasing the E_g parameter and increasing $\Delta\Phi$ in 3.4

$$T_{WKB} \approx exp(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g + \Delta\Phi)}) \tag{3.4}$$

This device presents a much more complex geometry and choice of materials, leading to an on-current that is about three times bigger than the conduction current of the previous InAs homojunction device.

3.2.2 Characteristics

The TFET has been characterized in Virtuoso using a DC power supply between gate and source (with parametric value *vgs*) and another DC power supply between drain and source (with parametric value *vds*).

The *trancharacteristic* has been obtained by sweepping *vgs* from 0 to 500mV keeping *vds* constant to 500mV. The results obtained have been validated with the data on the

reference paper, and the Hao Lu model itself has been validated comparing the data obtained by Spectre with those obtained with TCAD simulations (available online [28]).

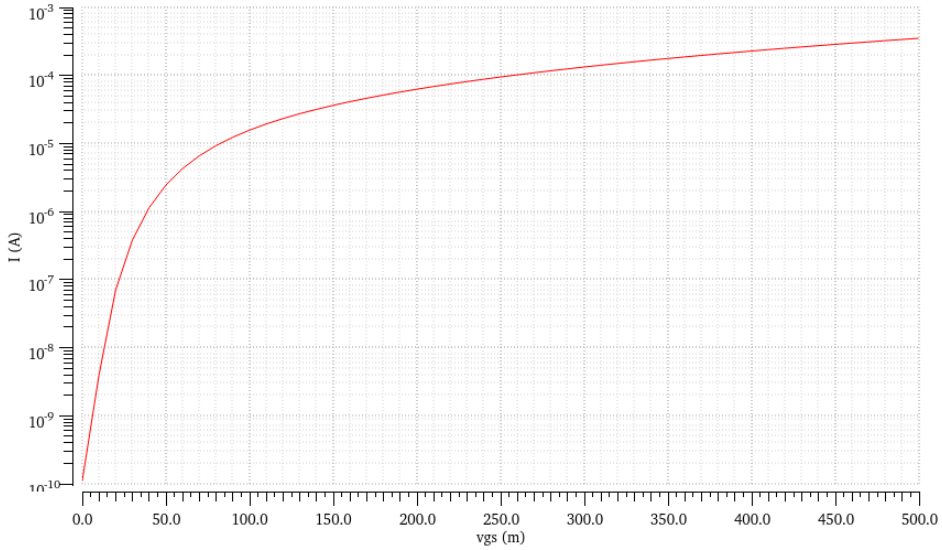

Figura 3.9: AlGaSb/InAs TFET transcharacteristic for $V_{DD} = 0.5V$.

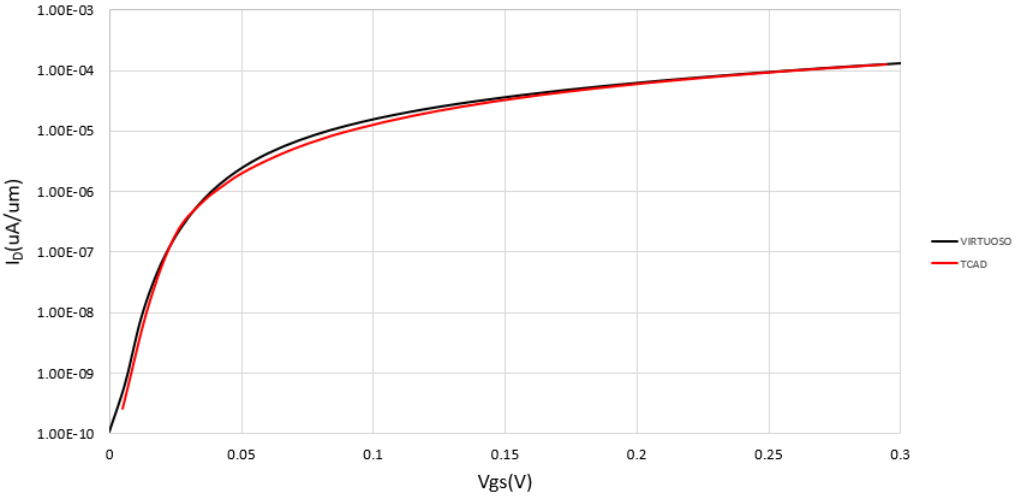

Figura 3.10: Comparison between Virtuoso results and TCAD data for $V_{DD} = 0.3V$.

For $V_{DD} = 500mV$ they have been found an on-current ($I_D(vgs = vds = 500mV)$) of $351\mu A/\mu m$ and an off-current ($I_{drain}(vgs = 0V, vds = 500mV)$) of $111pA/\mu m$, and consequently an I_{on}/I_{off} ratio of $3.16 * 10^6$.

The *trancharacteristic* has been obtained with a parametric simulation by sweepping vds from 0 to 500mV and using vgs as parameter.

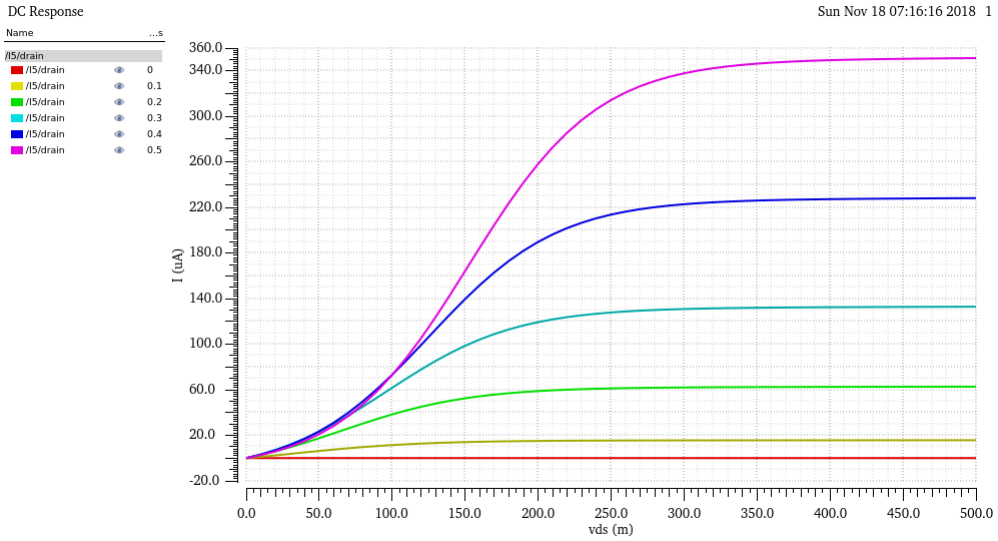

Figura 3.11: AlGaSb/InAs TFET characteristic.

The fact that the drain-current in TFETs is due to the Band-To-Band-Tunneling instead of thermionic emission lead to another peculiarity for these devices. In fact, the BTBT phenomenon is pratically independent from the carriers mobility [4] , so there is no more need to change the channel width in order to have a specular characteristic between n-type and p-type transistors.

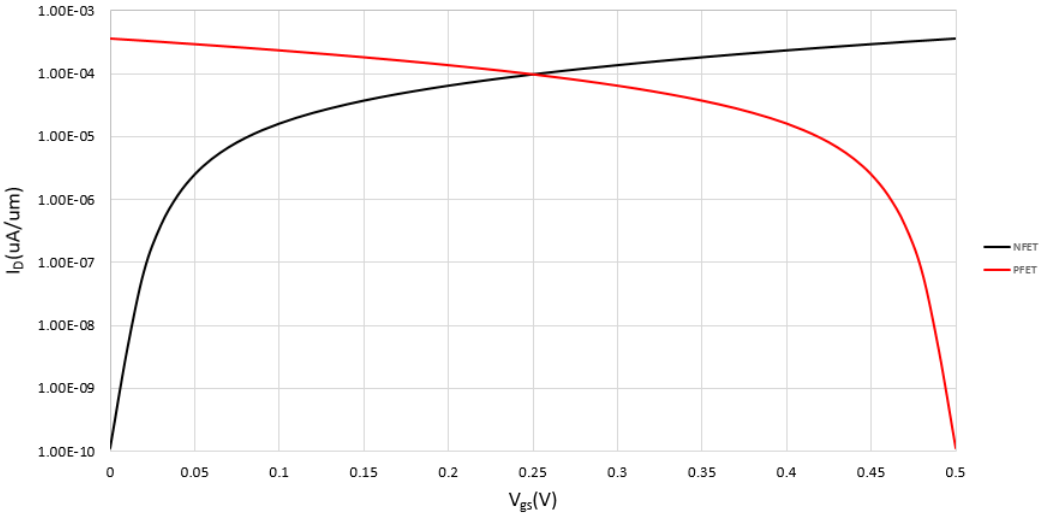

Figura 3.12: AlGaSb/InAs TFET n-type and p-type transcharacteristic comparison.

3.2.3 Voltage Threshold and Subthreshold Swing

The Subthreshold Swing is defined as the average slope of logarithmic transcharacteristic from $vgs = 0$ to $vgs = V_{TH}$ [5] :

$$SS = \frac{V_{TH}}{log\frac{I(vgs=V_{TH})}{I_{OFF}}} \tag{3.5}$$

The voltage threshold must be calculated before being able to evaluate the subthreshold slope. The voltage threshold is not a well-defined parameter because it is difficult to estabilish when the device turns on. Among the various methods developed in the years to give a numerical value to the threshold, the study of the second derivative of the transcharacteristic 3.13(that is the first derivative of the transconductance) has been considered the most reliable [29] [30] . V_{TH} is defined as the vgs value for the which there is the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

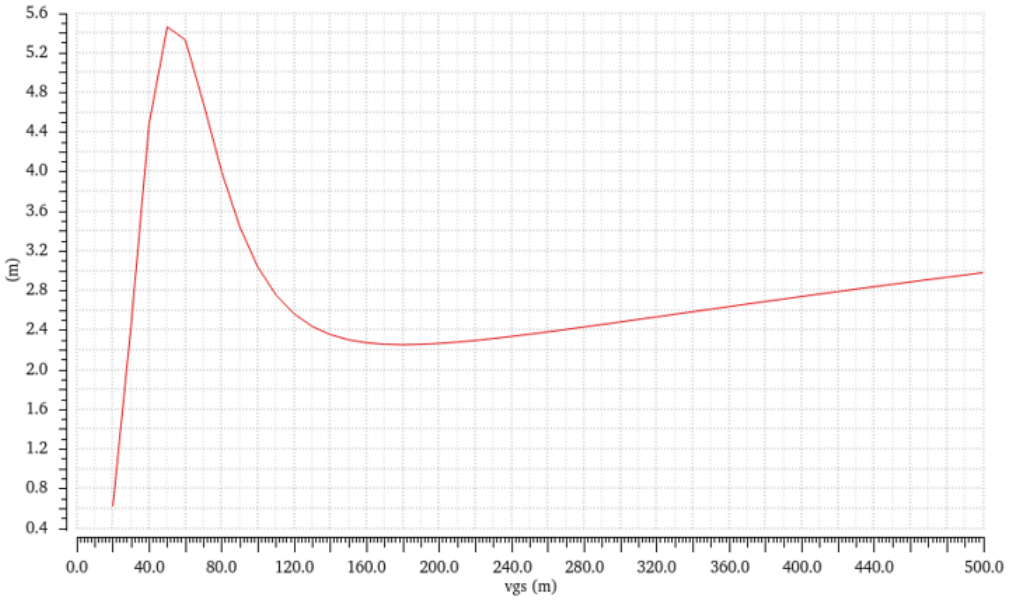

Figura 3.13: AlGaSb TFET plot of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

The curve has been plotted thanks to the function *deriv* of the Virtuoso Calculator. For the AlGaSb/InAs TFET it has been estimated a voltage threshold of 50mV, and using this value in the 3.5 it has been found $SS = 12.15mV/dec$.

3.2.4 Drain Induced Barrier Lowering

Drain-induced barrier lowering (DIBL) is a short-channel effect referring to a dependency of threshold voltage of the transistor from drain voltages. In particular the V_{TH} decreases with V_{DD} and this can lead to a prematurely turn-on of the transistor, and increases the leakage current of the device. On the other hand, the fact that V_{TH} increases with V_{DD} implies a penalty in the working frequency going up with the power supply.

$$DIBL = \frac{V_{TH}^{VDD} - V_{TH}^{VDS_{low}}}{VDD - VDS_{low}}[mV/V] \tag{3.6}$$

The DIBL has been evaluated with a parametric simulation in Virtuoso by plotting $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ for different values of *vds* (taken as parameter).

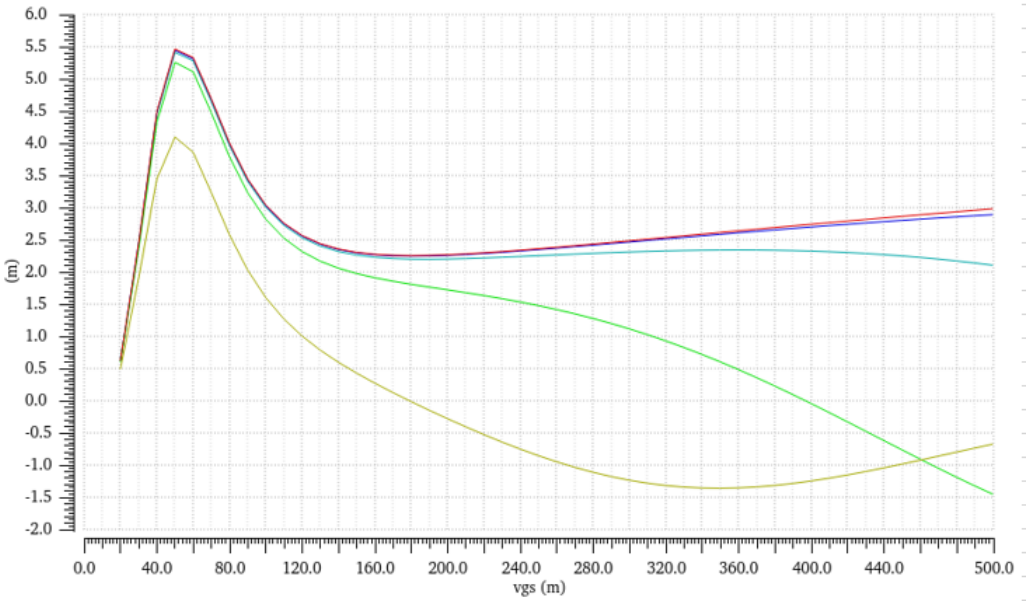

Figura 3.14: For the AlGaSb/InAs TFET the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ is independent from V_{DD}, this means a null DIBL.

For the AlGaSb/InAs TFET it has been found that DIBL= 0 mV/V. But this is due to the fact that in the Hao Lu model the DIBL phenomenon has not been implemented yet [25].

3.3 Heterojunction GaN/InN/GaN DG-TFET

The GaN/InN/GaN TFET is an heterojunction composed by a III-V binary compound(GaN) for the drain and source and a III-V binary compound(InN) the channel .

3.3.1 Structure

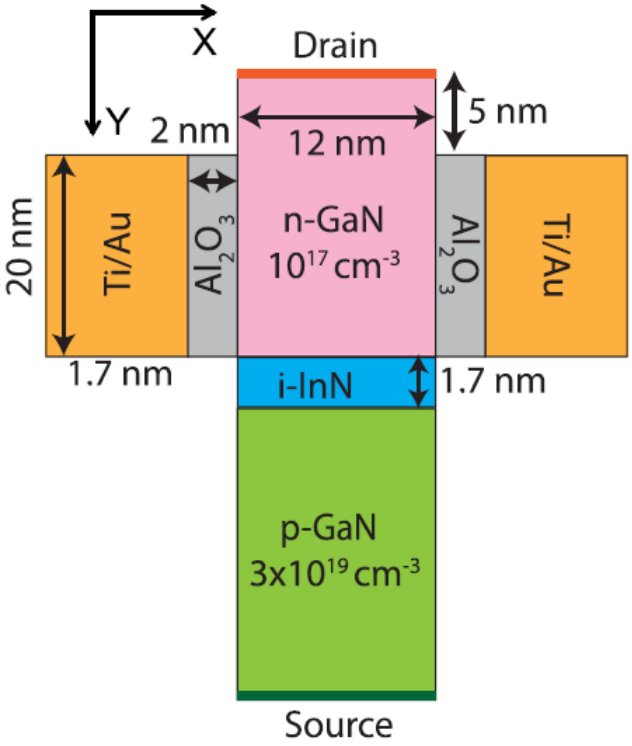

Figura 3.15: GaN/InN/GaN DG-TFET structure [24] .

The structure in 3.15 is characterized by:

- $L_G = 20nm$;
- $EOT = 2nm$;
- $T_{body} = 12nm$;
- $L_S = 25nm$;
- $T_{InN} = 1.7nm$;
- $L_D = 25nm$;

- $T_{gate} = 1.7nm$;
- $N^+ = 10^{17} cm^{-3}$;
- $P^+ = 3 * 10^{19} cm^{-3}$;

The 3.2-eV bandgap of GaN provides a low off-current, I_{OFF}, while effectively eliminating ambipolar current. The use of InN, with a bandgap of 0.7 eV and strong polarization discontinuity with respect to GaN, results in a 20 MV/cm built-in electric field within the p-GaN/i-InN/n-GaN heterojunction and a tunneling distance of approximately 1 nm [24] [31] [17] . The gallium nitride is a III-V binary compound, it has a wide band gap of 3.2 eV that affords it special properties for applications in optoelectronic high-power and high-frequency devices. The InN is a III-V binary compound rarely used in is binary form. It forms an alloy with GaN that is at the core of the blue diode laser [27]. The energy gap between the InN conduction and GaN valence bands jointly to the narrow bandgap of the InN [24], permits to increase the tunneling probability T_{WKB} and to boost the on-state current, decreasing the E_g parameter and increasing $\Delta\Phi$ in 3.7:

$$T_{WKB} \approx exp(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g + \Delta\Phi)}) \tag{3.7}$$

3.3.2 Characteristics

The TFET has been characterized in Virtuoso using a DC power supply between gate and source (with parametric value *vgs*) and another DC power supply between drain and source (with parametric value *vds*).

The *trancharacteristic* has been obtained by sweepping *vgs* from 0 to 500mV keeping *vds* constant to 500mV. The results obtained, have been validated with the data on the reference paper obtained from TCAD simulations [24].

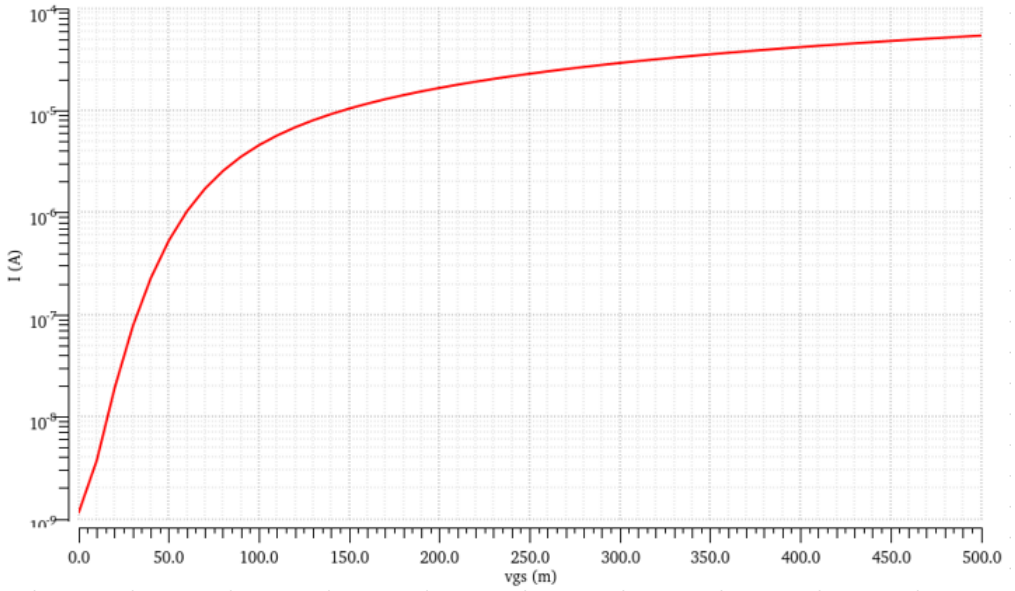

Figura 3.16: GaN/InN/GaN DG-TFET transcharacteristic for $V_{DD} = 0.5V$.

For $V_{DD} = 500mV$ they have been found an on-current, $(I_D(vgs = vds = 500mV))$, of $54.4\mu A/\mu m$ and an off-current, $(I_D(vgs = 0V, vds = 500mV))$, of $1.17nA/\mu m$, and consequently an I_{on}/I_{off} ratio of $4.65 * 10^6$.

The *trancharacteristic* has been obtained with a parametric simulation by sweepping *vds* from 0 to 500mV and using *vgs* as parameter.

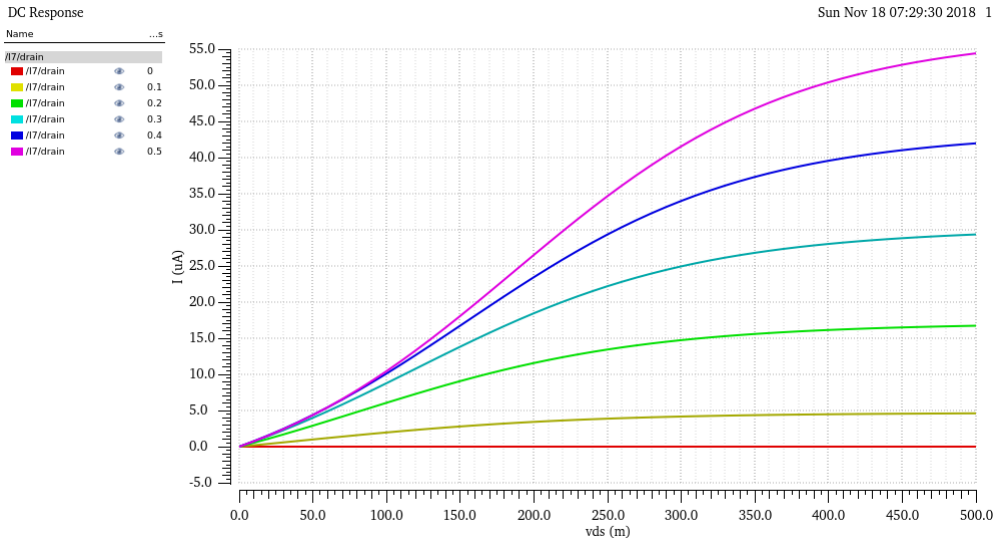

Figura 3.17: GaN/InN/GaN DG-TFET characteristic.

The fact that the drain-current in TFETs is due to the Band-To-Band-Tunneling

instead of thermionic emission lead to another peculiarity for these devices. In fact, the BTBT phenomenon is pratically independent from the carriers mobility, so there is no more need to change the channel width in order to have a specular characteristic between n-type and p-type transistors.

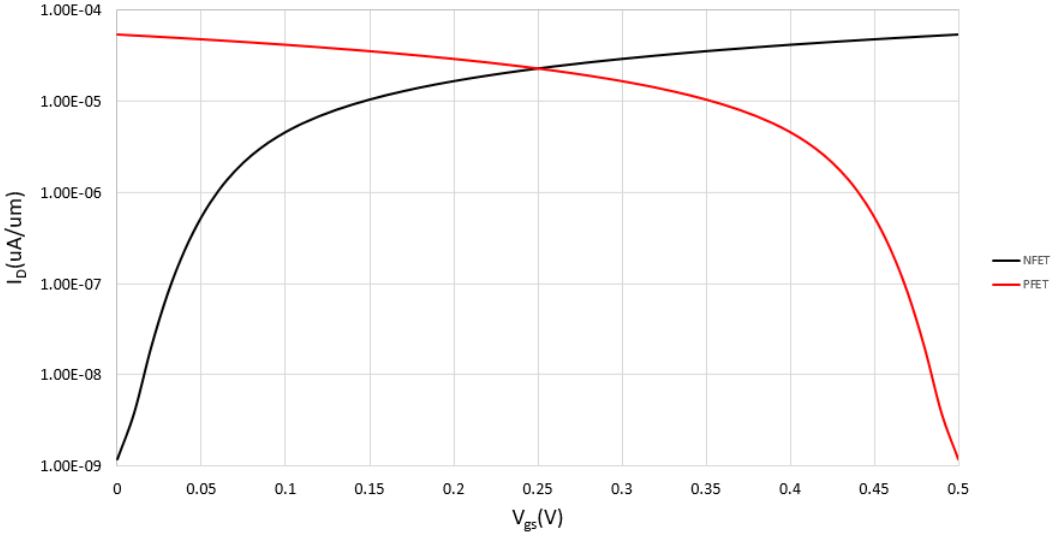

Figura 3.18: GaN/InN DG-TFET n-type and p-type comparison.

3.3.3 Voltage Threshold and Subthreshold Swing

The Subthreshold Swing is defined as the average slope of logarithmic transcharacteristic from $vgs = 0$ to $vgs = V_{TH}$ [5] :

$$SS = \frac{V_{TH}}{log\frac{I(vgs=V_{TH})}{I_{OFF}}} \tag{3.8}$$

So must be evaluated the voltage threshold before being able to evaluate the subthreshold slope. The voltage threshold is not a well-defined parameter because it is difficult to estabilish when the device turns on. Among the various methods developed in the last years to give a numerical value to the threshold it has been chosen the study of the second derivative of the transcharacteristic 3.19(that is the first derivative of the transconductance) [29] [30] . V_{TH} is defined as the vgs value for the which there is the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

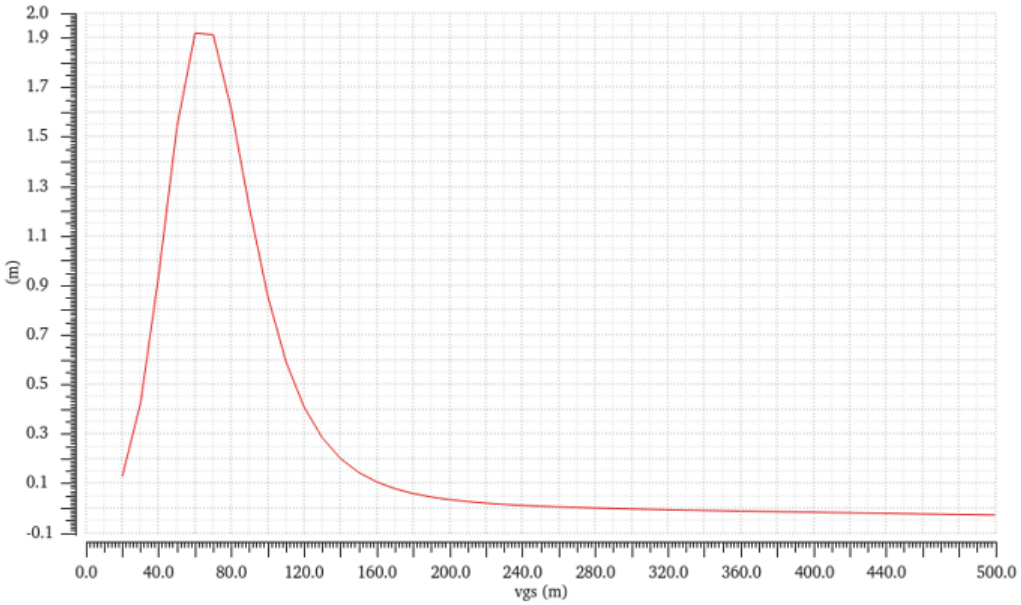

Figura 3.19: GaN/InN/GaN DG-TFET plot of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

The curve has been plotted thanks to the function *deriv* of the Virtuoso Calculator. For the GaN/InN TFET it has been estimated a voltage threshold of 60mV, and using this value in the 3.8 it has been found $SS = 20.35 mV/dec$.

3.3.4 Drain Induced Barrier Lowering

Drain-induced barrier lowering (DIBL) is a short-channel effect referring to a dependency of threshold voltage of the transistor from drain voltages. In particular the V_{TH} decreases with V_{DD} and this can lead to a prematurely turn-on of the transistor, and increases the leakage current. On the other hand, the fact that V_{TH} increases with V_{DD} implies a penalty in the working frequency going up with the power supply.

$$DIBL = \frac{V_{TH}^{VDD} - V_{TH}^{VDS_{low}}}{VDD - VDS_{low}} [mV/V] \tag{3.9}$$

The DIBL has been evaluated with a parametric simulation in Virtuoso by plotting $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ for different values of *vds* (taken as parameter).

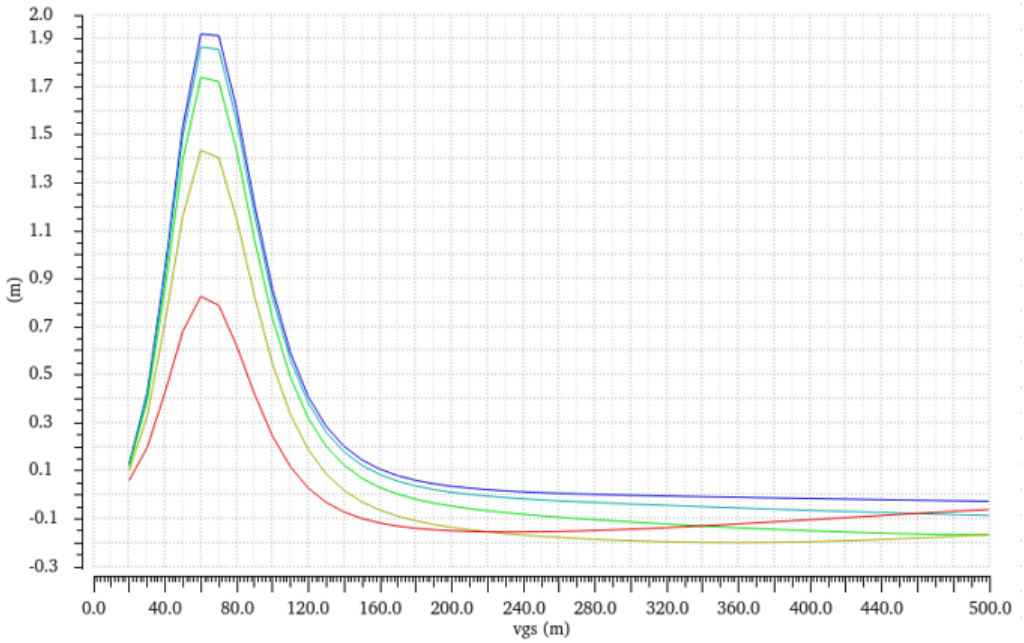

Figura 3.20: For the GaN/InN DG-TFET the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ is independent from V_{DD}, this means a null DIBL.

For the GaN/InN/GaN DG-TFET it has been found that DIBL= 0 mV/V. But this is due to the fact that in the Hao Lu model the DIBL phenomenon has not been implemented yet [25].

3.4 Heterojunction GaSb/InAs DG-TFET

The GaSb/InAs TFET is an heterojunction composed by a III-V binary compound(GaSb) for the source and a III-V binary compound(InAs)for the channel and drain.

3.4.1 Structure

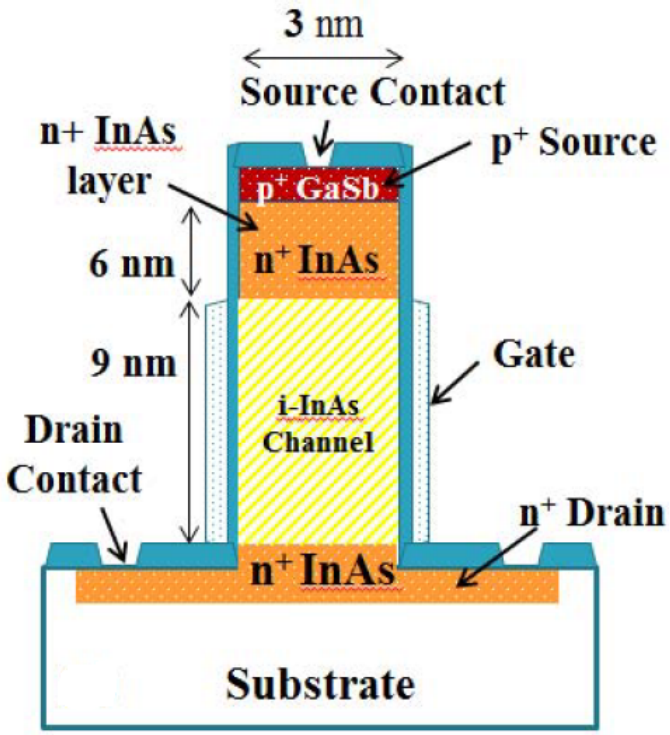

Figura 3.21: GaSb/InAs DG-TFET structure [16] .

The structure in 3.15 is characterized by:

- $L_G = 9nm$;
- $H_{FIN} = 12nm$;
- $EOT = 1.9nm$;
- $T_{body} = 3nm$;
- $L_{UL} = 6nm$;
- $L_D = 30nm$;

- $L_D = 30nm$;
- $N^+_{UNDERLAP} = 10^{18}cm^{-3}$;
- $N^+ = 10^{18}cm^{-3}$;
- $P^+ = 4 * 10^{18}cm^{-3}$;

The GaSb/InAs Het-j TFET is one of the leading TFET options because of the broken-gap band-alignment which results in high drive current. The proposed structure a GaSb/InAs DG n-TFET with an n+-doped underlap layer of InAs towards the source and a gate lengths of 9 nm. The gate is realized in HfO_2 and has a gate-substrate worfunction difference, $\delta\phi_g$, of -0.5eV. The presence of the underlap region is necessary to improve the current-voltage characteristics of the TFET, in particular it is needed to decrease the SS [32] [16].

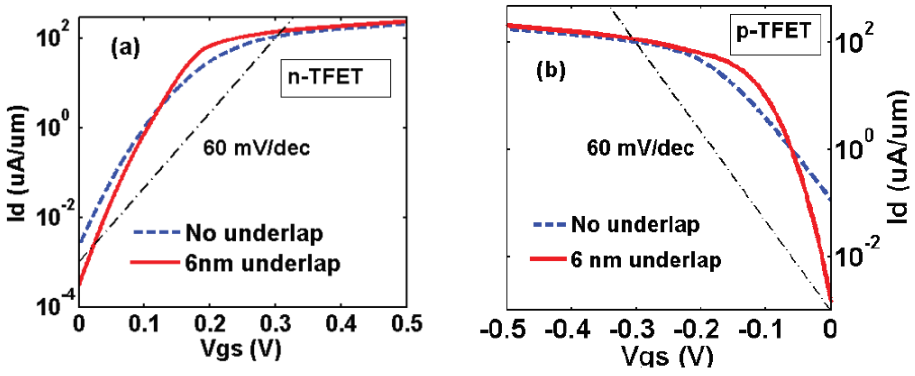

Figura 3.22: GaSb/InAs DG-TFET comparison between an underlapped structure and a non-underlapped one [16] .

Gallium antimonide (GaSb) is a semiconducting binary compound of gallium and antimony of the III-V family, it has a band gap of $\sim 0.8eV$ affords it special properties for mid-infrared applications in optoelectronic devices. The energy gap between the InAs conduction and GaSb valence bands jointly to the narrow bandgap of the InAs [27], permits to increase the tunneling probability T_{WKB} and to boost the on-state current, decreasing the E_g parameter and increasing $\Delta\Phi$ in 3.10

$$T_{WKB} \approx exp(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g + \Delta\Phi)}) \tag{3.10}$$

3.4.2 Characteristics

The TFET has been characterized in Virtuoso using a DC power supply between gate and source (with parametric value *vgs*) and another DC power supply between drain and source (with parametric value *vds*).

The *trancharacteristic* has been obtained by sweepping *vgs* from 0 to 500mV keeping *vds* constant to 500mV. The results obtained, have been validated with the data, on the reference paper [32] [16] , obtained from NEMO5 simulations. This is the only TFET for the which it has been used a LUT based model card [33] (available online [34]). The current values(I_D, I_S, I_G) and the capacitance values(C_GD, C_GS, C_D) obtained from the atomistic simulations have been disposed inside tables to be addressed according to the V_{GS} and V_{DS} values during the circuit simulations. This is implemented by a very basic Verilog-A script.

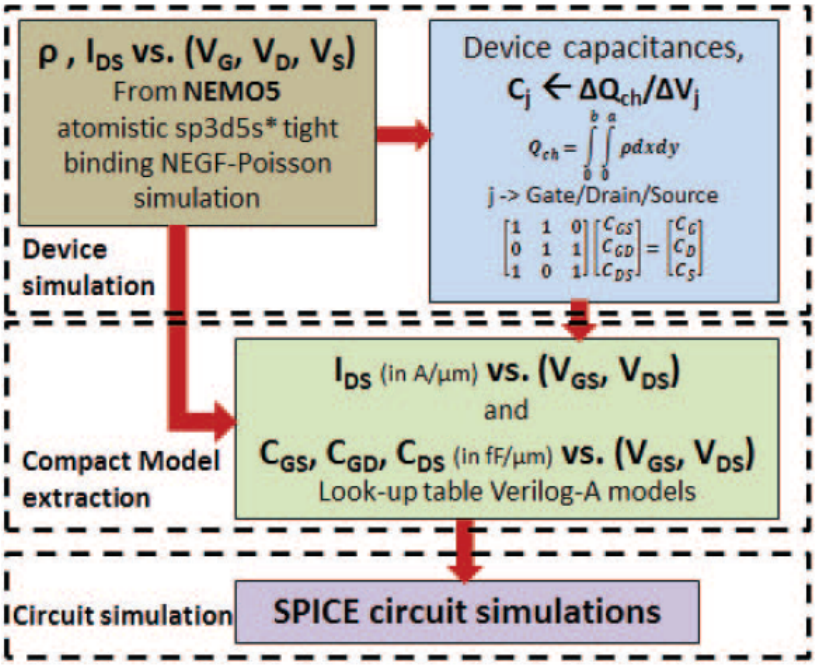

Figura 3.23: Simulation Flow [16] .

The model has been simulated with an H_{FIN} of 12nm, then the transcharacteristic has been manually modified in Excel to obtain the standardisation to $H_{FIN} = 1\mu m$.

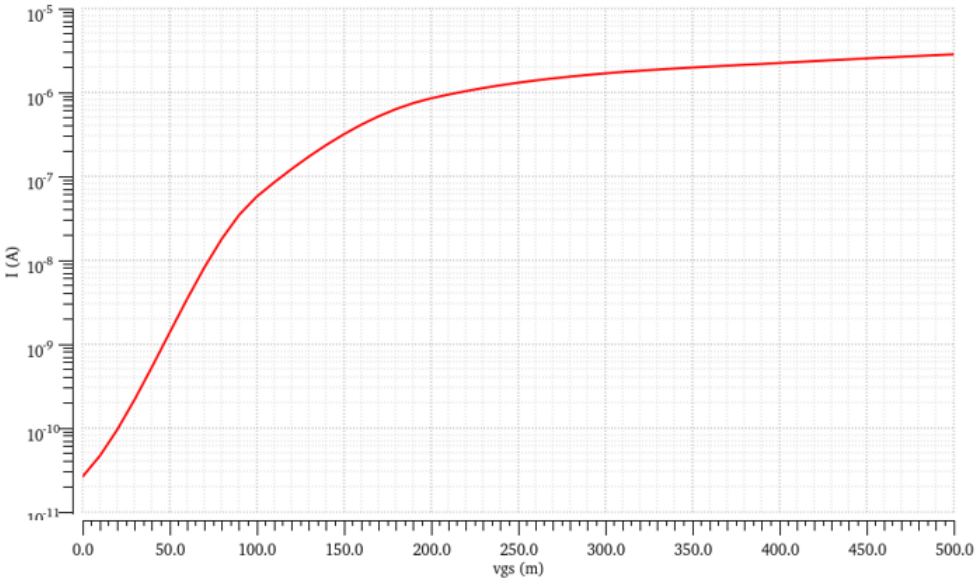

Figura 3.24: GaSb/InAs DG-TFET transcharacteristic for $V_{DD} = 0.5V$ and $H_{FIN} = 12nm$.

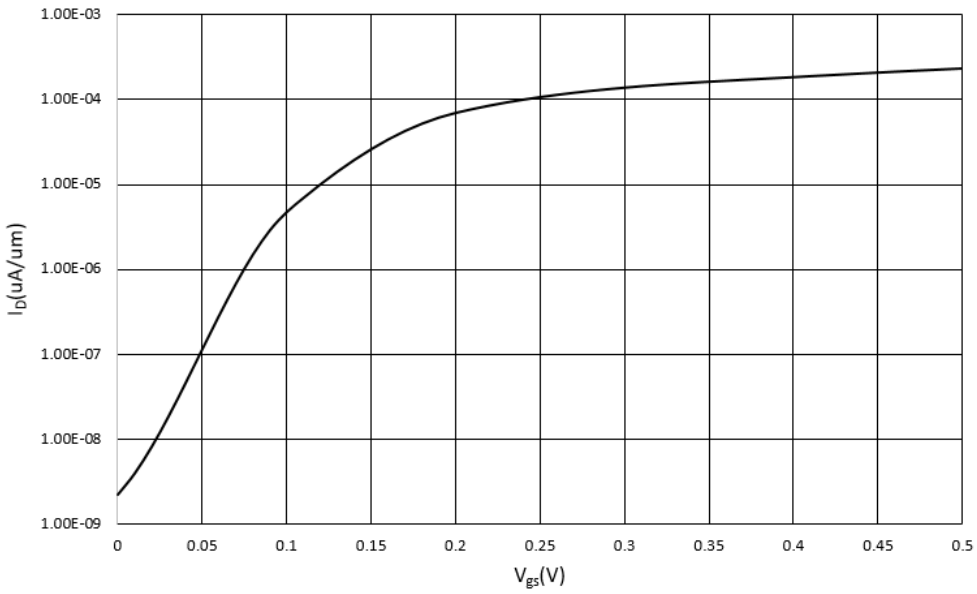

Figura 3.25: GaSb/InAs DG-TFET transcharacteristic for $V_{DD} = 0.5V$ and $H_{FIN} = 1\mu m$.

For $V_{DD} = 500mV$ they have been found an on-current, $(I_D(vgs = vds = 500mV))$, of $234.0\mu A/\mu m$ and an off-current, $(I_D(vgs = 0V, vds = 500mV))$, of $2.2nA/\mu m$, and consequently an I_{on}/I_{off} ratio of $1.06 * 10^5$.

The *trancharacteristic* has been obtained with a parametric simulation by sweepping vds from 0 to 500mV and using vgs as parameter.

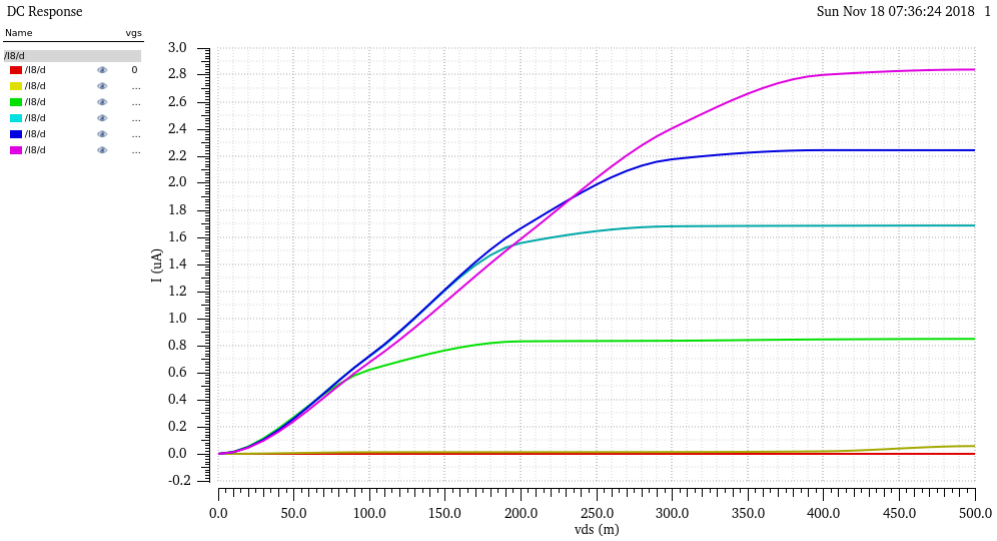

Figura 3.26: GaSb/InAs DG-TFET characteristic.

The fact that the drain-current in TFETs is due to the Band-To-Band-Tunneling instead of thermionic emission lead to another peculiarity for these devices. In fact, the BTBT phenomenon is pratically independent from the carriers mobility, so there is no more need to change the channel width in order to have a specular characteristic between n-type and p-type transistors.

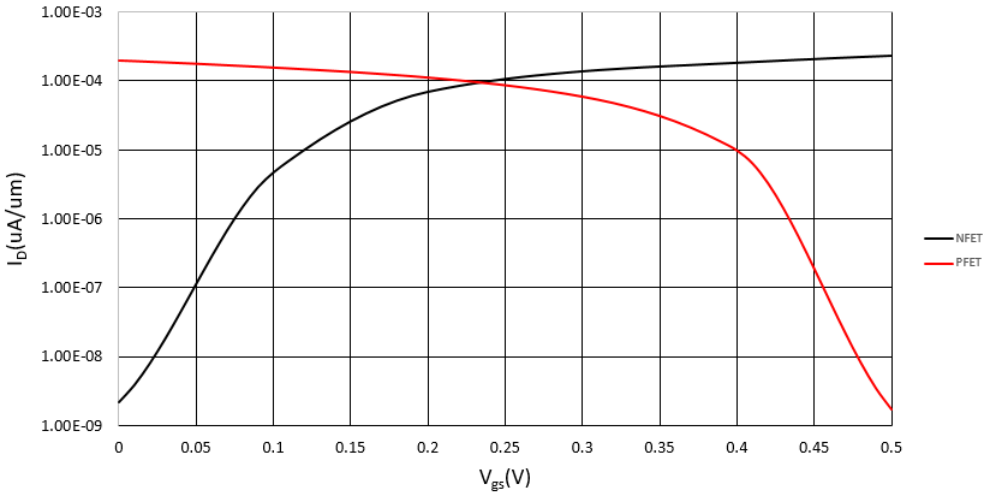

Figura 3.27: GaSb/InAs DG-TFET n-type and p-type comparison.

While for the Hao Lu-based models the match between n-type and p-type was perfect in this case we have some little difference between the two types ($I_{onP} = 200\mu A/\mu m$ and $I_{offP} = 1.7\mu A/\mu m$).

3.4.3 Voltage Threshold and Subthreshold Swing

The Subthreshold Swing is defined as the average slope of logarithmic transcharacteristic from $vgs = 0$ to $vgs = V_{TH}$ [5] :

$$SS = \frac{V_{TH}}{log\frac{I(vgs=V_{TH})}{I_{OFF}}} \tag{3.11}$$

So must be evaluated the voltage threshold before being able to evaluate the subthreshold slope. The voltage threshold is not a well-defined parameter because it is difficult to estabilish when the device turns on. Among the various methods developed in the last years to give a numerical value to the threshold it has been chosen the study of the second derivative of the transcharacteristic 3.28(that is the first derivative of the transconductance) [29] [30] . V_{TH} is defined as the vgs value for the which there is the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

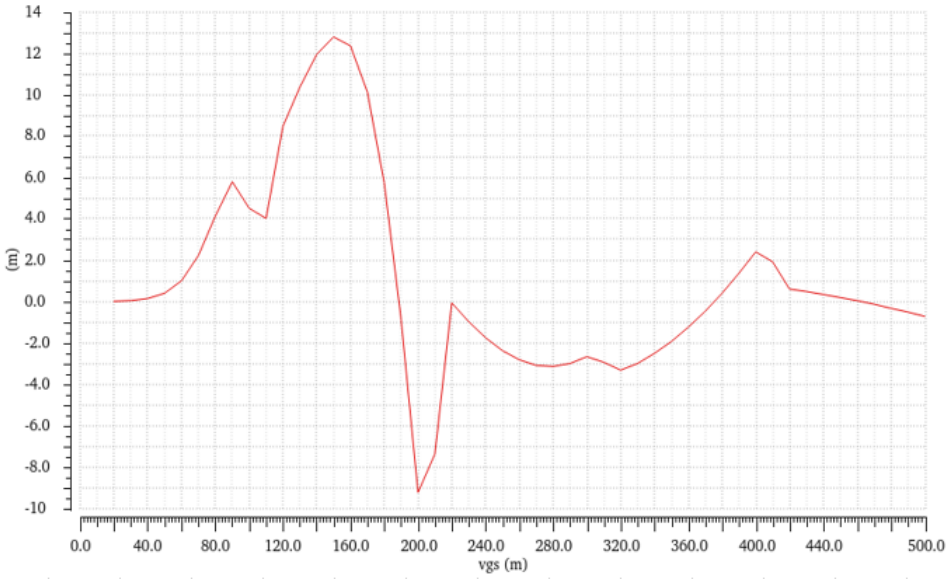

Figura 3.28: GaSb/InAs DG-TFET plot for $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

The curve has been plotted thanks to the function *deriv* of the Virtuoso Calculator. For the GaSb/InAs TFET it has been estimated a voltage threshold of 150mV, and using this value in the 3.11 it has been found $SS = 37mV/dec$.

3.4.4 Drain Induced Barrier Lowering

Drain-induced barrier lowering (DIBL) is a short-channel effect referring to a dependency of threshold voltage of the transistor from the drain voltage. In particular the V_{TH} decreases with V_{DD} and this can lead to a prematurely turn-on of the transistor, and increases the leakage current. On the other hand, the fact that V_{TH} increases with V_{DD} implies a penalty in the working frequency going up with the power supply.

$$DIBL = \frac{V_{TH}^{VDD} - V_{TH}^{VDS_{low}}}{VDD - VDS_{low}} [mV/V] \tag{3.12}$$

The DIBL has been evaluated with a parametric simulation in Virtuoso by plotting $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ for different values of *vds* (taken as parameter).

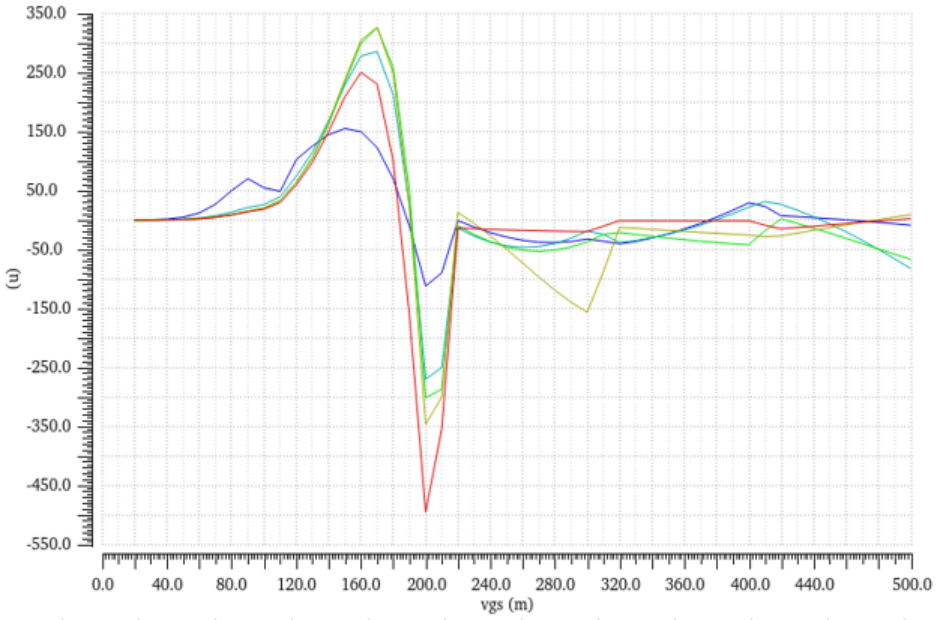

Figura 3.29: For the GaSb/InAs DG-TFET the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ is dependent from V_{DD}, this means a non-null DIBL.

For the GaSb/InAs DG-TFET it has been found that DIBL= 67 mV/V. In this case it is possible to see that the DIBL is different from 0, and the LUT simulation results are more reliable respect to those done with the Hao Lu analytical model.

3.4.5 Note

The waveforms obtained with the LUT-based model card are not so clean because of the difficulties of Spectre in simulating this kind of models.

3.5 BSIM-CMG model for FinFET

The values obtained with the TFETs simulations would be meaningless if they were not put in relationship with the results of another technology. It has been taken as benchmark a 7-nm double gated FinFET designed for low power application [35]. However the LUT-based model card provided for this FinFET cannot be well-simulated by Spectre due to divergence problems [36]. In order to overcome this problem it has been used the BSIM-CMG(v.109) model (online available [37]). BSIM-CMG (Common Multi-Gate) is a compact model for the class of common multi-gate FETs. BSIM-CMG has been implemented in Verilog-A, and it represents an industrial standard. The parameters of this model have been tuned in order to create a model of FinFET that could have current-voltage characteristics similar to the low-power FinFET characteristics found in literature [35]. However it must be clear that the model card developed does not belong to a real device but is based on the characteristics of a low power device.

3.5.1 Characteristics

The TFET has been characterized in Virtuoso using a DC power supply between gate and source (with parametric value vgs) and another DC power supply between drain and source (with parametric value vds).
The *trancharacteristic* has been obtained by sweepping vgs from 0 to 500mV keeping vds constant to 500mV. The results obtained from the simulation of the BSIM-CMG(v.109) have been validated making a comparison with the results of the simulation of the 7-nm FinFET LUT-based model card (online available [38]), in their turn validated with the data found on the reference paper [36] [35].

The model has been simulated with an H_{FIN} of 30nm with DELTAW=0, and accordingly to the user manual of the BSIM-CMG model [39] this represents an effective channel width of 60nm, for GEOMOD=0(DG-FINFET):

$$W_{eff} = 2 * H_{FIN} - DELTAW; \tag{3.13}$$

then the transcharacteristic has been manually modified in Excel to obtain the standardisation to $W_{eff} = 1\mu m$.

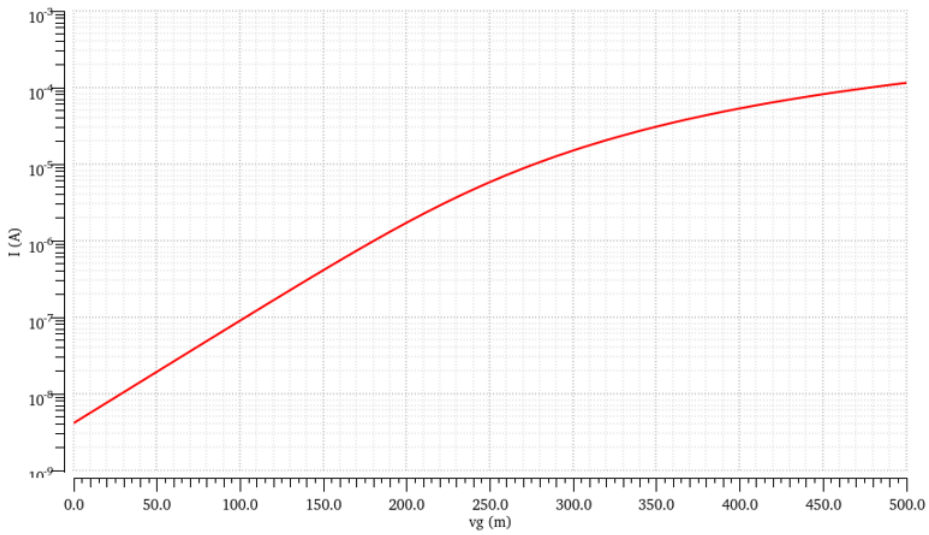

Figura 3.30: BSIM-CMG FinFET transcharacteristic for $V_{DD} = 0.5V$ and $H_{FIN} = 60nm$.

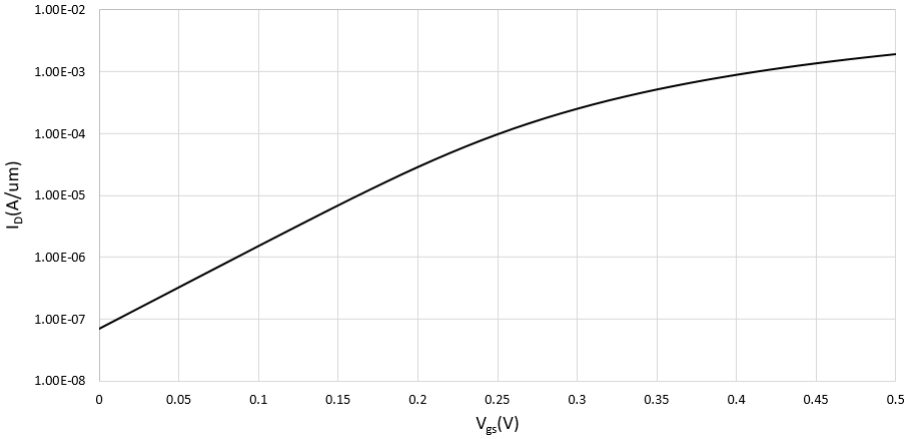

Figura 3.31: BSIM-CMG FinFET transcharacteristic for $V_{DD} = 0.5V$ and $H_{FIN} = 1\mu m$.

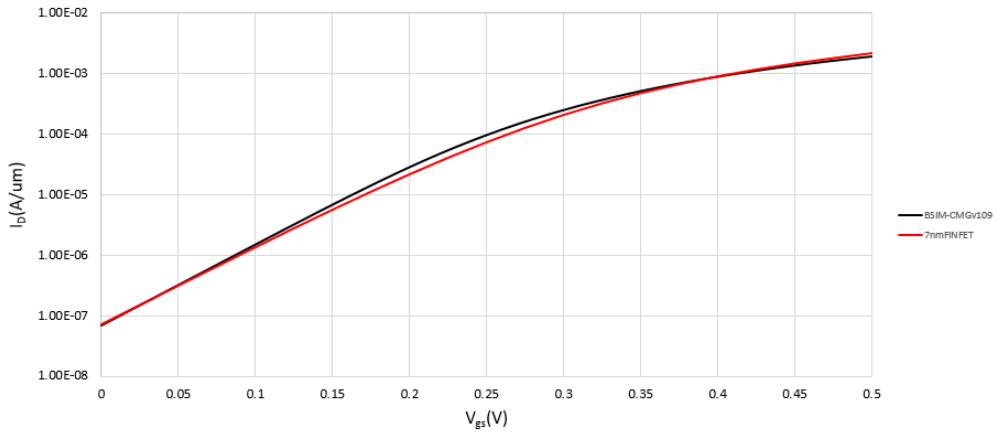

Figura 3.32: BSIM-CMG FinFET vs 7-nm reference FinFET transcharacteristic for $V_{DD} = 0.5V$ and $H_{FIN} = 1\mu m$.

For $V_{DD} = 500mV$ they have been found an on-current, $(I_D(vgs = vds = 500mV))$, of $1.91mA/\mu m$ while the and an off-current, $(I_D(vgs = 0V, vds = 500mV))$, of $69nA/\mu m$, and consequently an I_{on}/I_{off} ratio of $2.81 * 10^4$. From the comparison it is quiet clear that the two transcharacteristic are pratically overlapped. The 7nm reference FinFET has a slightly higher I_{ON} $(2.24mA/\mu m)$and a slightly higher I_{OFF} $(73nA/\mu m)$. The model parameters for the FinFET have been tuned in order to be slightly "more low-power" respect to the reference. The ratio I_{ON}/I_{OFF} is $3.3 * 10^4$ but this is substantially due to the fact that the 7-nm FinFET has an higher voltage threshold (360mV) and SS (91.5mV).

The *trancharacteristic* has instead been obtained with a parametric simulation by sweeping vds from 0 to 500mV and using vgs as parameter.

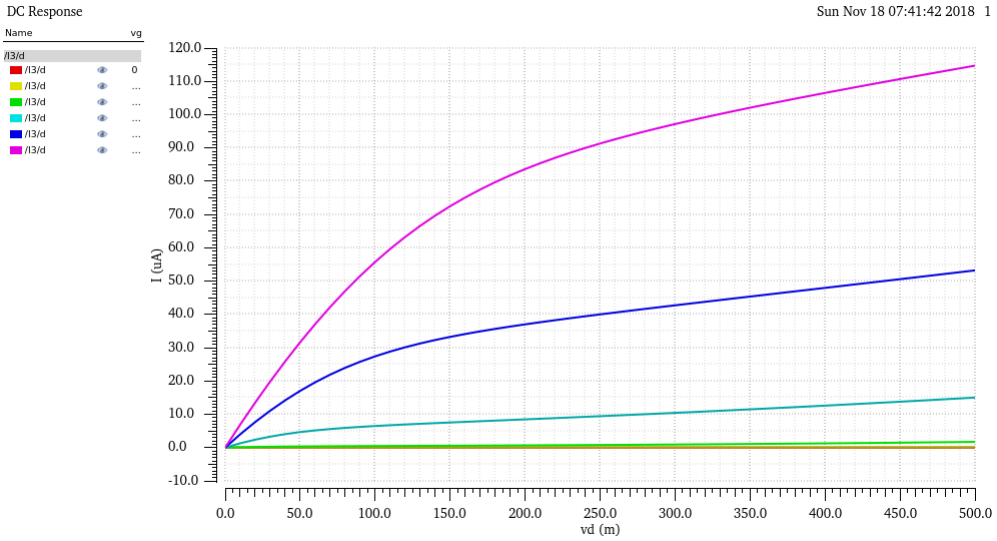

Figura 3.33: BSIM-CMG FinFET characteristic.

The parameters of the model have been set in order to have a specular characteristic between n-type and p-type transistors.

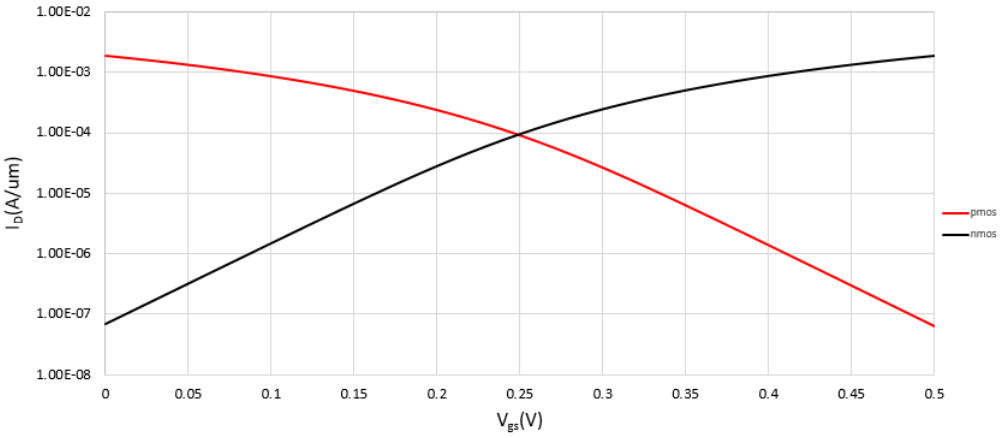

Figura 3.34: BSIM-CMG FinFET n-type and p-type comparison.

3.5.2 Voltage Threshold and Subthreshold Swing

The Subthreshold Swing is defined as the average slope of logarithmic transcharacteristic from $vgs = 0$ to $vgs = V_{TH}$ [5] :

$$SS = \frac{V_{TH}}{log\frac{I(vgs=V_{TH})}{I_{OFF}}} \tag{3.14}$$

So must be evaluated the voltage threshold before being able to evaluate the subthreshold slope. The voltage threshold is not a well-defined parameter because it is difficult to estabilish when the device turns on. Among the various methods developed in the last years to give a numerical value to the threshold it has been chosen the study of the second derivative of the transcharacteristic 3.35(that is the first derivative of the transconductance)[29] [30]. V_{TH} is defined as the vgs value for the which there is the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

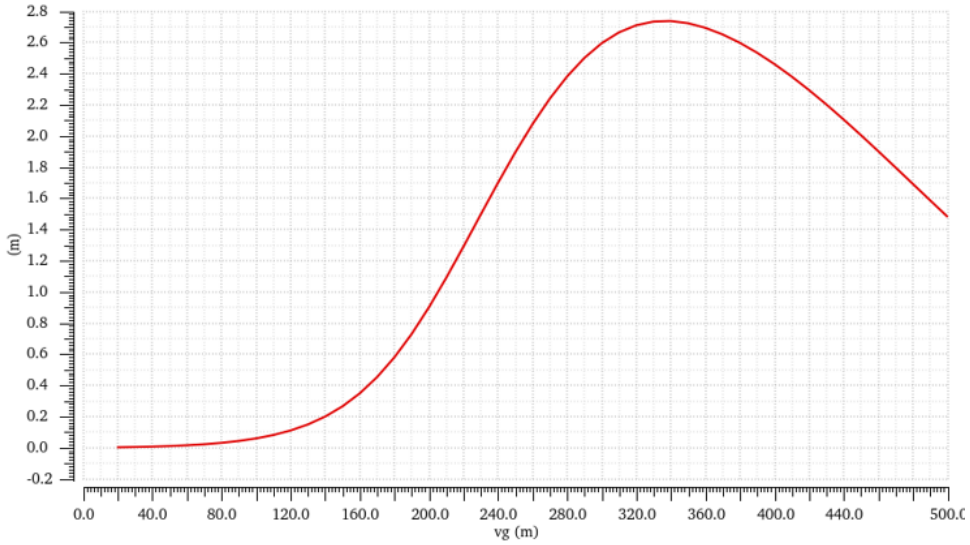

Figura 3.35: BSIM-CMG FinFET plot for $\frac{\partial^2 I_D}{\partial v_{gs}^2}$.

The curve has been plotted thanks to the function *deriv* of the Virtuoso Calculator. For the BSIM-CMG FinFET it has been estimated a voltage threshold of 340mV, and using this value in the 3.14 it has been found $SS = 89mV/dec$.

3.5.3 Drain Induced Barrier Lowering

Drain-induced barrier lowering (DIBL) is a short-channel effect referring to a dependency of threshold voltage of the transistor from drain voltages. In particular the V_{TH} decreases with V_{DD} and this can lead to a prematurely turn-on of the transistor, and increases the leakage current. On the other hand, the fact that V_{TH} increases with V_{DD} implies a penalty in the working frequency going up with the power supply.

$$DIBL = \frac{V_{TH}^{VDD} - V_{TH}^{VDS_{low}}}{VDD - VDS_{low}}[mV/V] \tag{3.15}$$

The DIBL has been evaluated with a parametric simulation in Virtuoso by plotting $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ for different values of *vds* (taken as parameter).

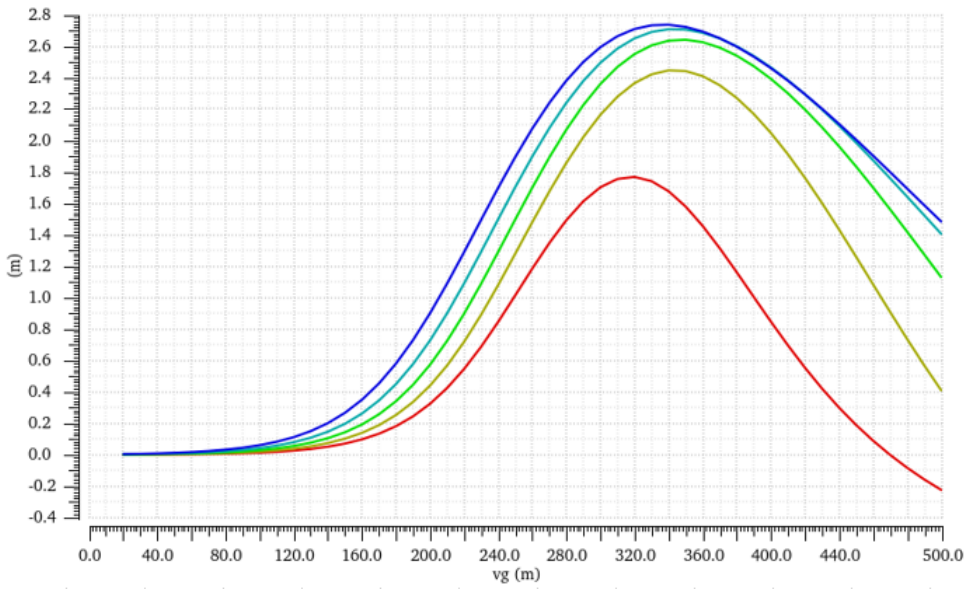

Figura 3.36: For BSIM-CMG based FinFET the maximum of $\frac{\partial^2 I_D}{\partial v_{gs}^2}$ is dependent from V_{DD}, this means a non-null DIBL.

For the FinFET it has been found that DIBL= 50 mV/V, as in the reference 7-nm FinFET.

3.6 Results summary

In this section the results obtained, simulating the several devices taken into account, are put together.

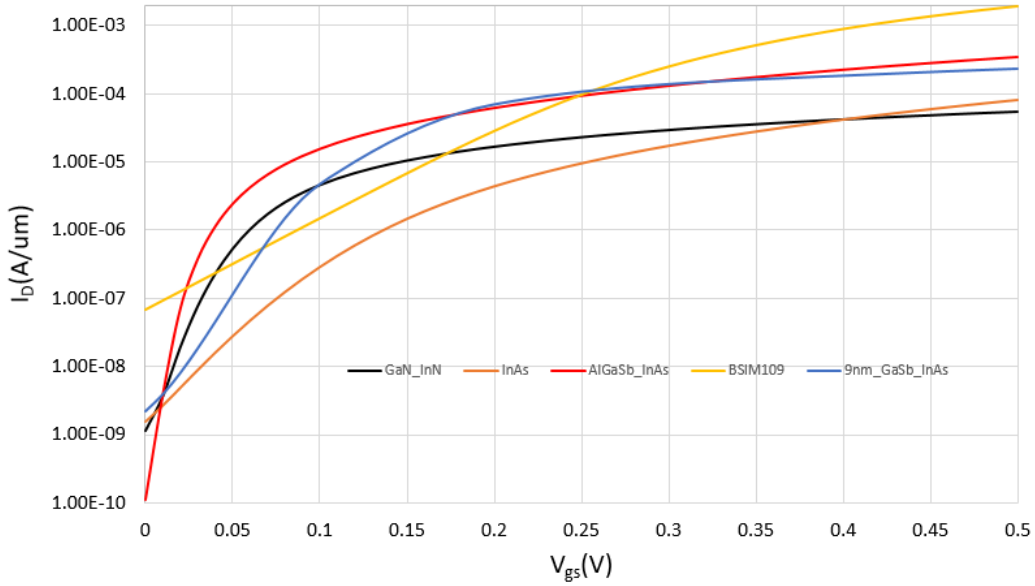

Figura 3.37: Comparison between the transcharacteristics of the simulated devices for $V_{DD} = 500mV$.

	Ion(uA/um)	Ioff(nA/um)	Ion/Ioff(k)	SS(mV/dec)	Vth(mV)
InAs	80.3	1.6	50.2	49	140
AlGaSb/InAs	351.0	0.111	3160	12.15	50
GaN/InN	54.4	1.2	46.5	20.35	60
GaSb/InAs	234.0	2.2	106	37	150
FinFET	1910	68	28.1	89	340

Tabella 3.1: Summary of the electrical parameters of the simulated devices for $V_{DD} = 500mV$.

The higher I_{ON} is, as expected, that of the FinFET, while the subthreshold swing of the AlGaSb/InAs TFET is lowest among the simulated devices. Consequently this device shows also the lower I_{OFF} and the greatest I_{ON}/I_{OFF} ratio, that is greater than two orders of magnitude respect to that of the FinFET.

CHAPTER 4

Performances evaluation of TFETs Ring Oscillators

The first logic circuits used to evaluate the Tunnel FETs performances are the ring oscillators. A ring oscillator consists of three or more odd number of inverter stages in a negative feedback loop configuration. They represent one of the most important element in all wired or wireless communication systems, and are also used in biomedical applications like pacemakers [40] [41]. The simulations are runned with a gate width of 30nm for the Hao Lu TFETs and an effective gate width W_{eff} of 60nm for the FinFET. The gate width does not affect the oscillation frequency since the drain-current is proportional to W such as the output capacitance. 7-staged, 11-staged and 15-staged ring oscillators have been taken into account. The first part of the chapter illustrates how the key parameters(frequency, dynamic and static power) depend from power supply, number of stages and temperature considering ring oscillators composed by FinFETs and AlGaSb/InAs TFET. The second part of the chapter contains the performances comparison between the several technologies considered, focusing on the performances variations going from a sub-threshold regime to a super-threshold regime [42] [26].

4.1 Oscillation Frequency

The output oscillation frequency depends on the number of the stages and from the voltage supply [43] :

$$f_{osc} = \frac{1}{2Nt_d} \tag{4.1}$$

where t_d is the delay of a single inverter, that is inversely proportional to V_{DD}. In order to validate the simulation results, it has been checked that the frequency variation coefficient(at a certain V_{DD}) for ring oscillators with different number of stages, was equal to the ratio beetwen the number of stages:

$$f_{osc1} = \frac{N2}{N1} f_{osc2} \tag{4.2}$$

The simulations have been carried out with Cadence Virtuoso, using Spectre as simulator. Several transient simulations have been set up varying the value of V_{DD}. The frequency has been evaluated by checking the signal on the feedback branch and extrapolating its frequency thanks to the *frequency* function present in the Virtuoso Calculator.

4.1.1 Oscillation Frequency for FinFET ring oscillators

In this section the results obtained simulating the 7, 11 and 15-staged oscillators composed by FinFETs are reported. The frequency has been plotted as a function of the power supply, using the number of stages and the temperature as parameters.

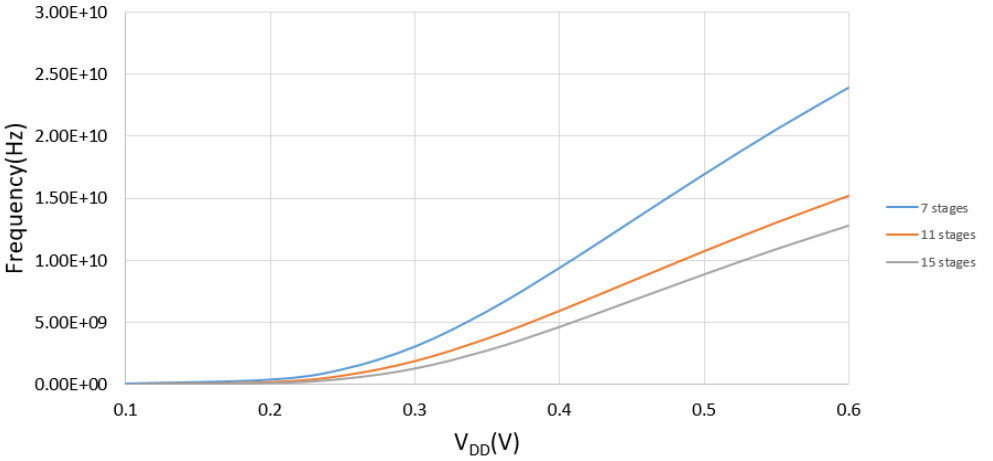

Figura 4.1: FinFETs ring oscillator frequency vs power supply, for different number of stages, at 27°C.

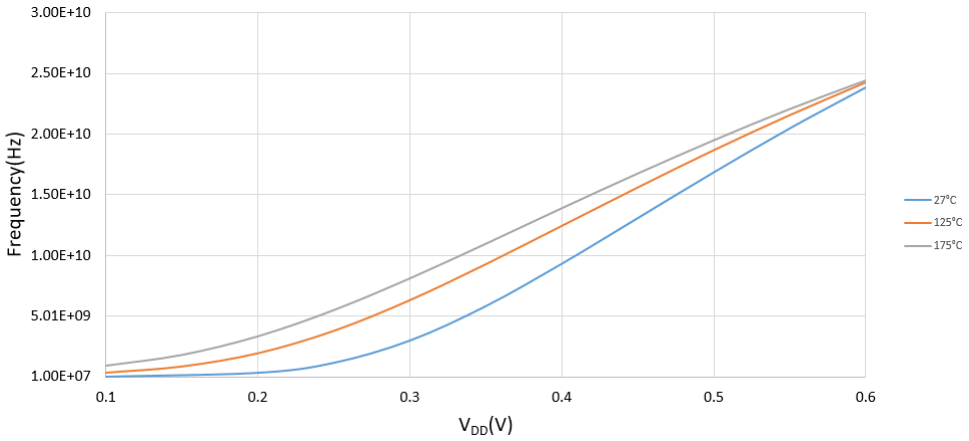

Figura 4.2: FinFETs 7-staged ring oscillator frequency vs power supply, for different temperatures.

From Fig.4.1 and Fig.4.2 it can be noticed the linear dependence of the frequency respect to the number of stages and a non linear dependence from V_{DD}. Moreover, it is showed also that the temperature seems to impact more for low values of V_{DD} while it is pretty irrelevant for $V_{DD} > 0.5V$.

4.1.2 Oscillation Frequency for TFETs ring oscillators

In this section the results obtained simulating the 7, 11 and 15-staged oscillators composed by AlGaSb/InAs TFETs are reported. The frequency has been plotted as a function of the power supply, using the number of stages and the temperature as parameters.

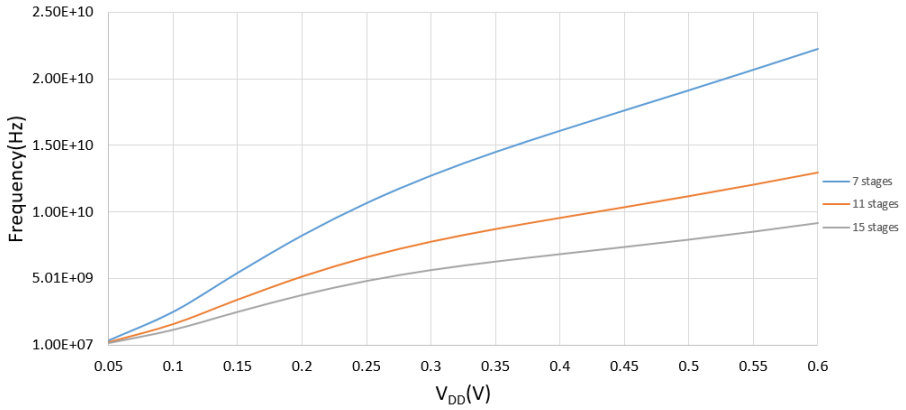

Figura 4.3: TFETs ring oscillators frequency vs power supply, for different number of stages, at 27°C.

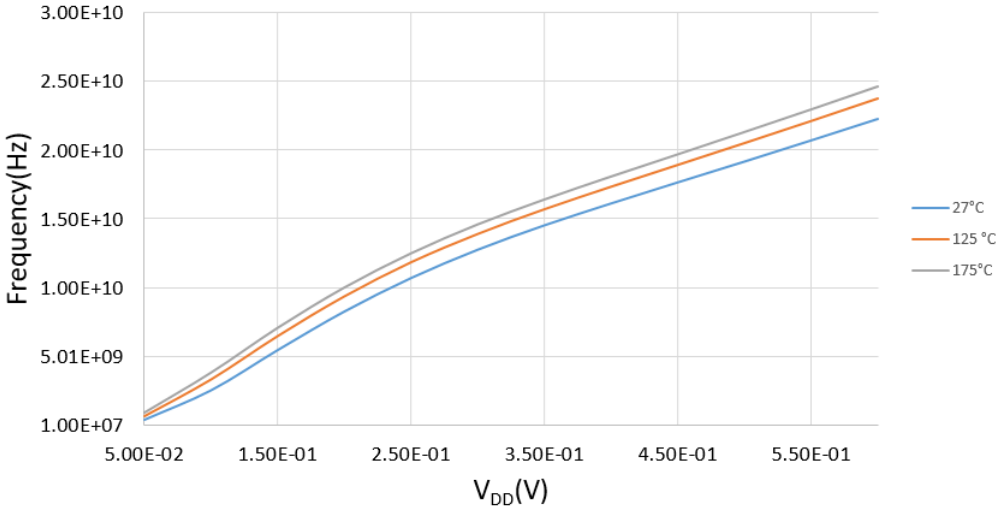

Figura 4.4: TFETs 7-staged ring oscillator frequency vs power supply, for different temperatures.

From Fig.4.3 and Fig.4.4 it can be noticed the linear dependence of the frequency respect to the number of stage and the nonlinear dependence from V_{DD}, just like in the traditional transistors. Moreover, it is showed also that in this case the temperature seems to be irrelevant also for low values of V_{DD}.

4.2 Dynamic Consumption

The dynamic power is the power needed by the ciruit during its normal activity. It is proportional to the output capacitance of the ring oscillators, other than to the voltage supply and oscillation frequency:

$$P_{Dyn} = fCV_{DD}^2 \tag{4.3}$$

The simulations have been carried out with Virtuoso, using Spectre as simulator. Several transient simulations have been set up varying the value of V_{DD}. The dynamic power has been evaluated by multiplying V_{DD} by the current provided by the power supply, during the normal activity of the circuit, and extrapolating its average value thanks to the *average* function present in the Virtuoso Calculator [44] .

4.2.1 Dynamic Consumption for FinFETs Ring Oscillators

In this section the results obtained simulating the 7, 11 and 15-staged oscillators composed by FinFETs are reported. The dynamic power has been plotted as a function of the power supply, using the number of stages and the temperature as parameters.

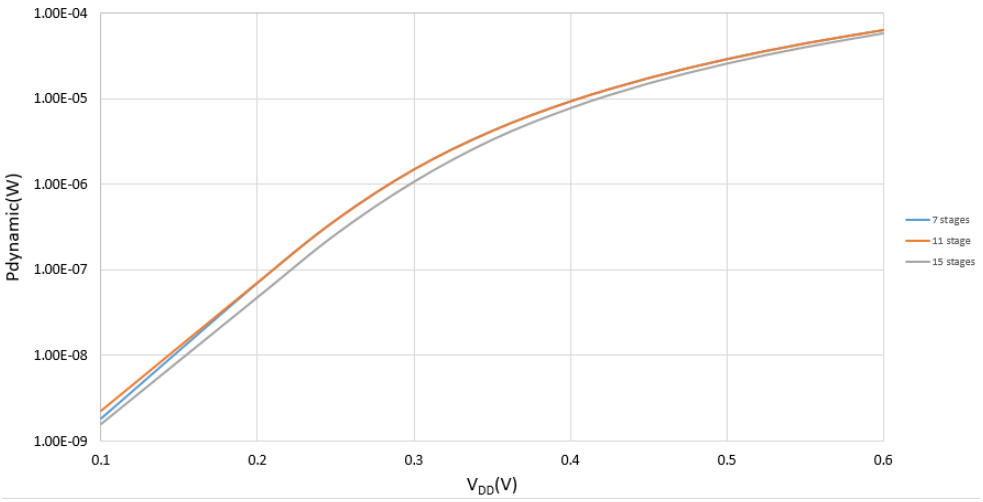

Figura 4.5: FinFETs ring oscillators dynamic consumption vs power supply, for different number of stages, at 27°C.

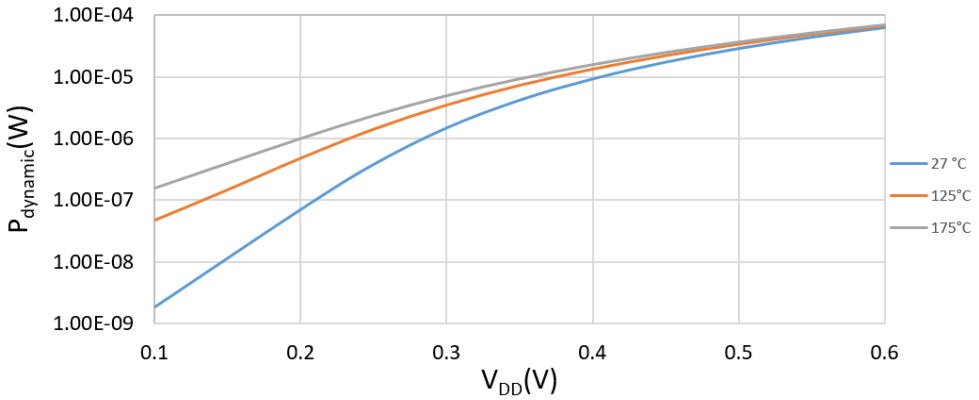

Figura 4.6: FinFETs 7-staged ring oscillator frequency vs power supply, for different temperatures.

From Fig.4.5 and Fig,4.6 it can be noticed that the dynamic power seems to be independent from the number of stages of the circuit. In fact, when N increases, f decreases proportionally, but the output capacitance of the circuit increases of the same amount, leaving nearly unaltered the power consumption. Just like in the frequency case, the temperature seems to have an higher impact for low V_{DD}s, while it is pretty irrelevant for $V_{DD} > 0.5V$.

4.2.2 Dynamic Consumption for TFETs Ring Oscillators

In this section the results obtained simulating the 7, 11 and 15-staged oscillators composed by AlGaSb/InAs TFETs are reported. The dynamic power has been plotted as a function of the power supply, using the number of stages and the temperature as parameters.

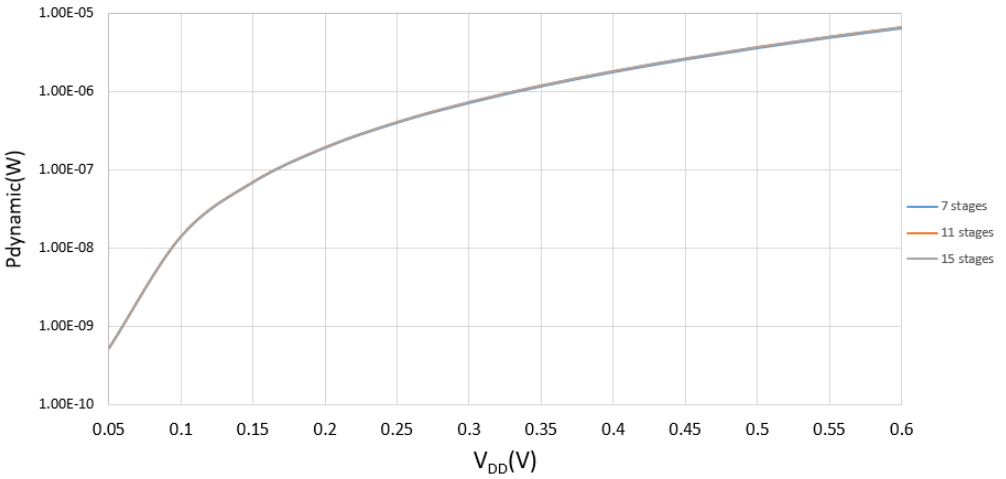

Figura 4.7: TFETs ring oscillators dynamic consumption vs power supply, for different number of stages, at 27°C.

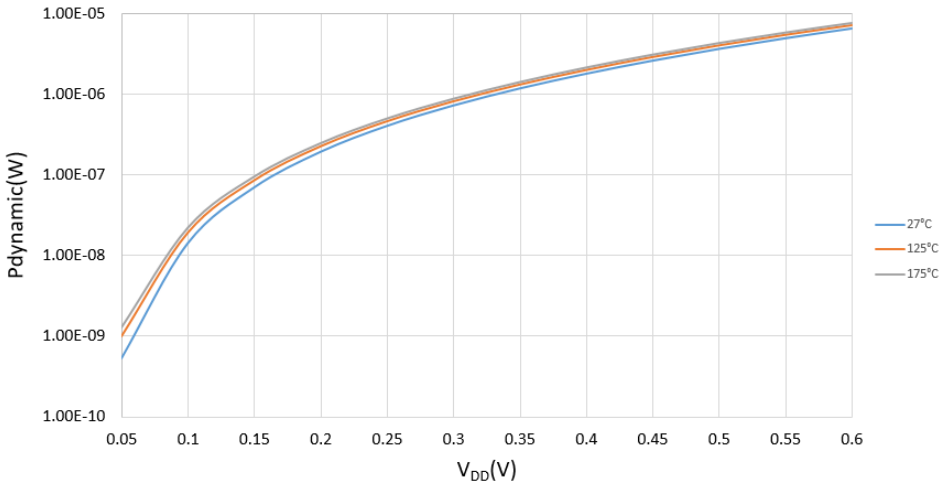

Figura 4.8: TFETs 7-staged ring oscillator frequency vs power supply, for different temperatures.

From Fig.4.7 and Fig.4.8 it can be noticed that the dynamic power seems to be independent from the number of stages of the circuit. In fact, when N increases, f decreases proportionally, but the output capacitance of the circuit increases of the same amount, leaving nearly unaltered the power consumption, just like for the traditional transistors. The temperature seems not to have a significant impact for any value of V_{DD}, just like in the frequency case for TFETs. The fact that the dynamic parameters for the TFETs have a lower dependency from the temperature reflects the lower importance of the temperature on the band to band tunneling proccess respect to the thermionic

emission.

4.3 Static Consumption

The static power is the power wasted by the ciruit when there is no circuit activity and it is due to the leakage current of each inverter. Supposing that each inverter of the chain has the same leakage current, the static consumption is given by:

$$P_{static} = N I_{leak} V_{DD} \tag{4.4}$$

Where I_{leak} is also dependent from the power supply, so there is not a true linear dependency from V_{DD}. In order to evaluate the static power consumption in Virtuoso, the output of the last inverter of the chain was disconnected from the input of the first inverter. The input of the first inverter was connected to GND, while the output of the last inverter was connected to V_{DD}. In this way the activity of the inverters is blocked. Many transient simulations were done by varying the value for V_{DD}. The static power has been evaluated by multiplying V_{DD} by the current provided by the power supply, when there is no switching activity in the inverters, and extrapolating its average value thanks to the *average* function present in the Virtuoso Calculator [44] .

4.3.1 Static Consumption for FinFETs Ring Oscillators

In this section the results obtained simulating the 7, 11 and 15-staged oscillators composed by FinFETs are reported. The static power has been plotted as a function of the power supply, using the number of stages and the temperature as parameters.

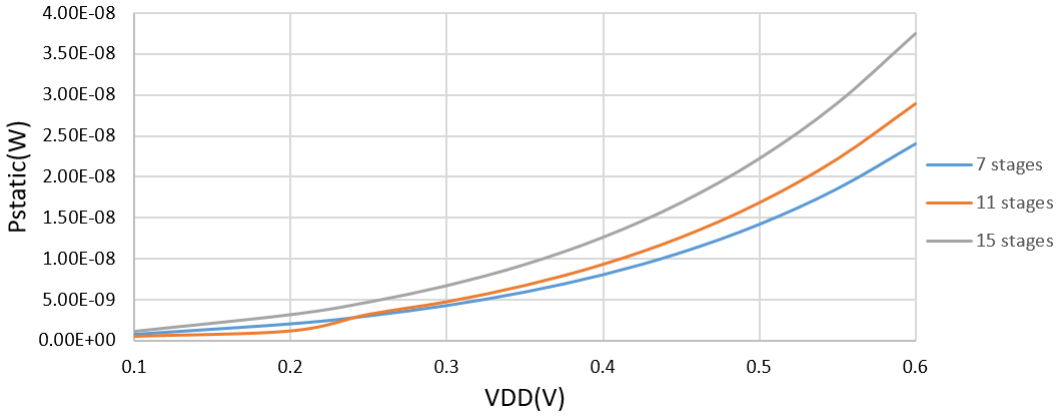

Figura 4.9: FinFETs ring oscillators static consumption vs power supply, for different number of stages, at 27°C.

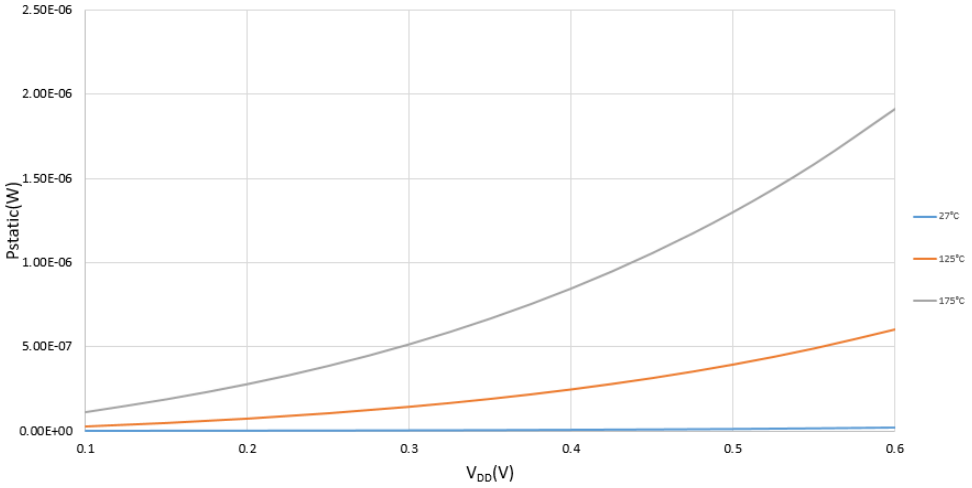

Figura 4.10: FinFETs 7-staged ring oscillator static consumption vs power supply, for different temperatures.

From Fig.4.9 and Fig.4.10 it can be noticed that the static power seems to be strongly dependent from the number of stages of the circuit. In fact, the more are the inverters in the circuit and the bigger will be the total leakage current. The temperature has a much greater impact on the static consumptions rather than on the dynamic ones. In fact, it can be seen that the static power increases of around 100 times for $V_{DD} = 0.6V$, when the temperature raises from 27°C to 175°C.

4.3.2 Static Consumption for TFETs Ring Oscillators

In this section the results obtained simulating the 7, 11 and 15-staged oscillators composed by AlGaSb/InAs TFETs are reported. The static power has been plotted as a function of the power supply, using the number of stages and the temperature as parameters.

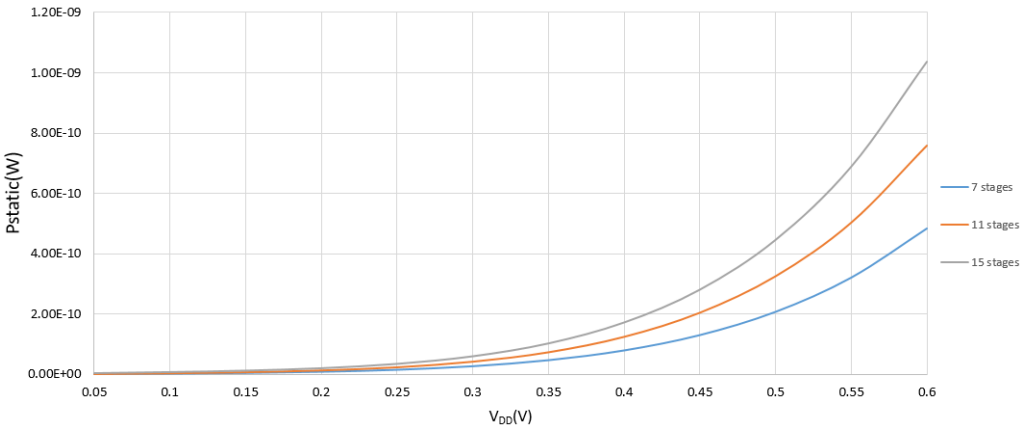

Figura 4.11: TFETs ring oscillators static consumption vs power supply, for different number of stages, at 27°C.

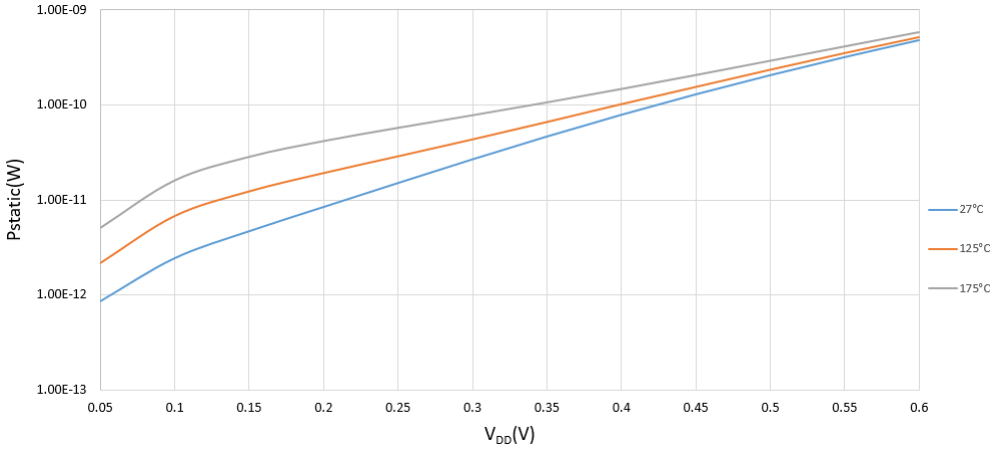

Figura 4.12: TFETs 7-staged ring oscillator static consumption vs power supply, for different temperatures.

From Fig.4.11 and Fig.4.12 it can be noticed that the static power seems to be strongly dependent from the number of stages of the circuit, just like in the FinFETs case. In fact, the more are the inverters in the circuit and the bigger will be the total leakage current. The temperature has a much lower impact for the static consumptions than for

the FinFETs case. In fact, the temperature sweep provokes a maximum power increase of around 5 times.

4.4 Performances for 7-staged ring oscillators

In this section the results obtained simulating the 7-staged oscillators composed by FinFETs, and the results obtained simulating the 7-staged oscillators composed by TFETs, are compared.

4.4.1 7-staged Ring Oscillators dynamic parameters

In this part the dynamic parameters of the simulated 7-staged ring oscillators are compared. In addition to frequency and dynamic power also the power-delay product has been evaluated. This factor shows the trade-off between speed and power consumption, so the lower is this factor, the better will be the circuit.

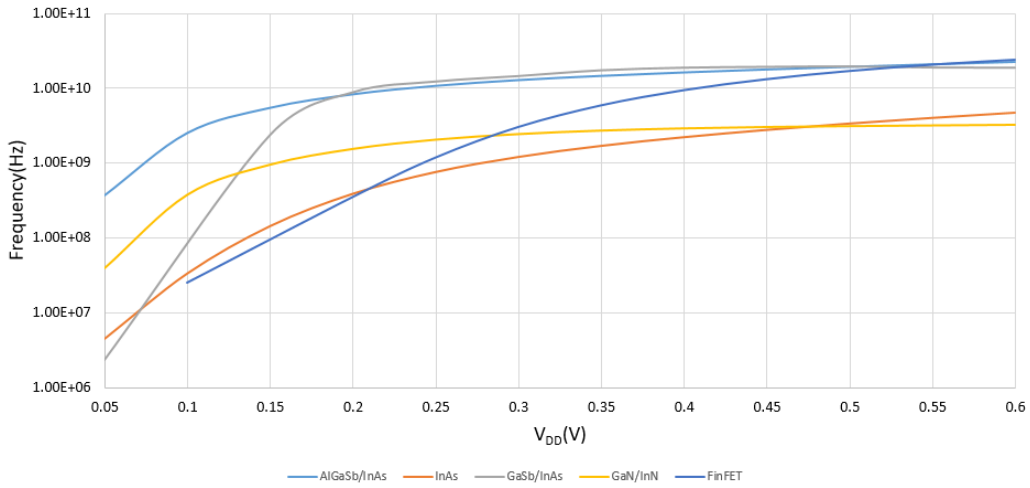

Figura 4.13: Comparison between the 7-staged ring oscillators frequencies for the several technologies used, at 27°C.

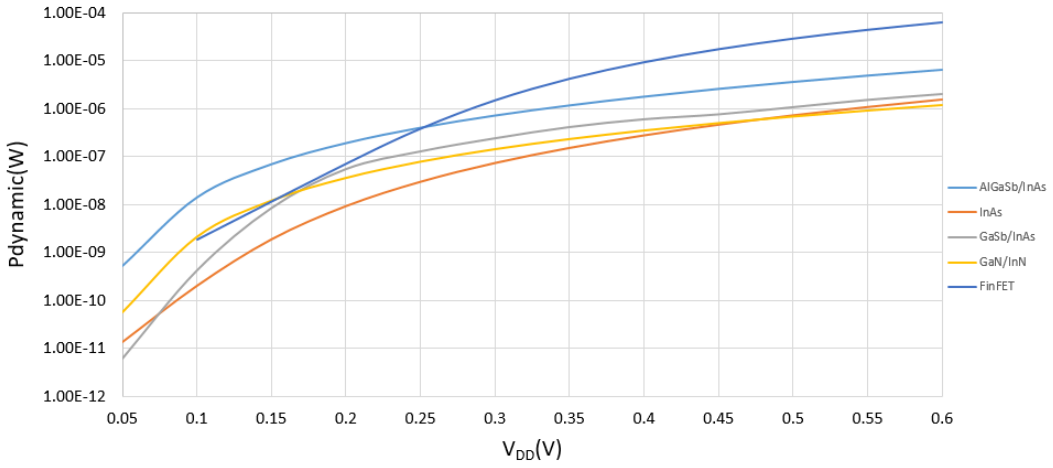

Figura 4.14: Comparison between the 7-staged ring oscillators dynamic consumption for the several technologies used, at 27°C.

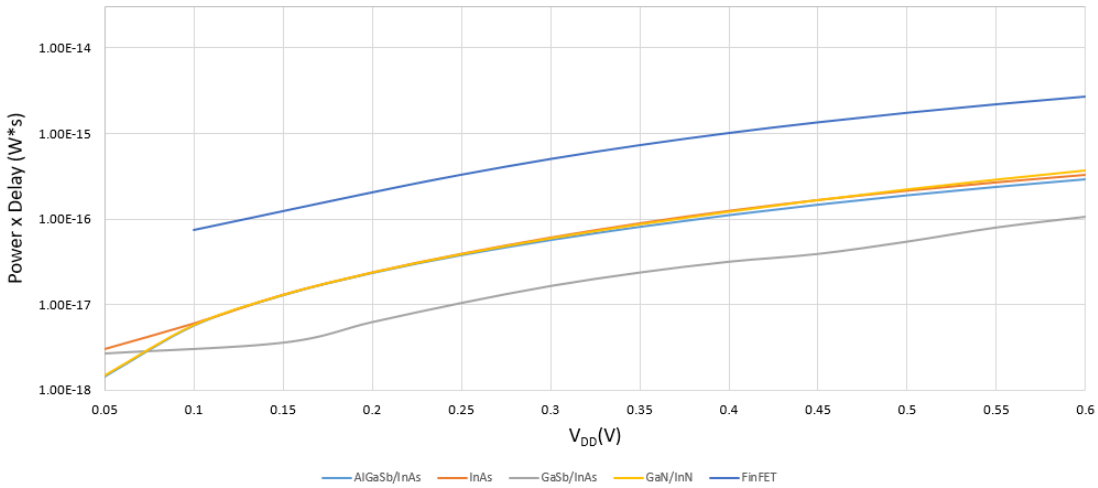

Figura 4.15: Comparison between the 7-staged ring oscillators power-delay factor for the several technologies used, at 27°C.

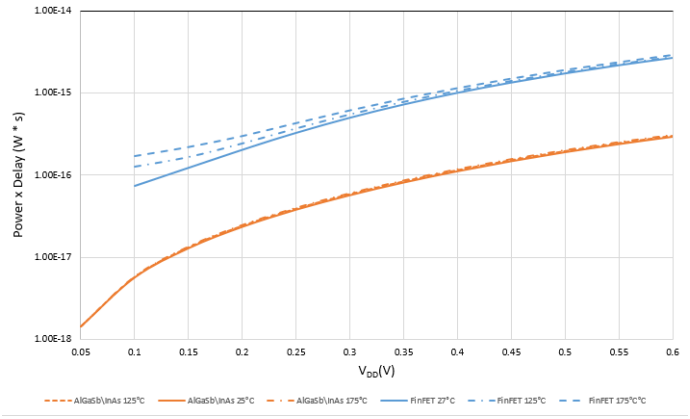

Figura 4.16: Comparison between the 7-staged ring oscillators power-delay factor for the FinFETs and AlGaSb/InAs technologies used, at 27°C, 125°C and 175°C.

From Fig.4.13, Fig.4.14, Fig.4.15 and Fig.4.16 it is possible to see that:

- For V_{DD} lower than 250mV (Subthreshold Region) the FinFETs ring oscillator is the slowest, but becomes the fastest for V_{DD} higher than 500mV (super threshold region). In the near threshold region (300mV - 500mV) the FinFETs ring oscillator is still slower than the AlGaSb/InAs and GaSb/InAs TFETs;
- For V_{DD} higher than 250mV the FinFETs ring oscillator is the circuit with the greatest power consumption;
- For V_{DD} lower than 600mV the FinFETs is the device with the worst trade-off between speed and power consumption;
- The power-delay factor for the TFETs ring oscillators is pratically not affected by the temperature sweep. The FinFETs dynamic parameters are still weakly influenced by temperature but for low values of V_{DD} can be observed a significant variation of the power-delay factor.

4.4.2 7-staged Ring Oscillators static consumption

In this section the static power consumptions of the simulated 7-staged ring oscillators are compared.

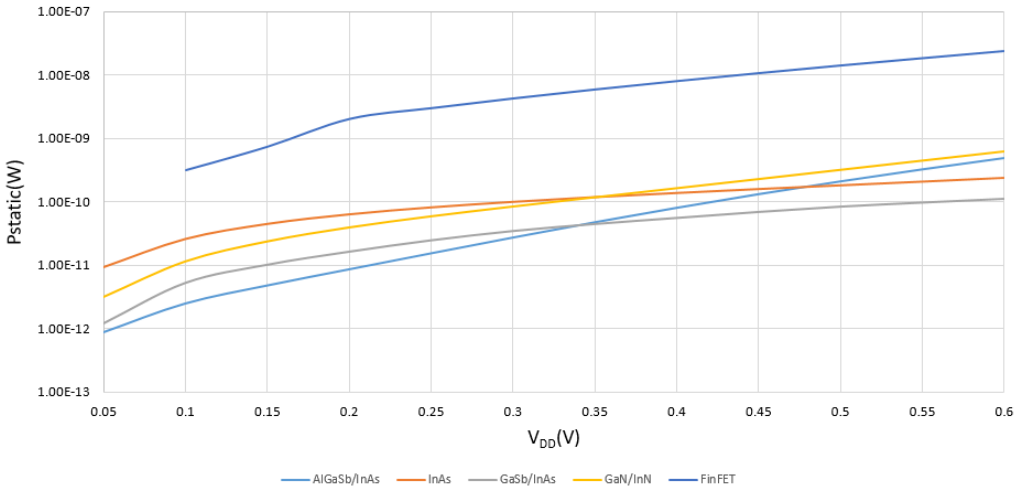

Figura 4.17: Comparison between the 7-staged ring oscillators static consumption for the several technologies used, at 27°C.

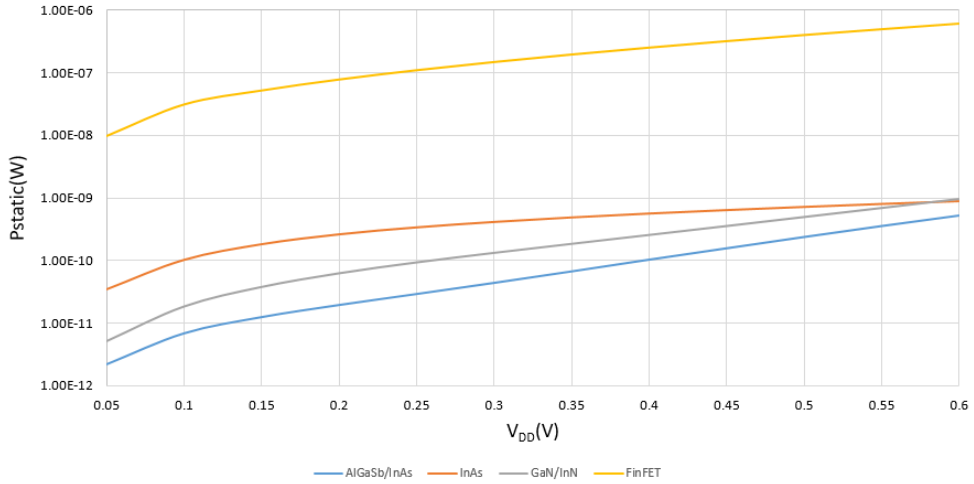

Figura 4.18: Comparison between the 7-staged ring oscillators static consumption for the several technologies used, at 125°C.

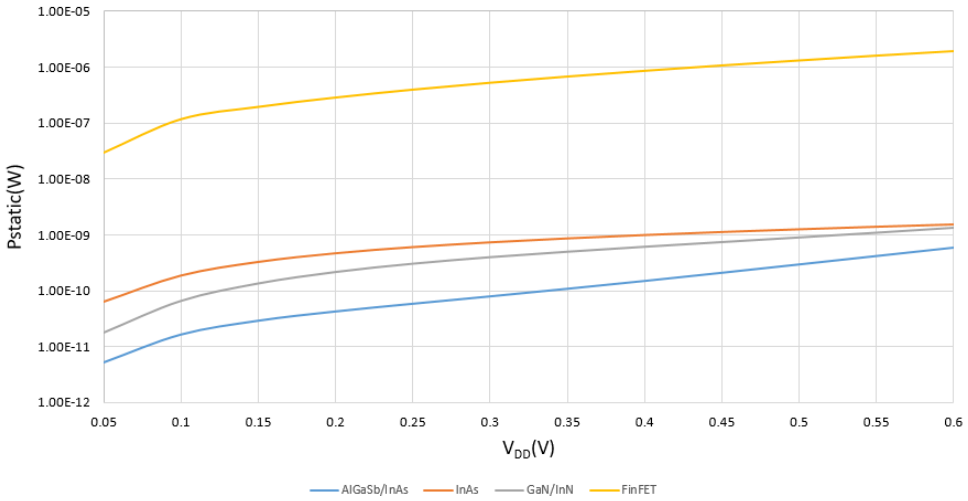

Figura 4.19: Comparison between the 7-staged ring oscillators static consumption for the several technologies used, at 175°C.

From Fig.4.17, Fig.4.18 and Fig.4.19 it is possible to see that the TFETs static consumption is, more or less, 50 times lower that the FinFETs one. For a temperature of 175°C the FinFETs power consumption becomes more than 1000 times greater than the TFETs one. The TFETs static power consumption remains pratically the same despite the rising of the temperature.

4.5 Performances for 11-staged Ring Oscillators

In this section the results obtained simulating the 11-staged oscillators composed by FinFETs, and the results obtained simulating the 11-staged oscillators composed by TFETs, are compared.

4.5.1 11-staged Ring Oscillators dynamic parameters

In this part the dynamic parameters of the simulated 11-staged ring oscillators are compared. In addition to frequency and dynamic power also the power-delay product has been evaluated. This factor shows the trade-off between speed and power consumption, so the lower is this factor, the better will be the circuit.

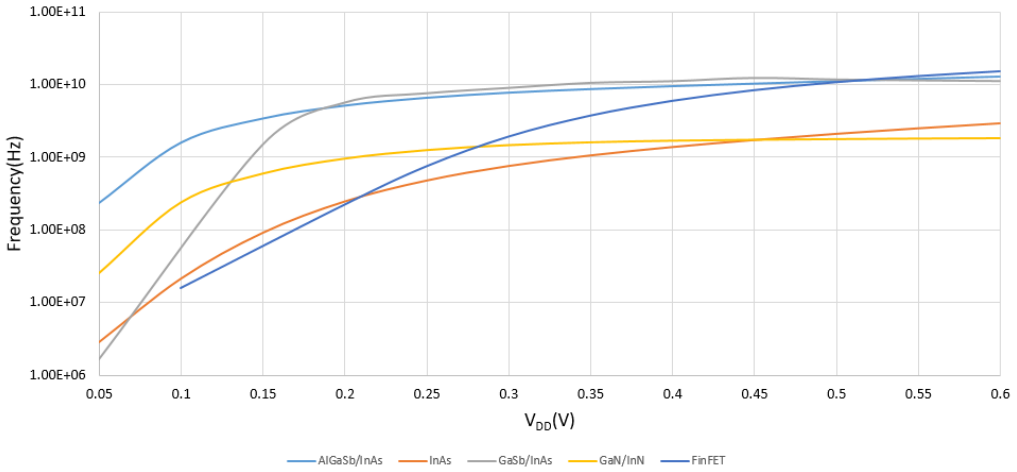

Figura 4.20: Comparison between the 11-staged ring oscillators frequencies for the several technologies used, at 27°C.

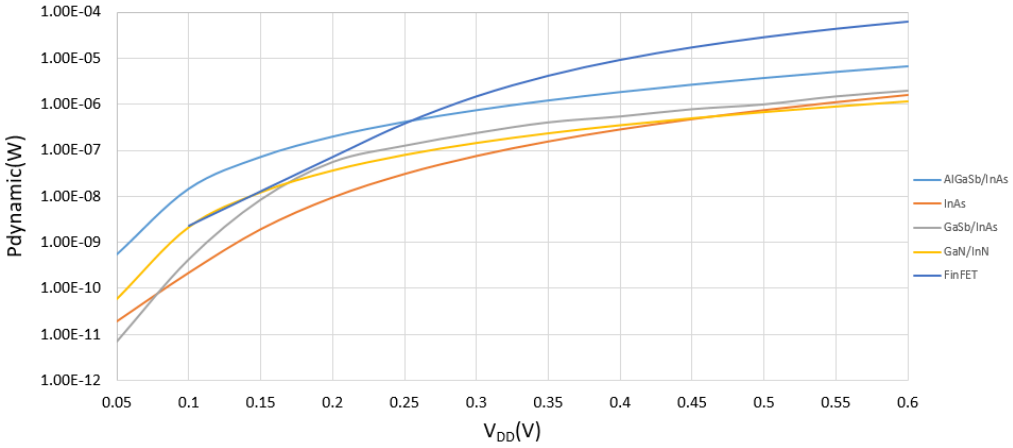

Figura 4.21: Comparison between the 11-staged ring oscillators dynamic consumption for the several technologies used, at 27°C.

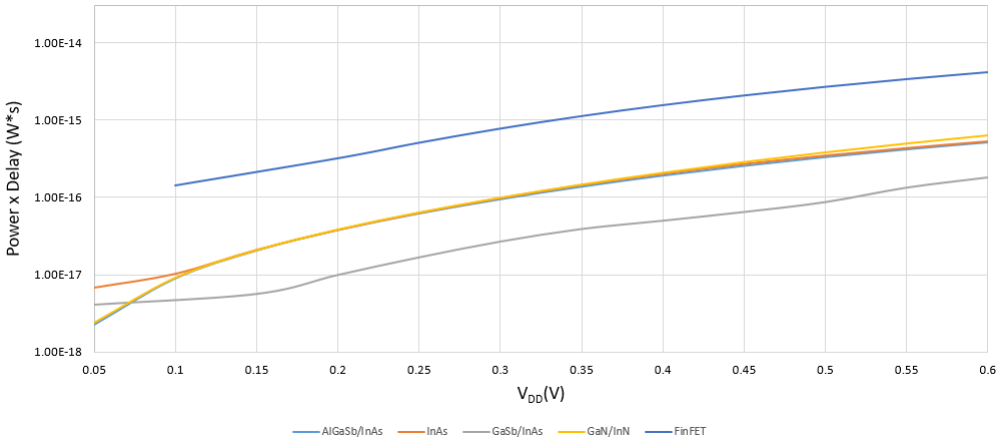

Figura 4.22: Comparison between the 11-staged ring oscillators power-delay factor for the several technologies used, at 27°C.

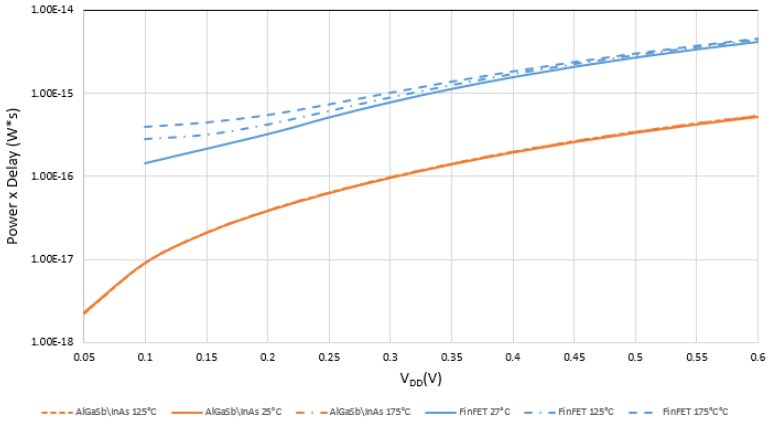

Figura 4.23: Comparison between the 11-staged ring oscillators power-delay factor for the FinFETs and AlGaSb/InAs technologies used, at 27°C, 125°C and 175°C.

From Fig.4.20, Fig.4.21, Fig.4.22 and Fig.4.23 it is possible to see that:

- For V_{DD} lower than 250mV (Subthreshold Region) the FinFETs ring oscillator is the slowest, but becomes the fastest for V_{DD} higher than 500mV (super threshold region). In the near threshold region (300mV - 500mV) the FinFETs ring oscillator is still slower than the AlGaSb/InAs and GaSb/InAs TFETs;
- For V_{DD} higher than 250mV the FinFETs ring oscillator is the circuit with the greatest power consumption;
- For V_{DD} lower than 600mV the FinFETs is the device with the worst trade-off between speed and power consumption;

- The power-delay factor for the TFETs ring oscillators is pratically not affected by the temperature sweep. The FinFETs dynamic parameters are still weakly influenced by temperature but for low values of V_{DD} can be observed a significant variation of the power-delay factor.

4.5.2 11-staged Ring Oscillators static consumption

In this section the static power consumptions of the simulated 11-staged ring oscillators are compared.

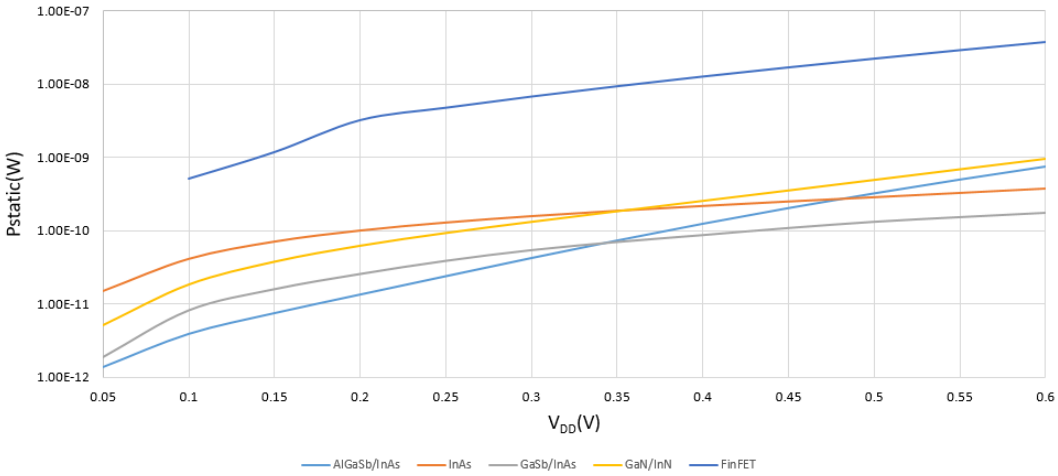

Figura 4.24: Comparison between the 11-staged ring oscillators static consumption for the several technologies used, at 27°C.

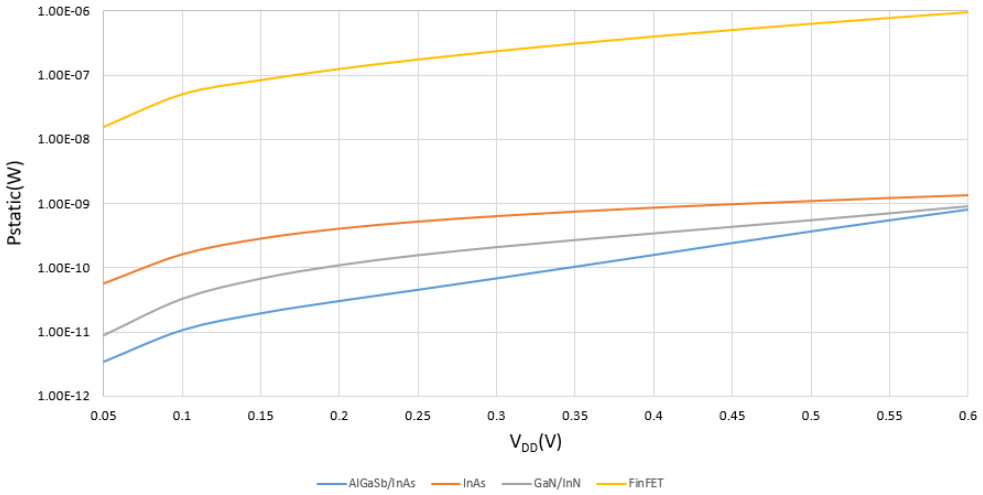

Figura 4.25: Comparison between the 11-staged ring oscillators static consumption for the several technologies used, at 125°C.

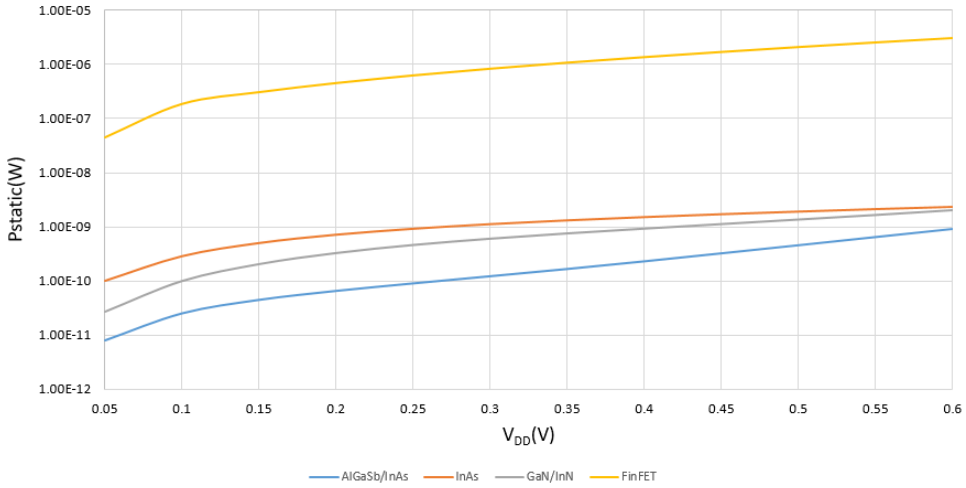

Figura 4.26: Comparison between the 11-staged ring oscillators static consumption for the several technologies used, at 175°C.

From Fig.4.24, Fig.4.25 and Fig.4.26 it is possible to see that the TFETs static consumption is, more or less, 50 times lower that the FinFETs one. For a temperature of 175°C the FinFETs power consumption becomes more than 1000 times greater than the TFETs one. The TFETs static power consumption remains pratically the same despite the rising of the temperature.

4.6 Performances for 15-staged ring oscillators

In this section the results obtained simulating the 15-staged oscillators composed by FinFETs, and the results obtained simulating the 15-staged oscillators composed by TFETs, are compared.

4.6.1 15-staged Ring Oscillators Dynamic parameters

In this part the dynamic parameters of the simulated 15-staged ring oscillators are compared. In addition to frequency and dynamic power also the power-delay product has been evaluated. This factor shows the trade-off between speed and power consumption, so the lower is this factor, the better will be the circuit.

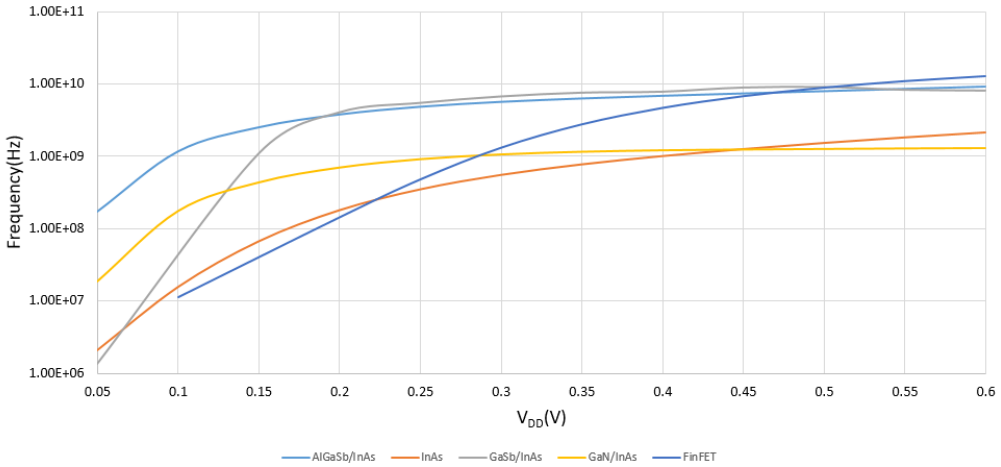

Figura 4.27: Comparison between the 15-staged ring oscillators frequencies for the several technologies used, at 27°C.

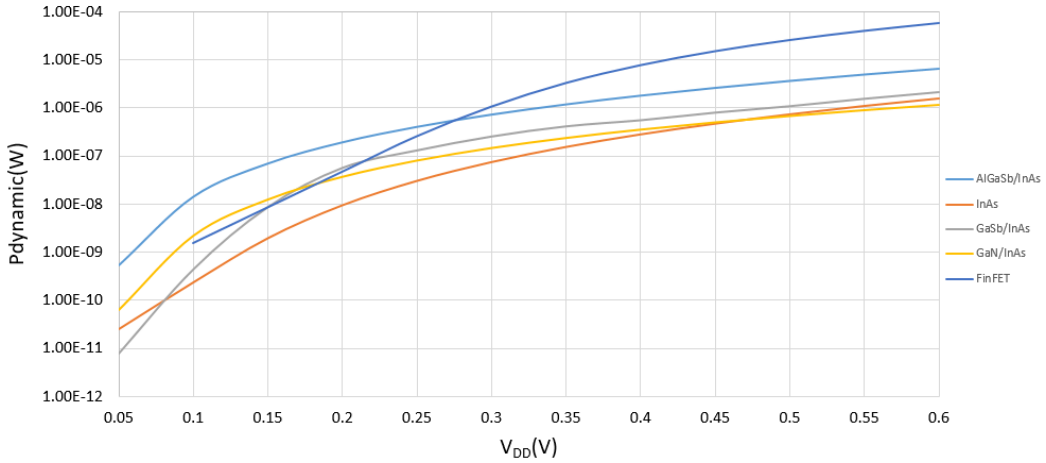

Figura 4.28: Comparison between the 15-staged ring oscillators dynamic consumption for the several technologies used, at 27°C.

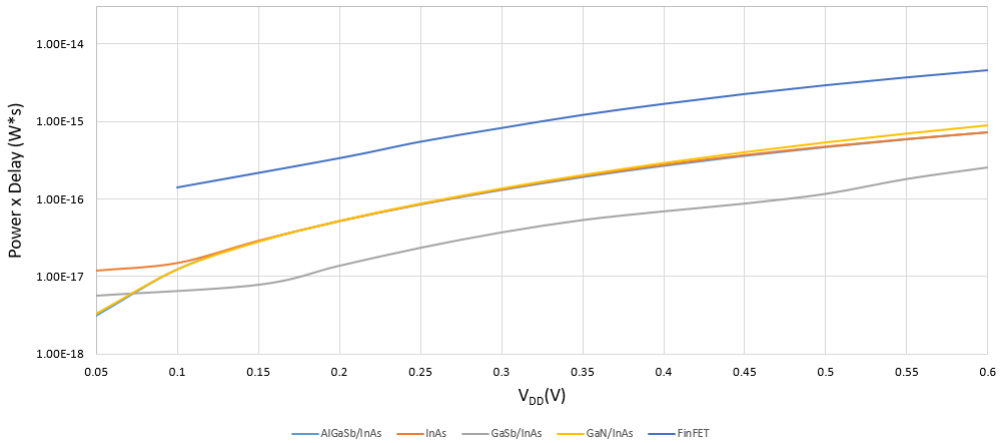

Figura 4.29: Comparison between the 15-staged ring oscillators power-delay factor for the several technologies used, at 27°C.

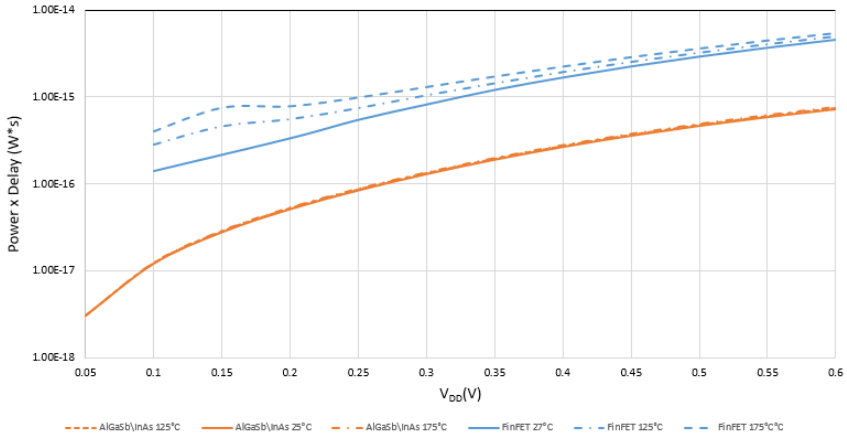

Figura 4.30: Comparison between the 15-staged ring oscillators power-delay factor for the FinFETs and AlGaSb/InAs technologies used, at 27°C, 125°C and 175°C.

From Fig.4.27, Fig.4.28, Fig.4.15 and Fig.4.30 it is possible to see that:

- For V_{DD} lower than 250mV (Subthreshold Region) the FinFETs ring oscillator is the slowest, but becomes the fastest for V_{DD} higher than 500mV (super threshold region). In the near threshold region (300mV - 500mV) the FinFETs ring oscillator is still slower than the AlGaSb/InAs and GaSb/InAs TFETs;
- For V_{DD} higher than 250mV the FinFETs ring oscillator is the circuit with the greatest power consumption;
- For V_{DD} lower than 600mV the FinFETs is the device with the worst trade-off between speed and power consumption;

- The power-delay factor for the TFETs ring oscillators is pratically not affected by the temperature sweep. The FinFETs dynamic parameters are still weakly influenced by temperature but for low values of V_{DD} can be observed a significant variation of the power-delay factor.

4.6.2 15-staged Ring Oscillators static consumption

In this section the static power consumptions of the simulated 15-staged ring oscillators are compared.

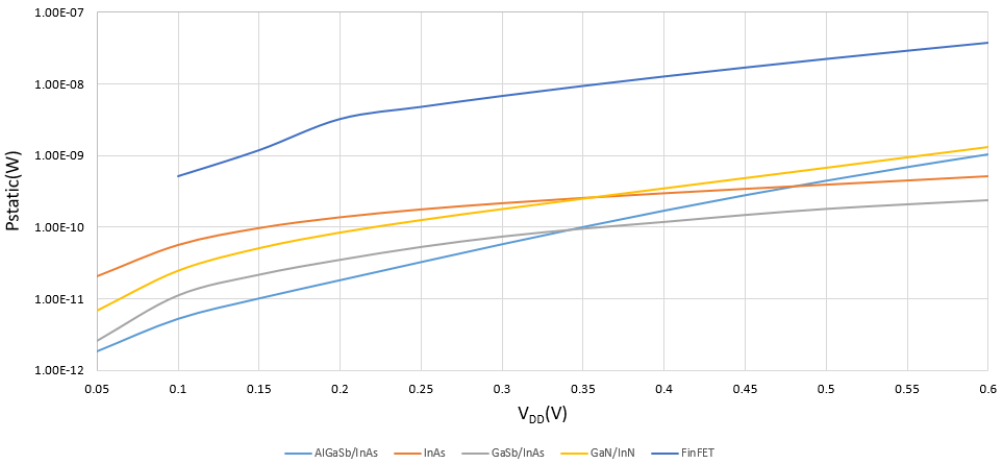

Figura 4.31: Comparison between the 15-staged ring oscillators static consumption for the several technologies used, at 27°C.

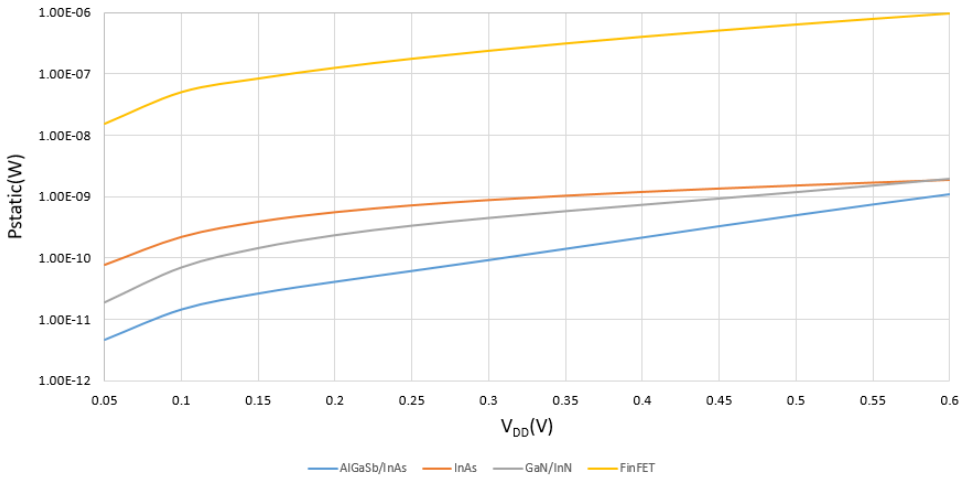

Figura 4.32: Comparison between the 15-staged ring oscillators static consumption for the several technologies used, at 125°C.

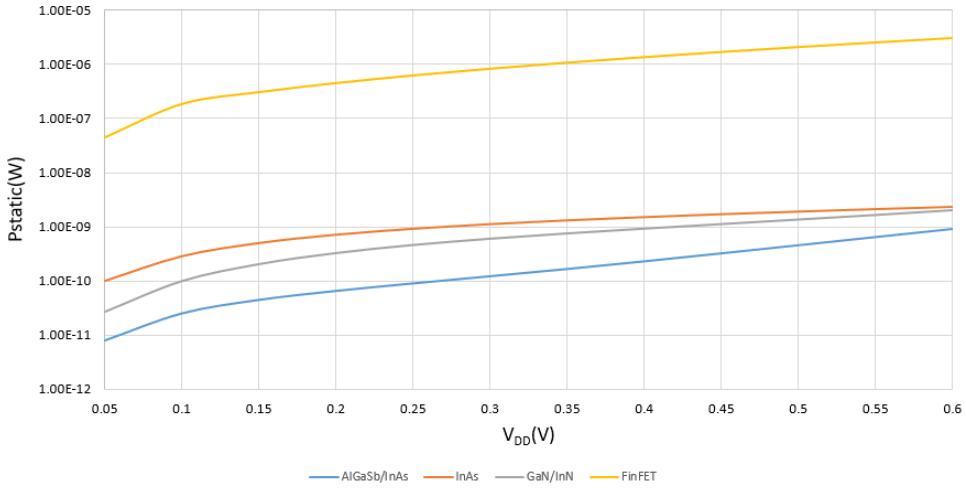

Figura 4.33: Comparison between the 11-staged ring oscillators static consumption for the several technologies used, at 175°C.

From Fig.4.31, Fig.4.32 and Fig.4.33 it is possible to see that the TFETs static consumption is, more or less, 50 times lower that the FinFETs one. For a temperature of 175°C the FinFETs power consumption becomes around 5000 times greater than the TFETs one. The TFETs power consumption remains pratically the same despite the rising of the temperature.

4.7 Results summary

The simulations carried out on different-staged ring oscillators demonstrate that:

- The FinFETs ring oscillators cannot work properly for $V_{DD} < 100mV$ due to the high V_{TH} of these devices;
- In subthreshold region the TFETs ring oscillators are faster and with a less power consumption respect to FinFETs ring oscillators;
- In near-threshold region the GaSb/InAs and AlGaSb/InAs TFETs ring oscillators are still faster than the FinFET ones;
- The TFETs circuit performances seem to be not affected by the temperature;

Another important point is the concept of stability in response to process variations.

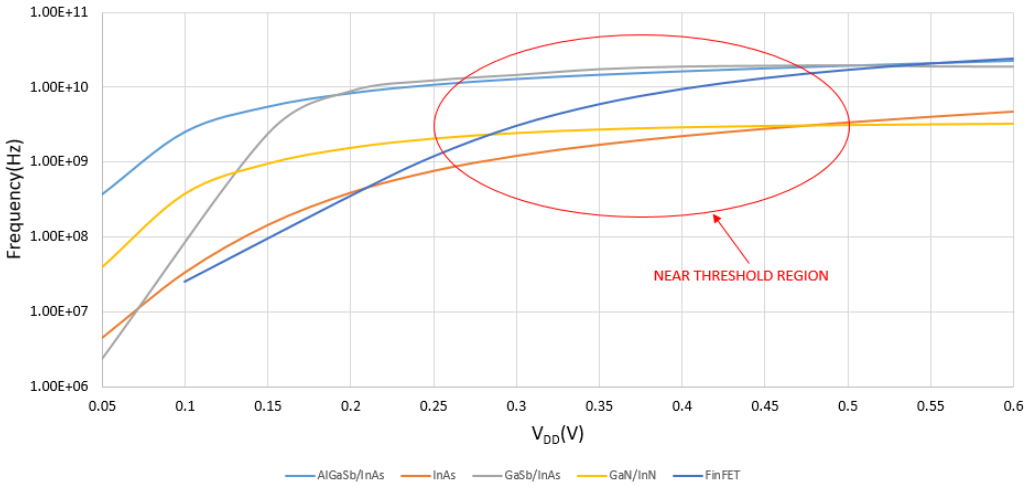

Figura 4.34: The frequency characteristic slopes in near-threshold region is much lower for TFETs-based ring oscillators respect to the FinFETs-based ring oscillators.

From Fig.4.34 it can be observed that the frequency characteristics in near-threshold regime for TFETs ring oscillators have a slope that is near to zero (flat characteristic) while the frequency characteristic for FinFETs ring oscillator is considerably greater than zero in that region. This means that process variations have a greater impact on the performances of the FinFETs ring oscillators, therefore the TFETs ring oscillators have a much more stable behaviour.

CHAPTER 5

Simulation of a TFETs SRAM cell

In this chapter it is shown the behaviour of the Tunneling FETs inside an SRAM cell. The Static Random Access Memories play a significant role in the modern technologies and continue to be a critical component across wide range of microelectronics applications [3]. While for ring oscillators the parameters can be reduced to the power-delay product and robustness to process variations, in a memory must be taken into account also the capacity to bear the electrical noise. During the last decade several alternate SRAM bitcell circuits and architectures have been proposed in order to overcome the power problems derived from transistor scaling, now it is time to investigate also how the development of this new kind of transistors can help the evolution of the memory systems [3] [45] [23] .

5.1 Cell Structures

In this section are shown two different architectural solutions for an SRAM cell, found in literature, both thought for low power purposes. One for the traditional CMOS devices and one for the Tunneling FETs. The unidirectional current conducting of TFETs, in fact, can be limiting for the traditional circuits, but it opens the way to new, maybe better, architectural solutions [3]. In order to have a fair comparison they have been chosen two "9-transistored" cells, but with different configurations [45] [23] .

5.1.1 9T SRAM cell for FinFETs

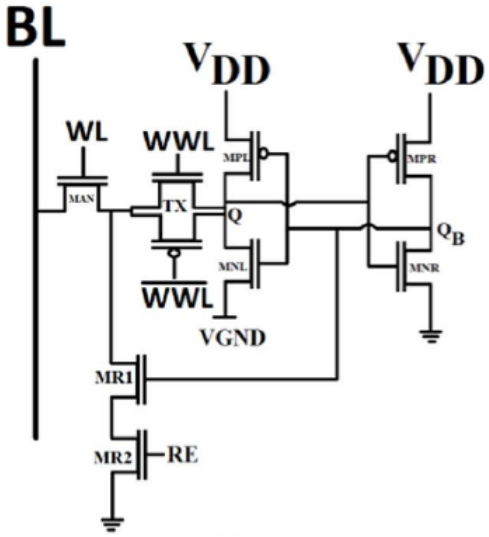

Figura 5.1: 9T single-bitline SRAM cell for FinFETs [45] .

The 9T single bit-line SRAM cell shown in 5.1 consists of:

- a "4-transistored" core, composed by two pull-up p-type transistors (MPL and MPR) and two pull-down n-type transistors (MNL and MNR), that contains the data;
- a writing path, consisting in the pass transistor MAN, controlled by Word-Line (WL) signal, and the transmission gate TX controlled by the Write-Word-Line signal (WWL);
- a reading path, composed by the transistors MAN, MR1, controlled by the stored signal QB, and MR2 controlled by the Read-Enable signal RE.

The signals status, for each operation, is summarized in the following table:

Signal	Write 1	Write 0	Read	Hold
BL	VDD	GND	Pre	VDD
WL	VDD	VDD	VDD	GND
WWL	VDD	VDD	GND	GND
RE	GND	GND	VDD	GND
VGND	float	float	GND	GND

The VGND signal is kept floating during the 0 and 1 WRITING operations in order to weaken the output node. In HOLD mode both WL and WWL are disabled, MR2

is off and VGND is kept at ground. The cross-coupled inverters isolated from bitline help in retaining the information [45] . In the READ mode, the bit-line is precharged to VDD, WL and RE are enabled, WWL is disabled and VGND is connected to GND. If the cell stores a 0, QB turns-on MR1 creating a discharging path for 'BL' through the transistors MAN, MR1 and MR2. The disabled transmission gate (TX) guarantees the isolation of Q and QB from BL during the read access, in order not to have destructive read operations. If the data stored is '1', the transistor MR1 is turned-off and BL does not have any path to GND, and the signal on BL remains VDD. Because of the usage of transmission gate for decoupling storage nodes (Q and QB) from BL, there is no sizing conflict between Read and Write operations. This enables independent selection of pull-up ratio and pull-down ratio according to the requirements for write operation [45] . So for each transistor it has been used an HFIN of 60 nm and NFIN=10. However, during the simulations, it was found that the '0' writing operation was not successfull with NFIN=10 for the pass transistor MAN 5.2 . So the simulations have been carried out with HFIN=60nm and NFIN=10 for all transistors except MAN, and HFIN=60nm and NFIN=30 for MAN.

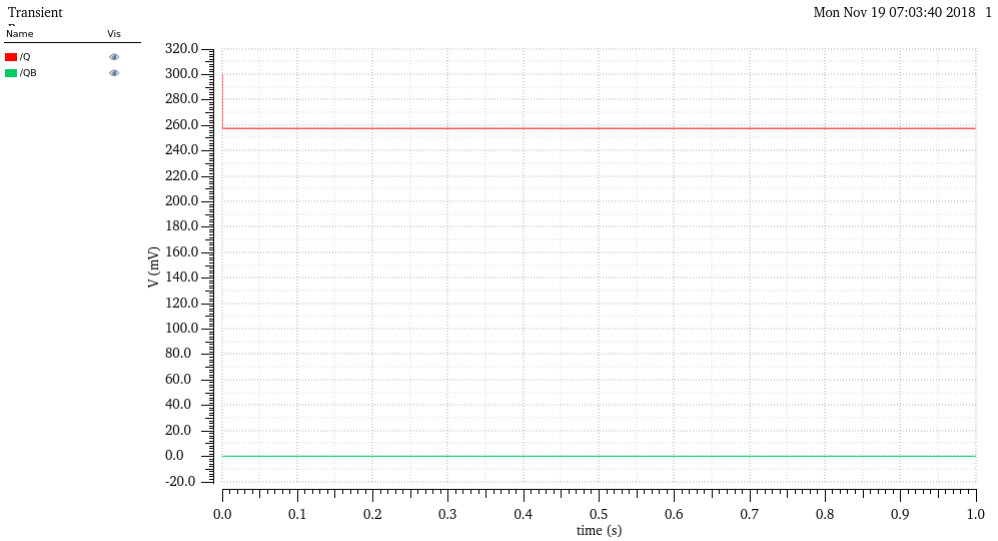

Figura 5.2: Fail in write '0' operation for NFIN=10 for the pass-transistor MAN.

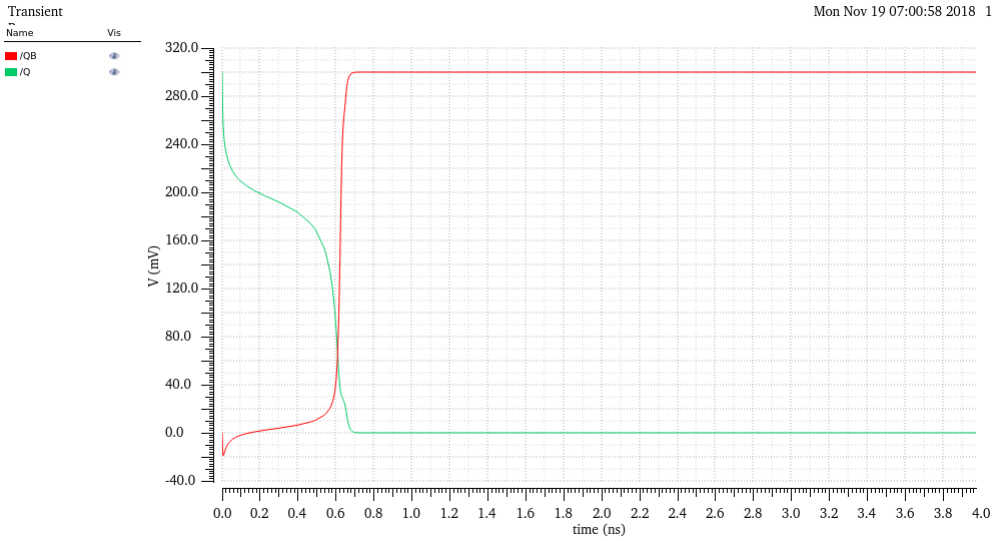

Figura 5.3: Success in write '0' operation for NFIN=30 for the pass-transistor MAN.

5.1.2 9T SRAM cell for TFETs

The design of this ultra-low power SRAM is thought for Internet of Thing (IoT) sensor nodes [23] .

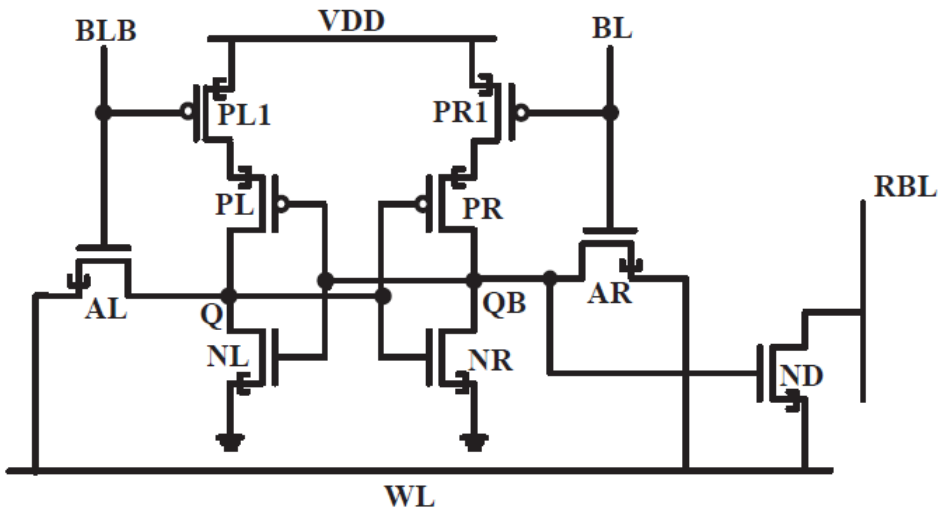

Figura 5.4: 9T SRAM robust cell for TFETs [23] .

The 9T TFETs-based SRAM bit cell shown in 5.4 consists of:

- A "6-transistored" core with 2 pull-down n-type transistors, NL and NR, and 4 pull-up p-type transistors, PL, PL1, PR, PR1. PL and PR are the real pull-up

transistors while PL1 and PR1 are used to disconnect the storage nodes from VDD so to speed up the write operations;

- Two n-type pass transistors, AR and AL, controlled by the two opposite bit-line signals BL and BLB, used to discharge Q and QB through the Write Line (WL);
- an n-type pass transistor, ND, controlled by QB, used to discharge the Read Bit Line (RBL) through the Write Line during the read operations;

The signals status, for each operation, is summarized in the following table:

Signal	Write 1	Write 0	Read	Hold
BL	VDD	GND	GND	GND
BLB	GND	VDD	GND	GND
WL	GND	GND	GND	VDD
RBL	GND	GND	Pre	GND

In the WRITE '0' operation BLB is '1', so enables AL and disables PL1. Q is disconnected from the power supply and can be easily discharged by the Write Line through AL. In the WRITE '1' operation BL is '1', so enables AR and disables PR1. QB is disconnected from the power supply and can be easily discharged through by the Write Line through AR. Actually the two write operations are both two '0' write operations [23] . During the READ mode RBL is precharged to VDD. If the data stored is '0' QB is '1' and turns-on ND, so RBL is discharged by the Write Line. If the data stored is '1', QB is '0' and ND is off, so RBL remains to VDD. During the READ mode BL and BLB are both '0' in order to disconnect the core from the WL. During the HOLD mode, BLB and BL are both '0' and since the TFETs are asymmetric WL is put to VDD in order to "turn-off better" the two pass transistors, AR and AL [23] . This configuration works because the TFETs are unidirectional, otherwise during a READ operation the cells of the same column (of others rows),that would be in HOLD mode, could write '1' to the RBL by charging it with their Write Line [23] .

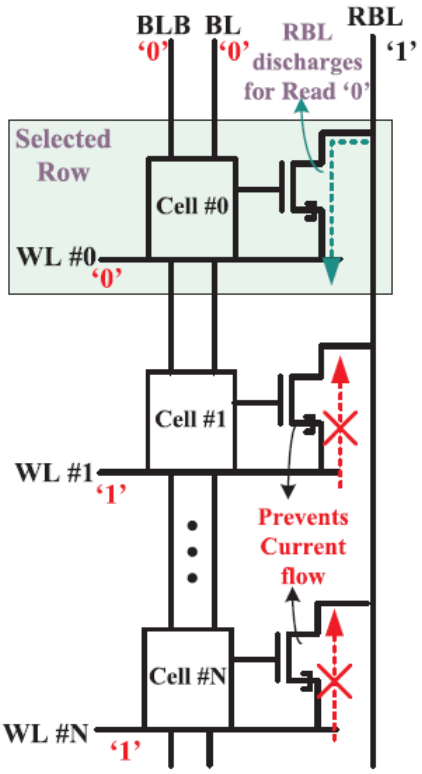

Figura 5.5: The importance of the unidirectional conducting of TFETs [23] .

The single bitline of the FinFET cell cannot be used since the TFETs based pass-transistors are unidirectional, so must be used two(or more) different bitlines to read and to write. For example, the classical 6T SRAM cell cannot work with the TFET technology [3] . The simulations for this cell have been carried out with W=30nm for the Hao Lu model based TFETs.

5.2 Simulation results

In this section are shown the results of the simulations, carried out with Spectre, for the several transistors taken into account.

5.2.1 Static Noise Margins

The best measure to quantify the stability of an SRAM bitcell during the read cycle and in hold state is the Static Noise Margin (SNM). The SNM is defined as the maximum amount of DC noise that can be tolerated by the cross-coupled inverter pair such that the

bitcell retains its data [46] [3] . Usually the bitcell stability during active operation (read cycle) represents a more significant limitation to SRAM operation than the hold state but in this case the cells analyzed have a separate buffer for the READ operation, so the read stability is the same of the hold stability [23] [45] .The read SNM is extracted from the read voltage transfer characteristics. The read VTC can be measured by sweeping the voltage at the data storage node Q (or QB) with both bitlines (BL, BLB) and wordline (WL) biased to GND while monitoring the node voltage at QB(or Q). Then from the Voltage Transfer Characteristic can be derived the Butterfly plot. Read stability of SRAM cells is commonly graphically estimated as the length of a side of the largest square that can be inscribed inside the smaller lobe of the butterfly curve [23] [45] [3] [47] [48] .

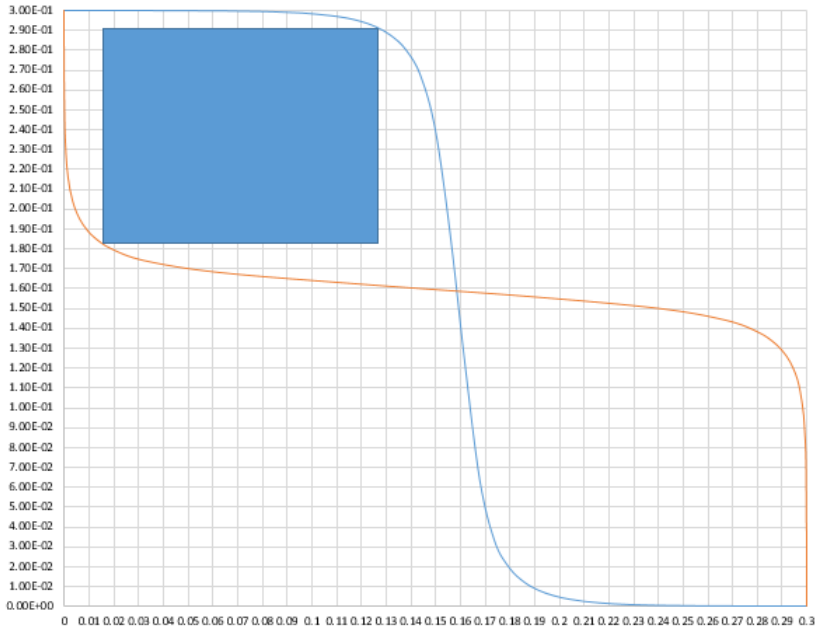

Figura 5.6: Graphical evaluation of the RSNM.

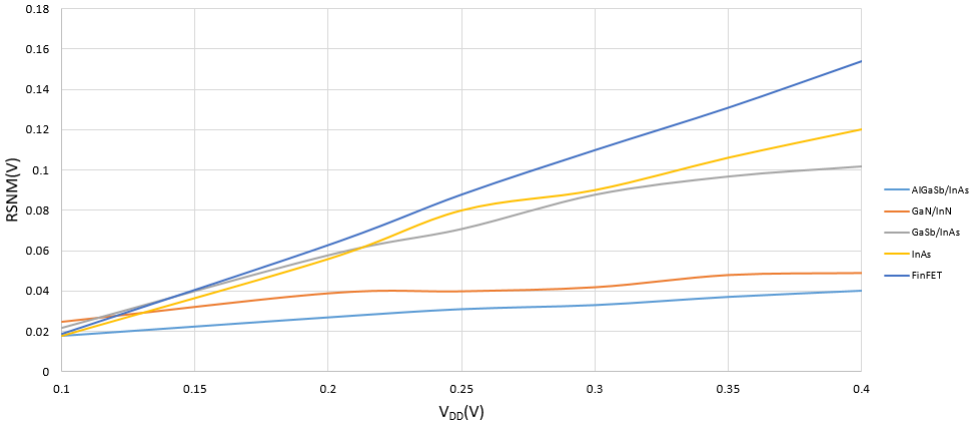

Figura 5.7: RSNM Comparison between the various analyzed technologies.

The write margin is defined as the minimum bit line voltage required to flip the state of an SRAM cell [48] . The write margin value and variation is a function of the cell design and process variation. The definition of write margin, however, is not very clear and depends also from the particular architecture of the cell, in fact, there are more than five different static approaches for measuring write margin [3] [48] . For the SRAM cells analyzed the write margins have been evaluated sweeping BL and monitoring Q and QB. The state of the cell is considered flipped when the derivative of the response of Q, or QB, reaches the value -1. The value of BL for the which $\frac{\partial Q(orQB)}{\partial BL} = -1$ has been taken as write margin.

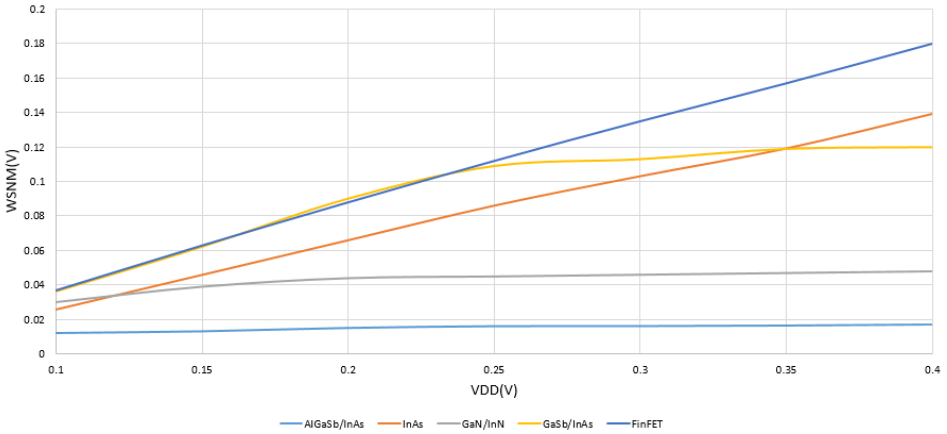

Figura 5.8: WSNM Comparison between the various analyzed technologies.

The static noise margins strongly depend on the voltage threshold. The device with greater V_{TH} demonstrated to have the greatest strenght to noise, while the AlGaSb/InAs

and GaN/InN TFETs (with a threshold lower than 100mV) have a WSNM lower than 100mV at $V_{DD} = 100mV$.

5.2.2 Hold Mode

During the HOLD mode the cells must mantain their data. Since there is no activity of the cells the power dissipated in this state is considered leakage. The SRAM leakage is the dominant factor in total power consumption in modern high performance microprocessors and SoCs, due to long standby time of majority of the cells. Therefore reducing SRAM leakage is a key element in the design of low power systems [49] [3]. The two considered SRAM cells are both designed in order to reduce the static power [23] [45] . The proposed TFET cell uses stacked transistors in pull-up path, which reduces the leakage in the cell core. The low leakage of the FinFETs SRAM cell is attributed to the single bit line operation and stacked transistors in the read/write path. The transistor stacking is helpful in reducing the static power dissipation since, putting more transistors between VDD and GND, the voltage drop on each transistor decreases [50] . The power leakage has been evaluated with a transient simulation monitoring the current and the voltage provided by the voltage supply. They are then multiplied and the product is averaged with the Virtuoso Calculator [44] .

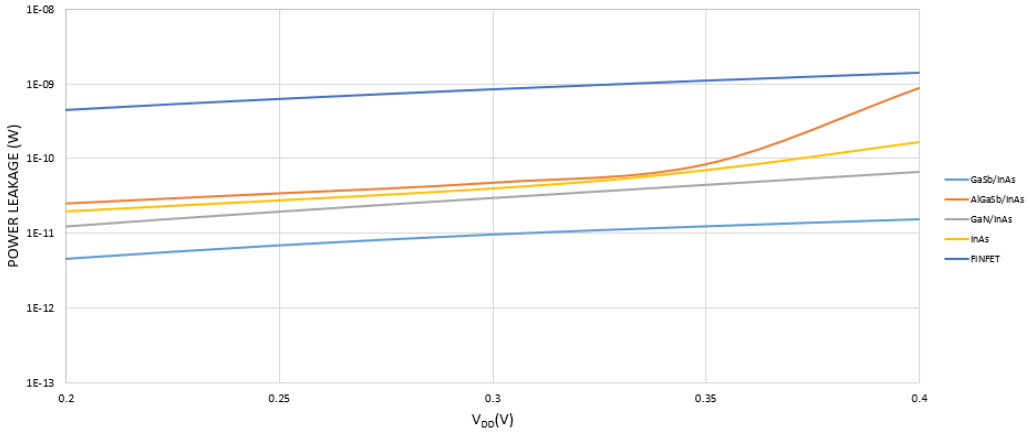

Figura 5.9: Comparison of the power leakages, varying VDD, for the analyzed technologies.

From Fig.5.9 it can be seen that the TFETs dissipate at lest ten times less than the FinFETs. The GaSb/InAs TFET has the lowest dissipation while the power leakage of the AlGaSb/InAs seems to raise very quickly after the 350mV.

5.2.3 Read Operation

The read delay is the time required to obtain a 100mV RBL voltage differences for a single-ended read cell [45] [23] . The read delay is evaluated with a transient simulation with RBL precharged to VDD and with an initial condition of Q=0 and QB=1. It is monitored the RBL signal (BL in the FinFETs SRAM configuration), the voltage and the current provided by the voltage supply. It is checked when the bit line signal decreased of 100mV then the product voltage x current (power) is integrated from '0' to 'read delay' to obtain the energy needed to complete a read operation [44] . In order to simulate the capacitive load that would be provided from other cells of the same column, in a SRAM matrix configuration, the simulations have been carried out with a capacitive load of 25fF [51] .

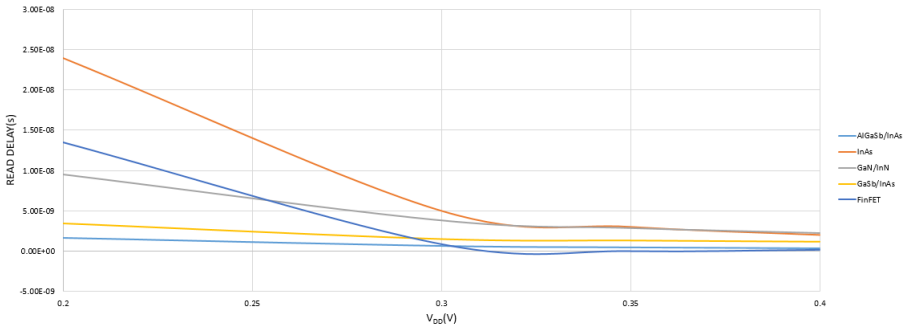

Figura 5.10: Comparison of the read delay, varying VDD, for the analyzed technologies.

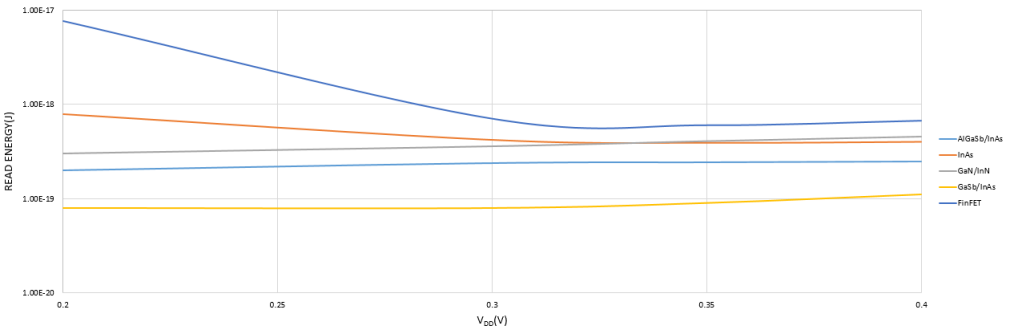

Figura 5.11: Comparison of the read energy, varying VDD, for the analyzed technologies.

From Fig.5.10 and Fig.5.11 it can be seen that in the sub-threshold region the TFETs cells are faster(except the InAs TFET) and spend less energy to complete a read operation. Over the 300mV(near-threshold region) the FinFETs cell becomes a bit faster and with an energy consumption higher but similar to that of TFETs.

5.2.4 Write Operation

For the TFETs cells the write access time is the time required to charge the '0' storing node to 90% of VDD, while for the FinFETs cell the write access time or write delay for writing '1' is estimated as the time duration between the WL activation time to the time when a '0' storing node charges up to 90% of VDD . Similarly, write access time for writing '0' is estimated as the time duration between the WL activation time to the time when a '1' storing node discharges to 10% of VDD [45] [23] . In fact, while for the TFETs cell the '0' and '1' write operation are pratically symmetrical for the FinFETs solution the difference between the two operations is significant. The write delay has been evaluated with a transient simulation with an initial condition for the which the cell contains the opposite data respect to that to be written. During the simulation Q, QB, the voltage and the current provided by the voltage supply are monitored. After the simulation it is checked the instant of time for the which the Q signal arrives to the 90% of VDD (or 10% in the write '0' operation) then the product voltage x current (power) is integrated from '0' to 'write delay' to obtain the energy needed to complete a write operation [44] .

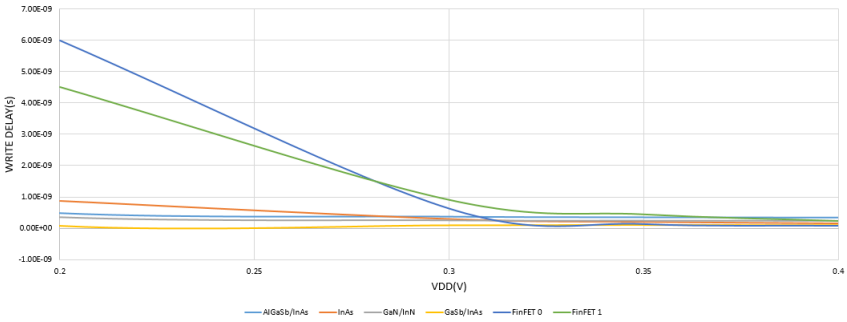

Figura 5.12: Comparison of the write delay, varying VDD, for the analyzed technologies.

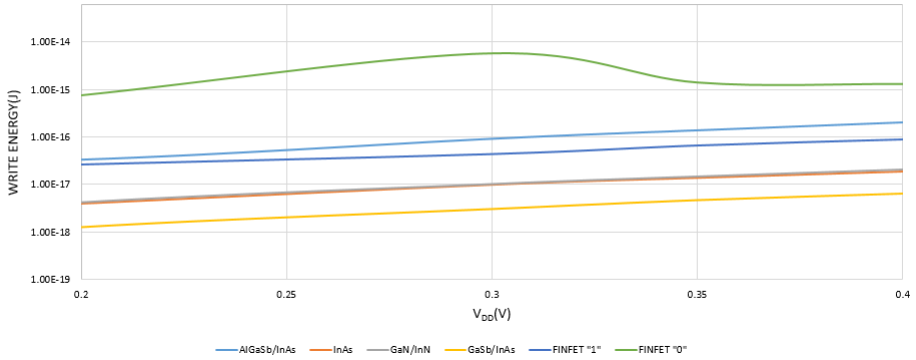

Figura 5.13: Comparison of the write energy, varying VDD, for the analyzed technologies.

From Fig.5.12 and Fig.5.13 in the sub-threshold region the TFETs cells are faster and spend less energy to complete a write operation. Only the AlGaSb/InAs TFETs cell spends more energy respect to the write '1' operation of the FinFETs cell. Over the 300mV(near-threshold region) the FinFETs cell becomes as fast as the TFETs ones and with an energy consumption at least ten times higher than that of TFETs.

5.3 Results summary

In the ring oscillators the low threshold guarantees high performance with low consumptions, but in the SRAM cells a low V_{TH} causes stability drawbacks. The AlGaSb/InAs TFET is the transistor that best performed into the ring oscillators while shows the worst behaviour inside an SRAM cell. Moreover, while in the ring oscillators the TFETs clearly have the best performances in every way, in the SRAMs the comparison is more balanced. The FinFETs cell shows a little bit more stability but has greater static and dynamic consumptions. In particular the remarkable lower power leakage of the TFETs cell can definitively tip the balance in favour of the TFETs solution, since the power leakage is the most important parameter to judge the goodness of an SRAM for a low power application.

CHAPTER 6

Conclusions

The work of thesis in mainly divided into two parts. In the first part is explained the principle of working of Tunnel FETs, is introduced the concept of Band To Band Tunneling, and its depence from the materials characteristics and temperature, and are analyzed their main electrical features. It is also explained the concept of subthreshold swing and its impact on the power consumptions. Then a brief comparison, between several devices, found in literature, has been done using Cadence Virtuoso running the model cards made available by the authors. The second part is focused on the TFETs behaviour not as a stand-alone device, but inside two essential electronic circuits as ring oscillators and SRAM cells, comparing their performances to those of a FinFETs. The simulation regarded not only the power consumption of these novel devices but also their speed and the trade-off between speed and consumptions. Moreover it has been carried out also a basic temperature analysis since the performance degrade due to the rise of temperature is a crucial problem in the electronic systems. The results obtained have been extremely satisfactory since for low voltage values (under the 500mV) the TFETs demonstrated better performances for power consumptions, strenght to process variations and also speed. However there is lot of work that must be done. The Hao Lu model is surely the most complete analytical model that can be found in literature, it is already a quiet complex model but it has not the complexity of a BSIM model. A lot of researches and studies must be done in order to complete the analytical models so to be able to do as realistic as possible circuit simulations of these devices. There are a lot of materials combinations, and geometrical solutions that must still be tried to enhance the

electrical characteristics of TFETs. The greatest problem regards the fact that it has been demonstrated that silicon TFETs have a too much low I_{ON}, so in a new TFETs world there would be no more place for silicon, and this would lead to a revolution in the semiconductor industry.

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