POLITECNICO DI TORINO

Development of protection systems for modular satellites

by

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A thesis for the
degree of Master of Science

in the
Department of Electronics and Telecommunications

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Declaration of Authorship

I, Yang yupeng , declare that I have done this thesis and the work by my own. I make a confirm that:

- I have done this work in the last year of master study in purpose of obtaining a degree at this University.
- I have stated if some parts of the thesis has been submitted by other institutions.
- I have made attribution whenever I consulted the published paper.
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"Keep what you say and carry out what you do."

Confucius

Abstract

The aim of this work is to develop a system for latch-up protection of digital CMOS components which also can auto-restart. The circuit shall comprise analyzing various techniques, including a current sensor, a threshold comparator, a switch in series with the load.

The idea is divided into three parts, the first part is that use a MOSFET driver lm5060 to realize the function of controlling switch using with MOSFET BSS119 to turn on or off within the threshold. The second part is to make the driver turn on automatically after the overcurrent happened and simulate all the circuit working. The last part is to design a PCB board, after reasonable layout, print it by a factory. Then, soldering and testing the whole design, until it can get a correct result.

In order to achieve these objectives, I use the Cadence 17.2 version which including Capture CIS for writing all the circuits, PSpice for simulating the circuit working and OrCAD PCB Designer for making PCB. Later, I should use some instruments to assemble and test the PCB.

Keywords: Latch-up, PCB, Current limit, Auto-restart.

Acknowledgements

I want to start with the feeling of appreciation to My supervisor, Prof. Leonardo Reyneri for his support and motivation throughout the course of this work. Without his help, my work and paper might not have been so smooth. He provided me with the opportunity to improve my technical skills and provided me with the resources to fulfill this task.

I am thankful to my parents and family and friends, who have always been a source of motivation for me in the endeavor of knowledge. Special thanks to my colleague Giorgio for helping me, in some ways, pointing and encouraging me.

Dedicated to my parents "Yang Hongwen" and "Wei Ling".

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Abbreviations

PCB	**P**rinted **C**ircuit **B**oard
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect**T**ransistor
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
IC	**I**ntegrated **C**ircuit
VLSI	**V**ery-**L**arge-**S**cale-**I**ntegration
ESD	**E**lectrostatic **D**ischarge
EOS	**E**lectronical **O**verload
STI	**S**hallow **T**rench **I**solation
SCR	**S**ilicon **C**ontrolled **R**ectifier
ZSR	**Z**ero **S**tate **R**esponse
ZIR	**Z**ero **I**put **R**esponse

Chapter 1

Introduction

1.1 Latch-up

CMOS integrated circuit is the most widely used technology in VLSI chip. The CMOS circuit uses a combination of p-and n-MOSFETS to implement logic gates and other digital circuits. Although CMOS has many advantages in circuit structure, it is not perfect.

1.1.1 Definition

A latch-up is a type of short circuit which can occur in an integrated circuit. It is a pnpn self-sustaining low impedance state, is inherent in standard bulk CMOS-integrated circuit structures[1]. More specifically, inadvertently created between power MOSFET circuits rail a low impedance path to trigger the parasitic structure, the normal function of the damaged parts, may even lead to it damaged by overcurrent.

1.1.2 Latch-up effect

The latch-up effect is generated by the n-p-n-p structure of the active region of the NMOS, the P-substrate, the N-well, and the PMOS active region. When one of the transistors is forward bias, a positive feedback latch is formed. Electrostatic discharge (ESD) is an invisible destructive force that affects electronic components. ESD and

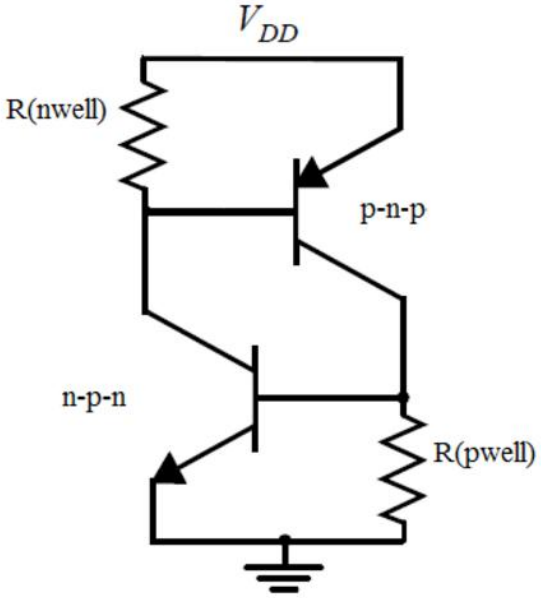

FIGURE 1.1: equivalent circuit of CMOS latch-up

related voltage transients all cause latch-up, one of the major causes of semiconductor device failure. If a strong electric field is applied to the oxide film in the device structure, the oxide film will be damaged by dielectric breakdown. Very thin metal traces are damaged by high currents and can form an open circuit due to overheating caused by inrush currents. This is the so-called latch-up effect. The equivalent circuit of CMOS latch-up is showing in figure 1.1

1.1.3 Latch-up prevention

In the case of latch-up, the device creates a short between the power supply and ground, causing high currents, EOS (electrical overload) and device damage, it will seriously affect the function of the circuit, resulting in the circuit doesn't work or burn. So how to prevent the latch-up occurring is much more important in the layout designing now.

The technology to implement it is divided into two areas: layout guidelines and process design. The first is closely related to any CMOS technology and is of interest to device and circuit designers. The second involves process engineers integrating CMOS processes into process characteristics.

- Layout level anti-latch-up:

1. Bold power lines and ground lines, reasonable layout power contact holes, reducing the lateral current density and series resistance, like bypass resistance.
2. Increase base width to minimize current gain as much as possible, like keeping NMOS as close as possible to GND, PMOS as close as possible to VDD, and keep enough distance between PMOS and NMOS.
3. Operate CMOS gates from relatively high impedance or low capacity supplies. This reduces the gate current which can flow and can prevent latch-up through the protection array[1].
4. Add guarding ring for minority carrier. In the N-well, the N+ ring rounding the NMOS and connect VDD, the P+ ring rounding PMOS and connect GND. This way can collect minority carriers in advance , reduce the gain of the lateral transistor PNP, so that reducing the latch-up effect. Showing in the figure 1.2.

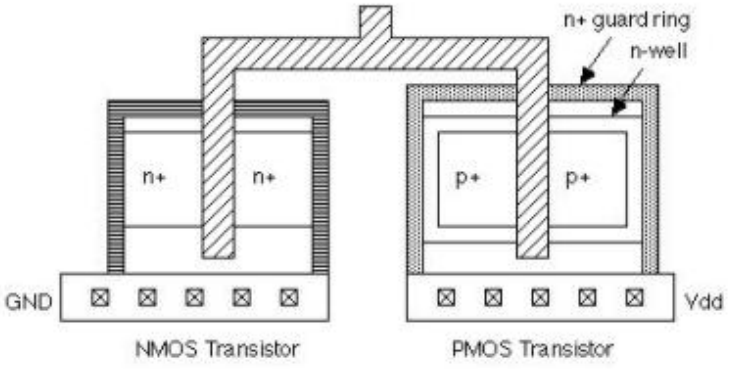

FIGURE 1.2: N+ ring rounding the NMOS and connect VDD

- Process level anti-latch-up:

1. Reducing the minority carrier lifetime can reduce the parasitic bipolar transistor current gain. Generally, we use doping with gold or neutron radiation technology, but this method is not easy to control and can also lead to increased leakage current.
2. Use the way of high-energy ion injection to make the impurities go to the bottom, which unlike the normal well that the well surface has the highest concentration and the lowest concentration at the bottom, that called Retrograded well. So that when the electron or hole arrive at the base, the high

concentration of deep wells can effectively increase the composite, do not want to go to the collector, and can reduce the gain of bipolar, so will not happen the reverse bias and will not cause the latch-up.

3. Latches can also be escaped by the trench isolation structure. In this technique, etching out a trench deeper than the well, and the thermal oxide layer is then grown on the bottom and sidewalls of the trench, and polysilicon or silicon dioxide is then deposited to fill the trench. Because n-channel and p-channel MOSFETs are separated by trenches, this approach eliminates latch-up.

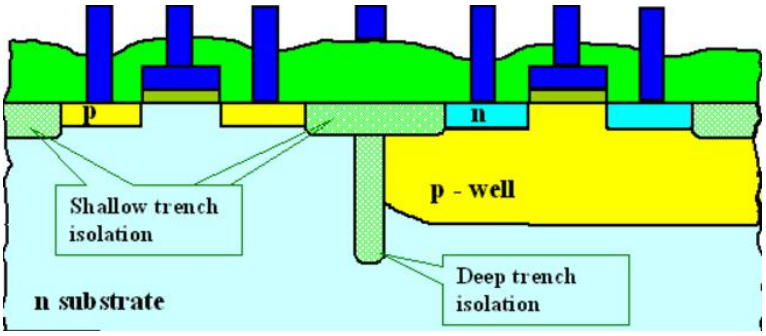

FIGURE 1.3: shallow trench isolation

Most of the use are STI, it is generally used on CMOS process technology nodes of 250 nanometers and smaller. The most important steps of the STI process involve etching a pattern of trenches in the silicon, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches. Showing in the figure 1.3.

- Circuit level anti-latch-up:

1. Pay attention to the power beating: To prevent the inductive component of the reverse induced electromotive force or grid noise fleeing into the CMOS circuit, causing instantaneous breakdown of the CMOS circuit to trigger the latch-up effect.
2. Current limit: CMOS is very low power consumption, so in the design of CMOS system power supply, the system actually needs how much current and we supply it how much, the power output current capacity not too big. We can know from the SCR, if the supply current is less than the holding

current of SCR, then even if it has the opportunities to trigger the latch-up but still cannot hold it. So, we can limit the current to prevent the latch-up. The pulse widths can be chosen from a range of values but most often in the industry, 2 ms to 10 ms is preferred. The current pulse height typical values are 100 mA while the over-voltage is 1.5 * $V_{\max}$ (operating).

1.2 Design contents

As we can see from the above discussion, layout level, and process level anti-latch-up due to the demanding technology and the cost of consumption, we can hardly achieve it in our laboratory with limited equipment, so my design will start at the circuit level.

1.2.1 Design flow

From the circuit level, I use the part of the current limit to make an overcurrent protection circuit with a limited current 10mA. When overcurrent occurs in the protected circuit, my design can detect current changes and cut off the current and then automatically restart after a certain period of time.

In this figure 1.4, we can see all the steps of my design. The design is divided into two parts. The first part is the circuit design. Draw the circuit schematic, and gradually correct the circuit through the simulation results, and finally get the final circuit.

The second part is the PCB design. Through the circuit diagram obtained in the previous step, a new PCB project is created. After a series of work such as placing, routing...A complete PCB layout is obtained, and then finish the PCB manufacture things such as creating NC drill and Gerber files, and finally sent them to the factory for printing. After get the PCB board, soldering with all components and testing work is performed(the detailed PCB production steps, we will see in Chapter 5). After everything has been successfully completed, the entire design has been finished.

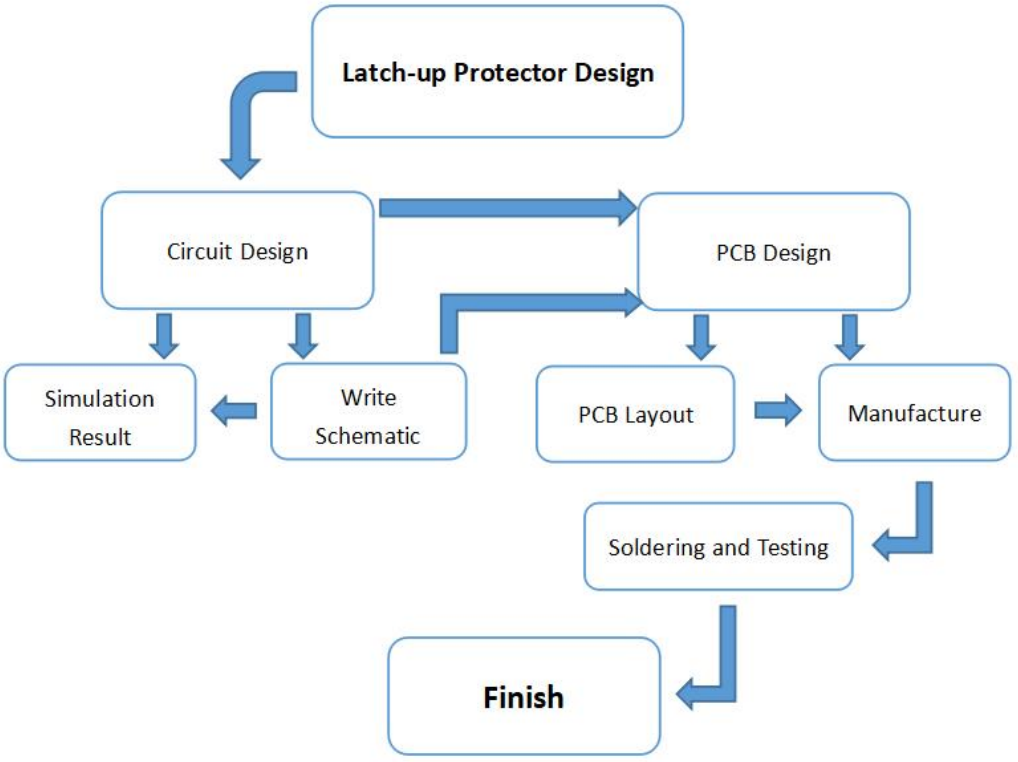

FIGURE 1.4: design flow graph

1.2.2 Design technology

For the above steps what I need to do, required some technology supporting. In this case, I used everything that I need from Cadence 17.2.

Using the OrCAD Capture CIS to write the circuit schematic, using the PSpice simulation manager to get the simulating results so that perfect my schematics step by step. Finally, using the OrCAD PCB Designer to make my PCB is able to print it out, then do the soldering and testing of some instruments such as Pick and Place machine, Reflow Oven, Power Generator, Signal Generator, Oscilloscope, and so on.

1.3 Thesis Organization

- In Chapter 2, introduce the main steps of designing PCB.
- In Chapter 3, comparing the design I already got with the methods I have found, see the simulation results, and select which one to use.

- In Chapter 4, in order to implement the automatic restart function, new circuits are designed and added in existing circuits. There are two methods for comparison and choice.
- In Chapter 5, produce my own PCB board with the detail steps.
- In Chapter 6, assemble all the devices to obtain the final designed PCB, test the board, and see it work or not.
- In Chapter 7, conclusion and future work.

Chapter 2

PCB Design Technology

2.1 Production process

Before entering the factory to print PCB, we need to create a PCB project by drawing the circuit schematic and testing the simulation results. Next, I will outline the process from circuit schematics to PCB fabrication.

2.1.1 From Schematic to PCB project

First, I will talk about how can we transfer a PCB project from a circuit schematic project. Steps showing as follows:

1. Get the principle circuit schematic ready

   According to different designs, draw different circuit schematics. By observing the results of the circuit simulation, we get the circuit functions we want to achieve. Finally, determine the circuit schematic. To prepare for making PCBs.

2. Add footprints

   To get PCB layout, we need to add each component with their own footprint. For example, if we want to use the resistor with package 0603, we should insert the footprint into a resistor in the schematic version, so that we can lay out the resistor in the PCB version. About getting the symbols of footprints, we can search on the

website or write by ourselves. And make sure to use a different file type depending on using different PCB design tools.

3. Create netlist

   The netlist can use the same part of the circuit as a group. When the network table is generated, it can be imported into the PCB. This can make it easier to place components in the PCB. The group number information will be arranged in the schematic and imported into the Layout.

   After finish drawing the schematic part, perform a DRC check of the schematic and see if your design complies with the design rules. If there are no errors, perform annotate and label the component by software braking, and specify the PCB package for each component. After the steps shown above, we create the netlist. Do not close the schematic project for communication between the schematic and the PCB diagram.

2.1.2 PCB design flow

These three steps above are the preparations for the transition from the schematic to the PCB diagram. Next, I will describe the specific process of drawing the PCB and how to making it available from the factory. Showing as figure 2.1.

1. Create a PCB project

   As I use the Cadence17.2, when I select create the netlist from the 'Tools' bar, in that edict part, I can choose create PCB directly, it depends.

2. Set design parameters

   According to the design requirements, to set the design and constraint parameters. You can first select the unit for drawing, that is, use mil, mm or other, this according to personal habits, generally choose mil, but I prefer mm, next is to select the drawing size. The third option is to select the coordinate origin of the drawing. You can select the center as the origin of the coordinates. This depends on the requirements. After these settings we go to set the constraints like the Minimum Line width, the Minimum Line to Line spacing, the Minimum Line to Pad spacing, and the Minimum Pad to Pad spacing, the size of them are depending on your own design, but normally set the constraints, size in 8 mils,

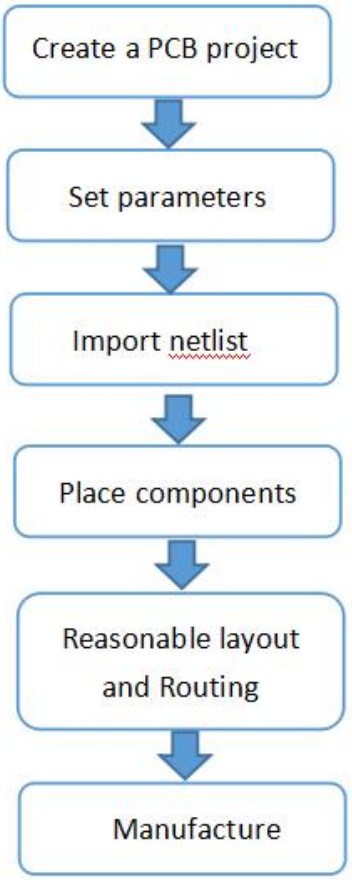

FIGURE 2.1: design flow

but as the policy of ”3W”, it is better to set the Minimum Line to Line spacing size is three times of line width. After all select the PCB shape rectangular board, the main set is the board width and height and some restrictions, including the wiring allowable area and the board frame the distance and the distance between the allowable component area and the board frame. After these, we finish the setting part.

3. Import netlist

   Import the netlist into the PCB can make it easier to place components in the PCB.

4. Place components

   Looking for the label ”Placing”, and place all the components. Depending on the tools, we can choose place quickly or place them one by one.

5. Reasonable layout and routing

   This step is the main part of PCB design. After all the components are placed, we can remove all the flying lines and arrange the components reasonably. We can rotate and mirror the components according to our demands. After placing, routing all the flying lines, and use the Add Via command to add vias at any time during routing, allowing the routing to travel between the top and bottom layers. If we found there are too many lines, we can also add planes for ground or VCC or any others.

6. Manufacture

   To print the board, we need to provide Gerber files to PCB manufacturers. Before making Gerber files, you must also do some necessary inspections, such as whether the package has any mistakes, whether there are unconnected networks, etc.. If you do not carefully test, you will most likely be tearful. In addition, if On-line DRC is turned on (in the rule constraint, the default is open), it also needs to pay special attention to where the DRC appears but if necessary, change it. After everything is correct, you can lay copper on the PCB. You can set parameters for copper paving before laying the copper. Click the menu Shape–Global Dynamic Params, select Smooth to smooth fill in the Dynamic fill option in the Shape fill tab, and open Void controls. In the Gerber file editor General Parameters tab, Device type select Gerber RS274X, Format Integer places: 3, Decimal places: 5, and then open the Film Control tab, add the required film, the general two-layer board, then you need TOP (top layer routing layer), BOTTOM (bottom trace layer), SOLDERMASK-TOP (top layer solder mask), SOLDERMASK-BOTTOM (bottom layer solder mask),SILK-TOP (top screen printing) and SILK-BOTTOM (bottom screen printing), OUTLINE of the board, after adding the required film file, set the Undefine line width to 8 mil(I do not know why this value), other settings use the default value, and finally click Create Artwork. After we get the Gerber file, we go to create the NC drill. Send these files we created in a package to the factory, go to print it out.

2.1.3 Assembly and Testing

The components are inserted into the printed circuit board according to the process requirements, such as vertical or horizontal installation, tight or non-tight installation. After the device is mounted, the heater is used to heat the PCB pads, device pins, and solder. The solder melts the pads and pins together. After all the devices have been assembled, clean the flux residue around the solder joint with absolute alcohol or banana water. Soldered and soldered areas need to be re-soldered and cleaned. Quality inspection after welding is very important for electronic products. It includes appearance inspection and electrical performance inspection.

By the end of assembly and testing, PCB's production is completed. Because according to different PCB design tools, the specific operation will be somewhat different. Next, in Chapter 5, I will describe the specific procedures I used to create a PCB by using Cadence 17.2.

2.2 Development

PCBs have evolved from single-layer to double-sided, multi-layered and flexible, and still maintain their own development trends. Due to the continuous development of high-precision, high-density, and high-reliability, and constantly reducing the size, cost, and performance, the printed boards still have a strong vitality in the future development of electronic devices.

Chapter 3

The Comparison of Components and Simulation

In this chapter, I will introduce the component needed for the existing design and the components needed for my design ideas. And draw out the circuit principle of each design, after the simulation results, compare and select the component that we need to use in this design.

3.1 Components

The electronic components are the core of the entire design. The design of the circuit and the results we want from the circuit depend entirely on the functions of the electronic components used. When designing a circuit, we first need to come up with ideas and then selecting the components, that is the most important step in the design. It can also be said that the beginning of the overall design starts with the determination of the components. Next, I will introduce the 1B127 that the existing design needs, and the TPS22945, FPF2700, and LM5060 that the ideas what I thought to need.

3.1.1 1B127

The 1B127 is a latch-up and overcurrent protection system suited for high radiation level environments, such as LowEarth Orbit satellites.It allows the use of low cost devices

in radiation environments such as space applications, high-energy physics experiments and biomedical devices by protecting them from the effects of latch-up. The system monitors the current flowing through the external sense resistor (Rs) and the internal pass transistor turns off the load whenever the threshold is reached. After a user-defined recovery time, the PASS transistor automatically restarts power back to the load. Once the latch has disappeared, the device can also act as a current-limited load switch by sending a TTL signal to the OFF pin. For higher voltages or currents, external PMOS pass transistors can be used. Inrush current effects or short current spikes can be filtered out. Permissible surge charging and recovery times can be set using external capacitors, and in addition, when using load capacitors to program inrush currents, the slew rate when the load supply voltage is turned on can be limited. The device is available in a small 13x13mm plastic 100BGA package. Showing the block digram as following figure 3.1.

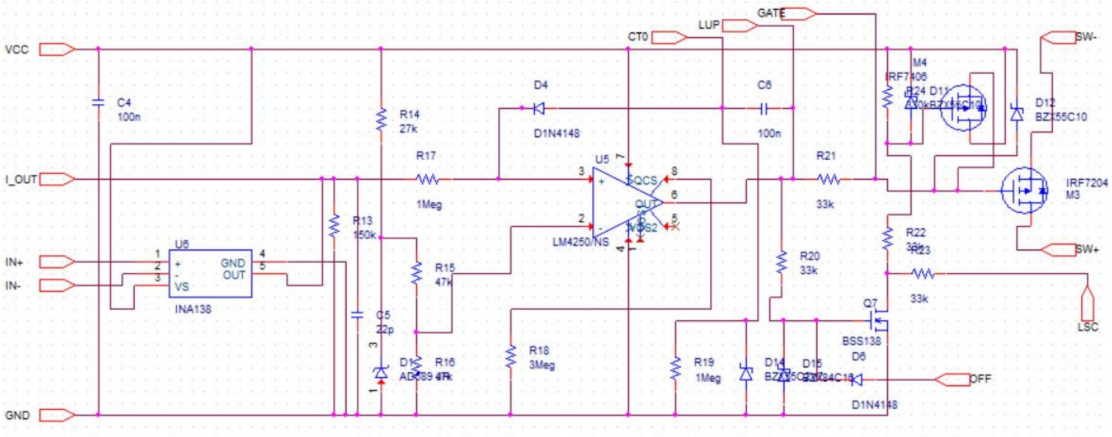

FIGURE 3.1: block diagram

3.1.1.1 Design with 1B127

It allows using low-cost devices in radiation environments like space applications, high-energy physics experiments and biomedical equipment, by protecting them against the effects of latch-up. The system monitors the current flowing through an external sense resistor $R_{\mathrm{s}}$and whenever a threshold value is reached the internal pass transistor switches off the load. After a user-defined recovery time, the pass transistor automatically turns on again restoring power supply to the load, once the latch-up has faded away. As I read the datasheet of 1B127, I can clearly understand the basic design principle of the

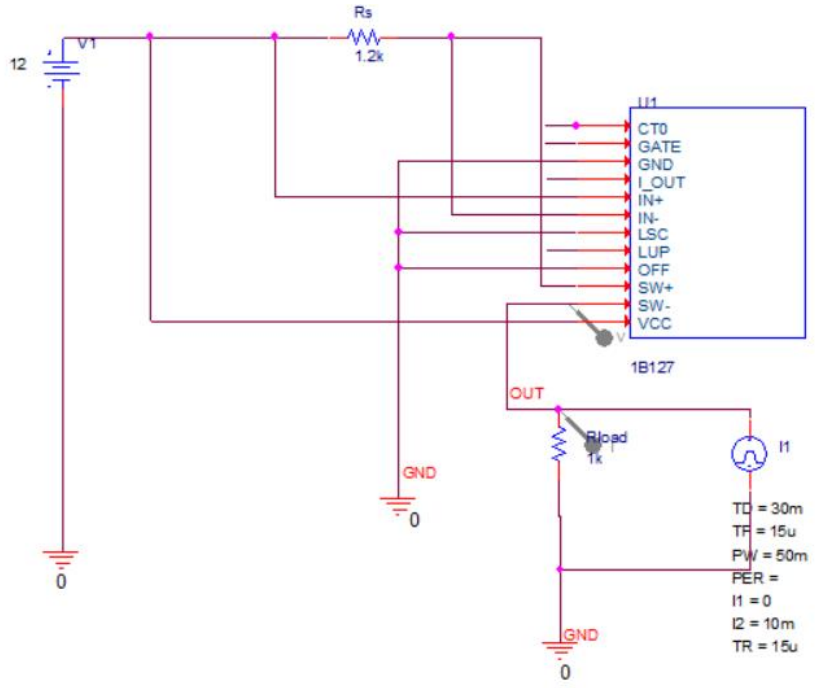

FIGURE 3.2: design with 1B127

1B127. The circuit schematic is showing in the figure 3.2. The SW- pin is connected with the external R_{load}, so this the output I want to detect. The current generator supplies current to make fault happen, which just holding for 50ms.

3.1.1.2 Simulation Result

First, we see the simulation result of 1B127 in figure 3.3. I set the one current generator next to the load, and start to work after 30ms, so that we can see the voltage of load go down, and after probably 50ms and auto-restart. Because I just use basic way to simulate and don't add any other external capacitors or resistors, so it just performs originally.

3.1.2 TPS22945

It is a Low-input-voltage Current-limited Load Switches With Shut Off And Auto-Restart Feature. The TPS22945 load switch protects the system and load under high current conditions. The device includes an 0.4Ω current-limited P-channel MOSFET whose input voltage of operation is from 1.62V to 5.5v. When the MOSFET is controlled by the ON / OFF input (ON), it prevents the current from flowing and can be

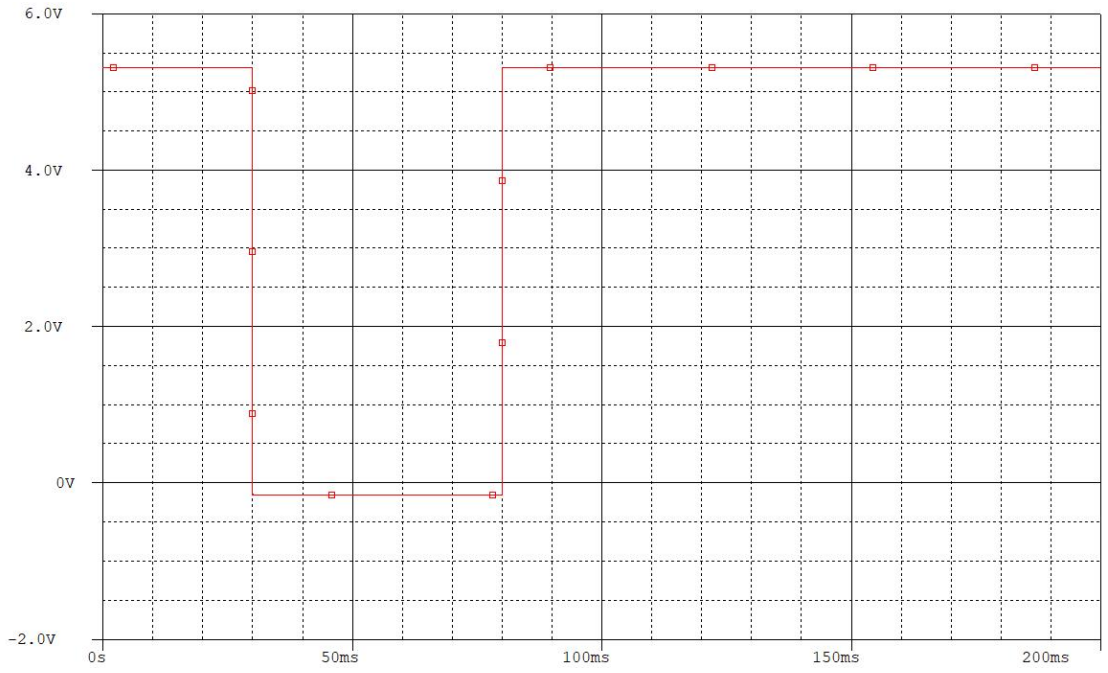

FIGURE 3.3: the voltage wave of R_{load}

directly connected to the low voltage control signal. Fail-safe protection prevents equipment overheating damage by turning off the switch when a continuous over-current condition happens. It can also auto restart in a fixed time 80ms and the minimum current limit is also a fixed value 100mA. The top view following with figure 3.4.

We can see that just five pins contained in TPS22945

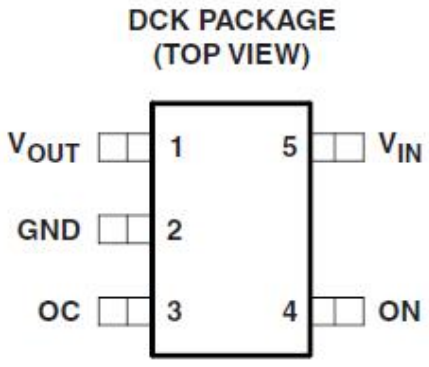

FIGURE 3.4: top view of TPS22945

GND is Ground. ON is switch control input. Don't leave it floating. OC is Over current output flag: active LOW, it will be an open drain output when an overcurrent, supply under voltage, or over-temperature happened. V_{out} is switch output. We need place bypass capacitor(s) between this terminal and GND. V_{in} is switch Input. We also need

place bypass capacitor(s) between this terminal and GND. We can see the details from the datasheet.

3.1.2.1 Design with TPS22945

See from the datasheet, we can also get the typical application circuit, showing with figure 3.5. The ON pin controls the state of the switch and if the input voltage falls

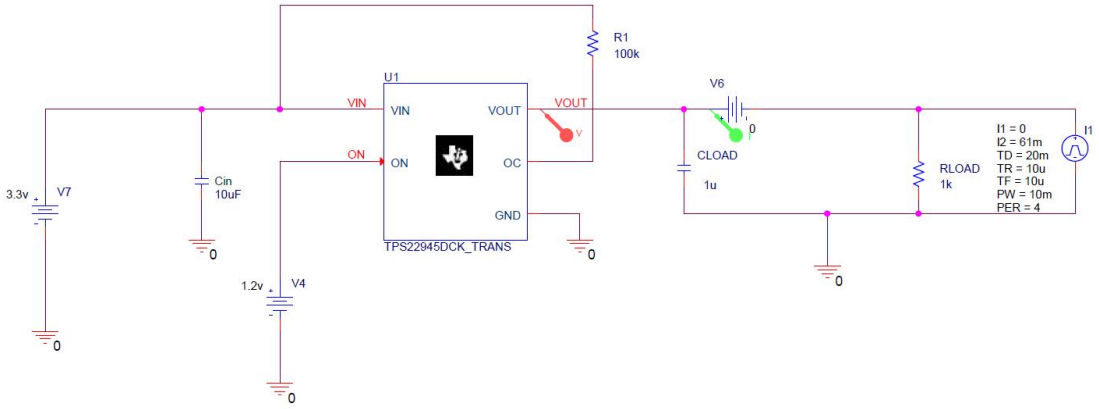

FIGURE 3.5: typical application circuit

below the under-voltage lockout threshold, under-voltage lockout will turn off the switch. When the ON pin is active, the input voltage rises above the under-voltage lockout threshold, causing the switch to be turned on, thereby limiting current overshoot. The two capacitors, the one connect input(C_{in}), which limits the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or a short-circuit, the capacitor needs to be placed between VIN and GND. The one connected output(C_{load}) to prevent parasitic inductance from forcing VOUT below GND when the switch turns off, and also make the output voltage stable. When an overcurrent, overtemperature, or input under-voltage condition is detected, OC pin is set active low to signal the fault mode. OC is an open-drain MOSFET and requires a pull-up resistor(R_1) between VIN and OC. During turn-off, the pull-down resistor on OC is disabled, reducing the current consumption of the power supply. A 3.3V DC power supply is used as VIN and a current generator is used to trigger fault happens.

3.1.2.2 Simulation Result

See the simulation result of TPS22945 in figure 3.6.

From the result, we can find that the auto-restart time and the current limit are not

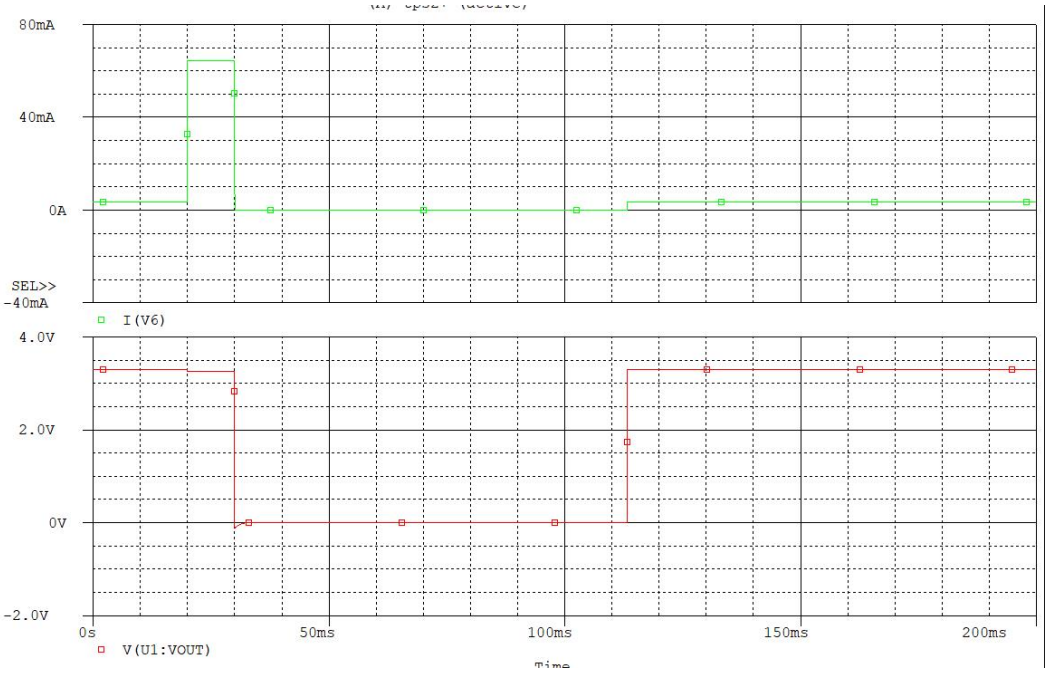

FIGURE 3.6: Simulation Results of TPS22945

like what is said in its datasheet. So, if we don't see the simulation results, just use the data ideal from the datasheet, will be not able to really get the result we want. The green line is the output current line, the red line is the output voltage line, so, obviously, the current limit is just more or less 64mA, and have 10ms fault detection delay time, and the auto-restart time is about 83ms.

3.1.3 FPF2700

FPF2700 is a current-limit load switch that provides full protection to systems and loads from excess current conditions, with an adjustable current limit range 0.4-2A. It includes an N-channel MOSFET rated speed controlled by a speed control to prevent power bus interference from being caused by "hot clogging" loads or transient overload requirements. The input voltage range is 2.8v 36V. It has auto-restart function with a fixed time 127.5ms. With the package SO8, 8 pins are contained. Showing the top view of it in figure 3.7.

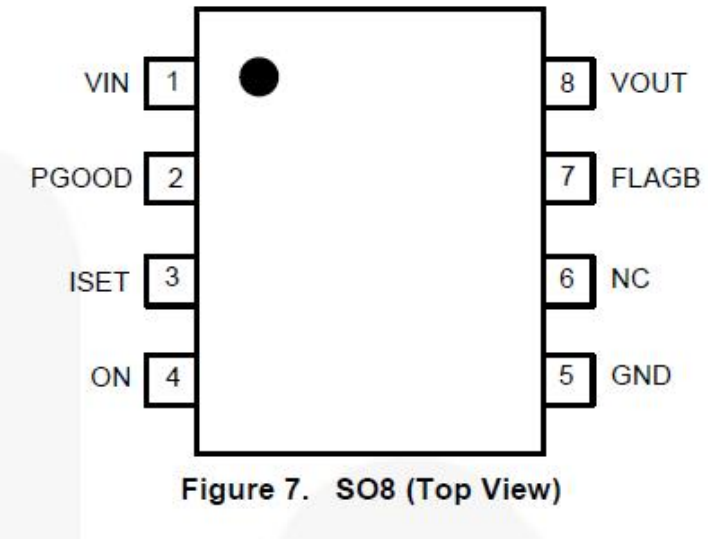

FIGURE 3.7: top view of FPF2700

VIN is the supply input, input to the power switch and the supply voltage for IC; PGOOD is power-good output, that is open-drain output to indicate that voltage has reached 90% of input voltage; ISET is the current limit set input, through using a resistor between ISET and ground to set the current limit value; ON is ON control input, active low; GND is the ground of the circuit; NC is no connection, just leave it floating; FLAGB is fault output active LOW, open-drain output that indicates the current limit, under-voltage, or over-temperature state; VOUT is the output comes from the switch.

3.1.3.1 Design with FPF2700

The design with FPF2700 is a little bit like the design with TPS22945, showing the typical application in the figure 3.8. The ON pin can be pulled HIGH to a maximum voltage of 5.5V; We can also find out there are two resistors connect on the FLAGB and PGOOD pin, they are the pull-up resistors needed to connect with an external source voltage so that it can work normally, the value of these two resistors is recommended to use 100kΩ; R_{set} is the resistor to set the current limit, the value depends; C_{in} is the input capacitor between the VIN and GND pins, it is used to limit the voltage drop of the transient current to the input power supply when the switch is on and it is converted into a discharge load capacitor or a short circuit, it is recommended to use from $10\,\mu F$ to $100\,\mu F$; C_{out} is the output capacitor which should be placed between the

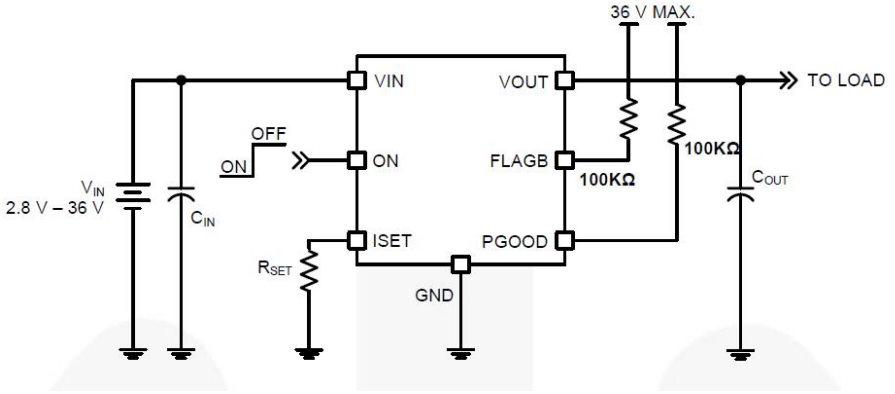

FIGURE 3.8: typical application of FPF2700

output pin and the GND pin. When the switch is off, the capacitor helps prevent the parasitic inductor from forcing the output voltage below the ground, it is recommended to use from $0.1\,\mu F$ to $1\,\mu F$. Unfortunately, I have not found any relevant materials for simulation for FPF2700, but for its limiting value range, it is already too large to use.

3.1.4 LM5060

LM5060 is a High-Side Protection Controller with Low Quiescent Current. The LM5060 provides intelligent control of high-side N-channel MOSFETs under normal on/off transitions and fault conditions[2]. When the output voltage reaches the input voltage and the MOSFET is fully turned on, the Power Good output indicates. It also provides input UVLO and programmable input OVP. A single capacitor programs the initial startup V_{GS} fault detection delay time and continuous overcurrent delay time. When the detected fault condition duration exceeds the allowable fault delay time, the MOSFET is latched until the enable input or UVLO input toggles low and then high. In a flexible design, it can also have an adjustable current limit. Showing the block diagram in figure 3.9.

There are 10 pins in it.

1. SENSE(Input voltage sense): with a constant current sink ($16\,\mu A$ typical) flowing, it can measure the threthold current through the external resistor.

2. VIN(Supply voltage input): the range of operating voltage is from 5.5 V to 65 V. When the VIN pin is greater than 5.1 V, the internal power-on-reset switches to

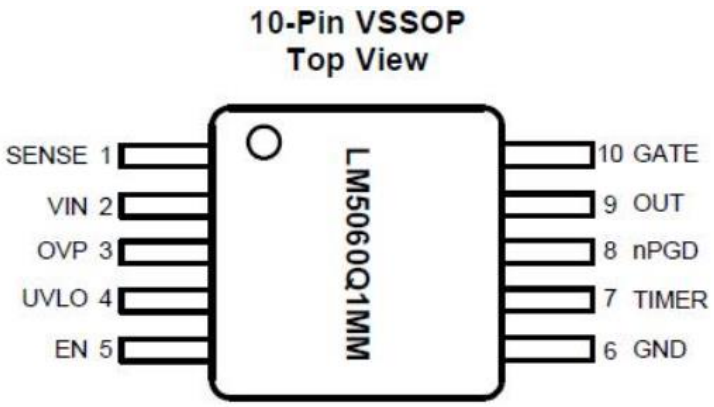

FIGURE 3.9: top view of LM5060

the active state. Placing a small bypass capacitor close to this pin can suppress noise.

3. OVP(Over-voltage protection comparator input): through an external resistor divider from the system input voltage supplied on the VIN pin to set the Over-Voltage turn-off threshold. When OVP exceeds the typical 2.0-V threshold the GATE pin is pulled low, but the controller is not latched off. When the OVP pin falls below typically 1.76 V, the controller resumes to normal opertaion.

4. UVLO (Under-voltage lock-out comparator input): it is used as an input under-voltage lock-out by connecting this pin to a resistor divider between input supply voltage and ground. The UVLO comparator is activated when EN is high. The voltage on the UVLO pin is typically higher than 1.6 V, which will release the pull-down device on the GATE pin and cause the output to rise gradually. For ensuring the UVLO pin is low when in an open circuit condition, a constant current sink ($5.5\,\mu A$ typical) is provided.

5. EN (Enable input): When the voltage on the EN pin is higher than 2.0 V, the internal bias circuit and the UVLO comparator can operate, and when the voltage on the EN pin under 0.8 V, it will switch the LM5060 to a low current shutdown. When both EN and UVLO are in the high state, the GATE pin pull-up bias is enabled. For ensuring the EN pin is low when in an open circuit condition, a constant current sink ($6\,\mu A$ typical) is provided.

6. GND: Ground of the circuit.

7. TIMER(Timing capacitor): connect this pin with an external capacitor to set the V_{DS} fault detection delay time. When this pin is above typically 2.0V, the LM5060 will latch off the MOSFET and remain off until either the EN, UVLO or VIN input is toggled low and then high.

8. nPGD(Fault status): an open drain output. When the external MOSFET V_{DS} decreases such that the values of OUT pin voltage and the SENSE pin voltage are same, the nPGD indicator is active (low = no fault).

9. OUT(Output voltage sense): connect to the external MOSFET source. Internally used to detect V_{DS} and V_{GS} conditions.

10. GATE(Gate drive output): connect to the external MOSFET's gate. The charge pump driven constant current source ($24\,\mu A$ typical) charges the GATE pin. An internal zener clamps the GATE pin at typically 16.8 V higher than the OUT pin.

3.1.4.1 Design with LM5060

Design with LM5060, it can be divided into three parts.

- The Protection Controller part:

  So, after knowing the basic information of LM5060, let us see how it works in design application,showing the figure 3.10. This design is related one typical design named LM5060EVAL, to help design and evaluate LM5060-based high-end protection controller solutions, the evaluation board can be reconfigured for different input voltage ranges by modifying undervoltage lockout(UVLO) and overvoltage protection(OVP) resistive divider (R_1, R_2, andR_3). By changing the value of the resistor R_4, the load current capacity can be increased to more than 5A. The protection transient voltage suppressor diode D_1. The PCB layout has not yet tested the current above 5A, so this should only be prudent to a certain extent.
  As I choose the N-channel MOSFET BSS119, which $R_{\mathrm{DS(on)}}$ is 10Ω when the Vgs is 4.5V and will be 6Ω when the V_{GS} (gate to source voltage) is 10V. And the I_{DS} (drain to source current) typically is 0.19A, seeing from the datasheet of BSS119. In our case, the V_{GS} typically is 5V, that we can find in the datasheet of LM5060. The formula to calculate the I_{sense} threshold.

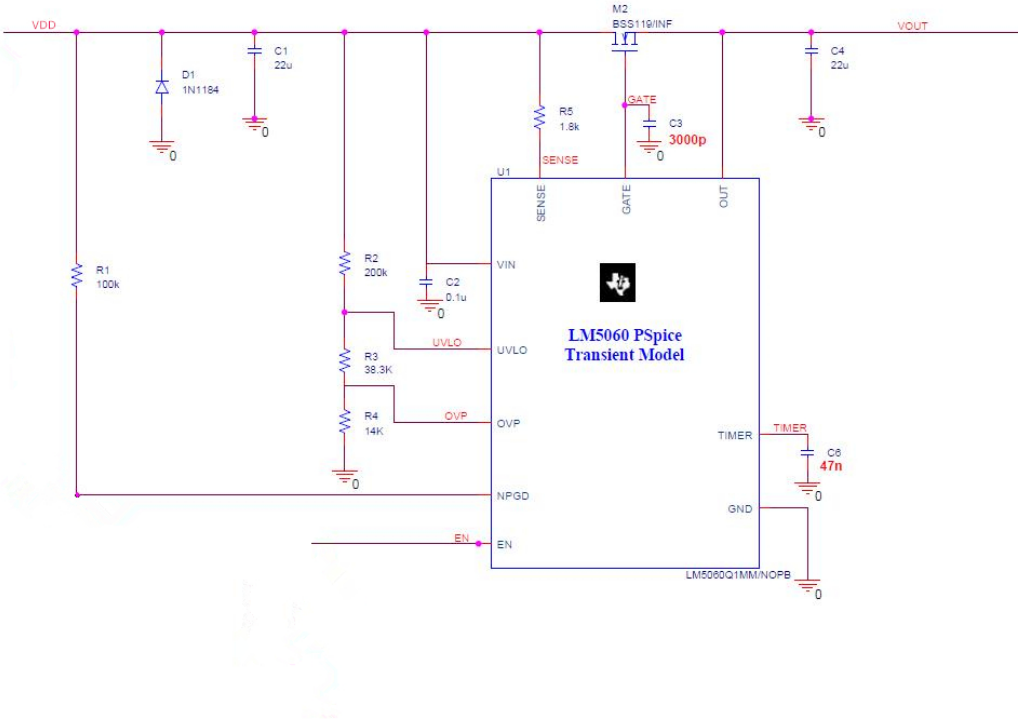

FIGURE 3.10: design application of LM5060

$$V_{\mathrm{DSTH}} = (R_{\mathrm{s}} * I_{\mathrm{sense}}) - V_{\mathrm{offset}} \tag{3.1}$$

$$I_{\mathrm{DSTH}} = \frac{V_{\mathrm{DS}}}{R_{\mathrm{DS(on)}}} \tag{3.2}$$

- V_{DSTH} is the drain to source voltage threshold.
- I_{DSTH} is the drain to source current threshold.
- $R_{\mathrm{DS(on)}}$ is the resistive drop of the pass element BSS119.
- V_{offset} is the offset voltage of the V_{DS} comparator, typically is 0.
- I_{sense} is the threshold programming current.
- R_{s} is the resisitor connecting on the SENSE pin.

From those two formulas we can get:

$$R_{\mathrm{s}} = \frac{I_{\mathrm{DSTH}} * R_{\mathrm{DS(on)}}}{I_{\mathrm{sense}}} \tag{3.3}$$

So, if we want the threshold current 10mA, use the formula, we can get the value of R_{s} is 1.9kΩ, but our V_{GS} is 5V, a little bit higher than 4.5V, so I try to make R_{s} smaller, like 1.8kΩ. And the V_1 and V_2 which is 12V DC voltage for VIN and 0-3.3V signal voltage for EN, has 10ms delay time, just for simulation work. VOUT is the voltage comes out of the protection controller part.

- The Regulator part:

AS I want the design working on an MCU, so I still need a voltage regulator, because the working voltage range of LM5060 is at least 5.5V and the voltage of the design circuit is normally 3.3V. So, I use LM1117, a 800-mA Low-Dropout Linear Regulator, which is available in an adjustable version, it can set the output voltage 1.8V, 2.5V, 3.3V, 5V with only two external resistors. The method we use it is showing in the figure 3.11. In this part the V_4 with value 0 is just for detecting current when simulate, R_{load} use 1kΩ, because our design uses the MCU MSP430F5438A under 10MHz working frequency. After checking the datasheet of MSP430F5438A, when working at 10MHz, the current almost like 3.0-3.3mA, and we set the VCC is 3.3V, so in the circuit, we can just think of load as a 1kΩ resistor. Because LM1117 is an adjustable regulator, so R_6 and R_7, those two resistors are used to set the OUT voltage. If we want to set the output voltage is 3.3V, use the formula:

$$V_{\mathrm{OUT}} = 1.25 * (1 + \frac{R_7}{R_6}) \tag{3.4}$$

- Trigger part:

This part is used to test whether the overall design works properly. The principle is to allow over-current in the entire system. The R_9 uses 1MegΩ to let the trigger part make no sense when we don't want to test the design. The R_8 uses 470Ω,

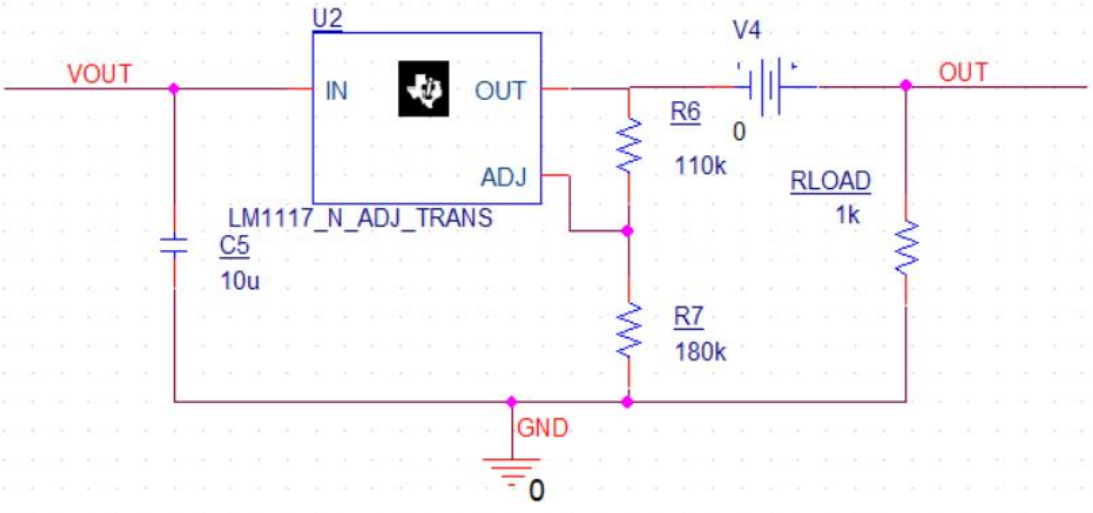

FIGURE 3.11: basic adjustable regulator

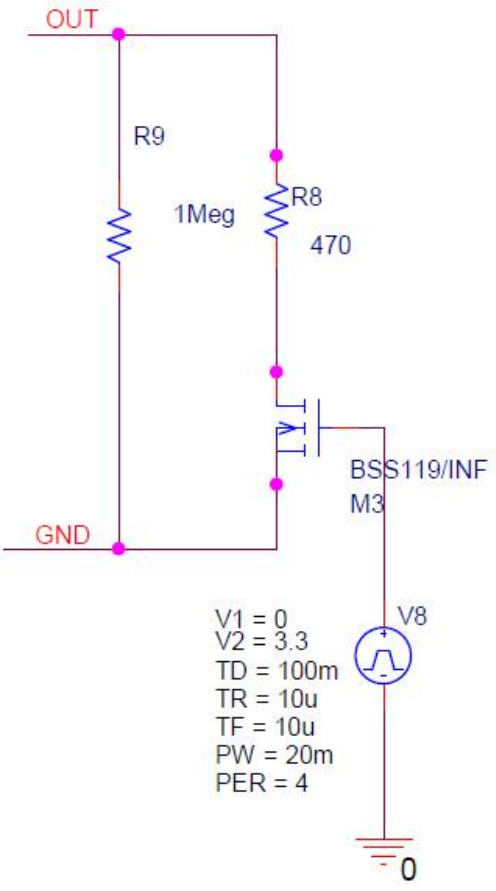

FIGURE 3.12: curcuit of trigger part

because it can make at least 10mA current in the system when used for testing. The N-channel MOSFET M_3 is used as a switch controlled by the pulse voltage generator V_8. Showing the circuit diagram in the figure 3.12

After introducing the three parts of the LM5060 design, we can get the schematic of the entire design used to simulate the circuit, showing in the figure 3.13

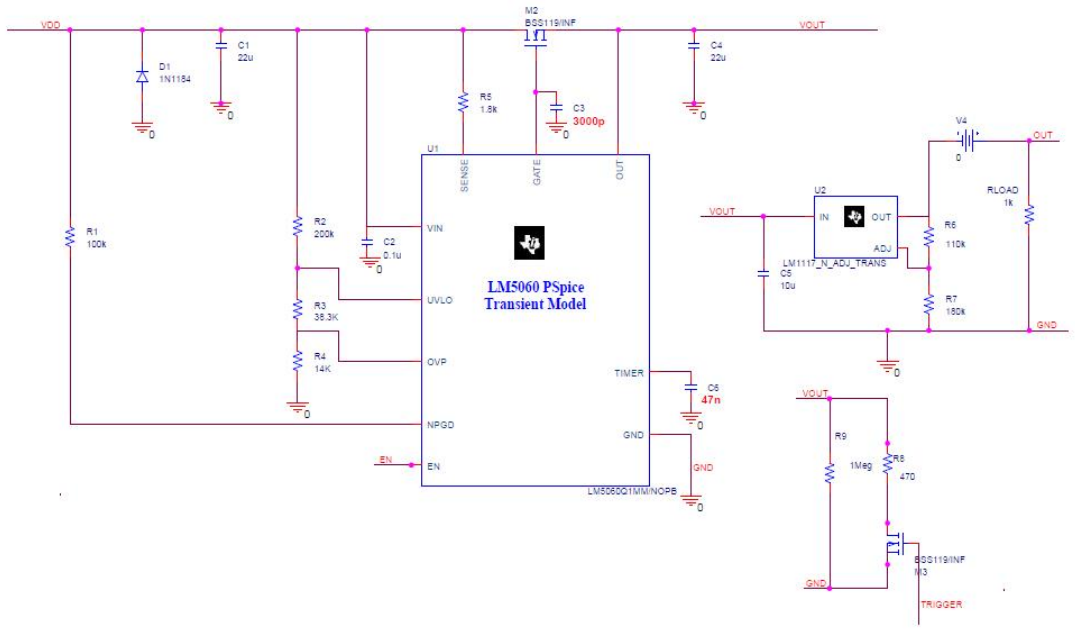

FIGURE 3.13: circuit schematic of the entire design

3.1.4.2 Simulation Results

Last but not least, we see the simulation result of LM5060 in figure 3.14. I chose N-channel MOSFET using BSS119, whose Rds is 6Ω, under 12v. So from the datasheet of LM5060, we can clearly find the formulas about calculating the sense resistor, according to I want to set current limit is 10mA, so we need set R_5 equals 1.8k. And, if let the pulse voltage generator V_8 start working at 80ms, we can detect that the red line is the current of the OUT and the green line is the voltage of the OUT. We can find that the current limit is actually only about 7mA, and the fault detection delay time is about 9ms, it is adjustable like the current limit does, related to the TIMER capacitor C_6, which I use 47nF.

3.2 Comparison

From the above, I can get a table about those three methods comparison. And from these comparisons, I need to choose the one using in my design.

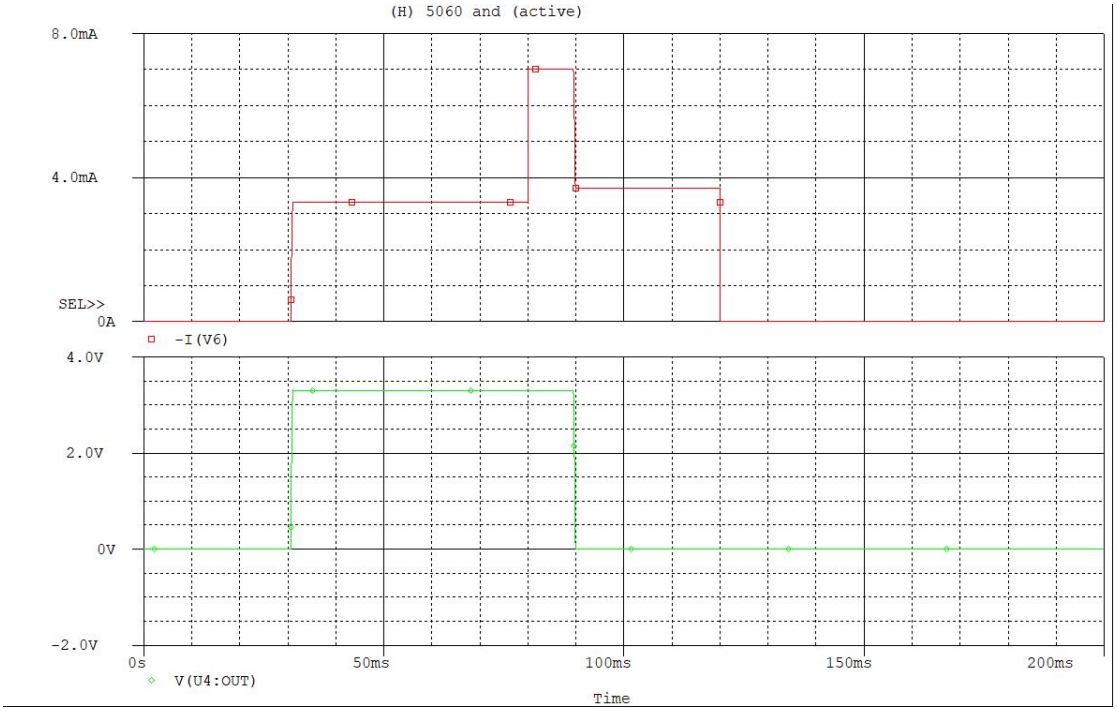

FIGURE 3.14: Simulation Results of LM5060

Component	1B127	TPS22945	FPF2700	LM5060
Current limit	adjustable(max 2A)	64mA(fixed)	0.2-4A	adjustable
Fault detection delay time	adjustable	10ms	0.5ms	adjustable
Auto-restart time	10ms after fault faded away	83ms(fixed)	127.5ms(fixed)	/
Package	100BGA	SC70(5)	SO8	VSSOP(10)

TABLE 3.1: comparison of three methods

TPS22945 is a good choice, but its current limit value and auto-restart time are fixed. FPF2700 is also with a fixed restart time, although the current limiting is in an interval, the first current limiting value is 200mA, which is relatively large and is not suitable for preventing latch-up. The design using 1B127 is already exited, it is really a good choice, but when I searching the component on the Digikey, there is no such a factory product it, that means if I use it I need write all of the devices inside the block so that becoming too complicated. And also the 1B127 just can restart when latch-up has faded away.

So, let us check the LM5060, its performative is good, and also can change the current limit and fault delay time. But just one problem, it cannot auto-restart. With seeing datasheet, there is the most important information that is when the LM5060 locks the external MOSFET, the EN pin must switch from low to high in order to start the reboot, so I can design one auto-restart circuit, which can let it restart also the fault persists, and add it on the EN pin.

3.3 Selection

According to the contents of the entire chapter, we first compare the components, TPS22945 is the simplest choice. Next, we can select through simulation results. The 1B127 can be said to be an ideal choice. The current limit threshold and auto-restart time are adjustable. However, although the TPS22945 can be auto-restarted, it cannot be adjusted in time, and the current limit threshold is also fixed, so I will consider not choosing it. The LM5060 can achieve a regulated current threshold, but it cannot automatically restart.

Finally, through market searches, I found that there is no factory to produce 1B127, so if I want to use 1B127, I need to draw the circuit inside all the electronic components, which greatly increases the complexity of the overall design. However, the LM5060 is a very economical option, and if I want it to have an automatic restart feature, just only need to design a small part of the circuit. It will also be a completely new design, we will be discussing in the next chapter. So I will choose the LM5060 to implement my design.

Chapter 4

Auto-Restart Circuit Design

In this chapter, I will explain why the LM5060 can be automatically restarted, as well as the two approaches that were envisaged, and verified by simulation results. Finally, through comparison, the final choice was made and the final circuit schematic of my design was obtained.

4.1 EN pin of LM5060

LM5060 Enable pin (EN) allows remote On/Off control. Enable pin on/off threshold compatibility with CMOS. External N-channel MOSFET can be closed remotely by placing the EN pin below the lower input threshold EN_{THL} (800mV). External N-channel MOSFET can be opened remotely by placing the EN pin above a high input threshold EN_{THH} (2.00v). When the EN pin is less than 0.5V(typical), LM5060 enters a low current (disabled) state. The function threshold levels showing in the figure 4.1 So, the main idea across my mind. I just need the voltage on the EN pin go to under the 0.5V first and then back to higher than 2V when the MOSFET cut off all the circuit because of the overcurrent happened. To make voltage changing without a source generation, we need to use capacitors. There are two methods I found to implement, showing in the next sections.

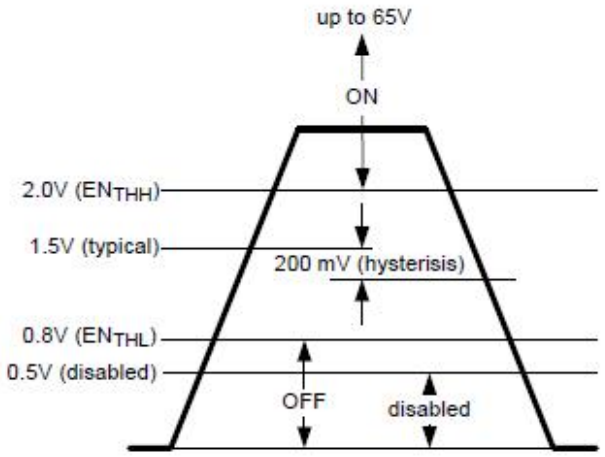

FIGURE 4.1: Enable Function Threshold Levels

4.2 Method using Operational Amplifier

Before introducimg the method I thought, I will show the circuit schematic firstly in the figure 4.2. We can see there is an op-amp and several resistors and capacitors, the

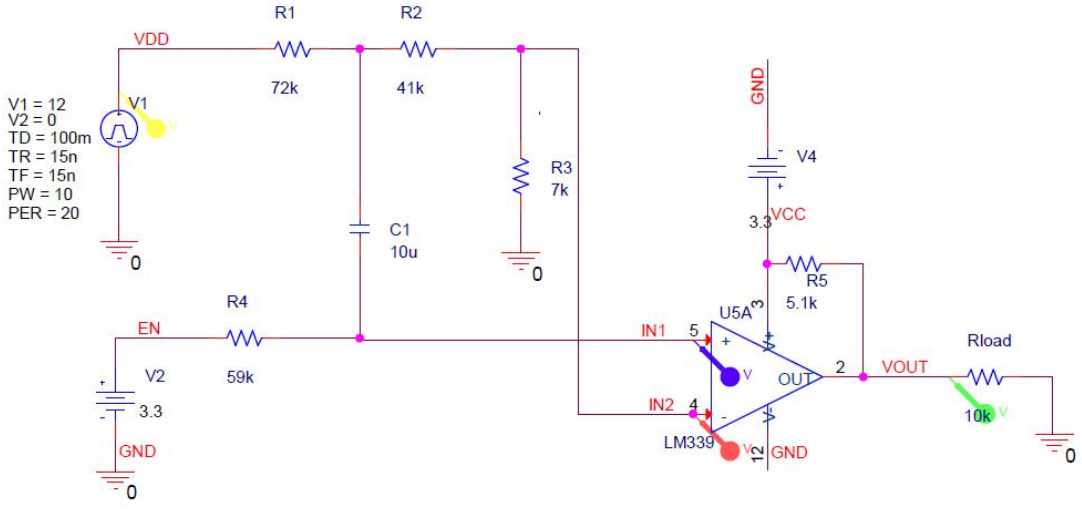

FIGURE 4.2: auto-restart circuit by using op-amp

source generators are used for simulation. VDD is 12V, it is the voltage for the device LM5060, and it will shut down after 100ms, this is for the simulation test. GND is the ground. VCC is the voltage for the circuit, normally is 3.3V. At EN pin of the design, I need to supply 3.3V voltage. The VOUT is the output from the amplifier, and also is the input voltage to the EN pin of LM5060. Next, I will explain the function of each part and how the entire circuit works.

4.2.1 LM339

The LM339 consists of four independent voltage comparators designed to work over a wide range of voltages. Dual power operation is also possible, as long as the difference between the two is 2V to 36V, VCC is at least 1.5V higher than the input common mode voltage. Current consumption is independent of the power voltage. The output can be connected to other open collector outputs for connections and relationships. The figure 4.3 shows the configuration of the voltage comparator using by LM339.

The voltage comparator has the positive and negative supply, and two inputs(IN1 and

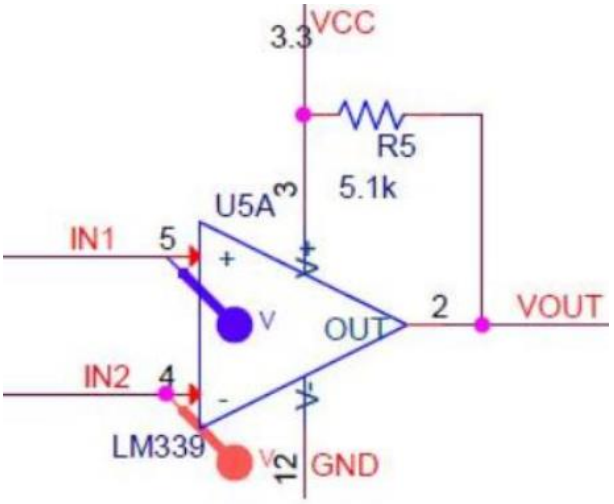

FIGURE 4.3: voltage comparator

IN2) and one output(VOUT), it's comparing the two voltages through comparing the voltage signal between the inverting and the non-inverting input. If the non-inverter (positive) input of the comparator is less than the inverter (negative) input, the output will be low, and the output will be negative saturation at the negative power voltage V-, when the output is 0. If the non-inverter (positive) input of the comparator is greater than the inverter (negative) input, the output voltage is higher to the positive power supply, and V+ results in output saturation.

The LM339 also requires an external pull-up resistor(R_5) which allows several outputs to be tied together and the overall output is low if any one of the outputs is low. This feature is important in the logic used as will become apparent[3]. The typical pull-up resistor is 4.7kΩ to 100kΩ when driving other CMOS or TTL gates. Lower resistor values are used when higher speeds are needed (less influence from output capacitance).

The LM339 is specified with a 5.1kΩ pull-up. So in the schematic, we can find that the R_5 which is the pull-up resistor setting with 5.1kΩ.

4.2.2 RC circuit

RC circuit is a circuit with resistance(R)and capacitance(C). RC circuit is a common component in electronic devices. They also play an important role in the transmission of electrical signals from nerve cells. A capacitor can store energy and a series resistor controls the rate at which it is charged or discharged. In this case, I only use the voltage change at one point in the circuit and compare it with the reference value by the input voltage comparator LM339. The resulting output will be input to and gate as a digital signal.

We can divide the process of the voltage change into three stages:

- First stage:

  In circuit theory, zero state response (ZSR), also known as a forced response, is the behavior or response when the initial state of the circuit is zero. ZSR is produced only by the external input or drive function of the circuit, not by the initial state. ZSR is also called the forcing or driving response of a circuit. So the first stage of the RC circuit is the ZSR, which we can also think of as a capacitor charge. Showing in the figure 4.4 In this stage, the voltage of the capacitor starts going

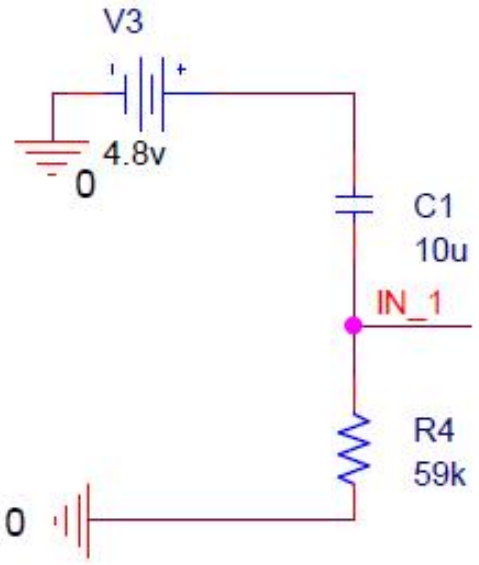

FIGURE 4.4: zero state response of RC circuit

high, the time when it is saturated is depending on the value of the resistor and capacitor. The equation is:

$$U_c = U_s * (1 - e^{-(\frac{t}{RC})}) \tag{4.1}$$

The U_s is 4.8V which is the voltage of VDD divided by resistors(V_3). Because we measure the voltage from IN1, and in this stage, IN1 is equal to the voltage of the resistor, since there is no current in this state, the voltage of the resistor is 0, so in the first stage IN1 = 0V.

- Second stage:

  In the second stage, we can see in the figure 4.5. It starts another charging on the other side of the capacitor, the source comes from the voltage supplied on EN(V_2). At this time, the voltage of IN1 will come to 3.3V.

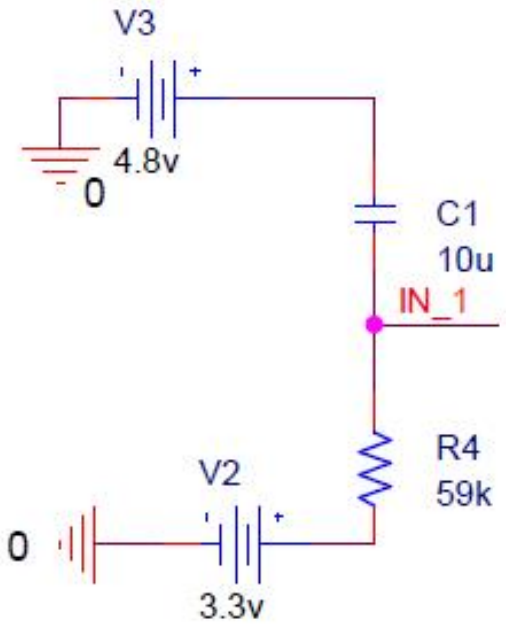

FIGURE 4.5: second stage

- Third stage:

  The total response of the circuit is the superposition of ZSR and zero input response. ZIR only comes from the initial state of the circuit, not an external drive. ZIR is also called the natural response, and the resonance frequency of ZIR is

called the natural frequency. ZIR seems to be the discharge of a capacitor. Showing in the figure 4.6. At this time, the voltage of IN1 is the voltage of capacitor

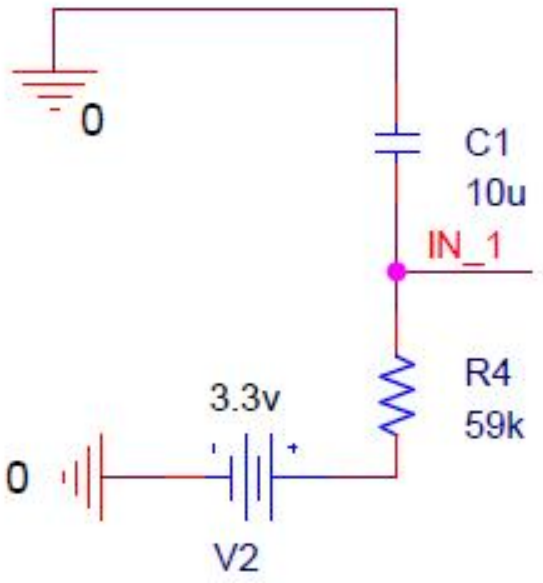

FIGURE 4.6: total response of the RC circuit

U_c. The U_s is 3.3V in this case and the U_0 which is the initial voltage is voltage drop at the two sides of the capacitor, we will know it is about 1.5V. According to the Kirchhoff's voltage law: The principle of conservation of energy implies that the directed sum of the electrical potential differences (voltage) around any closed network is zero. So, we can get the equation of U_c.

$$U_c = -U_0 * e^{-(\frac{t}{RC})} + U_s * (1 - e^{-(\frac{t}{RC})}) \tag{4.2}$$

So, as we know the left part about discharging finally goes to zero and the right part about charging finally goes to 3.3V. During this period, because the rate of initial voltage decrease is faster than the rate of increase of the input voltage (according to the value of the resistor), the voltage of the capacitor first drops to close to zero, and then the voltage gradually rises to 3.3V (according to the capacitance value) to reach a steady state. So, I can use the process of IN1's voltage from low to high to set a reference value as the inverting input to the comparator LM339, so that we can get a digital signal output what we want.

4.2.3 Designed Circuit Simulation Result

From the last section, if we want to implement the automatic restart function, the voltage on EN pin of LM5060 needs to be lowered and then raised. It seems like the digital signal we can get from the output of LM339(VOUT). First, I show the simulation result of the designed circuit schematic in figure 4.7. In this figure, the yellow is the

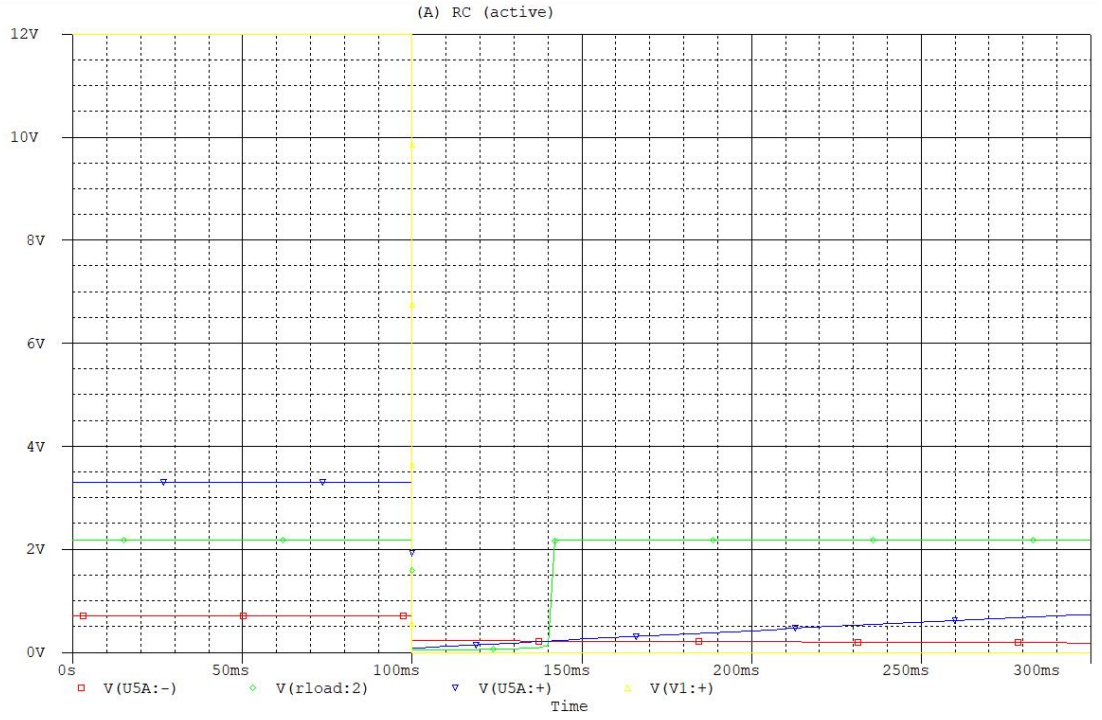

FIGURE 4.7: simulation result of designed circuit

voltage supply for the device lm5060(VDD), the blue line is the non-inverting input(IN1) of LM339, the red line is the reference voltage which connected to the inverting pin(IN2). The green line is the output line(VOUT), going to the EN pin of LM5060. We can find that when the VDD shut down(like cut off the circuit when overcurrent happened), the non-inverting input(IN1) falls to zero, below the voltage on the inverting input(IN2) so that the output of the comparator(VOUT) will go to zero. But, with the capacitor keeping charge, the voltage on IN1 will back to higher than IN2 voltage, and then the VOUT will back to the high state. In the figure the green line(VOUT) falling to the 0 immediately, but after a period of time, it will go back to high, I could just get the signal change process I needed, so this designed circuit can theoretically be used. Next, I will place it in the circuit of the overall protection system to see if it works or not.

4.2.4 Solution

From the previous and part of the introduction, I have obtained an external circuit diagram that can achieve EN voltage from high to low and then back to high, and verified by simulation results that it can be achieved. In this part, I will connect the designed circuit to the entire system and through the simulation to see if the automatic restart function can be implemented or not. The all system circuit showing in the figure 4.8 and the simulation result showing in the figure 4.9. From those two figures,

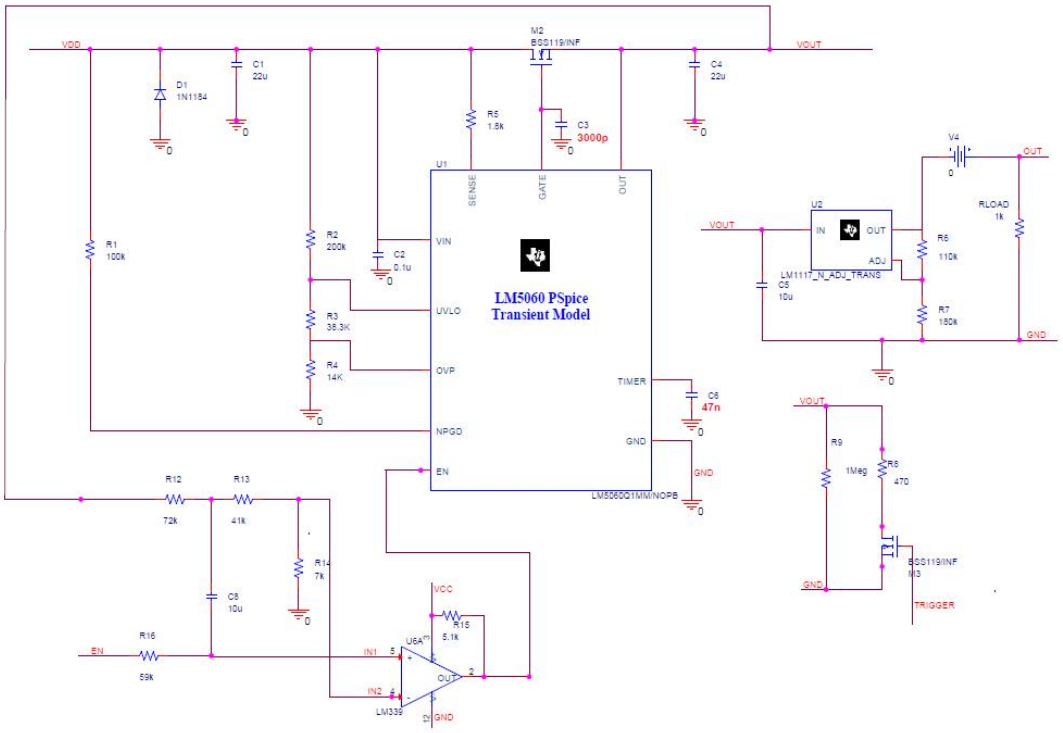

FIGURE 4.8: all system circuit schematic

it can be clearly seen that when the purple line which is the voltage of LM5060 OUT pin is going to 0, that meaning overcurrent happened and cut off all the circuit, the green line is the EN voltage, and the yellow line is the voltage of R_{load}, both of them go down first and then back to the normal. Obviously, the restart function is implemented. The auto-restart time is depended on the value of the capacitor C_{10}. In summary, this method is feasible. But is there a simpler way? Let us go to see the second method in the next section.

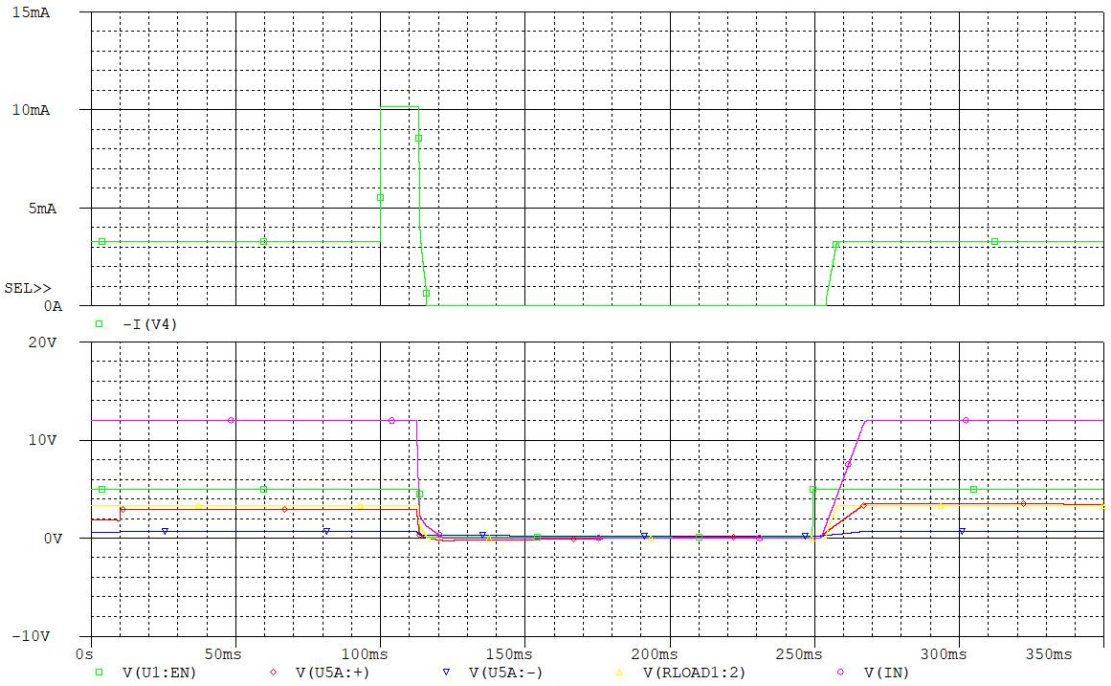

FIGURE 4.9: simulation result of all system

4.3 Method using AND Gate

Similar to the previous method, both need to get the change of the digital signal voltage of EN pin of LM5060 goes lower and then increase. The AND gate is a basic digital logic gate that implements logical conjunction. A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If none or not, a LOW output result. The function can be extended to any number of inputs. I will still show the designed circuit schematic first in figure 4.10. As we can see, VDD is 12V, it is the voltage for the device

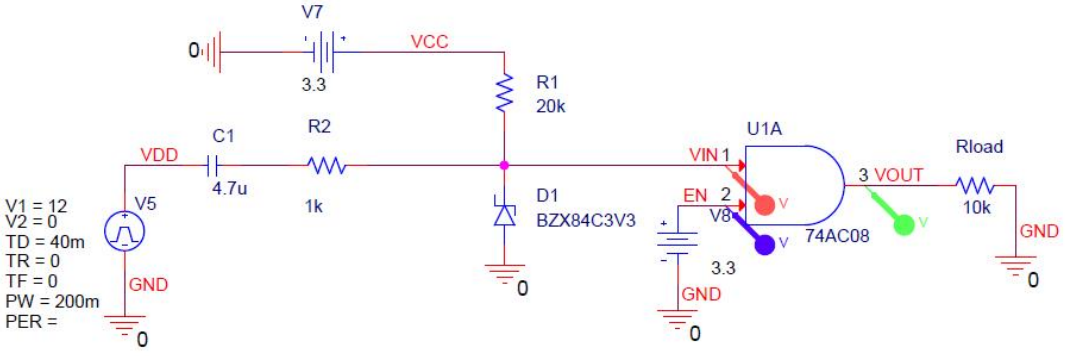

FIGURE 4.10: designed circuit schematic

LM5060, and it will shut down after 40ms, this is for the simulation test. GND is the ground. VCC is the voltage for the circuit, normally is 3.3V. The VIN is the VDD

voltage after divided, using as one input to the AND gate. At EN pin of the design, I need to supply 3.3V voltage. The VOUT is the output from the AND gate, and also is the input voltage to the EN pin of LM5060. There just contains one AND gate, one RC circuit and the zener diode which is the most important part in this design. Next subsections show the functions of them.

4.3.1 RC circuit with a Zener Diode

Show the circuit schematic in figure 4.11. This part is the core of the overall design,

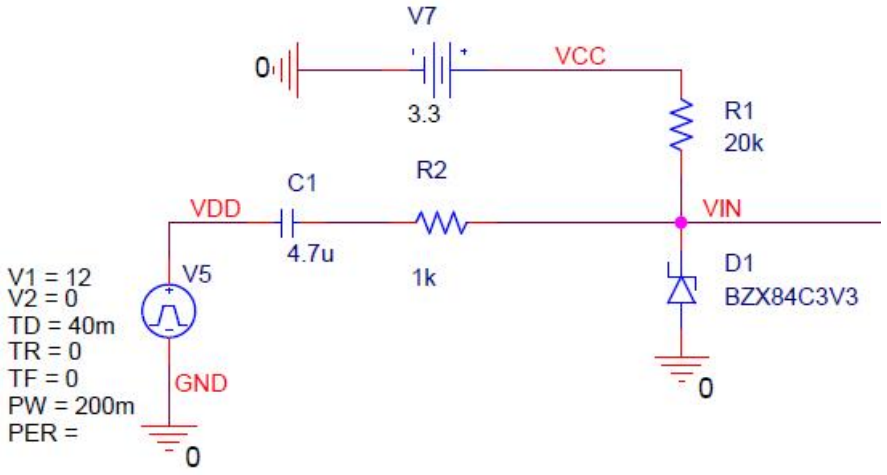

FIGURE 4.11: core of the design

through the voltage transformation and the role of zener diodes, we get the signal we need. The RC circuit is only doing charge and discharge work. When the circuit is powered off, provide a reverse voltage to the zener diode.

Zener diodes are some of the most extensively-used components in semiconductor technology, and they are used for a wide variety of applications, including voltage regulation and protection from electrostatic discharge events[4]. The zener diode is a surface-contact type semiconductor silicon diode manufactured by a special process. Its characteristic is that it can operate in a reverse breakdown state, and the breakdown voltage is almost constant. When the reverse voltage is removed, the normal state can be restored, that is, the reverse breakdown is reversible. I used the BZX84C3V3 whose steady voltage is 3.3V. The current limiting resistor(R_1)) must be connected in series to avoid permanent thermal breakdown and damage when the reverse current exceeds the specified value.

When the circuit is working in the normal state, the current of zener diode flows from the diode's anode to cathode, the voltage of VIN pin is 3.3V. But when the source generator shut down, the RC circuit start discharging, that provide a reverse voltage to the zener diode, that let the diode turn to reverse breakdown, and holding a constant breakdown voltage, at this time the voltage of VIN is the reverse breakdown voltage. This change just caused the original 3.3V voltage to mutate to a very small or even negative voltage, make the signal from high to low.

As the capacitor continues to discharge, the reverse voltage on the zener diode's anode side gradually decreases, until it is not enough to reverse breakdown the zener diode, the zener diode will recover to the positive breakdown voltage of 3.3V, and the voltage of VIN will return to 3.3V again. This change makes the signal of VIN from low back to high.

4.3.2 AND Gate

In this case, I choose series 74AC08 positive input AND gate because there maybe has the negative signal go through which will affect the digital signal output of the AND gate. The AND gate collects the two inputs VIN and EN. VIN changes as I have said before, and the EN is a steady voltage input. We will see the simulation result next and see it is feasible or not.

4.3.3 Designed Circuit Simulation Result

From the first section, if we want to implement the automatic restart function, the voltage on EN pin of LM5060 needs to be lowered and then raised. It seems like the digital signal we can get from the output of AND gate(VOUT). First, I show the simulation result of the designed circuit schematic in figure 4.12. In this figure, the red line is the VIN which is lowered and then raised and the blue line is the EN which is stable with 3.3V, the green line is the output of the AND gate(VOUT), which I will use it as the voltage signal on the EN pin of LM5060. We can find that when the source supply shut down(like cut off circuit when overcurrent happened), the VOUT falls to the 0 immediately, but after a period of time, it will go back to high, I could just get the signal change process I needed, so this designed circuit design can also theoretically be used.

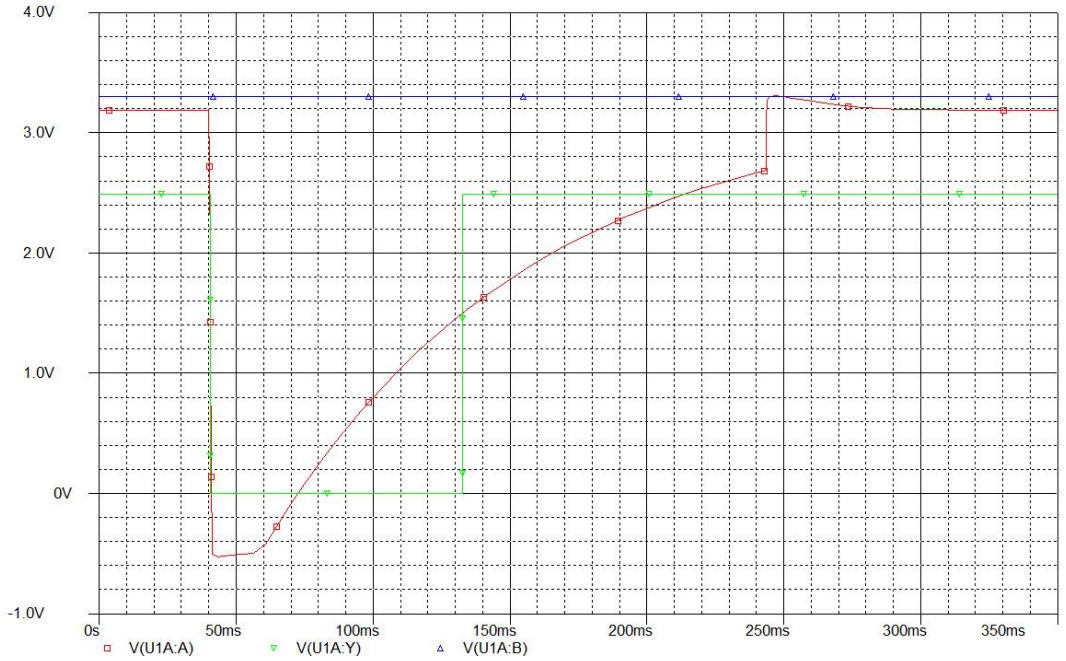

FIGURE 4.12: simulation result of designed circuit

Next, I will place it in the circuit of the overall protection system to see if it works or not.

4.3.4 Solution

From the previous and part of the introduction, I have obtained an designed circuit diagram that can achieve output voltage from high to low and then back to high, and verified by simulation results that it can be achieved. In this part, I will connect the designed circuit to the entire protection system and through the simulation to see if the automatic restart function can be implemented. The all system circuit showing in the figure 4.13 and the simulation result showing in the figure 4.14. From those two figures, it can be clearly seen that when the yellow line which is the voltage of LM5060 OUT pin is going to 0, that meaning overcurrent happened and cut off all the circuit, the green line is the EN voltage, and the purple line is the voltage of R_{load}, both of them go down first and then back to the normal. Obviously, the restart function is implemented. The auto-restart time is depended on the value of the capacitor C_7. In summary, this method is also feasible. But, which one is better?

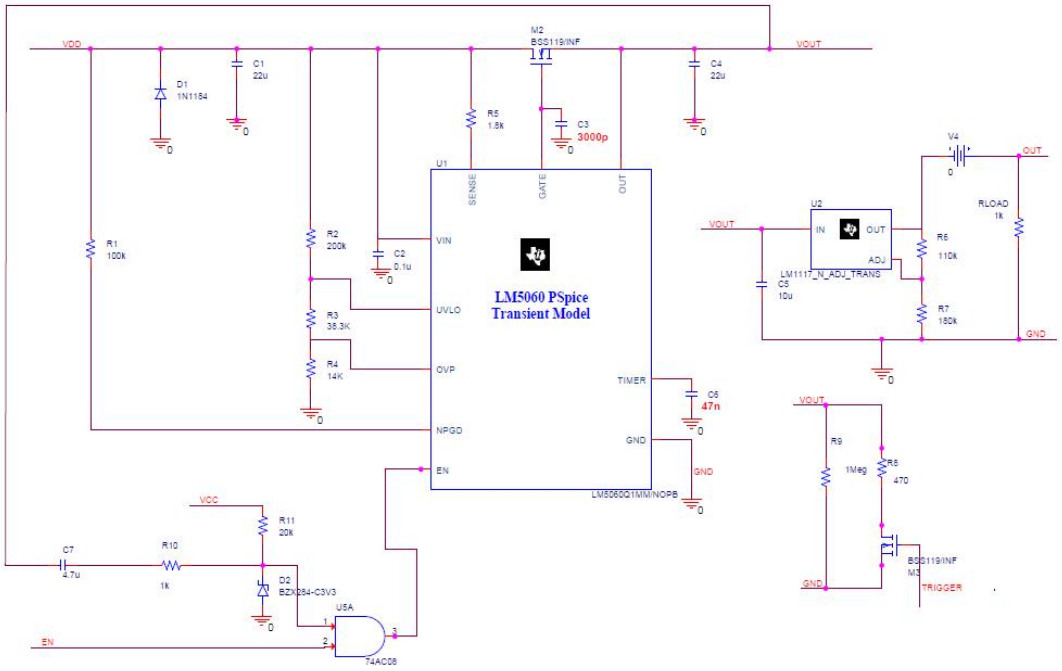

FIGURE 4.13: all system circuit schematic

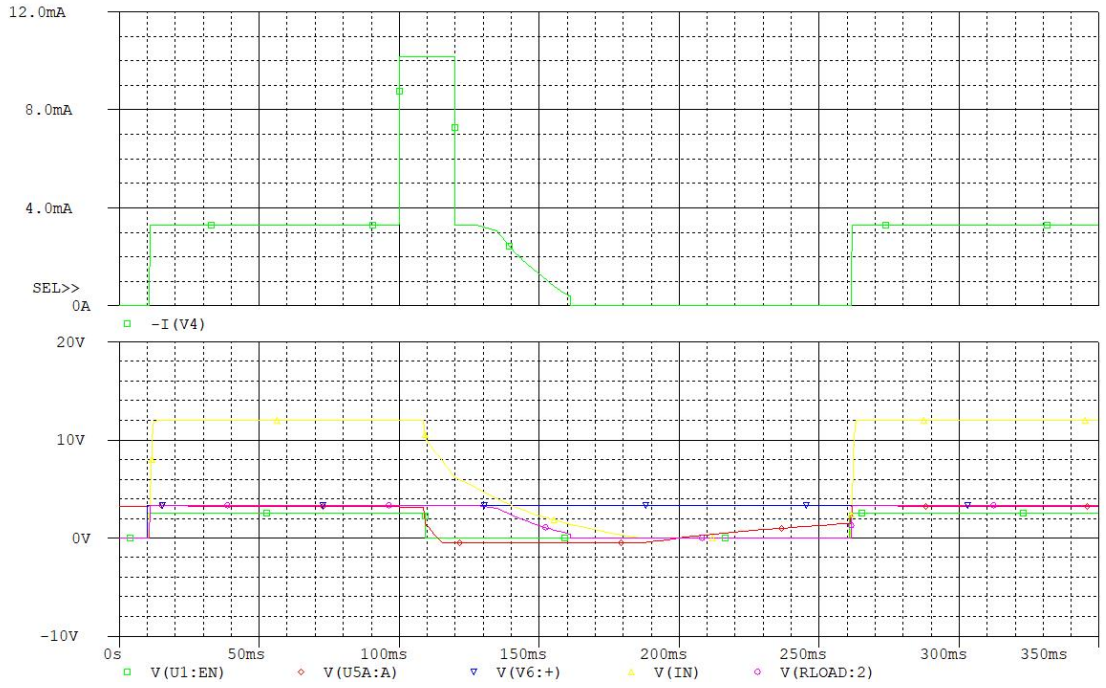

FIGURE 4.14: simulation result of all system

4.4 Conclusion

I introduced two designs that implement the LM5060 auto-restart function. One is to use the LM339 operational amplifier as the voltage comparator to get the digital signal

output of the EN voltage change. One is to use the AND gate to realize. In terms of complexity, the second method uses less three resistors, which reduces the number of wires and is not only simpler, but also reduces electromagnetic induction between wires on the PCB board. In terms of space, because the LM339 package has only 14 pins and only 5 pins in AND gates, it is more space-saving and simpler. From the simulation results, there is no delay in the signal change of the AND gate, and the effect is more superior. So to sum up, I will choose to use the method of AND gate to complete my design.

In conclusion, my design can be divided into three parts:

1. Control part

   The control part is detecting the magnitude of the current, performing an open or closed operation. Showing the block diagram in figure 4.15.

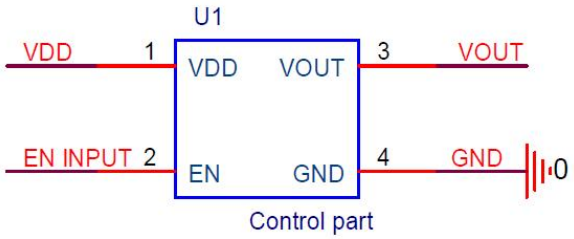

FIGURE 4.15: control part of design

   VDD is the voltage for the device, needed to connect with a 12V supply voltage. EN is the pin of enabling, it should be supplied with a voltage higher than 2V, so 3.3V is also suitable, but it is connected with the output of the auto-restart part to implement automatic restart function. VOUT is the output voltage, it is going to the input of the regulator and the input of the auto-restart part. GND is the ground.

2. Regulator part

   The regulator part transfers the output voltage of the control part from 12V to 3.3V, to make voltage suitable for the load circuit. Showing the block diagram in figure 4.16. IN is the input of the regulator part, it is connected with the output coming from the control part. OUT is the output of the regulator, it is also the

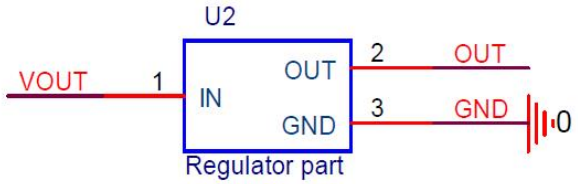

FIGURE 4.16: regulator part of design

output of the design, I need this pin to test the design, so the OUT pin also has to go to the triggering test part. GND is the ground.

3. Triggering test part

   Triggering test part is used to detect the final design. In the normal working state, it will not affect the operation of the circuit. When the voltage is connected by the Trigger pin, the detection state will be performed. Showing the block diagram in figure 4.17.

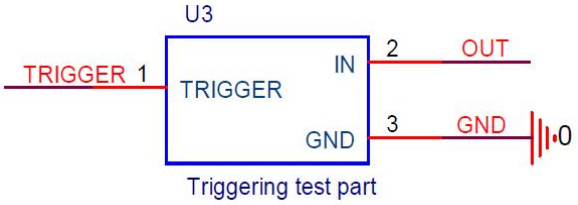

FIGURE 4.17: Triggering test part of design

IN is the input of this part, it should be connected with the output of the regulator part. Trigger is the gate of a N-channel MOSFET, when giving a voltage that is sufficient to allow the switch to close, and make the design in a fault condition, so that we can test the design is working correctly or not. GND is the ground.

4. Auto-restart part

   The auto-restart part is used to automatically make the control part closed again after the control part shut down the circuit in an adjustable time. Showing the block diagram in figure 4.18. VCC is the voltage for the circuit, so a 3.3V should be given on this pin. IN is the input of this part, it should be connected with the output of the control part. EN is the pin of enabling, it should be supplied with a voltage higher than 2V, so 3.3V is also suitable. OUT is the output of this part, it should be connected with the EN pin of the control part, to implement automatic restart function. GND is the ground.

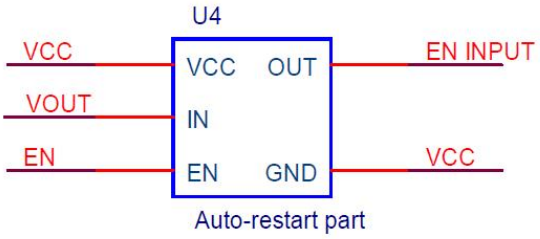

FIGURE 4.18: Auto-restart part of design

So, in my design, there are VDD, VCC, EN, OUT, TRIGGER and two GND pins, these 7 pins. In the next chapter, I will introduce detailed steps for PCB design.

Chapter 5

PCB Board Design

After designed the circuit schematic and passed the simulation test, I will carry out the most important part of this design, PCB design. In the second chapter, I have already talked about the concrete steps of making PCB. Then, in this chapter, I will explain in detail how I used the Orcad PCB Designer in Cadence 17.2 to design my PCB.

5.1 Transfer to PC Board Wizard project

From the Chapter 4 I have already completed the circuit design schematic as figure 4.13, I have to create a PCB project through it. But how can I transfer a simulation state schematic to a schematic for making a PCB project? Showing the next.

5.1.1 Recreate

Since the schematic I already get is created using PSpice Analog, so I need to recreate a new project in OrCAD Capture, this time choose the selection ”PC Board Wizard” showing in figure 5.1. I choose the libraries what I need, and then copy the circuit schematic which I already designed, and phrase it on the new project. After this, I can start planning the PCB circuit diagram.

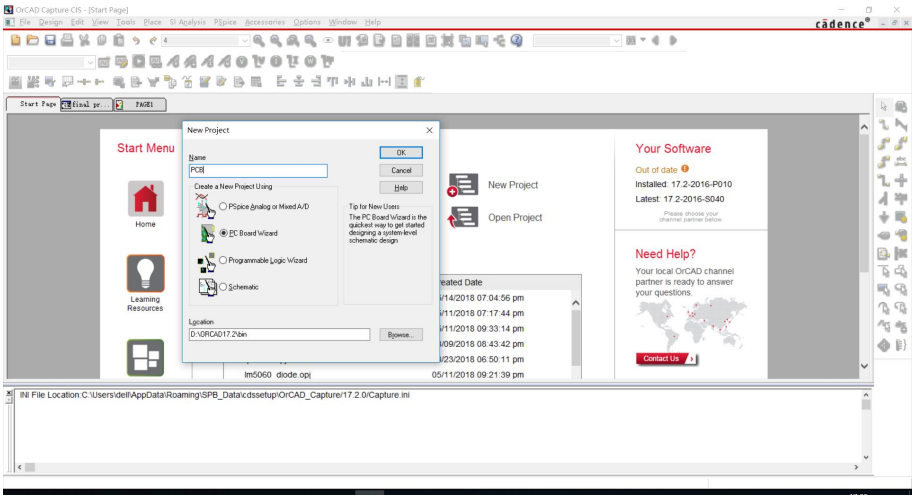

FIGURE 5.1: recreate table in ORCAD

5.1.2 PCB Circuit Diagram

In the original schematic, there are several power supplies for simulation. In PCB circuit diagram I don't need these, after delete these I should connect each input and output with a connector(J1 and J2 in the figure 5.2) which is an electro-mechanical device used to join electrical terminations and create an electrical circuit. Delete all the ground connection, and through "Place Net Alias", bring all ground wires together to a connector. I kept the circuit used for the detection and I separate it from the design circuit(the little right part in figure 5.2), also connect it with a connector.

After retrofit circuit diagram, in order to know the names of all parts more clearly when making PCB, I need to rename the disorderly names in order. And at this time, select which specific model of each device from the "Digi-key" website, and put the part number into corresponding device's reference. Finally, I can get the PCB circuit diagram showing in the figure 5.2.

5.1.3 Footprint

Footprint or land mode refers to the arrangement of a pad (in surface-mounting technology) or through-hole (in through-hole technology) for physically connecting and electrically connecting components to the PCB. The ground pattern on the circuit board matches the lead arrangement on the element. Therefore, adding memory footprint to each component is essential.

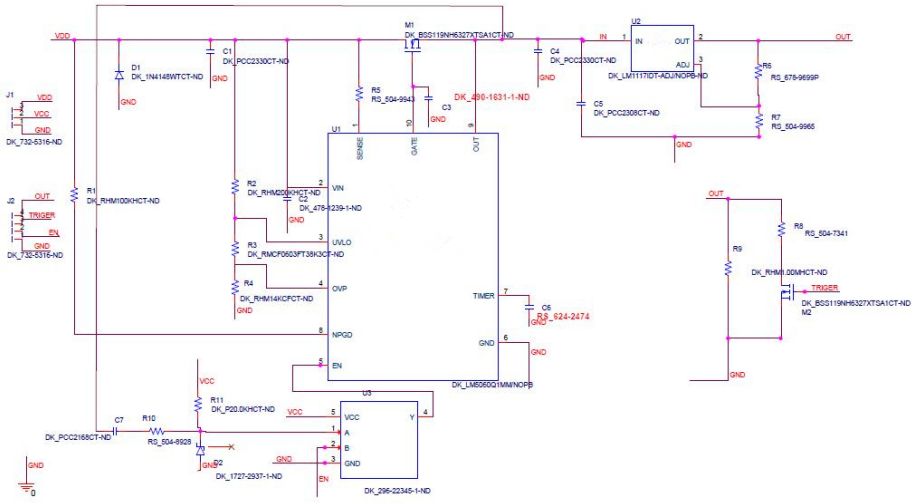

FIGURE 5.2: PCB circuit diagram

We can download the footprints from the website or write them by ourselves, but remember the file type is fit for the tools we use. In ORCAD Capture, the footprints are saved in a fixed folder, in my laptop, the path to save the file is shown in figure 5.3. Remember to save the .dra and .psm files into the fixed folder. After getting the footprints

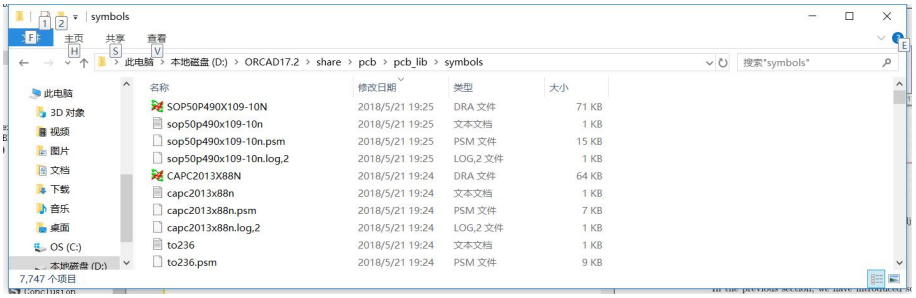

FIGURE 5.3: the path to save footprint file

file, I need to add them into each component, so double left clicks the component which I want to add footprint, showing the table as figure 5.4. We can clearly find that there is a section name "Footprint", I just copy the name of .dra file corresponding which component I have double clicked and phrase it into the form, and save. This completes the work of adding footprints.

5.1.4 PCB Project

After setting all of the components with the footprints, I go to create the PCB project, the main steps is Annotate and Create Netlist. Go to the main page select the .dsn file

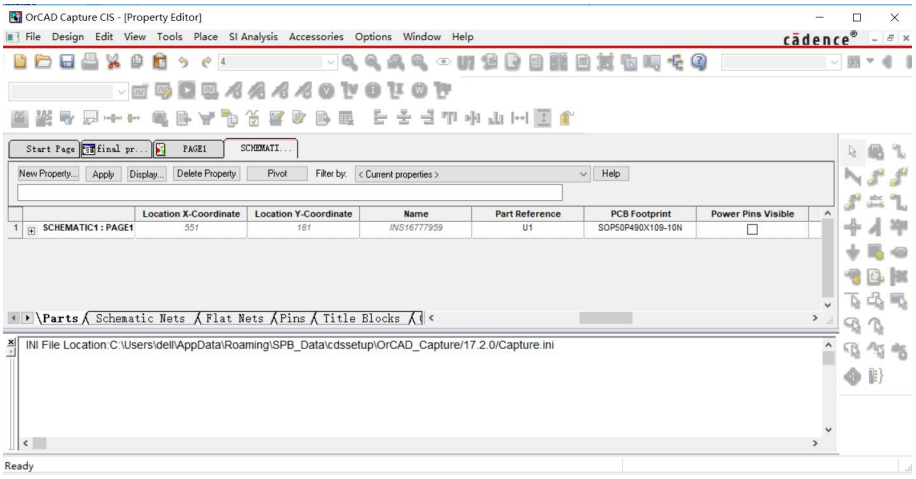

FIGURE 5.4: the table of adding footprint

about my project, and from the "Tools" on the top, we can clearly see those two options. In the figure 5.5 and figure 5.6 will show them. In the absence of any errors, I have already got a PCB project, and the OrCAD PCB designer will open automatically.

5.2 Design Steps

In this section, I will introduce the delicate steps in the design of PCB using OrCAD PCB Designer.

5.2.1 Set Design Parameters

At the beginning of the design, I have to set all the parameters such as the board size, the number of layers, shape the board and so on. But the first thing is to set the unit to millimeters, which I prefer. The most important is setting constraint values, showing in the figure 5.7, open from the "Setup". I need to set physical and spacing section, in my design set the minimum line width of 0.2mm because it will be cheaper when printing it out. And I set the space of line for all the other things is 0.3mm. Why don't I set three times line width? The reason is that my design is relatively simple, and there are not many components and wires. So in order to make my design as delicate as possible, but without affecting the layout of the circuit, I tried many times about the space with different values, finally, the 0.3mm is a good choice.

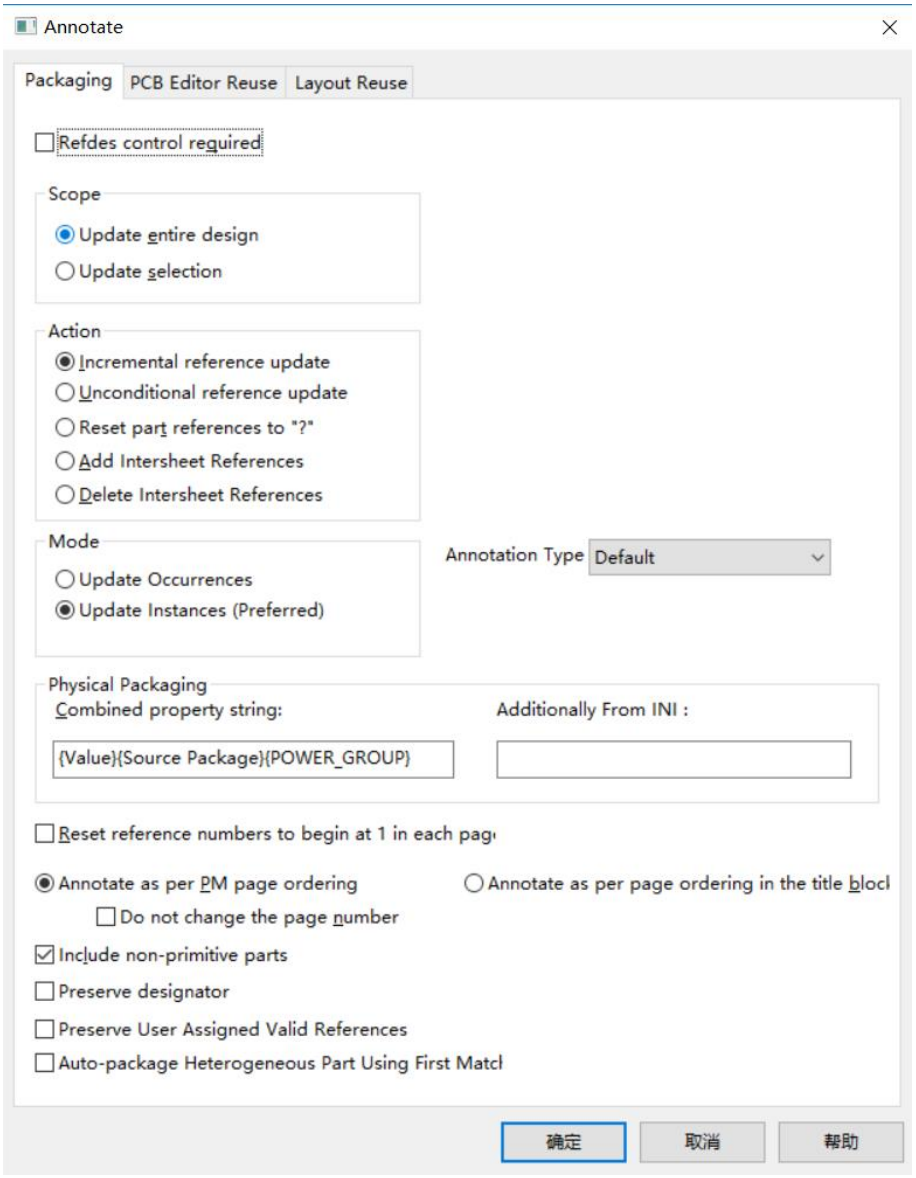

FIGURE 5.5: annotate option

5.2.2 Place Components

After setting all the parameters, I can start placing the components. From the menu bar, click ”Place” and select ”Components Manually”, and place the components one by one.

5.2.3 Reasonable Layout and Routing

As I told in Chapter 2, this is the most important part of the design. After all the components are placed, we can remove all the flying lines and arrange the components

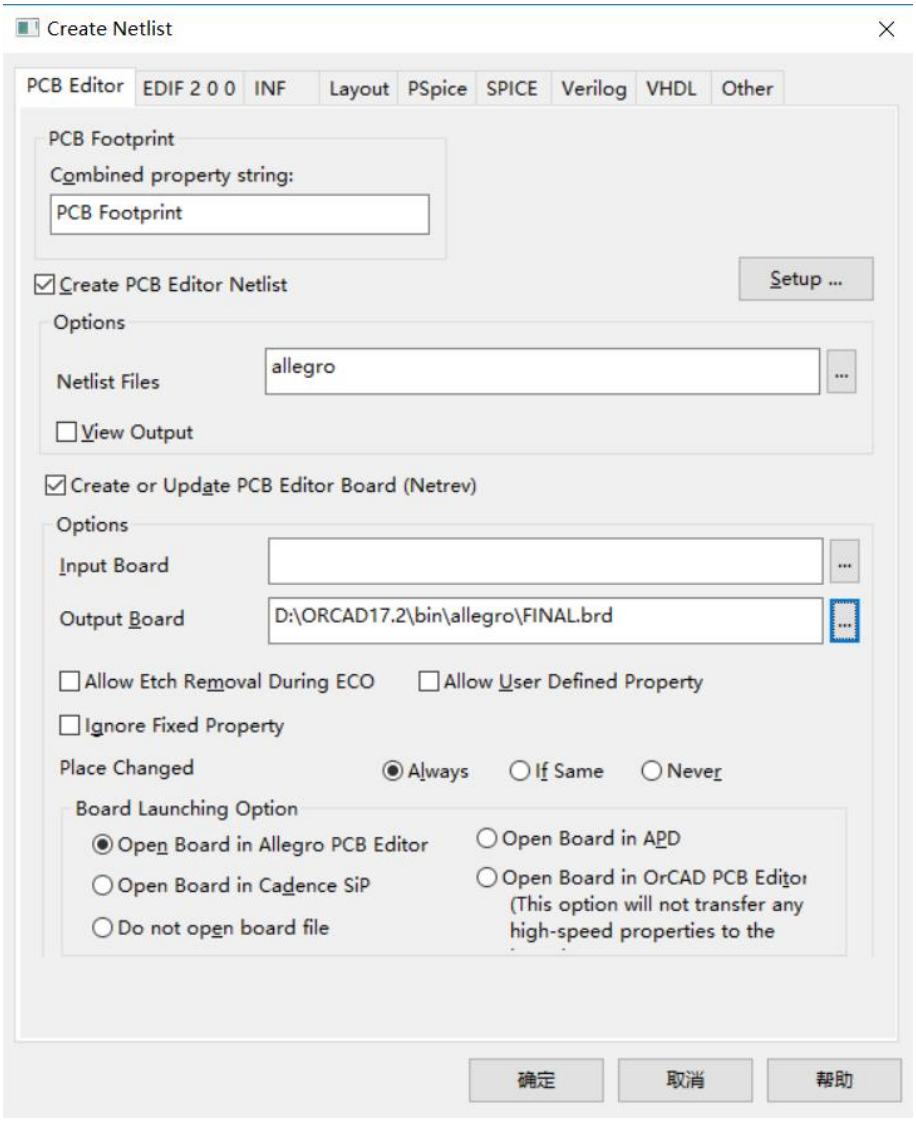

FIGURE 5.6: create netlist option

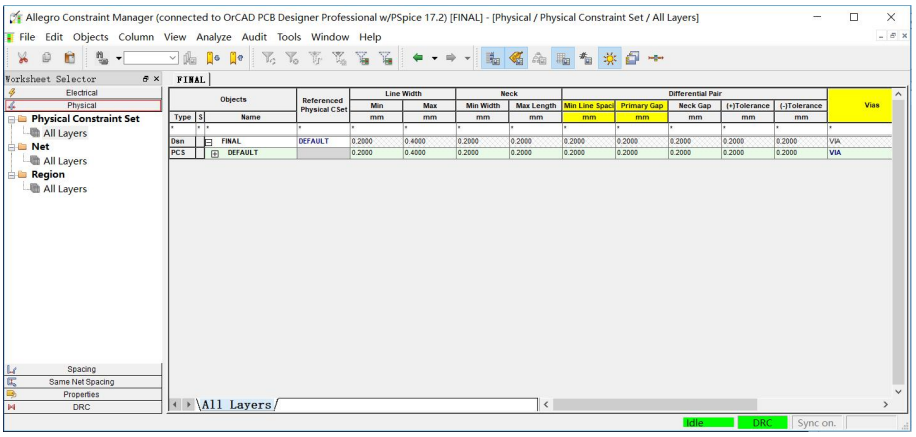

FIGURE 5.7: constraint manager

reasonably. We can rotate and mirror the components according to our demands. Showing in the figure 5.8, this is the layout of my design. After placing, routing all the flying

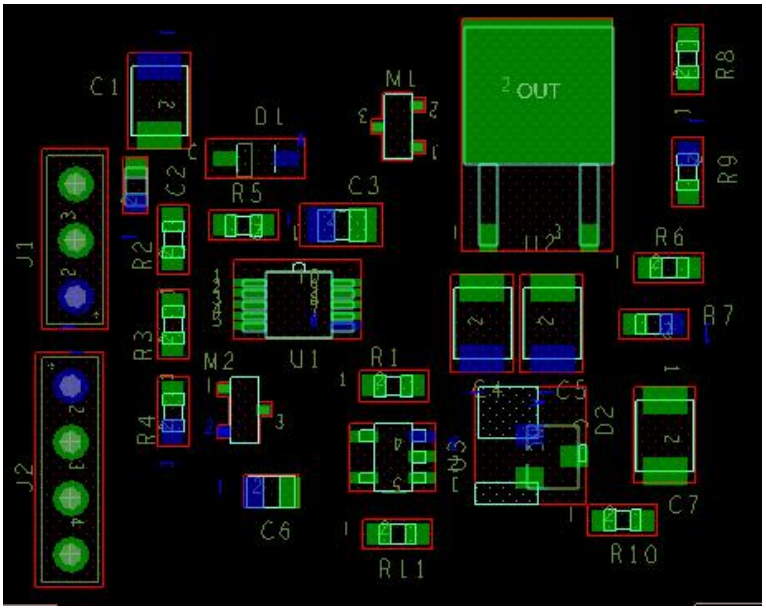

FIGURE 5.8: PCB layout

lines, and use the Add Via command to add vias at any time during routing, allowing the routing to travel between the top and bottom layers. And I also add a ground plane on the bottom of my PCB, so that I can use less wire and save space. The step is clicking the ”Shape” in the menu and select ”Rectangular”, the setting about options is shown in the figure 5.9. After adding the ground plane I need to connect the pins which need

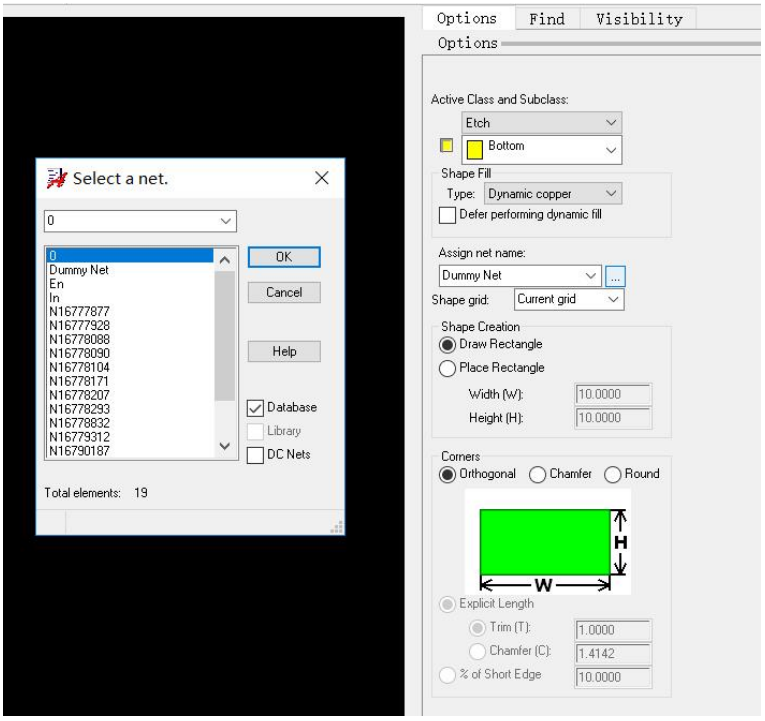

FIGURE 5.9: add ground plane

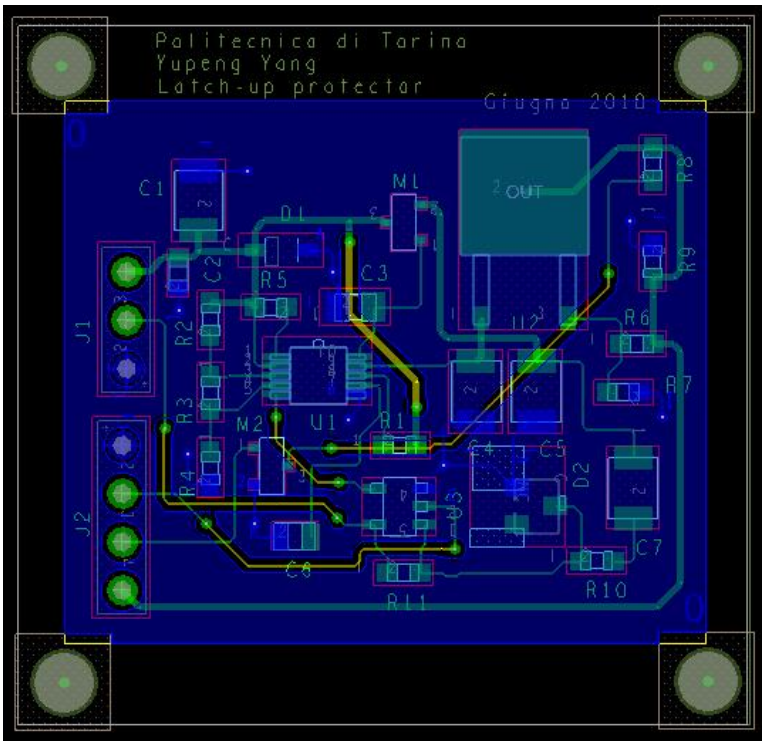

FIGURE 5.10: final layout view

to connect the ground to the bottom of the PCB. So, route such short wire on those pins and add via so that they are connected to the bottom. Place the plane cover all of the design, there are no existing flying lines. Add four holes on the four corners, and check the DRC if has errors or not and the final view of the layout showing in the figure 5.10.

5.3 Manufacture

To print the board, we need to provide Gerber files to PCB manufacturers. In the Gerber file editor General Parameters tab, Device type selects Gerber RS274X, Format Integer places: 3, Decimal places: 5, and then open the Film Control tab, add the required film, the general two-layer board, then you need TOP (top layer routing layer), BOTTOM (bottom trace layer), these two already get in the available films. Using the Color Dialog(showing in the figure 5.11) to make the other film file. First, click off on the Color Dialog to make all of the things not visible and then start making films, after each completion, it needs to use Color Dialog to make all of the things not visible again. I still need films like:

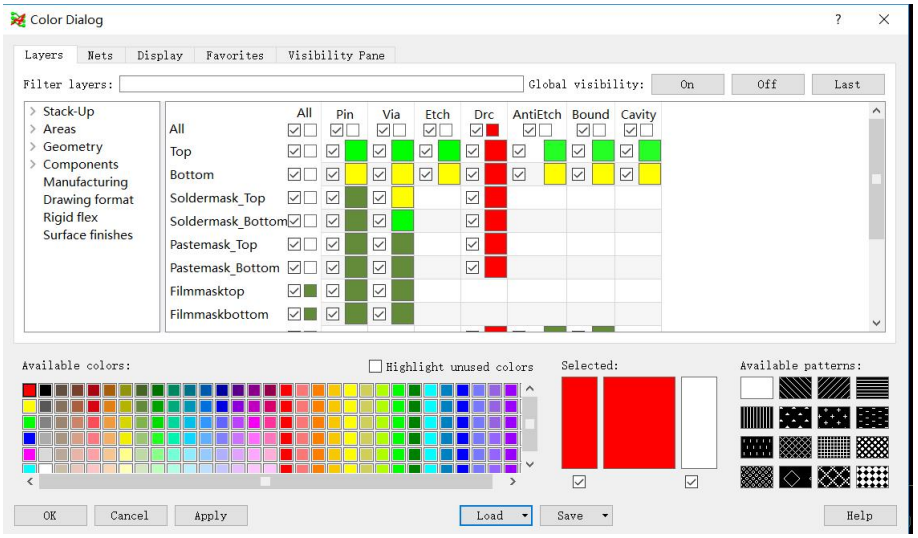

FIGURE 5.11: Color Dialog

FIGURE 5.12: Artwork Control Form

1. SOLDERMASK-TOP (top layer solder mask) and SOLDERMASK-BOTTOM (bottom layer solder mask) which contains subclass about soldermask top and bottom in the class such as Board Geometry, Package Geometry, Pin and Via class.

2. SILKCREEN-TOP (top screen printing) and SILKSCREEN-BOTTOM (bottom screen printing) which contains the subclass about silkscreen top and bottom in the class such as Board Geometry, Package Geometry and Ref Des.

3. PASTEMASK-TOP(paste protective on top layer) and PASTEMASK-BOTTOM(paste protective on bottom layer) which contains the subclass about pastemask top and bottom in the class Package Geometry, Pin and Via class.

4. OUTLINE of the board, use the outline under the Board Geometry class.

Show the Artwork Control Form in figure 5.12.

After adding the required film file, set the Undefine line width to 0.4mm, the others use the default value, and finally, click Create Artwork. After we get the Gerber file, we go to create the NC drill file from the ”Export” menu tab. Send these files we created in a package to the factory, and go to print it out. At this time I have already finished my PCB board design, after the board arrived, I need to assemble and test my board, will see in the next chapter.

Chapter 6

Assembly and Testing

In the last chapter I talked about how to get a Gerber file, and finally send it to the factory to print PCB. The figure 6.1 is the PCB getting from the factory. In this chapter, I will explain how to assemble the board and how to test it.

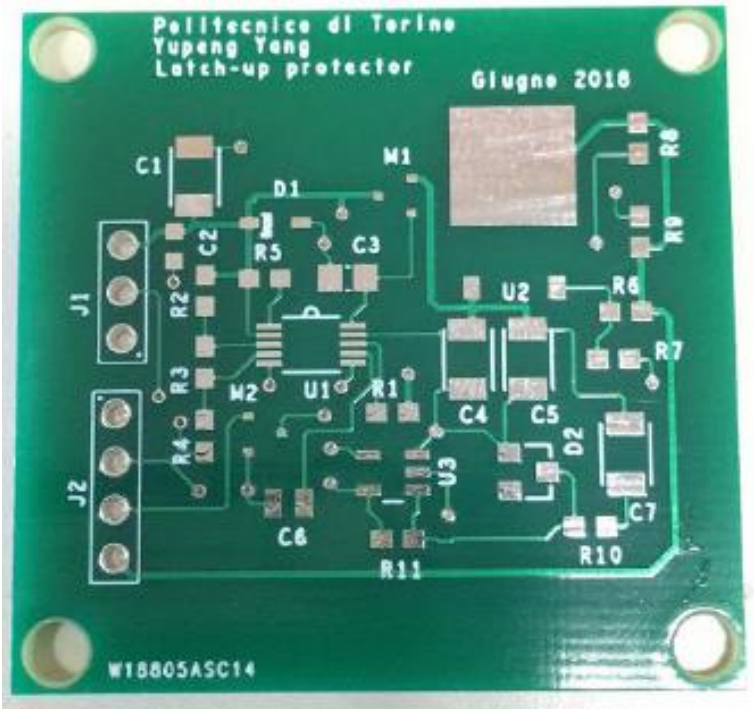

FIGURE 6.1: PCB of the design

6.1 Assembly

Soldering is a process in which two or more items (usually metals) are fused together and the filler metal (solder paste) is added to the joint. The melting point of solder is lower than that of adjacent metal. Soldering is different from welding because it does not involve melting the workpiece. In brazing, the filler metal melts at a high temperature, while the workpiece metal does not melt.

6.1.1 Solder Paste

Solder paste is a material used to make printed circuit boards. It is used to connect surface mounting elements to a solder plate on the board. We use the air gun to cover every pin on the PCB with solder paste. Because of my PCB is just 37mm*38mm, so I also need the Ergonomic stereo microscope (figure 6.2)whose wide range of magnification options up to 20x and it can also provide the LED lighting with real color vision, without shadows. Under the microscope, I use an air gun to print the solder paste on the solder mask of my PCB, remember don't print too much paste, it is possible to make components short circuit. In the figure 6.3, we can see the solder paste has already met on the board, it doesn't matter if the paste has been connected, because when after placing the components, we can use alcohol to clean it up.

6.1.2 Pick and Place

After applying the solder paste, placing the components is the next step. In this operation, I use EXPERT-M (figure 6.4) manual pick-and-place systems. They are widely used in prototype laboratories around the world. Single and multi-plate precision components can be assembled quickly and accurately. With expert systems, all kinds of components can be placed.

6.1.3 Reflow Oven

Reflow furnace is a kind of machine mainly used for surface installation of electronic components to PCB reflow welding machine. In this step, I use Infrared IC Heater T962 (figure 6.5)which is a microprocessor controlled reflow oven and adopts fast infrared

FIGURE 6.2: Ergonomic stereo microscope

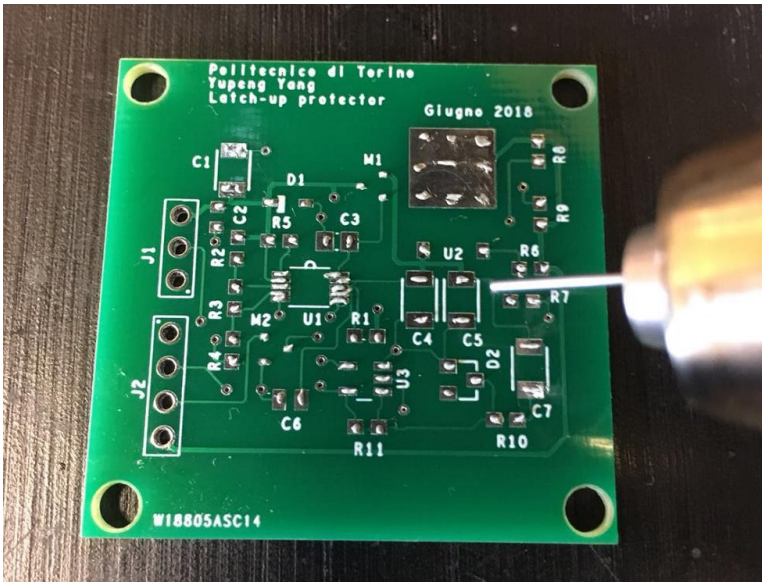

FIGURE 6.3: apply solder paste on PCB

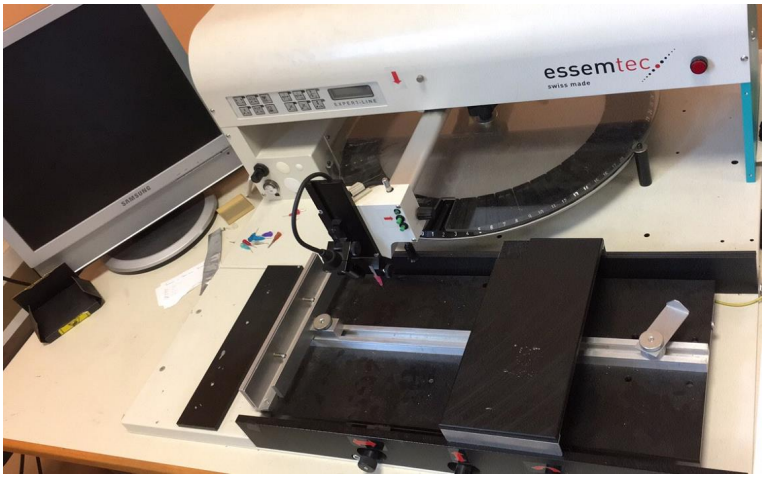

FIGURE 6.4: EXPERT System

radiation for heating and circular-wind to do temperature equalization, so the temperature in the drawer is very accurately and equilibrium. T962 can be used for automatic

FIGURE 6.5: Infrared IC Heater T962

"reflow" solder to correct defective soldering joints, remove/replace defective parts, and complete small engineering models or prototypes. Rapid infrared radiation and circulating wind heat are adopted to make the temperature very accurate and even. The accuracy of heat cycle is maintained through the closed loop microcomputer control of infrared heater, thermocouple and circulating air. The temperature curve setting is very important. There are eight temperature parameter waves provided, and I chose wave 3, which depends on the composition of the solder paste. The process cycle is about 8min,

and the whole welding process will be completed automatically. It's easy to operate.

The connectors should be soldered by manual, so finally the PCB of my design is

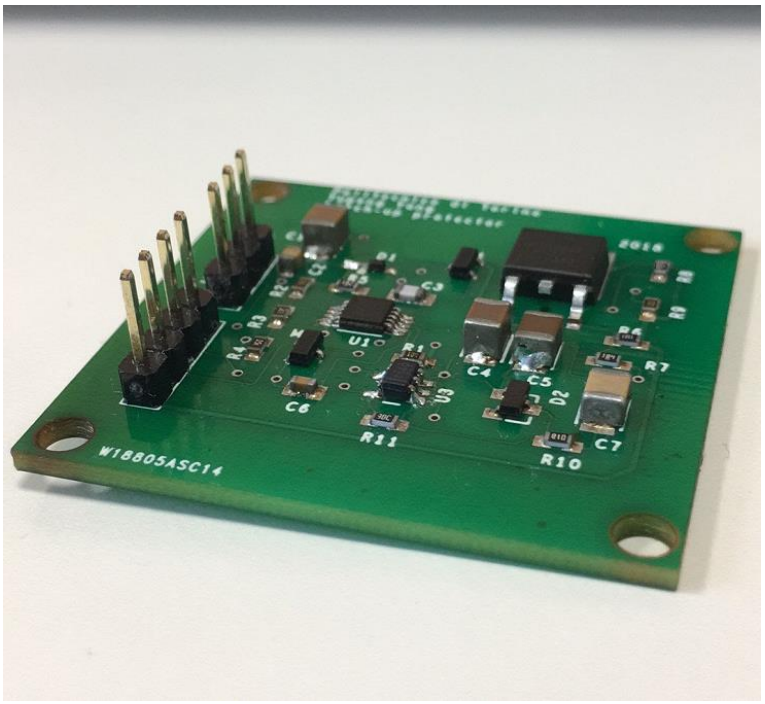

FIGURE 6.6: the final object

already finished, the final object is shown in the figure 6.6.

6.2 Testing

Testing is the last step in the entire design. Experiment to see if the physical object I get will have the same result as computer simulation.

6.2.1 Power supply

For my design, I need at least 2 power supplies, one is a 12V DC voltage which is given on the VDD, one is a 3.3V DC voltage which is given on the VCC and EN pin of the design. Use the signal generator to set a square wave whose range from 8V-0V, the period is 250ms, and the duty is 10%, because of the simulation, the auto-restart time takes about 130ms and still have some fault delay time, so this period is enough to see a whole working process.

One power supply machine and one function generator are needed to use. In my case,

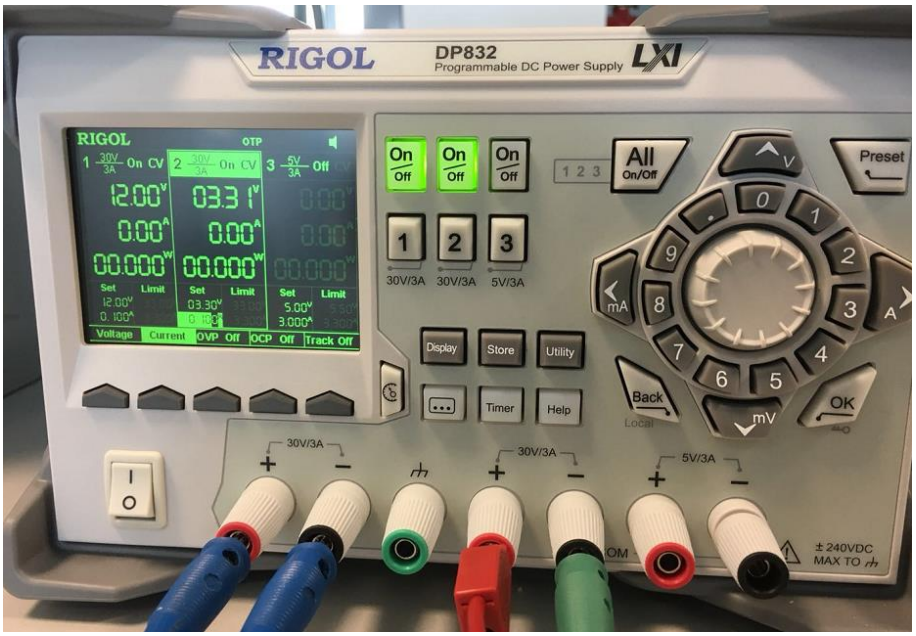

FIGURE 6.7: Rigol DP832 programmable DC power supply

FIGURE 6.8: DDS Signal Generator Hantek HDG2032B

I use Rigol DP832 programmable DC power supply(figure 6.7) to provide those two DC voltages that I need and use DDS Signal Generator Hantek HDG2032B(figure 6.8) to generate the signal voltage from 8V to 0V, this is used for triggering to test the board.

6.2.2 Testing Flow

- Set 12V and 3.3V on the DC power supply, turning them on and check the value with a multimeter, and then turn off.
- Set square wave voltage on the signal generator with 8V to 0V, period 250ms and duty 10%, connect the output on the channel 1 of the oscilloscope, turn it on, check the signal on the oscilloscope, and then turn it off.
- Connect 12V on the VDD, 3.3V on the VCC and EN, square wave voltage on the TRIGGER pin and connect the ground of the DC power supply on the two GND pins. At last, connect the OUTPUT pin on the oscilloscope channel 2.
- Check all the connections are set correctly or not, and turn on all the three inputs, turn on the channel 2 on the oscilloscope.
- Download the screenshot of the oscilloscope and turn off all the instruments.

Demonstrate the connection of each pin during detection using the block diagram in figure 6.9.

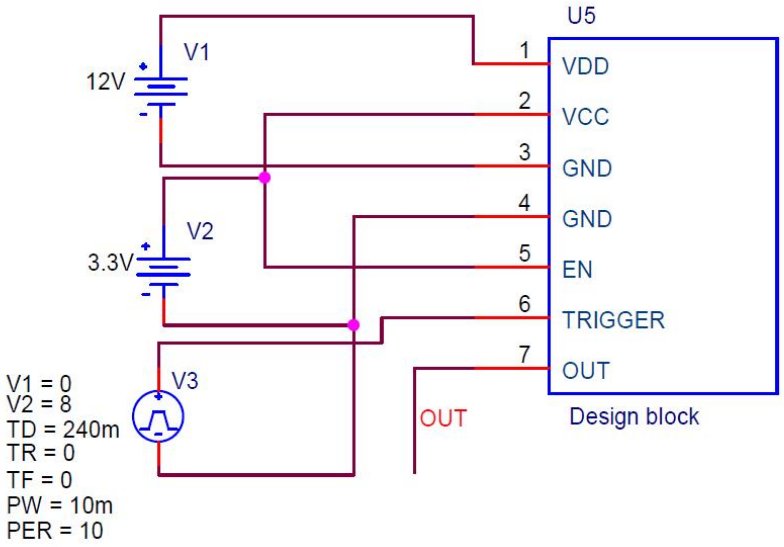

FIGURE 6.9: block diagram of design

The V1 is the power supply for the device which is 12V DC voltage, and the V2 is the power supply for the circuit and also for the EN pin, which is 3.3 DC voltage, V3 is a

signal generator which gives a square wave voltage to the TRIGGER pin. The VDD is connecting with the V1; the VCC and EN, they are connecting with the V2; the GND is connecting with the ground; the TRIGGER is connecting with the V3 and the CH1 of the oscilloscope; the OUT is connecting with the CH2 of the oscilloscope.

6.3 Problems Detected

6.3.1 Problems

There are four main problems in the PCB:

1. Between the footprint of LM5060 I used with the package of the LM5060, the OVP pin, and UVLO pin are inverted. Between the footprint of LM1117 I used with the package of the LM1117, the VIN pin, and ADJ pin are inverted.
2. Missing the output capacitor in the regulator LM1117 system, which makes the output stable.
3. The set resistors in LM1117(R_6 and R_7) are not used in typical range.
4. The LM1117 minimum working current is actually 20mA, it's NOT like showing in the datasheet, which just 5mA. Since the current limit is lowing to 20mA, so the whole system seems overcurrent inside.

Because I use the footprints which are downloaded from the website, I don't detect these two problems before, and also the simulation model of LM1117 is used from the internet, I didn't check the using range of those two resistors again from the datasheet. These take me a period of time to test it.

6.3.2 Solving Problems

For the first problem, first swap the positions of R_2 and R_4, and then connect the original GND of R_4 to VDD, and connect the original VDD of R_2 to the ground. The same method like before, just exchange the connection position of VIN pin and ADJ

pin.

For the second, just add one capacitor at the end of the output, which value is typically 100uF(C_8).

For the third, change R_6 to 200Ω and change the R_7 to 330Ω. Because after checked the datasheet of LM1117, can find that the range of R_6 is from 100Ω to 200Ω, and then follow the formulation:

$$V_{\text{OUT}} = 1.25 * (1 + \frac{R_7}{R_6}) \tag{6.1}$$

If I set R_6 to 200Ω, the R_7 should be 330Ω.

For the last one, I need to change the sense resistor(R_5), change it to the 8k2Ω, the current limit turn to around 24mA(ideal).

But these are only for the existing PCB has been modified, I still need to modify the PCB project. Because of the LM5060 and LM1117 templates downloaded on the Internet, there is a problem that the pin number does not match the number on the datasheet. I need to redraw these two.

First of all, in the library folder, select the one I have created, right-click it, and choose "New part" selection, and then it will appear like the figure 6.10

Type the name about the new part, and then enter edit version.

First to place rectangle for the new part, and then according to the datasheet, place the pins with the write name and number(figure 6.11), I just show the example to redraw the LM5060, the same operation to do to the LM1117. At last, don't forget to add the footprint for the new LM5060 and LM1117.

6.3.3 Test after modify

After modify the schematic the simulation results showing in the figure 6.12. I can measure all the value of simulation results easily, such like the current limit is 24mA, rise delay time is 2.2ms, the fault detection delay time is 9ms, the auto-restart time is 115.4ms when the fault persists there is a holding time 8ms.

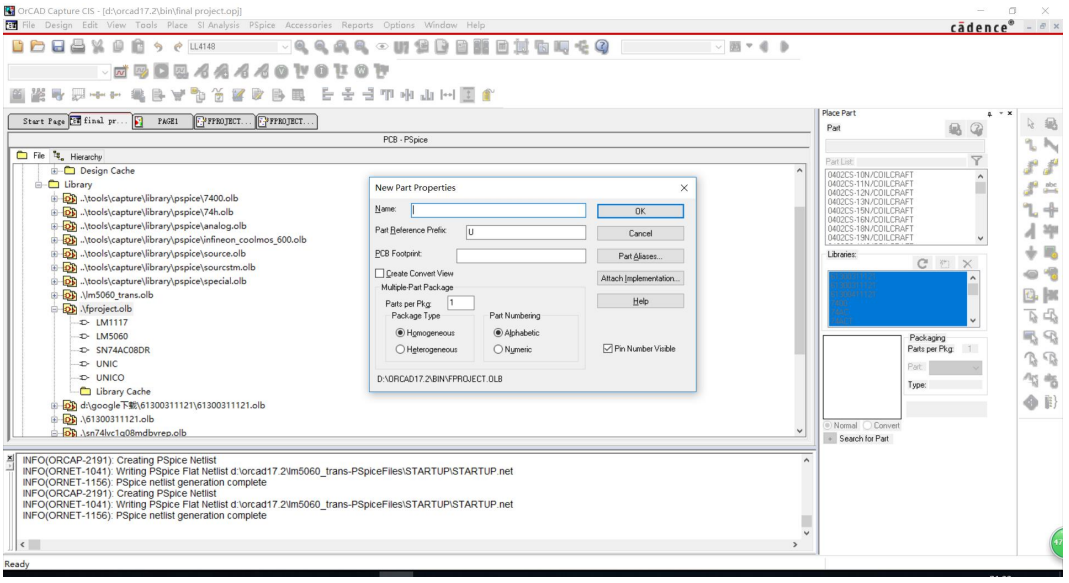

FIGURE 6.10: create a new part in the library

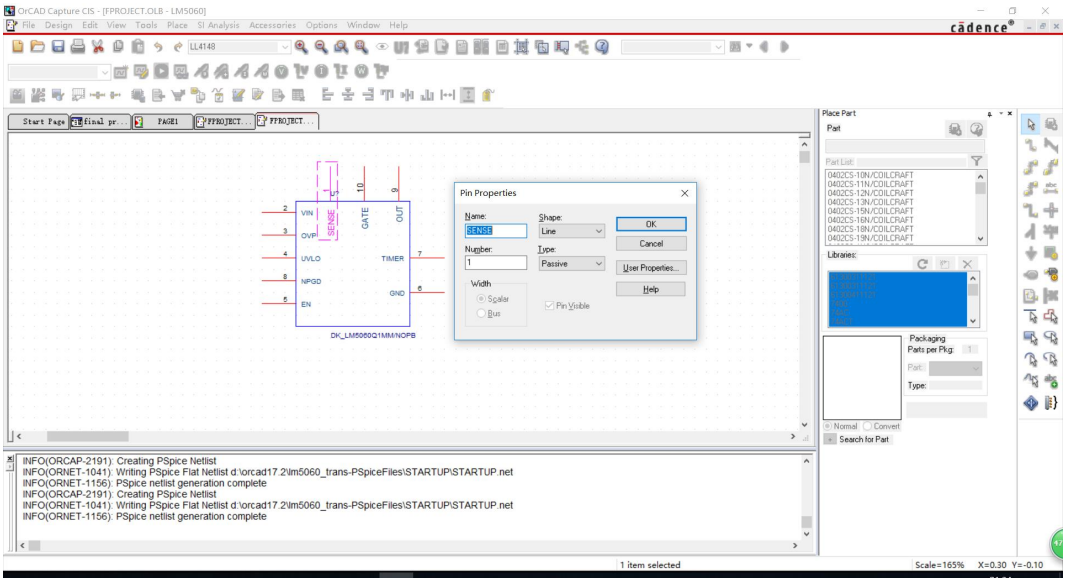

FIGURE 6.11: place the right pin name and number

Having said this, I need to explain what is the current limit, the fault delay time and the auto-restart time and holding time(just when the fault persists happen).

- Current limit: It is the threshold current that triggers the system for self-protection. It uses an external resistor R_5 at SENSE pin of LM5060 to set the threshold for fault detection.

- Rise delay time: It is the time required for the voltage of the regulator output goes from zero to a stable high state.

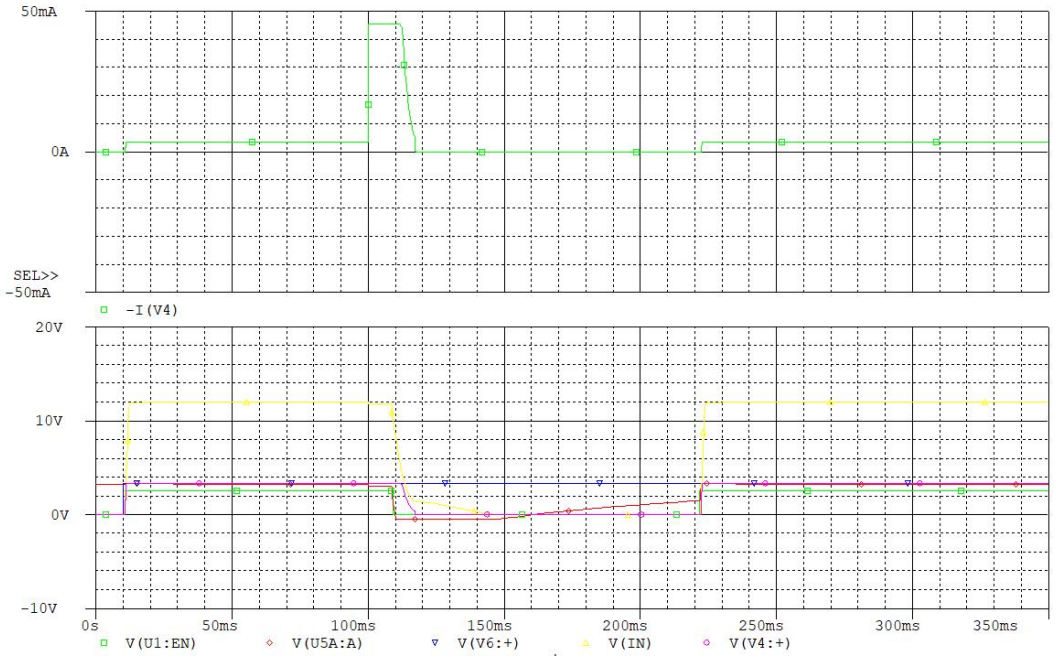

FIGURE 6.12: the simulation result afer change schematic

- Fault detection delay time: When the over-current occurs, the system needs a little time to detect the occurrence of an error. The time required is Fault detection delay time. It uses an external capacitor C_6 at TIMER pin of LM5060 to set the time size.

- Auto-restart time: It is the time required for the system to automatically return from the shutdown state to the normal operating state after performing the protection operation. It uses the capacitor C_7 in the RC circuit of the auto-restart circuit which I designed to control the time size.

- Holding time: When the system returns to normal operation from auto-restart with the fault persists, the time of the system maintains correctly working state is the holding time. After this time the system will back to the fault state.

As the schematic, I change the R_5 to 8k2Ω, and test again. But when I give TRIGGER voltage, nothing happens, seems the current limit is not just 24mA. So, I test the current limit is around 48mA for real, so the trigger current is not enough. So I change R_8 to 68Ω, which can let the trigger current around 49mA, it works. The new schematic showing in the figure 6.13, and the output which I use to trigger with a signal voltage to observe whether my design can work correctly, showing the wave on the oscilloscope in figure 6.14. On the oscilloscope, CH1 is the trigger voltage wave(yellow line), CH2 is

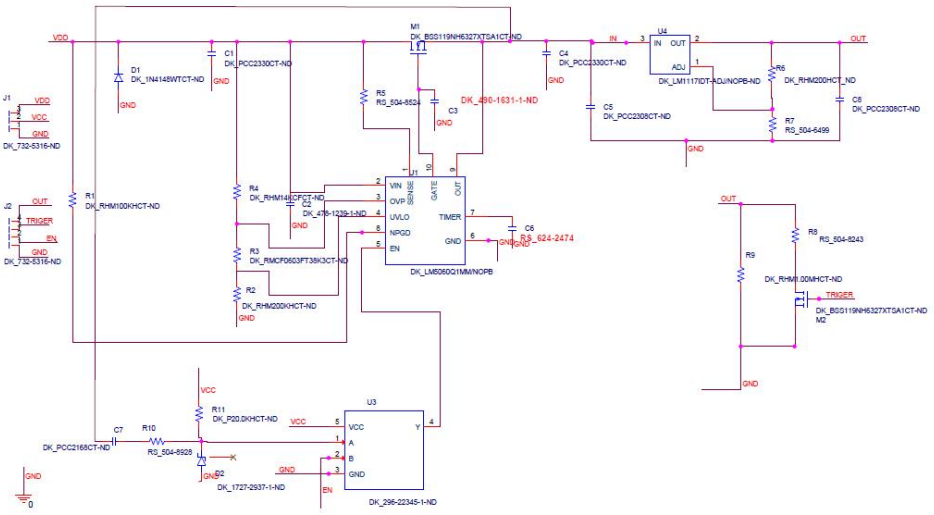

FIGURE 6.13: the new schematic

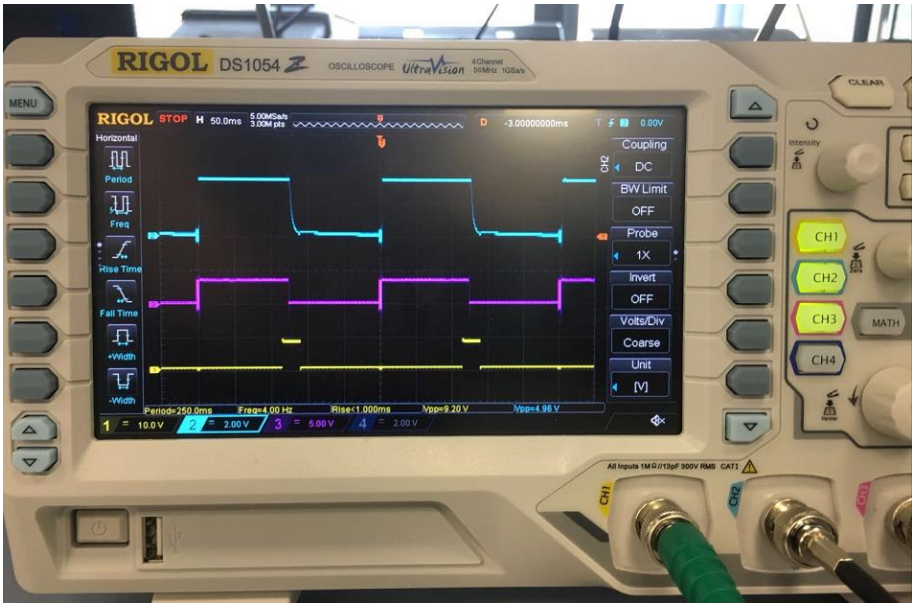

FIGURE 6.14: waves about a detected fault

the output wave(blue line), CH3 is the EN pin wave(purple line). Obviously, when the fault happens in the system, the system shuts down after a fault detection delay time. After about 130 ms, the fault no is longer exists, the system automatically restarts and resumes work.

Try another time with a persistent trigger voltage to keep the fault happening, showing the wave on the oscilloscope(figure 6.15), to make a persistent fault because it is easier to measure the values I need. Show the wave is already zoomed in the figure 6.16.

From the wave of the oscilloscope, we can clearly see that the unit of voltage is 2V,

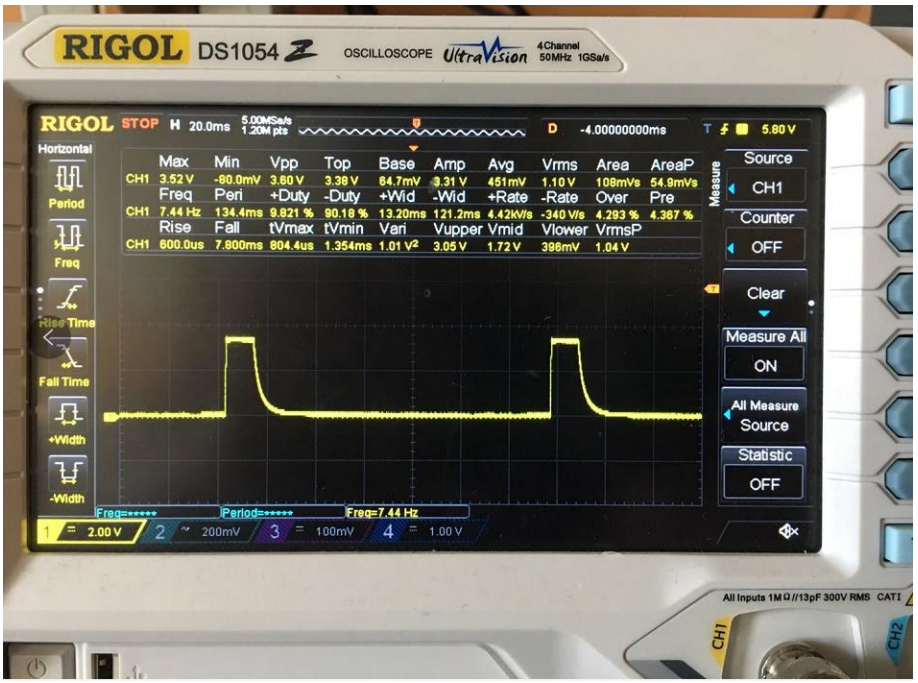

FIGURE 6.15: output wave about a persistent fault

FIGURE 6.16: output wave after zoom in

and the unit of the time is 5ms, so I can measure the rise delay time is 1ms, the fault detection delay time is 12ms, and the whole auto-restart time is 129ms. As the fault persists, when the system back to the able state, the holding time is also just 12ms, and then will be off again. With the testing is succeeding, I finish the whole design. The modified PCB is shown in the figure 6.17.

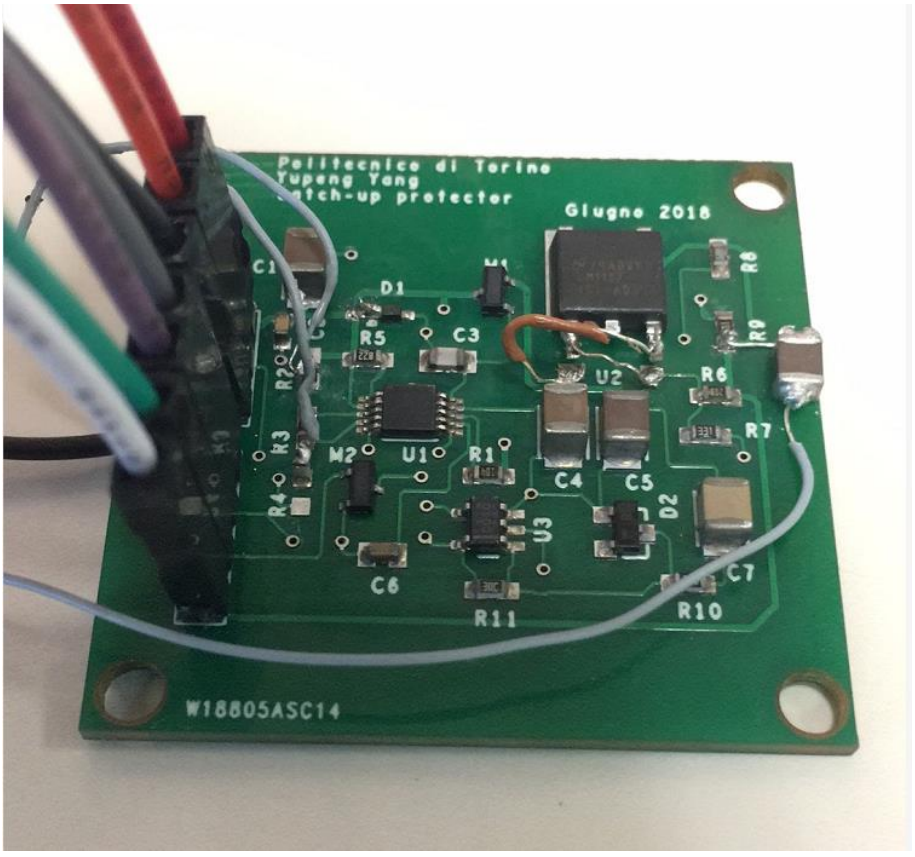

FIGURE 6.17: final modified PCB

6.4 Results

In summary, after successful detection of my design, some data can be obtained, including the current limit, fault delay time, restart time, rise delay time and so on. Can be demonstrated in Table 6.1, the result of the simulation is compared with the result obtained by the real test.

Result	Simulation	Testing
Current limit	24mA	48mA
Rise delay time	2.2ms	1ms
Fault detection delay time	9ms	12ms
Auto-restart time	115.4ms	129.2ms
Holding time	8ms	12ms

TABLE 6.1: Comparison of simulation and test results

By comparing the two results, we can know that there are significant errors in the results of real detection and simulation. However, it is often because these errors result in various problems in the detection. For example, in this design, the current limit error directly affects the current in the trigger module in the actual detection is not enough to make the design to achieve the state of over-current, and thus cannot get the true test results. Therefore, testing is the final key to the overall design and plays a decisive role.

Chapter 7

Conclusion and Prospect

7.1 Conclusion

This thesis focus on designing a protection system against latch-up for modular satellites, to achieve an overcurrent protection function. In this design, the final choice is determined by comparing a variety of different design methods using different components and designed a circuit to make all the system auto-restart. And also explained how to go through the circuit schematic to create a PCB and design a PCB board process in details. Finally, make a real PCB board about my design.

7.1.1 Significance of Design

CMOS circuits have the advantage of low power consumption that other circuits cannot match, and are the most promising circuit structures in the Ultra-Large-Scale-Integration (ULSI) field. However, the traditional CMOS circuit technology will produce an inherent latch-up effect, which limits its application. As far as possible to avoid, reduce or eliminate the formation of the latch-up, develop a system for latch-up protection of digital CMOS components and add it into the whole system is very necessary for better optimization of CMOS circuit. Fortunately, some achievements have been obtained finally.

7.1.2 Some Achievements

* Think of a variety of methods and choose the best one among them.
* The system has realized the function of the automatic restart after the circuit is turned off.
* Describes the detailed steps for PCB design through using Orcad PCB Designer.
* The actual object was made.

7.2 Prospect

7.2.1 Process Technique

In this paper, a lock protection system based on circuit level is designed. Most silicon insulators are naturally locked-in. A lock is a low resistance connection between the bathtub and the power supply rail. By adding a layer of insulating oxides (called grooves) around NMOS and PMOS transistors, a latch-resistant chip can be designed.
We can also use the method of reducing substrate crosstalk to prevent latch-up. Devices fabricated in lightly doped epitaxial layers grown on heavily doped substrates is a good choice. Observations indicate that reducing the inductance in the substrate bias is more effective than either physical separation or guard rings in minimizing substrate crosstalk[5]. Now, using Silicon-On-Insulator (SOI) technologies to reduce substrate crosstalk has been touted as a promising approach for fabricating advanced integrated circuits because of its advantage over bulk silicon circuits such as faster speed and improved radiation tolerance[6].
Although these technologies already exist, however, the process technology is relatively complicated and the higher cost issues still affect its widespread use.

7.2.2 Future

Circuit technology is more widely used because the technology he needs is simple and economical. In the future work, I think in order to prevent latch-up, circuit and process technology combine together, such as a method for manufacturing a transient voltage

suppressing array substantially following a manufacturing process for manufacturing a vertical semiconductor power device[7].

Or as I have told the TPS22945 which with fixed current limit and fixed auto-restart time. Maybe in the future work, we can develop such a current-limited load switch with shut off and auto-restart feature which can regulate the current limit value and auto-restart time. Anyway, this thesis is not the end but the start of the research.

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