Master Project Report

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Fabrication and characterization of microfluidic chips for implantable pumps

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Debiotech S.A

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3. Abstract

3.1 English

A new passive flow valve has been developed for drug infusion at a constant flow rate of 1mL/h and 1mL/day, independently of pressure variations. The design as well as the mechanical and fluidic simulations have already been carried out the past years. Based on this work, the pump has been built in the CMi cleanroom (EPFL) and then fluidic characterizations realised to compare these results with the one of the simulations. The pressure regulation is obtained from the deflection of a membrane against pillars to prevent a part of the fluid to flow until the outlet. The new device is made of three stacked wafers (SOI, Silicon and Borosilicate) that are patterned and then bonded together. Fluidic tests have been realized and they show a correct operation of the pump in terms of flow rate and pressure range. Other tests should be performed to better interpret the results and be able to improve the design.

3.2 French

Un nouveau type de régulateur de débit passif a été développé pour l'infusion de médicaments à un débit de 1mL/h et 1mL/jour, indépendamment des variations de de pression. Le design ainsi que les simulations mécaniques et fluidiques ont déjà été menés les années passées. A partir de ce travail, la pompe a été fabriquée dans la salle blanche du CMI (EPFL) et les caractérisations fluidiques ont été réalisées afin de comparer ces résultats à ceux des simulations. La régulation de la pression est obtenue grâce à la déflection d'une membrane contre des piliers, bloquant partiellement l'écoulement du fluide jusqu'à la sortie. Ce nouveau régulateur est composé de trois wafers empilés (SOI, Silicium, Borosilicate) qui sont usinés puis soudés ensemble. Les tests fluidiques ont été réalisés et ils montrent un fonctionnement correct de la pompe en terme de débit et de gamme de pression. D'autres tests devront être menés afin de mieux pouvoir interpréter ces résultats et ainsi améliorer le design.

3.3 Italian

Un nuovo tipo di regolatore di addebito passivo è stato sviluppato per l'infusione di medicinali ad un addebito di 1mL/h e 1mL/giorno, indipendentemente dalle variazioni di pressioni. Il design così come le simulazioni meccaniche e fluidica sono state condotte già gli anni passati. A partire da questo lavoro, la pompa è stata fabbricata nella sala bianca del CMI (EPFL) and le caratterizzazioni fluidica realizzate per paragonare questi risultati a quelli delle simulazioni. La regolazione della pressione è ottenuta grazie al deflection di una membrana contro i pilastri, bloccando una parte del fluido di trascorrere fino all'uscita. Questo nuovo regolatore è composto di tre wafers accatastati (Si, Silicio, Borosilicate) che sono designati e collegarono poi insieme. Le test fluidica sono state realizzate e mostrano un funzionamento corretto della pompa in termine di addebito e di gamma di pressione. Altri test dovuti stato condotti per potere interpretare meglio questo risultato e così migliorare il design.

4. Introduction

4.1 Debiotech S.A company

Debiotech S.A is a Swiss company based in Lausanne with more than 25 years of expertise in innovative medical devices. Its technology notably relies on microfluidic and micro-electronics devices (MEMS). Debiotech develops both implantable and non implantable pumps for different medical needs, in particular for drug delivery and dialysis. Two main products currently developed by Debiotech are the *DialEase*^{TM} which is device dedicated to peritoneal dialysis at home and the *JewelPUMP*^{TM} which is a patch pump for diabetic patients. Several implantable devices, like the *Chronoflow*^{TM} ones, have also been developed for hydrocephalus treatment and drug infusion at different flow rate and pressure level.

4.2 Presentation of the project

The goal of this internship is to develop a new *Chronoflow*^{TM} device aiming to deliver a very low and constant flow rate, defined at 1 mL/day and 1 mL/h, independently of the external pressure variation, for drug delivery like morphine. This kind of device is used for pain management, e.x for patients with cancer. The final goal is to show the competitive advantages of this new device over the other commercially available micropumps for the patient, mainly by limiting the risk of overdose. The design of the chip has been carried out in the past [1], [2] and now micromachining in cleanroom needs to be performed as well as the fluidic characterizations on these samples to demonstrate experimentally the working principle of such ultra-low flow control valves for implantable pumps.

At the end of the report, the report of the total costs (Appendix A) and the Gantt diagram (Appendix B) of this project are reported.

4.3 Working principle of the Chronoflow pump

The ultra low flow rate *Chronoflow*^{TM} device (cf. Figure 1) is a passive valve able to deliver a constant flow independently of the pressure applied on the membrane. The pressure and the flow rate are linked according the following equation (Eq.1) :

$$Q = \frac{\Delta P}{R_f} \qquad \text{(Eq.1)}$$

Where Q is the flow rate, ΔP is the difference of pressure between the inlet and the outlet, and R_f is the fluidic resistance.

Moreover, the flow is assumed to laminar (Re << 1000) where Re is the Reynolds number defined as (Eq.2) :

$$Re = \frac{\rho * v * L}{\mu} \quad \text{(Eq.2)}$$

Where ρ is the density of the fluid, v is the fluid velocity, L is the micro channel diameter in which the liquid flows and μ is the dynamic viscosity of the fluid. Knowing that for this kind of pump $\rho \approx 1000\ kg/m^3$, $L \approx 100\ \mu m$ and $\mu \approx 10^{-3} Pa.s$ it means the velocity need to be lower than 10 m/s which is indeed the case.

According the Eq.1, in order to keep a constant flow rate when the pressure on the membrane increases, the fluidic resistance should be a linear function of the pressure gradient ΔP. It is possible, by properly designing pillars which face the inlet holes and which will be put in contact with the deflected membrane when the outside pressure increases [3].

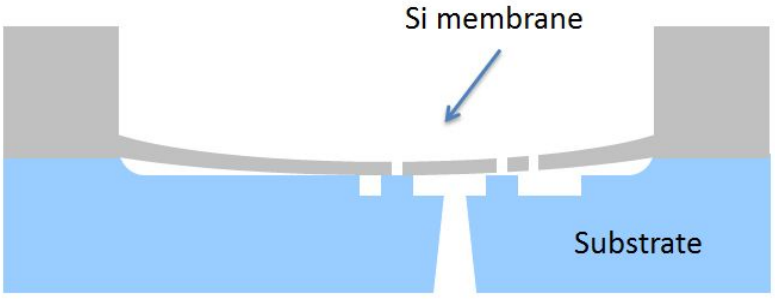

Figure 1 : Cross view of a classical *Chronoflow*™ pump design

5. Comparative study

In order to know what are the advantages of the new *Chronoflow*™ pump over the already existing micro pumps on the market and to develop a packaging in adequacy with the ones that the clinicians are used to work with, a comparative study of the main competitors of Debiotech has been carried out. The characteristics of the pumps in terms of flow rate, accuracy and components are analysed in the following part.

Five main competitors around the world are developing micro implantable pumps for drug delivery at constant and low flow rate. The table below (cf. Table 1) is a summary of the different models of the pumps on the market with the flow rate they can deliver and the compatible drugs.

Manufacturer	Model	Reservoir (ml)	Constant flow rate (ml/day)	Drug
Medtronic	Isomed	20	0.3 / 0.5 / 1 / 1.5	5FU, morphine
Medtronic	Isomed	35	0.5 / 1 / 1.5 / 2 / 2.5	5FU, morphine
Medtronic	Isomed	60	0.5 / 1 / 1.5 / 2 / 2.5 / 3 / 3.5 / 4	5FU, morphine
Johnson&Johnson	Codman 3000	16	1	5FU, morphine, baclofen
Johnson&Johnson	Codman 3000	30	1.2	5FU, morphine, baclofen
Johnson&Johnson	Codman 3000	50	2.5	5FU, morphine, baclofen
Tricumed	IP2000V	20 / 35 / 40 / 60	0.25 / 0.5 / 0.8 / 1 / 1.3 / 1.5 / 2 / 3	morphine, baclofen
Pfizer	Infusaid 400	50	From 1 to 6	5FU, morphine, baclofen
Flowonix	Prometra II	20	From 0 to 28.8	morphine, baclofen

Table 1 : The different models of the existing micro-implantable pumps

All these pumps can deliver drugs at a flow rate in the range of 1mL/day and are purely mechanical pumps, except the Prometra II of Flowonix which works with a battery and a micro-controller to regulate the flow rate. Moreover, most of the components are shared between the different designs and technology, in particular :

- Four suture loops to allow the surgeon to properly sew the pump into the patient's body and limit the post-implant complications.
- A reservoir filling port to regularly refill the reservoir with a self-sealing septum to avoid leakage from the reservoir.
- A catheter access port to realize bolus injection if needed, with a self-sealing septum to avoid leakage from the catheter.
- A "needle stop" at the bottom of the two access port to allow the clinician to know when the syringe is correctly placed for the injection.
- A bacteria filter with pores of 0.22µm to avoid the clogging of the catheter entrance.
- A drug reservoir to deliver medication to the patient for several weeks.
- A propellant chamber and a pump drive with a gas at 2.5bar to maintain a constant flow rate delivery.

The Figure 2 below is a cross view of the Codman3000 pump from Johnson&Johnson, with the aforementioned components.

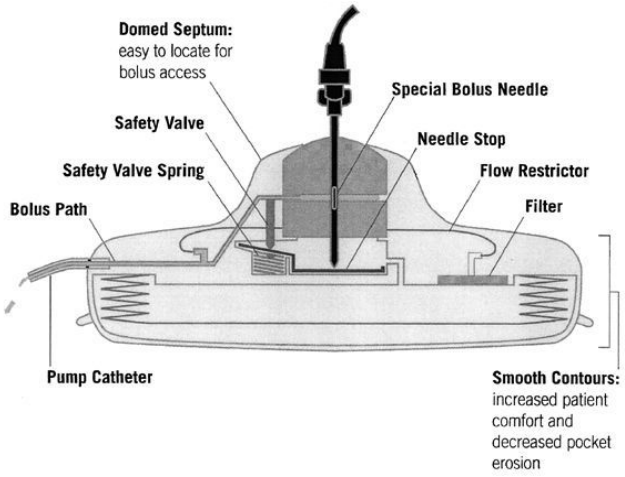

Figure 2 : Cross view of the Codman3000 pump

Even if most of the components are shared with all the pumps, they have their own technology to deliver the expected flow rate and it is dramatically dependant of external parameters called patient-related variables, such as the body temperature of the patient, his altitude above the sea level as well as the drug viscosity. When the pump is used out of the nominal value of these parameters, the accuracy of the flow rate can vary and the real dose delivered can be harmful for the patient. The following table (cf. Table 2) shows the variation of the nominal flow rate for different patient-related variables. These data are extracted from the datasheets of the pumps [4], [5], [6], [7], [8] and [9].

Source of flow rate error	ISOMED	Codman3000	IP2000V	Infusaid 400	Prometra II
Nominal	+/-12%	+/-14.9%	+/-10%	x	+/-14.5%
Pressurized cabin	+14.5%	x	x	35%	x
Altitude +2740m	+16%	+50%	+10%	62%	+1.8%
Altitude +1520m	+9%	+30%	+8%	+35%	+1%
Altitude +460m	+2.5%	+10%	+3%	+10%	+0.3%
Body fluid pressure (200 mmHg)	-12%	x	x	x	x
Body temp. 37°C to +43°C	+29%	+64%	+30%	+69%	-1%
Body temp. 37°C to +39°C	+10%	+29%	+10%	+23%	-0.3%
Body temp. 37°C to +35°C	-9%	-20%	-10%	-23%	+0.3%
Visosity of 1.1 cP	-9%	x	x	Influence mentionned	x
Visosity of 0.9 cP	11%	x	x	but no figure	x

Table 2 : Comparison of the nominal flow rate variation of the different pumps due to patient-related variables

We clearly see that all the pumps whose working principle principle is purely mechanical suffer from important flow rate variation as soon as the patient has fever or doesn't live on the seaside and these variations are additional. For instance, in the case of a Codman3000 pump, if the patient lives at 1500m and has a body temperature of 39°C since he is sick, the over infusion of drug is about 60%. It can be very harmful, even worse for patients suffering from cancer and thus who are already weakened.

The new *Chronoflow*^{TM} pump design needs to deal with these issues to avoid such effects.

6. Design

The design commonly used by Debiotech for the *Chronoflow*^{TM} pumps is composed of two stacked wafers (cf. Figure 1). The top one is the membrane with the inlets channels while the second one contains the cavity and pillars to regulate the flow, and the outlet channel.

This design is convenient for moderate or high flow rate (from 10 to 100 mL/h), but not anymore for very low flow rate such as 1 mL/h or 1mL/day. Indeed, to be able to keep a constant flow rate accurately over a wide range of pressure gradient, the fluidic resistance R_f needs to be very high. It means that the inlet channels must have a very small diameter and consequently, because of the tolerance errors induced during the micro-fabrication, the accuracy of the flow rate is impossible to guarantee.

That is why, for the new ultra low flow rate design, the inlet channels cannot be anymore on the membrane but are placed in the same wafer than the outlet. The control of the fluidic resistance is obtained by precisely etching micro-channels where the liquid will flow before entering in the cavity (cf. Figure 3). By calculating the appropriate length and cross section area of these channels, the desired fluidic resistance can be tailored as shown by H. Musard [1] for both the flow rates. As a result, four channels of different lengths will be patterned for a single pump. These channel lengths are different for the pumps with a flow rate of 1mL/day and 1mL/h.

Thus, the new design (cf. Figure 3) is composed of three stacked wafers : a top SOI wafer acting as a membrane, a middle Si wafer with the channels and pillars and a bottom Borosilicate wafer for the inlets and outlet channels. The three wafers are sealed by an anodic bonding process. The liquid comes from the bottom, flows in the micro-channels, goes through the inlets which are not deflected against the pillars and eventually goes through the outlet in the substrate.

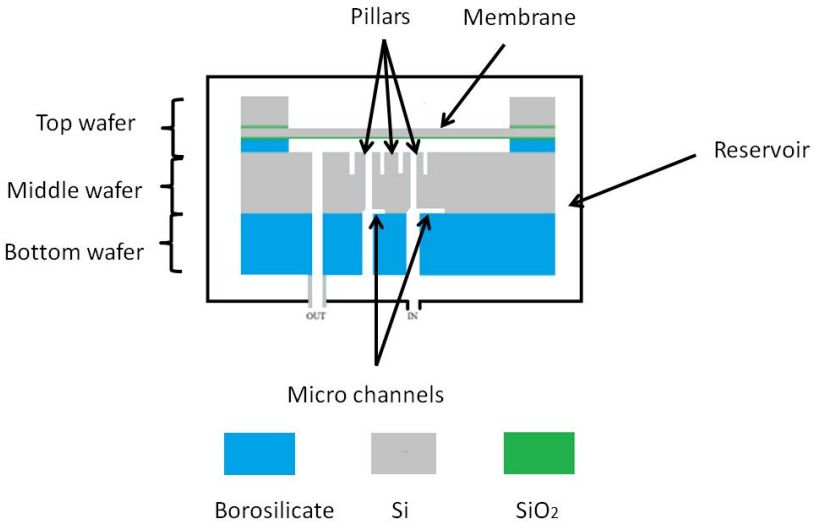

Figure 3 : Design of the new *Chronoflow*^{TM} pump

7. Micro-fabrication

This part describes the complete micro-fabrication of the new ultra low flow rate regulator at the EPFL cleanroom (CMi). The masks layout, the full process and the associated updated runcards are presented respectively in Appendix C, Appendix D and Appendix E.

7.1 Membrane

The top wafer, used to create the membrane of the pump (cf. Figure 3), is a SOI wafer with a BOX of 2µm at 50µm depth with a thin oxide layer on both its faces. Except where there are membranes, a 20µm layer of glass has been deposited on the frontside by an external company, *LithoGlass GmbH,* to facilitate the anodic bonding.

This process, up to the glass deposition by *LithoGlass GmbH* has already been done. The end of the process requires only one lithographic step to open the membrane of 400µm depth, by a dry etching and then to remove the silicon oxide at the back side of the wafer.

A SOI wafer has been chosen to allow an accurate etching of the membrane thanks to the buried oxide acting as an etch stop.

7.2 Micro channels and cavity

The middle wafer (cf. Figure 3) is a Si wafer with 1µm silicon oxide layer on both its faces. This wafer allows to pattern the micro channels and the cavity in which the liquid will flow (cf. Figure 4).

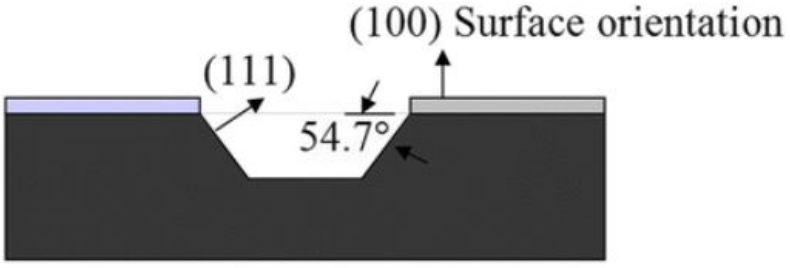

Figure 4 : Cross view of the micro-channels

Its fabrication is very critical and needs to be accurately realized to obtain the right fluidic resistance and thus the correct flow rate. Moreover, there are two different micro channels patterned on the wafers which represent the two different expected flow rates. For the flow rate of 1mL/h, the width of the micro channels is 100µm whereas it is 17.5µm for the micro channels which have to deliver 1mL/day. The all process requires four lithographic steps :

- Etching of the micro channels with a depth of 12.40µm.

The etching of the channels has been realised by an anisotropic wet etching in a bath of KOH at 40% at 60°C with a calibrated etch rate of 19µm/h. This anisotropic etching is possible by using the KOH whose etching rate is highly dependent on the crystal directions. It displays an etch rate selectivity 400 times higher in <100> crystal directions than in <111> directions.

In addition of the micro-channels depth, their length is also important to have the expected fluidic resistance. But due to the anisotropic wet etching, the shape of the etched micro-channels inputs is not exactly the same than the one on the layout (cf. Figure 5), leading to a reduction of the channel length.

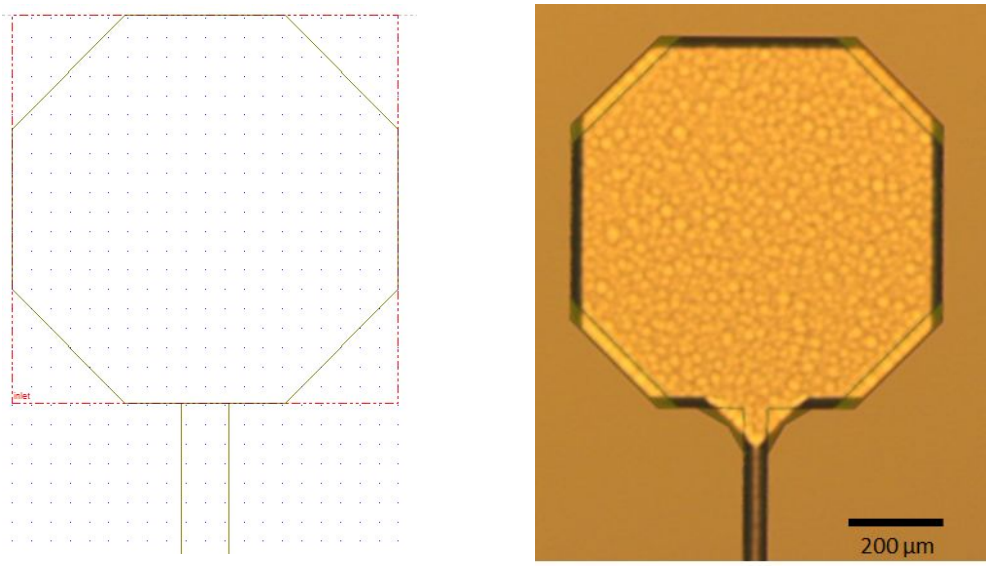

Figure 5 : Difference between the shape of the micro-channel input on the layout (left) and after etching (right) for the 1mL/day pump

We clearly see on the top right figure, the roughness as well as the triangular shape at the input of the channel which modifies the channel length and so the fluidic resistance, which are characteristic of the silicon wet etching. The tables below (cf. Table 3 and Table 4) compares the different channel lengths as designed on the layout and the measured ones after the wet etching for the two different flow rates pumps. The four different channel lengths correspond to the four micro channels which composed a single micro pump.

	Flow rate : 1mL/day			
Layout length [µm]	1070	2000	2070	4010
Patterned length [µm]	1003.25	1935.16	2133.23	3941.37
Delta length [µm]	66.75	67.84	66.77	68.63
Relative error (%)	6.24	3.39	3.04	1.71

Table 3 : Comparison between the expected and patterned channel length for the 1mL/day flow rate pump

	Flow rate : 1mL/h			
Layout length [µm]	1285	2185	3790	3790
Patterned length [µm]	1220.19	2117.24	3725.17	3723.27
Delta length [µm]	64.81	67.76	64.83	66.73
Relative error (%)	5.04	3.10	1.71	1.76

Table 4 : Comparison between the expected and patterned channel length for the 1mL/h flow rate pump

As a consequence, the wet etching reduces the channel length of around 65-70µm corresponding to an error between 1.7% and 6.3%. The layout lengths of the micro-channels have been evaluated again by simulation to take into account this over etching to obtain the right fluidic resistance after the etching.

After having modified the channels layout, a new batch of wafers have been processed. The measured depth has been done with the surface profiler Bruker Dektat XT for the four channels of each pump for the four samples. Within this range of depth, it as a vertical resolution of 8.0nm. The table below (cf. Table 5) shows that the average measured depth for each channel of the 1mL/h pumps and their global relative error with the expected depth of 12.40µm :

Wafers ID	5725	5726	7653	7655
Average channel 1 depth [µm]	12.47	12.50	12.48	12.43
Average channel 2 depth [µm]	12.43	12.47	12.44	12.41
Average channel 3 depth [µm]	12.48	12.50	12.50	12.43
Average channel 4 depth [µm]	12.45	12.48	12.47	12.42
Total average depth [µm]	12.45	12.49	12.47	12.42
Relative error (%)	0.44	0.69	0.58	0.19

Table 5 : Measured depth of the micro channels after wet etching

The difference of depth between the different wafers can be due to the bath temperature which is not perfectly homogeneous despite the pumping system as well as a variability during the measurement since only one measure along each channel has been done. According to this table, there is a difference of around 50nm compared with the expected depth which correspond to an over etch of only 10s over more than half an hour of process.

- Etching of the holes for the inlets and outlets.

This step allows to pattern a part of the inlet and outlets channels that will be then connected to their second part, patterned in the Borosilicate wafer.

The 350µm etching is done by Deep Reactive Ion Etching (DRIE) with the BOSCH process. Since it is a deep etching, a 15µm of AZ9260 photoresist has been coated and baked in a oven at 80°C for a night. Unfortunately it was not sufficient and the resist burnt during the etching because solvent bubbles was remaining in the resist (cf. Figure 6).

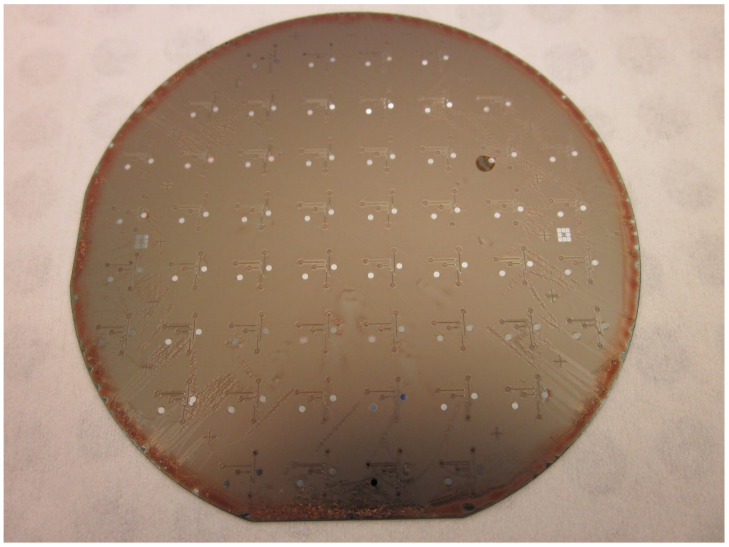

Figure 6 : Burnt wafer after etching

As a consequence, it was necessary to calculate the minimum thickness needed to be not totally etched during the process. According the characteristics of the AMS200 used for the etching, the selectivity between the photoresist and the silicon is 75:1. A theoretical thickness of at least 4.7µm was thus needed. But due to the presence of the microchannels on the wafer leading to sharp angles between the different structures, the coating would not have been uniform and some parts of the channels could have been coated with less of resist which would have led to an over etch of the channels and so to a modification of the expected flow rate. To be sure to avoid this and according to the recipes available on the ACS200 used for the photolithography coating, a AZ9260 photoresist of 8µm has been used.

In this second trial, no problem occurred for the resist during the etching but the etching rate was faster than expected and instead of etching 350µm, the holes totally goes through the wafer. Indeed, the etching rate is highly dependent on the design and mainly on the diameter of the hole. The larger they are, the faster they are etched. Consequently, it was impossible to go further in the process.

For the next attempt, in order to obtain an accurate etching rate and to avoid the problem of over etching, a calibration of the etch rate has been done after 15 min of process by focometry with an optical microscope, the Nikon Optishot 200. The focometry consists in focusing first on the surface of the wafer and then to focus on the bottom of the hole and to measure the variation of focal length. This technique allows to measure a depth with a precision of +/- 5µm. Thus, the depth of the obtained holes was between 340 and 360µm which is in the range of the expected value.

- Patterning of the anti stiction pattern.

Anti stiction pattern consists in a structuration of the surface. The contact surface between the membrane and the pillars is limited at high pressure, preventing any effect of squeeze film. Furthermore, this structuration is also mandatory to prevent stiction during anodic bonding. To do this, pillars with a diameter of 50µm and a height of 2µm are

patterned by a backside photolithography before being etched, at the center part of the pump, where there the membrane deflection is maximum.

- Etching of the pillars to keep constant the flow rate when the pressure increases.

The last step consists in the patterning of the pillars, with a 50µm DRIE, on which the membrane will deflect according the pressure and thus keeping the flow rate constant. This step finishes also the etching of the inlets and outlets through the wafer.

At the end of the process, the Silicon wafer looks like as shown on Figure 7.

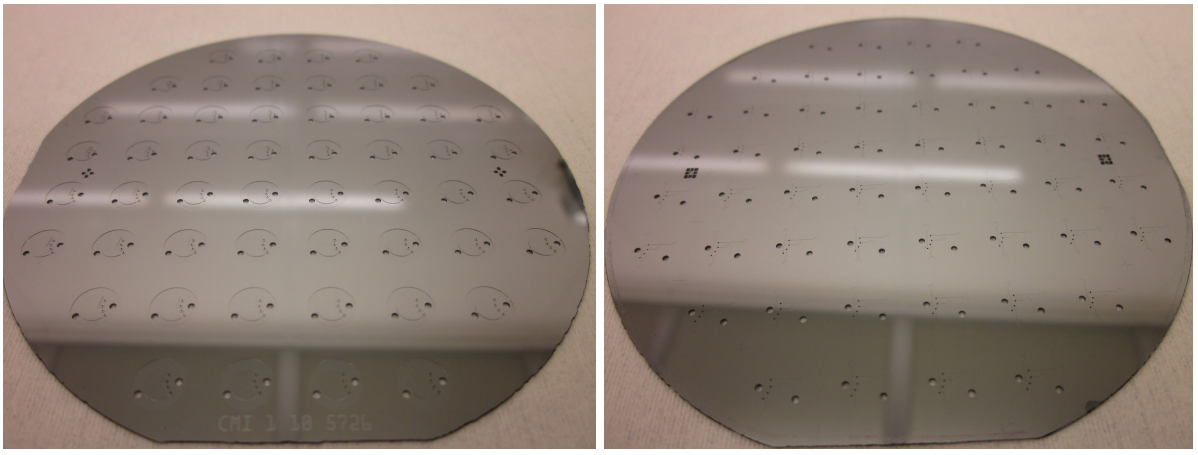

Figure 7 : Frontisde (left) and Backside (right) of the silicon wafer

7.3 Inlets and outlet channels

The bottom wafer, used to create the inlets and outlet channels as well as the alignment marks for the anodic bonding, is a Borosilicate (glass) wafer.

To realize the alignment marks, a lift-off process with an aluminium mask is used. The detailed process can be seen in Appendix D.

A negative resist has been chosen here for two reasons :

- The exposition is faster since only the marks needs to be exposed
- Thanks to the negative slope of the resist, the lift-off will be easier

The opening of the inlets and outlets channels is realized by sandblasting (cf Figure 8) by the company *Icoflex Sarl* (EPFL).

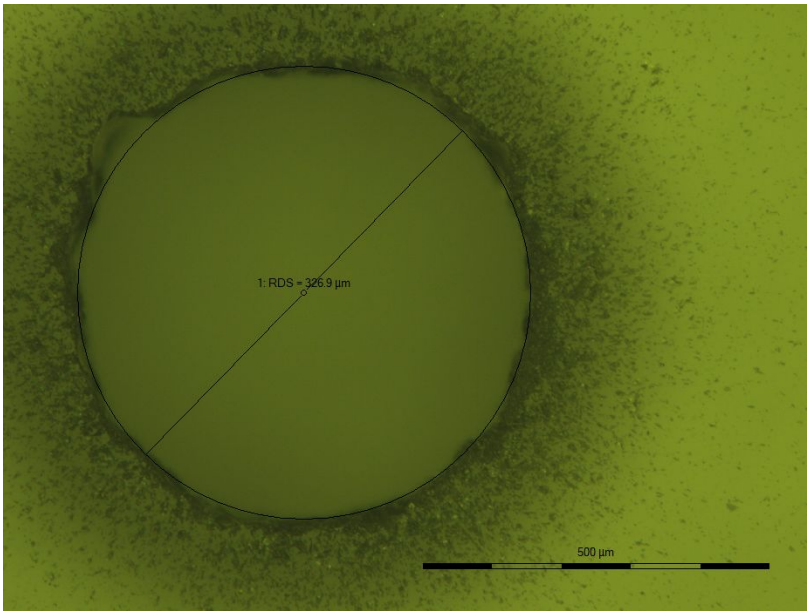

Figure 8 : Opening of an inlet after sandblasting by *Icoflex* (EPFL)

The targeted diameter of the inlet was 600µm, which is a bit lower than the measured opening sizes which is about 650µm. This difference will not really affect the design since the fluidic resistance of the inlets and outlets is not critical. Indeed, the fluidic resistance is mainly driven by the one of the micro-channels.

7.4 Anodic bonding

The last step of the process consists in the anodic bonding of the three wafers. This technique is commonly used to bond a silicon wafer with a glass wafer and has been described for the first time in 1969 [10]. To do so, the two wafers are put in contact at a temperature around 350°C and a voltage from 250V to 1000V. The oxygen ions contains in the glass move to the surface to form with the silicon atoms, a thin and very strong layer of silicon dioxide as depicted on Figure 9. The process continues until the current reaches a certain value, given as a percentage of the maximum current. To achieve a complete bonding, a current value of 5% of the maximum current is generally taken.

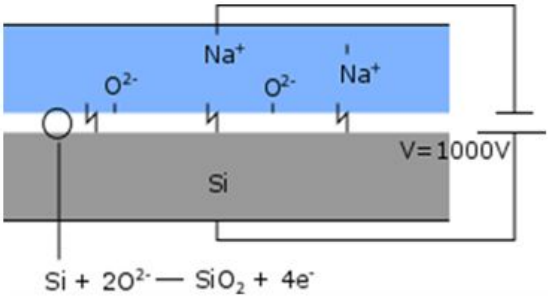

Figure 9 : Working principle of a silicon-to-glass anodic bonding

Right before the bonding, the 1µm of SiO2 on both sides of the silicon wafers are removed by using a BHF bath, composed of NH4F(40%):HF(50%) at 7:1, as well as the aluminium layer, which also acts as a protective layer on the borosilicate wafer. Then, the wafers are cleaned in a Piranha bath (H2SO4 at 96% with 200mL of H2O2).

- Anodic bonding between the silicon and the SOI wafers

For the first bonding, between the silicon and SOI wafers, the recipe has been tailored to take into account the structures on the silicon wafer and the presence of the thin film of glass [11]. The complete recipe of the bonding is detailed on the Table 6 below. A voltage of 200V for the pre-bonding and 150V for the bonding is chosen, in order to not pull-in the membranes, whose voltage pull-in is calculated according to this equation (Eq. 3) [12].

$$V_{PI} = \sqrt{\frac{\left[\frac{64D}{a^4} + \frac{4\sigma D}{h^2 a^4}\right].\left(\frac{d_0}{3}\right) + \frac{128\alpha D}{h^2 a^4}.(\frac{d_0}{3})^3}{\varepsilon_0.[\frac{5}{6d_0^2} + \frac{4}{3\pi a d_0} + \frac{1.918}{\pi a^2}]}} \quad \text{(Eq. 3)}$$

Where :

- h is the membrane thickness
- D = $\frac{\hat{E}*h^3}{1-\upsilon^2}$ is the flexural rigidity
- $\hat{E}$ = $\frac{E}{1-\upsilon^2}$ is the effective Young modulus
- α = $\frac{7505 + 4250*\upsilon - 2791*\upsilon^2}{35280}$
- a is the membrane radius
- σ is the residual stress
- E is the Young modulus of the silicon
- υ is the Poisson ratio of the silicon
- d_0 is the initial gap
- ε_0 is the vacuum permittivity

Moreover, the bonding is stopped when the current drops below 4% of the maximum current be sure to have a complete bonding.

Step	1	2	3	4	5	6
Top temperature (°C)	50	350	350	350	350	350
Bottom temperature (°C)	50	350	350	350	350	350
Chamber pressure (mBar)	5	5	950	950	950	950
Tool pressure (kPa)	0	0	0	0	0	0
Voltage (V)	0	0	0	-200	0	0
Wait condition			4min	5min		
Actions	Contact	Clamps off		Voltage ON	Spacers out	Tool down

Step	7	8	9	10	11	12
Top temperature (°C)	350	350	350	350	200	130
Bottom temperature (°C)	350	350	350	350	200	100
Chamber pressure (mBar)	950	950	950	Purge	Purge	Purge
Tool pressure (kPa)	50	120	0	0	0	0
Voltage (V)	-150	-150	0	0	0	0
Wait condition	30s	4% I_{max}	4min			
Actions	Voltage ON	Voltage ON		Tool up		Unload

Table 6 : Recipe of the bonding

- Anodic bonding between the SOI/Silicon and the borosilicate wafers

For the second bonding between the stack of the SOI/Silicon wafers and the Borosilicate one, the same recipe is used but by applying a voltage of 500V since there are no delicate structures.

8. Fluidic characterization

After the microfabrication, the wafers are diced and the fluidic characterization is performed in the cleanroom at Debiotech. The goal is to demonstrate the chips have a correct flow rate and this latter is indeed independent of external pressure variations.

8.1 Protocols

In order to measure the flow rate, the chips and the set-up measurement need to be prepared. The experimental protocol is detailed below and need to be carefully applied for each test to avoid to damage the chips and to have a good repeatability.

- Rinse the connectors with alcohol and put in a ultrasonic bath.
- Glue the connectors at the outlets of the pumps and put in a oven at 40°C for 12h to let the glue polymerize.
- Prime the pump with water to remove air bubble in the micro-channels and the cavity.
- Dip the chip in a pressurized bottle containing distilled water.
- Connect a pipe from the pressure controller to the top of the bottle to applied the pressure.
- Connect another pipe from outlet of the pump to the scale on which a beaker is placed to collect the fluid.
- Calibrate the pressure controller to have no flow rate when there is no applied pressure.
- Weight the beaker and write down the result.
- Turn on the pressure controller to the desired pressure and wait for one minute to reach the equilibrium in all the fluidic line.
- Launch the timer.
- When the timer is elapsed, weight the beaker and write down the result.
- Estimate the flow rate by comparing the difference of mass in the beaker.

The complete measurement set-up with the aforementioned components is shown on Figure 10.

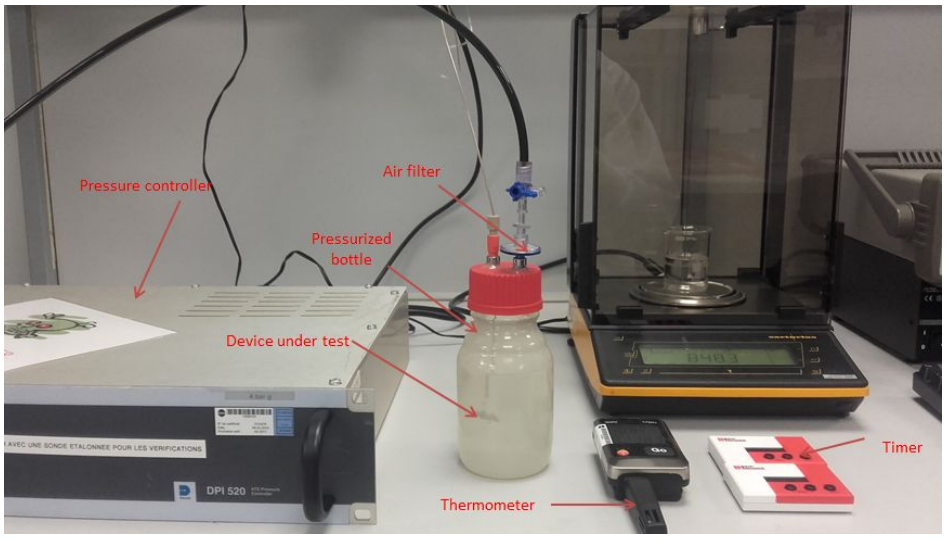

Figure 10 : Photo of the complete set-up

8.2 Fluidic tests

For the fluidic tests, the chips are labelled as follow :

- The number of the stack from 1 to 3 which are composed with the following wafers :
  - Stack 1 : SOI (n°3052) / Si (n°5725) / Boro (n°4)
  - Stack 2 : SOI (n°3050) / Si (n°7653) / Boro (n°3)
  - Stack 3 : SOI (n°3054) / Si (n°5726) / Boro (n°1)
- Their position on the wafer from A0 to D7 for the 1ml/day pumps and from E0 to H5 for the 1mL/h pumps.

There are three different fluidic tests to be done to check the pumps match their specifications :

- The characterization test which consists to measure the flow rate of the pump according to the applied pressure.
- The pressure test which consists to measure the variation of the flow rate when the outside pressure is changed compared with the nominal pressure of operation.
- The temperature test which consists to measure the variation of the flow rate when the temperature is changed.

Several parameters can modify the flow rate, in particular for very low flow rates as it is the case here. Some of their effects can be reduced or even totally cancelled. These

parameters are listed below with, for each, a solution to reduce their influence on the measure and to better interpret the results.

- The scale precision

  The scale has a precision of 0.1µL. In order to have an error of less than 5% on the measured flow rate, it is necessary to measure it for at least 5 min for the 1mL/day design and 15s for the other. A value of 30s has been chosen to reduce even more this error without increasing too much the time of the experiment.

- The water evaporation

  Due to the environment temperature, the water in the beaker evaporates. The rate of evaporation has been measured at 0.8µL/min, which is more important than the lowest flow rate to be measured. In order to prevent this phenomenon, a layer of paraffin oil has been added on the top of the water in the beaker. It allowed to have no evaporation at all.

- The hydrostatic pressure

  When no pressure is applied, the flow rate between the pressurized bottle and the beaker has to be zero. To reach this equilibrium, the level of water in the bottle and the beaker has to be the same. Indeed, if the water level is higher in the bottle than in the beaker, the fluid will flow from the bottle to the beaker which will increase the measured flow rate. On the contrary, if the water level is lower in the bottle, the fluid will flow from the beaker to the bottle, which will reduce the measured flow rate.

- Air bubbles in the fluidic lines

  If there are air bubble in the micro channels or in the fluidic line, the flow rate will be modify. In order to remove all the air, the pump and the fluidic line have to be correctly primed. Since the micro channels are very small, it can take several minutes to remove all the air. An inspection with a microscope allows to check if the channels are correctly primed

- The temperature

  Since the simulated flow rate is valid only for a given temperature, it is necessary to write down the temperature of the water during the experiment which can be slightly different from the one used during the simulation.

- The timer

  The flow rate is calculated according to a difference of mass for a given time.

To be sure the mass on the scale is the one obtained for the expected time, the timer has to be launched at the same time the zero is done on the scale and the result writes down as soon as the time is elapsed.

Other parameters, independent of the operator, may modify the expected flow rate.

- Leakage

The set-up has connectors at the outlets and at the top of the bottle where the pressure is applied and between the bottle and the fluidic line. All these connections can be a source of leakage, in particular at high pressure. It can result in a too high flow rate whose chip design is not responsible for.

- Clogged channels

The micro-channels depth is 12.4µm and they can be easily clogged by a dust particle. If it is the case, the measured flow rate would be less important than expected. To try to prevent this issue, an air filter of 0.22µm is added.

- Process related

During the fabrication of the chips, the depth of the micro-channels and the height of the gap between the SOI et the Silicon wafers may not be exactly the expected value. That is why the thickness of the glass layer deposited by *LithoGlass GmbH* and the depth of each channel have been precisely measured. By knowing these value, it is possible to remake the simulation to know what is the flow rate that should be obtained.

Moreover, some of the chips can have defects due to the process. For instance a pillar can be damaged or the bonding may not be perfect between two wafers. In order to be sure it is a problem of process and not of design, the measure has to be done with several different chips.

- Wrong model

A difference between the experimental and theoretical curves can be due a wrong model, or at least an incomplete or too much simplified one. These fluidic test will allow to tailor the model to get the expected flow rate.

8.2.1 Characterization test

This fluidic test consists in measuring the flow rate of the pumps for a pressure going from 0 to 1 bar and to compare the experimental curve with the theoretical one. The tests are realized in Debiotech cleanroom at 20°C. Consequently the expected flow rate is not

anymore 1mL/h (low flow rate) and 1mL/day (ultra low flow rate) since these values are calibrated for a temperature of 37°C , but 0.7mL/h and 0.7mL/day. This variation is directly linked to the viscosity of water which is less important at higher temperature [13] . The flow rate is expected to be constant between 200 mbar and 1 bar as shown on Figure 11.

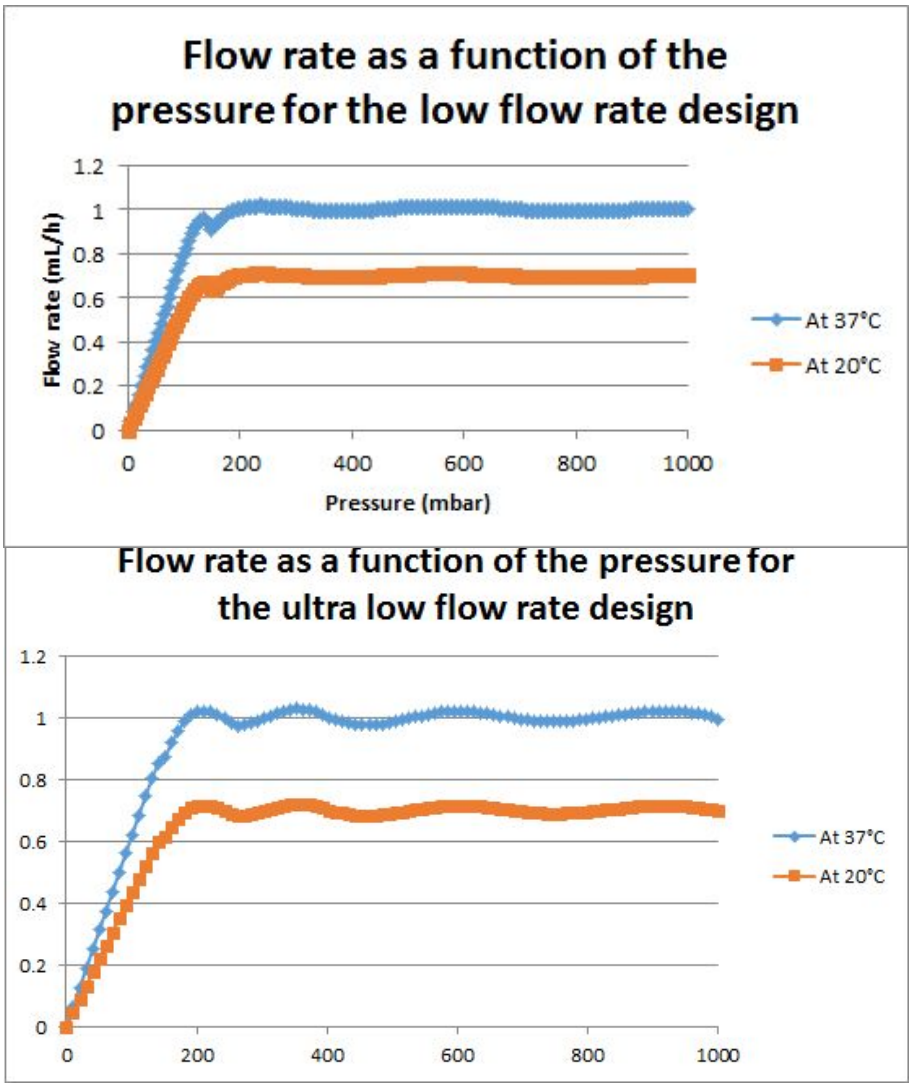

Figure 11 : Theoretical curves at 37°C and 20°C for the low *(top)* and ultra low *(bottom)* flow rate designs

The flow rate has been successfully measured for five chips of the low flow rate design : Stack 1 - H4, Stack 1 - G4, Stack 1 - H5, Stack 1 - G2, Stack 2 - F7 (cf. Figure 12) and for three chips of the ultra low flow rate : Stack 1 - D1, Stack 1 - C2 and Stack 1 - B2 (cf. Figure 13).

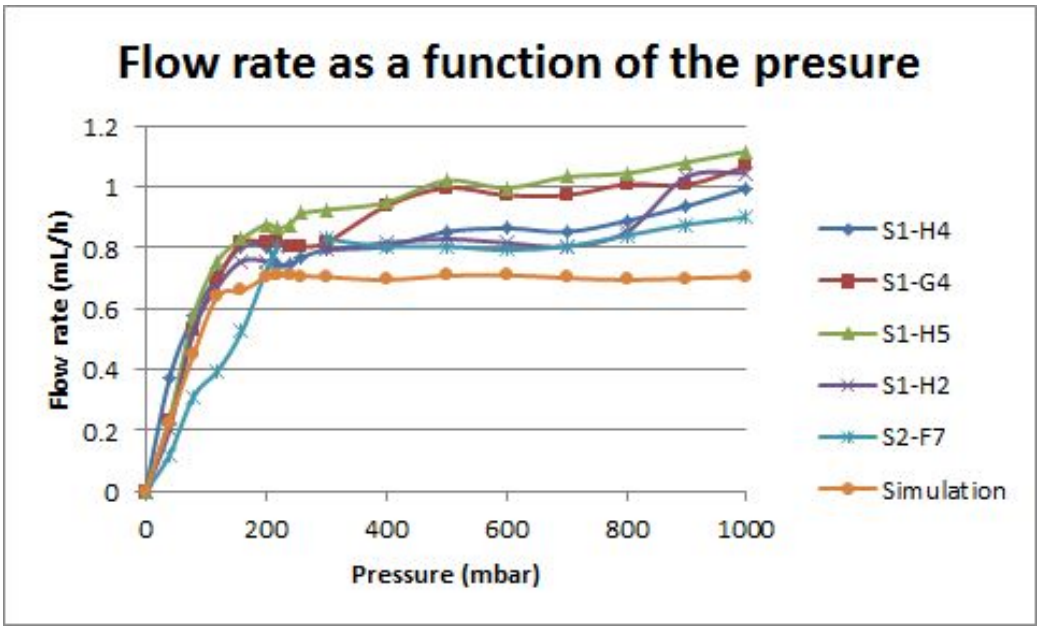

Figure 12 : Experimental curves of the flow rate as a function of the pressure for the low flow rate design compared with the simulation

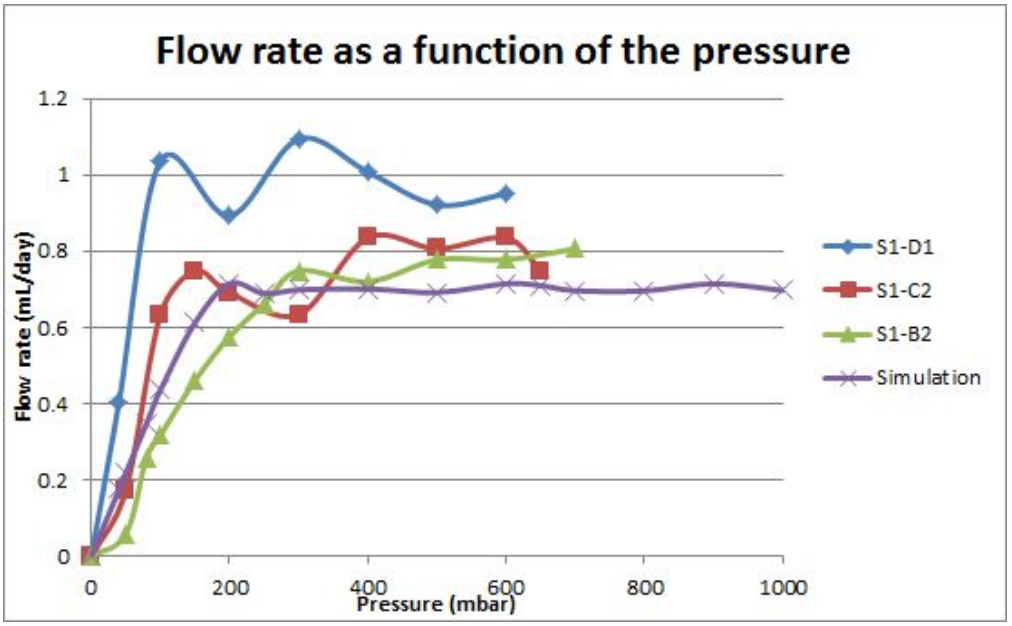

Figure 13 : Experimental curves of the flow rate as a function of the pressure for the ultra low flow rate design compared with the simulation

These curves show a correct operation of the chips, that is to say to be a valve regulator between 200 mbar and 1 bar with a constant flow rate. However, some non-idealities can be pointed out :

- The flow rate can suddenly increase at high pressure (above 700 - 800 mbar) as it is the case for the chip S1-H2 and even more for the chips of the ultra

low flow rate. Values are thus not reported since not relevant. It is likely to a leakage between the fluidic line and one of the connector on the chip.

- The regulation is not perfectly constant as it is the case for the chips S1-D1 and S1-B2. It can be due to a damage pillar, a dust particle near a pillar which prevent to correctly regulate the flow rate or because the measure uncertainties.
- The flow rate is around 0.8mL/h (0.8mL/day) instead of 0.7mL/h (0.7mL/day) as predicted by the theory (cf. Figure 11). It can come from the fact that the micro-channels are slightly deeper than expected (cf. Table 5) or that the model is not accurate enough. To know what is the correction hypothesis, it would be necessary to remake the simulation with the measured micro-channels lengths, depths and the right height of the cavity.

During the test of some of the chips, the flow rate was up to twice lower than expected with important variations for a pressure to another. In order to understand why the behavior of the chip does not match the expectations, an infrared microscope can be used. The pictures below (cf. Figure 14) are infrared pictures of the chip S1-C1 whose flow rate was twice lower than expected. The left pictures shows that there is an air bubble near the pillar while there are dust particles on the second one. These two issues can explain why the flow rate was lower than expected.

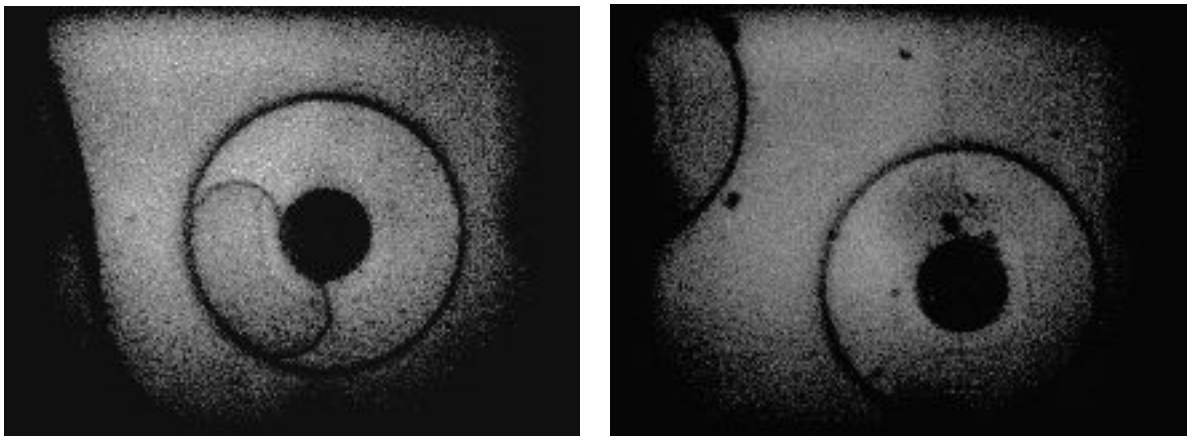

Figure 14 : Infrared pictures of an air bubble *(left)* and dust particles *(right)*

8.2.2 Pressure test

This fluidic consists in measuring the error of the flow rate when the pressure is reduced compared with the nominale pressure. It allows to simulate the case where the patient goes in mountains or takes the plane where the atmospheric pressure is reduced. Consequently, the difference of pressure which is applied on the fluid is not the same. The

goal is to have a minimum variation of flow rate to avoid under or over drug infusion for the patient.

In our case, the nominal pressure is 600 mbar (above the atmospheric pressure) and an altitude up to 4000m will be simulated. The value of the pressure at a given altitude compared with the zero level is given by the National Oceanic and Atmospheric Administration (NOAA) [14]. The obtained results for the low and ultra flow rate are respectively presented on Figure 15 and Figure 16. These results also are compared with the one of the Isomed pump from Medtronic [4].

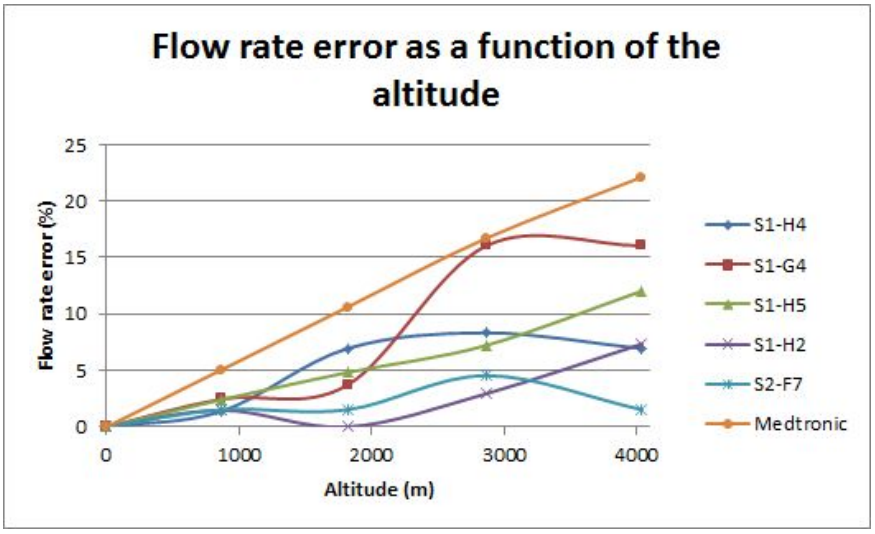

Figure 15 : Comparison of the flow rate error as a function of the altitude between the Chronoflow pump from Debiotech and the Isomed pump from Medtronic for the low flow rate design

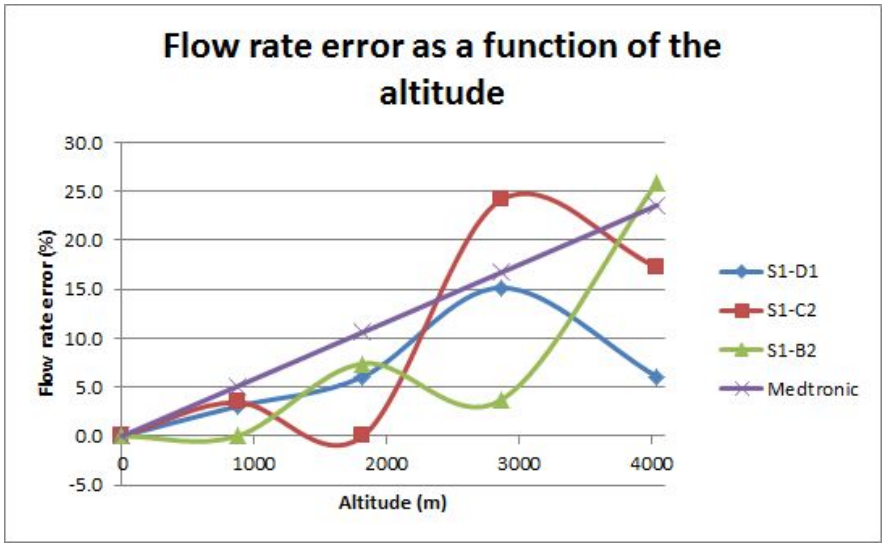

Figure 16 : Comparison of the flow rate error as a function of the altitude between the Chronoflow pump from Debiotech and the Isomed pump from Medtronic for the ultra low flow rate design

For the low flow rate design, the variation of the flow rate with the altitude is below 10% up to almost 4000m (except for one sample) which is more than twice lower than the Medtronic's pump. Thus the flow rate is almost independent on the altitude which is one of the Chronoflow pump requirement and at least much better than the Isomed pump.

For the ultra low flow rate design, the flow rate error is still lower than the one from Medtronic but the trend is less clear. It is mainly due the measurement error.

To reduce this error of measurement for both the design and have better results, the measure should be make again but over a longer period, for instance 5 minutes for the low flow rate andr 30 minutes for the ultra low flow rate for a given pressure.

8.3.3 Temperature test

The temperature test allows to check what is the influence of the body temperature of the patient on the flow rate of the fluid. Indeed, a variation of temperature due to fever or hypothermia for example, leads to a variation of viscosity of the fluid [13]. Consequently the variation of flow rate is modified and this variation is supposed to be inversely proportional to the variation of viscosity. For instance if the viscosity is divided by two, the flow rate is supposed to be doubled. If it increases more, it means that the temperature has a consequence on another parameter like the vapor pressure of the gas which will add an error if the flow rate is not independent of the pressure.

This fluidic test has been realized for three different temperatures : 20, 30 and 40°C for two chips of the low flow rate : S1-H2 and S1-H4. The protocol is the same as the previous experiments except that the bottle is previously put in the oven to heat the water at the right temperature. The Figure 17 displays the flow rate as a function of the temperature for the three different temperatures for the two aforementioned chips.

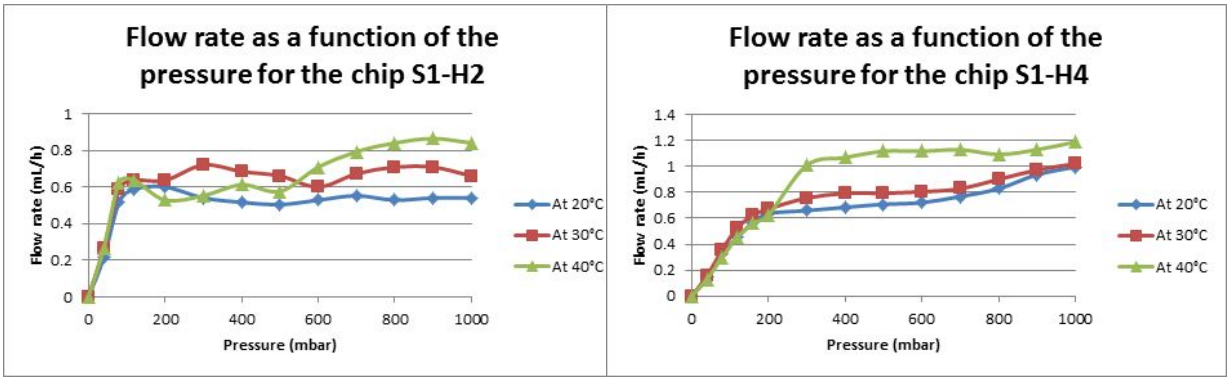

Figure 17 : Fluidic test results of the temperature test for the chip S1-H2 *(left)* and S1-H4 *(right)*

According to the Figure 17, we see that the higher the temperature, the higher the flow rate is, which is consistent with the theory since the viscosity of the water is lower at high temperature. In order to have a quantitative result, the Table 7 shows the variation of the flow rate that has been experimentally measured between two temperatures as well as the theoretical value. Only the values between 200 and 1000 mbar, where there is the regulation, are reported.

Pressure (mbar)	Experimental variation of flow rate between 20 and 30°C (%)		Experimental variation of flow rate between 30 and 40°C (%)		Experimental variation of flow rate between 20 and 40°C (%)	
	S1-H2	S1-H4	S1-H2	S1-H4	S1-H2	S1-H4
200	5.7	5.7	-17.0	-7.1	-12.0	-1.9
300	25.0	14.5	-23.3	33.3	2.2	52.7
400	24.6	15.8	-10.5	34.8	18.6	56.1
500	23.6	11.9	-12.7	40.9	14.3	57.6
600	12.0	11.7	18.0	38.8	34.1	55.0
700	17.9	7.8	17.9	36.2	43.5	46.9
800	25.4	8.7	18.6	21.3	59.1	31.9
900	23.7	3.8	22.0	16.0	60.0	20.5
1000	18.2	2.4	27.3	16.5	55.6	19.3
	Theoretical variation of flow rate between 20 and 30°C : 25.6%		Theoretical variation of flow rate between 30 and 40°C : 18.1%		Theoretical variation of flow rate between 20 and 40°C : 34.8%	

Table 7 : Comparison between the experimental and theoretical flow rate variation due to the temperature

It can be pointed out that the flow rate variation is not constant all over the plateau as it should be. Several reasons can explain this result :

- The water temperature is not exactly the same at the beginning and the end of the measure.
- There are uncertainties on the mesure which leads to small variation of flow rate on the regulation part of the curve.

- There can have leakage at high pressure as it is the case with the chip S1-H4 at 40°C beyond 700 mbar. Thus, it abnormally increases the flow rate variation.
- If air bubble or particle dust are present during a part of the measure it can drastically modify the flow rate.

In order to have more accurate results, these tests should be realized on several other chips and the time of the measure should be increased to reduce some uncertainties like the precision of the scale.

However, it can be expected that the variation of flow rate is similar to the theoretical one since it has been demonstrated that the pressure does not modify significantly the flow rate (<10%).

9. Passive flow valve regulator fabrication for hydrocephalus treatment

In parallel of the fabrication of the micro pump for the drug delivery, another process has been realized for a different application. It allowed me to realize the trainings of the different processes I needed for the *ChronoFlow* pump on a complete device and not only on test wafers. Indeed, this device is very similar in its fabrication but with less steps and cheaper wafers.

This device is a shunt valve for hydrocephalus treatment. Hydrocephalus is a disease which appears when the circulation of the cerebrospinal fluid is malfunctioning. Generally, a shunt is implanted in order to drain the excess of fluid in the brain toward another body cavity through a catheter.

The working principle of this pump is exactly the same, i.e they are holes and pillars which allow keeping constant the flow rate of the liquid whatever is the temperature and the pressure in a certain range. Since the expected flow rate is higher the one for the other pumps, it only required two wafers which are then sealed by anodic bonding (cf. Figure 18):

- A SOI wafer where there are the holes (inlets) and the membrane
- A Borosilicate wafer where there are the pillars and the outlet.

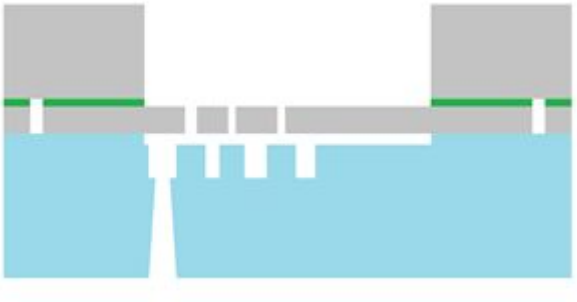

Figure 18 : Design of the pump for the hydrocephalus treatment

For this process, two different designs, called *wave* and *flat* have been realized. For the process, the only difference between them is on the lithographic masks where the position and number of the holes, as well as their size and the size of the pump itself are different. The mask layout, process flow and updated runcards are respectively detailed in Appendix F, Appendix G and Appendix H. In the following parts, the Borosilicate wafers 1 and 2 correspond to the *flat* design while the wafers 3 and 4 are dedicated to the *wave* design.

9.1 SOI wafer process

The top wafer is a SOI wafer with a BOX of 2µm at 50µm depth from the frontside (cf. Figure 18) with 1µm of SiO2 on both its faces. Its process requires only two lithographic steps.

- Etching of the holes

This step allows to create the holes on the frontside of the wafer, where the liquid will flow. They are realized by a DRIE at a depth of 50µm. The time of etching does not need to be very accurate since at this depth, there is a layer of SiO2 acting as etch stop. Indeed the selectivity of the SiO2 over the silicon is very large 150:1.

- Etching of the membrane

The second lithographic step allows to open the membrane. It is also realized by a DRIE at a depth of 380µm. And the same layer of SiO2 than the previous step acts as an etch stop.

Then, before the bonding, the oxide layers on both wafer sides and the one of the BOX are removed which allows to connect the membrane to the holes and thus to the liquid to flow toward the outlet.

9.2 Borosilicate wafer process

The bottom wafer is a Borosilicate wafer comprising the pillars and a gap (micro channel) which are used to regulate the flow rate. The etching of the gap is critical since it determines the fluidic resistance and thus the flow rate (cf. Eq1.). This process requires only two lithographic steps.

- Etching of the gap

This etching allows to create the cavity in which the liquid will flow once it is entered through the inlets etched in the membrane, before been evacuated through the outlet. The flow rate is very dependent on the gap depth, which is expected to be 20µm for the desired application. This value has to be reached with an accuracy of +/- 100nm.

Before depositing the photoresist, it is necessary to define a hard mask in metal since the photoresist may be removed during the etching. This mask is composed of four sputtered layers as follow : Cr/Au/Cr/Au with a thickness of 15/150/15/150nm. The chromium layer is used to to improve the adhesion between the borosilicate wafer and the above metal layers.

Then, the etching is done at room temperature in a bath composed of HF(50%) : H2O at 1:4 in volume. In order to know accurately the etching rate, a measure of the gap depth is done after 20 minutes and gave an etch rate of 350nm/min. So, the total duration of the etching is set at 57 minutes.

At the end, each gap depth has been measured with the surface profiler Bruker Dektat XT in order to be able to compare the theoretical and experimental flow rate. The results of the measured depths are shown in the tables below for each wafer. Within this range of depth, the vertical resolution is 1.0nm.

	Borosilicate wafer 1				Borosilicate wafer 2			
Gap depth [µm]	19.598	19.644	19.455	19.456	19.672	19.891	19.963	20.185
	19.648	19.653	19.708	19.375	19.656	19.767	19.858	20.078
	19.831	19.804	19.894	19.941	19.805	19.573	19.919	20.044
	20.209	20.246	20.276	20.133	20.002	19.839	19.957	19.939
Average [µm]	19.804				19.884			
Relative error (%)	0.978				0.579			
Standard Deviation [µm]	0.282				0.158			

Table 8 : Measured gap depth of the design *flat* of the hydrocephalus pump

	Borosilicate wafer 3					
Gap depth [µm]			20.030	19.945		
		19.885	19.788	19.952	19.989	
	19.902	19.989	19.884	19.858	19.868	19.989
	20.122	19.951	19.620	19.764	19.849	20.088
	20.106	19.818	19.709	19.813	19.923	19.972
	19.793	19.706	19.562	19.721	19.792	19.803
		20.018	19.759	20.138	19.905	
Average [µm]	19.883					
Relative error (%)	0.587					
Standard Deviation [µm]	0.138					

Table 9 : Measured gap depth of the design *wave* of the hydrocephalus pump for the Borosilicate wafer 3

	Borosilicate wafer 4					
Gap depth [µm]			19.661	19.841		
		19.707	19.639	19.984	20.110	
	19.836	19.716	19897	19.930	20.046	20.161
	19.760	19.710	19799	19.885	20.030	20.046
	19.761	19.821	19.842	19.884	19.942	20.051
	19.932	19.931	19.959	19.899	19.883	19.965
		19.983	20.062	19.82	19.837	
Average [µm]	19.892					
Relative error (%)	0.540					
Standard Deviation [µm]	0.128					

Table 10 : Measured gap depth of the design *wave* of the hydrocephalus pump for the Borosilicate wafer 4

These tables show that most on the pumps have a depth in the expected range. The variability between the different pumps is mainly due to the bath temperature which was not perfectly homogeneous despite the pumping system, and consequently results in different etching rates.

Eventually, the hard mask is removed layer by layer by using KI (at 25g/L) + I_2 (at 12g/L) for the gold and $(NH_4)_2Ce(NO_3)_6$ + $HClO_4$ for the chromium.

- Etching of the pillars

The pillars allow to regulate the flow rate by progressively blocking some inlets when the membrane deflects when the pressure increases. Exactly the same process is used than for the gap but this time the targeted etching depth is 50µm.

9.3 Anodic bonding

The bonding between the SOI and the Borosilicate wafers is then realized. But before performing the bonding, since there is a buried oxide, which is an insulator, in the SOI, the electric field is decreased at its frontside. To avoid the potential drop between the two sides of the wafer and to guarantee we apply the correct voltage, it is necessary to electrically connect the two faces. To do so, a small piece of aluminium foil was folded on the side of the wafer to connect to two faces.

After calculation, the pull-in voltage for the design *flat* is around 120V and 305V for the design *wave*. To not take any risk, the applied voltage during the bonding is set to the half of the pull-in voltage.

After this first attempt, the bonding was pretty correct, except on the side where it was not totally bonded (cf. Figure 19), but unfortunately the stacked moved during the process. Consequently the misalignment is too important, about 300µm (cf. Figure 20), and the chips can not be used for the fluidic tests since beyond 5µm they are not working properly and do not work at all beyond 10µm of misalignment between the holes and the pillars.

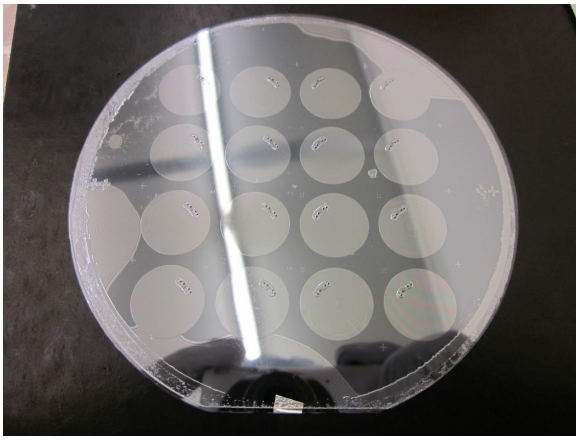

Figure 19 : Bonding 2 for the *flat* design

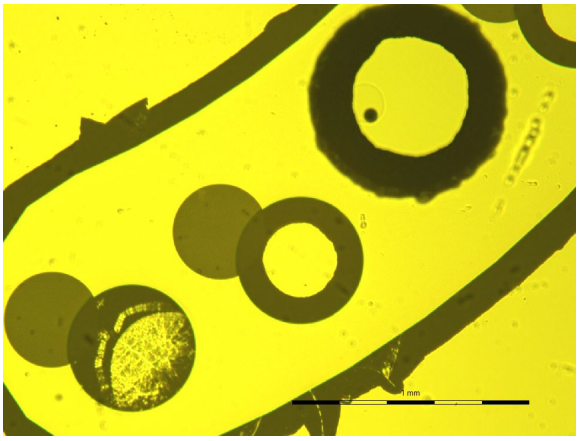

Figure 20 : Misalignment between the holes and pillars for the *flat* design

In order to understand why a correct result can not be achieved, that is to say, both a correct alignment between the two wafers and a bonding over the entire wafer without stuck membranes, a serie of tests has been carried out to determine what the problem is and how to solve it. A classical bonding recipe was used during the previous attempts (cf. Table 6).

The mains step are the following :

- Before the bonding, the wafers are manually aligned with the Bond Aligner.

- The stack is heated at 350°C and pressure reduced.
- A first bonding (or pre-bonding) is done during few minutes while the spacers (if present) between the two wafers are in place and an electrode comes in contact with the center of the wafer to initiate the bonding and avoid the stack to move when the spacers will be removed.
- The spacers (if present) are then removed.
- A pressure is then applied on the totality of the surface of the wafers.
- A voltage is applied for a certain amount of time, which is determined in terms of fraction of maximum current or in terms of charges through the wafers.
- The stack is cooled and the pressure comes back to the atmospheric pressure before unloading the wafers.

Among these steps, several parameters can explain why the bonding fail and will be tested :

- The duration of the pre-bonding is too low (mainly due to these low voltages)
- The voltage of the pre-bonding is too low to overcome oxide voltage breakdown.
- The stack moves when the spacers, placed during the alignment, are removed.
- The electrode is not perfectly perpendicular to the wafers and induces a force that makes them moved when it comes into contact.

The different tests realised as well as their parameters and results are presented in the Table 11 below :

Test n°	Wafers type	Parameters of the recipe	Result	Remarks
1	SOI/Pyrex	Voltage : -60 V Duration : 15 min With spacers	No bonding at all	- No current through the stack - Voltage not high enough
2	SOI/Pyrex	Voltage : -150 V Duration : 15 min With spacers	Not bonding at all	- No current through the stack - Voltage not high enough
3	Si/Pyrex	Voltage : -150 V Duration : 15 min With spacers	Not bonding at all	- No current through the stack - Voltage not high enough
4	SOI/Pyrex	Voltage : -60V Duration : ~4h Without spacers	- Bonding correct - Alignment correct	- Only 90% of the surface is bonded

Table 11 : Summary of the different tests of anodic bonding

The first three tests have been realized in order to check if the pre-bonding was correctly done (tests 1 and 2) and that the poor bonding did not result in the voltage drop in the SOI (test 3). As a result, the applied voltage during the pre-bonding was too low (in absolute value) to start the bonding, even in the case of a bonding between a silicon and a glass wafers. The conclusion is that the misalignment which has been observed is likely due to the clamps, located between the two wafers, which are removed just after the pre-bonding.

To solve this problem, another test (test 4) consisted to realize a full anodic bonding at 60V, like it has been done during the first attempts of bonding, but without the spacers. The process has been stopped the evening before the end of the process which results in a non complete surface bonding. However it is not important since it was not the aim of the test. What is important here is that the bonding is done on 90% of the surface and most important, the alignment is still correct.

As a conclusion, these several tests allowed to understand the origin of the problem and to define a new process that allows to correctly bond the wafers at very low voltage while keeping a excellent alignment between the two wafers. This recipe will be used for the next anodic bonding of both the designs.

A new serie of anodic bonding has been realized for both the designs whose parameters during the bonding and the results are shown on the table below (cf. Table 12). The recipe is similar to the one described in Table 6 except for the voltage which is set at -60V for both pre-bonding and bonding, as well as the limit current value sets at 5% of the maximum current to stop the bonding process.

Design	Wafers used	Voltage (V)	Maximum current (mA)	Results
Flat 1	SOI 448 and Boro 2	-60	0.369	- Membranes sticked except 1 of them - Misalignment (~3-4µm)
Flat 2	SOI 449 and Boro 1	-60	0.317	- Membranes sticked except 4 of them - Misalignment (~3-4µm)
Wave 1	SOI 446 and Boro 3	-60	0.508	- Bonding correct - Misalignment (~3-4µm)
Wave 2	SOI 447 and Boro 4	-60	0.586	- Bonding correct - Misalignment (~7-8µm)

Table 12 : Summary of the parameters and results of the second batch of anodic bonding

The anodic bonding of the *wave* design has been successfully realized as shown on Figure 21 and Figure 22. The error of alignment between the holes and the pillars is around 3-4µm which is in the range of tolerance.

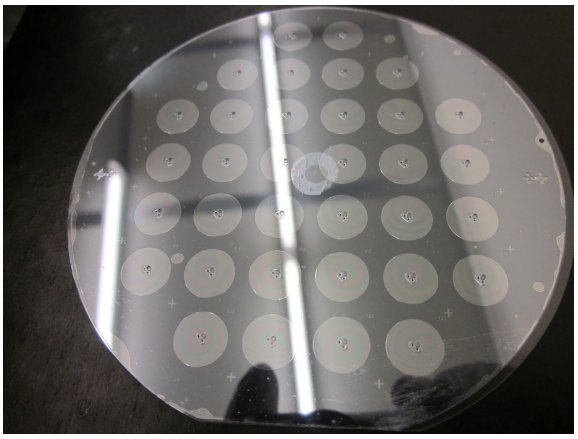

Figure 21 : Successful bonding of the *wave 1* design

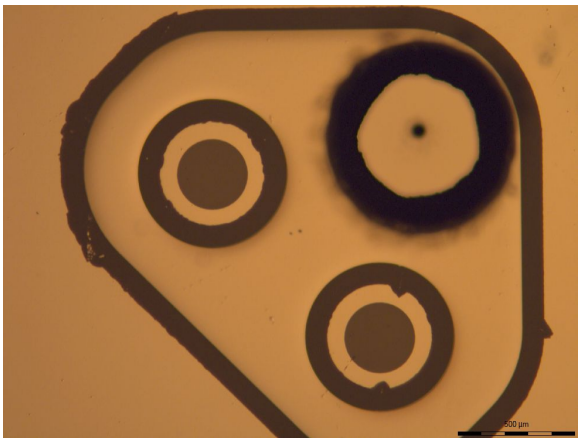

Figure 22 : Correct alignment between the holes and the pillars

Unfortunately, the anodic bonding still did not work as expected for the *flat 1* design, except one, all the membranes are stuck. Despite the voltage is lower than the pull-in voltage, this result can be due to a high flexibility of the membranes. Since the voltage is already at the lowest possible value to realize a bonding, it is necessary to make the membrane stiffer.

To do so, a wafer has been processed by adding a circle of 1µm thick silicon oxide at the center of the membrane, smaller than the membrane diameter. Consequently, to take into account this modification the size of the outlets holes have been adjusted to still keep a constant flow rate. However, this modification did not allow to have a correct bonding (*flat 2*) because except four membranes, they are all pulled-in after the bonding (cf. Figure 23).

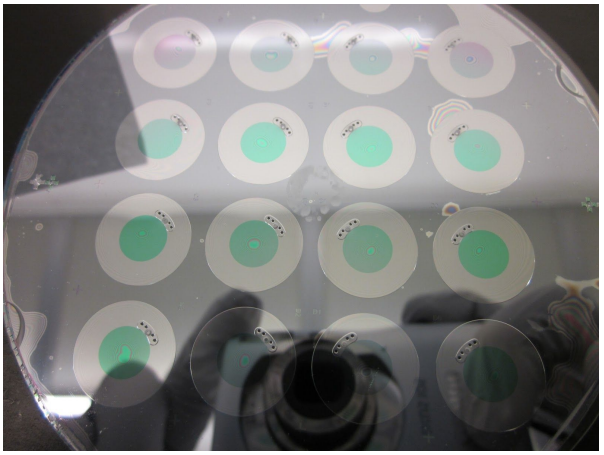

Figure 23 : Bonding of the modified *flat* design with sticked membranes

To try to unstick the membranes, the chips are dipped in a bath of HF to etch the silicon dioxide. After about 1min30s, the membranes have been successfully released and can be used for the fluidic tests.

10. Conclusion

During the internship, a market study of the implantable pumps for intrathecal drug delivery of the different competitors of Debiotech has been conducted in order too see what are the advantages of the Chronoflow pump currently developed by Debiotech.

Then, the full process flow and the microfabrication of these first prototypes, whose mechanical and fluidic simulation have already been performed, have been realized in cleanroom. Since the fabrications of these wafers requires long processes, another process for a different application has been realized previously in order to be trained and better know what are the difficulties and redo the same error. In particular, critical point during the fabrication was the anodic bonding of the triple stack of wafers, where several recipes have been tested in order to find the right recipe and not wasting these expensive and long processed wafers.

Then, fluidic tests have demonstrated the working principle of such low flow rate regulator valve, that is to say be able to deliver a constant flow rate over a wide range of pressure. It has also shown that the pressure does not modify significantly the flow rate which match one of the specification of the Chronoflow pump.The measure of such low flow rate is difficult due to a lot a external parameters that can directly modify the measured flow rate. That is why it is important to know which are these parameters to try to reduce or prevent their impact on the measured flow rate. Despite all these considerations, there are still error in the measure. It is thus necessary to correctly interpret these results and try to understand the origin of these errors.

All these results are very encouraging for the future and show the advantages of this design compare with the ones of the competitors. But, more tests need to be performed to be able to have statistical and more reliable results, see if the measurements are repeatable and how to improve the model.

11. Acknowledgements

I would like to thank Eric Chappel and Dimitry Dumont-Fillon for giving me the opportunity to work on this project and for their help and advices during the internship.

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I also thank Laurent-Dominique Piveteau who accepted me in his company, which allow me to learn a lot during this internship without forgetting Philippe Renaud, Harald Van Lintel and Youla Morfouli to have accepted to supervise me.

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13. Glossary

5FU : Fluorouracil
HF : Hydrofluoric acid
BHF : Buffered HF
BOX : Buried Oxide
BSA : BackSide Alignment
CMi : Center of MicroNanoTechnology (EPFL)
FSA : Front Side Alignment
KOH : Potassium hydroxide
PR : Photoresist
Si : Silicon
SiO2 : Silicon dioxide
SOI : Silicon On Insulator

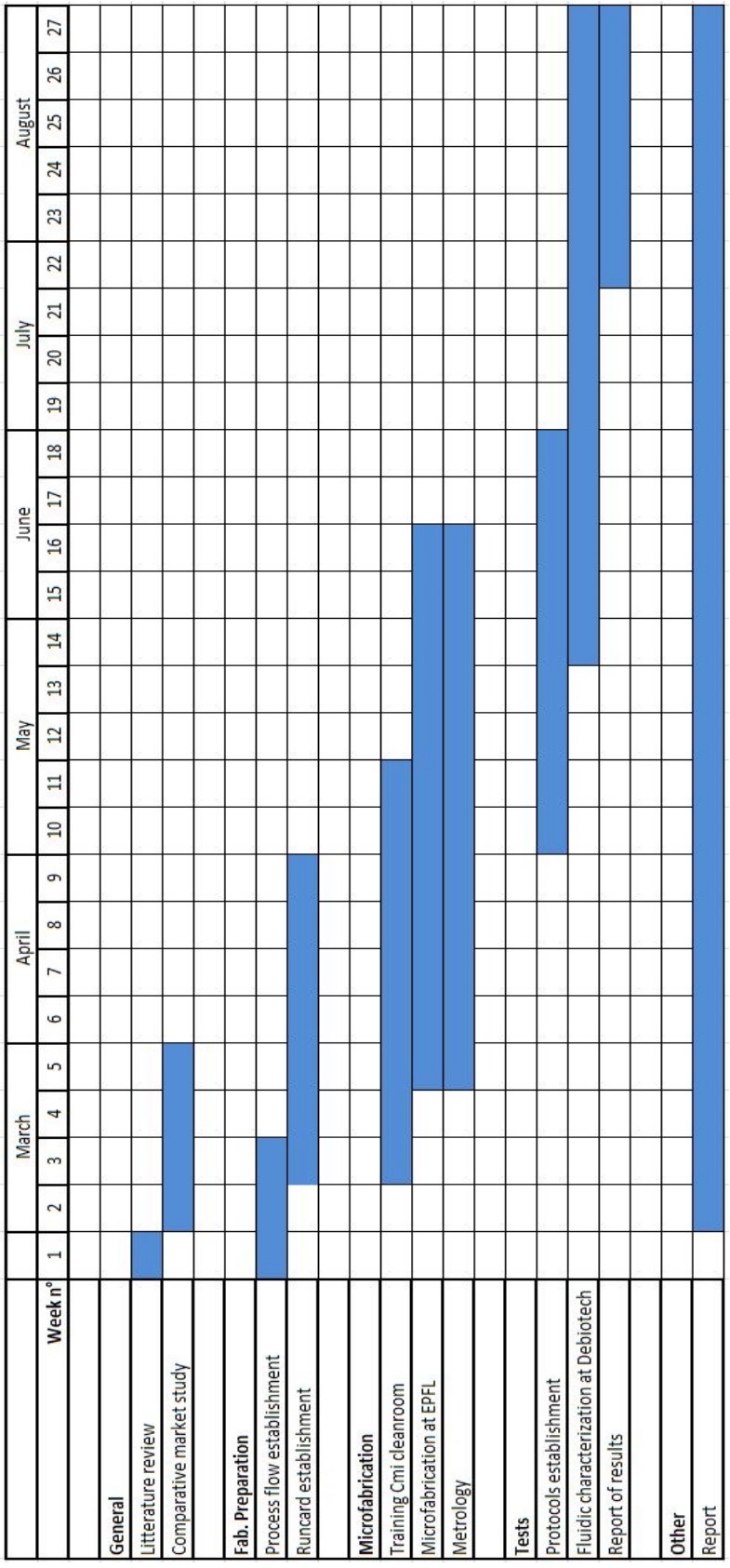
14. Appendix

A. Cost evaluation of the internship

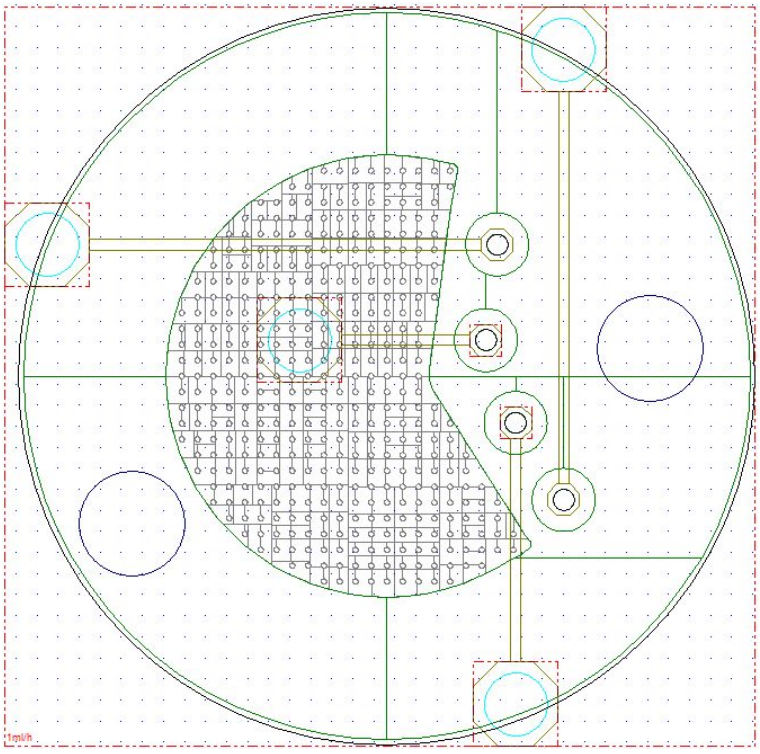
Salary for 6 months :..... 4’800 CHF
Work in the CMi cleanroom (consumables + machine reservation + training) :..... 24’430 CHF
Sandblasting at Icoflex :.....4’800 CHF
Glass deposition by LithoGlas : .....
5’300 CHF

Total :..... 39’330 CHF

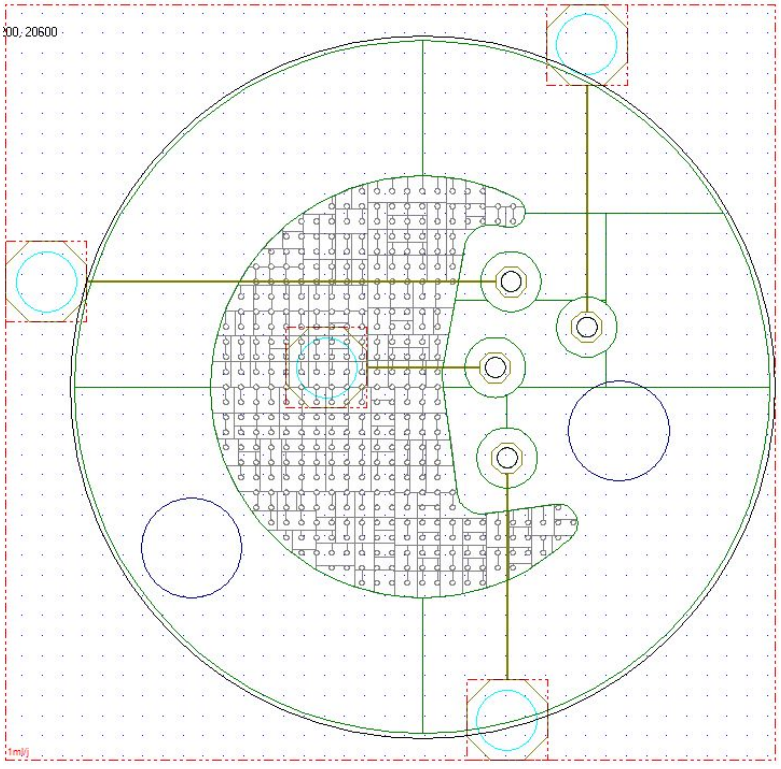
B. Gantt diagram of the project



C. Masks layout of the new *Chronoflow*^{TM} pump

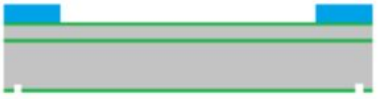
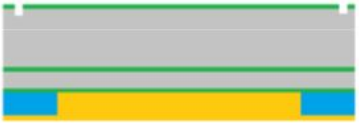


C1 : Mask for the 1mL/h flow rate pump



C2 : Mask for the 1mL/day flow rate pump

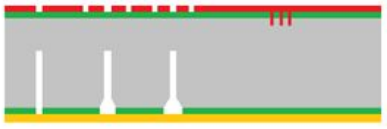
D. Detailed process flow of the *Chronoflow*^{TM} pump

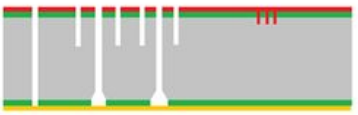
Step	Description	Equipment	Process		Aim		Schematic drawing
			Characteristics	Comment	Target	Measure	
01	Starting Material (FS is up)		SOI	Laser marking on **backside**			
02	Measurement	Nanospec		Oxide thickness on both sides	0.99 um on FS, 2.37 um on BS	49 points	
03	Photolitho BS1	Coating	Positive PR	AZECI 3027	3 µm		
		Exposition	L0_BS Alignment 1	Center wafer with Mask on the right	Mirror Y		
		Development				Optical measurements	
04	Silicon oxide etching BS	Dry etching			2.37µm		
05	Silicon etching BS	Dry etching			3 µm (create alignement marks)	Optical	
06	Cleaning	Plasma O2		Remove PR residues		Visual inspection	
07	Cleaning	Piranha				Visual inspection	
08	Glass deposition FS	Lithoglas		Glass film deposition for anodic bonding on Front Side = NO LASER MARKING. Alignement on BS	20 µm	Profilometre on each chip	
09	Parylene deposition FS	Put wafer test on BS			5 µm		
10	Silicon oxide etching BS	Dry Etching		Remove 0.37 µm oxide to have same thickness everywhere for step 15	0.37 µm		
11	Photolitho BS2	Coating	Positive PR	AZ9260	8 µm		
		Exposition	L1_BS Membrane 1	FSA 10	Mirror Y		
		Development				Optical measurements	
12	Silicon oxide etching BS	Dry etching			2 µm		

13	Silicon etching BS	Dry etching			400 µm	Optical	
14	Cleaning	Remover 1165 + (Plasma O2)		Remove PR residues			
15	Silicon oxide etching BS	Dry etching			2 µm		
16	Cleaning	Plasma O2		Remove PR and parylene residues		Visual inspection	
17	Piranha		Clean	Before bonding			

D1 : Process flow of the SOI wafer (top wafer)

Step	Description	Equipment	Process		Aim		Schematic drawing
			Characteristics	Comment	Target	Measure	
01	Starting Material		FS := flat on the left	process 4 wafers + 1 dummy to purge lines			
02	Measurement	Nanospec		Oxide thickness	1 µm on both side	49 points	
03	Photolitho BS1	Coating	Positive PR	AZECI 3027	3 µm		
		Exposition	L5_BS Channels 2	Center wafer w. mask on the left (or correct if necessary)			
		Development				Optical measurements	
04	Silicon oxide etching BS	Dry etching			1 µm		
05	Cleaning	Plasma O2		Remove PR residues		Visual inspection	
06	Silicon etching BS	Wet etching (KOH)		Channels definition	12.4 µm	Profilometre to measure channels depth, 1st after 3/4 of time (take oxide thickness into account)	

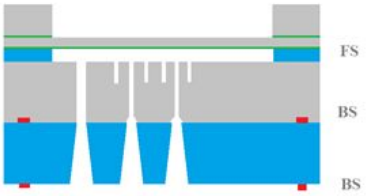
07	Photolitho BS2	Coating	Positive PR	AZ3260	8 µm		
		Exposition	L6_BS Holes 2	FSA with L5_BS Channels 2			
		Development				Optical measurements	
08	Silicon oxide etching BS	Dry etching			1 µm		
09	Silicon etching BS	Dry etching			350 µm	Optical measurements on smallest holes	
10	Cleaning	Plasma O2				Visual inspection	
11	Photolitho FS3	Coating	Positive PR	AZECI 3027	4 µm		
		Exposition	L3_FS Anti Stiction 2	BSA with L6_BS Holes 2	Mirror Y		
		Development				Optical measurements	
12	Silicon oxide etching FS	Dry etching			1 µm		
13	Silicon etching FS	Dry etching			2 µm		
14	Cleaning	Plasma O2		Remove PR and parylene residues			
15	Parylene deposition BS		Put wafer test	Avoid leaking during Si dry etching	5 µm		
16	Photolitho FS4	Coating	Positive PR	AZECI 3027	4 µm		
		Exposition	L4_FS Pillars 2	BSA with "HOLES"	Mirror Y		
		Development				Optical measurements	
17	Silicon oxide etching FS	Dry etching			1 µm		

18	Silicon etching FS	Dry etching			50 µm	Optical measurements	
19	Cleaning	Plasma O2		Remove PR and parylene residues		Visual inspection	
20	Silicon oxide etching	Wet etching		BHF	1 µm	Interferometer + visual	
21	Piranha		Clean	Before bonding			

D2 : Process flow of the silicon wafer (middle wafer)

Step	Description	Equipment	Process		Aim		Schematic drawing
			Characteristics	Comment	Target	Measure	
01	Starting Material		Borofloat 33	one flat at 90°			
02	Visual check						
03	Photolitho BS1	Coating	Negative PR	AZ nLOF 2020	3 um		
		Exposition	L7_BS Alignment 3	Center wafer with mask on the left (or correct if necessary)	No mirror	2mm offset	
		Development				Optical measurements	
04	Al deposition	Evaporation or sputtering		Al used as mask for alignement marks	500 nm		
05	Lift-off resist dissolution	Lift-off					
06	Borosilicate etching	Dry etching	Soft etching SPTS	Etching of alignement marks	3 um		
07	Through holes etching	Icoflex (Powder Blasting)	1mm and 0.6mm holes	modify mask to have good dimensions			
08	Metal stripping	Arias Acid	Al stripping				
09	Piranha		Clean	Before bonding			

D3 : Process flow of the Borosilicate wafer (bottom wafer)

Step	Description	Equipment	Process		Aim		Schematic drawing
			Characteristics	Comment	Target	Measure	
01	Anodic Bonding		SOI [400+50 µm / Si [380 µm]	Aluminium contact between the backside of the SOI and the bottom of the membranes			
02	Anodic Bonding		SOI/Si [830 µm] - Borofloat [500 µm]	Aluminium contact between the surface of the SOI and the surface of the Silicon wafers			
03	UV tape + dicing frame mountaing			UV tape is placed on both sides to avoid chip contamination during dicing			
04	Dicing						

D4 : Process flow of the anodic bonding and dicing

E. Updated runcard for the *Chronoflow™* pump

Step N°	Description	Equipement	Program / Parameters	Target	Remarks
0	WAFER PREPARATION				
0.1	Stock out				
0.2	Check & Measurement	Z3/Nanospec/AFT6100	Prog. 001 Si/SiO2, 49 points per wafer, 4x magnification		
1	PHOTOLITHOGRAPHY - Mask "L0_BS Alignment 1" (mirror)				
1.1	HMDS	Z1/ ACS200	0127 - Cmi AZ ECI 3027 HMDS topEC		
1.2	AZ ECI 3um	Z1/ ACS200	0127 - Cmi AZ ECI 3027 HMDS topEC	3.0 µm	
1.3	PR bake	Z1/ ACS200	0127 - Cmi AZ ECI 3027 HMDS topEC	2min30s	
1.4	PR expose	Z6/ MA6	Alignment with the mask on the right, offset 2 mm	15s	
1.5	PR develope	Z1/ ACS200	0927 - CMiDev.AZECI3027 3um0.puddle		
1.6	PR postbake	Z1/ ACS200	0927 - CMiDev.AZECI3027 3um0.puddle	02min	100°C
1.7	Inspection	Z6/ µScope	Resolution and alignment		
1.8	Spin Rinser Dryer	Z1/ Semitool SRD	Prog. 1		If BS is dirty
2	OXIDE DRY ETCHING				
2.1	Oxide Dry Etch	Z2/ SPTS APS	SiO2_PR_3_1_SOFT @ 10°C	2.37um	
2.2	Inspection	Z3/ Nanospec/AFT6100	Prog. 001 Si/SiO2, 4x magnification, 49 points		
3	Si DRY ETCHING				
3.1	Si Dry Etch	Z2/ AMS200	SOI_accurate++ @ 30°C	3um	
3.2	Inspection	Z2/ µScope			
4	CLEANING				
4.1	Plasma O2 clean	Z2/ Tepla GIGAbatch	PR_Strip_High_5min		
4.2	Piranha cleaning	Z2/ UTF remover			
5	FS GLASS DEPOSITION				
5.1	Glass Deposition	Lithoglass GMBH		20um	
5.2	Glass thickness measurement	Z4/ Bruker Dektak XT		20um	
6	PARYLENE DEPOSITION				
6.1	Surface preparation	Z14/ Wet bench, solvent	Silanization		
6.2	PARYLENE DEPOSITION	By Cmi Staff		5um	
7	OXIDE DRY ETCHING				
7.1	Oxide Dry Etch	Z2/ SPTS APS	SiO2_PR_1_1 @ 10°C	0.37um	
7.2	Inspection	Z3/ Nanospec/AFT6100	Prog. 001 Si/SiO2, 4x magnification		
8	PHOTOLITHOGRAPHY - Mask "BS2 MEMBRANE" - SECOND MASK				
8.1	HMDS	Z1/ ACS200	0150 - Cmi AZ9260 8um0 HMDS topEC		
8.2	AZ9260 8um	Z1/ ACS200	0150 - Cmi AZ9260 8um0 HMDS topEC	8.0 µm	
8.3	PR bake	Z1/ ACS200	0150 - Cmi AZ9260 8um0 HMDS topEC	05min	
8.4	Waiting time			20min	waiting for re-oxygenation
8.5	PR expose	Z1/ MA6 Gen3	Alignement with BS1	630 mJ/cm2	BSA alignment with Hole mask
8.6	PR develope	Z1/ ACS200	0950 - CMiDev.AZ9260 8um0.puddle	230s	
8.7	Inspection	Z6/ µScope	Resolution and alignment		
8.8	Spin Rinser Dryer	Z1/ Semitool SRD	Prog. 1		
9	OXIDE DRY ETCHING				
9.1	Oxide Dry Etch	Z2/ SPTS APS	SiO2_PR_1_1 @ 10°C	2um	
9.2	Inspection	Z3/ Nanospec/AFT6100	Prog. 001 Si/SiO2, 4x magnification		
10	Si DRY ETCHING				
10.1	Si Dry Etch	Z2/ AMS200	SOI_accurate++++ @ 30°C	400um	Etch stop
10.2	Inspection	Z2/ µScope			
11	CLEANING				
11.1	Remover 1165	Z6/ Coillard Photo	SVC-14 (2 baths)	15 min/bath	
11.2	Plasma O2 clean	Z2/ Tepla GIGAbatch	PR_Strip_High_1min		
12	OXIDE DRY ETCHING				
12.1	Oxide Dry Etch	Z2/ SPTS APS	SiO2_PR_1_1 @ 10°C	2um	
12.2	Inspection	Z3/ Nanospec/AFT6100	Prog. 001 Si/SiO2, 4x magnification		
13	CLEANING				
13.1	Plasma O2 clean	Z2/ Tepla GIGAbatch	PR_Strip_High_7min		Remove parylene
13.2	Piranha 1	Z2/ WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	Remove organich residues from
13.3	Piranha 2	Z2/ WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	Bosch processing
13.4	Quick Dump Rinse	Z2/ WB_UFT_Piranha			
13.5	Cascade tank	Z2/ WB_UFT_Piranha			

E1 : Runcard of the SOI wafer (top wafer)

Step N°	Description	Equipement	Program / Parameters	Target	Remarks
0	WAFER PREPARATION				
0.1	Stock out				
0.2	Check & Measurement	Z3/ Nanospec/AFT6100	Prog. 001 Si/SiO2, 49 points per wafer, 4x magnification		
1	PHOTOLITHOGRAPHY - Mask "L5_BS Channels 2"				
1.1	HMDS	Z1/ ACS200	0127 - Cmi AZ ECI 3027 HMDS topEC		
1.2	AZ ECI 3um	Z1/ ACS200	0127 - Cmi AZ ECI 3027 HMDS topEC	3.0 µm	
1.3	PR bake	Z1/ ACS200	0127 - Cmi AZ ECI 3027 HMDS topEC	2min30s	
1.4	PR expose	Z1/ MA6 Gen3	Alignment with Mask + offset 2mm	405 mJ/cm2	
1.5	PR develope	Z1/ ACS200	0927- CMiDev.AZECI3027 3um0.puddle		
1.7	Inspection	Z6/ µScope			
1.8	Spin Rinser Dryer	Z1/ Semitool SRD	Prog. 1		
2	OXIDE DRY ETCHING				
2.1	Oxide Dry Etch	Z2/ SPTS APS	SiO2_PR_1_1 @ 10°C	1um	
2.2	Inspection	Z4/ Bruker Dektat XT	Range : 6.5µm - Profile : Valleys - stylus force : 1mg		
3	CLEANING				
3.1	Plasma O2 clean	Z2/ Tepla GIGAbatch	PR_Strip_High_5min		
4					
4.1	Silicon Wet Etch	Z5/ Plade Six Sigma	KOH 40% @ 60°C	12.4µm	
4.2	Inspection	Z4/ Bruker Dektat XT	Range : 65µm - Profile : Valleys - stylus force : 1mg	13.4µm	channel depth (12.4um) + SiO2 (1um)
5	PHOTOLITHOGRAPHY - Mask "BS2 HOLES" - Second mask				
5.1	HMDS	Z1/ ACS200	0150 - Cmi AZ9260 8um0 HMDS topEC		
5.2	AZ9260 8um	Z1/ ACS200	0150 - Cmi AZ9260 8um0 HMDS topEC	8 µm	
5.3	PR bake	Z1/ ACS200	0150 - Cmi AZ9260 8um0 HMDS topEC	5min	
5.4	Waiting time			20min	waiting for re-oxygenation
5.5	PR expose	Z1/ MA6 Gen3	Alignement with channels	700 mJ/cm2	FSA alignment with Hole mask
5.6	PR develope	Z1/ ACS200	0960 - CMiDev.AZ9260 8um0.puddle		
5.7	Inspection	Z6/ µScope	Resolution and alignment		
5.8	Spin Rinser Dryer	Z1/ Semitool SRD	Prog. 1		
6	OXIDE DRY ETCHING				
6.1	Oxide Dry Etch	Z2/ SPTS APS	SiO2_PR_1_1 @ 10°C	1um	
6.2	Inspection	Z3/ Nanospec/AFT6100	Prog. 001 Si/SiO2, 4x magnification		
7	Si DRY ETCHING				
7.1	Si Dry Etch	Z2/ AMS200	SOI_accurate++++ @ 30°C	350um	Calibration by focometry
7.2	Inspection	Z2/ µScope			
8	CLEANING				
8.1	Plasma O2 clean	Z2/ Tepla GIGAbatch	PR_Strip_High_7min		
9	PHOTOLITHOGRAPHY - Mask "FS3 SURFACE" - Third mask				
9.1	HMDS	Z1/ YES3	Prog. 5		
9.2	ECI 4um	Z1/ Rite Track 1	C_NoEBR_AZ_ECI_4um	4.0 µm	
9.3	PR bake	Z1/ Rite Track 1	C_NoEBR_AZ_ECI_4um		
9.4	Waiting time			7min	waiting for re-oxygenation
9.5	PR expose	Z6/ MA6	Alignement with holes	525mJ/cm2	BSA with antistiction mask
9.6	PR develope	Z1/ Rite Track 2	Dev_ECI_4um		
9.7	PR postbake	Z1/ Rite Track 2	Dev_ECI_4um		
9.8	Inspection	Z6/ µScope	Resolution and alignment		
9.9	Spin Rinser Dryer	Z2/ Semitool SRD	Prog. 2		
10	OXIDE DRY ETCHING				
10.1	Oxide Dry Etch	Z2/ SPTS APS	SiO2_PR_1_1 @ 10°C	1um	
10.2	Inspection	Z3/ Nanospec/AFT6100	Prog. 001 Si/SiO2, 4x magnification		
11	Si DRY ETCHING				
11.1	Si Dry Etch	Z2/ AMS200	SOI_accurate-- @30°C	2um	
11.2	Inspection	Z2/ µScope			
12	CLEANING				
12.1	Plasma O2 clean	Z2/ Tepla GIGAbatch	PR_Strip_High_5min		
13	PARYLENE DEPOSITION				
13.1	Surface preparation	Z14/ Wet bench solvent	Silanization		
13.2	PARYLENE DEPOSITION	By Cmi Staff			
14	PHOTOLITHOGRAPHY - Mask "FS4 PILLARS" - Fourth mask				
14.1	HMDS	Z1/ ACS200	0128 - Cmi AZ3027 4um0 HMDS topEC		
14.2	AZ3027 4um	Z1/ ACS200	0128 - Cmi AZ3027 4um0 HMDS topEC	4.0 µm	
14.3	PR bake	Z1/ ACS200	0128 - Cmi AZ3027 4um0 HMDS topEC	02min30	
14.4	Waiting time			5min	waiting for re-oxygenation
14.5	PR expose	Z1/ MA6 Gen3	BSA with Holes - Soft contact	525 mJ/cm2	
14.6	PR develope	Z1/ ACS200	0928 - CMiDev.AZECI3027 4um0.puddle		
14.7	Inspection	Z6/ µScope	Resolution and alignment		
14.8	Spin Rinser Dryer	Z1/ Semitool SRD	Prog. 1		
15	OXIDE DRY ETCHING				
15.1	Oxide Dry Etch	Z2/ SPTS APS	SiO2_PR_1_1 @ 10°C	1um	
15.2	Inspection	Z3/ Nanospec/AFT6100	Prog. 001 Si/SiO2, 4x magnification		
16	Si DRY ETCHING				
16.1	Si Dry Etch	Z2/ AMS200	SOI_accurate ++++ @30°C	50um	
16.2	Inspection	Z2/ µScope			
17	CLEANING				
17.1	Plasma O2 clean	Z2/ Tepla GIGAbatch	PR_Strip_High_7min		
18	OXIDE WET ETCHING - BHF				
18.1	Silicon oxide Wet Etch	Z2/ Plade Oxide	NH4F(40%):HF(50%) at 7:1	1 µm	
18.2	Inspection	Z2/ µScope			
19	CLEANING				
19.1	Piranha 1	Z2/ WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	Remove organich residues from Bosch
19.2	Piranha 2	Z2/ WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	processing
19.3	Quick Dump Rinse	Z2/ WB_UFT_Piranha			
19.4	Cascade tank	Z2/ WB_UFT_Piranha			

E2 : Runcard of the silicon wafer (middle wafer)

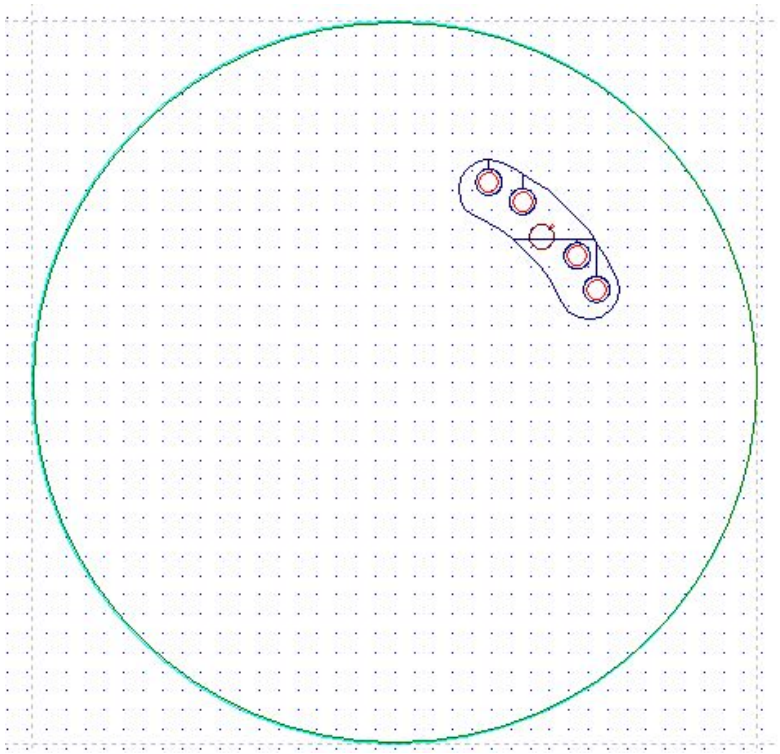
Step N°	Description	Equipement	Program / Parameters	Target	Remarks
0	**WAFER PREPARATION**				
0.1	Stock out				
1	**PHOTOLITHOGRAPHY - Mask "ALIGNEMENT MARKS" - FIRST MASK**				
1.1	Surface preparation	**Z1/** Yes III	Thermal dehydratation		
1.2	AZ nLOF 2020	**Z6/ EVG150**	nLOF_2020_GlassOnly_NoDehydrate_5_3 Recipe : nLOF_2020_3um	3.0 µm	
1.3	PR expose	**Z1/** MA6 Gen3	BSA - Soft contact	150 mJ/cm2	
1.4	PR develope	**Z6/ EVG150**	Dev_nLOF_3um0_max		Maximim PR negative profile
1.5	Inspection	**Z6/** µScope	Resolution and alignment		
1.6	Spin Rinser Dryer	**Z1/** Semitool SRD	Prog. 1		
2	**ALUMINIUM DEPOSITION**				
2.1	Evaporation	LAB 600H	Recipe : HRN - Al	500 nm	
3	**Lift-off resist dissolution**				
3.1	Lift-off	**Z1/** Plade solvent	Remover 1165 bath		Around 45min
3.2	Fast Fill Rinse	**Z1/** Plade solvent		2min	
3.3	Final rinse	**Z1/** Plade solvent			
3.4	Clean&Dry	**Z1/** Plade solvent	SRD clean and dry (Prog.1)		
4	**Borosilicate dry etching**				
4.1	Boro. dry etch	**Z2/** SPTS	Pyrex	3 µm	
4.2	Inspection	**Z2/** µScope			
5	**Glass powder blasting**				
5.1	Sand blasting	Icoflex		Through all	
6	**Aluminium stripping**				
6.1	Al stripping	**Z14/** Arias Acid	ANP solution	1min45sec	
7	**CLEANING**				
7.1	Piranha 1	**Z2/** WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	Remove organich residues from Bosch processing
7.2	Piranha 2	**Z2/** WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	
7.3	Quick Dump Rinse	**Z2/** WB_UFT_Piranha			
7.4	Cascade tank	**Z2/** WB_UFT_Piranha			

E3 : Runcard of the borosilicate wafer (bottom wafer)

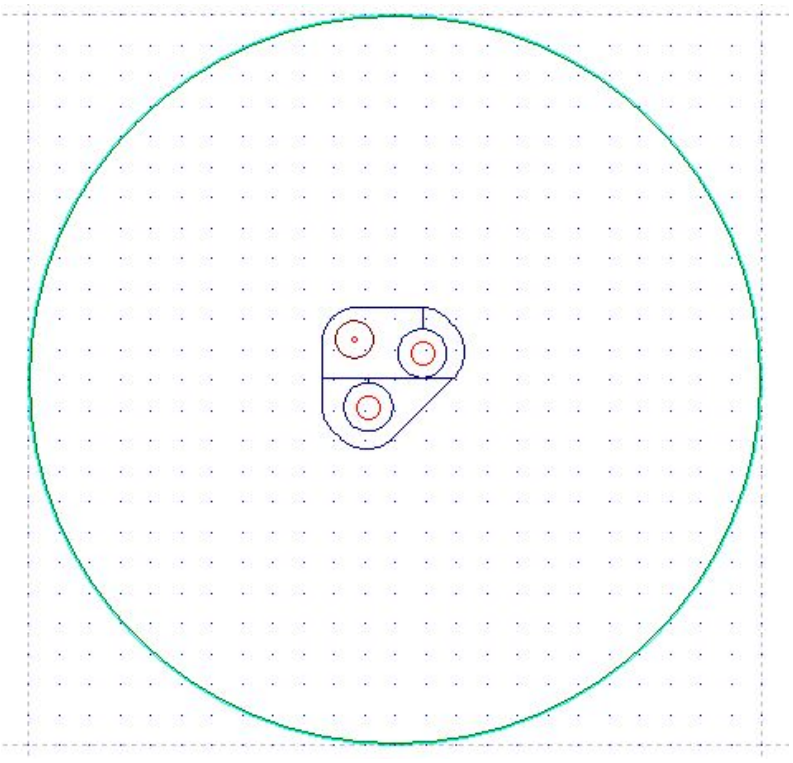
Step N°	Description	Equipement	Program / Parameters	Target	Remarks
1	**FIRST ANODIC BONDING**				
1.1	Bonding alignment	**Z6/** BA6			
1.2	Lateral contacting				
1.3	Anodic bonding	**Z6/** SB6	Debiotech_CF_SOI_Si		Wait condition : Current = 4% of Imax
1.4	Inspection	**Z6/** µScope			
2	**SECOND ANODIC BONDING**				
2.1	Bonding alignment	**Z6/** BA6			Without spacers
2.2	Lateral contacting				
2.3	Anodic bonding	**Z6/** SB6	Debiotech_CF_Si_Boro		Wait condition : Current = 4% of Imax
2.4	Inspection	**Z6/** µScope			
3	**DICING**				
3.1	UV tape application	**Z11/** Laminator	UV tape on both sides		
3.2	Dicing	**Z9/** DAD-321			
3.3	Tape release	**Z9/** "UV-box"			

E4 : Runcard of the anodic bonding and dicing

F. Masks layout of the *Hydrocephalus* pump



F1 : Mask for the *flat* design



F2 : Mask for the *wave* design

G. Detailed process flow of the *Hydrocephalus* pump

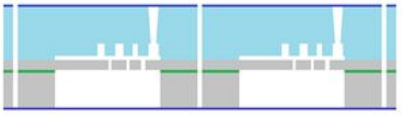
Step	Description	Equipment	Process		Aim		Schematic drawing
			Characteristics	Comment	Target	Measure	
01	Starting Material		2 µm BOX @ 50 µm	bow < 60um	432 µm +/- 10 µm		
02	Measurement			Silicon device layer (FS) thickness		Wafer thickness, 49 points + Bow	
03	Oxidation	WetOx	Double side process	Silicon oxide as mask for FS and as protection on BS	1 um +/- 60nm	Interferometer, 49 points	
04	Photolitho FS 1	Coating	Positive PR	AZECI 3027	3 µm		
		Exposition	Mask "Holes"	First mask			
		Development				Optical measurements	
05	Silicon oxide etching FS	Dry etching			1 µm	Interferometer + visual	
06	Silicon etching FS	Dry etching		Etching of the holes, dicing lines and chip IDs	50 µm	Interferometer + visual	
07	Cleaning	Plasma O2		Remove PR residues			
08	Photolitho BS 1	Coating	Positive PR	AZECI 3027	3 µm		
		Exposition	mask "MEMBRANE"	BS alignment with "Holes"	+/- 5 um		
		Development				Optical measurements	
09	Silicon oxide etching BS	Dry etching			1 µm	Interferometer + visual	
10	Silicon etching BS	Dry etching			380 µm	Interferometer + visual	
11	Cleaning	Plasma O2		Remove PR residues			
12	Silicon oxide etching FS	Wet etching		BHF	2 µm	Interferometer + visual	

G1 : Process flow of the SOI wafer (top wafer)

Step	Description	Equipment	Process		Aim		Schematic drawing
			Characteristics	Comment	Target	Measure	
01	Starting Material		Borofloat 33	bow < 30um	500 µm +/- 20 µm		
02	Visual check						
03	Metal deposition 1 FS	Sputtering	Single side process	Hard mask definition	330 nm		
04	Photolitho FS 1	Coating	Positive PR	AZECI 3027	3 µm		
		Exposition	mask "GAP"	First mask			
		Development				Optical measurements	
05	Metal dry etching FS	Ion beam etching			330 nm	Optical measurements	
06	Borofloat etching	Wet etching		HF 10% @ RT	20 µm		
07	Cleaning	Wet etching		PR stripping Metal etching		Visual inspection	
08	Metal deposition 2 FS	Sputtering	Single side process	Hard mask definition	330 nm		
09	Photolitho FS 2	Coating	Positive PR	High topo AZ9260	14 µm		
		Exposition	mask "PILLARS"	FS alignment with "GAP"			
		Development				Optical measurements	
10	Metal dry etching FS	Ion beam etching			330 nm	Optical measurements	
11	Borofloat etching	Wet etching		HF 10% @ RT	50 µm		

12	PR removal	Wet etching		PR stripping		Visual inspection	
14	Borofloat etching	Sandblasting		Outlet etching BS alignment with "PILLARS" Subcontracted to Icoflex		Optical measurements	
15	Final cleaning	Wet etching		Metal etching Piranha cleaning	2.4 µm	Interferometer + visual	

G2 : process flow of the Borosilicate wafer (bottom wafer)

Step	Description	Equipment	Process		Aim		Schematic drawing
			Characteristics	Comment	Target	Measure	
01	Anodic Bonding		SOI / Borofloat	Anodic bonding with side voltage contact			
02	UV tape + dicing frame mountaing			UV tape is placed on both sides to avoid chip contamination during dicing			
03	Dicing						

G3 : Process of the anodic bonding and dicing

H. Updated runcard for the *Hydrocephalus* pump

Step N°	Description	Equipement	Program / Parameters	Target	Remarks
0	**WAFER PREPARATION**				
0.1	Stock out				
0.2	Wetox			1µm	
0.3	Check & Measurement	**Z3/** Nanospec/AFT6100	Prog. 001 Si/SiO2, 25 points per wafer, 4x magnification		
1	**PHOTOLITHOGRAPHY - Mask "HOLES" FS - ø - First mask**				
1.1	HMDS	**Z1/** YES3	Prog. 5		
1.2	ECI 3um	**Z1/** Rite Track 1	C_NoEBR_AZ_ECI_3um	3.0 µm	First 2 purge wafers (provided by CMI)
1.3	PR bake	**Z1/** Rite Track 1	C_NoEBR_AZ_ECI_3um		
1.4	PR expose	**Z6/** MA6	First mask	405mJ/cm2	
1.5	PR develope	**Z1/** Rite Track 2	Dev_ECI_3um		First 2 purge wafers (provided by CMI)
1.6	PR postbake	**Z1/** Rite Track 2	Dev_ECI_3um		
1.7	Inspection	**Z6/** µScope	Resolution and alignment		
1.8	Spin Rinser Dryer	**Z2/** Semitool SRD	Prog. 2		
2	**OXIDE DRY ETCHING**				
2.1	Oxide Dry Etch	**Z2/** SPTS APS	SiO2_PR_1:1 @ 10°C	1.0 µm	5 min
2.2	Inspection	**Z2/** µScope			
3	**Si DRY ETCHING**				
3.1	Si Dry Etch	**Z2/** AMS200	SOI_accurate++++ @ 30°C	50um	
3.2	Inspection	**Z2/** µScope			
4	**CLEANING**				
4.1	Plasma O2 clean	**Z2/** Tepla GIGAbatch	PR_Strip_High_5min		
5	**PHOTOLITHOGRAPHY - Mask "MEMBRANE" BS - Mirror - BSA**				
5.1	HMDS	**Z1/** YES3	Prog. 5		
5.2	ECI 3um	**Z1/** Rite Track 1	C_NoEBR_AZ_ECI_3um	3.0 µm	First 2 purge wafers (provided by CMI)
5.3	PR bake	**Z1/** Rite Track 1	C_NoEBR_AZ_ECI_3um		
5.4	PR expose	**Z6/** MA6	BS alignement	405mJ/cm2	Align with "HOLES"
5.5	PR develope	**Z1/** Rite Track 2	Dev_ECI_3um		First 2 purge wafer (provided by CMI)
5.6	PR postbake	**Z1/** Rite Track 2	Dev_ECI_3um		
5.7	Inspection	**Z6/** µScope	Resolution and alignment		
5.8	Spin Rinser Dryer	**Z2/** Semitool SRD	Prog. 2		
6	**OXIDE DRY ETCHING**				
6.1	Oxide Dry Etch	**Z2/** SPTS APS	SiO2_PR_1:1 @ 10°C	1.0 µm	5 min
6.2	Inspection	**Z2/** µScope	Silicon reached & defects		
7	**Si DRY ETCHING**				
7.1	Si Dry Etch	**Z2/** AMS200	SOI_accurate++++ @ 30°C	380 µm	
7.2	Inspection	**Z2/** µScope			
7.3	Inspection	**Z3/** Nanospec/AFT6100	Prog. 001 Si/SiO2 with 4x magnification		
8	**CLEANING**				
8.1	Plasma O2 clean	**Z2/** Tepla GIGAbatch	PR_Strip_High_5min		
9	**OXIDE WET ETCHING**				
9.1	Silicon oxide Wet Etch	**Z2/** Plade Oxide	BHF 7:1 clean @ RT	2.0 µm	
9.2	Inspection	**Z2/** µScope			
10	**CLEANING**				
10.1	Piranha 1	**Z2/** WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	Remove organich residues from Bosch processing
10.2	Piranha 2	**Z2/** WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	
10.3	Quick Dump Rinse	**Z2/** WB_UFT_Piranha			
10.4	Cascade tank	**Z2/** WB_UFT_Piranha			

H1 : Runcard of the SOI wafer (top wafer)

Step N°	Description	Equipement	Program / Parameters	Target	Remarks
0	**WAFER PREPARATION**				
0.1	Stock out				
0.2	Check				
1	**Cr/Au deposition 1**				
1.1	Cr/Au deposition 1	**Z11/** DP-650	RTU_Cr-Au	15/150 nm	At room temperature
1.2	Cr/Au deposition 2	**Z11/** DP-650	RTU_Cr-Au	15/150 nm	At room temperature
2	**PHOTOLITHOGRAPHY - Mask "GAP" FS - Mirror - First mask**				
2.1	HMDS	**Z1/** YES3	Thermal dehydratation		
2.2	ECI 3um	**Z1/** Rite Track 1	C_NoEBR_AZ_ECI_3um	3.0 µm	First 2 purge wafers (provided by CMI)
2.3	PR bake	**Z1/** Rite Track 1	C_NoEBR_AZ_ECI_3um		
2.4	Exposure	**Z6/** MA6	First mask	300mJ/cm2	
2.5	PR develope	**Z1/** Rite Track 2	Dev_ECI_3um		First 2 purge wafer (provided by CMI)
2.6	PR postbake	**Z1/** Rite Track 2	Dev_ECI_3um		
2.7	Spin Rinser Dryer	**Z2/** Semitool SRD	Full program		
2.8	Inspection	**Z6/** µscope	Resolution		
2.9	Thickness measurement	**Z4/** Bruker Dektat			

3	**METAL DRY ETCHING**				
3.1	Ion Beam Etching	**Z11/** IBE350 Veeco	Medium_IBE (standard) Tilt: -10° (standard)	330 nm -> 3 min	1st wafer (dummy): WarmUp recipe According to SIMS: 2-2.5min enough)
3.2	Thickness measurement	**Z15/** Alpha-step 500			
3.3	X-Y measurement	**Z5/** Nikon	100x magnification, alignment marks		
4	**BOROFLOAT WET ETCHING**				
4.1	Borofloat etching (1/2)	**Z2/** Plade Ox	HF10% @ RT	20 min	
4.2	Rinse & Dry	**Z2/** Plade Ox	FFR 2 times, SDR drying only		
4.3	Inspection	**Z2/** µScope			
4.4	Thickness measurement	**Z15/** Alpha-step 500			Take the metal layer into account !
4.5	Borofloat etching (2/2)	**Z2/** Plade Ox	HF10% @ RT	20µm	
4.6	Rinse & Dry	**Z2/** Plade Ox	FFR 2 times, SDR drying only		
4.7	Inspection	**Z2/** µScope			
4.8	Thickness measurement	**Z4/** Bruker Dektat			Take the metal layer into account !
5	**METAL WET ETCHING**				
5.1	Stripping photoresist	**Z6/** Coillard Photo	SVC-14 (2 baths)	20 min/bath	
5.2	Inspection	**Z6/** µScope			
5.3	Au-etch	**Z14/** Arias Acid	Au-etch @ RT (new solution)	> 3 min	2 times
5.4	Rinsing (intermediate)	**Z14/** Arias Acid	H2O	30 sec	
5.5	Cr-etch	**Z14/** Arias Acid	Cr-etch @ RT (new solution)	15 sec	2 times
5.6	Rinsing (final)	**Z14/** Arias Acid	2 baths of H2O	30 sec	
5.7	Inspection	**Z14/** µscope	Stripping efficiency		
5.8	Thickness measurement	**Z4/** Bruker Dektat			
5.9	X-Y measurement	**Z5/** Nikon	100x magnification, alignment marks		
6	**Cr/Au deposition 2**				
6.1	Cr/Au deposition 1	**Z11/** DP-650	RTU_Cr-Au	15/150 nm	At room temperature
6.2	Cr/Au deposition 2	**Z11/** DP-650	RTU_Cr-Au	15/150 nm	At room temperature
7	**PHOTOLITHOGRAPHY - Mask "PILLAR" FS - Mirror - FSA**				
7.1	HMDS	**Z1/** YES3	Prog. 5		
7.2	AZ9260 coating	**Z6/** EVG150	AZ9260_5to14mu_GlassOnly_5_3 Recipe: Coat_AZ9260_14um_NoEBR (incl. Dehydration @ 160°C)	14 µm	1st wafer (dummy): purge (CMI)
7.3	Exposure	**Z6/** MA-6	FS alignement with GAP	650 mJ/cm2	
7.4	AZ9260 develop	**Z6/** EVG150	AZ9260_5to14mu_GlassOnly_5_3 Recipe: SprayDev_14um_AZ9260	2 times	1st wafer: purge (CMI)
7.5	Back-side cleaning	**Z2/** Ultrafab Piranha	Full SRD program		
7.6	Inspection	**Z6/** µscope	Alignment + development		
8	**METAL DRY ETCHING**				
8.1	Ion Beam Etching	**Z11/** IBE350 Veeco	Medium_IBE (standard) Tilt: -10° (standard)	330 nm -> 3 min	1st wafer (dummy): WarmUp recipe According to SIMS: 2-2.5min enough)
8.2	Thickness measurement	**Z4/** Bruker Dektat			
8.3	X-Y measurement	**Z5/** Nikon	100x magnification, alignment marks		

9	**BOROFLOAT WET ETCHING**				
9.1	Borofloat etching (1/2)	**Z2/** Plade Ox	HF10% @ RT	30 min	
9.2	Rinse & Dry	**Z2/** Plade Ox	FFR 2 times, SDR drying only		
9.3	Inspection	**Z2/** µscope	Adhesion of photoresist and defects		
9.4	Thickness measurement	**Z4/** Bruker Dektat			
9.5	Borofloat etching (2/2)	**Z2/** Plade Ox	HF10% @ RT	50 µm (total)	
9.6	Rinse & Dry	**Z2/** Plade Ox	FFR 2 times, SDR drying only		
9.7	Inspection	**Z15/** µscope			
9.8	Stripping photoresist	**Z2/** Ultrafab Remover	Remover 1165		
10	**CLEANING**				
10.1	Stripping photoresist	**Z6/** Coillard Photo	SVC-14 (2 baths)	20 min/bath	
11	**DRILLING by SANDBLASTING @ Icoflex (Lausanne)**				
			Subcontracted to IcoFlex		
11.1	Inspection	**Z6/** µscope	Alignment		
11	**METAL WET ETCHING**				
11.2	Au-etch	**Z14/** Arias Acid	Au-etch @ RT (new solution)	> 3 min	2 times
11.3	Rinsing (intermediate)	**Z14/** Arias Acid	H2O	30 sec	
11.4	Cr-etch	**Z14/** Arias Acid	Cr-etch @ RT (new solution)	15 sec	2 times
11.5	Rinsing (final)	**Z14/** Arias Acid	2 baths of H2O	30 sec	
11.6	Inspection	**Z14/** µscope	Stripping efficiency		
11.7	Thickness measurement	**Z4/** Bruker Dektat			
11.8	X-Y measurement	**Z5/** Nikon	100x magnification, alignment marks		
12	**CLEANING**				
12.1	Piranha 1	**Z2/** WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	Manual agitation to eliminate bubbles on wafers
12.2	Piranha 2	**Z2/** WB_UFT_Piranha	H2SO4:H2O2	5 min 100°C	Manual agitation to eliminate bubbles on wafers
12.3	Cascade tank	**Z2/** WB_UFT_Piranha			+ SRD full program
12.4	X-Y measurement	**Z5/** Nikon	100x magnification, alignment marks		

H2 : Runcard of the Borosilicate wafer (bottom wafer)

Step N°	Description	Equipement	Program / Parameters	Target	Remarks
1	**ANODIC BONDING**				
1.1	Bonding alignment	**Z6/** BA6			
1.2	Lateral contacting				piece of Al foil to make the contact between the BS and FS
1.3	Anodic bonding	**Z6/** SB6	Debiotech_Hydro_60V		
1.4	Inspection	**Z6/** µScope			
2	**DICING**				
2.1	UV tape application	**Z11/** Laminator	UV tape on both sides		
2.2	Dicing	**Z9/** DAD-321	Prog ID 1984 @ 1 mm/s **10.25 mm index**		Hairline measured by DAD-321: 252µm
2.3	Tape release	**Z9/** "UV-box"	2 min / side		

H3 : Runcard for the anodic bonding and dicing