POLITECNICO DI TORINO
Corso di Laurea Magistrale in Ingegneria Elettronica
Collegio di Ingegneria Elettronica, Fisica e delle Telecomunicazioni

Toward CMOS compatible on-chip micro-supercapacitors: Design, Fabrication and Analysis

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Anno Accademico 2017-2018

Acknowledgment

I would first like to thank my thesis supervisors Prof. Danilo Demarchi of Politecnico di Torino, Anderson Smith of Chalmers University of Technology. Always ready to help me whenever I ran into a trouble spot.

I would also like to thank all members of Microtechnology and Nanoscience department involve in this project and the staff of the Myfab cleanroom in Chalmers. You involved me with enthusiasm and professionalism, providing me with all the necessary facilities for the research.

My special thanks go to my family and friends. You supported and encouraged me during these years.

Finally, thanks to the main character of my present, past and future, Chiara. Thank you for reminding me how much I'm worth and filling my life with love.

Abstract

In this work are presented two steps toward the integration of microsupercapacitors (MSC) in semiconductor micro-systems.

The first step is the investigation of Palladium Pd as current collector material for vertical graphene (VG) electrodes in wafer-scale MSC fabrication. Palladium is known as a CMOS compatible metal but here is demonstrated that a Titanium (Ti) barrier is needed to prevent short-circuit.
Fabricated MSCs demonstrate a capacitance of $1.3\,\mu\mathrm{F/cm^2}$ with an energy density of $0.42\,\mu\mathrm{J/cm^2}$.

The second step is the development of a fabrication process for microsupercapacitor (MSC) where deposition of the electrode material, Graphene Oxide (GO) is performed using spin-coating. High temperature or chemicals aren't involved in this technique, making it suitable for application in CMOS compatible processes. Four groups of MSCs with 1, 5, 10 and 20 pairs of interdigital electrodes have been fabricated to study the influence of finger numbers on the MSC performances.

The 1-pair fingers device shows the highest capacitance of $0.47\,\mathrm{mF/cm^2}$ and an areal energy density of $0.0302\,\mu\mathrm{Wh/cm^2}$ which are very promising results. Others devices like the 20-pair showed a capacitance of $0.21\,\mathrm{mF/cm^2}$ which is less than half the previous device. The same level of average power density at $100\,\mu$ A/cm of $39.7\,\mu$ W/cm^2 has been found for all fabricated MSCs. This provocative result states that the power density is not necessarily dependent on the number of fingers. Accordingly, is not always advantageous to increase the number of fingers because energy density will then be reduced, while the fabrication complexity is increased. The fabrication process, which is at wafer-scale, is also a step towards large-volume production.

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Chapter 1

Introduction

As microsystems are reduced in size and start to be integrated in the Internet of Things (IoT) the need for integrated power supply and energy storage units which can be integrated at the same size scale is increased. For the development of self-powered implantable devices, environment sensor, portable and wearable electronics and MEMS systems, integrated power-sources are essential.

Nowadays, self-powered devices are based on batteries to provide the required power. Small size batteries are available in the market but share the same limitations of large-scale counterparts: limited lifetime and low power density. As an alternative to batteries, energy harvesters look promising as power supply for micro-systems. The possibility to harvest energy from environment, makes possible to power standalone micro-devices. However, currently energy harvesters are not able to power the devices continuously, but an energy storage unit is required.

For devices that require being in active mode periodically, is possible to distinguish two states: a standby state where the energy storage unit store the energy from the energy harvester and an active state where the device use the stored energy. Supercapacitors are suitable candidates for this purpose because of high power density which means they can be quickly charged and discharged. Moreover, the longer cycle lifetime with respect to batteries makes them promising for maintenance-free applications.

The push towards integration of energy storage units with microsystems requires the development of miniaturized energy storage devices, microsupercapacitors (MSC). However, there is difficulty in developing industrial-scale fabrication technique for mass production of high-performance microsupercapacitors that are compatible with fabrication technologies of microelectronic devices.

In this thesis project, CMOS (Complementary Metal-Oxide Semiconductor) compatibility of MSCs has been investigated following two paths. The first is the introduction of CMOS compatible materials as a substitute of commonly used not CMOS compatible materials. The second is the development of a fully CMOS compatible fabrication technique based on spin-coating.

1.1 Thesis Structure

The thesis is structured as follow.

In Chapter 2, macro supercapacitors will be first discussed. Carbon-based supercapacitors working principles and possible electrolytes choices, which together with the electrode carbon material are the most important part of supercapacitors' structure, will be presented. Moreover, a view on the electrochemical characterization techniques: Cyclic Voltammetry (CV), Electrochemical Impedance Spectroscopy (EIS), and Galvanostatic Charge and Discharge (GCD) are explained since will be used to evaluate the performances of the fabricated micro-supercapacitors.

In Chapter 3, the design and the structure of the micro-supercapacitors will be presented. The discussion will include both the design of the masks used in the fabrication process and the chosen features for the fabricated micro-supercapacitors, giving an explanation of every design choice.

In Chapter 4, the entire fabrication process which consists of equipment, process flow, and issues will be discussed. The novel fabrication method based on spin-coating of the electrode material and the choice of Palladium as current collector's material will be the key points of this chapter. In order to provide a brief theoretical support to the reader, all the used techniques will be first explained and then linked to the process step.

Chapter 5 will be dedicated to the performed measurements. The obtained results will be exposed and discussed, in comparison with other literature studies.

Chapter 6 all the obtained results will be summarized giving an overview on the project and introducing to the future studies and perspectives.

Chapter 2

Background

Supercapacitors are considered the third generation of capacitors, while electrostatic and electrolytic capacitors are respectively the first and second generation. Macro supercapacitors are here introduced instead of micro-supercapacitors because share the same working principle, the material used for the electrode and electrolyte, but are different in design, fabrication, and size.

The first prototype of supercapacitor based on carbon material electrode was developed by Becker in 1957 and showed a higher capacitance than comparable size counterparts[7]. The first practical supercapacitor was then invented almost twenty years later, in 1979 by Boos.[8]

The high power capabilities showed by these devices caught the interest of many industries and research groups working in the energy field, which started to invest on supercapacitor research and development, studying new material for electrode and electrolyte to improve performance and make this technology competitive in the market.

2.1 Electrochemical Double Layer Capacitors

Electrochemical capacitors, also known as supercapacitors consists of two metal plates, called current collectors with an electrolyte solution between them. Unlike electrolytic capacitors which are fabricated using two conduc-

tive foils (typically Aluminum or Tantalum) one coated with an oxide layer which acts as insulator and a spacer wet by the electrolyte, supercapacitors can achieve high capacitance values because the two metal plates are coated with a highly porous material. One plate, or electrode, is positive, and the other is negative.

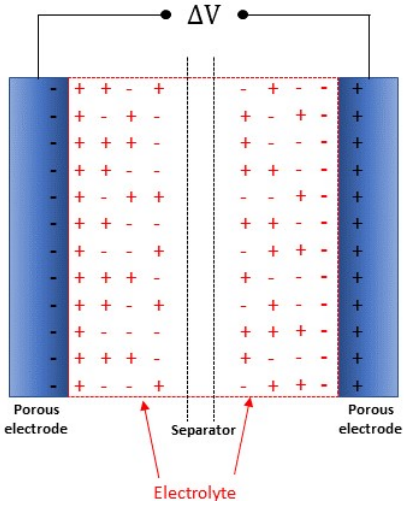

Figure 2.1: EDLC schematic

When a potential difference is applied between the two electrodes, an accumulation of charges appear on the electrodes structure. Due to Coulomb's force, the accumulation of positive charges on one of the two electrodes attracts an equal number of positive charges close to the electrode's surface. An opposite situation appears on the negative electrode. The electrolyte function is then to conduct ions in order to balance the charge on the electrodes.

The layers made of the electrode and electrolyte charges, represent an electric double-layer (EDL). These two layers, one for each electrode-electrolyte interface, are the space where the charges are electrostatically stored. The performances of the supercapacitor are linked to these layers.

A first EDL theory was carried out by Helmholtz[9], who describes the double-layer as a compact structure where any charge densities at the electrode surface are strongly screened by ions of opposite sign in the electrolyte

solution, forming a layer with a distance of the size of the solvent from the electrode. However, this model doesn't take into account the temperature effect on ions, which are not standing still in a compact array but are subjected to a thermal fluctuation according to Boltzmann principle.

To take into account the thermal effect, a subsequent model known as Gouy-Chapman [10][11] model describes the behavior of ions in the solution no more as a compact structure but as a scattered layer. Ions are scattered with higher concentration close to the electrode and lower concentration in the solution. The combination of the scattered layer and the charge density array on the electrode surface forms the so-called *diffuse layer*.

The thickness of the diffuse layer is not fixed as in the Helmoholtz model

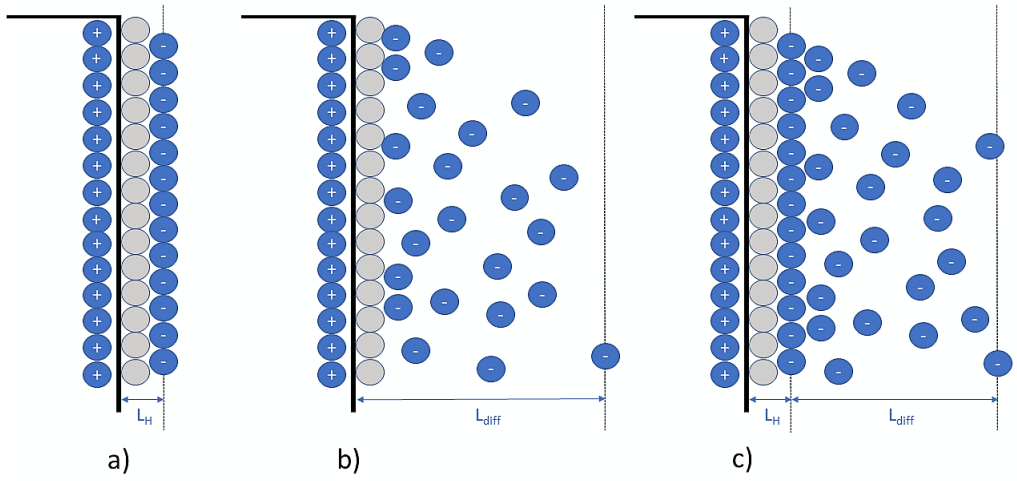

Figure 2.2: Representation of the EDLC Models: Helmholtz model a), Gouy-Chapman model b) and Stern-Grahame model c)

but depends on different parameters like temperature, the dielectric constant of the electrolyte solution and electrolyte concentration. Under low-temperature conditions, the diffuse layer becomes very thin leading to a compact electric double layer as in the Helmholtz model. This result suggests the coexistence of the two layers, as adopted by the Stern-Grahame model[12][13].

In this model the overall double-layer capacitance C_{dl} is considered as the series of two capacitors:

$$\frac{1}{C_{dl}^{+}} = \frac{1}{C_H} + \frac{1}{C_{diff}} \tag{2.1}$$

C_H related to the Helmholtz type compact double layer and C_{diff} that is the capacitance of the diffuse region introduced by the Gouy-Chapman model. The equivalent circuit is presented in figure 2.3.

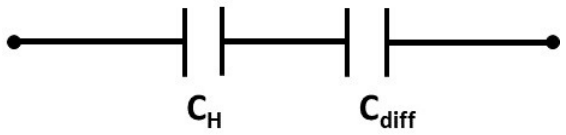

Figure 2.3: Stern-Grahame equivalent circuit

A double-layer is established at each side of the electrode, meaning that the overall capacitance of the supercapacitor can be seen as the series of two differential capacitance:

$$\frac{1}{C_{dl}} = \frac{1}{C_{dl}^{+}} + \frac{1}{C_{dl}^{-}} \tag{2.2}$$

Considering supercapacitors with identical electrodes is clear from the formula that the total capacitance of the double-layer is half the capacitance of the single electrode.

Knowing the total capacitance of the cell is possible to calculate a fundamental parameter for performances evaluation of the supercapacitor, the energy density. The expression of energy density can be written as:

$$E = \frac{1}{2} C_{dl} V_{sc}^2 \tag{2.3}$$

where C_{dl} is the total double layer capacitance and V_{sc} voltage windows apply to the cell. This formula comes from the evaluation of the energy stored in a capacitor as the work to charge the capacitor. Charge a capacitors means carrying a quantity of charge on the two plates. The work done to move a quantity of charge dq from one plate to the other plate is equal to Vdq. The

element of energy stored becomes: $dE = Vdq = \frac{q}{C}dq$. Calling Q the total amount of charge stored in the capacitor when the voltage window is applied to the two electrodes, then the stored energy is obtained from the integral:

$$E = \int_0^Q \frac{q}{C}dq = \frac{1}{2}\frac{Q^2}{C} = \frac{1}{2}CV^2 \tag{2.4}$$

where the definition of capacitance $C = \frac{Q}{V}$ has been used.

The energy density is strictly related to the electrolyte choice since each electrolyte solution has a different maximum voltage window. For the most of practical applications, is better to use the specific energy density, obtained dividing the energy density E by the active material mass, m:

$$E_m = \frac{E}{m} \tag{2.5}$$

The other important parameter is the power density, that describes how fast can be charged and discharge the capacitor, and its expression is:

$$P_{max} = \frac{1}{4m}\frac{V_{sc}^2}{R_{ESR}} \tag{2.6}$$

where V_{sc} is the maximum voltage windows of the electrolyte and R_{ESR} is the equivalent series resistance (ESR) that is an ohmic component of the capacitor that takes into account several phenomena: external contact resistance, the contact resistance between the current collector and the electrode layer and the electrolyte resistance. As the energy density, also the power density is more popular and useful to be defined as the specific power density, for this reason, the m term appear in the formula.

To visually compare and evaluate the performances of electrochemical energy storage devices, Ragone plots are used. Along the vertical axes is reported the specific power density, while on the horizontal axis the specific energy density. Is reported an example of Ragone plot (figure 2.4) which confirms that supercapacitors have higher specific power density compared to batteries but less specific energy density.

To be able to use supercapacitors as storage devices, the first challenge to overcome is the low specific energy density.

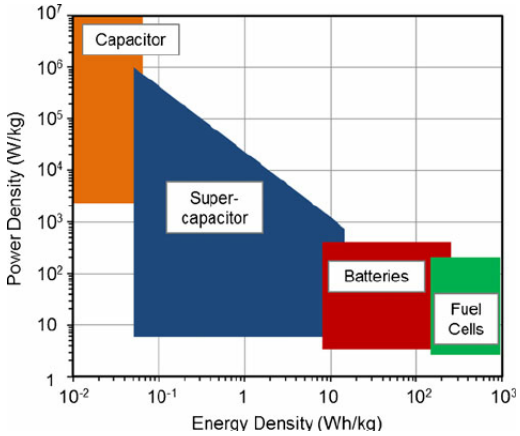

Figure 2.4: Ragone plot of different electrochemical energy storage devices [1]

2.2 Electrode Materials

The electrode material plays an important role in the definition of the capacitance and energy density of the device. A correct choice of the material can significantly increase the performance of the supercapacitors. As presented in the previous section, the fundamental part of the supercapacitor is the double-layer at the electrode-electrolyte interface. Choosing an electrode material with a high surface area would increase the overall capacitance and the specific energy density.

Electrochemical stability and high electrical conductivity, which mean low resistance of the electrode layer and high power density, are other important properties for the electrode material. Carbon-based materials are usually used since well fit all those requirements and show very high surface areas thank highly porous structures.[14]
The porosity of the electrode material is a crucial parameter for the performances of the supercapacitor. Three are the categories of pores based on size: macropores with a size greater than 50 nm, mesopores with a pore size range between 2-50 nm and micropores with a size lower than 2 nm.[15]

Despite micropores, which are too narrow and deep and the electrolyte ions may have difficulties to penetrate them, mesopores and micropores make a significant contribution to the surface area and hence specific capacitance. A correct match between the electrolyte ions size and the pore size can

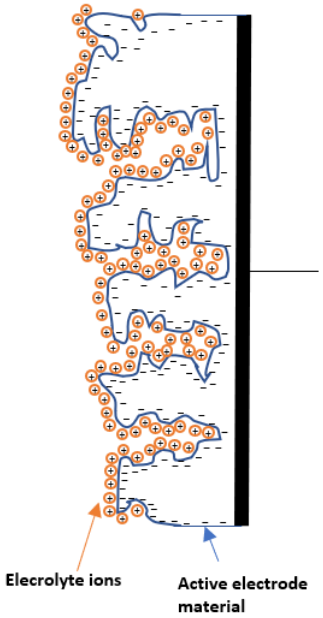

Figure 2.5: Representation of an EDLC's electrode with porous electrode materials

strongly increase the performances of the supercapacitors.[16]

In the next sections are described more into detail properties and performances of electrode materials which have been used or are intended to be used in this project.

2.2.1 Activated Carbon (AC)

Activated carbons are the most basic high surface area carbon material, which is the reason why are widely used materials for supercapacitors electrode, combining low cost and good electrical properties [17][18].

Carbonaceous materials are the precursors for the production of activated carbons. The terms *activated* is related to the process which makes porous the carbon structure, increasing the surface area. Two are the methods typically used for the activation: thermal (or physical) and chemical.

In thermal activation, two gasifying agents, carbon dioxide and water vapor are used to remove carbon atoms from the structure of the carbon precursors. Temperatures ranging from 700 to 1200 °C are involved.[19]

In chemical activation the modification of the precursor's structure in due to the use of chemicals as phosphoric acid (H_3PO_4), or zinc chloride ($ZnCl_2$). Precursor materials are pitches or resins derived from coal and petroleum. Is possible to combine the two activation process to have a finely controlled porosity of the carbon. Alternative carbon precursors are derived from wood, polymers, and hard shells.

Increasing the surface area does not imply a direct increment of the capacitance, as many studies show the relation between pores and electrolyte ions size is important. As presented in table 2.1 despite some samples have a very high value of surface area, the value of specific capacitance is lower than other samples with a lower surface area value.

AC precursors	Specific Surface Area ($m^2\ g^{-1}$)	Specific Capacitance ($\mu F\ cm^{-2}$)
Coal	3150	9.9
Semi-Coal	3190	7.0
Pitch Mesophase	2660	11.0
Pitch Semi-Coke	2750	9.5
Commercial AC	1900	10.4

Table 2.1: Examples of specific surface area and capacitance of AC precursors

All these different types of ACs have been tested with the same aqueous electrolyte H_2SO_4. This proves, as discussed in several articles[20][21][17], that in order to increase the capacitance value, a good match between ions and pore size is needed.
Capacitance values of devices with activated carbons as electrode material are in general in the range from 100 to 200 Fg^{-1} in aqueous electrolytes and from 50 to 150 Fg^{-1} in organic electrolytes.[22]

Being able to well control pore structure could effectively improve the performances of AC based supercapacitors. Unfortunately, pore structure control is still challenging.

2.2.2 Carbon Nanotubes (CNT)

More advanced carbons are being studied for their potential in controlling structures and enhanced properties compared to activated carbon. Carbon nanotubes are considered as nanostructured carbons. Their name derives from their cylindrical structure and diameter size, with the walls made by one Graphene sheets. These sheets consist of a single-atom-thick sheet of carbon. Rolling angle of the graphene sheet and size are two parameters that set the nanotube properties.

The hollow structure of CNTs creates a unique pore structure together with excellent electrical properties and thermal stability, make this material suitable for supercapacitor electrode application.[23][24]

Single-walled carbon nanotubes (SWNTs) and multi-walled carbon nanotubes (MWNTs) are two categories of CNTs which differ for the number of concentric nanotubes. Both categories have been studied as energy storage electrode materials. CNTs have relatively small specific surface area compared to ACs (Table 2.1). Specific capacitance of between 10 and $350\,\mathrm{Fg}^{-1}$ have been reported for different preparations of CNTs [23][24].

The orientation of CNTs has been showed to have a strong impact on device performances. Interweave CNTs are characterized by an irregular pore distribution that makes ions diffusion slower compared to aligned CNTs.[25] For this reason, the use of a vertically oriented structure seems to be very promising for high power density applications.

To improve energy density of CNTs, is possible to increase their specific surface area via chemical activation.[26] Porosity and conductivity are two important parameters which have a strong impact on performances of the device. Optimizing these parameters, capacitance and power performance can be improved.

A high specific surface area of $1059\,\mathrm{m}^2\mathrm{g}^{-1}$ and specific capacitance of $524\,\mathrm{Fg}^{-1}$ have been obtained in an interesting application based on CNT-aerogel electrode material. Carbon aerogel has been dispersed throughout a CNT host matrix, without affecting the structure, obtaining the composite

material.[27]

The limited surface area of CNTs and high cost of production still limit their practical applications as EDLC electrode material.

2.2.3 Reduced Graphene Oxide (rGO)

Interesting properties as excellent electrical conductivity and chemical stability have increased the interest towards graphene-based materials for applications in supercapacitors and in other energy storage devices .[28]

Graphene oxide consists of monolayer and few-layer graphene, spaced with water. Oxygen-containing functional groups as hydroxyl (OH), carboxyl (C=O) and epoxy groups (C−O) decorates the basal plane of graphene sheets stabilize the bi-dimensional structure.[29]

Due to high affinity to water molecules by these groups, Graphene Oxide is hydrophilic and can be readily dispersed in water. The dispersibility in water makes the deposition of the thin films of Graphene Oxide straightforward.

Reducing graphene oxide to produce reduced graphene oxide, is the process which allows the conversion, in terms of structure, of GO into graphene. Graphene oxides can be converted into graphene by a number of ways. All methods are based on chemical, thermal or electrochemical treatment. To be used as electrode material in supercapacitors, reduction of GO is essential to make the material conductive thanks to the electronic conjugation.

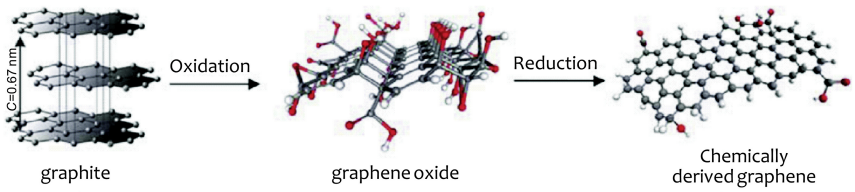

Figure 2.6: Graphene oxide reduction[2]

Figure 2.6 shows the effect of graphene oxide reduction[30].

High volumes of natural graphite can be oxidized to obtain graphene oxide. This process is a cost-effective method to derive GO, which is a precursor of graphene.

Good values of specific capacitance are showed by devices which use rGO as electrode material. As already discussed, is not possible to display capacitance values without including the influence of electrolytes. Devices that use gel electrolyte, showed specific capacitance values of $81\,\mathrm{Fg}^{-1}$ at $0.5\,\mathrm{Ag}^{-1}$[31], while for aqueous solution devices specific capacitance ranged from $130\,\mathrm{Fg}^{-1}$ at $1\,\mathrm{Ag}^{-1}$ to $54.9\,\mathrm{Fg}^{-1}$ at $10\,\mathrm{Ag}^{-1}$[32].

2.2.4 Vertically Oriented Graphene (VOG)

Graphene is a lattice of sp^2 hybridized carbon atoms placed in a hexagonal structure with promising properties like excellent electrical and thermal conductivity, high surface area and good chemical stability [33][34].

As for CNTs, even Graphene sheets arrangement has been showed to have a strong impact on device performances. Growth orientation of graphene could be horizontal or vertical, obtaining sheets in parallel or perpendicular to the substrate.

Different applications, i.e supercapacitors, lithium-ion batteries, gas sensor, usually require different morphology and structures of VG nanosheets. When is used as electrode's material for EDL capacitors, a high surface area is desired to maximize ions trapping. The inter-sheet distance needed to be adjusted to allow the ions to diffuse and be absorbed optimizing the energy storage performance.

Chemical vapor deposition (CVD) is the typical method used for VG synthesis. Plasma-enhanced CVD (PECVD), involving a plasma region, offers several advantages: a low temperature of the substrate, selectivity of the material's growth and good control of the graphene arrangement. Those advantages make PECVD a preferable method with respect to thermal CVD.

In figure 2.7 a schematic of graphene nanosheets grown parallel to the current collector are displayed. This morphology leads to a higher acces-

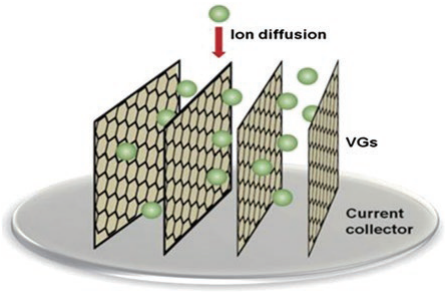

Figure 2.7: Vertically Oriented Graphene structure and ions diffusion.[3]

sibility of electrode material for electrolyte's ions, improving capacitance. Moreover, other materials used for ELDCs are characterized by a porous structure which limits their applications to low-frequency devices. The vertical orientation and inter-sheet space are directly accessible, facilitating ion diffusion in the nanostructure and minimizing the porosity effects that limits EDLCs to work at low frequency. VG as electrode material makes possible to use EDLCs in high-frequency applications.[3]

EDLCs based on VG electrode material directly growth on metallic current collector showed specific capacitance of $129\,\mathrm{Fg}^{-1}$ and $112\,\mathrm{mVs}^{-1}$ respectively in aqueous and organic electrolyte[35].

2.3 Electrolyte

The electrolyte is one of the key factors of supercapacitor's performance. According to the energy density and power density equation, being able to increase the voltage windows means increase these two parameters at the same time. As shown in eq2.3, the energy density is proportional to the square of the cell voltage, therefore being able to improve the operating voltage would be more effective than increasing the electrode capacitance. Limiting factor of the maximum operating cell voltage is the electrochemical stable potential window of the electrolyte (ESPW). Furthermore, electrolyte ions conductivity affects the internal resistance. The viscosity, boiling and freezing point play an important role in the thermal stability range and the electrochemical decomposition is related to the aging and failure of supercapacitors.

Requirements for an ideal electrolyte are:

- Wide electrochemical stable potential window
- High ionic conductivity
- High chemical and electrochemical stability
- Wide operating temperature range
- Low volatility and flammability
- Environment friendly
- Low cost

What follows is a brief discussion about four families of electrolytes widely used for EDL supercapacitors: aqueous electrolytes and organic electrolytes, gel polymer electrolytes and ionic liquids.
The discussion will be focused on the advantages and drawbacks of each type of electrolyte.

2.3.1 Aqueous Electrolytes

Aqueous electrolytes are largely used in the research and development because are almost inexpensive and easy to handle, simplifying the fabrication process. Normally, aqueous electrolyte exhibits high ionic conductivity which is beneficial for lowering ESR and improving the power delivery. Unfortunately, due to the decomposition of the water, these type of electrolyte are based on, voltages window is limited to $\approx$ 1V. This drawback strongly limits the energy density and is the main reason why such kind of electrolytes are not used in commercial applications. Moreover, the presence of water restricts the temperature range to its freezing and boiling point.

The low viscosity of aqueous electrolyte and corrosive problems should be taken into account. Since the main goal of this project is to move toward CMOS compatibility, this kind of electrolyte is to be avoided because tents to spread on the whole wafer reaching areas where is unwanted. Being corrosive could damage or degrade neighbor devices.

Aqueous Electrolyte	Electrode material	Cell voltage (V)	Temp.(°C)	Ref.
H_2SO_4	AC fibers	0.9	RT	[36]
KOH	Graphene planes	1	-	[37]
$NaNO_3$	AC	2	0 to 60	[38]
Na_2SO_4	AC	1.6	RT	[39]

Table 2.2: Example of devices with aqueous electrolytes and carbon-based electrode's material

2.3.2 Organic Electrolytes

Organic electrolytes dominate the commercial market thanks to their wider ESPW (typically in the range of 2V to 3V) with respect to aqueous ones. As already discussed, enlarging the operating cell voltage can determine a significant improvement in power and energy density.

Despite this advantage, other problems should be considered when organic electrolytes are used. Unlike aqueous electrolytes, organic electrolytes are difficult to handle because requires a controlled environment to remove possible contaminants and impurities that can degrade the performances and present safety risks due to the flammability, volatility, and toxicity. Moreover, organic electrolytes usually have a lower ionic conductivity compared to aqueous electrolytes, resulting in a much higher ESR which can limit the maximum power density. Temperature range for supercapacitors where organic electrolytes are used is in the range -40 to 60 °C.

Organic Electrolyte	Electrode material	Cell voltage (V)	Temp.(°C)	Ref.
$TEABF_4$/ACN	Carbon nanosheets	2.7	-	[40]
$TEABF_4$/PC	Graphene-CNT	3	RT	[41]
TEAODFB/PC	AC	2.5	-40 to 60	[42]

Table 2.3: Example of devices with organic electrolytes and carbon-based electrode's material

2.3.3 Ionic Electrolytes

Ionic liquids (ILs) are salts with melting points below 100 °C [43], which mean are liquid at low temperature. Ionic liquids with ESPW above 3V, have been studied as an electrolyte for supercapacitors applications.

ILs are based on combinations of organic anions and inorganic or organic cations which reduce lattice energy lowering the melting point. These electrolytes have acquired a lot of interest in particular for the possibility to design and customize physical and electrochemical properties by changing the electrolyte composition. With the right cations and anions combinations, is possible to increase the thermal and electrochemical stability, obtain ILs with negligible volatility and flammability risk.

Despite the wider voltage window, the high viscosity and low conductivity of ILs affect the ESR values reducing the power performance and limit their practical applications. This issue is more serious at low temperature, up to room temperature.

Ionic Electrolyte	Electrode material	Cell voltage (V)	Temp.(°C)	Ref.
$LiClO_4$/PC	Activated carbon fibers	2.3	-	[44]
$BMIPF_6$	Graphene oxide	2.4	-	[45]
$PYR_{1(2O1)}TFSI$	PICACTIF SUPERCAP BP10	3.7	-30 to 60	[46]

Table 2.4: Example of devices with ionic electrolytes and carbon-based electrode's material

2.3.4 Gel Polymer Electrolytes

Gel polymer electrolytes belong to the family of solid-state electrolytes for supercapacitors and consist of a polymer matrix and a liquid electrolyte. The solid-state electrolyte can serve as the ionic conducting element but also simplify packaging and fabrication process for liquid-leakage free supercapacitors. Among solid-state electrolytes, gel polymer electrolytes are the

ones with the higher ionic conductivity thanks to the presence of a liquid phase, which is also the reason why in some studies are defined as semi solid-state electrolytes and dominates the solid electrolyte-based supercapacitor products. The use of this branch of electrolytes has the main advantage of allowing bendable and flexible structures, expanding the applications spectrum to flexible and wearable electronics.

Various matrices can be used as host polymer: poly-vinyl alcohol (PVA), polyacrylic acid (PAA), poly-methylmethacrylate (PMMA), poly-ethyl oxide (PEO). Matrices act only as a structural component of the solid-state electrolyte to offer mechanical strength, but do not play any role in the electrochemical behavior of the device.

Water or organic solvents can be used as solvents (or plasticizer). Electrolytes based on water are called hydrogel polymer electrolytes while the seconds organogel electrolytes.

Hydrogel polymer electrolytes are similar to aqueous electrolytes, sharing the same problems like narrow ESP and limited thermal stability. Organogel electrolytes allow to a wider working cell voltage and high cyclic stability but normally suffer from low ionic conductivity.

Gel Polymer Electrolyte	Electrode material	Cell voltage (V)	Temp.(°C)	Ref.
PVAPVA	Graphene/carbon black	1	RT to 70	[47]
PVA/H_2SO_4	Carbon Cloths	1	-	[48]
$PYR_{14}TFSI$	AC	3.5	25	[49]

Table 2.5: Example of devices with gel polymer electrolytes and carbon-based electrode's material

2.4 Electrochemical Characterization

As presented in the previous sections, the supercapacitor's structure is made of several components. In order to investigate the effect and influence of each

component, different electrochemical characterization techniques have been used.
Here follow a theoretical description of these techniques as support for the comprehension of the results reported in Chapter 5.

2.4.1 Cyclic Voltammetry

Cyclic voltammetry (CV) is a potential-dynamic electrochemical technique, which can be employed to characterize the electrode material in terms of capacitive behavior and stability.[50]

During CV measurements, the current is measured against the voltage. The applied potential is the controlled parameter and linearly changes between an upper and a lower limits as shown by arrows in figure 2.8 for a desired number of cycles.

The slope of the potential line is known as *Potential scan rate*. Changing the potential scan rate can be useful to study electrode kinetics and other non-ideal phenomena such as pseudo-capacitance and electrolyte degradation. If the potential scan rate is too fast, the electrochemical reactions on the electrode may have no time to occur, giving untrue results.

For an ideal electric double layer supercapacitor, the voltammogram has a rectangular shape. Due to non-ideal phenomena mentioned above, the voltammogram for a real supercapacitor deviates from the rectangular shape. Figure 2.8 displays both ideal shape and how non-ideal phenomena affect the CV shape.

Pseudo-capacitance behavior is represented by peaks in the CV curve (figure 2.8c) originates from the faradic red-ox reactions taking place at the surface of the electrodes. Due to different resistances involve in the system, a delay of potential during reversing the potential sweep can be observed, this phenomenon is called rate limitation (figure 2.8b).
The electrolyte degradation happens when the voltage range exceeds the maximum voltage window of the electrolyte, peaks appear at the voltage upper and lower limits.

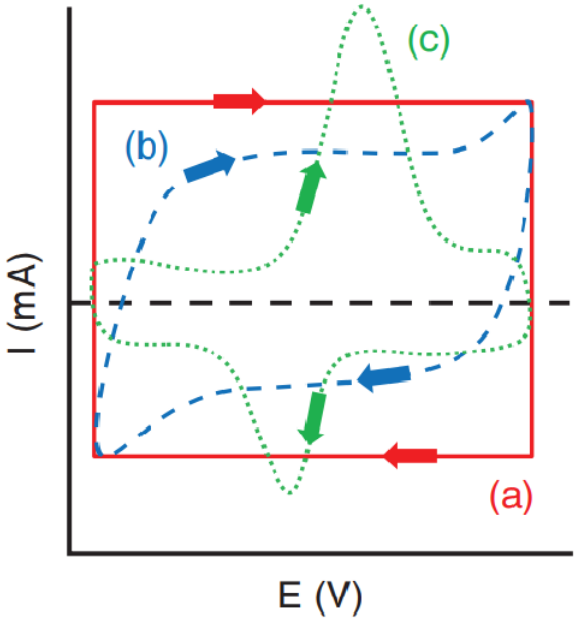

Figure 2.8: Cyclic voltammogram curves of (a) ideal capacitor, (b)EDLC, and (c) pseudocapacitive materials.[4]

2.4.2 Eletrochemical Impedance Spectroscopy

Eletrochemical Impedance Spectroscopy (EIS) is a technique for electrode-electrolyte interfaces characterization.

In this technique, the system is perturbed using a small sinusoidal potential, applied in the frequency range 1 mHz-1 MHz. The ratio of the corresponding sinusoidal voltage and current give the complex impedance for a particular frequency. In a capacitor, the current and the voltage have a phase displacement of an angle (ϕ), where ϕ is 90° for an ideal capacitor. Defining the applied voltage as:

$$V(\omega) = V_p exp(j\omega t) \tag{2.7}$$

The corresponding current signal is:

$$I(\omega) = I_p exp(j(\omega t - \phi)) \tag{2.8}$$

$$Z(\omega) = \frac{V_p}{I_p} exp(-j\phi) = Z_{Re} + jZ_{Im} \tag{2.9}$$

The resulting impedance modulus is defined as:

$$|Z(\omega)| = \sqrt{Z_{Re}^2 + Z_{Im}^2} \tag{2.10}$$

and the phase angle:

$$\theta = \arctan\left(\frac{Z_{Re}}{Z_{Im}}\right) \tag{2.11}$$

The impedance derived from the EIS data is generally plotted in two ways: the Nyquist plot and Bode plot. In a Nyquist plot, the imaginary part of impedance (Z_{Im}) is plotted against the real part of the impedance(Z_{Re}). For an ideal EDLC, the Nyquist plot is represented by a vertical line containing only the double layer capacitance, $Z_{Re} = 0$. However, the typical plot contains three regions, an intercept at x-axis at high frequency (R_{esr}), a semi-circle region (R_{ct}) presents at high frequencies and associated with the the resistance between electrode and electrolyte, a region characterized by a line with a slope of 45° called Warburg region (W) and at low frequency, a vertical line that corresponds to the capacitive behaviour.

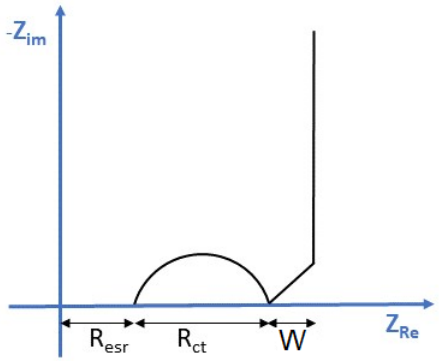

Figure 2.9: Example of EIS curve for an EDLC

As already discussed, R_{esr} represents the real impedance, which is the sum of different resistance as contacts, current collector and bulk electrolyte resistances. The diameter of semi-circle represents the charge transfer resistance of the electrochemical reaction producing pseudocapacitance[51]. The W region on Z_{Re} represents diffusion resistance, which arises at high frequency due to the small time ions have to diffuse in small pores of the electrodes.
The resulting equivalent circuit model of a supercapacitor is presented in

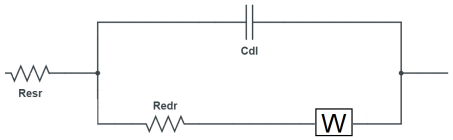

Figure 2.10: EDLC equivalent circuit

figure 2.10.

The "W" component is the so-called $Warburg$ element which characterizes the Warburg region.[52]

The Bode plot gives the information about the frequency behavior of the supercapacitor. The modulus of the impedance and its phase angle are plotted versus the frequency. A -90° phase angle represents the ideal capacitive behavior of the supercapacitor at particular frequency range. In real supercapacitors, the phase angle does not reach -90° mainly due to the series resistance R_{esr} of the system [53].

The frequency value where the phase angle reaches -45° is called the *characteristic frequency* (f_0) and it is used to compare the frequency behavior of supercapacitors. At frequencies above f_0 the resistive behavior of the impedance dominates whereas below f_0 the capacitive behavior dominates.

2.4.3 Galvanostatic Charge and Discharge

Galvanostatic Charge and Discharge (GCD) is a reliable approach to determine capacitance, energy density, power density, equivalent series resistance, and cycle lifetime of a supercapacitor. A GCD cycle consists of charge the supercapacitor applying a constant current up to a wanted voltage and then discharge inverting the current. The cell voltage is recorded as a function of charging and discharging time. Unlike cyclic voltammetry where a constant voltage sweep is applied since in GCD a constant current is applied, obtained performance metrics are not dependent on voltage sweep.

For an ideal supercapacitor, the charge and discharge plots should be triangular in shape, like in figure 2.11a.

Real supercapacitors do not fit such linear plots, non-linearity appears in

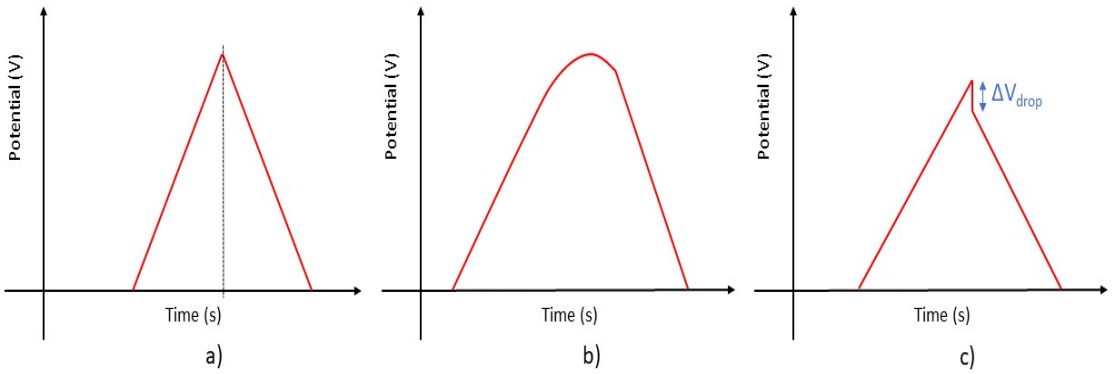

Figure 2.11: GCD curves of ideal EDLC and the effect of non ideal phenomena

the plots pointing out non-idealities in the supercapacitor behavior.

An exceeding of the electrolyte stable window potential is an example of such non-idealities and the resulting GCD plot is reported in fig 2.11b. The plateau in the GCD plot represents a non-capacitive process that is the decomposition of the electrode material or the electrolyte[54].

Figure 2.11c shows a second non-ideal behavior, the IR drop. This is a voltage drop due to the internal resistance at the beginning of the discharge represented by the vertical line in the discharge curve. The equivalent series resistance, or ESR, can be calculated through the IR drop by the equation:

$$R_{esr} = \frac{\Delta V_{drop}}{\Delta I} \tag{2.12}$$

Charge and discharge over many cycles is a method to investigate the degradation of a supercapacitor and to observe the changes in both specific capacitance and equivalent series resistance. The capacitance of a supercapacitor will gradually reduce while the equivalent series resistance will increase after many cycles, leading to decreases in performances of the device.

Chapter 3

On-chip Micro-supercapacitors

Due to the large size, conventional supercapacitors are not suitable for many applications like flexible and wearable electronics or integration with on-chip devices. For those applications, miniaturized power sources are required. Furthermore, manufacturing methods used for supercapacitors are not compatible with micro-system fabrication. On-chip supercapacitors fabricated with techniques compatible with CMOS-based microelectronics devices are needed. As anticipated, micro-supercapacitors are based on the same working principle of the conventional supercapacitors, but differ for a different approach in the design, architecture and fabrication technologies.

In this work will be solved challenges which are faced due to the transition from macro to micro-scale. CMOS compatibility is one of the hardest challenges to overcome because of limited choices of materials and fabrication methods. Common techniques used for thin electrode fabrication such as sputtering or chemical vapor deposition (CVD) are not compatible with CMOS technologies. Moreover, most of these methods are not reliable for large volume applications but limited to the scope of the research.

In chapter 5, will be presented a fabrication method for carbon material electrodes based on spin-coating, which is fully CMOS compatible and potentially suitable for large-volume productions.

3.1 Design

The device design for micro-supercapacitors is a very important aspect to be considered. Different architectures introduce advantages and disadvantages that must be taken into account. Follow a brief discussion of the chosen architecture and the design of the wafer's masks suitable for large volume production used for fabrication.

3.1.1 Device Architecture

First micro-supercapacitors where designed following the same 2D architecture of thin film micro-batteries. Two thin film electrodes and a solid electrolyte are stacked on top of each other as presented in figure 3.1. Despite

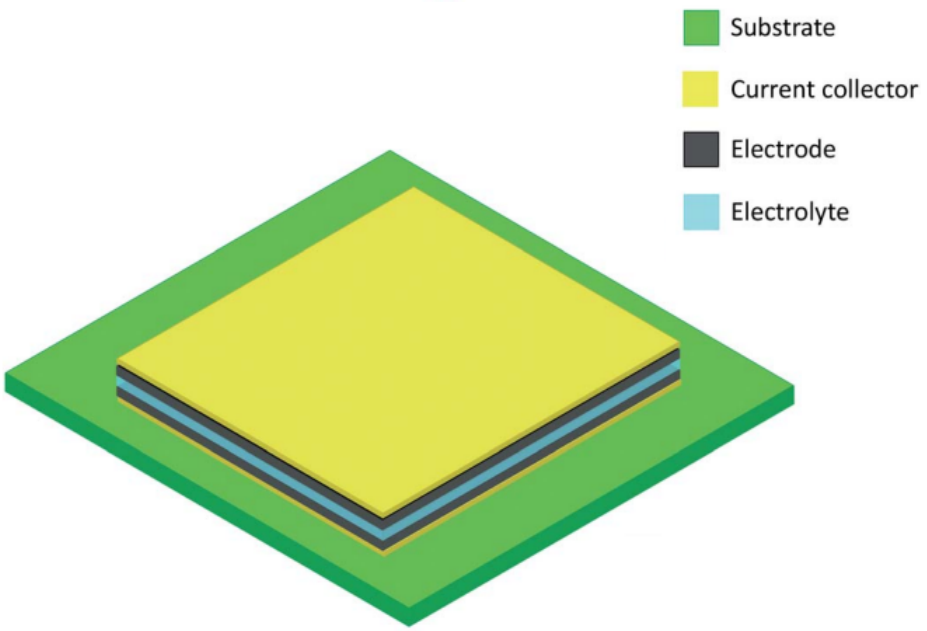

Figure 3.1: 2D in-plane architecture[5]

the simple design, the performances are limited to the thickness of electrodes. Thicker electrodes can improve capacitance and energy density but increase the length of ion diffusion, affecting the power density

An alternative to this 2D architecture has been chosen for this project (Figure 3.2). In this architecture, each electrode consists if several fingers

interdigitally arranged on a substrate. The advantage of this architecture is that electrodes are on the same plane, facilitating the fabrication and integration of the device.

The gap between the fingers can be controlled accurately by using conventional microfabrication techniques, small fingers' distance means decreasing the ion transport resistance in the cell. Furthermore, in such architecture also the sides of the fingers are exposed to the electrolyte, increasing the accessibility of the electrodes. With this architecture is possible to increase the thickness of electrodes improving capacitance and energy density, without affecting power density.

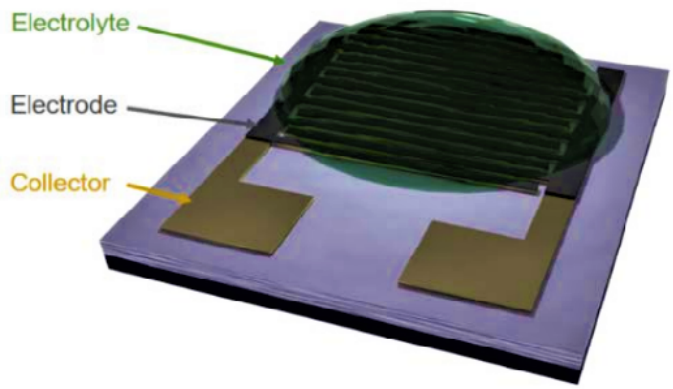

Figure 3.2: 2D interdigitated architecture

3.1.2 Geometries

To understand the impact of the architecture on the performances, micro-supercapacitors with different fingers' width, fingers' number and the gap between fingers have been designed and fabricated. In table 3.1 are reported the values of the device configurations.

	Finger Width (mm)	Finger Length (mm)	Gap (mm)	Finger N.
1F40um	4.76	2.2	0.04	1
5F20um	0.44	4.2	0.04	5
10F40um	0.2	4.2	0.04	10
20F40um	0.08	4.2	0.04	20
10F20um	0.2	4.2	0.02	10
10F60um	0.2	4.2	0.06	10

Table 3.1: Device configurations

For micro-supercapacitors the weight of materials at the electrode is almost negligible, that makes energy density (Eq 2.3) and gravimetric specific capacitance inappropriate parameters for evaluating the performances. When deal with micro-supercapacitors, is better to relate performance metrics to the footprint area of the device than to the weight of materials at the electrode. Areal energy and power density become the performance metrics.

In table 3.2 three different areas have been calculated since the goal is to evaluate the impact of the device and material area. In figure 3.3 the meaning of the areas reported in table 3.2 are illustrated. The device area is calculated considering the surface where the electrode material is deposited. The material area is calculated by subtracting the area of the gaps from the device area, obtaining an area parameter that depends only on the surface the electrode exposes to the electrolyte.

For four device geometries: *1F40um*, *5F20um*, *10F40um* and *20F40um* the device area is kept constant, but the material area changed. On *10F40um*, *10F20um* and *10F60um* the material area that is kept constant while the device area is changed.

	Material Area (cm^2)	Device Area (cm^2)	Whole Device Area (cm^2)
1F40um	0.2094	0.211344	0.27528
5F20um	0.1848	0.211344	0.27528
10F40um	0.168	0.211344	0.27528
20F40um	0.1344	0.211344	0.27528
10F20um	0.168	0.193596	0.27404
10F60um	0.168	0.229244	0.27652

Table 3.2: Area calculations

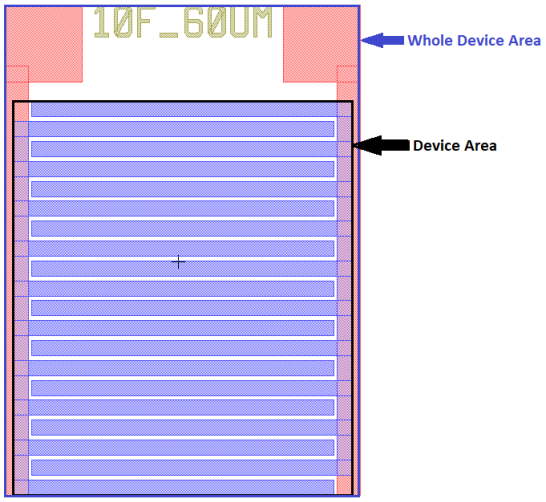

Figure 3.3: Illustration of areas meaning

3.2 Mask Design

Two masks (Figure 3.4) were designed using the CAD-program L-Edit which is a common program for mask design.

A 2" wafer, corresponding to 51mm diameter was used. In the first mask, only micro-supercapacitors are present, as already introduced in the *Geometry* section, 6 different supercapacitor's geometries were designed.

In figure 3.5 are shown the L-Edit model for each supercapacitors design.

The red parts indicate areas where the current collector material, palladium or gold, has been deposited, while the blue part indicates areas where the electrode material is wanted.

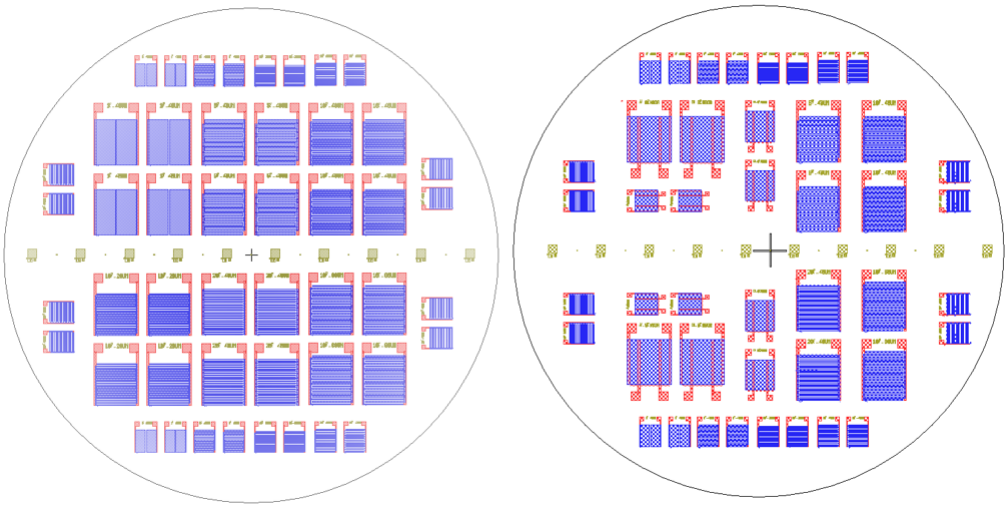

Figure 3.4: Masks designed using L-Edit

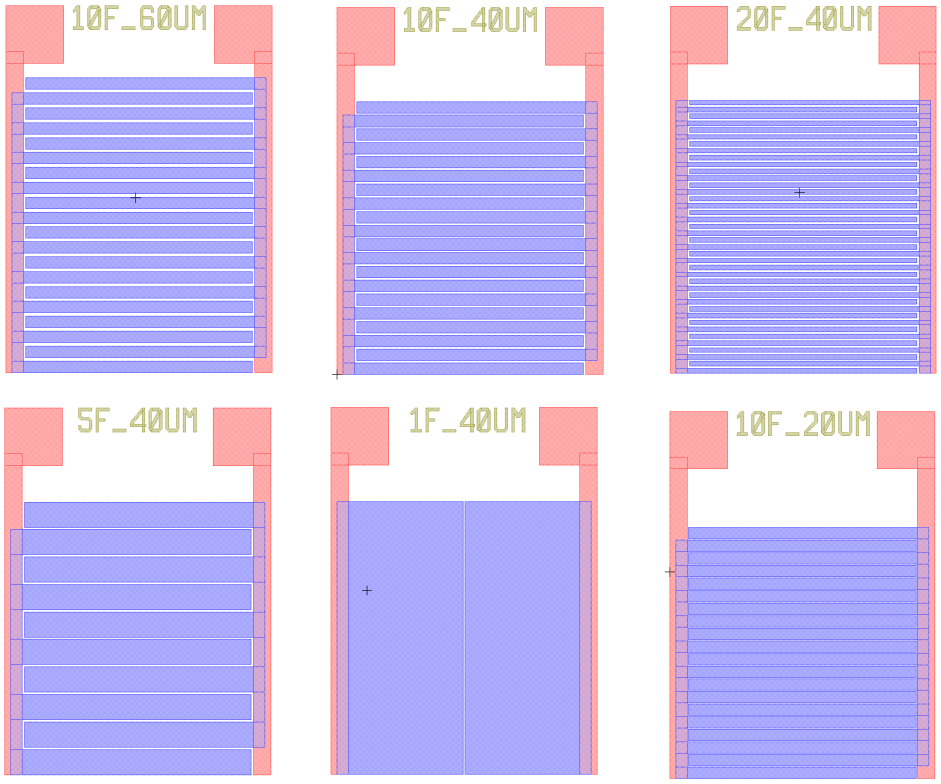

Figure 3.5: L-edit models of different device geometries

To distinguish each supercapacitors' configuration text markings are placed close to the device. Every device is labeled with a text in the form nF_mUM, where n and m are numbers, respectively indicating the number of fingers and gap in between.

All the device are placed into a grid structure to facilitate the dicing later on.

A test structure to verify the photolithography process is displayed in figure3.6a. If the checkered pattern squares are not clear and overlapping

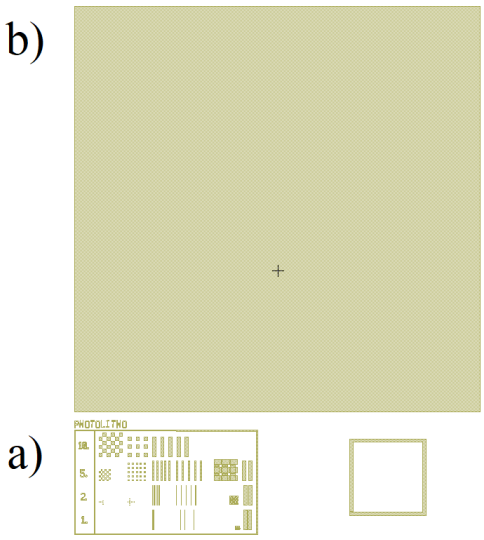

Figure 3.6: Test structures: a)Photolithography b) Etch rate

each other, this indicates that the wafer has been overexposed. Moreover, this structure is an indicator of the maximum achievable resolution.

Since one layer for the current collector and another for the electrode are needed, alignment marks (Figure 3.7) are placed in the middle of the wafer. Is very important to have the overlapping of patterns for a reliable process.
In addition to the test structure for observing the exposure effects, another test structure is shown in figure 3.6b is used to measure etch rate. The big square is a 1 mm^2 trench to measure the etch depth, while the small one is a 10 μm wide groove to measure how much the sides are over-etched.

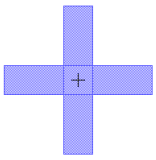

Figure 3.7: Alignment mark

In the second mask, some of the supercapacitors are replaced by humidity sensors. Such sensors, as shown in figure 3.8 are made by five contact pads and the electrode material cover the whole area between the contact pads, without a fingers structure.
Also in this mask, test structures have been placed.

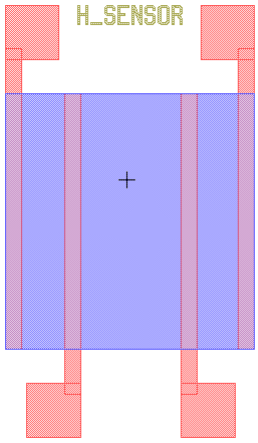

Figure 3.8: Humidity sensor

Chapter 4

Microfabrication process for on-chip supercapacitors

The fabrication method is the heart of this project, an unconventional technique such as spin-coating is used to deposit the electrode material. Beside being CMOS compatible, because no high temperature or contaminants substances are needed, is also suitable for high volume productions.

It is desired to extend the developed techniques for future industrial application; therefore, designing a fast, simple and reliable procedure for the micro-fabrication is very important. Unfortunately, since is not being used as a deposition technique before, needs to be improved and optimized in order to reach the same reliability of other already optimized techniques.

In the following sections, the microfabrication steps will be described in detail, focusing on problems encountered in the process. Possible improvement will be discussed in *Future work* section on Chapter 6.

All the used tools including evaporator machine, laser writer and test equipment were all available in Chalmers' Myfab cleanroom.

4.1 Photolitoghraphy

For the microfabrication of on-chip supercapacitors, 2" Silicon (Si) with 400nm SiO_2 wafers are used. These wafers with the oxide thermally growth,

are directly provided by the Myfab's cleanroom staff.

Bi-layer lift-off method has been adopted. Bi-layer method is commonly used to assist the lift-off and reduce the defects. Is based on the deposition of two photoresists in order to obtain a gap between the later on evaporated metal and the resist, as shown in figure 4.1.
S1813 photoresist layer functions as an imaging layer and is deposited on the lift-off resist (LOR) which is characterized by an undercut profile when is developed, to facilitate lift-off.

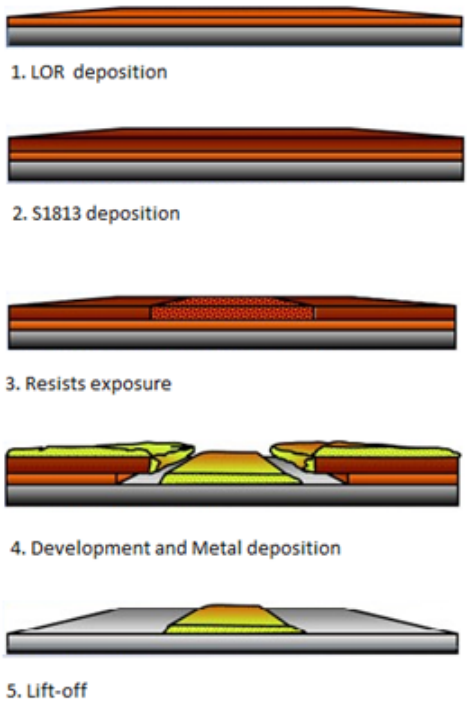

Figure 4.1: Bi-layer lift-off process [6]

The thickness of the two resists can be easily adjusted by changing the spinning speed of the spin-coater equipment. The datasheet provided by the company shows the relation between the spinning speed and thickness. The important thing that must be taken into account is that the thickness of the resist must be at least five times one of the metals which will be deposited, otherwise the lift-off will be difficult or in some cases impossible.

The spin-coating is performed using Suss LabSpin6 spinner, located in the cleanroom.

The spin coating process consists of:

- HMDS(hexamethyldisilazane) treatment: is a common primer spun before spin coating that serves as an adhesion promoter for photoresists.
- Dispense the LOR for first, squeeze with a pipette an amount of resist that cover approximately the 80% of the wafer.
- Start the spinner, previously set at 4000 rpm speed, 2000 rpm/s as acceleration, for 60 seconds. According to the datasheet, with these parameters, a 300nm thick resist is achieved.
- Soft Bake: After coating photoresist, the wafer was put on a hot plate to evaporate the solvent; The wafer is baked at 180°C for 5 min.
- Once the wafer is cool down, S1813 is dispense with the same procedure as LOR. Also, the settings for the spinner are the same, but the thickness obtained is 1.5μm.
- The wafer is then soft baked at 120°C for 80s.

Exposure and Development

After the S1813 baking, the wafer is ready for the exposure. An important property of the resist is the polarity, which can be positive or negative. Positive resists are materials composed of long polymer chains that if exposed to radiation may be broken. The result is that the exposed part will be weakened by radiation and then removed after development.

Negative resists are instead composed of weak and short polymer chains that can be cross-linked by exposure to the radiation source. The result is a decreasing of solubility, thus after development exposed parts will remain while unexposed ones will be removed. Both LOR and S1813 are positive resists.

Normally UV light is used as source for exposure but needs the physical fabrication of masks that are expensive. For this project, in order to have more flexibility in case the design needs modifications, laser writer Heidelberg Instruments DWL 2000 has been used. This machine allows direct laser writing of photo-resist on substrates, using a single source laser with multiple writing modes. No physical masks are needed but just upload the L-edit mask file on the software.

Alignment between mask and wafer is important for good results. With a writing speed of 100mm^2/min this process takes almost 20 min, that is much more than a normal UV exposure where the whole wafer is irradiated at the same time.

After exposure, a post-exposure bake (PEB) has been performed on a hot plate to further increase the adhesion and remove solvent's residue. Moreover, this step reduces the effect of standing waves by means of redistribution of photo-active compounds of the resist. Standing waves are unwanted effects due to the reflection of the incident radiation on the substrate underneath the resist that may cause overexposure, in case the interference between incoming radiation and the reflected one is constructive or underexposure of the resist if the interference is destructive.
The wafer is post-baked at 120°C for 1min.
Once the wafer is completely cooled down to room temperature, can be immersed into MF 319 for developing. The develop process takes 90s while agitation is applied, then the wafer is transferred into water for 5 min to get rid of the developer.

After developing, the sample is better to be checked under the microscope to make sure the resit is completely removed from the area is not wanted.
In the following figure 4.2 is displayed a well done development process:
If resist is still on these areas, the sample should be developed again.

Due to the non-uniformity of the resist, areas close to the edge of the wafer may suffer from incomplete development as shown in figure 4.3. This phenomenon is called edge beads and is related to surface tension that makes difficult for the solution that is flowing radially outward to leave the wafer. The result is a thicker resit in the outer rim.

Figure 4.2: Detail of a micro-supercapacitors after development

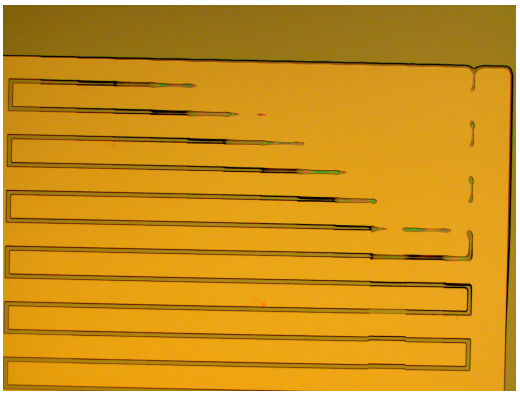

Figure 4.3: Incomplete development due to the presence of edge beads

4.2 Evaporation of current collectors and Lift-off

After development, the wafer is placed into the vacuum chamber of the evaporator machine to evaporate the metal's current collectors. For this project, the evaporator machine used is Lesker PVD 225 (Figure 4.4).

Physical vapor deposition (PVD) working principle, is based on the condensation of a vapor onto a cool substrate. Two techniques are mainly used: PVD thermal evaporation and Sputtering. The machine used in this project is a thermal evaporator, where the source materials are hosted in a crucible and the evaporation is induced by heating the material exploiting the col-

Figure 4.4: Lesker PVD 225 used for metal evaporation

lision of accelerated electrons obtained by heating a filament (Thermionic emission). By using magnetic fields, electrons are directed toward the crucible.

In order to increase the mean free path of material's particles, ensuring the quality of the metal film, the vacuum chamber was pumped down to 1×10^{-6} bar before the evaporation started.

The first step is to evaporate a 20nm thick Titanium (Ti) adhesion layer. The thickness of the evaporated material is well controlled by a quartz oscillator whose frequency depends on the mass. Increasing the thickness of the deposited material, the mass on the oscillator increases and the frequency changes:

$$\Delta m \rightarrow \Delta f \tag{4.1}$$

Ti has good adhesion to silicon and silicon dioxide, as well as metals, therefore Ti could improve the adhesion between Palladium or Gold layer and SiO_2 layer.

After Titanium layer deposition, the metal current collector is evaporated using recipes already saved in the machine. The switch of the crucibles is controlled by the software installed in the machine. Palladium and Gold are used as current collector metals. For both materials, 100nm thick layer is evaporated.

The wafer is then hard baked for 1min at 120°C, reinforcing the resist

film removing all remaining solvent and improving adhesion. Once the wafer is completely cooled down to room temperature, the lift-off process can start.

The wafer is put in an MR 400 bath for the lift-off of the resist. This tool also allows selecting the power of ultrasonic agitation in order to facilitate the process. For this project, 100% is used.

After 55min the wafer is moved to the Isopropyl Alcohol (IPA) bath for 5 min and then rinse into water.

Finally, the wafer is dried into the appropriate dryer. The consequences of a bad development of resit close to the edges of the wafer will be reflected also in the lift-off step. In figures 4.5 are displayed defects occurred during Gold lift-off, while in figures 4.6 defects during Palladium lift-off.

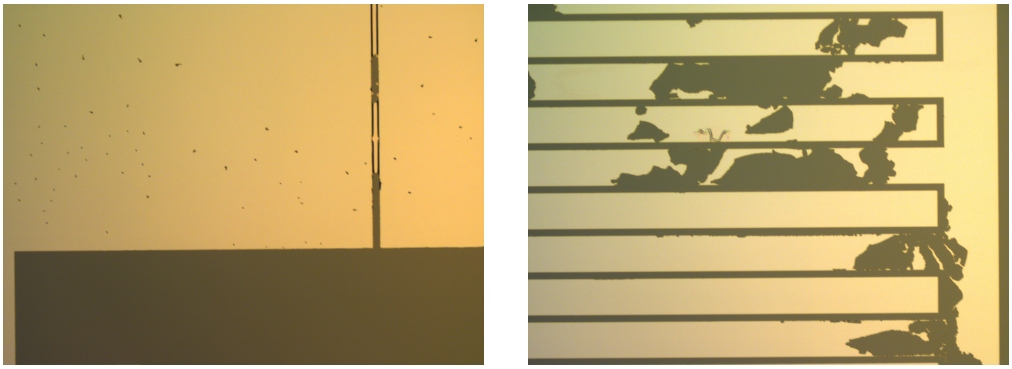

Figure 4.5: Defects occurred during Gold lift-off

4.2.1 Palladium as current collector material

Investigation into MSCs has been traditionally performed using electrodes deposited over Gold (Au) current collectors for their electrical characteristics and chemical stability [55]. However, usage of Au should be avoided in semiconductor technology as it diffuses into the underlying layers even at moderate temperatures. Diffusion of Au causes a creation of a deep-level trap and hole recombination centers leading to a short-circuit [56]. Moreover, it is susceptible to electromigration [57] and is well known to critically

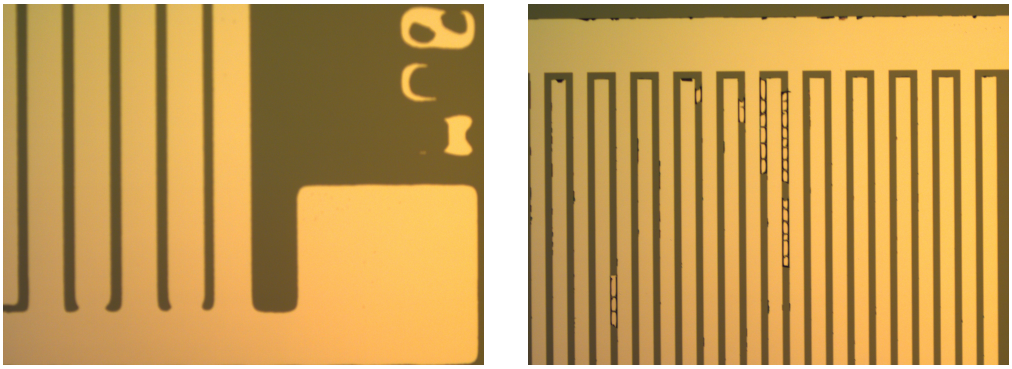

Figure 4.6: Defects occurred during Palladium lift-off

contaminate subsequent process steps.

Palladium can offer lower diffusion properties than Au and can improve the longevity of the devices [58]. Therefore, CMOS compatible Pd metal electrode is a step towards the integration of MSCs in semiconductor microsystems.

4.3 Carbon material spin-coating

Before proceeding with carbon material spin-coating, the wafer's surface should be functionalized to make it hydrophilic for spin-coating. This step is performed in the PlasmaTherm Reactive Ion Etcher (RIE) using oxygen bombardment at a power of 250W for 1min.

Spin-coating of carbon materials has been performed using the station shown in figure 4.7, equipped with a Laurell WS-400-6NPP-LITE/IND spinner and two BLE hotplates.

Two are the materials which have been spin-coated in this work: Graphene Oxide (GO) and Carbon nanotubes (CNTs). For each material, a proper solution was prepared.

Commercial graphene oxide solution with 6.2 g/L concentration, was diluted with distillates water obtaining a concentration of 3 mg/mL which is less viscous than the commercial one and thus more suitable for spin-coating.

Figure 4.7: Laurell WS-400-6NPP-LITE/IND spinner and two BLE hotplates

For Graphene Oxide, five coatings are enough to obtain a uniform wafer's coverage. Each layer has been spun at a speed of 1000 rpm with an acceleration of 3000 rpm/s for 60s and then baked at 100°C for 1 min. Once the five coatings have been performed, the wafer is post-baked for 2 min at 100°C.

CNTs have been spin-coated five times but three times at 500 rpm, 3000 rpm/s for 60s and two times at 1000 rpm, 3000 rpm/s for 60s. Each coating was followed by a bake step of 1 min at 100°C post-bake at 100°C for 2min, exactly has been done for GO.

Variation of the number of coatings can be done to increase or reduced the thickness of electrode material. Moreover, an higher number of layers can increase the uniformity of the coated material.

In order to completely remove the solvent and any residual moisture which can affects the performances, the wafer is baked overnight in over at 100°C.

4.4 Growth process of VOGs

Vertically-oriented Graphene was grown on the prepared substrates in a cold-wall low-pressure PECVD reactor (Black Magic, Aixtron). The substrate was heated to 775°C with the ramp rate of 300°C/min and annealed for 1 min with the mixing of 20 sccm H_2 gas and 1000 sccm Ar gas flowed in since the process started.

The plasma was then turned on with a DC bias with the power of 75 W. The plasma voltage is 800 V with the current limit of 0.5 A. The actual growth was initiated by introducing Acetylene gas C_2H_2, and maintained for 10 min. After the growth, the system was evacuated to be less 0.2 mbar and cooled down to room temperature.

Growth time and C_2H_2 flow rate used in this process can be changed to control the size of VOG.

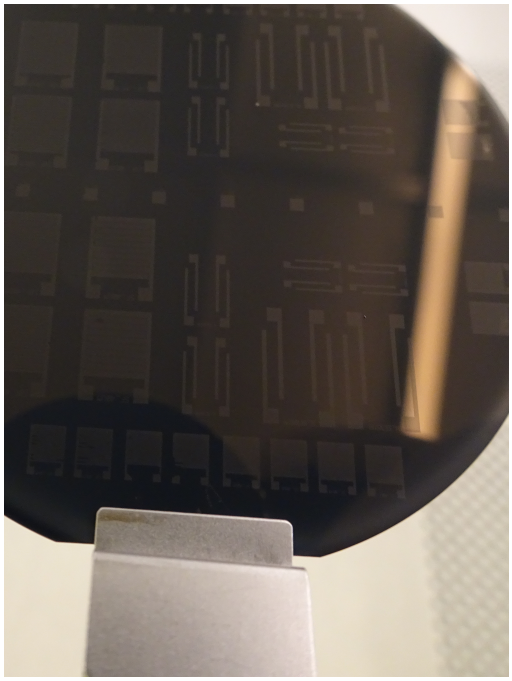

Figure 4.8: VG growth on wafer pattern with the second mask

4.5 Aluminum Hard-masking

When resist are not tolerant enough for the harsh etch conditions, like chlorine plasma etching, hard masking is needed. Aluminum and silicon dioxide are two examples of materials typically used as hard masks in a reactive ion etching (RIE) process. [59]

Two layers of PMMA 950 A4 were spin-coated at 3000 rpm, 2000 rpm/s for 60s as protective layers and to planarize the surface. After this step is important to bake in the oven overnight to remove bubbles and solvent's residual.

A 50nm thick layer of Aluminum is then evaporated on the wafer as hard mask material, using the Lesker PVD 225 machine. This layer needs to be patterned with the mask for the electrode material. To remove Al from areas where is not wanted, S1813 resist is spun on the wafer, exposed to the laser writer and then developed as in the previous photolithography process but with a different mask pattern.

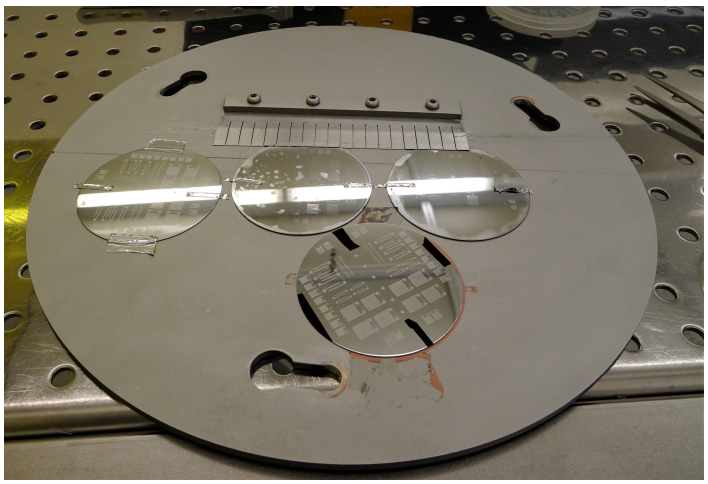

Figure 4.9: Four wafers after Aluminum evaporation

This step is followed by an overnight bake at 100°C in vacuum oven, thus to remove moisture and bubble.

Using the *Plasmalab 100 ICP180*, the aluminum not covered by the resist

is dry etched and the resist is then removed with oxygen bombardment at a power of 100W and 100 mTorr pressure.

4.6 Carbon Material Etching

Once the resist is removed, Aluminum is masking only the areas where the carbon material is wanted. The gap between the fingers and the rest of the wafer expose the carbon material which needs to be etched. For this purpose, Plasma-Therm Reactive Ion Etcher (RIE) has been used. Reactive ion etching is a dry etch technique that combines both chemical and physical etching. The first is due to the reaction of the used gas with the film, while the second is based on ions that hurt and damages the film.

Dry etch technique is preferred to wet etch because doesn't need acid and solvents that can damage or reacts with the fabricated structures. Moreover, directional etching may be achieved with less undercut with respect to wet etching.

Oxygen plasma allows etching the carbon material without compromise the aluminum mask. Oxygen is bombarded at a power of 100W and a pressure of 100 mTorr for a total of 1 hour. If the etching of carbon material is not complete, another hour of stripping should be enough to get rid of all carbon material residual.

4.7 Aluminum etching

The final step is the etching of the aluminum mask. By means of *Plasmalab 100 ICP180* used also for Aluminum patterning, the mask is completely removed.

However, one of the main disadvantages of using dry etching is the possible re-deposition of non-volatile chemical compounds. In the figure 4.10, are displayed example of Al re-deposition faced during the fabrication. In figure 4.10a is displayed short circuit caused by re-deposition, this makes the device unusable. Even if the re-deposition is not critical can affects the accessibility of pores of the electrode material to the electrolyte, causing degradation of

performances (figure 4.10).

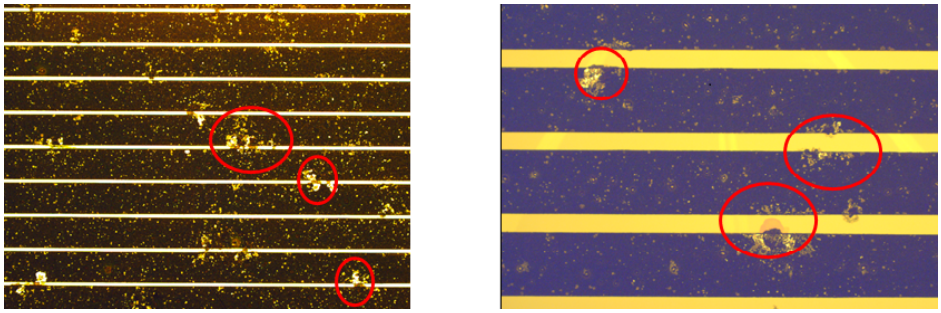

Figure 4.10: (a)Electrodes short circuit due to Al re-deposition (b)Non critical Al re-deposition

4.8 rGO activation and electrolyte deposition

Graphene Oxide electrodes should be activated in order to ensure electronic conjugation, as discussed in Chapter 3. The reduction of GO is performed thermally, heating the entire wafer at 500°C for 20 min. The temperature is reached with a ramp of 10°C/min starting from 150°C. Ramp duration takes 35 minutes.

The wafer is ready for the electrochemical characterization. In figure 4.11 are reported how the fabricated wafers look at the end of the fabrication process.

H_2SO_3 liquid electrolyte has been used in this project. As discussed in Chapter 5, liquid electrolytes are easy to handle and have very high ionic conductivity but suffer from very limited stable voltage window. Since the aim of this work is to develop a CMOS compatible fabrication process, the influence of the electrode material on performances is more important than electrolyte characteristic.

Is worth to mention that liquid electrolyte should be avoided for complete CMOS compatible micro-supercapacitors. Solid state electrolytes have to be preferred because don't spread on the whole wafer with the risk of contaminating other devices.

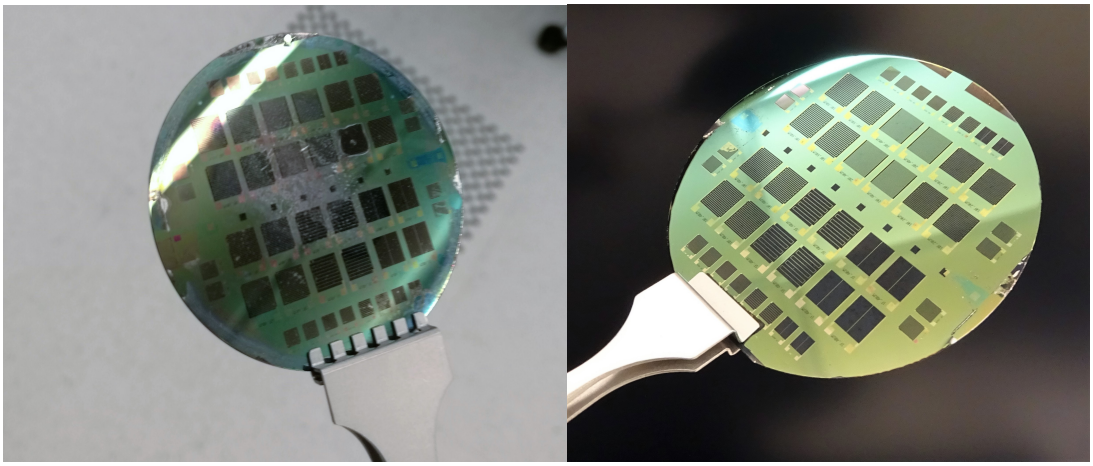

Figure 4.11: Left: rGO wafer; Right: VOG wafer

Chapter 5

Electrochemical Characterization

The electrochemical tests, Cyclic Voltammetry (CV) and Galvanostatic Charge and Discharge (GCD), have been carried out using Gamry Reference 3000 Potentiostat and Galvanostat/ZRA.
Since the pads of devices are very small, a probe station needs to be used for the measurement. The Gamry Reference 3000 was connected to the probe station for measuring the micro-supercapacitors parameters.

The electrolyte was dispensed the day before measurements on the MSC devices in order to let it penetrate into the electrode's material and balance with the laboratory environment.

Follow a presentation and discussion of obtained results.

5.1 Cyclic Voltammetry Measurements

The CV test was carried out at 2 Vs^{-1} for the VOG wafers with Au and Pd contact and at 20Vs^{-1} and 200 Vs^{-1} for rGO wafers.

CNT wafers, as displayed in the previous chapter, showed bad coverage of the electrode material and this reflects on bad performances. Most of the devices were unusable due to short circuits between electrode fingers. Due to the impossibility to test the different geometries, the results for these wafers

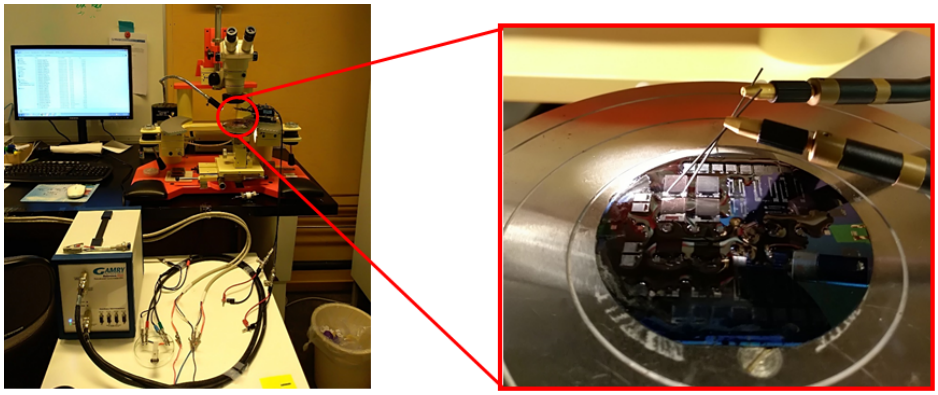

Figure 5.1: Setup used for electrochemical characterization

will not be reported.

5.1.1 VOG Wafer

Figure 5.2 displays the cyclic voltammograms of MSC sample with 10 fingers with 40 μm interspacing on the three fabricated wafers: Au/Ti contact, Pd and Ti-enhanced Pd contacts.

In wafers where only Pd where used, devices showed a resistive behavior due to the short circuit as shown in figure 5.2(b). Is possible to address this problem to Pd diffusion into the insulating SiO_2 layer.

Regarding devices on Ti/Au contacts, and Ti-enhanced (figure 5.2a, c) wafer, a capacitive behavior at a scan rate of 2 V/s is shown. The quasi-rectangular shape of the CV curves for the potential windows range 0-0.8 V indicates the electrochemical double-layer capacitive behavior of the device.

CV curves for Ti-enhanced Pd wafer show a peak at the upper limit of the electrolyte potential window due to the electrolyte degradation. This phenomenon usually happen in water-based electrolytes at voltage around 1 V. However, since the used measurement setup is an open system with interaction between wafer and environment, possible oxygen absorption of the electrolyte can cause the shift of electrolyte degradation at lower potential.

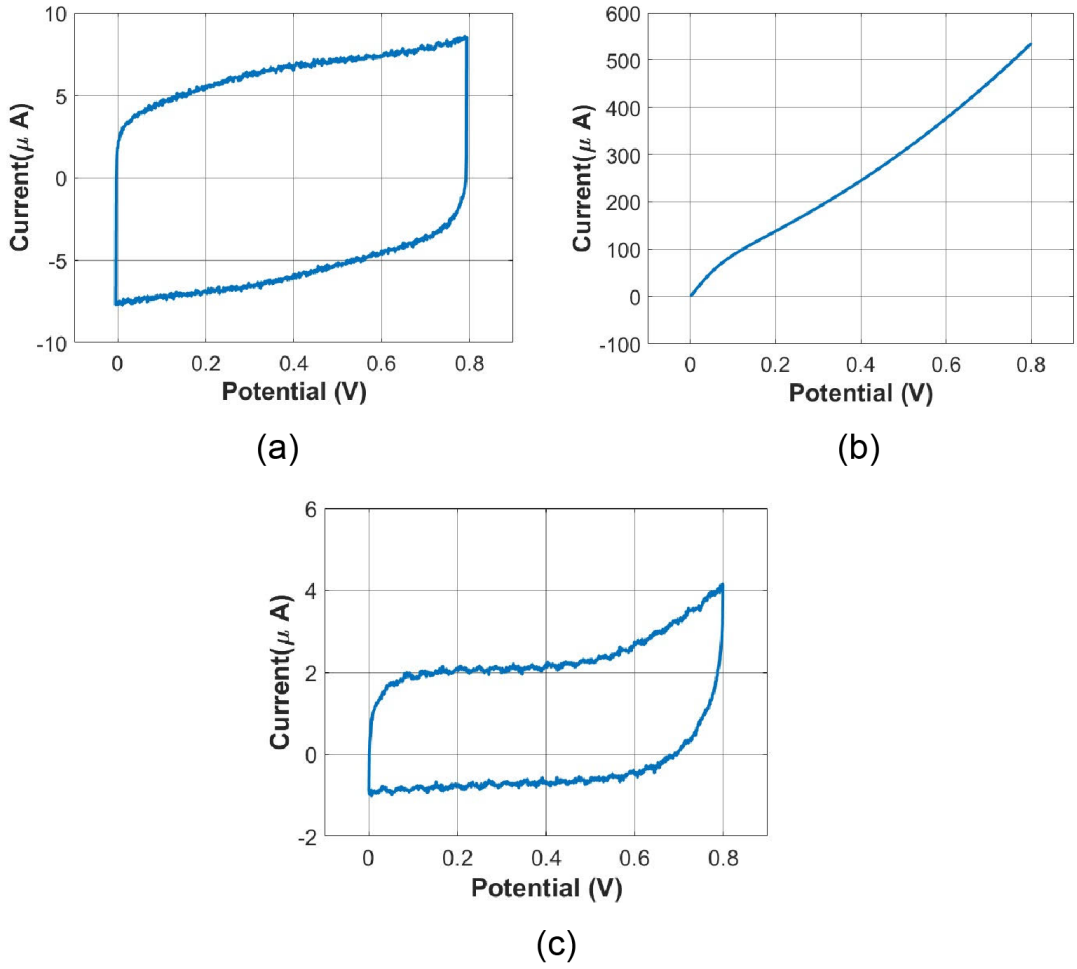

Figure 5.2: Cyclic Voltammograms of: (a) Ti/Au current collectors. (b) Pd sample. (c) Ti-Pd sample

The areal capacitance of the devices has been obtained by evaluating the cyclic voltammograms using the following equation:

$$C_A = \frac{\frac{1}{2}\int IdV}{sA\Delta V} \tag{5.1}$$

where $\int IdV$ is the area of the CV curve, s is the scan rate (V/s), A is the area of the device (cm^2) and ΔV (V) is the potential window.

MSCs with Ti/Au-current collectors demonstrated a capacitance of 5.5 $\mu F/cm^2$ while the Ti-enhanced sample showed 1.3 $\mu F/cm^2$. Ti/Au-contact

devices demonstrate the highest capacitance.

The significant difference in capacitance requires further investigation, e.g. reaction of the electrolyte with Pd, or difference in electrode properties on different wafer samples.

5.1.2 rGO Wafer

Due to fabrication problems with Ti/Pd and Ti/Au VOG wafers were not possible to test the different device configurations.

On rGO wafers only 10F20 and 10F60 configurations were not testable, limiting the maximum resolution of fingers interspace at 40 μm.

Furthermore, this result does not allow to investigate how different fingers' gap affect performances. Figure 5.3 displays the cyclic voltammograms of devices with a different number of fingers.

The shape of the CV is not affected by the device configurations. However, is clear that the CV curve areas are different. This result is expected because, as shown in table 3.2, each configuration has a different electrode area that is related to the capacitance value. Using equation 5.1 the areal capacitance of the devices has been obtained.

	C_{areal} ($mFcm^{-2}$) 20 mVs^{-1}	C_{areal} ($mFcm^{-2}$) 200 mVs^{-1}
1F40um	0.47	0.44
5F20um	0.35	0.33
10F40um	0.30	0.28
20F40um	0.21	0.2

Table 5.1: Areal capacitance for different configurations

The device with one finger shows the highest capacitance, this result is related to the highest electrode area of the device. Exposing more electrode area with respect to other devices is clear that the capacitance will be higher.

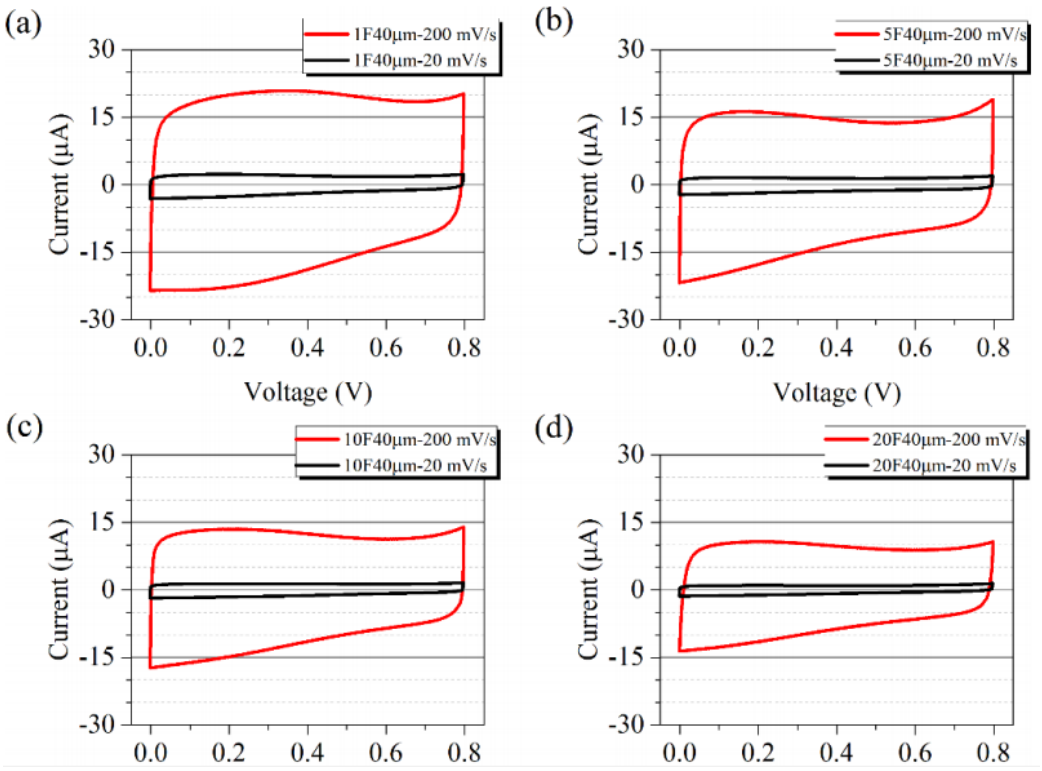

Figure 5.3: Cyclic Voltammograms of different device geometries: a) 1F40um, b) 5F40um, c) 10F40um, d) 20F40um

Areal capacitance results are comparable with typical values in literature in scan rate range 1-100 mVs^{-1}: 0.4-2 $mFcm^{-2}$[60].

5.2 Galvanostatic Charge and Discharge

Galvanostatic Charge and Discharge measurements were conducted with a potential range from 0 to 0.8 V. A current density of $100\frac{\mu A}{cm^2}$ was selected in order to evaluate the power performance of the devices simulating a possible real scenario e.g when being charged by a micro energy harvester in a self-power system.

Figure 2.11 shows GCD data recorded on the different device configurations. The cycle is shown with voltage plotted versus time, with each configuration graphed in a different color. MSCs exhibit linear charge/discharge curves representing capacitive energy storage.

Figure 5.5 shows the voltage drop, called IR drop, due to the resistive behavior (ESR) of the devices. The difference in the charge-discharge time is a result of different device capacitance ($C_A = \frac{It}{\Delta V}$, where I is the current, t is the discharge time and ΔV is the voltage window excluding IR drop).

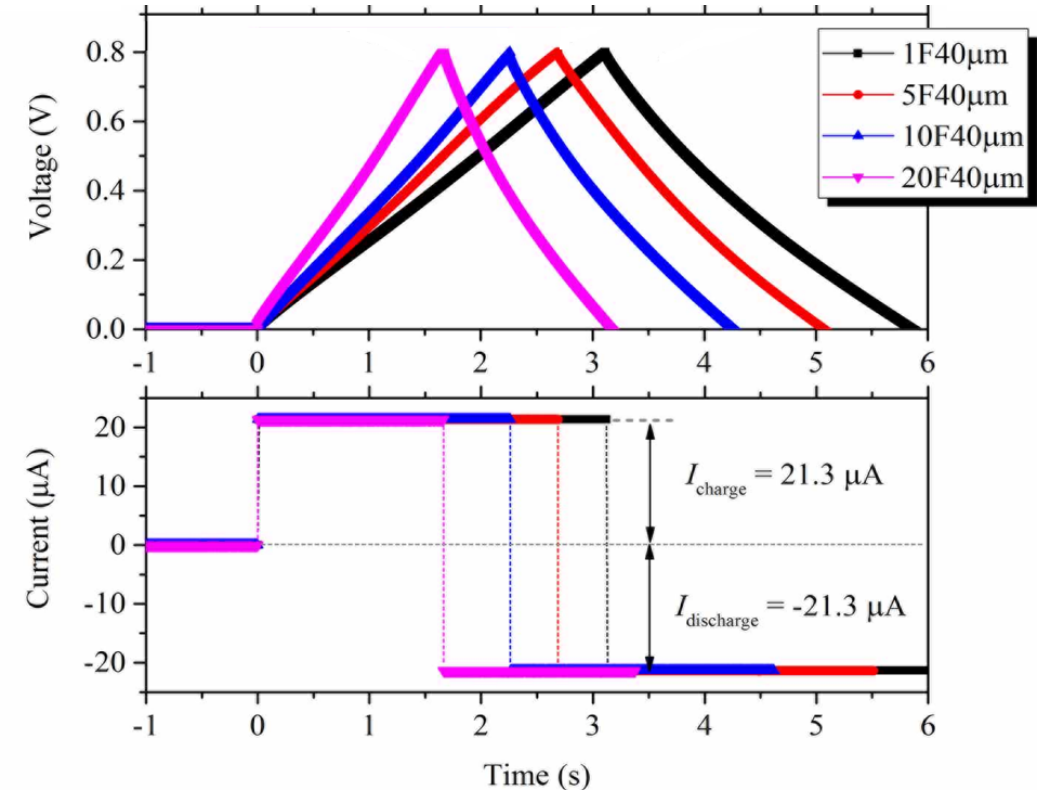

Figure 5.4: Galvanostatic charge/discharge measurements at current density of 100 $\mu A/cm^2$

Through IR drop the ESR can be calculated by the equation $ESR = \frac{V_{IR}}{I_{charge} - I_{discharge}}$. Energy density is calculated by $E_A = \frac{1}{2} C_A \Delta V^2$ and average power density $P_A = \frac{E_A}{t}$. The obtained performance metrics from GCD measurements are listen in table 5.2.

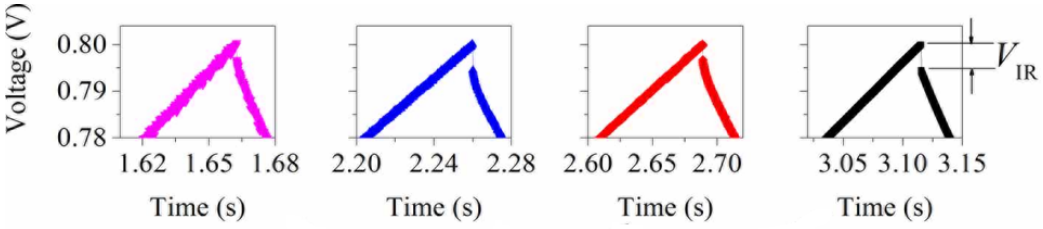

Figure 5.5: IR drops in galvanostatic charge/discharge measurements

Device	V_{IR} (V)	Voltage (V)	ESR (ohm)	Discharge time (s)	Areal capacitance ($\frac{mF}{cm^2}$)	Areal energy density ($\frac{\mu Wh}{cm^2}$)	Average power density ($\frac{\mu Wh}{cm^2}$)
1F40um	0.006	0.794	141	2.74	0.345	0.0302	39.7
5F20um	0.003	0.797	70	2.38	0.299	0.0264	39.9
10F40um	0.005	0.795	117	2.00	0.252	0.0221	39.8
20F40um	0.003	0.797	70	1.53	0.192	0.0169	39.9

Table 5.2: Areal capacitance for different configurations

Similar to the CV results, there is not a clear trend showing the power-related metrics (e.g IR drop, ESR) are highly dependent on the number of fingers. Especially for the average power density, only a $0.2\,W/cm^2$ difference exists between the highest and lowest values. The benefit of increasing areal capacitance and energy by reducing finger numbers is again evident.

It is noteworthy that this observation might be applied to only a certain category of electrode materials, as well as fabrication methods. A theoretical modeling considering both current collector and electrode/electrolyte material properties should be conducted to establish the correlation between optimized device configurations and the type of electrode/electrolyte material.

The device capacitance as function of the active surface area that is used for depositing electrode materials is plotted in figure 5.6.

The measured capacitance is less than expected from the active surface area. The more fingers designed the larger loss of capacitance results.

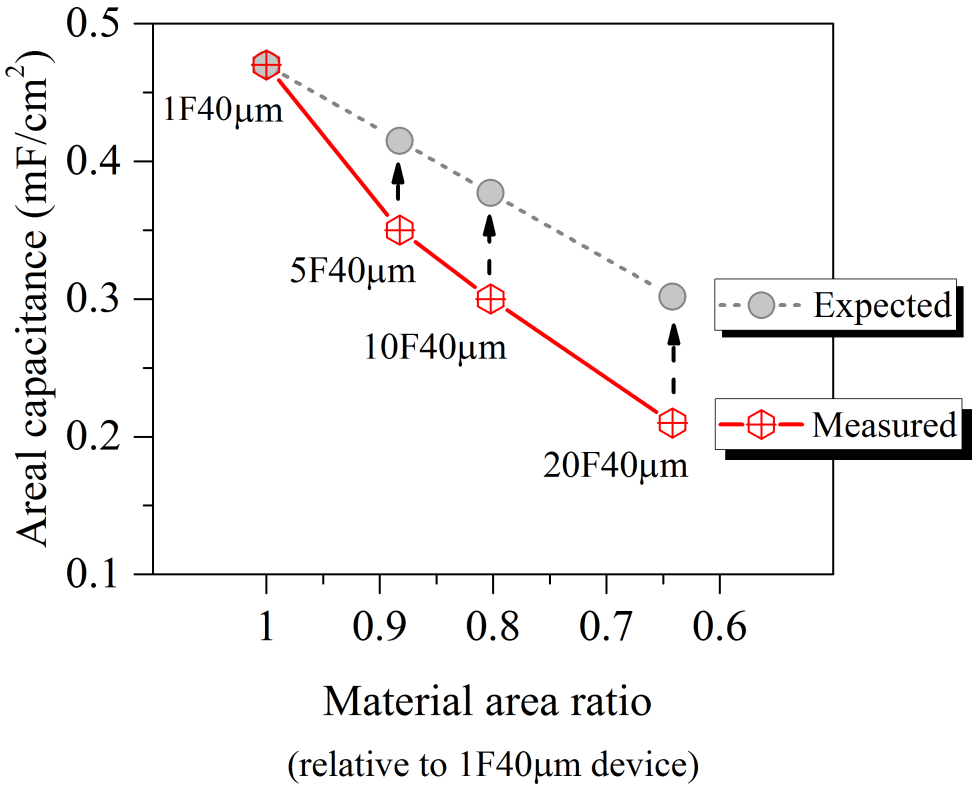

Figure 5.6: Areal capacitance of devices as function of electrode material area ratio

This may be partly because more finger design leads to more exposure area to plasma etching of rGO materials. The plasma etching is isotropic and therefore materials on the edge of the finger can be easily etched.

Chapter 6

Conclusion

Two ways towards a potential future integration in CMOS based microsystems for on-chip energy storage solutions have been investigated.

The first involves Palladium as material for metal contacts, instead of Gold. The fabricated micro-supercapacitors demonstrate capacitance of $1.3\mu F/cm^2$ with an energy density of $0.42\mu J/cm^2$ at a scan rate of 2000 mV/s. The fabrication method includes Titanium as a diffusion barrier to overcome the issue of devices' short circuit due to Palladium diffusion in SiO_2. Performances of Ti/Pd devices are comparable with devices which follow the same fabrication process but used Gold as metal contacts material. However, for both MSCs based on Vertically Oriented Graphene performances are worse than other devices found in literature. The developed fabrication method may drastically affect the morphology of graphene planes. PMMA coating and Aluminum deposition for hard masking may press the graphene planes causing a loss of accessibility and consequently a loss of capacitance.

The second is the development of CMOS compatible fabrication method compatible based on methods and techniques which are even suitable for large-scale production. Two electrode material have been used for this method: Carbon Nanotubes (CNTs) and Reduced Graphene Oxide (rGO). Devices based on CNTs as electrode material were unusable because of a bad coverage of the CNTs solution and issues faced during the fabrication, as explained in Chapter 4. Recipe for spin-coating of CNTs needs to be optimized or is possible to directly grow this material on metal contacts as done for VOG. However, rGO-based devices showed good performances comparable with

other device found in literature, as displayed in Chapter 5.

Influence of different number of fingers has been investigated. MSCs with 1,5,10 and 20 pairs of interdigital electrodes have been fabricated. The 1-pair of fingers device exhibits the highest capacitance of 0.47 mF/cm^2 which is more than two times of that with 20-pair device, and average power density at 100 μA/cm^2 reached 39,7 μW/cm^2, the same level as all other MSCs of multiple pair of fingers.
The evaluation of these devices suggests a huge benefit of designing only one pair of electrode fingers in maximizing the energy density within a given footprint area, while at nearly no sacrifice in power performance. This result may be only specific to certain category of materials and fabrication methods, but are provocative in the regard of MSC design for miniaturized system applications where only limited footprint is allowed. A comprehensive model considering contribution from all cell components should be established to finally give an answer to the question whether to give MSCs more fingers or nor, and how many fingers will lead to optimized performances for specific type of material.

6.1 Future work

As reported in Chapter 4, the development of an innovative fabrication method led to faced different issues. First of all, the presence of edge beads during spin-coating of the resist can drastically affect the fabrication, making some devices unusable, as shown in section 4.1. A possible solution is to fabricate devices using larger wafers, where the influence of edge beads are less and the area usable for fabrication is larger. Another solution is the use of solvents for edge beads removing, being careful to not affect further fabrication steps.

The second issue is the Aluminum re-deposition after the plasma etching. Possible solutions are the optimization of the recipe to use in the machine or change material for hard masking. Anyway, a more in-depth study of the phenomenon needs to be done in order to find the optimized solution to the problem.

Currently the maximum resolution, in terms of space between electrodes, for this fabrication methods is 40 μm, since all the fabricated devices with 20μm were unusable. Being able to increase the resolution of the process means to increase the areal capacitance within a given footprint area and may lead to increase in power performances.

Adhesion of spin-coated material needs to be optimized in order to use other material like Activated Carbon (AC) and carbon nanotubes (CNTs) or increase the reliability of the already used rGO. A solution to this problem was already studied and is summarized in figure 6.1.

A Lester PVD 225 has been used to deposit the Iron (Fe) on silicon dioxide, starting 4nm of Fe. The substrate is then heated at high temperature, around 700°C, for 6min to anneal the Fe into nanoparticles, creating a rougher surface (figure 6.1c).

Nanoparticles are than coated with 20nm Ti and 100nm Au as the current collector for supercapacitors.

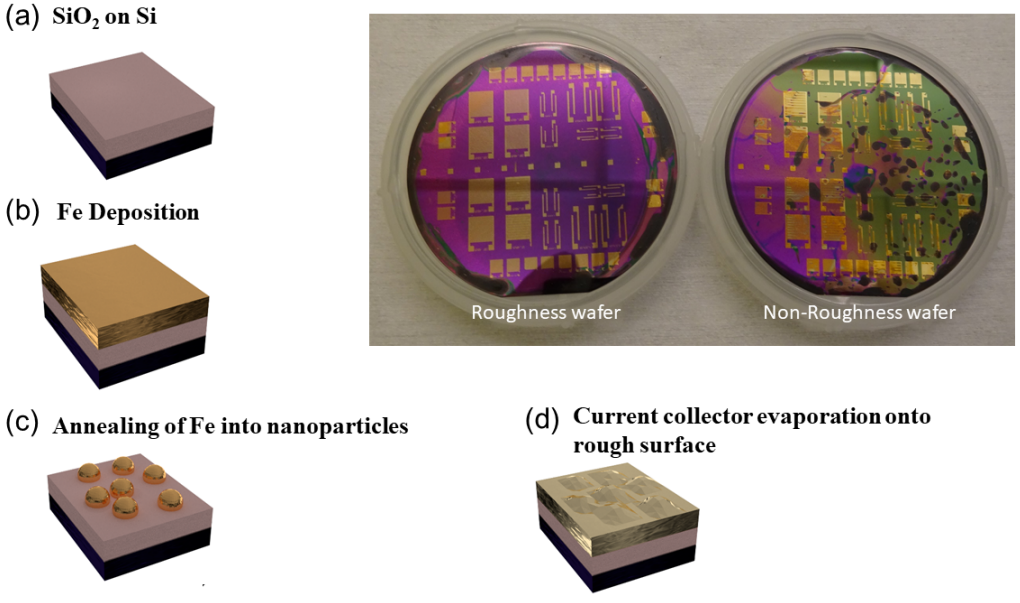

Figure 6.1: Roughness Treatment

In figure 6.1 are displayed two wafers where the first followed the roughness treatment while the second followed the conventional fabrication flow. Is clear that the treatment improves the adhesion of the carbon material. However, a more in-depth study of the influence of Fe nanoparticles needs to be carried out, since short circuits due to the Fe conductivity can occur.
All points discussed in this section might be further subjects of future study.

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