Master Thesis

Design and implementation of an Automatic Test Equipment Adapter application for a Bed of Nails system

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1. Introduction and motivation

Personal motivation

In the engineering world and more specifically, for mechatronic engineers, multidisciplinary work is essential. For this reason, ATE industry results to fit with the mechatronic profile, where automatic systems meet electronic testing.

In SPEA, I have had the opportunity to experience with electronic and mechanical disciplines, and at the same time, I was introduced to the industry world. Furthermore, the necessity of managing the work flow of the project, coordinating my thesis activity with the project needs, helped me to enhance my self-management and communication abilities.

Context of electronic testing industry

Today, the electronic devices are present in most of the industries, whether on the manufactured products or the production lines. Some examples would be: automotive industry, mobile industry, Defense... that shown a growing trend of the complexity of electronics devices and its production rate. Accordingly, the reliability of the electronic devices is compromised by the high production numbers and high technological complexity, which make on field failure very probable and difficult to detect. These factors, in conjunction with the higher responsibilities attributed to the electronic devices makes of testing a necessity.

In application fields as Defense, reliability is critical. No matter the manufacturing process quality, testing must be performed to ensure the well-functioning of the on-field electronic devices. On the contrary, automotive industry production must be cost effective, to survive in a high competitiveness market; and reliable, to be compliant with the day by day stricter legal regulations. The various needs of the different industries come along with the importance of efficiently testing the growing variety of electronics devices.

The Automatic test equipment is becoming a key technology for the Electronic Industry, both to test the single components as to test the end of line electronic boards. The necessity of using ATE instead of the conventional test methods arises mainly for the electronic industry constant growth, which demands high production rates, and the high complexity of the final product. This last consequence implies that late error detection is very costly, which make preventive measures very attractive.
Thesis scope

During this thesis, I have participated in the design and debug process of an ATE adapter application for a Bed of Nail Systems in a real industrial environment.

The thesis has two different kinds of objectives:

1. Academic aims
   a. Work in a multidisciplinary environment
   b. Understanding the necessities and possibilities of the ATE industry
   c. Learn the technological background of the ATE industry
   d. Acquire communication skills

2. Content aims:
   a. Design with criteria a complete ATE adapter for a BON system
   b. Follow and understand the manufacturing process of the mentioned adapter
   c. Debug the adapter and make it operative
   d. Analyze the stability of the tests realized by the adapter

The objectives 1-a, 1-b and 1-c have been reached by the daily work at SPEA installations. Furthermore, the objective 1-d, is expected to be covered by the thesis documentation writing and its presentation.

On the other hand, the content objectives from 2-a to 2-c are covered (as is possible to confirm reading the corresponding chapters). Leaving 2-d pending from a more exhaustive analysis with a higher amount of data (more analyzed boards). This work will be done in the future but is not been possible to add it to this thesis document on time.

Document structure

The document is divided into two main parts:

- **Technological Background**: In this chapter, the theoretical basis of the used ATE equipment, testing process and testing models are explained. The aim of this chapter is to contextualize the Case of Use chapter in order to clarify its contents.

- **Case of Use**: Is the core chapter. It is a practical example of what has been explained on the previous chapter. An ATE adapter is designed from start to end and to guide it some appendixes has been added:
  o Appendix A: Electrical schematics of the adapter
  o Appendix B: General flow charts of the complete test sequence
  o Appendix C: Some LabVIEW block diagrams of the test sequence implementation

As a conclusion, an analysis of the stability of the adapter together with some reflections can be found at the Results chapter.
2. Technological background

The industry of Automatic Testing develops along with Electronics. At the beginnings of 1960s, when the Electronics industry was just born, the testing of the electronic products was carried out internally by each manufacturer. However, the increasing complexity of the electronics components and its products, made of automatic testing, a feature only for those who could afford it. For this reason, the biggest companies of the sector like Fairchild, Semiconductor, Signetics and Texas Instruments started selling their test equipment to smaller competitors and their customers.

Within this context of emerging market some specific ATE oriented companies came into scene, like Teradyne founded on 1960 in USA which was the first of its kind, or SPEA 1976 Italy, the company that has contributed to make this thesis possible.

Nowadays Electronic Industry provides an extensive catalogue of products susceptible of being tested. These products are usually tested more than one time along the production line to allow an early detection of defects. To be considered:

- **Semiconductors stage**: test of individual components like conventional ICs (DIODs, LEDs, Regulators, sensors...) or MEMS\(^1\).
- **Mounted electronic board stage**: PCBs with mounted components
- **End Of Line stage**: ready to go products that need a final check to go into field work or to be assembled into another structure. For example, a Hybrid car DC/DC converter once enclosed in its protective shielding.

This allows early detection of faulty components, thus reducing the overall cost of production (Fig. 3 Failure costs over life span of a product) and improving the client usage experience. Testing is especially important for customers that must rely on the well-functioning of electronics devices

\[\text{Fig. 3 Failure costs over life span of a product}\]

\(^1\) Micro Electro-Mechanical
like those concerning military industry, or to critical commercial systems, like those related to Automotive Industry.

Automatic Test Equipment ATE

To realize the test of electronics boards different solutions are available to adapt to different production targets. The most important technologies up to now are:

- **Bed Of Nails systems**: Based on fixed contacting point from the measurement system to the UUT. Focussed on production. The flexibility of this systems is comparatively low. Change UUT Test Point layout or simply change slightly the production product implies developing and manufacturing a new specific UUT adapter.

- **Flying Probes systems**: Based on mobile probes that contact sequentially the needed test point on the board. Focussed on flexibility, thanks to rapid TPGM/TPS developing. Based on mobile probes, it can access all the board components and can process different products without any mechanical adaptation. FP systems are penalized in production rates respect BON systems.

At the same time, these systems can be aimed to form part of a production line (in line systems) or not (manual systems). In line systems need an input and output conveyors as well as a board handler to classify the boards according to the test results.

  - **In Line Automated systems**

To maximize benefits with high production rates is important to minimize unitary variable cost. This costs impact on the total variable costs that increases with the manufactured quantity. On the contrary, fixed costs (related to the machinery and operators salaries) don’t depend on quantity. For this reason, fixed cost is low compared to variable cost (Fig. 4 Production costs over unit quantity).

![Fig. 4 Production costs over unit quantity](image)
Minimize variable costs is the main purpose of an automated production line, even if it raises the fixed costs that will be amortized once produced a certain number of units.

- Bed Of Nails systems BON

BON systems are equipped with instrumentation, a receiver (performs board contacting movement) and a controlling system that, in case of SPEA systems is composed by a general-purpose PC and various PLC and drivers to control the receiver sensors and actuators.

![Fig. 5: BON SPEA 3030IL System](image)

Additionally, to permit the production of a specific UUT, its needed the so-called adapter. A BON adapter is a “system interface” with the board. For this reason, an adapter varies depending on the board and so it needs to be developed accordingly to UUT. The adapter is in direct contact with UUT and has the aim of contacting the UUT test points with minimal signal interference and board deformations.

**System Instruments**

This section could be abstracted to all standard SPEA ATE systems for electronics boards ² (ease instrument interchangeability), it is also very similar in concept to other ATE systems brands.

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² Except Multicore feature, it is exclusively for BON systems.
Apart from the main power supply, mother board, analog bus and digital bus, the SPEA 3030IL can have one or two racks (depending on the testing needs) where instruments are placed. These instruments can vary depending on application. It has a modular architecture, so designed to be scalable and adaptable.

A 3030IL system has a “Multi-Core” architecture. This allows a high customization (see table below) to match a wide range of test requirements. The tester can have up to 4 test cores/enGINes, each of which is equipped with the instruments needed to test the boards (fig 2). The setup could be changed at any moment, by modifying and/or expanding to answer an eventual change on the test needs. Additionally, there is a feature so called “Bay Link” that allow to virtually convert a quad-core system into dual-core or into single-core. Note that, in the images below, engine corresponds to core as an equivalent notation.

<table>
<thead>
<tr>
<th>Active Bay Link</th>
<th>Rack Number</th>
<th>Single Core (real/virtually)</th>
<th>Dual Core (real/virtually)</th>
<th>Quad Core</th>
</tr>
</thead>
</table>
| NO              | 1           | Engine 1
|                 |             | Test Area                   | Engine 1
|                 |             |                             | Test Area |
|                 | 2           | Engine 1
|                 |             | Test Area                   | Engine 1
|                 |             |                             | Test Area |
| YES             | 1           | Engine bridge               | Engine 1
|                 |             | Test Area                   | Test Area |

Fig. 6 Instrument Rack (SPEA 3030IL IR500)
Each instrument placed on a rack is directly connected to the system and to the Fixture. In some cases, external instruments or loads are connected through a rack. The board that allows do so (YAPROL) is mainly use for non SPEA bulky instruments like counters, picometers, AC generators or communication ports for fixture internal instrumentation.

There is a minimal configuration that would allow the system to be initialized. The minimal configuration is:

- Mother board (ABUS, MBUS): comprises the sharing buses. This is, Analog Bus and Mod Bus (internal bus). It manages the instrument interfacing and communication.
- Power supply board (YAPSU): power supply unit. Provides power to the rack instruments but not to the PC and automation actuators.
- Matrix Relays board (YASCA #1): it allows to connect any TP/TPs to any of the ABUS line/s.
- CPU board (YACPU): each bay (equivalent in number to core) must have one YACPU. This will allow the system to parallelize the test sequence to reduce the test time.
- Measurement Unit Board (YAICT): It has different instruments depending on each application needs. The basic instruments are:
  - Drivers: high precision low voltage general purpose generators (+-10V +-100mA). It’s HOT and COLD (System Earth) terminals can be connected to any ABUS/MBUS line/s, or can be wired directly into the fixture.
  - Digital Voltmeter (DVM): It is equipped with some customizable low pass filters among other typical features. It’s HOT and COLD terminals can be connected to any ABUS/MBUS line/s, or can be wired directly into the fixture.
  - Guard: It is a module that inhibits some parts of the board circuit if needed during a component measurement. Simply speaking, it uses a voltage follower or a direct connection to change the circuit behavior and thus isolating the component of interest from the rest of the board.

Some other boards could be added in the rack depending on the application needs. The most frequently used optional board, YAPSU, is equipped with medium voltage power supplies so called boosters, which complement the limitations of the drivers. The boosters can manage up to +100V+-1A or +40V +3A way more than a driver.

**External instruments**

On demand or ad hoc instrumentation for a UUT. This instrumentation can be potentially anything given that safety conditions are not compromised and the system in use is compatible.
Receiver and conveyors

This module is in charge of handling the board. In a In Line system this phase is done automatically, without the human intervention.

The handling sequence consist on (Fig. 8):

1. Move the board into the system
   a. Verify the board presence on the output conveyor
   b. Start movement
   c. Verify the transition, board in not in output conveyor
   d. Verify the board is in the test area
2. Move down the receiver
   a. Verify the optical barriers are not interrupted and that the system doors are closed
   b. Verify that the board is well positioned, not rotated, and that it is the correct UUT
   c. Start movement
   d. Abort if any prior condition changes
3. Perform the test
4. Move up the receiver
5. Move the board out
   a. Verify output conveyor is free
   b. Start movement.

Fail boards can be separated mechanically with a handler at the output conveyor or/and its serial number can be written in a fail boards data base.

The board positioning within the test area is verified by three sensors (figure below):

- Presence sensor: Verifies that a board has arrived and that its front edge is placed correctly
- Volumetric sensor: Verifies the board length (is the right UUT)
- Anti-rotation sensor: Verifies that the board is in the correct orientation. Note that a board have 8 possible rotations (conveyors with is adjustable)
  o Anti-crash: Verifies that the presser corresponds to the fixture (see adapter chapter below)
The time needed to manage all the process is near 3 seconds and depending on the application can be have different impacts on the overall test time. In the application developed in this thesis, ICT and FCT are realized. Furthermore, within the FCT some test will last more than 30 seconds so the impact of the board handling timing will be low.

Finally, during an installation, debug or board production change, the different adapters (see adapter chapter below for details) are intended to be extracted and inserted into the system receiver. This task is responsibility of the receiver that must ensure that the locking of the adapter is been perform correctly and the interface strips are well connected to the system.

Furthermore, because of the heavy duty autonomous mechanism present in the receiver urges the need of protecting operators and UUT from a failure or a malfunctioning. To realize its duty safely and correctly the receiver is equipped with sensors that allows it to abort the movement in case an anomalous behavior is detected.

A safety system is frequently based on a safety chain method. Generally speaking, if this chain is opened, receiver actuators are automatically disabled. A safety chain is commonly implemented through hardware, so it cannot be bypassed with software. This ensures its integrity even if a software fail occurs. The sensors used in a 3030IL system are:

- Front door sensor
- Back door sensor
- Laser array sensor: prevent

This way is impossible to access to the test area without interrupting the safety chain. This would protect an operator from performing a bad use of system. For example, opening the door while HV present or to prevent an operator from moving the receiver while other operator is realizing maintenance from the back door.
Control

The 3030IL system is controlled at top level by a PC with windows OS. The computer connects through CAN to the power supplies and through GPIB to each bay. Additionally, as explained in System Instruments chapter, each bay has its own core that will manage instruments at low level. This structure (Fig. 5), together with the dedicated instrumentation for each bay, allows a real parallel execution on each bay. In conclusion, The PC is the one that synchronizes the execution on all bays in a system and manages is the actual interface with the operator.

Fig. 9 Controlling structure

The PC controls as well the receiver thought a dedicated controller. The receiver controller employs a modular structure where the most dangerous actuator, pressor mechanism, is controlled directly while the control of the rest of actuators (conveyors, adapter locking mechanism ...) are delegated to other minor controllers.

The base software used to control the system is the so-called LEONARDO. It is the software developed by SPEA and use by SPEA to manage their systems and guide the engineers to design, construct, debug... a new adapter. It generates the TP layout and wiring schematics automatically from a CAD file and a BOM list. It also generates the test sequence for the ICT (some FCT test can
be done here, as LED intensity among other simple test) as indicated by the engineer and predispose the flow of the board handling process. It has as well an OBP development toolkit.

Furthermore, it provides a GUI to control SPEA systems to witch we will refer to as RunPack.

In the use case developed in this thesis, LabVIEW will be used to develop the functional test. It will work in a top layer respect to RunPack. Nevertheless, all the commands used by LabVIEW to manage the non-external system resources and result managing will pass through RunPack, that already has a library to manage all the 3030IL instrumentation and has a SPEA looking GUI.

**LabVIEW**

**External instruments**

**RUNPACK**

**System Instruments**

**Adapter**

The adapter is a device that adapts a system to a specific board. As its been analyzed in Instrumentation chapter, the system manages instruments and TP interconnection with a relay matrix that manage a four rows analog bus. This are connected to the TP of the UUT through the adapter.

As shown in the sketch, the wiring goes from a needle (that will contact the board TP) through the adapter to end up on an interface strip that will connect that TP to the correspondent channel of the system relay matrix.

In case the TP is placed on the UUT top, the wire routing will pass through a top-bottom interface to reach the interface strip in the fixture.

As can be deduced from the image, the nails layout varies on each board. To position the holes in the correct position is needed the CAD file of the board, that supplies all the information related
to the TP coordinates on a board (Fig. 10). This is managed by Leonardo that will generate the drilling file for the NC machine placing the TP were needed.

![Diagram](image)

*Fig. 10 Board data flow*

As seen in the image above, an adapter consists of two main parts:

- **Fixture**: is a structure that contains auxiliary hardware, sensors and contacting nails. It is placed fiscally on the inferior part of the receiver and remains locked during the test.
- **Presser**: is a structure that contains auxiliary hardware, sensors and nails. It is placed fiscally on the top part of the receiver. The presser realizes the pushing movement during the test, driving the nails of Fixture and Presser in contact with the UUT.

The nails/probes are a critical part of the adapter for many reasons:

- Its repetitive contacting movement wear the nails which makes maintenance mandatory.
- Dirt can cause contacting problems by increasing the contacting resistance.
- Some probes must contact the UUT when presser is in half position (long travel nails) while others must contact only when the presser is in down position (short travel nails)
- The nails must adapt to different topologies of TP pads, the most important probes types are:
  - Sword Nails
  - Nine points Nails
  - Pyramid Nails

<table>
<thead>
<tr>
<th>TP TYPE</th>
<th>PROBE SKETCH</th>
<th>PROBE TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAD</td>
<td><img src="image" alt="Sketch" /></td>
<td>Sword</td>
</tr>
<tr>
<td>THROUGHT HOLE PIN</td>
<td><img src="image" alt="Sketch" /></td>
<td>Nine Points</td>
</tr>
</tbody>
</table>
The adapter, apart from the nails, comprehends as well specific hardware use to test the UUT. This hardware can vary, relays, colorimeters, programmers... All this hardware and needle must be testable in order to rapidly find failures if a malfunctioning is detected during the production. Exist a test sequence specifically to test the adapter called fixture check. The tests are realized using a cooper plate instead of a UUT. These tests are:

- **Floating probe test:** Realized in down position. Through a dichotomic algorithm detects rapidly if a probe is not touching the cooper plate. This would mean that either the needle is not present or that is not wired correctly.
- **Touching probe test:** Realized in half position. Through a dichotomic algorithm detects rapidly if a probe is touching the cooper plate. This would mean that either the needle has an incorrect length or that is not wired correctly.
- **Dirty probe test:** Realized in down position. Measures the resistance of the contact between the needle and the cooper plate. If the resistance is above a certain threshold this would mean that the needle head is dirty or weathered.
- **Short Probe test:** Realized in up position. Check that no needle is shorted with another.
- **Internal hardware test:** This set of tests varies from adaptor to adapter. It is an ad hoc test realized to verify the integrity and wiring of the internal hardware.
Flying probe technology

Flying probe systems are from by four or more robotic arms that are capable of contacting the board components even if not design for testability its been done. This is due to the possibility of contacting directly on components pin (Fig. 11 Flying probe). This fact, in addition to direct adaptation to the UUT (does not need an adapter) makes of flying probe systems the most flexible tester in board testing. The coordinates of the probes can be actively modified, so the system can perform different test over different boards without the need of stopping the system or replacing anything (if board width is the same).

Following a small capitation between BON systems and FP systems:

Advantages of FP systems:
- Production changes flexibility
- Fast test implementation
- Higher precision
- Higher accessibility

Disadvantages of FP systems:
- High cost of system
- Slower than BON system
- Limitations on complex test

In this thesis use case the system is aimed to work with two different versions of boards over big lots. For this reason, the most advisable choice would be a BON system, as selected by SEPA client.
Board testing procedure

Exist a standard board testing procedure that consist on three steps (Fig. 15 Board testing procedure):

- In circuit test or ITC
- On board programming or OBP
- Functional test or FCT

These three actions must be done sequentially. An option would be to remove the ICT or FCT test in order to shorten the test time or to reduce costs, though reducing the test coverage as well. On the other hand, is important to notice that OBP must be done before FCT test, given that otherwise the board would not be operative and so the FPT would be vain. Furthermore, ICT prevents FAIL boards to go into FCT, reducing risk of damaging the adapter and the UUT due to short circuits combined with a power on stage.

- In Circuit Test ICT

The ICT, if required, is the first stage on any board testing procedure. Ideally, its aim, is to verify if each individual component properties are within its tolerance values. However, this is not usually possible due to components inaccessibility or to lack of instrumentation. For this reason, three different levels of component check (defect detection) have been determined depending on the coverage level. There are three test Concepts:

- **Process test**: Detect process defect such as missing, misplaced, or wrong components; not soldered pins; and short circuits.

- **Component test**: Find faulty components. Tests the basic function of components in addition to process defects.

- **Parametric test**: Finds a parameter out of specification. Tests the prominent parameters in addition to the basic function and process defects.

Another consideration is how the test sequence is n this stage. A typical ICT sequence consist on:

1. Discharge of the board capacitors
2. Float test verify the contact between the system channels and the UUT
3. Short test on nets that shall not be shorted
4. Link test on linked nets
5. Resistors test
6. Capacitors test
7. Test of Diodes, Schottky diode … testable components at low voltage
8. Test of Transistors, MOSFETS, Zener diode … medium voltage components
9. Optional, power on test. Verification of some IC and voltage regulators.
10. Discharge of the board capacitors
During a standard ICT the UUT is powered off. Therefore, digital components that have the need of a power supply are not functionally testable. However, pin soldering wealth of these IC can be tested with two different technics: clap diode presence or electroscan test.

A final power on stage can be added to an ICT test sequence to realize component test to IC and voltage regulators. This stage depends strongly on the board nature and if it is already programmed or not.

**Float test**

The purpose of the following test is to verify the contact between the system channels and the UUT. The system measures the equivalent resistance with respect to all the others in short between each other for each channel connected to the UUT.

The resistance is measured by forcing a very low current and measuring the fall of voltage that it creates. This voltage will be as low as a threshold. In fact the equivalent resistance is less between the test point under test and all the others.

Since this equivalent resistance depends on the polarity of the voltage generator (for the effect of the joints, for example), in case of FAIL result, a test will be carried out automatically, by inverting the polarity of the driver.

If the test result is lower than the expected resistance threshold (200Kohm is normally used), we will have a positive test result.

**Short test functioning**

The purpose of the following test is to verify the absence of short circuits between the UUT nets. For each channel connected to the UUT the system injects a known current and verifies the voltage with respect to all the others in short between each other. This voltage will be as high as the equivalent resistance is greater between the test point and all the others. If a short is shown between one channel and all the others, other measurements will be carried out to identify which of the other channels is effectively in short with the first.

- **On Board Programming OBP**

This stage consists on programming the pertinent UUT components. Additionally, at the end of OBP, a checksum or an equivalent test is realized to verify the correct flashing of data. For some UUT passing this test does not ensure well-functioning, in this case performing FCT is recommended.

The mayor problems during this stage are due to the interferences and the noise that could alter the writing procedure and corrupt the data. In order to avoid this phenomenon, some measures could be implemented:

- An adapter design to reduce the length of the conductors that drive the OBP signals.
- The use of amplifiers and drivers to enhance the noise to signal ratio.
- The use of twisted cables to further reduce the noise effects.
• The use of minimal contacting points (TP) while programming to prevent the addition of interference on other nets of the UUT.

These interferences could have unexpected effects on the OBP success. Those effects would strongly depend on the environmental electromagnetic field, and would be a source of sporadic instabilities. For these reasons this stage is realized using long travel nails, and then moving the presser in a medium position (so called half position) where short travel nails (used for ICT) does not contact the UUT. This way the number of nails in contact with the UUT are those strictly needed.

For the use case (pg. 28) two external programmers in parallel are used to perform the OBP. The programming protocol is JTAG which consist on 6 all four of them susceptible to noise. This will be further discussed on use case chapter.

- Functional Circuit Test FCT

The functional test pretends verify the correct working condition of the board once it’s been programmed. This stage allows the system to verify that the programming stage is been performed successfully and to further improve the test coverage.

This stage requires to reproduce the working conditions of the UUT. This could imply the use of approximated models to simulate possible inputs or loads (motors, lights, RF communication...) that could be stressing the UUT or communicating with it.

The FCT requires a detailed design because once the adapter is assembled, modifications could be expensive or unfeasible. This fact makes the information exchanges between the test engineer and board engineer crucial. This communication is standardized by ATML mark-up language, but its use is not yet spread. This lack of standardization introduces a uncertainty that could affect costs and deadlines if a mis understanding occurs.

The test sequence on a FCT varies from board to board but some steps can be considered general:

- Power supply check
- Current consumption test
- Board reference voltages test
- Input/output communication test
- Board’s specific test sequence
- Discharge

This is the final stage, once finished the board is considered Pass or Fail.

Test models

To measure the various components values and to check its position and orientation (in the case of polarized components) a wide range of test models are available. Along this chapter the most significant Test Models will be described.
Today ATE are based on these test models. By using the proper test model, the testability coverage can be increased, and each measurement accuracy optimized. For this reason, and for debugging the already implemented test solutions, is important to understand and analyse how Test Model are implemented.

- Passive Component Test models

To test passive components, DC and AC measurements methods can be used. Impedance of capacitors and inductors depends on the stimulus frequency used to measure them. This implies that, to optimize the test, measurements at different frequencies are to be made. As it can be seen in Fig. 12 *Impedance at DC, 10kHz and 100 kHz*, the 1kΩ resistor is hidden to the measurement instruments when the stimulus voltage is DC, while at 10kHz it is barely measurable.

In short, reactive components may result to be hidden or to hide another component from the measurement instruments at some frequencies.

For ICT is necessary to measure each component individually. However, once

![Fig. 12 Impedance at DC, 10kHz and 100 kHz](image)

components have been mounted on the electronic PCB, is not possible to measure each component without taking into account the rest of the circuit. To achieve it, Guard techniques are used. They can be classified as active guard, if a source of power of power is needed, or as passive guard, if a source of power is not needed.

In the Fig. 13 Guarding techniques: ActiveFig. 13 is shown an example of active guard. It consist on a voltage follower (marked in blue) that provides the needed current to ensure a zero voltage drop between points A and B, and consequently insulating $Z_x$ from the rest of the circuit. Now $Z_x$ can be measured directly.

The implemented guard on Fig. 14 is passive, is not required an external power supply. By bypassing point B to ground, the current $I_{Z1}$ does not affect the ammeter measurement and $I_{Z2}$ is zero because $Z_2$ terminals results in an equipotential chain. Subsequently, $Z_x$ is isolated and ready for measure.

Along with guard techniques DC and AC methods can be used. However, a guard could not be used if the guarded component impedance is considerably less than impedance of the component under test.

---

3 Automatic Test Equipment
ZAC measure Test Method

This test method is used to obtain the impedance value, both real and imaginary parts. It consists on producing sequentially two AC stimulus at different frequencies. Then, for each frequency, measure the peak to peak current flowing through the circuit.

Equations below represent the components under test impedance value in function of the two impedance measurements. Two cases are considered, RL circuit in parallel (1.1) and RC circuit in parallel (1.2).

\[
R_x = F_{RKL}(Z_{F1}, Z_{F2}) \quad (1.1)
\]

\[
R_x = F_{RKC}(Z_{F1}, Z_{F2}) \quad (1.2)
\]

Out from those sets of two equations imaginary and real part of the impedance can be calculated thus obtaining the desired information.

Transformer Test Models

A lot of different models can be applied, below are listed two of them, one is a process test (impedance measurement method) and the other is a parametric test (Ratio measurement).

Impedance measurement method (resistance):

The model uses four wires measurement. • The resistance value for a transformer winding can be considered as a low value resistance measurement. This means that is required to perform a Kelvin measurement (4 terminals resistance measurement).
The generator “I0” forces a programmed current (I0) trough transformer winding. Then, the voltage meter “V” measure the voltage drop on the winding. Because, typically, the resistance value is “small” the wiring and the contact resistance should influence the measure. Two additional test points are used to connect the voltage meter “V” at the circuit. Due to its high impedance the measured voltage drop (V rx) will be equal to the voltage drop on the tested resistor.

**Ratio measurement method**

The model uses two wires measurement. The generator “G” forces a pulse on the transformer primary coil. Then, the voltage meter “V” measure and store the voltage drop on the transformer primary winding. Afterwards, the generator “G” forces a pulse on the transformer primary winding. Finally, the voltage meter “V” measures the voltage drop on the transformer secondary winding. With the measurement data is possible to calculate the percent ratio.

**Open Pin Test Models**

This test pretends to detect the soldering status of a IC, so it is classified as a process test. There are two methods.

**Electroscan**

The generator “G1” generates a sinus waveform that is injected through the pin of the IC. Then, a sensor plate picks-up the electromagnetic field and the active probe amplifies the signal. Once acquired the signal, a voltage meter measures the Electroscan active probe continuous signal output.

If the pin is soldered, the current pass through the IC generating a changing electromagnetic field. So is possible to appreciate an output of the Electroscan probe. If the pin is not soldered, the Electroscan Probe output signal would normally be significantly lower than 2 V.

**Clamp Diodes**

Each pin of an integrated circuit is usually connected to GND and VDD thought to two diodes. Such diodes are normally within the IC. Measuring one of the internal diodes, it is possible to
assure that the pin is soldered. If the pin is not soldered, you will measure an open circuit, otherwise you will measure a diode junction. In order to detect if the pin is soldered, it is enough to measure one of the two internal diodes.

If a similar pin (or a diode or something electrically similar) is connected in parallel to the pin under test, a problem arises: it’s not possible to discriminate if the pin under test is soldered. In such configuration you can’t use the “Clamp diode” measure method.
3. Case of use: BON (SPEA 3030IL) adapter design for an actual board production line

Working environment

This thesis was entirely developed in SPEA headquarters at Volpiano, Piemonte. I have been developing this specific adapter application in the SPEA system area and office during two months. For reasons of NDA (Non-Disclosure Agreements) between me and SPEA and client/s (with a direct or indirect relationship with my thesis work) and SPEA, I am not permitted to write or talk about client names or provide detailed information that could endanger any of the stakeholders.

The main characteristics of the application are:

- The system to be used is a 3030 IL BON single core with input and output conveyors
- The boards are organized in pallets of two boards respectively
- The specification requires the following steps (figure below):
  - ICT: It must be realized with LEONARDO.
  - OBP: It must be programmed with an external programmer with JTAG interface. The driver is provided by the client.
  - FCT: It must be realized in LabVIEW. The test sequence documentation will be provided by the client (block diagram appendix B). The LabVIEW implementation can be found in the appendix C.

![Fig. 15 Board testing procedure](image)

For the ICT test is not required a power on stage given that it will be covered by the FCT test. The ICT analysis will focus on its results, given its simplicity is not worth to explain all its implementation details. However, some examples of stabilization and of measurements on resistors, capacitors and other electronics components will be shown as an example.

The OBP test is actually realized within the FCT test. Nevertheless, it is usually considered a standalone step (and so do I) because of its importance, complexity and vulnerability to noise. Some problems that have been found during its implementation and that will be exposed and discussed. It will be explained, as well, the solution that it is been adopted.

The FCT test is the one that has taken the most of my time. It’s been developed in LabVIEW to improve the interoperability SPEA-Client and to reduce the cost of possible future projects in common. Unify the use of a programming language ease the exchange of information and so enhances the overall problem-solving capacity. The FCT test uses different external hardware like RF instrumentation or AC generators. For details see the appendix B.
Daniel Cabrera Fernández

- **Software Tools**

As can be seen on Fig. 16, the programs that have been used to develop the application are Leonardo and LabVIEW. RunPack at a lower level will manage all the commands sent to the non-external system instruments and to the system itself.

- **LabVIEW** (for developers) 2015 32 bit. Along with some packages:
  - GPIB drivers. “NI-488.2”
  - Vector Signal Generator driver (Signal Hound VSG)
  - Spectral Analyzer driver (Signal Hound SAXXX)
  - Elgar-cw801p AC generator driver
  - Spectrum Measurement Toolkit library (SMT). “NISMT1700”
- Leonardo YA ICT v2.90
- Windows 7 OS

The start test command is sent from the PC where the organizer is lunch to manage the flow of execution (Appendix B.1). Then, the organizer will manage the receiver movements and it will launch sequentially the ICT sequence (programmed in Leonardo) and the OBP and FCT sequences (programmed in LabVIEW) that, for this particular application, are mixed in a unique mixed sequence.

Then the executables will communicate with the system through dynamic libraries that form part of RunPack. In this particular case there are some external instruments that are directly commanded from LabVIEW, as a RF vector signal generator, an non SPEA generator AC…

All instruments (excluding RF communication) will have to interface the board through the adapter that will gather all these devices and drive them to the corresponding board TP.

Is important to notice the importance of LabVIEW in this project given that is acting at the same time as programming language and as a model to ease the SPEA-client and client-SPEA communication to exchange data at general sequence level and at technical low level about the test protocol.

---

**Fig. 16 Execution layer diagram**

<table>
<thead>
<tr>
<th>PC</th>
<th>Leonardo (organizer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OBP</td>
<td>FCT</td>
</tr>
<tr>
<td>LabVIEW</td>
<td>Leonardo</td>
</tr>
<tr>
<td>External instruments</td>
<td>System Instruments</td>
</tr>
<tr>
<td>Adapter</td>
<td>UUT</td>
</tr>
</tbody>
</table>

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29
ATE specific Equipment and external instrumentation

To develop the application the following system configuration it’s been used.

System Instruments

- Digital Voltmeter (DVM): To perform direct and indirect voltage measurement on the board. On it is used to measure the correct functioning of the UUT voltage regulators and to check the input voltage (By using a partition resistor)
- Counter (CNT1): The is one led sensor that transduces the light intensity to frequency and this counter is used to measure it.
- Driver (DRI): It is a high precision low voltage generator and it can generate low voltage sine waveforms as well. This instrument is use to generate the stimulus of the different test.
- Booster (BSTV): It is a medium voltage generator. This instrument is use to generate the stimulus of the some test.
- User Flags(USERFLAG): They are low voltage relays of the system. Is the most used way of interaction between system and adapter.

System Power Supplies

On the system there are four power supply, bur only two are used:

- Fixed Power Supply 1 (5v): Adapter internal hardware supply and for power on of the UUT at low voltage, this is, bypassing the voltage regulators and feeding directly the microprocessor.
- Fixed Power Supply 4 (24v): Use to supply the electro-valve coils to control the three pneumatic fingers used to press the three UUT switches.
System Channels

To access all the test points of the UUT, the number of channels of the system must be at least equal to the number of the number of TP. Additionally, some service channels are needed. These channels are reduced compare to the number of TP channels but are important to perform some functional test and the discharge. All together TP channels and service channels must not the system channels. This check was done during the feasibility analysis and so two relay matrixes have been added reaching 640 (Fig. 19) channels on the systems that are enough to cover the application necessities (used 566 probes)

There are used two types of scanner⁴:

- Conventional Scanner: It manages 64 signals that are below 100 volts at any moment. There is not a proper relay to cut higher voltages.
- Conventional Scanner + Insulating modulus: It manages 48 signals that are below 100 volts at any moment. There is not a proper relay to cut higher voltages. Additionally, it has another 16 signals that are sectioned by a HV relay, so in case of need, the channel can be isolated from the signal.

The UUT main supply is three-phase 230V 50Hz so there are some nets that are expected to reach voltages above 100V and so the need of the Insulating modulus.

![Fig. 19 System channels](image)

External instruments

Some external instruments are to be used for each board site individually (two boards on the panel of boards):

- **Elgar cw801p AC generator**: used for board power supply
- **Frequency Counter Key Sight 53230A**: To measure the real time clock of the UUT with high precision.
- **J-Link programmers**
- **Client provided optical communication device**

Common resources:

- **Signal Hound VSG**: To superficially test the RF reception antenna and circuitry of the board. Is not possible a rigorous test given that the system is not an anechoic chamber.
- **Signal Hound SAXX**: To superficially test the RF emission antenna and circuitry of the board. Is not possible a rigorous test given that the system is not an anechoic chamber.

---

⁴ so is called the board that contains the relay matrix and the control circuitry
A system modulus called breaking unit BRU is used for safety reasons. This device is introduced between the external AC generator output (neutral and phase) and the system interface. At the same time the BRU is connected to the system thought CAN allowing it to interact with the system status, for example, if the test program will be interrupted or the system abruptly tuned off the BRU will cut off the AC generator input. Furthermore, the BRU is to be connected to the safety chain not allowing the operator to access the HV area and so being compliable with the 2006/42/CE directive.

In Fig. 20 is possible to see the adapter interface where each section is highlighted and classified as its been done in this chapter:

![Fig. 20 System interface, Adapter side](image)

**Test sequence**

The test sequences are the essential part off the application. During the test design all the requirements will pop up. So, instruments and system necessities will be determined, as well as drivers, software to be used... In this way we can ensure that this is the concept stage the top abstraction level of the application.

Within this section are included the design and debug off each stage:

- Design: Specification analysis, execution flow, and necessary instruments to perform it
- Debug: Calibration, adaptation and error detection performed.

The appendix B has block diagrams that ease the execution flow understanding and during this section references to it will be frequent.

- Automation and top-level test sequence management (Organizer)

The organizer is a building script of LEONARDO that execute the high-level automation commands of the receiver and the various executables execution (ICT and FCT) (APPENDIX B: Case of study Test sequence flow chart-1). It manages part of the messages displayed to the user as “ICT test started” and is capable of setting the final result of an UUT.

In this case of study, the organizer its used to control the automation and to manage the top-level test sequence (ICT, OBP&FCT)
This step is characterized for being a very standardized process where the sequences of test are well known (APPENDIX B: Case of study Test sequence flow chart-2). For this reason, it will not be deeply analyzed.

The general test flow is shown on Fig. 22. Of this flow the steps that were skipped were: Fuse, Digital transistor, Opto-couplers and Power on test.

The problematics found during the ICT were manually adjusted helped with the UUT schematics, that provides the necessary information to perform the adjustments, for example where to place a guard.

The first problem that popped up (apart from some minor adjustments) was due to some resistance measurements. The presence of voltage regulators that were absorbing the current from the driver affected the measure. In some of these cases, the voltage regulators could be disabled by the use of a guard on the disable pin and so switch the output pin to a high impedance status.

The measure of some capacitors of 100pF was unstable, depending on the board Supper capacitor net status the voltage measure could vary from 100pF to 150pF.

The power on of the UUT was implemented but not enabled given that the FCT covers these components.
Notice that the ICT will have the most relevant considerations on the results chapter where the stability analysis and repeatability analysis are performed.

- FCT

The FCT has been entirely programmed in LabVIEW. The majority of the block diagrams are very large and so they have been placed into the appendix C. The block diagrams are numerated and will be referenced when needed.

On the contrary, the FCT conceptual sequence is in the appendix B where the complete Flow diagram of the test application is represented.

The protocol document with the specifications and the concrete values is not provided to preserve the SPEA-client NDA. However, even if this document is used as an official reference of what client is requesting, the actual technical communication "document" it’s been the LabVIEW program on its own. Different virtual instruments where shared and with them information about instruments setting, tests thresholds, testing procedure, etc…. For this reason, it is possible to ignore the protocol document for the scope of this thesis. Note that some sets of values have been modified or an old version used to hide the client identity and its board real characteristics.

The FCT test sequence is (item 0 is an example):

0. Task long name (task short name for LabVIEW case structure):
   a. test 1 (short name for LabVIEW case structure), test 2 ...

1. Initialization of instrumentation (Initialization) and SART:
2. Consumption measurements (CONSUMO):
3. Output voltage AC generator check (V\_MEAS\_Pres)
   a. V\_PRes\_FA, V\_PRes\_FB, V\_PRes\_FC
4. Power nets check before programming (MEDIDAS\_V)
   a. +5V(TP3), +3v3(TP27), +3v3\_AFE(TP8)
5. Programming OBP (PROGRAMACION)
6. Power nets check after programming (MEAS\_AFTER\_PROG)
   a. +3v3\_WMBus(TP17), +3V9\_LTE(TP65), +5V\_P1(TP15)
7. Real time clock calibration (RTC\_CAL)
   a. RTC\_PERIOD, RTC\_CAL
8. Main power supply measurement by optical command (DLMS\_Read\_V)
   a. V\_FASE\_A, V\_FASE\_B, V\_FASE\_C
9. DC-DC simulated current read by optical command (DLMS\_Read\_I)
   a. FASE\_A, FASE\_B, FASE\_C
10. Component test of stitches 1 to 3 and led DS (Sw1Sw3Sw5+LED)
   a. SW1, SW2, SW3, LED\_S1: Red(%), LED\_S2: Blue(%), LED\_S3: Green(%), LED\_S4: Clear
11. UART communication (P1\_COM)
   a. P1COM head, P1DATASize
12. SIM chip ID read (SIM\_CHIP\_ID)
   a. SIM\_CHIP\_ID\_LEN, SIM\_CHIP\_ID
13. LTE modulus power supply check by optical command (LTE\_VOLTAGE)
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a. LTE_VBATT, LTE_VCOIN
14. LTE emission (LTE_TX)
a. LTE_TX_AB, LTE_TX_FREQ_L, LTE_TX_FREQ_H, LTE_TX_POWER_med
15. LTE reception (DLMS_LTE_RX)
a. LTE_RX_banda20, LTE_RX_banda8, LTE_RX_banda3
16. WMBUS TX (WMBUS_TX)
a. WMBUS_RF_FREQ, WMBUS_RF_POWER, WMBUS_CALIBRATED
17. WMBUS RX (WMBUS_RX)
a. PKT_REC
18. Battery test (BATERIA)
a. SuperCap, V_BackUp

The implementation of this sequence in LabVIEW is done with a state machine form by, a que and a case structure nested in a while loop (APPENDIX C: LabVIEW-1). The case structure contains all the different test and execute them as ordered in the que until the end state is reached. As can be seen on the block diagram Fig. 23, each state follows the same sequence:

1. Deque
2. Task execution
3. Task results interpretation and storage
4. Site AC generator switch off and site disable only if the task has failed
5. Sequence end if both sites have failed otherwise execute next step

The final result check is done once the test is finished or the two sites are fail.

On the APPENDIX B: Case of study Test sequence flow chart the task sequence is shown. Now each task will be studied in detail.

Initialization of instrumentation and START

In this step its realized a check of the communication of all instruments:

Fig. 23 Flow chart state machine LabVIEW
• AC generator for site 1 & 2: Open visa communication, set voltage value to zero and query the voltage value. They use a GPIB port configured in series.
• Frequency counter site 1 & 2: Open communications, query IDN. USB port
• Vector Signal generator: Open communication. USB port
• Spectral Analyzer: Open communication. USB port

Is the first step to be executed. If for any reason the communication with an instrument or instruments the program will have to disable the corresponding site or sites execution.

Notice that in this step the passive discharging resistors (APPENDIX A: Electrical scheme-9) are disabled by closing the user flag 13 and that the fixed power supplies 1 (5v) and 4 (24v) are enabled.

This stage was initially projected to be an independent program executed once for each production lot. Instead it is executed on each panel test. This ease the debug and reduce the time needed to check the different instrument connection status. However, it increases the overall test time over large production lots given that an extra time is added on each test execution for a check that was already done on the previous panel test.

Additionally, the initialization step loads the test sequence from an initialization file and store it in a cluster with a string array (test sequence) and a string (board description).

![Initialization (LabVIEW), Loading test sequence](image)

This test sequence will be added on a step called START that will inter in order all the steps in the que that sequentialize the state machine.

![LabVIEW, case step START](image)

1. Consumption measurements

The aim is to measure the absorbed current by the UUT on eight different UUT main supply conditions:

1. $I_{VA110}$: Phase A at 110V ac
2. $I_{VB110}$: Phase B at 110V ac
3. $I_{VC110}$: Phase C at 110V ac
4. $I_{VABC110}$: Three phase at 110V ac
5. $I_{VA230}$: Phase A at 220V ac  
6. $I_{VB230}$: Phase B at 220V ac  
7. $I_{VC230}$: Phase C at 220V ac  
8. $I_{VABC230}$: Three phase at 220V ac

And with two loads of 20 ohms connected to certain nets.

First of all, the loads are activated by closing the User Flag 12 (as can be seen on APPENDIX A: Electrical scheme-8). Then the AC generator is set to the corresponding setting (1-8) and a certain time is waited to ensure a stable measurement. After this, a safety check is done by reading by VISA from the AC generator the output current. If any short circuit is present the test would be stopped at this pint disabling the generator and the site in short circuit. The reason to do the safety check is that this step is the first HV test realized on the board and so the importance of a fast detection of a short circuit (fixture and UUT could be damaged, even if there is a 500mA fuse).

Finally, the measure is done first in site 1 and then in site 2 because of the use of common resources (digital voltmeter). System instruments in this case are appertaining to the same bay (single bay machine).

The measure of the current is done using a shunt resistor (50 ohm) between the neutral of the AC generator and the board mass. See APPENDIX A: Electrical scheme-8, there is present the wiring explained just before.

Go to APPENDIX C: LabVIEW-2 to see the LabVIEW implementation.

2. **Output voltage AC generator check**

This is a test that was not in the protocol document but that has been added to ensure that the voltage input on the board was within the tolerances of the AC generator. This check allow is mainly for debug and fail in case the fixture or the instrumentation are damaged or not well calibrated. For example, the fuse on APPENDIX A: Electrical scheme-4&5 would be detected if it were burned.

The measures are done with the DVM of the system, one by one first on site 1 and then on site 2. Notice that the voltage to be measured is above the specification of the analog bus (ABUS) and...
of the DVM as well. To reduce the voltage to a measurable level a voltage divider is used. The partition resistors are settled to divide the tension by 100. This hardware is in APPENDIX A: Electrical scheme-10

3. Power nets check before programming

This substitutes the power on ICT where the board internal power nets are checked. It simply uses the DVM to measure the voltage of three nets respect to the board mass: +5V(TP3), +3v3(TP27), +3v3_AFE(TP8).

The LabVIEW block diagram is exactly as in Fig. 26 LabVIEW, step Output AC GEN check but changing the TPs to measure.

4. Programming the UUT, OBP

This step is performed in parallel. Each site has an individual J-Link programmer that allows a real parallel execution.

The wiring from the J-link programmer to the UUT TPs are commutated with 7 relays (APPENDIX A: Electrical scheme-5&6):

- TCK, TMS TDI and TDO signals are commutated with a FXBUF board commanded by user flag 10 for site 1 and user flag 11 for site 2
- GND and RESET signals are commutated with FXSEX200 commanded by user flag 10 for site 1 and user flag 11 for site 2
- EZP_CS is sectioned directly with the User flag 18 for site 1 and user flag 19 for site 2

When the user flags are open the TP goes into the system channel that corresponds to the TP. On the contrary when the user flags are closed the TP is wired to the J-Link programmer. This commutation is done to avoid that the programmer state affects the board during other test and to avoid interferences during the OBP from the channels of the system.

On first place the user flags 10 and 16 are closed to connect the programmers to both UUT. Then, in parallel, are generated two security keys, one for each UUT. This key is used to “lock the UUT” to the not allowed users. It will be stored in memory and encrypted once finished the test with a positive result.

After the key has been generated the microprocessor is flashed. To check that the programing has been completed successfully, four verifications are made:

1. The command has ended with no error, this is, the return value is different from -1
2. A key word, in this case REBOOT, is verified on the output string of the command window
3. The OBP has not taken more than 40 seconds, it usually takes around 35 seconds.
4. Read the firmware version by optical command. It must correspond to the required version.

Once all these verifications are passed the board is considered well programmed. To end the task execution the J-Link programmers are disconnected again by opening the user flag 10,11,18 and 19

The LabVIEW block diagram can be seen on APPENDIX C: LabVIEW-3
5. *Power nets check after programming*

This step checks the power nets of the peripherals. It simply uses the DVM to measure the voltage of three nets respect to the board mass: +3v3_WMBus(TP17), +3V9_LTE(TP65), +5V_P1(TP15)

The LabVIEW block diagram is exactly as Fig. 26 LabVIEW, step Output ACGEN check but changing the TPs to measure.

6. *Real time clock calibration*

Within this step the real time clock of the UUT is calibrated. To do so it is used an external high precision frequency counter. Both counters are connected by closing the user flag 17 (see APPENDIX A: Electrical scheme-14) that will close the corresponding relays of the FXSEZ200 relay board.

Then real clock time of the board must be activated by entering the parametric mode of the board. For this reason, is necessary to send then corresponding command to the board through the optical port.

Then, programmed with a state machine on LabVIEW, are sequentially realized the following sub-steps:

1. Frequency read: The frequency is measured with the frequency counter and stored in a shift register.
2. Write constant: The calibrating content is calculated using the board standards and sent to the UUT by optical command
3. Reboot UUT: In order to make effective the change the board must be rebooted
4. Read Constant: The constant is read by optical command from the UUT to check the correct writing of the calibration constant.

To consider this test pass, the frequency has to be in between a value and the constant written must correspond to the read constant.

Once ended the task the frequency counters are disconnected, user flag 17 is open.

The LabVIEW block diagram can be seen on APPENDIX C: LabVIEW-4

7. *Main power supply measurement by optical command*

This step consists on using the build-in board measurement instruments to check the voltage value of the input power line. To perform it is necessary to switch selectively the different phases of the UUT: phase A (V_FASE_A), phase B (V_FASE_B), phase C (V_FASE_C)

The User flags that manages the phases switching are common to the two UUT (see APPENDIX A: Electrical scheme-4&5). To reduce the task time execution and the number of relay switching, each test of this task is realized in pseudo-parallelisms. In other words, the relays of a phase are first closed, then the command (to measure that phase voltage) in send to both UUT in parallel and finally the this is repeated with the next phase.
8. *Current read by optical command, build-in intensity measurement IC test.*

This step executes a task to test an internal IC that measures the current on each phase. In this case the UUT must be put through a simulated current on certain nets. This will allow to simulate approximately the real working conditions of the IC.

This task has suffered some modification during the debug of the application, so the hardware used to implement it is not on the electrical diagram. For this reason, it is displayed on ¡Error! No se encuentra el origen de la referencia., instead.

On first place, the phase B and C must be switched off and the phase A must be switched on. Then, as can be seen on ¡Error! No se encuentra el origen de la referencia., both sites TPs are connected in parallel over the rows 1 and 4. Next, the driver signal generator output is connected to the row 1 referred to the row 4. The output of the driver is calculated to match voltage fall on the board nets described on the protocol document (not available).

Finally, all three currents are read by optical command on both sides in parallel.

The LabVIEW block diagram can be seen on APPENDIX C: LabVIEW-6

9. *Component test of stitches 1 to 3 and led D5*

Due to the size of the block diagram of this test, it has been separated into two screen shots (shown below) even if some information is missed.

**Switches 1 to 3 test**

The switches are tested by pushing them with pneumatic fingers for one second and then releasing them for 3 seconds. This action is stored on a register that will increase by one the integer value already stored. This variation is read by with an optical command.

So, as shown in the figure below, the first step is to read the value of the three registers of each board. Then this value is stored.

Then, the electro-valve disposed on APPENDIX A: Electrical scheme-12 is activated to move the pneumatic fingers down. To do so is necessary to close the user flag 15. After one second the pneumatic finger is released (user flag 15 reset).

After 3 seconds, the three registers of each board are read again and compared to the previous value. If the value is the same or less the register is read again up to four time before the test is considered failed. This retries were include because the optical port communication can be unstable under certain circumstances.
LED test

The LED is turned on with a command sent on the beginning of the three switches test. Then the measurement is done with a colorimeter that transduces the light intensity into electrical signal frequency. Additionally, this sensor is equipped with three filters red, green and blue, that will allow to take four different measurements (no filter is the fourth). On Fig. 28 V009-V012 correspond to each of that measurements.

Is possible to appreciate in the figure that an extra command has been added before realizing the frequency measurement. This is done because, during debug, has been observed a change on the led status when the different switches where pressed (is done in parallel), and so affecting the measure of the LED. By adding this extra command is possible to ensure no disturbances between the two tests.

UART communication

This sequence aims to test that the serial port (P1_COM) works correctly and only when the DATA_REQ signal is active. The first bytes are a known header, so they are used to make a comparison. The port sends constant frames every 1s, so activating the signal during 1,2s and
deactivating it for another 1.2 seconds, we should see the number of frames corresponding to when the signal has been active.

The same PC COM used in fixture to communicate with the optical port is used to communicate with the TTL signal coming from the data out signal. This is possible thanks to the use of a transceiver that converts the TTL signal from the board to the RS232 signal of the PC (APPENDIX A: Electrical scheme-15). To use the transceiver the user flag 16 has to be closed to commutate the relay4 of both FXSEZ200 (site 1 and 2).

Then the sequence is implemented using the system user flags (APPENDIX A: Electrical scheme-3).

The header is checked to verify that the data coming out from the UUT is correct. Instead, the data length check is done to verify that the DATA REQ signal is acquired correctly and that the UUT stop sending data after 1 second.

The LabVIEW block diagram can be seen on APPENDIX C: LabVIEW-7

11. SIM chip ID read

The SIM is build-in the UUT so to get its number and store it as requested by the specifications, has to be done by optical communication. This is realized in parallel on both sites by sending the correct command to the UUT. The data received is expected to have a length of 19 ASCI characters otherwise the UUT is considered FAIL.

![LabVIEW, Step SIM CHIP](image)

12. LTE modulus power supply check by optical command

This step checks the power nets of the LTE modulus. It simply sends two commands for each board to read the voltage on two nets: LTE_VBATT and LTE_VCOIN. Then the information is subtracted from the data returned by the UUT.
13. LTE emission

This task pretends to test the LTE emission modulus. To do so, a command is sent to force the UUT to generate a tone of known bandwidth and central frequency that then will be measured by the spectrum analyzer. If the measure is within a determined threshold the test will be considered pass. Notice that this test has to be performed in series for the two sites because one UUT could interfere with the other.

The LabVIEW implementation (APPENDIX C: LabVIEW-8), is done by the use of a state machine. The states are: Enable UUT LTE TX, Configure the spectrum analyzer, Perform the measure and finally, disable the LTE modulus. The last test is important in order not to interfere with the UUT measurements on site 2.

There is implemented a reboot on fail on the Enable UUT state. During debug some misbehaviors have been detected while performing the generate tone instruction, being necessary to reboot the UUT to recover the control over it.

This test is very sensitive to the antenna positioning and can just guarantee the central frequency precision and band width, not the signal power.

14. LTE reception

This task pretends to test the LTE reception modulus. Three known signals are generated sequentially, checking the UUT reception by reding it by through its optical port.

The test is implemented in LabVIEW (APPENDIX C: LabVIEW-9) using a state machine. The states are:

1. Initialization of VSG RF signal for band 20
2. Data read from UUT (band 20)
3. Initialization of VSG RF signal for band 8
4. Data read from UUT (band 8)
5. Initialization of VSG RF signal for band 3
6. Data read from UUT (band 3)
7. RF disabling

As can be seen there is an initial state for each of the three bands were the instrument is settled to the corresponding values of frequency, amplification, tones spacing, number of tones and band width. And a second stage were the band is read by the UUT and received through the optical port. The data is then processed, and the result compared to the tolerance thresholds.

As LTE emission step, this step is performed sequentially to avoid unexpected interferences.

15. WMBUS TX

In this step the Wireless M-Bus modulus is calibrated and tested.

A command is sent to the board to start emitting the carrier signal (not calibrated). Then the frequency of the carrier signal is acquired by the spectrum analyzer and stored. Next, the value is used to calculate the calibration constant of the WMBUS for that UUT that will be sent through the optical port to the UUT.

After that, the command to activate the carrier signal will be send again (already calibrated) continuing with its measurement with the spectrum analyzer. This measure has to match the target frequency, otherwise the UUT will be considered FAIL.

The implementation in LabVIEW, as usual, is a state machine. Its states are:

1. Enable UUT carrier wave
2. Configure the spectrum analyzer
3. Measure the carrier wave
4. Calibrate the UUT
5. Reset the UUT: needed for the calibration to take effect
6. Measure calibrated carrier wave
7. Disable the carrier wave

This test is performed in series to avoid interferences between both UUT

16. WMBUS RX

This task tests the ability of the UUT to received RF modulated data. A file with a predefined IQ values is loaded into the vector signal generator. The VSG emit the data frames, allowing a the UUT to read them. Finally, the number of data frames is read from the board with the optical port. This number must match the predefined value (depending on the IQ data file) to consider the test pass.

The test is implemented in LabVIEW with a state machine. The states are

1. Enable UUT WMBUS RX modulus
2. Generate data frames
3. Read the received frames
4. Disable the WMBUS RX modulus (and Reboot the UUT)

17. Battery test

This task switches off the UUT and, after 2 seconds, measures with the system DVM the voltage of the nets which its voltage depends directly on the super capacitor. It is present in the UUT for emergency situations in which the power supply is abruptly interrupted.

The related nets are: SuperCap and V_BackUp.

These nets must reach a voltage threshold to consider that the task have a positive result.

Adapter design

Before starting the development of the application, it is necessary to be clear about the objectives of the test (test time, specifications to be respected etc.), and to have all the essential input data at your disposal (these will be listed later).

Analysis of the customer’s requests, It is important to receive all the information on the product to be tested, in order to develop an application, and in particular:

• Type of board: The type of test depends heavily on the board to be tested. For example, a test of a board which would be installed in a satellite, must be checked 100%, so as to avoid any type of problem (no components must be left uncovered). In our case the board does not require a complete coverage, in fact, the coverage is around 60%. The board will be used for non-critical commercial use so no special measurements are to be taken.

• Type of test to apply: Based mainly on the type of board and on the type of system, the customer may request different types of tests on its board. In this case the client required ICT, OBP and FCT. This way they ensure the well-functioning of the board.

• Number of boards to be tested: It is important to know approximately how many boards will be produced. For example, if there are a large number of boards to be tested, a brief testing time will be required. In our case the production through put is low and so the test time is not critical.

• Start of production: It is essential to know when the customer will start production of the boards, and consequently know when the application can work on its testing systems. In this use case, the resources needed to develop the board application, were disposed and planned in time taking into consideration this data. It is not yet installed.

• Mechanical constraints: It is also sometimes necessary to ensure at the customer’s site, that there are no mechanical constraints for the UUT testing or for the interface construction. This is very important so as to avoid any damage to the production boards during their testing. No problems have been found for this case of use.

Test specifications, all information regarding the boards and the test, received from the customer, shall be included in a specific test document. This document is necessary for the writing
and designing of the functional tests. It includes all the various steps necessary to complete the test. The test specifications are generally written by the same person who designed the board.

In this case of use the protocol document exists but will not be shown to protect the client identity and the board data. This protocol is shown in the appendix B were a flow diagram shows the FCT test sequence.

**Feasibility analysis**, can be performed, based on the information supplied by the customer, including or not the test specifications. The tasks must be planned, and the responsibilities, equipment and timing of whole project must be defined. The result of the feasibility analysis must be communicated directly to the person who has requested the test.

**“Testability” analysis**, besides feasibility analysis, it is also necessary to analyze the “testability” of a board. The board must be designed to perform the type of test that the customer requests. For example, to perform an in-circuit test (ICT), all the board internal connections (net) must be accessible from the test points.

All these considerations have been made applied to the case under study. A screen capture of the testability results for the ICT are shown in Fig. 31. For FCT, is been required a change on the system configuration and the acquisition of some instruments.

![Testability analysis](Fig. 31 Testability analysis)
Daniel Cabrera Fernández

- Mechanical design

My work has been centered on the electrical and programming part of this case of use, so the mechanical part will be explained superficially. Notice that, projecting the mechanical part, is a very standardized process that leaves little margins to adopt different solutions.

The adapter is constituted of the following main elements.

**Presser**

This presser is projected to handle a panel of two UUT. In which respect the mechanical aspects it is constituted of:

1. **Reference plane:** Plane fixed to the system receiver
2. **Presser free plane:** A plane with a little freedom of movement. The position of this plane with respect to the reference plane can change around 5mm on all directions.
3. **Two centering spines:** The plane nearer to the panel is free respect the other plane. These spines refer the presser free plane with the top plane of the fixture, assuring a high positioning precision of the presser respect the fixture and UUT.
4. **Conveyor Pusher**
5. **Top-Bottom interface:** Is not possible to communicate with the system directly from the presser, so this kit allows to use the fixture as an interface with the system for the presser.
6. **Discharge holes:** UUT high components may crash with the UUT if it is too high. In this case the screen of the UUT is too high so this discharge hole is being projected
7. **Pressing fingers:** Strategically collocated as explained on Strain analysis section.
8. **UUT pre-pushers:** Predispose the UUT and pushes it before of the pressing fingers until it opposes a certain force (mobile plane springs)
9. **Anti-crash sensor:** On the fixture there is a complementary hole that prevents this sensor from engaging when the receiver goes down. It is connected to the safety chain of the system receiver so, if the fixture is not compatible with the presser, the sensor will be engaged and so the receiver motors stopped
10. **Presence Sensor** (10): Explained on previous sections
11. **Anti-rotation Sensor:** Explained on previous sections
12. **Volumetric Sensor**: Explained on previous sections

This application does not require a top contacting so the presser does not have any probes. However some hardware must be tested (or used) from the top part of the UUT:

- **One Led**: So two sensors (one for each site) are needed to measure the intensity and color of the led. The sensor is placed inside the presser while a optical fiber is disposed between the sensor and the led (Fig. 32 Presser-14).
- **Three switches**: Six pneumatic fingers are positioned (Fig. 19 Presser-15) and so one pressure input (Fig. 19 Presser-16).
- **Optical port**: Communication with the UUT realized with a device That has been provided by the client (Fig. 19 Presser-17)

**Fixture**

The fixture shall contact the UUT from below and all the probes must contact with the corresponding TP. This part of the adapter is characterized for being fixed to the system, to which is perfectly coupled thanks to two centering spines on the bottom part of the fixture. Additionally, the receiver has locking mechanism that prevents the fixture from moving. In this case, the following components has been considered in the design:

1. **Test area**: The UUT will be placed over this area
2. **Presser centering hole**
3. **Fixture locking mechanism**: The screws present on that area of the fixture are contacted by the receiver locking mechanism. The adapter side system interface (Fig. 20) has its own centering system, this is, it is a free plane with two centering spines.
4. **Centering Nail**: It centers the board approximately so the centering spines (for the UUT) enter the UUT reference hole limiting the friction.
5. **UUT centering spines**: The UUT is referred to the fixture by means of two reference holes and two centering spines. As farther is one reference hole from the other, better will be
the UUT centering due to a lower sensitivity of the tolerances produced during the spine positioning.

6. **Springs**: Explained on Strain analysis section
7. **Anti-crash hole**: as explained before, it prevents the anti-crash sensor from being engaged.
8. **Presence Sensor** (10): Explained on previous sections
9. **Anti-rotation Sensor**: Explained on previous sections
10. **Volumetric Sensor**: Explained on previous sections

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**Strain analysis**

After being designed, the adapter is constructed on the basis of the standard working cycles, in which some phases may be omitted, if not requested.

The adapter is chosen to contact the board from the bottom, entering the board from the input conveyor with the soldering part looking down. This is the normal approach given that on the top part are mounted components, this makes more difficult the access to the TP pads.

Then, as previously mentioned, drilling file is generated from board cad file. This file is used by a CN machine to drill the TP layout on the fixture.

However, before realizing the drilling operation, a stress and deformation analysis is performed on the board.

In order to perform this analysis, the so-called pressure fingers are placed first. Its mission is to press the board against the fixture nails. Neglecting friction, this force will be equal to the force exerted by fixture nails. Note that, because of the differences between the nails layout and
pressure fingers layout a deformation will be produced on the board, and so, to avoid damaging the board, will be important to reduce the deformation effect. Of course, depending on where pressure fingers are placed this effect will change. However, they must respect some tolerances with respect the mounted components, and so its position is restricted by this fact.

There is another element that is used to further reduce the board deformation. It is a mobile plane (and so we will refer to it, Fig. 35) placed between the UUT and the fixture. Note that, to let the nails pass through, this plane must be drilled with the TP layout. The idea is to place standoff columns that will support the UUT until the receiver goes down. These standoff columns will react to the force realize by the pressure fingers thanks to a several springs that will push the mobile plane up against the UUT.

![Fig. 35 Mobile plane for the UUT](image)

So, we have a force balance:

\[ F_{p.fingers} = F_{nail} \cdot N_{nails} + F_{spring} \cdot N_{springs} \]

Where: \( F_{nail} = 300 \text{g} \); \( N_{nails} = 534 \); \( F_{spring} = 1 \text{kg} \); \( N_{springs} = 10 \)

This design analysis has been done with the warpage simulator that helps to optimize the positioning of the pressure fingers. An iterative approach has been adopted.

Once the deformation is reasonable, is possible to proceed with the drilling.

As the simulation is an approximation to the real board deformation, it has been done an analysis of the real deformation by using strain gauges and a data acquisition system. This way is possible to compare the results to see the warp page reliability and to confirm that the real board deformation is within the tolerance values.

The internal hardware distribution will be discussed on Electrical design section.

**Centering check**

To check the correctness and tolerances of the needle positioning, a test is performed. It consists on verify, with a microscope, if the nails contacts on the center of the TP pads (Fig. 36) and so validating the mechanical design.
This check is crucial to realize an early detection of any mechanical problem of the adapter. If one probe goes out of tolerance it would probably mean that many probes will have this offset. The holes have been drilled by a CN machine so no error, or very little error is introduce during drilling (maybe drill bit wear). Thus, an offset on one of the nails, usually means a dimensioning error of the panel of boards dimension’s. It could also mean a bad calibration of the system receiver.

This implies that, in most of the cases, an error detected at this point would mean that all the fixture would have to be remanufactured. Thus, the importance of an early error detection of the nails alignment.

- **Electrical design**

The design process of the fixture is ideally done linearly. In other words, an initial design is done aiming not to realize mayor changes on the adapter. The design of the adapter cannot be cyclical or have any design iteration due to the high cost of a post manufacturing modification.

Nevertheless, is predictable that design errors will occur. The most frequently are:

- Wiring error: Very frequent, it has little impact on the adapter cost. The adapter can be modified easily.

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5 Is the reference UUT, that is characterized of being a defect free board.
• Hardware not considered: Depending on the necessities of this hardware it can have a considerable impact on the adapter cost. To be consider: if the HW is at our disposal; if it fits into the presser or the fixture; if the requested power supply is accessible or present; If the system has the User flags and resources to manage the new HW; etc.
• TPs not considered: This could impact highly on the application cost. In some cases, TPs cannot be drilled manually, so the fixture must be disassembled and drilled entirely again.

Additionally, the client could change the specifications: changing of the test sequence, increased coverage of the test, change on the PCB or the nets...

For these reasons, the adapter is designed in such a way that maximizes the possible modifications. Having into account possible future uses of the fixture or design errors. For this reason:

• All feasible TPs are drilled on the adapter even if no probes are placed on them.
• The holes needed to test LEDs, screens, switches... are drilled as well
• The number of relay boards on the adapter are over dimensioned (in number and power)
• Not all space on fixture is used if possible.

In this way, predictable or minor changes on the adapter can be made with low costs.

The electrical design of the adapter uses as source the protocol document that is not available here (NDA) so for justify the use of the different HW I will refer to the section Test sequence. The design has been divided into ICT, OBP, FCT and protection devices. This classification permits to identify the aim of each HW used in this application.
The ICT is a very standardized test and so the system has the need resources to perform it. The different TPs are wired directly (in case of LV net) or indirectly\(^6\) (HV net) to the system channels. These channels are then managed by the system through the analog BUS.

The TPs HV are wired with an AWG24 BLUE cable and the TPs LV are wired with an AWG26 cable, see “Fig. 37 Fixture internal HW” and “Fig. 20 System interface, Adapter side”.

During the initial and final UUT capacitors discharge, the adapter uses two discharge resistors (one for site) to increase the discharging velocity. APPENDIX A: Electrical scheme-3 (discharge low voltage capacitors).

Note that some system instruments must be referred to the board ground. These instruments are, the counter, both drivers (in this system there is just one) and the booster (APPENDIX A: Electrical scheme-1).

The majority of the customized HW present in the adapter aim to cover the FCT necessities. A general overview of all the HW used in fixture will be done (Fig. 38 Fixture internal HW, blocks) and then design process will follow. The previously discussed Test Sequence order will be used as a guide to explain why each hardware is been chosen.

Following an image of the internal part fixture where each hardware has been identified with a name and with the main characteristics. Notice that on the top part of the fixture (exterior) are placed the J-Link programmers, two lamps to indicate the HV presence and two fused to protect the fixture HW.

- Yellow wires (LV system channels-TP)
- Blue wires (HV system channels isolation modulus-TP)
- Gray wires (HV service channels)
- Green wires (LV service channels)
- Red wires (5v/24v)
- Black wires (GND and EARTH)

\(^6\) Insulating modulus (active when performing OBP and FCT)
On the other hand, the presser is equipped with:

- Two colorimeters
- Six pneumatic fingers with one electro valve
- Two optical communication devices (provided by the client)
- Presence sensor and anti-rotation sensor

Now, the design process be faced task by task (as it was actually done), deciding on each step, which HW will be necessary to execute the task.

First, the UUTs must be powered on. To do so the needed instruments are:

- One generic **AC generator** (used Elgar cw801cp for stock reasons) for each UUT of the panel (two in total)
- The corresponding relays to sectionalize each UUT. Note that the UUT has a triphasic input, so three relays for each UUT ought to be used (six in total). Due to the nature of the test sequence, in which the different phases must be switched on and off being the AC generators at 230V ac, is recommendable to use **solid state relays** to avoid the stuck problems of the conventional relays. In this case the used relays are MCX240D5 (board
E08REL) that can manage up to 5A at 240V Ac. Even if they are over dimensioned, they can work with a minimum nominal current of 20mA that is within the UUT current consumption specifications. Other reason for which these relays has been chosen is the accessibility and reliability (they have been used in other similar projects with no inconvenient).

Due to the HV nature of the application, some safety measures must be taken into consideration, see section Protection devices.

For the tasks 1 to 3, 5 and 17, a voltage measurement is realized. This is realized using directly the system DVM instrument on all test but the task 2-Output voltage AC generator check.

The task 2, is perform a series of measurements at 230 V, and for this reason the system DVM is not able to measure it directly (voltage out of limits). Hereby, a board consisting on high impedance resistors (to minimize power dissipation) is used to divide the voltage applied on the TPs by 100 (board 2021300). Remember that these TPs are not directly accessible during FCT because are isolated from the system by the isolating modulus previously discussed. Instead, a service channel wired to measuring pin of the mentioned board. In total 6 measures must be realized, three phases and two boards, so six of the eight measurement pints of the board are used leaving two for possible future modifications.

The task 1, is a direct measure of a shunt resistor placed between the AC generator neutral and the UUT GND. This shunt produces a voltage fall on and so alters the board input voltage. However, taking into consideration that the nominal current of the board is 30mA, the shunt resistor (50Ω) is been designed to have a nice measure voltage range (0-0.8 V) allowing a nice resolution and maintaining a negligible voltage drop (0.4%) respect to the input voltage 230V. Its been considered the use of the sense output of the generator to counteract this perturbance but finally is been considered not worth for the risk of appearance of instabilities. The task 1 uses the relays of the E08REL to switch from one phase to another, note that both E08REL coils have been wired in parallel to both UUT this is UFL7-phase A, UFL8-phase A, UFL9-phase C. If one of the UUT is not to be tested the AC generator is to be turned off, otherwise one UUT power supply cannot be managed independently from the other. Additionally, the test protocol document requires to connect two load (20Ω) on two different nets. Given the low value of the load resistors, relays of the FXSEX200 has been used instead of UFLs, reducing the wiring length so increasing the accuracy of the load impedance. Both relays coils in both sites are connected in parallel through a single user flag UFL12, that connect simultaneously the four loads (two for site).

The rest of task do not use the DVM of the system to realize any measurements. Instead, the data acquisition / UUT stimulus is performed by:

- Sending a command or reading a register of the UUT by the optical port (Task 6-16)
- Using the Sensors and actuators on fixture (9-Switch&LED)
- Using external instrumentation, frequency counter (6), VSG (14,16) and Spectrum Analyzer (13,15).
- Using TTL com port (10)

The task 6, Real time clock calibration, is a measure of a frequency output on a net. This frequency ought to be calibrated and for that reason the calibration constant must be sent to the UUT. Two instruments are need the frequency counter and the optical port.
To avoid interferences during the ICT test and the OBP, the frequency counter has been sectionalized. The precision of the measurement must be of the order of µs, thus the signal wire must be shielded. Additionally, to reduce impedance and delays on signal, a relay on the FXSEZ200 is used to reduce the wiring length. The coil of the relay is driven by the UFL19. Note that the signal will have to go through a twisted cable from the TP to the system interface, and then to the IO board (YAPROLL). Finally, thought a shielded wire the signal will be taken to the frequency counter input.

On the other hand, the optical communication is realized from the UUT top, so the communication device is placed on the presser. From there, the signal will descend via top-bottom interface and will cross the fixture to arrive to the FXSEZ200, where the signal is multiplexed with the TTL-RS232 transceiver (task 10). The normally close signal is connected to the optical port while the normally open signal is connected to the transceiver. The common output of the relay is connected to the PC through the IO board (YAPROLL). The signal multiplexing is requested due to retro-compatibility of the system with other adapter applications, where the wire of the IO board does not predispose a second PC com slot. The five relay coils of the FXSEZ200 used to perform this commutation are commanded by the UFL16

The task 10, UART communication, has been modified during the debug phase, when is been noticed that the communication protocol of the board was inverted TTL rather than RS232. So, a transceiver (TTL-RS232) along with a “NAND” logic port (shorted inputs) have been added to the initial fixture design (APPENDIX A: Electrical scheme-15). This HW can be enabled (disabling the optical port) by closing the UFL16

The task 7 simply uses the optical port to read a register value switching the different phases as done in the task 1, “consumption measurements”.

The task 8 request a specific stimulus and then a register value is read from the UUT. The UUT has three internal resistors of known value (6.4 Ω). The stimulus requested by the board test protocol determines that is to be applied three sinusoidal signals of noticeable different values to the three resistors terminals. The applicable voltage range is from 0 to 200 mV. However, the system driver can only generate a single sine wave form from 0 to 10V 100mA maximum. To face this limitation, some partition resistors has been added to the initial project design. The first version (Fig. 40 Voltage dividers for build-in intensity measurement IC) was based on a low impedance partition resistors and a very low stimulus from the driver’s waveform generator. During debug this solution proved to be not applicable because the contact resistors of the probes were comparable to the partition resistors, and thus altering the measure and making it unstable. To find a right solution a sensitivity analysis is performed.

\[
\begin{align*}
(1) \quad V_o &= \frac{R_{\text{UUT}} \cdot V_{\text{in}}}{R_c + R_p + R_{\text{UUT}}} ; \\
(2) \quad \frac{\partial V_o}{\partial R_c} &= \frac{-R_{\text{UUT}} \cdot V_{\text{in}}}{(R_c + R_p + R_{\text{UUT}})^2}
\end{align*}
\]
The aim is to minimize (2) to minimize the contact resistance sensitivity. The easiest way is increasing the partition resistors value \( (R_p) \). Note that the contact resistance is near to 3Ω, but it can vary each time that the presser goes down and from UUT to UUT. It can also increase because of probe tip dust and wear.

The task 9-a, that test the switches 1 to 3, is characterized for the use of the pneumatic fingers. These pneumatic fingers are commanded by an electro valve placed on the presser. The UFL that commands the EV (UFL15) has been placed between GND and the negative pin of the EV valve command. This helps to prevent the relay to stuck.

The task 9-b, that test the LED color and light intensity, is characterized for the use of a colorimeter. This colorimeter transduces light to frequency, so it is necessary to measure this frequency. As this measure does not need a high accuracy, the system counter is used instead of the external counter.

The task 11 is a reading from a register through the optical port, no additional hardware is needed.

The tasks 12 to 14, are managed entirely with the hardware previously described and additionally with the RF instruments. These instruments are directly connected to the PC and placed on the vicinities of the test area. No additional HW is needed to perform these tasks.

There are two strips (GND and 5V) where the FPS1 of the system has been wired. All HW in the fixture that needs to be feed is at 5v except the excitation of the electro valve coil that is at 24V, supplied directly from the FPS4 of the system.

**OBP**

To do the OBP is very important to prevent the effects of the noise. For this reason, some measures have been applied. The programmer has been placed as near as possible to the programming TPs. As can be seen on Fig. 38 Fixture internal HW, blocks the J-Link Out Strip is placed very near to the test area. All the programing signals are twisted together with a GND wire that is soldered right next to the TP, on the GND plane. The wires have been sectioned with a the FXBUF100 board, that incorporates four low impedance relays, this way is possible to avoid that
the channels act as antennas. Note that the programmers have to be connected to the PC in order to send the programming data. This connection is done through the YAPROLL. The J-Link connection is USB based. For this reason, the power supply is expected to arrive few milliseconds before the Rx-Tx signals. Otherwise, the HW can enter in error mode, and cause troubles. To resolve this matter, a customized board has been added. It is a board with four relays, but its commands depend on the arrival time of the power supply. More specifically, the board delays the GND and 5v signals relays 2 seconds and the Tx-Rx signals relays 2.2 seconds, thus simulating the effect of the conventional use of a USB (plugging USB).

**Protection devices**

As this fixture works with HV some safety measures ought to be taken.

**Passive discharge. Discharge capacities with normally connected discharge resistors**

In this application, in the UUT, there are capacitors with high capacitive value and high voltage (of the order of 200uF 230V). These capacitors during the functional tests are loaded with high voltages, thus accumulating large amounts of energy. To prevent the operator from coming into contact with the capacitors still charged with energy. These components must be discharged. It is therefore necessary to connect the discharge resistors to the capacitor terminals by means of normally closed relays. These resistors must be appropriately sized both from a resistive point of view, to allow the capacitors to discharge in good times, and from the point of view of power, inserting appropriate dissipators if necessary (not in this case). As a sectioning relay with normally closed contact, is available on "FXDSC100". It is also important to monitor the voltage across capacitors to make sure it is actually discharged. This measurement can be made using voltage dividers inside the board. See APPENDIX A: Electrical schemefor the detailed electrical schematics.

Additionally, with in this board is present a safety chain that if connected in series with both sites and the AC generator BRU (security unit used to cut off the power supply in case)

**Test Point Power. Power point for reference UUT to ground with relay contact N.C.**

For safety reasons, during the execution of a high voltage functional test, the mass of the UUT must be connected to the ground of the machine. We therefore need to "sacrifice" a mass test point for this purpose. This test point, which we will call "TP POWER", will not be connected to any machine channel and will be connected to earth via a relay with normally closed contact (APPENDIX A: Electrical scheme-2). The Board “FXSEZ110 " has been used for this purpose.

The reason why the "TP POWER" is not connected to a system channel is to protect the system from over-currents to earth and prevent this channel from being always when using the pin finder.

**Fuse and Led signaling Power on**

To protect the voltage generator and the UUT, a fuse is introduced in series to the power supply. This fuse must be appropriately sized taking into account both the voltage and current that the generator will have to deliver during the test. In this case it will be 30mA with 230V, so a fuse of 500mA has been chosen (mistaken on the Appendix A).

As a good practice, it’s been inserted a LED lamp to evidence the presence of high voltage. See APPENDIX A: Electrical scheme-4&5
Sizing section of wires

The UUT nets where it is necessary to apply high voltages and high currents, must be contacted with appropriate probes and these test points must be wired with appropriately sized cables. A nail 100 mils sword carries up to 500mA, while a nail 100 mils 4 tips or 9 tips can manage up to 3A. In this case the current will not exceed 120mA so 100mils probes were used to contact the supply TPs of the board.

It is also necessary to correctly size the wire section (1 mm$^2$ leads 3A) and evaluate the insulation of the covering, of the wire itself, according to the tension. In our case the voltage is less than 400Vdc, and therefore, either the normal solder wire or the "W.W. AWG24 blue iso. 600V ".

Switching from the wires / cables to the fixture

Evaluating the path of high voltage wiring inside the fixture avoids the creation of various problems in the debugging phase. High voltage involves the creation of important magnetic fields that can compromise the operation of digital testing. In order to avoid these problems, the following countermeasures has been implemented:

- The high voltage wiring has been moved apart from the wiring involved in the digital tests
- Phase and neutral have been twisted together making sure that the magnetic field is cancelled or attenuated
- A ground plane has been inserted but not around the power test points, in order to avoid unpleasant short circuits due to the creation of voltage arcs.
Relays overview tables

Here all the used relays have been written to clarify how many boards were need and how many system relays (UFL) and fixture relays (E08REL & FXSEZ200) remained free.
4. Results

The adapter performance can be determined by four parameters:

- **Stability**: Over a single UUT the adapter is intended to measure always the same values for each component. The level of dispersion on this measure can stand within a threshold but if this threshold is surpassed the test is considered unstable. To test the stability of the adapter, a Test Repeatability Analysis (TRA) is performed. It consists on testing the same board a high number of times and then analyze the measure dispersion on each test (cp, cpk).

- **Repeatability & Reproducibility**: The adapter is intended to work correctly on all the UUTs being operated with any operator performing the test in any conditions (if performed correctly). Ideally the UUT are identical one to another but in practice these variations occur, even if both UUT are functional, and it affect the measure. Other reason that can alter the measure, is the way the board is inserted on the conveyor or how fast the UUTs arrive. On operative conditions this would depend on the previous system in the production line, but during the analysis this is simulated by using different operators (manually inserted). This factor is measured by the Gauge Repeatability and Reproducibility test (GR&R). It consists on testing a certain number of UUTs a certain number of times. This must be done following a certain sequence where no UUT is tested two times consecutively.

- **Coverage**: Not analyzed here because is subject of NDA

- **Test time**

For reasons of time no TRA and GR&R have been realized over the FCT and OBP test steps. Instead a debug has been performed where the basic functionality has been tested but not its stability.

- **Test Repeatability Analysis**

After all the debug and adjustments of the different measurements a reference UUT is chosen. This UUT is probed to be functional and all the tested components are compliant to the specification. The mission of this board, if the adapter becomes unstable for any reason, is to have a reference to recalibrate it.

Over this board a TRA analysis has been done. The number of repetitions chosen was 25 (time restrains). The number of UUT that will be tested in production will be much higher and for this reason 25 times might be not enough. Nevertheless, it helps to predict which test could return a false Fail.

The complete analysis will not be shown on this document given its extension. However, the instabilities that have been detected will be listed and analyzed.

The analysis consists on storing the 25 measures realized for each test and then calculate the value mean, maximum, minimum and process capability indexes ($C_p$, $C_{pk}$). Then a limit values are chosen for the $C_p$ and $C_{pk}$ indexes in order to classify each test into:

- **Good**: the test is stable and is not expected to return a false fail result.
- Acceptable: the test is stable but under some circumstances it could return a false fail result.
- Critical: The test can return a false fail in normal operation. To be calibrated or disabled.

The overall summary of the TRA analysis is shown on the image below. On the right is possible to see a pie graph where the different tests are classified by its stability. At the right there is a graph that shows the $C_p$ and $C_{pk}$ values over the various tests. Possible to appreciate a zone of higher instability. This zone corresponds to the capacitors tests.

When measuring capacitors, the measure can be easily influenced by many factors, even if the stray capacitance is subtracted from the result a higher instability is expected for small capacitors. An example can be found on the Fig. 42, where the value changes up to a 50% depending on the site of the panel of boards. This could be due to the different routing and length of the cables on the adapter, when the capacitor is very small, a little variation on the testing conditions can alter the measurements.

When increasing the value of the capacitor, this effect can still cause distortions but, as the capacitor is bigger, the measurement deviation is reduced in proportion to the measured value (Fig. 43).
In conclusion, the tests are stable in general, but a tuning of the capacitor tests will have to be done during the adapter installation on the target ATE system at the production plant. The corrective action would be:

- Force an offset of site 2 respect 1 on tests that are similar to the one shown in Fig. 42.
- Tune the frequency used on the capacitor tests with a high \( C_P \) to improve the measure stability.

As seen on Fig. 41 the rest of the test are very stable except for the last test that corresponds to the sink test. Because of its nature (board consumption), this test can return a high variety of values depending on the charging condition of the board or if it is programed or not.

### Gauge Repeatability and Reproducibility

The test has been conducted by one operator with three different panels of two UUTs tested each one of them ten times. The panels have been tested one after another to check the R&R of the adapter.

<table>
<thead>
<tr>
<th>Tested Panels</th>
<th>Tested UUT</th>
<th>Tests per UUT</th>
<th>Total tested UUT</th>
<th>Operator</th>
<th>Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 (P1,P2,P3)</td>
<td>6</td>
<td>10</td>
<td>60</td>
<td>D.Cabrera</td>
<td>(P1&gt;P2&gt;P3)x10</td>
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</table>

As the TRA, the complete analysis cannot be shown in this document due to its dimensions. The most characteristic test will be mentioned.

Coming back to the same capacitor analyzed on the previous section, with the GR&R is possible to verify the repeatability of the measurement and not only its stability. The graph below shows the ten series of measurements over the six UUT. Is possible to appreciate that the different series (different color lines) are very close. This means that no matter how or who does the test, the
measure will be very similar. The offset between site 1 and 2 detected during the TRA, can be appreciated here as well. The even UUTs are in the site 2 and the odd UUT are in the site 1. The UUT tested in the site one shows a measure value of around 105pF while on the site 2 it is around 85pF.

An example that shows higher instability would be the resistor R1 (Fig. 44). Now is possible to appreciate the different measurement series. On the UUT 1 the measure less stable and change more over the different trials that the other boards. On the contrary the UUT 5 and 6 seem to be more stable. To reach a conclusion a GR&R with more samples would have to be done, however it seems that the panel one (UUT 1 and 2) behaves different from the other two panels.
In general, the GR&R is favorable, thus is possible to ensure that:

- The amount of variation due to the adapter is low compared with the variation due to UUT variation
- The adapter’s capability to discriminate between different panels

Due to limited resources just one operator has realized the analysis and for this reason the repeatability is not ensured. In other words, the amount of variation of the measure that is due to operator influence has not been verified.

- Test time

The average test time is 3:32 minutes. Divided by test step it is:

- ICT: 37.3 seconds
- OBP: 35.4 seconds
- FCT: 140 seconds

The test time is within the client requirements. However, its performance could be improved by reducing the needed time for the FCT test. This could be performed by improving the optical communication speed and by changing test protocol for the most expensive tasks.

A detailed analysis of each individual test time is to be done. This would help to detect how to improve the overall test time by addressing to the most time expensive tests.
5. Bibliography


6. APPENDIX A: Electrical scheme

The electrical diagram of the fixture is divided into the following parts:

1. Title cover page
2. Mass wiring (Richiuse di massa)
3. Service signals
4. Power Supply UUT 1
5. Power Supply UUT 2
6. OBP wiring UUT 1 (Cablaggi OBP Figure 1)
7. OBP wiring UUT 2 (Cablaggi OBP Figure 2)
8. Load Connections
9. Passive Discharge and Safety chain
10. Voltage divider resistors wiring (Partionres)
11. Led sensor and its top-bottom interface wiring
12. Electro-valve and its top-bottom interface wiring
   PC COM multiplexing.
14. Counter wiring
15. RS232-TTL transceiver wiring (Cablaggi RS232)
Power Supply Fig 1

Note: Wire AWG 24 High Voltage Grigio

Command parallel for Fig.1 and Fig.2

ENABLE RELAYS EL08REL

Tipologia di No
A  AWG 26 ROSSOWW
B  AWG 26 NERO WW
C  AWG 36 VERDE WW
D  AWG 26 BIANCODW
R  AWG24 NERO HV WW
S  AWG24 GRIGIO HV
T  AWG24 BLUHV
Power Supply Fig 2

Note: Connesse a nastro (Earth) tramite shunt in pagina 9

ENABLE RELAYS EL08REL

Command parallel for Fig.1 and Fig.2

Typologia di filo

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<thead>
<tr>
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<th>Description</th>
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</tr>
<tr>
<td>B</td>
<td>AWG26 NERO WW</td>
</tr>
<tr>
<td>C</td>
<td>AWG26 VERDE WW</td>
</tr>
<tr>
<td>D</td>
<td>AWG26 BIANCO WW</td>
</tr>
<tr>
<td>R</td>
<td>AWG24 NERO NV NV</td>
</tr>
<tr>
<td>S</td>
<td>AWG24 GRIGIO HV</td>
</tr>
<tr>
<td>T</td>
<td>AWG24 BLU HV</td>
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</tbody>
</table>

Sheet description: Alimentazioni HV Figura 2
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Drawing type: ELECTRICAL DIAGRAM

FILE NAME: [Redacted]

APPO: Crespi A.
Cablaggi OBP Figure 2

Tolleggi filo

A  AWG 26 ROSSO W/W
B  AWG 26 NERO W/W
C  AWG 26 VERDE W/W
D  AWG 26 VERDE W/W
R  AWG 26 NERO+V+W

Note: se indicato usare AWG26 Verde.
Figura 1

Figura 2

Note: SKV GND Strip is equipotential to system EARTH

Safety chain

<table>
<thead>
<tr>
<th>Topologia del Relé</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
<tr>
<td>B</td>
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<tr>
<td>C</td>
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<td>D</td>
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</tbody>
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Fixture sensor
7. APPENDIX B: Case of study Test sequence flow chart

1. Top level flow chart. Managed by the organizer
2. ICT flow chart
3. FCT general view flow chart


8. APPENDIX C: LabVIEW

This appendix contents all the material referring to LabVIEW block diagrams that are too large to add into the document.

The present block diagrams are:

1. Main block diagram: test sequence ordering and final management.
2. Consumption measurements
3. UUT programming OBP
4. Real time clock
5. Power Supply measurement by optical command
6. Current read by optical command, build-in intensity measurement IC test.
7. UART communication
8. LTE TX
9. LTE RX
Test performed.

AC generator setting for each test.

Power on.

Safety power in case of overcurrent.

Shunt resistor measurement site 1

Shunt resistor measurement site 2

Daniel Cabrera Fernández